Compal Confidential

ICW50 Schematics Document

AMD Turion/Sempron + Nvidia MCP67-MV

2007 / 04 / 20 Rev:1.0 FOR Pre-MP

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

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Title: Cover Sheet

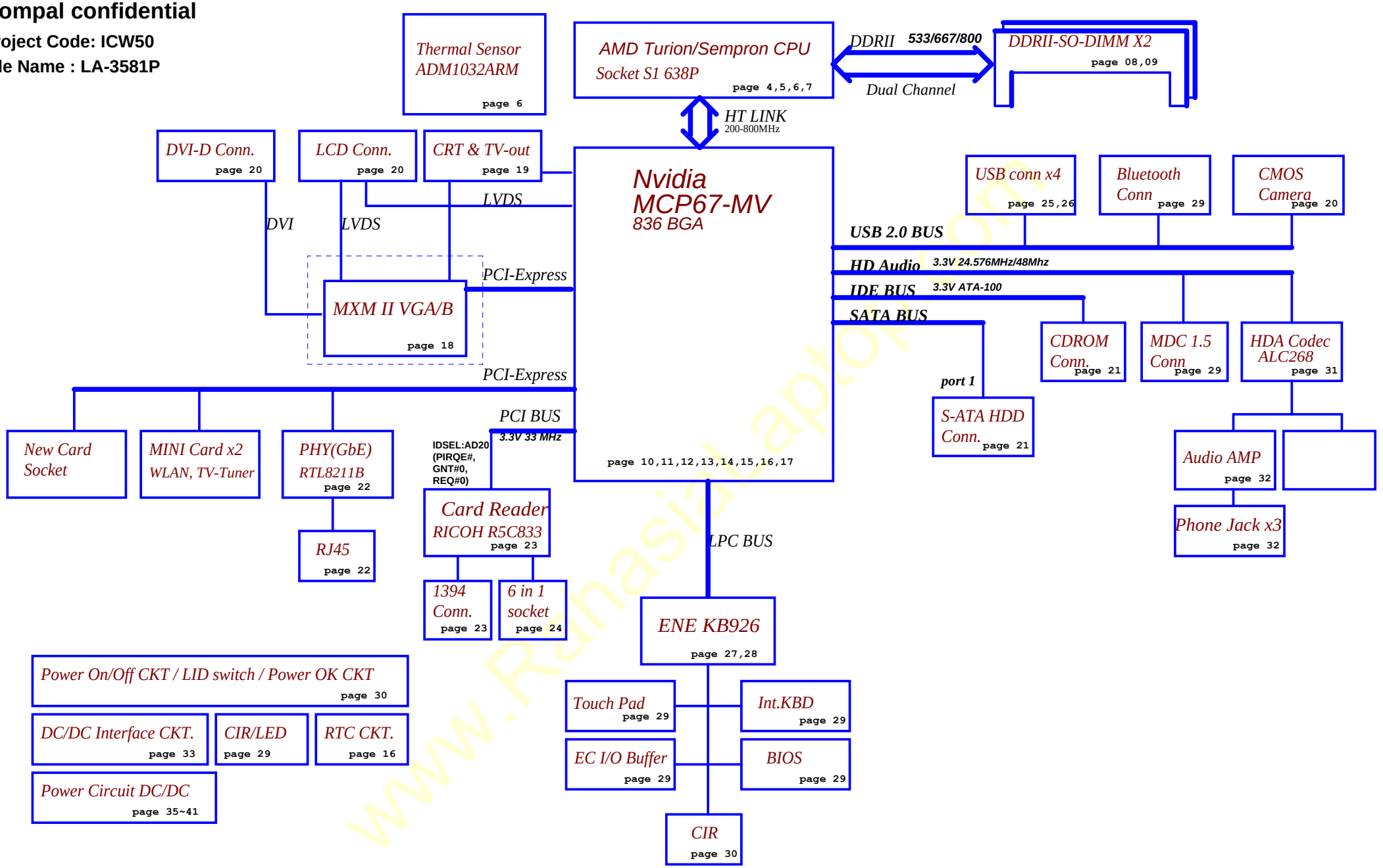
Size: Custom | Document Number: ICW50 / ICY70 LA-3581P | Rev: 1.0

Date: Friday, April 20, 2007 | Sheet 1 of 42

Compal confidential

Project Code: ICW50

File Name : LA-3581P



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Issued Date	2006/08/18	Deciphered Date	2007/8/18

Title	BLOCK DIAGRAM		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 2 of 42		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.2VALW	1.2V always on power rail	ON	ON	ON*
+1.2VS	1.2V switched power rail	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW/+3V/+3VAUX	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD20	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

MCP67 SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 001Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	UMA (0V)
1	DISCRETE (3.3V)
2	
3	
4	
5	
6	
7	

SKU ID Table

SKU ID	SKU
0	B - PHASE
1	C - PHASE
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIP CAP & RTC	45@
UMA	UMA@
VGA	VGA@
UMA & TV-OUT	UMA&TV@
2 SATA HDD	SATA2@
CAMERA	CMOS@
BLUETOOTH	BT@
MINI CARD 1(TV)	MINI1@
MINI CARD 2(WLAN)	MINI2@
NEW CARD	EXPRESS@
TV-OUT	TV@
DVI	DVI@
1394	1394@
CARD READER	5IN1@
HT Debug Port	HT@

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

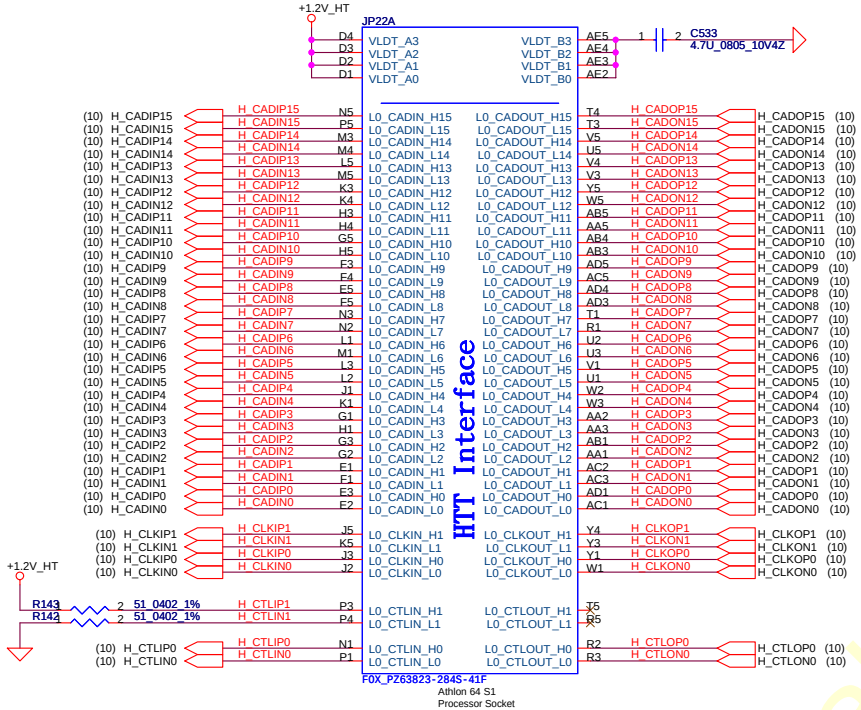
Title: TABLE OF CONTENTS

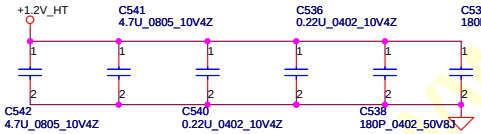
Size	Document Number	Rev
Custom	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 Sheet 3 of 42

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

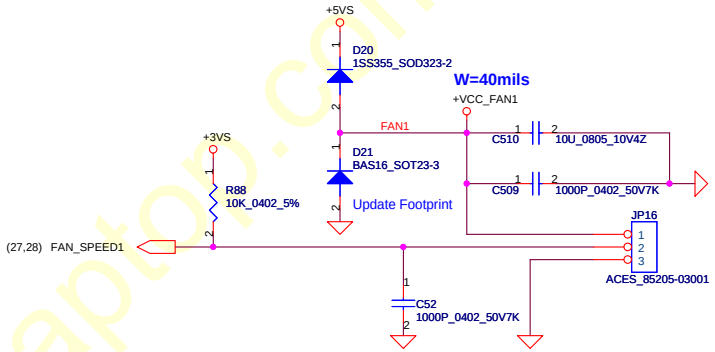


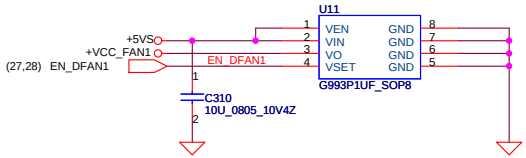


LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

FAN Conn





FAN1 Conn

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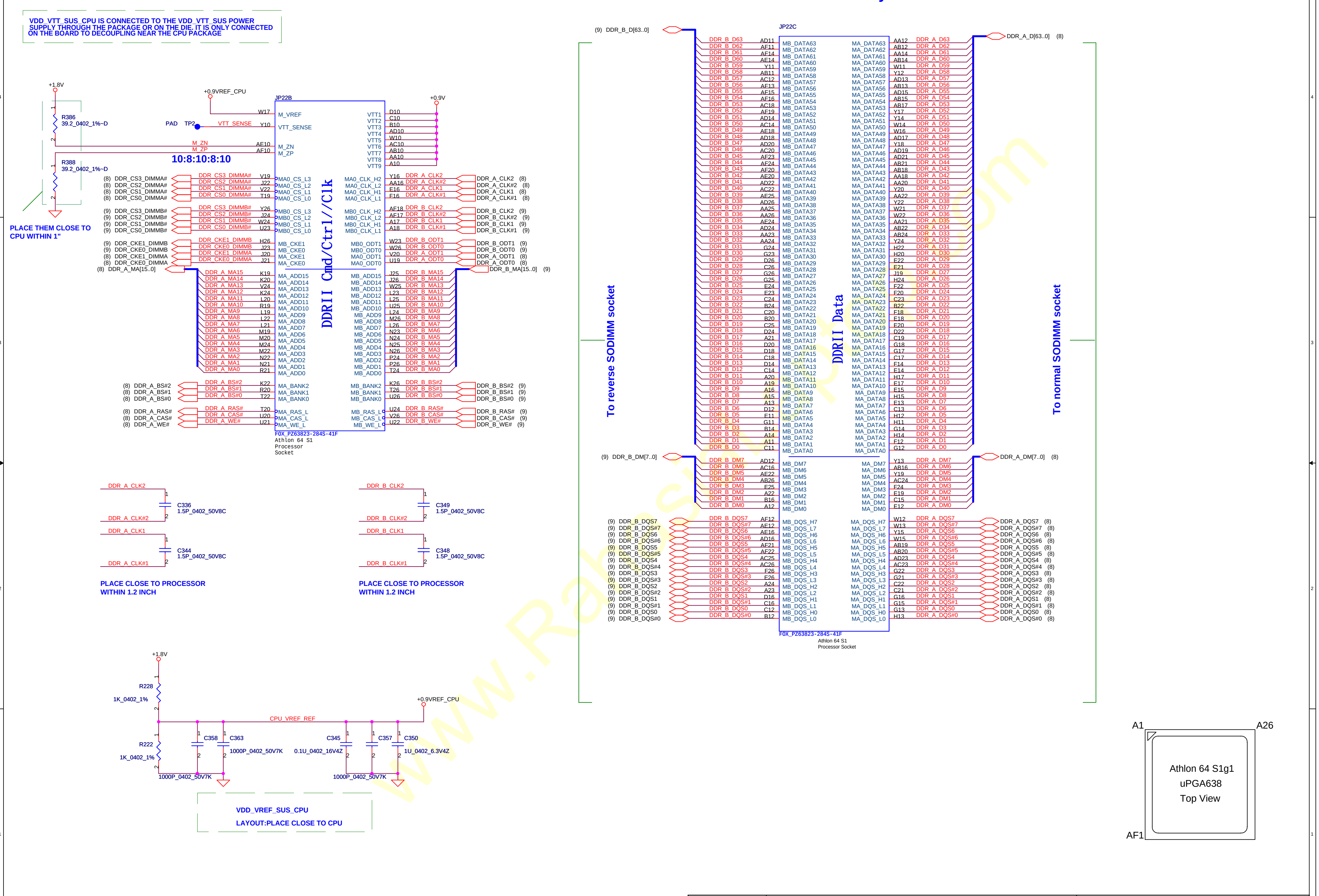
Title	AMD CPU HT I/F		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 4 of 42		

Processor DDR2 Memory Interface



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Title: AMD CPU DDRII MEMORY I/F

Size: Custom | Document Number: ICW50 / ICY70 LA-3581P | Rev: 1.0

Date: Friday, April 20, 2007 |

ATHLON Control and Debug

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

W=50mils

place them to CPU within 1"

5:10

5:5:5

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

10:10

MISC

JP22D

F0X_PZ63823-284S-41F

AMD NPT S1 SOCKET
Processor Socket

HDT Connector

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

SAMTEC_ASP-68200-07

PVT Modify 2007/03/22

Connect to MCP67

U2 CLOSE CPU,
CPU_THERMDA&CPU_THERMDC PLACE
CLOSE TO PROCESSOR WITHIN 1" INCH

ADM1032ARM_RM8

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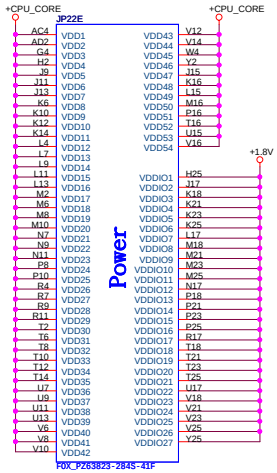
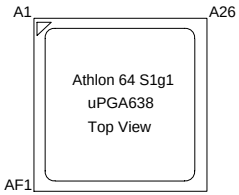
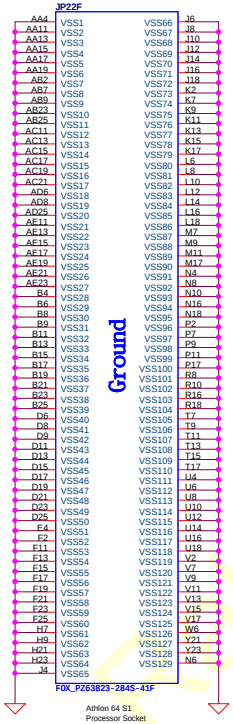
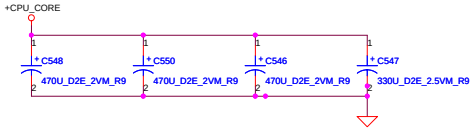
Title	AMD CPU CTRL & DEBUG		
Size	Document Number		Rev
C	ICW50 / ICY70 LA-3581P		1.0
Date:	Friday, April 20, 2007	Sheet	6 of 42

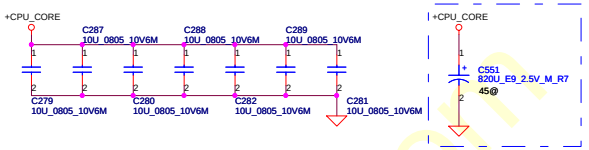
PROCESSOR POWER AND GROUND



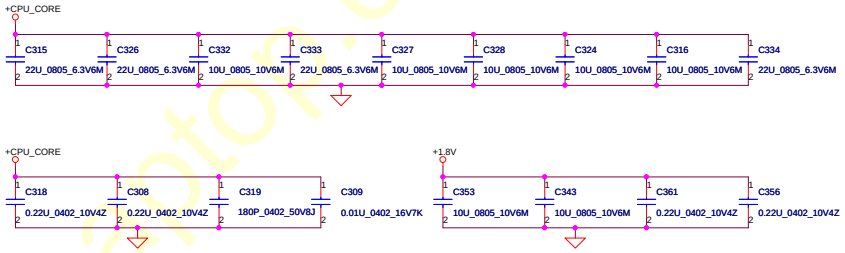




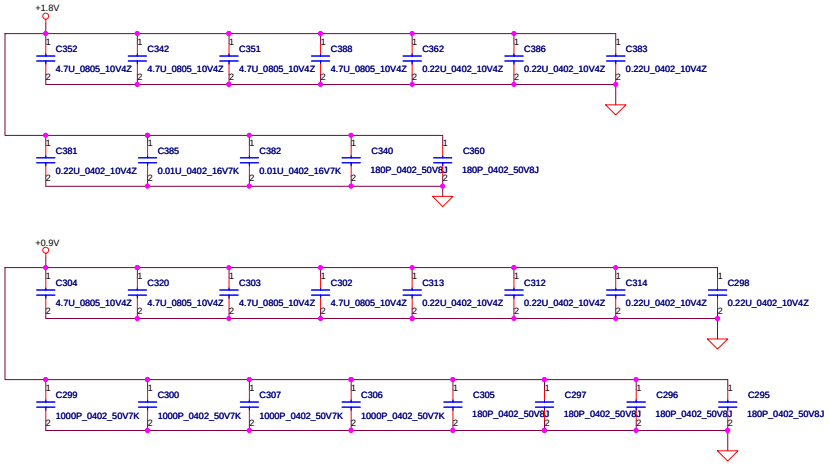




CPU SOCKET S1 DECOUPLING



DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



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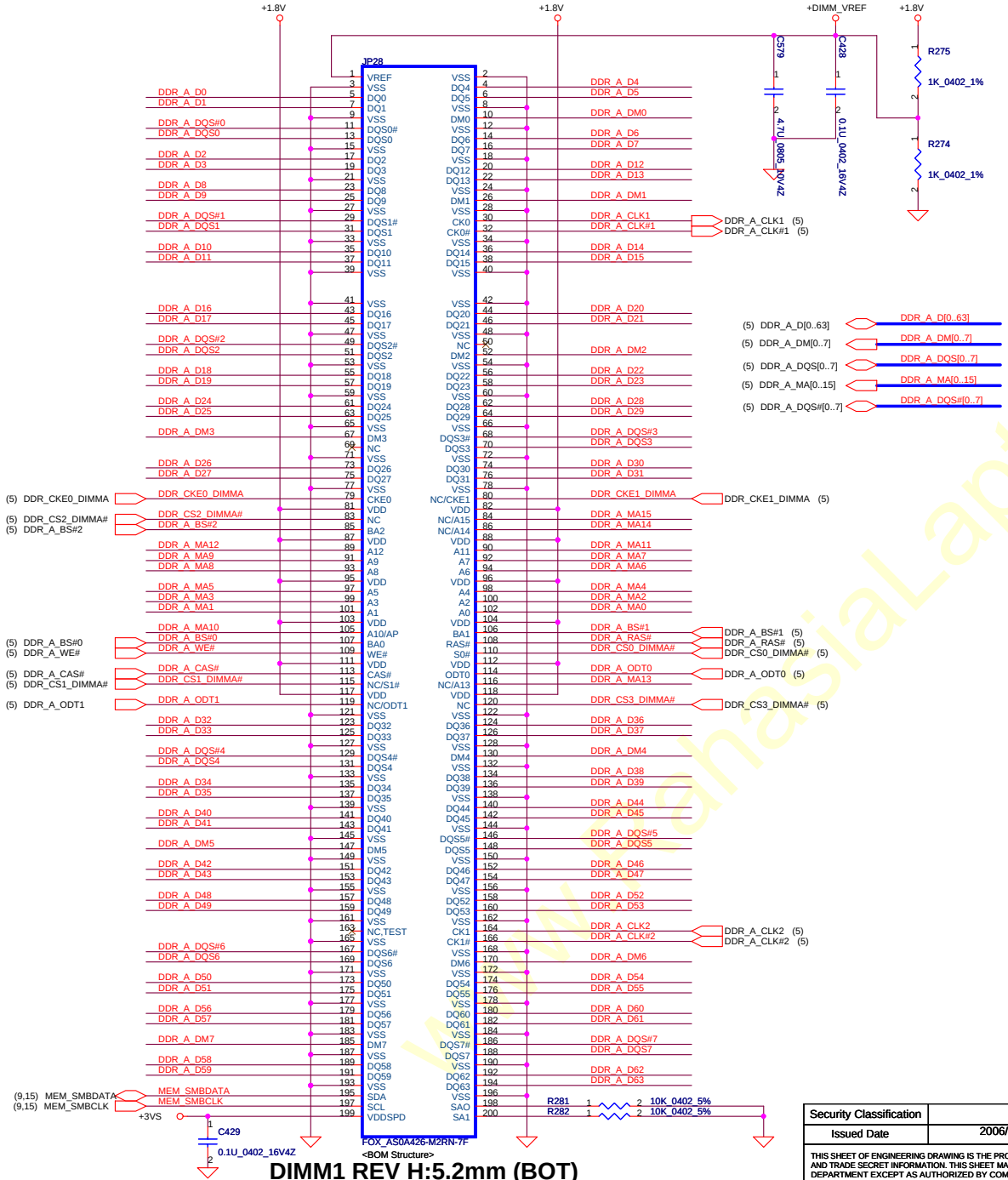
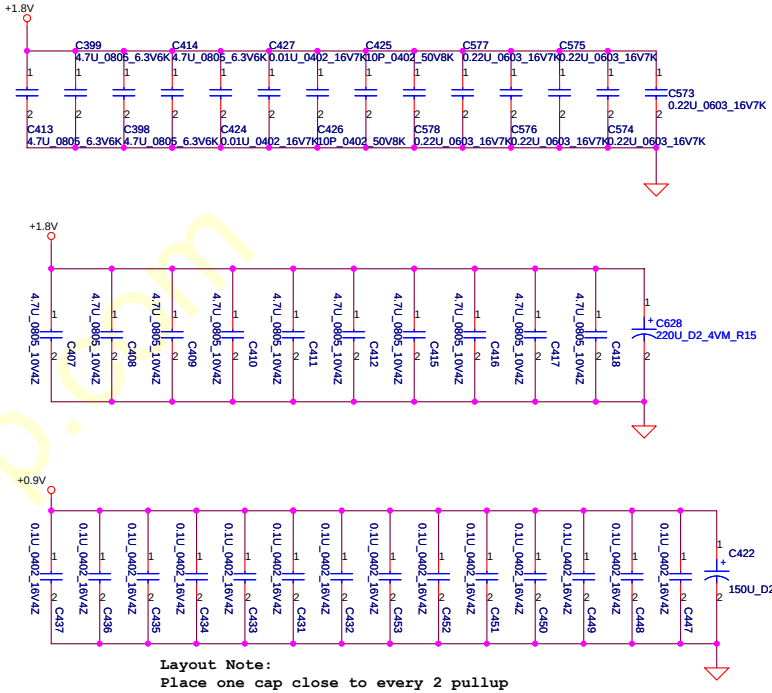
Issued Date	2006/08/18	Deciphered Date	2007/8/18

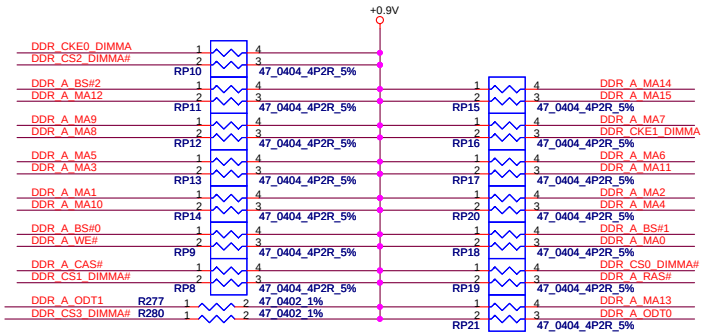
Title	AMD CPU PWR & GND	
Size: C	Document Number: ICW50 / ICY70 LA-3581P	Rev: 1.0
Date: Friday, April 20, 2007	Sheet 7 of 42	

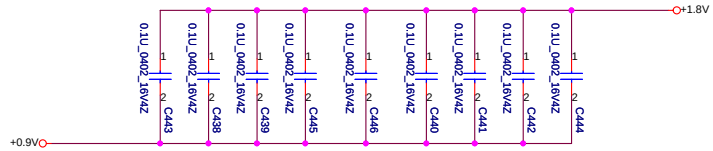


DIMM1 REV H:5.2mm (BOT)



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

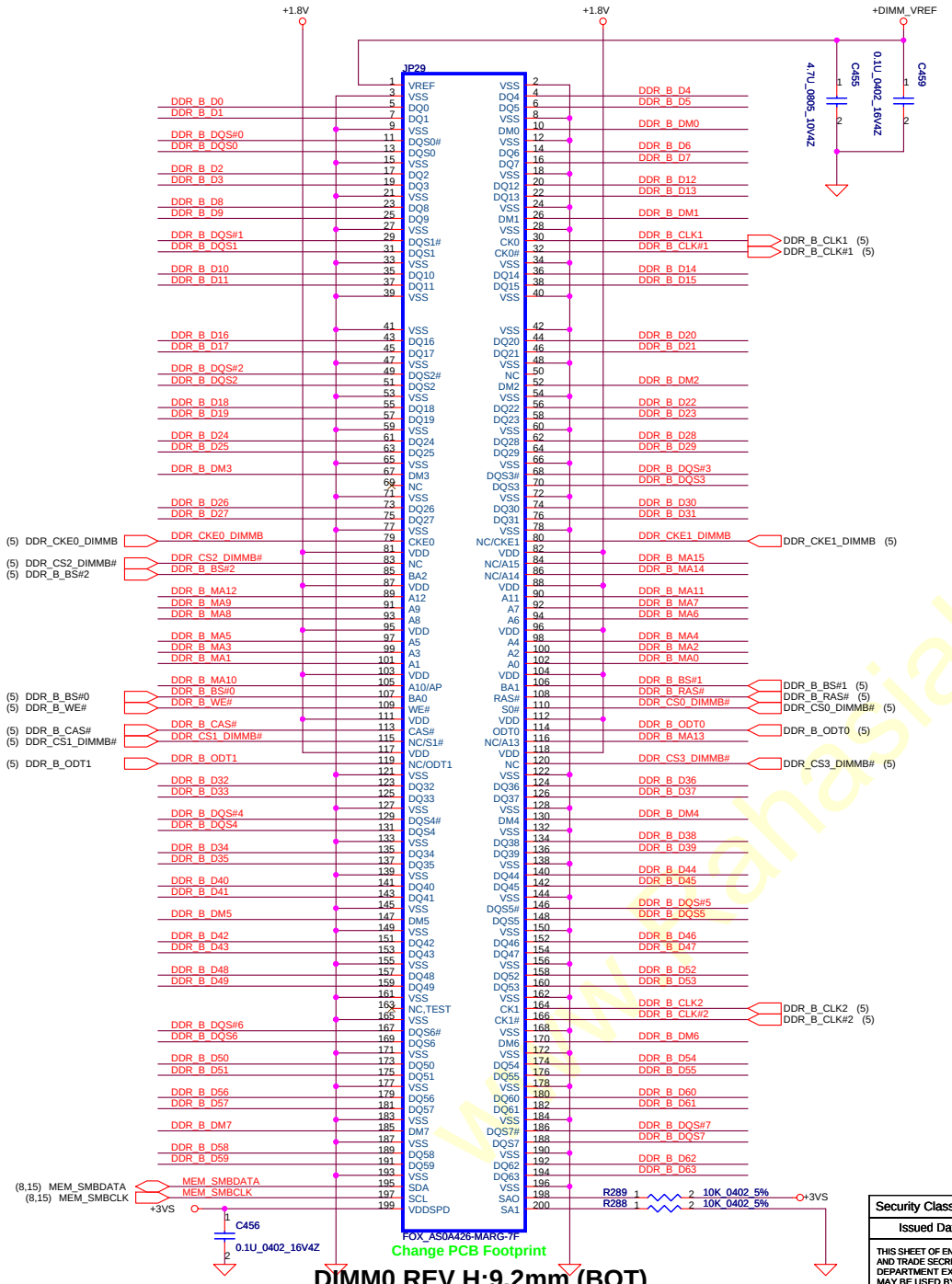




Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Title	DDR2 SO-DIMM I		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 8 of 42		



(5) DDR_B_D[0..63] → DDR_B_D[0..63]
(5) DDR_B_DM[0..7] → DDR_B_DM[0..7]
(5) DDR_B_DQS[0..7] → DDR_B_DQS[0..7]
(5) DDR_B_MA[0..15] → DDR_B_MA[0..15]
(5) DDR_B_DQS#[0..7] → DDR_B_DQS#[0..7]

+1.8V
C654 1000P_0402_50V7K
C656 1000P_0402_50V7K
C653 1000P_0402_50V7K
C655 1000P_0402_50V7K

+1.8V
4.7U_0805_10V4Z: C625, C624, C623, C622, C627, C626, C632, C633, C630, C631
+ C629 220U_D2_4VM_R15

+0.9V
0.1U_0402_16V4Z: C483, C482, C481, C480, C479, C478, C466, C464, C465, C463, C462, C461

Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V

+0.9V
DDR_CS2_DIMMB# DDR_CKE0_DIMMB → RP22 47_0404_4P2R_5%
DDR_B_MA12 DDR_B_BS#2 → RP23 47_0404_4P2R_5%
DDR_B_MA8 DDR_B_MA9 → RP24 47_0404_4P2R_5%
DDR_B_MA3 DDR_B_MA5 → RP25 47_0404_4P2R_5%
DDR_B_MA10 DDR_B_MA1 → RP26 47_0404_4P2R_5%
DDR_B_WE# DDR_B_BS#0 → RP27 47_0404_4P2R_5%
DDR_CS0_DIMMB# DDR_B_RAS# → RP29 47_0404_4P2R_5%
DDR_B_ODT1 DDR_CS3_DIMMB# → R286 47_0402_1%, R287 47_0402_1%
RP30: DDR_CKE1_DIMMB, DDR_B_MA15
RP31: DDR_B_MA14, DDR_B_MA11
RP32: DDR_B_MA7, DDR_B_MA6
RP33: DDR_B_MA4, DDR_B_MA2
RP34: DDR_B_MA0, DDR_B_BS#1
RP28: DDR_B_CAS#, DDR_CS1_DIMMB#
DDR_B_ODT0, DDR_B_MA13
RP35: 47_0404_4P2R_5%

+1.8V
0.1U_0402_16V4Z: C476, C472, C471, C470, C469, C457, C458, C477, C486, C485, C484
+0.9V

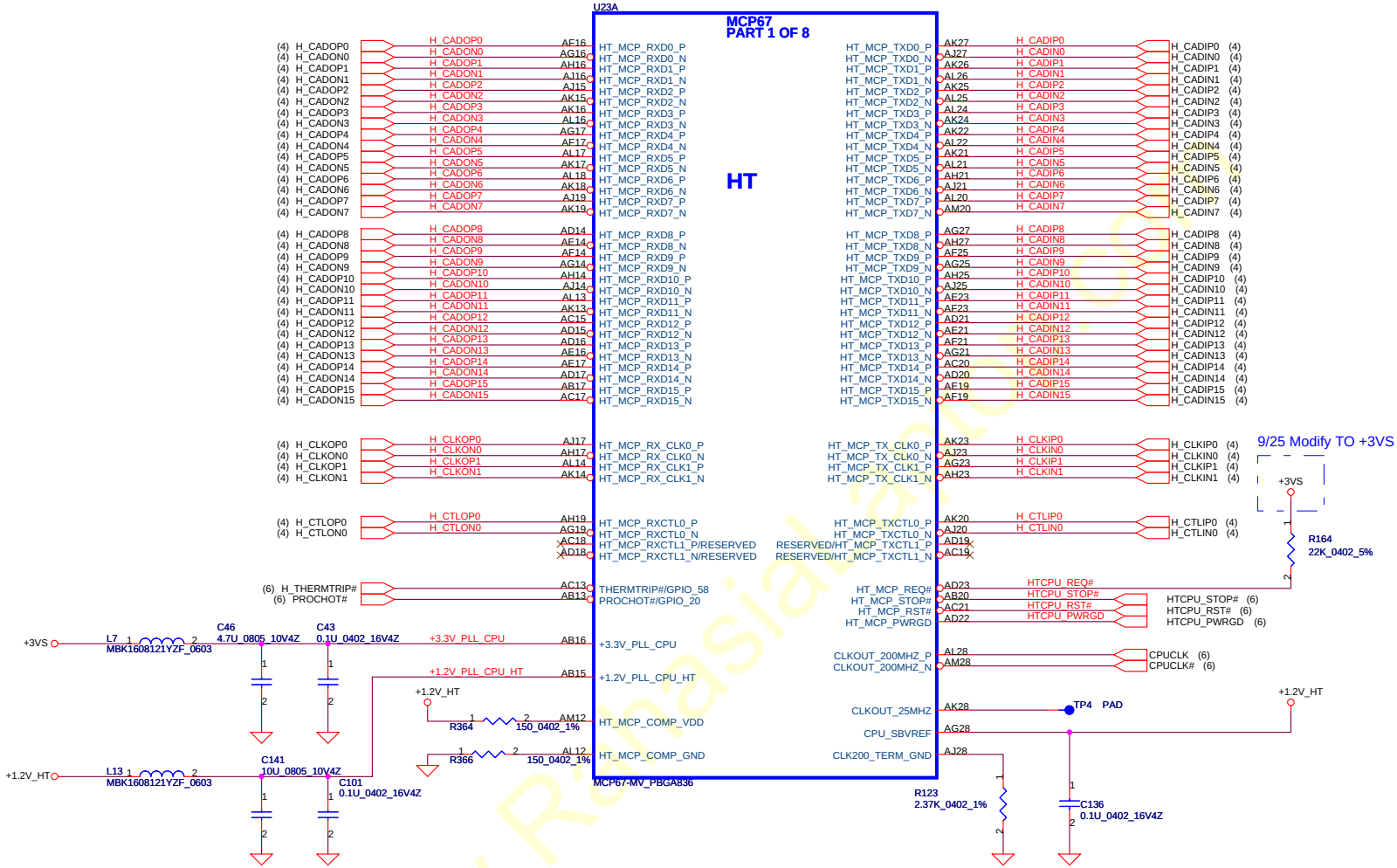
Layout Note:
Place one 0.1uF cap close to every 2 pullup resistors terminated to +0.9V

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Title: DDR2 SO-DIMM II

Size	Document Number	Rev
Custom	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 Sheet 9 of 42



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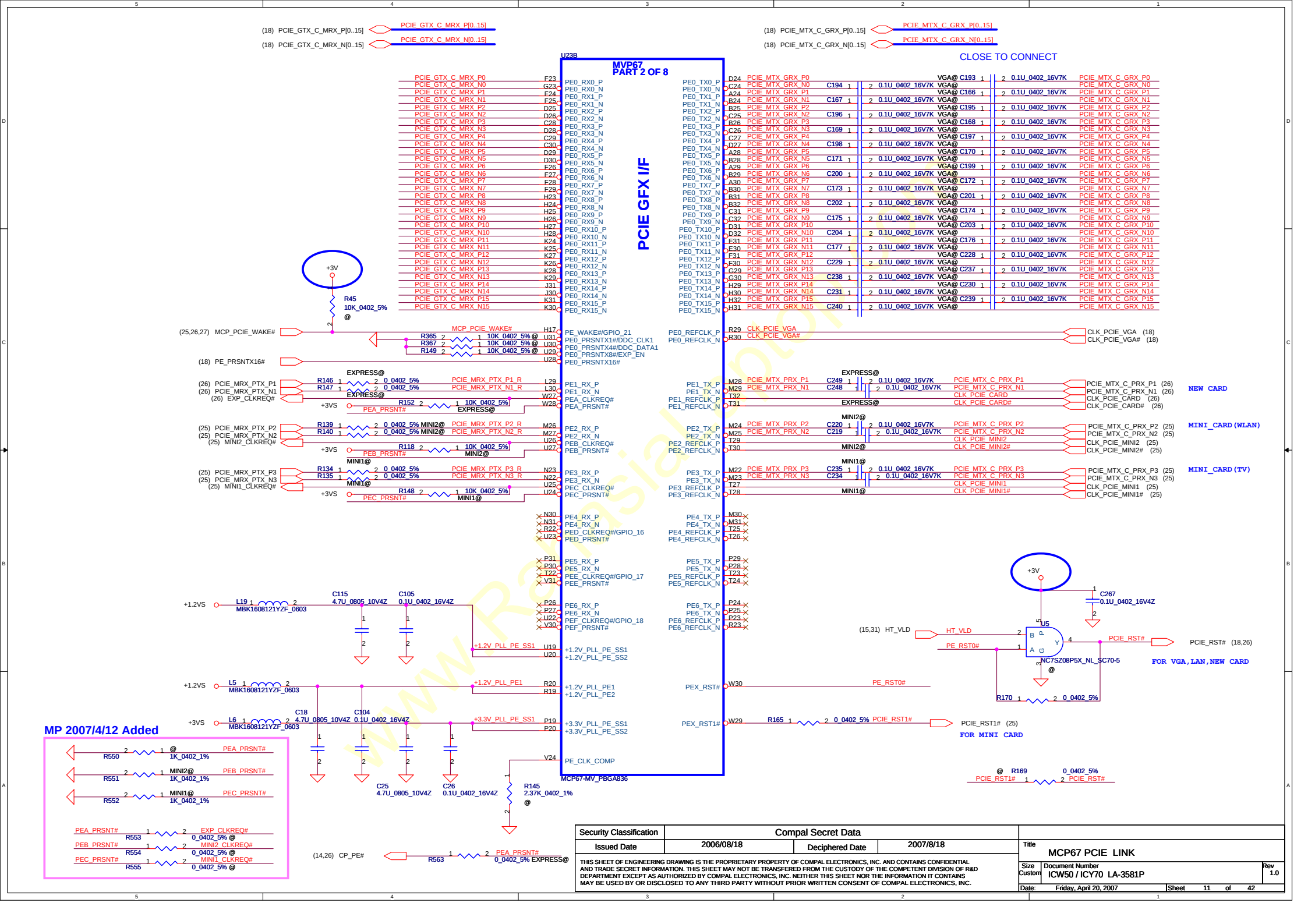
Title	MCP67 HT LINK		
Size	Document Number		Rev
Custom	ICW50 / ICY70 LA-3581P		1.0
Date:	Friday, April 20, 2007	Sheet 10 of 42	



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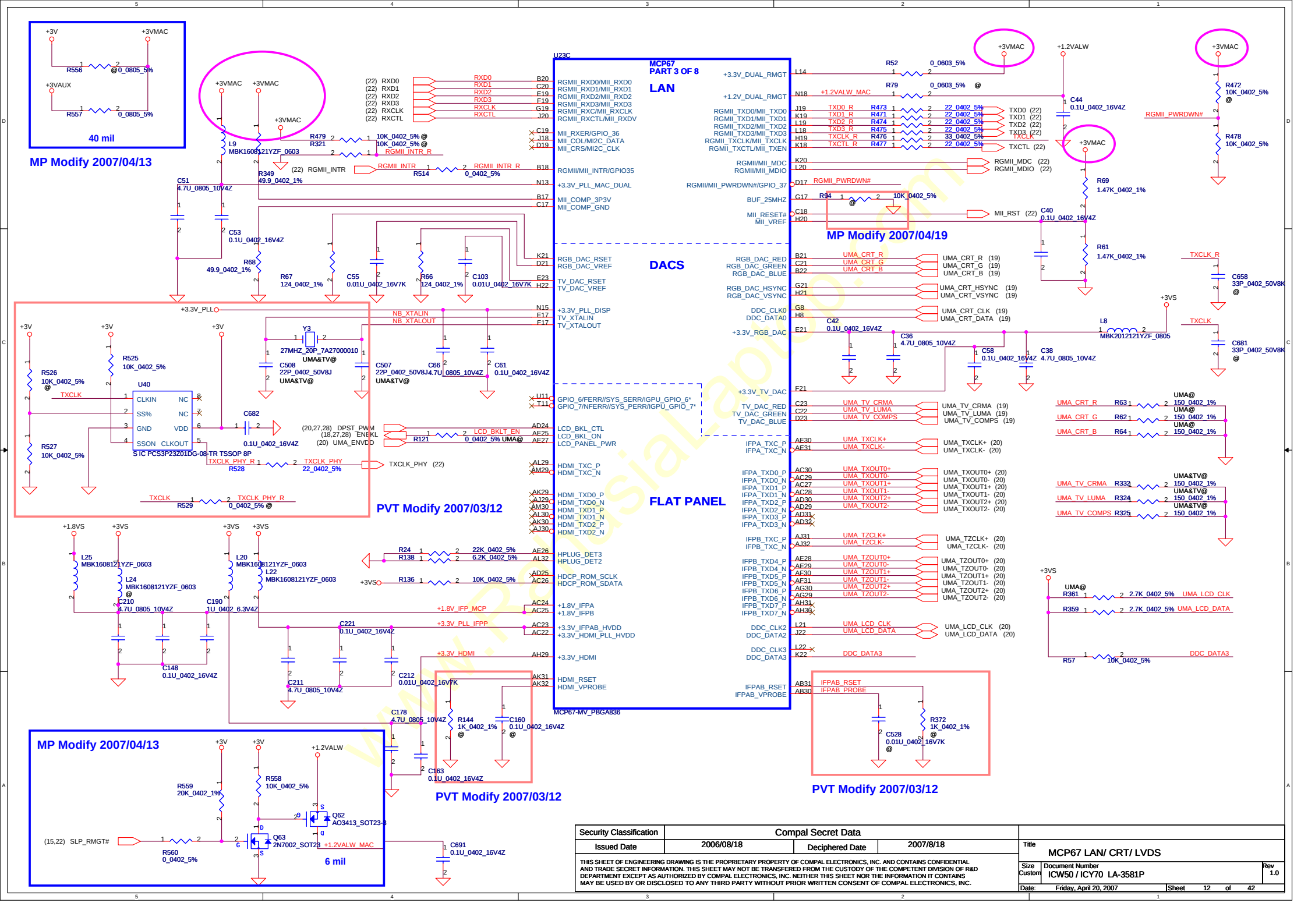
Title	MCP67 PCIE LINK		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 11 of 42		


MP Modify 2007/04/13
40 mil
U23C
MCP67
PART 3 OF 8
LAN
DACS
FLAT PANEL
MCP67-MV_PBGA836
MP Modify 2007/04/19
PVT Modify 2007/03/12
PVT Modify 2007/03/12
MP Modify 2007/04/13
6 mil
PVT Modify 2007/03/12
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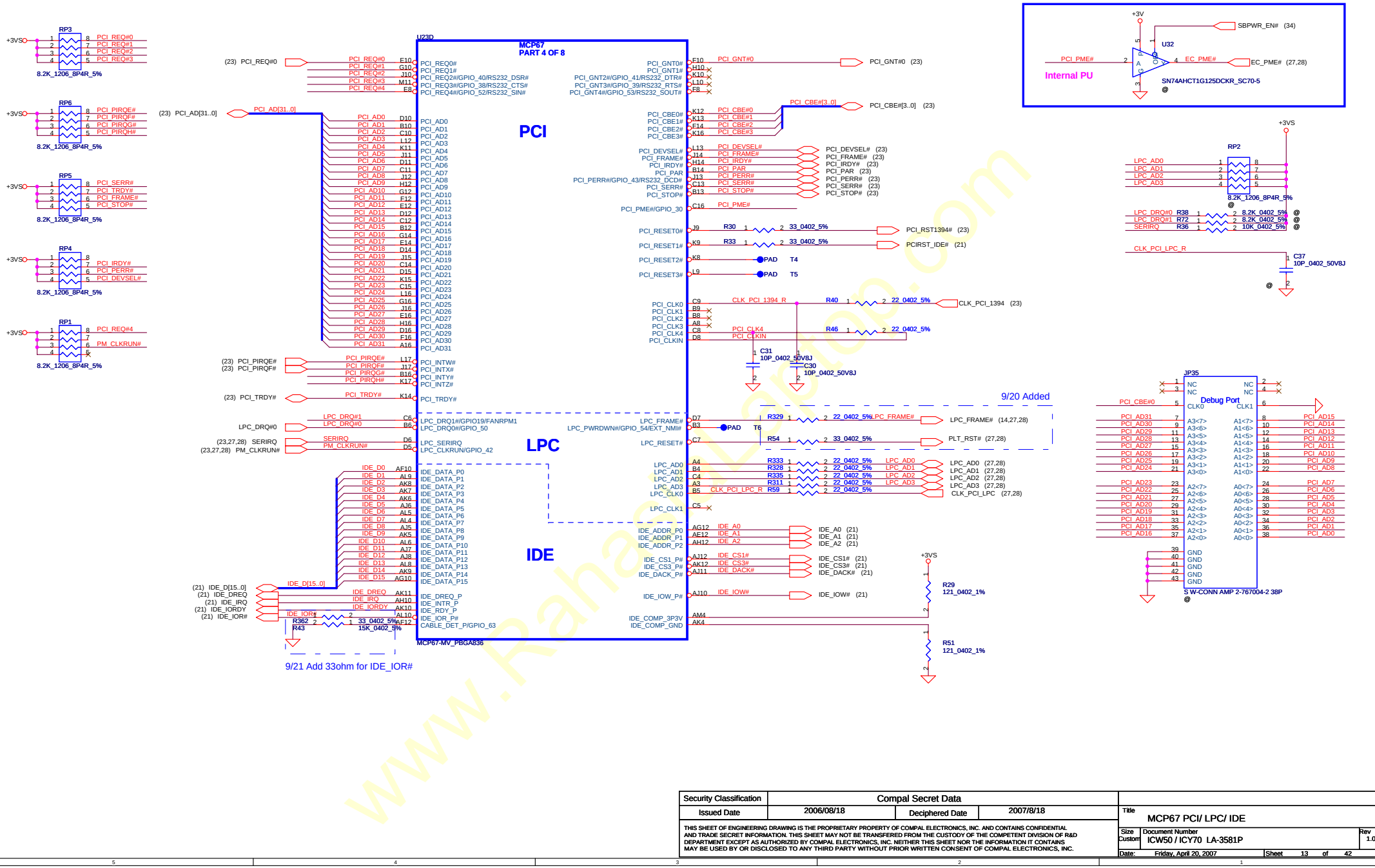
Size
Custom
Document Number
ICW50 / ICY70 LA-3581P
Rev
1.0
Date:
Friday, April 20, 2007
Sheet
12
of
42



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Title	MCP67 PCI/ LPC/ IDE		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 13 of 42		

PLACE SATA AC COUPLING
CAPS CLOSE TO MCP67

U23E
MCP67
PAR 5 OF 8
MCP67-MV_PBGA836

SATA

USB

HDA

JUMPER		
HDA_SDOUT	LPC_FRAME	FUNCTION
"0"	"0"	LPC BIOS*
"0"	"1"	PCI BIOS
"1"	"0"	SPI BIOS
"1"	"1"	RESERVED

*DEFAULT

U36
ASM3P623S00CF-08TR_TSSOP8

USB PORT_1
USB PORT_1
USB/B Connector
USB/B Connector
USB CAMERA
BLUETOOTH
MINI1
MINI2
NEW CARD
NON-USE

Security Classification	Compal Secret Data		
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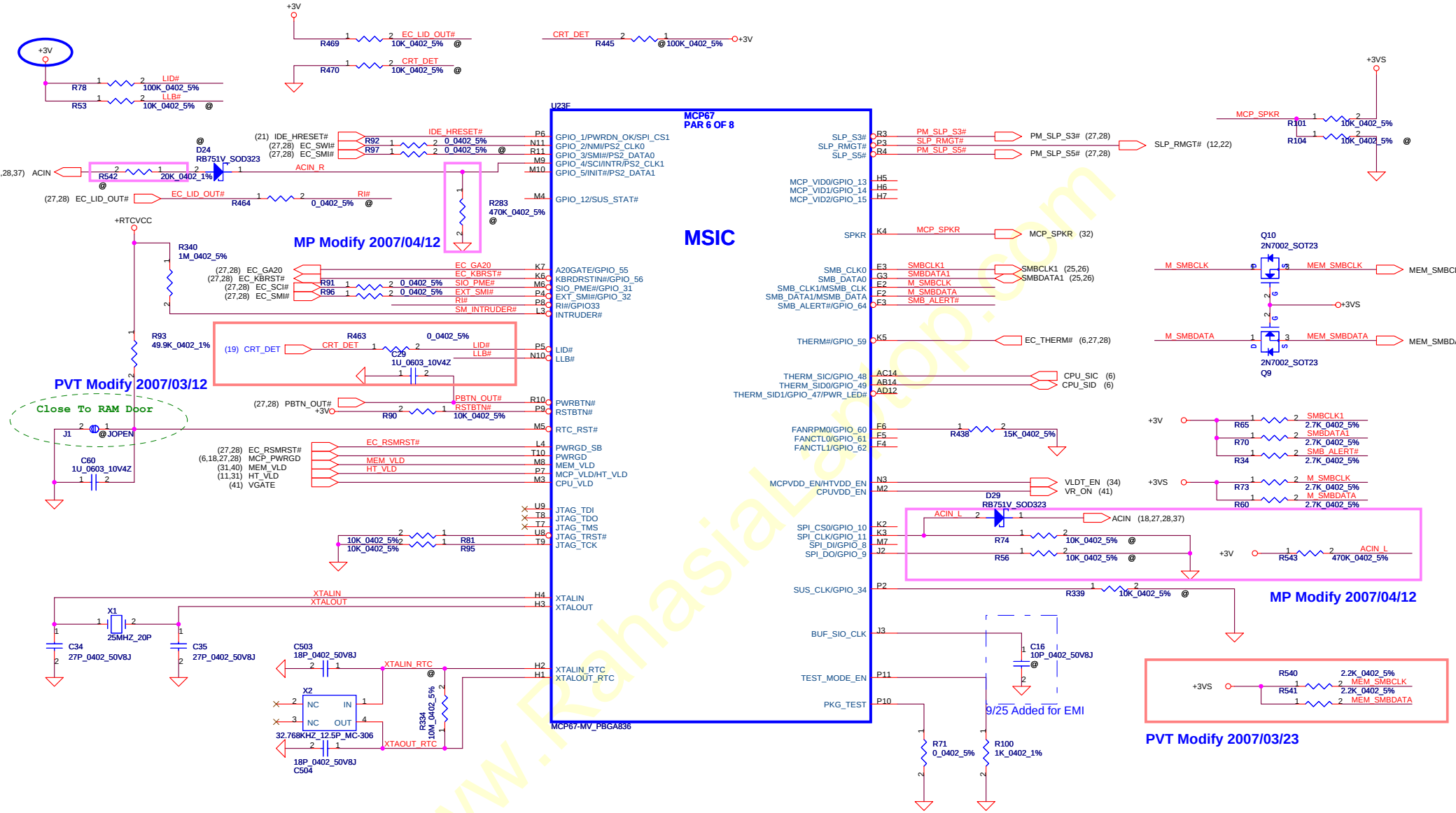
Title	MCP67 SATA/ USB/ HDAUDIO		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 14 of 42		



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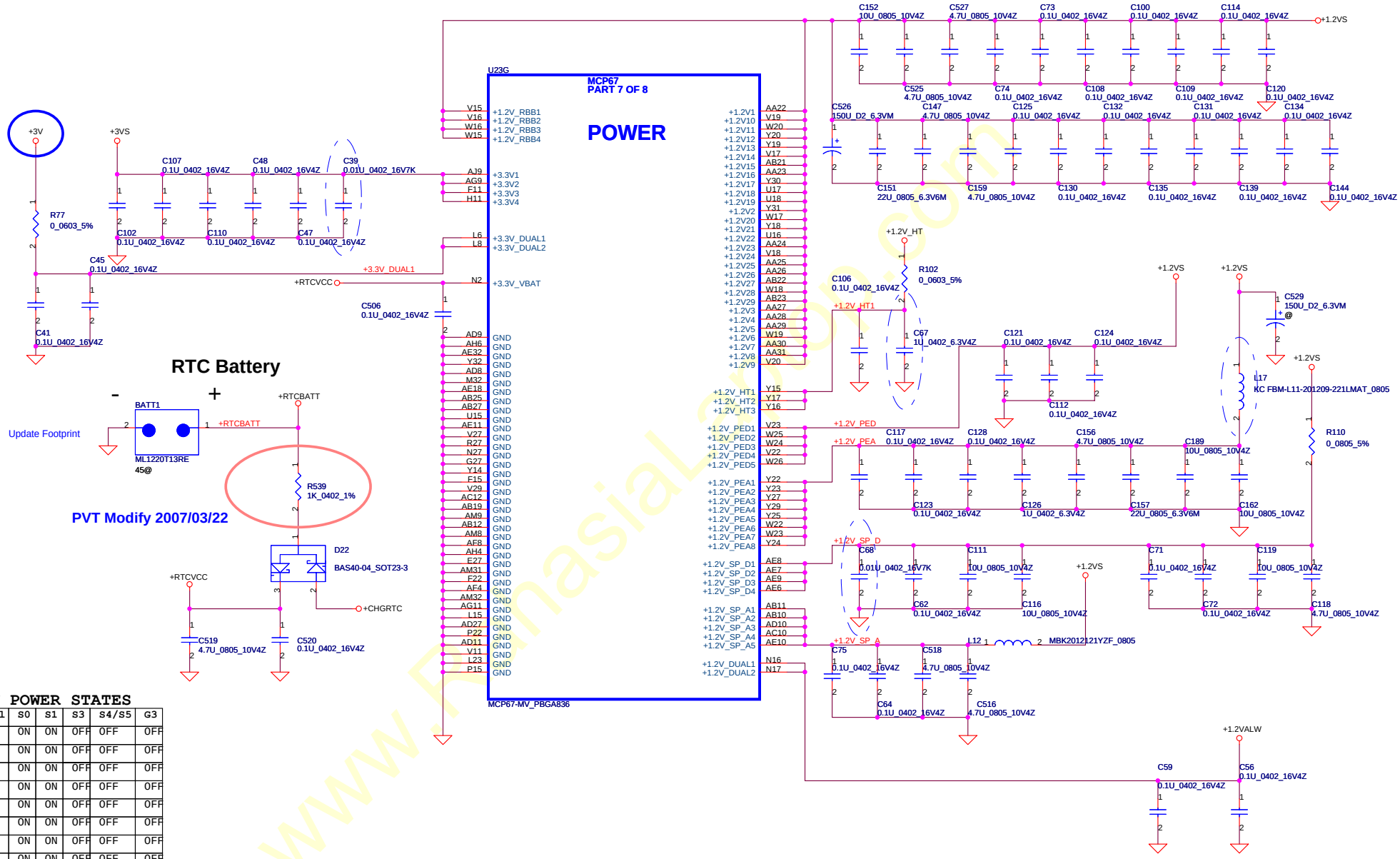
Title	MCP67 MISC		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 15 of 42		



MCP67-MV POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF
	ON	ON	OFF	OFF	OFF

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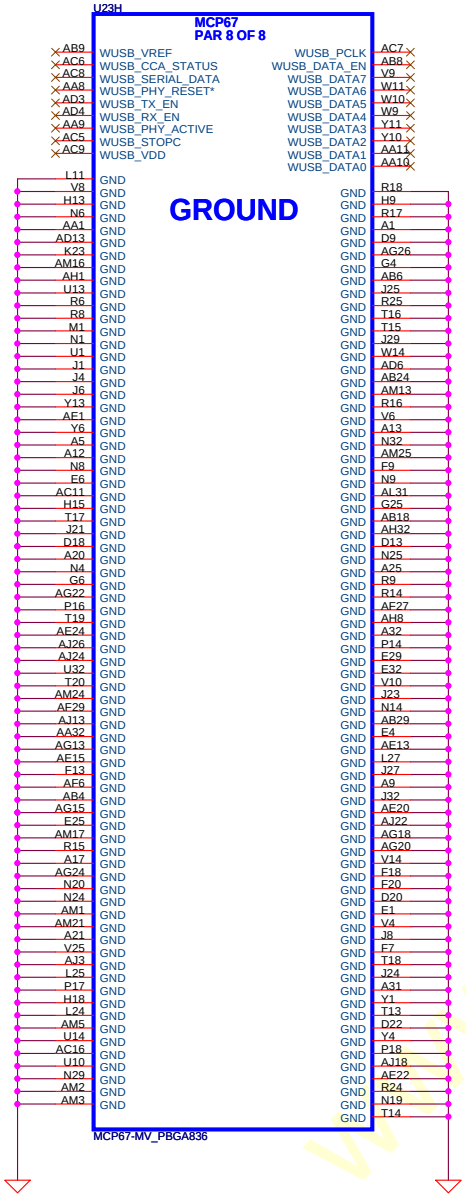
Title	MCP67 POWER		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 16 of 42		



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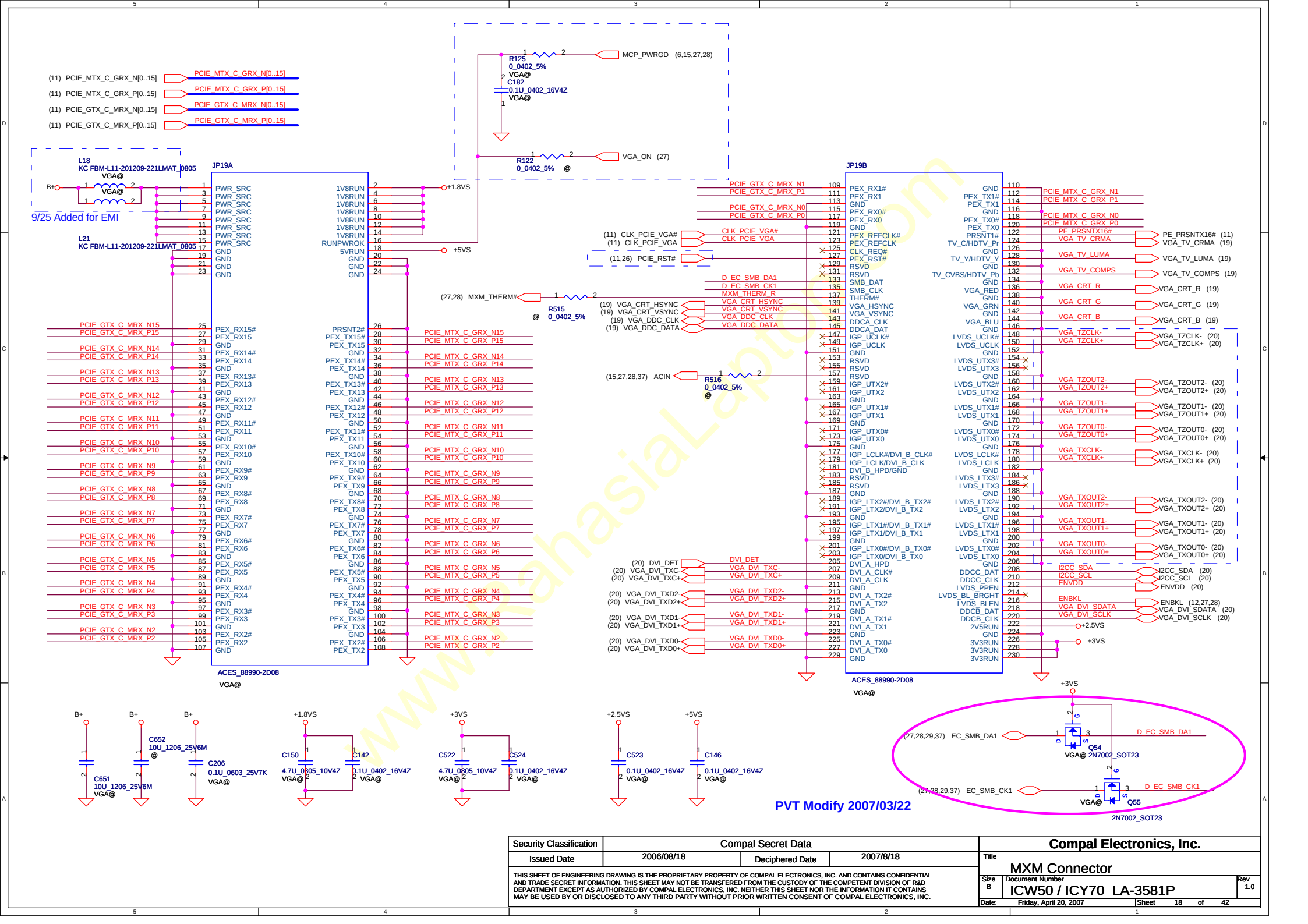
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: MCP67 GROUND

Size	Document Number	Rev
Custom	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 Sheet 17 of 42



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

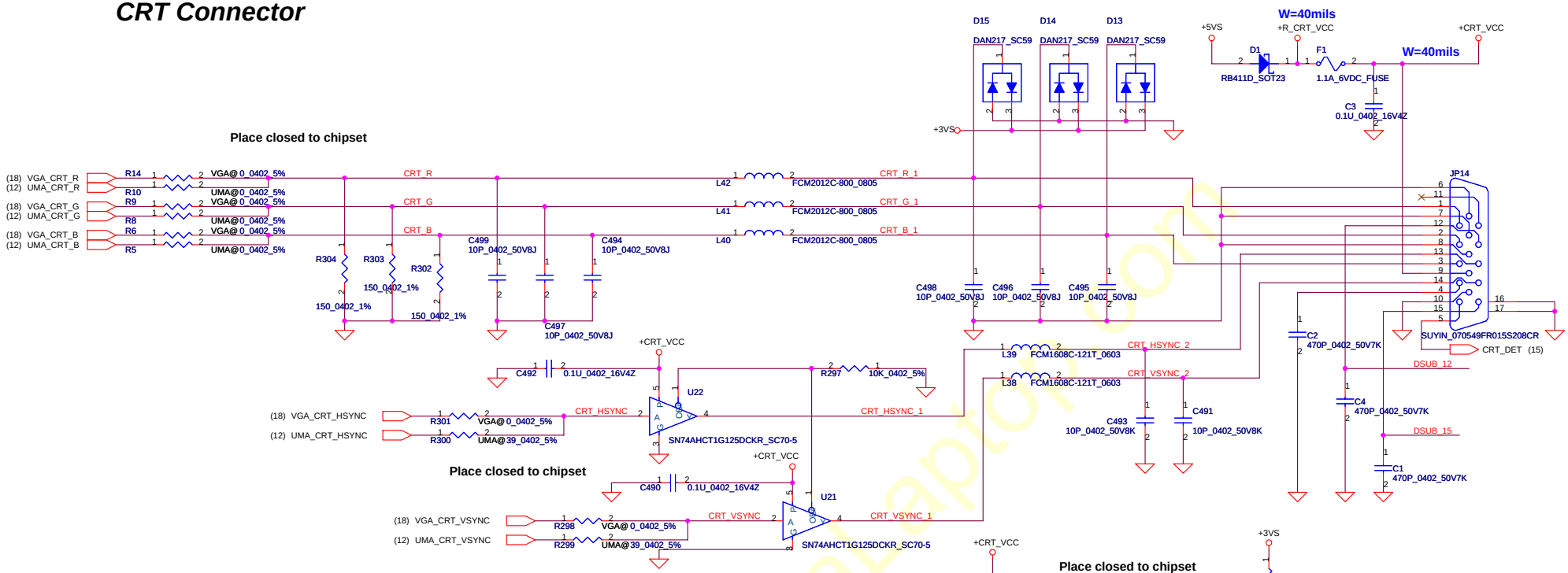
Compal Electronics, Inc.

Title: MXM Connector

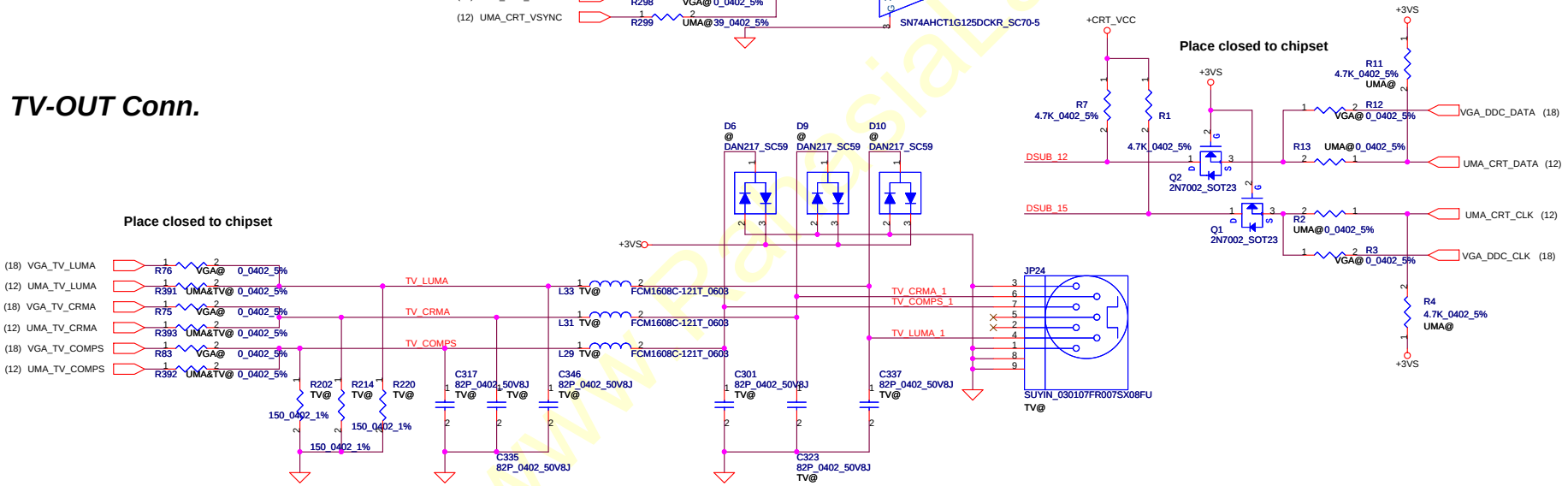
Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 | Sheet 18 of 42

CRT Connector



TV-OUT Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

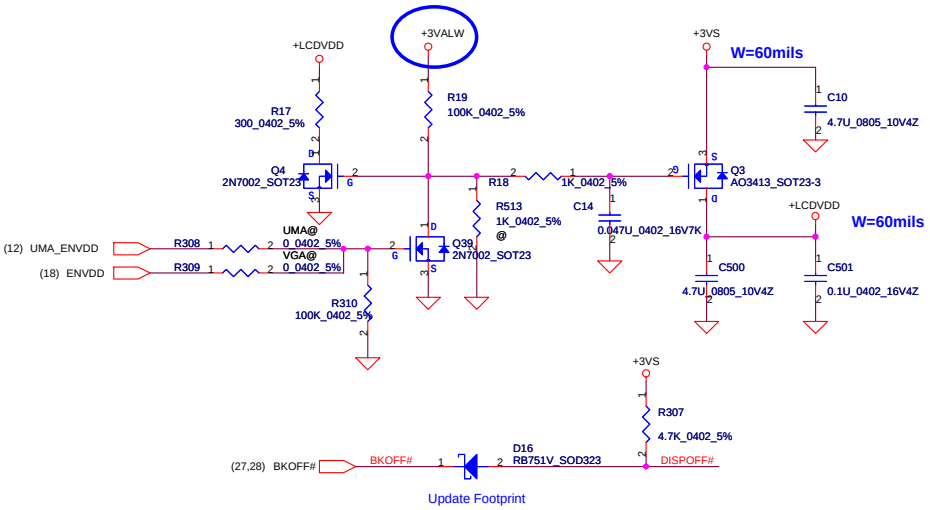
Compal Electronics, Inc.

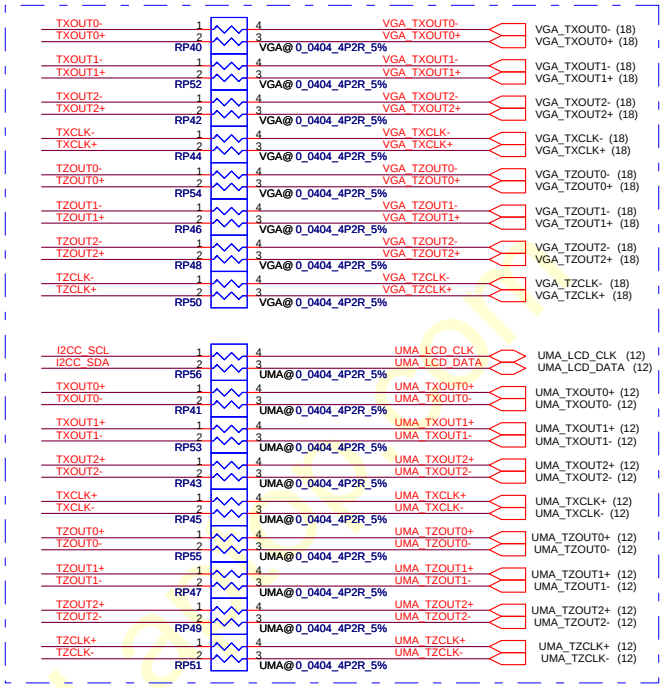
Title: CRT & TV-OUT Connector

Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 Sheet 19 of 42

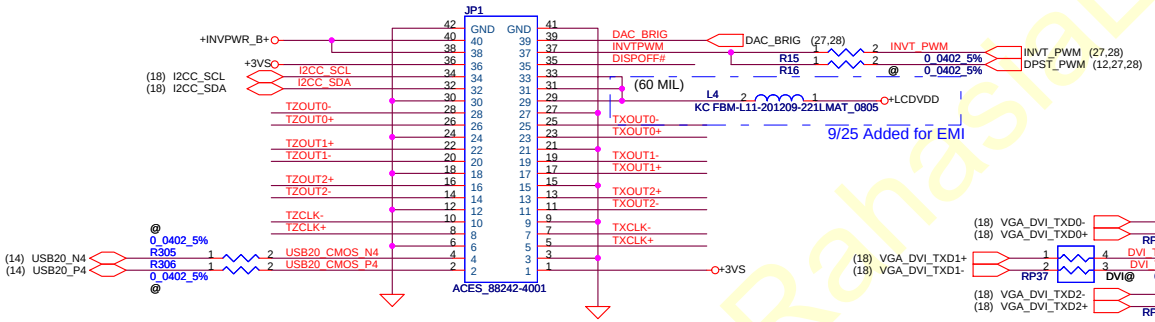
LCD POWER CIRCUIT

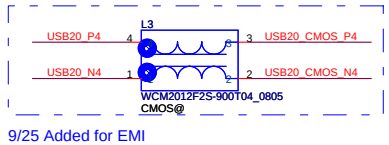


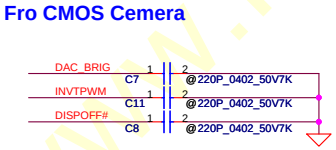


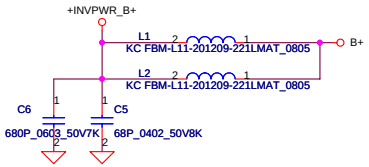
10/2 SWAP PIN

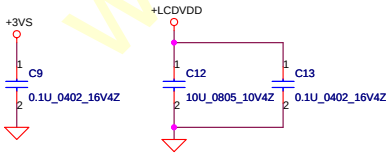
LCD/PANEL BD. Conn.

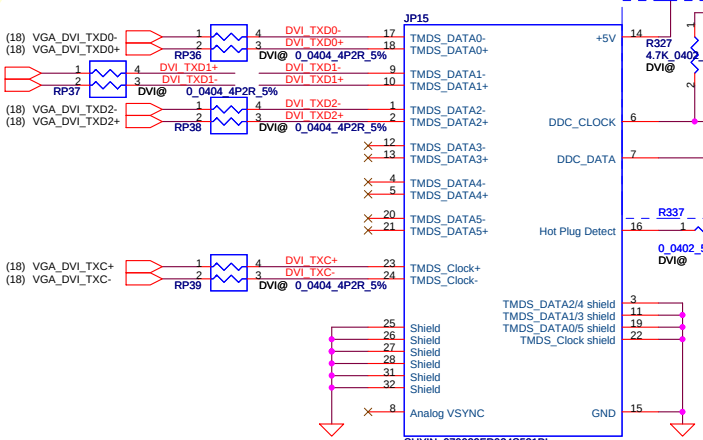


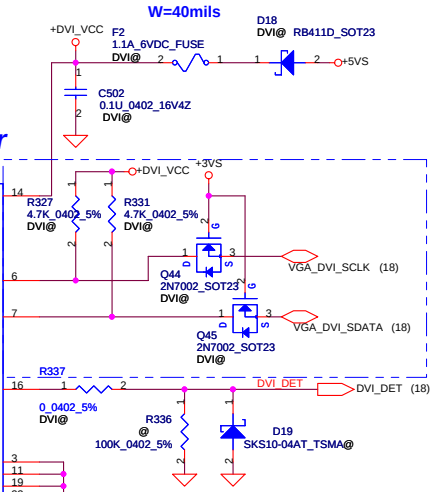












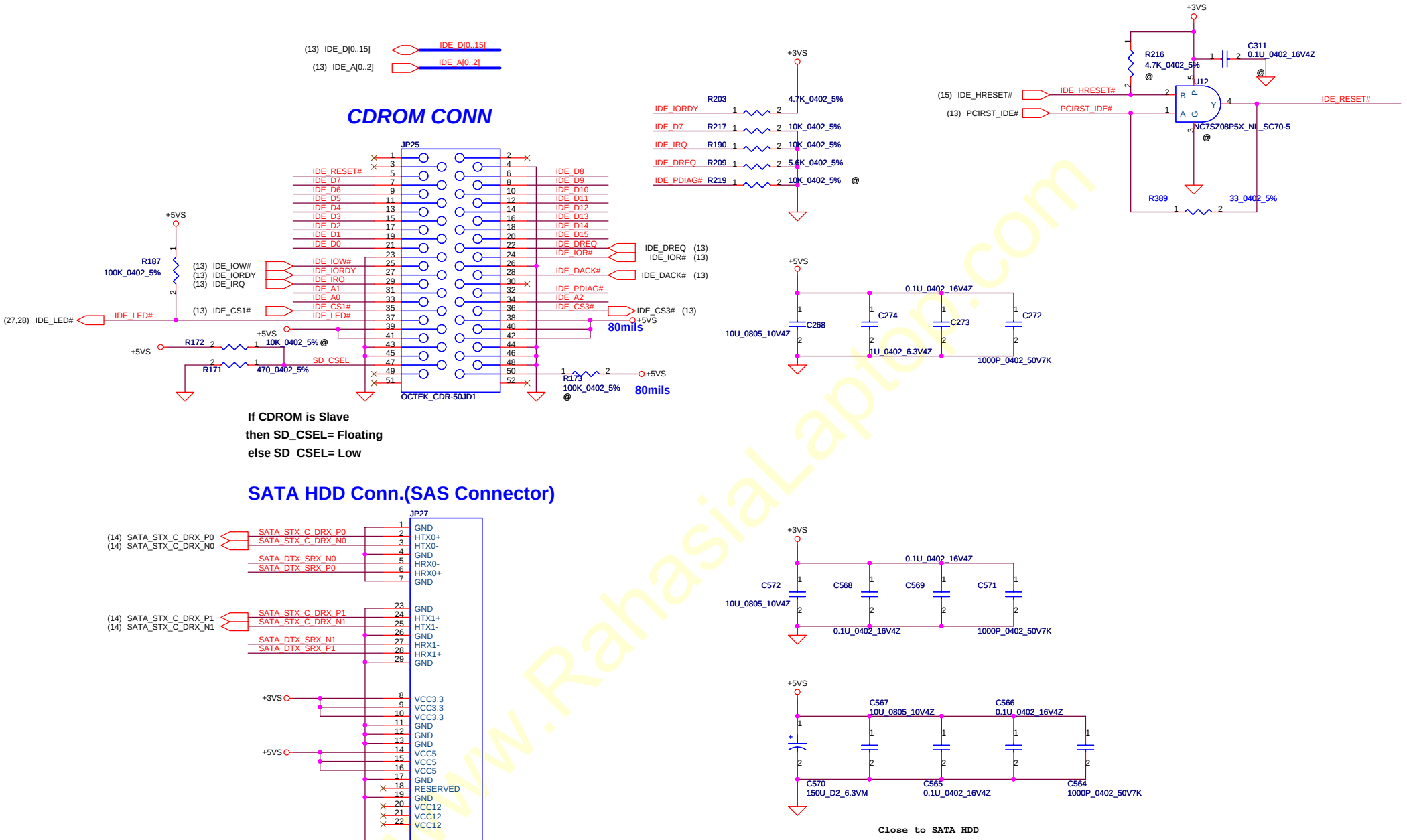
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: LVDS & DVI Connector

Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 | Sheet 20 of 42



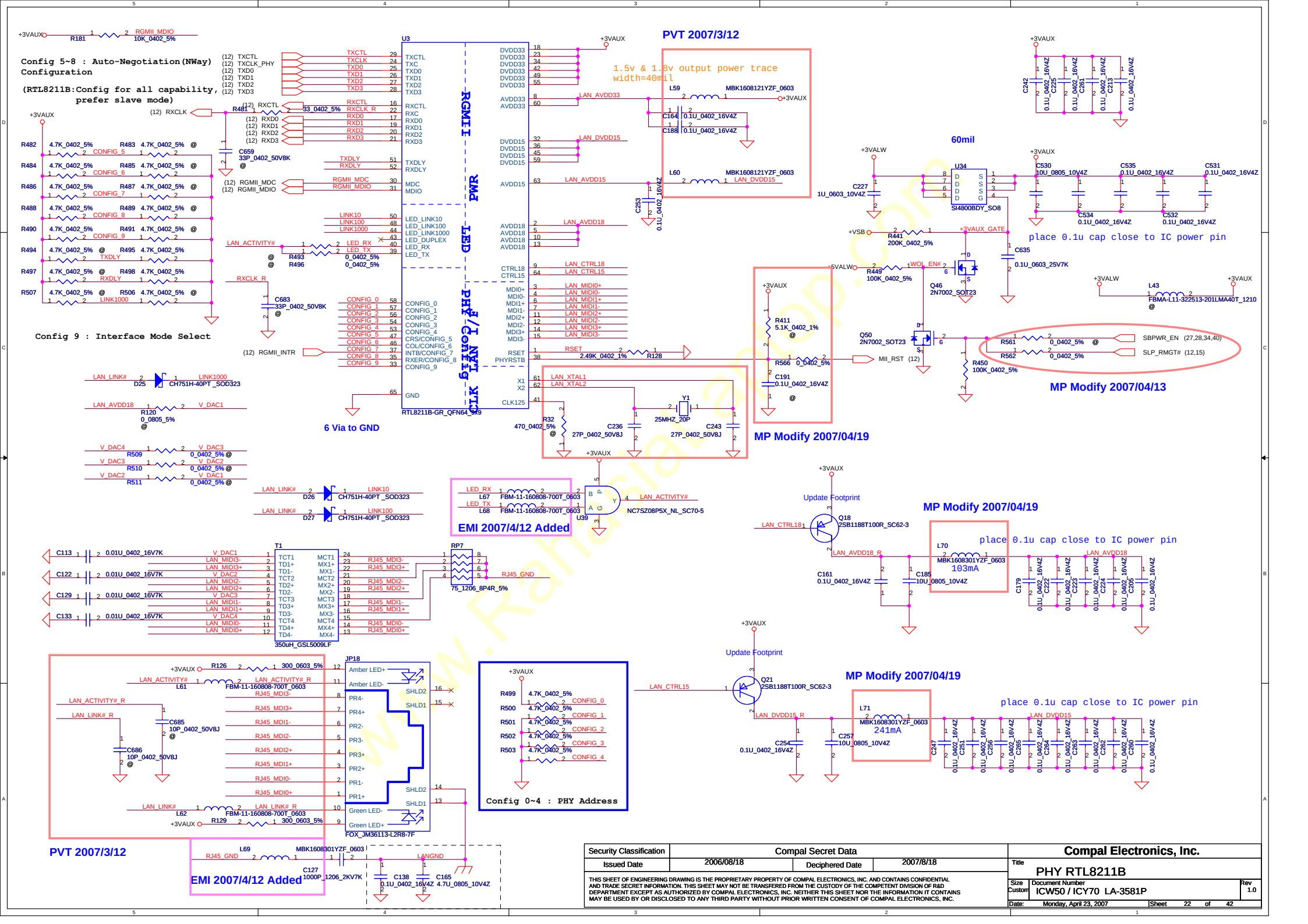
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

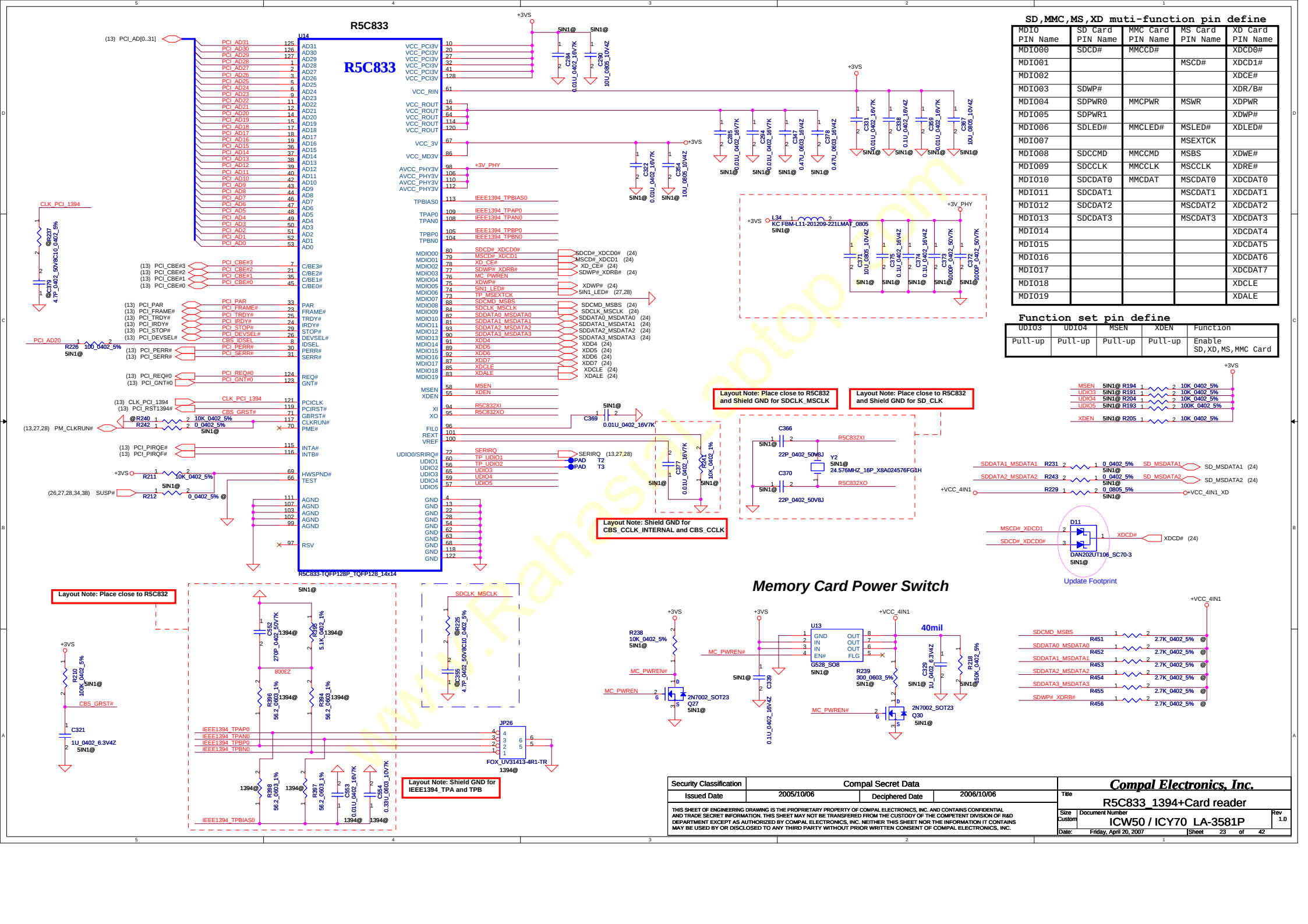
Compal Electronics, Inc.

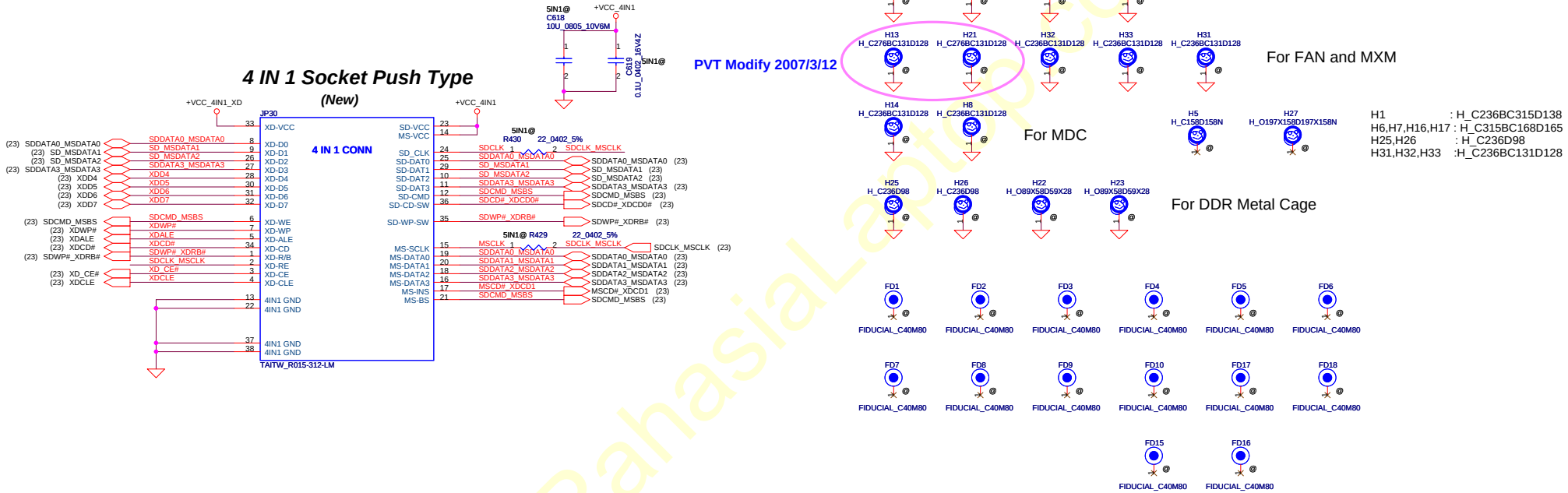
Title: SATA HDD & IDE ODD Connector

Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 | Sheet 21 of 42




R5C833
U14
R5C833-TQFP128P_TQFP128_14x14
SD,MMC,MS,XD muti-function pin define
MDIO PIN Name | SD Card PIN Name | MMC Card PIN Name | MS Card PIN Name | XD Card PIN Name
MDIO00 | SDCD# | MMCCD# | | XDCD0#
MDIO01 | | | MSCD# | XDCD1#
MDIO02 | | | | XDCE#
MDIO03 | SDWP# | | | XDR/B#
MDIO04 | SDPWR0 | MMCPWR | MSWR | XDPWR
MDIO05 | SDPWR1 | | | XDWP#
MDIO06 | SDLED# | MMCLED# | MSLED# | XDLED#
MDIO07 | | | MSEXTCK |
MDIO08 | SDCCMD | MMCCMD | MSBS | XDWE#
MDIO09 | SDCCLK | MMCCLK | MSCCLK | XDRE#
MDIO10 | SDCDAT0 | MMCDAT | MSCDAT0 | XDCDAT0
MDIO11 | SDCDAT1 | | MSCDAT1 | XDCDAT1
MDIO12 | SDCDAT2 | | MSCDAT2 | XDCDAT2
MDIO13 | SDCDAT3 | | MSCDAT3 | XDCDAT3
MDIO14 | | | | XDCDAT4
MDIO15 | | | | XDCDAT5
MDIO16 | | | | XDCDAT6
MDIO17 | | | | XDCDAT7
MDIO18 | | | | XDCLE
MDIO19 | | | | XDALE
Function set pin define
UDIO3 | UDIO4 | MSEN | XDEN | Function
Pull-up | Pull-up | Pull-up | Pull-up | Enable SD,XD,MS,MMC Card
Layout Note: Place close to R5C832 and Shield GND for SDCLK_MSCLK
Layout Note: Place close to R5C832 and Shield GND for SD_CLK
Layout Note: Shield GND for CBS_CCLK_INTERNAL and CBS_CCLK
Layout Note: Place close to R5C832
Layout Note: Shield GND for IEEE1394_TPA and TPB
Memory Card Power Switch
Update Footprint
Compal Electronics, Inc.
R5C833_1394+Card reader
ICW50 / ICY70 LA-3581P
Security Classification: Compal Secret Data
Issued Date: 2005/10/06
Deciphered Date: 2006/10/06
Date: Friday, April 20, 2007
Sheet 23 of 42
Rev 1.0
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Security Classification	Compal Secret Data		
Issued Date	2005/10/06	Deciphered Date	2006/10/06

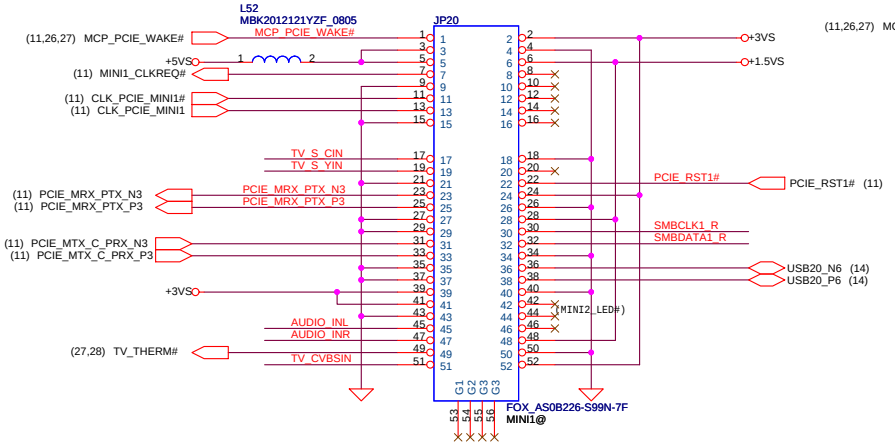
Compal Electronics, Inc.

Title: Card Reader Conn / Screw

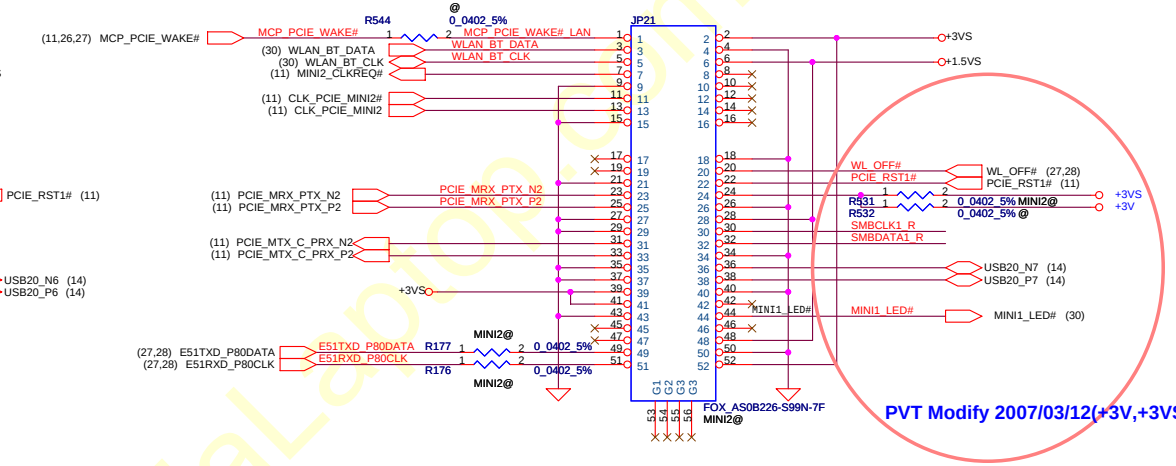
Size: Custom | Document Number: ICW50 / ICY70 LA-3581P | Rev: 1.0

Date: Friday, April 20, 2007 | Sheet 24 of 42

TV TUNNER

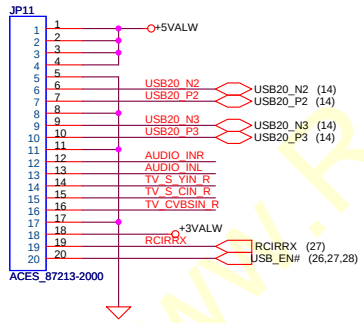


PVT2 Modify 2007/04/12



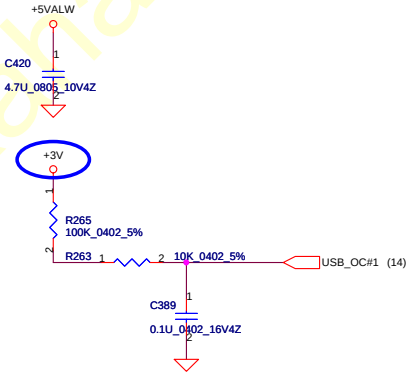
PVT Modify 2007/03/12(+3V,+3VS)

USB/B Connector

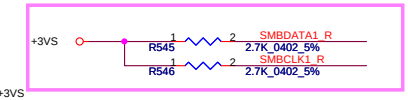


AV-IN Connector

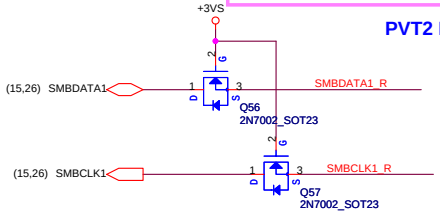
CIR

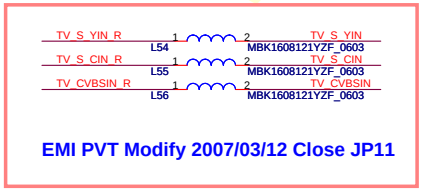


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



PVT2 Modify 2007/04/12





EMI PVT Modify 2007/03/12 Close JP11

Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

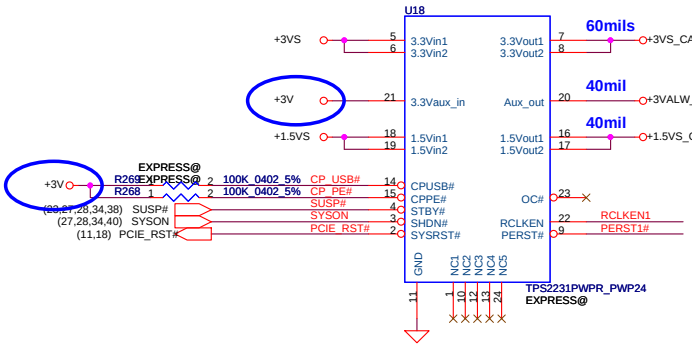
Compal Electronics, Inc.

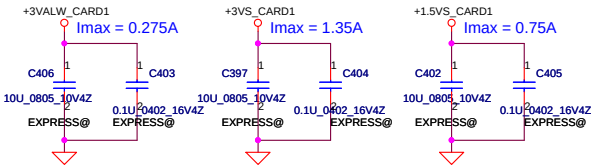
Title: MINI CARD / USB-B Conn.

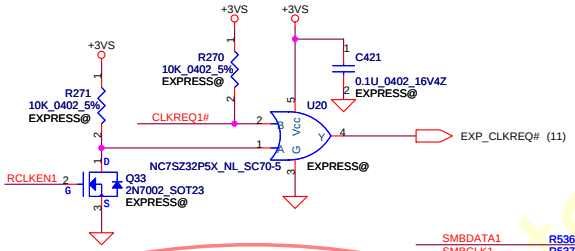
Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

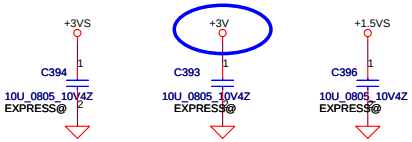
Date: Friday, April 20, 2007 Sheet 25 of 42

New Card Power Switch

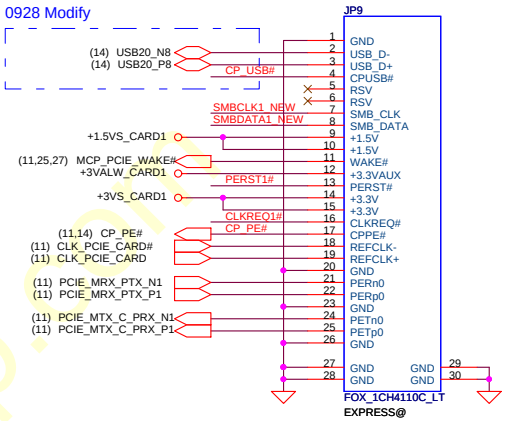


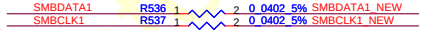


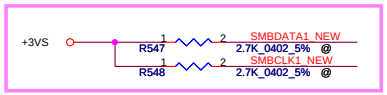




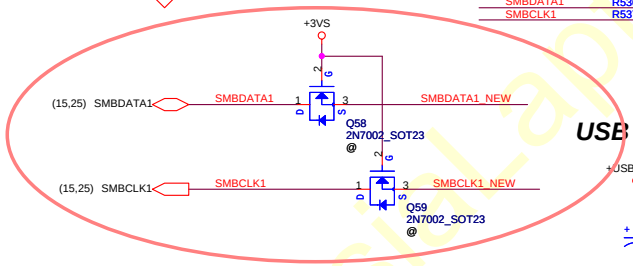
New Card Socket (Left/TOP)





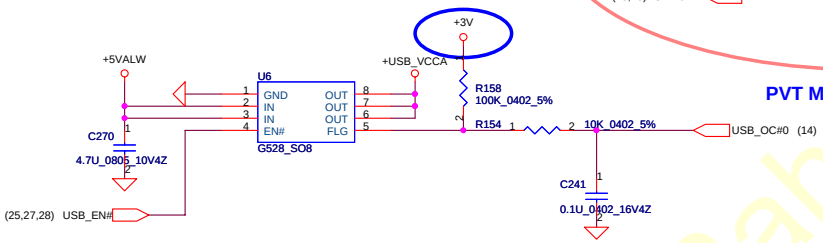


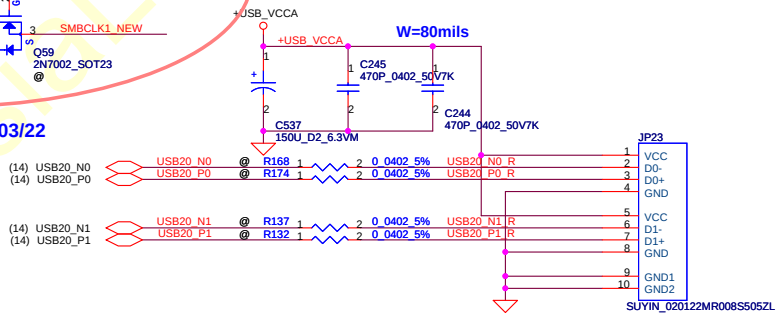
PVT2 Modify 2007/04/11

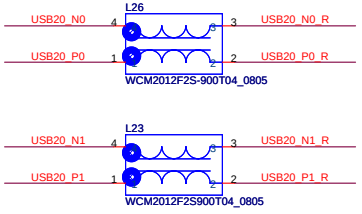


USB CONN. 1(Stack-up Type)

PVT Modify 2007/03/22







SUYIN_020173MR004G533ZR_4P

SUYIN_020173MR004G533ZR_4P

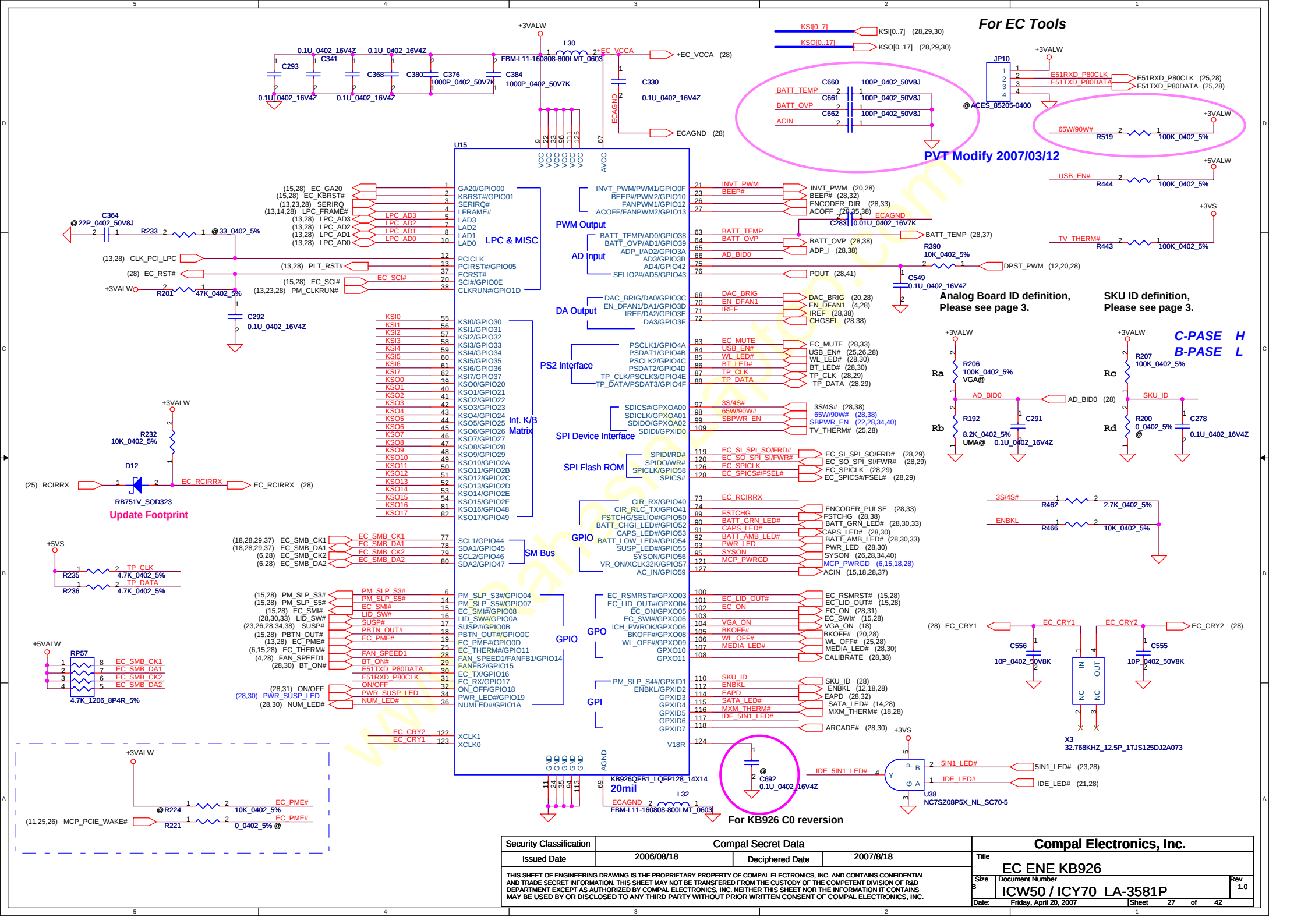
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

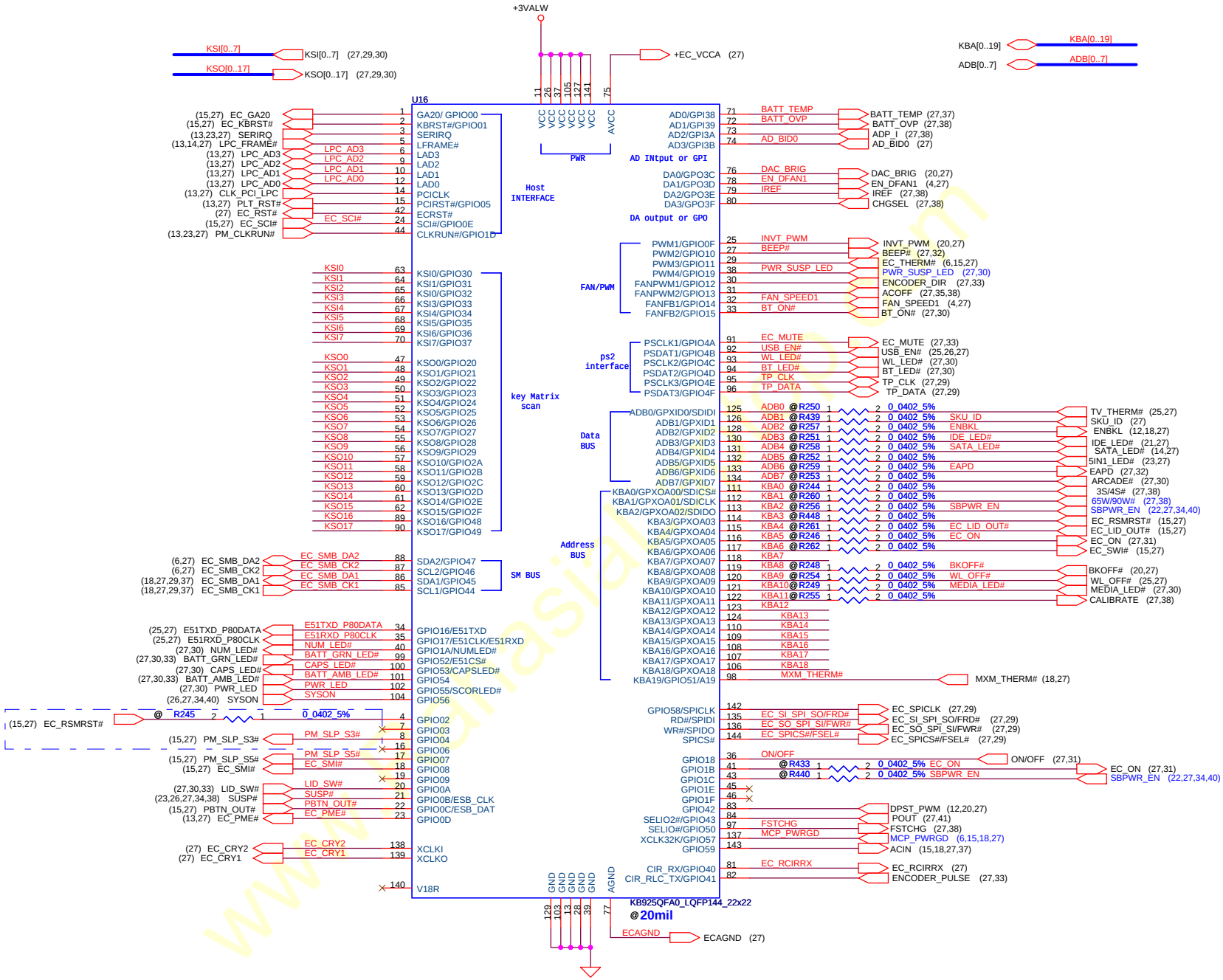
Compal Electronics, Inc.

Title: NEW CARD & USB Connector

Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 Sheet 26 of 42





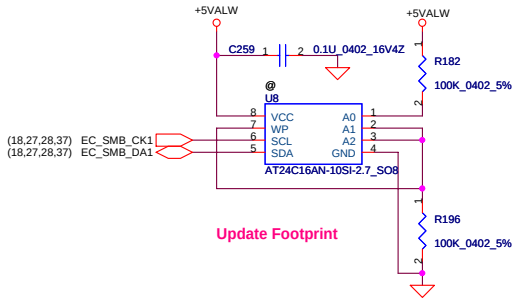
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: EC ENE KB910L/925(Reserved)

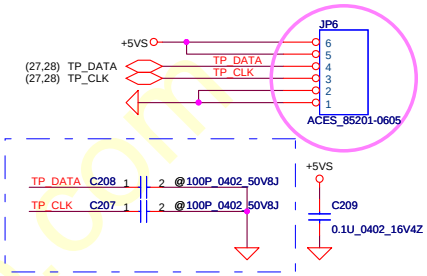
Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 | Sheet 28 of 42

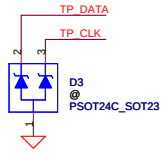


Update Footprint

To TP/B Conn.



9/25 Added for EMI



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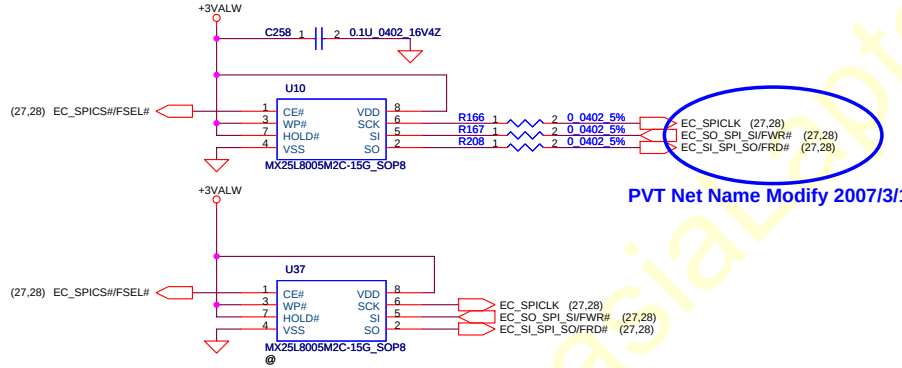
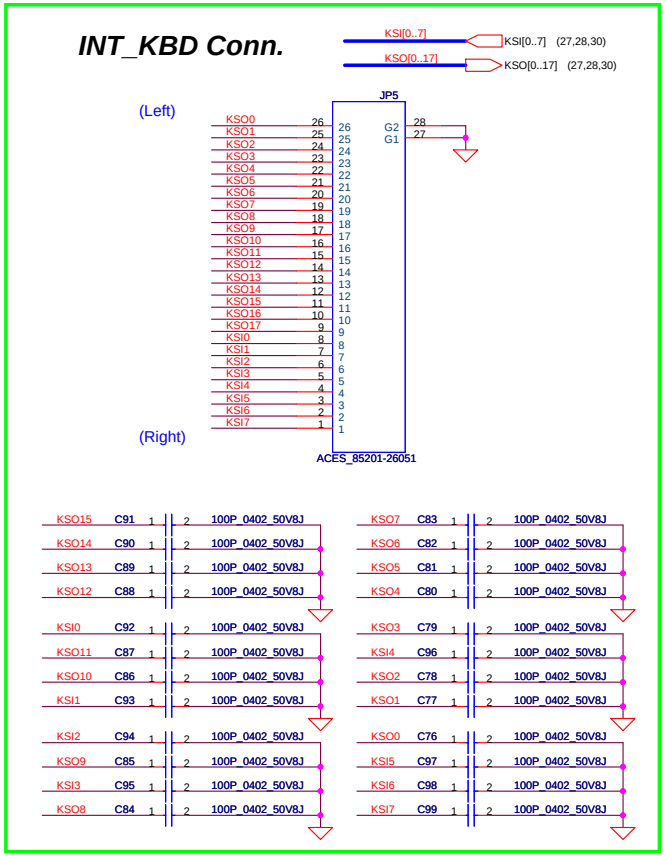


PVT Net Name Modify 2007/3/12

INT_KBD Conn.



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

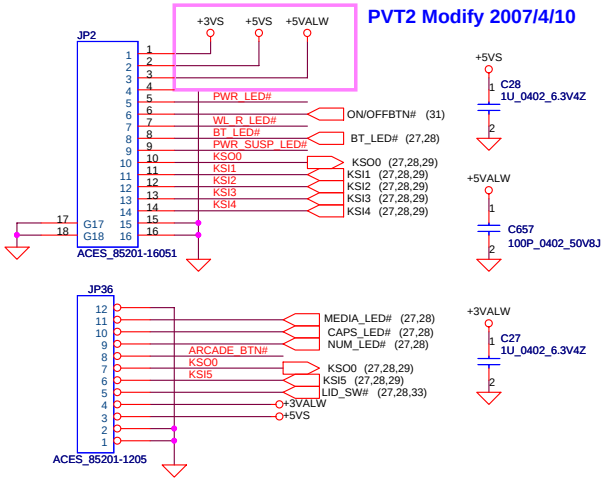
Title: BIOS, I/O Port & K/B Connector

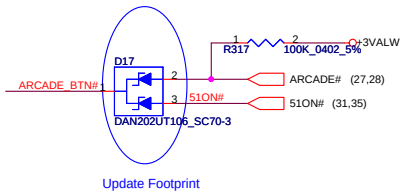
Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Monday, April 23, 2007 Sheet 29 of 42

	KSO0
KSI1	WL_BTN#
KSI2	BT_BTN#
KSI3	EMAIL_BTN#
KSI4	IE_BTN#
KSI5	E-KEY_BTN#

Check 15.4" K/B Matrix





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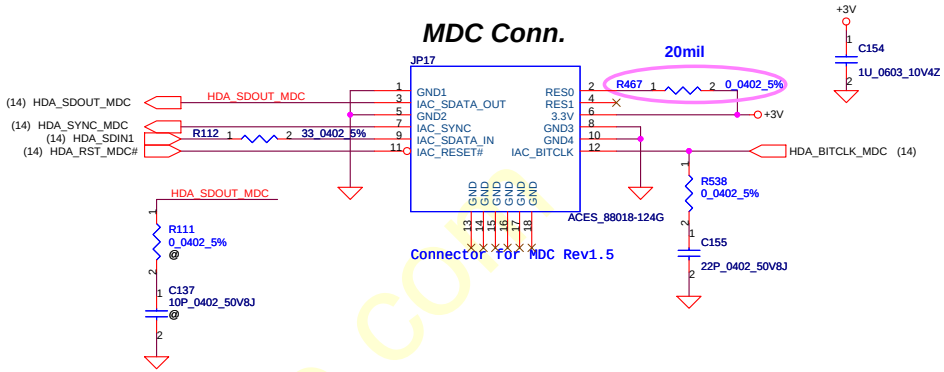
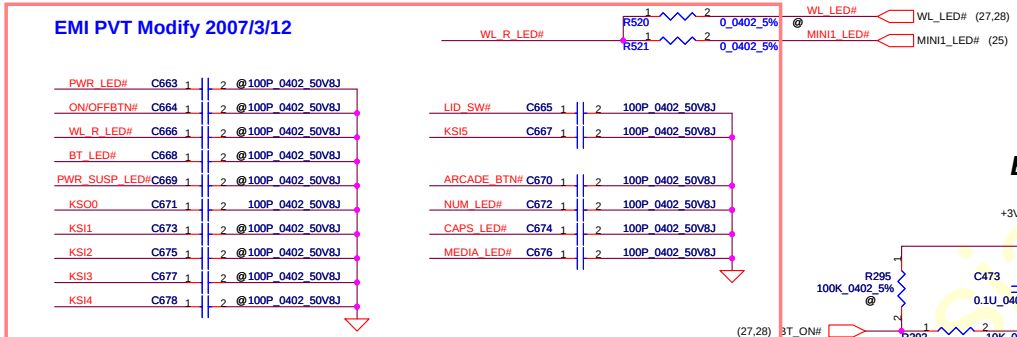
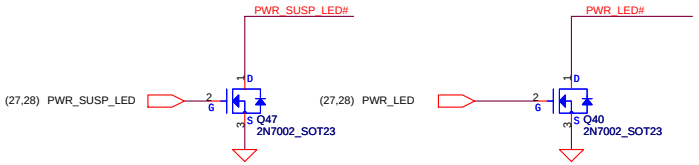
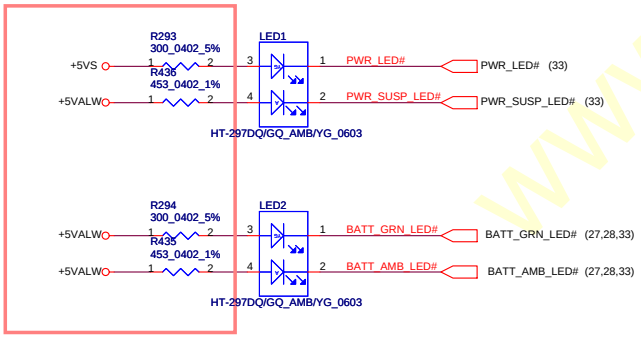
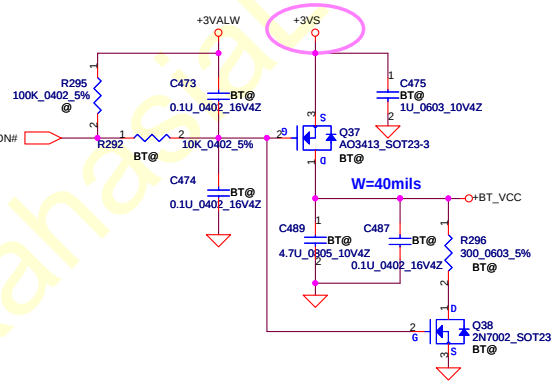


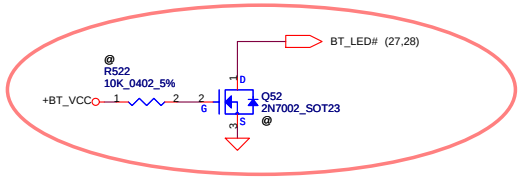




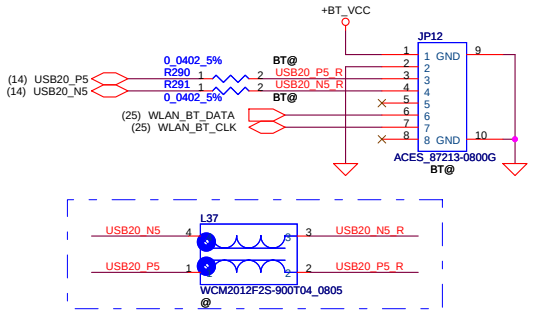


PVT Value Modify to 453E 2007/3/12





PVT Modify 2007/3/12



9/25 Added for EMI

Compal Footprint

4 2
3 1

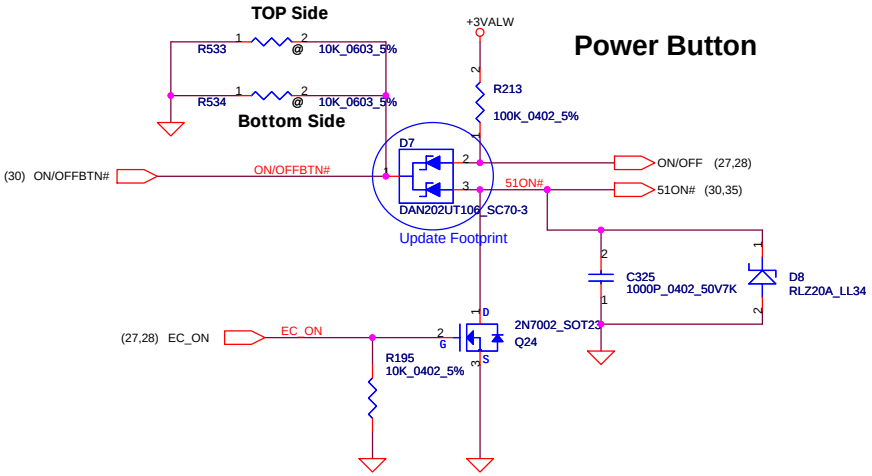
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

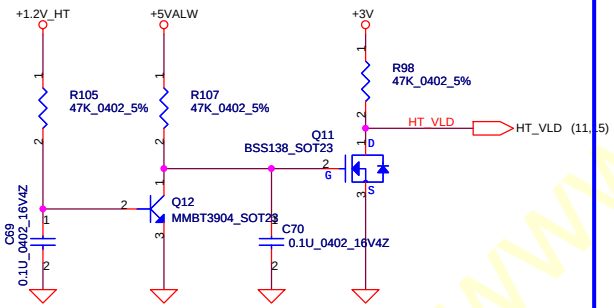
Title: MDC / BT / CIR / LED

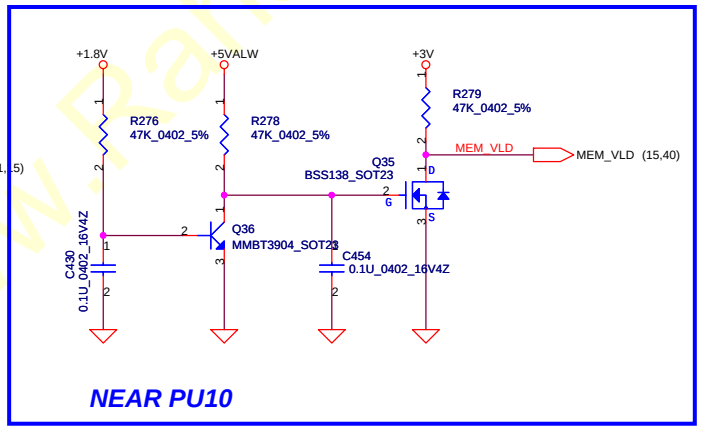
Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 | Sheet 30 of 42



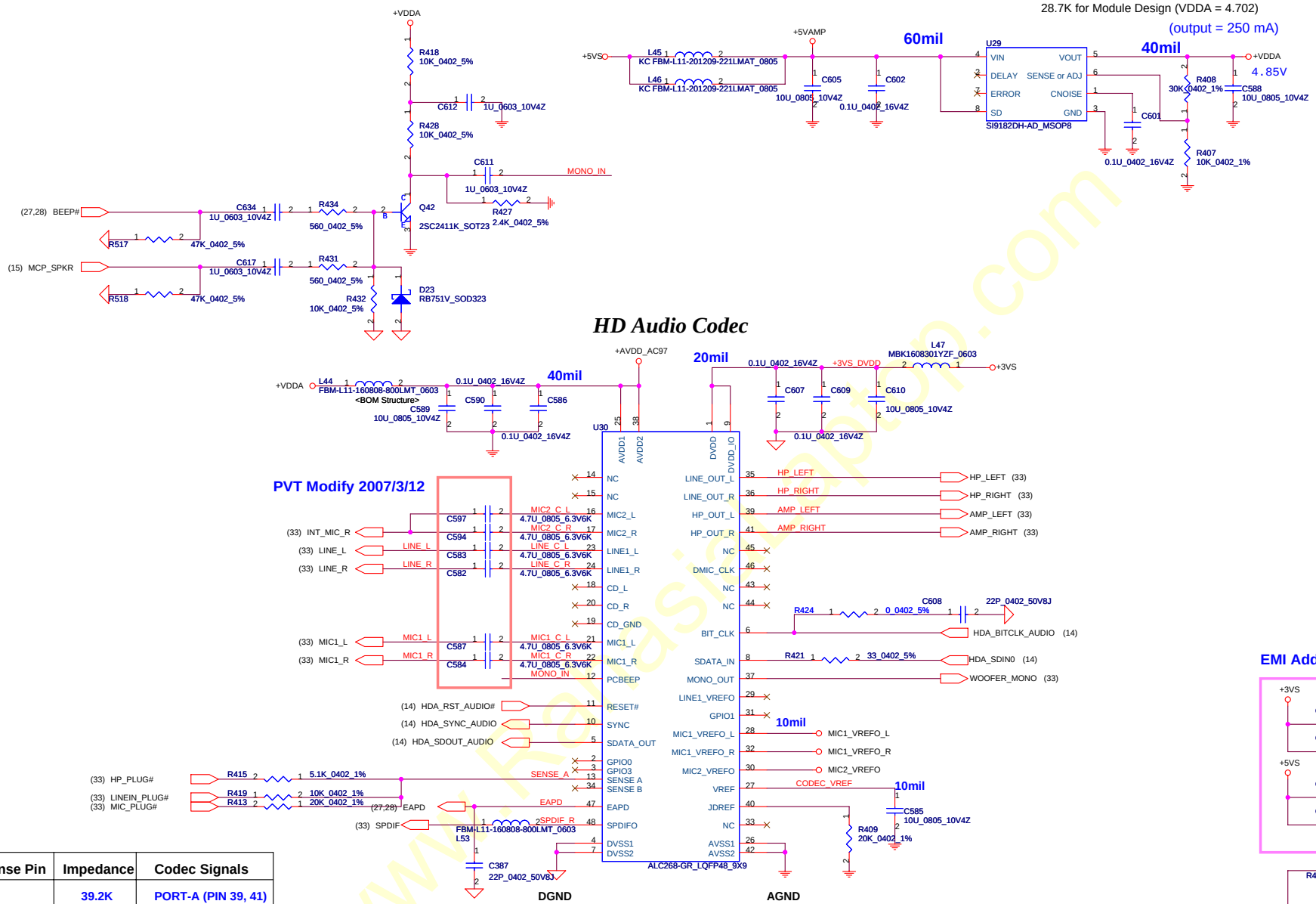
Power ON Circuit





Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Title	PWR_OK CIRCUIT/ BTN		
Size: Custom	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 31 of 42		



Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

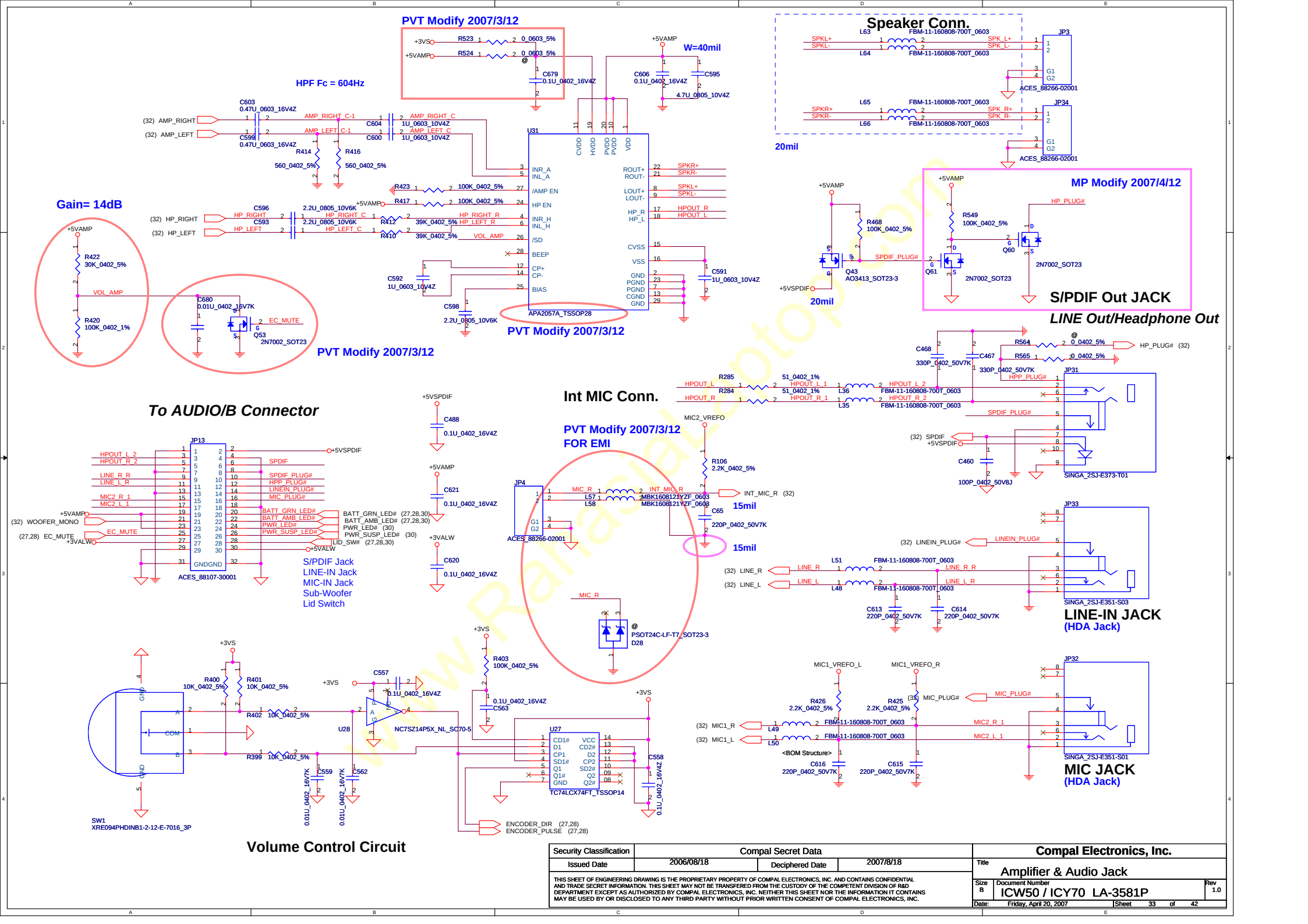
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: HD Audio Codec ALC268

Size: B | Document Number: ICW50 / ICY70 LA-3581P | Rev: 1.0

Date: Friday, April 20, 2007 | Sheet 32 of 42



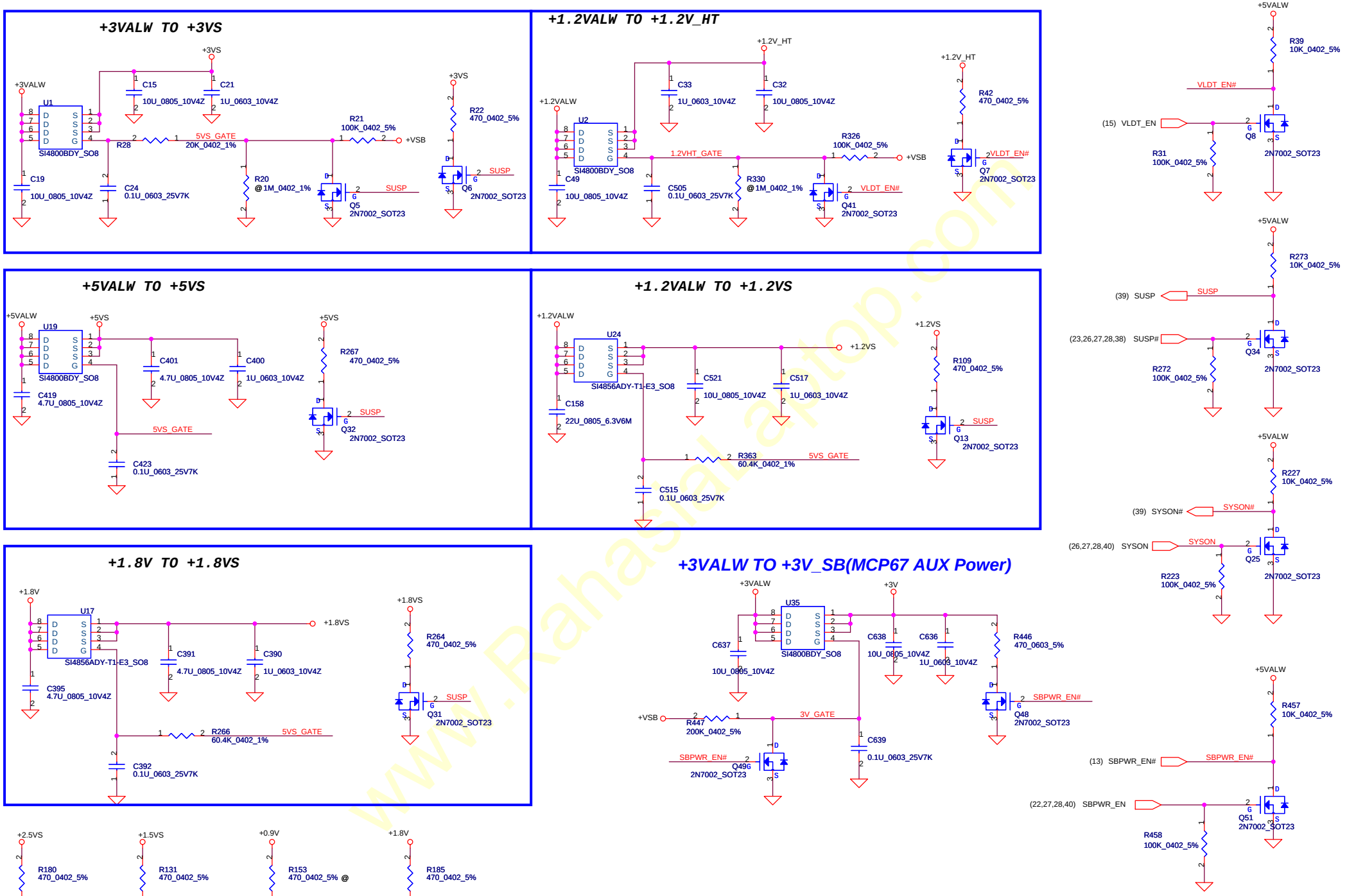
Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Compal Electronics, Inc.

Title: Amplifier & Audio Jack

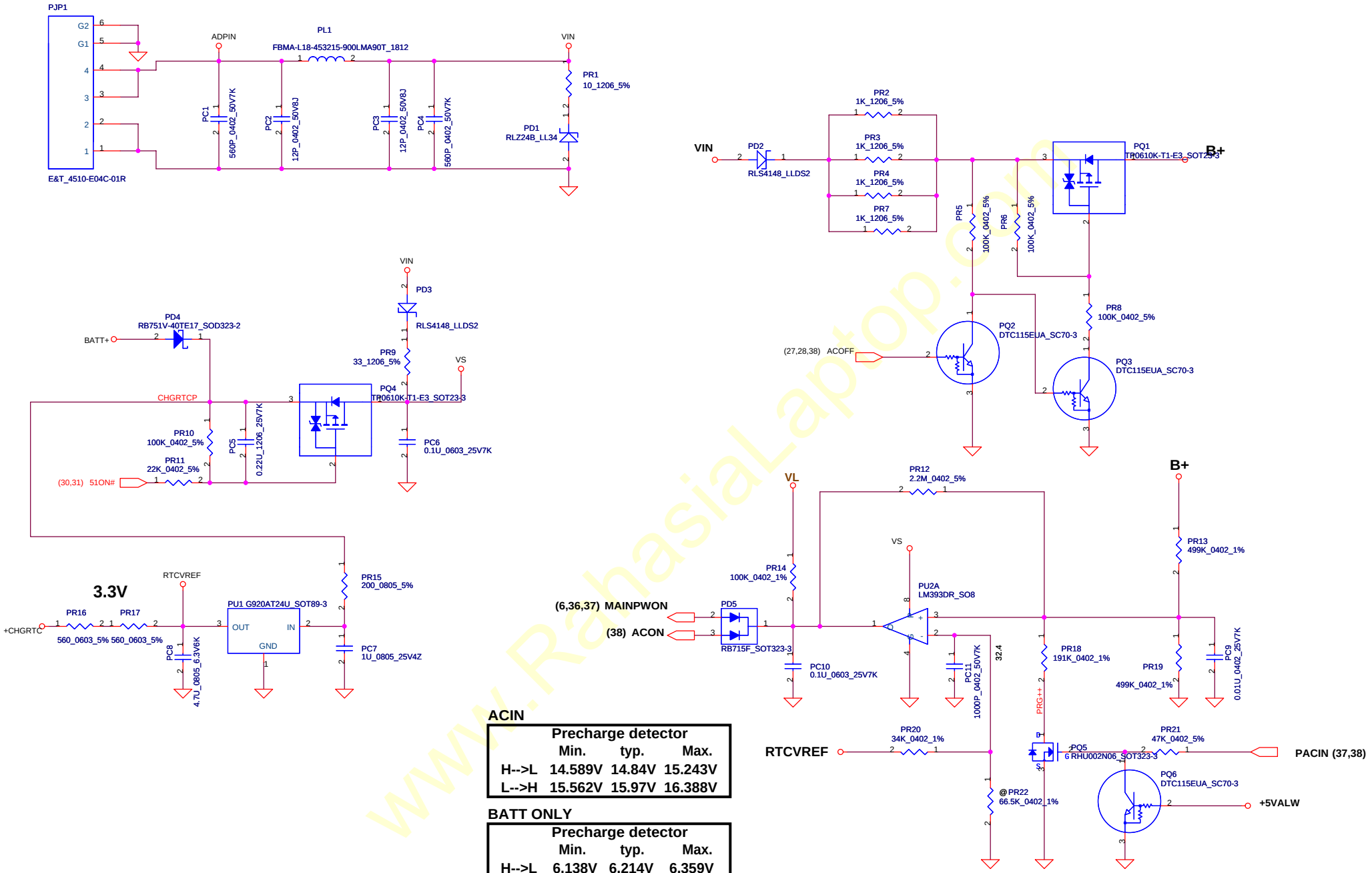
Size	Document Number	Rev
B	ICW50 / ICY70 LA-3581P	1.0

Date: Friday, April 20, 2007 | Sheet 33 of 42



Security Classification	Compal Secret Data		
Issued Date	2006/08/18	Deciphered Date	2007/8/18

Title	DC INTERFACE		
Size: B	Document Number: ICW50 / ICY70 LA-3581P		Rev: 1.0
Date: Friday, April 20, 2007	Sheet 34 of 42		



ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

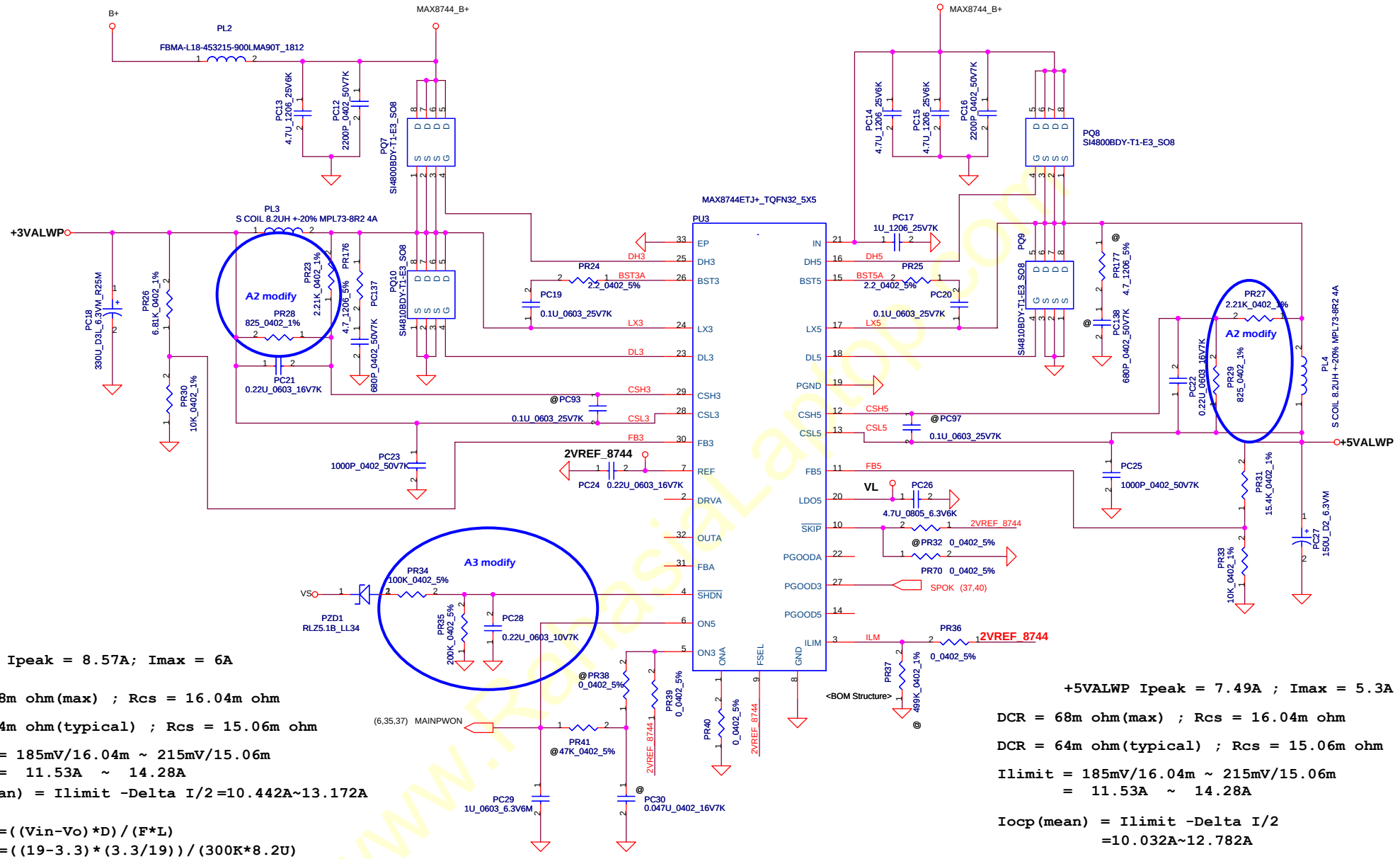
Security Classification	Compal Secret Data		
Issued Date	2006/09/01	Deciphered Date	2007/09/01

Compal Electronics, Inc.

Title: DCIN/DECTOR

Size	Document Number	Rev
B	ICW50/ICY70	1.0

Date: Friday, April 20, 2007 | Sheet 35 of 42



+3VALWP Ipeak = 8.57A; Imax = 6A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m
= 11.53A ~ 14.28A

Iocp(mean) = Ilimit -Delta I/2 =10.442A~13.172A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-3.3)*(3.3/19))/(300K*8.2U)
=1.108A

Notes :

fESR<=fOSC/π ; fESR=1/(2*π*RESR*COUT)

ON3 = REF --->3.3V starts up delay 2ms after 5V starts up

+5VALWP Ipeak = 7.49A ; Imax = 5.3A

DCR = 68m ohm(max) ; Rcs = 16.04m ohm

DCR = 64m ohm(typical) ; Rcs = 15.06m ohm

Ilimit = 185mV/16.04m ~ 215mV/15.06m
= 11.53A ~ 14.28A

Iocp(mean) = Ilimit -Delta I/2
=10.032A~12.782A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-5)*(5/19))/(300K*8.2U)
=1.498A

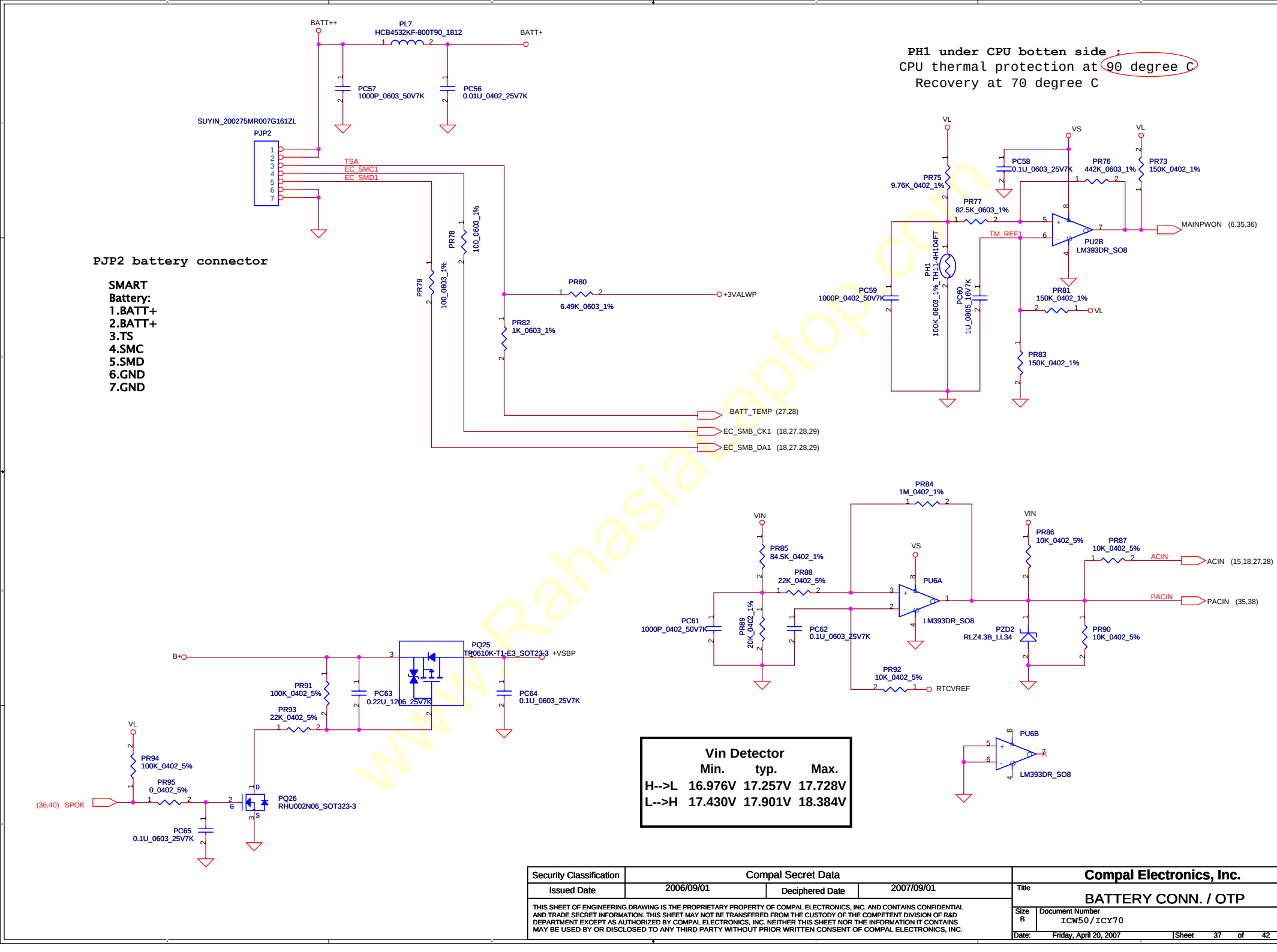
Security Classification	Compal Secret Data		
Issued Date	2006/09/01	Deciphered Date	2007/09/01

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size	Document Number	Rev
Custom	ICW50/ICY70	1.0

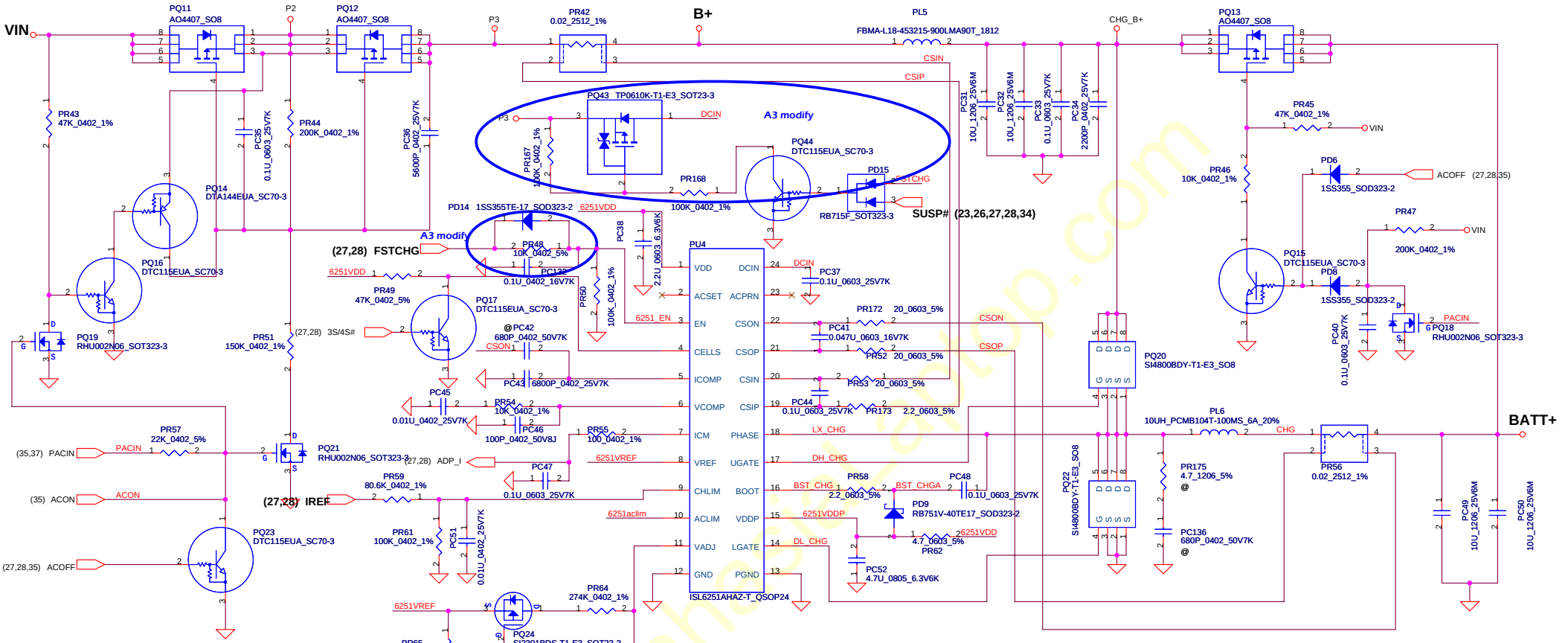
Date: Friday, April 20, 2007 | Sheet 36 of 42



Iada=0~4.74A(90W)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

OVP voltage :

LI-4S :18.0V--BATT-OVP=2.677V

BATT-OVP=0.1487*BATT+

LI-3S :13.50V--BATT-OVP=2.007V

BATT-OVP=0.1487*BATT+

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

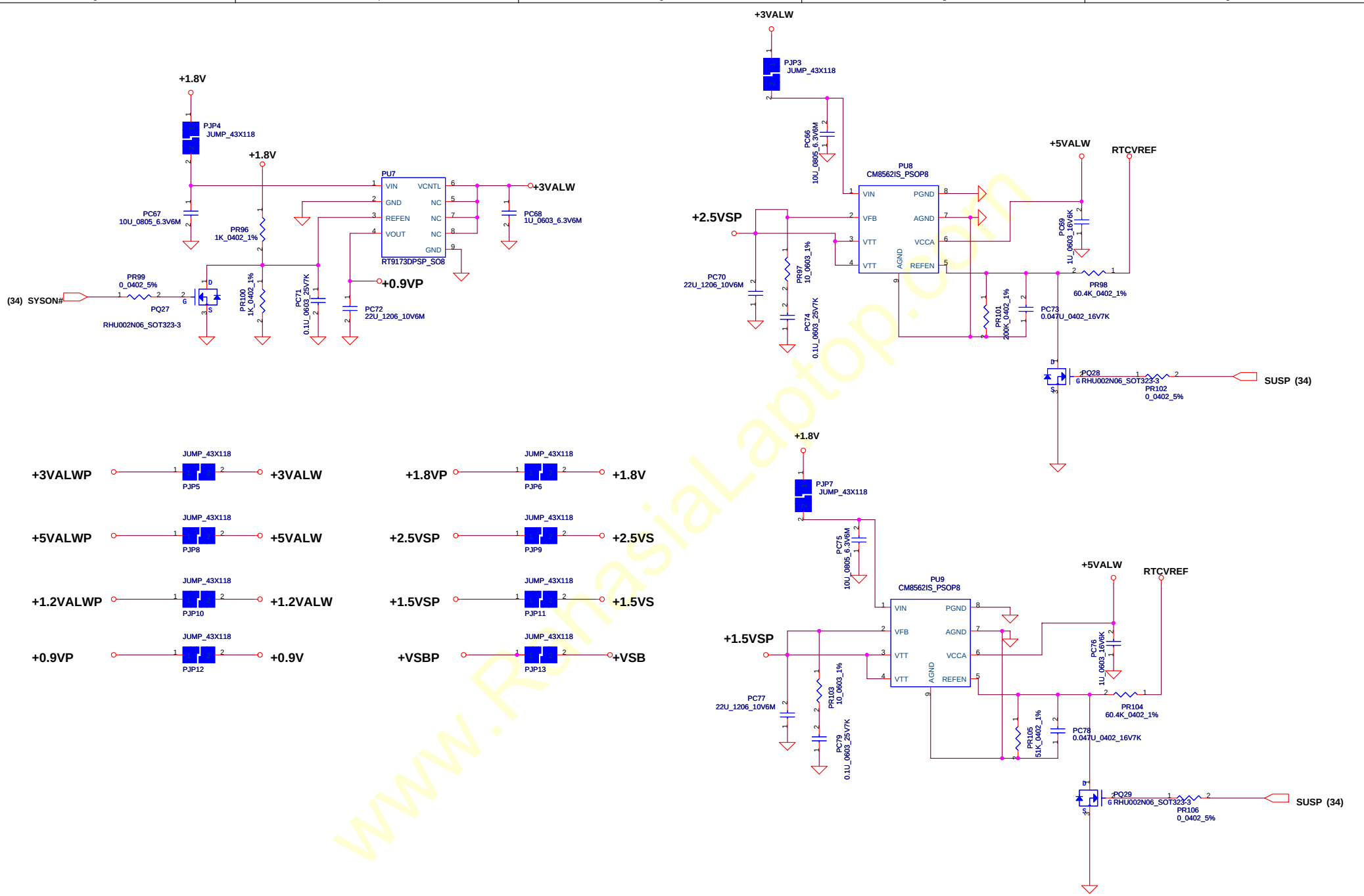
Security Classification	Compal Secret Data		
Issued Date	2006/09/01	Deciphered Date	2007/09/01

Compal Electronics, Inc.

Title: CHARGER

Size | Document Number: ICW50/ICY70 | Rev: 1.0

Date: Friday, April 20, 2007 | Sheet 38 of 42



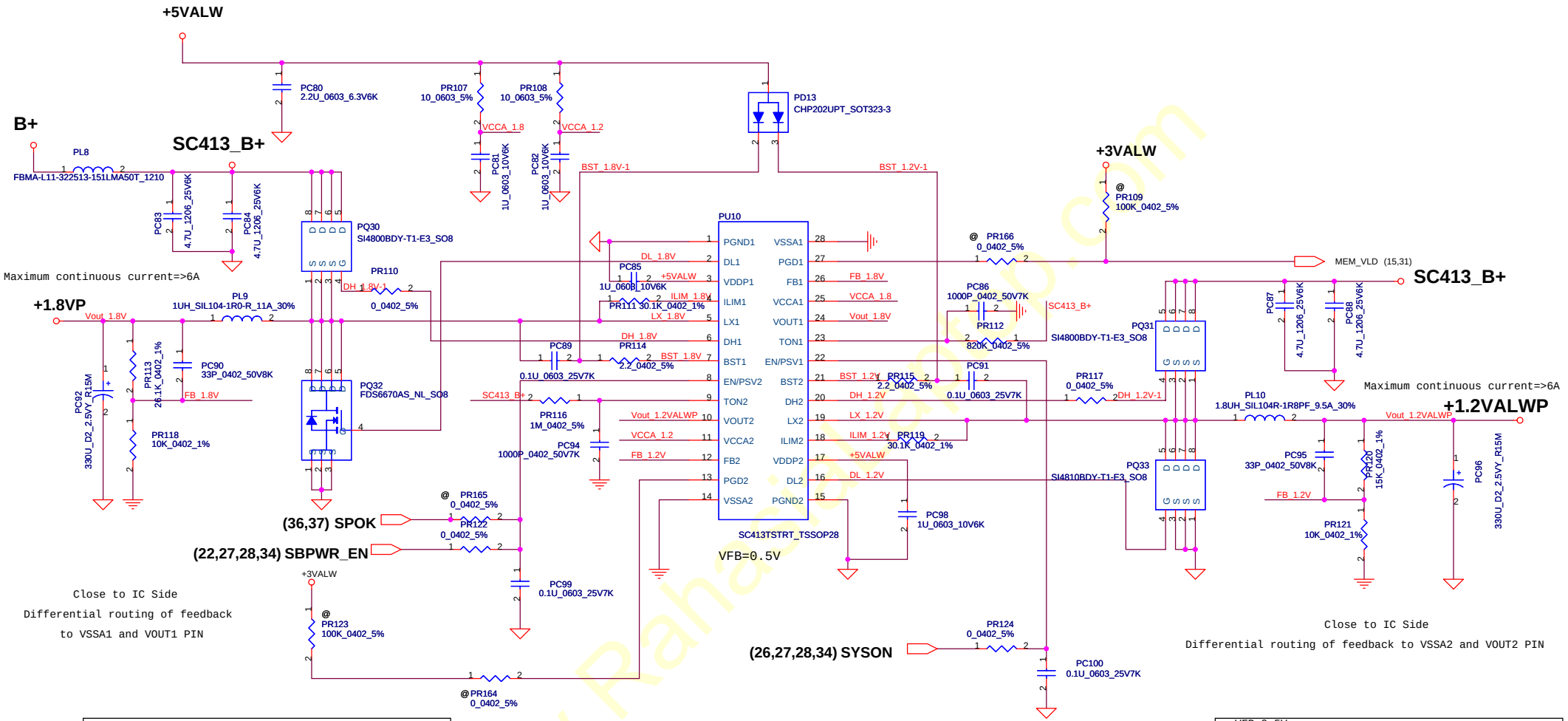
Security Classification	Compal Secret Data		
Issued Date	2006/09/01	Deciphered Date	2007/09/01

Compal Electronics, Inc.

Title: +0.9VSP/+1.5VSP/+2.5VSP

Size	Document Number	Rev
Custom	ICW50/ICY70	1.0

Date: Friday, April 20, 2007 Sheet 39 of 42



VFB=0.5V
Vo=VFB*(1+PR122/PR127)=1.805V
Ipeak=13.82A, Imax=9.68A
Ton=(3.3E-12*(PR112+37K)*(Vout/VBat))+50ns
=3.3E-12*(820K+37K)*(1.805/19)+50ns=0.319us
FDS6670AS:Rds(on)=>Typ:9 mOhm
Max:11.5 mOhm
Iocp=Ivalley+ Iripple /2
Iripple=(vin-vout)*(Ton/L)=5.485A
Ivalleymin=9E-6*(PR106/Rds(ON)max*1.4)=16.826A
Ivalleymax=11E-6*(PR106/Rds(ON)typ*1.2)=30.657A
OCP==>19.5685A~33.3995A

VFB=0.5V
Vo=VFB*(1+PR120/PR121)=1.25V
Ipeak=8.54A, Imax=6A
Ton=(3.3E-12*(PR116+37K)*(Vout/VBat))+50ns
=0.2661us
SI4810BDY:Rds(on)=>Typ:16 mOhm
Max:20 mOhm
Ivalleymin=9E-6*(PR119/Rds(ON)max*1.3)=10.419A
Ivalleymax=11E-6*(PR119/Rds(ON)typ*1.1)=18.8125A
Iripple=(vin-vout)*(Ton/L)=2.631A
Iocp=Ivalley+ Iripple /2
OCP==>11.7345A~20.128A

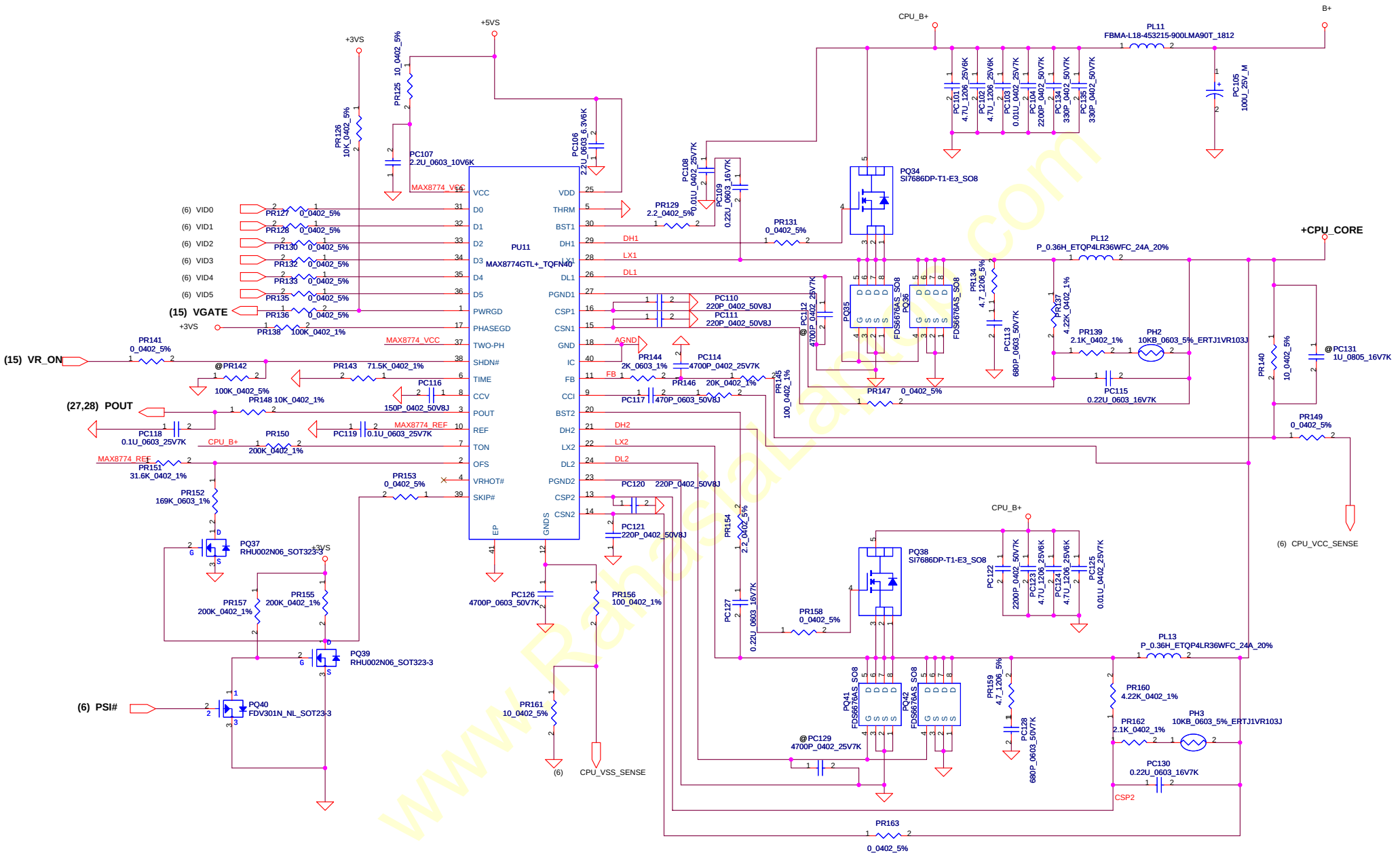
Security Classification	Compal Secret Data		
Issued Date	2006/09/01	Deciphered Date	2007/09/01

Compal Electronics, Inc.

Title: +1.8VALWP/+1.2VALWP

Size	Document Number	Rev
Custom	ICW50/ICY70	1.0

Date: Friday, April 20, 2007 Sheet 40 of 42



Security Classification	Compal Secret Data		
Issued Date	2006/09/01	Deciphered Date	2007/09/01

Compal Electronics, Inc.

Title: **+CPU_CORE**

Size	Document Number	Rev
Custom	ICW50/ICY70	1.0

Date: Friday, April 20, 2007 | Sheet 41 of 42

Version change list (P.I.R. List)

Item	Fixed Issue	Rev.	PG#	Modify List	Date	Phase
1	BOM Change.	0.4	12	Remove R144, R372, C160, C528.		PVT
2	Added SSC for Lan TXCLK. (EMI Request)	0.4	12	Added U40, R525, R526, R527, R528, C682.		PVT
3	Improve Samsung Memory Module compatibility.	0.4	15	Added R540,R541 2.2K pull up +3VS.		PVT
4	Design Modify.(SCH Change)	0.4	15	Change CRT_DET form GPIO_5 to LID#, Add R78 10K. (Bios Request)		PVT
5	BCIC0172 : When Reset or Cold Boot MCP67 ACIN 會漏電到EC.	0.4	15	D24 反向, 47K Pull High移除.Added R283 200K Pull Down.		PVT
6	RTC Battery 電壓過低.	0.4	16	Added R539 1K.		PVT
7	Design Modify.(SCH Change)	0.4	22	Change Q50.G Pin Net Name to SBPWR_EN.		PVT
8	Added R-C for BUF_25Mhz (EMI Request).	0.4	22	Added R530,C684.		PVT
9	Design Modify for EMI.	0.4	22	Added L59, L60, L61, L62, C685, C686.		PVT
10	解決+3VS 漏電 when enter S3 Mode.	0.4	25,26	Added Q56, Q57, Q58, Q59, R536, R537.		PVT
11	Design Modify for Acer WLAN LED.	0.4	25	JP21.44 Pin Added MINI1_LED# Net, Added R520, R521.		PVT
12	防止 BATT_TEMP, BATT_OVP, ACIN 被干擾.	0.4	27	Added C660, C661, C662.		PVT
13	Design Modify for Power. (65W/95W Detect Function)	0.4	27	U15.98 Pin Added 65W/95W# Net, Added R519 100K to +3VALW.		PVT
14	Design Modify for EMI.	0.4	30	Added C663~C678.		PVT
15	For AUDIO EA Test.	0.4	32	Change C582, C583, C584, C587,C594, C597 to 4.7uF.		PVT
16	解決關機 bo bo 聲問題.	0.4	33	Added Q53,C680.		PVT
17	Design Modify for EMI.	0.4	33	Added L57, L58 for Mic. L63, L64, L65, L66 for SPK. D28 for ESD.		PVT
18	Change Codec Amp to APA2057RI-TRL_TSSOP28.	0.4	33	Change U31 to SA00001QD00, added R523,R524.		PVT
19	Remove PJP14.	0.4	34	Remove PJP14.		PVT
20	Change MCP67-MV form A01 to A02.	0.4	10~17	Change MCP67-MV form A01 to A02.		PVT
21	解決系統時間延遲問題.	0.4	15	Change C503, C504 form 18pF to 6.8pF.		PVT
22	Improve WLAN Module compatibility.	0.3	11,25	Change WLAN Port form PCIE4 to PCIE2.		DVT2
23	Fixed LAN LED work abnormal.	0.3	22	Added D25,D27,D27, U39.		DVT2
24	Change LAN to RTL8211B.	0.2	22	Change Page 22 all compnent. DVT1		