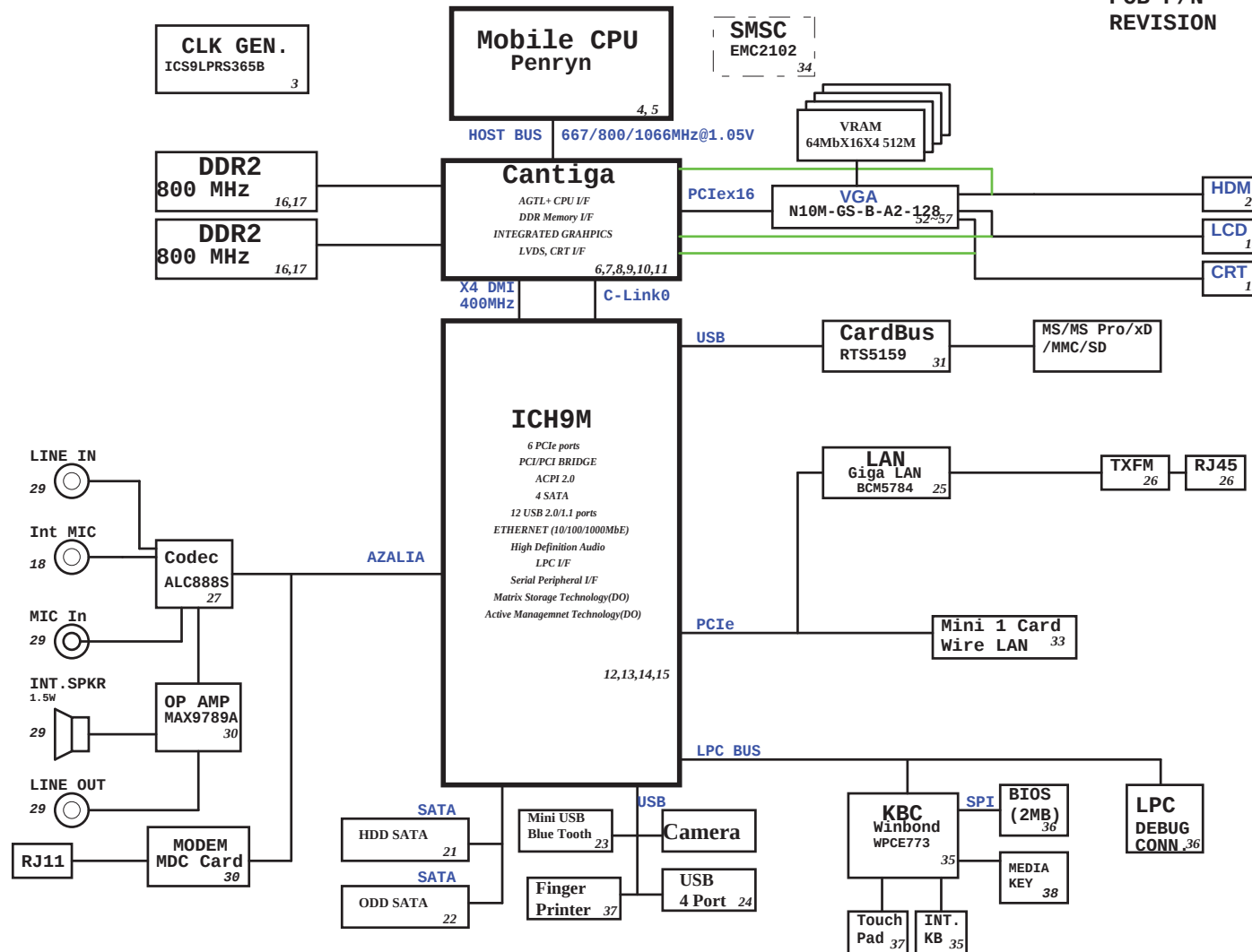


JV71-MV Block Diagram

Project code: 91.4FX01.001
PCB P/N : 48.4FX01.0SA
REVISION : 09242 -1



SYSTEM DC/DC ISL62392 42	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A) 5V_AUX_S5 3D3V_AUX_S5
SYSTEM DC/DC TPS51124 43	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9A) 1D5V_S3(12A)
RT9026 44	
1D5V_S3	DDR_VREF_S3(1.2A)
RT9018 44	
1D5V_S3	1D1V_S0(2A)
TPS51117 45	
DCBATOUT	FBVDD(4A)
CHARGER ISL88731A 47	
INPUTS	OUTPUTS
DCBATOUT	BT+
CPU DC/DC ISL6266A 41	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 38A
VGA_CORE RT8202A 47	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 13A
GFXCORE ISL6263A 46	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE (7A)

PCB STACKUP

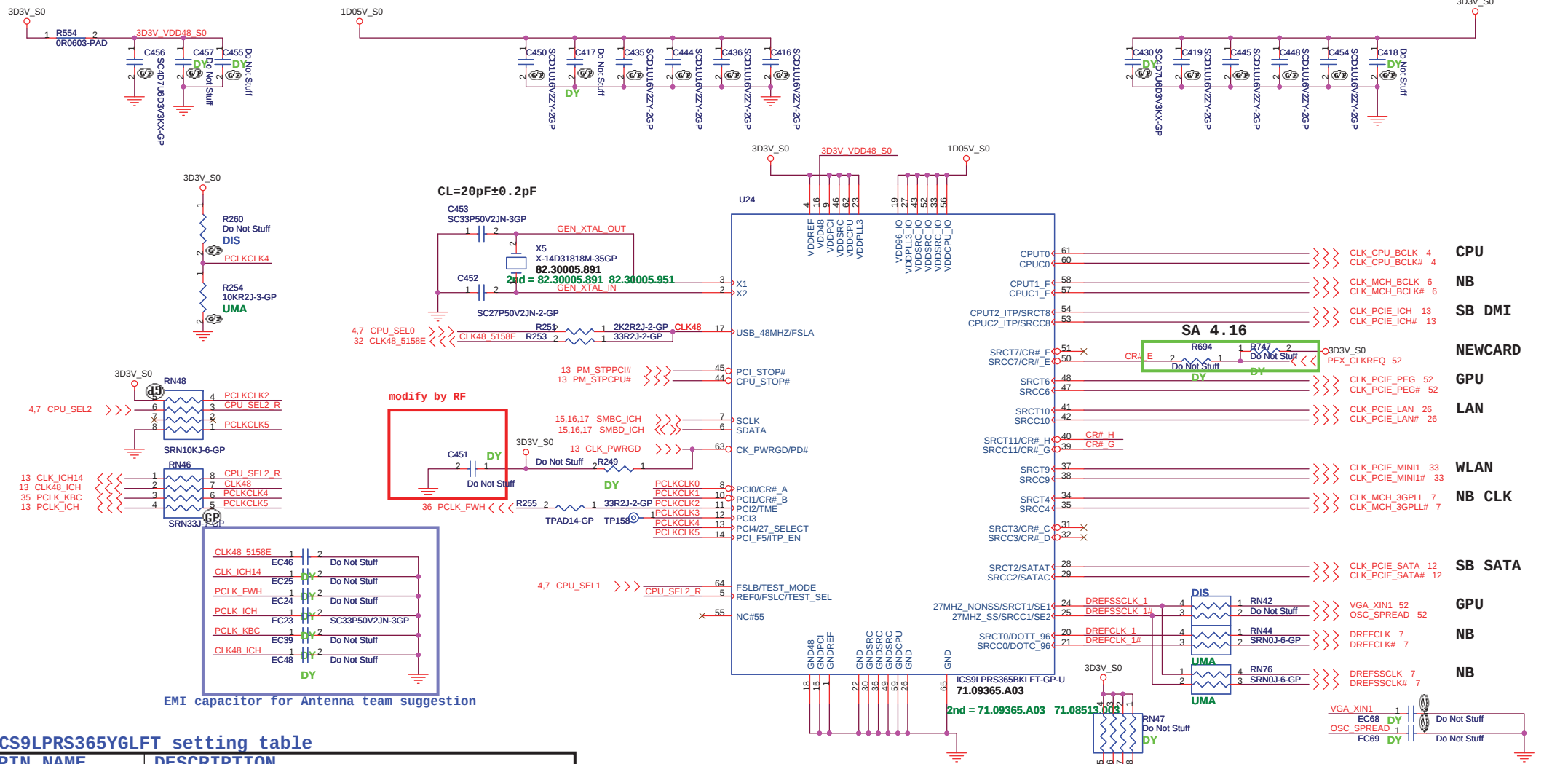
TOP	L1
GND	L2
S	L3
S	L4
GND	L5
BOTTOM	L6

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/GPIO53	PCIe config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#:SPI_CS1#/GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resistor.

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55, 53, 51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) 1=The iTPM Host Interface is disabled(default)
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality 1 = TLS cipher suite with confidentiality (default)
CFG9	PCIe Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG10	PCIe Loopback enable	0 = Enable (Note 3) 1= Disabled (default)
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) 11 = Disabled (default)
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG19	DMI Lane Reversal	0 = Normal operation(Default): Lane Numbered in Order 1 = Reverse Lanes x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display Port or PCIe is operational (Default). 1 = Digital display Port and PCIe are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 =No SDVO Card Present (Default) 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	0 = LFP Disabled (Default) 1= LFP Card Present; PCIe disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG12/CFG13 straps can be enabled at any time.



ICS9LPRS365YGLFT setting table

PIN	NAME	DESCRIPTION
PCI0/CR#_A		Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR# A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR# A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B		Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR# B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR# B controls SRC1 pair (default) 1= CR# B controls SRC4 pair
PCI2/TME		0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3		
PCI4/27M_SEL		0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN		0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C		Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR# C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR# C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, Bit 1 0 = SRC3 enabled (default) 1= CR# D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7 enabled (default) 1= CR# F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR# F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

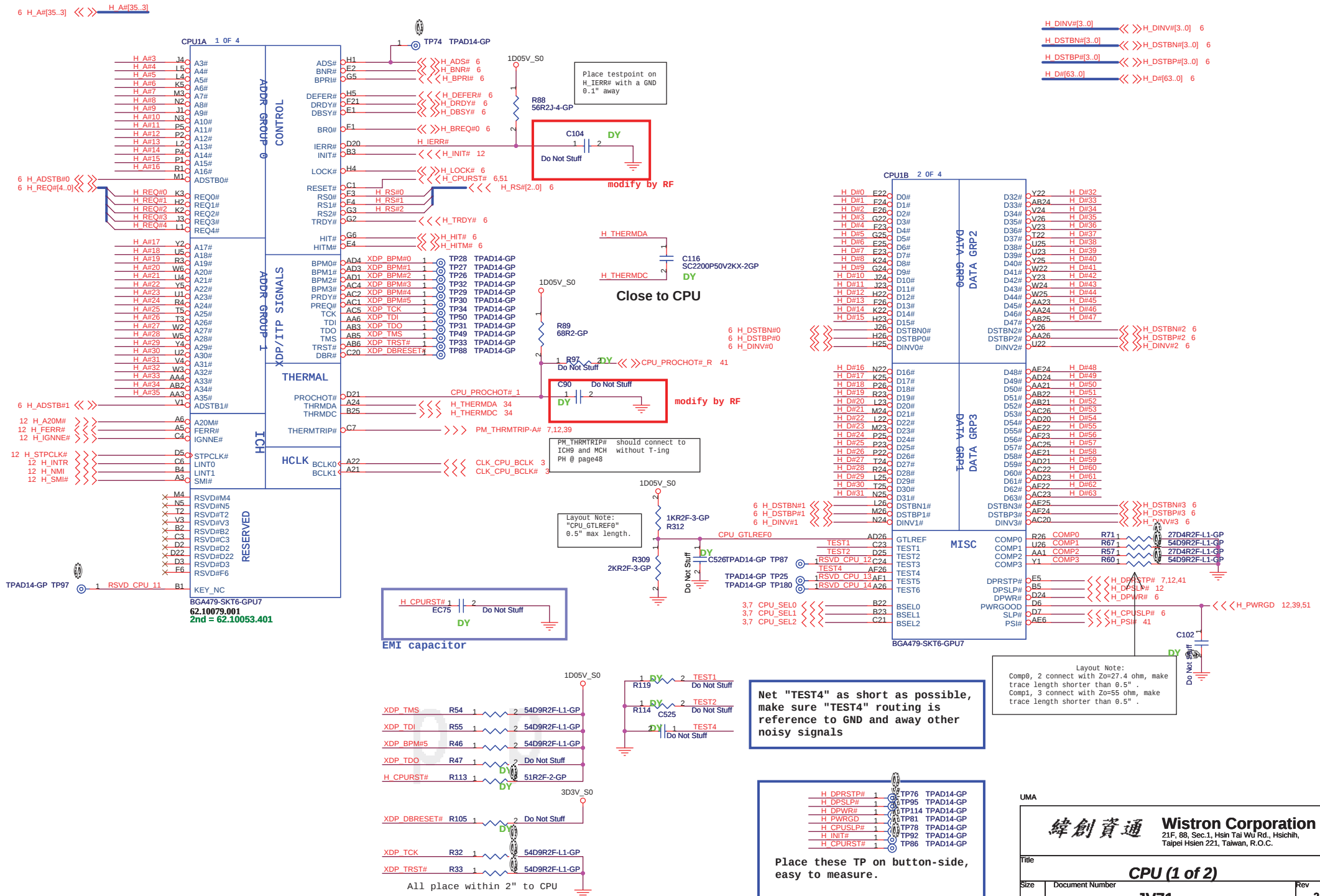
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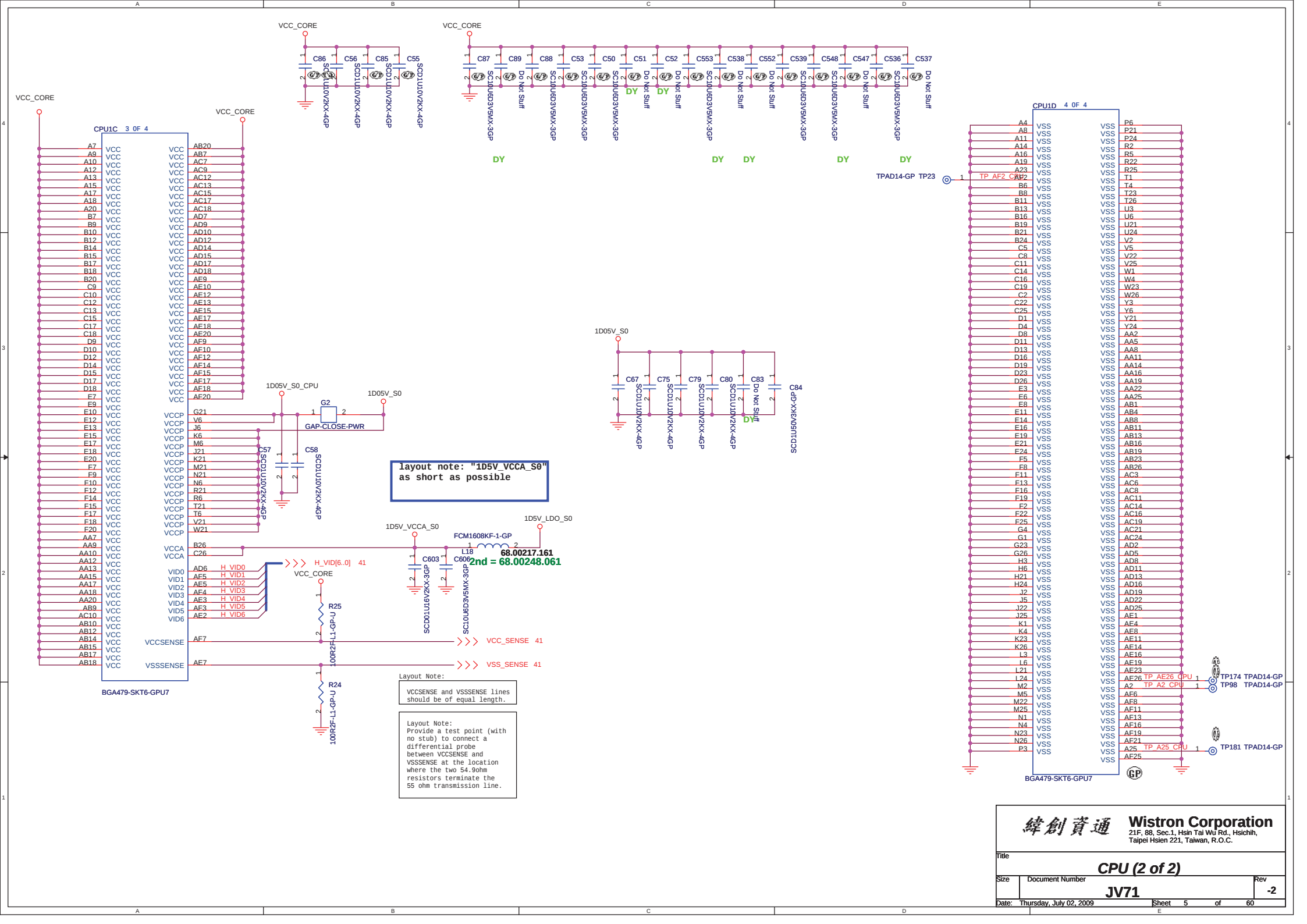
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Title: **Clock Generator**

Size: Document Number **JV71** Rev **-2**

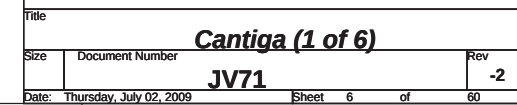
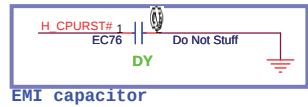
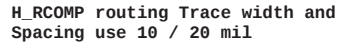
Date: Thursday, July 02, 2009 Sheet 3 of 60

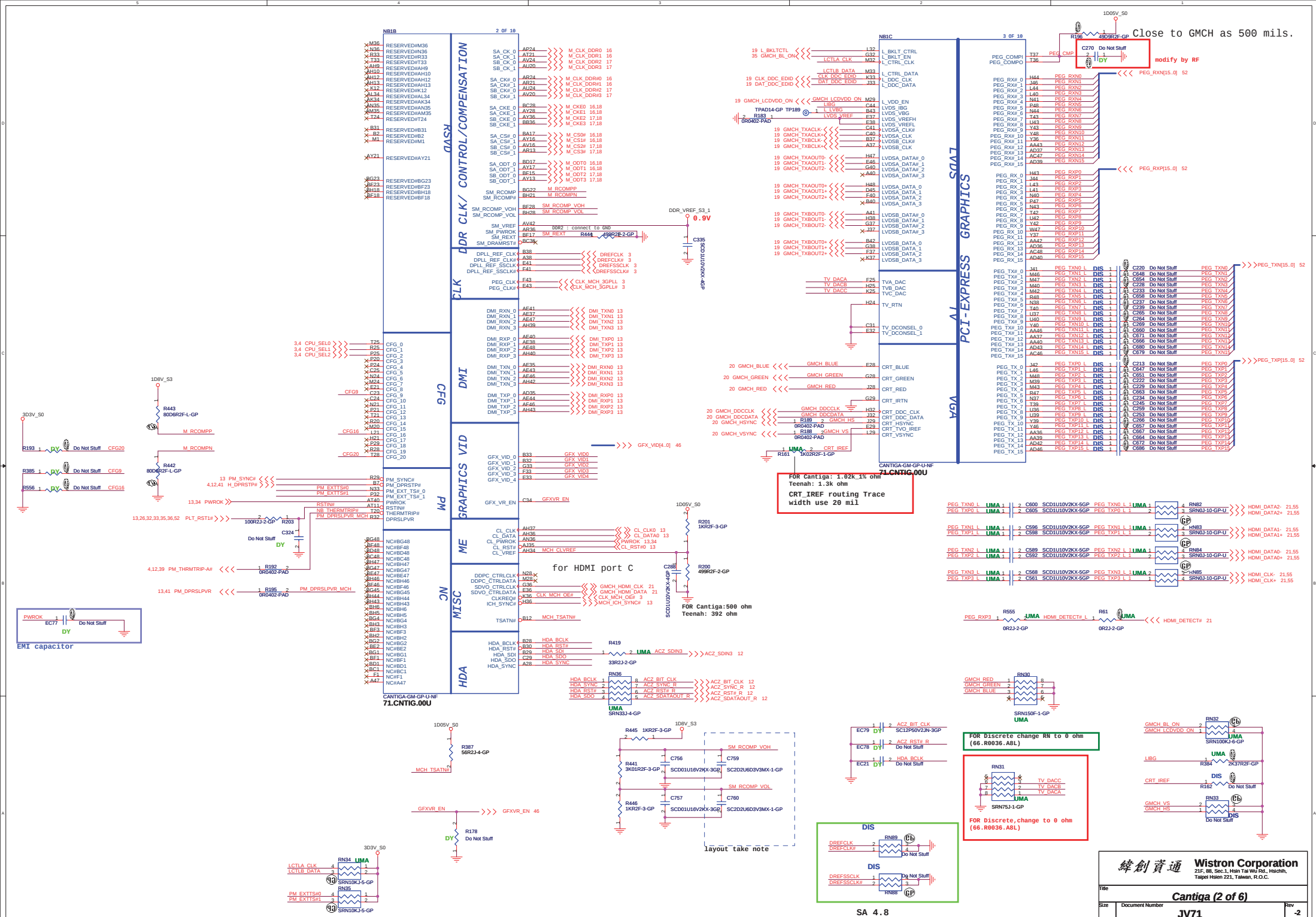


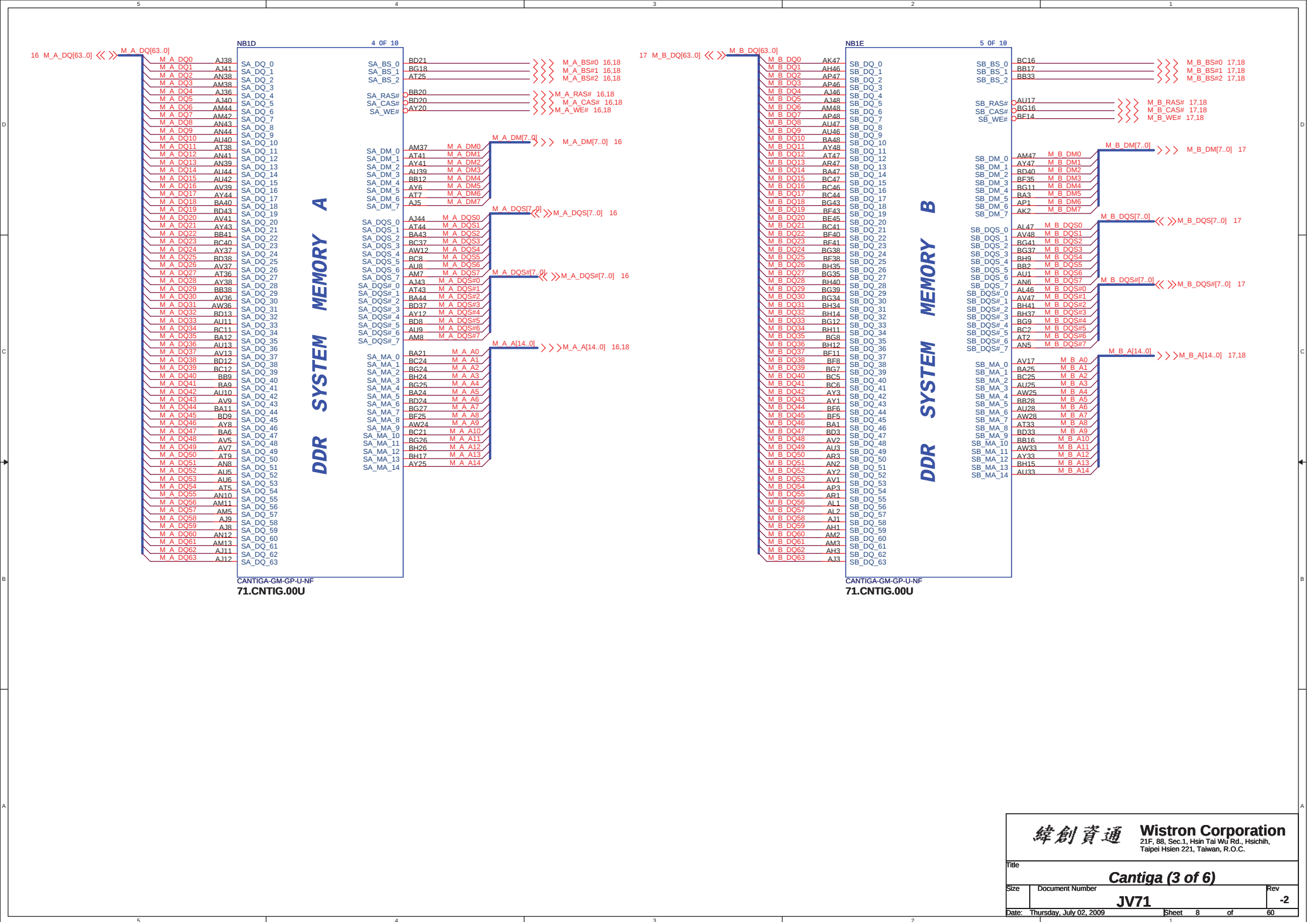


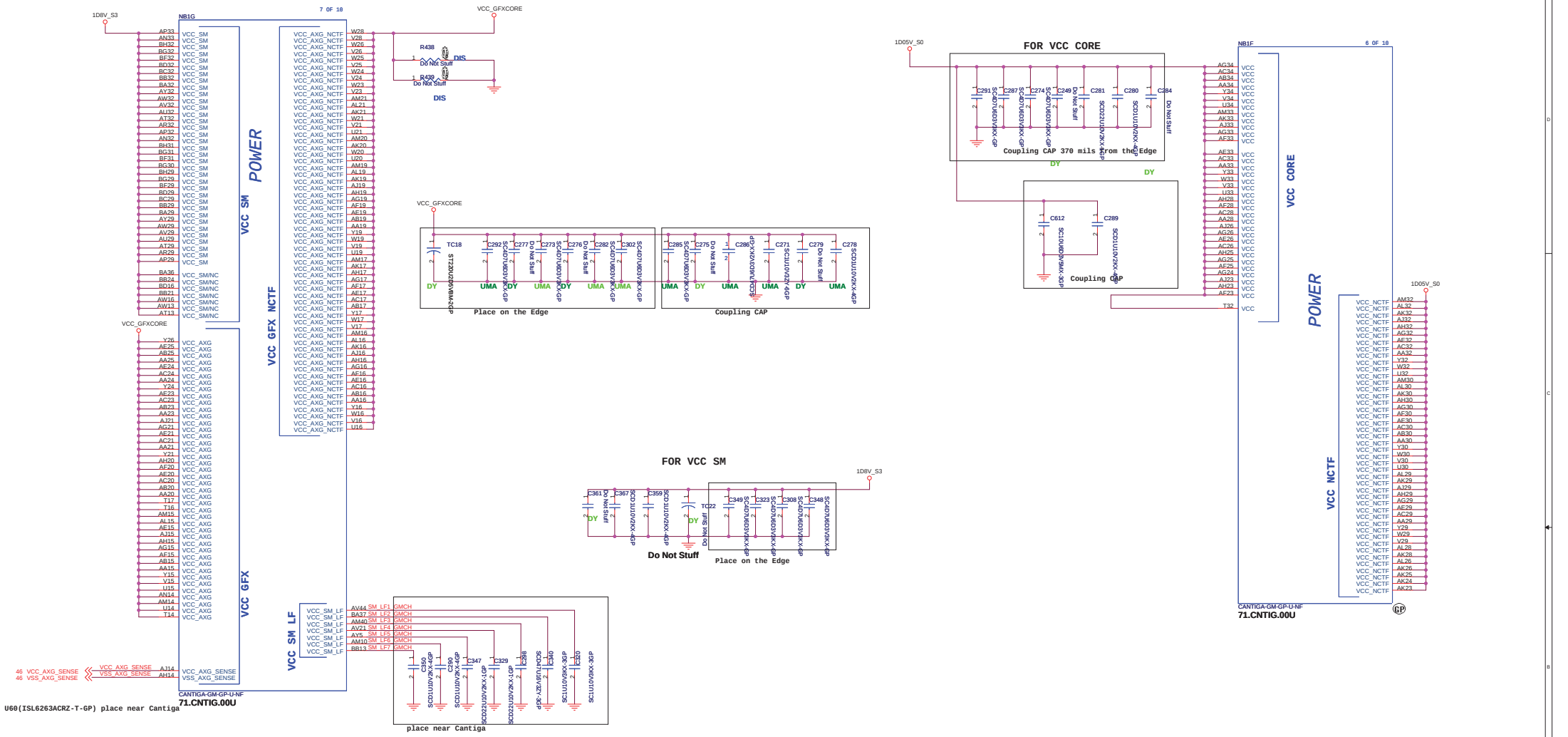
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

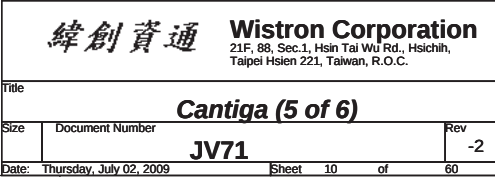
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)

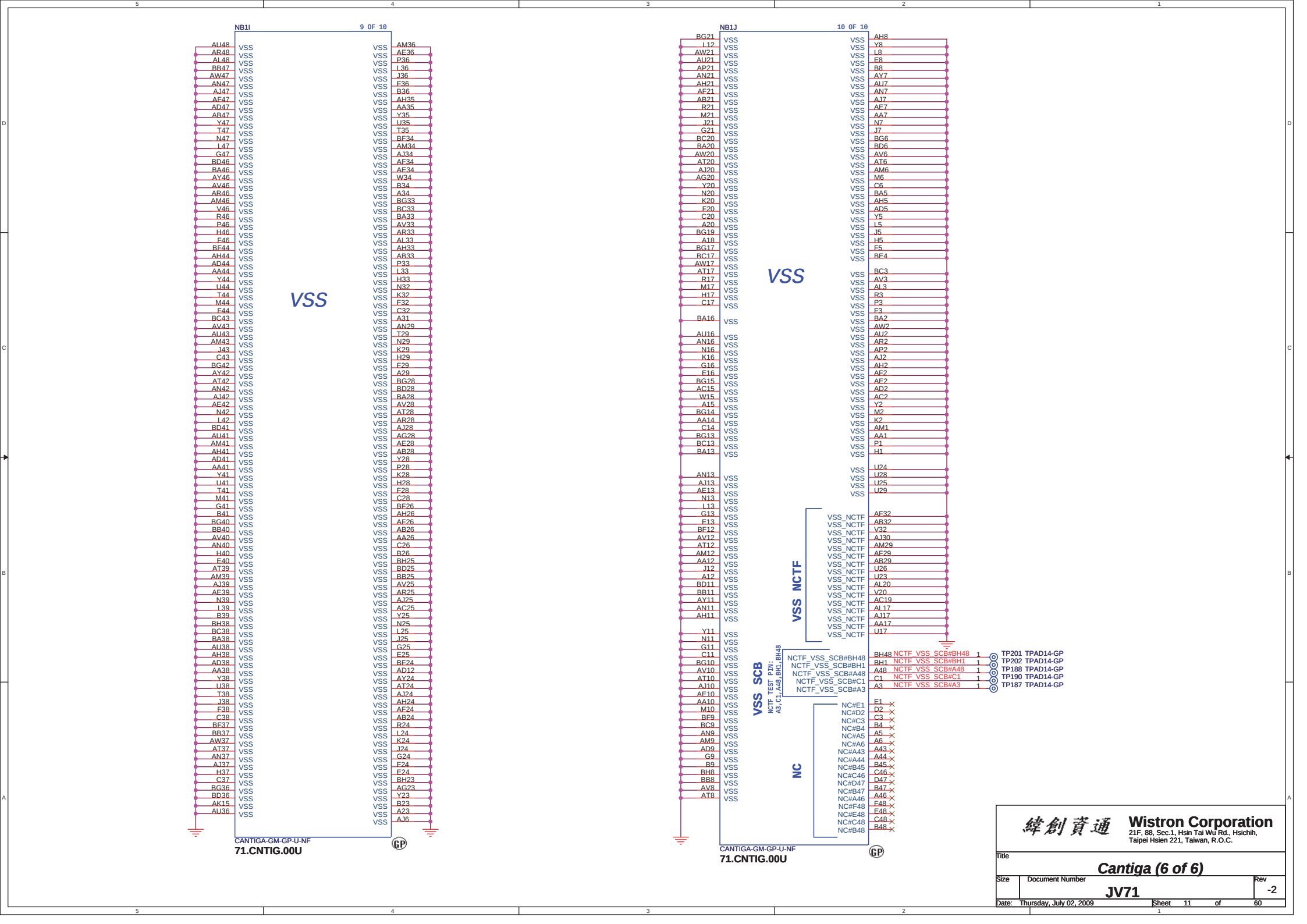
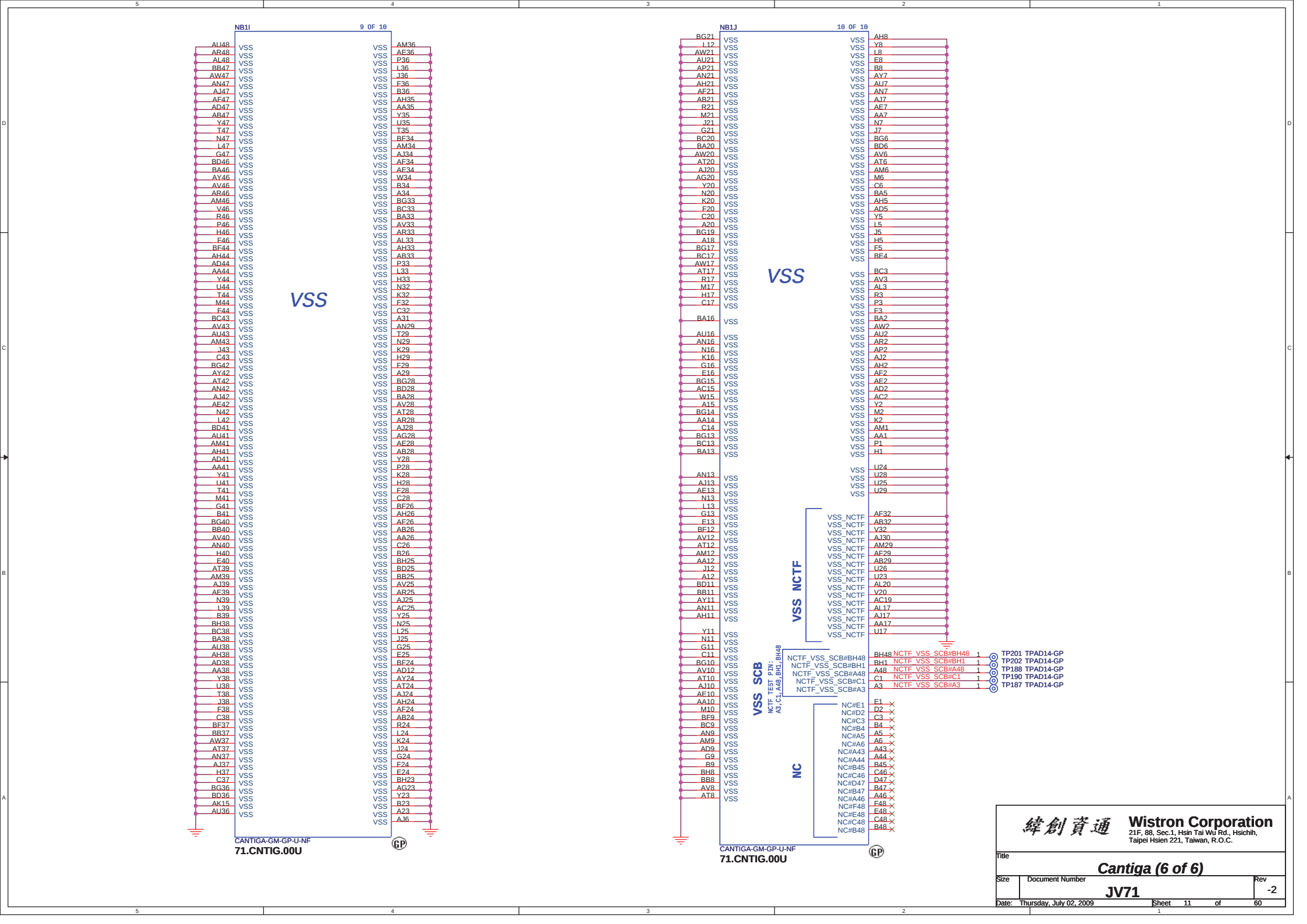


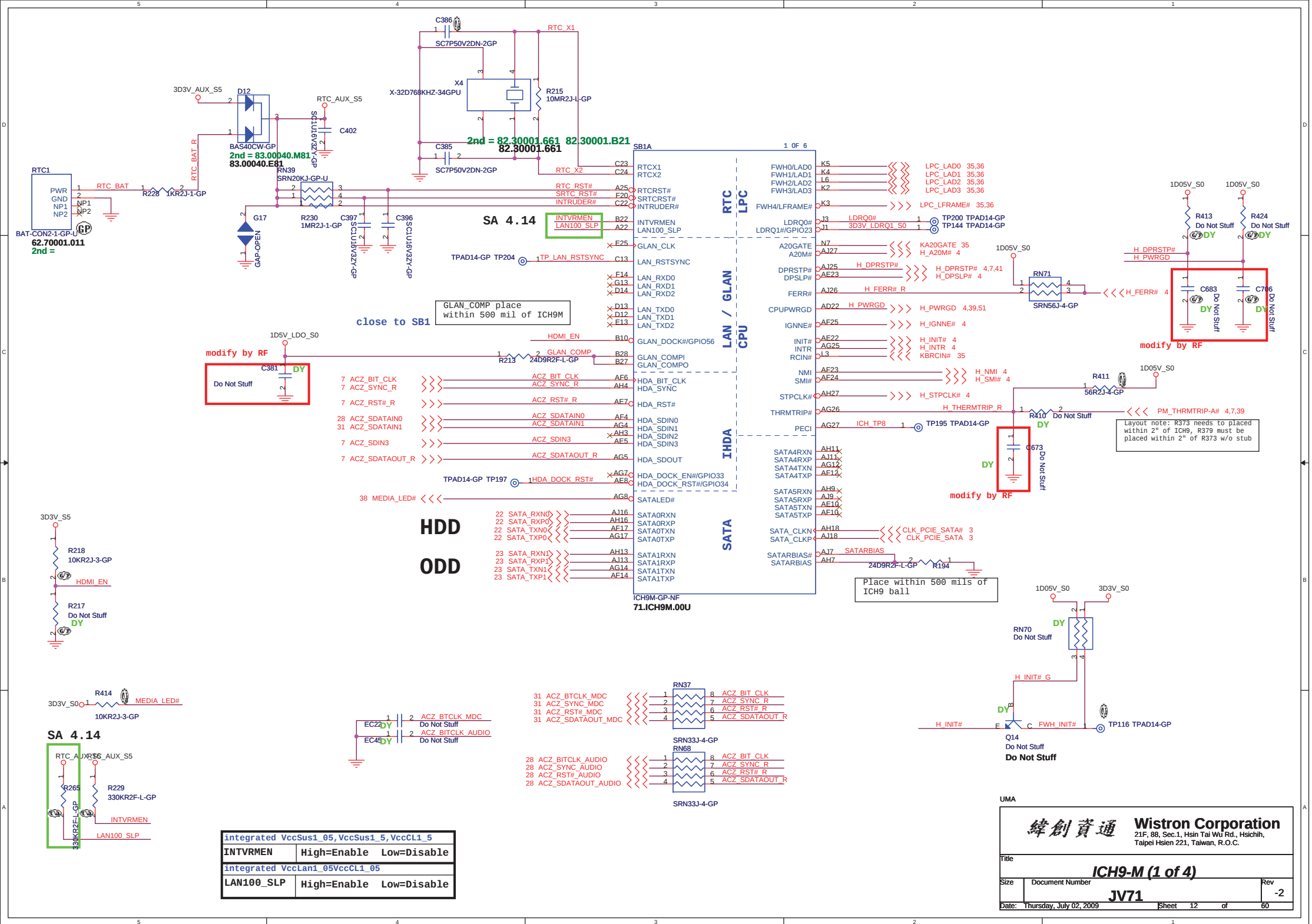










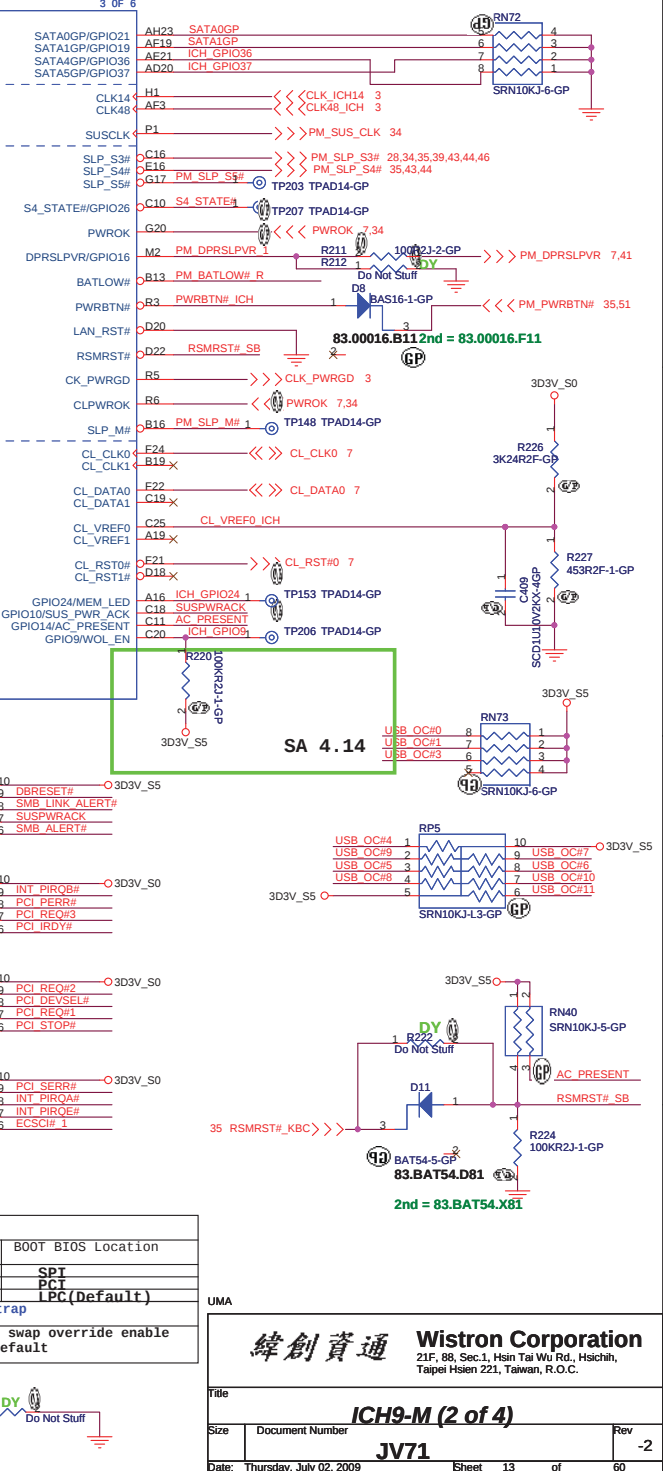
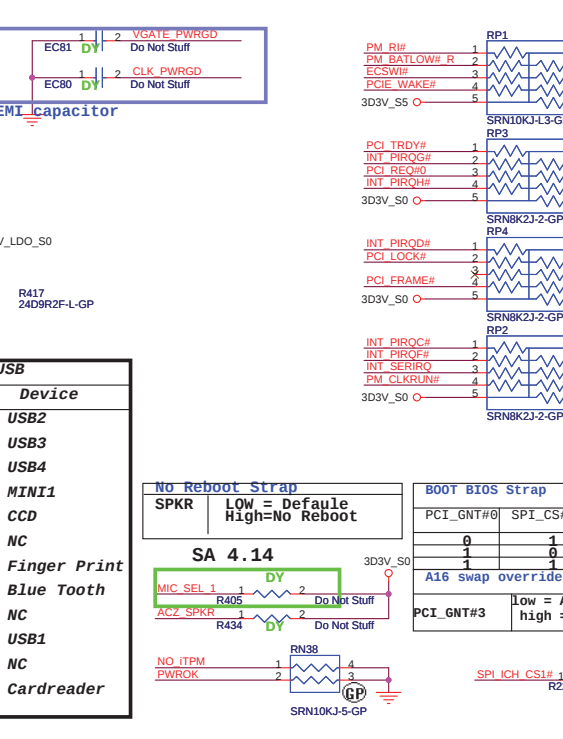
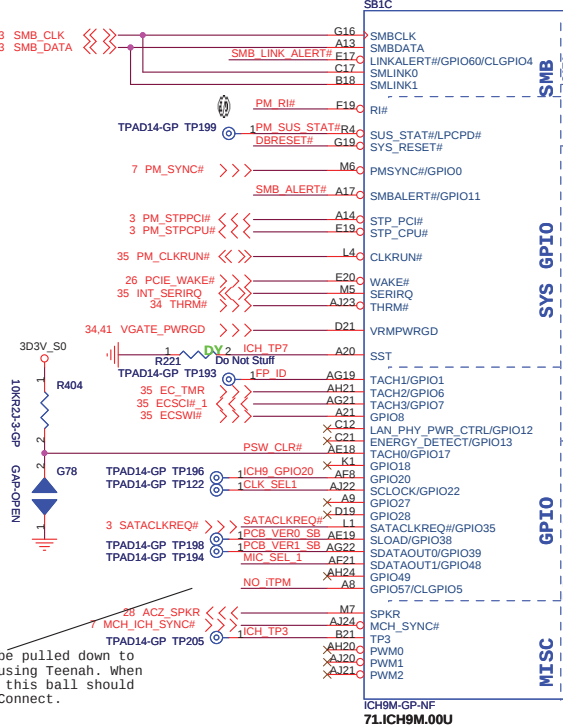
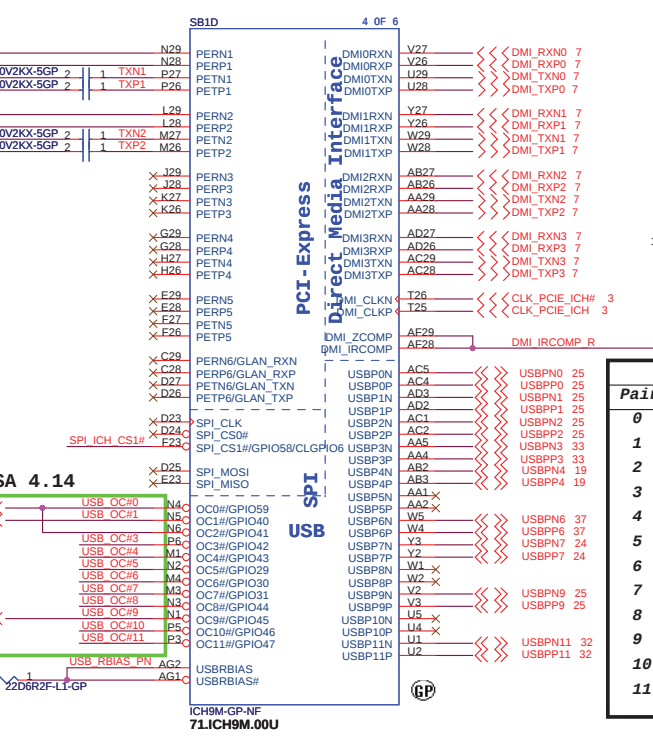
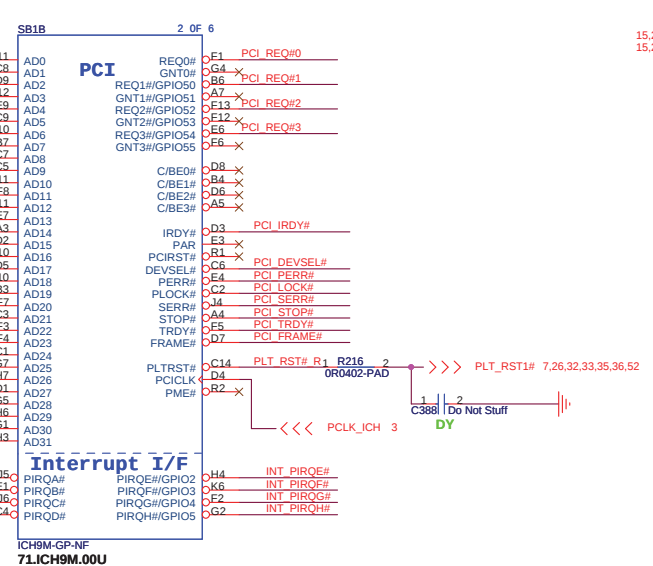


PCI_GNT#0 and SPI_CS1#
have weak internal Pull up

LAN
MINICARD1

These R need close SB
within 600 mils

5



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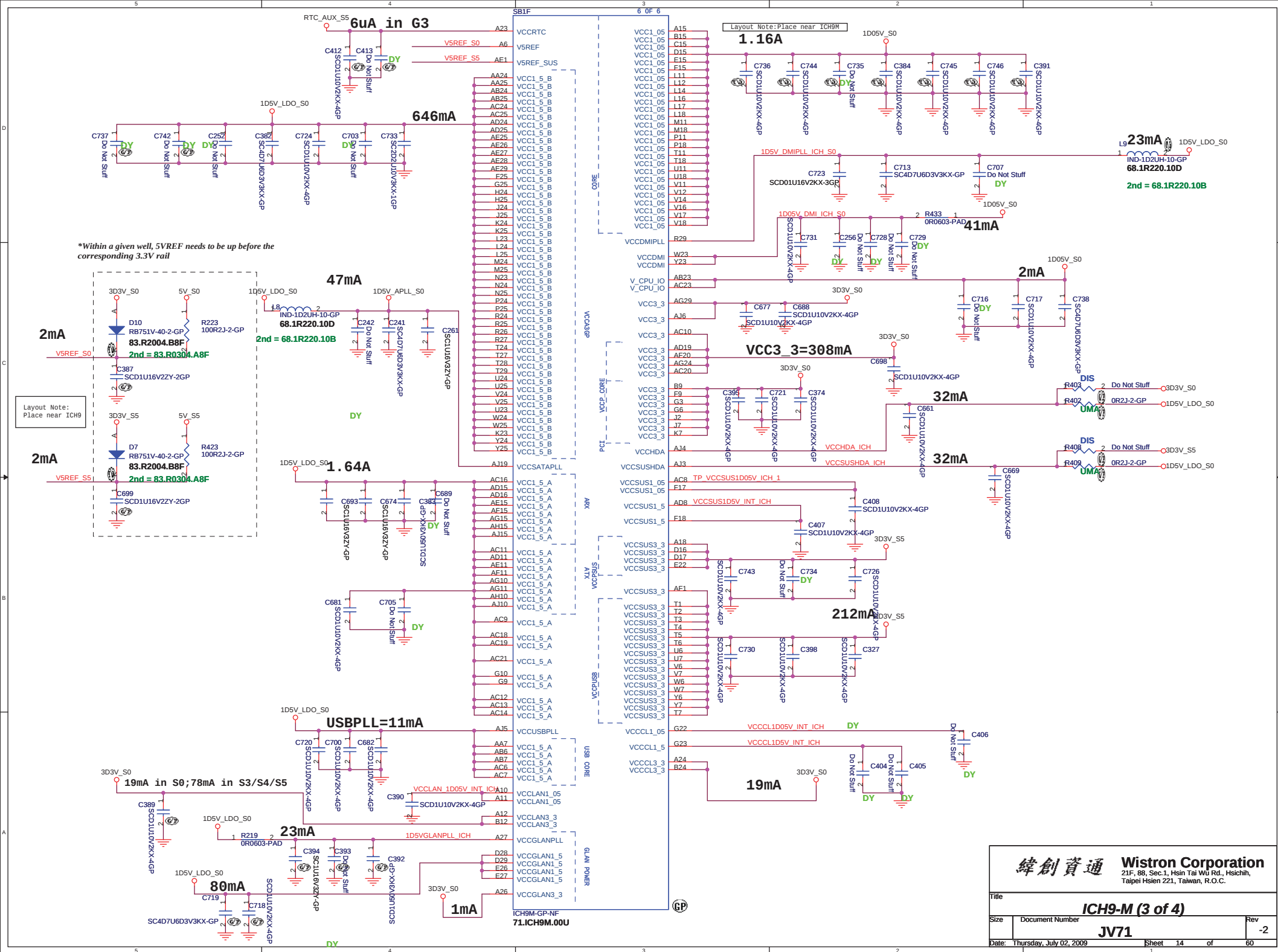
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ICH9-M (2 of 4)

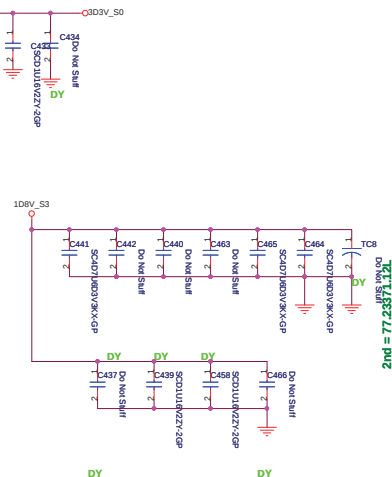
JV71

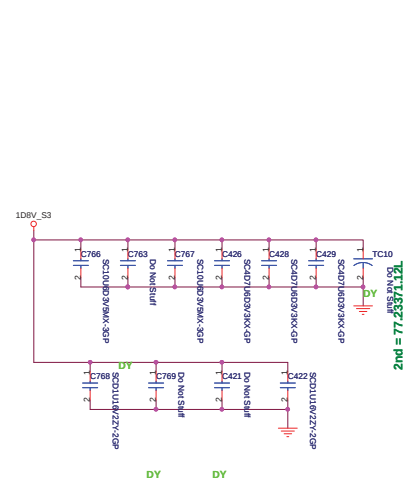
Rev -2

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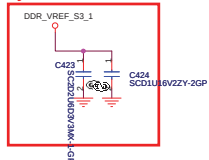




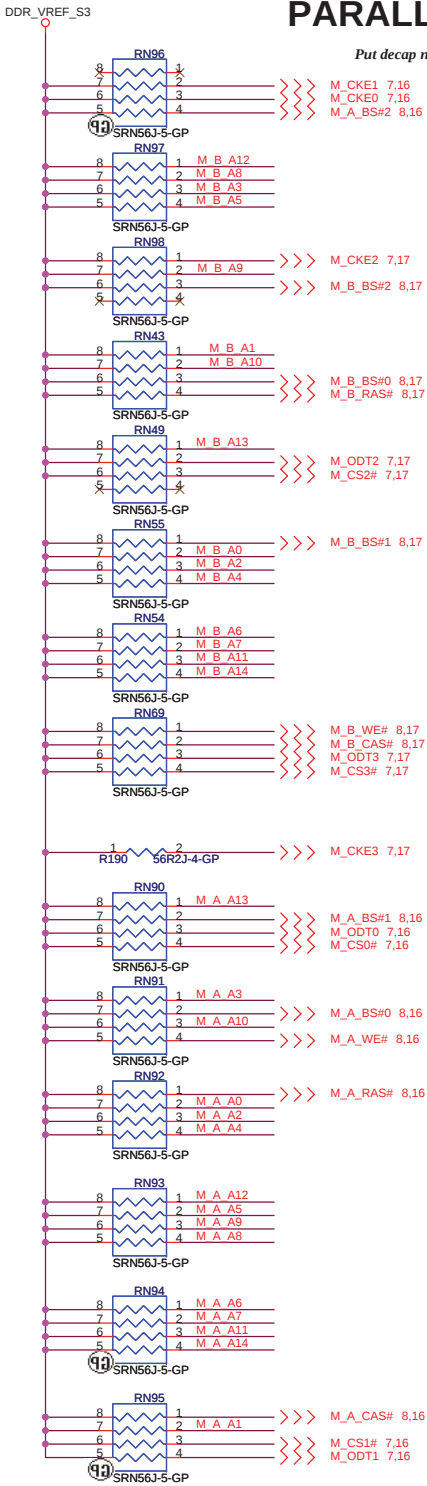




Layout Note : Near Pin 1

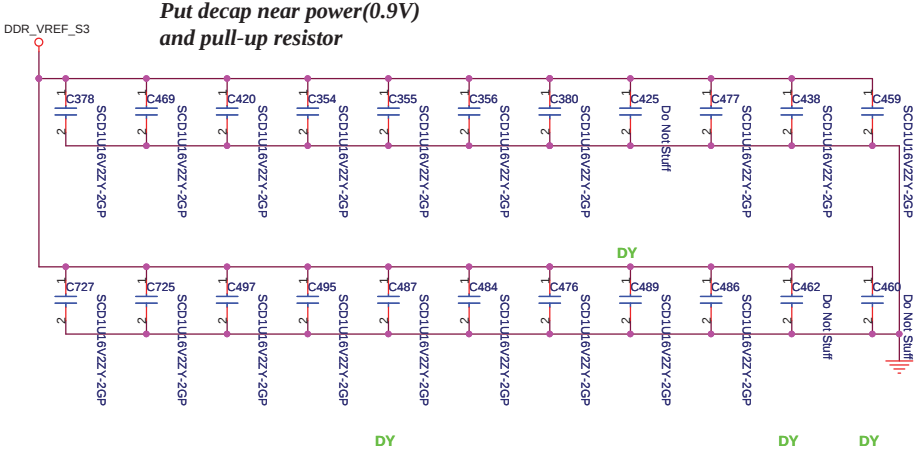


PARALLEL TERMINATION

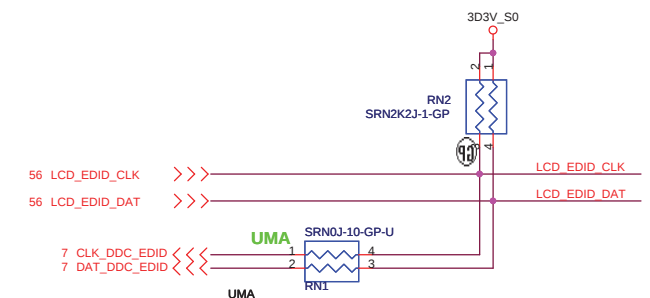
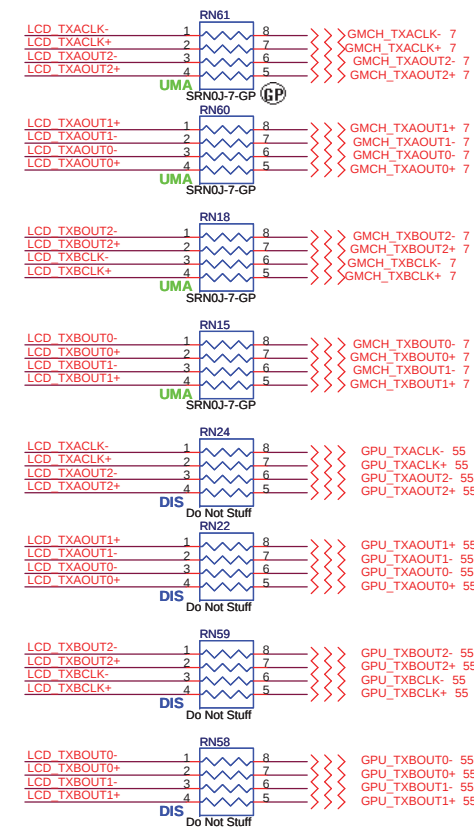
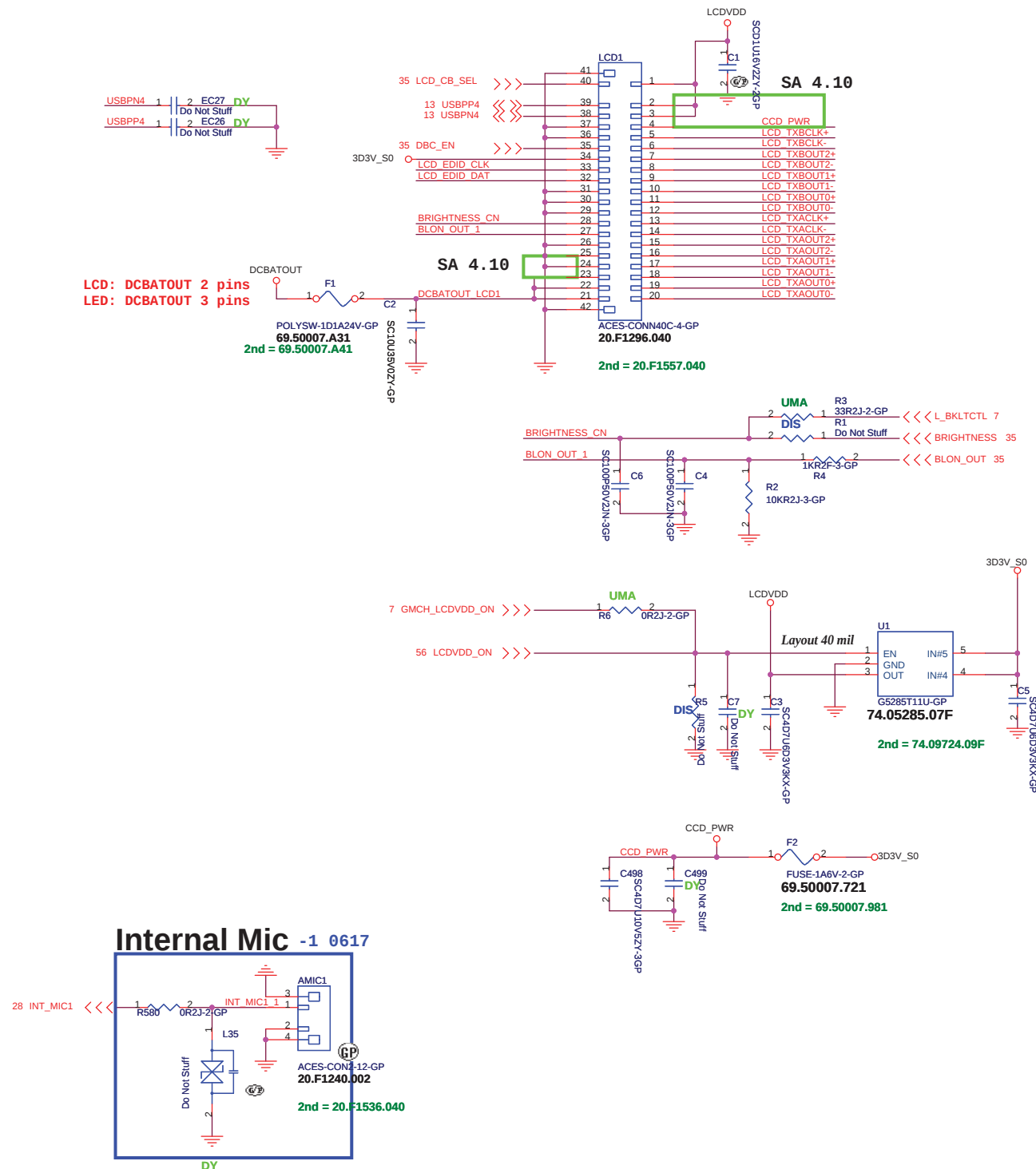


M_A A[14..0] >>> M_A A[14..0] 8,16
M_B A[14..0] >>> M_B A[14..0] 8,17

Decoupling Capacitor



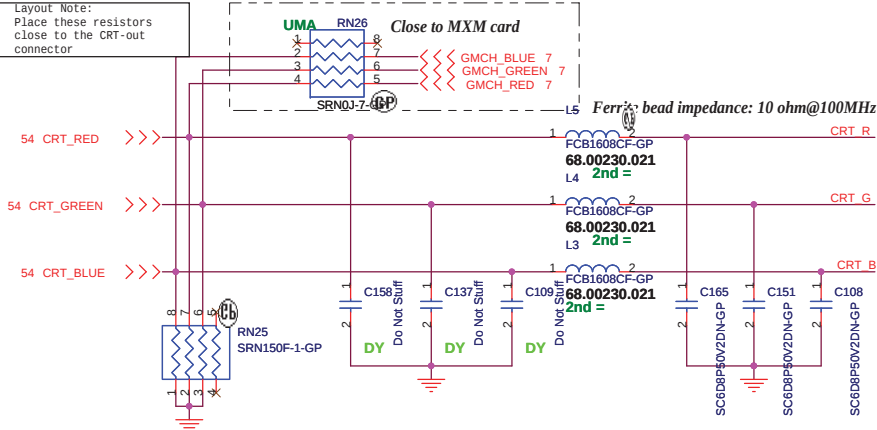
LCD/INVERTER/CCD CONN



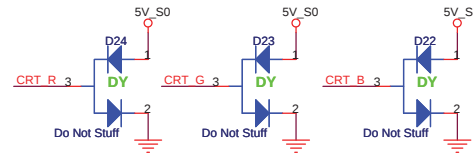
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Title			LCD CONN	
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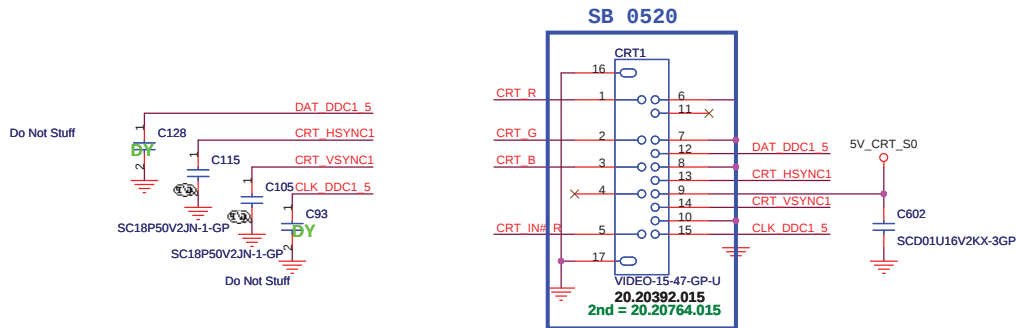
Layout Note:
Place these resistors
close to the CRT-out
connector



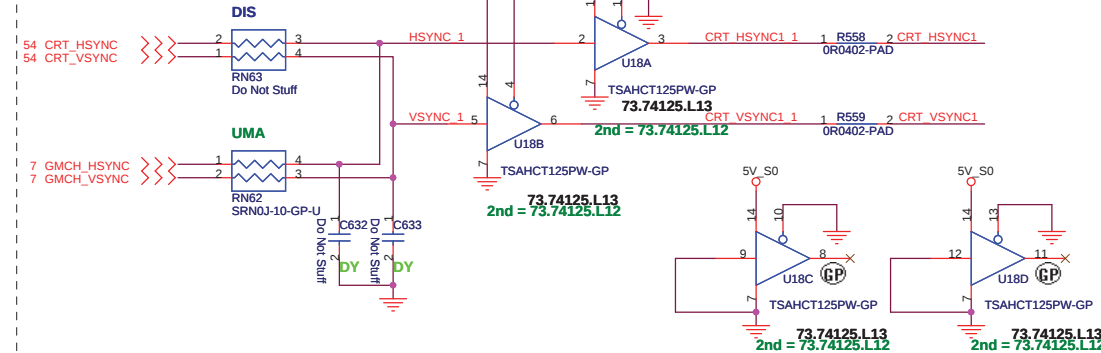
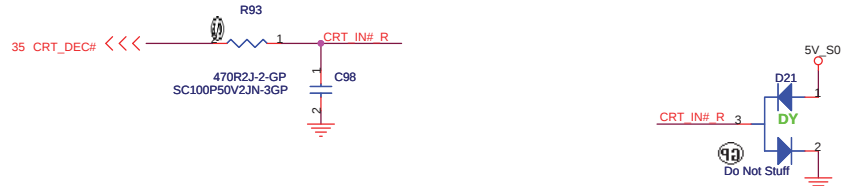
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



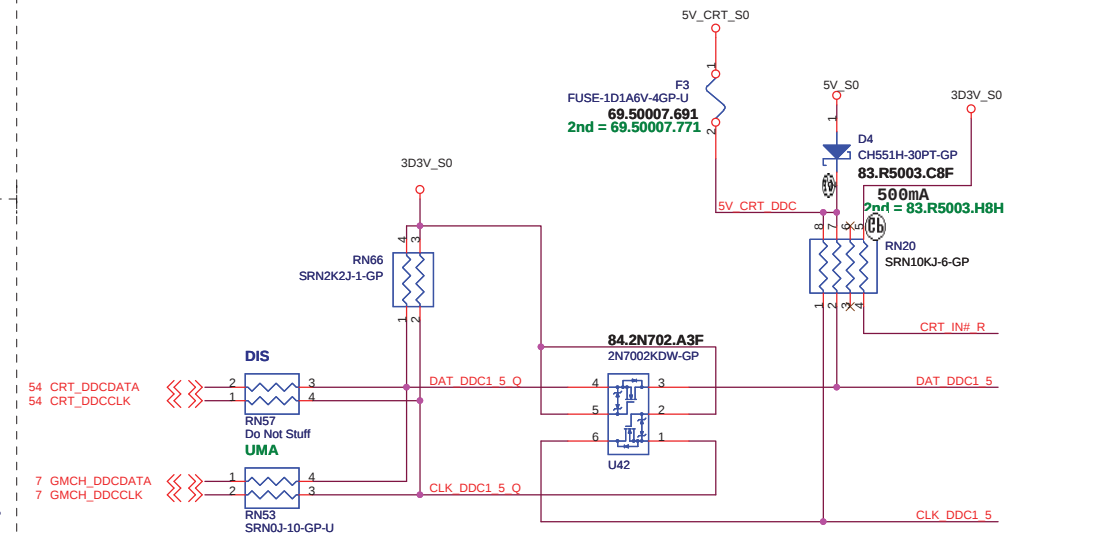
CRT I/F & CONNECTOR



6
1
7
2
8
3
9
4
10
5

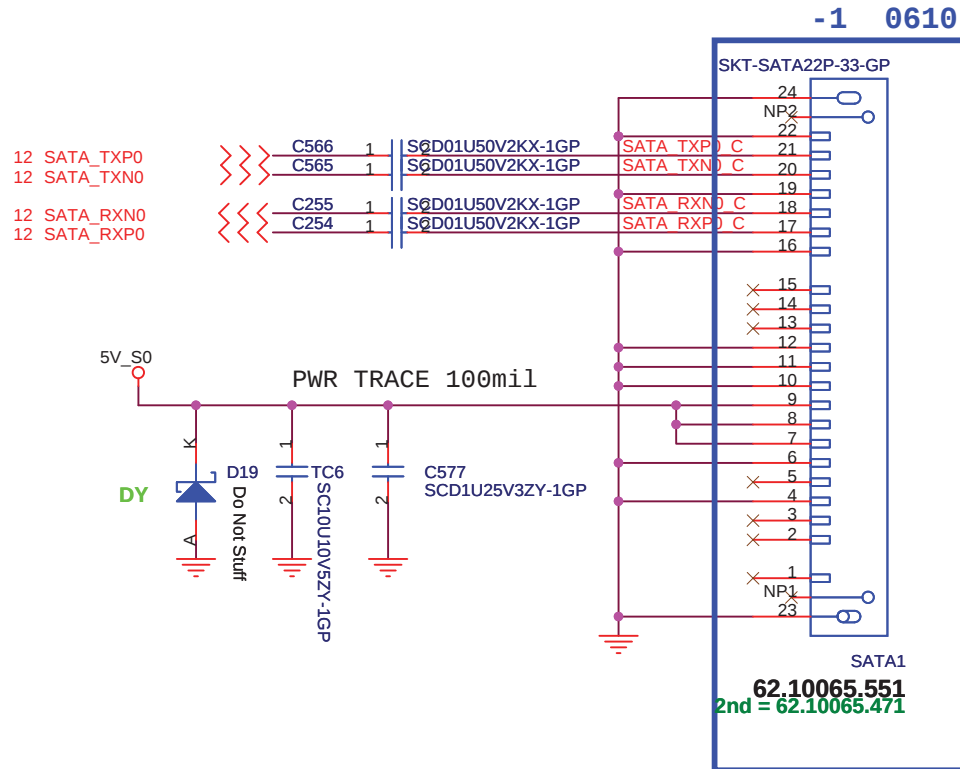


DDC_CLK & DATA level shift





SATA Connector



UMA

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Title

HDD CONN

Size	Document Number
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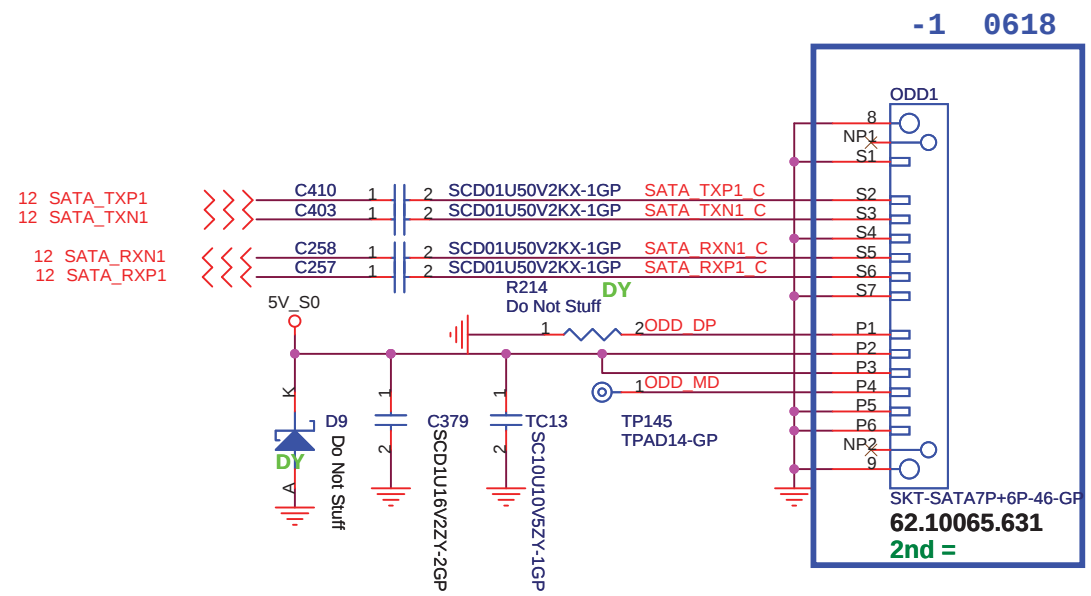
JV71

Rev	-2
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Date: Thursday, July 02, 2009

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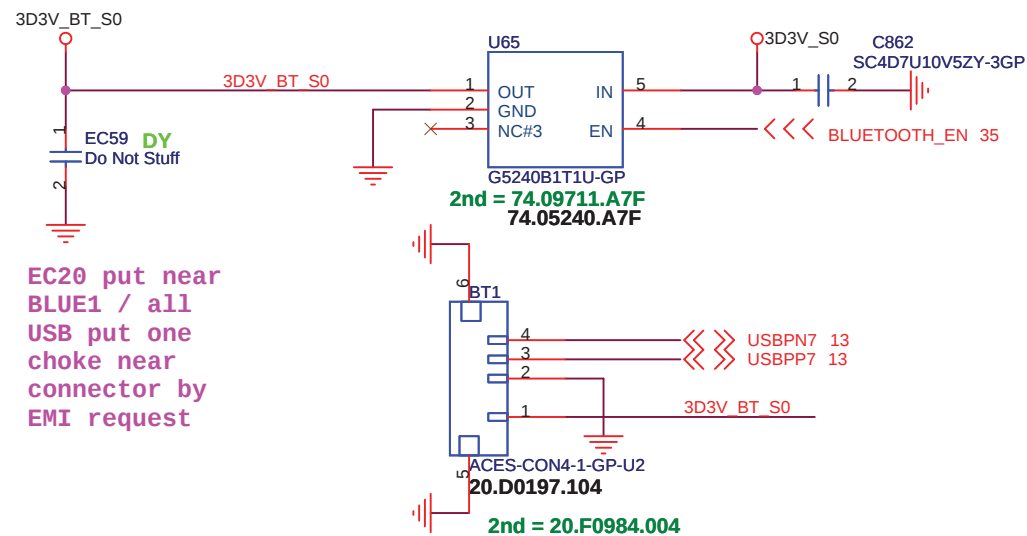
ODD Connector



UMA

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Title			
ODD			
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BLUETOOTH MODULE



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Title

BLUETOOTH

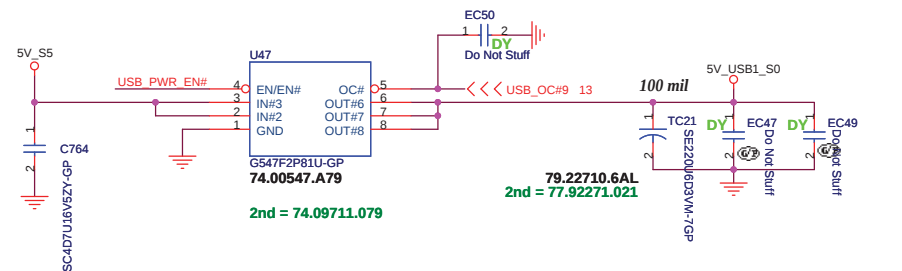
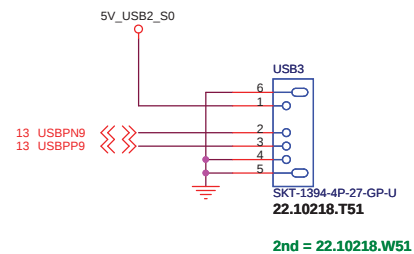
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JV71

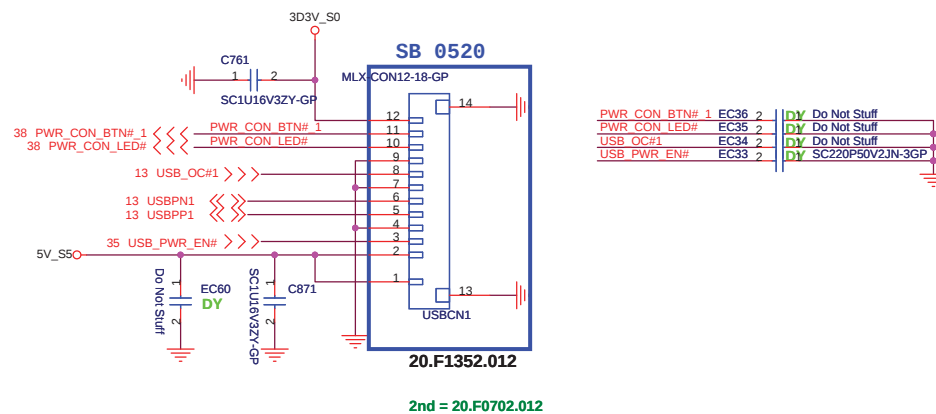
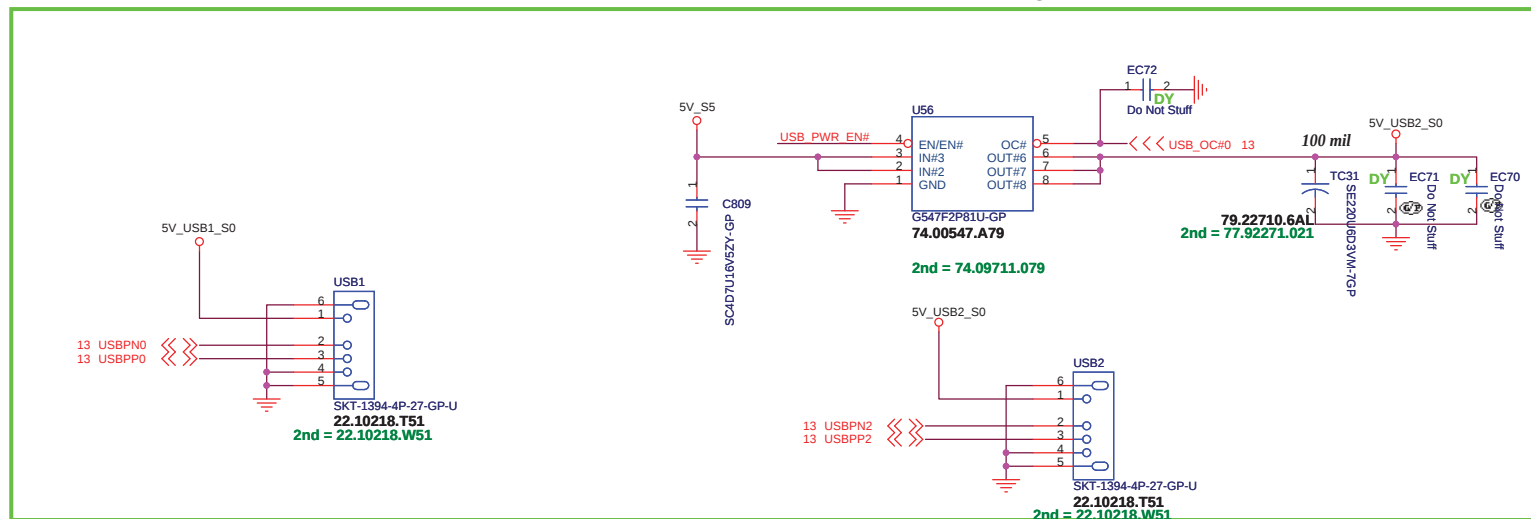
Rev
-2

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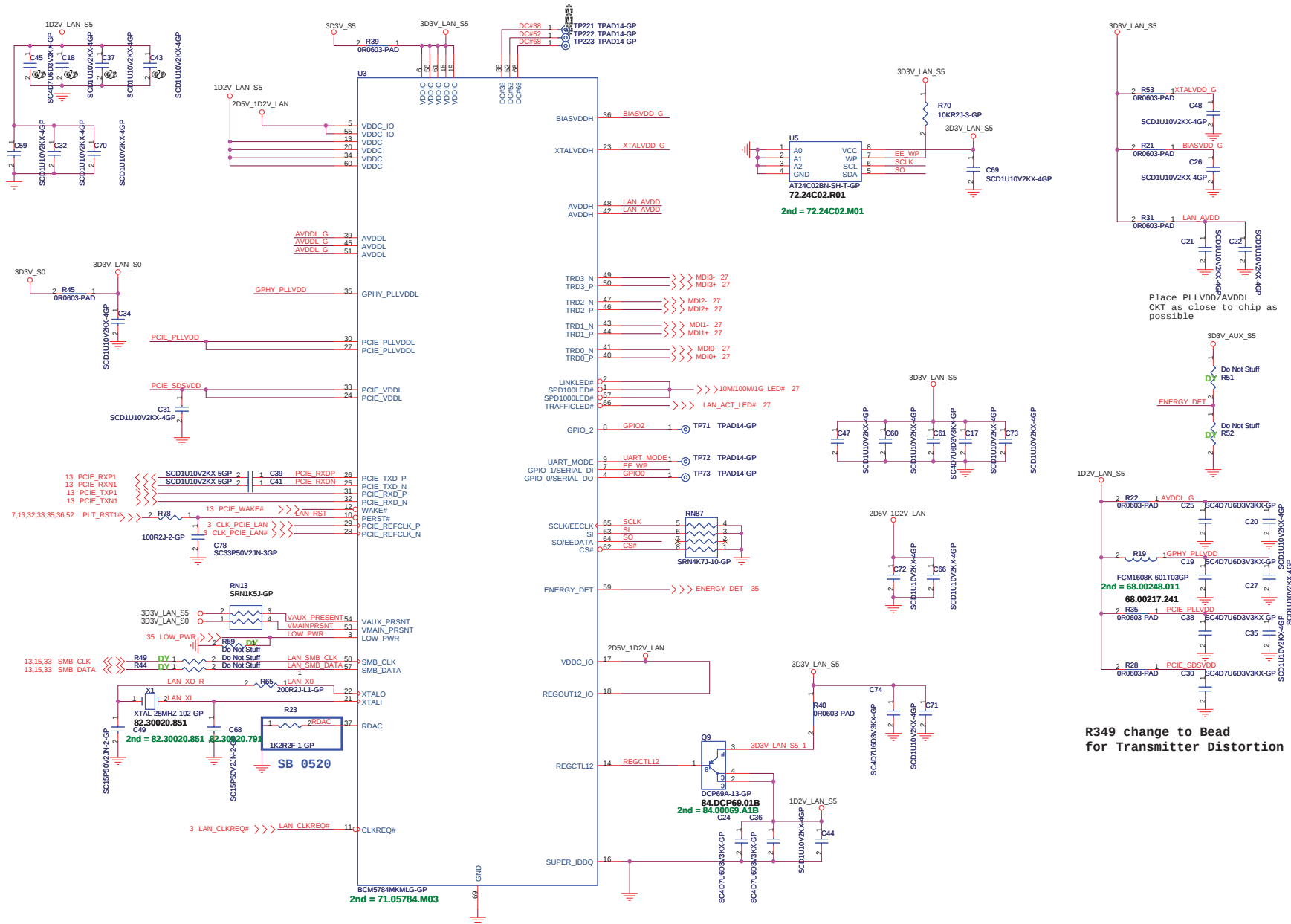


SA 4.14



UMA

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Title USB CONN			
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Place PLLVDD/AVDDL
CKT as close to chip as
possible

R349 change to Bead
for Transmitter Distortion

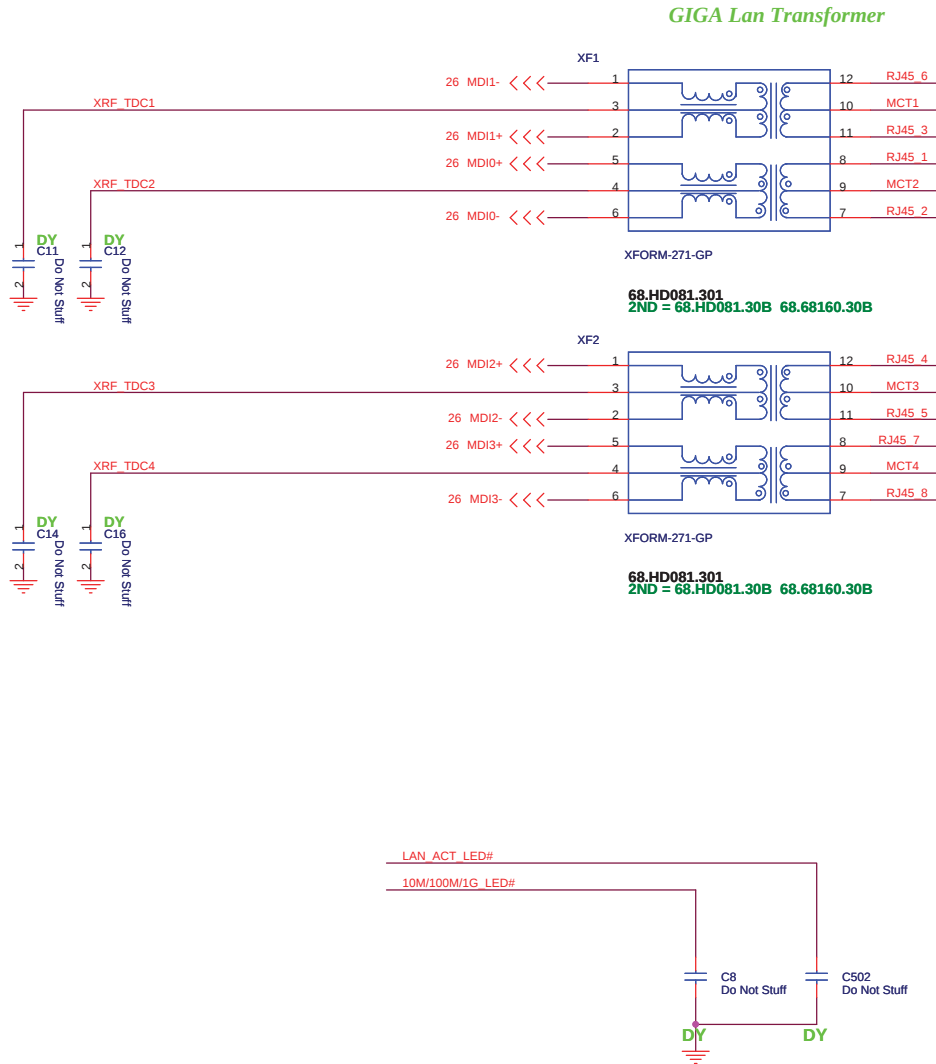
UMA

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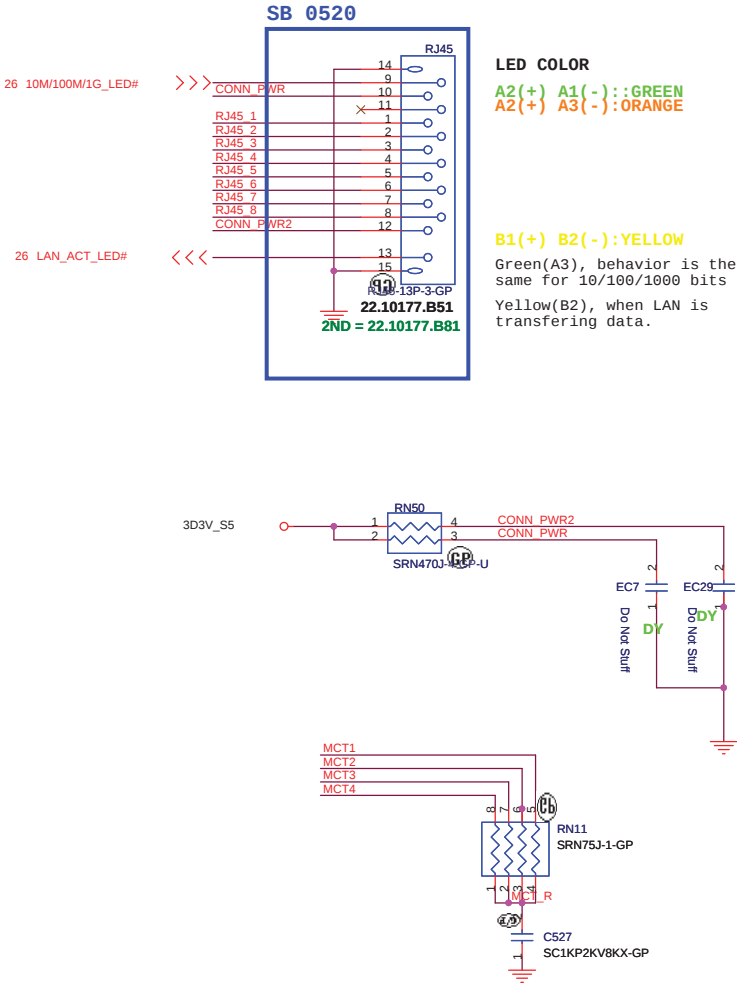
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Size	Document Number	Rev
Custom	JV71	-2
Date: Thursday, July 02, 2009	Sheet 26	of 60

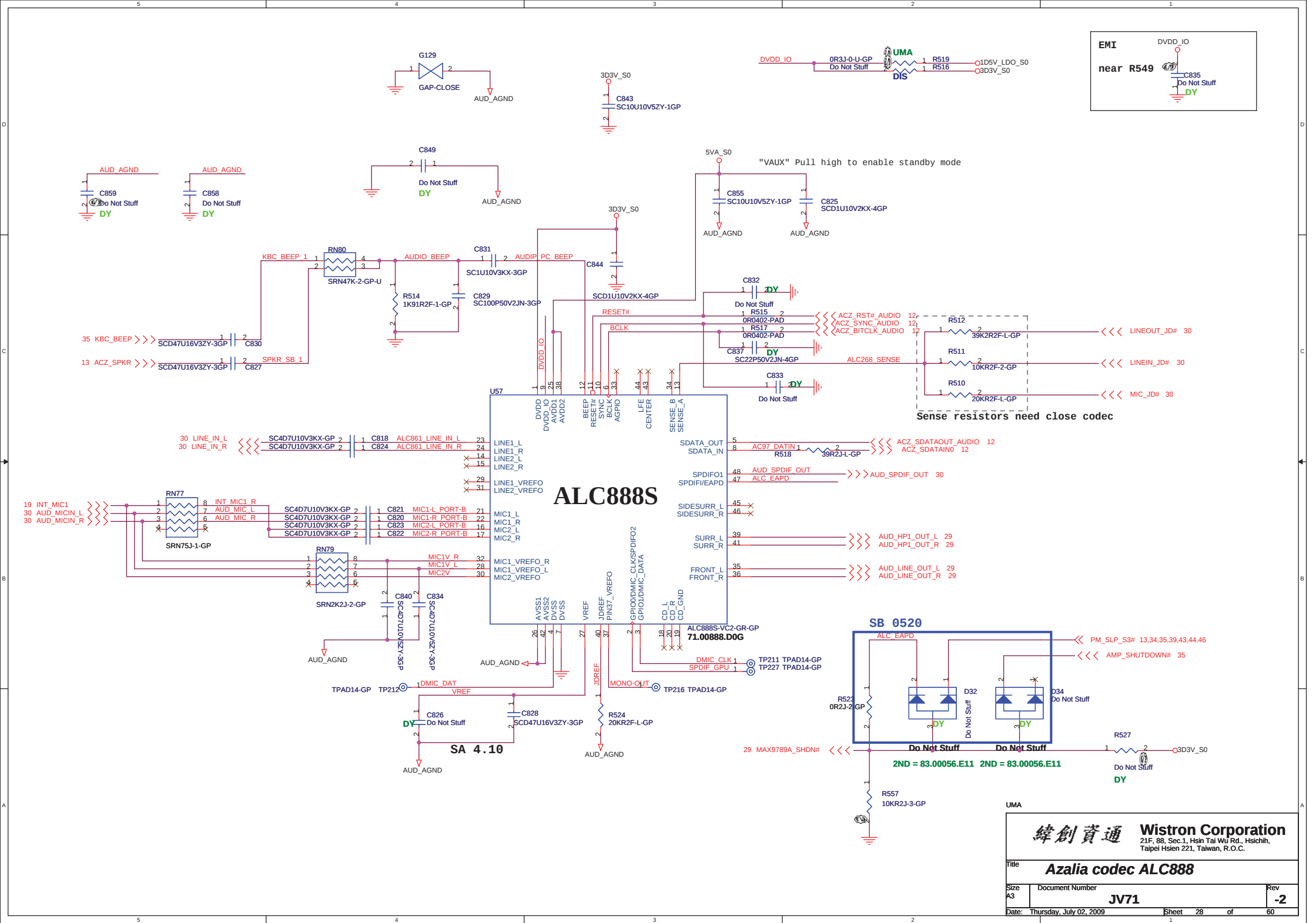
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

LAN Connector

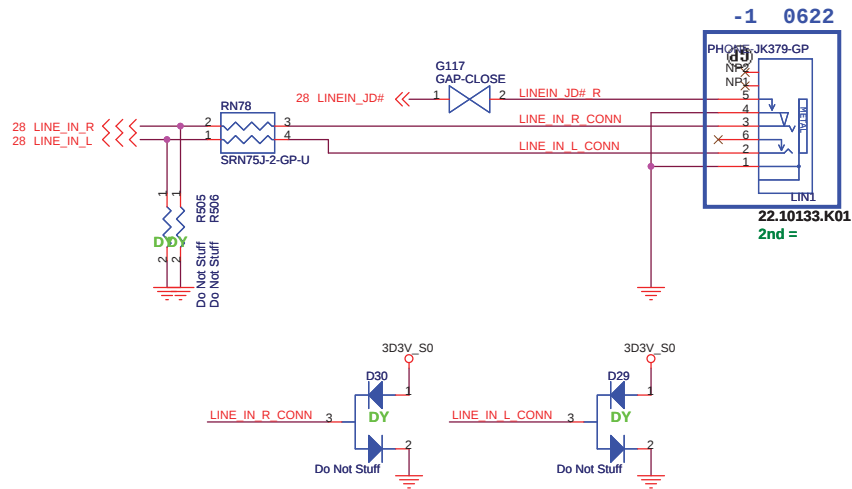


LAN Connector

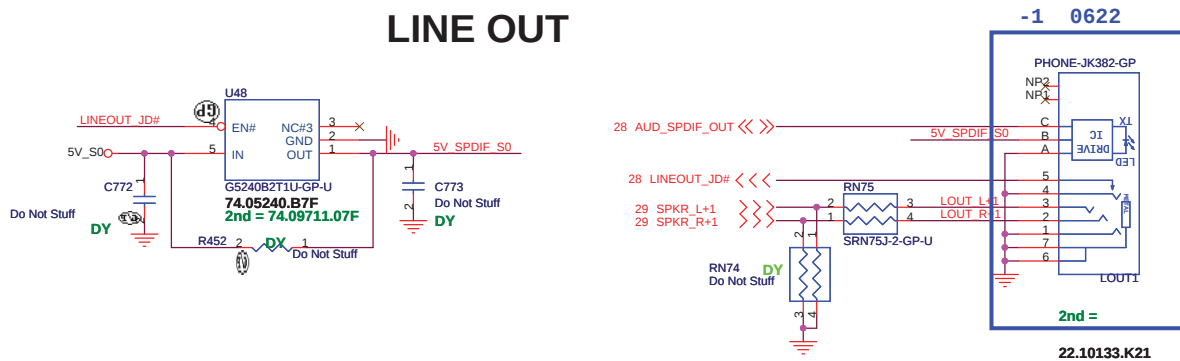




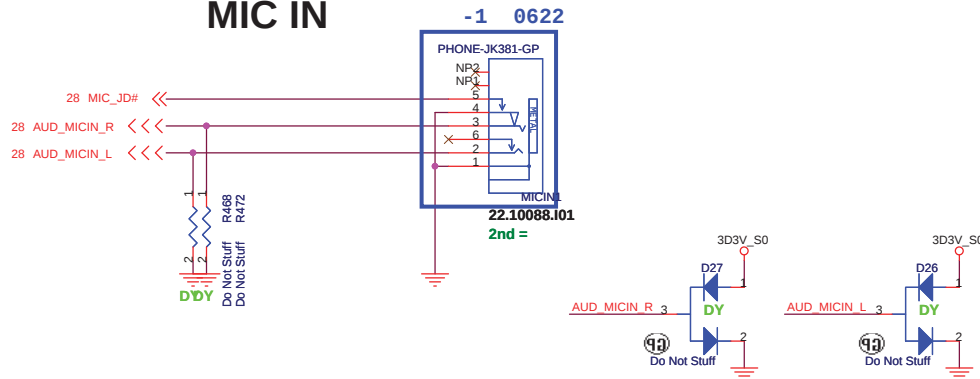
LINE IN



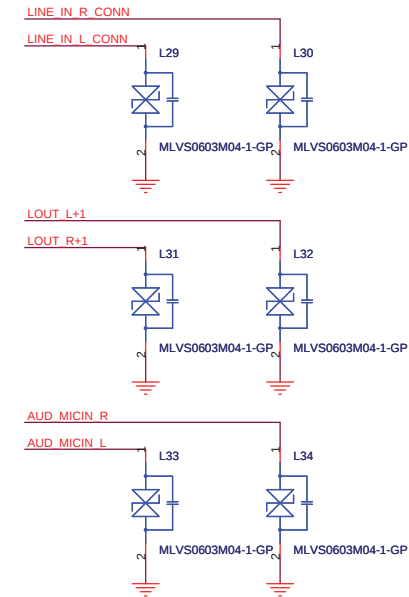
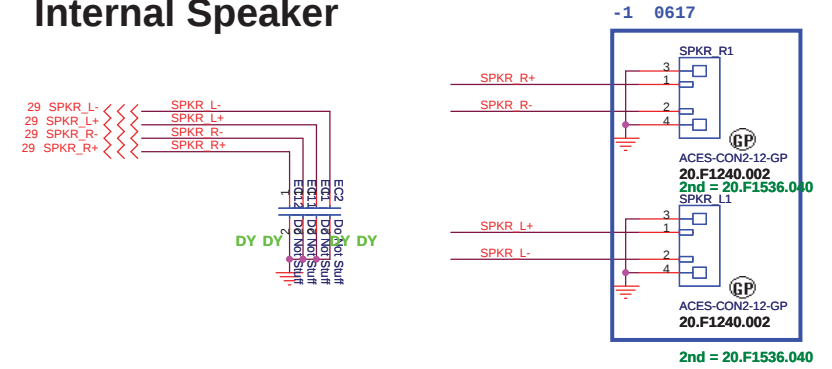
LINE OUT



MIC IN



Internal Speaker

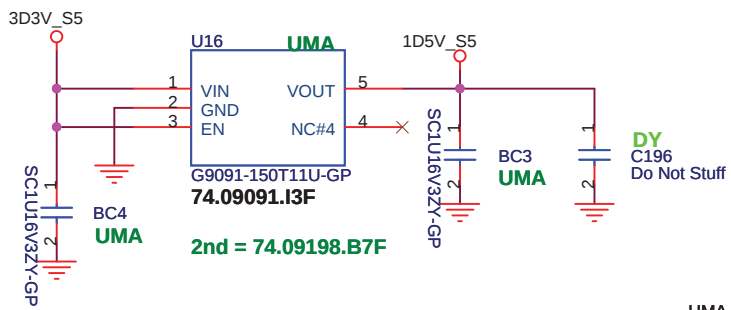
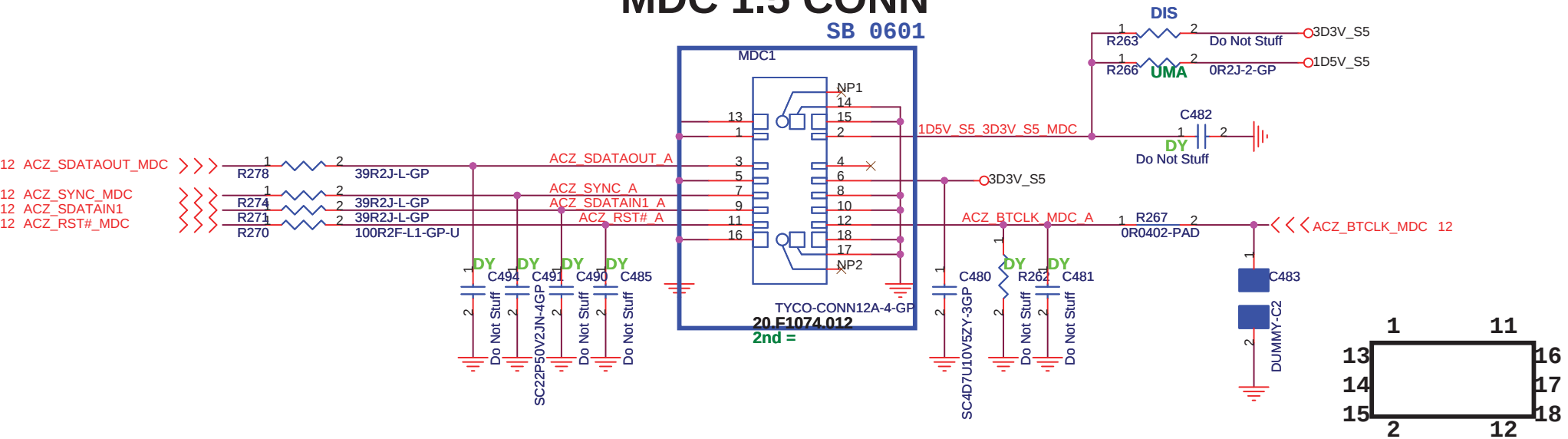


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Title			
AUDIO jack			
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MDC 1.5 CONN

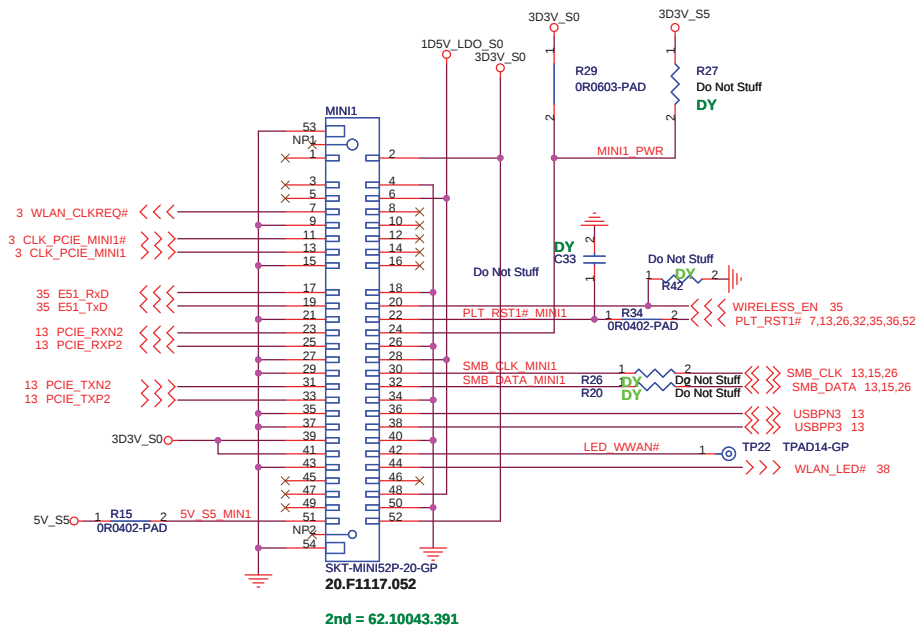
SB 0601



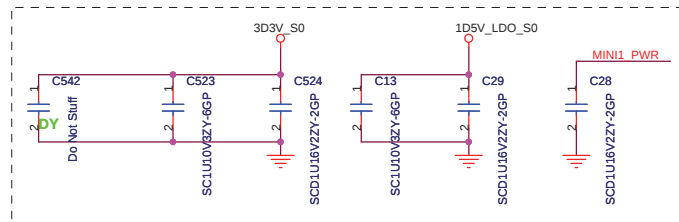
UMA

Mini Card Connector(WLAN)

Support debug-card

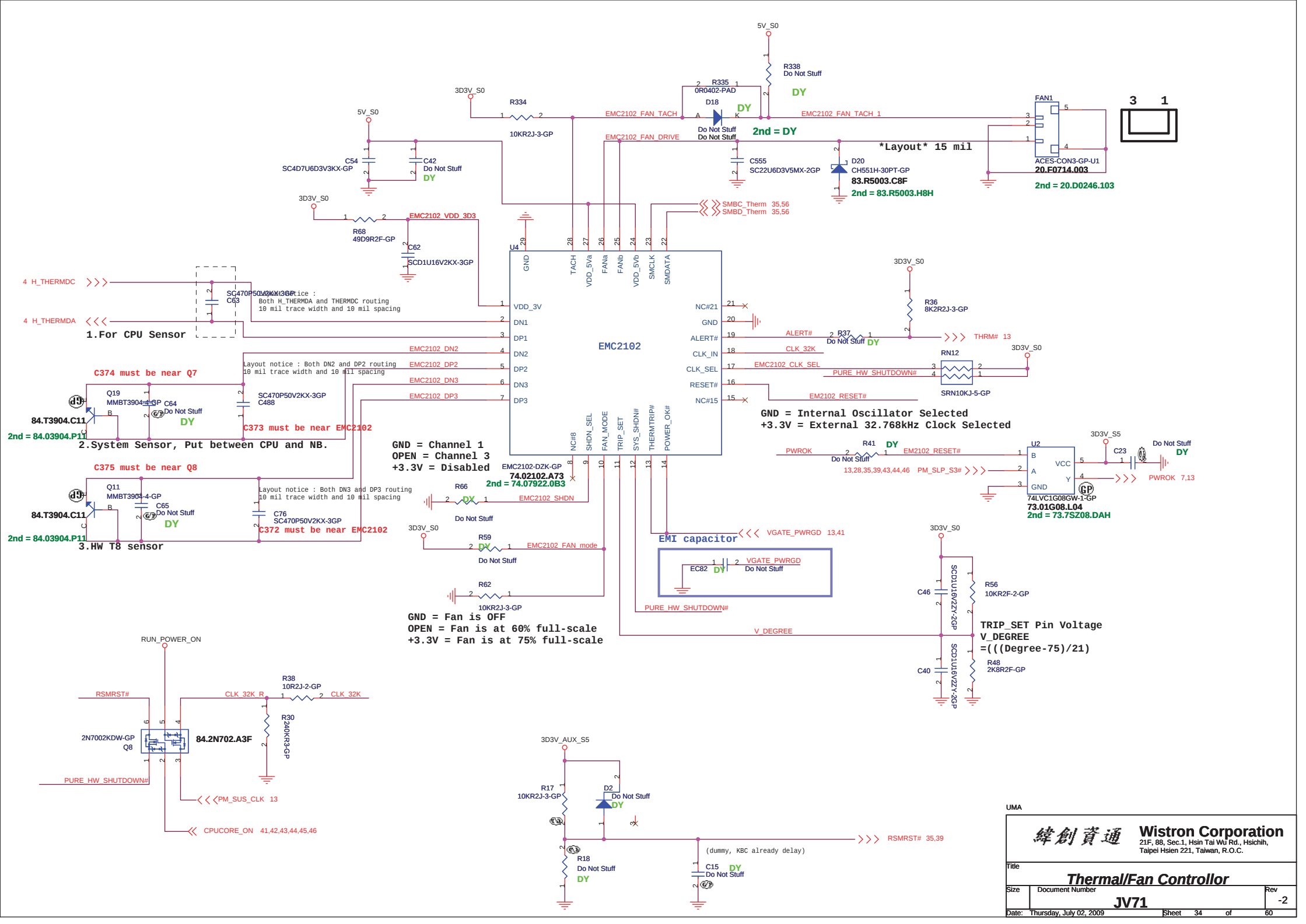


Place near MINI1

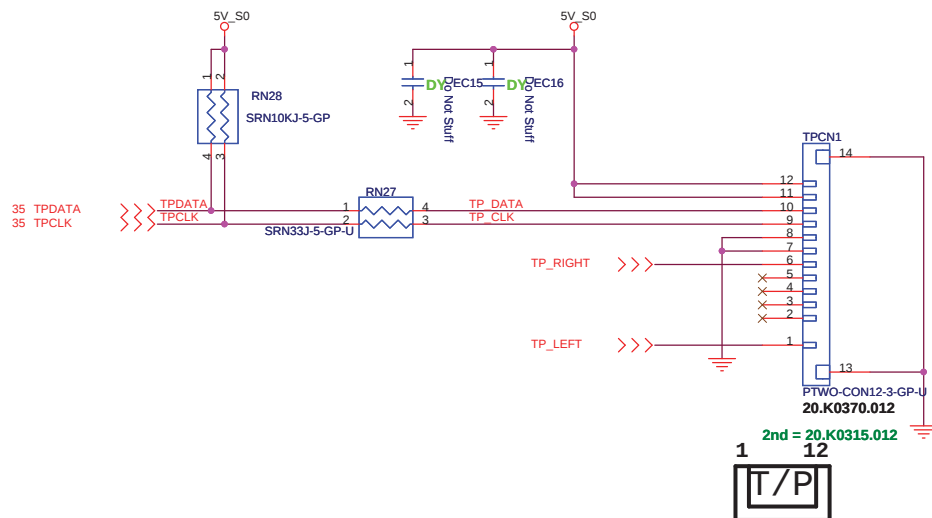


Mini Card Connector

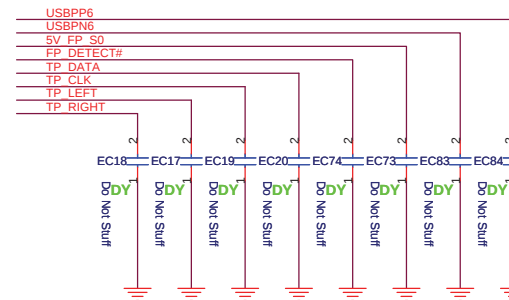
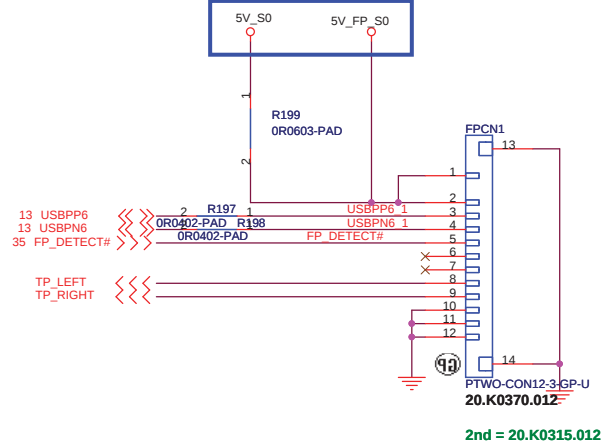
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TOUCH PAD



SB 0518 Finger printer



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Title			
Touch PAD and FP			
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Power LED

FRONT_PWRLED# Q 4
STDBY_LED# Q 3
DC_BATFULL# Q 2
CHARGE_LED# Q 1

PN81

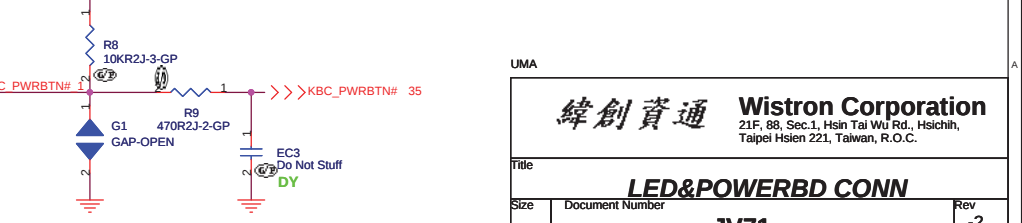
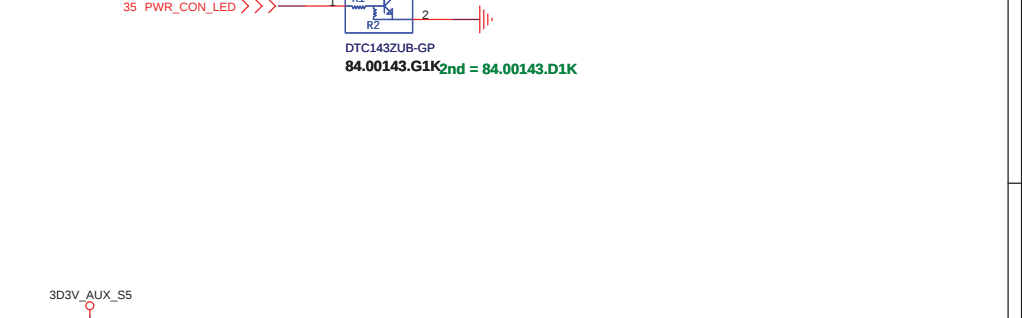
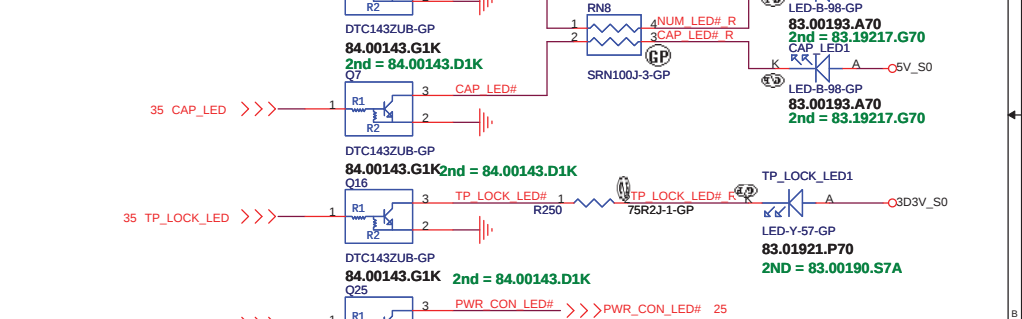
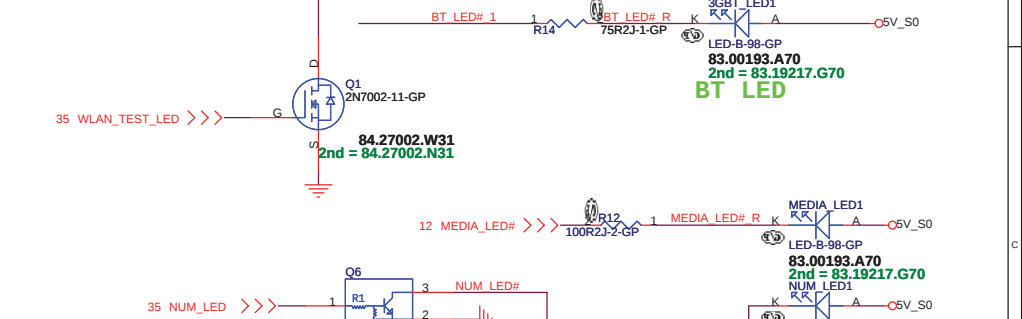
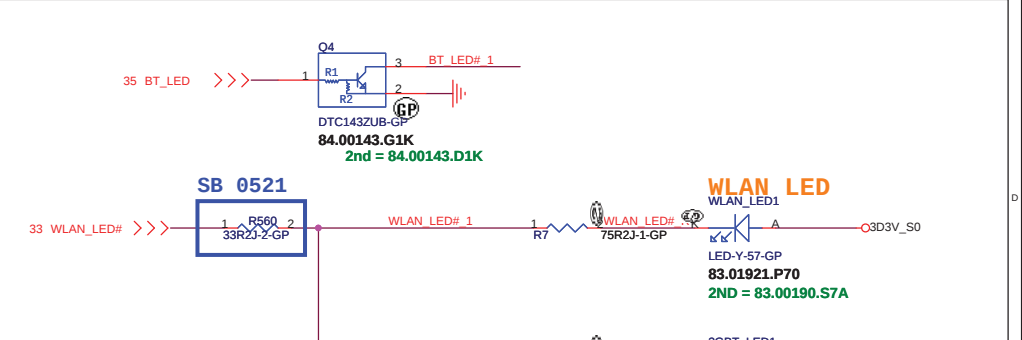
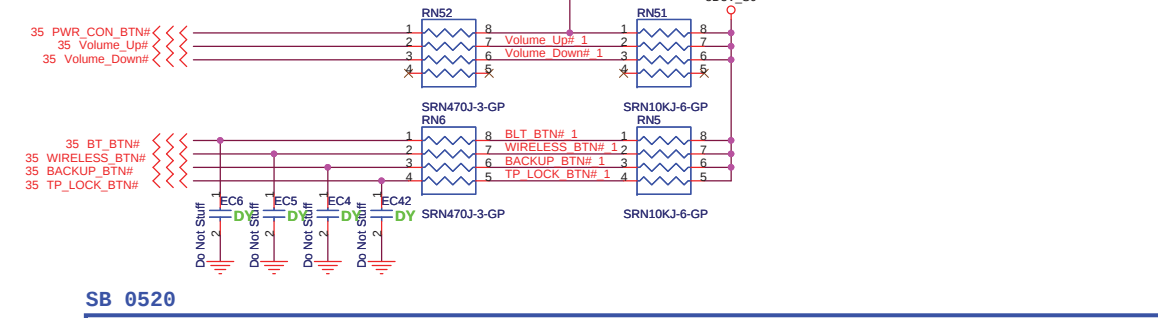
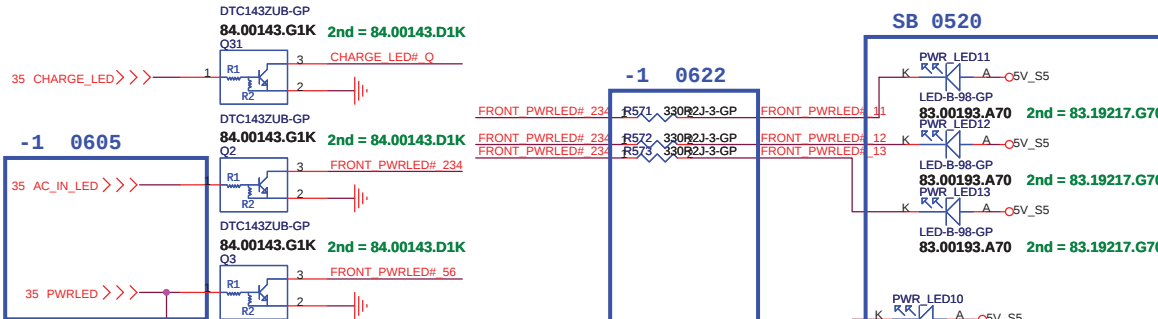
LED-OB-2-GP
83.19223.A70
2nd =
CHARGER_LED1

DC_BATFULL# R
CHARGE_LED# R

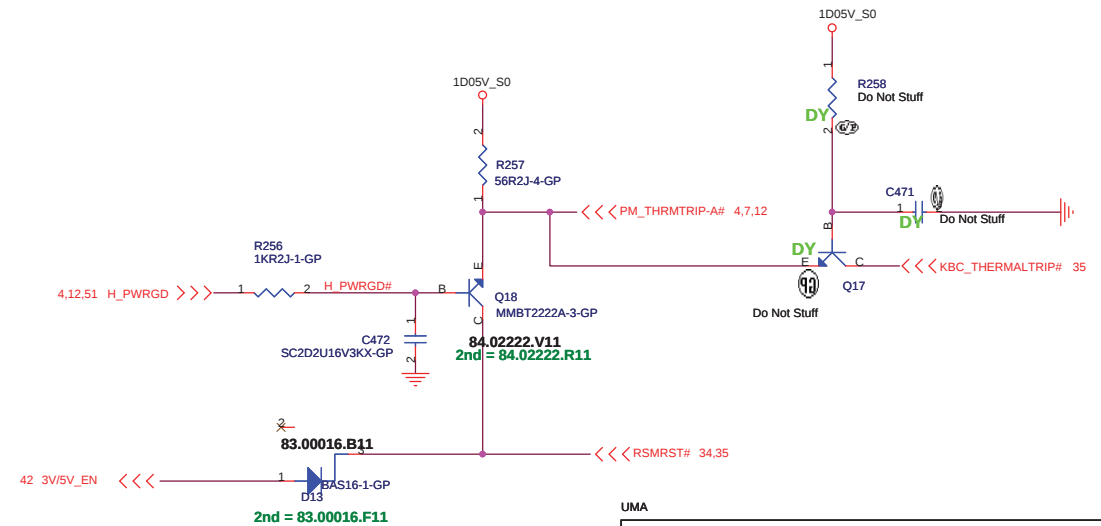
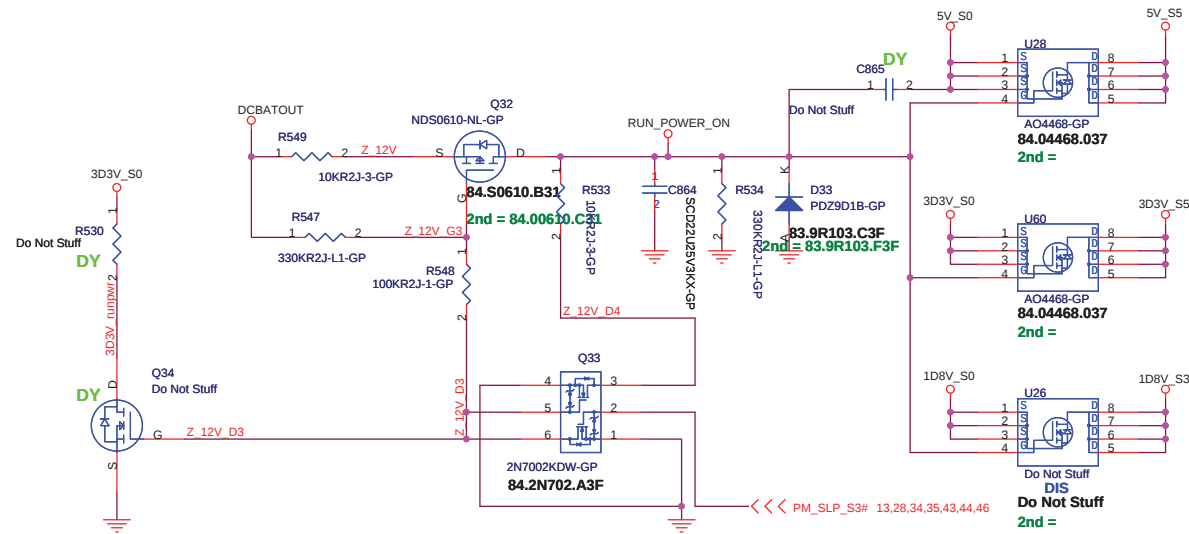
5V_AUX_S5

Charger LED

LED-OB-2-GP
83.19223.A70
2nd =



Run Power



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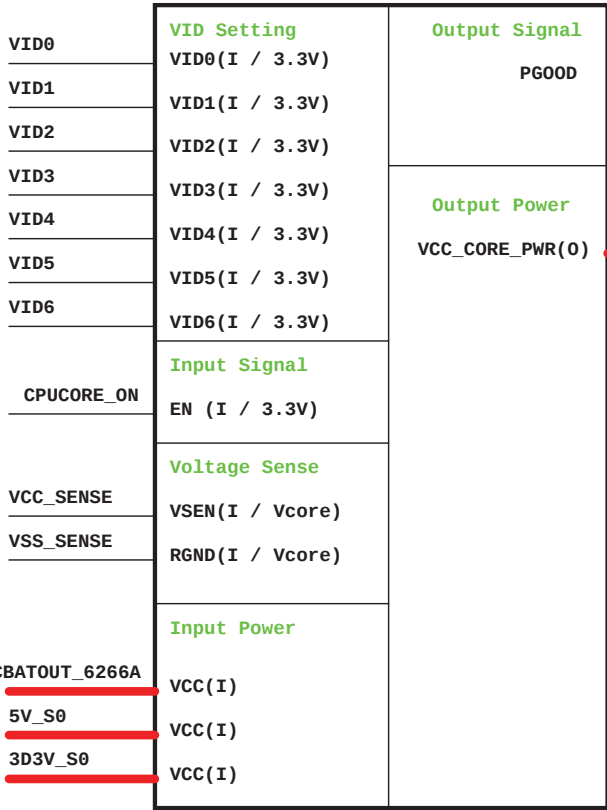
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5
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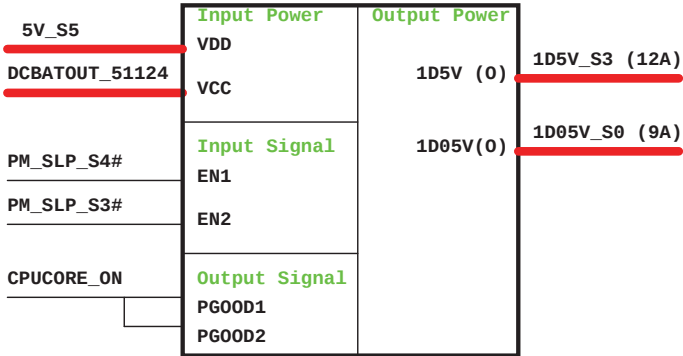
Size	Document Number	Rev
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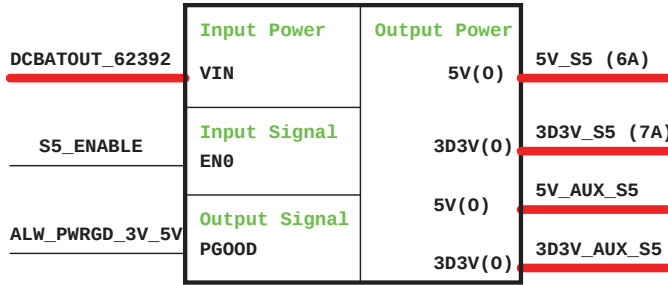
CPU_CORE
ISL6266A



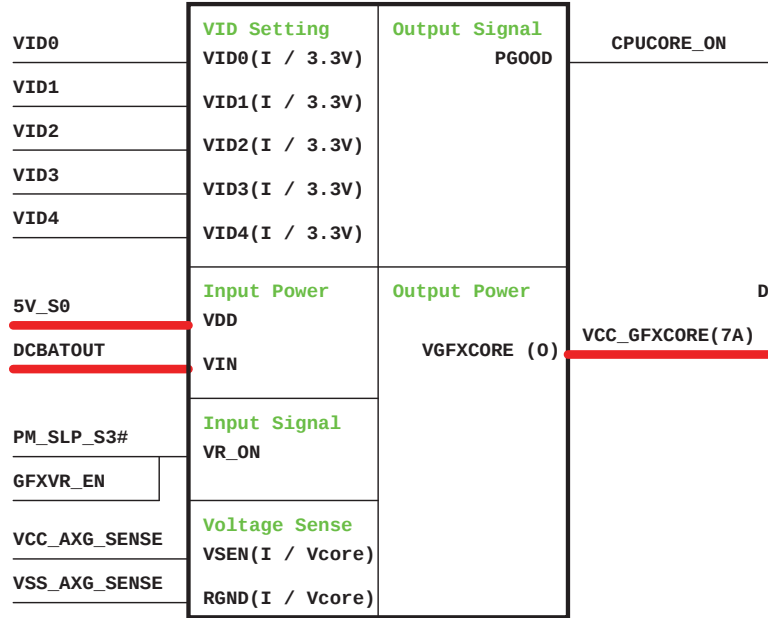
TPS51124
1D8V/1D05V



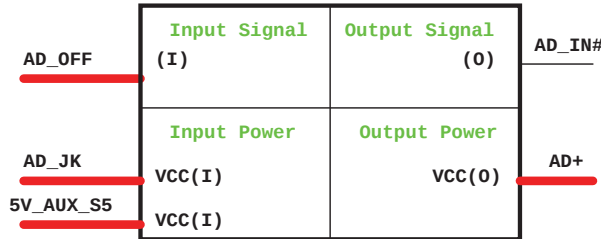
ISL62392
5V/3D3V



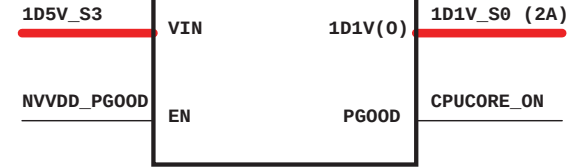
GFX_CORE
ISL6263A



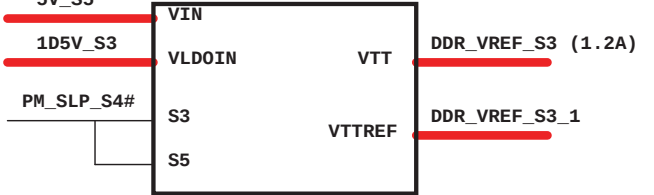
Adapter



RT9018A 1D1V S0



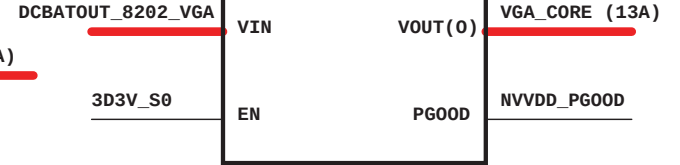
RT9026 DDR_VREF_S3



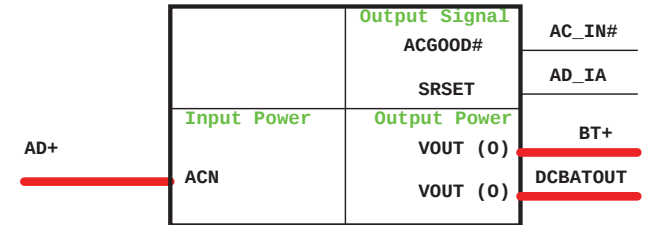
TPS51117 FBVDD

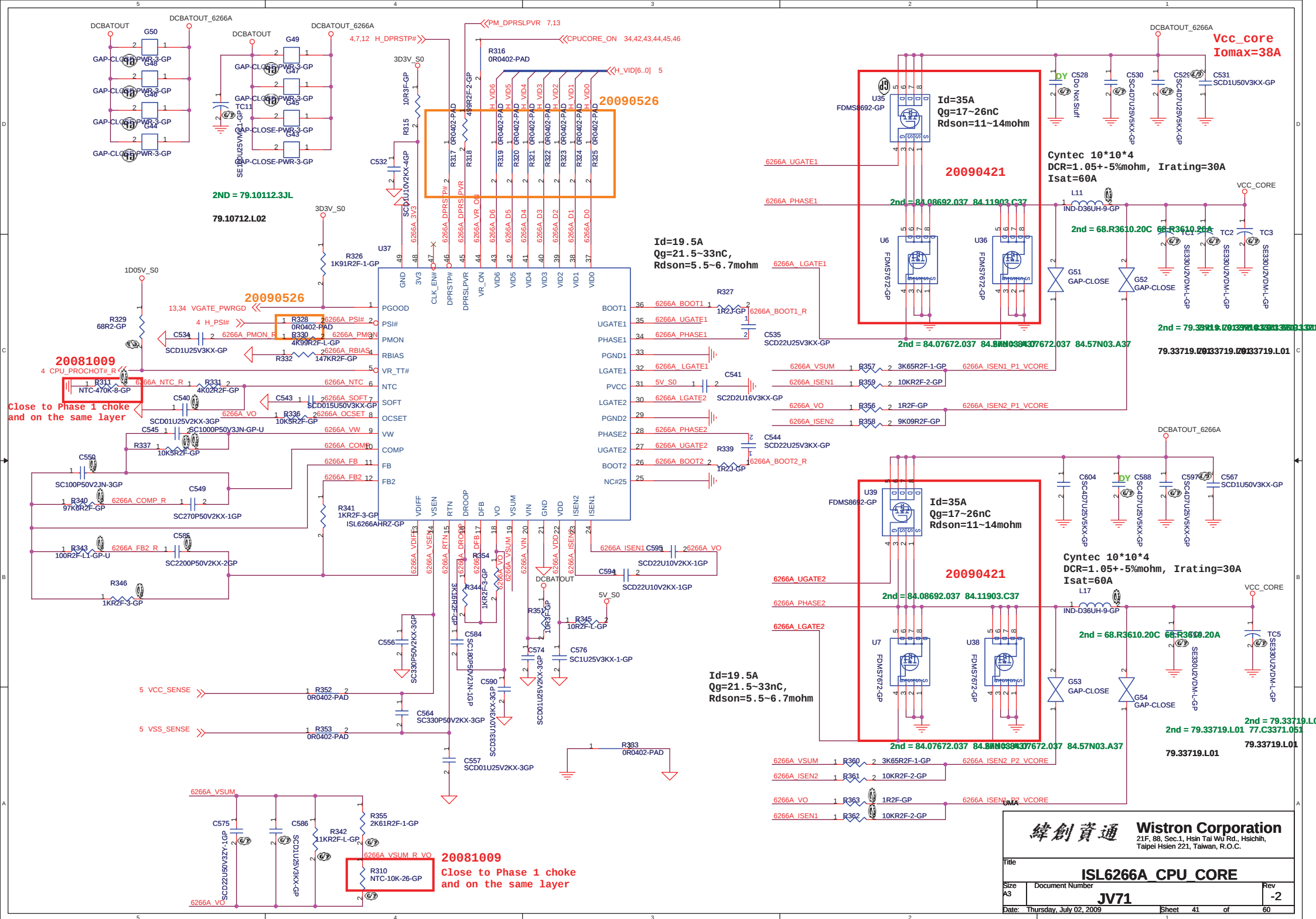


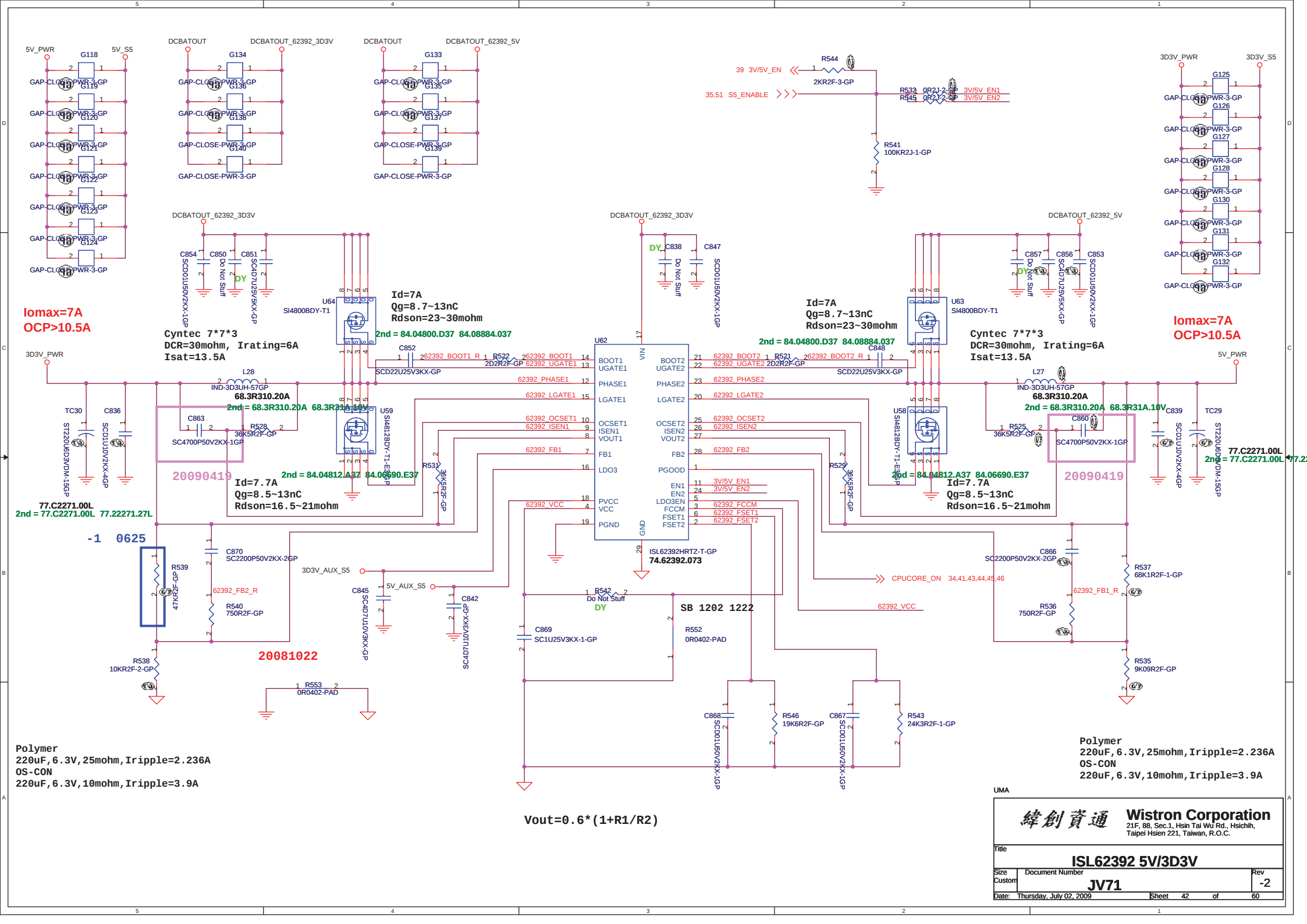
RT8202A VGA CORE



Charger ISL88731A







Iomax=7A
OCP>10.5A

Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

77.C2271.00L
2nd = 77.C2271.00L 77.22271.27L

Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm

20081022

Polymer
220uF, 6.3V, 25mohm, Irripple=2.236A
OS-CON
220uF, 6.3V, 10mohm, Irripple=3.9A

$V_{out} = 0.6 * (1 + R1/R2)$

Id=7A
Qg=8.7~13nC
Rdson=23~30mohm

2nd = 84.04800.D37 84.08884.037

Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm

Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A

77.C2271.00L
2nd = 77.C2271.00L 77.22271.27L

Iomax=7A
OCP>10.5A

Polymer
220uF, 6.3V, 25mohm, Irripple=2.236A
OS-CON
220uF, 6.3V, 10mohm, Irripple=3.9A

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Taipei Hsien 221, Taiwan, R.O.C.

Title
ISL62392 5V/3D3V

Size
Custom

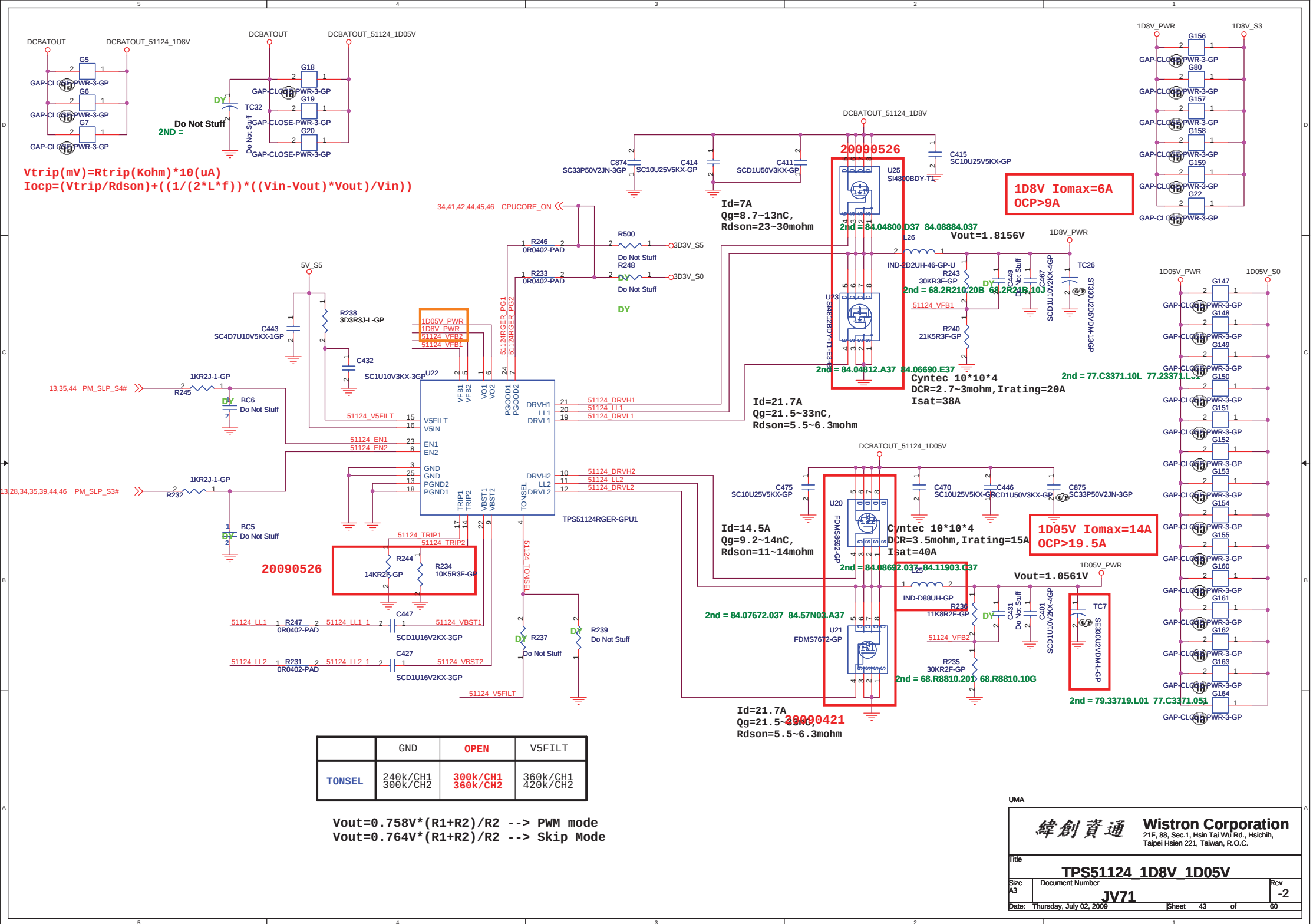
Document Number
JV71

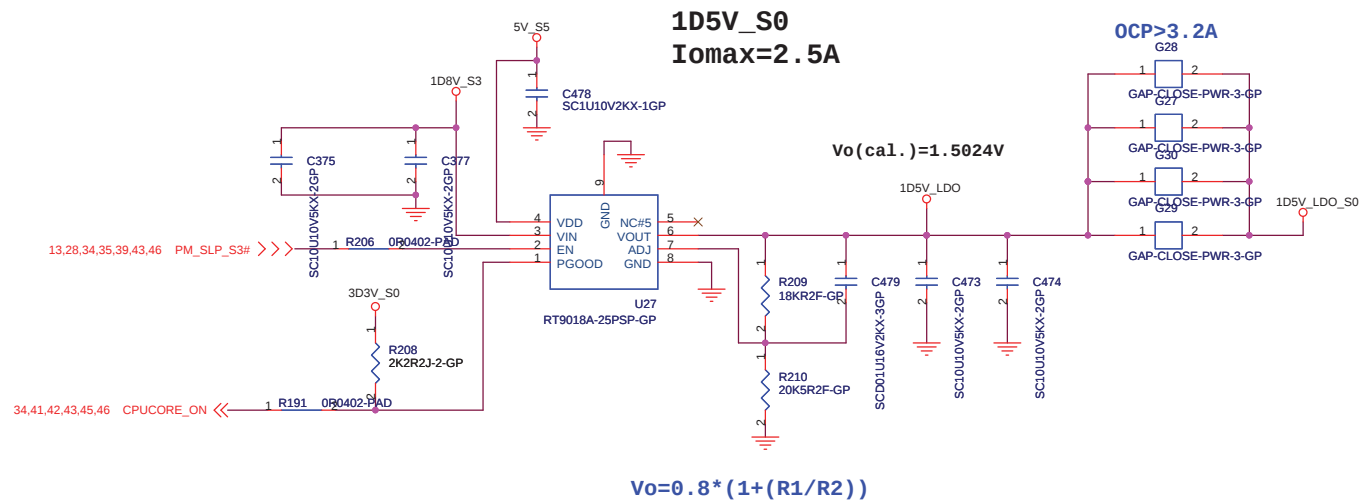
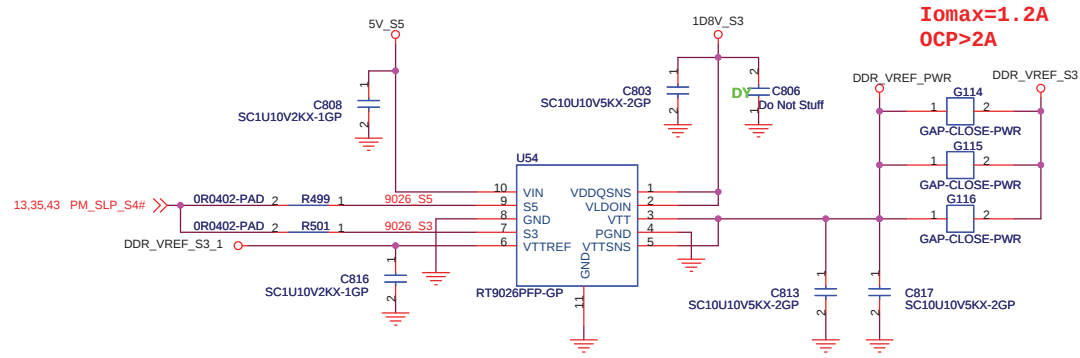
Date
Thursday, July 02, 2009

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 Taipei Hsien 221, Taiwan, R.O.C.

Title

0D75V

Size
A3

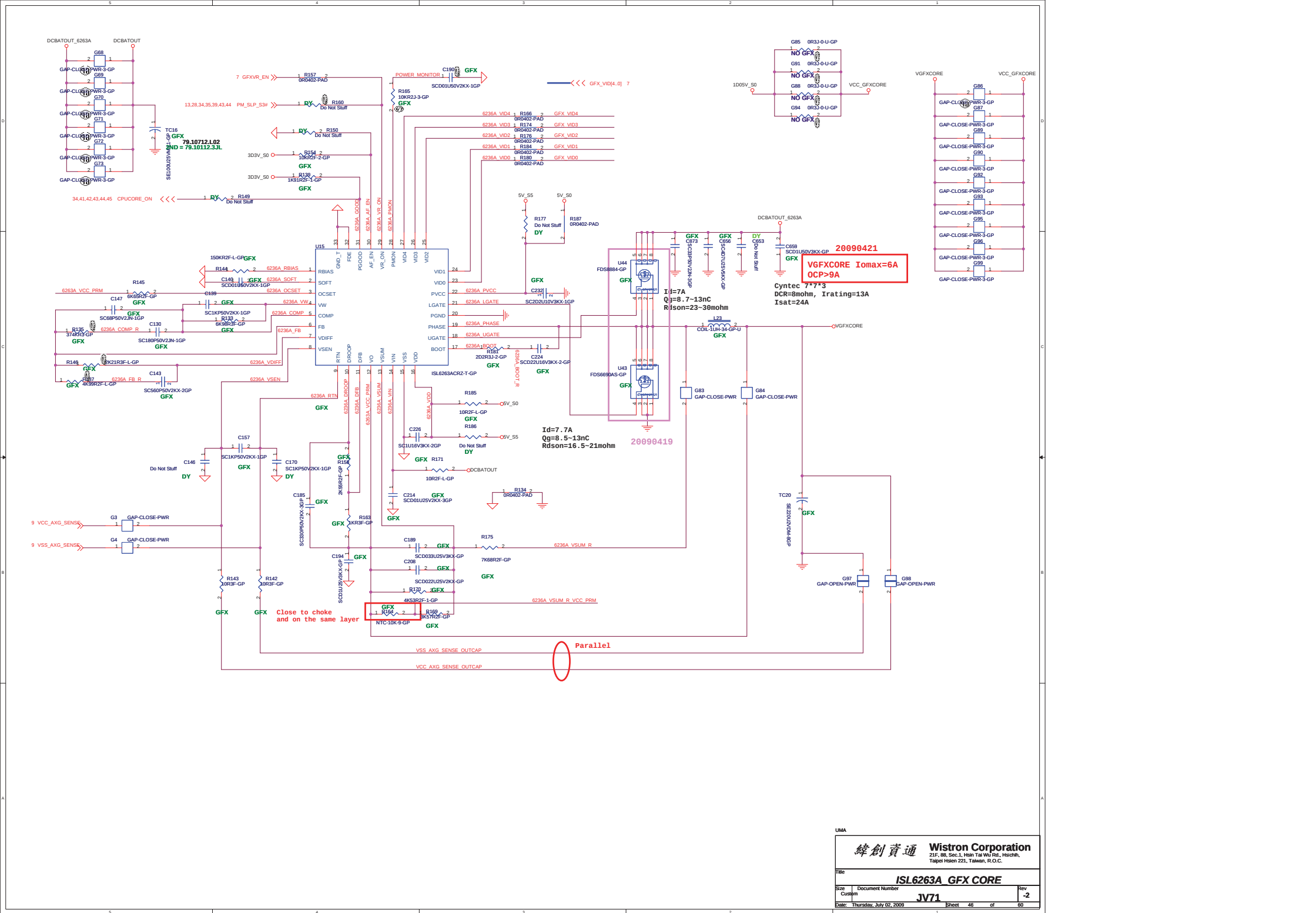
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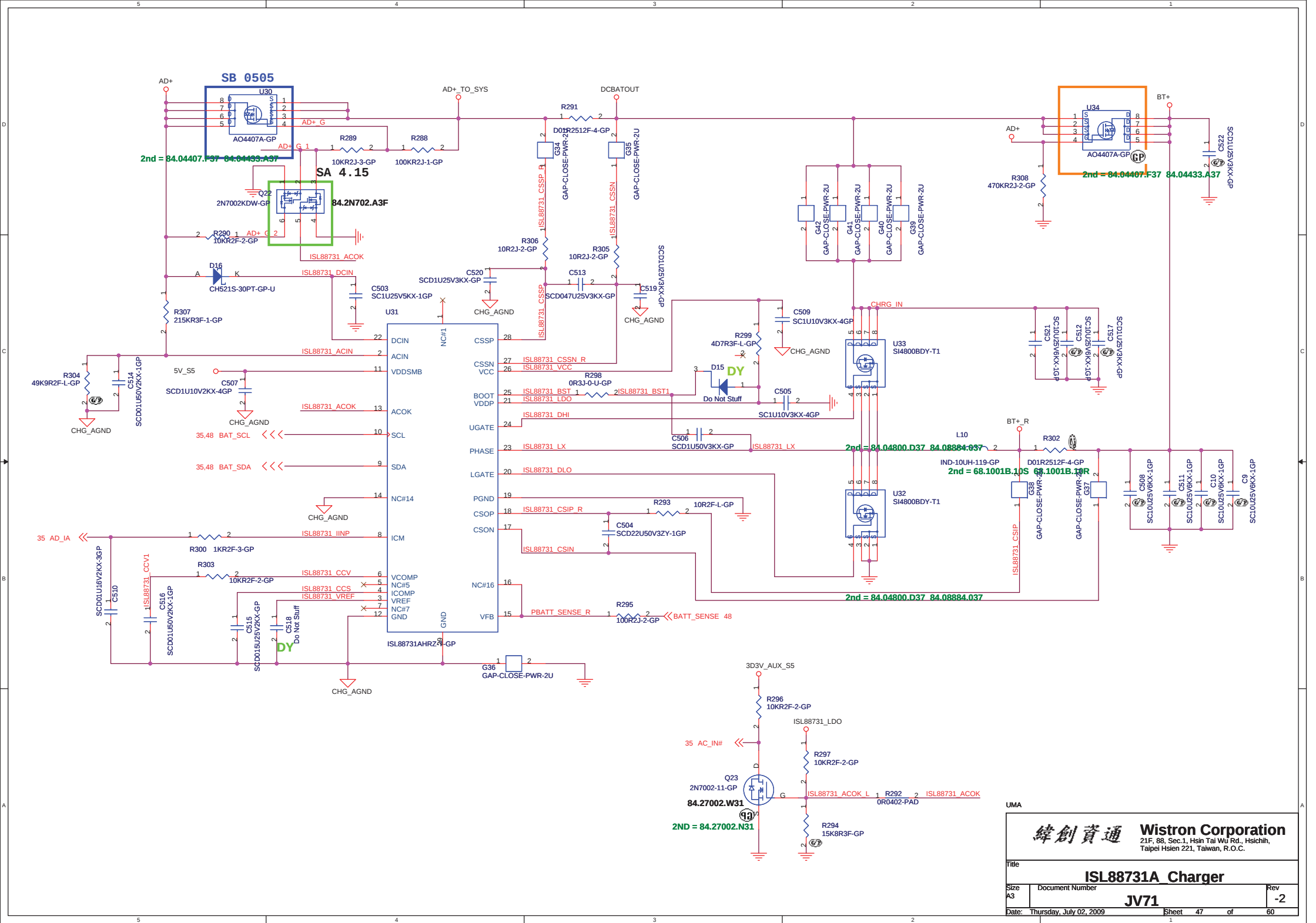
JV71

Rev
-2

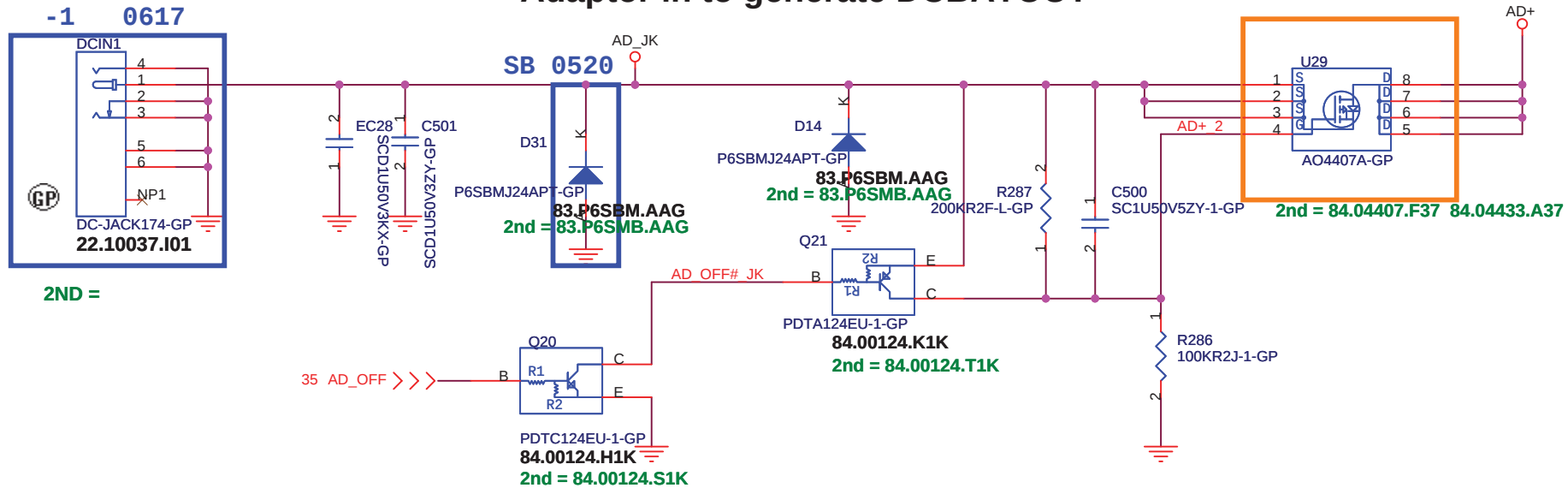
Date: Thursday, July 02, 2009

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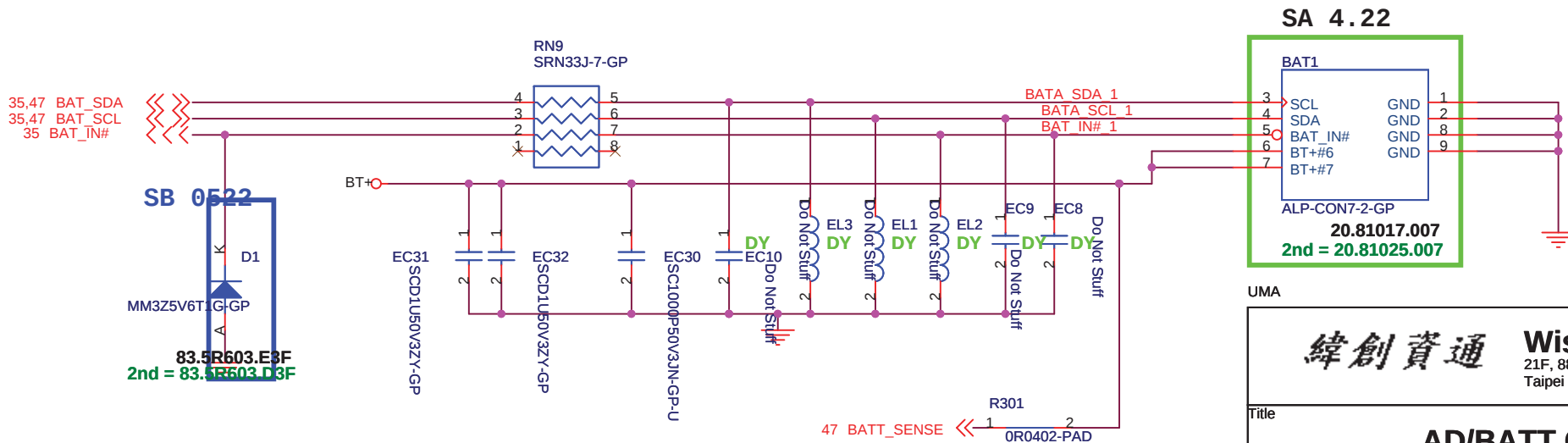




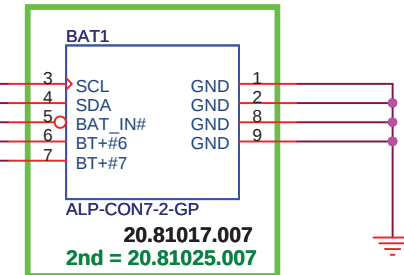
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



SA 4.22



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Wistron Corporation

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Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size

Document Number

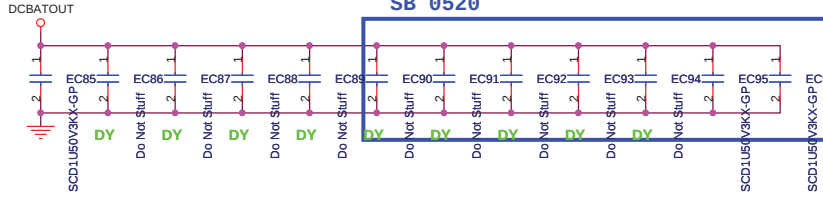
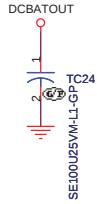
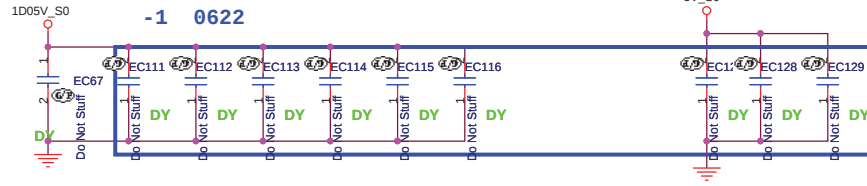
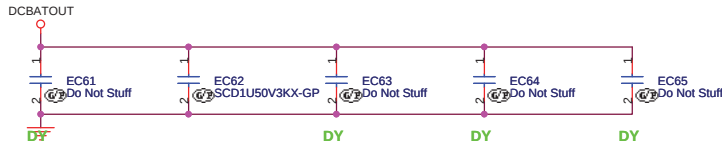
JV71

Rev

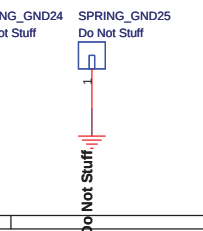
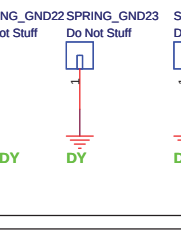
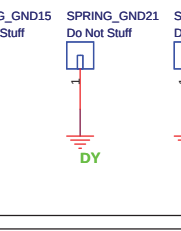
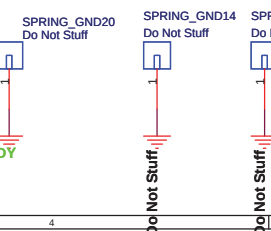
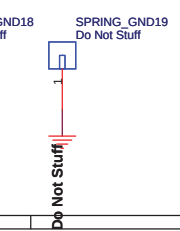
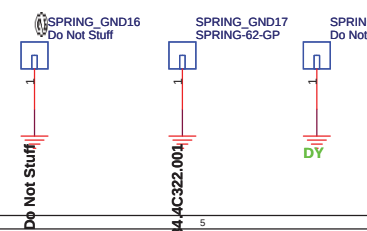
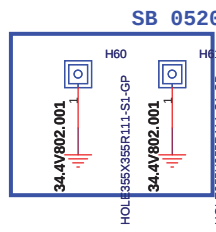
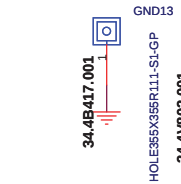
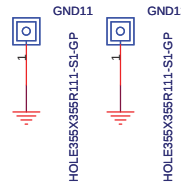
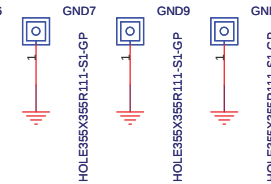
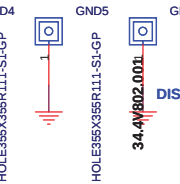
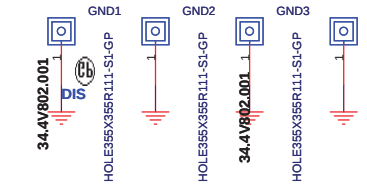
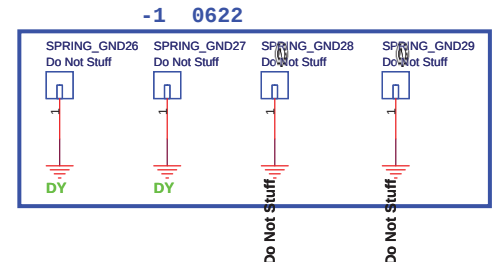
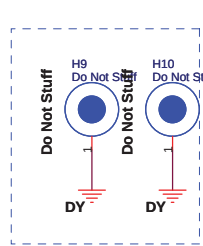
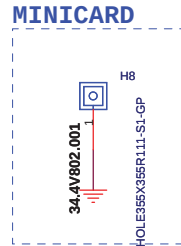
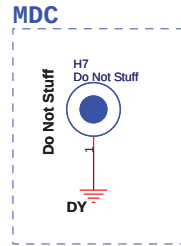
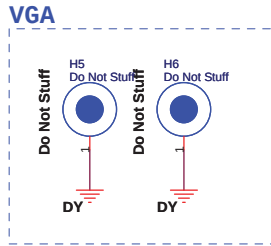
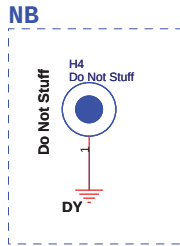
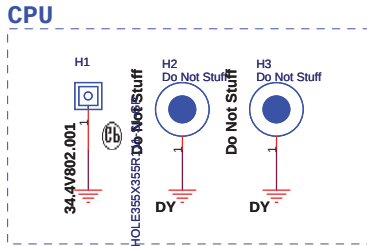
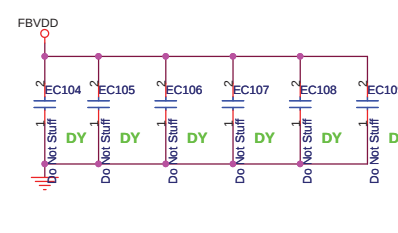
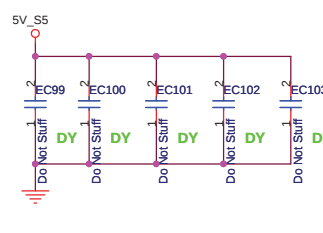
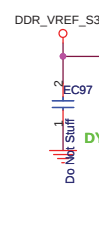
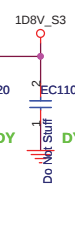
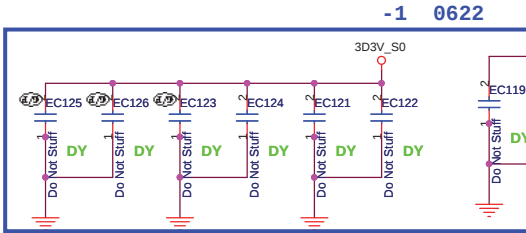
-2

Date: Thursday, July 02, 2009

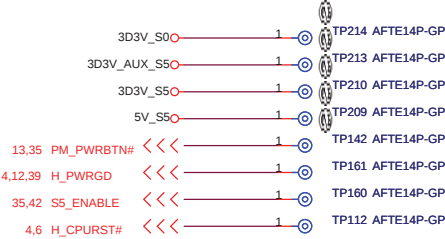
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2ND = 79.10112.3JL
79.10712.L02

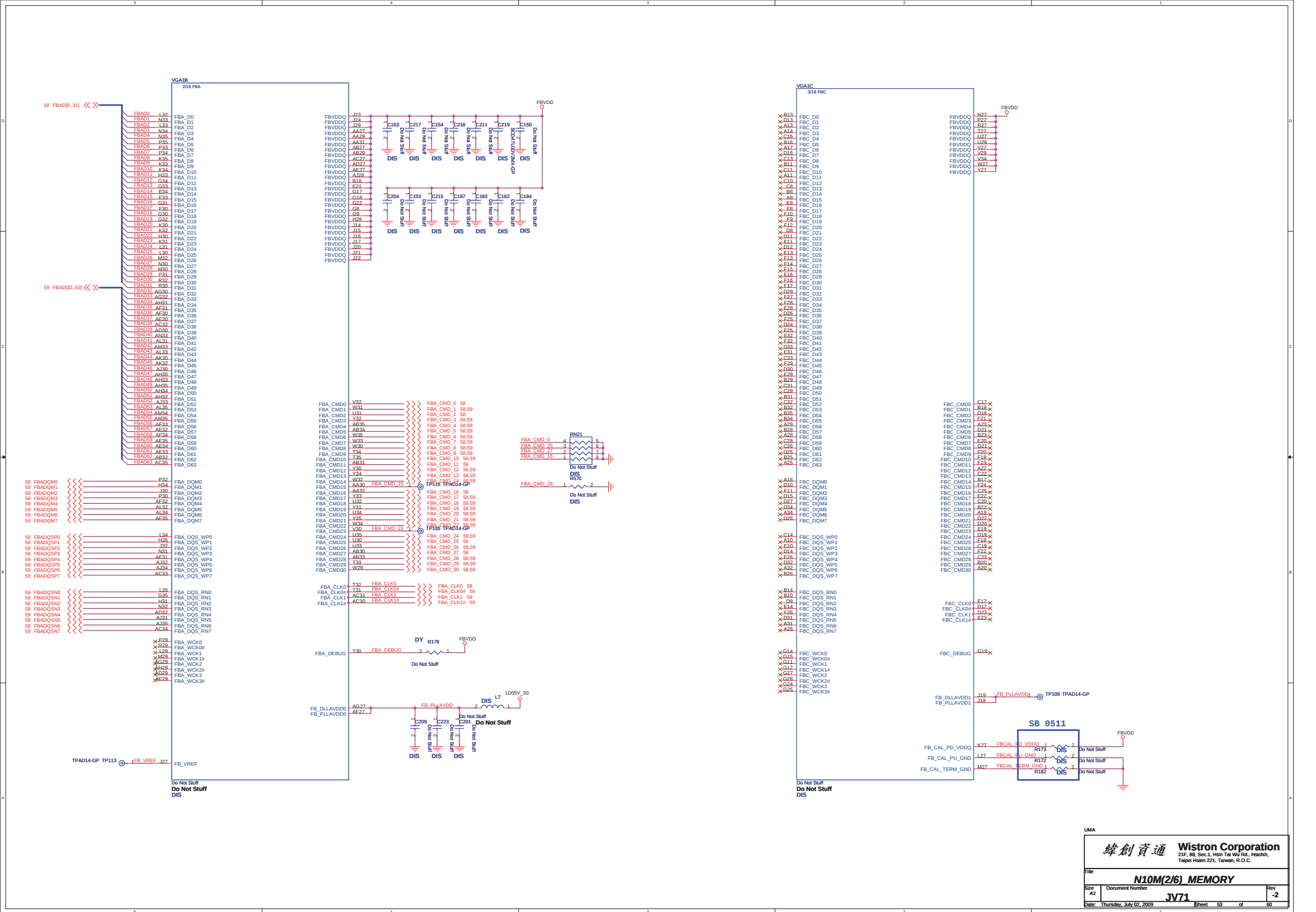


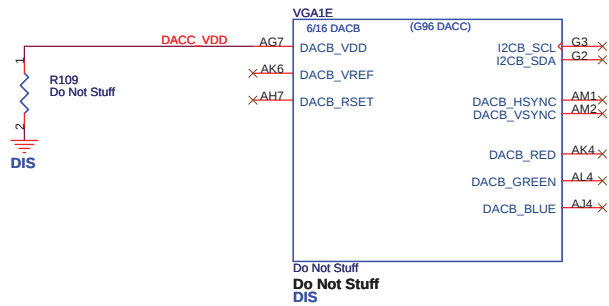
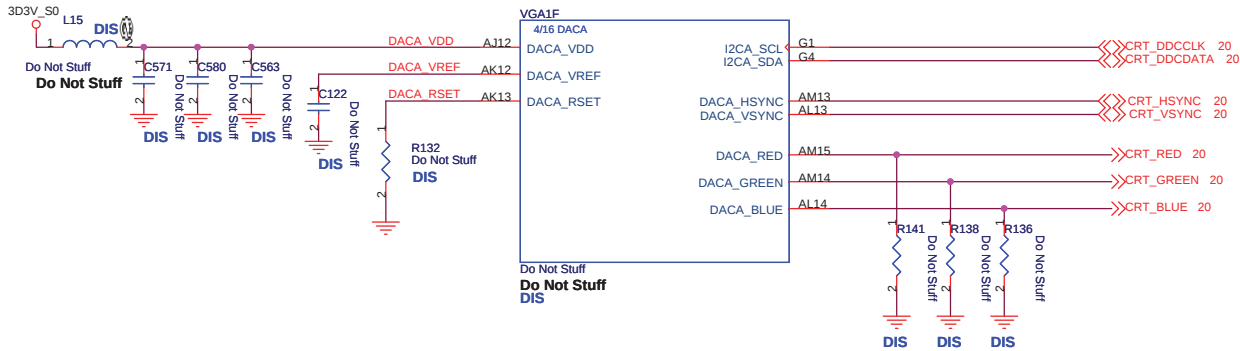
Check test point



Test Point放在Dimm Door打開可量測處

UMA





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緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
N10M(3/6) DAC			
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