Compal Confidential

Schematics Document

Intel Huron River

Sandy Bridge with Couger Point core logic

2010-10-27

REV:1.0

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.		
Title: Cover Page		
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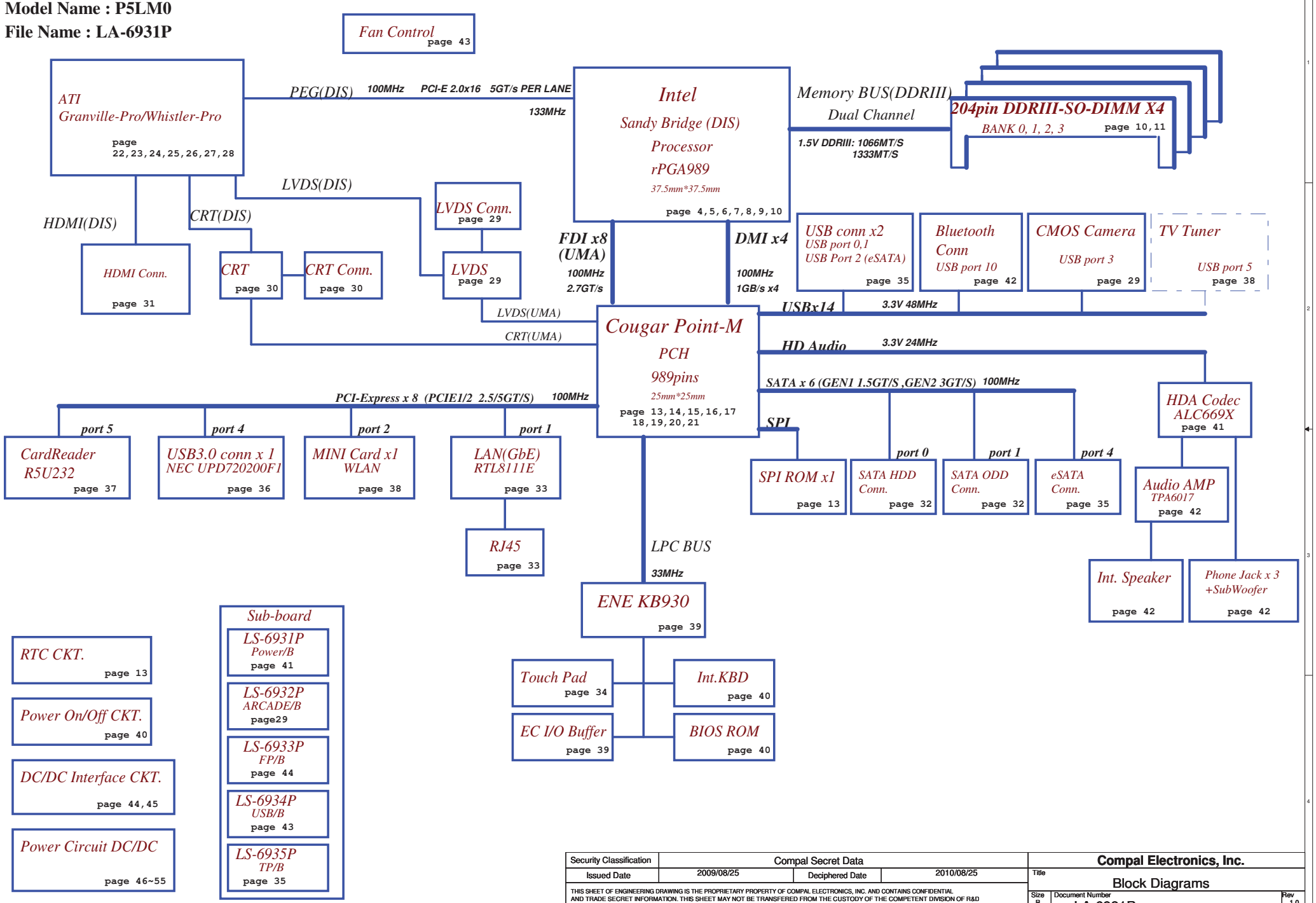
Model Name : P5LM0
File Name : LA-6931P



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Compal Electronics, Inc.		
Title: Block Diagrams		
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Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (DIS)	IGPU (SG)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS_VCCP	1.05V switched power rail for CPU (PCH)	ON	OFF	OFF		
+VGFX_CORE	Core voltage for IGPU	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3VALW_PCH	3.3V power rail for PCH	ON	ON	ON*		
+LAN_IO	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+VGA_CORE	5V power rail for GPU	ON	OFF	OFF	ON	OFF
+1.5VSDGPU	1.5V power rail for VRAM	ON	OFF	OFF	ON	OFF
+1.8VSDGPU	1.8V switched power rail for GPU	ON	OFF	OFF	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
* 3	0.4
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
DIS Only	DIS@
Switchable Graphics	SG@
Granville	GRA@
Whistler	WHI@
For CIR	CIR@
USB2.0 bus	USB2@
DDR M1	M1@
DDR M3	M3@
For 45 level	45@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB/B
		1	USB Conn.
	UHCI1	2	
		3	
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	eSATA USB
	UHCI5	10	CMOS Camera
		11	Finger Print
	UHCI6	12	USB3.0 @
		13	Blue Tooth

43 Level BOM Config

Granville DIS: GRA@ DIS@ CIR@ M1@
Whistler SG: WHI@ SG@ CIR@ M1@

45 Level BOM Config

45@

VRAM BOM Config

X76255BOL01: HYNIX 1G (old die)
X76255BOL02 HYNIX 1G (new die)
X76255BOL04 HYNIX 2G

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Title: Notes List

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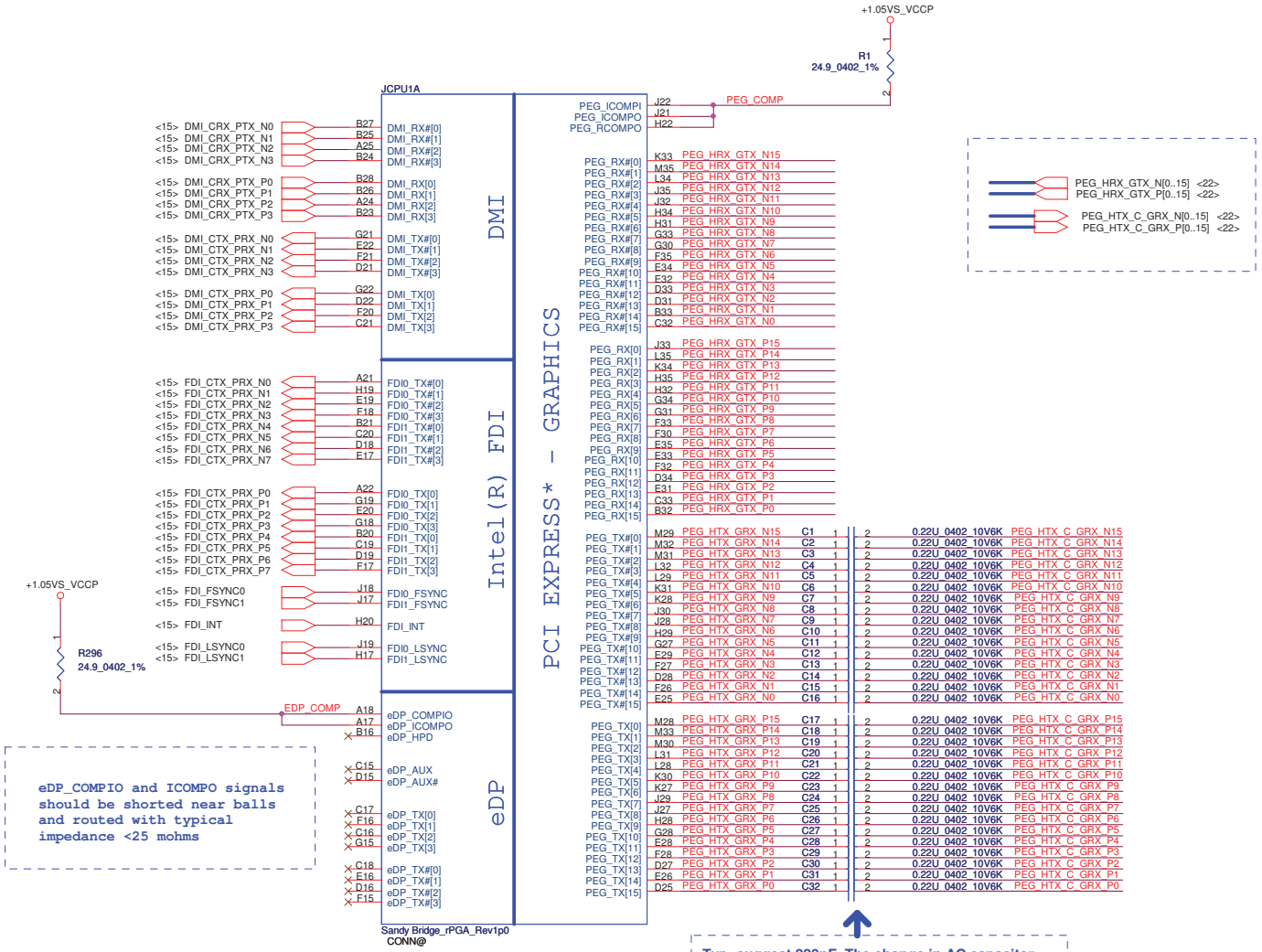

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

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Title: PROCESSOR(1/7) DMI,FDI,PEG

Size	Document Number	Rev
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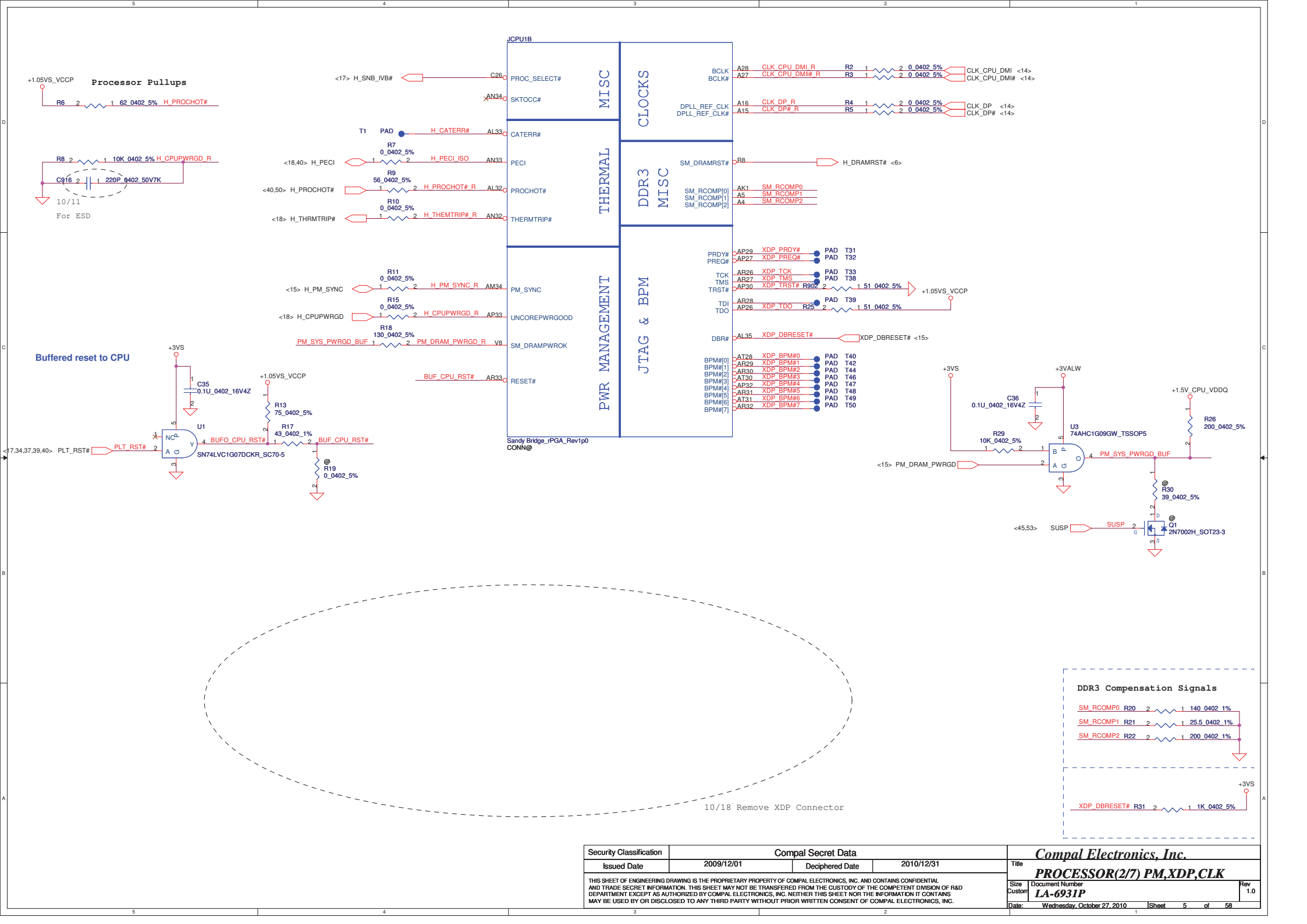

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Title	Compal Electronics, Inc.		
	PROCESSOR(2/7) PM,XDP,CLK		
Size: Custom	Document Number: LA-6931P		Rev: 1.0
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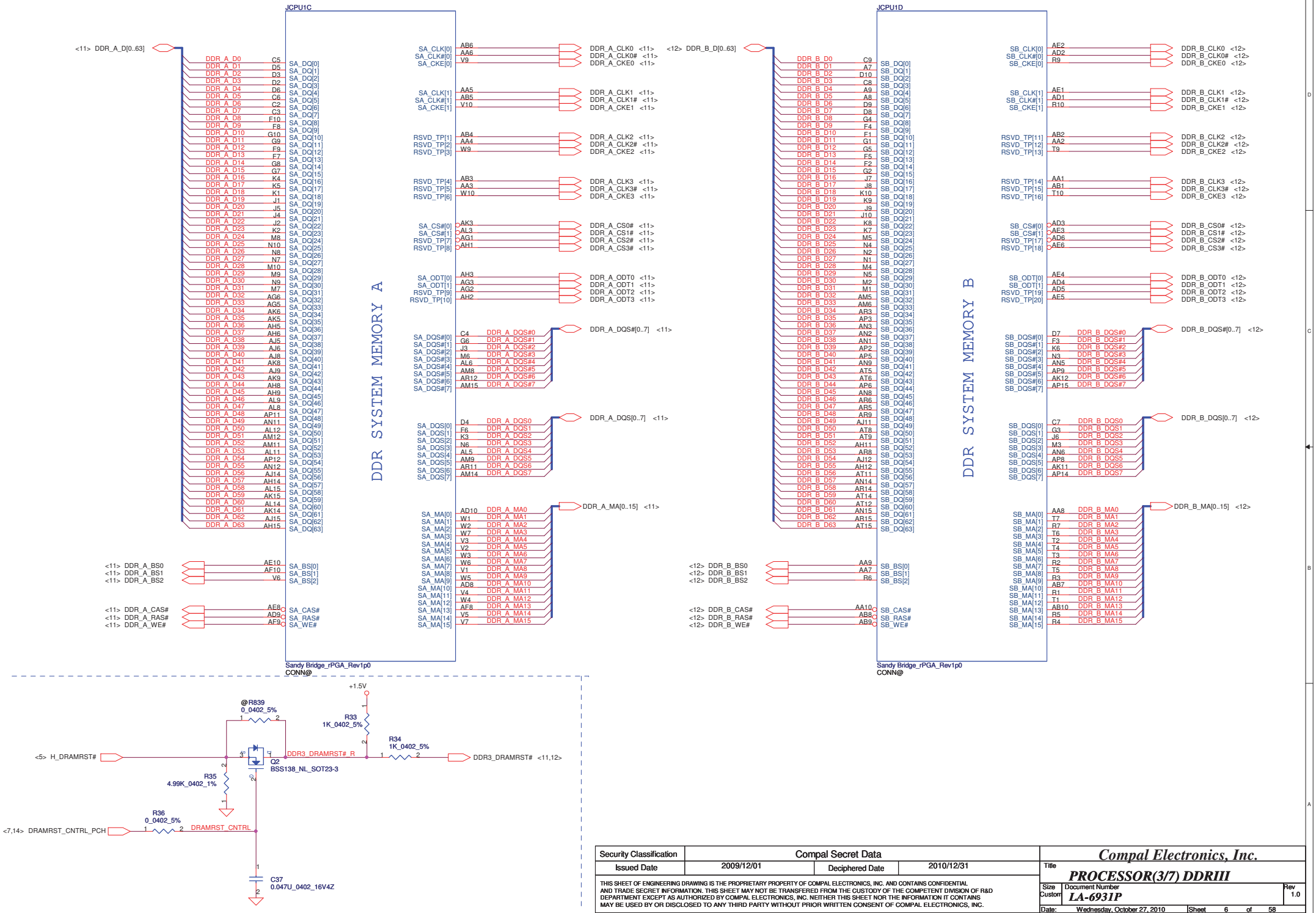

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PROCESSOR(3/7) DDRIII

Size	Document Number	Rev
Custom	LA-6931P	1.0

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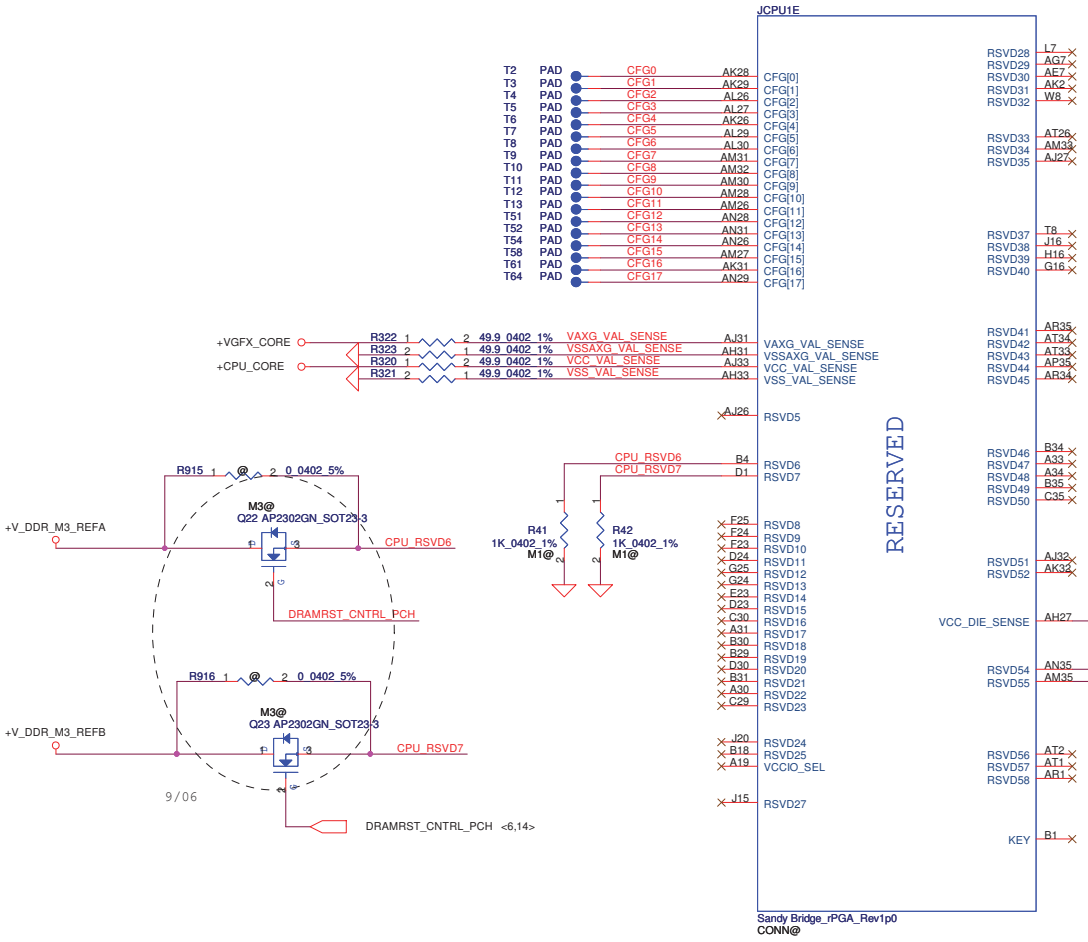
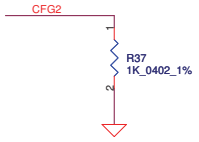
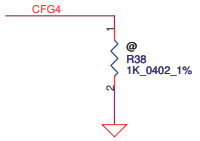
CFG Straps for Processor

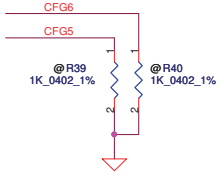




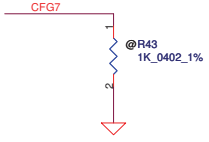
PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

Compal Electronics, Inc.

Title: PROCESSOR(4/7) RSVD,CFG

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POWER

SV type CPU

JCPU1F

Bottom Socket Cavity

+CPU_CORE

C38 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C40 10U_0805_6.3V6M
C41 10U_0805_6.3V6M
C42 10U_0805_6.3V6M
C788 10U_0805_6.3V6M
C789 10U_0805_6.3V6M
C790 10U_0805_6.3V6M
C791 10U_0805_6.3V6M
C792 10U_0805_6.3V6M

Top Socket Cavity

+CPU_CORE

C799 22U_0805_6.3V6M
C800 22U_0805_6.3V6M
C801 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C807 22U_0805_6.3V6M
C802 22U_0805_6.3V6M
C803 22U_0805_6.3V6M
C804 22U_0805_6.3V6M

Top Socket Edge

C73 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C805 22U_0805_6.3V6M
C806 22U_0805_6.3V6M
C807 22U_0805_6.3V6M
C808 22U_0805_6.3V6M
C809 22U_0805_6.3V6M
C810 22U_0805_6.3V6M

Bottom Socket Edge

+CPU_CORE

C811 330U_D2_2.5VY_R9M
C812 330U_D2_2.5VY_R9M
C813 470U_D2_2VM_R4.5M
C814 470U_D2_2VM_R4.5M

09/10

53A

AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26

VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

Sandy Bridge rPGA Rev1p0

18A

MB Bottom Socket Cavity

+1.05VS_VCCP

AH13 AH10 AG10 AC10 Y10 U10 P10 L10 J14 J13 J12 J11 H14 H12 H11 G14 G13 G12 F14 F13 F12 F11 E14 E12 E11 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11 J23

VCCIO1 VCCIO2 VCCIO3 VCCIO4 VCCIO5 VCCIO6 VCCIO7 VCCIO8 VCCIO9 VCCIO10 VCCIO11 VCCIO12 VCCIO13 VCCIO14 VCCIO15 VCCIO16 VCCIO17 VCCIO18 VCCIO19 VCCIO20 VCCIO21 VCCIO22 VCCIO23 VCCIO24 VCCIO25 VCCIO26 VCCIO27 VCCIO28 VCCIO29 VCCIO30 VCCIO31 VCCIO32 VCCIO33 VCCIO34 VCCIO35 VCCIO36 VCCIO37 VCCIO38 VCCIO39 VCCIO40

C43 22U_0805_6.3V6M
C44 22U_0805_6.3V6M
C785 22U_0805_6.3V6M
C786 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C794 330U_D2_2V_Y
C906 330U_D2_2V_Y
C48 22U_0805_6.3V6M
C49 22U_0805_6.3V6M
C50 22U_0805_6.3V6M
C51 22U_0805_6.3V6M
C787 22U_0805_6.3V6M

MB Top Socket Cavity

C795 22U_0805_6.3V6M
C796 22U_0805_6.3V6M
C797 22U_0805_6.3V6M
C798 22U_0805_6.3V6M
C793 330U_D2_2V_Y
C910 22U_0805_6.3V6M
C209 22U_0805_6.3V6M
C904 22U_0805_6.3V6M
C211 22U_0805_6.3V6M
C212 22U_0805_6.3V6M

+1.05VS_VCCP

R44 130_0402_5%
R903 75_0402_5%
R46 43_0402_1%

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

R842 0_0402_5%
R843 0_0402_5%

VR_SVID_ALRT# <56>
VR_SVID_CLK <56>
VR_SVID_DAT <56>

Place the PU resistors close to VR

+CPU_CORE

R844 100_0402_1%
R52 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R

R50 0_0402_5%
R51 0_0402_5%

VCCSENSE <56>
VSSSENSE <56>

VCCIO_SENSE B10 VCCIO_SENSE
VSSIO_SENSE A10 VSSIO_SENSE

VCCIO_SENSE <53>
VSSIO_SENSE <53>

Place the PU resistors close to CPU

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Title: PROCESSOR(5/7) PWR,BYPASS

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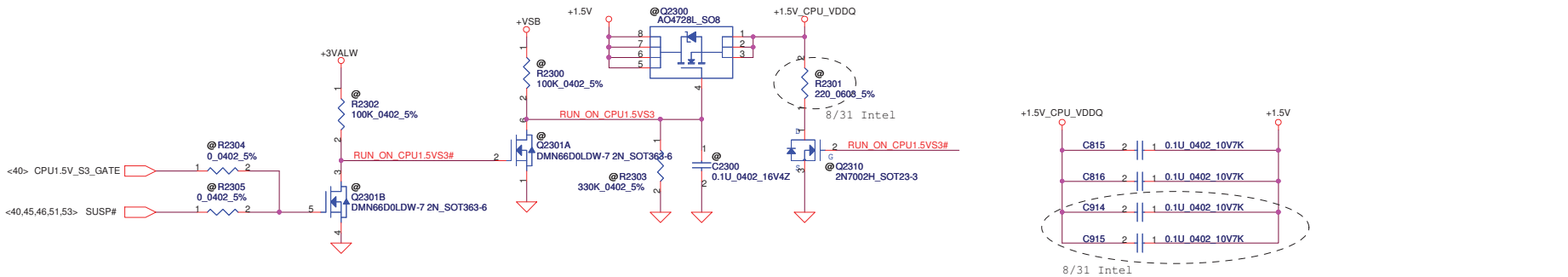
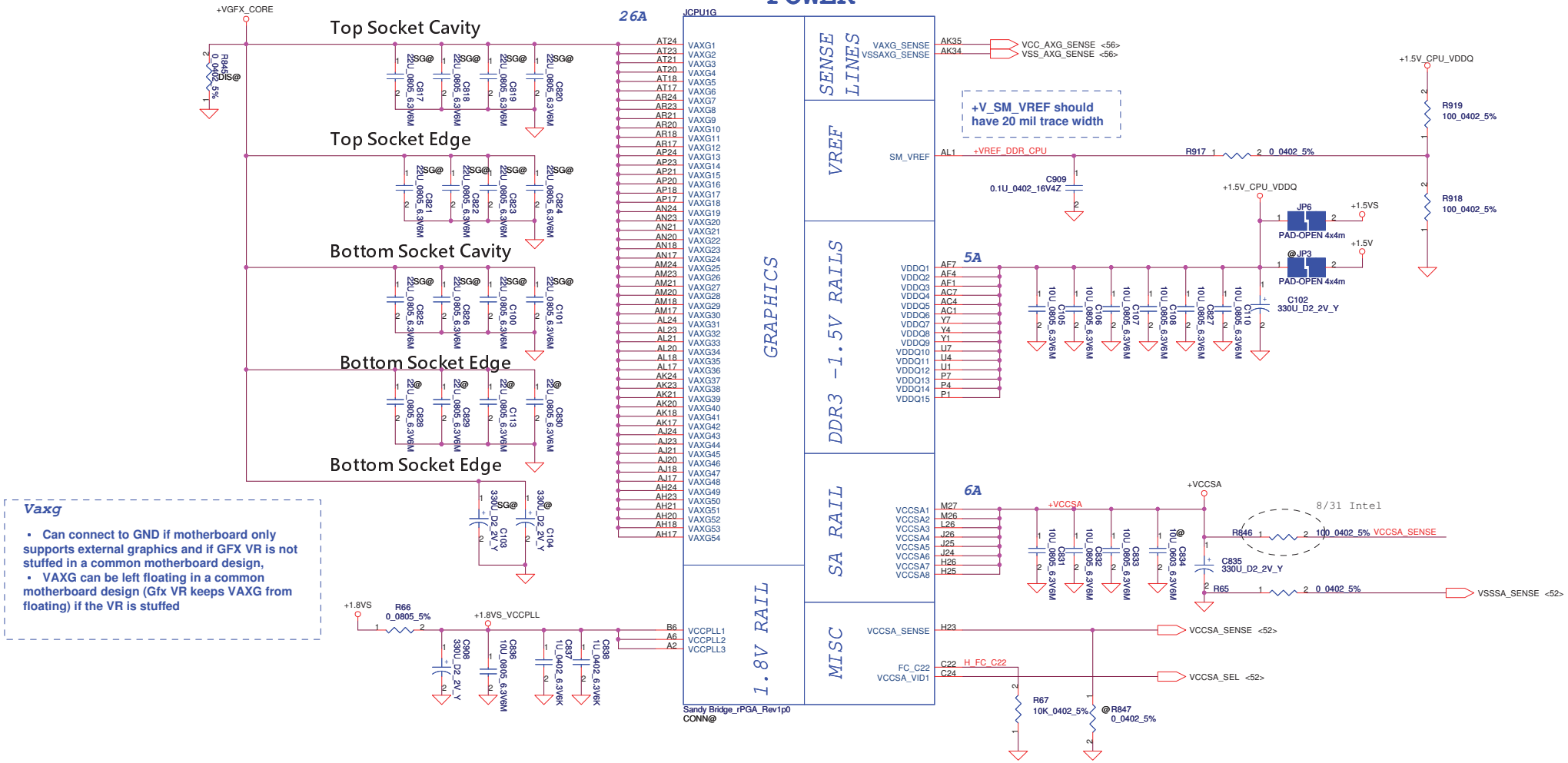
+1.5V_CPU_VDDQ Source



POWER



Vaxg

- Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed in a common motherboard design,
- VAXG can be left floating in a common motherboard design (Gfx VR keeps VAXG from floating) if the VR is stuffed

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Title: PROCESSOR(6/7) PWR

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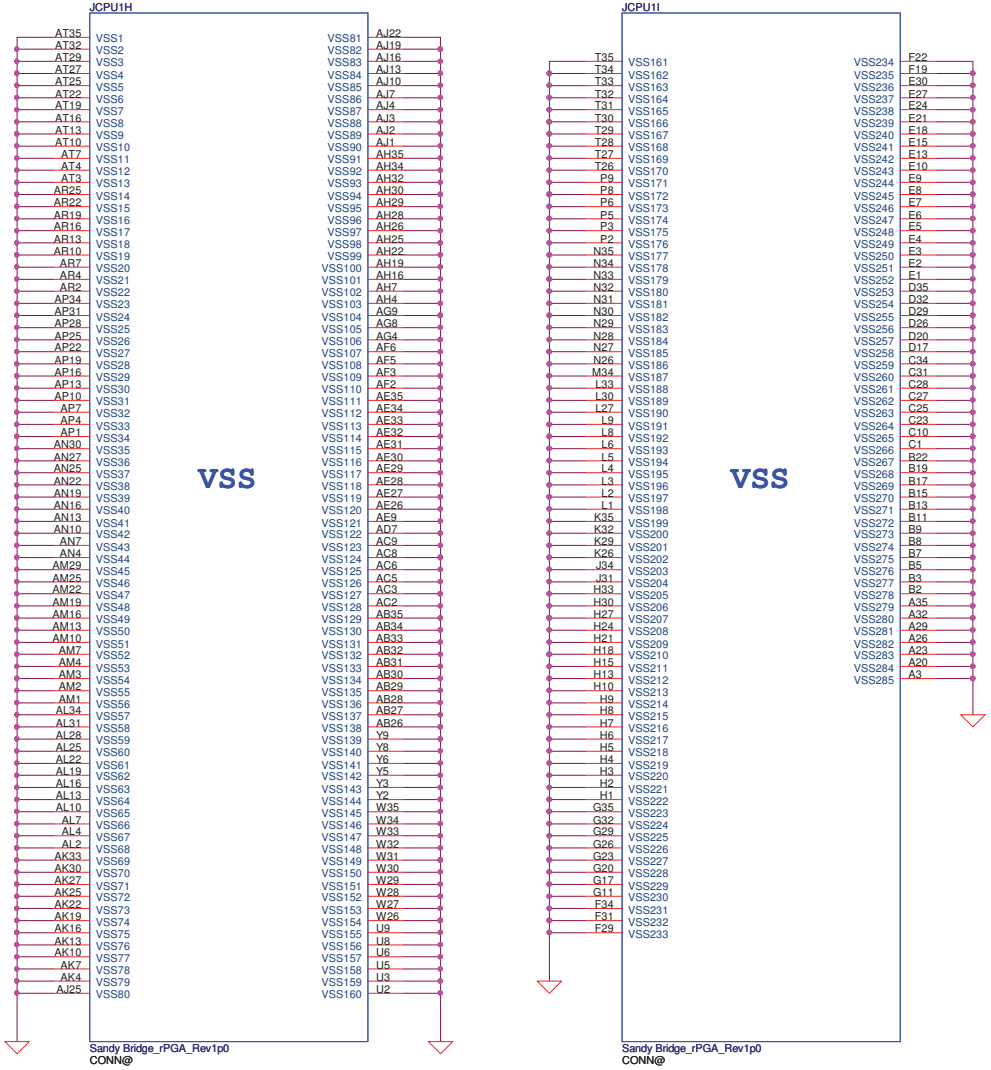

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Title: PROCESSOR(7/7) VSS

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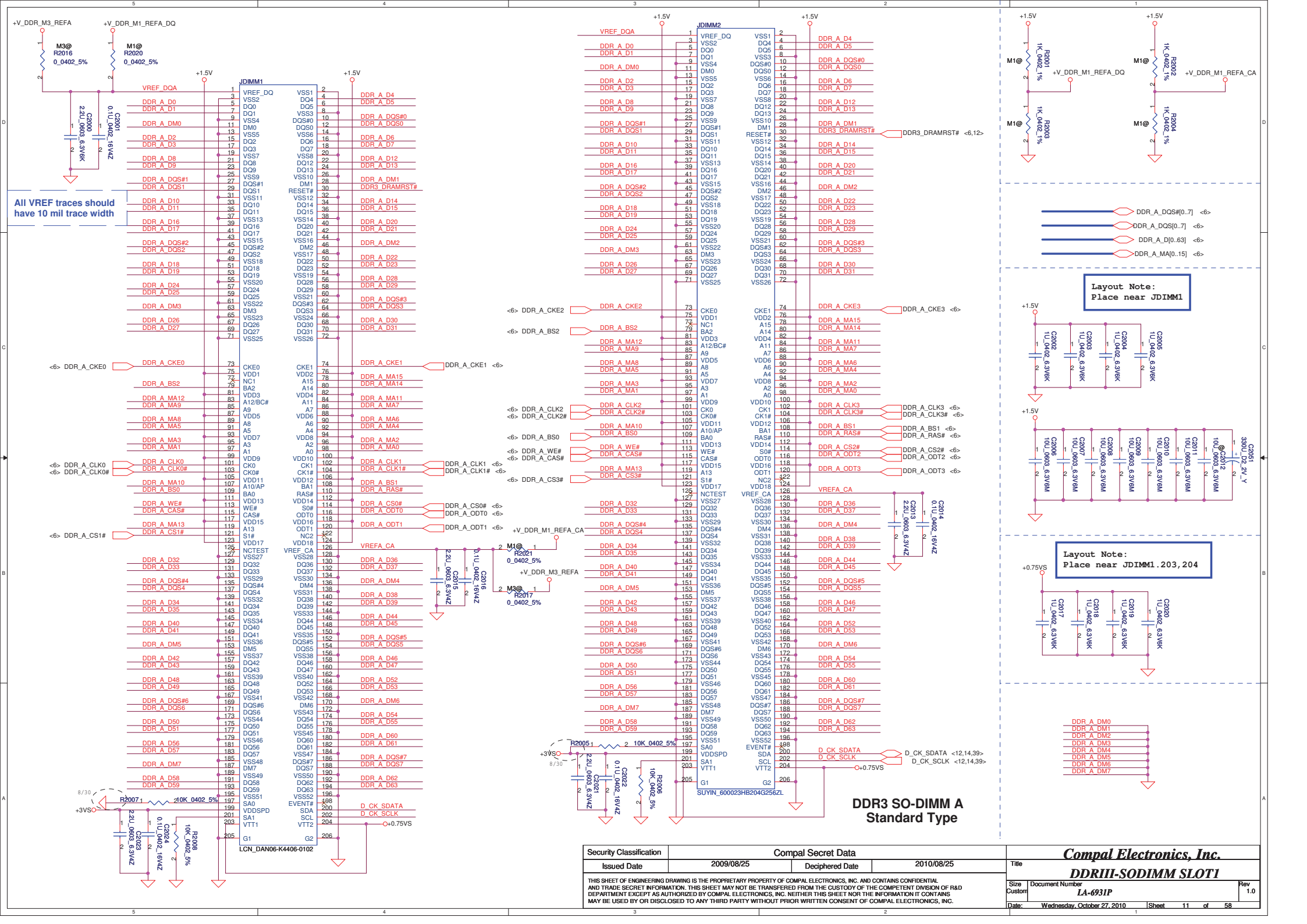

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Title: **DDRIII-SODIMM SLOT1**

Size	Document Number	Rev
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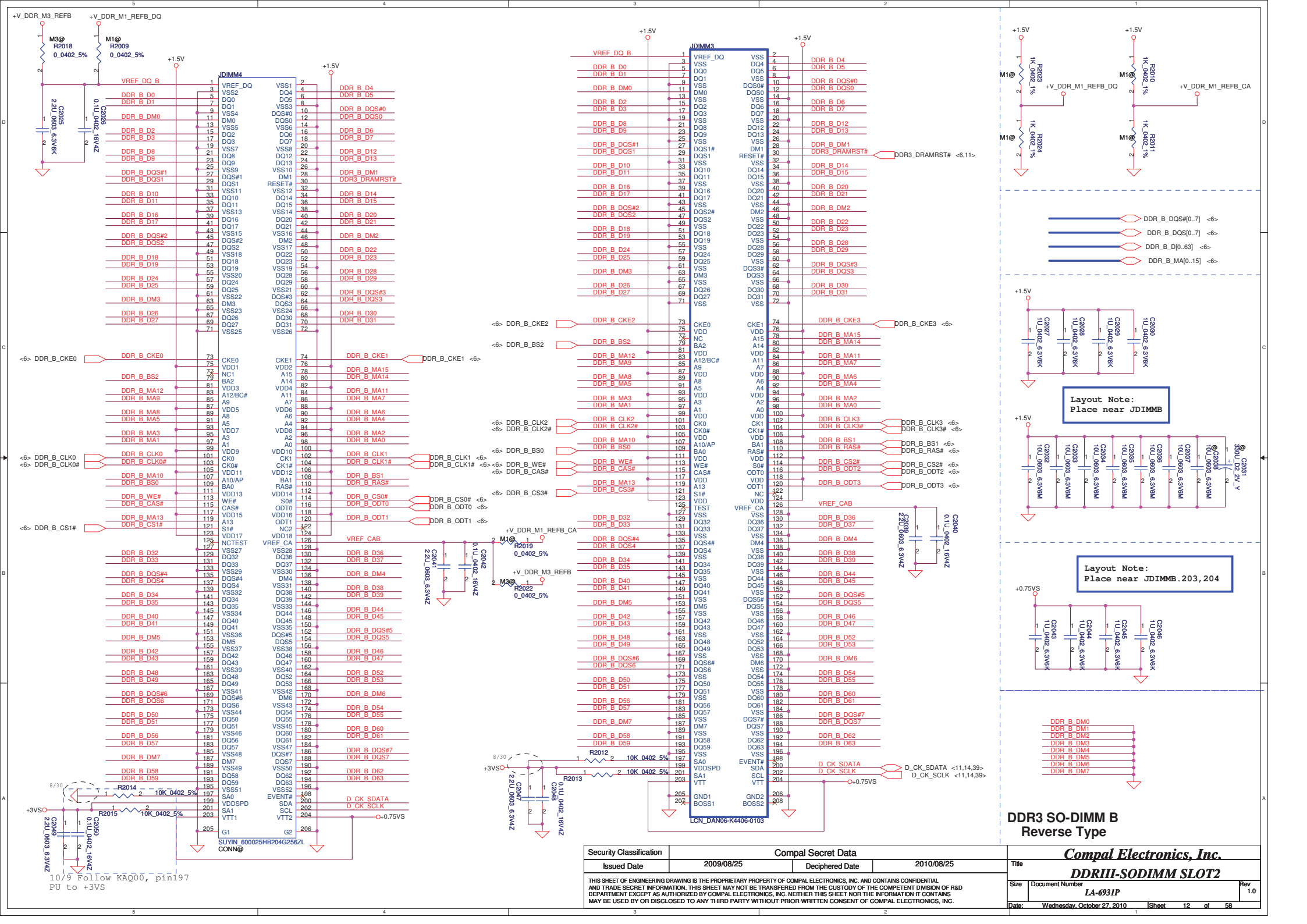

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Compal Electronics, Inc.			
Title	DDRIII-SODIMM SLOT2		
Size	Document Number		Rev
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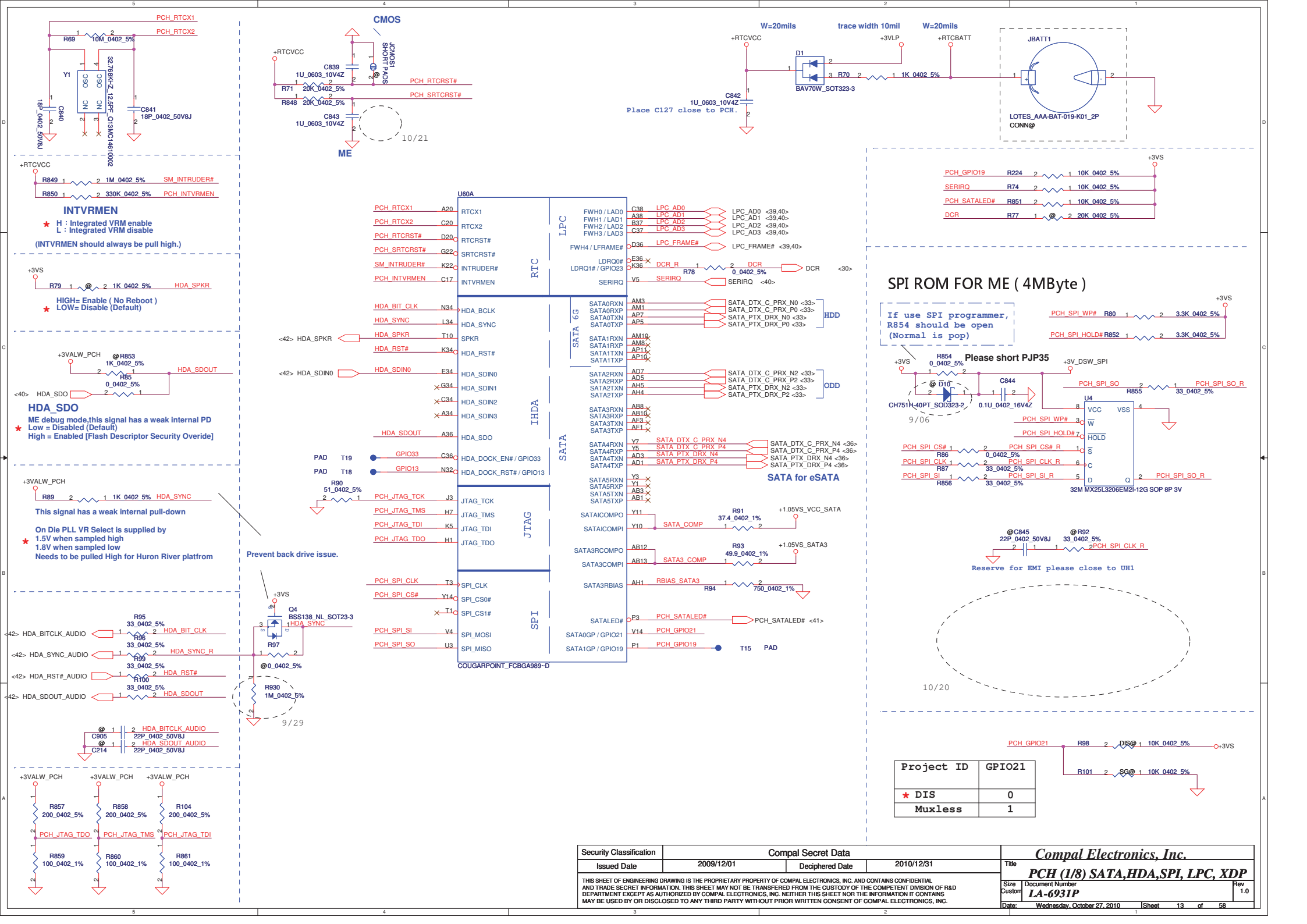
PCH_RTCX1
PCH_RTCX2
R69 10M_0402_5%
Y1 32.768KHZ_12.5PF_Q13MC14610002
C840 18P_0402_50V8J
C841 18P_0402_50V8J
+RTCVCC
R849 1M_0402_5% SM_INTRUDER#
R850 330K_0402_5% PCH_INTVRMEN
INTVRMEN
★ H : Integrated VRM enable
L : Integrated VRM disable
(INTVRMEN should always be pull high.)
+3VS
R79 @ 1K_0402_5% HDA_SPKR
★ HIGH= Enable (No Reboot)
LOW= Disable (Default)
+3VALW_PCH
@R853 1K_0402_5%
R85 0_0402_5% HDA_SDOUT
<40> HDA_SDO
HDA_SDO
ME debug mode,this signal has a weak internal PD
★ Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Overide]
+3VALW_PCH
R89 1K_0402_5% HDA_SYNC
This signal has a weak internal pull-down
On Die PLL VR Select is supplied by
★ 1.5V when sampled high
1.8V when sampled low
Needs to be pulled High for Huron River platfrom
CMOS
+RTCVCC
C839 1U_0603_10V4Z
JCMOS1 SHORT PADS
R71 20K_0402_5% PCH_RTCRST#
R848 20K_0402_5% PCH_SRTCRST#
C843 1U_0603_10V4Z
10/21
ME
W=20mils
trace width 10mil
W=20mils
+RTCVCC
+3VLP
+RTCBATT
D1 BAV70W_SOT323-3
R70 1K_0402_5%
C842 1U_0603_10V4Z
Place C127 close to PCH.
JBATT1
LOTES_AAA-BAT-019-K01_2P
CONN@
U60A
PCH_RTCX1 A20 RTCX1
PCH_RTCX2 C20 RTCX2
PCH_RTCRST# D20 RTCRST#
PCH_SRTCRST# G22 SRTCRST#
SM_INTRUDER# K22 INTRUDER#
PCH_INTVRMEN C17 INTVRMEN
RTC
LPC
FWH0 / LAD0 C38 LPC_AD0 LPC_AD0 <39,40>
FWH1 / LAD1 A38 LPC_AD1 LPC_AD1 <39,40>
FWH2 / LAD2 B37 LPC_AD2 LPC_AD2 <39,40>
FWH3 / LAD3 C37 LPC_AD3 LPC_AD3 <39,40>
FWH4 / LFRAME# D36 LPC_FRAME# LPC_FRAME# <39,40>
LDRQ0# E36
LDRQ1# / GPIO23 K36 DCR_R R78 0_0402_5% DCR DCR <30>
SERIRQ V5 SERIRQ SERIRQ <40>
HDA_BIT_CLK N34 HDA_BCLK
HDA_SYNC L34 HDA_SYNC
<42> HDA_SPKR HDA_SPKR T10 SPKR
HDA_RST# K34 HDA_RST#
<42> HDA_SDIN0 HDA_SDIN0 E34 HDA_SDIN0
G34 HDA_SDIN1
C34 HDA_SDIN2
A34 HDA_SDIN3
HDA_SDOUT A36 HDA_SDO
IHDA
PAD T19 GPIO33 C36 HDA_DOCK_EN# / GPIO33
PAD T18 GPIO13 N32 HDA_DOCK_RST# / GPIO13
R90 51_0402_5%
PCH_JTAG_TCK J3 JTAG_TCK
PCH_JTAG_TMS H7 JTAG_TMS
PCH_JTAG_TDI K5 JTAG_TDI
PCH_JTAG_TDO H1 JTAG_TDO
JTAG
PCH_SPI_CLK T3 SPI_CLK
PCH_SPI_CS# Y14 SPI_CS0#
T1 SPI_CS1#
PCH_SPI_SI V4 SPI_MOSI
PCH_SPI_SO U3 SPI_MISO
SPI
COUGARPOINT_FCBGA989~D
SATA
SATA 6G
SATA0RXN AM3 SATA_DTX_C_PRX_N0 <33>
SATA0RXP AM1 SATA_DTX_C_PRX_P0 <33>
SATA0TXN AP7 SATA_PTX_DRX_N0 <33>
SATA0TXP AP5 SATA_PTX_DRX_P0 <33>
HDD
SATA1RXN AM10
SATA1RXP AM8
SATA1TXN AP11
SATA1TXP AP10
SATA2RXN AD7 SATA_DTX_C_PRX_N2 <33>
SATA2RXP AD5 SATA_DTX_C_PRX_P2 <33>
SATA2TXN AH5 SATA_PTX_DRX_N2 <33>
SATA2TXP AH4 SATA_PTX_DRX_P2 <33>
ODD
SATA3RXN AB8
SATA3RXP AB10
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN Y7 SATA_DTX_C_PRX_N4 SATA_DTX_C_PRX_N4 <36>
SATA4RXP Y5 SATA_DTX_C_PRX_P4 SATA_DTX_C_PRX_P4 <36>
SATA4TXN AD3 SATA_PTX_DRX_N4 SATA_PTX_DRX_N4 <36>
SATA4TXP AD1 SATA_PTX_DRX_P4 SATA_PTX_DRX_P4 <36>
SATA for eSATA
SATA5RXN Y3
SATA5RXP Y1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO Y11 R91 37.4_0402_1% +1.05VS_VCC_SATA
SATAICOMPI Y10 SATA_COMP
SATA3RCOMPO AB12 R93 49.9_0402_1% +1.05VS_SATA3
SATA3COMPI AB13 SATA3_COMP
SATA3RBIAS AH1 RBIAS_SATA3 R94 750_0402_1%
SATALED# P3 PCH_SATALED# PCH_SATALED# <41>
SATA0GP / GPIO21 V14 PCH_GPIO21
SATA1GP / GPIO19 P1 PCH_GPIO19 T15 PAD
Prevent back drive issue.
+3VS
Q4 BSS138_NL_SOT23-3
HDA_SYNC
R97 @0_0402_5%
R930 1M_0402_5%
9/29
<42> HDA_BITCLK_AUDIO R95 33_0402_5% HDA_BIT_CLK
<42> HDA_SYNC_AUDIO R96 33_0402_5% HDA_SYNC_R
<42> HDA_RST#_AUDIO R99 33_0402_5% HDA_RST#
<42> HDA_SDOUT_AUDIO R100 33_0402_5% HDA_SDOUT
@ C905 22P_0402_50V8J HDA_BITCLK_AUDIO
@ C214 22P_0402_50V8J HDA_SDOUT_AUDIO
+3VALW_PCH
R857 200_0402_5% PCH_JTAG_TDO
R858 200_0402_5% PCH_JTAG_TMS
R104 200_0402_5% PCH_JTAG_TDI
R859 100_0402_1%
R860 100_0402_1%
R861 100_0402_1%
+3VS
PCH_GPIO19 R224 10K_0402_5%
SERIRQ R74 10K_0402_5%
PCH_SATALED# R851 10K_0402_5%
DCR R77 @ 20K_0402_5%
SPI ROM FOR ME (4MByte)
If use SPI programmer, R854 should be open (Normal is pop)
+3VS
PCH_SPI_WP# R80 3.3K_0402_5%
PCH_SPI_HOLD# R852 3.3K_0402_5%
R854 0_0402_5% Please short PJP35
+3V_DSW_SPI
@ D10 CH751H-40PT_SOD323-2
C844 0.1U_0402_16V4Z
9/06
PCH_SPI_SO R855 33_0402_5% PCH_SPI_SO_R
U4
PCH_SPI_WP#
PCH_SPI_HOLD#
PCH_SPI_CS# R86 0_0402_5% PCH_SPI_CS#_R
PCH_SPI_CLK R87 33_0402_5% PCH_SPI_CLK_R
PCH_SPI_SI R856 33_0402_5% PCH_SPI_SI_R
PCH_SPI_SO_R
VCC VSS W HOLD S C D Q
32M MX25L3206EM2I-12G SOP 8P 3V
@C845 22P_0402_50V8J
@R92 33_0402_5% PCH_SPI_CLK_R
Reserve for EMI please close to UH1
10/20
PCH_GPIO21 R98 DIS@ 10K_0402_5% +3VS
R101 SG@ 10K_0402_5%
Project ID GPIO21
★ DIS 0
Muxless 1
Security Classification Compal Secret Data
Issued Date 2009/12/01 Deciphered Date 2010/12/31
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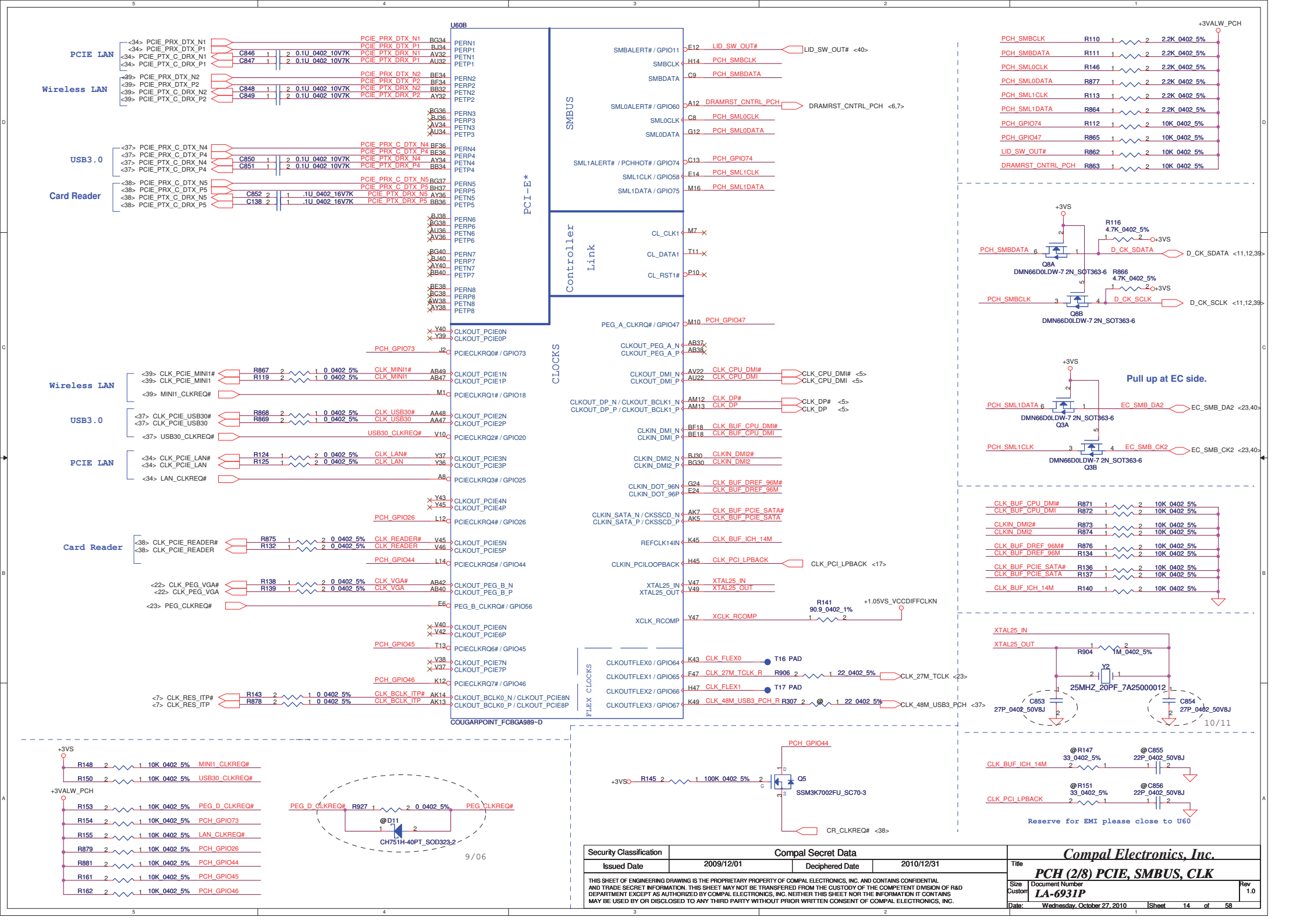
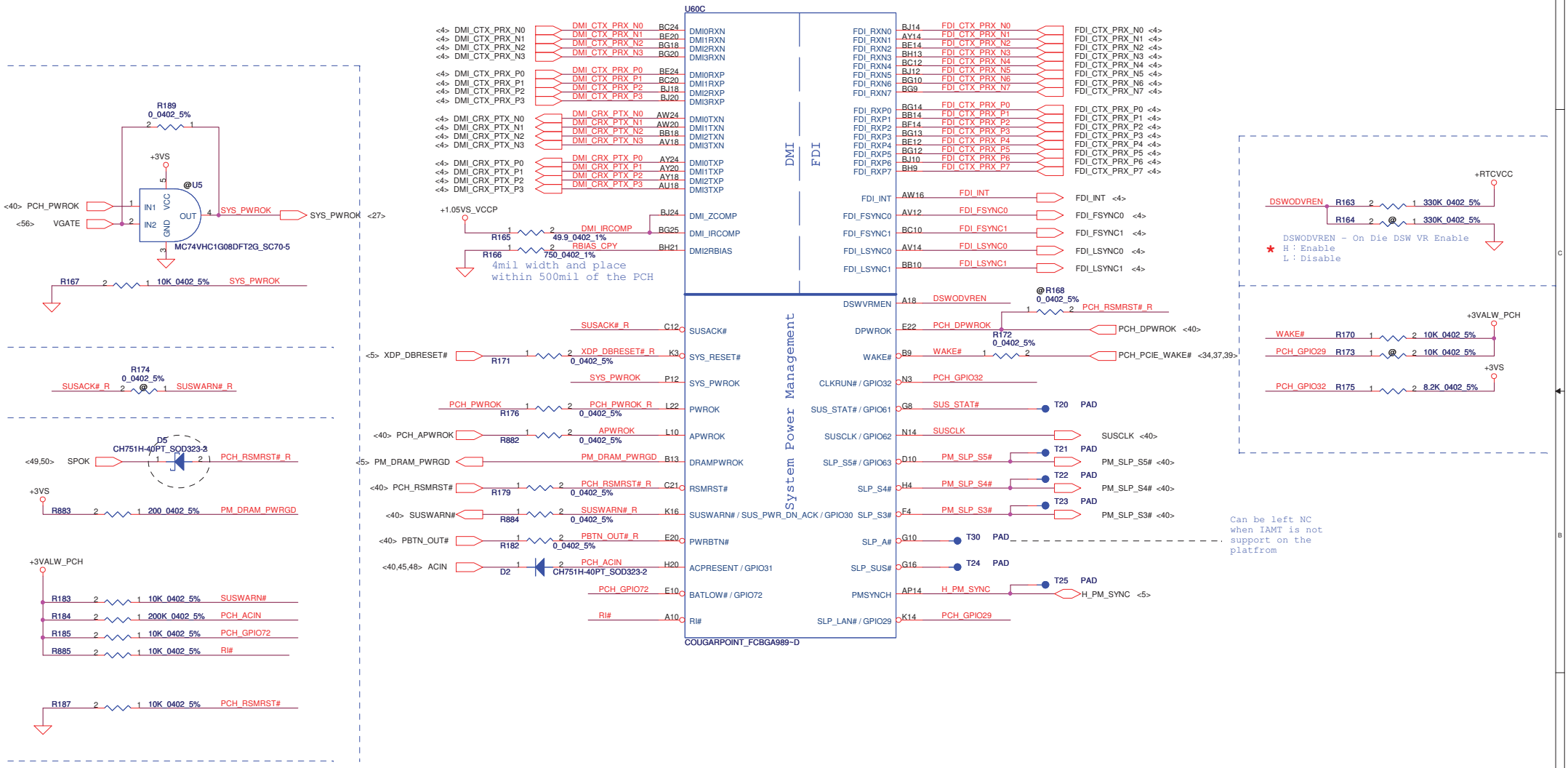
Compal Electronics, Inc.
Title PCH (1/8) SATA,HDA,SPI, LPC, XDP
Size Custom Document Number LA-6931P Rev 1.0
Date: Wednesday, October 27, 2010 Sheet 13 of 58


U60B
PCIE LAN
Wireless LAN
USB3.0
Card Reader
PCI-E*
SMBUS
Controller Link
CLOCKS
FLEX CLOCKS
COUGARPOINT_FCBGA989~D
+3VALW_PCH
Pull up at EC side.
Reserve for EMI please close to U60
Compal Secret Data
Compal Electronics, Inc.
PCH (2/8) PCIE, SMBUS, CLK
LA-6931P
Rev 1.0
Wednesday, October 27, 2010
Sheet 14 of 58
2009/12/01
2010/12/31
10/11
9/06



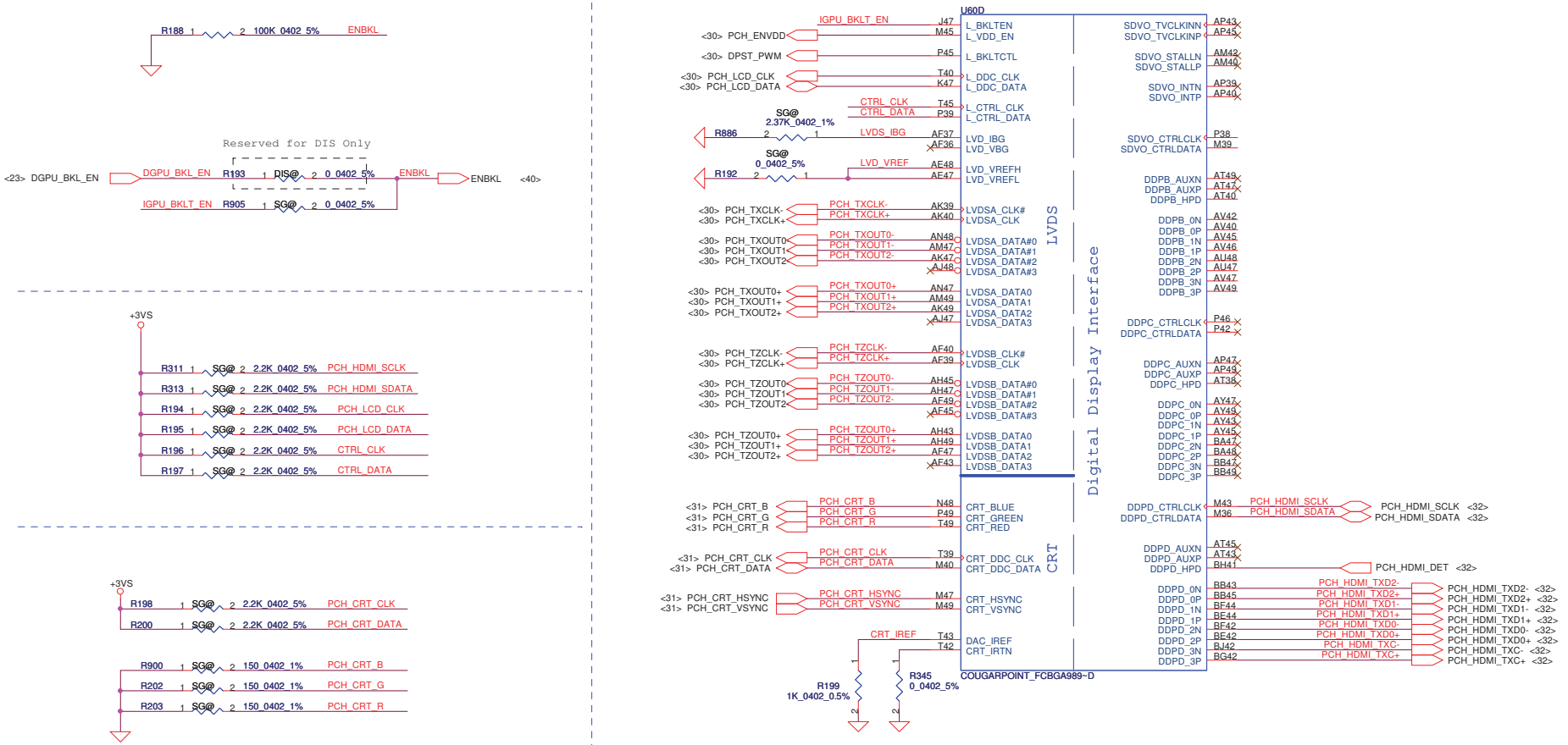
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (3/8) DMI,FDI,PM,

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 15 of 58



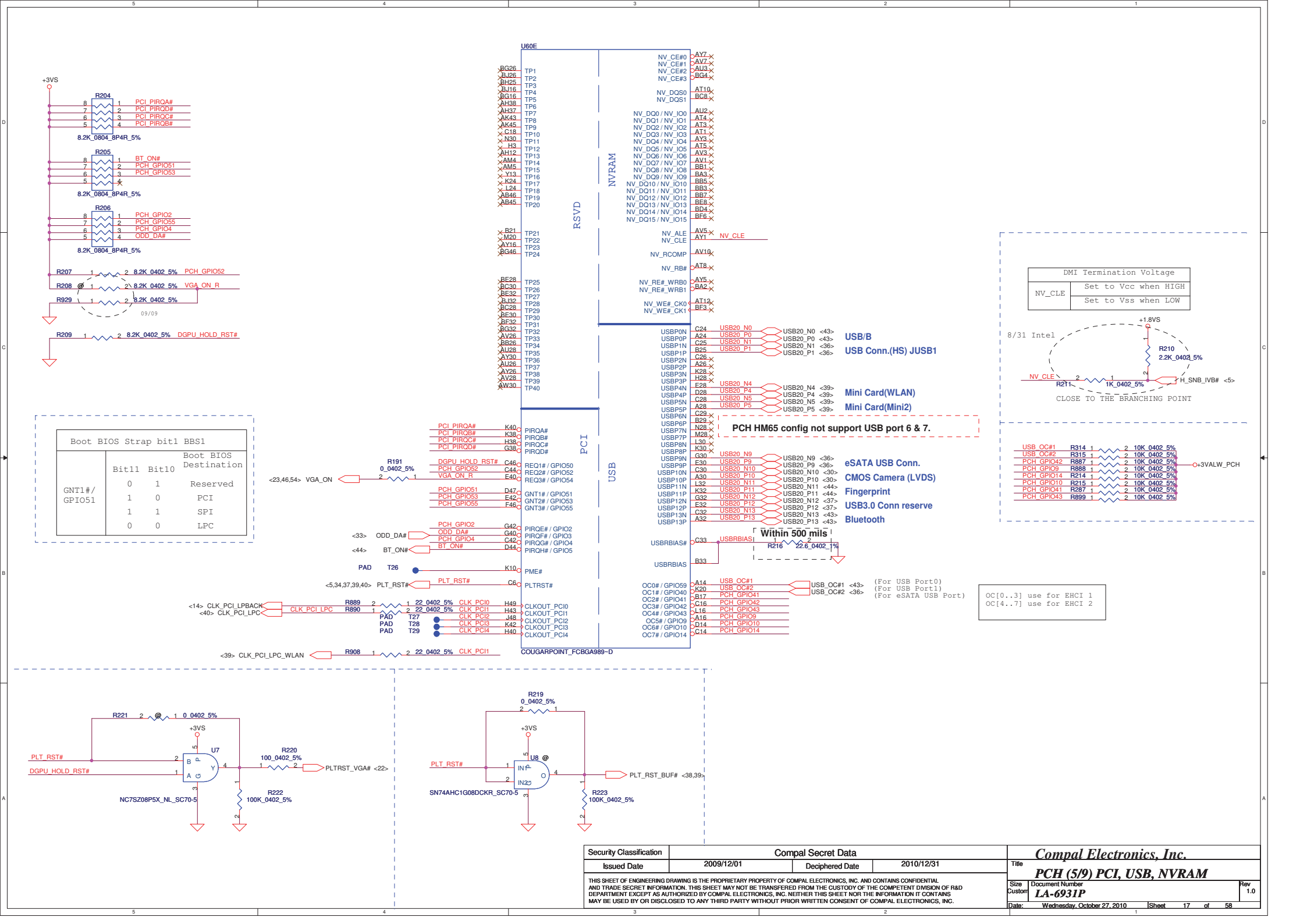
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 16 of 58



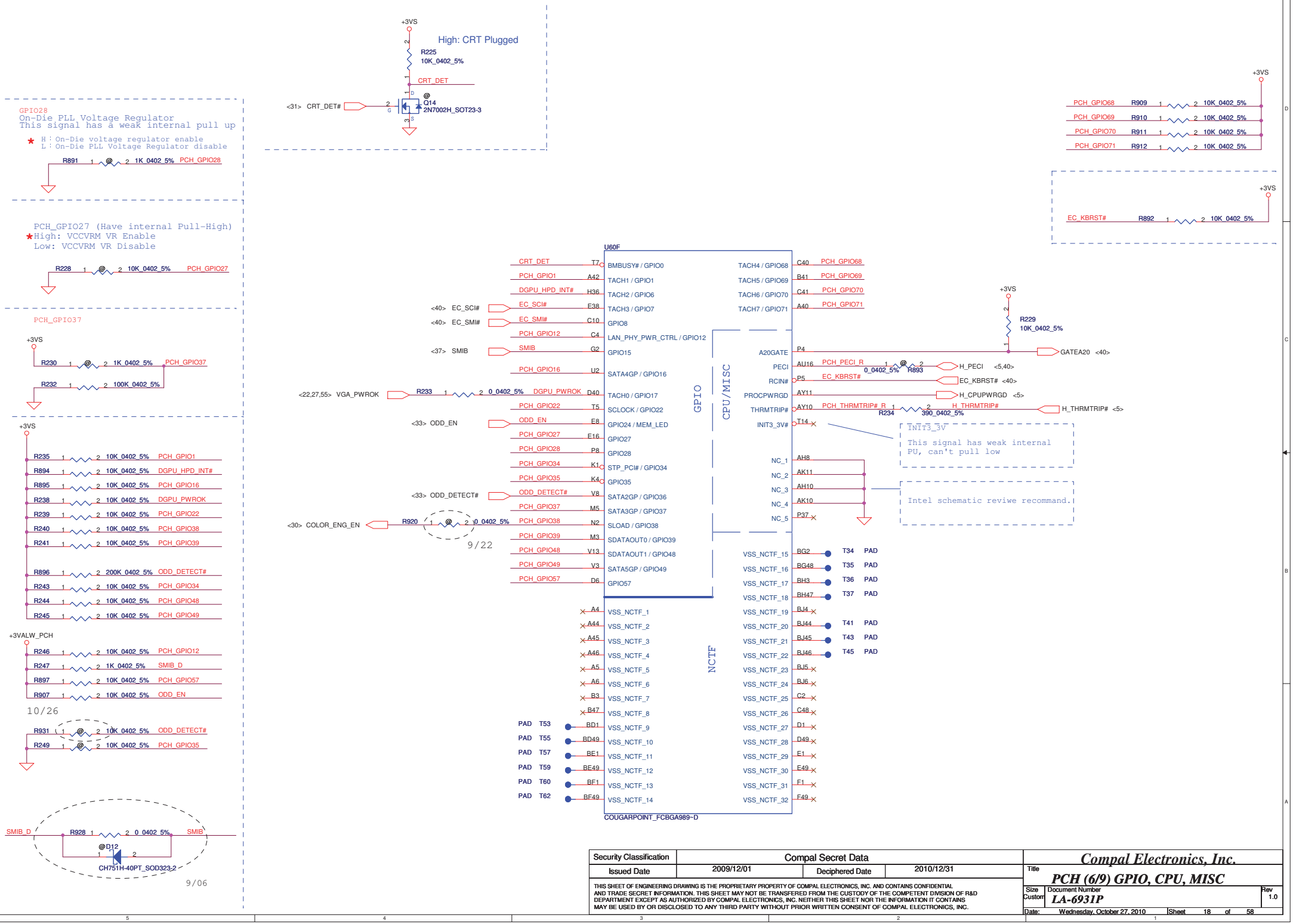
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, NVRAM

Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 17 of 58



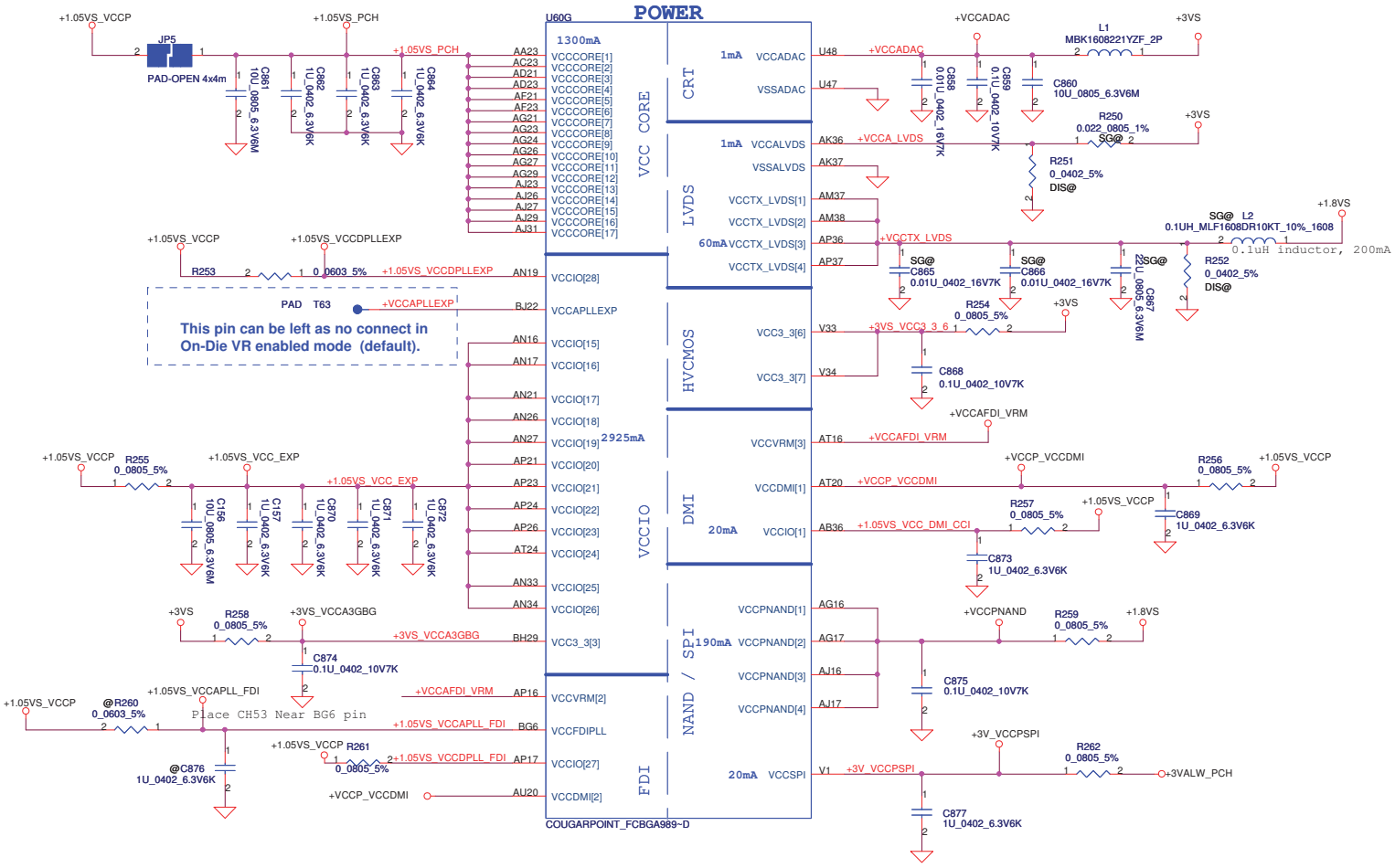
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

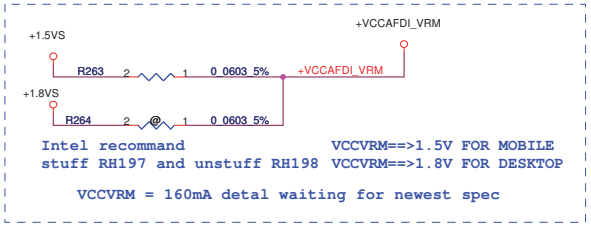
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 18 of 58





PCH Power Rail Table

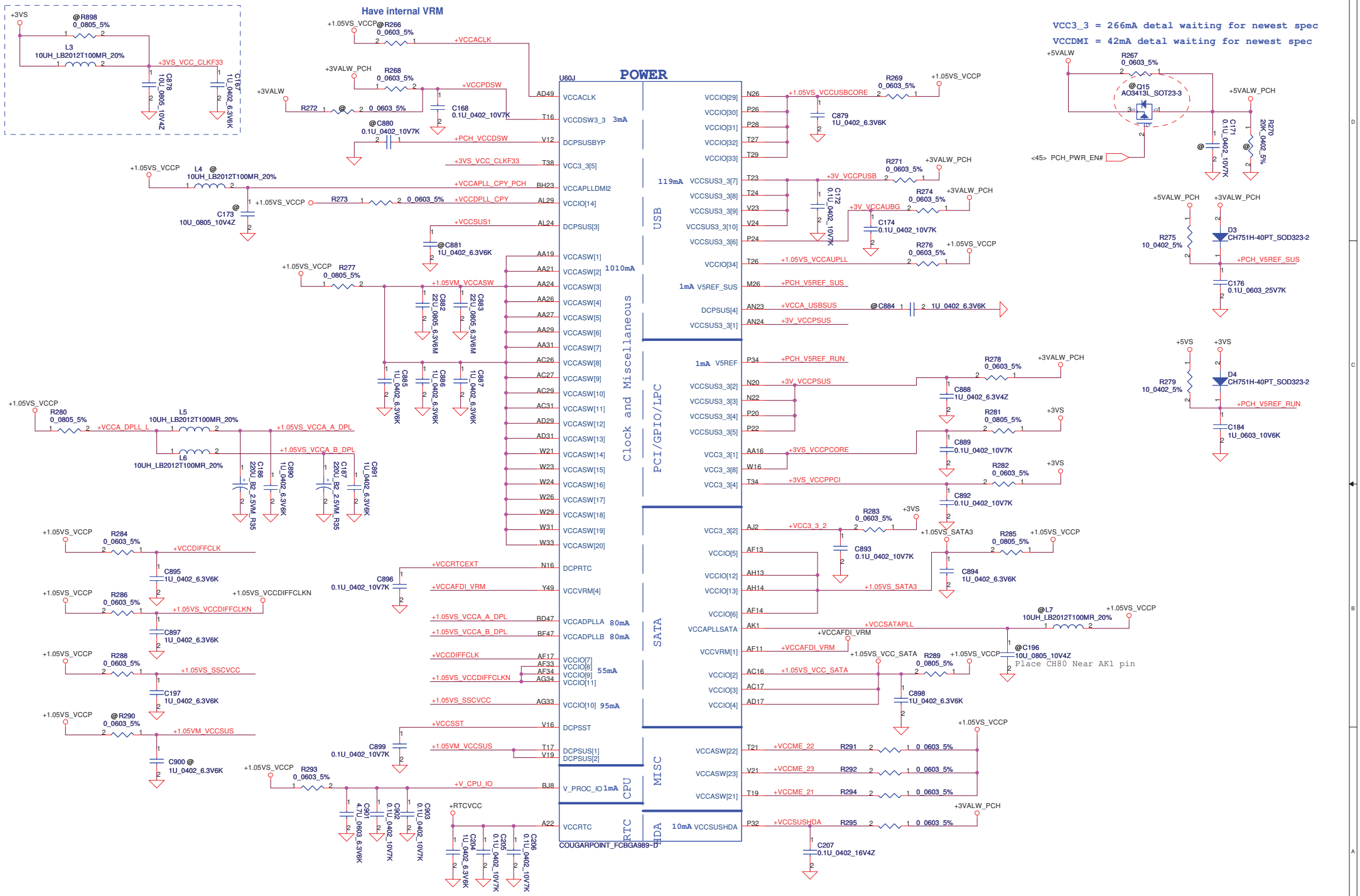
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 19 of 58



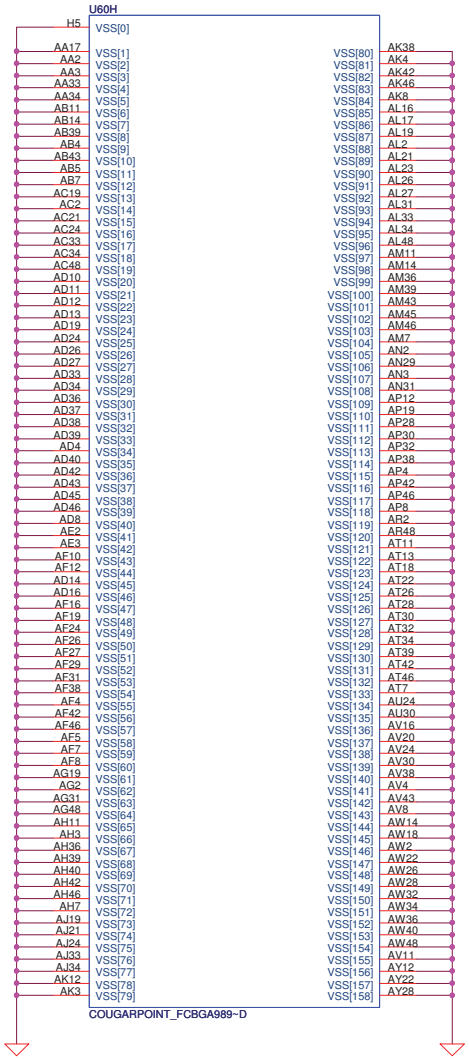
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

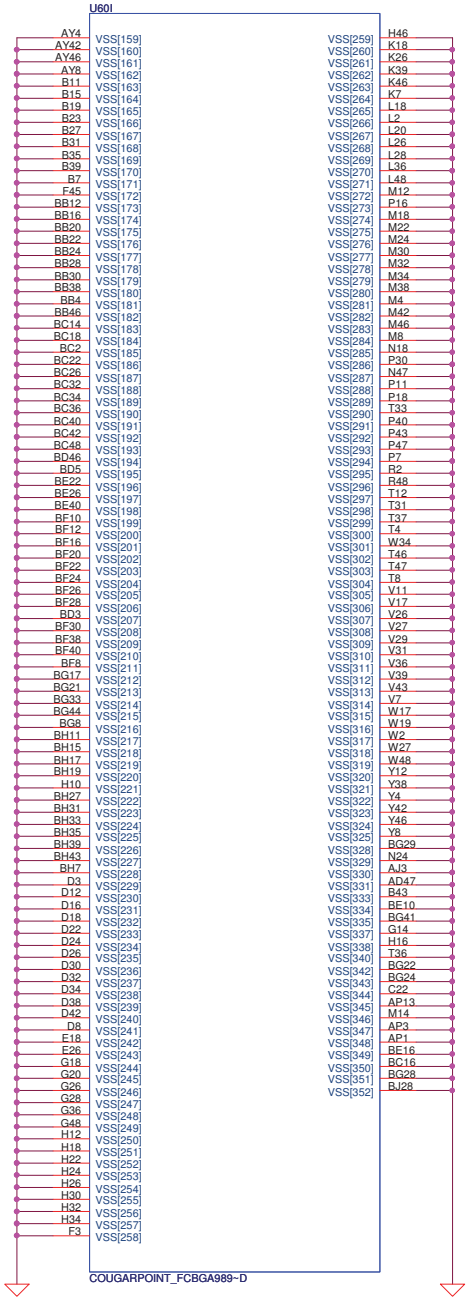
Compal Electronics, Inc.

Title: PCH (8/9) PWR

Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 20 of 58





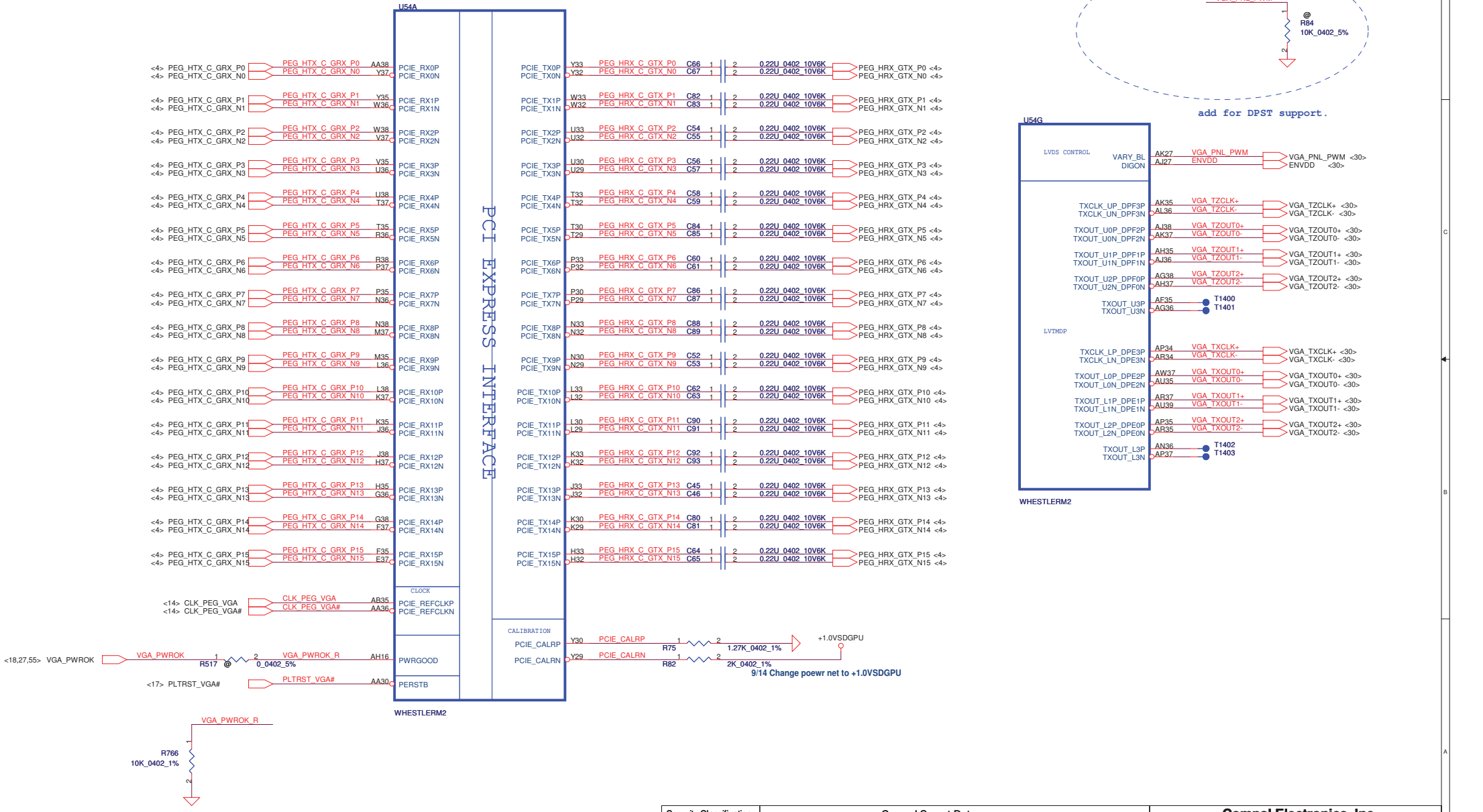
Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PCH (9/9) VSS

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 21 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_ PCIE / LVDS**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 22 of 58

Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
CONFIG[1] CONFIG[2] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. memory apertures CONFIG[3:0] 128 MB 000 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD(0)	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
SMS_EN_HARD	H2SYNC	Can be unconnected if not used.	0
VIP_DEVICE _STRAP_DIS	V2SYNC	Can be unconnected if not used.	0

VRAM \ Location	VRAM_ID2	VRAM_ID1	VRAM_ID0	
Hynix(8pcs) 1GB (old) H5TQ1G63BFR-12C	O	O	1	
Hynix(8pcs) 1GB (900MHz) H5TQ1G63DFR-11C	O	1	O	
Samsung(8pcs) 1GB (900MHz) K4W1G1646G-BC11 LF	O	1	1	
Hynix(8pcs) 2GB (800MHz) H5TQ2G63BFR-12C	1	O	O	
Samsung(8pcs) 2GB (800MHz) K4W2G1646C-HC12	1	O	1	

External VGA Thermal Sensor

U15 @ ADM1032ARMZ-2REEL_MSOP8

+3VS_DELAY

3/2 Change Bom structure of C120 to mount,Change value of R525 to 24k ohm(1%)

Use boradway GPU, R28 change to 0 Ohm(SD028000080)

PWR Sequence

+3VS_DELAY
VGA_CORE (VDDC)
+1.8VS

M96 only

HDMI

CRT

Y3 must install on SG mode

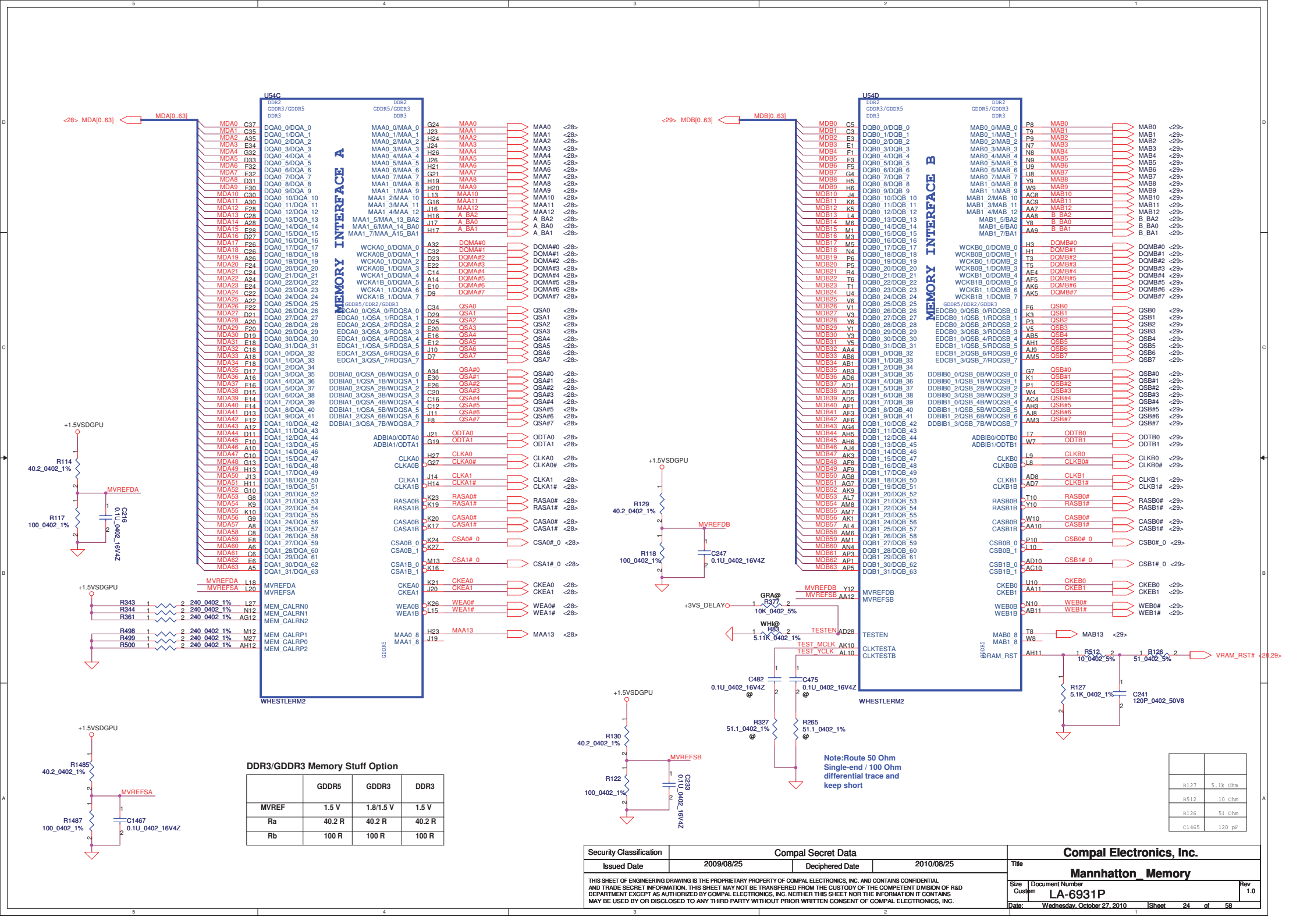
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Mannhatton_Strape/DP/HDMI//CRT

Size	Document Number	Rev
C	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 23 of 58



DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
MVREF	1.5 V	1.8/1.5 V	1.5 V
Ra	40.2 R	40.2 R	40.2 R
Rb	100 R	100 R	100 R

R127	5.1k Ohm
R512	10 Ohm
R126	51 Ohm
C1465	120 pF

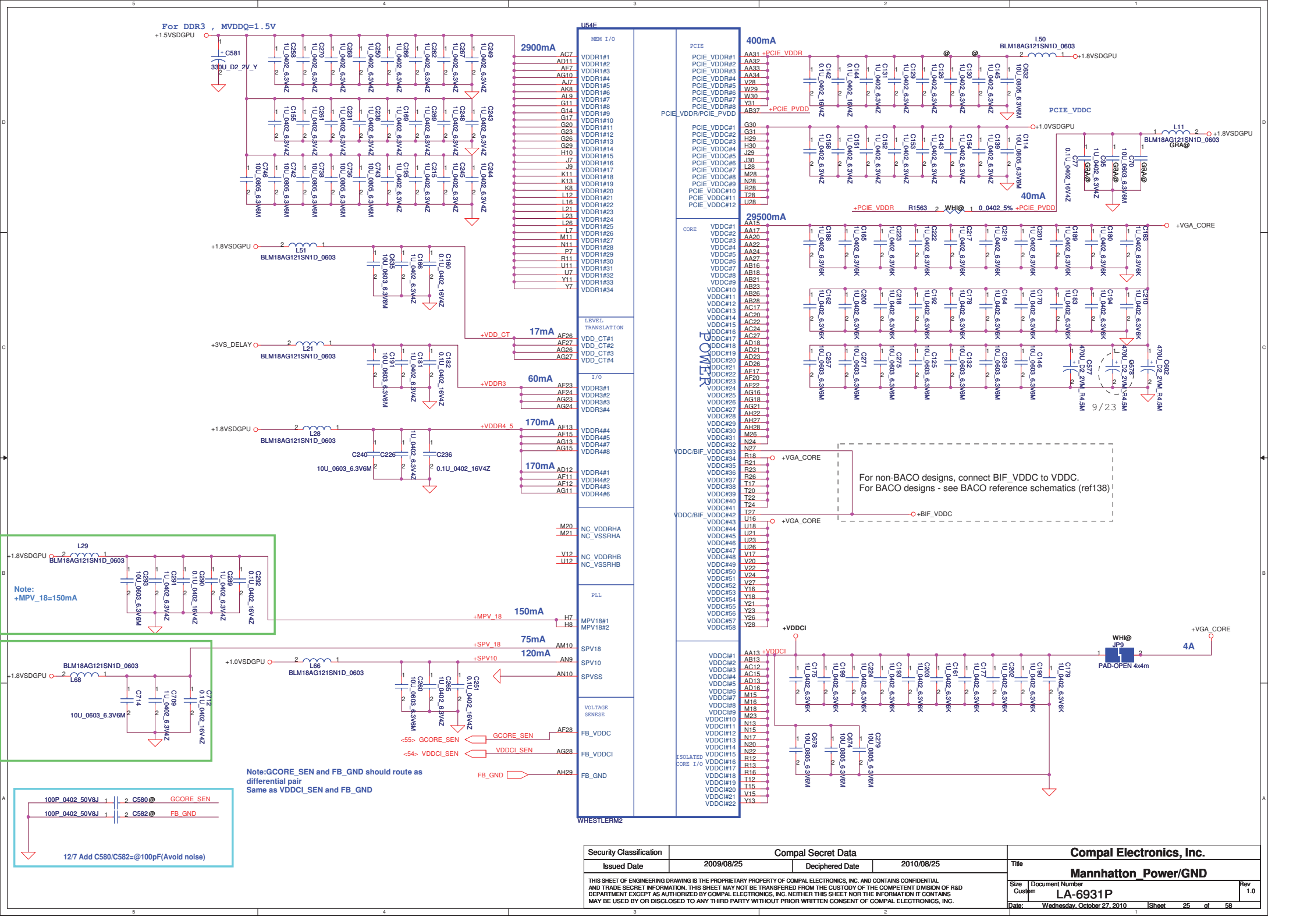
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_ Memory**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 24 of 58



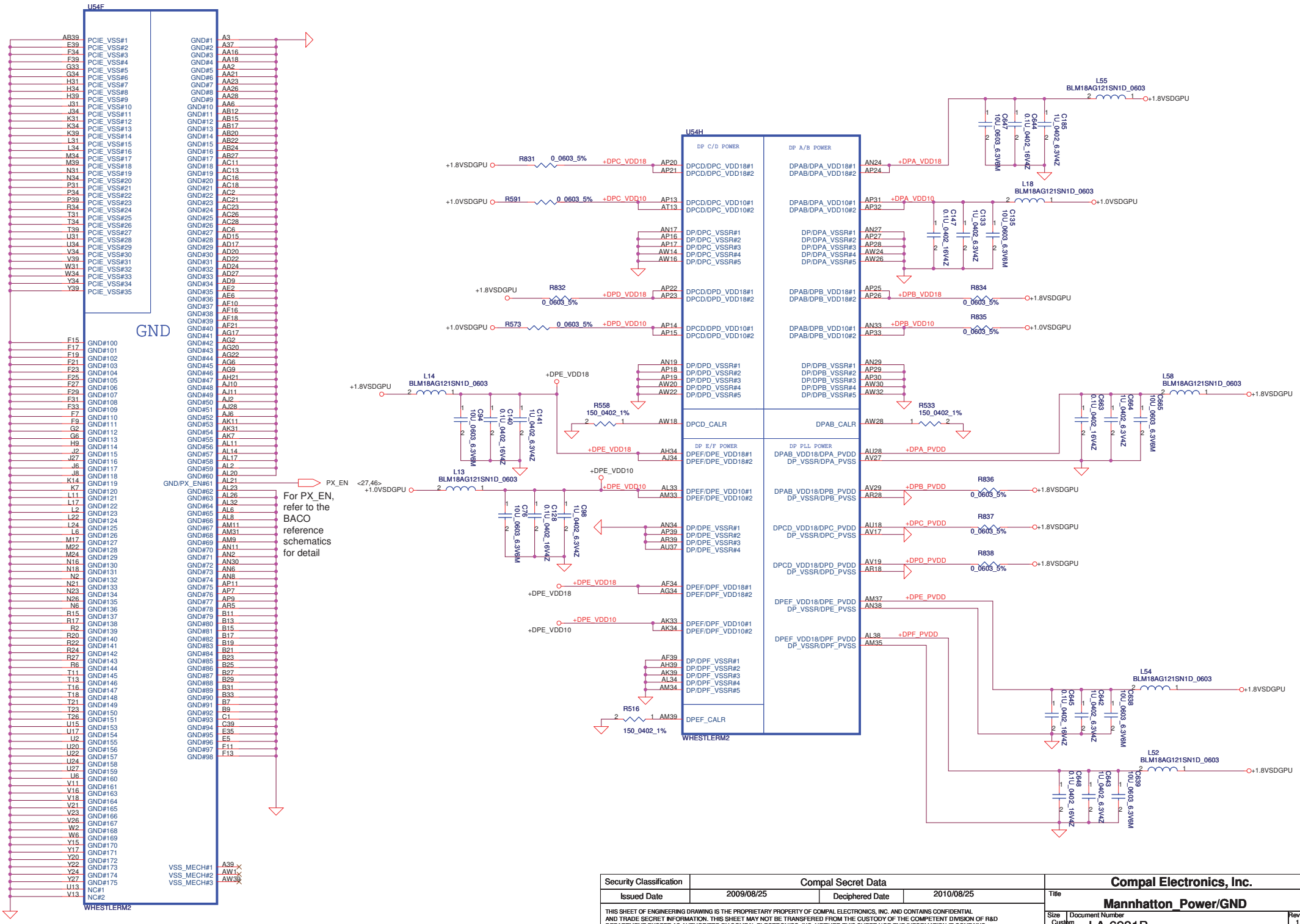
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **Mannhatton_Power/GND**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 25 of 58


U54F
GND
WHESTLERM2
U54H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
DPD_CALR
DPAB_CALR
DPEF_CALR
WHESTLERM2
For PX_EN, refer to the BACO reference schematics for detail
PX_EN
L55 BLM18AG121SN1D_0603
L18 BLM18AG121SN1D_0603
L14 BLM18AG121SN1D_0603
L13 BLM18AG121SN1D_0603
L58 BLM18AG121SN1D_0603
L54 BLM18AG121SN1D_0603
L52 BLM18AG121SN1D_0603
+1.8VSDGPU
+1.0VSDGPU
+DPC_VDD18
+DPC_VDD10
+DPD_VDD18
+DPD_VDD10
+DPE_VDD18
+DPE_VDD10
+DPA_VDD18
+DPA_VDD10
+DPB_VDD18
+DPB_VDD10
+DPA_PVDD
+DPB_PVDD
+DPC_PVDD
+DPD_PVDD
+DPE_PVDD
+DPF_PVDD
R831 0_0603_5%
R591 0_0603_5%
R832 0_0603_5%
R573 0_0603_5%
R834 0_0603_5%
R835 0_0603_5%
R836 0_0603_5%
R837 0_0603_5%
R838 0_0603_5%
R558 150_0402_1%
R533 150_0402_1%
R516 150_0402_1%
Security Classification
Compal Secret Data
Issued Date
2009/08/25
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2010/08/25
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Compal Electronics, Inc.
Title
Mannhatton_Power/GND
Size
Custom
Document Number
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Rev
1.0
Date:
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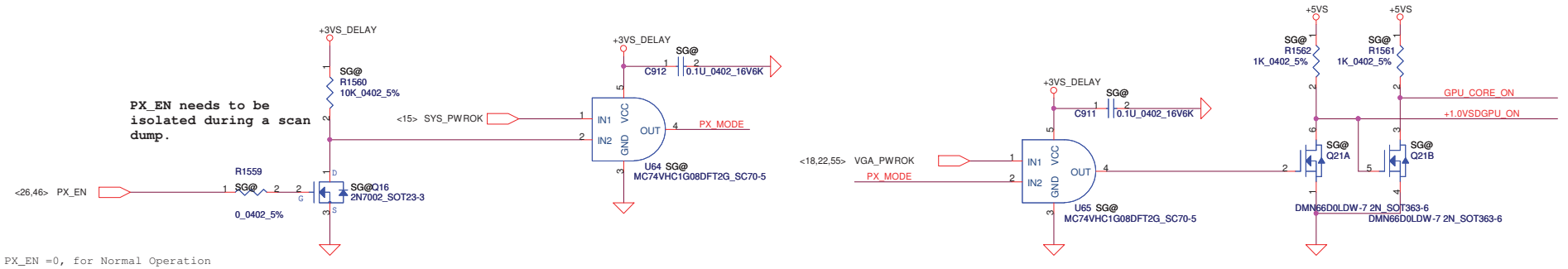
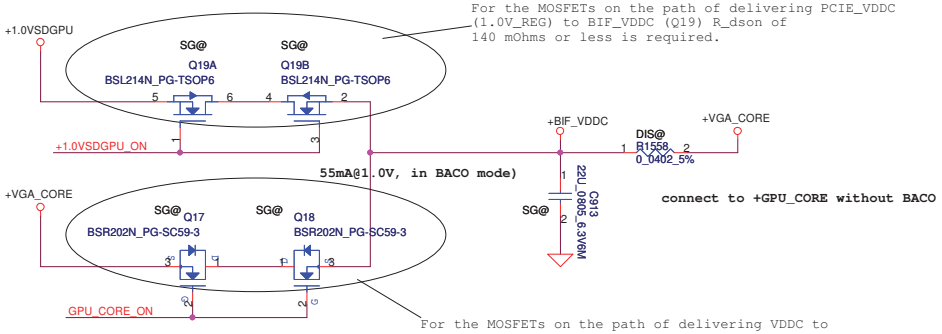
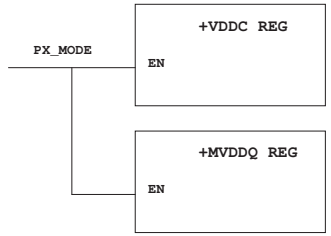
PX_MODE =1, for Normal Operation
PX_MODE =0, for BACO MODE



PX_EN =0, for Normal Operation
PX_EN =1, for BACO MODE



	Voltage	In BACO mode
VDDR1	1.5V	OFF
VDDC/VDDCI	0.85~1.15V	OFF
others		ON



power on sequence:
(1) +3VS_Delay ----> +VDDC ----> +1.8VS
(> 0ms) (reach 90%)

(2) +3VS_Delay ----> +1.8VS ----> +VDDC
(> 0ms) (reach 90%)

Security Classification	Compal Secret Data		
Issued Date	2009/11/12	Deciphered Date	2010/11/12

Compal Electronics, Inc.

Title: BACO

Size	Document Number	Rev
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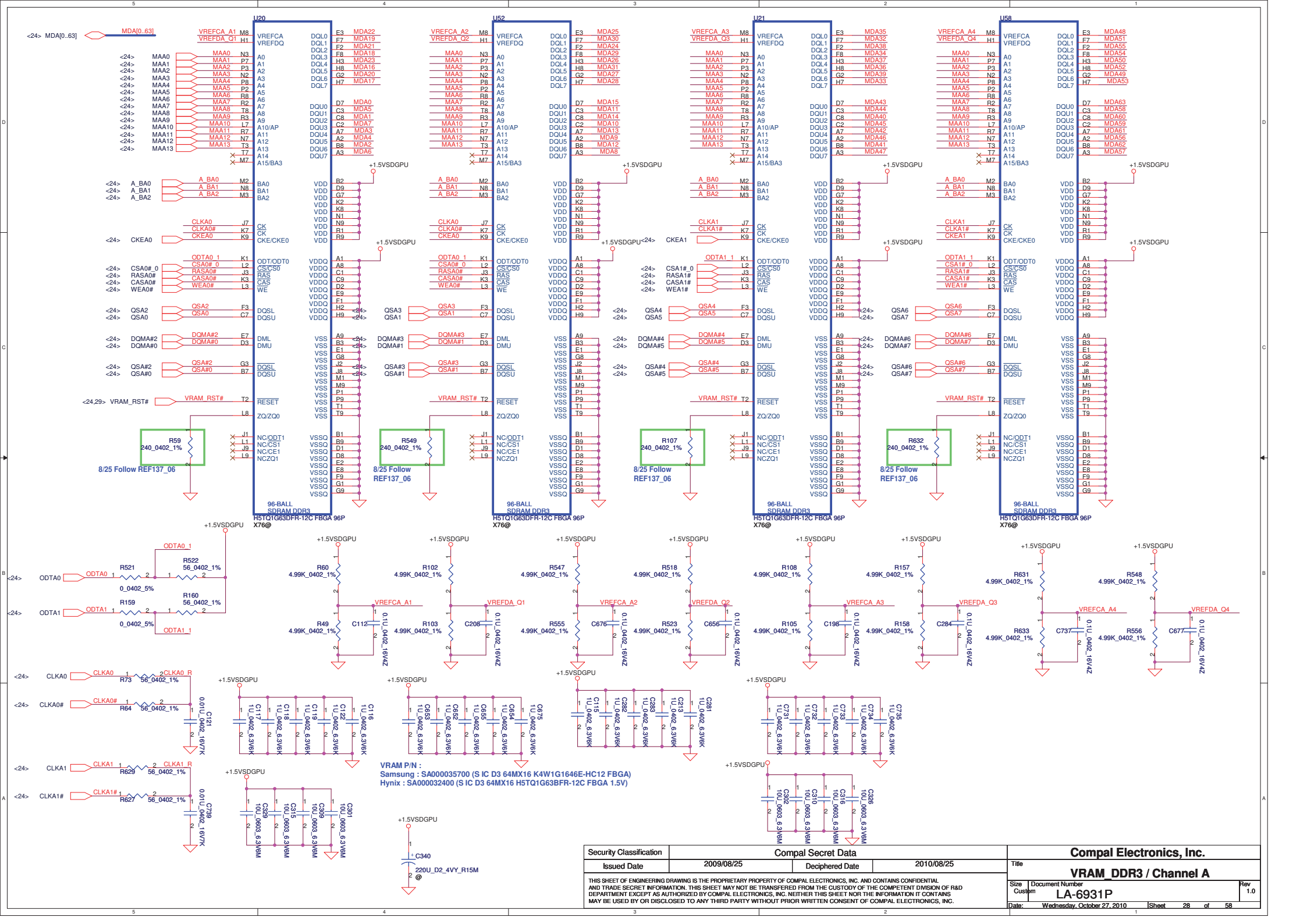
Date: Wednesday, October 27, 2010 Sheet 27 of 58



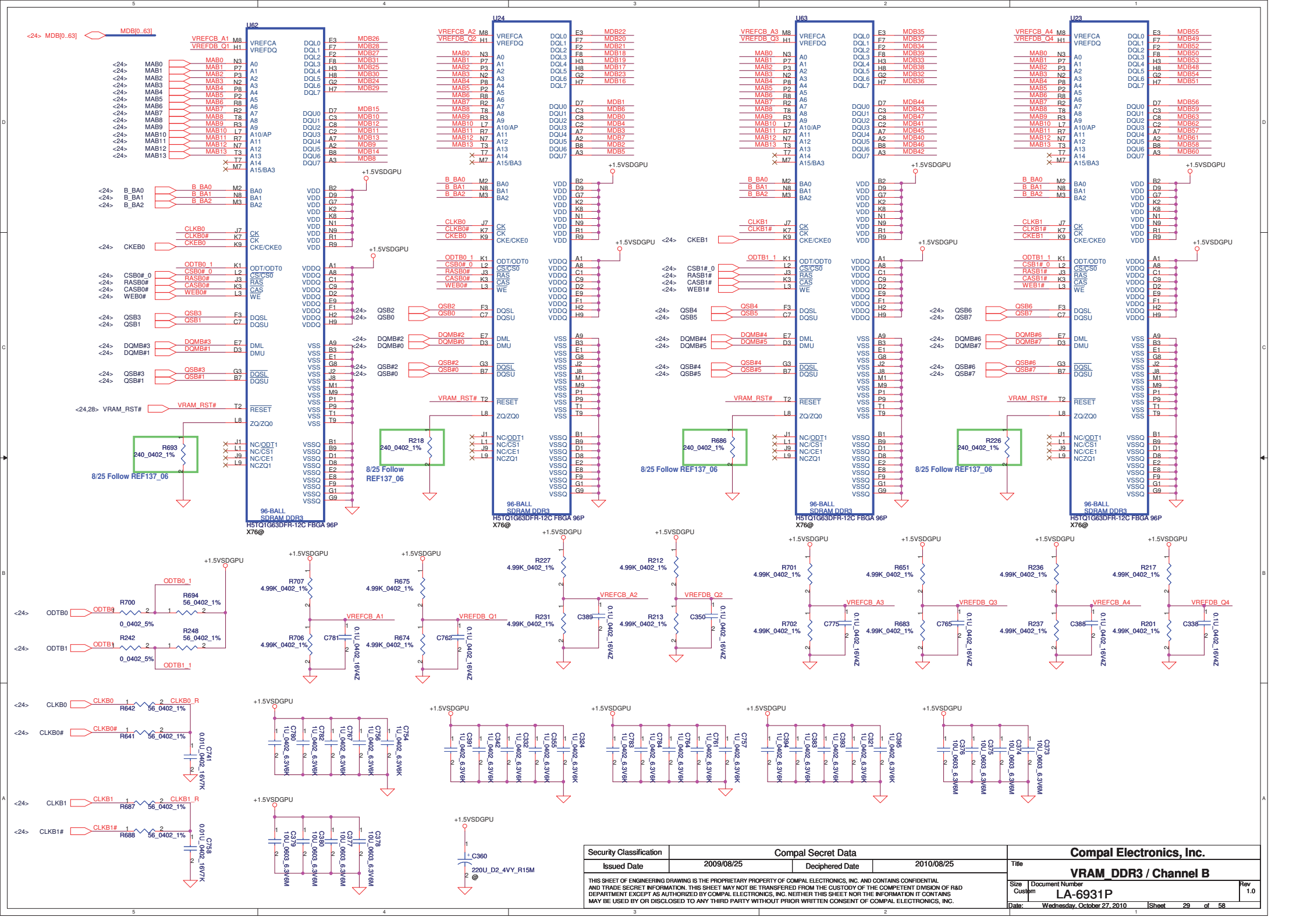
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **VRAM_DDR3 / Channel A**

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 28 of 58



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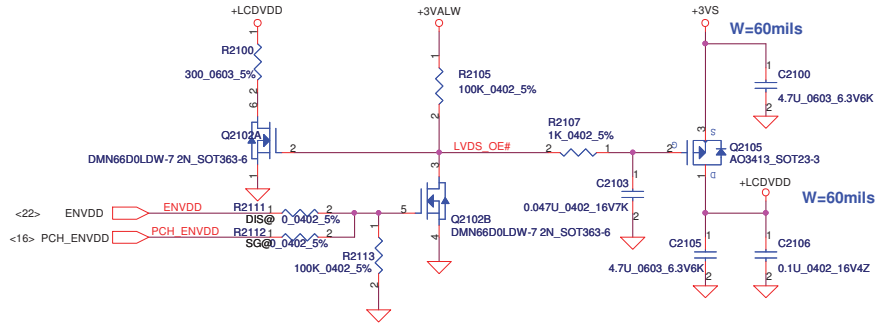
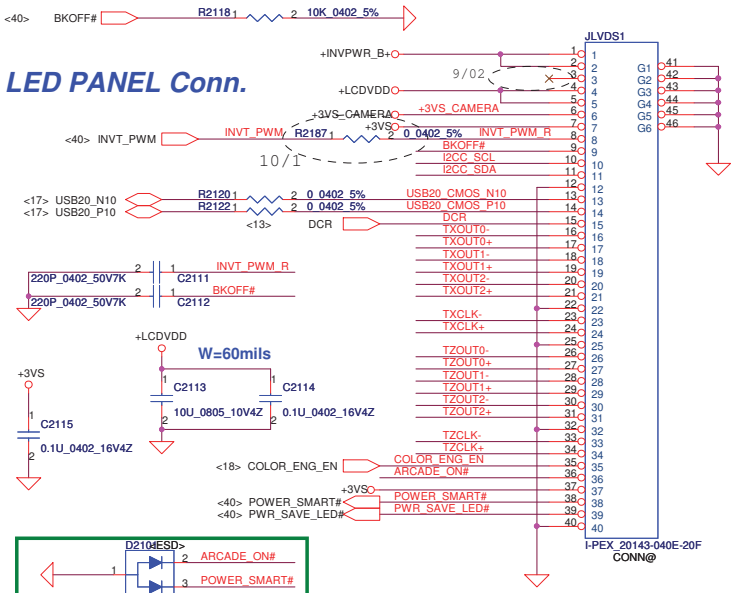
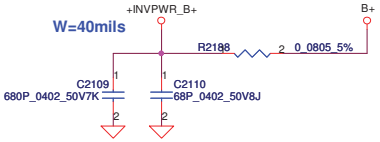
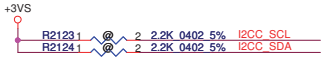
LCD POWER CIRCUIT

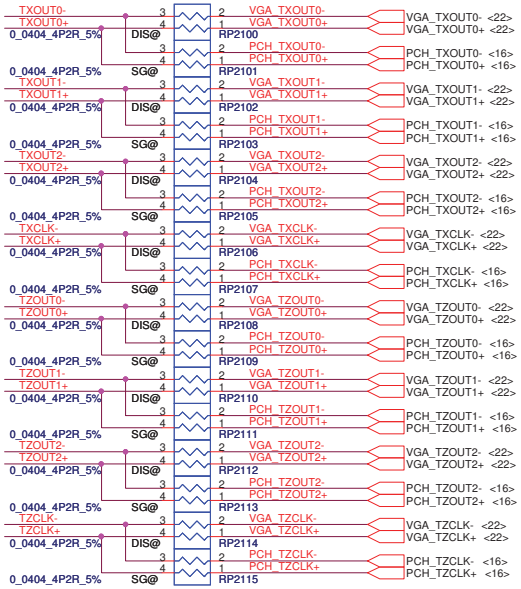


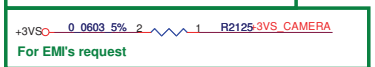
LED PANEL Conn.

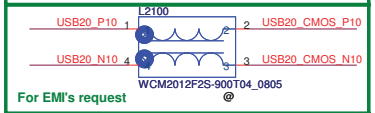


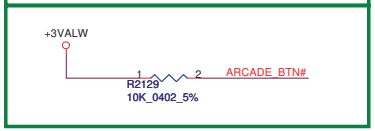


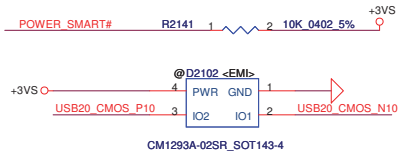












Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

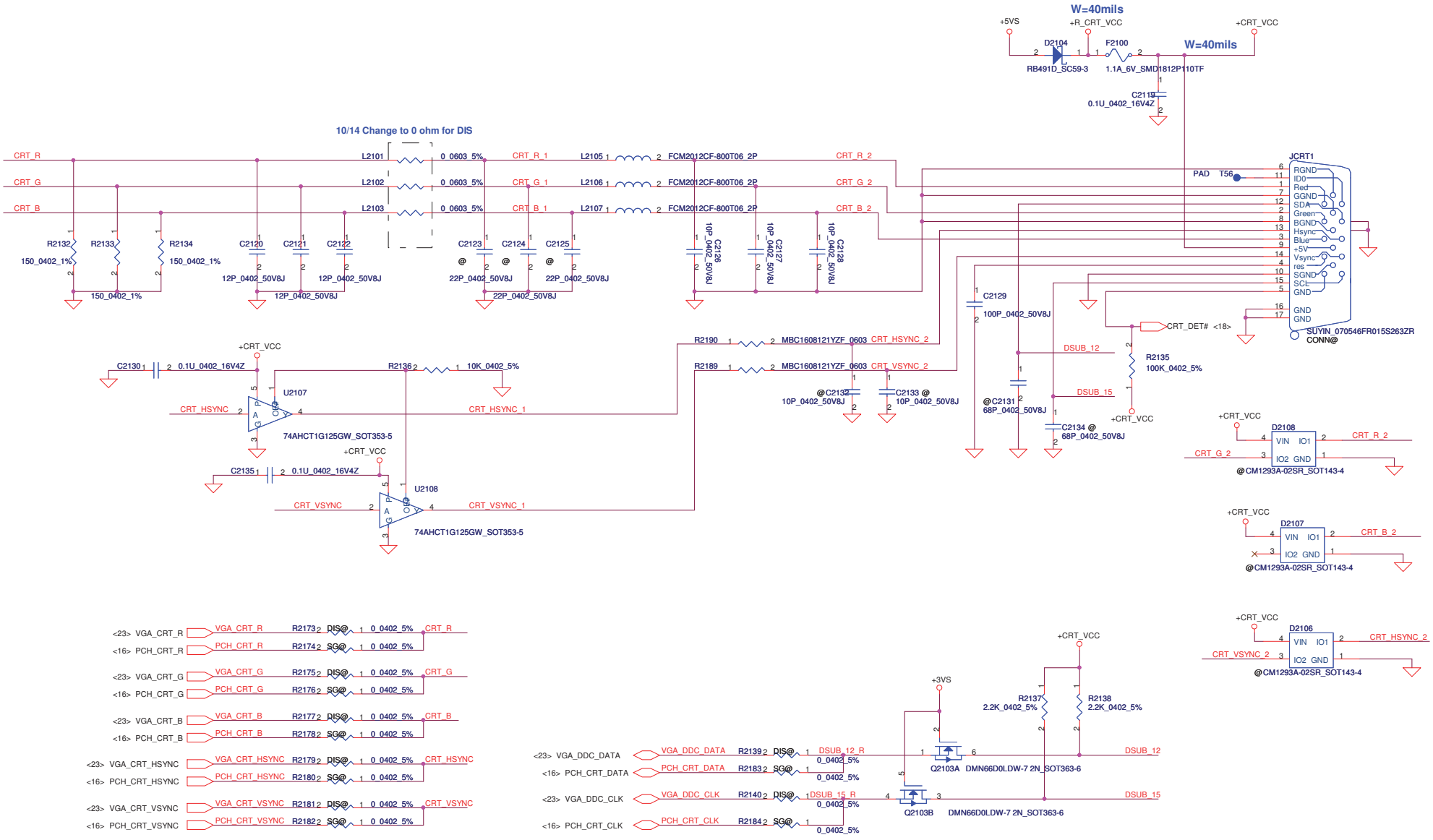
Compal Electronics, Inc.

Title: LVDS Connector

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 | Sheet 30 of 58

CRT Connector

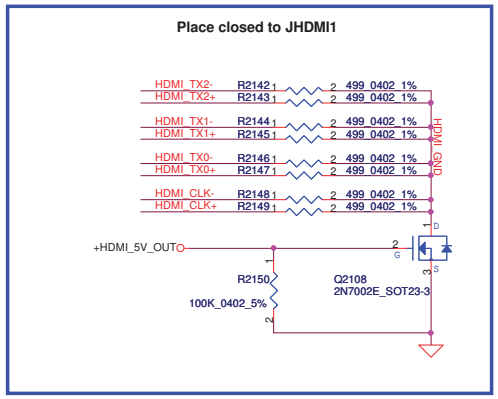


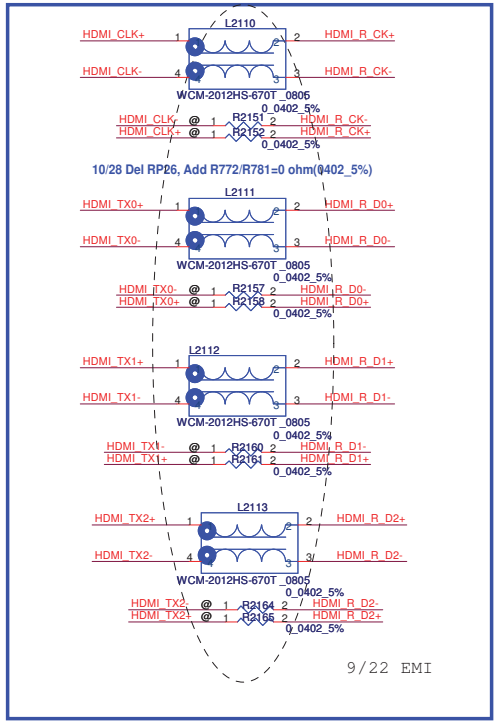
Compal Electronics, Inc.

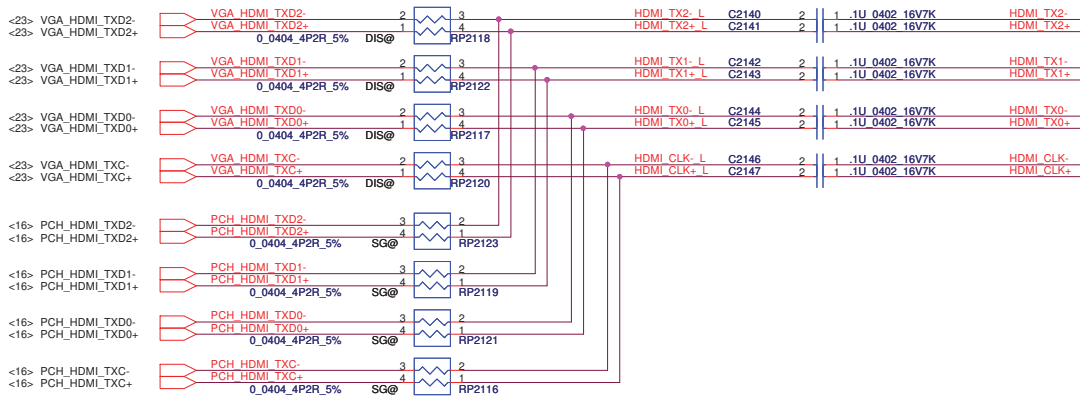
Title: CRT Connector

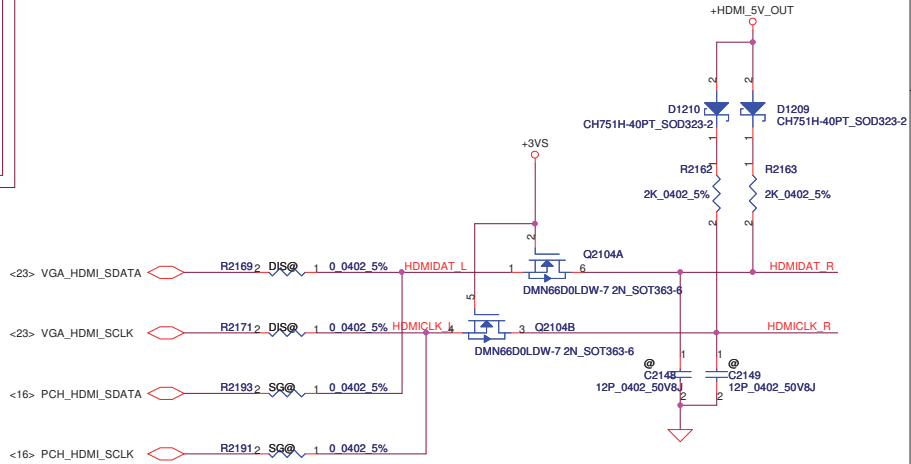
Size	Document Number	Rev
B	LA-6931P	1.0

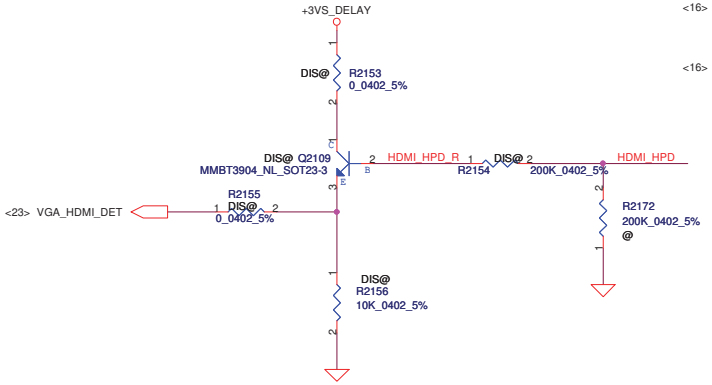
Date: Wednesday, October 27, 2010 Sheet 31 of 58

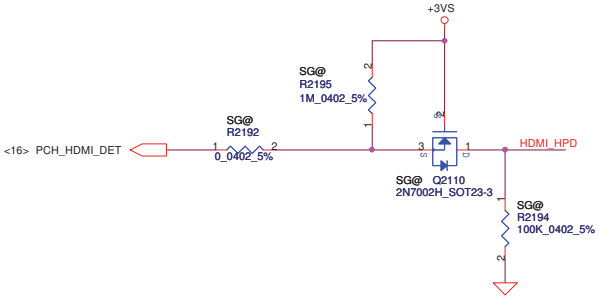


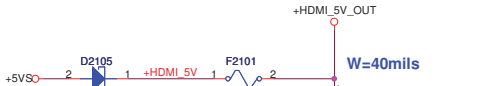


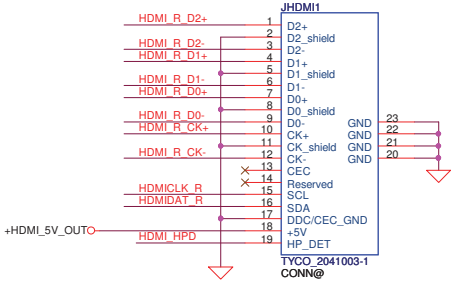












Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

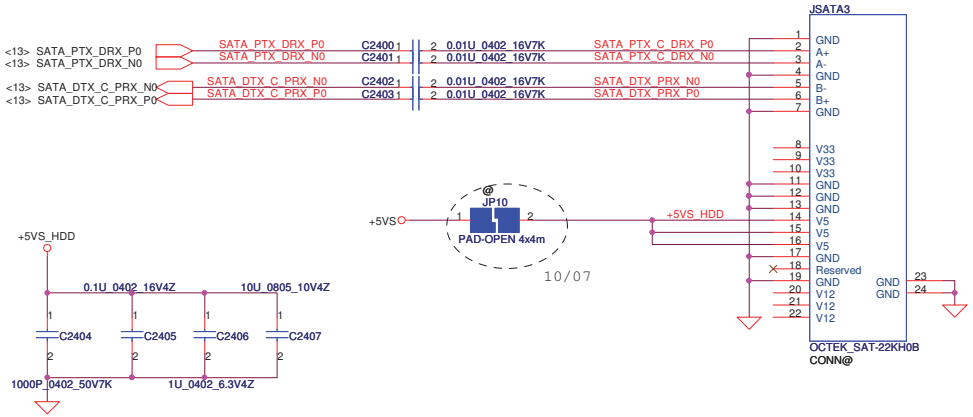
Title: HDMI Level Shife & Conn

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 32 of 58

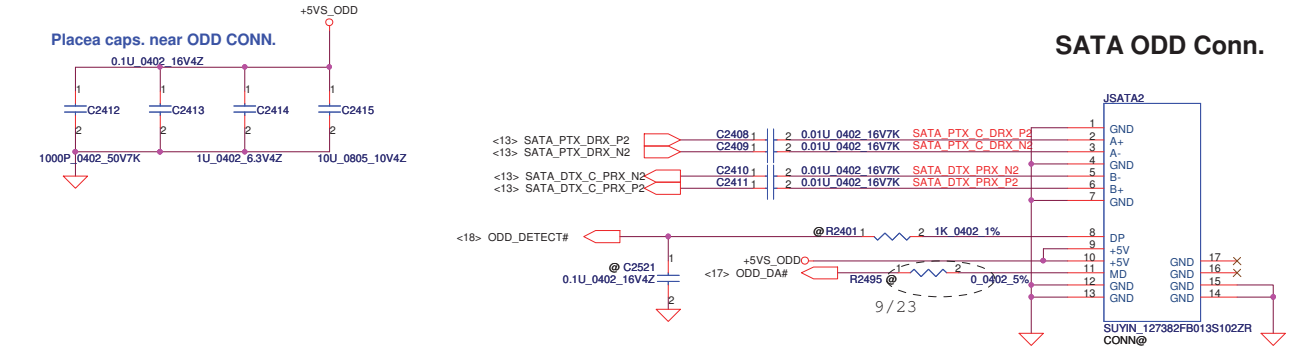
HDD

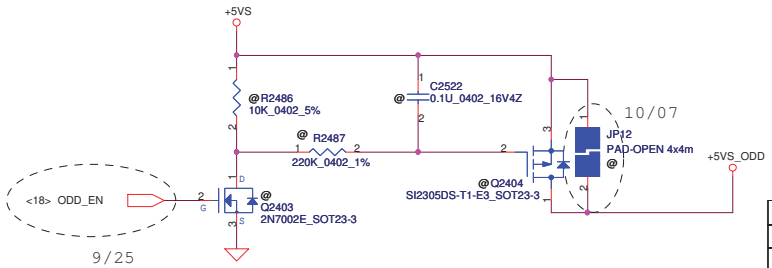
SATA HDD Conn.



ODD

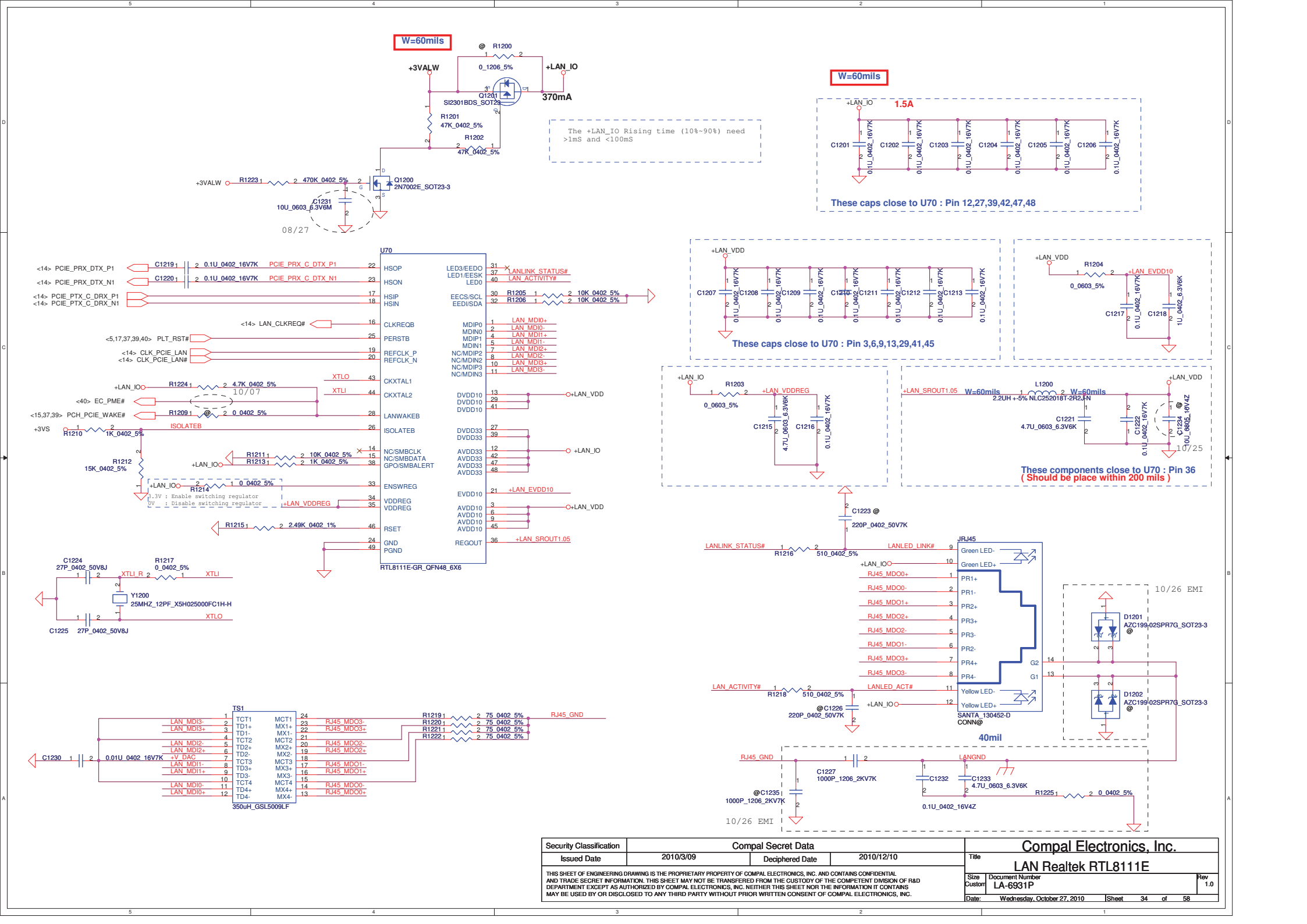
SATA ODD Conn.





Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: HDD & ODD Connector			
Size: B	Document Number: LA-6931P		Rev: 1.0
Date: Wednesday, October 27, 2010	Sheet 33 of 58		



Security Classification	Compal Secret Data		
Issued Date	2010/3/09	Deciphered Date	2010/12/10

Compal Electronics, Inc.

Title: LAN Realtek RTL8111E

Size	Document Number	Rev
Custom	LA-6931P	1.0

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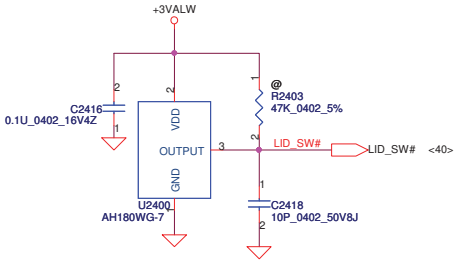
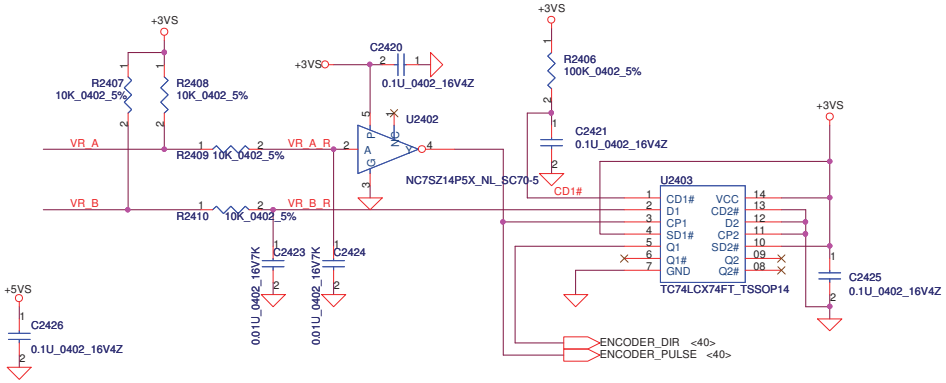
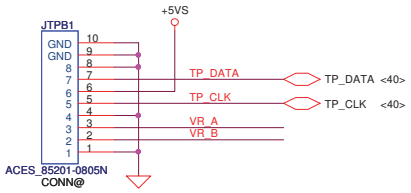
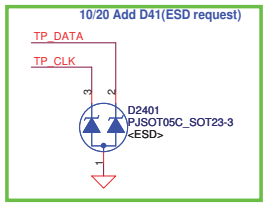
Lid Switch



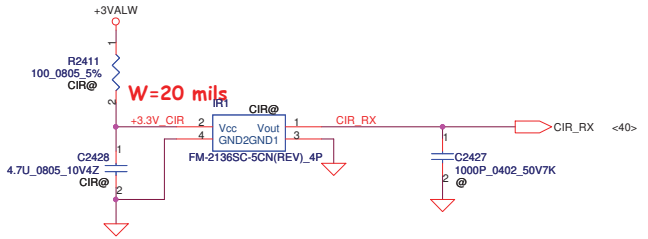
Touch Pad







CIR



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.			
Title: LID/RTC/CIR			
Size	Document Number: LA-6931P		Rev: 1.0
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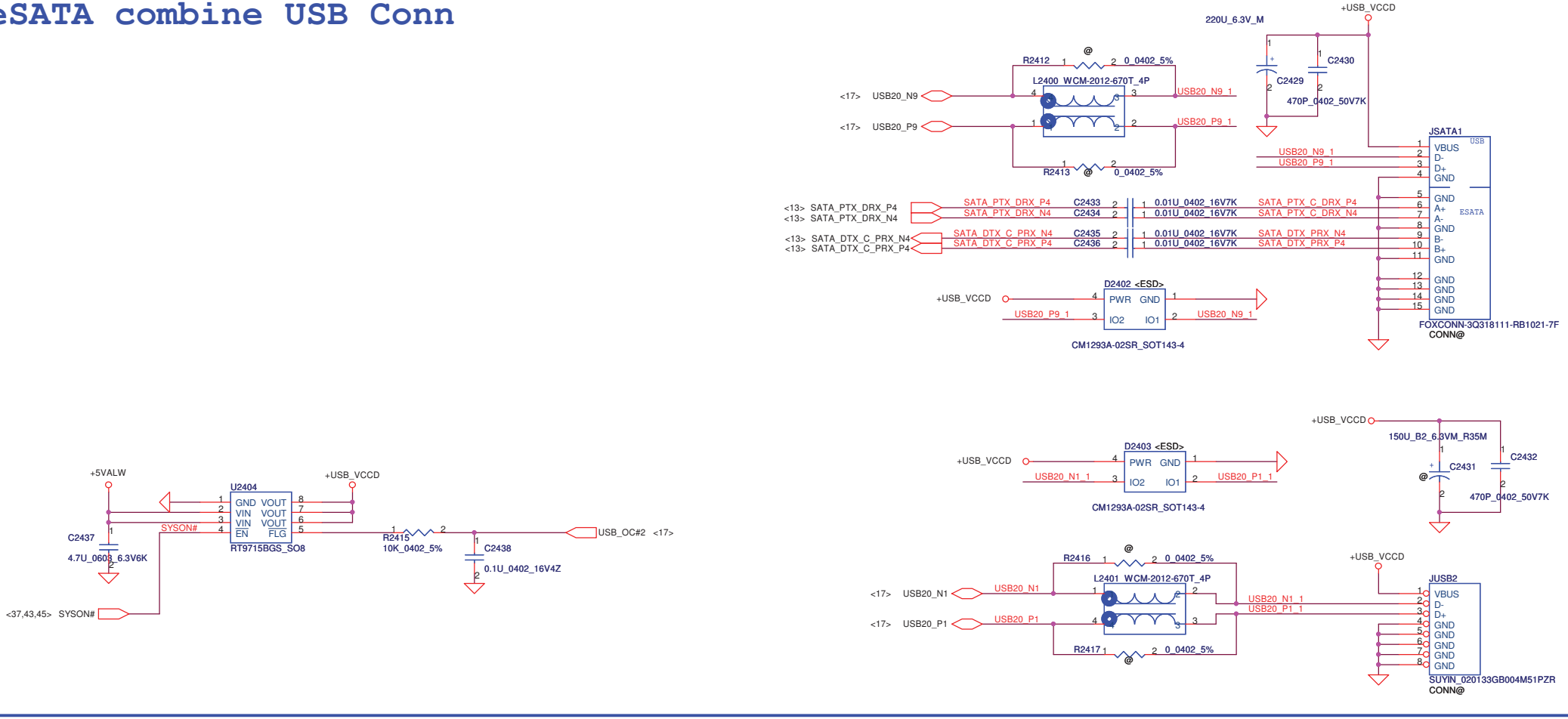
eSATA combine USB Conn



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: USB / eSATA

Size: Custom | Document Number: LA-6931P | Rev: 1.0

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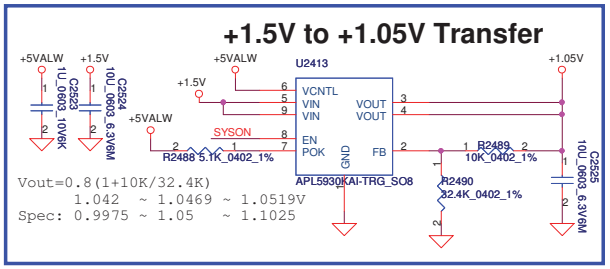
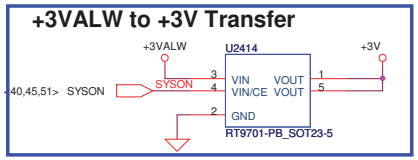
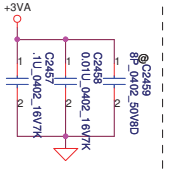
+1.5V to +1.05V Transfer



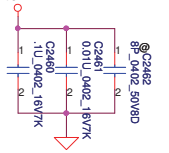
+3VALW to +3V Transfer

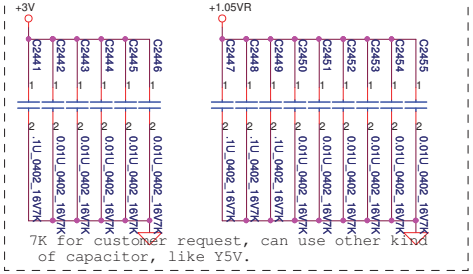


Close to U2407.D7

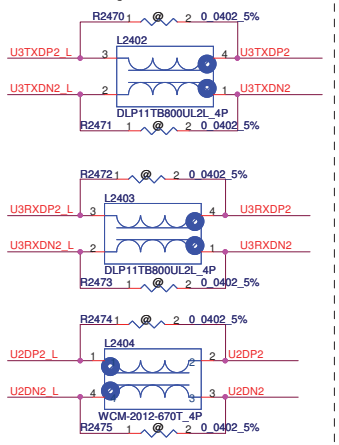


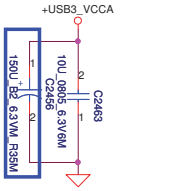
Close to U2407.P13



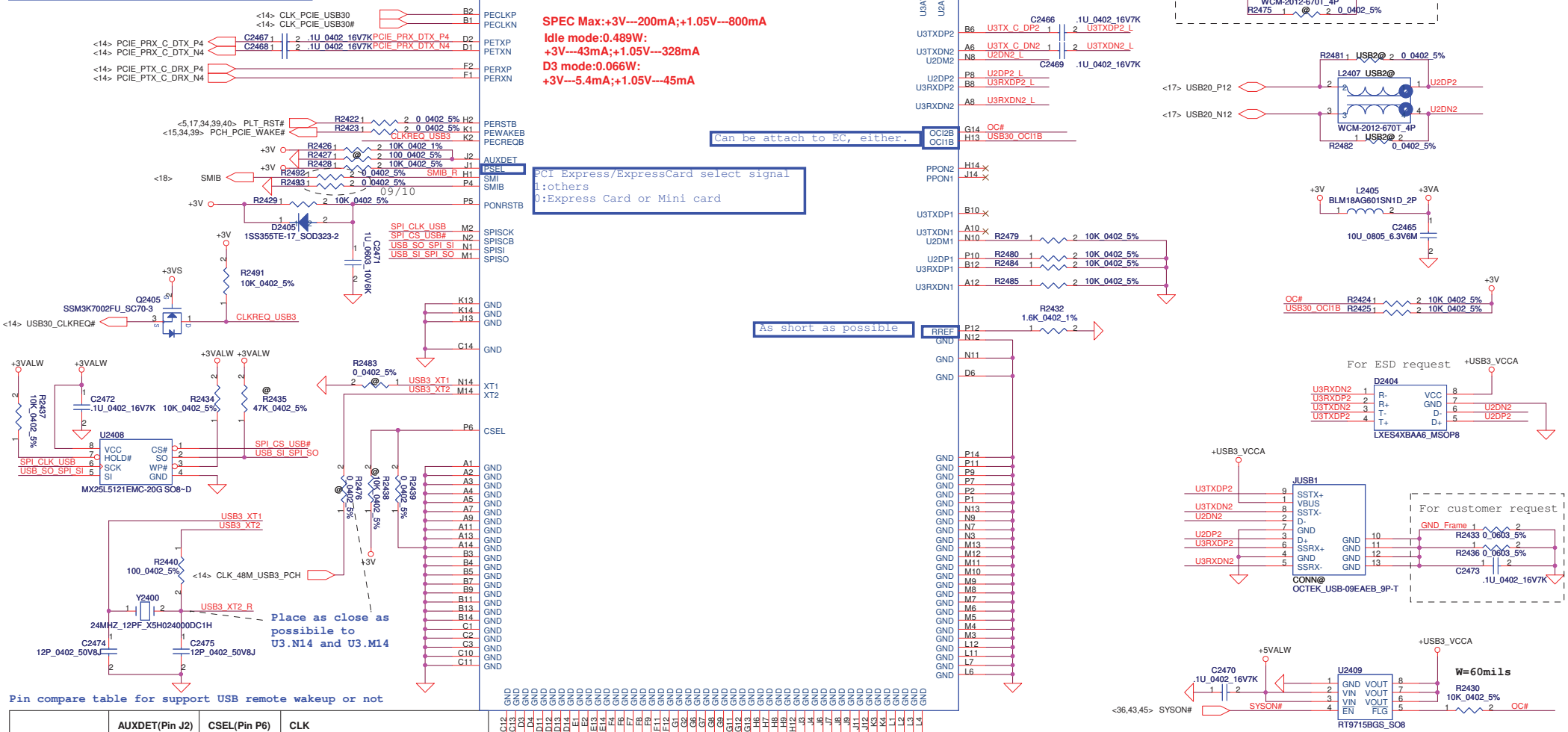


For EMI request (need confirm)





D-case for customer request
can use B-case, either.



Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y2400,2440,C2474,C2475
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R2476,R2483

UPD720200AF1-DAP-A

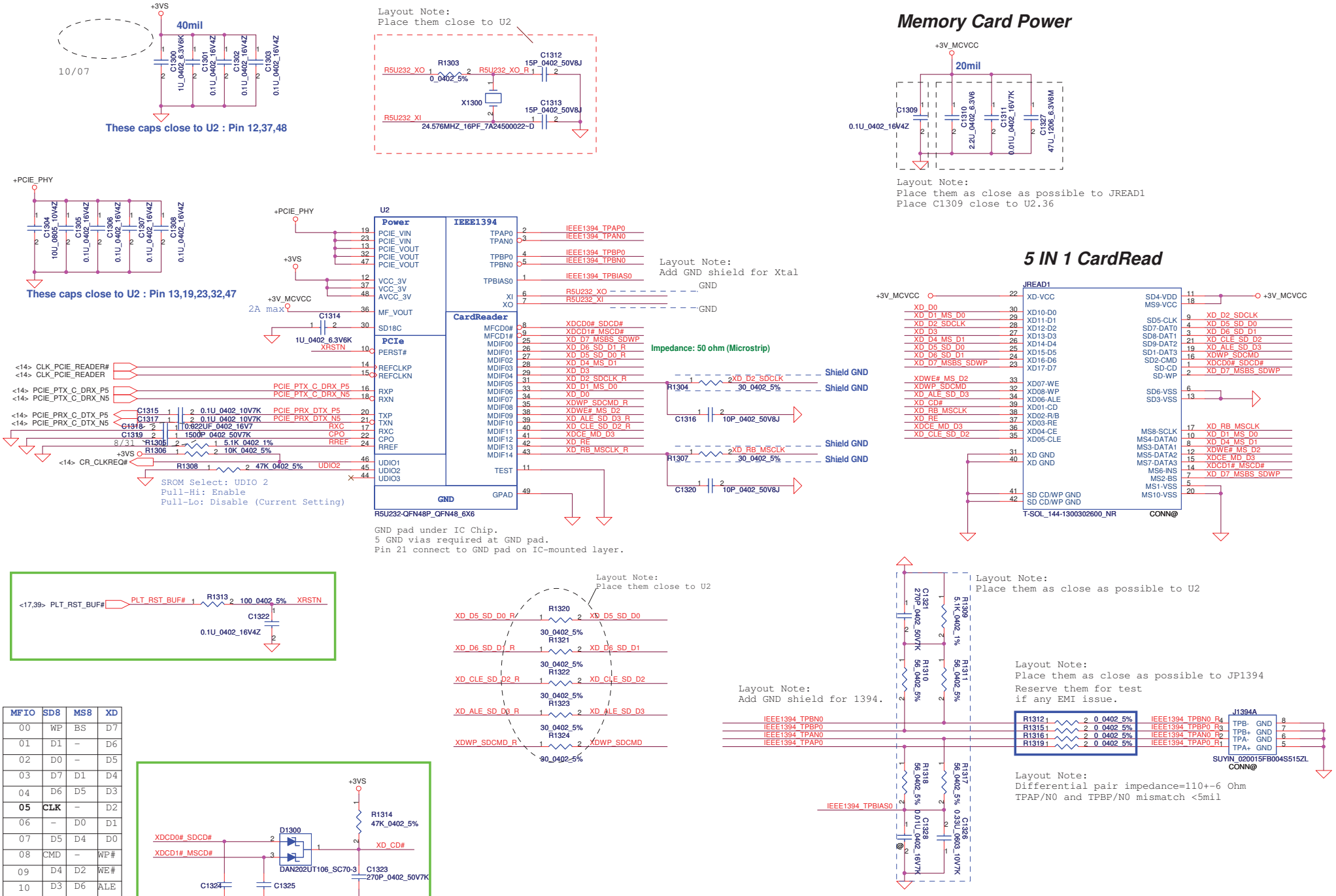
Security Classification: Compal Secret Data

Issued Date	2007/1/15	Deciphered Date	2008/1/15

Title: USB3.0 PD720200

Size: Custom | Document Number | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 37 of 58



MFIO	SD8	MS8	XD
00	WP	BS	D7
01	D1	–	D6
02	D0	–	D5
03	D7	D1	D4
04	D6	D5	D3
05	**CLK**	–	D2
06	–	D0	D1
07	D5	D4	D0
08	CMD	–	WP#
09	D4	D2	WE#
10	D3	D6	ALE
11	D2	–	CLE
12	–	D3	CE#
13	–	D7	RE#
14	–	**CLK**	R/B#

Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: R5U232

Size: Custom | Document Number: LA-6931P | Rev: 1.0

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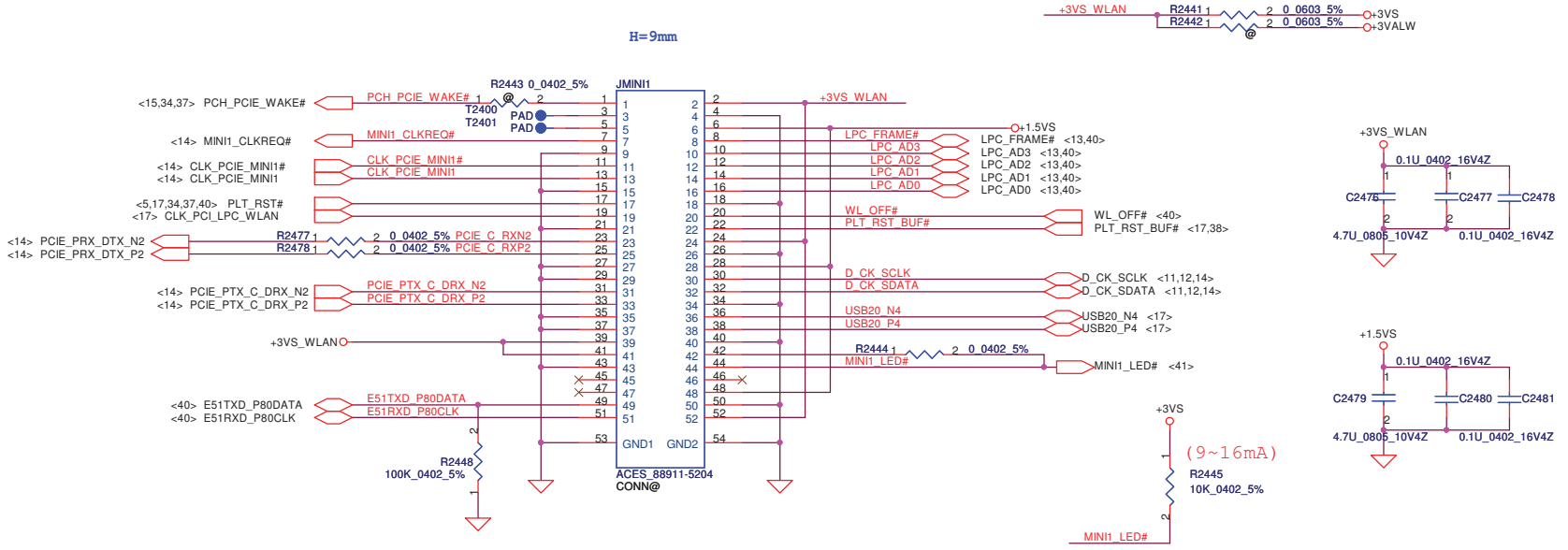
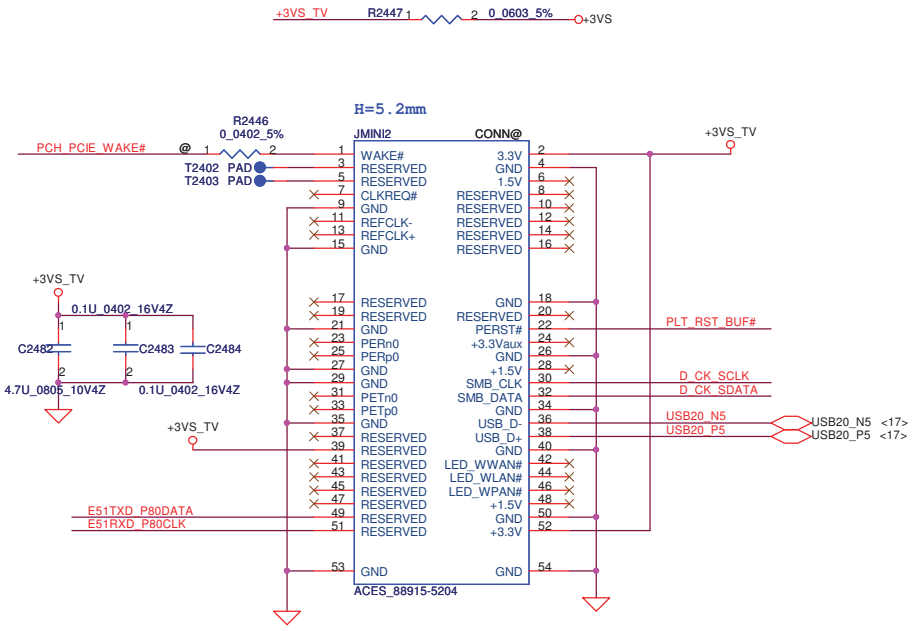
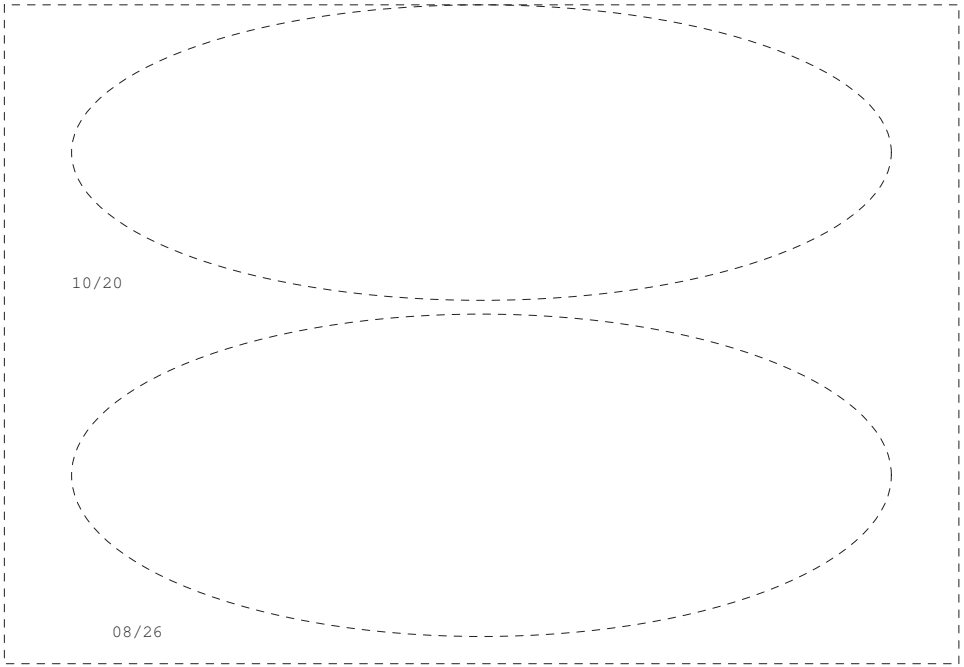
WLAN



MINI

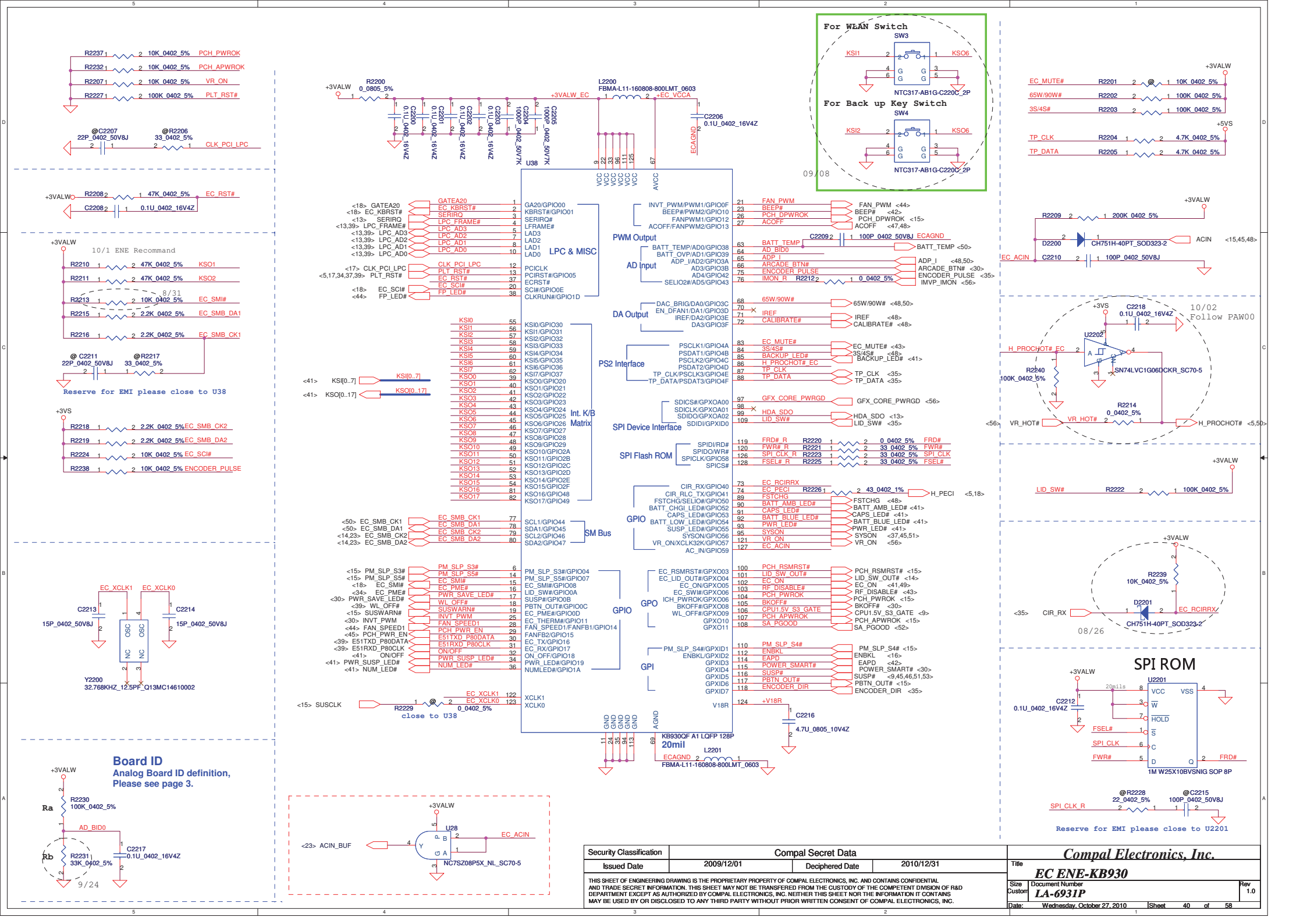




Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title	WLAN&MINI	
Size: Custom	Document Number: LA-6931P	Rev: 1.0
Date: Wednesday, October 27, 2010	Sheet 39 of 58	



Security Classification	Compal Secret Data		
Issued Date	2009/12/01	Deciphered Date	2010/12/31

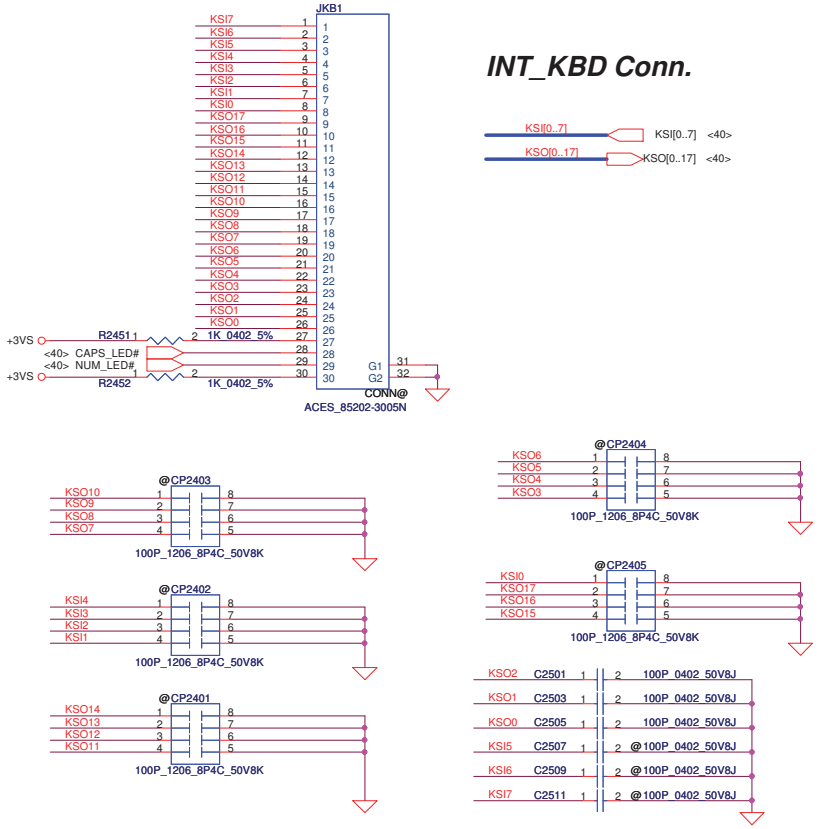
Compal Electronics, Inc.

Title: EC ENE-KB930

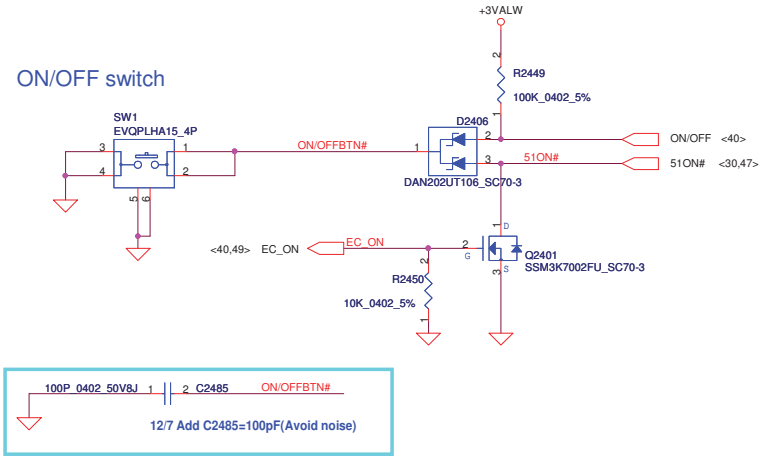
Size: Custom | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 40 of 58

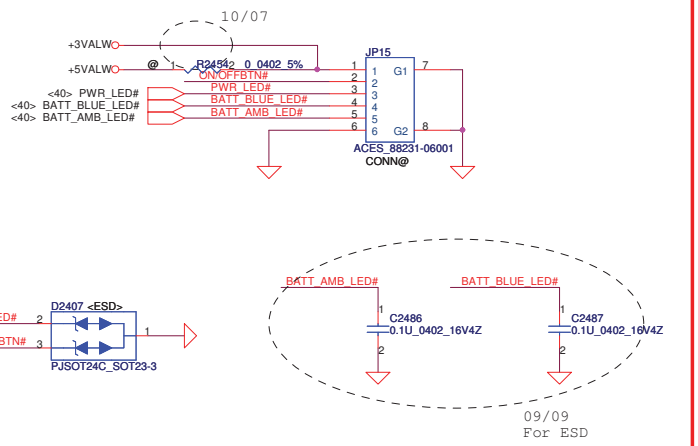
INT_KBD Conn.



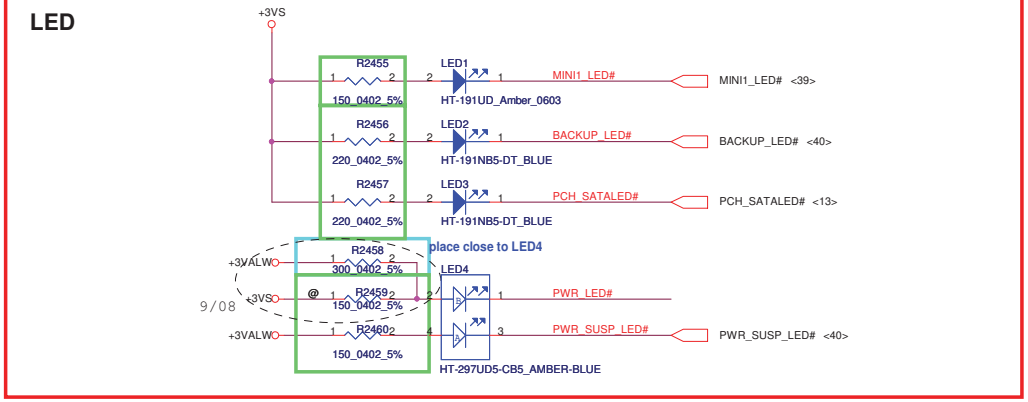
Power Button



Power Conn



LED



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

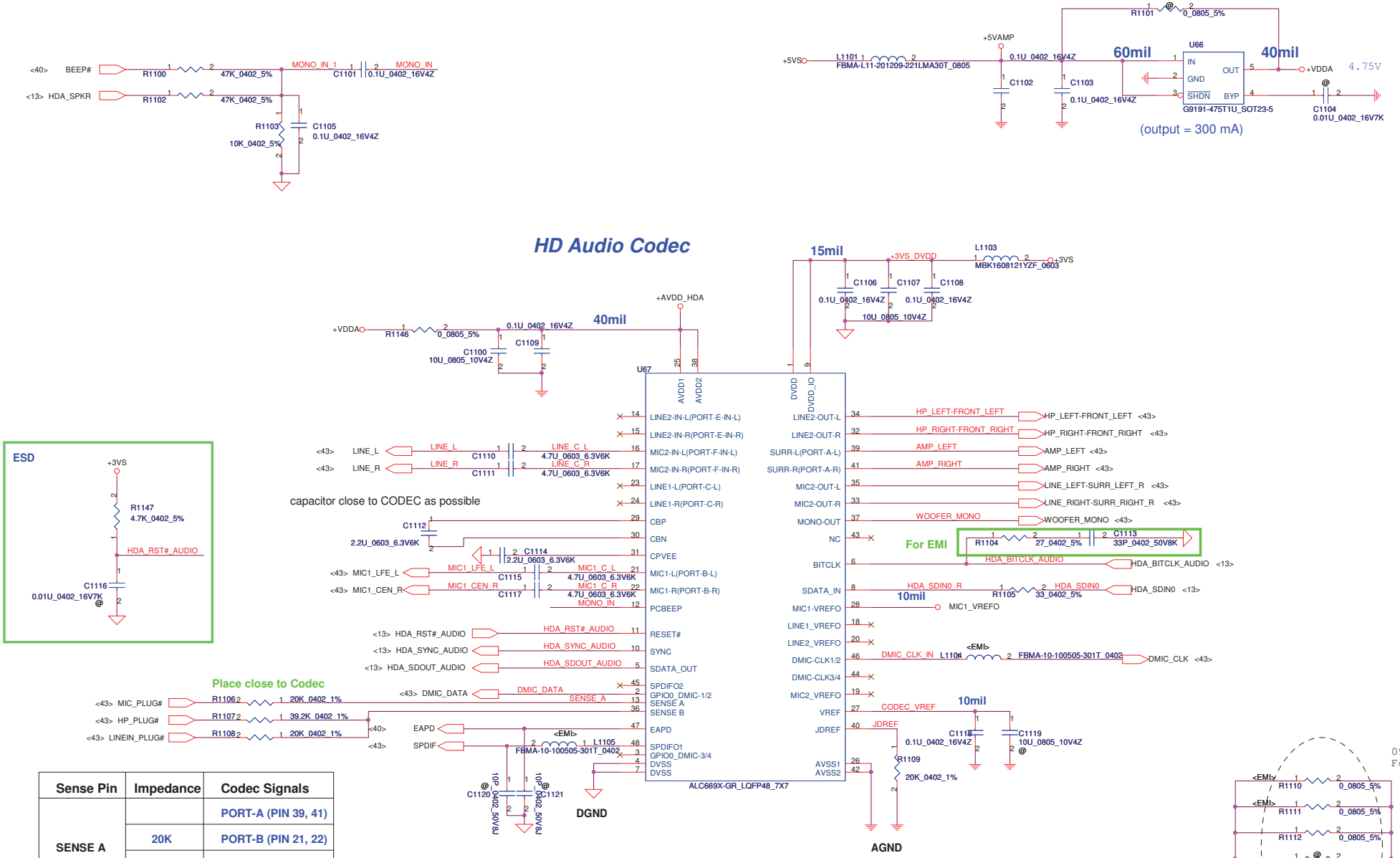
Compal Electronics, Inc.

Title: Power OK, I/O Port & K/B Connector

Size	Document Number	Rev
B	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 41 of 58

HD Audio Codec



Sense Pin	Impedance	Codec Signals
SENSE A		PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

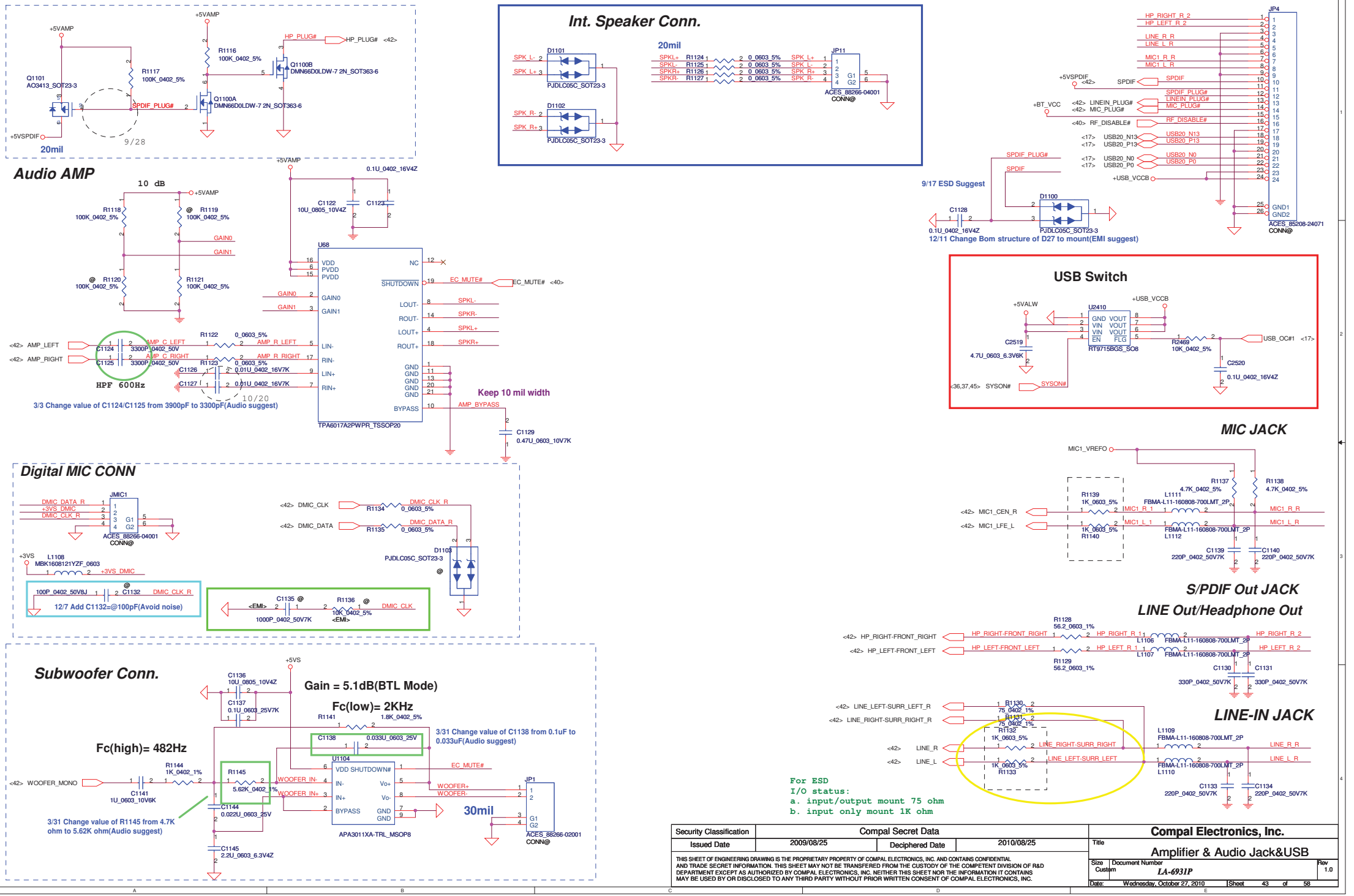
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: HD Audio Codec ALC669X

Size	Document Number	Rev
B	LA-6931P	1.0

Date: Wednesday, October 27, 2010 | Sheet 42 of 58



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

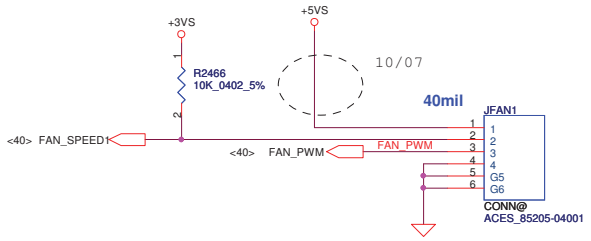
Compal Electronics, Inc.

Title: Amplifier & Audio Jack&USB

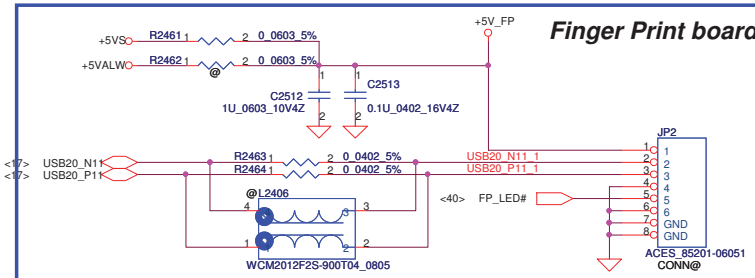
Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 | Sheet 43 of 58

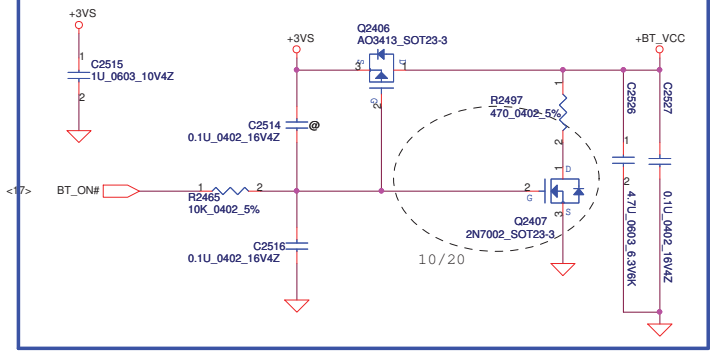
FAN1 Conn



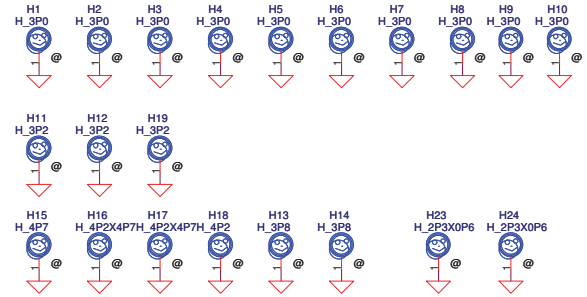
Finger Print board



BT



Screw



NON-PDH

2/25 Change footprint of H22

Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

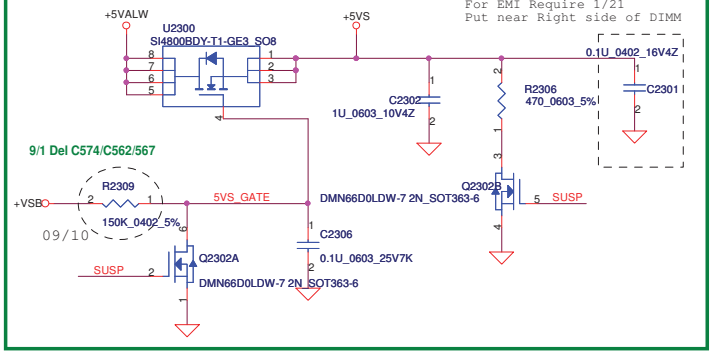
Compal Electronics, Inc.

Title: FAN & Screw Hole

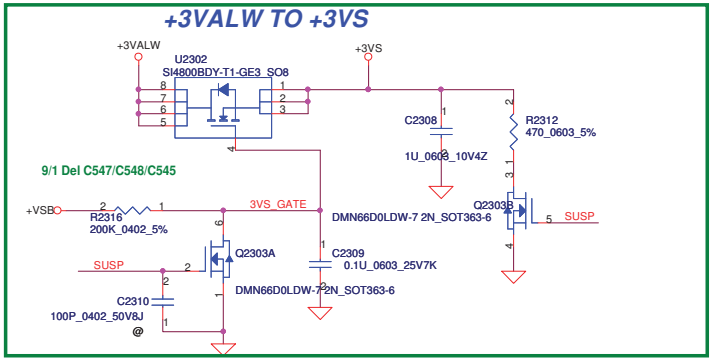
Size	Document Number	Rev
B	LA-6931P	1.0

Date: Wednesday, October 27, 2010 Sheet 44 of 58

+5VALW TO +5VS

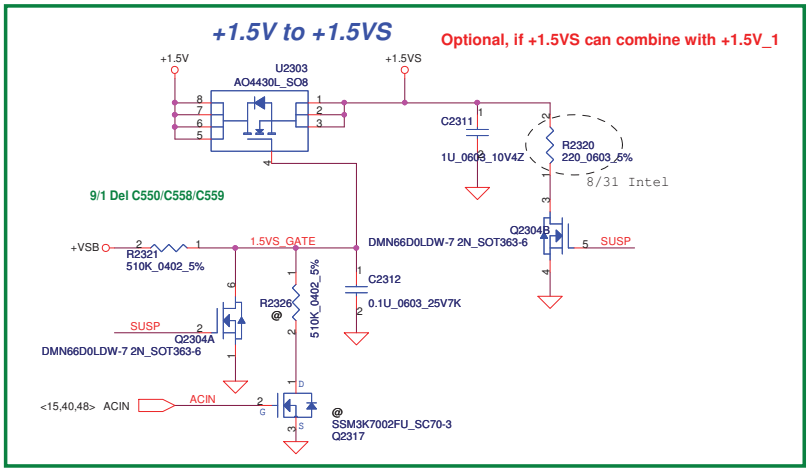


+3VALW TO +3VS



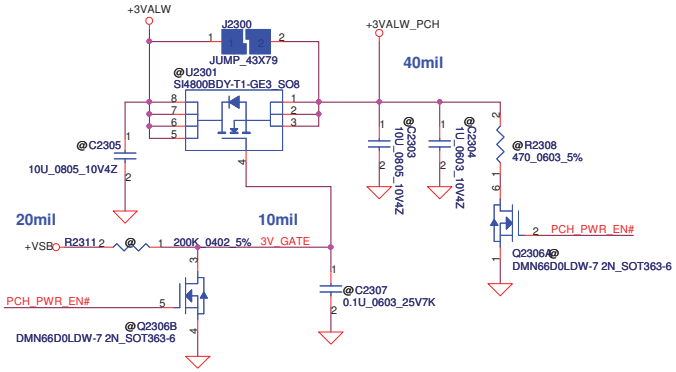
+1.5V to +1.5VS

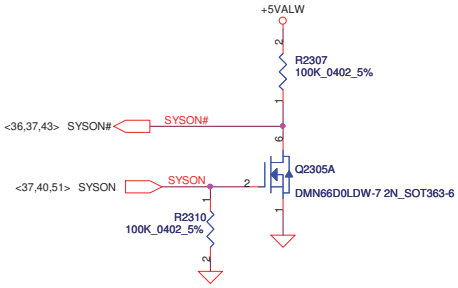
Optional, if +1.5VS can combine with +1.5V_1

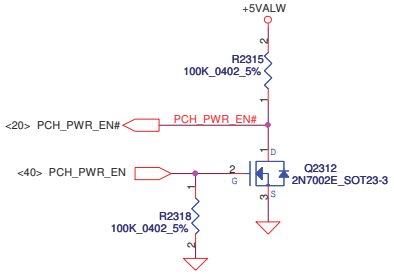


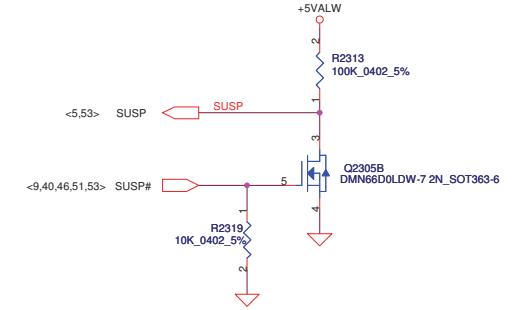
+3VALW TO +3VALW(PCH AUX Power)

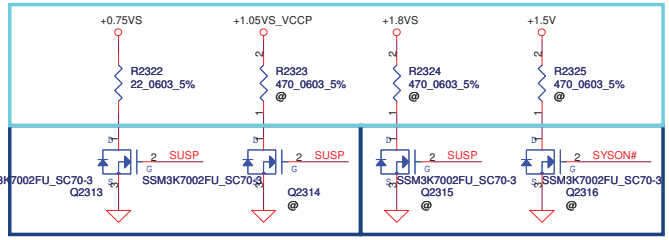
Short J5 for PCH VCCSUS3.3











Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

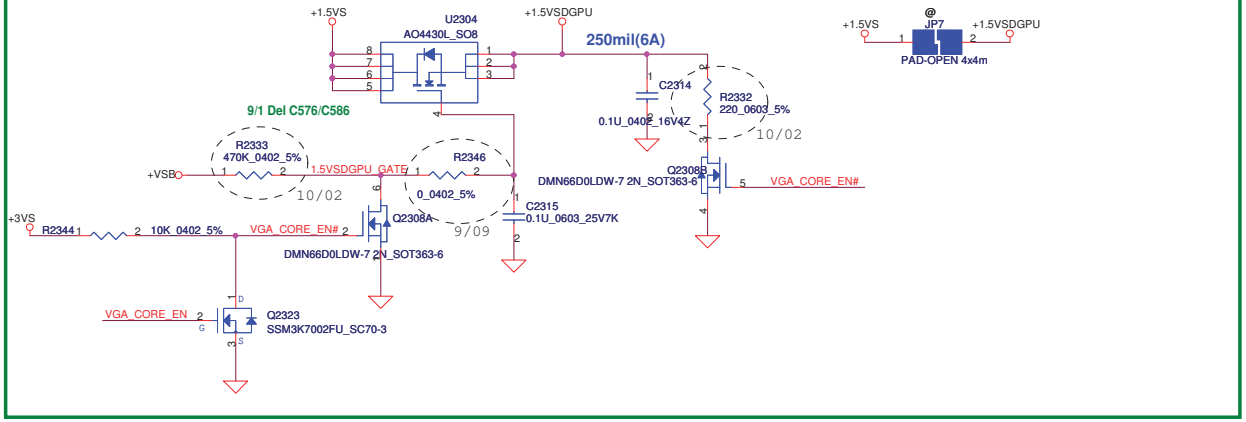
Compal Electronics, Inc.

Title: DC Interface

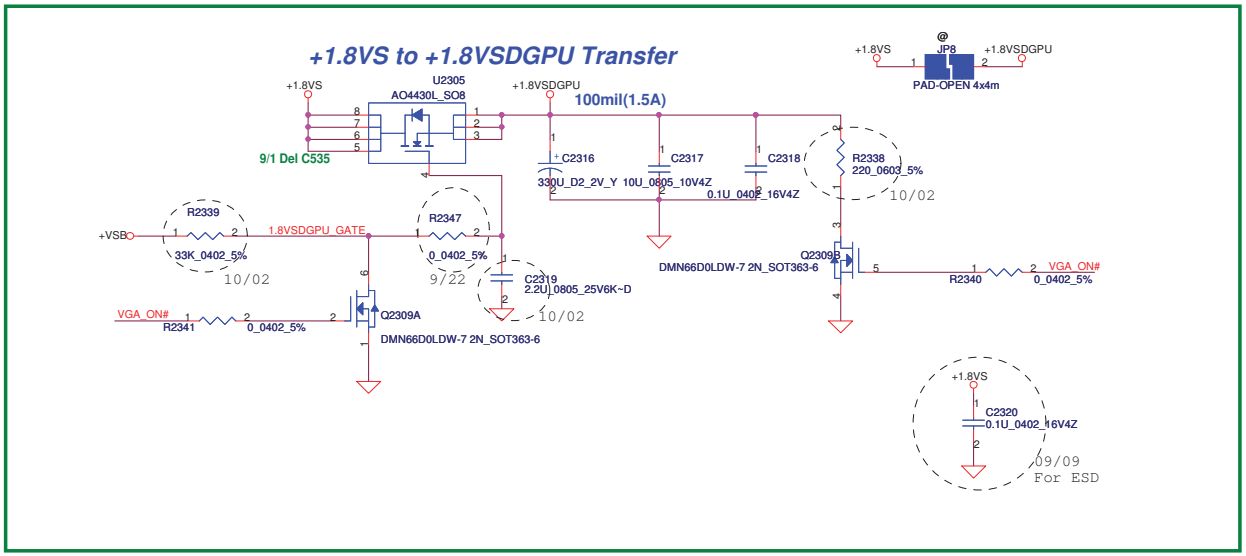
Size	Document Number	Rev
B	LA-6931P	1.0

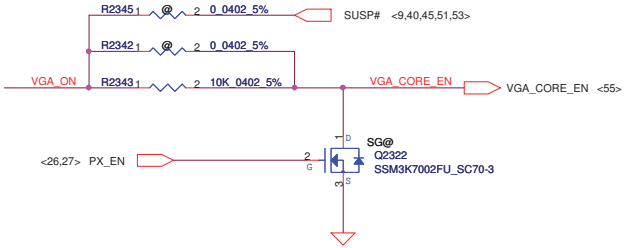
Date: Wednesday, October 27, 2010 Sheet 45 of 58

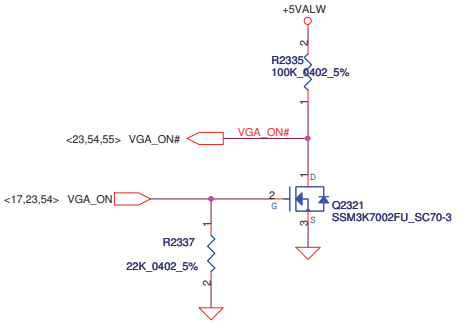
+1.5VS to +1.5VSDGPU Transfer



+1.8VS to +1.8VSDGPU Transfer







Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: VGA DC Interface

Size	Document Number	Rev
B	LA-6931P	1.0

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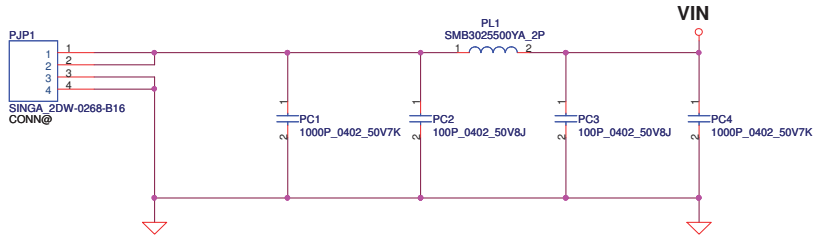
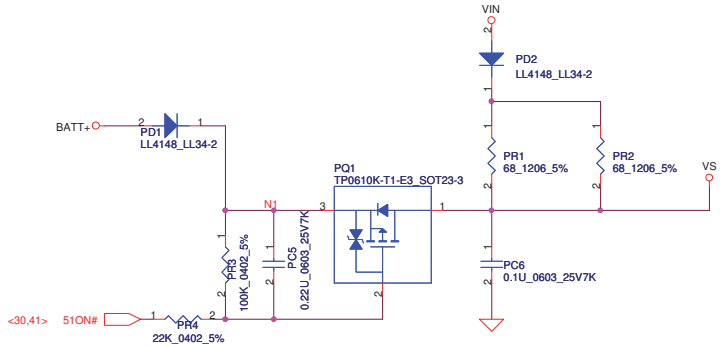
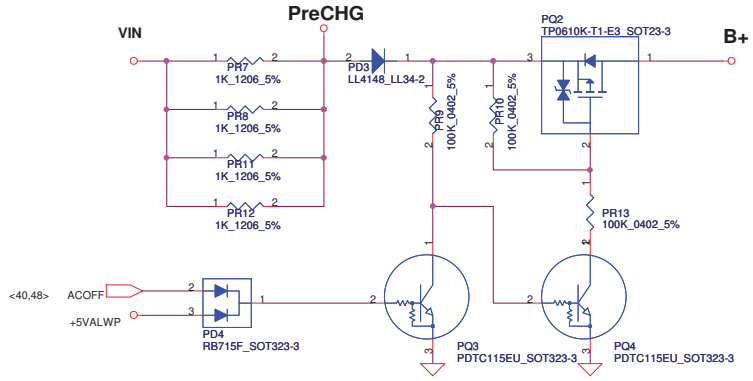






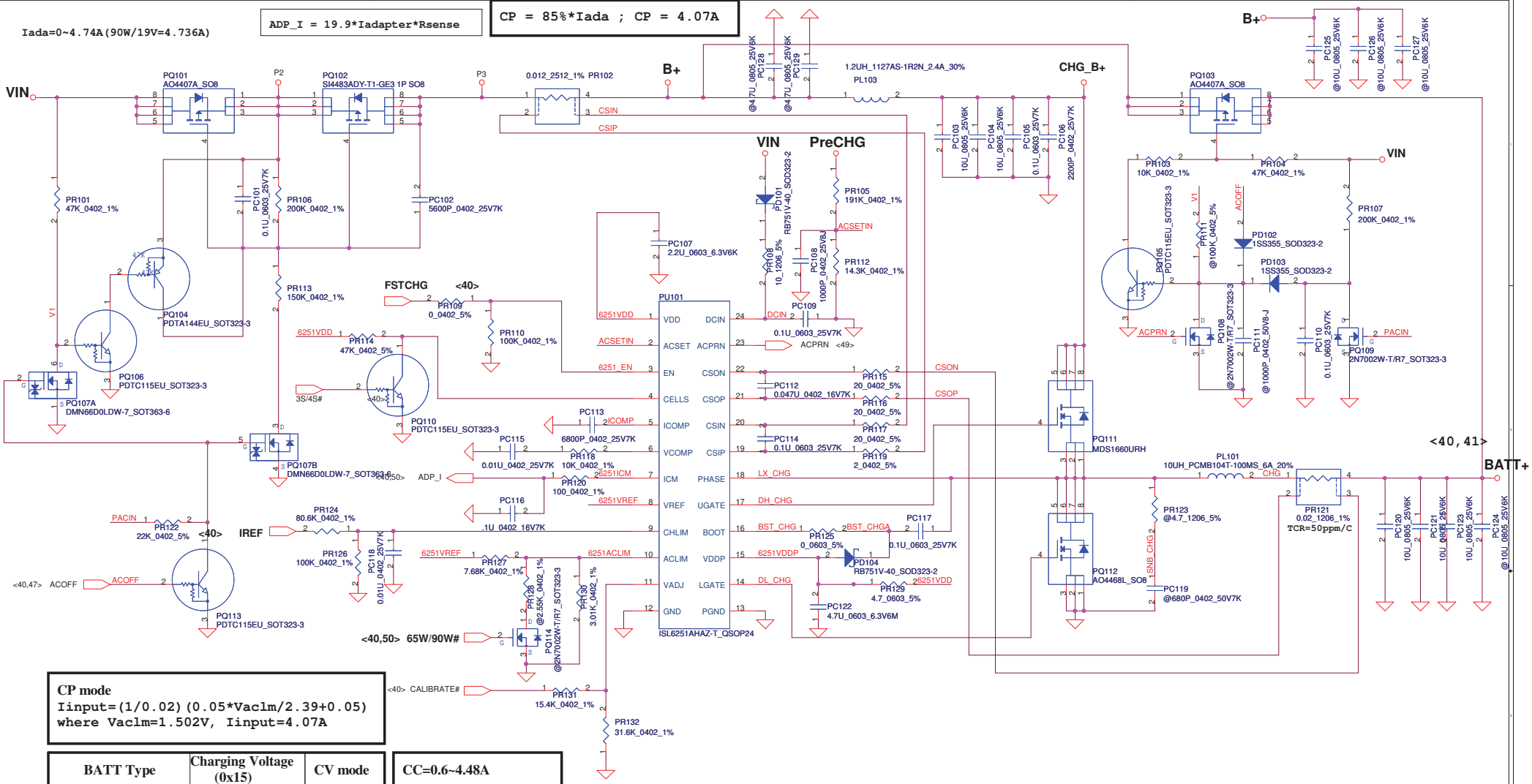
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.			
Title: PWR DCIN / Pre-charge			
Size: Custom	Document Number: LA-6931P		Rev: 0.1
Date: Wednesday, October 27, 2010	Sheet 47 of 10		

Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//(15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

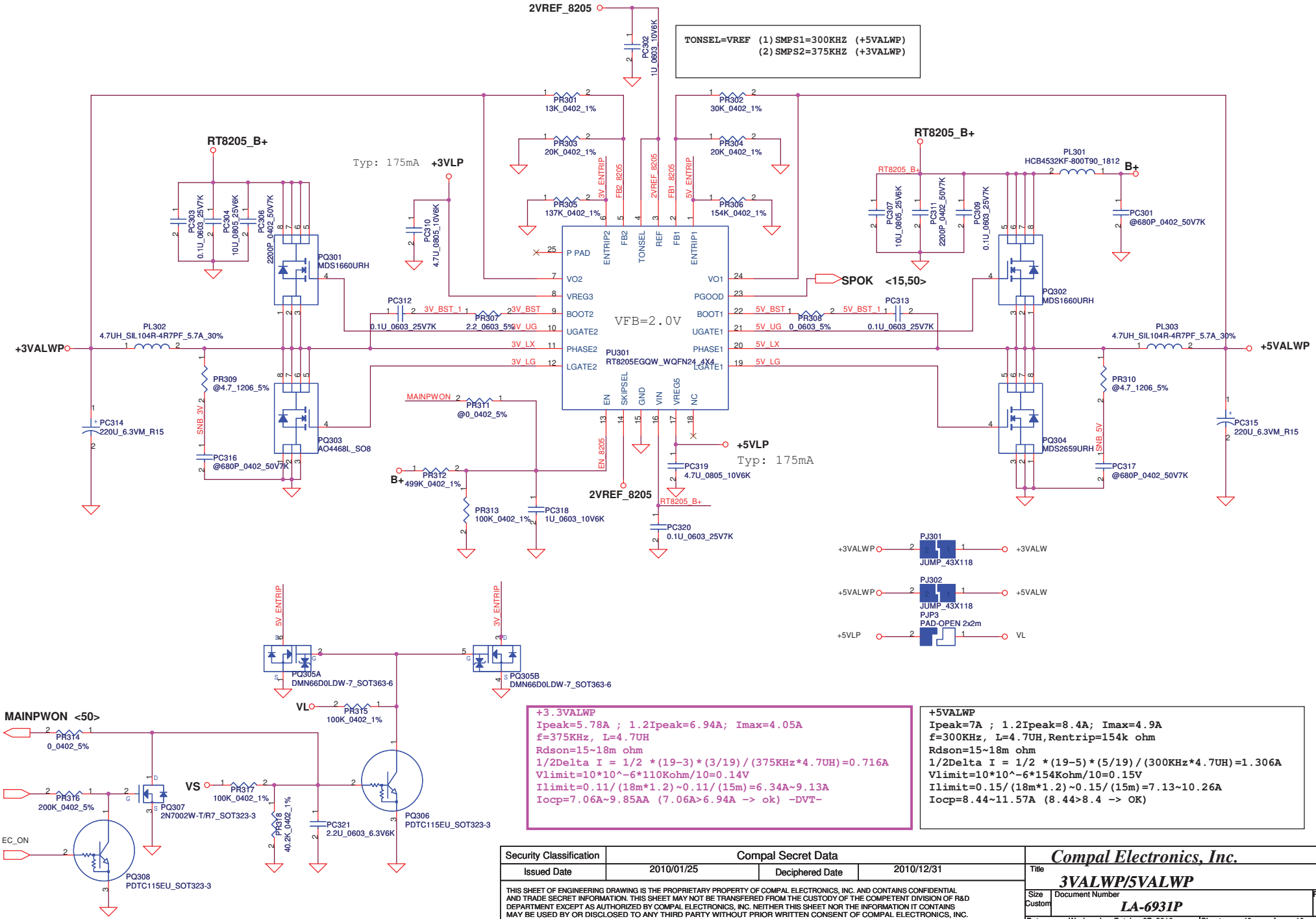
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: LA-6931P | Rev: 0.1

Date: Wednesday, October 27, 2010 | Sheet 48 of 10



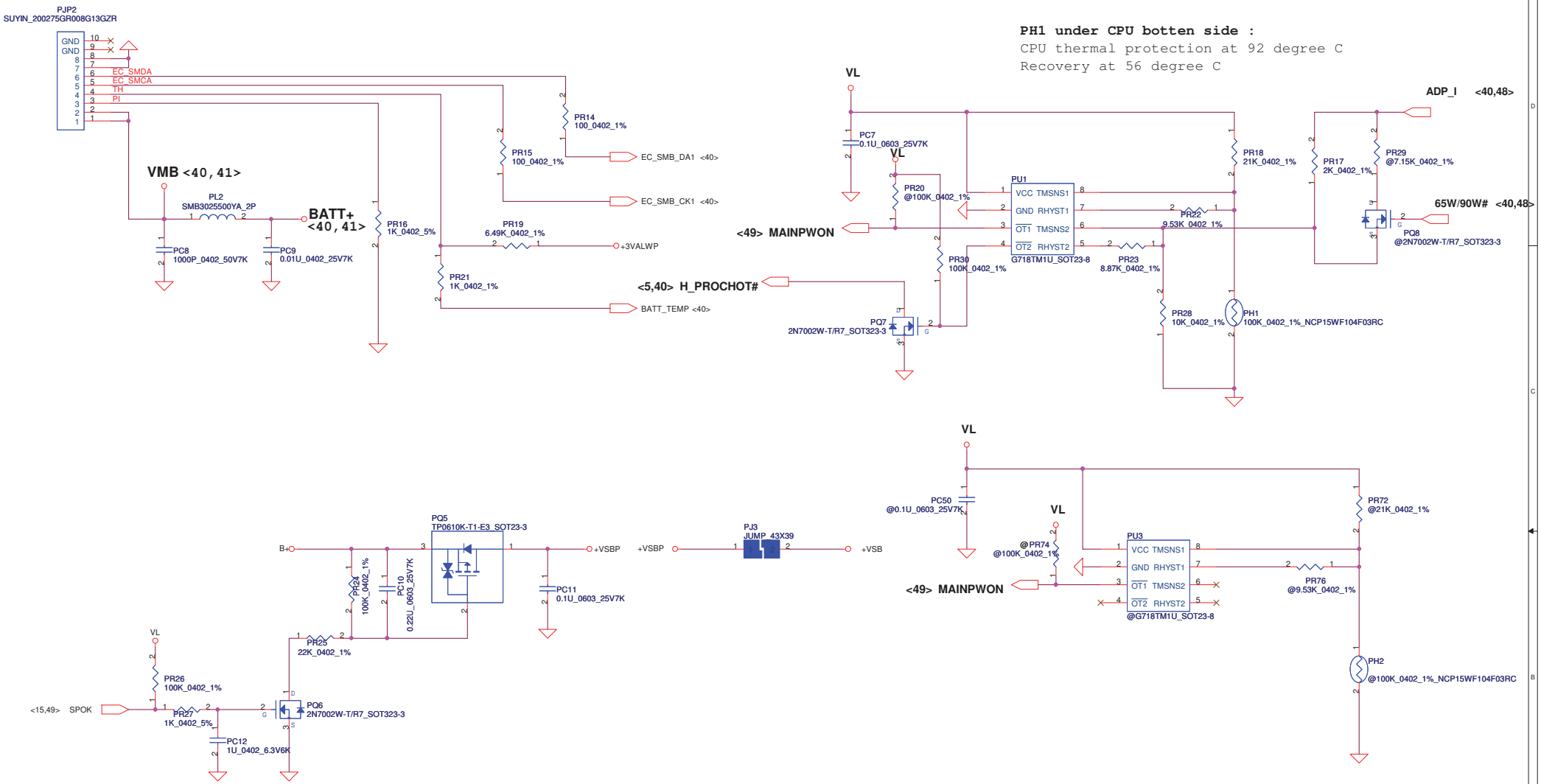
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

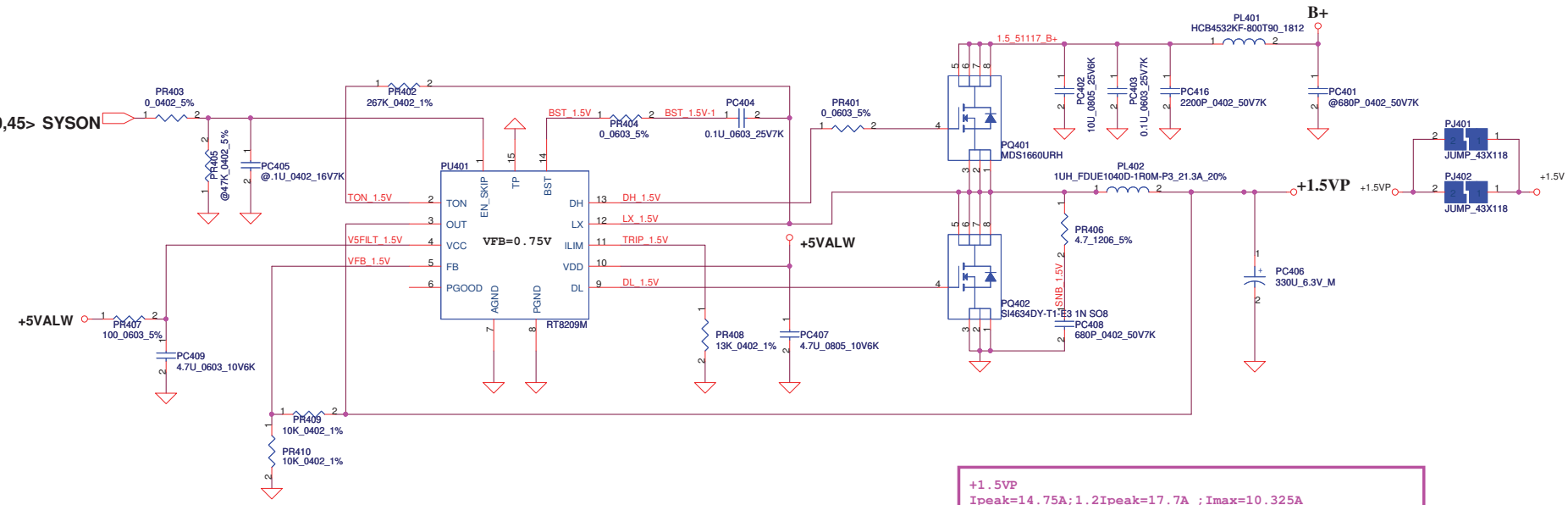
Size: Custom | Document Number: LA-6931P | Rev: 0.1

Date: Wednesday, October 27, 2010 | Sheet 49 of 10

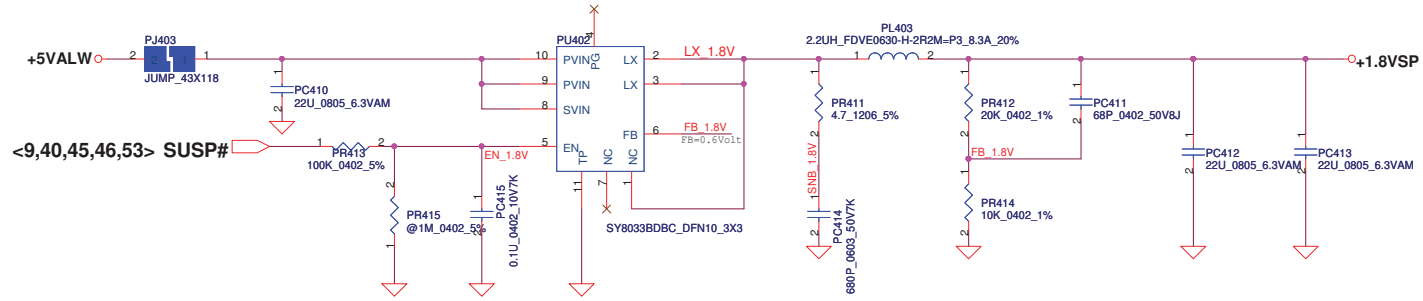


Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.		
Title: PWR-BATTERY CONN/OTP		
Size: Custom	Document Number: LA-6931P	Rev: 0.1
Date: Wednesday, October 27, 2010	Sheet 50 of 10	



+1.5VP
Ipeak=14.75A;1.2Ipeak=17.7A ;Imax=10.325A
Rton=267K, Fsw=298KHz ,Rdson=4.5~5.6mohm
Rtrip=12K
Iocp=18.17~28.98A



1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V
-DVT-

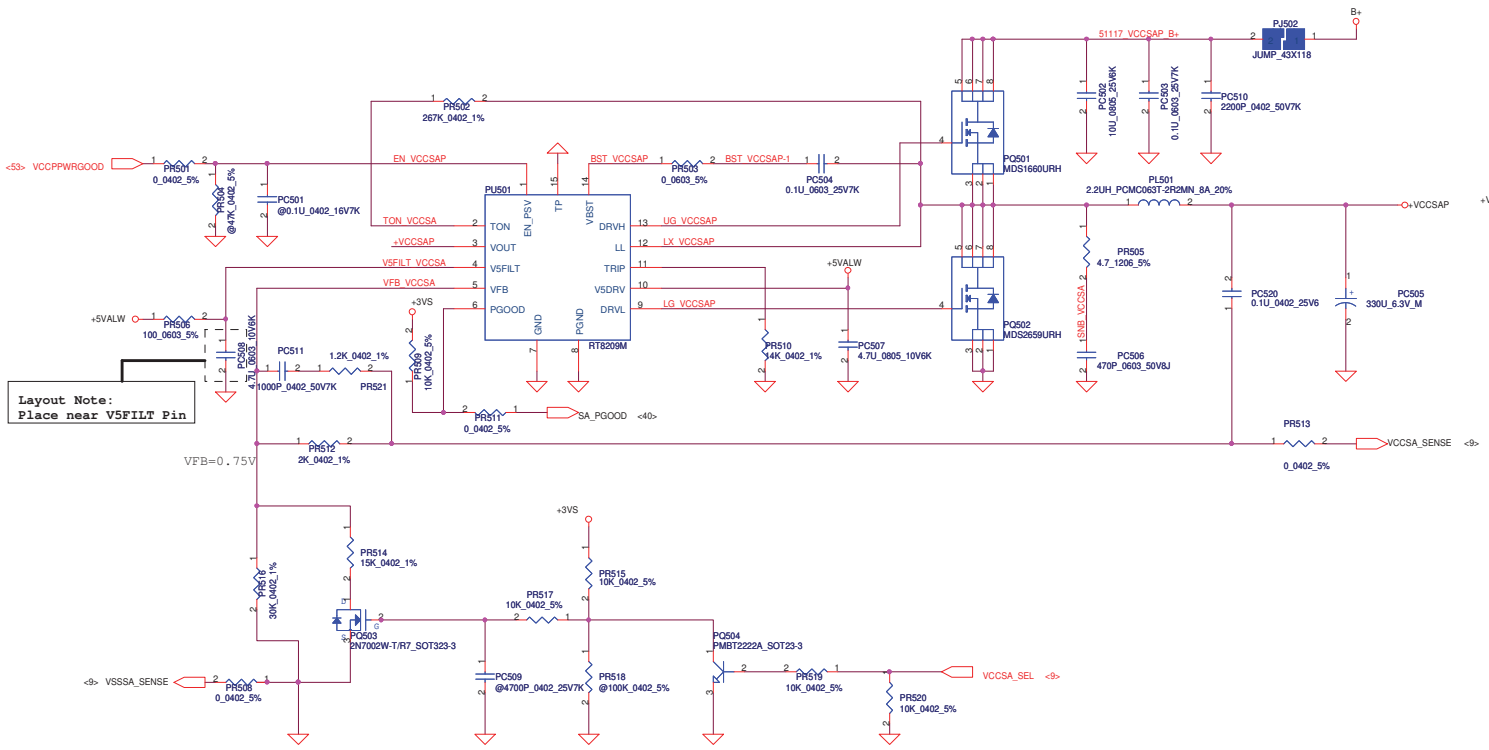
Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

Title: PWR-+1.5VP/+1.8VSP

Size: Custom | Document Number: LA-6931P | Rev: 0.1

Date: Wednesday, October 27, 2010 | Sheet 51 of 10



+VCCSAP
Ipeak=6A , Imax=4.2A, 1.2Ipeak=7.2A
DCR= 9 m(typ)~10 m(max)
Rlimit=12K,Rdson=15~18mohm
Ilimit=10uA
Iocp=Rlimit/Rdson*10^(-5)= 7.61~9.13A

VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=213KHz

Cesr=15m ohm
Ipeak=7.2A Imax=6.0A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0787V

Iocp=7.28~7.41A

VID[0]	VID[1]	VCCSA Vout	Require on 2011/2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	0	0.725V	No/Yes
1	1	0.675V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

the resister change
from @ to pop component

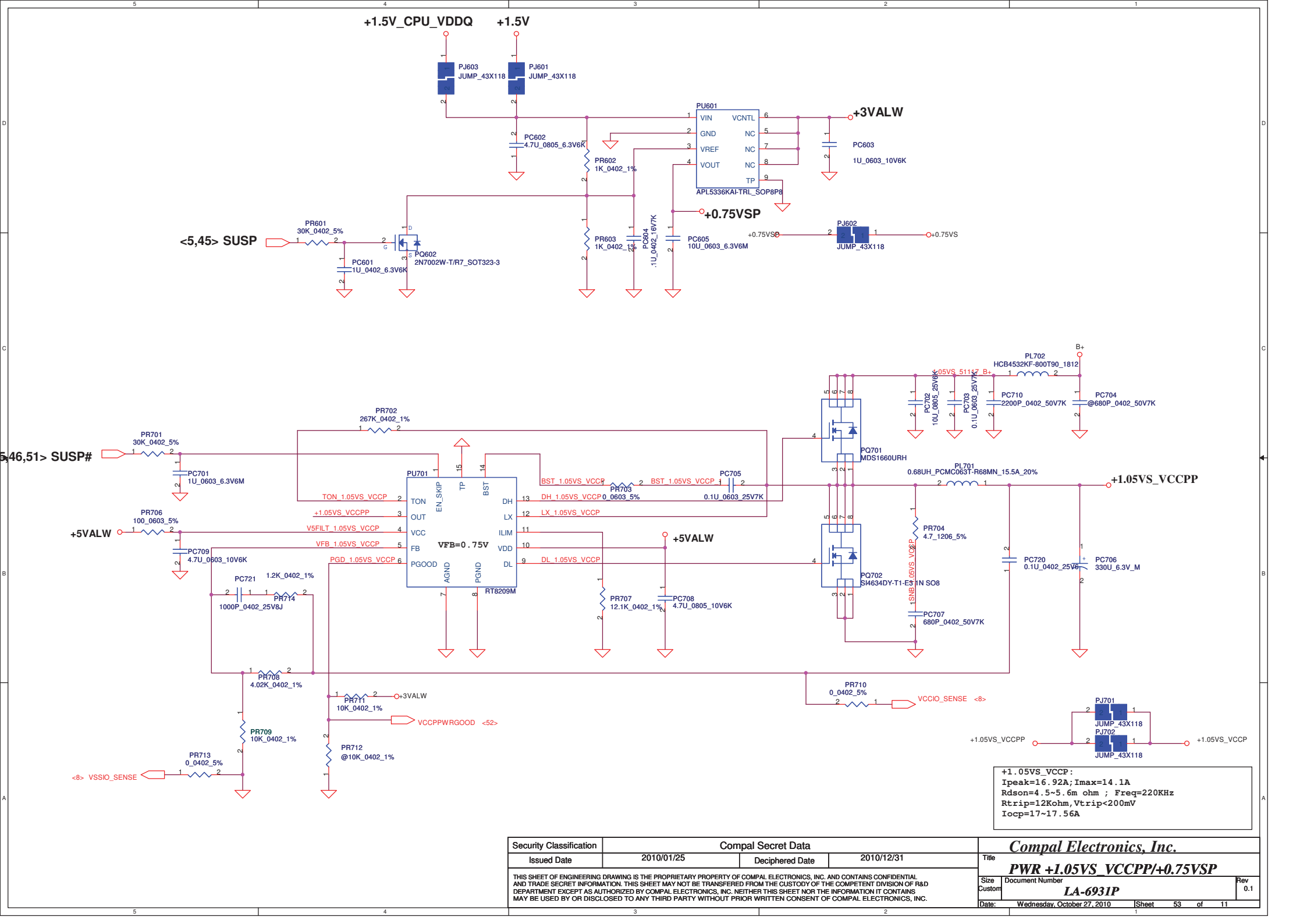
Add two jumpers on the HW's output cap of the
+VCCSA's PIN(+) and PIN(-) to sense the
feedback voltage for VCCSA_SENSE & VSSSA_SENSE.

Compal Electronics, Inc.

Title: PWR +VCCSAP

Size	Document Number	Rev
C	LA-6931P	0.1

Date: Wednesday, October 27, 2010 Sheet 52 of 10

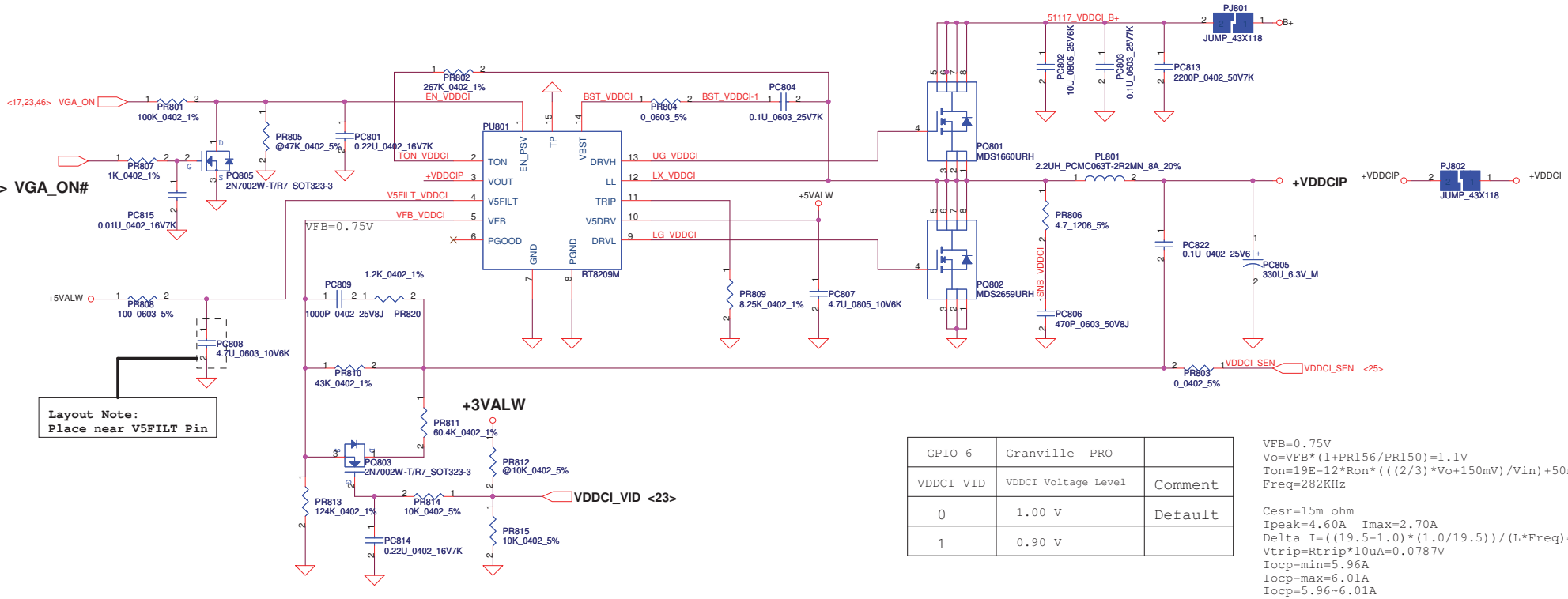


Compal Electronics, Inc.

Title: PWR +1.05VS_VCCPP/+0.75VSP

Size	Document Number	Rev
Custom	LA-6931P	0.1

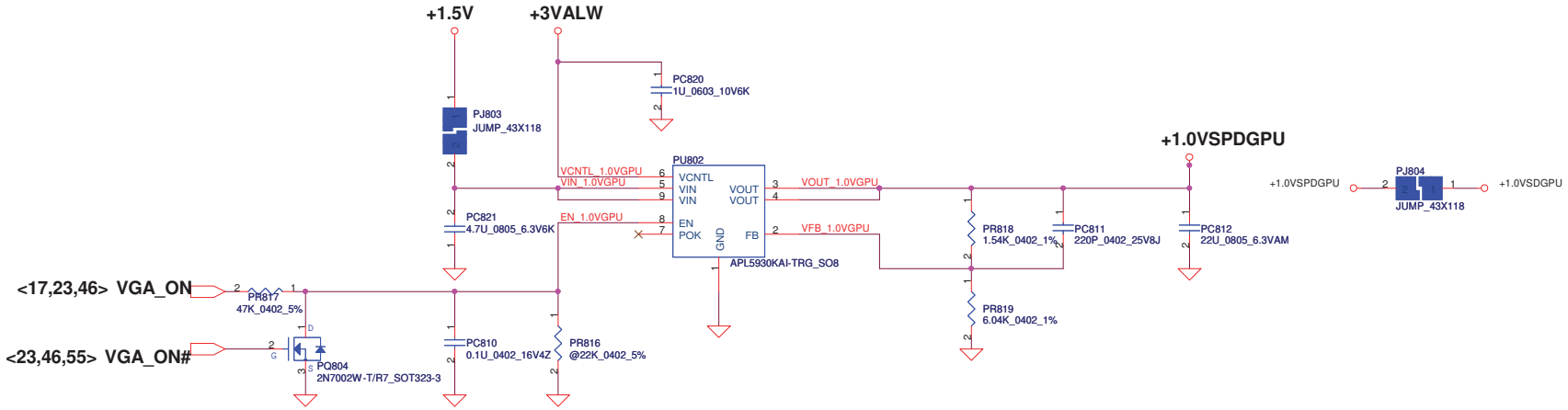
Date: Wednesday, October 27, 2010 Sheet 53 of 11



GPIO 6	Granville PRO	
VDDCI_VID	VDDCI Voltage Level	Comment
0	1.00 V	Default
1	0.90 V	

```
VFB=0.75V
Vo=VFB*(1+PR156/PR150)=1.1V
Ton=19E-12*Ron*(((2/3)*Vo+150mV)/Vin)+50ns=2.4E-7
Freq=282KHz

Cesr=15m ohm
Ipeak=4.60A  Imax=2.70A
Delta I=((19.5-1.0)*(1.0/19.5))/(L*Freq)=1.48A
Vtrip=Rtrip*10uA=0.0787V
Iocp-min=5.96A
Iocp-max=6.01A
Iocp=5.96~6.01A
```



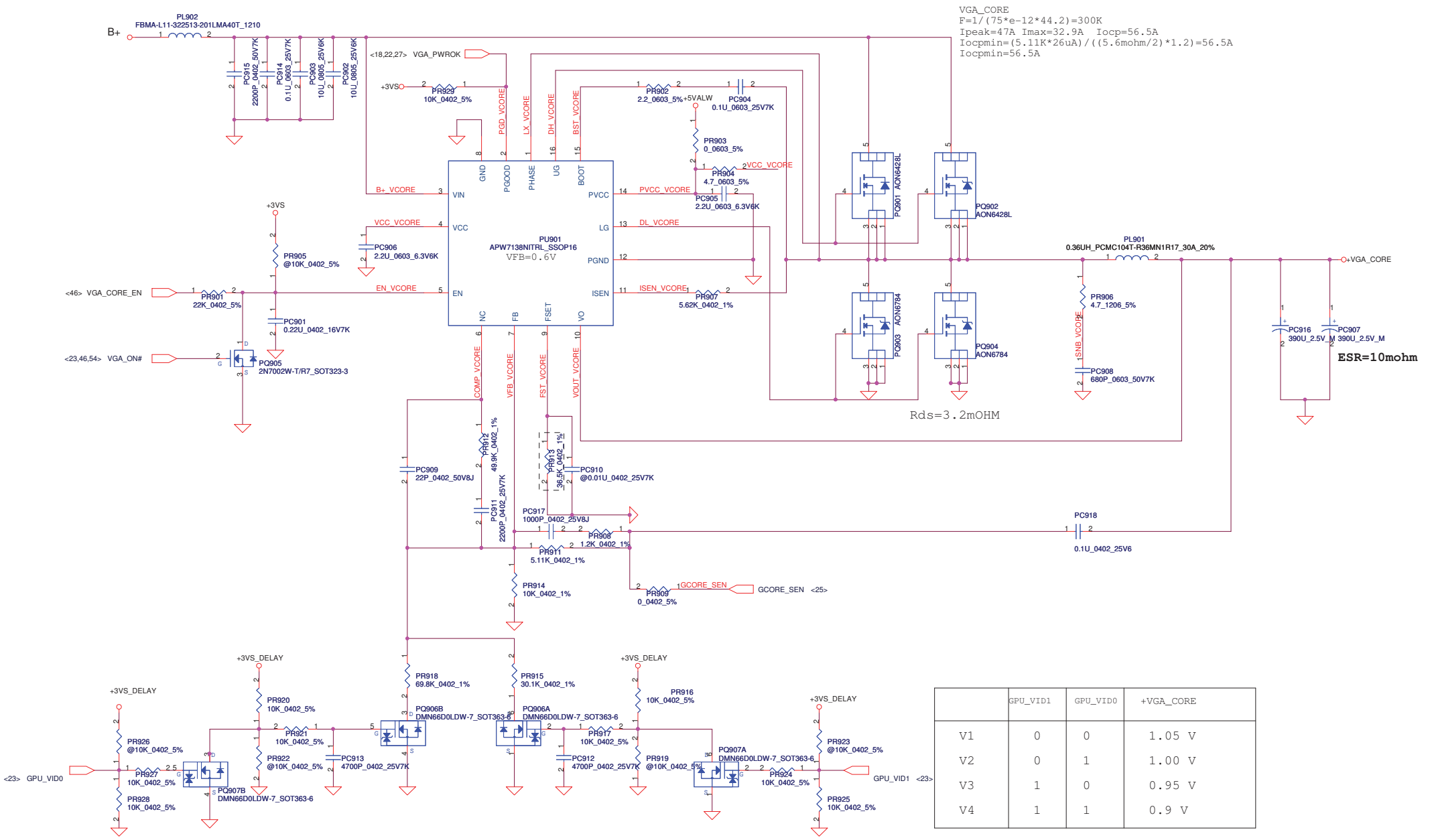
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: **VDDCIP/1.0VSDGPU**

Size	Document Number	Rev
Custom	LA-6931P	0.1

Date: Wednesday, October 27, 2010 | Sheet 54 of 11



	GPU_VID1	GPU_VID0	+VGA_CORE
V1	0	0	1.05 V
V2	0	1	1.00 V
V3	1	0	0.95 V
V4	1	1	0.9 V

Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: +VGA_COREP

Size	Document Number	Rev
Custom	LA-6931P	0.2

Date: Wednesday, October 27, 2010 Sheet 55 of 11

Alert# PU resister need close CPU,
so the PU resister in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resister in POWER schematic.

Parallel and tune length

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE

Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)10U_0805_4V *10
(2)22U_0805_6.3V *15
(3)470U_D2_2V *4(ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP

Ipeak=26A , Imax=18.2A , 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1)22U_0805_6.3V *12
(2)470U_D2_2V *2(ESR=4.5m ohm)

*OCP setting value=37A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2010/12/31

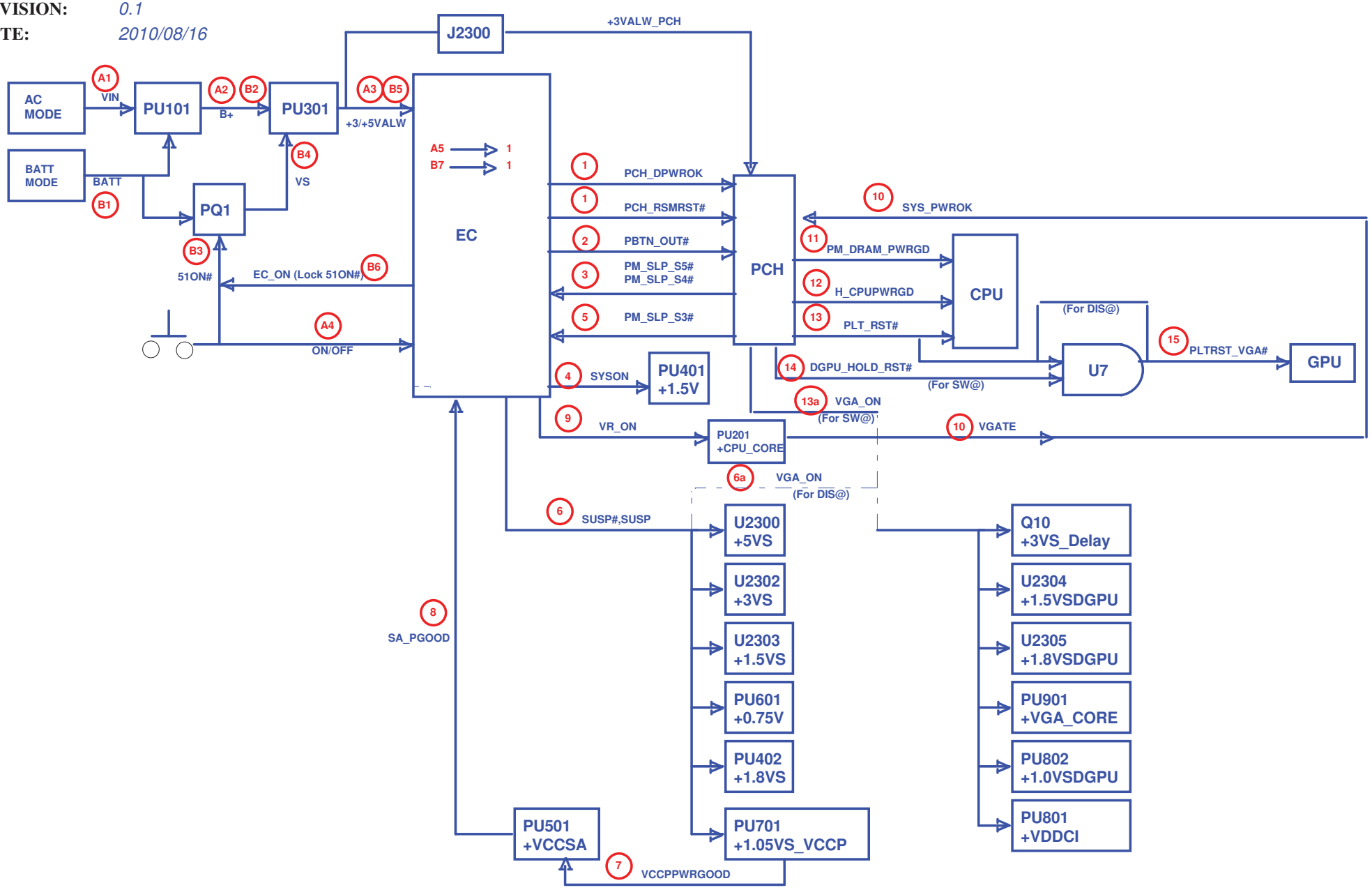
Title: PWR +CPU_CORE/+VGFX_CORE

Size	Document Number	Rev
C	LA-6931P	0.1

Date: Wednesday, October 27, 2010 Sheet 56 of 10

COMPAL CONFIDENTIAL

MODEL NAME: *P5LM0 Power Sequence Block Diagram*
PCB NAME: *LA-6931P*
REVISION: *0.1*
DATE: *2010/08/16*



Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: Power Sequence Block Diagram

Size	Document Number	Rev
Custom	LA-6931P	1.0

Date: Wednesday, October 27, 2010 | Sheet 57 of 58

Version Change List (P. I. R. List) for HW Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	37	USB3.0	8/26	Compal	For USB3.0 wake up function	Instal R2423	0.3
2	30	LVDS	8/26	Compal	For LED panel EDID	Change R2130,R2131,R2185,R2186 from 2.2K to 0 Ohm	0.3
3	35	CIR	8/26	Compal	For CIR can't work	Add R2239,D2201 and pull up to +3VALW on EC side	0.3
4	34	LAN	8/27	Compal	Fine tune LAN_IO rising time	Add C1231 and change R1223 from 47K to 470K Ohm	0.3
5	40	KBC	8/28	Acer	For PWR LED function in low battery mode.	Pull up to +3VALW with R2240 (10K Ohm.)	0.3
6	40	KBC	8/30	Compal	Leakage for +5VS	Delete net "BT_ON" from KBC side	0.3
7	38	Card Reader	8/31	Compal	Card reader function fail	Chang C1318, C1319 to 0.022 uF and 1500 pF	0.3
8	13, 14	PCH	9/06	Compal	Leakage for +3VS	Add R927, D10, D11 to prevent leakage.	0.3
9	18	PCH	9/06	Compal	Leakage for +3V	Add R928, D12 to prevent leakage.	0.3
10	43	Audio	9/09	Compal	SPDIF jack's LED always on.	Add R1148.	0.3
11	33	ODD	9/23	Compal	Don't support ODD zero power	Add R2494, R2495	0.4
12	40	KBC	9/24	Compal	Board ID	Change R2231 from 8.2 K to 33K,	0.4
13	13	PCH	9/29	Compal	HDA_SYNC potential leakage concern.	Add pull down with 1M Ohm (R930) for HDA_SYNC.	0.4
14	30	LVDS	10/1	Compal	Fn+Left/Right hotKey no function, can not adjust brightness	Uninstall R2101 and install R2187	0.4 0.4
15	46	GPU DC-DC	10/2	Compal	Fine tune 1.5VSDGPU timing	Change R2333 from 510K to 470K	0.4
16	46	GPU DC-DC	10/2	Compal	Fine tune 1.8VSDGPU timing	Change R2339 to 33K and C2319 to 2.2u	0.4
17	46	GPU DC-DC	10/2	Compal	For 1.8VSDGPU discharge	Change R2338 from 470 to 220	0.4
18	46	GPU DC-DC	10/2	Compal	For 1.5VSDGPU discharge	Change R2332 from 470 to 220	0.4
19	34	LAN	10/7	Compal	For EMI's request	Add C1232, C1233	0.4
20	14	PCH	10/11	Compal	<RTC Accuracy>Add 90% loading,after 24h about 5s gap,can not meet spec +/-2.5s	Change C853, C854 from 18p to 27p	0.4
21	44	BT	10/20	Compal	For BT discharge	Add R2496, R2497 and Q2407	1.0
22	43	AUDIO	10/20	Compal	Has "po" noise when system enter/resume S3/S4/S5.	Change C1126, C1127 to 0.01u	1.0

Compal Electronics, Inc.

Title: <Title>

Size | Document Number: LA-6931P | Rev: 1.0

Date: Wednesday, October 27, 2010 | Sheet 58 of 58