ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM

X'TAL 14.318MHZ

CLOCK GENERATOR
SELGO: SLG8SP512K05
P2

Merom 479 uFCPGA
P3, P4

CPU Thermal Sensor
P3

FSB 667/800 Mhz

TVOUT CRT
P19

TFT LCD Panel
WXGA
WSXGA+
WUXGA
P18

VGA
LVDS

NB Crestline PM965
P5, P6, P7, P8, P9, P10, P11

Dual Channel DDR2 533/667 MHz

DDRII SO-DIMM 0 SO-DIMM 1
P16

PCI-Express 16X Lan
DVI
LVDS
VGA/TV out

MXM-NB8P-GS (nVidia)
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VRAM 512M
P17

X4 DMI interface

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P24

ODD (PATA)
P24

SATA0
SATA1
PATA

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P12, P13, P14, P15

USB 2.0
Azalia

PCI-Express

PCI Bus

X'TAL 32.768KHZ

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P21

USB Port x 4
USB0~3
P25

CCD
USB7
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Int MIC
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Azalia Audio Controller ALC268&888
P26

Audio Amplifier
P27

MIC Jack
P27

Line in
P27

Connector

Speaker
P27

Phone Jack
P27

MDC 1.5
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LPC

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Touch Pad
P30

K/B COON.
P30

VR
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CIR
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X'TAL24.576MHZ

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R5C832/833
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IEEE 1394 Port
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Media Card Reader
P28

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USB5

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Robson
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PCIE-4
PCIE-1
PCIE-5

PCIE-6

X'TAL 25M

BROADCOM
10/100/1G LAN
5787M
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Transformer
P20

RJ45
P21

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P21, P30

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P33

+1.2V/+1.25V/1.5V/2.5V
P37

5V/3.3V (ISL6236)
P33

BATTERYCHARGER (ISL6251)
P32

DISCHARGE
P37

+1.8V / +1.05V
P35, 36

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Quanta Computer Inc.

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Clock Generator

Change list:
B-test
1.Change U31 P/N to ALPRS365K13 (ICS)

+3V R205 BKP1608HS181-T +3V_VDD_A
C347 10U, C349 1U_4, C340 1U_4, C352 1U_4, C362 1U_4, C342 1U_4, C345 1U_4, C339 10U

+1.25V R220 BKP1608HS181-T +1.25V_VDD
C355 10U, C350 1U_4, C375 1U_4, C372 1U_4, C353 1U_4, C360 1U_4, C359 1U_4, C358 10U

+3V R435 *10K_4 PCI_CLK_SIO R439 10K_4
+3V R443 *10K_4 PCLK_ICH R207 10K_4

+3V R433 10K_4 PCLK_DEBUG
MCH_BSEL0 R446 2.2K_4 CLKUSB_48
MCH_BSEL2 R424 10K_4 FSC

U31

VDD_PCI	2	VDD_I/O	12
VDD_48	9	VDD_PLL3_I/O	20
VDD_PLL3	16	VDD_SRC_I/O_1	26
VDD_SRC	39	VDD_SRC_I/O_2	36
VDD_CPU	55	VDD_SRC_I/O_3	45
VDD_REF	61	VDD_CPU_I/O	49
CPU_STOP#	37		
PCI_STOP#	38		
CKPWRGD/PD#	56		
XTAL_OUT	59	CPU_0	54
XTAL_IN	60	CPU_0#	53
PCI_0/CLKREQ_A#	1	CPU_1_MCH	51
PCI_1/CLKREQ_B#	3	CPU_1_MCH#	50
PCI_2	4	SRC_8/CPU_ITP	47
PCI_3	5	SRC_8#/CPU_ITP#	46
^PCI_4/LCDCLK_SEL	6		
PCIF_5/ITP_EN	7		
		NC	48
USB_48MHz/FS_A	10		
FS_B/TEST_MODE	57		
		LCDCLK/27M	17
		LCDCLK#/27M_SS	18
REF/FS_C/TEST_SEL	62		
SRC_0/DOT_96	13	SRC_2	21
SRC_0#/DOT_96#	14	SRC_2#	22
		SRC_3/CLKREQ_C#	24
SCL	64	SRC_3#/CLKREQ_D#	25
SDA	63	SRC_4	27
		SRC_4#	28
		SRC_6	41
		SRC_6#	40
		SRC_7/CLKREQ_F#	44
		SRC_7#/CLKREQ_E#	43
VSS_PCI	8	SRC_9	30
VSS_48	11	SRC_9#	31
VSS_I/O	15	SRC_10	34
VSS_PLL3	19	SRC_10#	35
VSS_SRC_1	23	SRC_11/CLKREQ_H#	33
VSS_SRC_2	29	SRC_11#/CLKREQ_G#	32
VSS_SRC_3	42		
VSS_CPU	52		
VSS_REF	58		

ICS9LPRS365BGLFT

+3V_VDD_A
0_4 R206 VDD_A_48
0_4 R431 VDD_A_REF

+1.25V_VDD
CPU_STOP# PM_STPCPU# <14>
PCI_STOP# PM_STPPCI# <14>
CKPWRGD/PD# CK_PWRGD <14>

CG_XOUT
CG_XIN
<14> SATACLKREQ# R430 475_4 SATACLKREQ# R
<28> PCLK_PCM R432 33_4 PCI_CLK_7412_R
<22,30> PCLK_DEBUG R434 33_4 PCLK_MINI_R
<31> PCLK_591 R436 33_4 PCLK_591_R
PCI_CLK_SIO R440 33_4 PCI_CLK_SIO_R
<13> PCLK_ICH R444 33_4 PCLK_ICH_R
<14> CLKUSB_48 R447 33_4 FSA
MCH_BSEL1
<14> 14M_ICH R423 33_4 FSC
<7> CLK_DREFCLK RP43 4 3 IV@0X2 DREFCLK_R
<7> CLK_DREFCLK# 2 1 DREFCLK#_R
CGCLK_SMB
CGDAT_SMB

CPU_0 CLK_CPU_BCLK_R RP42 1 2 0X2 CLK_CPU_BCLK <3>
CPU_0# CLK_CPU_BCLK#_R 3 4 CLK_CPU_BCLK# <3>
CPU_1_MCH CLK_MCH_BCLK_R RP44 1 2 0X2 CLK_MCH_BCLK <5>
CPU_1_MCH# CLK_MCH_BCLK#_R 3 4 CLK_MCH_BCLK# <5>
SRC_8/CPU_ITP PCIE_CLK_RBS_R RP46 1 2 0X2 PCIE_CLK_RBS <29>
SRC_8#/CPU_ITP# PCIE_CLK_RBS#_R 3 4 PCIE_CLK_RBS# <29>
LCDCLK/27M CLK_DREFSSCLK_R RP45 3 4 IV@0X2 CLK_DREFSSCLK <7>
LCDCLK#/27M_SS CLK_DREFSSCLK#_R 1 2 CLK_DREFSSCLK# <7>
SRC_2 CLK_PCIE_SATA_R RP47 3 4 0X2 CLK_PCIE_SATA <12>
SRC_2# CLK_PCIE_SATA#_R 1 2 CLK_PCIE_SATA# <12>
SRC_3/CLKREQ_C# CLK_PCIE_LAN_R RP49 3 4 0X2 CLK_PCIE_LAN <20>
SRC_3#/CLKREQ_D# CLK_PCIE_LAN#_R 1 2 CLK_PCIE_LAN# <20>
SRC_4 CLK_PCIE_MINI1_R RP51 3 4 0X2 CLK_PCIE_MINI1 <22>
SRC_4# CLK_PCIE_MINI1#_R 1 2 CLK_PCIE_MINI1# <22>
SRC_6 CLK_PCIE_ICH_R RP50 1 2 0X2 CLK_PCIE_ICH <13>
SRC_6# CLK_PCIE_ICH#_R 3 4 CLK_PCIE_ICH# <13>
SRC_7/CLKREQ_F# PECLK_VGA_R RP48 1 2 EV@0X2 CLK_MXM <17>
SRC_7#/CLKREQ_E# PECLK_VGA#_R 3 4 CLK_MXM# <17>
SRC_9 CLK_PCIE_NEW_C_R RP53 3 4 0X2 CLK_PCIE_NEW_C <23>
SRC_9# CLK_PCIE_NEW_C#_R 1 2 CLK_PCIE_NEW_C# <23>
SRC_10 CLK_PCIE_3GPLL_R RP52 3 4 0X2 CLK_PCIE_3GPLL <7>
SRC_10# CLK_PCIE_3GPLL#_R 1 2 CLK_PCIE_3GPLL# <7>
SRC_11/CLKREQ_H# CLK_PCIE_TV_R RP36 3 4 0X2 CLK_PCIE_TV <22>
SRC_11#/CLKREQ_G# CLK_PCIE_TV#_R 1 2 CLK_PCIE_TV# <22>

C563 33P_4 CG_XIN
<check list>
XTAL length < 500mils
Y4 14.318MHz
C565 33P_4 CG_XOUT

Main: ICS9LPRS365BGLFT:ALPRS365K13
SLG8SP512T: AL8SP512K05

Clock Gen I2C

+3V
Q27 RHU002N06
R428 10K_4 R429 10K_4
<14,16,22,23> PDAT_SMB CGDAT_SMB
+3V
Q28 RHU002N06
<14,16,22,23> PCLK_SMB CGCLK_SMB

CPU Clock select

<3> CPU_BSEL0 R455 0_4 MCH_BSEL0 MCH_BSEL0 <7>
+1.05V R456 *56_4
R450 *1K_4
<3> CPU_BSEL1 R451 0_4 MCH_BSEL1 MCH_BSEL1 <7>
R449 *0_4
+1.05V R454 *1K_4
<3> CPU_BSEL2 R425 0_4 MCH_BSEL2 MCH_BSEL2 <7>
R427 *0_4
+1.05V R426 *1K_4

BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

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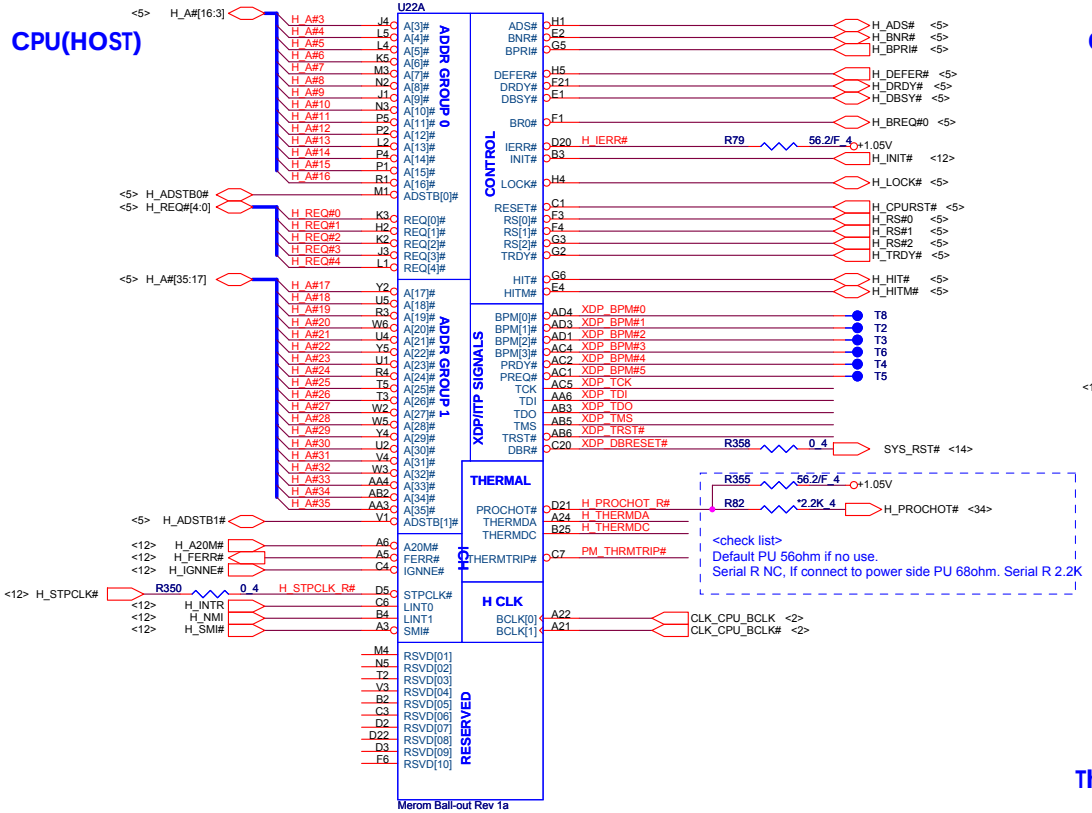
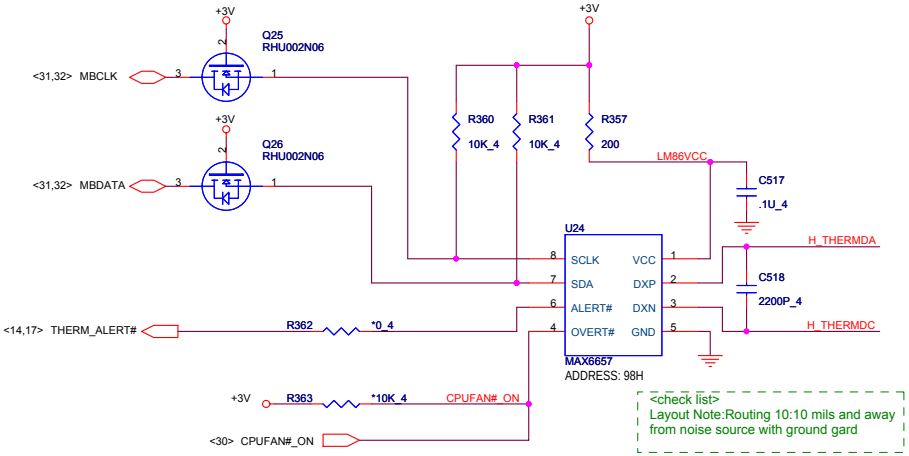
CPU(HOST)



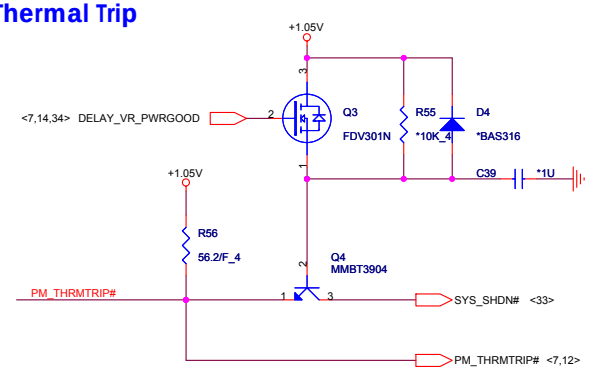
<check list>
Default PU 56ohm if no use.
Serial R NC, If connect to power side PU 68ohm. Serial R 2.2K

CPU Thermal monitor



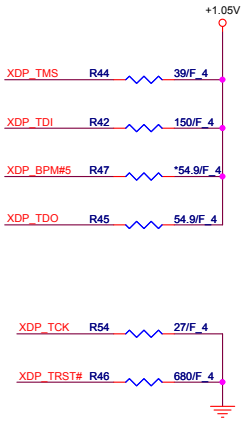
<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard

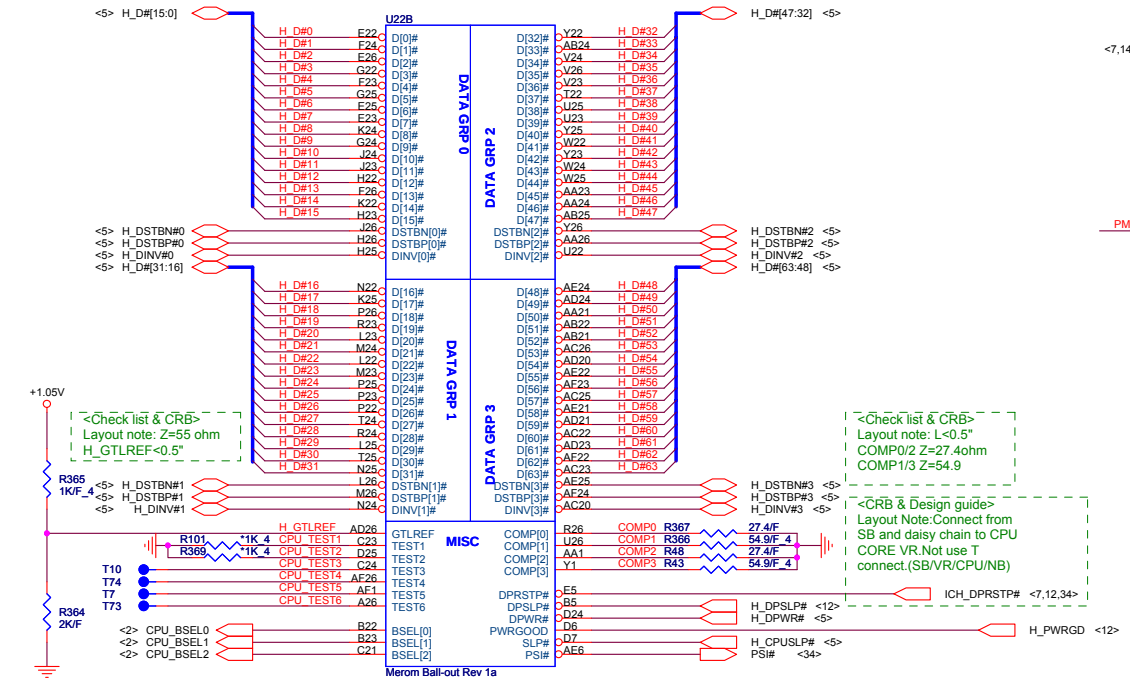
Thermal Trip



<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

PU/PD (ITP700)





<Check list & CRB>
Layout note: Z=55 ohm
H_GTLREF<0.5"

<Check list & CRB>
Layout note: L<0.5"
COMP0/2 Z=27.4ohm
COMP1/3 Z=54.9

<CRB & Design guide>
Layout Note:Connect from SB and daisy chain to CPU CORE VR.Not use T connect.(SB/VR/CPU/NB)

Merom Ball-out Rev 1a

PROJECT : ZD1

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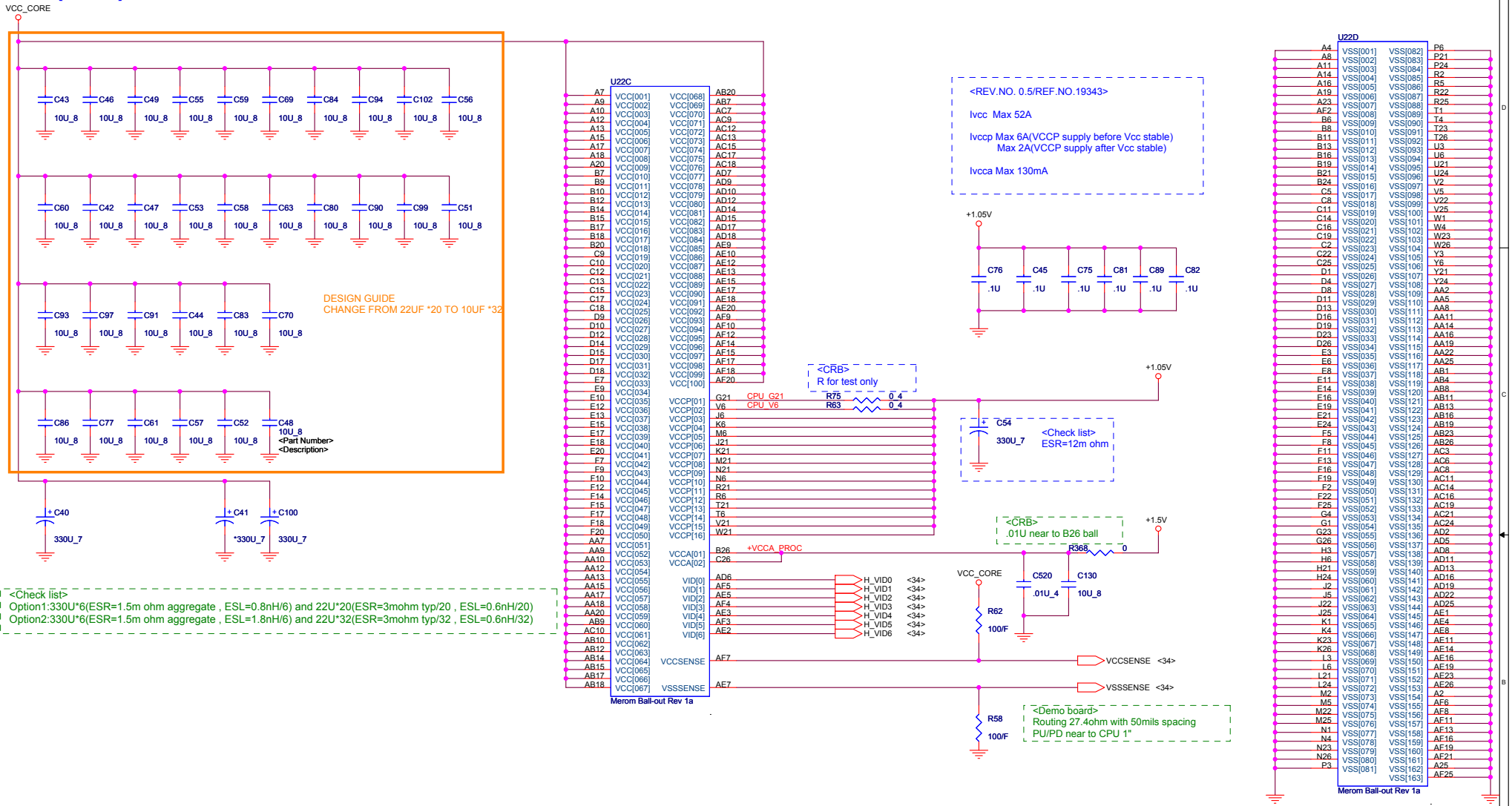
CPU(Power)



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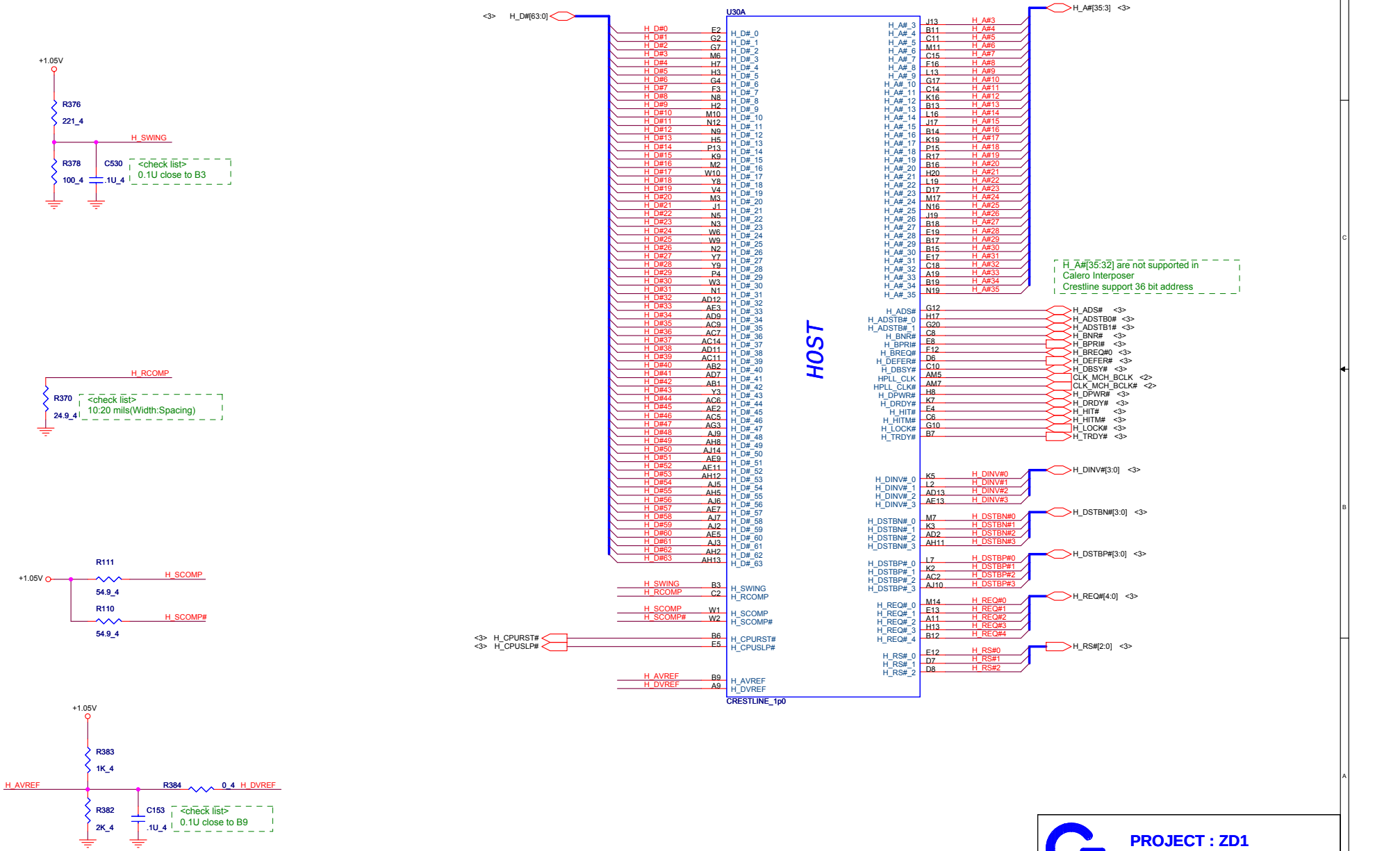
NB(HOST)



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Quanta Computer Inc.		
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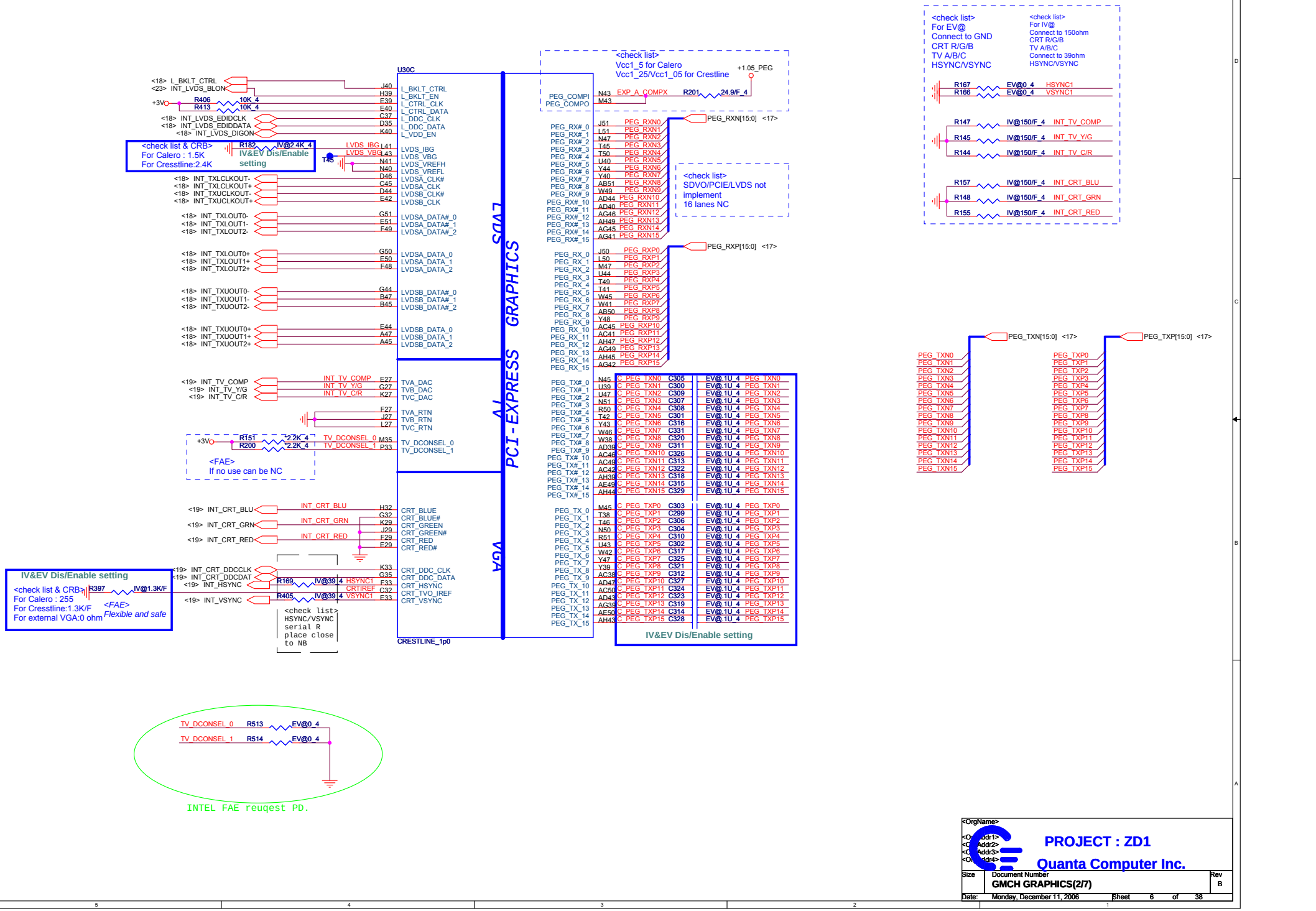
U30C
LVDS
TV
PCI-EXPRESS GRAPHICS
VGA
CRESTLINE_1p0
<check list>
Vcc1_5 for Calero
Vcc1_25/Vcc1_05 for Crestline
+1.05_PEG
PEG_COMPI
PEG_COMPO
N43 EXP_A_COMPX R201 24.9/F_4
M43
PEG_RXN[15:0] <17>
PEG_RXP[15:0] <17>
<check list>
SDVO/PCIE/LVDS not implement
16 lanes NC
PEG_TXN[15:0] <17>
PEG_TXP[15:0] <17>
<check list>
For EV@
Connect to GND
CRT R/G/B
TV A/B/C
HSYNC/VSYNC
<check list>
For IV@
Connect to 150ohm
CRT R/G/B
TV A/B/C
Connect to 39ohm
HSYNC/VSYNC
R167 EV@0_4 HSYNC1
R166 EV@0_4 VSYNC1
R147 IV@150/F_4 INT_TV_COMP
R145 IV@150/F_4 INT_TV_Y/G
R144 IV@150/F_4 INT_TV_C/R
R157 IV@150/F_4 INT_CRT_BLU
R148 IV@150/F_4 INT_CRT_GRN
R155 IV@150/F_4 INT_CRT_RED
L_BKLT_CTRL
INT_LVDS_BLON
R406 10K_4
R413 10K_4
INT_LVDS_EDIDCLK
INT_LVDS_EDIDDATA
INT_LVDS_DIGON
<check list & CRB>
For Calero : 1.5K
For Cresstline:2.4K
R182 IV@2.4K_4
IV&EV Dis/Enable setting
T45
LVDS_IBG
LVDS_VBG
INT_TXLCLKOUT-
INT_TXLCLKOUT+
INT_TXUCLKOUT-
INT_TXUCLKOUT+
INT_TXLOUT0-
INT_TXLOUT1-
INT_TXLOUT2-
INT_TXLOUT0+
INT_TXLOUT1+
INT_TXLOUT2+
INT_TXUOUT0-
INT_TXUOUT1-
INT_TXUOUT2-
INT_TXUOUT0+
INT_TXUOUT1+
INT_TXUOUT2+
INT_TV_COMP
INT_TV_Y/G
INT_TV_C/R
+3V
R151 2.2K_4
R200 2.2K_4
TV_DCONSEL_0
TV_DCONSEL_1
<FAE>
If no use can be NC
INT_CRT_BLU
INT_CRT_GRN
INT_CRT_RED
INT_CRT_DDCCLK
INT_CRT_DDCDAT
INT_HSYNC
INT_VSYNC
R169 IV@39_4 HSYNC1
CRTIREF
R405 IV@39_4 VSYNC1
<check list>
HSYNC/VSYNC serial R place close to NB
IV&EV Dis/Enable setting
<check list & CRB>
For Calero : 255
For Cresstline:1.3K/F
For external VGA:0 ohm
R397 IV@1.3K/F
<FAE>
Flexible and safe
TV_DCONSEL_0 R513 EV@0_4
TV_DCONSEL_1 R514 EV@0_4
INTEL FAE reuqest PD.
<OrgName>
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Quanta Computer Inc.
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GMCH GRAPHICS(2/7)
Rev B
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Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal Cperation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
CRESSTLINE SHOULD USE 20OHM

<check list & CRB>
R Value select
For Calero : 80.6ohm
For Cresstline:20ohm
But check list use 80.6ohm

M_RCOMP# — R387 20/F_4 — <FAE> 80.6ohm — R388 20/F_4 — +1.8VSUS
M_RCOMP

+3V
R170 10K_4 CLK_MCH_OE#
R395 10K_4 PM_EXTTS#0
R149 10K_4 PM_EXTTS#1

DREFSSCLK R411 EV@4.7K_4 +1.25V
DREFSSCLK# R410 EV@4.7K_4
<FAE>
If no use DREFCLK PU and DREFCLK# PD

IV&EV Dis/Enable setting

DREFCLK R409 EV@4.7K_4 +1.25V
DREFCLK# R408 EV@4.7K_4
<design guide>
If no use DREFCLK PU and DREFCLK# PD

MCH_CFG_5 R138 *4.02K/F_4
MCH_CFG_9 R127 *4.02K/F_4
MCH_CFG_12 R139 *4.02K/F_4
MCH_CFG_13 R137 *4.02K/F_4
MCH_CFG_16 R129 *4.02K/F_4

+3V
MCH_CFG_19 R171 *4.02K/F_4
MCH_CFG_20 R174 *4.02K/F_4

+SMDDR_VREF
+1.8VSUS
R416 *1K/F_4
R417 BK1608LL121
+SM_VREF_MCH
R418 *1K/F_4
C295 .1U_4
C143 .1U_4

+1.8VSUS R154 1K/F_4 SM_RCOMP_VOH
R165 3.01K/F_4 C241 .01U_4 C232 2.2U
SM_RCOMP_VOL
R163 1K/F_4 C250 .01U_4 C233 2.2U

INTEL CRB
ADD 0.1UF
C165 .1U_4

U30B

RSVD
P36 RSVD1
P37 RSVD2
R35 RSVD3
N35 RSVD4
AR12 RSVD5
AR13 RSVD6
AM12 RSVD7
AN13 RSVD8
J12 RSVD9
AR37 RSVD10
AM36 RSVD11
AL36 RSVD12
AM37 RSVD13
D20 RSVD14

H10 RSVD20
B51 RSVD21
BJ20 RSVD22
BK22 RSVD23
BF19 RSVD24
BH20 RSVD25
BK18 RSVD26
BJ18 RSVD27
BF23 RSVD28
BG23 RSVD29
BC23 RSVD30
BD24 RSVD31

BH39 RSVD32
AW20 RSVD33
BK20 RSVD34
C48 RSVD35
D47 RSVD36
B44 RSVD37
C44 RSVD38
A35 RSVD39
B37 RSVD40
B36 RSVD41
B34 RSVD42
C34 RSVD43

DDR MUXING
SM_CK_0 AV29 M_CLK0 <16>
SM_CK_1 BB23 M_CLK1 <16>
SM_CK_3 BA25 M_CLK2 <16>
SM_CK_4 AV23 M_CLK3 <16>
SM_CK#_0 AW30 M_CLK#0 <16>
SM_CK#_1 BA23 M_CLK#1 <16>
SM_CK#_3 AW25 M_CLK#2 <16>
SM_CK#_4 AW23 M_CLK#3 <16>
SM_CKE_0 BE29 M_CKE0 <16>
SM_CKE_1 AY32 M_CKE1 <16>
SM_CKE_3 BD39 M_CKE2 <16>
SM_CKE_4 BG37 M_CKE3 <16>
SM_CS#_0 BG20 M_CS#0 <16>
SM_CS#_1 BK16 M_CS#1 <16>
SM_CS#_2 BG16 M_CS#2 <16>
SM_CS#_3 BF13 M_CS#3 <16>
SM_ODT_0 BH18 M_ODT0 <16>
SM_ODT_1 BJ15 M_ODT1 <16>
SM_ODT_2 BJ14 M_ODT2 <16>
SM_ODT_3 BE16 M_ODT3 <16>
SM_RCOMP BL15 M_RCOMP
SM_RCOMP# BK14 M_RCOMP#
SM_RCOMP_VOH BK31 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF_0 AR49 +SM_VREF_MCH
SM_VREF_1 AW4

CLK
DPLL_REF_CLK B42 DREFCLK CLK_DREFCLK <2>
DPLL_REF_CLK# C42 DREFCLK# CLK_DREFCLK# <2>
DPLL_REF_SSCLK H48 DREFSSCLK CLK_DREFSSCLK <2>
DPLL_REF_SSCLK# H47 DREFSSCLK# CLK_DREFSSCLK# <2>
PEG_CLK K44 CLK_PCIE_3GPLL CLK_PCIE_3GPLL <2>
PEG_CLK# K45 CLK_PCIE_3GPLL# CLK_PCIE_3GPLL# <2>

DMI
DMI_RXN_0 AN47 DMI_TXN0
DMI_RXN_1 AJ38 DMI_TXN1
DMI_RXN_2 AN42 DMI_TXN2
DMI_RXN_3 AN46 DMI_TXN3
DMI_TXN[3:0] <13>
DMI_RXP_0 AM47 DMI_TXP0
DMI_RXP_1 AJ39 DMI_TXP1
DMI_RXP_2 AN41 DMI_TXP2
DMI_RXP_3 AN45 DMI_TXP3
DMI_TXP[3:0] <13>
DMI_TXN_0 AJ46 DMI_RXN0
DMI_TXN_1 AJ41 DMI_RXN1
DMI_TXN_2 AM40 DMI_RXN2
DMI_TXN_3 AM44 DMI_RXN3
DMI_RXN[3:0] <13>
DMI_TXP_0 AJ47 DMI_RXP0
DMI_TXP_1 AJ42 DMI_RXP1
DMI_TXP_2 AM39 DMI_RXP2
DMI_TXP_3 AM43 DMI_RXP3
DMI_RXP[3:0] <13>

CFG
<2> MCH_BSEL0 P27 CFG_0
<2> MCH_BSEL1 N27 CFG_1
<2> MCH_BSEL2 N24 CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
T30 MCH_CFG_3 C21
T75 MCH_CFG_4 C23
MCH_CFG_5 F23
T34 MCH_CFG_6 N23
T24 MCH_CFG_7 G23
T29 MCH_CFG_8 J20
MCH_CFG_9 C20
T37 MCH_CFG_10 R24
T28 MCH_CFG_11 L23
MCH_CFG_12 J23
MCH_CFG_13 E23
MCH_CFG_14 E20
T25 MCH_CFG_15 K23
T27 MCH_CFG_16 M20
MCH_CFG_17 M24
T32 MCH_CFG_18 L32
T40 MCH_CFG_19 N33
MCH_CFG_20 L35

PM
<14> PM_BMBUSY# R184 0_4 PM_BMBUSY#_R G41 PM_BM_BUSY#
<3,12,34> ICH_DPRSTP# R177 0_4 ICH_DPRSTP#_R L39 PM_DPRSTP#
<16> PM_EXTTS#0 R401 0_4 PM_EXTTS#0_R L36 PM_EXT_TS#_0
<16> PM_EXTTS#1 R150 0_4 PM_EXTTS#1_R J36 PM_EXT_TS#_1
<3,14,34> DELAY_VR_PWRGOOD AW49 PWROK
<13> PLTRST#_NB R140 100_4 RST_IN#_MCH AV20 RSTIN#
<3,12> PM_THRMTRIP# R130 *0_4 PM_THRMTRIP#_GMCH N20 THERMTRIP#
<14,34> PM_DPRSLPVR R407 0_4 PM_DPRSLPVR_GMCH G36 DPRSLPVR

GRAPHICS VID
GFX_VID_0 E35 MCH_GFX_VID_0 T41
GFX_VID_1 A39 MCH_GFX_VID_1 T42
GFX_VID_2 C38 MCH_GFX_VID_2 T43
GFX_VID_3 B39 MCH_GFX_VID_3 T44
GFX_VR_EN E36 R183 *0_4 SUSB# <14,31>

ME
CL_CLK AM49 CL_CLK0 <14>
CL_DATA AK50 CL_DATA0 <14>
CL_PWROK AT43 MPWROK <14,31>
CL_RST# AN49 CL_RST#0 <14>
CL_VREF AM50 +1.25V_CL_VREF

MISC
NC_1 BJ51
NC_2 BK51
NC_3 BK50
NC_4 BL50
NC_5 BL49
NC_6 BL3
NC_7 BL2
NC_8 BK1
NC_9 BJ1
NC_10 E1
NC_11 A5
NC_12 C51
NC_13 B50
NC_14 A50
NC_15 A49
NC_16 BK2
SDVO_CTRL_CLK H35
SDVO_CTRL_DATA K36
CLK_REQ# G39 CLK_MCH_OE#
ICH_SYNC# G40 MCH_ICH_SYNC# <14>
TEST_1 A37 GMCH_TEST1 R178 0_4
TEST_2 R32 GMCH_TEST2 R168 20K_4

CRESTLINE_1p0

+1.25V
R422 1K/F_4
C559 .1U_4
R420 392/F

DREFCLK R529 EV@0_4
DREFCLK# R531 EV@0_4
DREFSSCLK R532 EV@0_4
DREFSSCLK# R533 EV@0_4
INTEL FAE suggest PD for external graphics

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (STRAPPING/OTHER 3/7)	B

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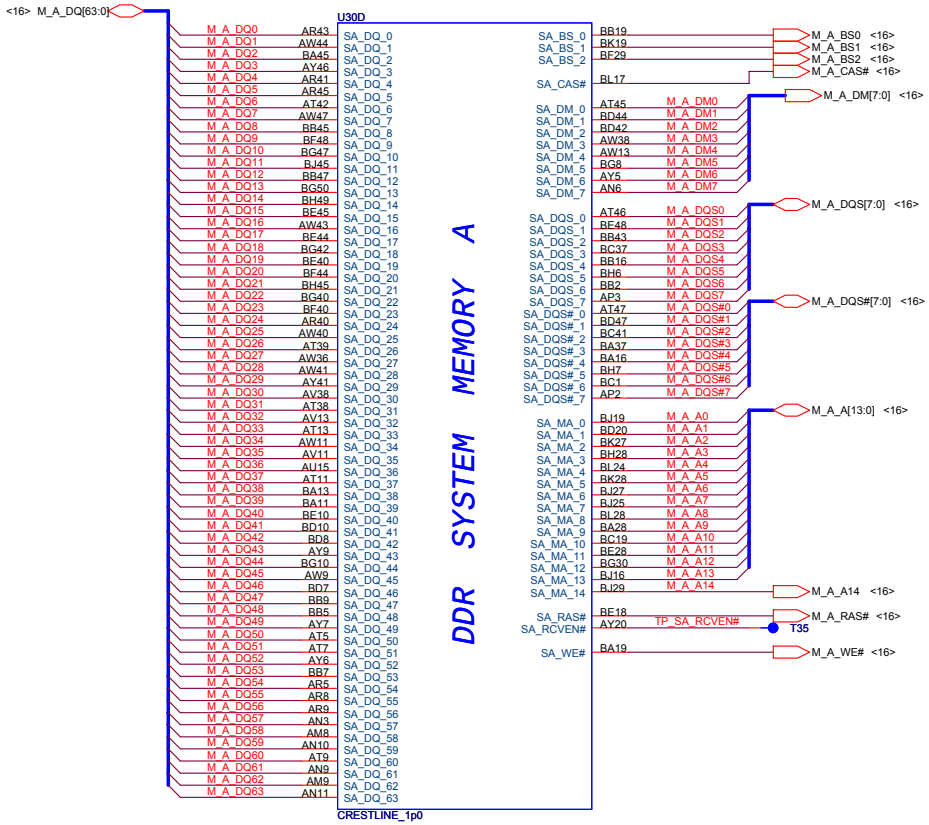
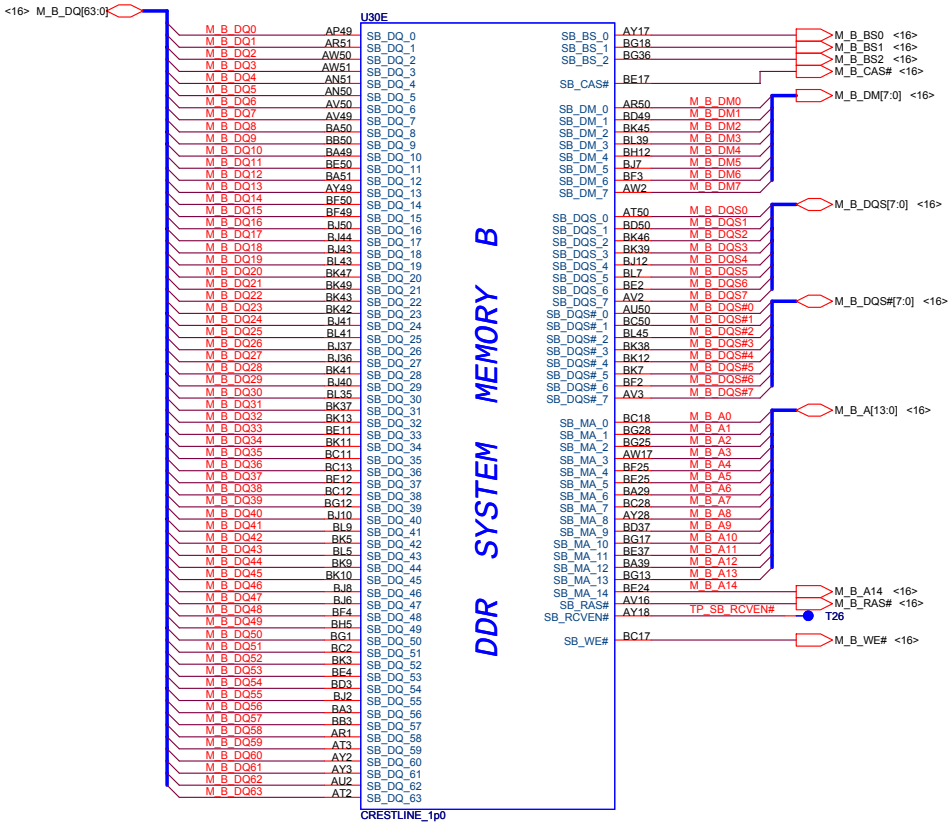
NB(Memory controller)





PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(4/7)	B

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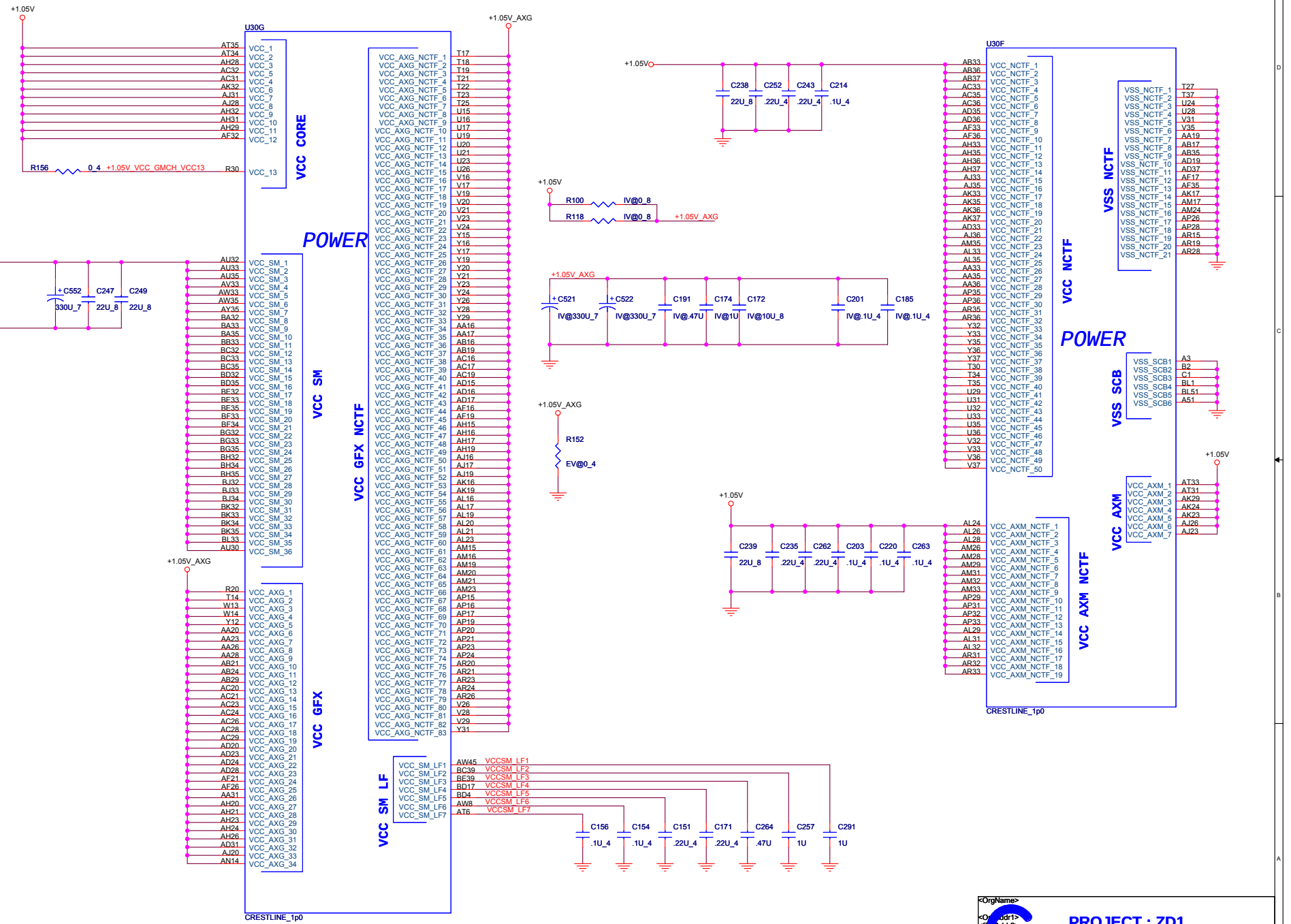
NB(Power-1)



<OrgName>
<Addr1>
<Addr2>
<Addr3>
<Addr4>

PROJECT : ZD1

Quanta Computer Inc.

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	GMCH Power-1(5/7)	B

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NB(Power-2)

CRT/TV Disable/Enable guideline

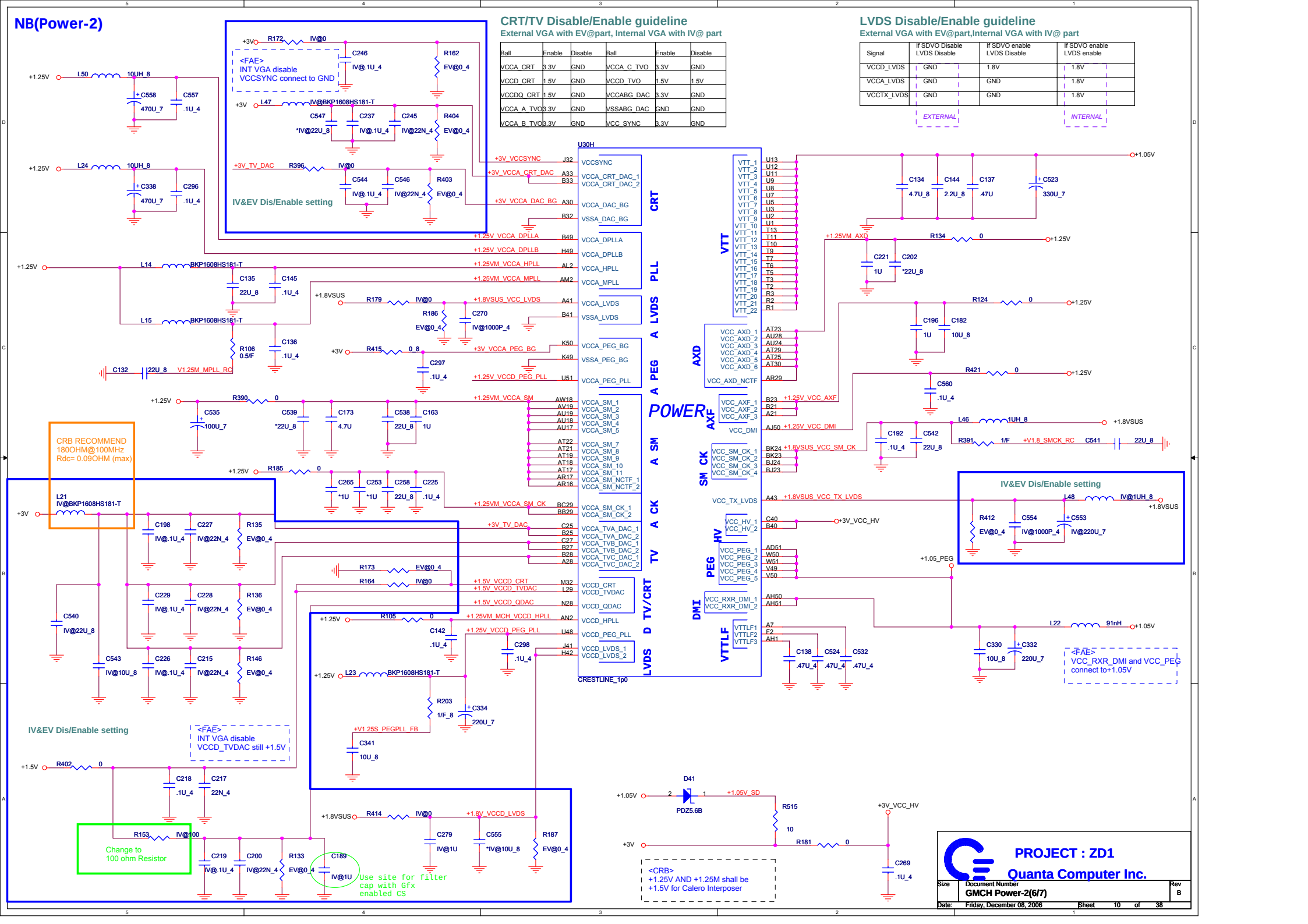
External VGA with EV@part, Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

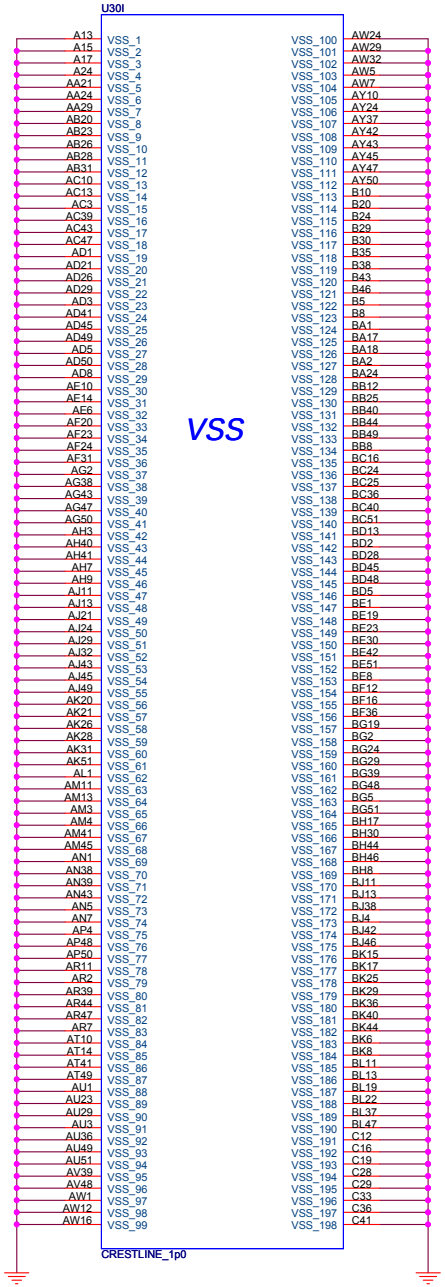
External VGA with EV@part,Internal VGA with IV@ part

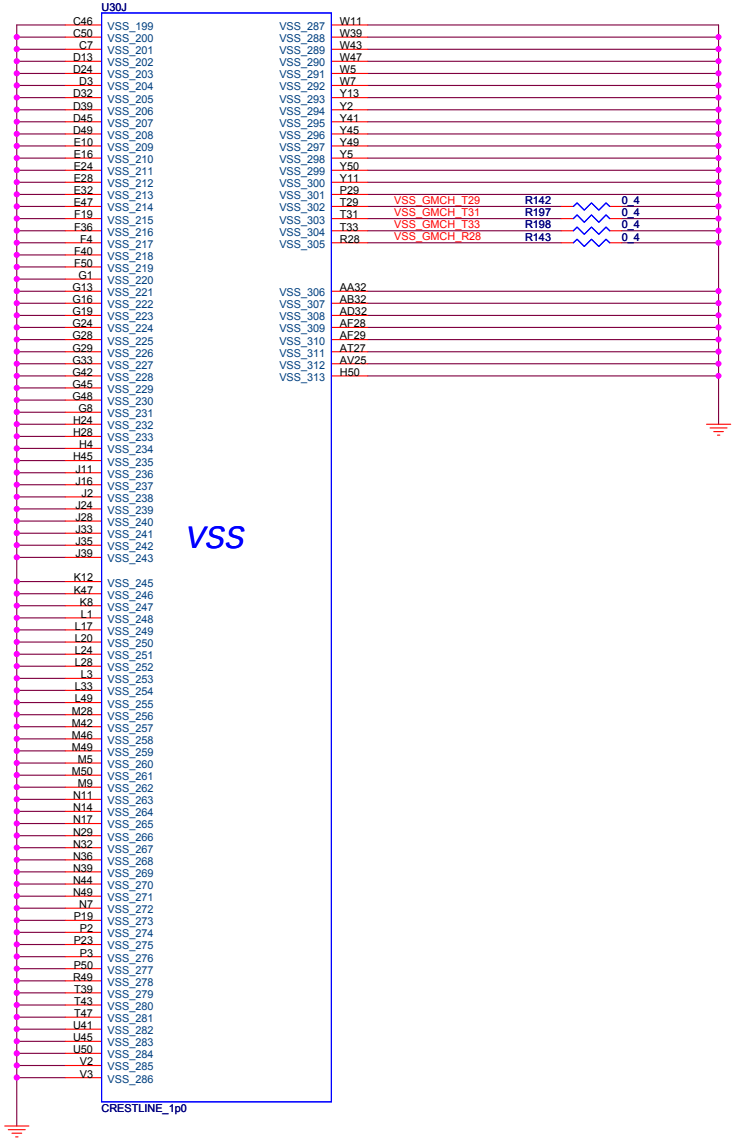
Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V
	EXTERNAL		INTERNAL



PROJECT :	ZD1
Quanta Computer Inc.	
Size	Document Number: GMCH Power-2(6/7) — Rev: B
Date: Friday, December 08, 2006	Sheet 10 of 38

NB(Power-3)





PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-3(7/7)	B
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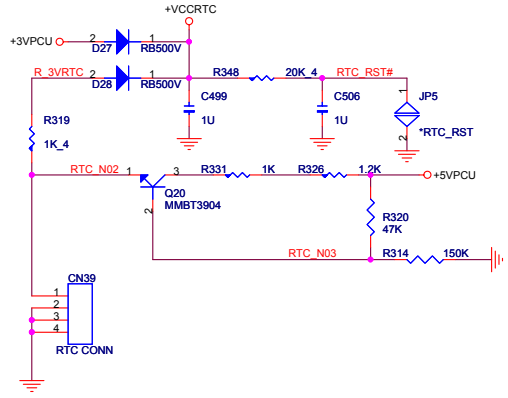
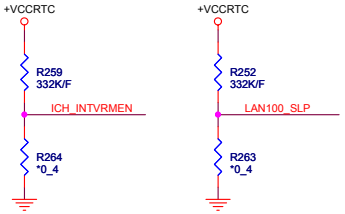
RTC



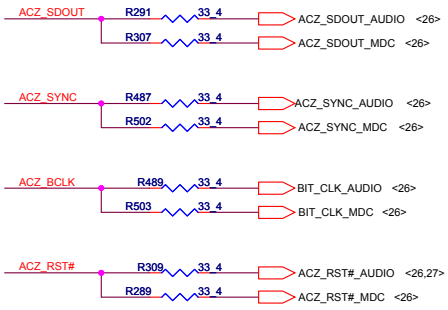
SB Strap

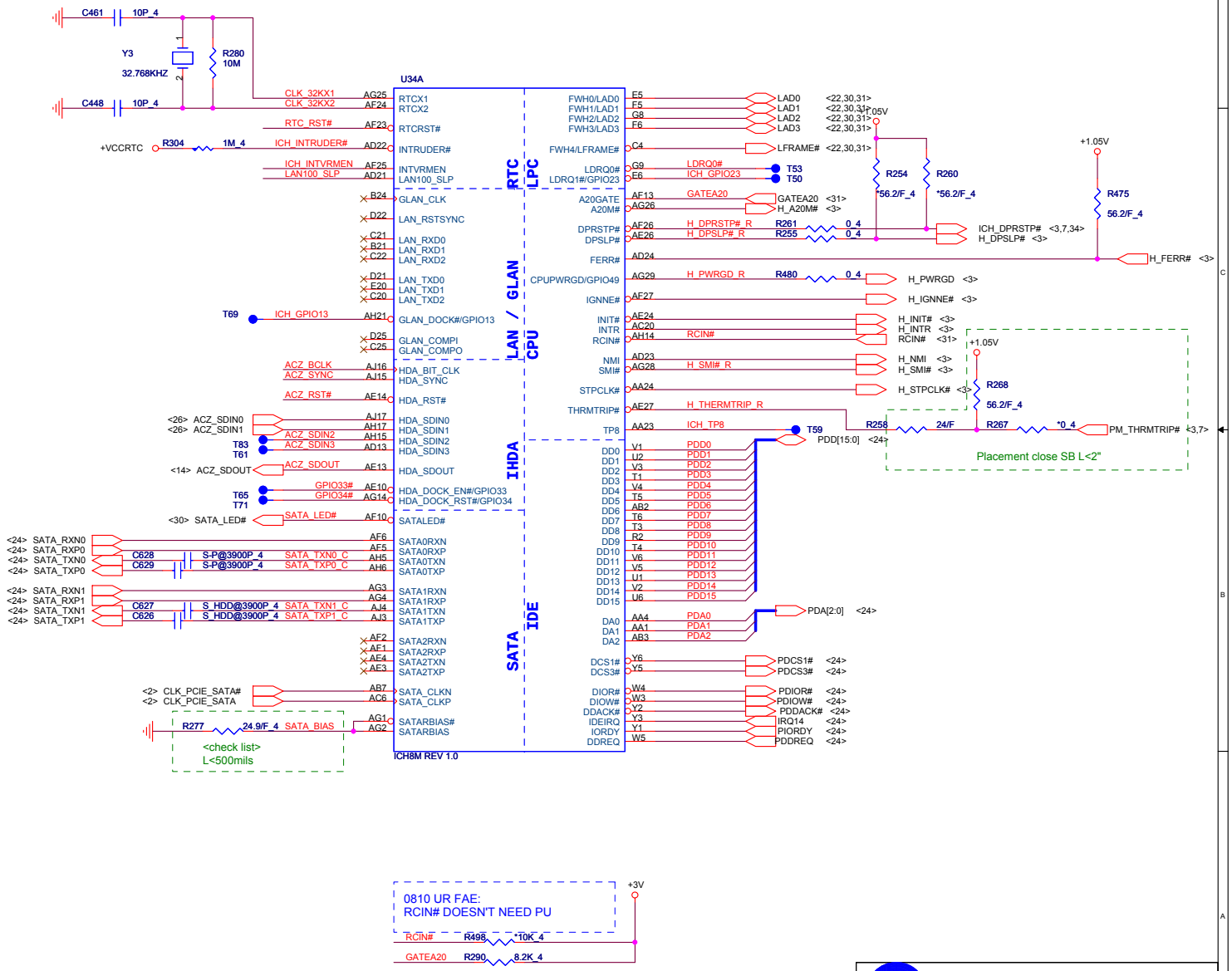
INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



HDA





PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M HOST(1/4)	B
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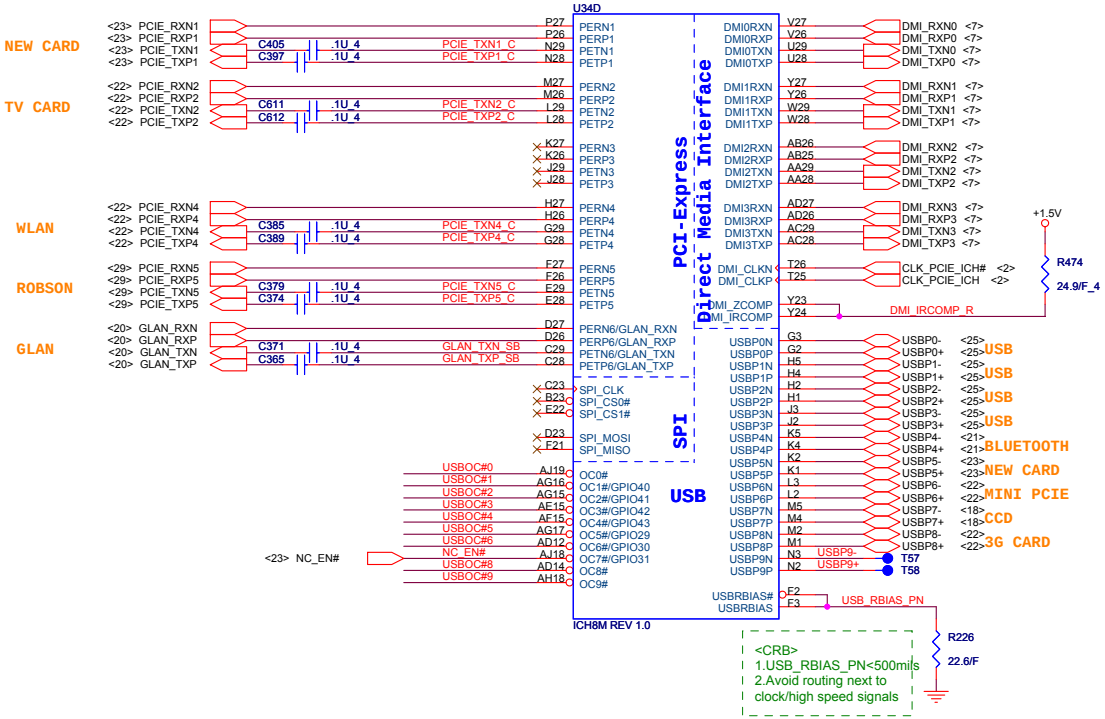
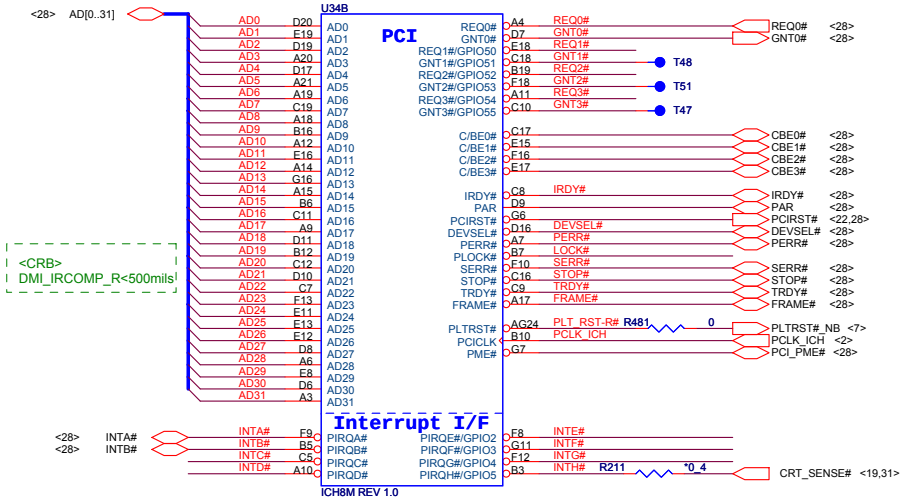
SB-PCIE/USB/DMI

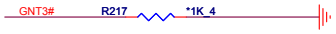


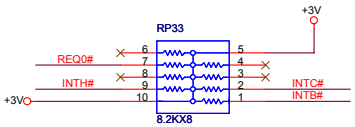
SB-PCI

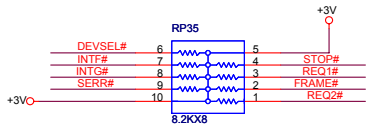


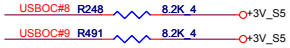
A16 SWAP Override strap

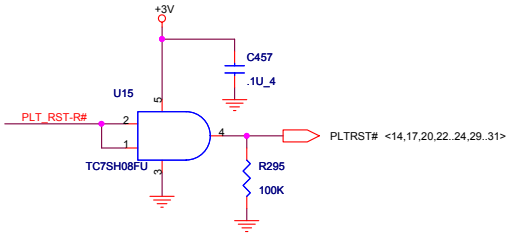
PCI_GNT#3	Low = A16 swap override enabled High = Default

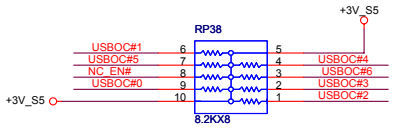


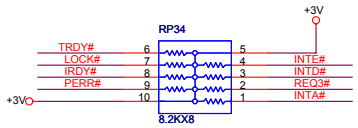












PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE\PCI\USB(2/4)	B
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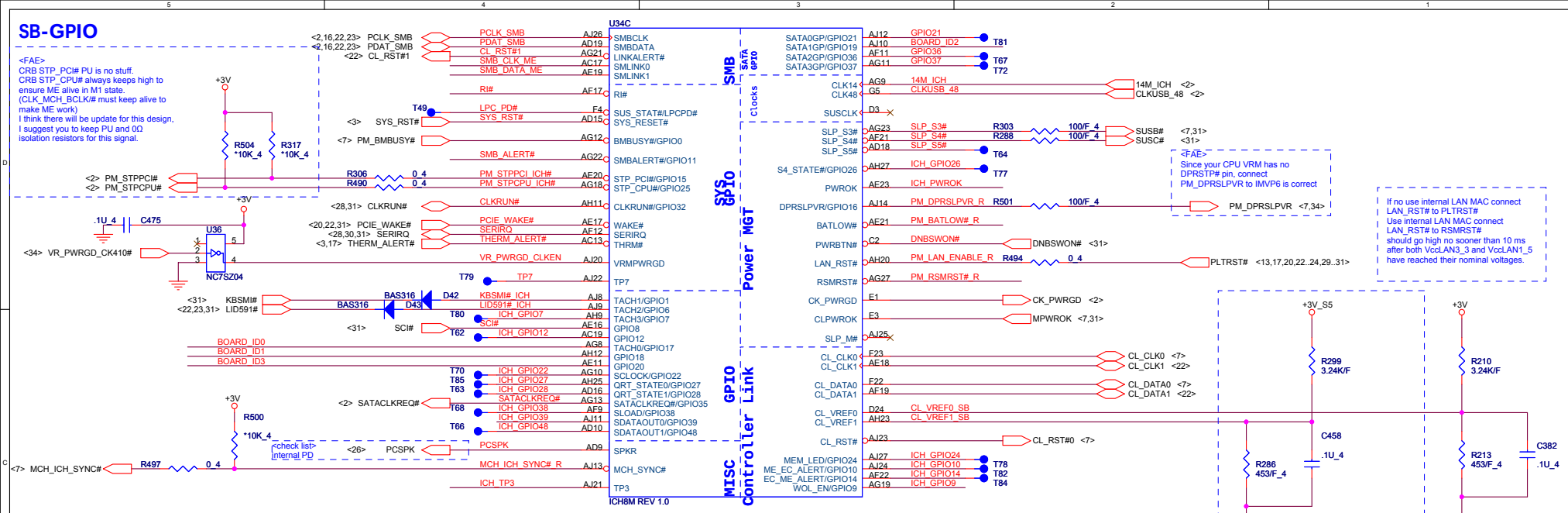
SB-GPIO



<FAE>
CRB STP_PCI# PU is no stuff.
CRB STP_CPU# always keeps high to ensure ME alive in M1 state.
(CLK_MCH_BCLK/# must keep alive to make ME work)
I think there will be update for this design, I suggest you to keep PU and 0Ω isolation resistors for this signal.

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST#
should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

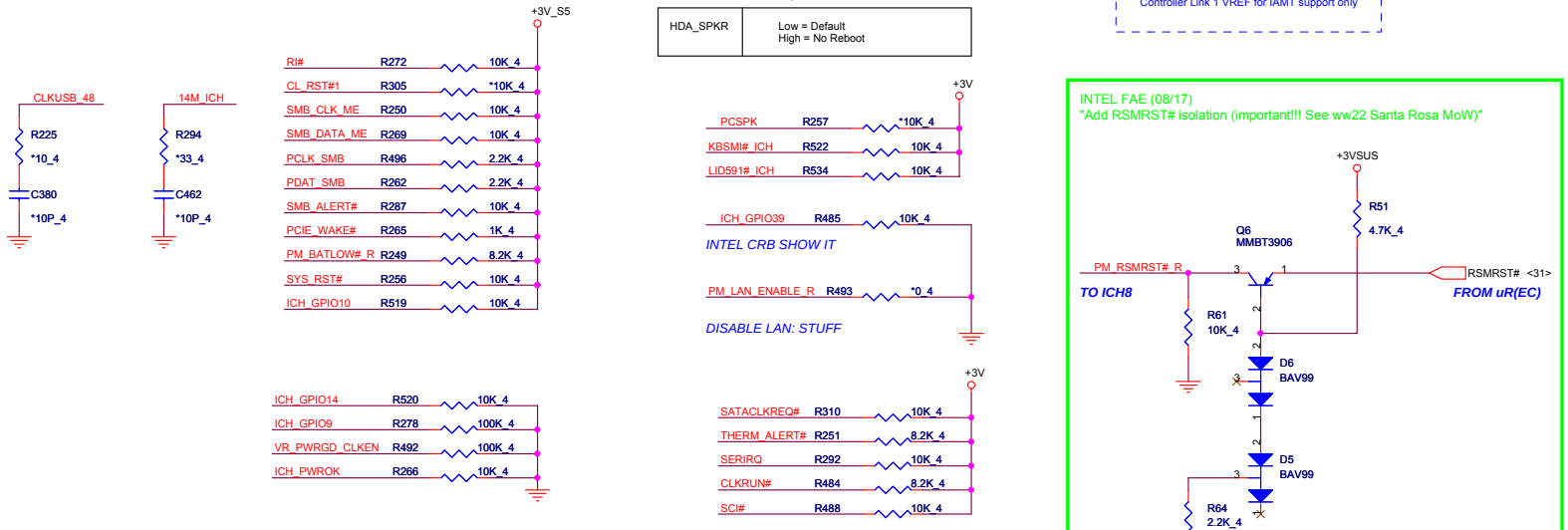
Controller Link 1 VREF for IAMT support only

No Reboot strap

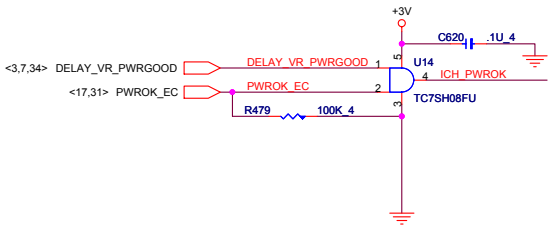
HDA_SPKR	Low = Default High = No Reboot

XOR Chain Entrance Strap

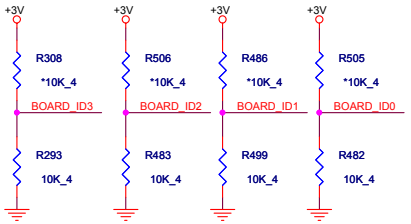
ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1



INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"



Board ID	ID3	ID2	ID1	ID0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0



PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M GPIO(3/4)	B
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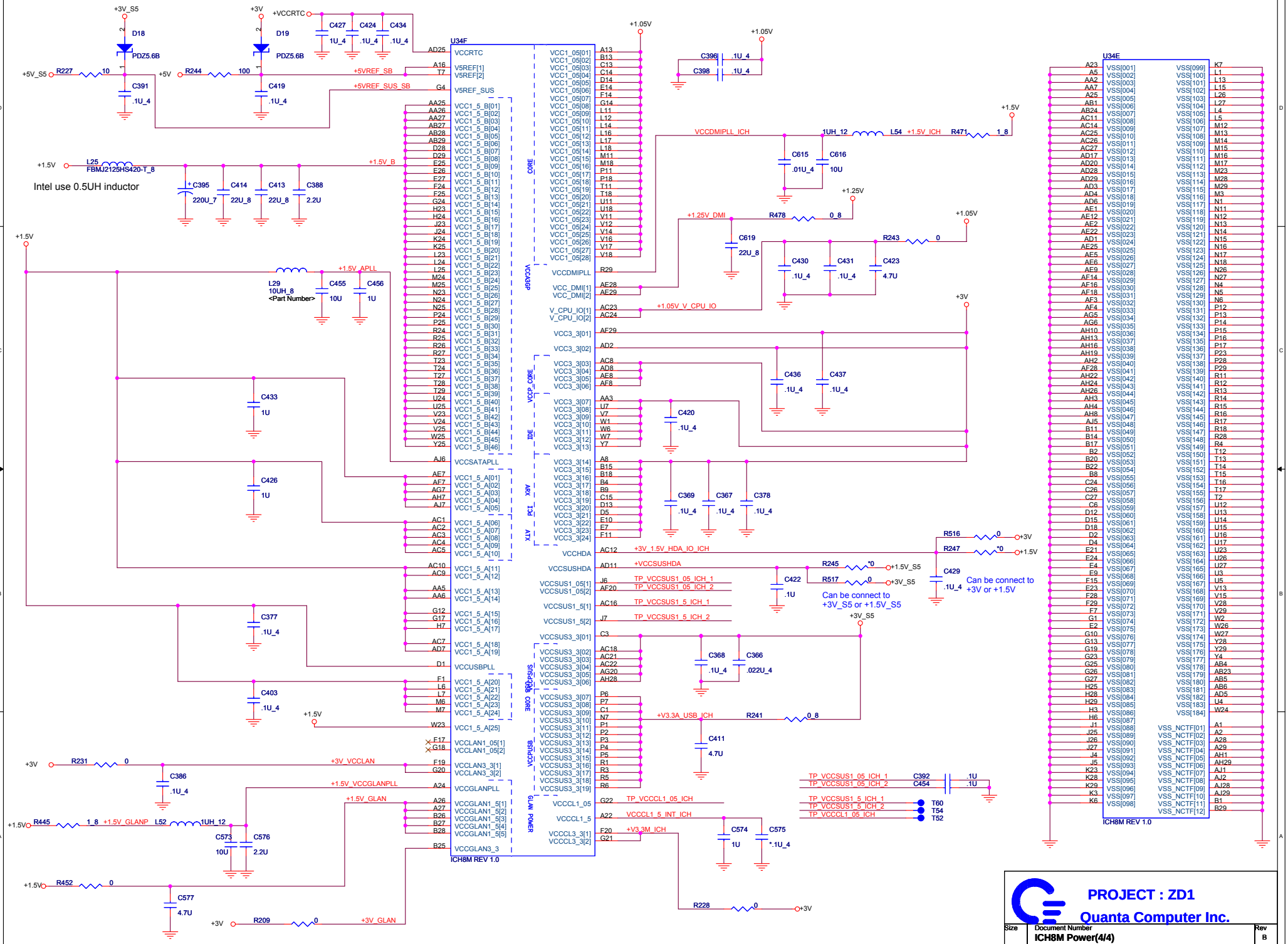
U34F
ICH8M REV 1.0
U34E
ICH8M REV 1.0
Intel use 0.5UH inductor
Can be connect to +3V or +1.5V
Can be connect to +3V_S5 or +1.5V_S5
PROJECT : ZD1
Quanta Computer Inc.
ICH8M Power(4/4)
Size
Document Number
Rev
B
Date: Friday, December 08, 2006
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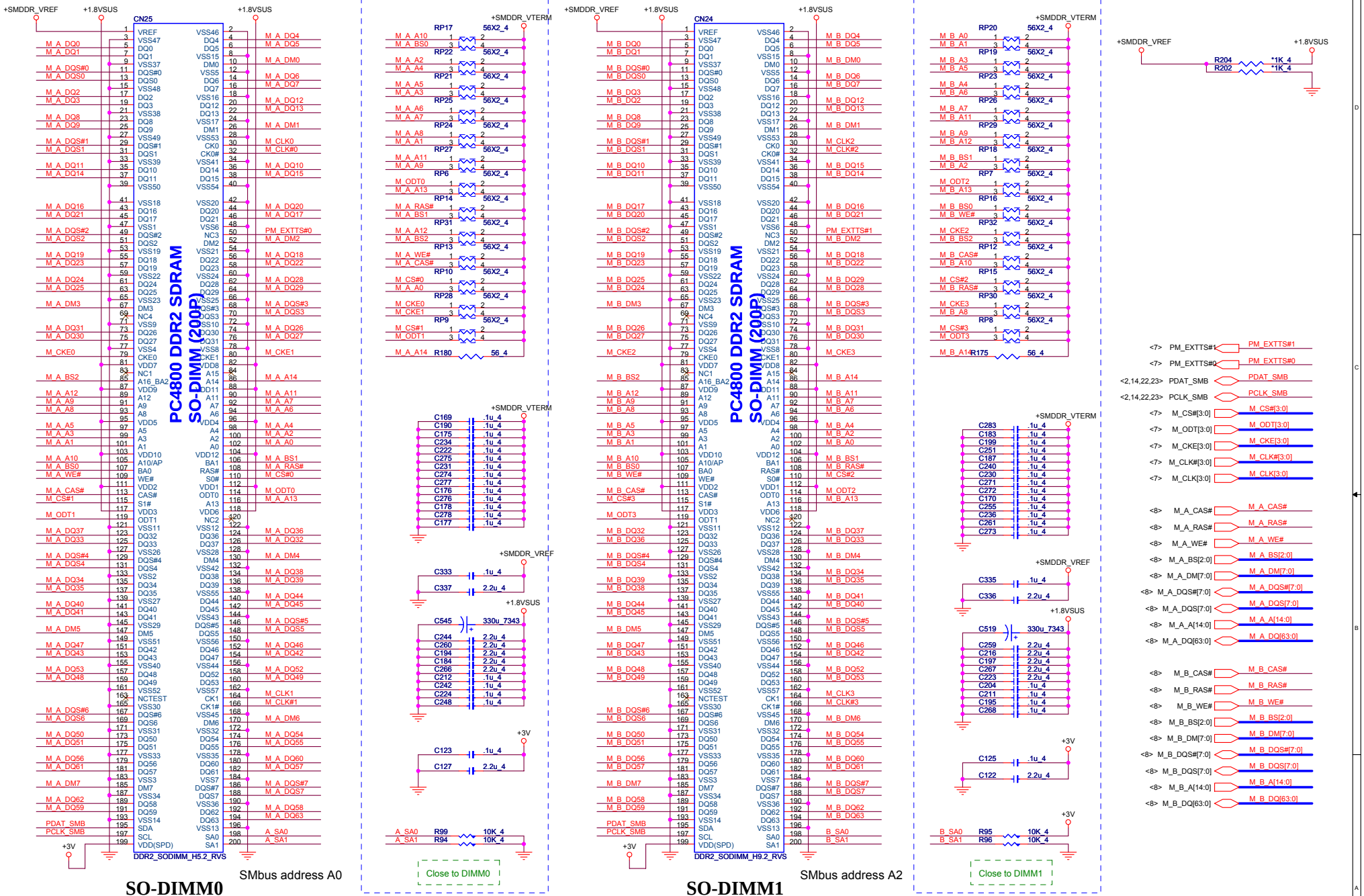

Project : ZD1		
Quanta Computer Inc.		
Size	Document Number: DDRII SO-DIMM	Rev: B
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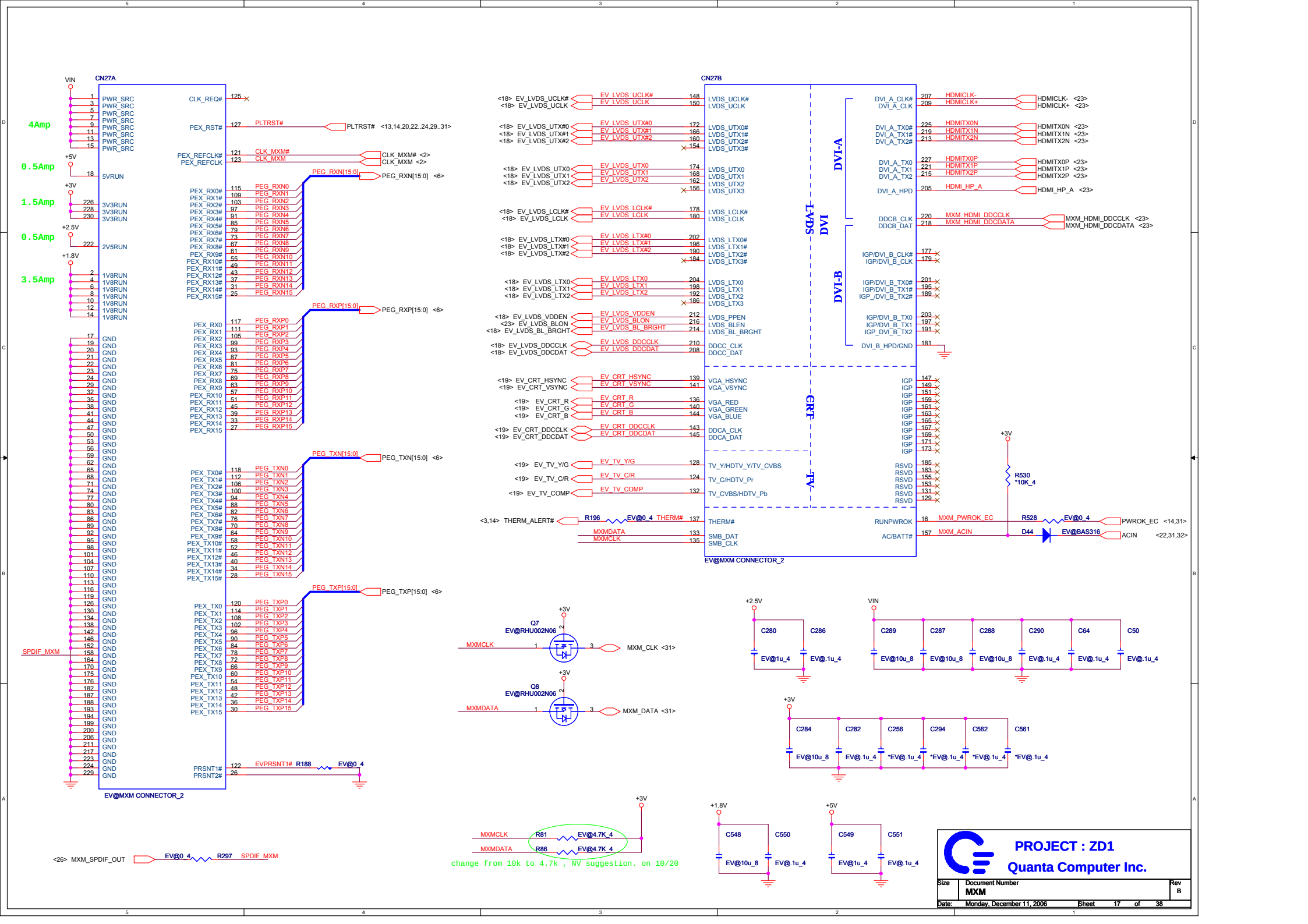

PROJECT : ZD1

Quanta Computer Inc.

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	MXM	B

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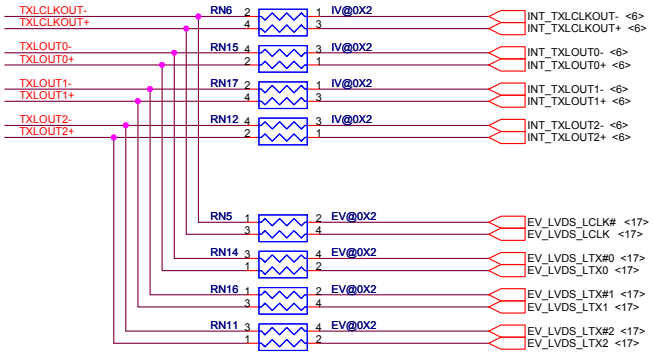
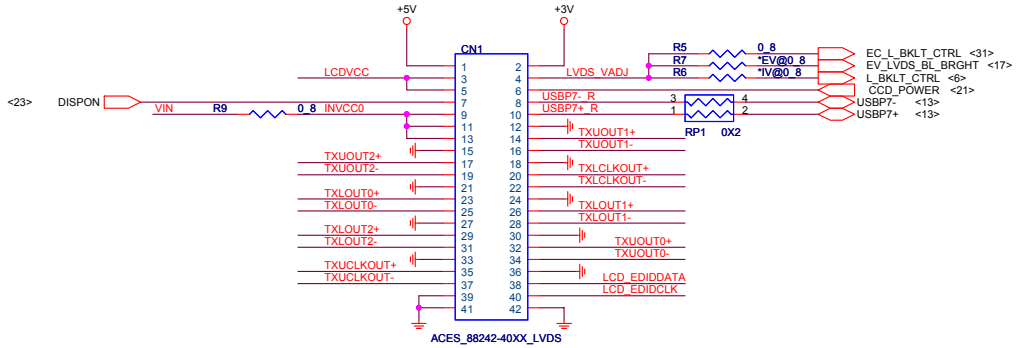
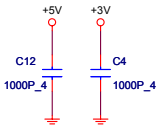
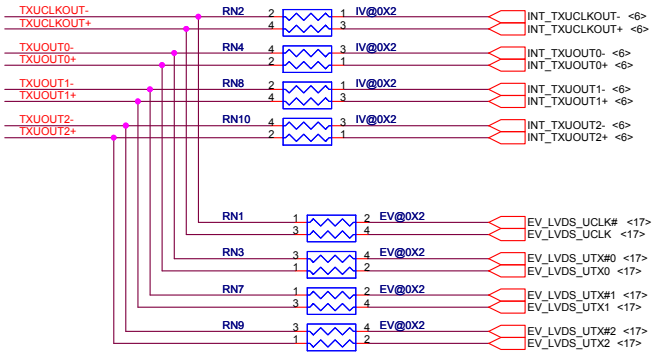
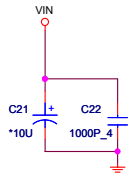
LVDS

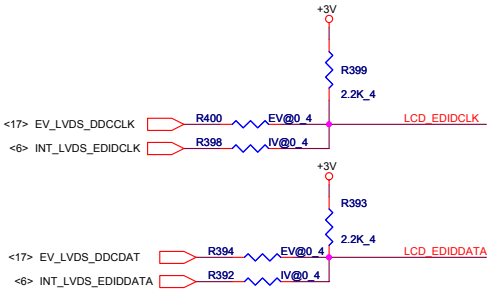


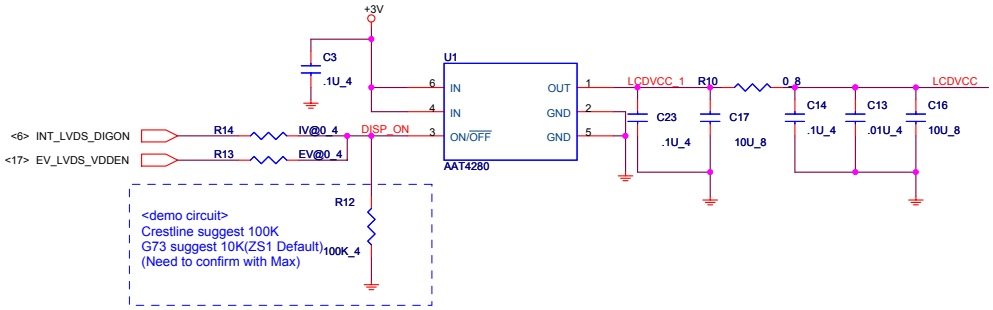












PROJECT : ZD1

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	LVDS	B
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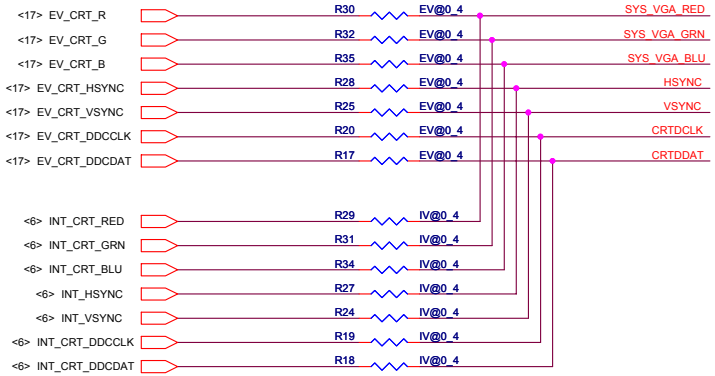
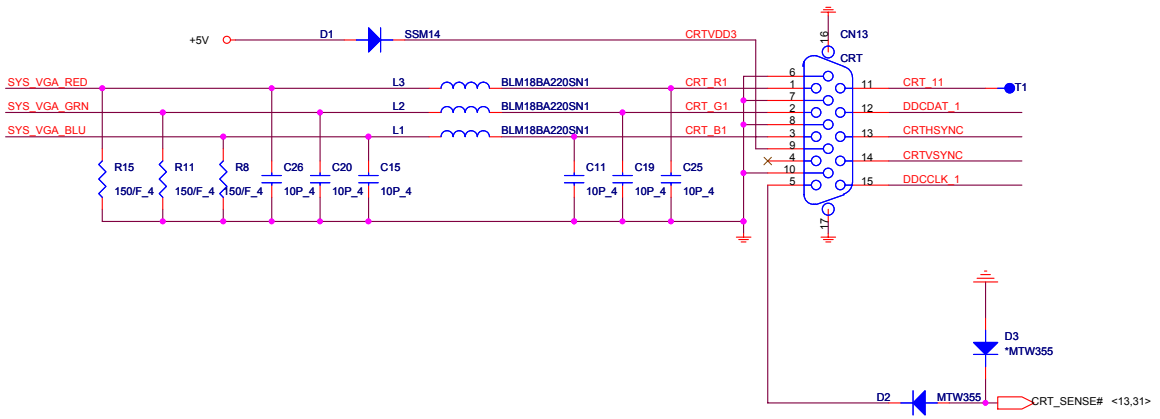
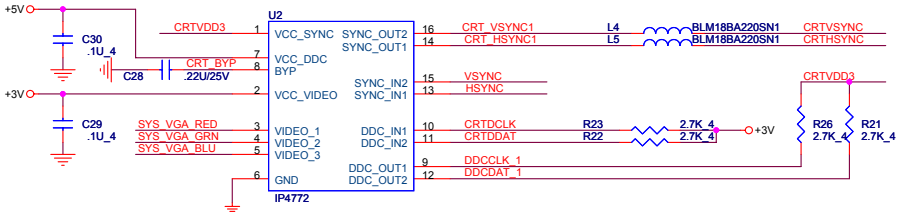
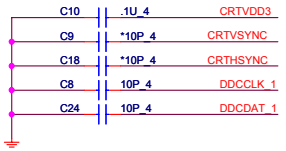
CRT Select



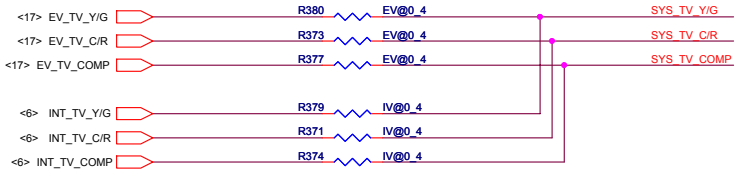
CRT CONNECTOR AND ESD

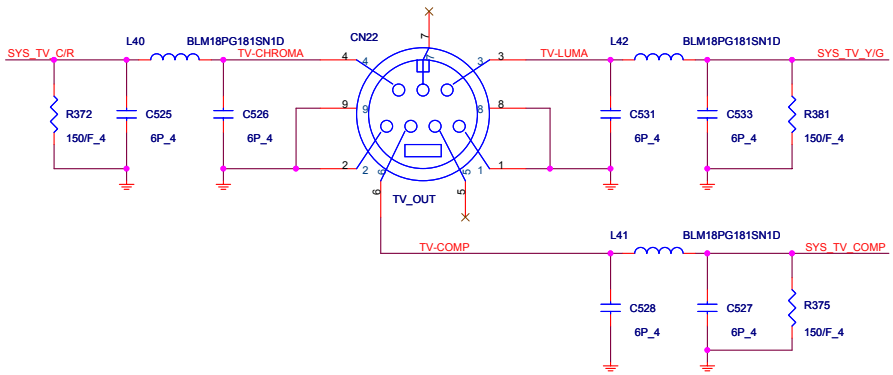


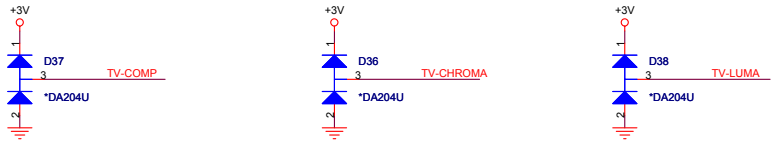




TV Out (SVHS) MiniDIN 7-pin







PROJECT : ZD1

Quanta Computer Inc.

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	CRT/TVOUT	B

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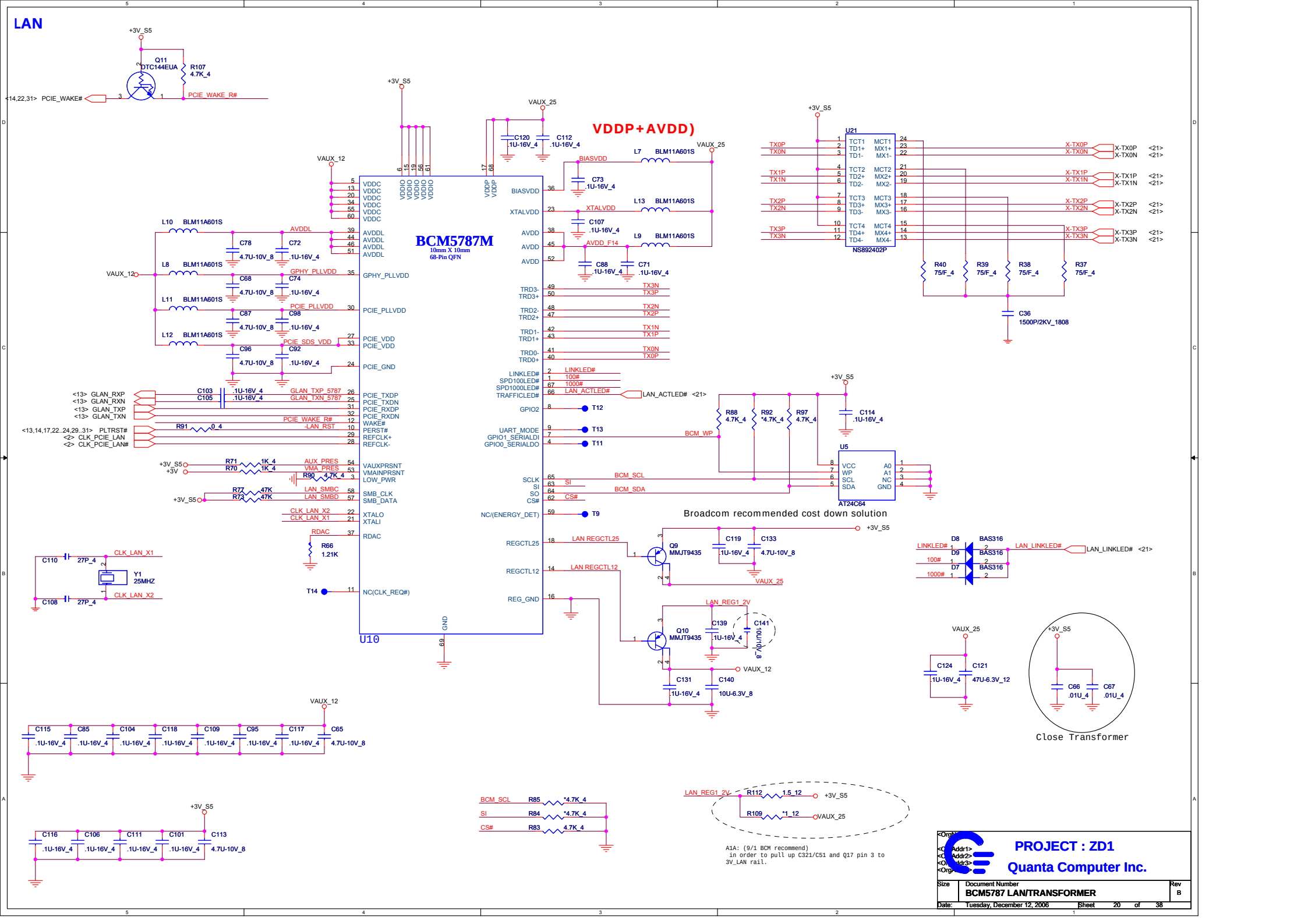
LAN


+3V_S5
Q11
DTC144EUA
R107
4.7K_4
<14,22,31> PCIE_WAKE#
PCIE_WAKE_R#
VAUX_25
VAUX_12
BCM5787M
10mm X 10mm
68-Pin QFN
U10
VDDP+AVDD)
L7 BLM11A601S
L13 BLM11A601S
L9 BLM11A601S
L10 BLM11A601S
L8 BLM11A601S
L11 BLM11A601S
L12 BLM11A601S
BIASVDD
XTALVDD
AVDD_F14
GPHY_PLLVDD
PCIE_PLLVDD
PCIE_SDS_VDD
PCIE_GND
PCIE_VDD
PCIE_TXDP
PCIE_TXDN
PCIE_RXDP
PCIE_RXDN
WAKE#
PERST#
REFCLK+
REFCLK-
VAUXPRSNT
VMAINPRSNT
LOW_PWR
SMB_CLK
SMB_DATA
XTALO
XTALI
RDAC
NC(CLK_REQ#)
REGCTL25
REGCTL12
REG_GND
GND
TRD3-
TRD3+
TRD2-
TRD2+
TRD1-
TRD1+
TRD0-
TRD0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
LAN_ACTLED# <21>
GPIO2
UART_MODE
GPIO1_SERIALDI
GPIO0_SERIALDO
SCLK
SI
SO
CS#
NC/(ENERGY_DET)
U21
NS892402P
X-TX0P
X-TX0N
X-TX1P
X-TX1N
X-TX2P
X-TX2N
X-TX3P
X-TX3N
R40 75/F_4
R39 75/F_4
R38 75/F_4
R37 75/F_4
C36 1500P/2KV_1808
R88 4.7K_4
R92 *4.7K_4
R97 4.7K_4
C114 .1U-16V_4
BCM_WP
BCM_SCL
BCM_SDA
U5
AT24C64
Broadcom recommended cost down solution
Q9 MMJT9435
Q10 MMJT9435
C119 .1U-16V_4
C133 4.7U-10V_8
C139 .1U-16V_4
C141 10U/10V_8
C131 .1U-16V_4
C140 10U-6.3V_8
LAN_REG1_2V
LAN REGCTL25
LAN REGCTL12
D8 BAS316
D9 BAS316
D7 BAS316
LAN_LINKLED#
LINKLED#
100#
1000#
Y1
25MHZ
C110 27P_4
C108 27P_4
CLK_LAN_X1
CLK_LAN_X2
C115 .1U-16V_4
C85 .1U-16V_4
C104 .1U-16V_4
C118 .1U-16V_4
C109 .1U-16V_4
C95 .1U-16V_4
C117 .1U-16V_4
C65 4.7U-10V_8
C116 .1U-16V_4
C106 .1U-16V_4
C111 .1U-16V_4
C101 .1U-16V_4
C113 4.7U-10V_8
C124 .1U-16V_4
C121 47U-6.3V_12
C66 .01U_4
C67 .01U_4
Close Transformer
BCM_SCL R85 *4.7K_4
SI R84 *4.7K_4
CS# R83 4.7K_4
LAN_REG1_2V R112 1.5_12 +3V_S5
R109 *1_12 VAUX_25
A1A: (9/1 BCM recommend)
in order to pull up C321/C51 and Q17 pin 3 to
3V_LAN rail.
PROJECT : ZD1
Quanta Computer Inc.
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BCM5787 LAN/TRANSFORMER
Rev
B
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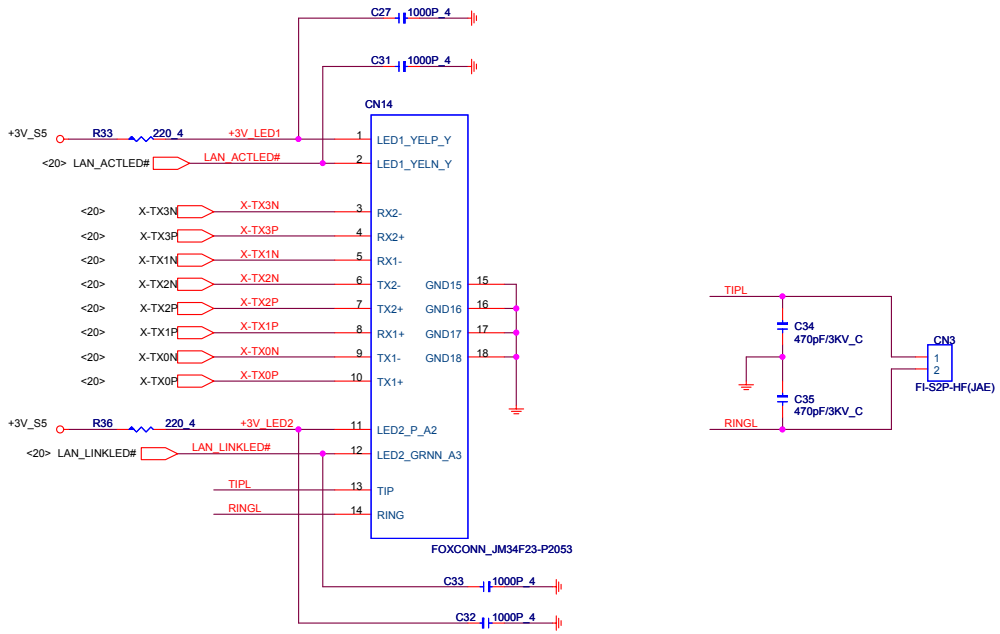
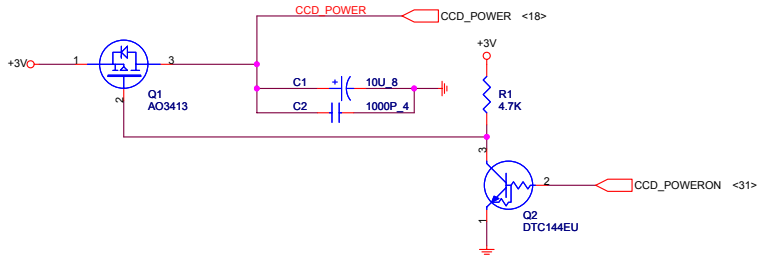
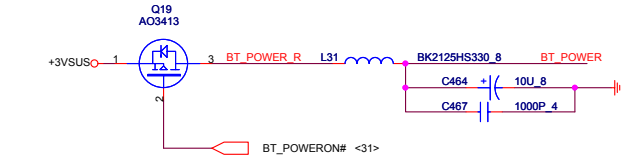
RJ45-11

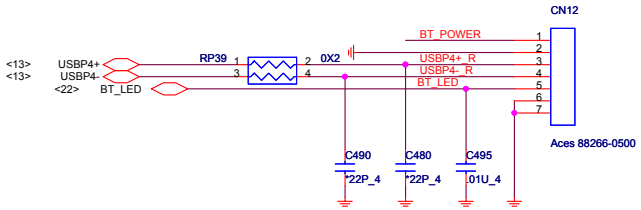


CAMERA MODULE CONNECTOR

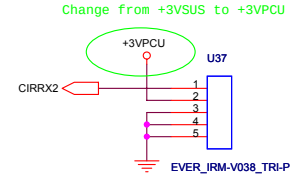


BLUETOOTH MODULE CONNECTOR

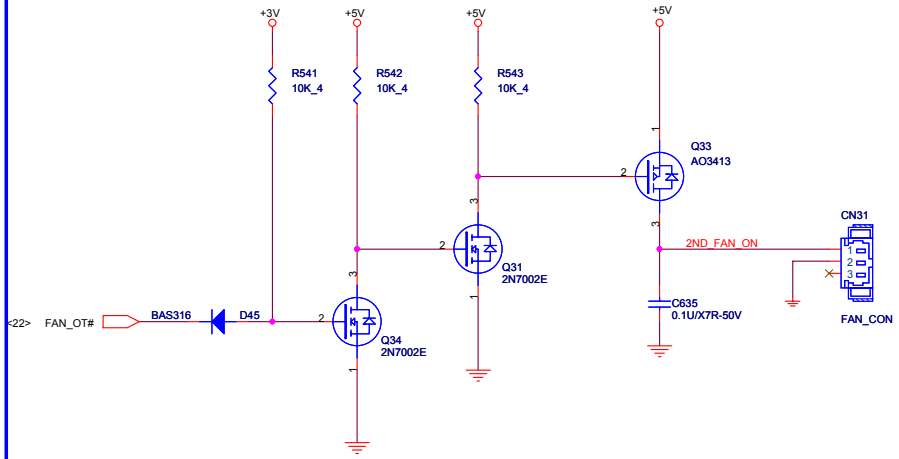




CIR



2nd FAN



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Quanta Computer Inc.		
Size	Document Number: BT/CCD/RJ45-11/CIR/2nd FAN	Rev: B
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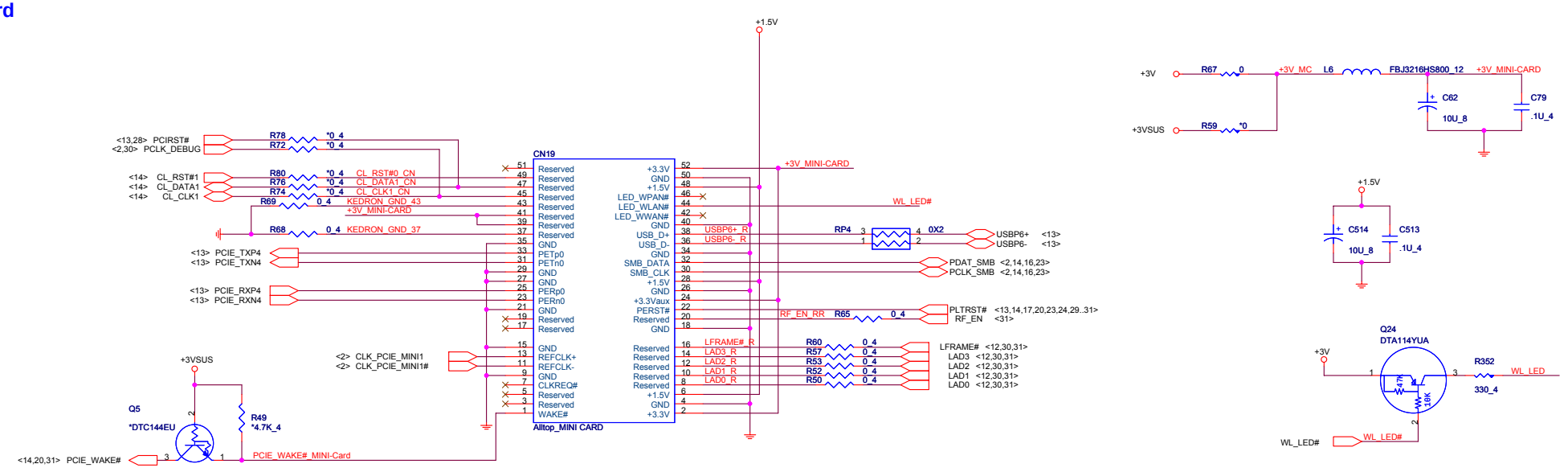
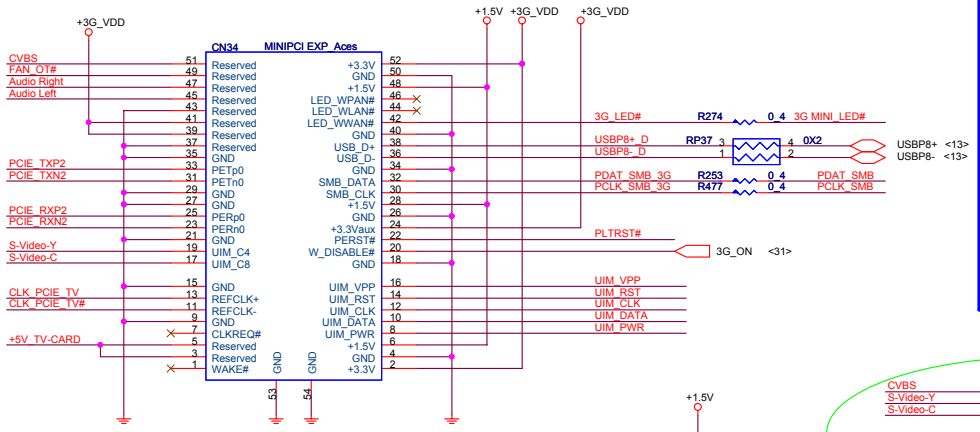
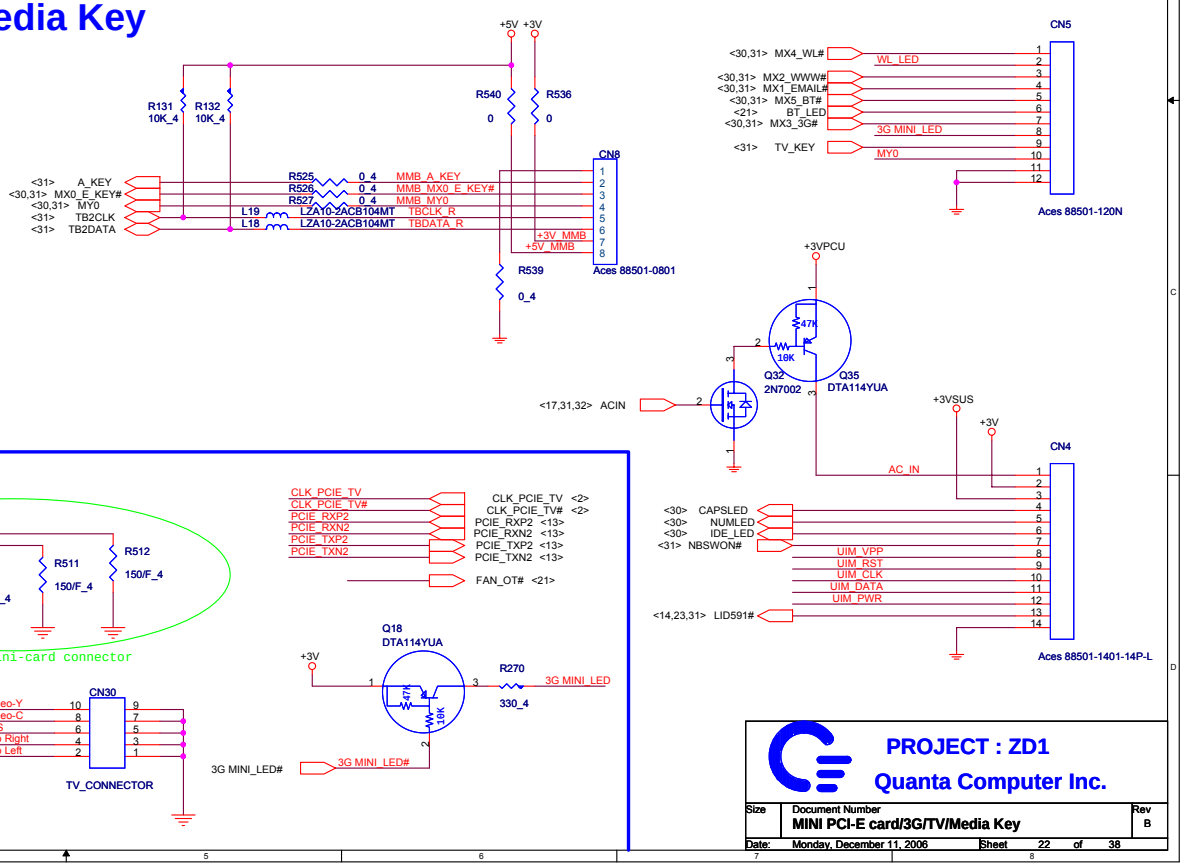
MINI-Card



3G/TV MINI CARD



Media Key



PROJECT : ZD1			
Quanta Computer Inc.			
Size	Document Number		Rev
	MINI PCI-E card/3G/TV/Media Key		B
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New card

CN9

<13> PCIE_TXP1
<13> PCIE_TXN1
<13> PCIE_RXP1
<13> PCIE_RXN1
<2> CLK_PCIE_NEW_C
<2> CLK_PCIE_NEW_C#
<13> NC_EN#
C381
C376
PERP3
PERN3
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
<13> USBP5+
<13> USBP5-
R441 0_4 USBP5+_R
R442 0_4 USBP5-_R

GND5 GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND6

*Aces_NEW CARD

CN44

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30

*Taitwun_NEW CARD

CN43

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30

FOX_EXPCARD

NEW CARD'S POWER SWITCH

U33
QFN-TPS2231RGP

+3V → 3.3VIN 3.3VIN
+3V_S5 → AUXIN
+1.5V → 1.5VIN 1.5VIN
PLTRST#_NEW → *SYSRST# *SHDN#
*RCLKEN NC GND GNDPAD

3.3VOUT 3.3VOUT → +NEW_3V 1.3A
AUXOUT → +NEW_3VAUX 275mA
1.5VOUT 1.5VOUT → +NEW_1.5V 650mA
*STBY# *CPPE# *CPUSB# → CPPE# CPUSB#
PERST# OC# → PERST#

REV:B MODIFY

TI : AL002231001
RICOH : AL005538001
GMT : AL000577008

<13,14,17,20,22,24,29..31> PLTRST#
Q37 2N7002
PLTRST#_NEW

REV:B MODIFY

+3V_S5: C599 .1U_4
+3V: C581 .1U_4, C582 .1U_4
+1.5V: C598 .1U_4, C597 .1U_4
+NEW_3VAUX: C351 .1U_4
+NEW_3V: C579 4.7U_8, C354 .1U_4, C357 .1U_4
+NEW_1.5V: C348 4.7U_8, C344 .1U_4

+NEW_3V
Q30 2N7002E
RP41 10KX2_4
<2,14,16,22> PDAT_SMB
NEW_SMDATA

+NEW_3V
Q29 2N7002E
<2,14,16,22> PCLK_SMB
NEW_SMCLK

LID SWITCH

+3V
R194 10K_4
<18> DISPON
DISPON D11 BAS316 LID591# <14,22,31>
D10 BAS316 R190 IV@0_4 INT_LVDS_BLON <6>
R189 EV@0_4 EV_LVDS_BLON <17>
R192 *1K_4
R191 100K_4

<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
(Need confirm with Max)

Q12 DTC144EU
EC_FPBACK# <31>

HDMI

+5V
D35 BAS316 D34 BAS316
R354 2K_4 R353 2K_4
<17> MXM_HDMI_DDCCLK → L39 220R@100MHZ → HDMI_DDCCLK
C515 *.1U_4
<17> MXM_HDMI_DDCDATA → L38 220R@100MHZ → HDMI_DDCDATA
C516 *.1U_4

NV suggestion near HDMI connector

+5V
C632 .1u_4 C631 .1u_4 C633 .1u_4

CN21
HDMI CON

<17> HDMITX2P HDMITX2N HDMITX1P HDMITX1N HDMITX0P HDMITX0N HDMICLK+ HDMICLK-
HDMI_DDCCLK HDMI_DDCDATA
<17> HDMI_HP_A → R359 EV@10K_4 HP_DET
R356 EV@10K_4

HDMI monitor default have PU to 5V.So ZY3 PD for level change.And serial R for current limited

U27 *RClamp0514M_AG
HDMITX2P HDMITX2N HDMITX1P HDMITX1N

U25 *RClamp0514M_AG
HDMICLK+ HDMICLK- HDMI_DDCDATA HDMI_DDCCLK

U26 *RClamp0514M_AG
HDMITX0P HDMITX0N HDMI_HP_A

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Quanta Computer Inc.

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	NEW CARD/HDMI/LID	B
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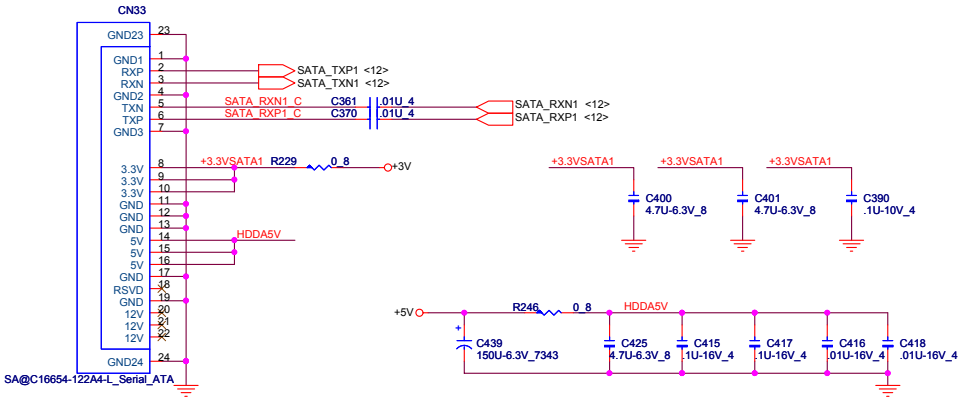
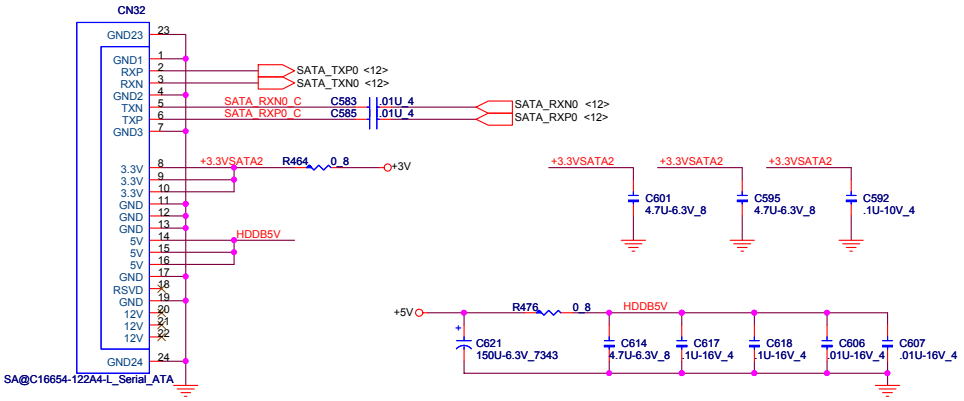
SATA HDD1

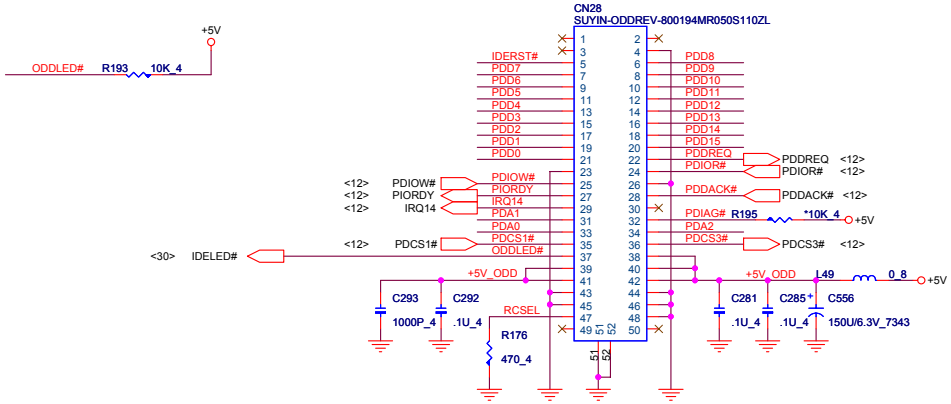


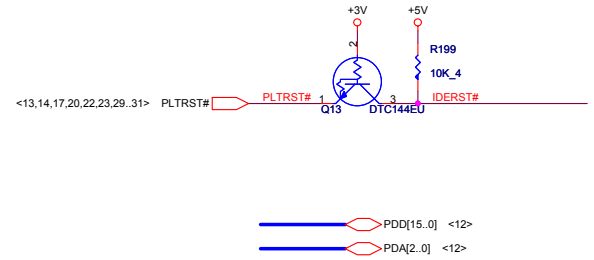
SATA HDD2

Main



ODD (PATA)





<OrgName>

PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	SATA-HDD & PATA-ODD	B

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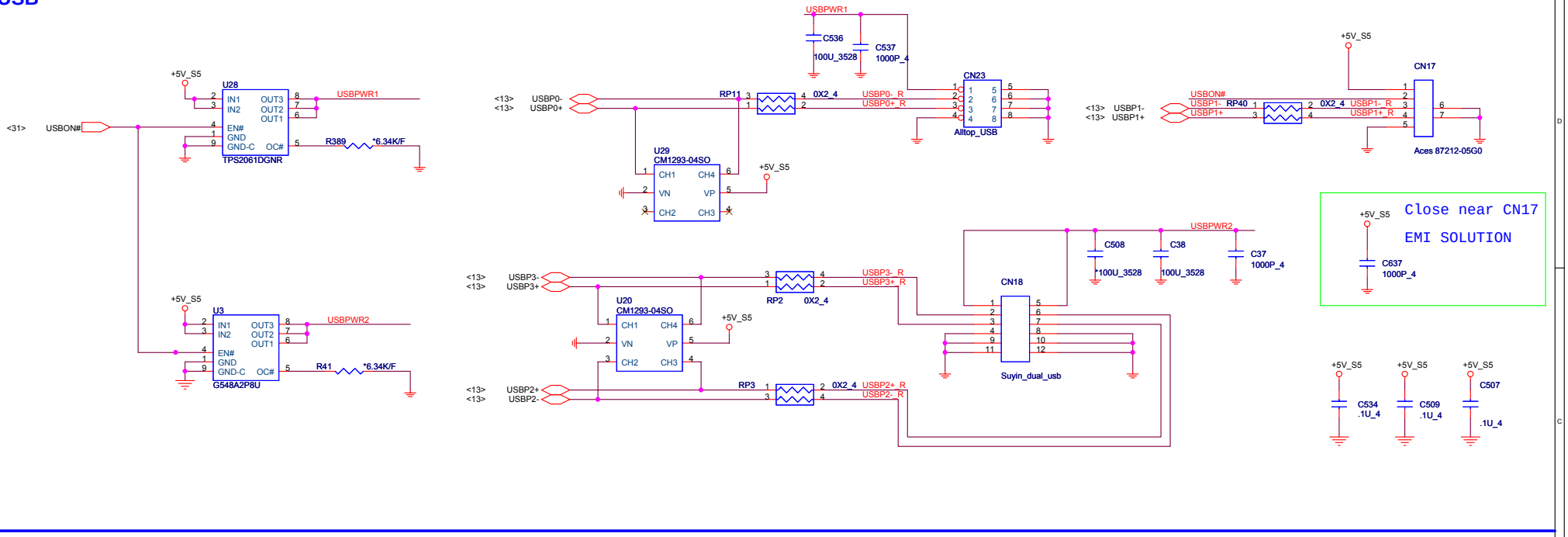
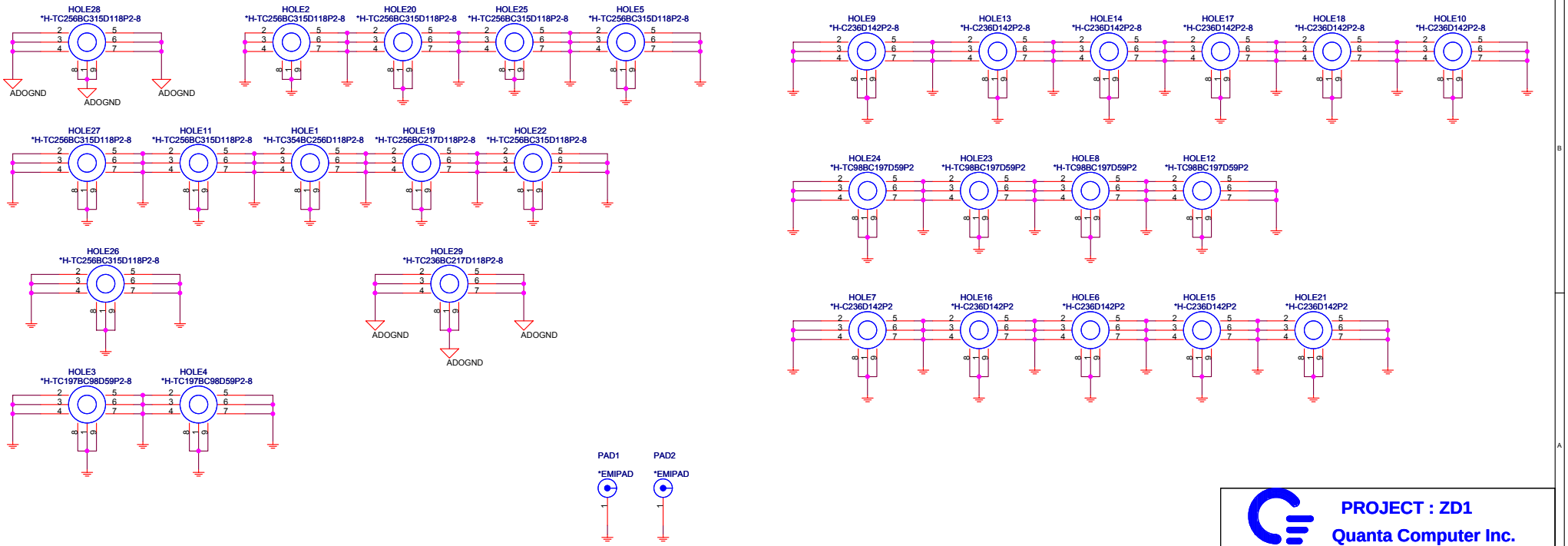
USB



HOLES



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Quanta Computer Inc.

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	USB/HOLE	B
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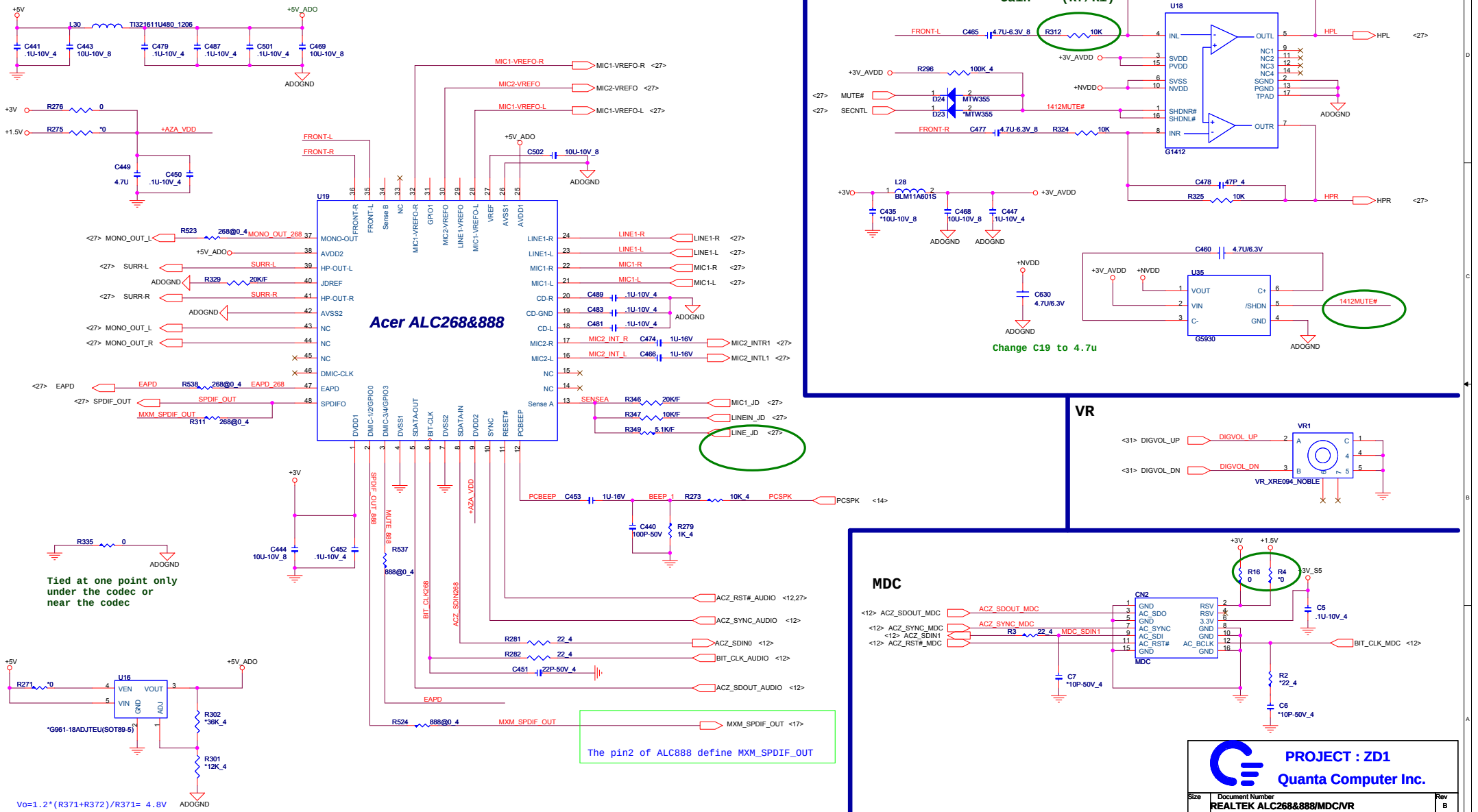
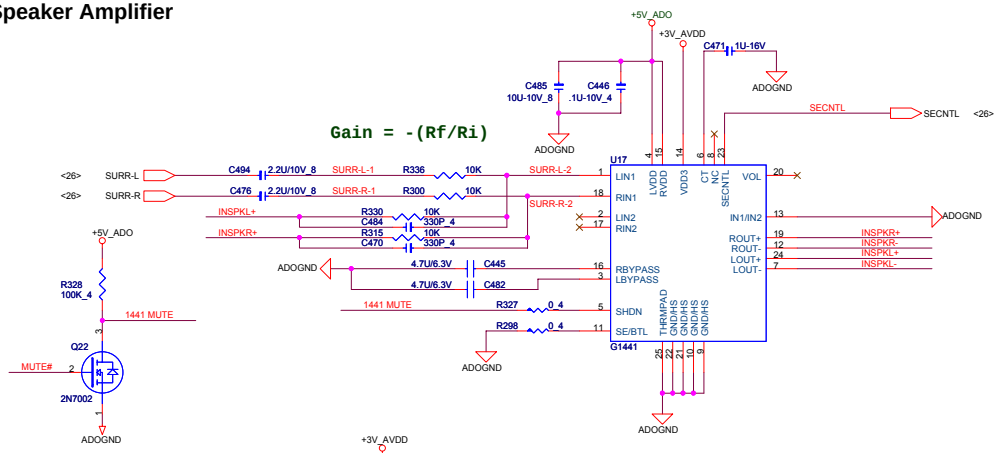
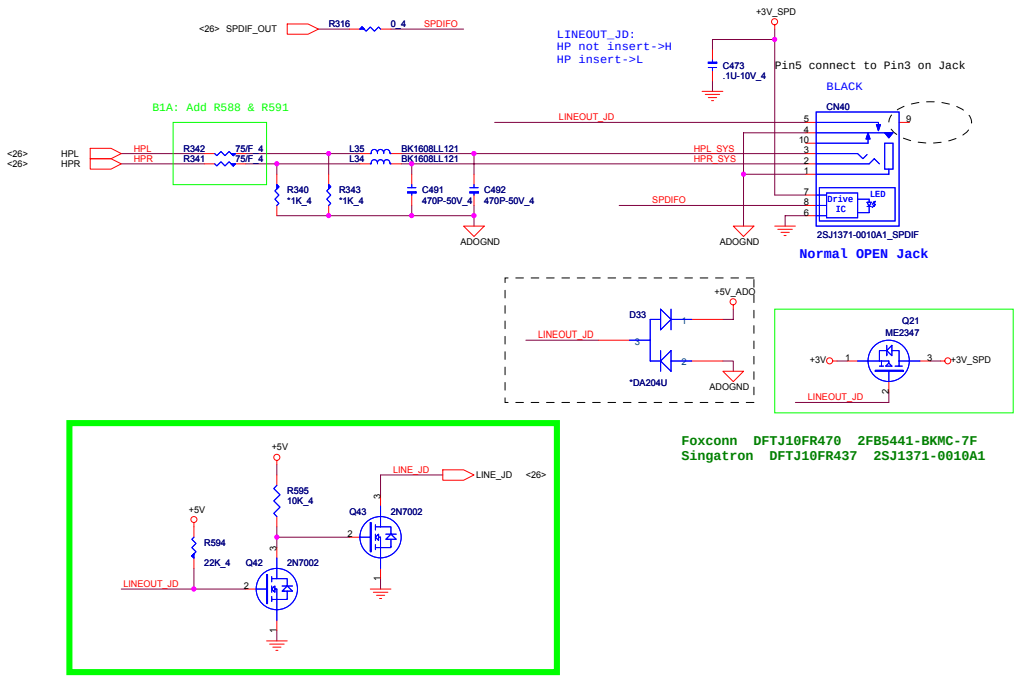
CODEC(ALC268)



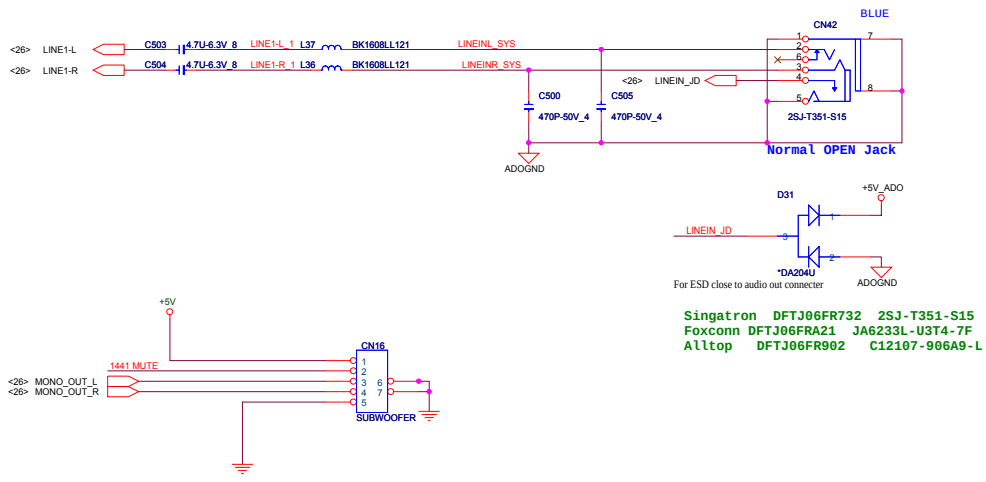
Speaker Amplifier



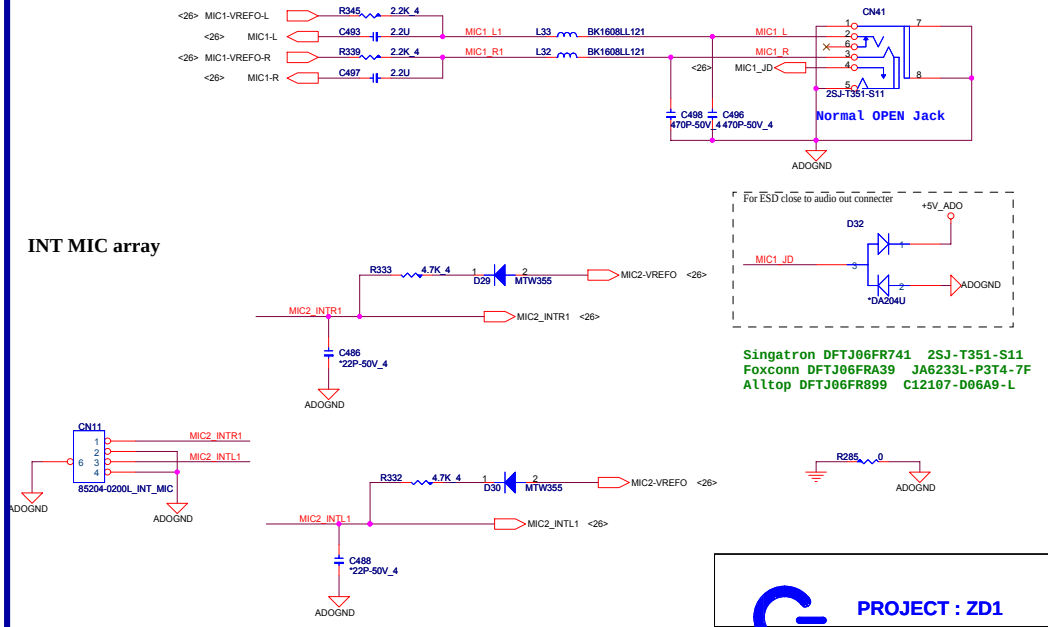
SYSTEM LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER



MIC



PROJECT : ZD1

Quanta Computer Inc.

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	AMP_AUDIO JACK CONN	B
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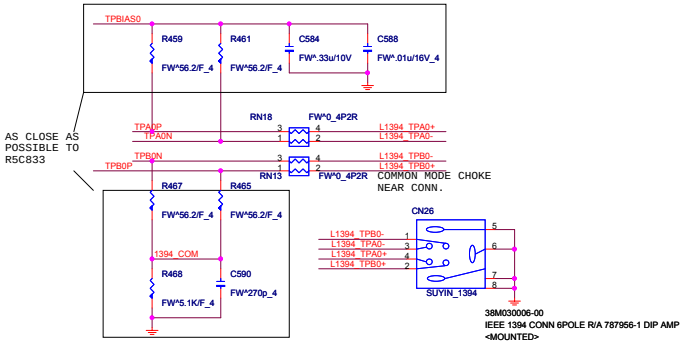
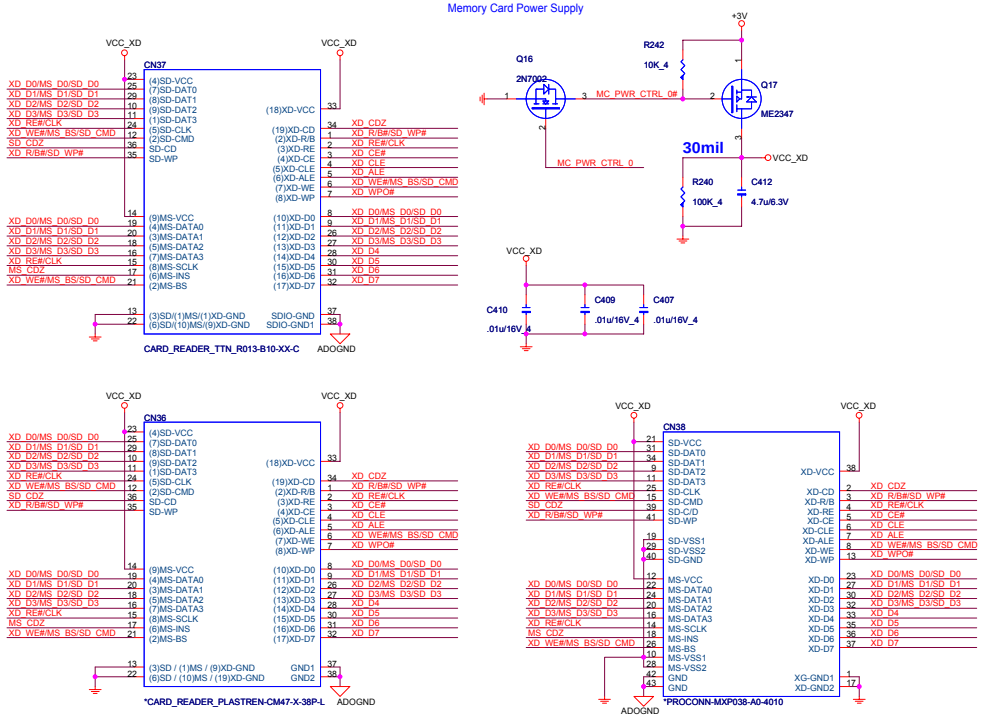
R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

1394



5 IN 1 CARD READER



PowerOnReset for VccCore

When GRESET# is controlled by system, the pull-up resistor(R762) and capacitor(C492) do not need to apply.

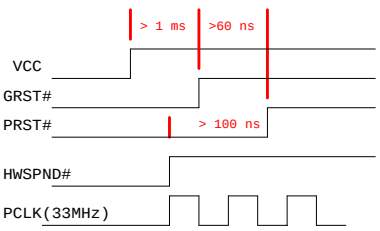
When HWSPND# is controlled by system, the pull-up resistor(R755) dose not need to apply.

* NOT Use EEPROM : PU
* Use EEPROM : PD

Ground guard

GUARD GND

* NOT Use EEPROM : R759 : installed R760,U43,C505 : NOT installed
* Use EEPROM : R760,U43,C505 : installed R759 : NOT installed



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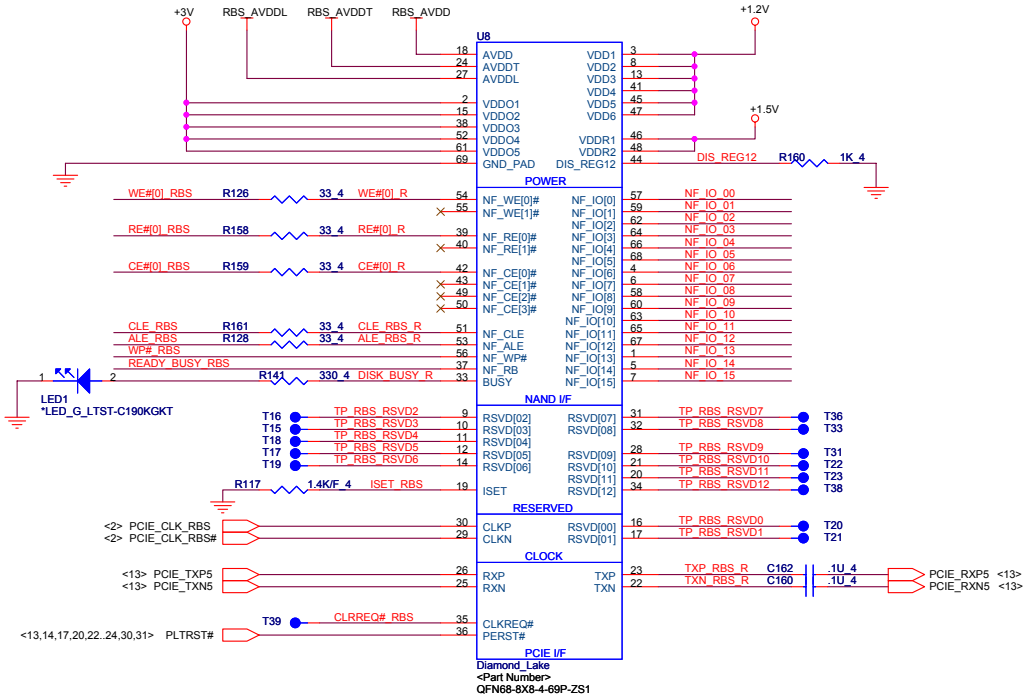
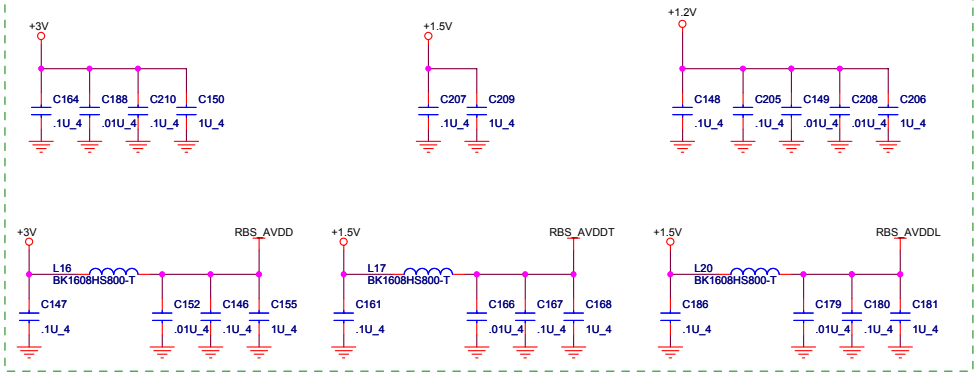
Quanta Computer Inc.

ROBSON

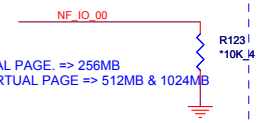
DIAMOND-LAKE ASIC



PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

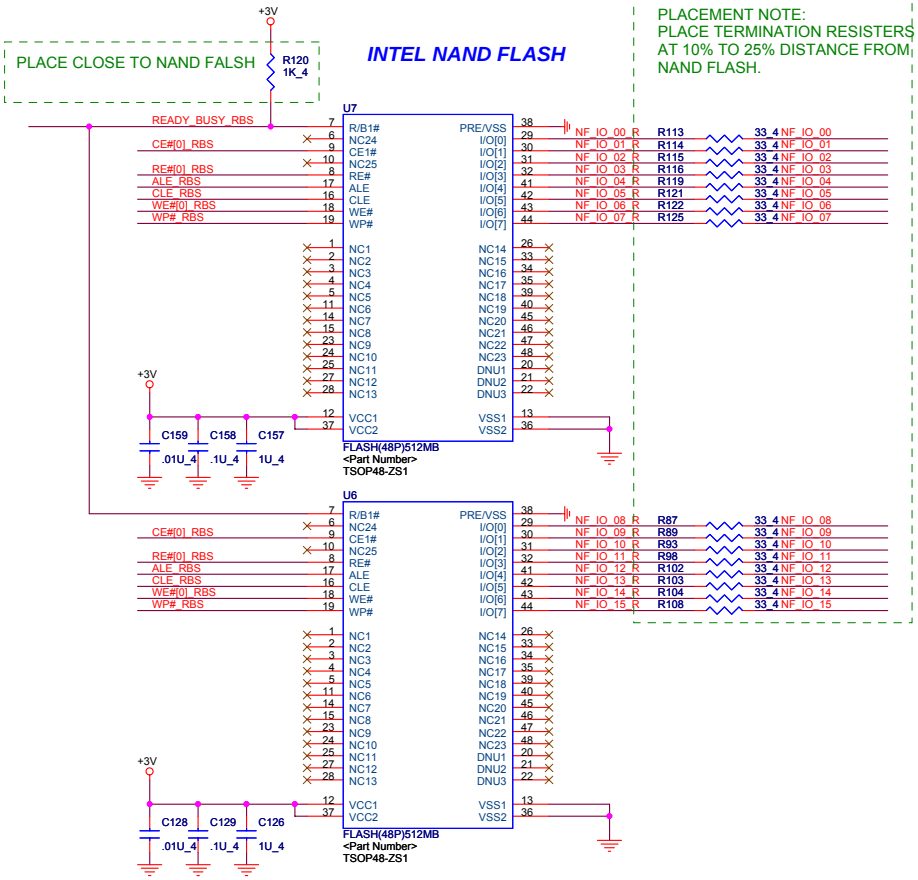


STUFF: INDICATES A 2KB VIRTUAL PAGE. => 256MB
DESTUFF: INDIACTESS A 4KB VIRTUAL PAGE => 512MB & 1024MB



PLACE CLOSE TO NAND FALSH

INTEL NAND FLASH



PLACEMENT NOTE:
PLACE TERMINATION RESISTERS AT 10% TO 25% DISTANCE FROM NAND FLASH.

LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

PROJECT : ZD1

Quanta Computer Inc.

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	ROBSON	B
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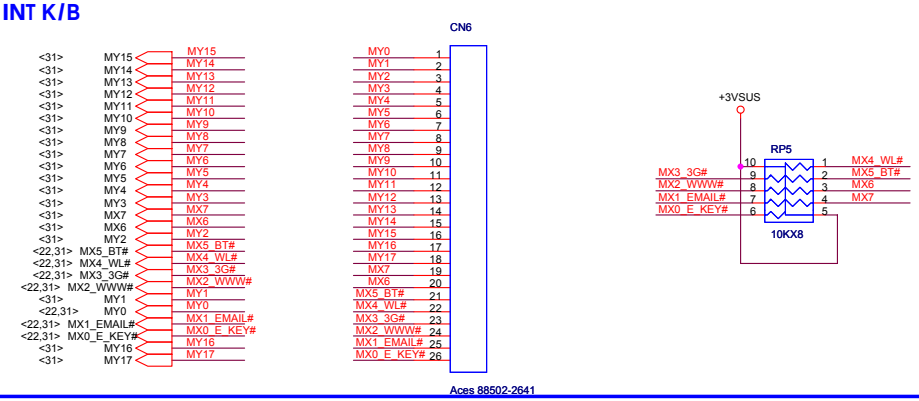
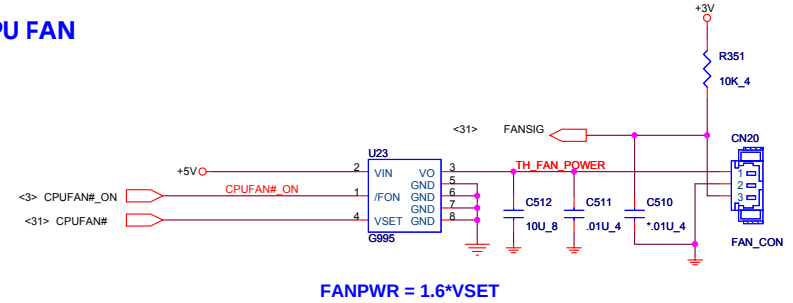
INT K/B

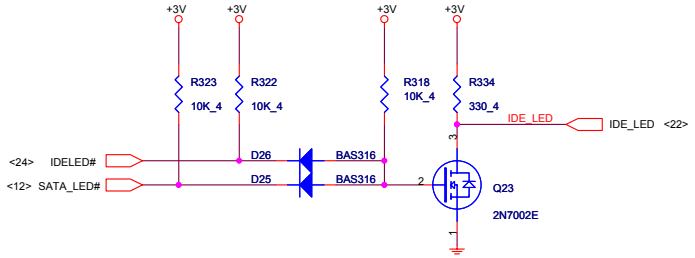


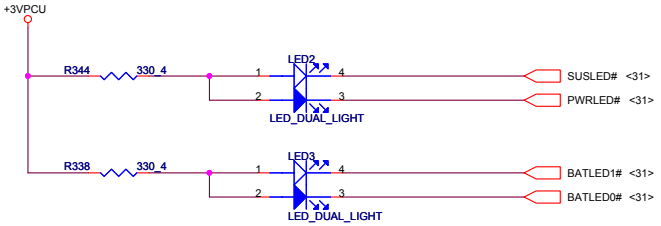
CPU FAN

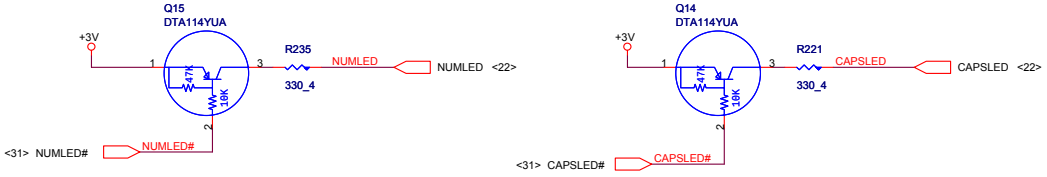


FANPWR = 1.6*VSET

LED

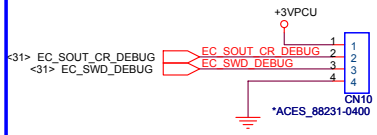




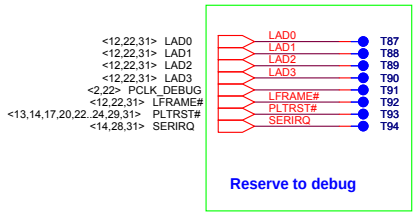


DEBUG PORT

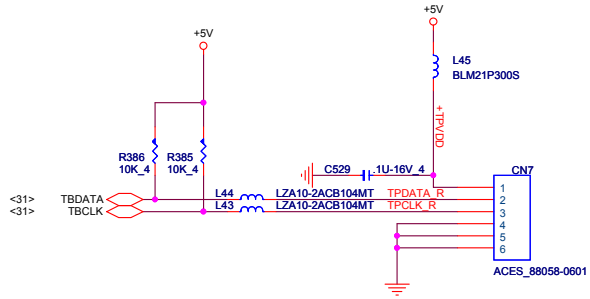
EC Debug Port



Reserved for LPC debug card



T/P



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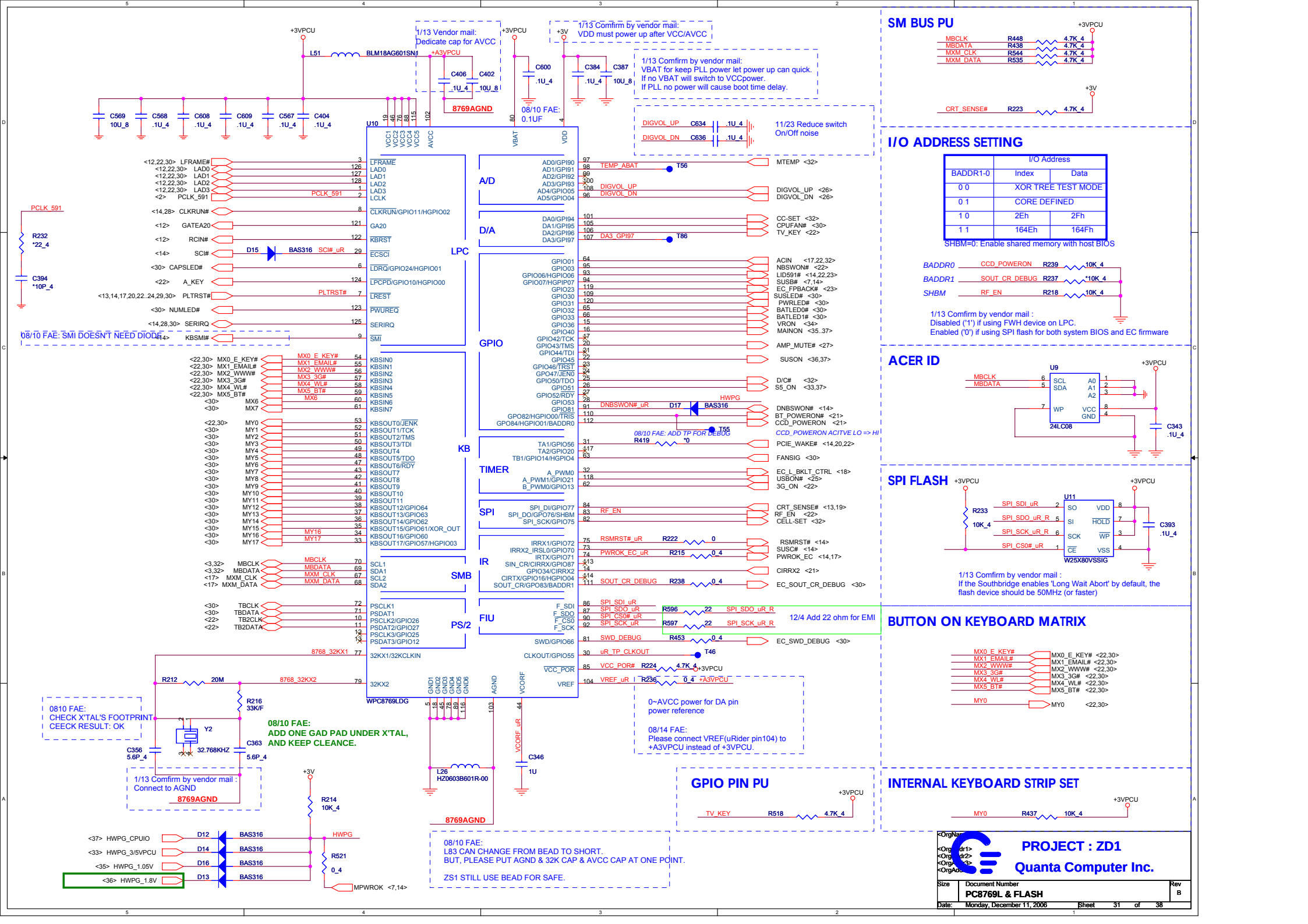
PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	FAN,LED,KB,DEBUG PORT,TP	B
Date: Monday, December 11, 2006	Sheet 30 of 38	


SM BUS PU
MBCLK R448 4.7K_4
MBDATA R438 4.7K_4
MXM_CLK R544 4.7K_4
MXM_DATA R535 4.7K_4
CRT_SENSE# R223 4.7K_4
I/O ADDRESS SETTING
I/O Address
BADDR1-0 | Index | Data
0 0 XOR TREE TEST MODE
0 1 CORE DEFINED
1 0 2Eh 2Fh
1 1 164Eh 164Fh
SHBM=0: Enable shared memory with host BIOS
BADDR0 CCD_POWERON R239 10K_4
BADDR1 SOUT_CR_DEBUG R237 *10K_4
SHBM RF_EN R218 10K_4
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ACER ID
U9
24LC08
SPI FLASH
U11
W25X80VSSIG
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)
BUTTON ON KEYBOARD MATRIX
INTERNAL KEYBOARD STRIP SET
GPIO PIN PU
1/13 Vendor mail:
Dedicate cap for AVCC
1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
11/23 Reduce switch On/Off noise
08/10 FAE: 0.1UF
08/10 FAE: SMI DOESN'T NEED DIODE
08/10 FAE: ADD TP FOR DEBUG
CCD_POWERON ACITVE LO => HI
12/4 Add 22 ohm for EMI
0~AVCC power for DA pin power reference
08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.
0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK
08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
U10
WPC8769LDG
LPC
A/D
D/A
GPIO
KB
TIMER
SPI
IR
SMB
PS/2
FIU
PROJECT : ZD1
Quanta Computer Inc.
PC8769L & FLASH
Monday, December 11, 2006
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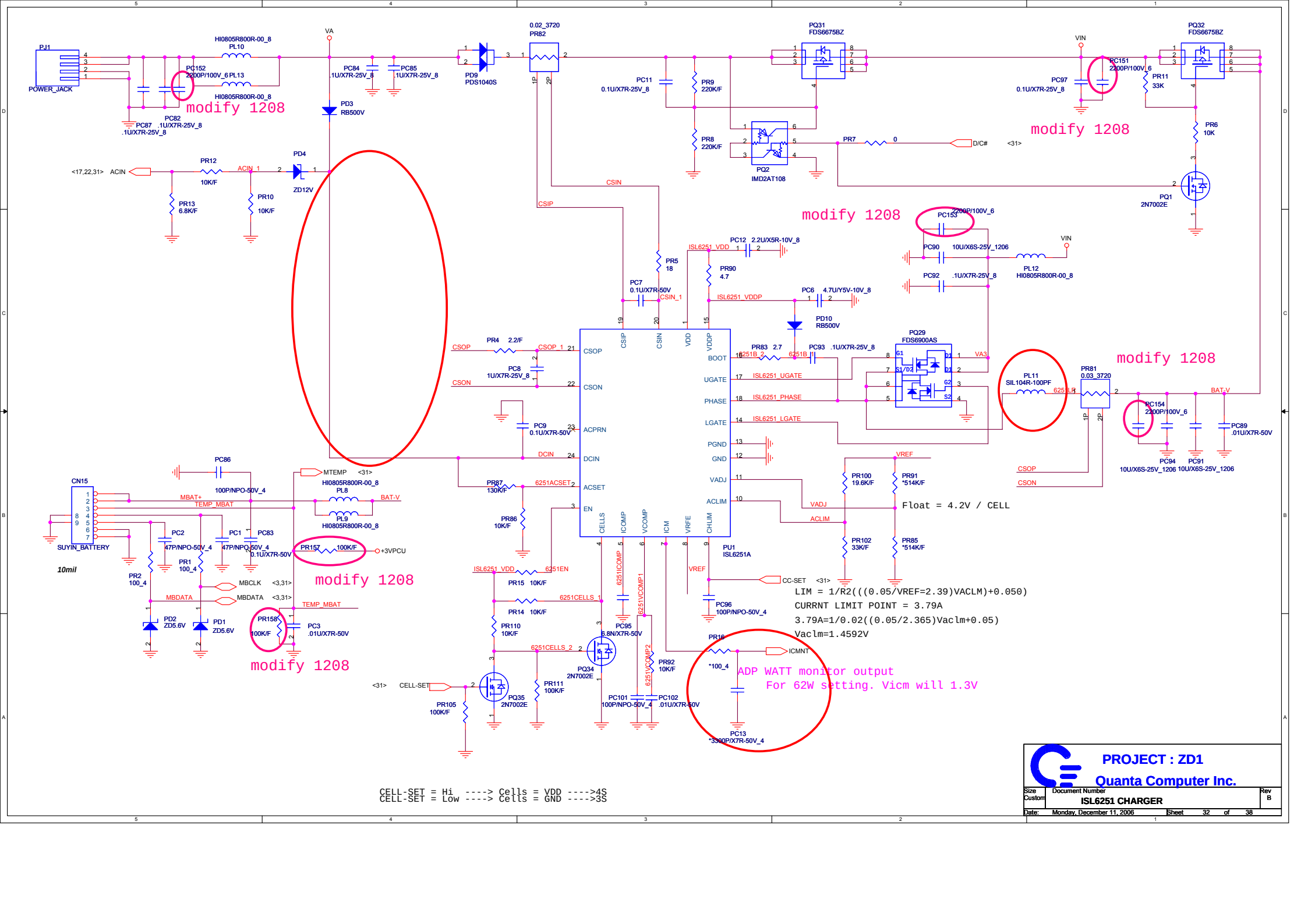
modify 1208
modify 1208
modify 1208
modify 1208
modify 1208
Float = 4.2V / CELL
LIM = 1/R2(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT = 3.79A
3.79A=1/0.02((0.05/2.365)Vaclm+0.05)
Vaclm=1.4592V
ADP WATT monitor output
For 62W setting. Vicm will 1.3V
CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S
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Quanta Computer Inc.
ISL6251 CHARGER
Monday, December 11, 2006
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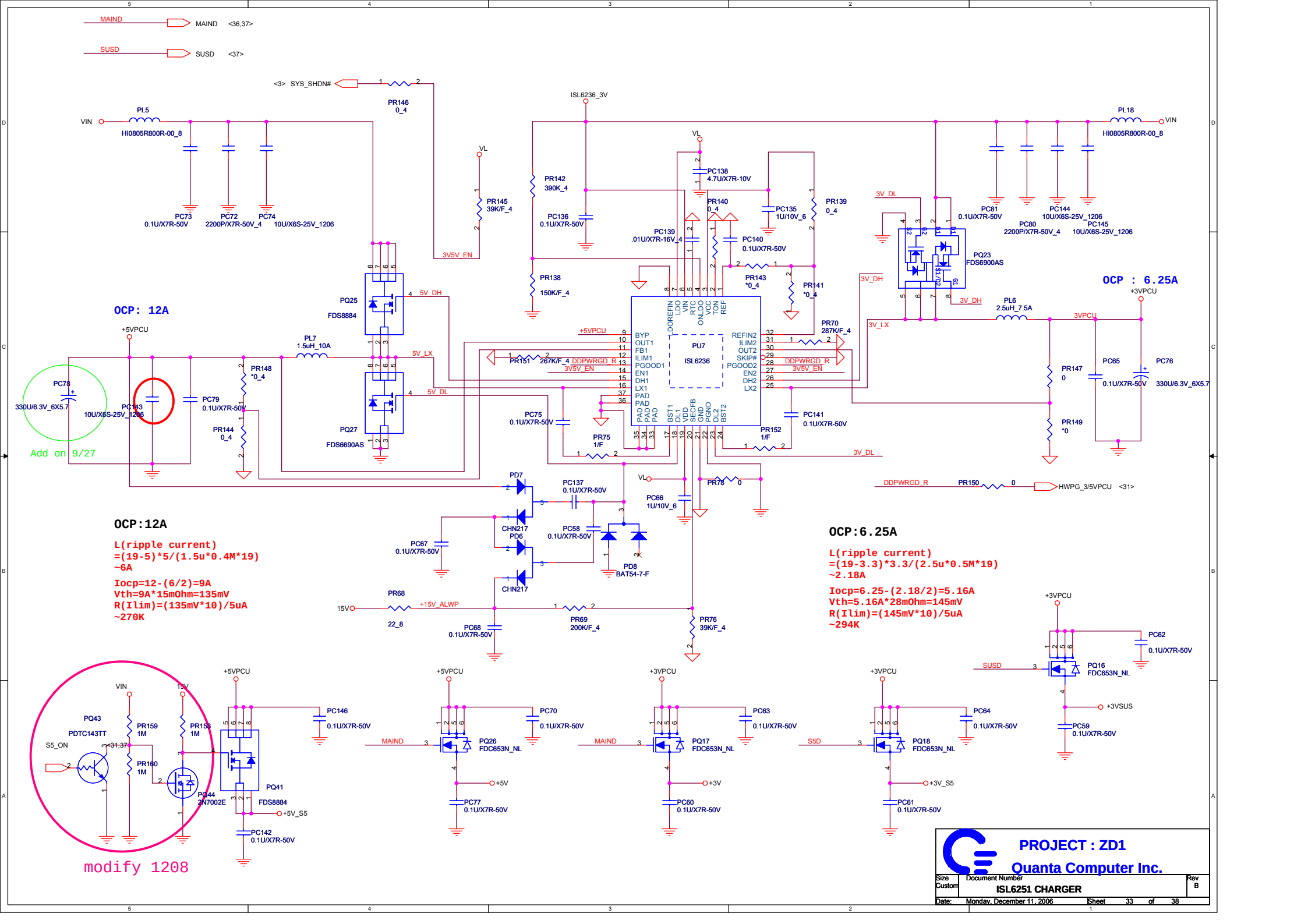
MAIND
MAIND <36,37>
SUSD
SUSD <37>
<3> SYS_SHDN#
PR146 0_4
ISL6236_3V
VIN
PL5
HI0805R800R-00_8
PC73 0.1U/X7R-50V
PC72 2200P/X7R-50V_4
PC74 10U/X6S-25V_1206
VL
PR145 39K/F_4
3V5V_EN
PR142 390K_4
PC136 0.1U/X7R-50V
PR138 150K/F_4
PC138 4.7U/X7R-10V
PR140 0_4
PC135 1U/10V_6
PR139 0_4
PC139 .01U/X7R-16V_4
PC140 0.1U/X7R-50V
PR143 *0_4
PR141 *0_4
PL18
HI0805R800R-00_8
PC81 0.1U/X7R-50V
PC80 2200P/X7R-50V_4
PC144 10U/X6S-25V_1206
PC145 10U/X6S-25V_1206
3V_DL
PQ23 FDS6900AS
3V_DH
3V_LX
PL6 2.5uH_7.5A
3VPCU
+3VPCU
OCP : 6.25A
OCP: 12A
+5VPCU
PL7 1.5uH_10A
PQ25 FDS8884
5V_DH
5V_LX
5V_DL
PQ27 FDS6690AS
PR148 *0_4
PR144 0_4
PC78 330U/6.3V_6X5.7
PC143 10U/X6S-25V_1206
PC79 0.1U/X7R-50V
Add on 9/27
PU7 ISL6236
DDREFIN LDO VIN RTO ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 VDD SFB SGND PGND DL2 BST2
PR70 287K/F_4
PR151 267K/F_4
DDPWRGD_R
PC75 0.1U/X7R-50V
PR75 1/F
PC141 0.1U/X7R-50V
PR152 1/F
PR147 0
PR149 *0
PC65 0.1U/X7R-50V
PC76 330U/6.3V_6X5.7
PR150 0
HWPG_3/5VPCU <31>
PD7
PC137 0.1U/X7R-50V
PC66 1U/10V_6
PR78 0
CHN217
PD6
PC58 0.1U/X7R-50V
PD8 BAT54-7-F
PC67 0.1U/X7R-50V
15V
PR68 22_8
+15V_ALWP
PC68 0.1U/X7R-50V
PR69 200K/F_4
PR76 39K/F_4
OCP:12A
L(ripple current)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp=12-(6/2)=9A
Vth=9A*15mOhm=135mV
R(Ilim)=(135mV*10)/5uA
~270K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
PQ43 PDTC143TT
S5_ON
PR159 1M
PR160 1M
PR158 1M
PQ44 2N7002E
PQ41 FDS8884
+5V_S5
PC142 0.1U/X7R-50V
PC146 0.1U/X7R-50V
PQ26 FDC653N_NL
PC70 0.1U/X7R-50V
+5V
PC77 0.1U/X7R-50V
PQ17 FDC653N_NL
PC63 0.1U/X7R-50V
+3V
PC60 0.1U/X7R-50V
PQ18 FDC653N_NL
PC64 0.1U/X7R-50V
+3V_S5
PC61 0.1U/X7R-50V
PQ16 FDC653N_NL
PC62 0.1U/X7R-50V
+3VSUS
PC59 0.1U/X7R-50V
modify 1208
PROJECT : ZD1
Quanta Computer Inc.
Size Custom
Document Number
ISL6251 CHARGER
Rev B
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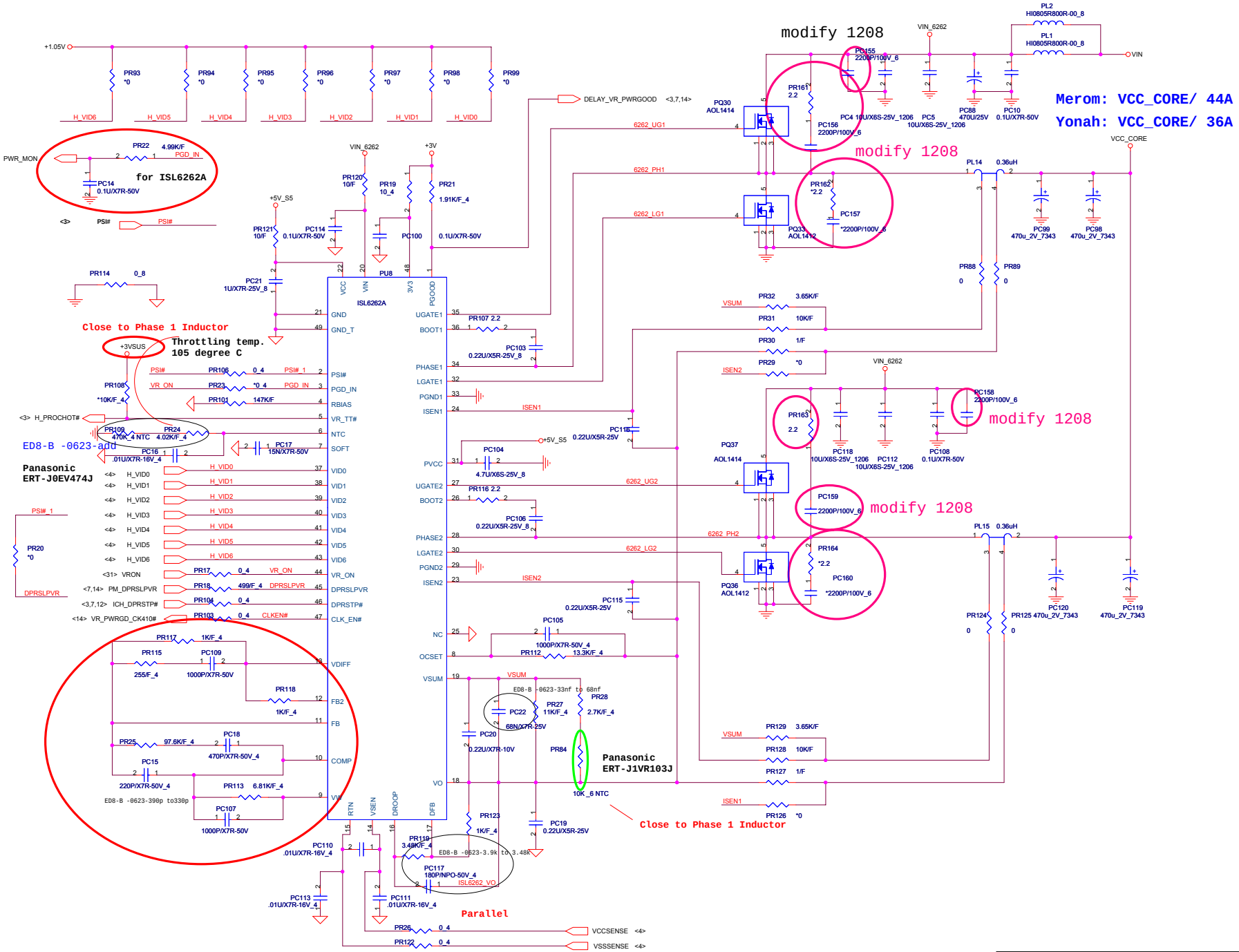
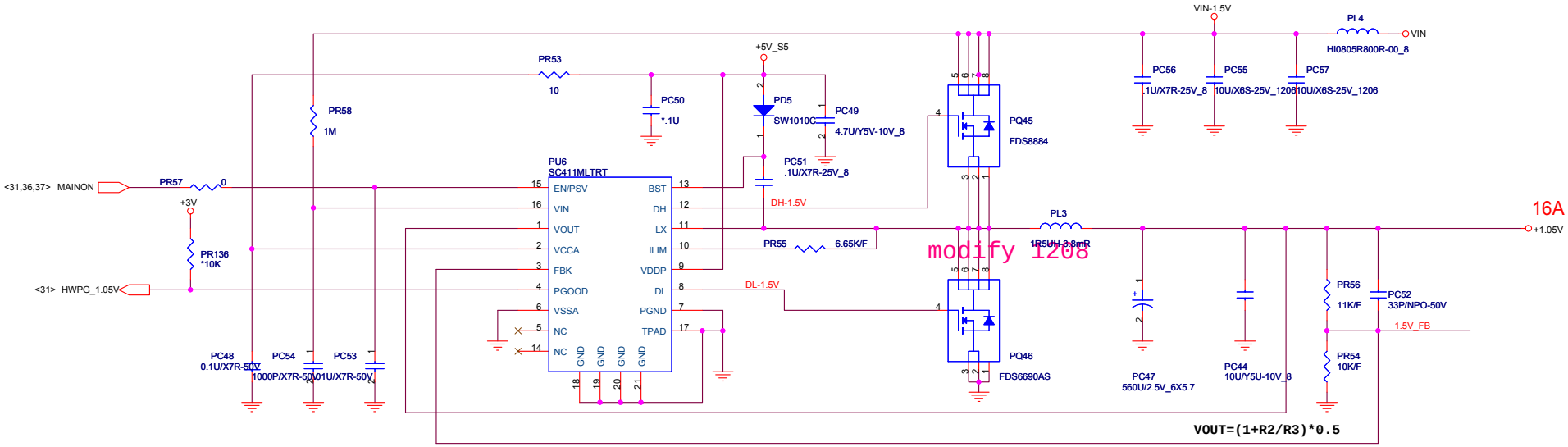

modify 1208
Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
ED8-B -0623-add
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Parallel
Close to Phase 1 Inductor
ISL6262A
PROJECT : ZD1
Quanta Computer Inc.
CPU CORE(ISL6262)
Monday, December 11, 2006



PROJECT : ZD1		
Quanta Computer Inc.		
Size	Document Number: +1.5V / +2.5V	Rev: B
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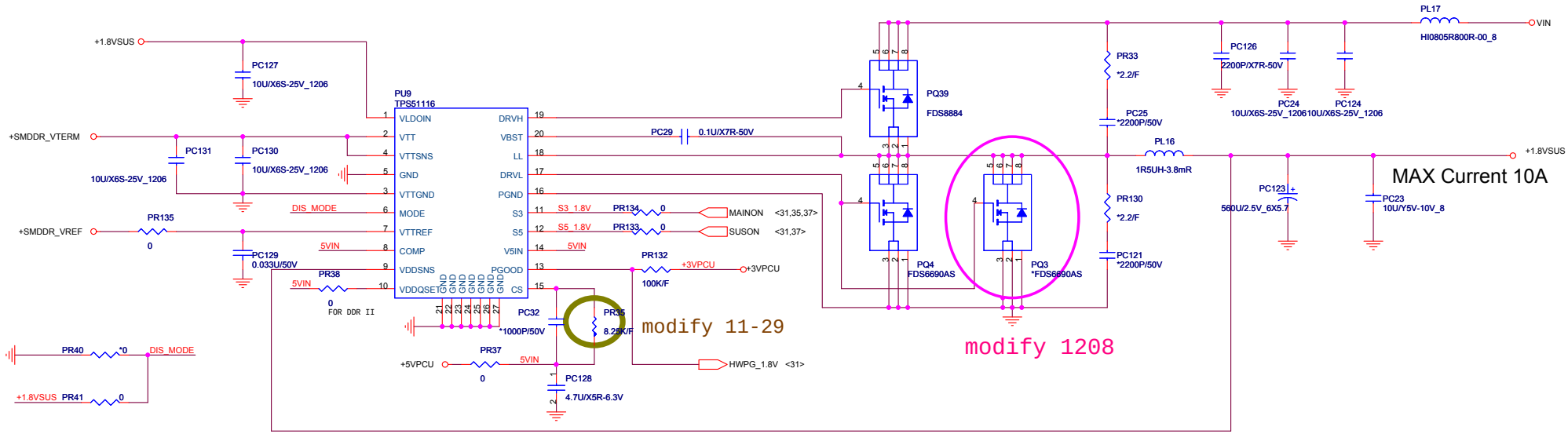
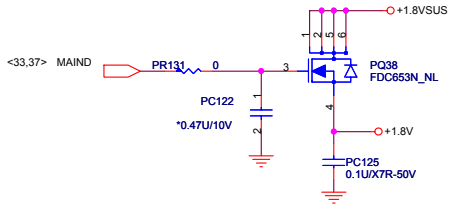


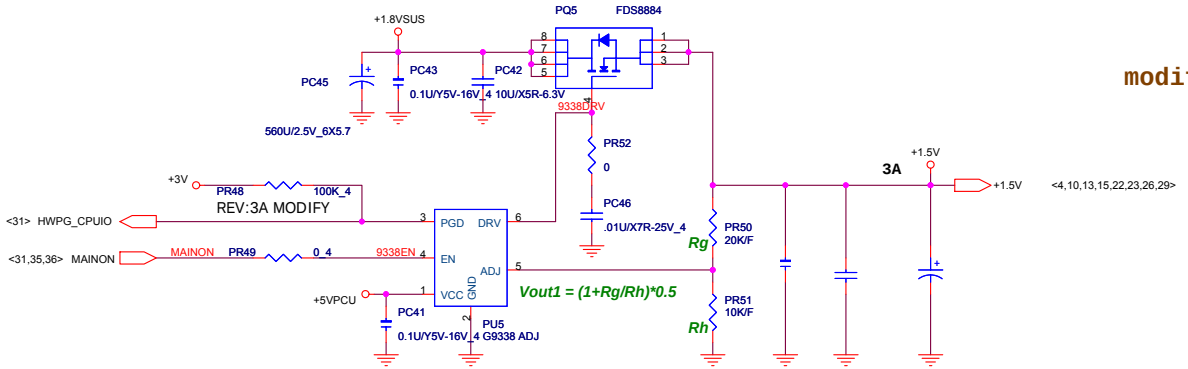


MAX Current 3.5A

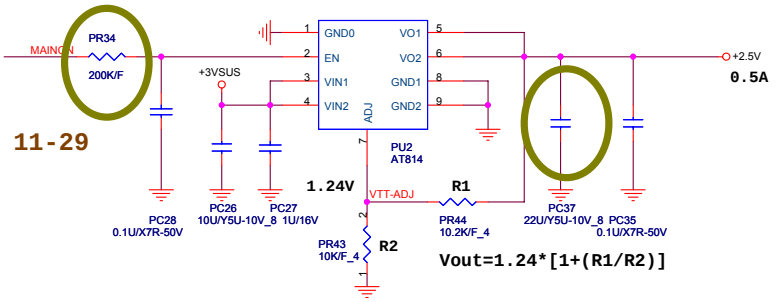
PROJECT : ZD1

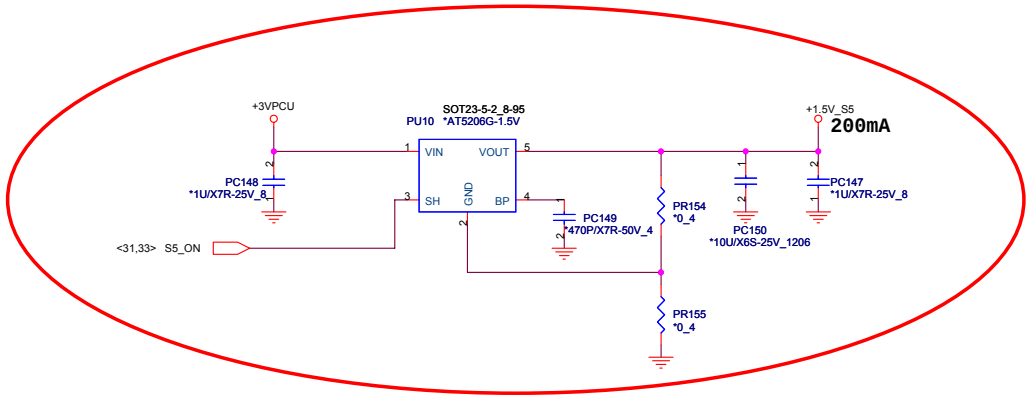
Quanta Computer Inc.

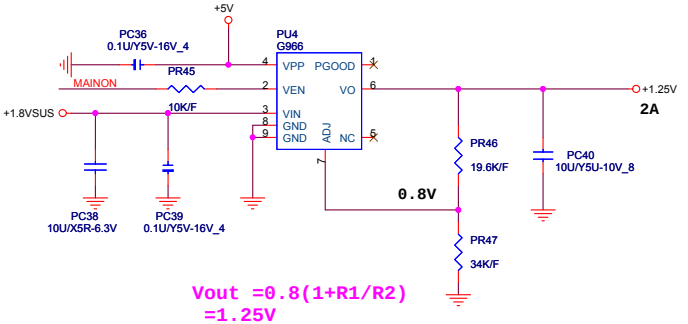
Size	Document Number	Rev
	DDR 1.8V(TPS51116)	B
Date: Monday, December 11, 2006	Sheet 36 of 38	

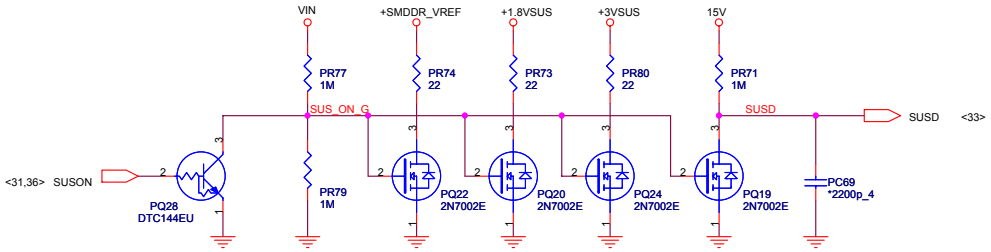


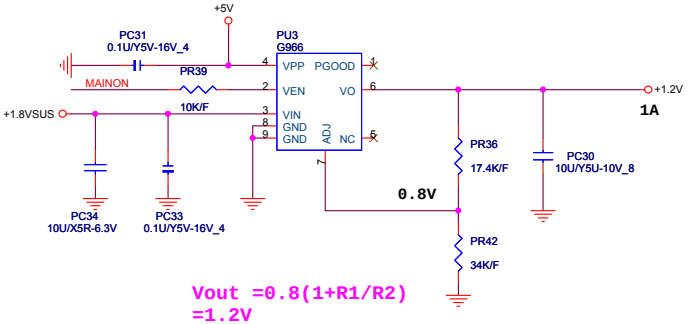
modify 11-29



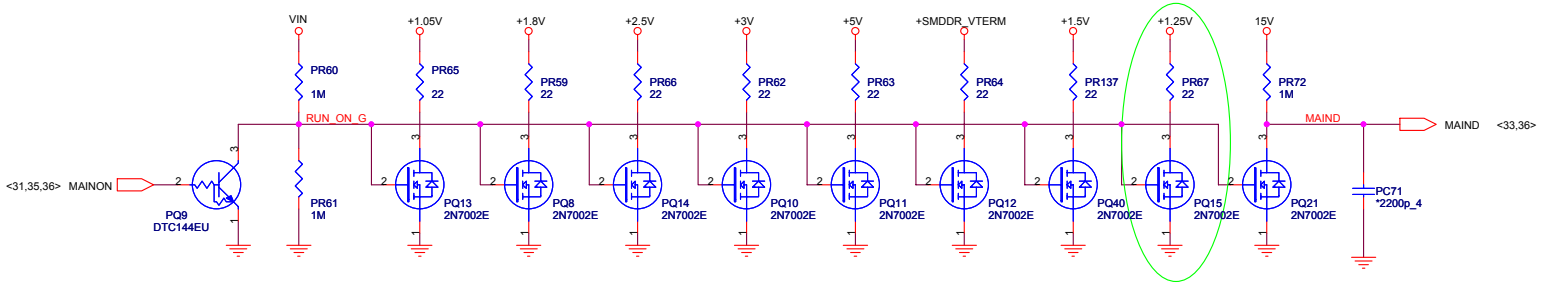








Add by power on 10/19



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	B
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Change list

Item	Fixed Issue	Reason for change	Schematic Rev.	PG#	Modify List
1	R5C833 SD CARD FAIL	SD CARD NO FUNCTION	B	28	SD card can not be detected , U32(ES2) sample will fix this issue.
2	R5C833 MMC CARD FAIL	MMC CARD NO FUNCTION	B	28	MMC card can not be detected , U32(ES2) sample will fix this issue.
3	TV CARD NO FUNCTION	Add +1.5V,Liteon without +1.5V; Avermedia need +1.5V	B	22	CN34.6 & .28 & .48 connect +1.5V
4	CAN'T BRING UP	power sequence fail	B	14	The CLPWROK pin of ICH8 connect with HWPG signal
5	VOLUME CONTROL ISSUE	VR switch have On/Off noise	B	31	add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins
6	T/P NO FUNCTION	the pin definiton is wrong	B	22	change CN7 pin definition.
7	MMB NO FUNCTION	the pin definiton is wrong	B	22	change CN8 pin definition.
8	NONE	Modem have different interface which is +3V and +1.5V	B	15	reserve +3V and +3V_S5
9	NONE	INTEL request to add for AMT function	B	14	GPIO10: Reserve PU, 10K => It is GPO and OD GPIO14: Reserve PD, 10K => It is GPI as AC present and active high
10	ICH8 ELECTRIC LEAKAGE ISSUE	INTEL request to add for AMT function , ICH8 have electric leadage from EC	B	14	The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5
11					
12					
13					
14					
15					
16					
17					
18					
19					
20					

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Quanta Computer Inc.

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	CHANGE LIST	B
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