Compal Confidential

NEW71/91 M/B Schematics Document

Intel Arrandale Processor with DDRIII + Ibex Peak-M
NV N11P-GV2H

2009-12-23

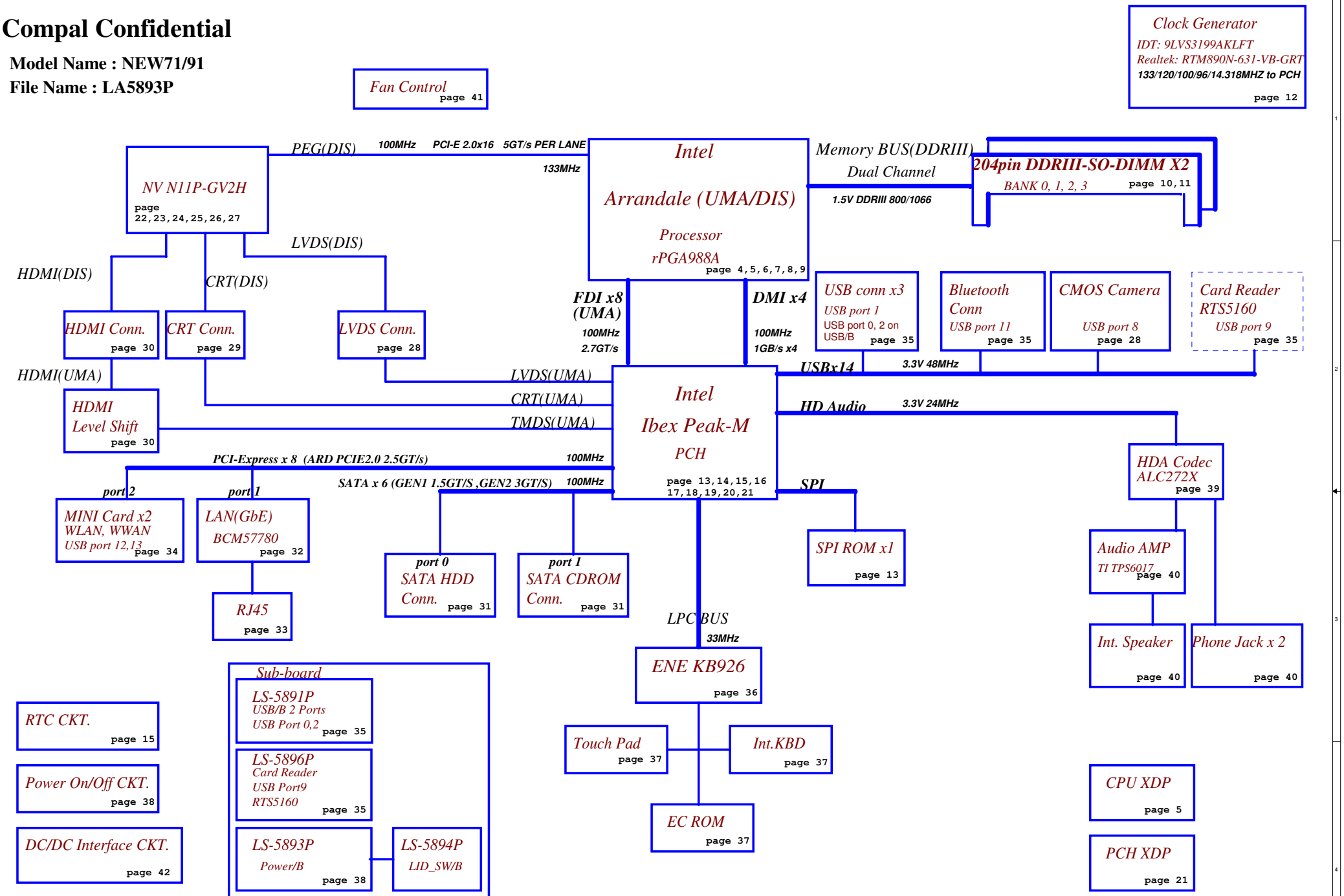
REV:0.1

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.		
Title: Cover Page		
Size: Custom	Document Number: NEW71/91 M/B LA-5893P Schematic	Rev: 0.1
Date: Wednesday, December 23, 2009	Sheet 1 of 56	

Compal Confidential

Model Name : NEW71/91
File Name : LA5893P



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.			
Title: Block Diagrams			
Size: B	Document Number: NEW71/91 M/B LA-5893P Schematic		Rev: 0.1
Date: Friday, December 18, 2009	Sheet 2 of 56		

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for Arrandale GPU (only for arrandaleCPU)	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.0VSDGPU	+1.0VSPDGPU to +1.0VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.05VS_VTT	+1.05VS_VTTP to +1.05VS_VTT switched power rail for ARD CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VTT to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3V	+3VALW to +3V power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5V	+5VALW to +5V switched power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.				

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

BOM Config	
NEW71 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,71@,X7621@,XDP@
NEW91 SKU DISCTETE ONLY	BT@,3G@,DIS@,DIS ONLY@,NonSG@,91@,X7621@,XDP@

VRAM BOM Config

X7621@: X76198BOL21 ALT. GROUP PARTS 1G SAM

X7622@ X76198BOL22 ALT. GROUP PARTS 1G HYN

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMA ONLY@
Discrete	DIS@
Discrete Only	DIS ONLY@
VRAM	X76@
Switchable	SG@
Connector	CONN@
3G	3G@
Blue Tooth	BT@
Unpop	@
XDP	XDP@
NonSG	NonSG@
NEW71	71@
NEW91	91@

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB Port (Left Side)
	UHCI1	2	USB/B (Right Side)
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Camera
		9	Card Reader
	UHCI5	10	SIM Card
		11	Blue Tooth
	UHCI6	12	Mini Card(WLAN)
		13	Mini Card(GPS)

VRAM P/N :
Samsung : SA000035720 (S IC D3 64MX16 K4W1G1646E-HC12 FBGA ABO!)
Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA ABO!)

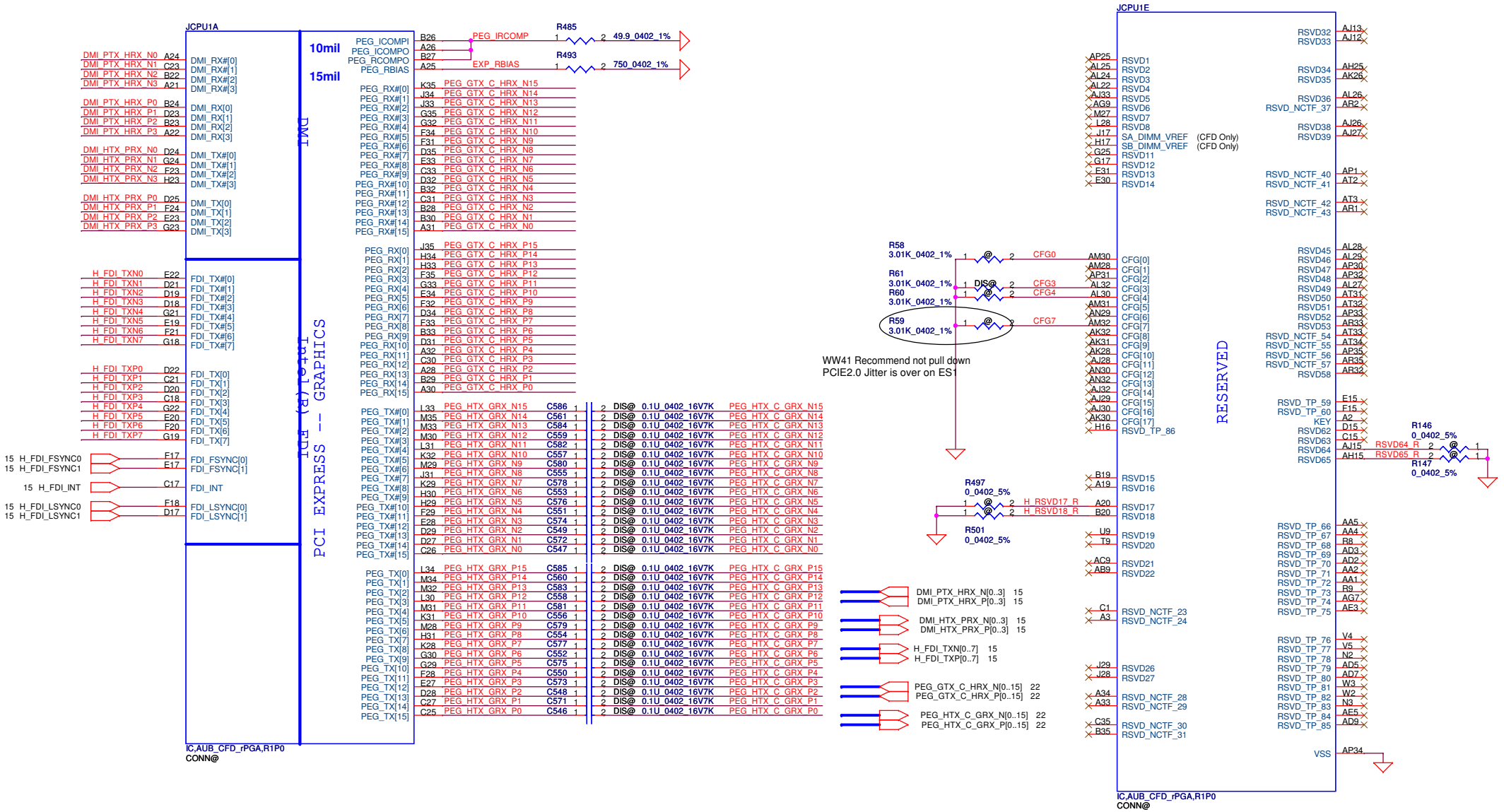
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Notes List

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 3 of 56



eDP Signals Mapping

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

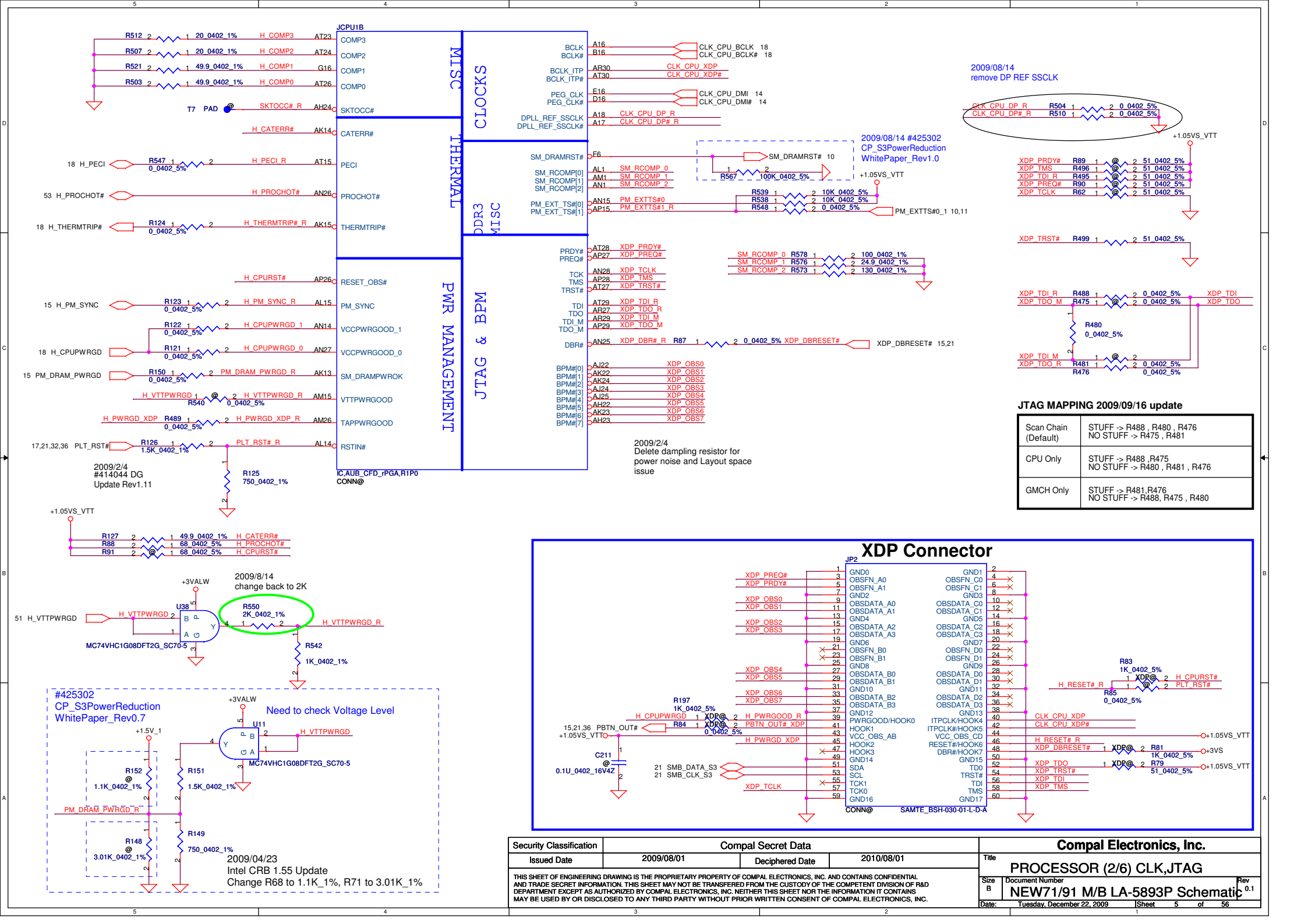
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

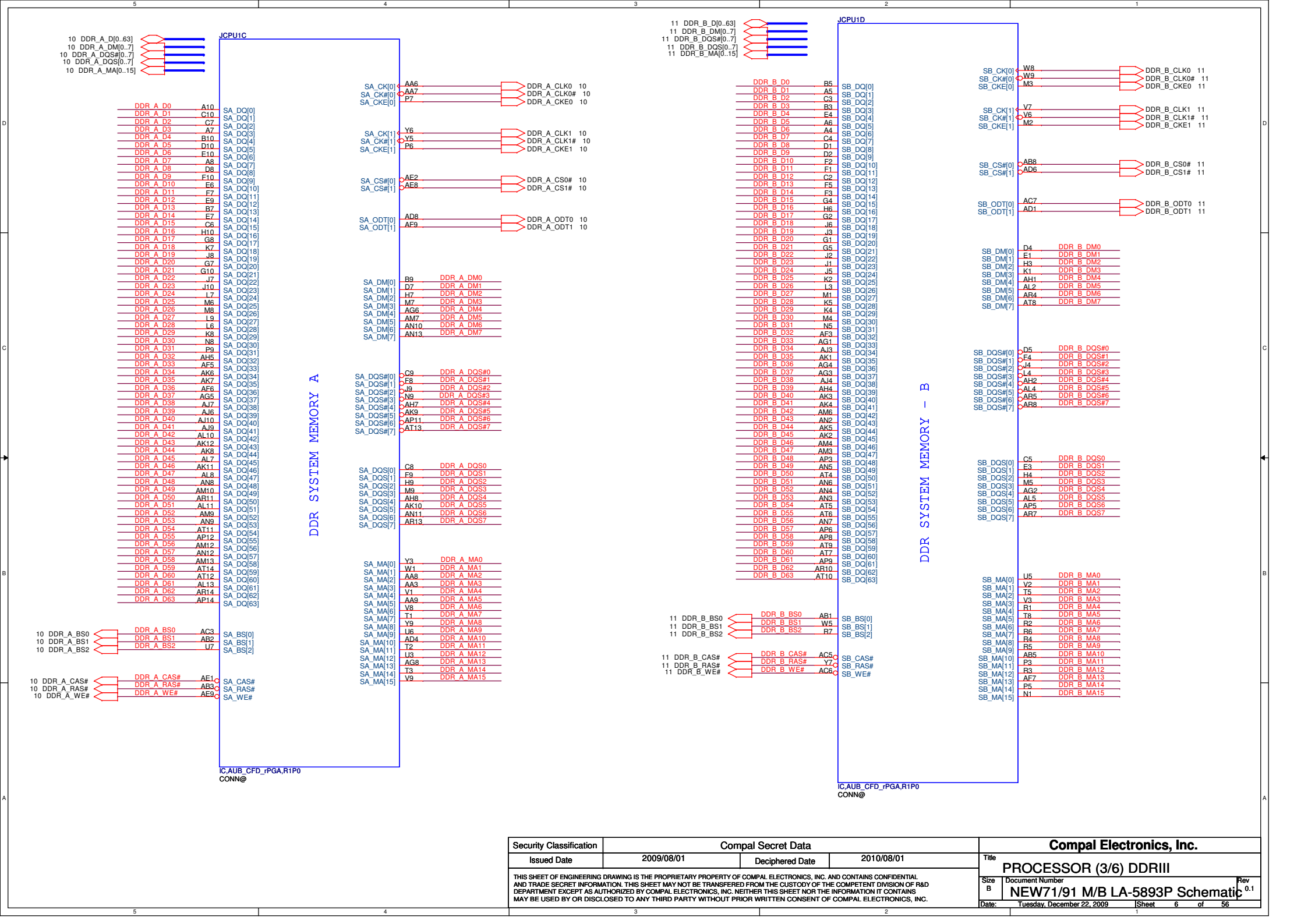
Date: Tuesday, December 22, 2009 Sheet 4 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title	PROCESSOR (2/6) CLK,JTAG	
Size B	Document Number NEW71/91 M/B LA-5893P Schematic	Rev 0.1
Date: Tuesday, December 22, 2009	Sheet 5 of 56	



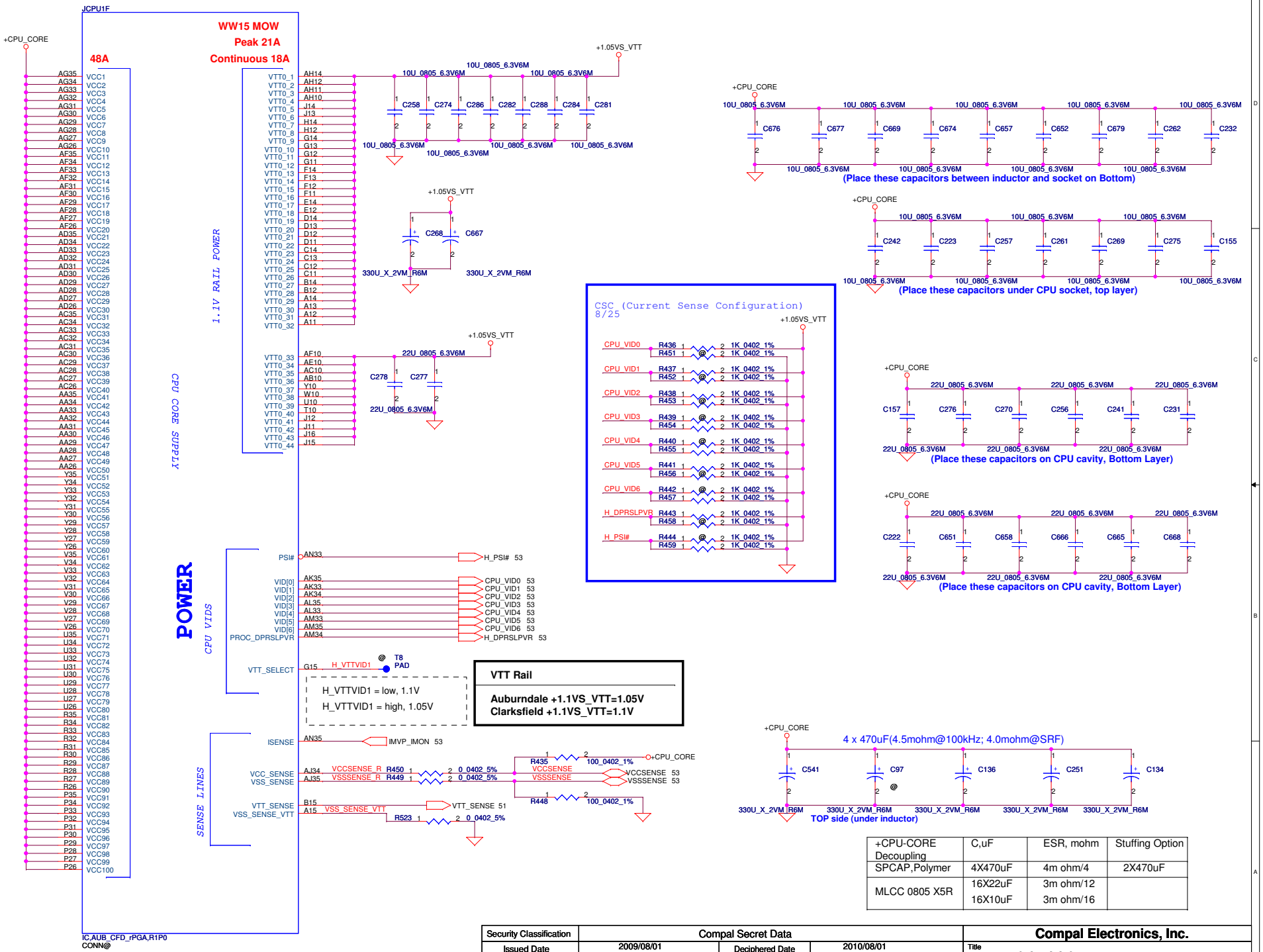
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 6 of 56



+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X470uF	4m ohm/4	2X470uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

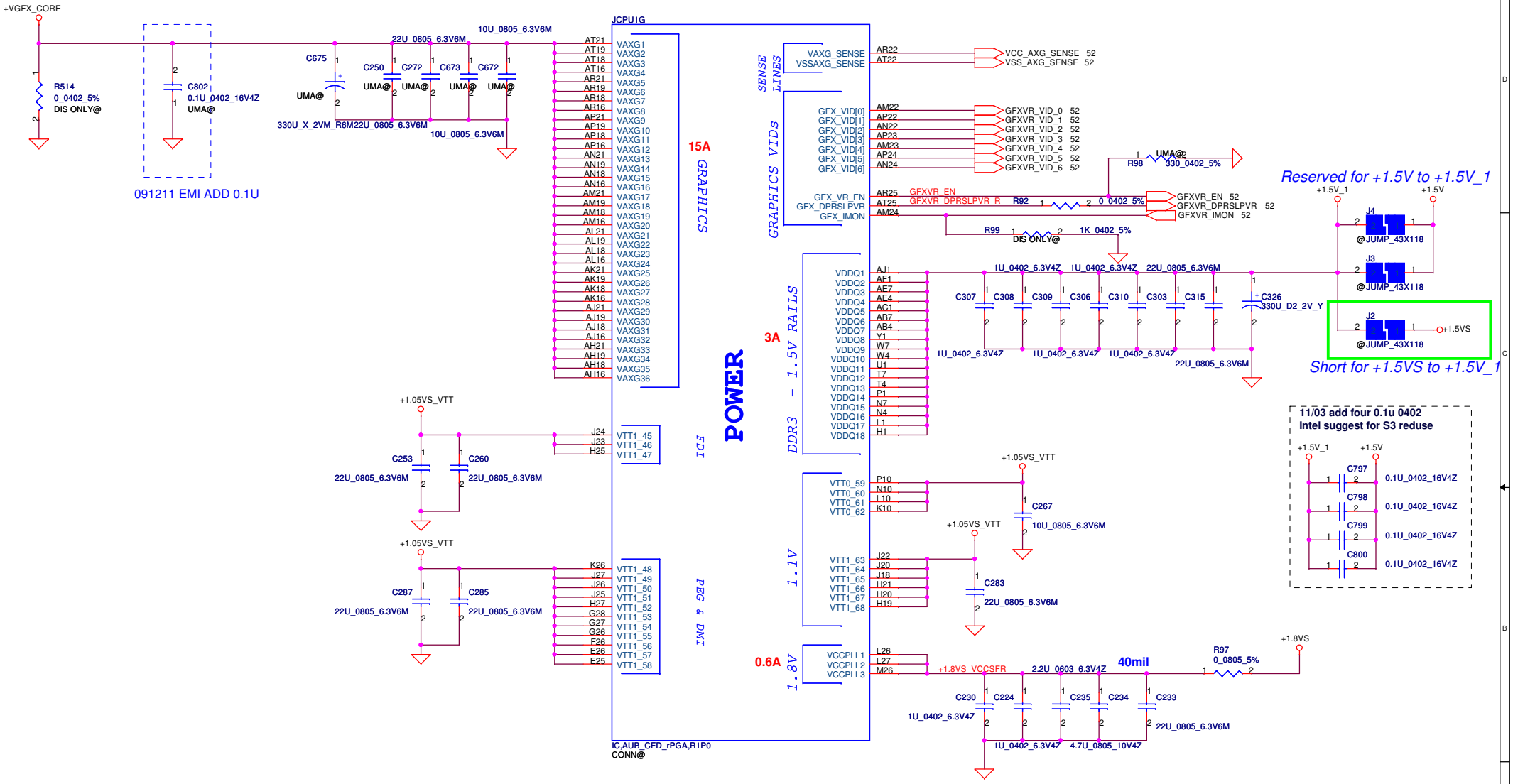
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (4/6) PWR,Bypass

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 7 of 56



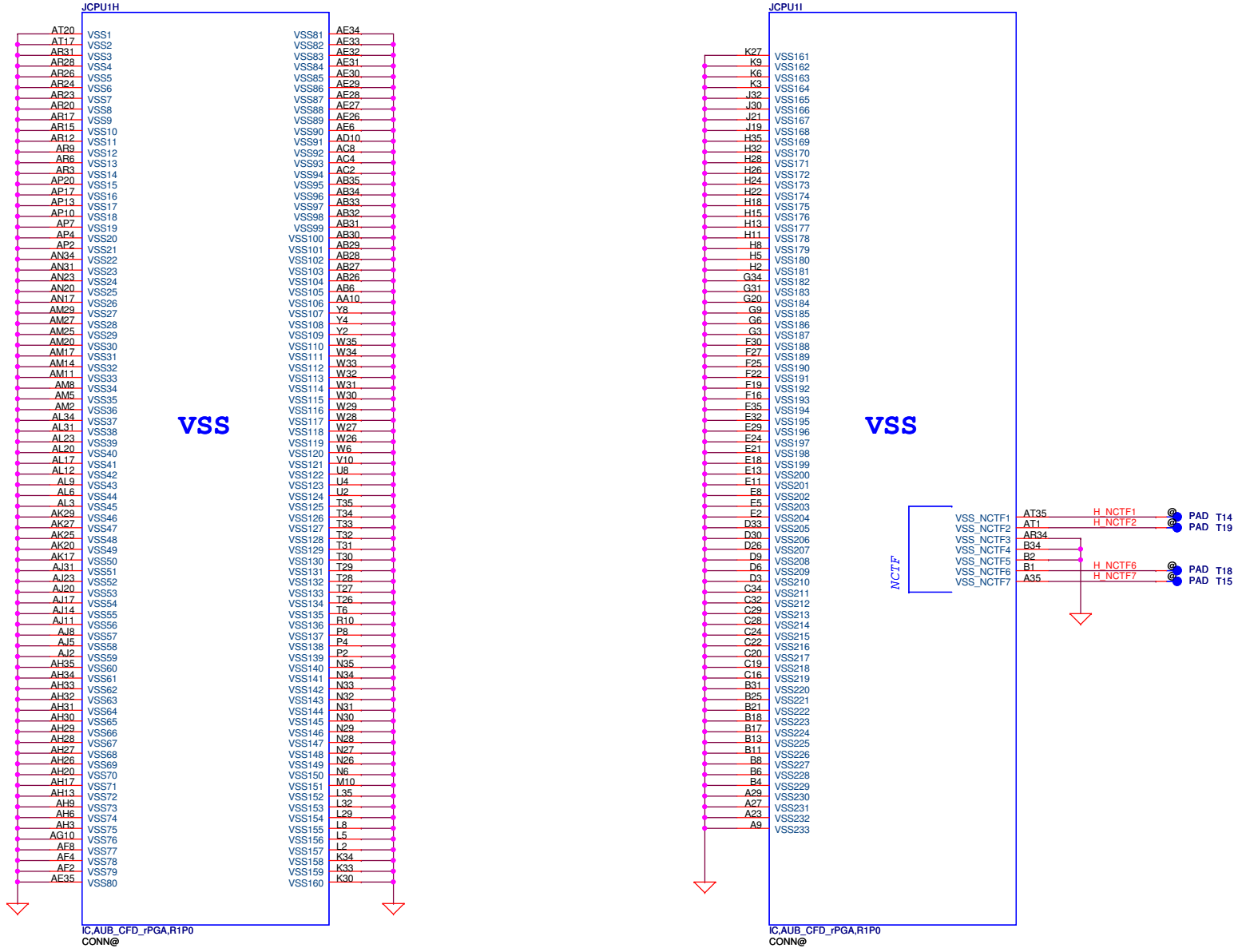
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (5/6) PWR

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 8 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Friday, December 18, 2009 | Sheet 9 of 56

DIMMA VREFDQ M1 Circuit

+1.5V

R222 1K_0402_1%

+DIMM_VREFDQA

20mil

R227 1K_0402_1%

DIMMA & DIMMB VREFCA circuit

+1.5V

R203 1K_0402_1%

+DIMM_VREFCA

20mil

R201 1K_0402_1%

6 DDR_A_DQS#[0..7]
6 DDR_A_D[0..63]
6 DDR_A_DM[0..7]
6 DDR_A_DQS[0..7]
6 DDR_A_MA[0..15]

#425302
CP_S3PowerReduction
WhitePaper_Rev1.0

+1.5V

R254 0_0402_5%

R274 1K_0402_1%

5 SM_DRAMRST#

DIMM_DRAMRST#

DIMM_DRAMRST# 11

Q17 BSS138LT1G_SOT23-3

C422 0.047U_0402_16V7K

18 RST_GATE

RST_GATE

+DIMM_VREFDQA

C401 0.1U_0402_16V4Z

C402 2.2U_0603_6.3V4Z

JDIMM1

		1	VREF_DQ	VSS1	2		
		3	VSS2	DQ4	4	DDR_A_D4	
DDR_A_D0	DDR_A_D1	5	DQ0	DQ5	6	DDR_A_D5	
		7	DQ1	VSS3	8		
DDR_A_DM0		9	VSS4	DQS#0	10	DDR_A_DQS#0	
		11	DM0	DQS0	12	DDR_A_DQS0	
DDR_A_D2	DDR_A_D3	13	VSS5	DQ6	14	DDR_A_D6	
		15	DQ2	DQ7	16	DDR_A_D7	
DDR_A_D8	DDR_A_D9	17	DQ3	VSS8	18		
		19	VSS7	DQ12	20	DDR_A_D12	
DDR_A_DQS#1	DDR_A_DQS1	21	DQ8	DQ13	22	DDR_A_D13	
		23	DQ9	VSS10	24		
DDR_A_D10	DDR_A_D11	25	VSS9	DM1	26	DDR_A_DM1	
		27	DQS#1	RESET#	28	DIMM_DRAMRST#	
DDR_A_D16	DDR_A_D17	29	DQS1	VSS12	30		
		31	VSS11	DQ14	32	DDR_A_D14	
DDR_A_DQS#2	DDR_A_DQS2	33	DQ10	DQ15	34	DDR_A_D15	
		35	DQ11	VSS14	36		
DDR_A_D18	DDR_A_D19	37	VSS13	DQ20	38	DDR_A_D20	
		39	DQ16	DQ21	40	DDR_A_D21	
DDR_A_D24	DDR_A_D25	41	DQ17	VSS16	42		
		43	VSS15	DM2	44	DDR_A_DM2	
DDR_A_DM3		45	DQS#2	VSS17	46		
		47	DQS2	DQ22	48	DDR_A_D22	
DDR_A_D26	DDR_A_D27	49	VSS18	DQ23	50	DDR_A_D23	
		51	DQ18	VSS19	52		
		53	DQ19	DQ28	54	DDR_A_D28	
		55	VSS20	DQ29	56	DDR_A_D29	
		57	DQ24	VSS21	58		
		59	DQ25	DQS#3	60	DDR_A_DQS#3	
		61	VSS22	DQS3	62	DDR_A_DQS3	
		63	DM3	VSS24	64		
		65	VSS23	DQ30	66	DDR_A_D30	
		67	DQ26	DQ31	68	DDR_A_D31	
		69	DQ27	VSS26	70		
		71	VSS25		72		
6 DDR_A_CKE0	DDR_A_CKE0	73	CKE0	CKE1	74	DDR_A_CKE1	DDR_A_CKE1 6
		75	VDD1	VDD2	76		
		77	NC1	A15	78	DDR_A_MA15	
6 DDR_A_BS2	DDR_A_BS2	79	BA2	A14	80	DDR_A_MA14	
		81	VDD3	VDD4	82		
DDR_A_MA12	DDR_A_MA9	83	A12/BC#	A11	84	DDR_A_MA11	
		85	A9	A7	86	DDR_A_MA7	
		87	VDD5	VDD6	88		
DDR_A_MA8	DDR_A_MA5	89	A8	A6	90	DDR_A_MA6	
		91	A5	A4	92	DDR_A_MA4	
		93	VDD7	VDD8	94		
DDR_A_MA3	DDR_A_MA1	95	A3	A2	96	DDR_A_MA2	
		97	A1	A0	98	DDR_A_MA0	
		99	VDD9	VDD10	100		
6 DDR_A_CLK0	DDR_A_CLK0	101	CK0	CK1	102	DDR_A_CLK1	DDR_A_CLK1 6
6 DDR_A_CLK0#	DDR_A_CLK0#	103	CK0#	CK1#	104	DDR_A_CLK1#	DDR_A_CLK1# 6
		105	VDD11	VDD12	106		
DDR_A_MA10	DDR_A_BS0	107	A10/AP	BA1	108	DDR_A_BS1	DDR_A_BS1 6
6 DDR_A_BS0		109	BA0	RAS#	110	DDR_A_RAS#	DDR_A_RAS# 6
		111	VDD13	VDD14	112		
DDR_A_WE#		113	WE#	S0#	114	DDR_A_CS0#	DDR_A_CS0# 6
6 DDR_A_WE#	DDR_A_CAS#	115	CAS#	ODT0	116	DDR_A_ODT0	DDR_A_ODT0 6
6 DDR_A_CAS#		117	VDD15	VDD16	118		
DDR_A_MA13		119	A13	ODT1	120	DDR_A_ODT1	DDR_A_ODT1 6
6 DDR_A_CS1#	DDR_A_CS1#	121	S1#	NC2	122		
		123	VDD17	VDD18	124		
		125	NCTEST	VREF_CA	126	DDR_VREF_CA_DIMMA	
		127	VSS27	VSS28	128		
DDR_A_D32	DDR_A_D33	129	DQ32	DQ36	130	DDR_A_D36	
		131	DQ33	DQ37	132	DDR_A_D37	
DDR_A_DQS#4	DDR_A_DQS4	133	VSS29	VSS30	134		
		135	DQS#4	DM4	136	DDR_A_DM4	
DDR_A_D34	DDR_A_D35	137	DQS4	VSS31	138		
		139	VSS32	DQ38	140	DDR_A_D38	
DDR_A_D40	DDR_A_D41	141	DQ34	DQ39	142	DDR_A_D39	
		143	DQ35	VSS33	144		
DDR_A_DM5		145	VSS34	DQ44	146	DDR_A_D44	
		147	DQ40	DQ45	148	DDR_A_D45	
DDR_A_D42	DDR_A_D43	149	DQ41	VSS35	150		
		151	VSS36	DQS#5	152	DDR_A_DQS#5	
DDR_A_D48	DDR_A_D49	153	DM5	DQS5	154	DDR_A_DQS5	
		155	VSS37	VSS38	156		
DDR_A_DQS#6	DDR_A_DQS6	157	DQ42	DQ46	158	DDR_A_D46	
		159	DQ43	DQ47	160	DDR_A_D47	
DDR_A_D50	DDR_A_D51	161	VSS39	VSS40	162		
		163	DQ48	DQ52	164	DDR_A_D52	
DDR_A_D56	DDR_A_D57	165	DQ49	DQ53	166	DDR_A_D53	
		167	VSS41	VSS42	168		
DDR_A_DM7		169	DQS#6	DM6	170	DDR_A_DM6	
		171	DQS6	VSS43	172		
DDR_A_D58	DDR_A_D59	173	VSS44	DQ54	174	DDR_A_D54	
		175	DQ50	DQ55	176	DDR_A_D55	
		177	DQ51	VSS45	178		
		179	VSS46	DQ60	180	DDR_A_D60	
		181	DQ56	DQ61	182	DDR_A_D61	
		183	DQ57	VSS47	184		
		185	VSS48	DQS#7	186	DDR_A_DQS#7	
		187	DM7	DQS7	188	DDR_A_DQS7	
		189	VSS49	VSS50	190		
		191	DQ58	DQ62	192	DDR_A_D62	
		193	DQ59	DQ63	194	DDR_A_D63	
		195	VSS51	VSS52	196		
		197	SA0	EVENT#	198	PM_EXTTS#0_1	PM_EXTTS#0_1 5,11
		199	VDDSPD	SDA	200	D_CK_SDATA	D_CK_SDATA 11,12
		201	SA1	SCL	202	D_CK_SCLK	D_CK_SCLK 11,12
		203	VTT1	VTT2	204	+0.75VS	
		205	G1	G2	206		

FOX_AS0A626-U8RN-7F

+1.5V

+3VS

R218 10K_0402_5%

C403 2.2U_0603_6.3V4Z

C398 0.1U_0402_16V4Z

R217 10K_0402_5%

+DIMM_VREFCA

R202 0_0402_5%

C358 2.2U_0603_6.3V4Z

C361 0.1U_0402_16V4Z

Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V

C354 10U_0805_6.3V6M
C355 10U_0805_6.3V6M
C356 10U_0805_6.3V6M
C405 10U_0805_6.3V6M
C404 10U_0805_6.3V6M
C406 10U_0805_6.3V6M
C362 0.1U_0402_16V4Z
C363 0.1U_0402_16V4Z
C399 0.1U_0402_16V4Z
C400 0.1U_0402_16V4Z
C425 330U_2.5V_M_R15 @

Layout Note:
Place near JDIMM1.203 & JDIMM1.204

+0.75VS

C391 1U_0402_6.3V4Z
C388 1U_0402_6.3V4Z
C397 1U_0402_6.3V4Z
C396 1U_0402_6.3V4Z
C394 10U_0805_6.3V6M

DDR3 SO-DIMM A
H=8mm

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT1

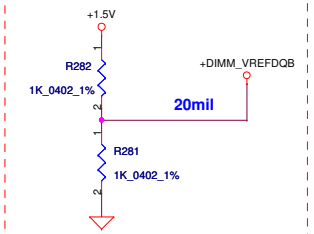
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 10 of 56

6 DDR_B_DQS#[0..7]
6 DDR_B_D[0..63]
6 DDR_B_DM[0..7]
6 DDR_B_DQS[0..7]
6 DDR_B_MA[0..15]

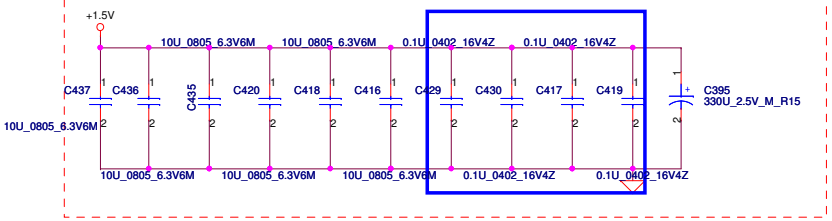
2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

DIMMB VREFDQ M1 Circuit

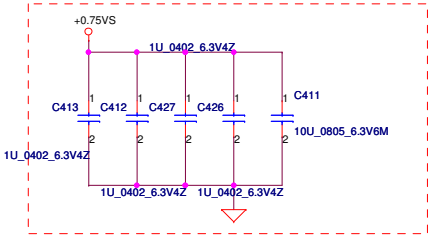


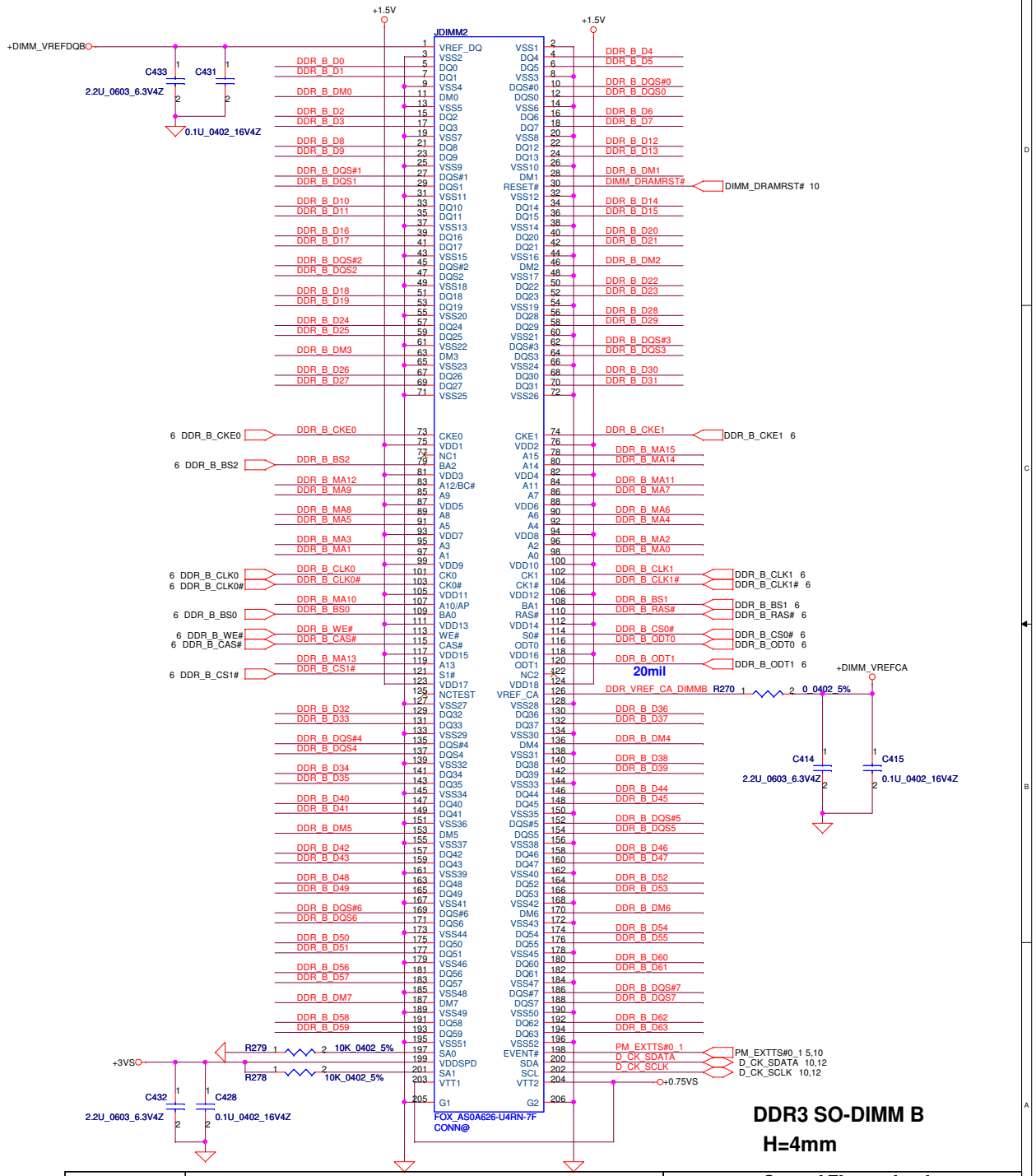
Layout Note:
Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMB



Layout Note:
Place near JDIMM2.203 & JDIMM2.204





DDR3 SO-DIMM B
H=4mm

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

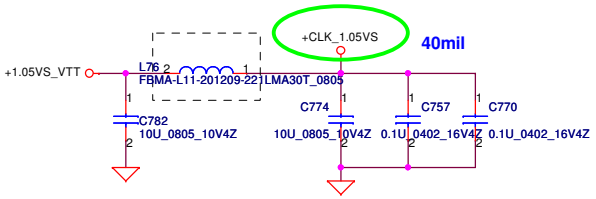
Compal Electronics, Inc.

Title: DDRIII-SODIMM SLOT2

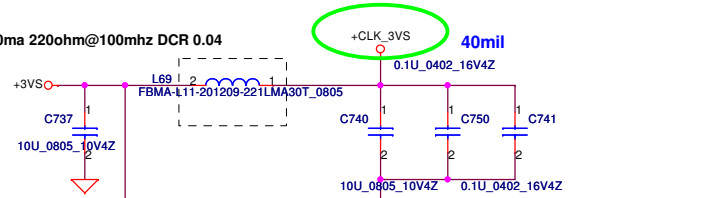
Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 11 of 56

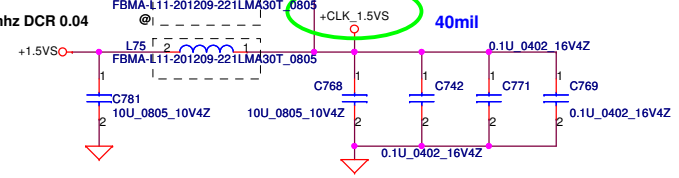
SM010014520 3000ma 220ohm@100mhz DCR 0.04



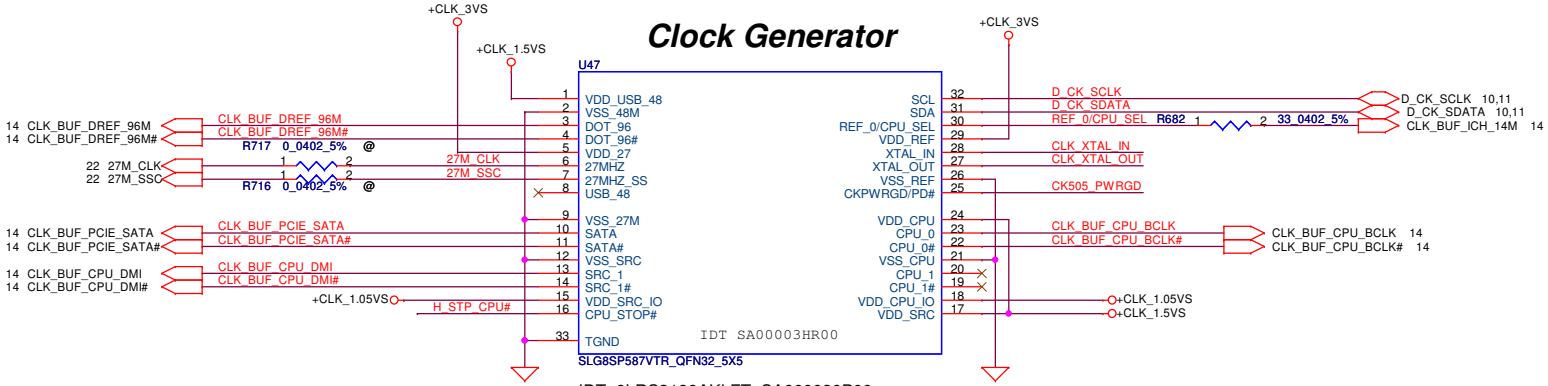
SM010014520 3000ma 220ohm@100mhz DCR 0.04



SM010014520 3000ma 220ohm@100mhz DCR 0.04



Clock Generator



IDT: 9LRS3199AKLFT, SA000030P00

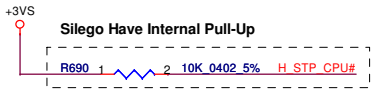
SILEGO: SLG8SP587V(WF), SA00002XY10

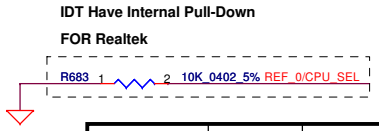
Low Power:

IDT: 9LVS3199AKLFT, SA00003HR00

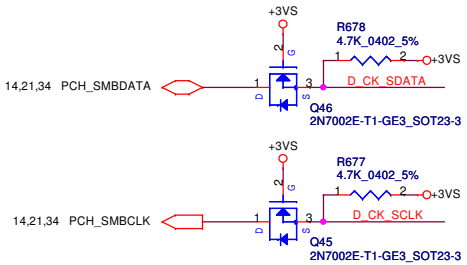
Realtek: RTM890N-631-VB-GRT, SA00003HQ10

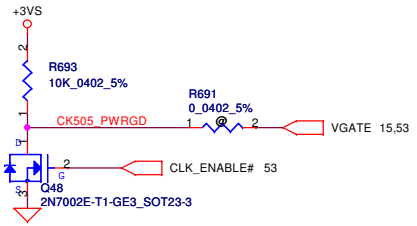
IDT 9LVS3199AKLFT NC

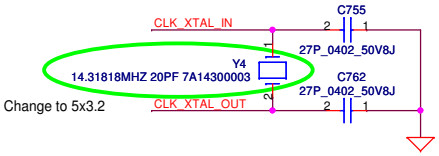




PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz







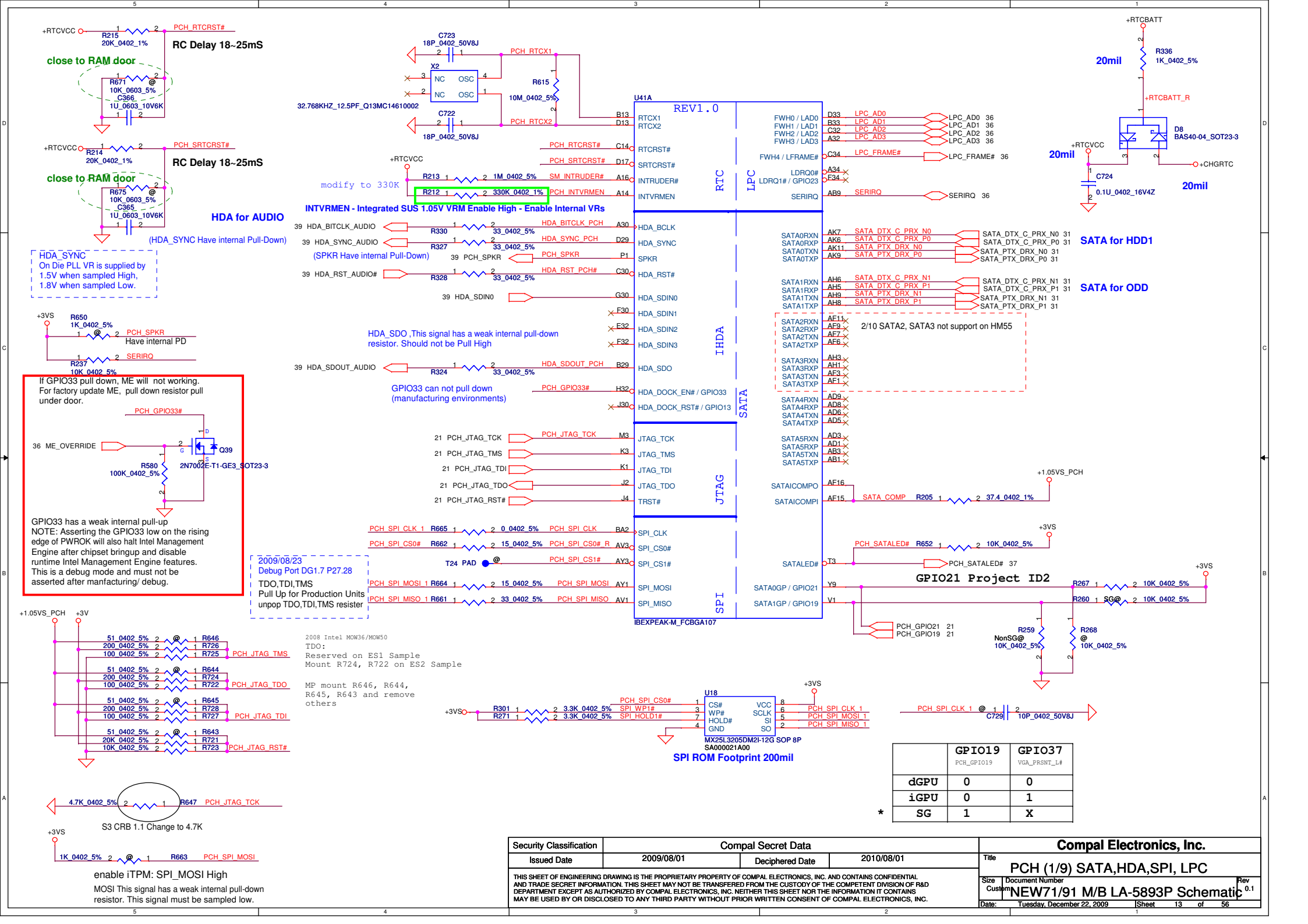
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Clock Generator (CK505)

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 12 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 13 of 56

1. Connect Directly
   EXPRESS CARD, MINI1, MINI2
2. Level Shift1, Pull-Up to +3VS
   CLOCK GEN, DIMM1, DIMM2
3. Level Shift2, Pull-Up to +3VS
   LAN
4. Level Shift3, Pull-Up to +3VS
   CPU & PCH XDP

U41B
REV1.0
IBEXPEAK-M_FCBGA107

For PCIE LAN
32 PCIE_DTX_C_PRX_N1
32 PCIE_DTX_C_PRX_P1
32 PCIE_PTX_C_DRX_N1
32 PCIE_PTX_C_DRX_P1
C335 0.1U_0402_16V7K
C339 0.1U_0402_16V7K
PCIE_DTX_C_PRX_N1 BG30
PCIE_DTX_C_PRX_P1 BJ30
PCIE_PTX_DRX_N1 BF29
PCIE_PTX_DRX_P1 BH29

For Wireless LAN
34 PCIE_DTX_C_PRX_N2
34 PCIE_DTX_C_PRX_P2
34 PCIE_PTX_C_DRX_N2
34 PCIE_PTX_C_DRX_P2
C332 0.1U_0402_16V7K
C334 0.1U_0402_16V7K
PCIE_DTX_C_PRX_N2 AW30
PCIE_DTX_C_PRX_P2 BA30
PCIE_PTX_DRX_N2 BC30
PCIE_PTX_DRX_P2 BD30

PERN1 PERP1 PETN1 PETP1
PERN2 PERP2 PETN2 PETP2
PERN3 PERP3 PETN3 PETP3
PERN4 PERP4 PETN4 PETP4

For Mini2
2009/08/25: remove PCIE5
PERN5 PERP5 PETN5 PETP5

PERN6 PERP6 PETN6 PETP6

2/10 PCIE7, PCIE8 not support on HM55
PERN7 PERP7 PETN7 PETP7
PERN8 PERP8 PETN8 PETP8

PCI_E* Controller Link

SMBus
SMBALERT# / GPIO11 B9 EC_LID_OUT# → EC_LID_OUT# 36
SMBCLK H14 PCH_SMBCLK → PCH_SMBCLK 12,21,34
SMBDATA C8 PCH_SMBDATA → PCH_SMBDATA 12,21,34
SML0ALERT# / GPIO60 J14 PCH_GPIO60
SML0CLK C6
SML0DATA G8
SML1ALERT# / GPIO74 M14 PCH_GPIO74
SML1CLK / GPIO58 E10 PCH_SML1CLK
SML1DATA / GPIO75 G12 PCH_SML1DAT

CL_CLK1 T13
CL_DATA1 T11
CL_RST1# T9

PEG_A_CLKRQ# / GPIO47 H1 PEG_CLKREQ#_R
CLKOUT_PEG_A_N AD43 → CLK_PEG_VGA# 22
CLKOUT_PEG_A_P AD45 → CLK_PEG_VGA 22
CLKOUT_DMI_N AN4 → CLK_CPU_DMI# 5
CLKOUT_DMI_P AN2 → CLK_CPU_DMI 5

PEG

CLKOUT_DP_N / CLKOUT_BCLK1_N AT1
CLKOUT_DP_P / CLKOUT_BCLK1_P AT3

+3V
R636 10K_0402_5%
DGPU_PWR_EN 18,21,38,42
R275 DIS@ 10K_0402_5%
Q18 DIS@ 2N7002E-T1-GE3_SOT23-3
R247 @ 2.2K_0402_5%
R276 @ 2.2K_0402_5%
PEG_CLKREQ# 22

For PCIE LAN
32 CLK_PCIE_LAN#
32 CLK_PCIE_LAN
AK48 CLKOUT_PCIE0N
AK47 CLKOUT_PCIE0P
32 LAN_CLKREQ# R258 0_0402_5% PCH_GPIO73 P9 PCIECLKRQ0# / GPIO73

For Wireless LAN
34 CLK_PCIE_MINI1#
34 CLK_PCIE_MINI1
AM43 CLKOUT_PCIE1N
AM45 CLKOUT_PCIE1P
34 MINI1_CLKREQ# R266 0_0402_5% PCH_GPIO18 U4 PCIECLKRQ1# / GPIO18
21 PCH_GPIO18

AM47 CLKOUT_PCIE2N
AM48 CLKOUT_PCIE2P
21 PCH_GPIO20 PCH_GPIO20 N4 PCIECLKRQ2# / GPIO20

AH42 CLKOUT_PCIE3N
AH41 CLKOUT_PCIE3P
PCH_GPIO25 A8 PCIECLKRQ3# / GPIO25

2009/08/25: Change back to +3V
remove mini2
+3V
R241 10K_0402_5%
MINI2_CLKREQ#_1

2009/08/25: remove mini2 clk
AM51 CLKOUT_PCIE4N
AM53 CLKOUT_PCIE4P
MINI2_CLKREQ#_1 M9 PCIECLKRQ4# / GPIO26

AJ50 CLKOUT_PCIE5N
AJ52 CLKOUT_PCIE5P
PCH_GPIO44 H6 PCIECLKRQ5# / GPIO44

AK53 CLKOUT_PEG_B_N
AK51 CLKOUT_PEG_B_P
PCH_GPIO56 P13 PEG_B_CLKRQ# / GPIO56

From CLK BUFFER

CLKIN_DMI_N AW24 → CLK_BUF_CPU_DMI# 12
CLKIN_DMI_P BA24 → CLK_BUF_CPU_DMI 12
CLKIN_BCLK_N AP3 → CLK_BUF_CPU_BCLK# 12
CLKIN_BCLK_P AP1 → CLK_BUF_CPU_BCLK 12
CLKIN_DOT_96N F18 → CLK_BUF_DREF_96M# 12
CLKIN_DOT_96P E18 → CLK_BUF_DREF_96M 12
CLKIN_SATA_N / CKSSCD_N AH13 → CLK_BUF_PCIE_SATA# 12
CLKIN_SATA_P / CKSSCD_P AH12 → CLK_BUF_PCIE_SATA 12
REFCLK14IN P41 CLK_BUF_ICH_14M 12
R163 10_0402_5% C319 10P_0402_50V8J
1109 RF request
CLKIN_PCILOOPBACK J42 → CLK_PCI_FB 17

6/9 MOW23 Request add 25MHz crystal supporting Integrated Graphics
R563 DIS ONLY@ 0_0402_5%
C693 UMA@ 27P_0402_50V8J
R564 1M_0402_5% UMA@
Y2 25MHZ_20PF_7A25000012 UMA@
C694 27P_0402_50V8J UMA@
Change to 5x3.2

XTAL25_IN AH51
XTAL25_OUT AH53
XCLK_RCOMP AF38 XCLK_RCOMP R170 90.9_0402_1% +1.05VS_PCH

Clock Flex

CLKOUTFLEX0 / GPIO64 T45
CLKOUTFLEX1 / GPIO65 P43 PROJECT_ID1
CLKOUTFLEX2 / GPIO66 T42 PROJECT_ID0
CLKOUTFLEX3 / GPIO67 N50

Project Structure ID
+3VS
R156 10K_0402_5%
R144 10K_0402_5%
R157 10K_0402_5%
R167 10K_0402_5%

Project Structure			
GPIO21 ID2	GPIO65 ID1	GPIO66 ID0	Structure
0	0	0	NEW70
0	0	1	NEW80
0	1	0	NEW90
* 1	0	0	NEW71/91

+3VS
10K_0402_5% R265 MINI1_CLKREQ#
10K_0402_5% R649 PCH_GPIO20

Schematic_Checklist_Rev1.6

GPIO18	Main (core) power well (+V3.3S)	Muxed with PCIECLKRQ1#. If not used, requires 8.2-k to 10-k pull-up to +Vcc_3.3 (+V3.3S)
GPIO25	Resume (Sus) well (+V3.3A)	Muxed with PCIECLKRQ3# If not used, requires 8.2-k to 10-k pull-up to +V3.3A rail.

+3V
10K_0402_5% R623 EC_LID_OUT#
2.2K_0402_5% R602 PCH_SMBCLK
2.2K_0402_5% R626 PCH_SMBDATA
10K_0402_5% R208 PCH_GPIO60
2.2K_0402_5% R639 PCH_SML1CLK
2.2K_0402_5% R249 PCH_SML1DAT
10K_0402_5% R207 PCH_GPIO74
10K_0402_5% R244 PCH_GPIO44
10K_0402_5% R206 PCH_GPIO56
10K_0402_5% R257 PCH_GPIO73

+3V
9/1: Change to +3VS
2009/08/13: Change back to +3V
10K_0402_5% R624 PCH_GPIO25

+3VS
PCH_SML1CLK 6 Q19A 2N7002DWH_SOT363-6 1 EC_SMB_CK2 → EC_SMB_CK2 22,36

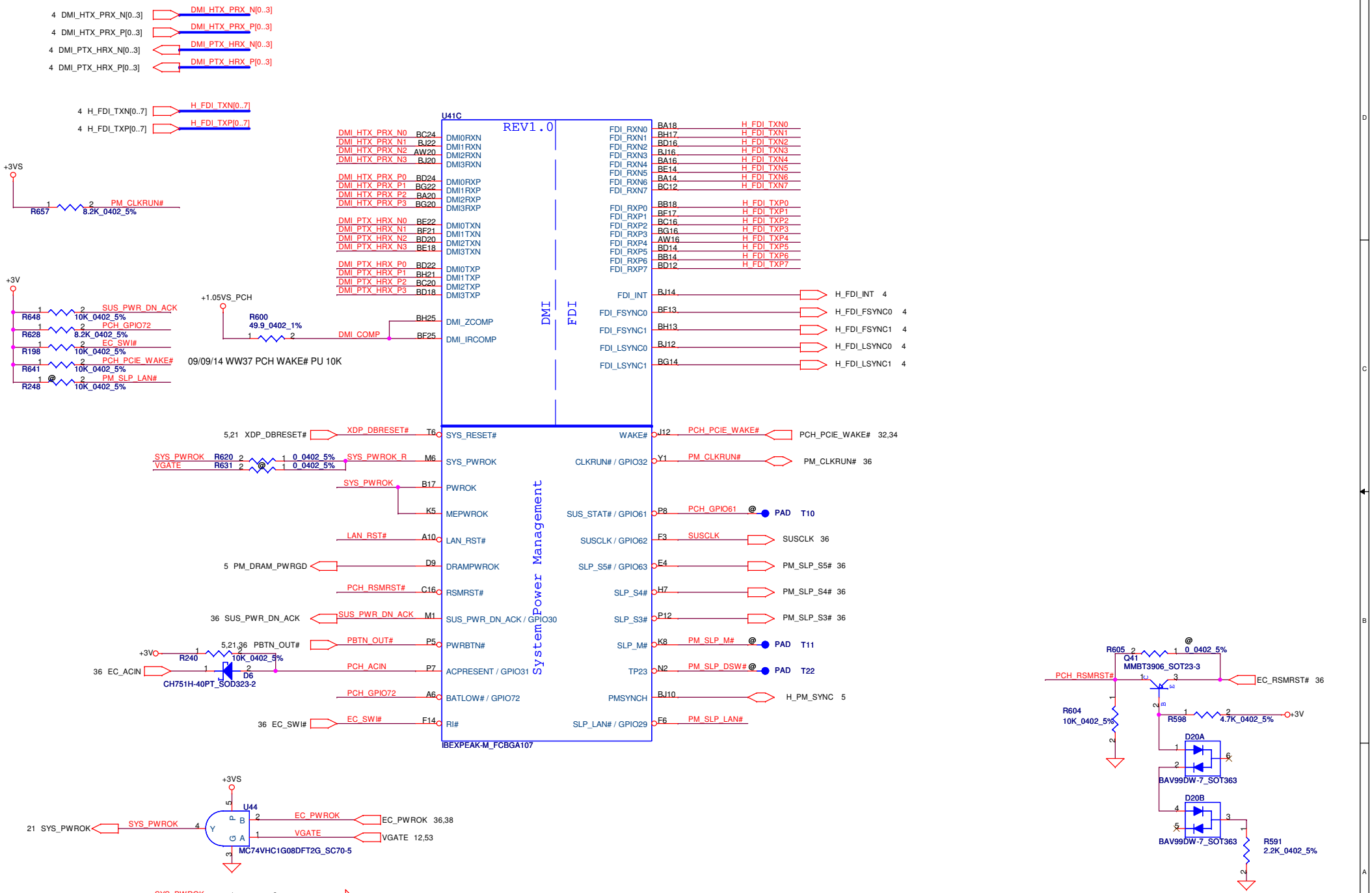
+3VS
Pull high +3VS at KB926 side
PCH_SML1DAT 3 Q19B 2N7002DWH_SOT363-6 4 EC_SMB_DA2 → EC_SMB_DA2 22,36

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1
Date: Tuesday, December 22, 2009	Sheet 14 of 56	



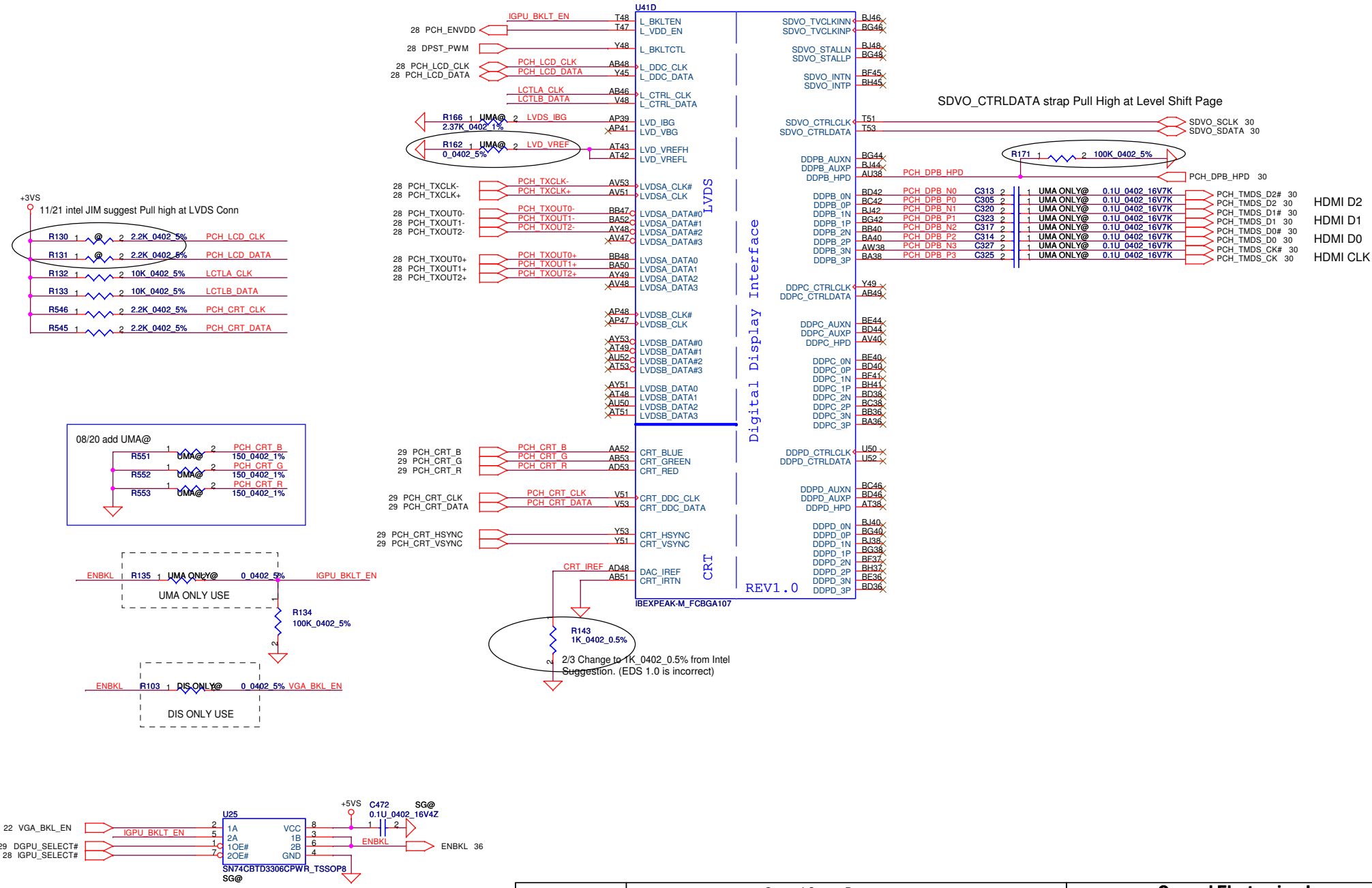
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 Sheet 15 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 16 of 56

U41E

REV1.0

IBEXPEAK-M_FCBGA107

PCI_GNT0#,PCI_GNT1#,PCI_GNT2#,PCI_GNT3#
has a weak internal pull-up

PCI_GNT2# ESI Strap (Server Only)
this signal should not be pulled low

2008/1/6 2009MOW01 change to 22 ohm

NV_ALE,NV_CLE
has a weak internal pull-down

Design Guide 1.5 Ver:
3.26.13 Terminating Unused Braidwood Interface

If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.

USB/B (Right Side)
USB Port (Left Side)
USB/B (Right Side)
EHCI 1

2/10 USB6, USB7 not support on HM55

CMOS Camera (LVDS)
Card Reader
Mini Card(SIM Card)
Bluetooth
Mini Card(WLAN)
Mini Card(WWAN)
EHCI 2

(For USB Port0, 2)
(For USB Port1)

OC[0..3] use for EHCI 1
OC[4..7] use for EHCI 2

Intel Anti-Theft Techonlogy	
NV_ALE	High=Endabled
	Low=Disable(floating) ★

DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

NV_ALE
Enable Intel Anti-Theft Technology : 8.2K PU to +3VS

Disable Intel Anti-Theft Technology : floating(internal PD)

NV_CLE

DMI termination voltage.
weak internal PU, don't PD

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

A16 swap overide Strap/Top-Block Swap Override jumper	
PCI_GNT3#	Low=A16 swap override/Top-Block Swap Override enabled High=Default ★

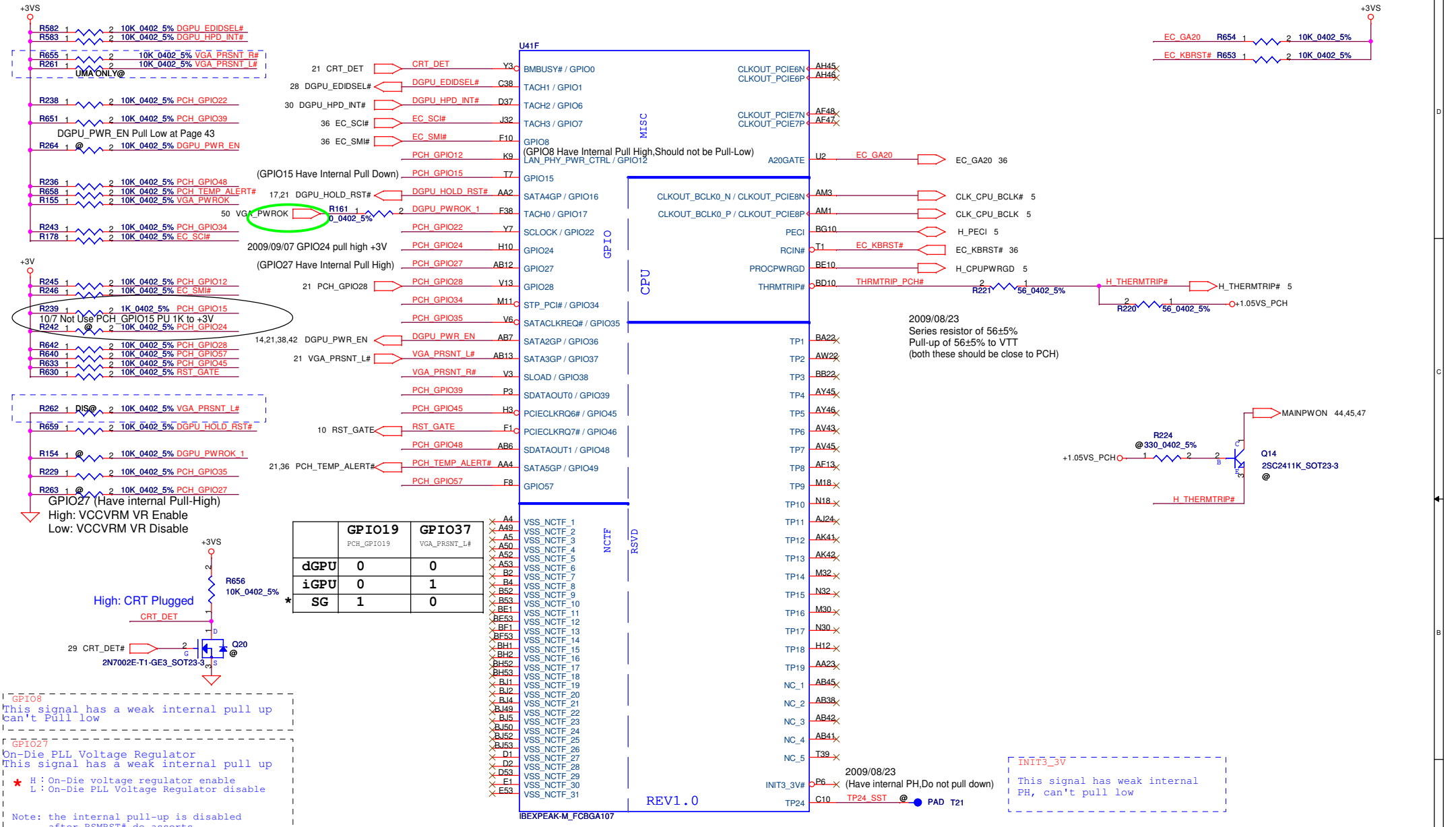
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 17 of 56



	GPIO19 (PCH_GPIO19)	GPIO37 (VGA_PRSNT_L#)
dGPU	0	0
iGPU	0	1
SG	1	0

GPIO8
This signal has a weak internal pull up can't Pull low

GPIO27
On-Die PLL Voltage Regulator
This signal has a weak internal pull up

★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

Note: the internal pull-up is disabled after RSMRST# de-asserts.
The On-Die PLL voltage regulator is enabled when sampled high. When sampled low the On-Die PLL Voltage Regulator is disabled.

GPIO15
★ L : Intel ME Crypto Transport Layer Security(TLS) chiper suite with no confidentiality

H : Intel ME Crypto Transport Layer Security(TLS) chiper suite with confidentiality

CRB has a 1-k pull-up on this signal to +3.3VA rail.

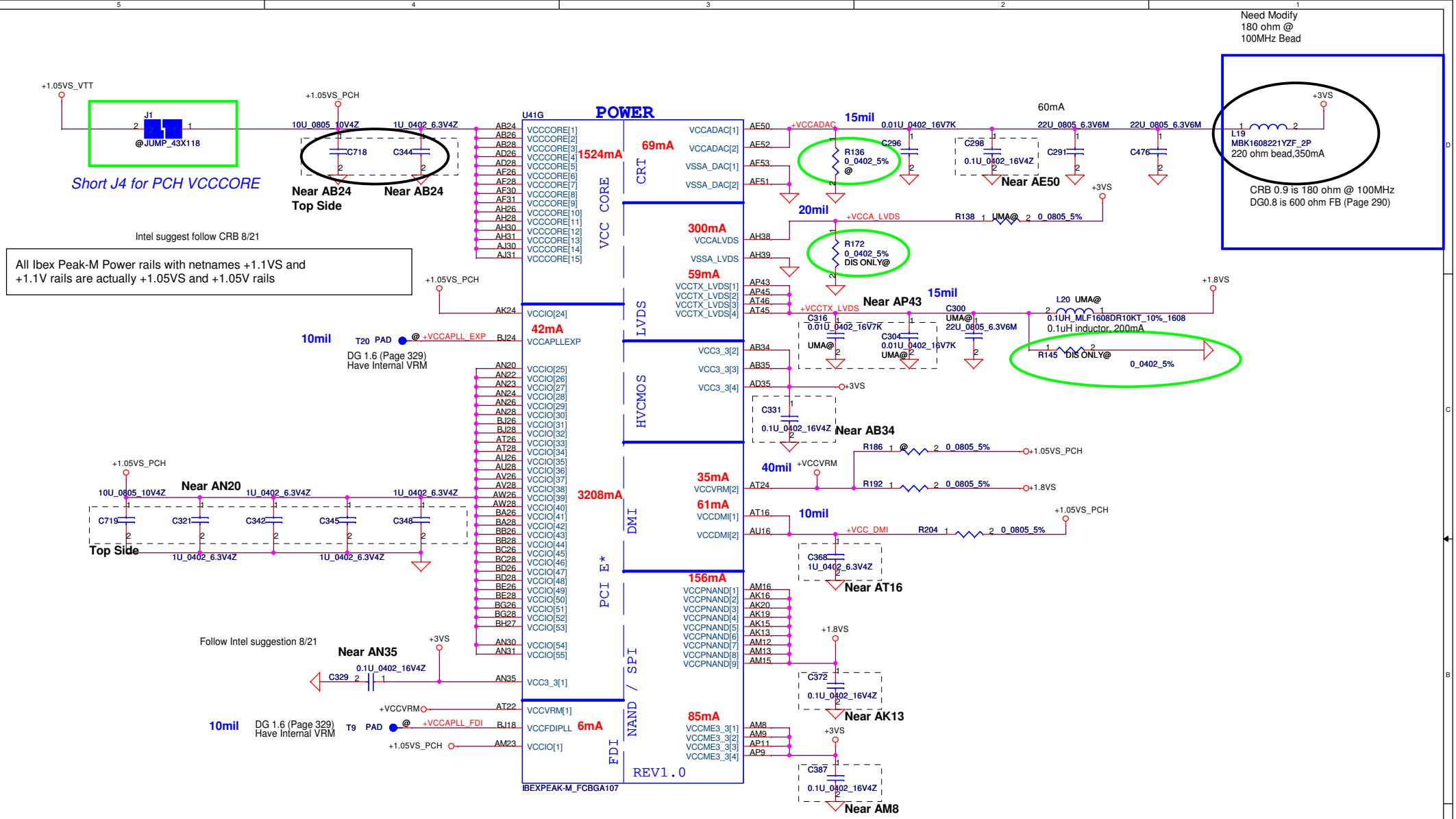
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 18 of 56



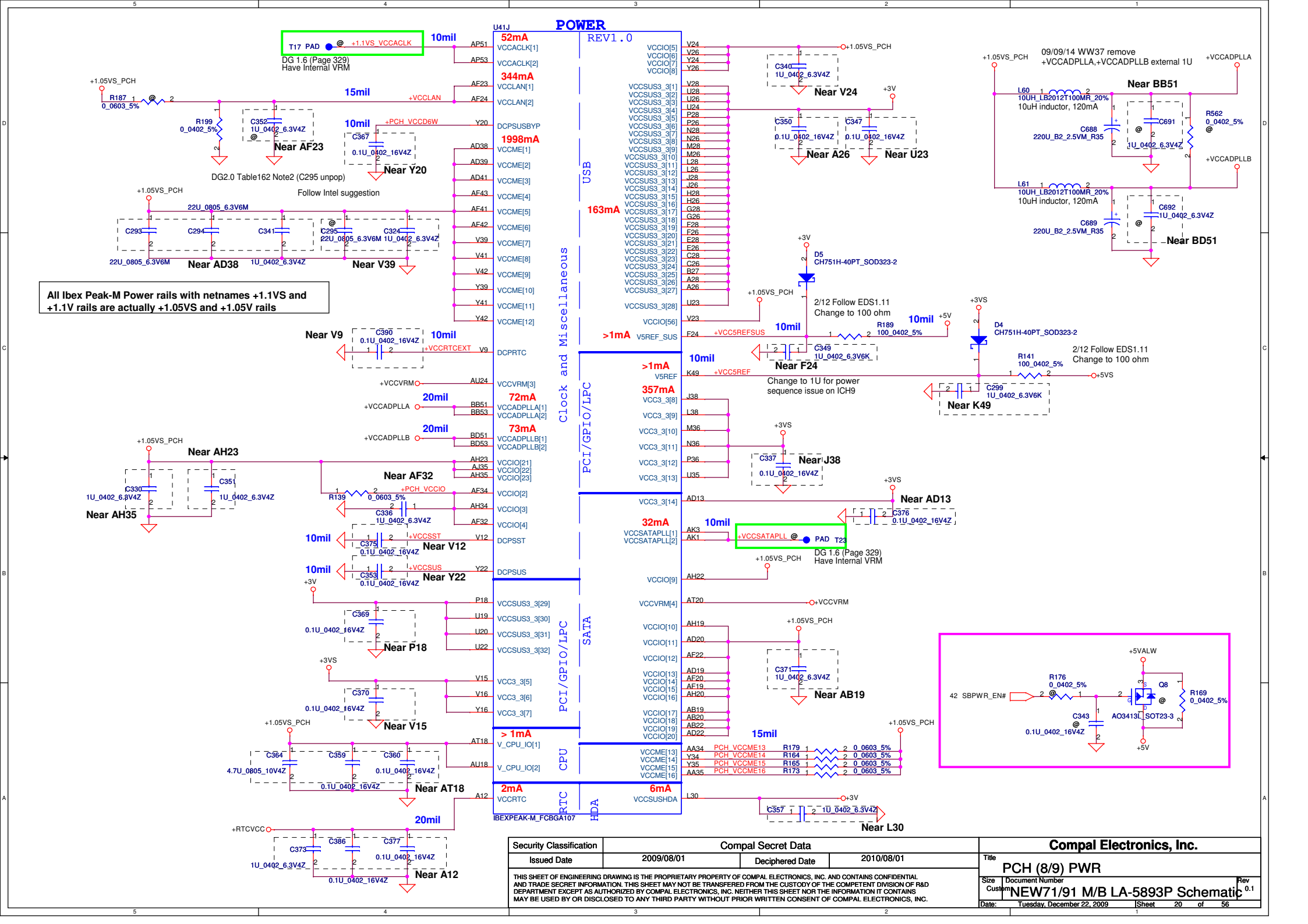
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (7/9) PWR

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Friday, December 18, 2009 Sheet 19 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

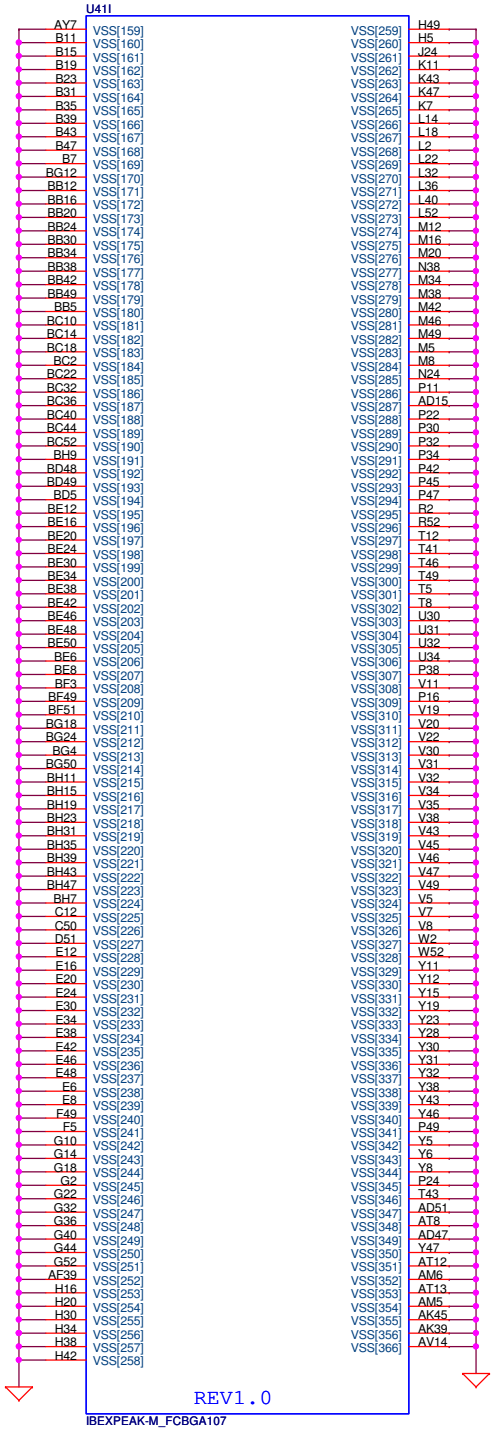
Compal Electronics, Inc.

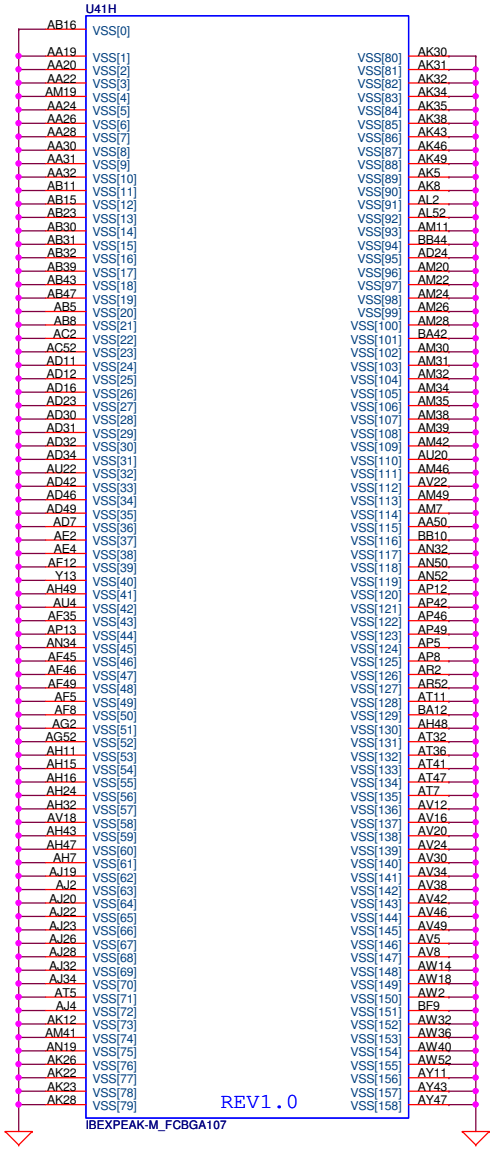
Title: PCH (8/9) PWR

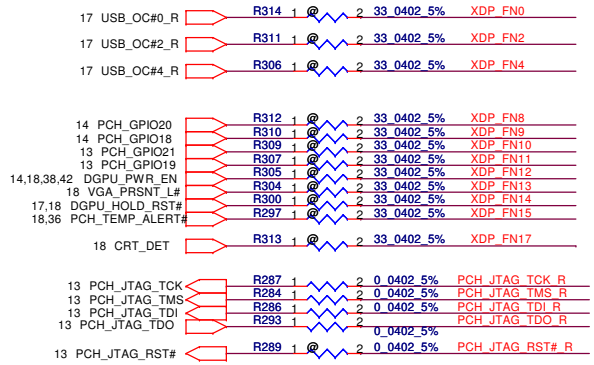
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

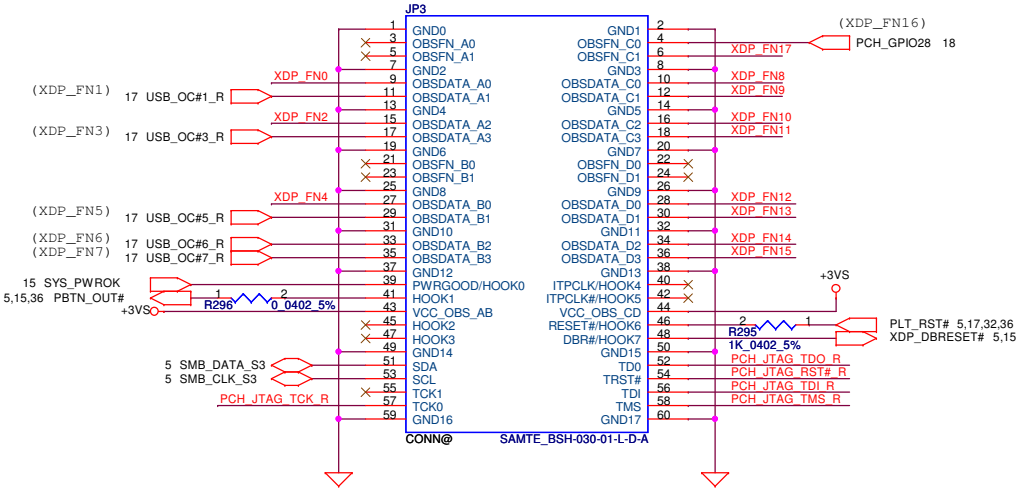
Date: Tuesday, December 22, 2009 | Sheet 20 of 56

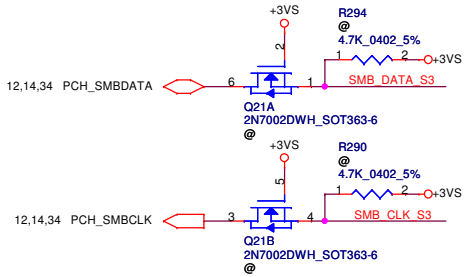
PCH XDP Port











Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 Sheet 21 of 56

GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

Unused MIO interface

When the MIOx interface is unused, the interface must still be powered by 3.3V, a decoupling capacitor of 0.1uF should still be placed on thx MIOx_VDDQ power rail and 10k pull down should be used on MIOx_CLKIN

External Spread Spectrum

If External Spread Spectrum not stuff then stuff resistor

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

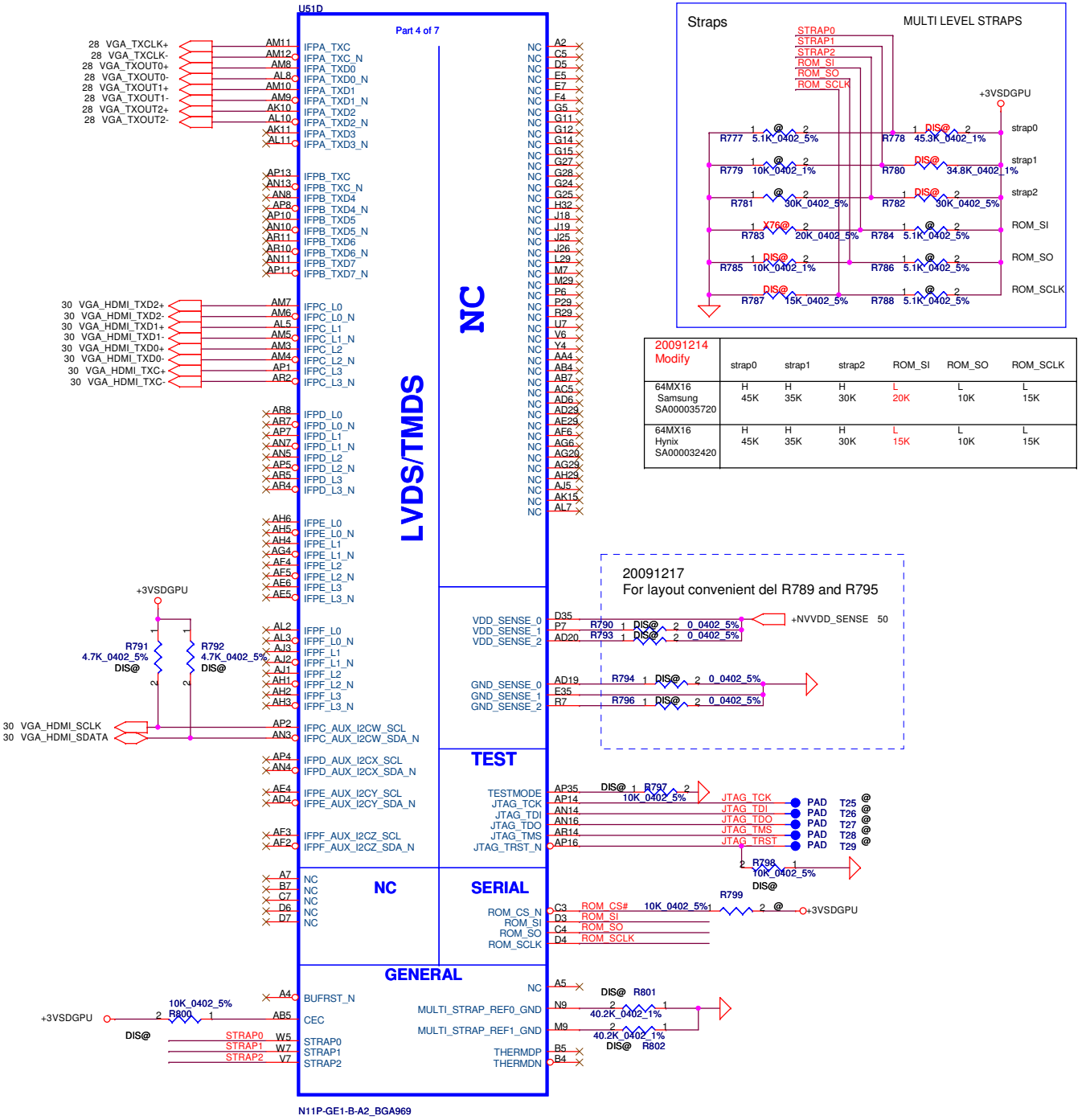
Compal Electronics, Inc.

Title: N11P-GV2H PEG I2C

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Wednesday, December 23, 2009 | Sheet 22 of 56

Mode E Command Mapping GB2-128 Package Femi	Mode C Command Mapping GB1-128 Package	Data Bit	0..31	32..63
FBx_CMD3	FBx_CMD0		CKE_L	
FBx_CMD8	FBx_CMD1		A8	A8
FBx_CMD2	FBx_CMD2		CS0_L*	
FBx_CMD21	FBx_CMD3		A7	A6
FBx_CMD24	FBx_CMD4		A2	A1
FBx_CMD23	FBx_CMD5		A11	A9
FBx_CMD26	FBx_CMD6		A5	A4
FBx_CMD7	FBx_CMD7		A0	A12
FBx_CMD15	FBx_CMD8		CAS*	CAS*
FBx_CMD13	FBx_CMD9		BA1	A3
FBx_CMD4	FBx_CMD10		A9	A11
FBx_CMD18	FBx_CMD11			CS0_H
FBx_CMD29	FBx_CMD12		BA0	BA0
FBx_CMD27	FBx_CMD13		BA2	A15
FBx_CMD6	FBx_CMD14		A3	BA1
FBx_CMD17	FBx_CMD15			CS1_H
FBx_CMD19	FBx_CMD16			ODT_H
FBx_CMD22	FBx_CMD17		A4	A5
FBx_CMD12	FBx_CMD18		A13	A14
FBx_CMD28	FBx_CMD19		WE*	A10
FBx_CMD10	FBx_CMD20		A1	A2
FBx_CMD25	FBx_CMD21		A10	WE*
FBx_CMD9	FBx_CMD22		A12	A0
FBx_CMD1	FBx_CMD23		CS1_L*	
FBx_CMD11	FBx_CMD24		RAS*	RAS*
FBx_CMD0	FBx_CMD25		ODT_L	
FBx_CMD5	FBx_CMD26		A6	A7
FBx_CMD16	FBx_CMD27			CKE_H
FBx_CMD20	FBx_CMD28		RST	RST
FBx_CMD14	FBx_CMD29		A14	A13
FBx_CMD30	FBx_CMD30		A15	BA2
FBx_CMD31				
			LOW	HIGH



20091214 Modify	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035720	H 45K	H 35K	H 30K	L 20K	L 10K	L 15K
64MX16 Hynix SA000032420	H 45K	H 35K	H 30K	L 15K	L 10K	L 15K

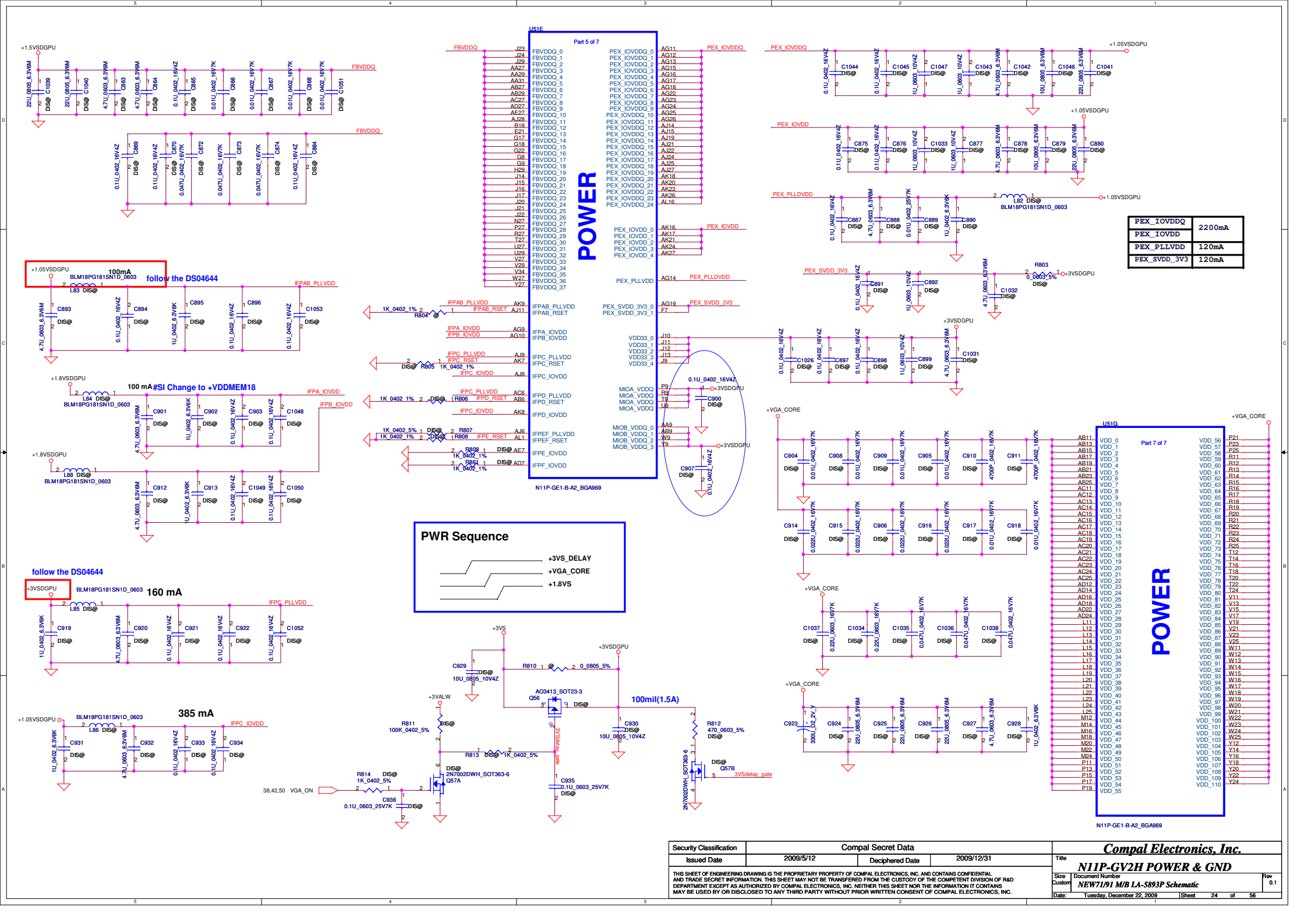
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: N11P-GV2H LVDS

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev:

Date: Tuesday, December 22, 2009 | Sheet 23 of 56



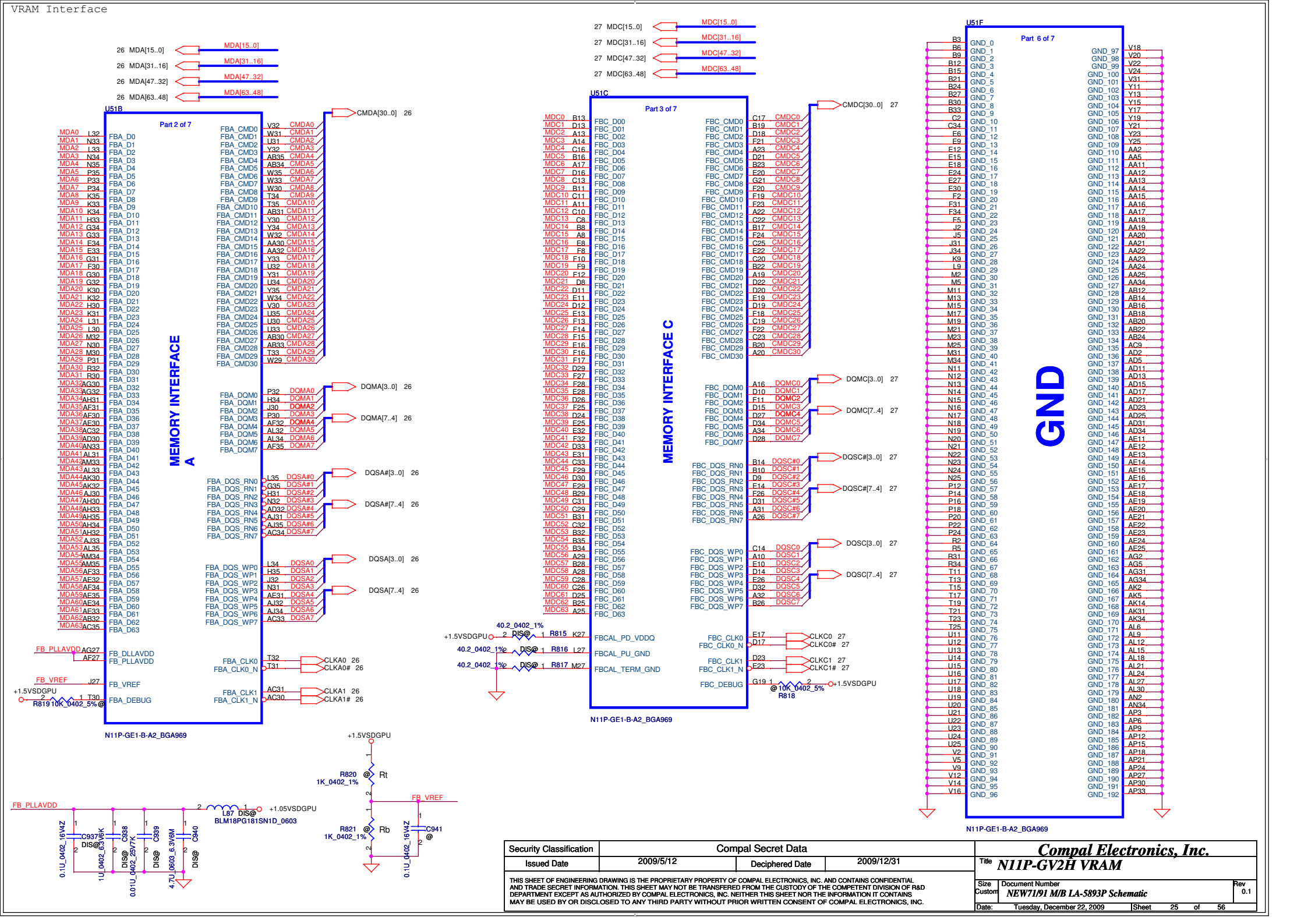
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: **N11P-GV2H POWER & GND**

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 24 of 56



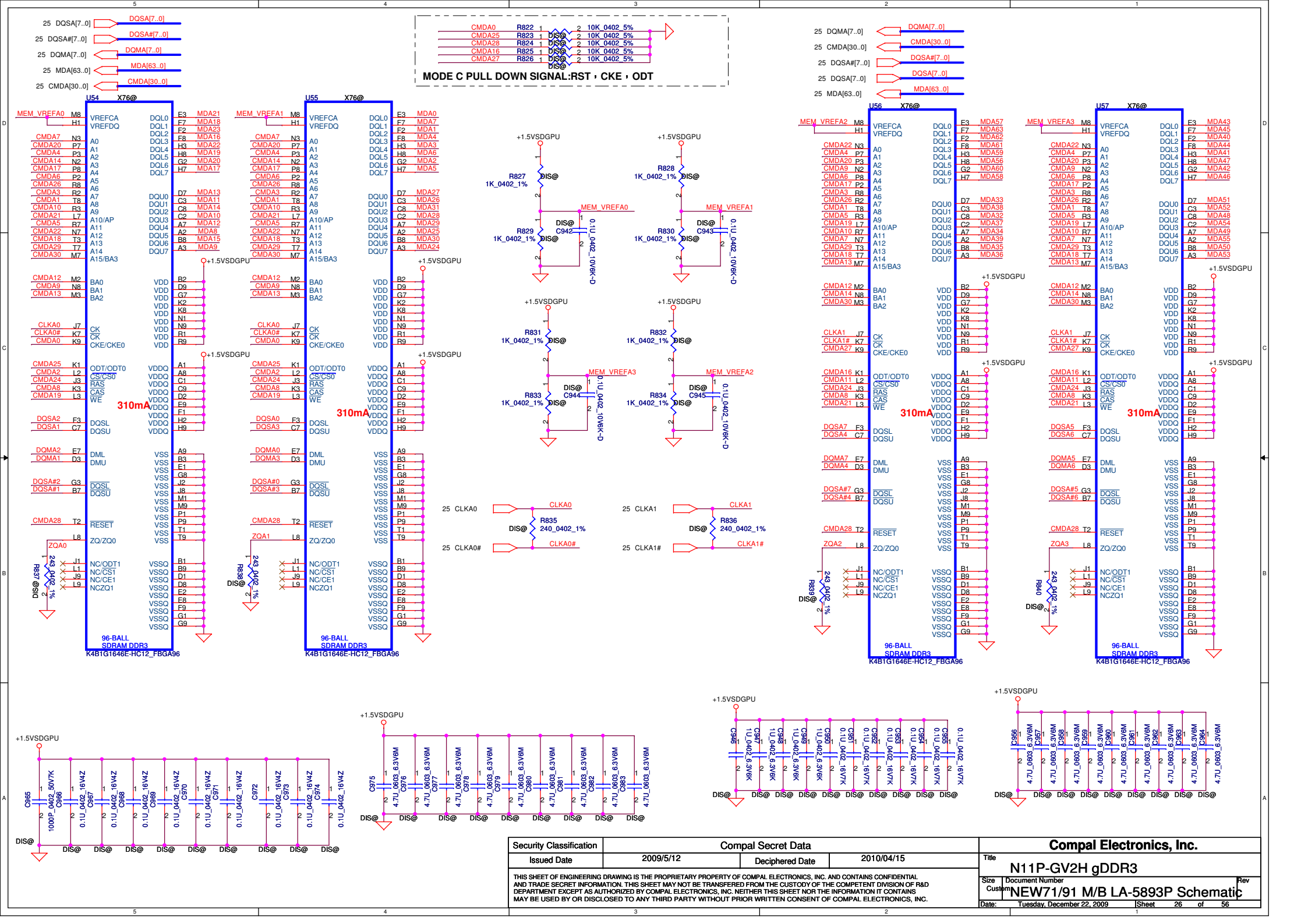
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

Compal Electronics, Inc.

Title: **N11P-GV2H VRAM**

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 25 of 56



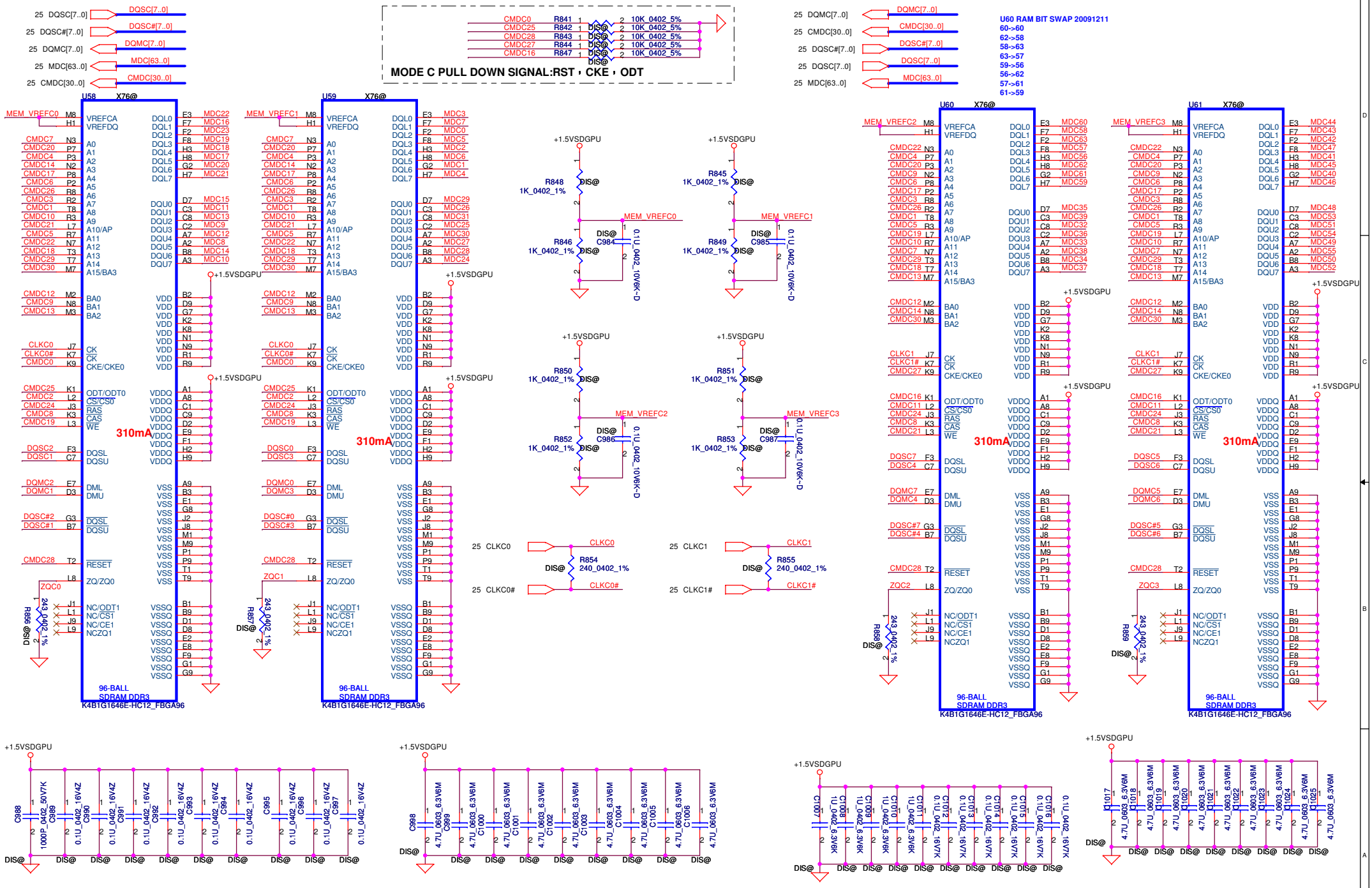
Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

Compal Electronics, Inc.

Title: N11P-GV2H gDDR3

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev:

Date: Tuesday, December 22, 2009 | Sheet 26 of 56



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

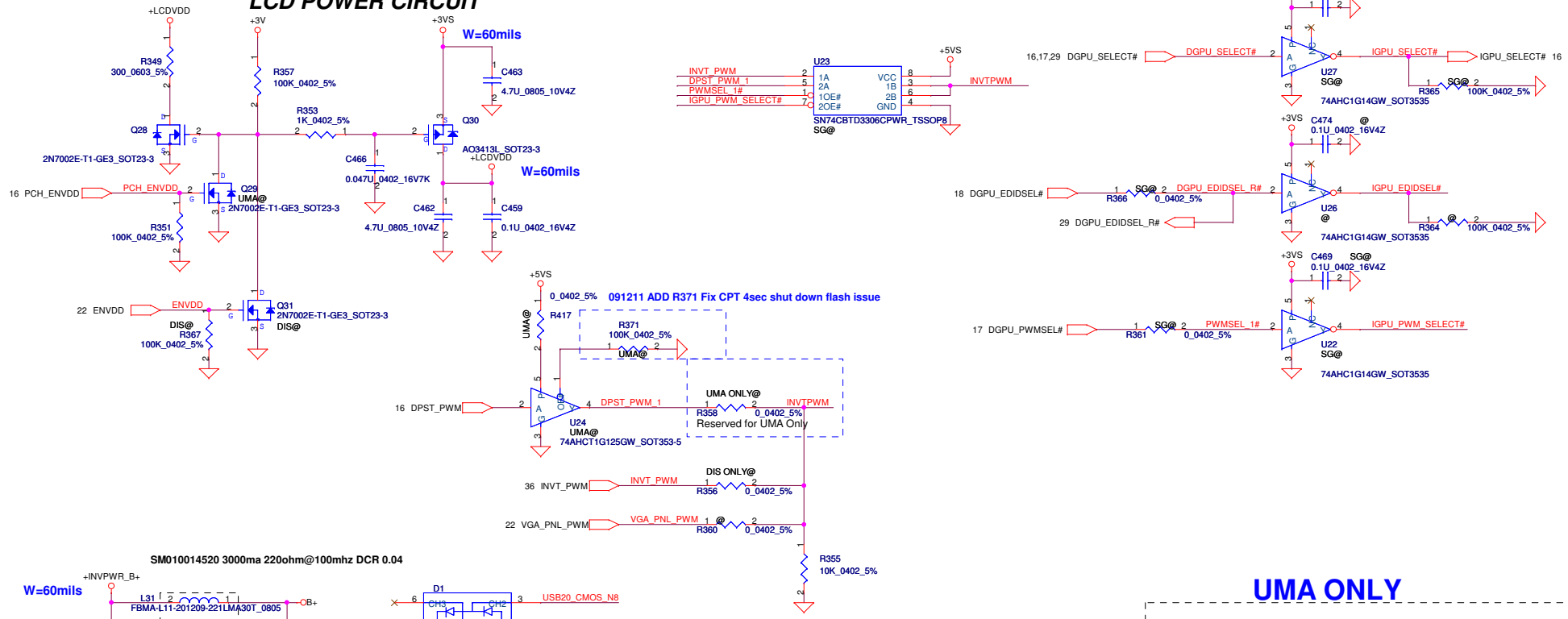
Compal Electronics, Inc.

Title: N11P-GV2H gDDR3

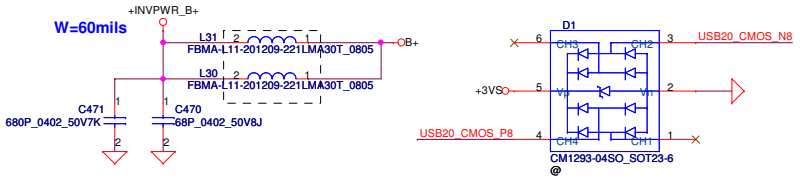
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 27 of 56

LCD POWER CIRCUIT



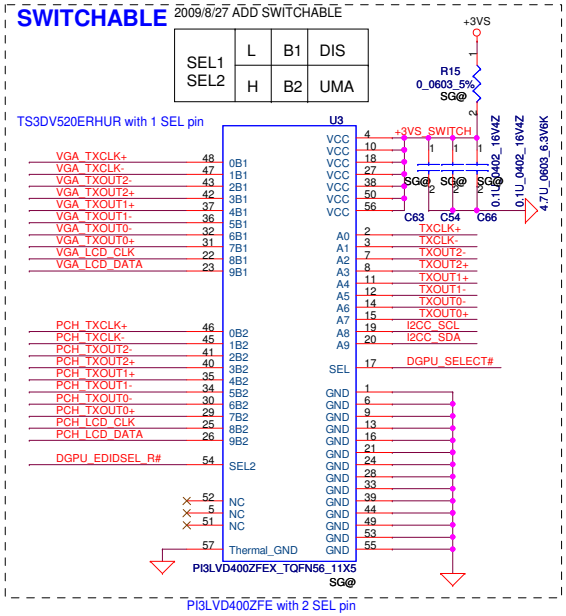
SM010014520 3000ma 220ohm@100mhz DCR 0.04



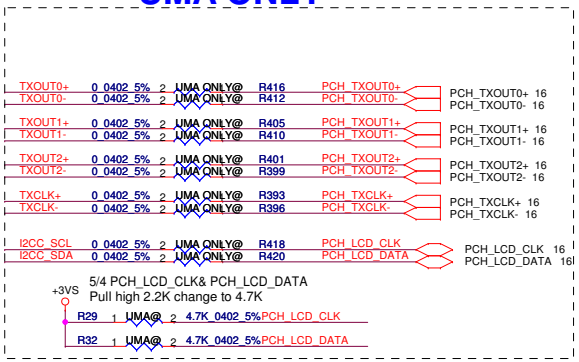
SWITCHABLE

2009/8/27 ADD SWITCHABLE

SEL1 SEL2	L	B1	DIS
	H	B2	UMA

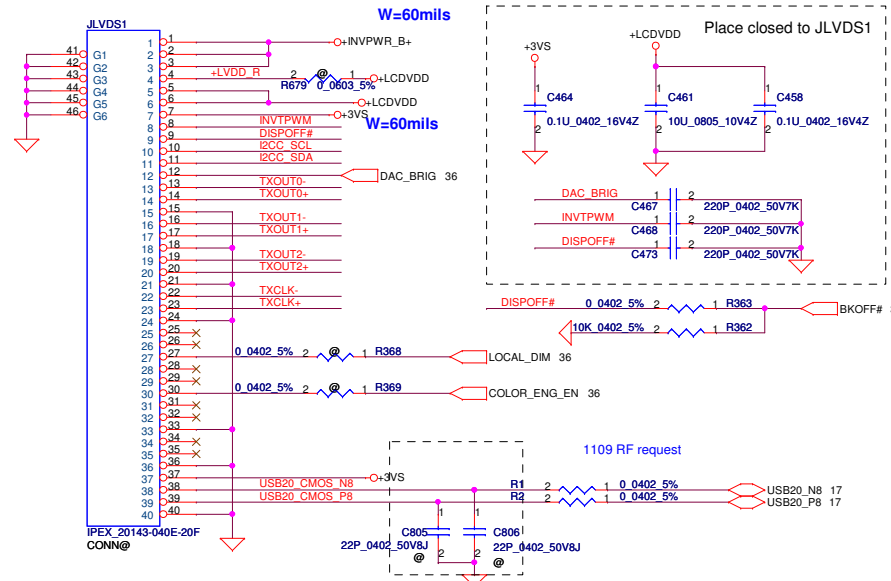


UMA ONLY



Discrete ONLY

LCD/LED PANEL Conn.



Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

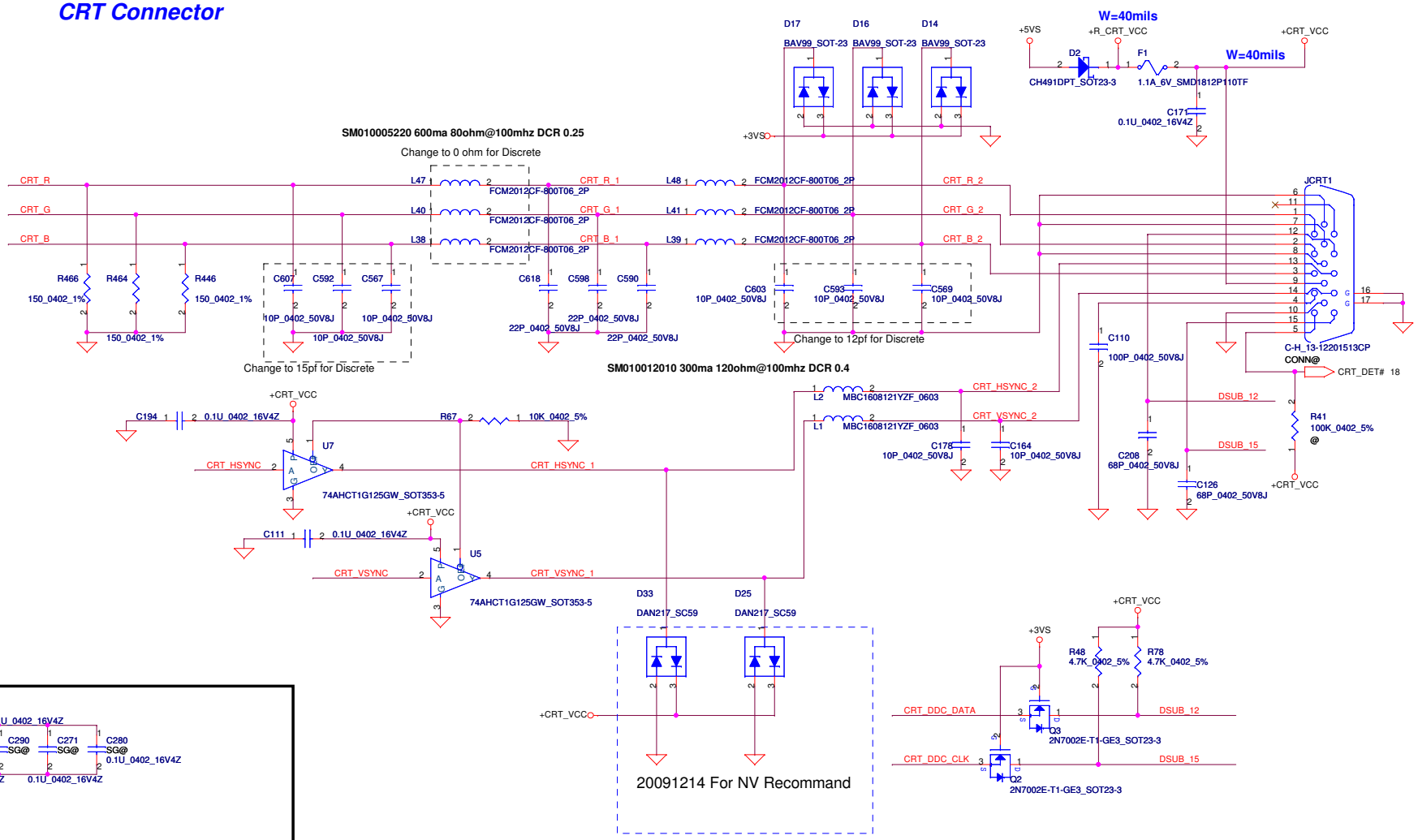
Compal Electronics, Inc.

Title: LVDS Connector

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

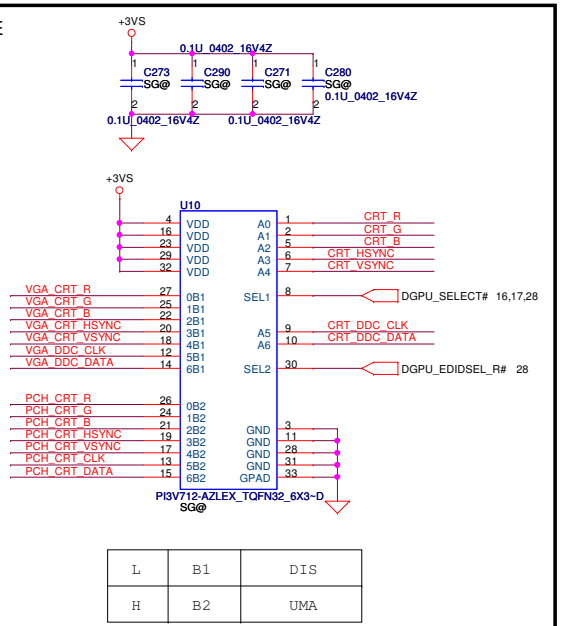
Date: Tuesday, December 22, 2009 | Sheet 28 of 56

CRT Connector



SWITCHABLE

2009/08/27



L	B1	DIS
H	B2	UMA

Discrete only

22 VGA_CRT_R — VGA_CRT_R — R537 2 DIS ONLY@ 0_0402_5% — CRT_R
22 VGA_CRT_G — VGA_CRT_G — R535 2 DIS ONLY@ 0_0402_5% — CRT_G
22 VGA_CRT_B — VGA_CRT_B — R533 2 DIS ONLY@ 0_0402_5% — CRT_B
22 VGA_CRT_HSYNC — VGA_CRT_HSYNC — R531 2 DIS ONLY@ 0_0402_5% — CRT_HSYNC
22 VGA_CRT_VSYNC — VGA_CRT_VSYNC — R529 2 DIS ONLY@ 0_0402_5% — CRT_VSYNC
22 VGA_DDC_CLK — VGA_DDC_CLK — R527 2 DIS ONLY@ 0_0402_5% — CRT_DDC_CLK
22 VGA_DDC_DATA — VGA_DDC_DATA — R526 2 DIS ONLY@ 0_0402_5% — CRT_DDC_DATA

VGA_DDC_DATA and VGA_DDC_CLK Pull high at Page22

UMA only

16 PCH_CRT_R — PCH_CRT_R — R536 2 UMA ONLY@ 0_0402_5% — CRT_R
16 PCH_CRT_G — PCH_CRT_G — R534 2 UMA ONLY@ 0_0402_5% — CRT_G
16 PCH_CRT_B — PCH_CRT_B — R532 2 UMA ONLY@ 0_0402_5% — CRT_B
16 PCH_CRT_HSYNC — PCH_CRT_HSYNC — R530 2 UMA ONLY@ 0_0402_5% — CRT_HSYNC
16 PCH_CRT_VSYNC — PCH_CRT_VSYNC — R528 2 UMA ONLY@ 0_0402_5% — CRT_VSYNC
16 PCH_CRT_CLK — PCH_CRT_CLK — R544 2 UMA ONLY@ 0_0402_5% — CRT_DDC_CLK
16 PCH_CRT_DATA — PCH_CRT_DATA — R543 2 UMA ONLY@ 0_0402_5% — CRT_DDC_DATA

PCH DDC PU 2.2K on Page 17

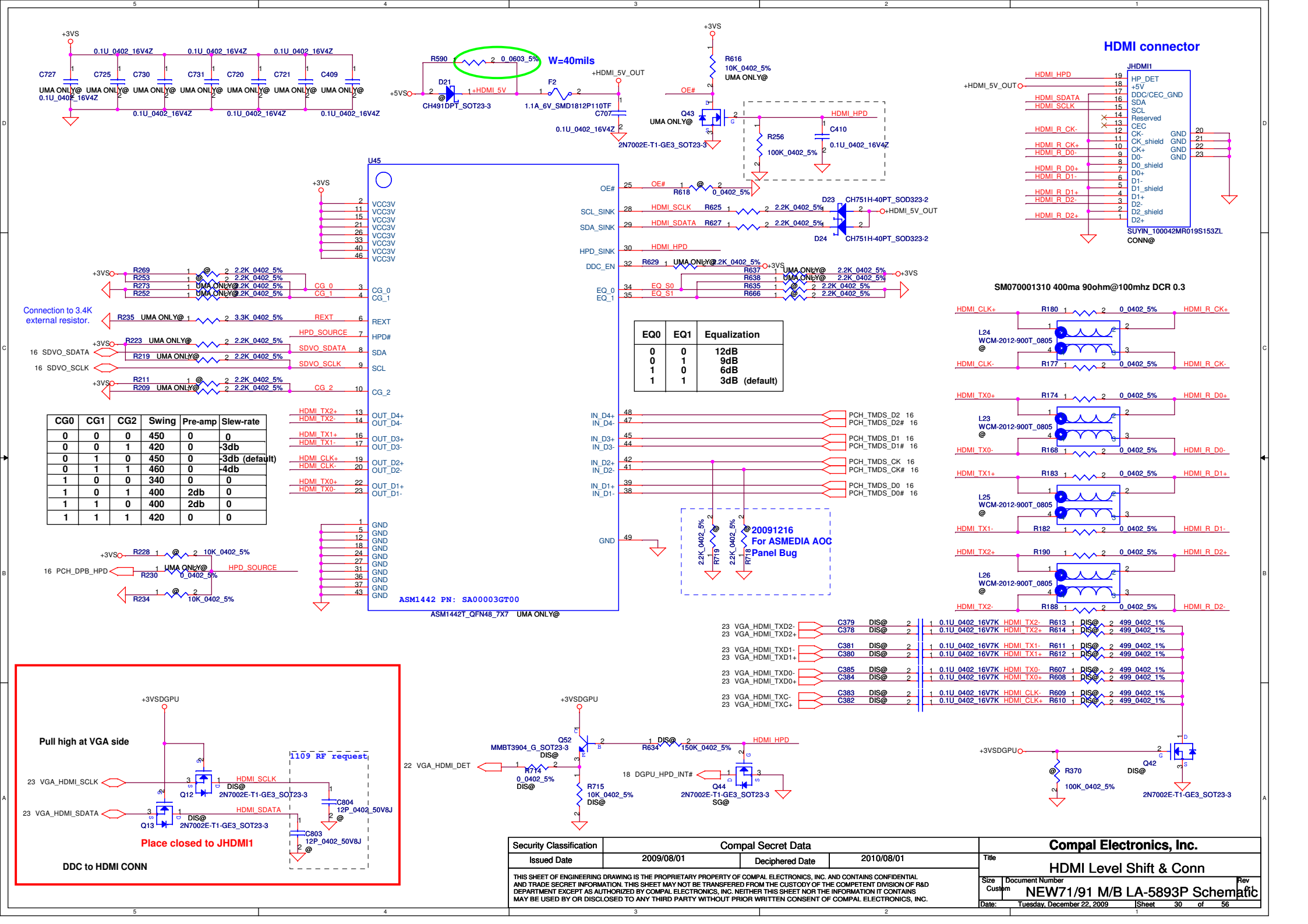
Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: CRT Connector

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 29 of 56



EQ0	EQ1	Equalization
0	0	12dB
0	1	9dB
1	0	6dB
1	1	3dB (default)

CG0	CG1	CG2	Swing	Pre-amp	Slew-rate
0	0	0	450	0	0
0	0	1	420	0	-3db
0	1	0	450	0	-3db (default)
0	1	1	460	0	-4db
1	0	0	340	0	0
1	0	1	400	2db	0
1	1	0	400	2db	0
1	1	1	420	0	0

Security Classification	Compal Secret Data		
Issued Date	2009/08/01	Deciphered Date	2010/08/01

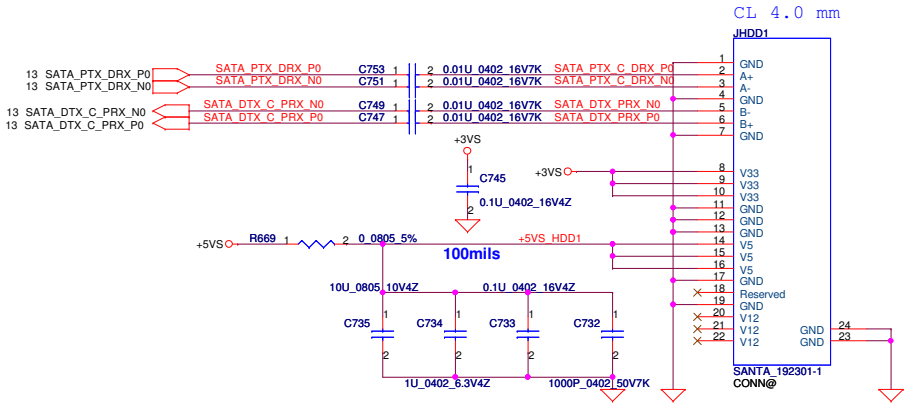
Compal Electronics, Inc.

Title: HDMI Level Shift & Conn

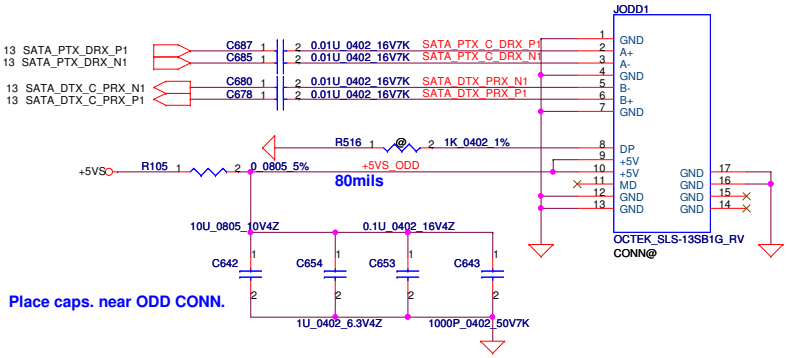
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 30 of 56

SATA HDD1 Conn.



SATA ODD Conn.



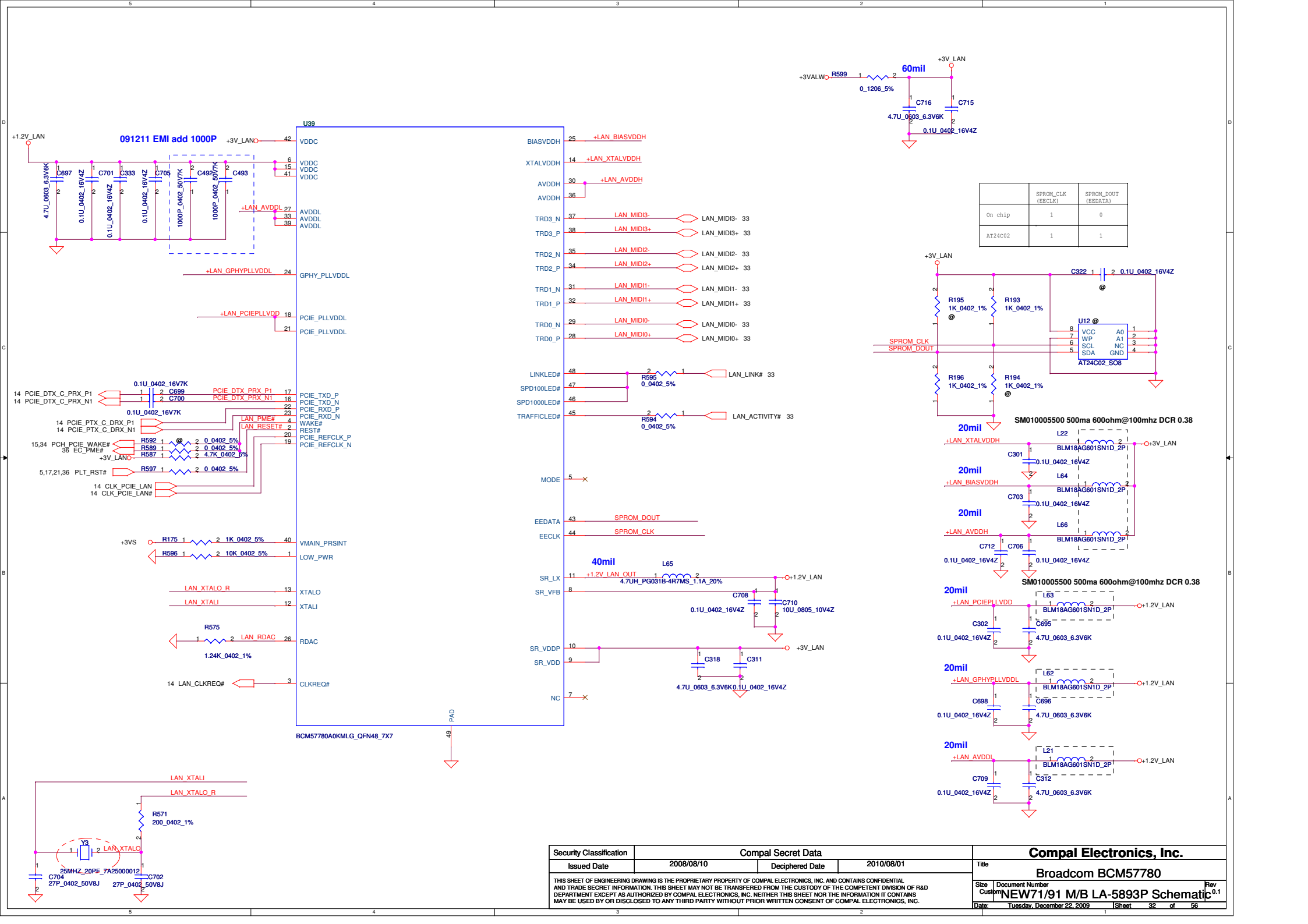
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 31 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

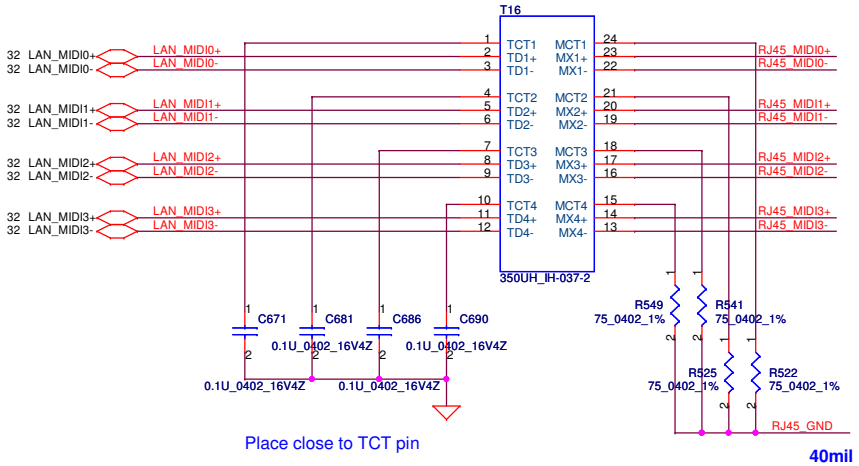
Compal Electronics, Inc.

Title: Broadcom BCM57780

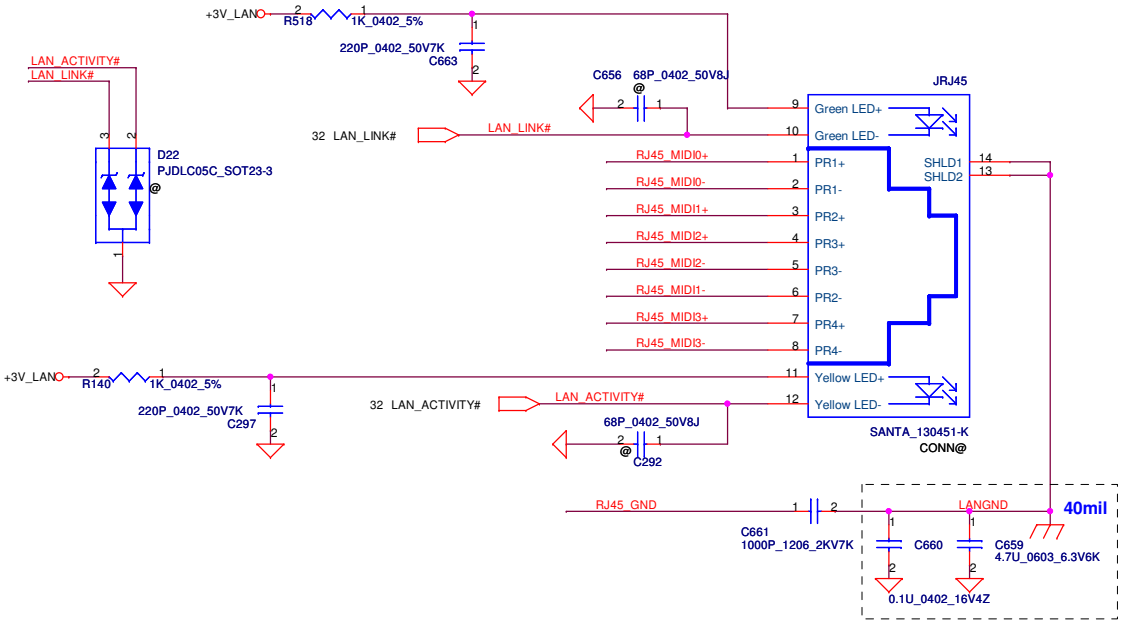
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 32 of 56

LAN Connector



BOTHHAND: S X'FORM_ GST5009-D LF LAN, SP050006B00
TIMAG:S X'FORM_ IH-160 LAN , SP050006F00



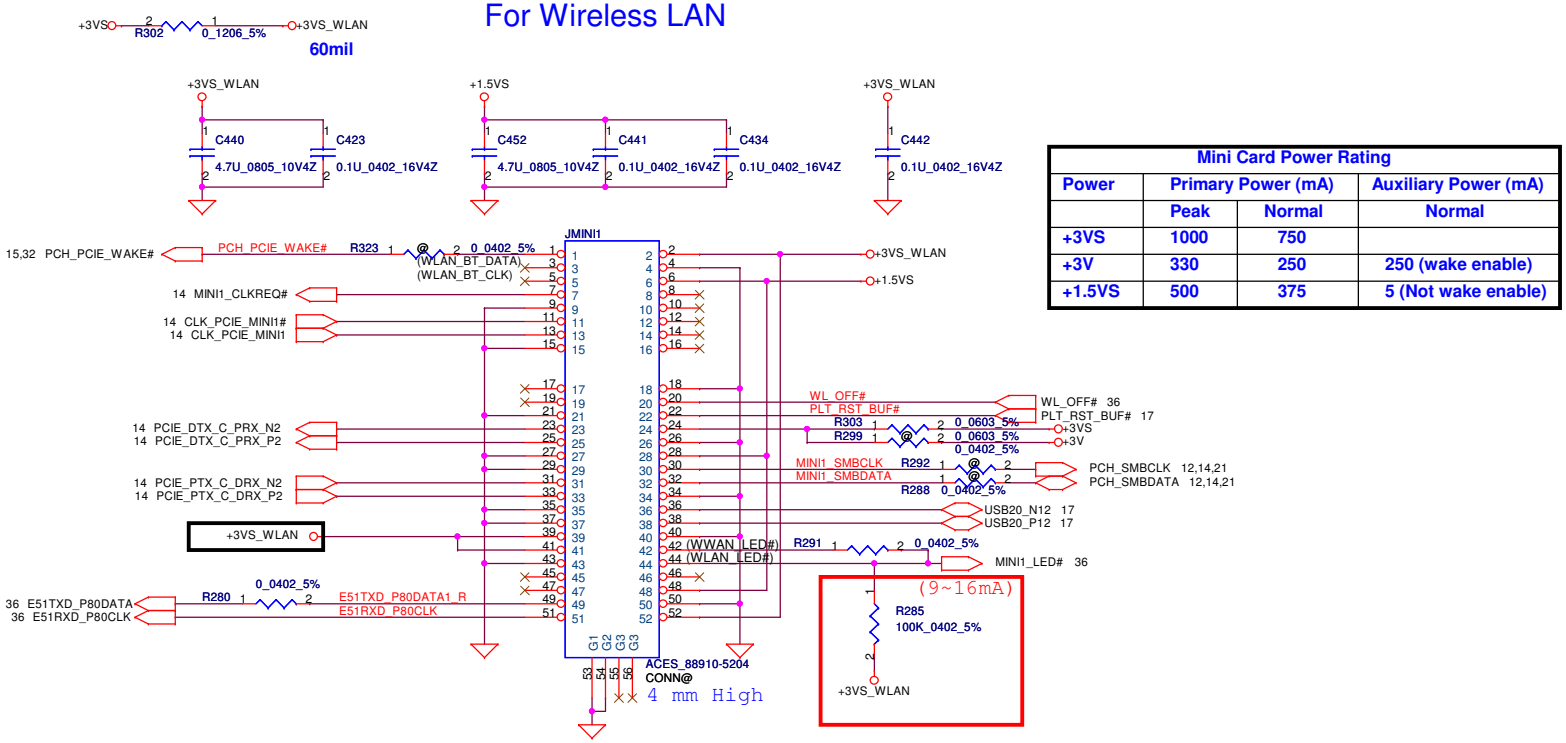
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

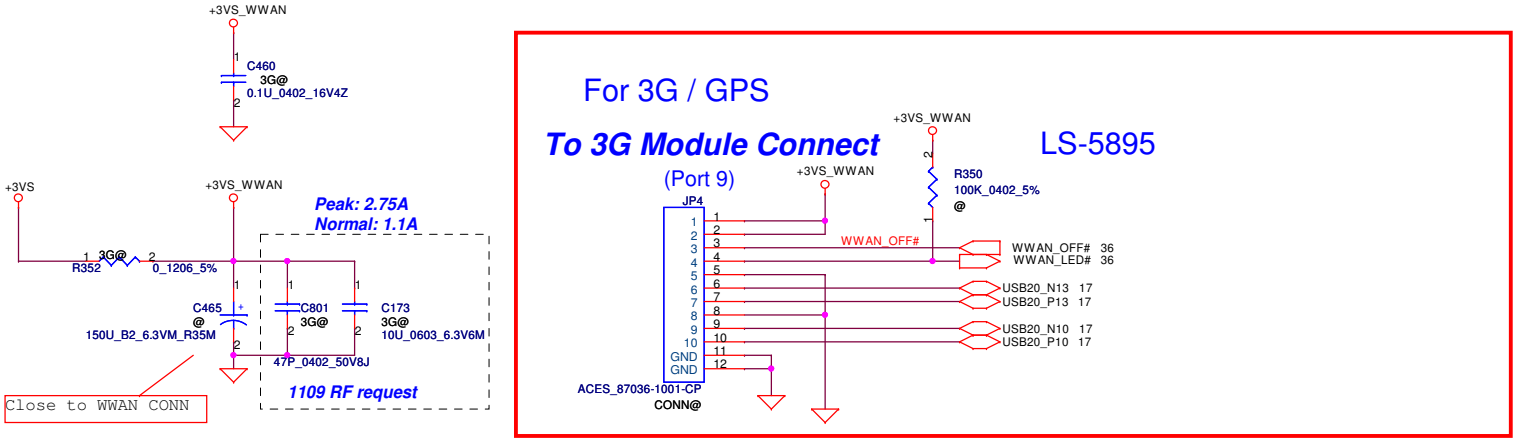
Title: LAN Magnetic & RJ45

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 33 of 56



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

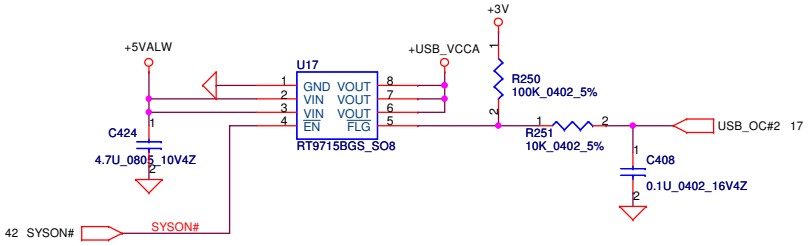


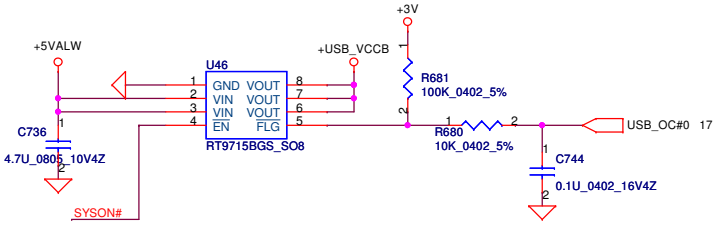
Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

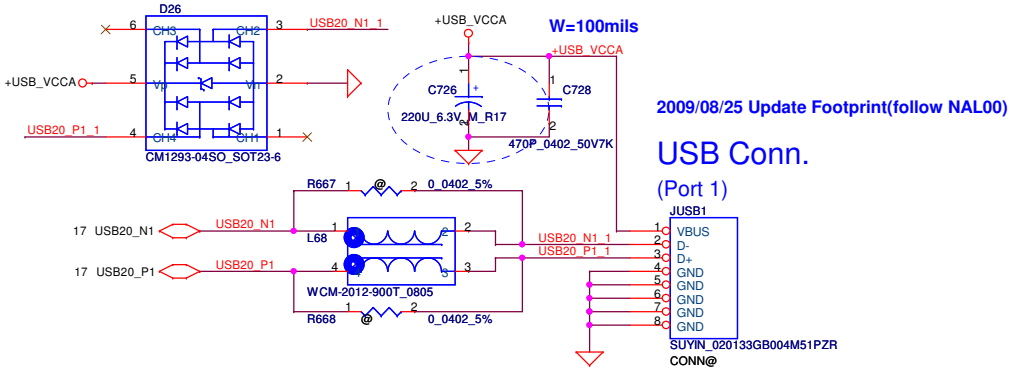
Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 34 of 56





2009/08/14 CHANGE cap



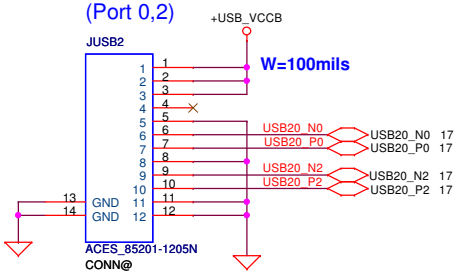
2009/08/25 Update Footprint(follow NAL00)

USB Conn.

(Port 1)

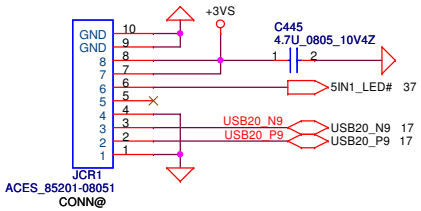
USB/B Conn. LS-5891

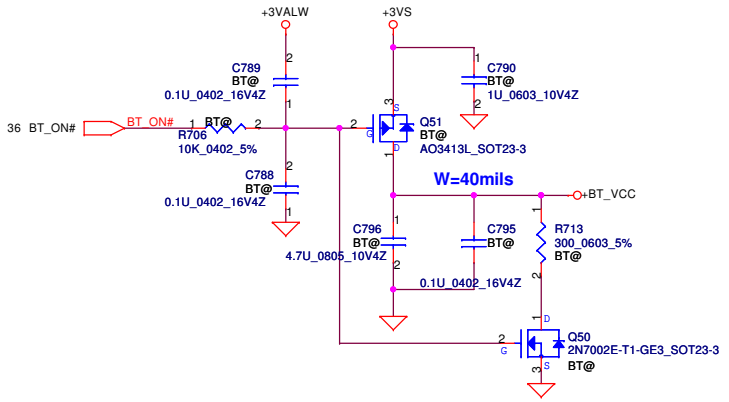
(Port 0,2)



2009/08/24 CHANGE Conn to FFC Type

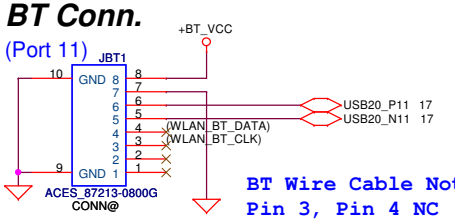
Card Reader Conn. LS-5896





BT Conn.

(Port 11)



BT Wire Cable Note:
Pin 3, Pin 4 NC

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: USB / BT / USBB

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Thursday, December 24, 2009 | Sheet 35 of 56

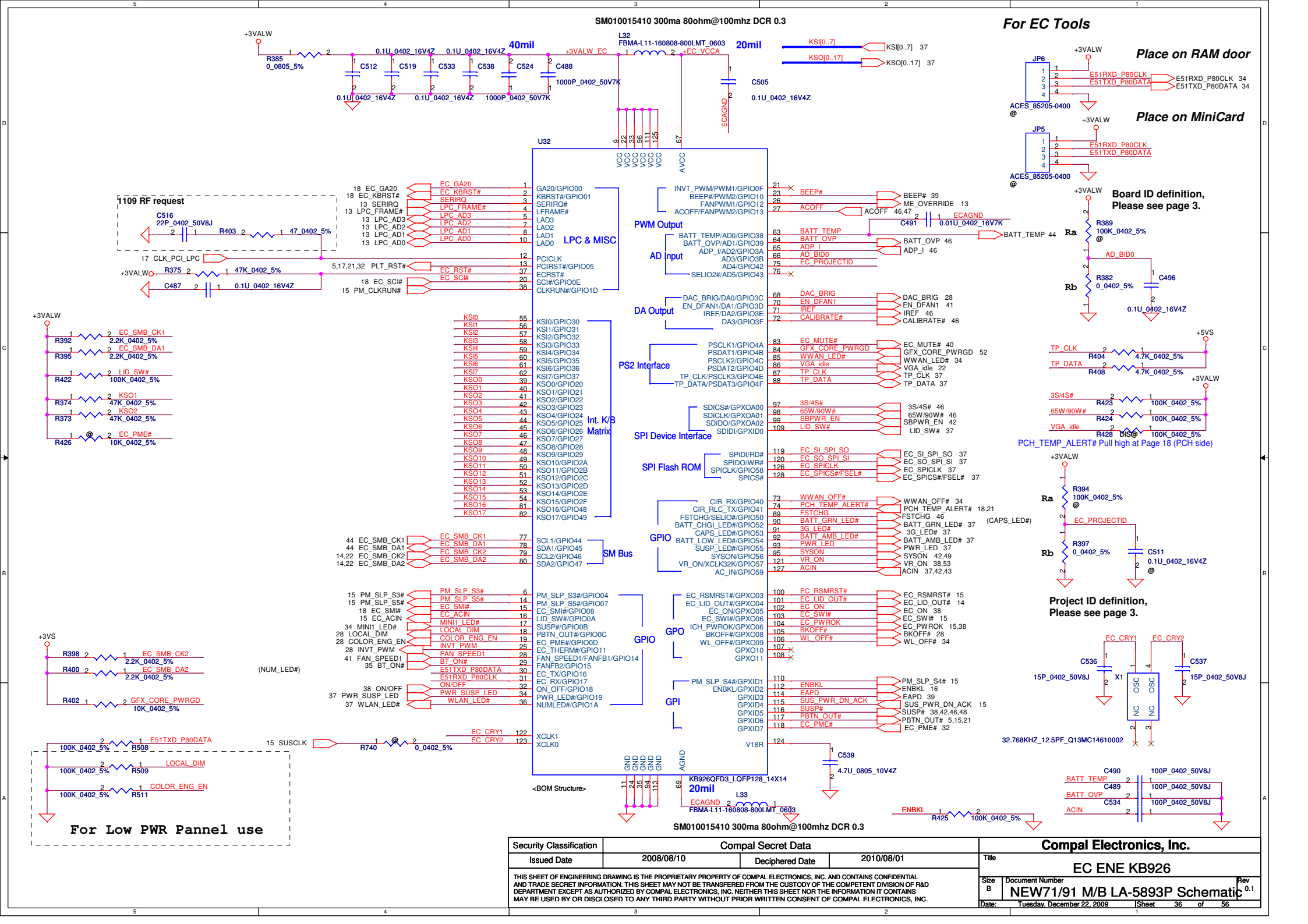
SM010015410 300ma 80ohm@100mhz DCR 0.3

For EC Tools

Place on RAM door

Place on MiniCard

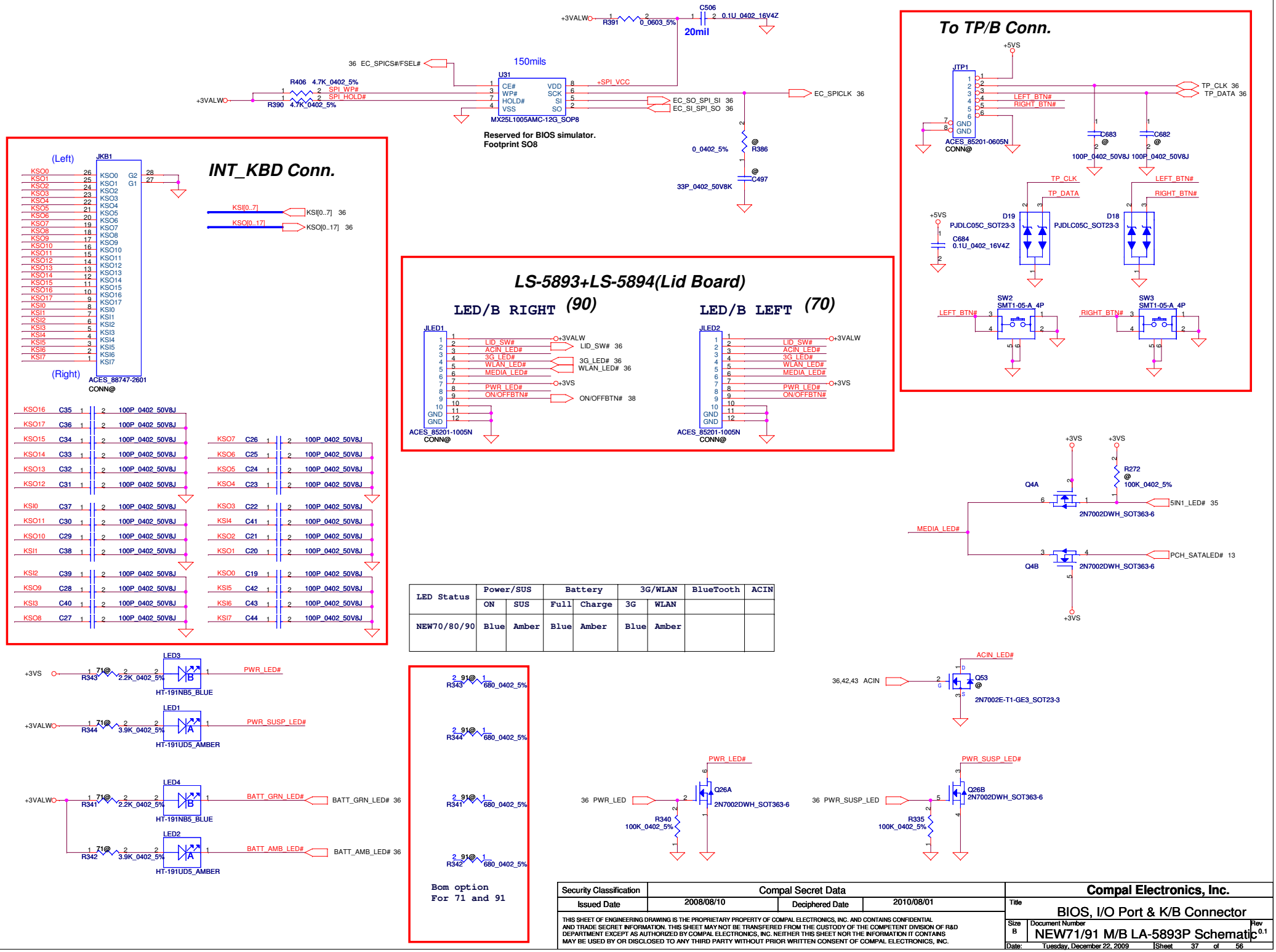
U32 — KB926QFD3_LQFP128_14X14



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title	EC ENE KB926
Size	B
Document Number	NEW71/91 M/B LA-5893P Schematic
Rev	0.1
Date:	Tuesday, December 22, 2009
Sheet	36 of 56



LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
NEW70/80/90	Blue	Amber	Blue	Amber	Blue	Amber		

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

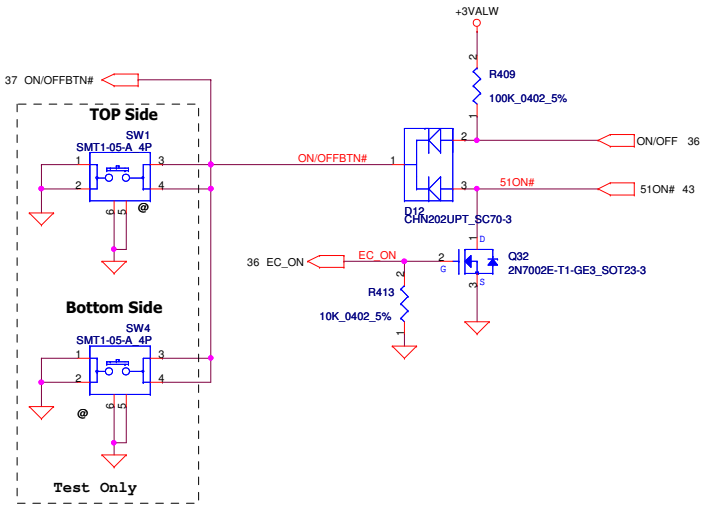
Title: BIOS, I/O Port & K/B Connector

Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

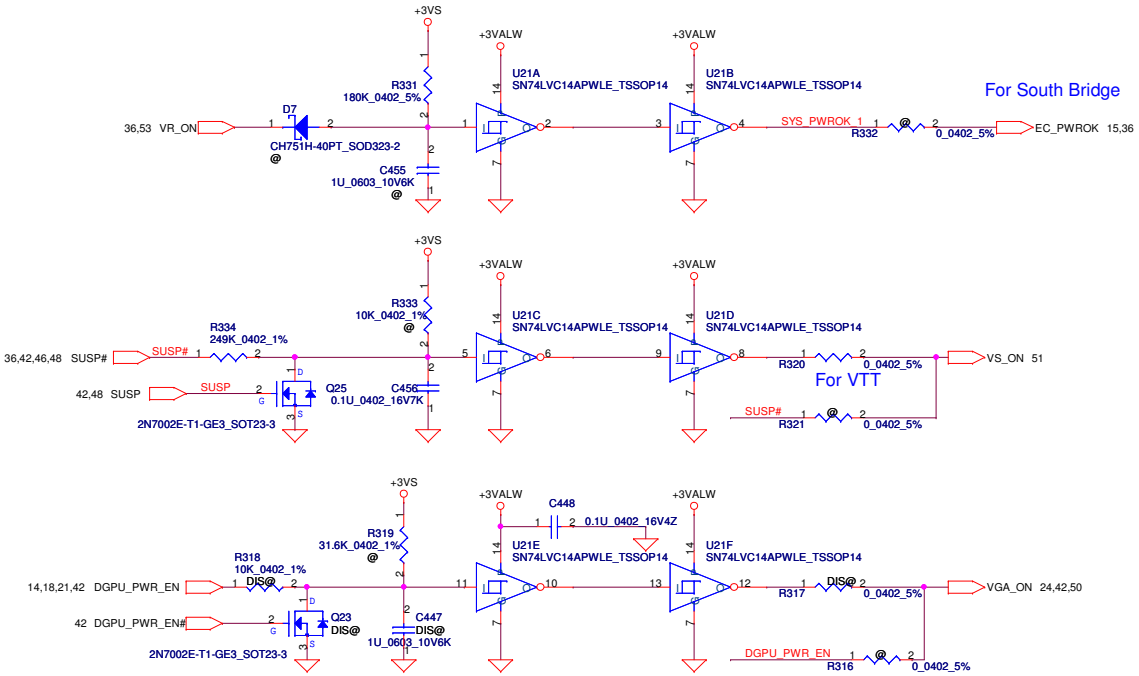
Date: Tuesday, December 22, 2009 Sheet 37 of 56

Power Button

ON/OFF switch



Power ON Circuit



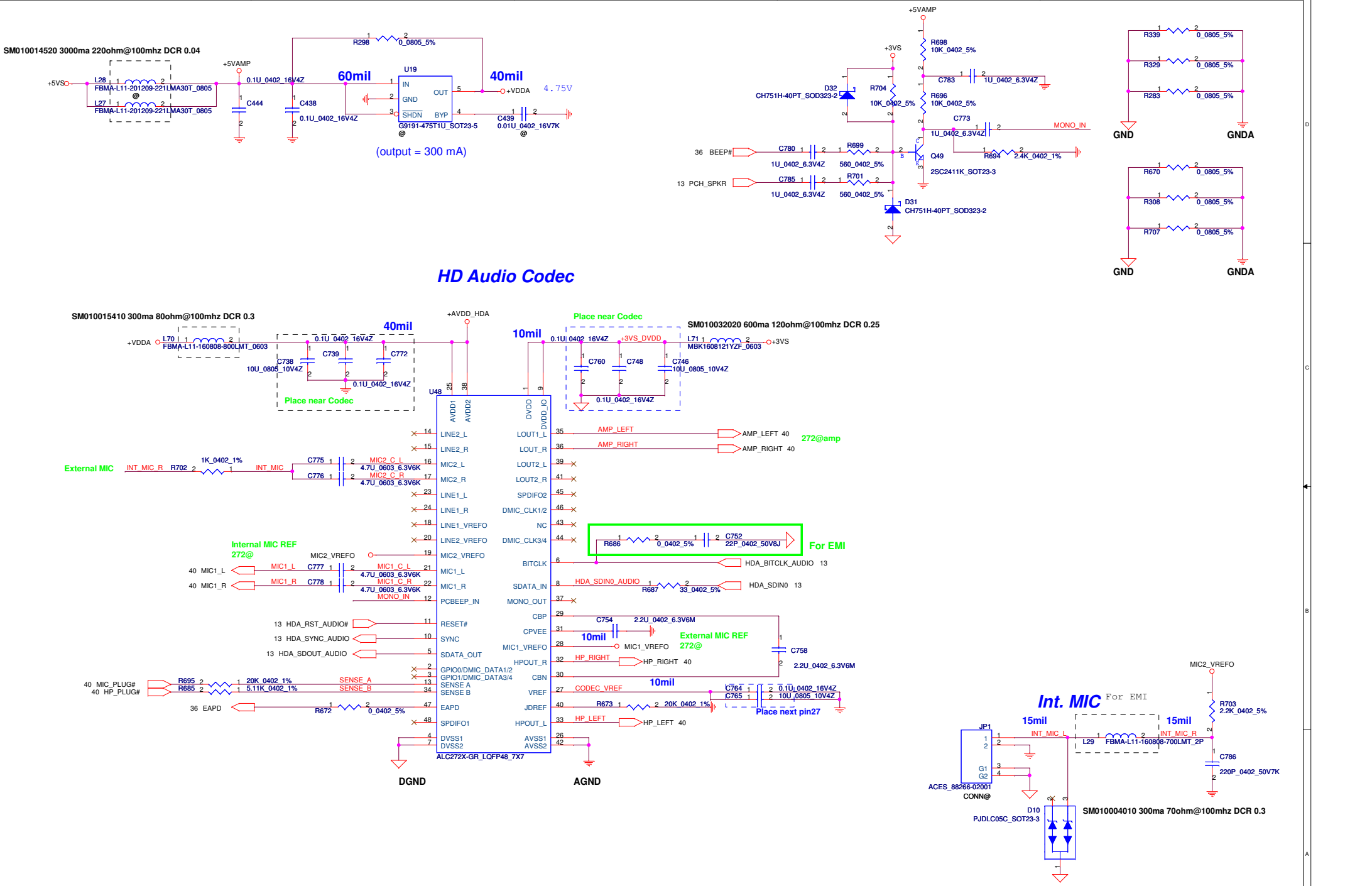
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: Power OK

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 38 of 56



Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

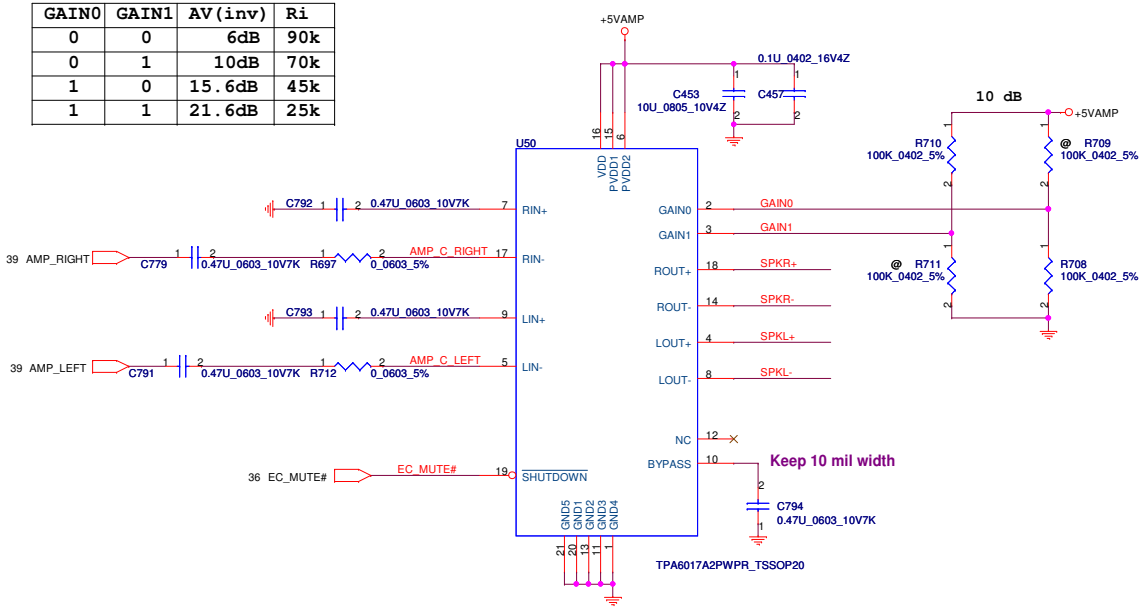
Compal Electronics, Inc.

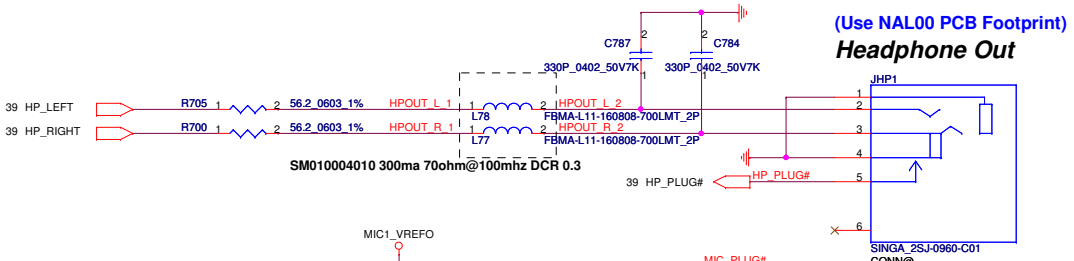
Title: HD Audio Codec ALC272X

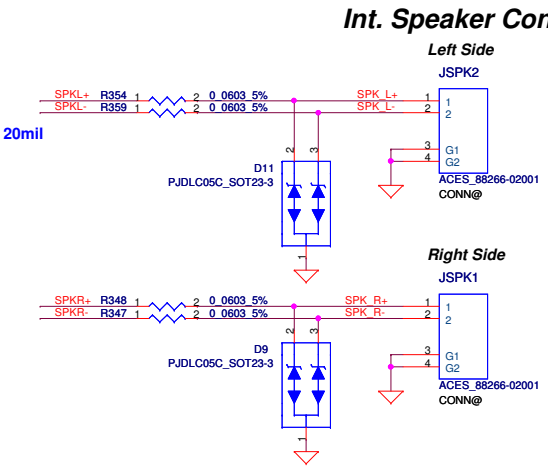
Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5893P Schematic	0.1

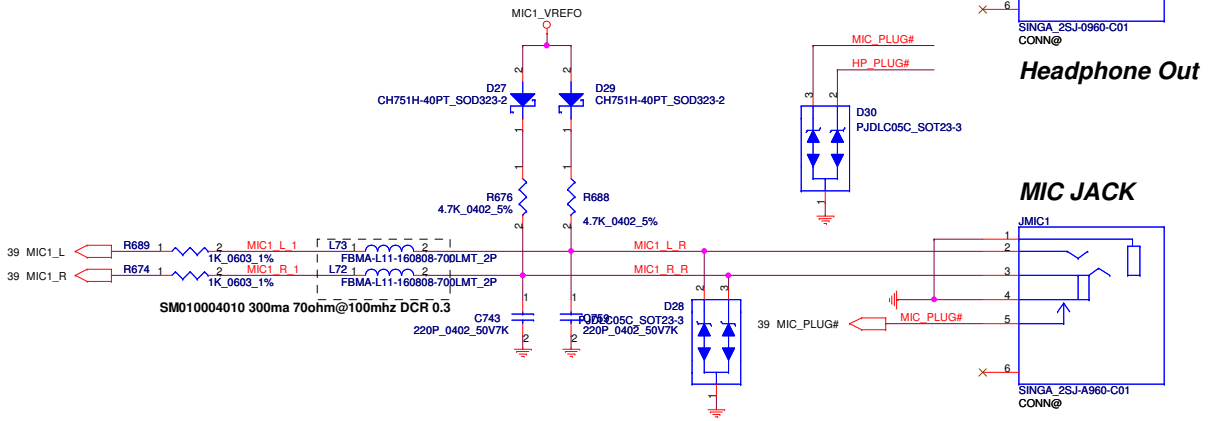
Date: Tuesday, December 22, 2009 | Sheet 39 of 56

GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k









Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

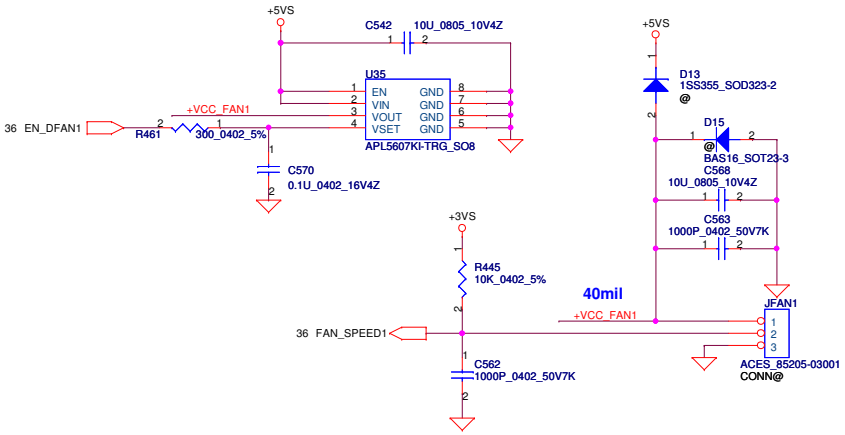
Compal Electronics, Inc.

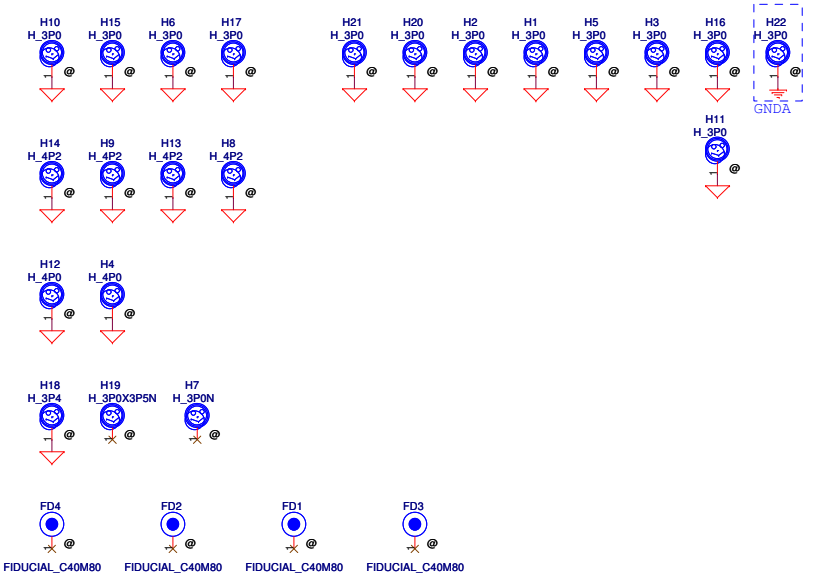
Title: Amplifier & Audio Jack

Size: Custom | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 40 of 56

FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

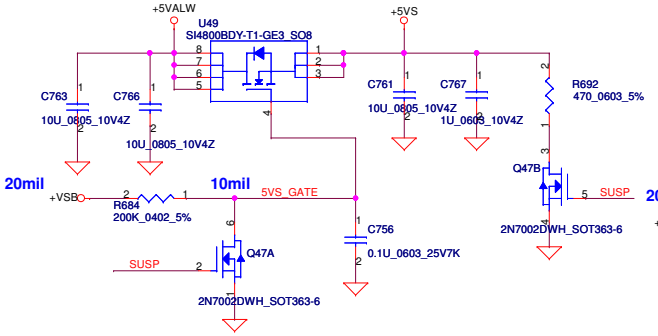
Compal Electronics, Inc.

Title: FAN & Screw Hole

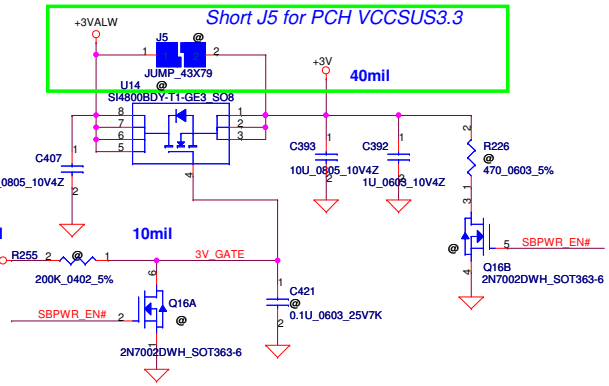
Size	Document Number	Rev
B	NEW71/91 M/B LA-5893P Schematic	0.1

Date: Tuesday, December 22, 2009 | Sheet 41 of 56

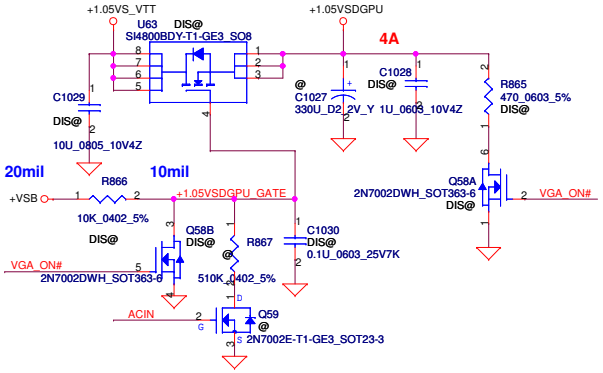
+5VALW TO +5VS



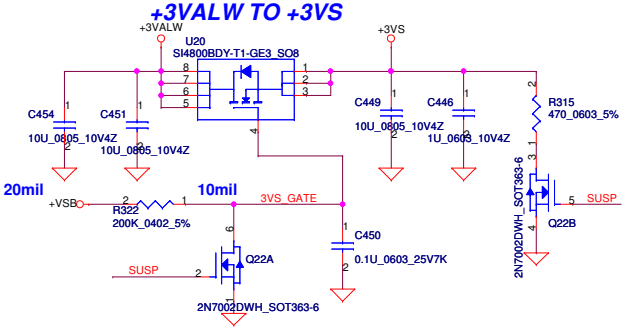
+3VALW TO +3V(PCH AUX Power)



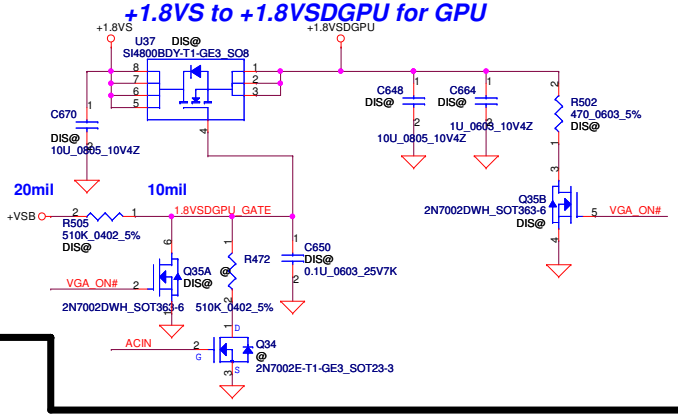
+1.05VS_VTT to +1.05VSDGPU for GPU

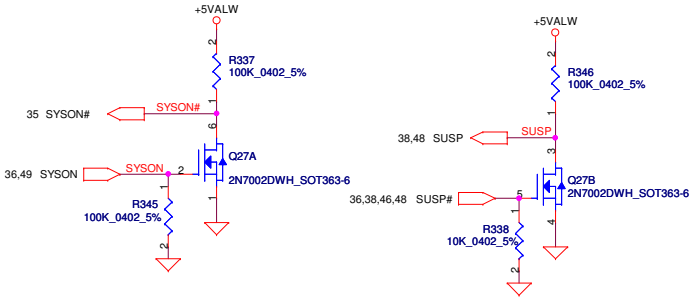


+3VALW TO +3VS



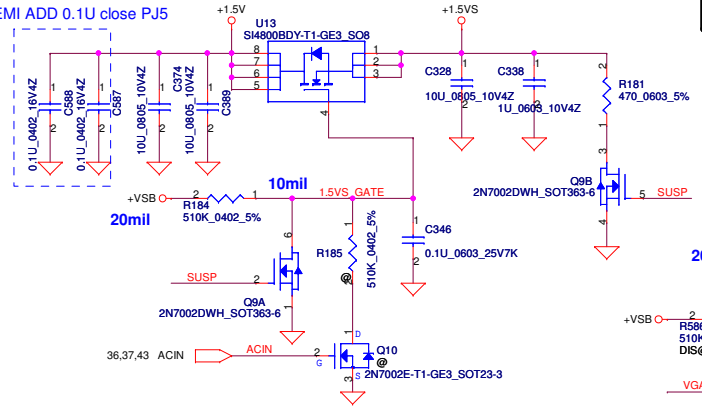
+1.8VS to +1.8VSDGPU for GPU



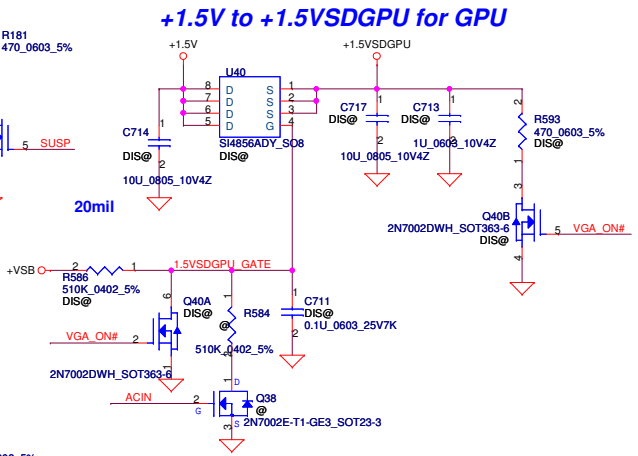


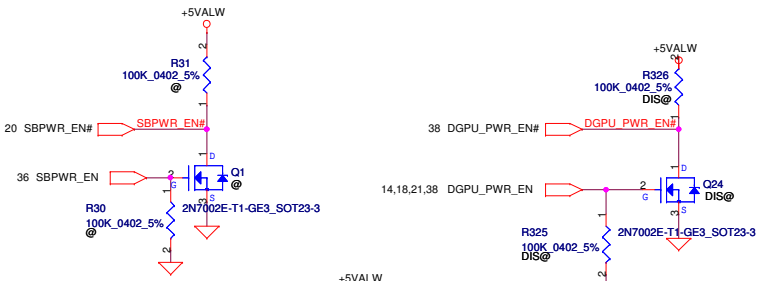
+1.5V to +1.5VS

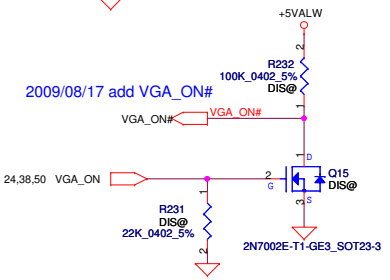
1211 EMI ADD 0.1U close PJ5

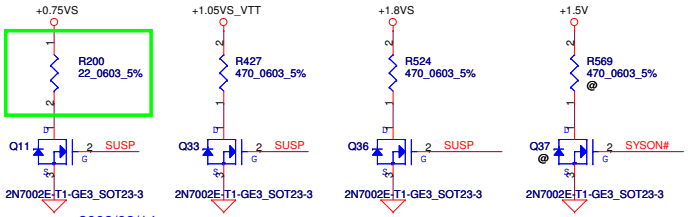


+1.5V to +1.5VSDGPU for GPU









2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

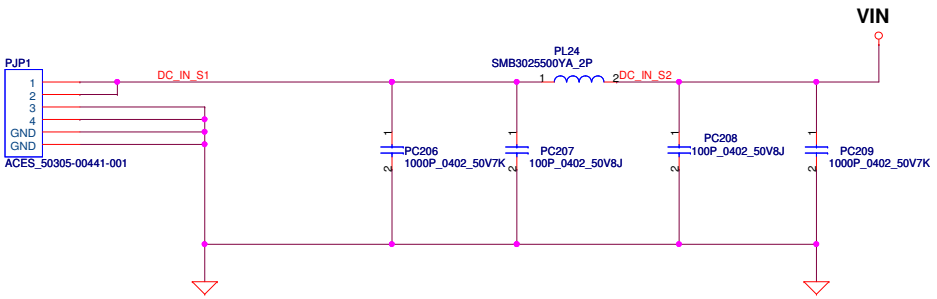
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

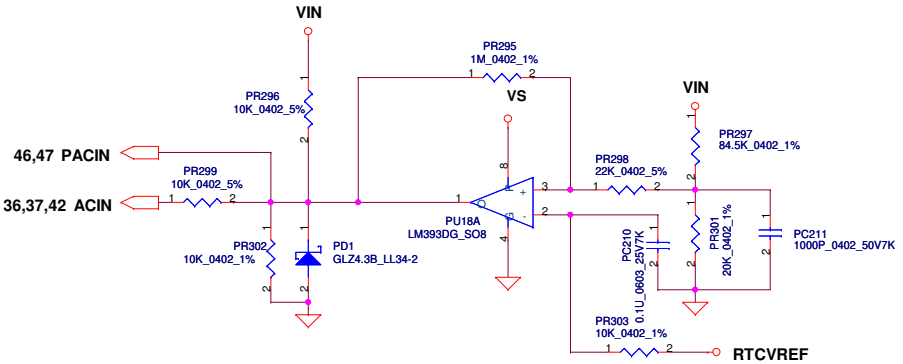
Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: NEW71/91 M/B LA-5893P Schematic | Rev: 0.1

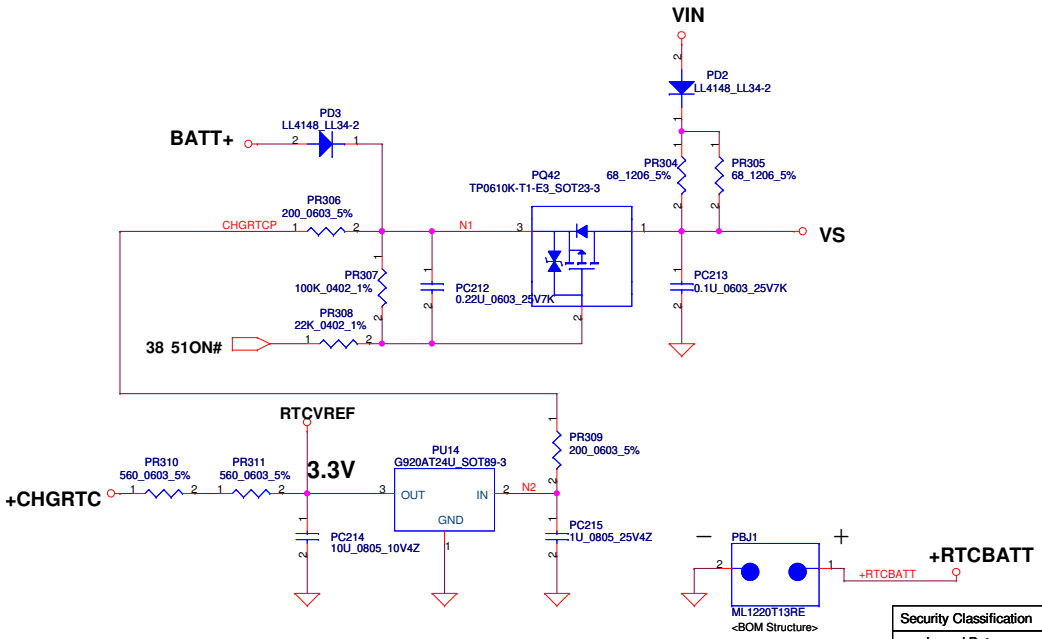
Date: Tuesday, December 22, 2009 | Sheet 42 of 56

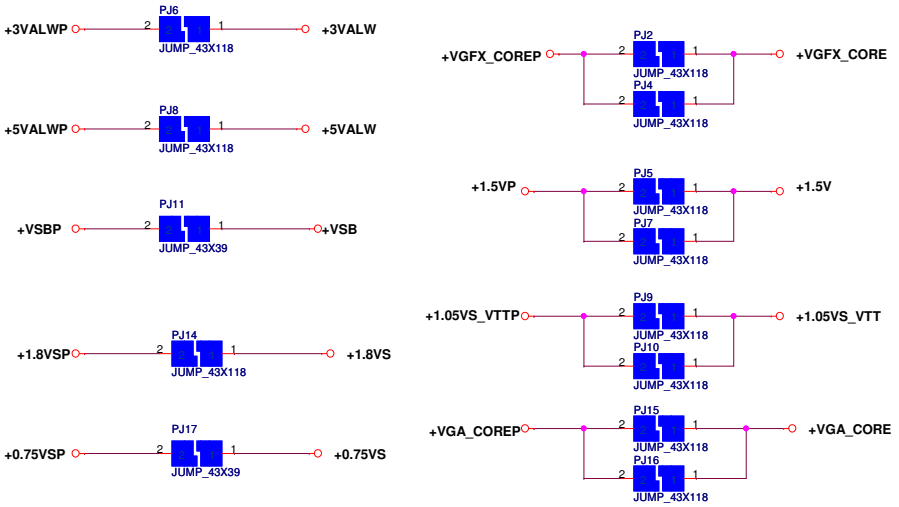




Vin Dectector

	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V





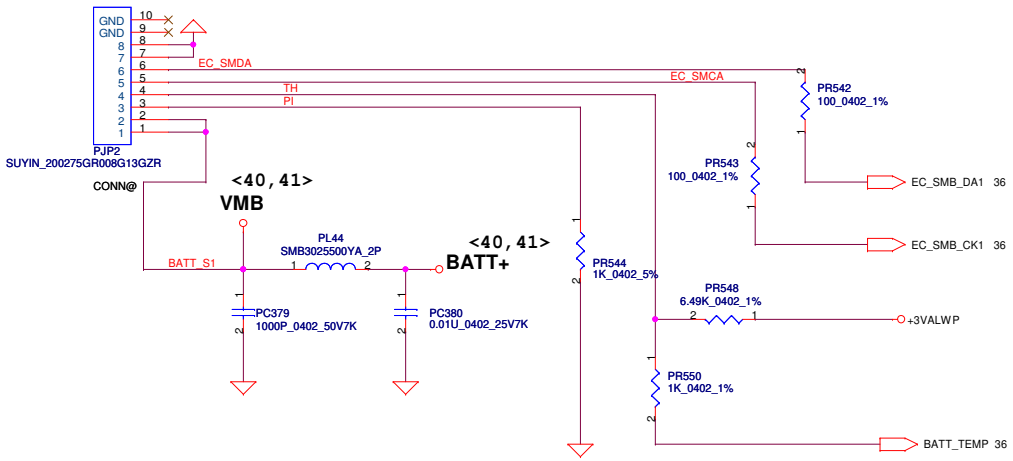
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

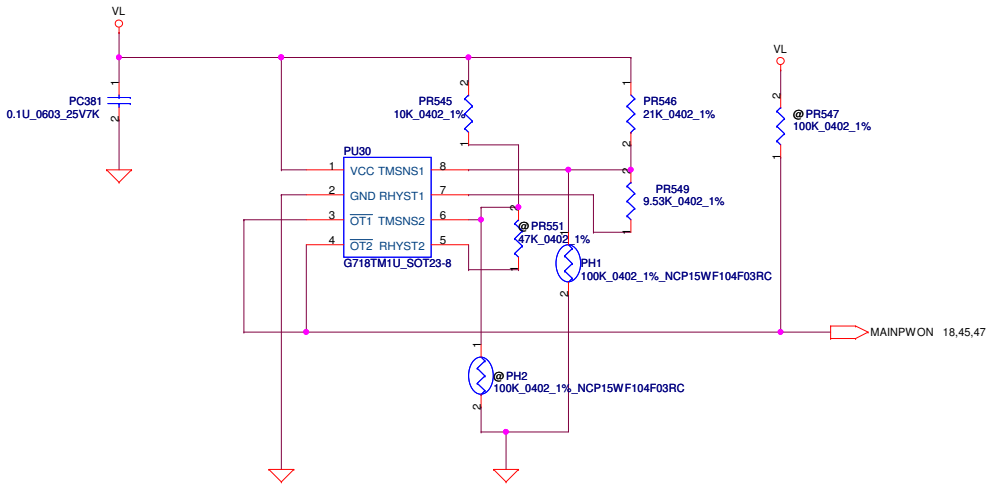
Size	Document Number	Rev
Custom	NEW71	0.1

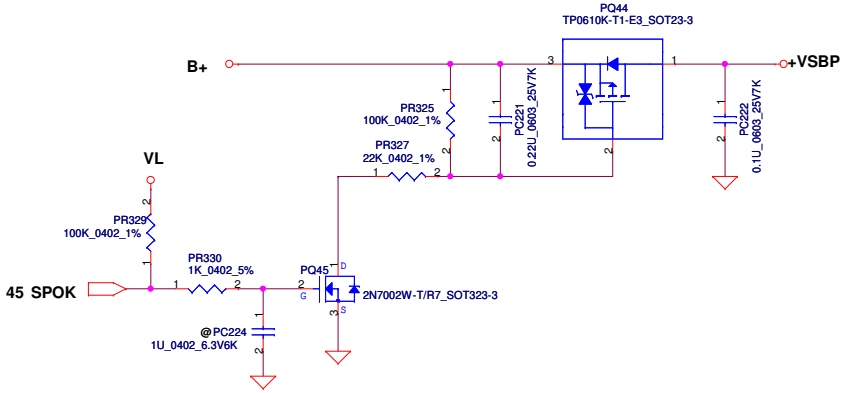
Date: Tuesday, December 22, 2009 | Sheet 43 of 56



PH1 under CPU botten side :

CPU thermal protection at 92 degree C





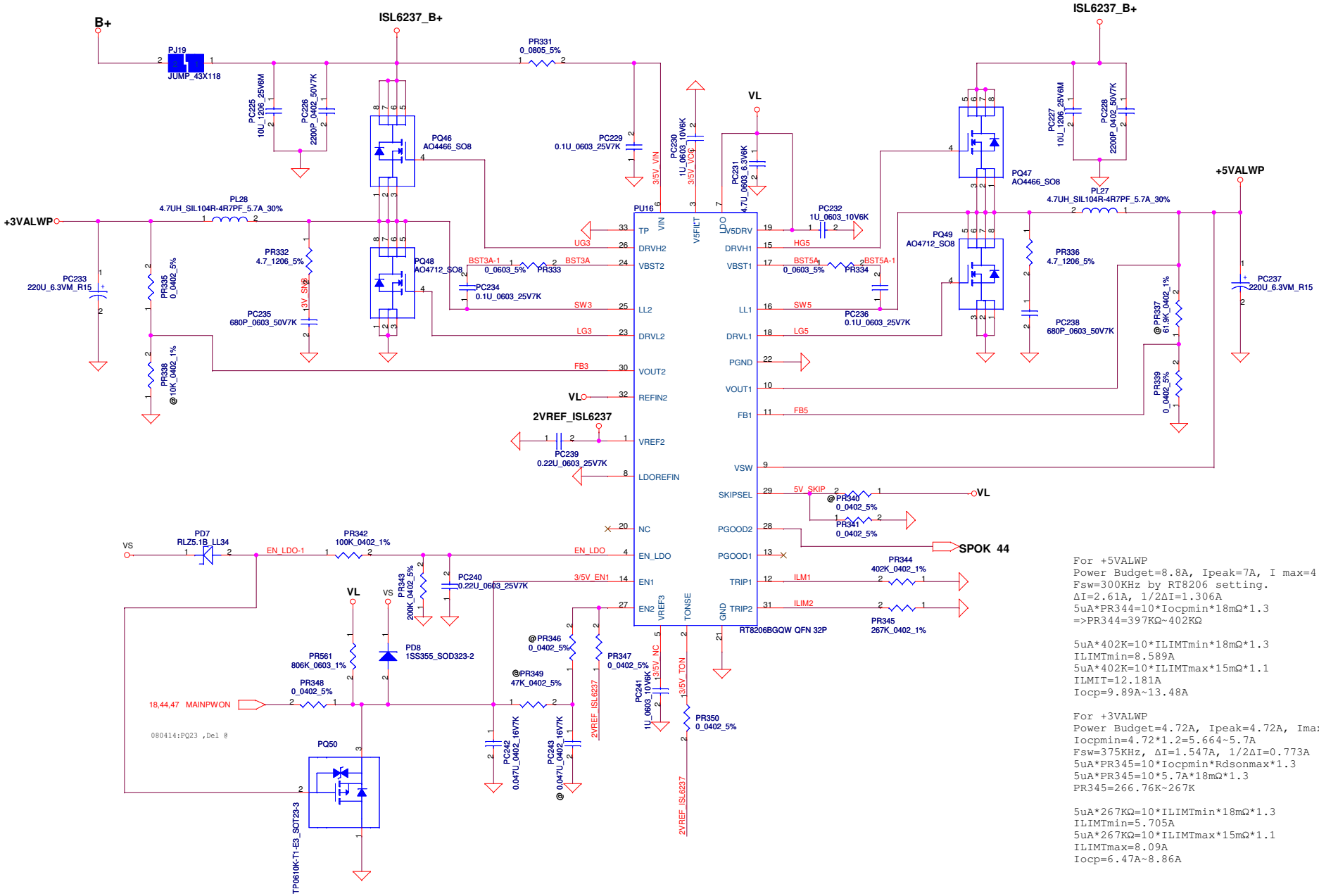
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 44 of 56



For +5VALWP
Power Budget=8.8A, Ipeak=7A, I max=4.9A
Fsw=300KHz by RT8206 setting.
ΔI=2.61A, 1/2ΔI=1.306A
5uA*PR344=10*Iocpmin*18mΩ*1.3
=>PR344=397KΩ~402KΩ

5uA*402K=10*ILIMTmin*18mΩ*1.3
ILIMTmin=8.589A
5uA*402K=10*ILIMTmax*15mΩ*1.1
ILMIT=12.181A
Iocp=9.89A~13.48A

For +3VALWP
Power Budget=4.72A, Ipeak=4.72A, Imax=4A
Iocpmin=4.72*1.2=5.664~5.7A
Fsw=375KHz, ΔI=1.547A, 1/2ΔI=0.773A
5uA*PR345=10*Iocpmin*Rdsonmax*1.3
5uA*PR345=10*5.7A*18mΩ*1.3
PR345=266.76K~267K

5uA*267KΩ=10*ILIMTmin*18mΩ*1.3
ILIMTmin=5.705A
5uA*267KΩ=10*ILIMTmax*15mΩ*1.1
ILIMTmax=8.09A
Iocp=6.47A~8.86A

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: 3VALW/5VALW

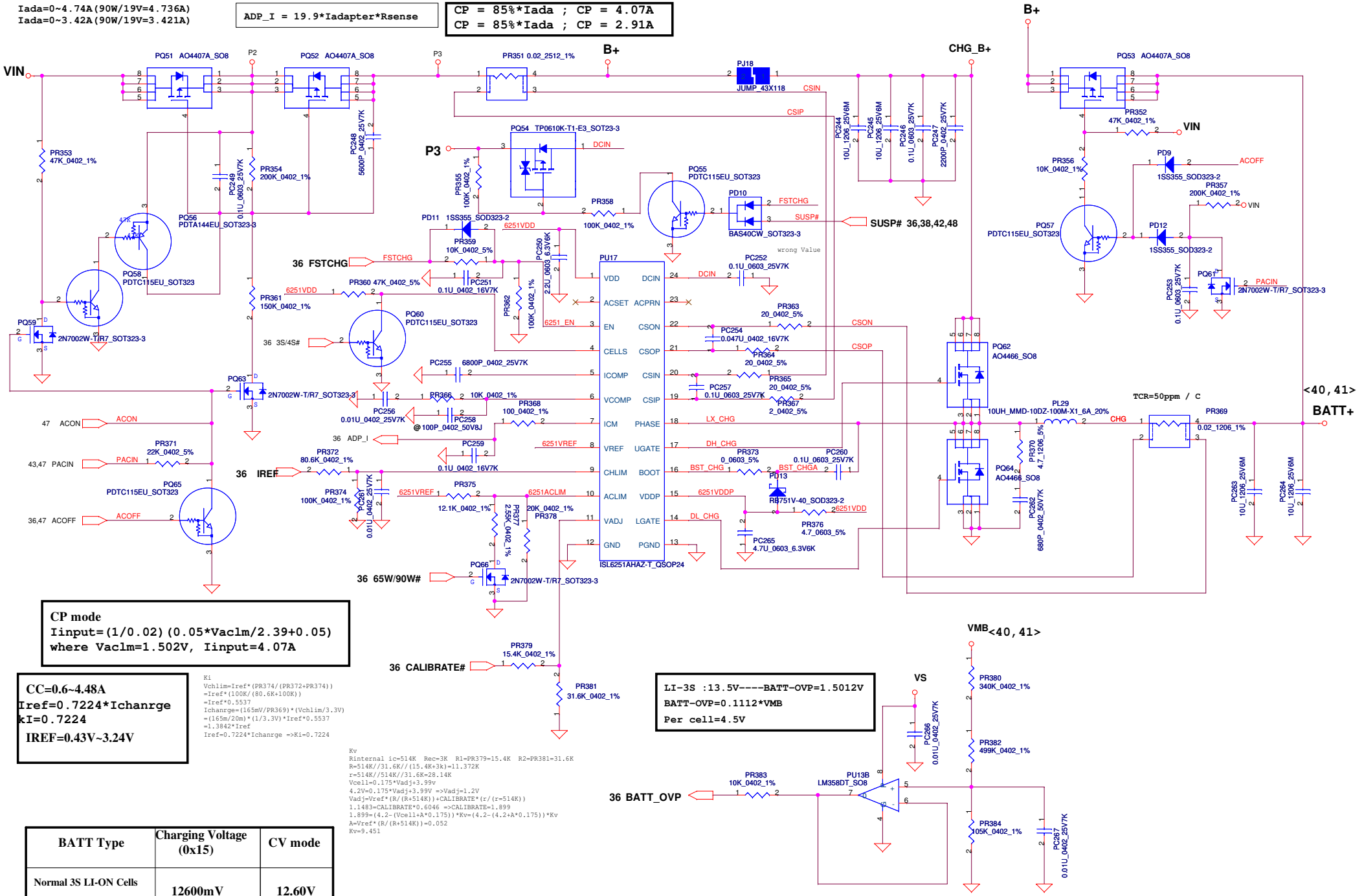
Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 45 of 56

Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A
Iref=0.7224*Ichanrge
kI=0.7224
IREF=0.43V~3.24V

Ki
Vchlim=Iref*(PR374/(PR372+PR374))
=Iref*(100K/(80.6K+100K))
=Iref*0.5537
Ichanrge=(165mV/PR369)*(Vchlim/3.3V)
=(165m/20m)*(1/3.3V)*Iref*0.5537
=1.3842*Iref
Iref=0.7224*Ichanrge =>Ki=0.7224

Kv
Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K
R=514K//31.6K//((15.4K+3k)=11.372K
r=514K//514K//31.6K=28.14K
Vcell=0.175*Vadj+3.99v
4.2V=0.175*Vadj+3.99V =>Vadj=1.2V
Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))
1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899
1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv
A=Vref*(R/(R+514K))=0.052
Kv=9.451

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

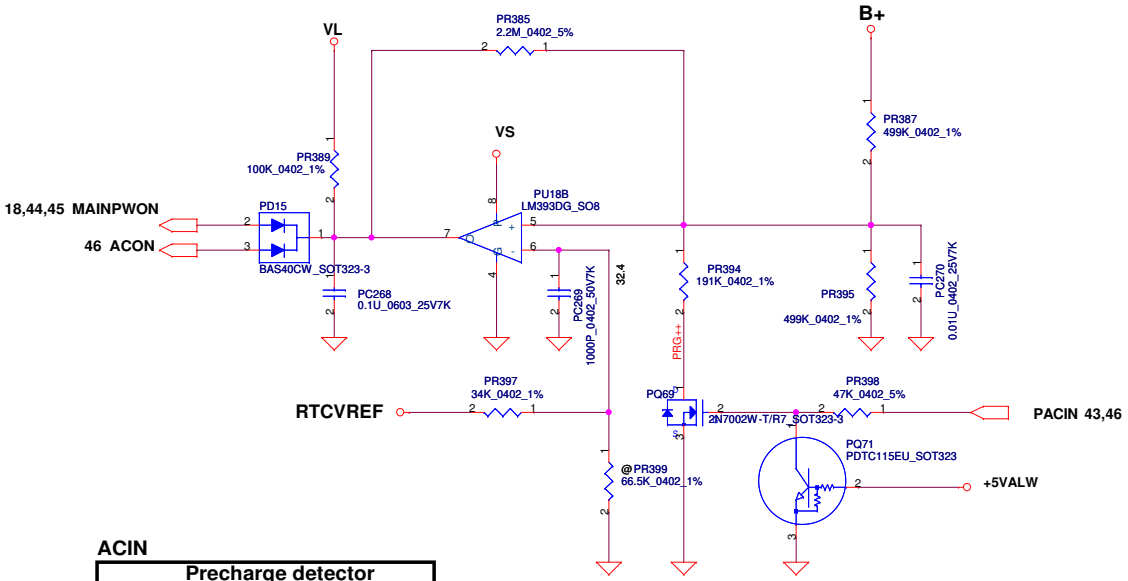
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

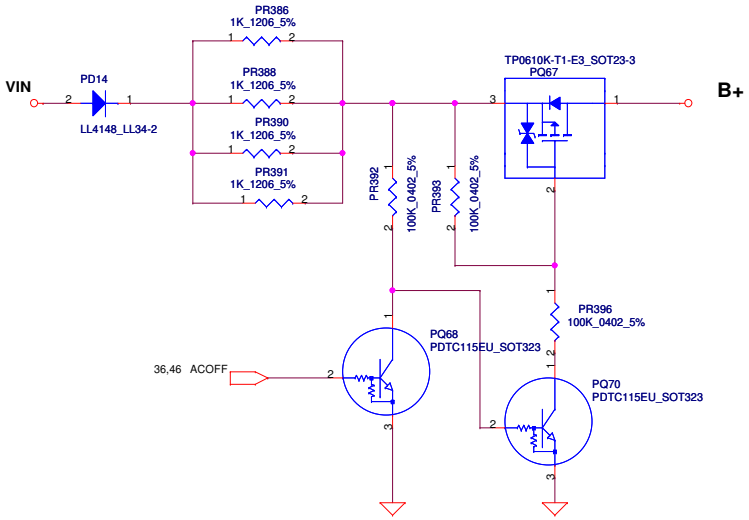
Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 46 of 56





ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

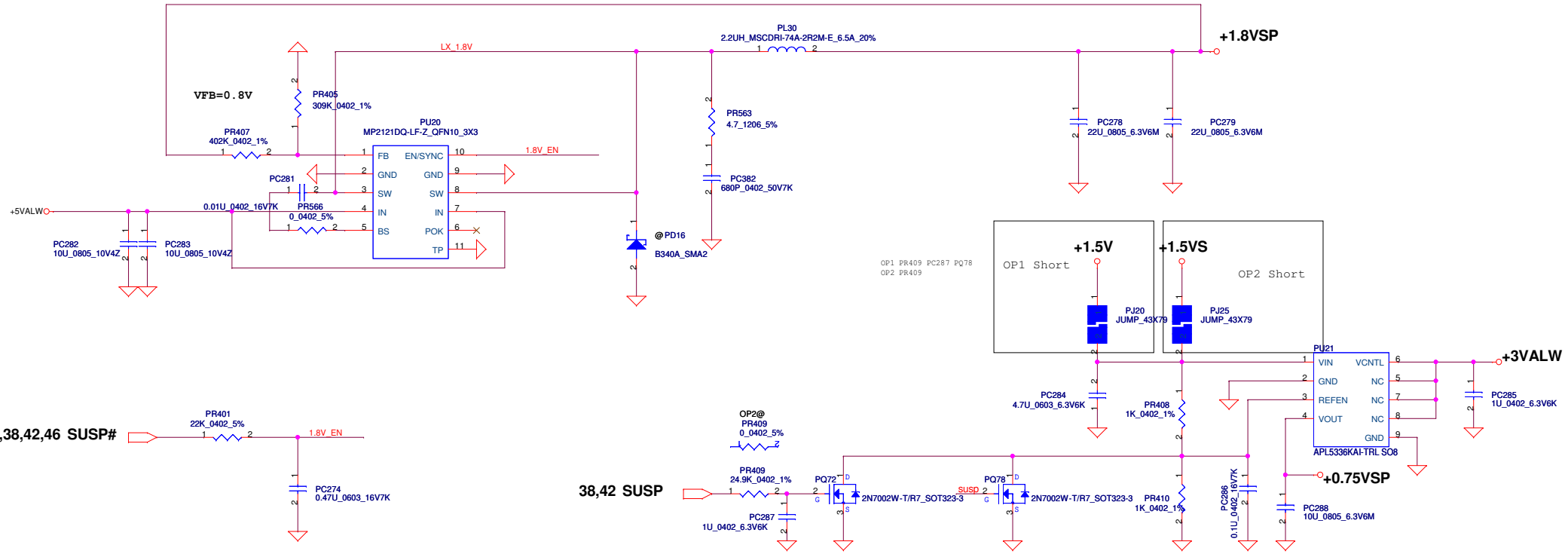
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **PRECHARGE**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 47 of 56



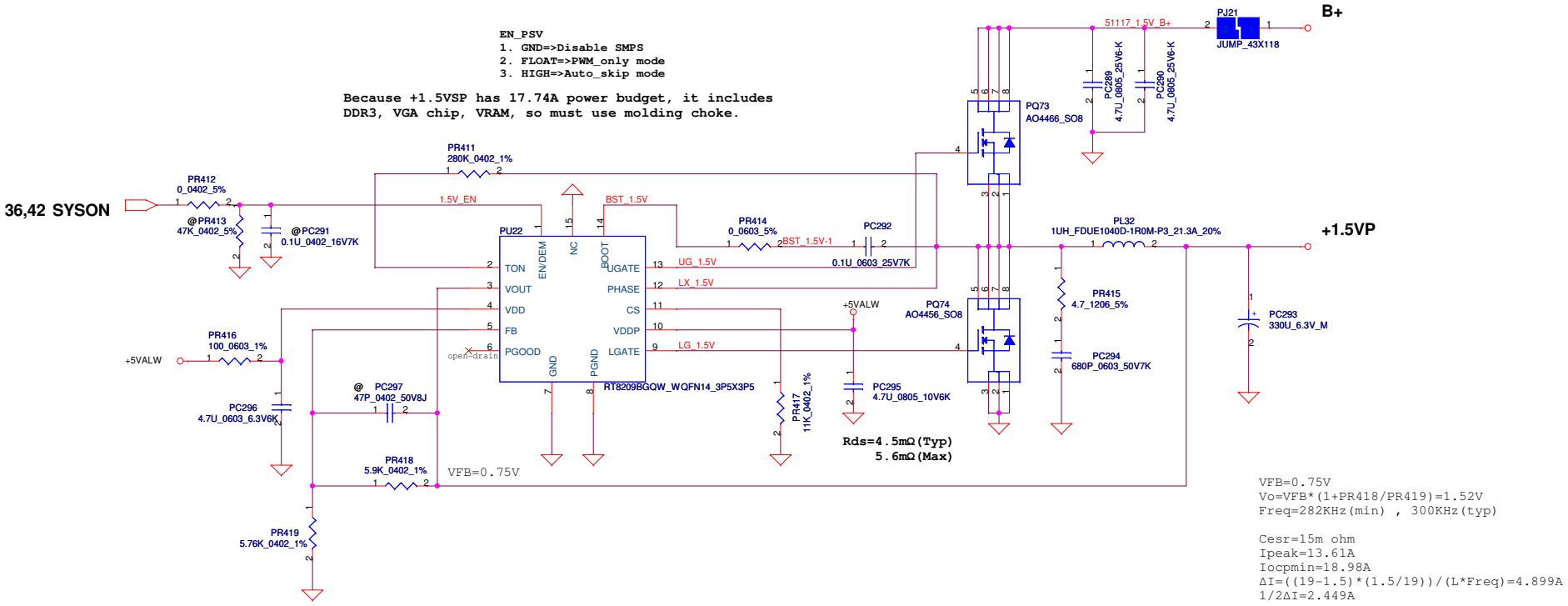
Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 48 of 56



VFB=0.75V
Vo=VFB*(1+PR418/PR419)=1.52V
Freq=282KHz(min) , 300KHz(typ)

Cesr=15m ohm
Ipeak=13.61A
Iocpmin=18.98A
ΔI=((19-1.5)*(1.5/19))/(L*Freq)=4.899A
1/2ΔI=2.449A

Iocp=18.09A~29.13A

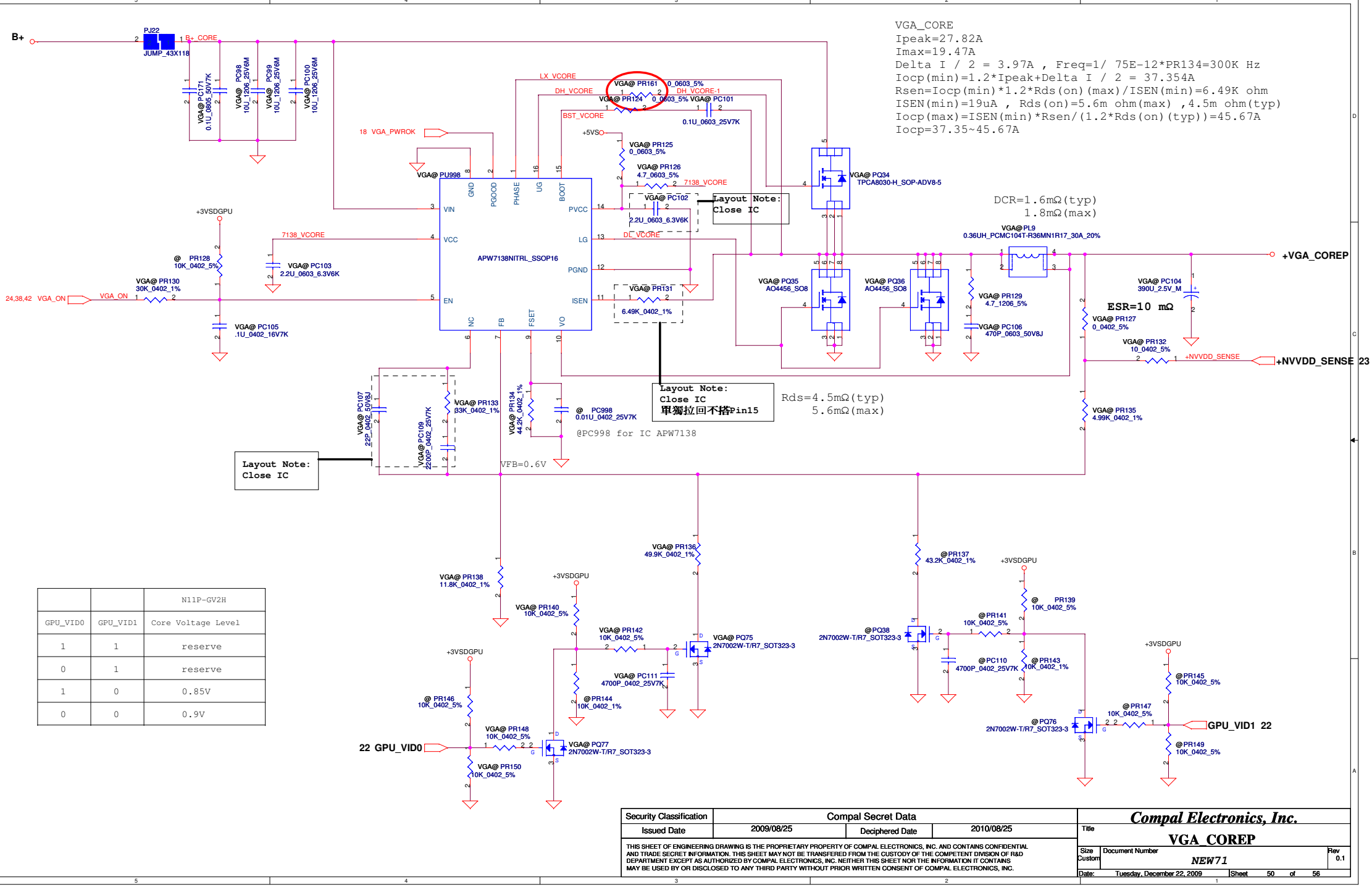
Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: **1.5VP**

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 | Sheet 49 of 56



		N11P-GV2H
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	reserve
0	1	reserve
1	0	0.85V
0	0	0.9V

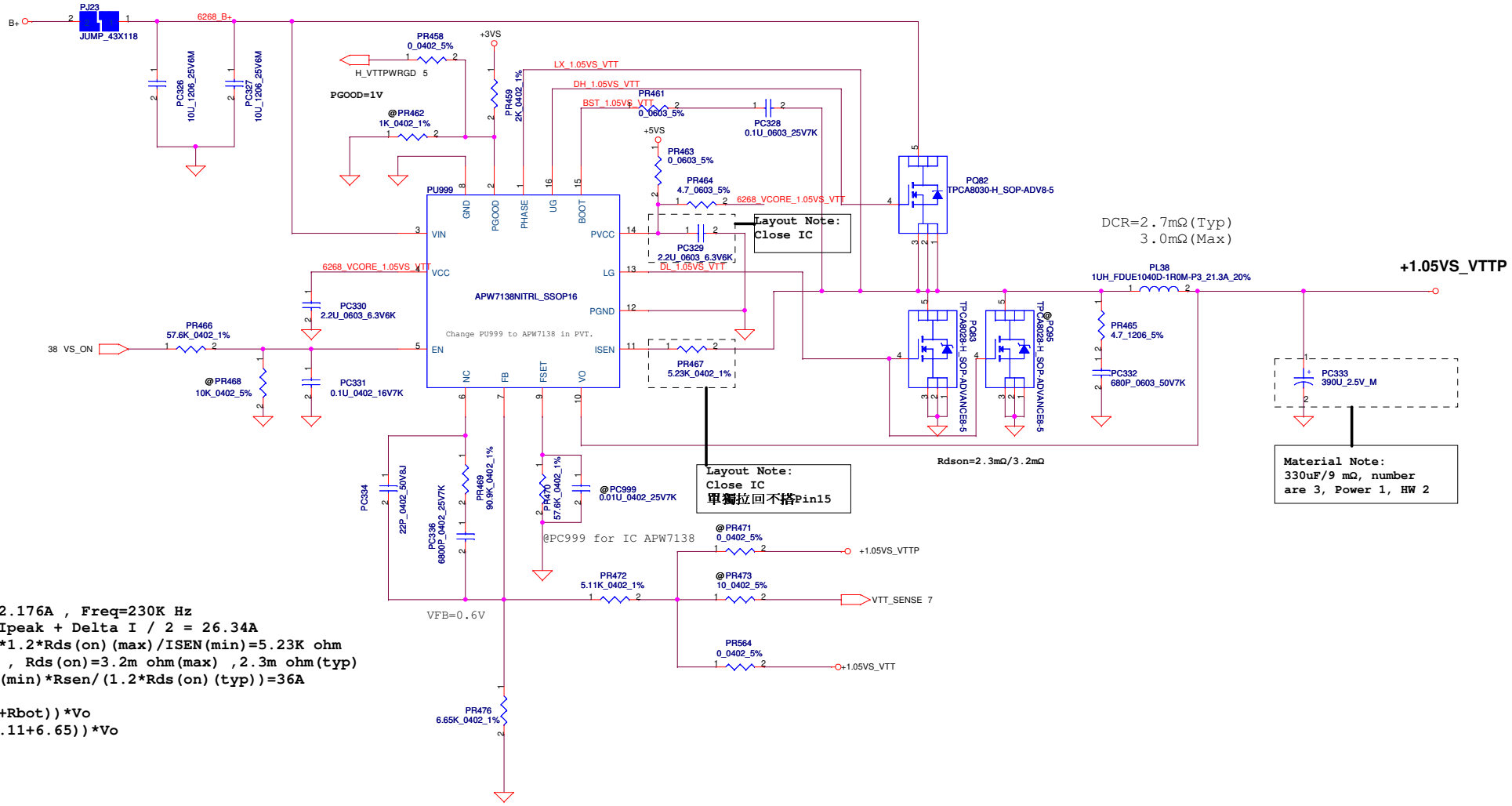
Security Classification	Compal Secret Data		
Issued Date	2009/08/25	Deciphered Date	2010/08/25

Compal Electronics, Inc.

Title: VGA_COREP

Size	Document Number	Rev
Custom	NEW71	0.1

Date: Tuesday, December 22, 2009 Sheet 50 of 56



+1.05VS_VTT
Ipeak=20.14A
Imax=14.10A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=1.2*Ipeak + Delta I / 2 = 26.34A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=5.23K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=36A
Iocp=26.34~36A
Vref=(Rb/(Rtop+Rbot))*Vo
=>0.6=(6.65/(5.11+6.65))*Vo
Vo=1.061V

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

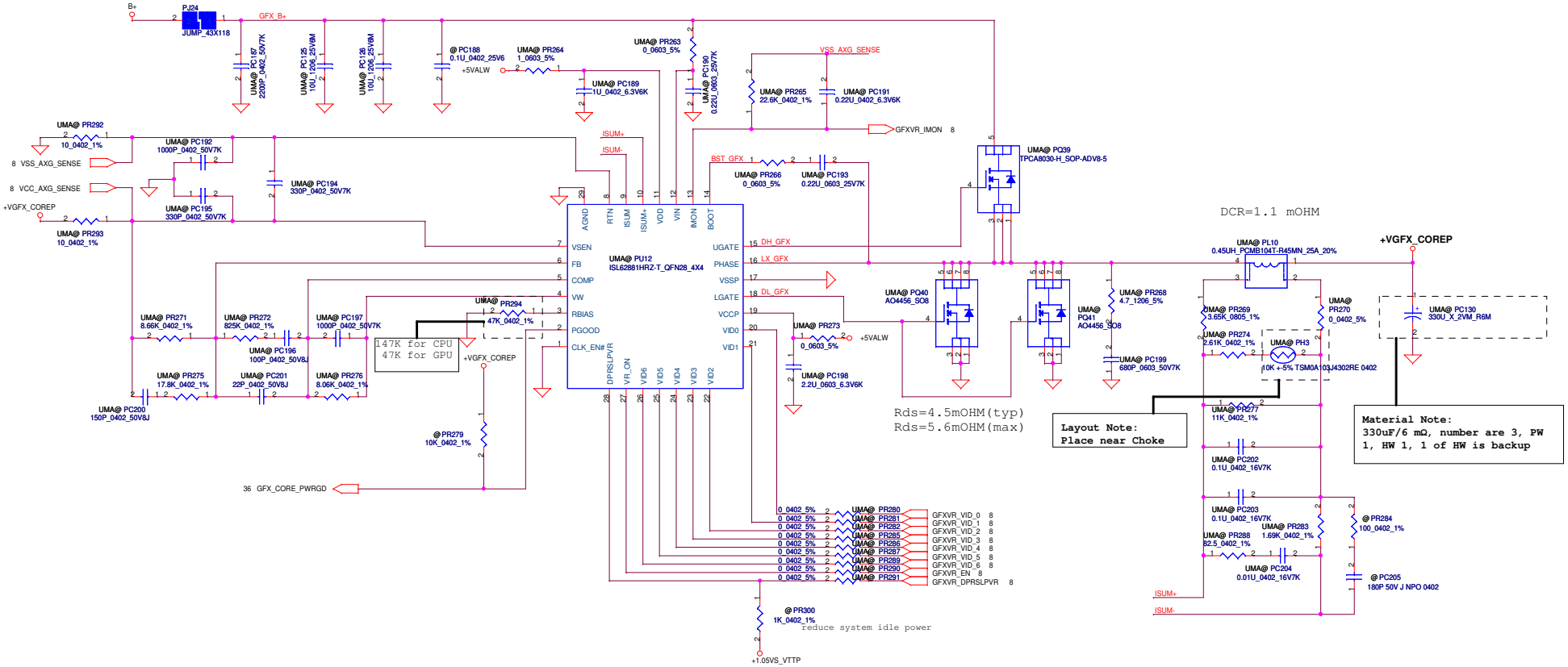
Compal Electronics, Inc.

Title: +1.05VS_VTTP

Size: Custom | Document Number: NEW71 | Rev: 0.1

Date: Tuesday, December 22, 2009 | Sheet 51 of 56

Intel Auburndale CPU(Integrate Graphics) Ipeak=22A Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



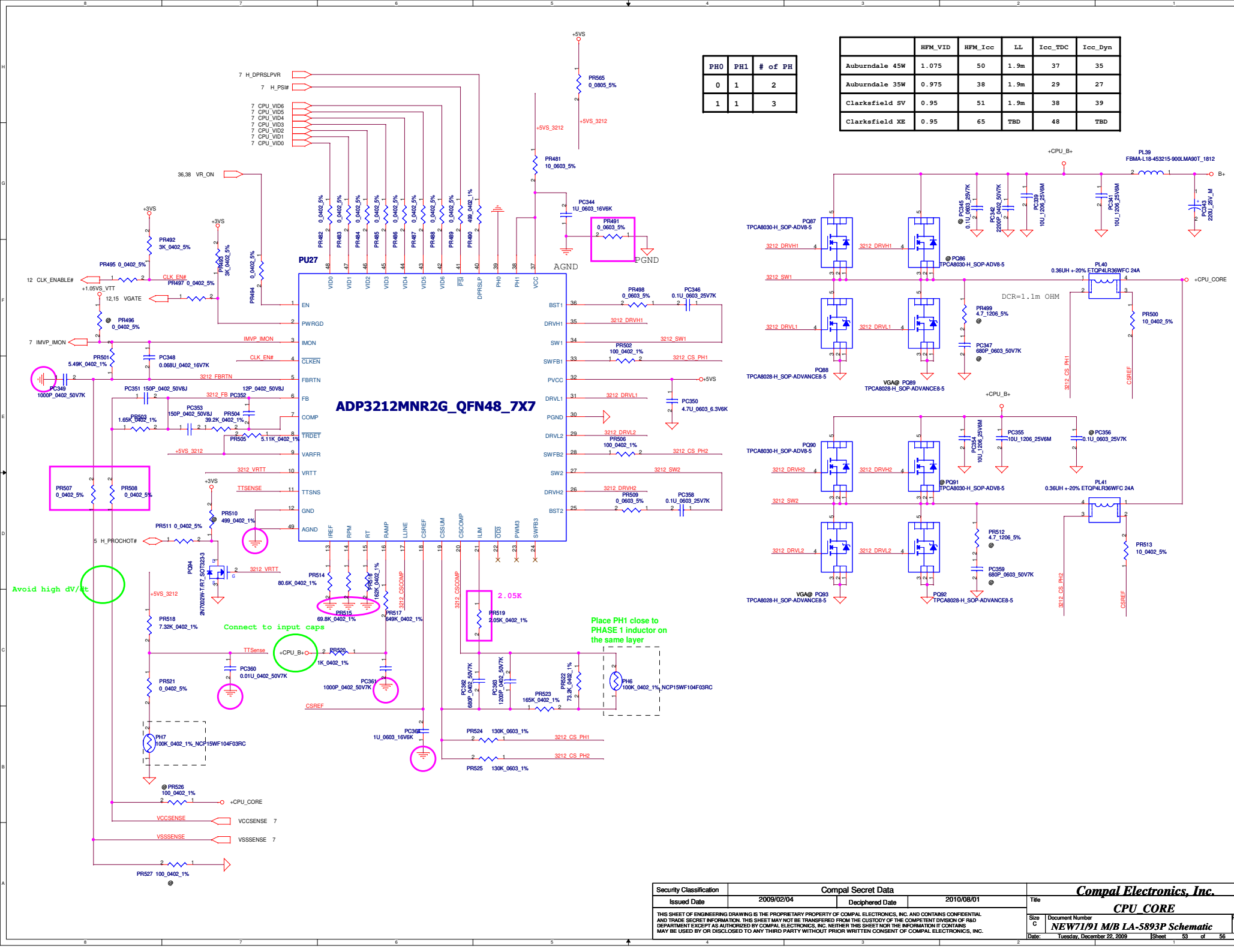
Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: GFX_COREP

Size	Document Number	Rev
C	NEW71	0.1

Date: Tuesday, December 22, 2009 Sheet 52 of 56



PH0	PH1	# of PH
0	1	2
1	1	3

	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	1.075	50	1.9m	37	35
Auburndale 35W	0.975	38	1.9m	29	27
Clarksfield SV	0.95	51	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

Security Classification	Compal Secret Data		
Issued Date	2009/02/04	Deciphered Date	2010/08/01

Compal Electronics, Inc.	
Title	CPU_CORE
Size: C	Document Number: NEW71/91 M/B LA-5893P Schematic
Rev: 0.1	
Date: Tuesday, December 22, 2009	Sheet 53 of 56

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	For BOM unique.	For BOM unique.	0.1	46	Change PD8 from SC1SS355003(S DIO 1SS355) to SC100001K00(DIO 1SS355 SOD323 T/R-5K)	2009-1021	to DVT
2	For BOM unique.	For BOM unique.	0.1	54	Delete PQ86/PQ91 SB00000HL00(S TR TPCA8030-H 1N SOP). Add PQ87/PQ90 SB00000HL00(S TR TPCA8030-H 1N SOP).	2009-1021	to DVT
3	For UMA Arrandale CPU commond design.	For UMA Arrandale CPU, we just only pop 1 HS MOS and 1 LS MOS.	0.1	54	Delete PQ89/PQ93 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
4	For VTT Power rail commond design.	For VTT Power rail commond design, we pop 1 HS MOS and 1LS MOS.	0.1	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP)	2009-1021	to DVT
5	CIS link error.	CIS link error.	0.1	54	Change PR500 from SD028100A00(S RES 1/16W 10 +-5% 0402) to SD028100A80(S RES 1/16W 10 +-5% 0402)	2009-1021	to DVT
6	BOM unique.	BOM unique.	0.1	47	Chnage PC265 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
7	BOM unique.	BOM unique.	0.1	49	Chnage PC284 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
8	BOM unique.	BOM unique.	0.1	54	Chnage PC350 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
9	BOM unique.(For Madison/Park SKU)	BOM unique.(For Madison/Park SKU)	0.1	52	Chnage PC367 from SE107475M80(S CER CAP 4.7U 6.3V M X5R 0603 to SE107475K80(S CER CAP 4.7U 6.3V K X5R 0603)	2009-1021	to DVT
10	BOM unique.	BOM unique.	0.1	46	Change PC225/PC227 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
11	BOM unique.	BOM unique.	0.1	54	Change PC339/PC341 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206) Change PC354/PC355 from SE153106K80(S CER CAP 10U 25V K X6S 1206) to SE142106M80 (S CER CAP 10U 25V M X5R 1206)	2009-1021	to DVT
12 13	+1.05VS_VTTP Cost down 1 LS MOS. HW request.	+1.05VS_VTTP Cost down 1 LS MOS. Because +1.05VS_VTT has voltage drop issue, HW request, remote sense to close to PCH.	0.2	52	Delete PQ95 SB00000GL00(S TR TPCA8028-H 1N SOP) Delete PR471 SD028000080(S RES 0 0402 5%) Delete PR473 from SD034100A80(S RES 10 0402 5%) Add PR564 SD028000080(S RES 1/16W 0 0402 5%)	2009-1029	to DVT
14	Adjust +1.05VS_VTTP OCP.	Because we remove a LS MOS, so OCP must adjust.	0.2	52	Change PR467 from SD000004O80(S RES 1/16W 2.2K +-1% 0402) to SD034499180(S RES 1/16W 4.99K 0402 1%)	2009-1029	to DVT
15	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PU19 SA00001NC00 (S IC APL5913-KAC-TRL SO 8P)	2009-1029	to DVT
16	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PR402 SD034150280, PR404 SD034120280. Delete PC273 SE075103K80 PC275 SE000000I10	2009-1029	to DVT
17	+1.8VSP2, Using MP2121 for 1.8V only.	No need to use LDO for +1.8V. Delete all PU19 circiut.	0.2	49	Delete PC272 SE107475K80, PC271 SE107105M80 Delete PR401 and PR403 SD028220280, PC274 SE026474K80	2009-1029	to DVT
18	+VGA_COREP, efficiency issue.	Increase Freq, decrease choke, to improve efficiency.	0.2	51	Change PR196 from SD034442280 to SD034365280. Change PL14 from SL200000V00 to SH000005680	2009-1029	to DVT
19	+VGA_COREP, OVP issue.	Becasue if PR199/PR202 pop 0ohm, it will cause OVP when VID change from 00 to 11)	0.2	51	Change PR199/PR202 from SD028000080 to SD028100280 (S RES 1/16W 10K 0402 5%)	2009-1029	to DVT
20	+VGA_COREP, cost issue.	Cost down.	0.2	51	Change PQ75/PQ78 from SB00000GL00(S TR TPCA8028-H 1N SOP) to SB000009F80(S TR AO4456 1N SO8)	2009-1029	to DVT
21	+VGA_COREP, satndard design.	+VGA_COREP, satndard design, pop 1HS MOS and 2LS MOS, so remove one HS MOS PQ79.	0.2	51	Delete PQ79 SB000008L80 (S TR SI7686DP-T1-E3 1N POWERPAK SO8)	2009-1029	to DVT
22	+GFX_COREP, spike issue.	Because +GFX_COREP has spike voltage issue, add schottky diode across GFXVR_EN and VS_ON to solve it.	0.2	51	Add PD17 SCS00000Z00 (S SCH DIO RB751V-40 SOD-323)	2009-1029	to DVT
23	+VGA_COREP, OCP caaculation erroe issue.	Because VGA_CORE has 2 LS MOS, APW7138 detect LS Rdson, so when caculate OCP, Rdson must reduce 1/2.	0.2	51	Change PR190 from SD034649180 to SD034511180 (S RES 1/16W 5.11K 0402 1%)	2009-1029	to DVT

A -->Modify item

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2010/08/01

Compal Electronics, Inc.

Title: PIR (HW)

Size	Document Number	Rev
Custom	NEW71/91 M/B LA-5891P Schematic	0.1

Date: Friday, December 18, 2009 | Sheet 55 of 56

PCB

ZZZ

LA-5893P REV0 M/B

ZZZ1

X76198BOL21

ALT. GROUP PARTS 1G SAM

ZZZ2

X76198BOL22

ALT. GROUP PARTS 1G HYN

Compal Electronics, Inc.

Title: Option Component

Size: Custom | Document Number: NEW70 M/B LA-5891P Schematic | Rev: 0.1

Date: Monday, December 21, 2009 | Sheet 56 of 56