ZB2

CPU CORE
SENTECH
SC451ITSTR
Page:32

SYSTEM 3V/5V
MAXIM
MAX1999
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5VSUS
+5V
+15V
Page:33

+1.8VSUS
+1.8V
+0.9VSUS
+0.9V
+1.5V
+1.05V
Page:34
+2.5V
+1.2V
VGA_CORE
Page:36

BATTERY CHARGER
MAXIM
MAX8724
Page:35

X'TAL 14.318MHZ
CLOCK GEN
ICS954310BG
Page:4

Yonah/Merom
INTEL Mobile_479 CPU
Page:2, 3

HOST BUS 533/667 MHz

VRAM x4
DDR2
16Mx16
32Mx16

CRT
Page: 22

LVDS
Page: 22

ATi M52P /M52PG /M54P
Page: 17, 18,19, 20

PCIE
RGB
LVDS
UMA(option)

CALISTOGA-GM
1466 FCBGA
Page: 5, 6 , 7, 8, 9, 10

DDR-II SODIMM1
Page: 12
DDR-II SODIMM2
Page: 12
DDR-II

DMI I/F

MINI-Card slot Wireless LAN
Page: 24

SATA HDD
Page: 23
PATA HDD
Page: 23
IDE-ODD
Page: 23
ATA 66/100
ATA 66/100
HD Audio

ICH7-M
652 BGA
Page: 13,14,15,16

PCI-E BUS
PCI BUS 33MHZ
USB 2.0
LPC 33MHZ

X'TAL 32.768KHZ

TI PCI7412
AD25
REQ0#
GNT0#
INTE#
INTF#
INTG#
Page: 26

OSC 48MHZ

TYPE II SLOT
Page: 26

6 IN 1 Cardreader
Page: 27

MINI-PCI Wireless LAN
AD19
REQ2# / GNT2#
INTC# , INTD#
Page: 24

REALTEK RTL8100CL
AD16
REQ1#
GNT1#
INTB#
Page: 25

X'TAL 25M

RJ45
Page: 25

AUDIO CODEC
Realtek
ALC883 (ALC260)
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AMP
MAX9755
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MODEM
Page: 28

Connector

RJ11
Page: 25

MIC IN
Page: 29
SPEAKER
Page: 29
LINE OUT
Page: 29

X'TAL 32.768K

KBC
NS PC97551/541V
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Touchpad
Page: 29
Keyboard
Page: 31
FLASH
Page: 30
FAN
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SYSTEM USB PORT *3
Page:24

Bluetooth USB interface
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Quanta Computer Inc.

Size	Document Number	Rev
	BLOCK DIAGRAM	1A

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CPU

U29A

ADDR GROUP 0

CONTROL

XDP/ITP SIGNALS

THERM

H CLK

RESERVED

PZ47903-2741-01

Near to MCH <500mils

XDP PU_R < 0.2"

U29B

DATA GRP 0

DATA GRP 1

DATA GRP 2

DATA GRP 3

MISC

PZ47903-2741-01

Close CPU

Close CPU

TO VRD

H_PWRGD is CMOS driving by ICH

XDP_TCK PD 27.4/1%
XDP_TRST PD 680ohm /5%
XDP_TDI PU 150ohm /1.05V
XDP_TMS PU 39.2/1%

REV_2A/12-13 Add

To EC

H/W MONITOR

SLAVE ADDRESS: 98

15 MIL

U8

G781

To SB

To FAN

10 mil trace /
10 mil space

PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	CPU(1 OF 2)	2A
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CPU

U29D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
A26	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	AF3
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	AF24

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+1.05V
VCC_CORE
+1.5V

+1.05V [2,4,5,8,9,13,16,33,34]
VCC_CORE [2,32]
+1.5V [7,9,14,16,24,28,33,34]

U29C

A7	VCC[001]	VCC[68]	AB20
A9	VCC[002]	VCC[69]	AB7
A10	VCC[003]	VCC[70]	AC7
A12	VCC[004]	VCC[71]	AC9
A13	VCC[005]	VCC[72]	AC12
A15	VCC[006]	VCC[73]	AC13
A17	VCC[007]	VCC[74]	AC15
A18	VCC[008]	VCC[75]	AC17
A20	VCC[009]	VCC[76]	AC18
B7	VCC[010]	VCC[77]	AD7
B9	VCC[011]	VCC[78]	AD9
B10	VCC[012]	VCC[79]	AD10
B12	VCC[013]	VCC[80]	AD12
B14	VCC[014]	VCC[81]	AD14
B15	VCC[015]	VCC[82]	AD15
B17	VCC[016]	VCC[83]	AD17
B18	VCC[017]	VCC[84]	AD18
B20	VCC[018]	VCC[85]	AE9
C9	VCC[019]	VCC[86]	AE10
C10	VCC[020]	VCC[87]	AE12
C12	VCC[021]	VCC[88]	AE13
C13	VCC[022]	VCC[89]	AE15
C15	VCC[023]	VCC[90]	AE17
C17	VCC[024]	VCC[91]	AE18
C18	VCC[025]	VCC[92]	AE20
D9	VCC[026]	VCC[93]	AF9
D10	VCC[027]	VCC[94]	AF10
D12	VCC[028]	VCC[95]	AF12
D14	VCC[029]	VCC[96]	AF14
D15	VCC[030]	VCC[97]	AF15
D17	VCC[031]	VCC[98]	AF17
D18	VCC[032]	VCC[99]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	V6
E12	VCC[036]	VCCP[02]	G21
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA	B26
AA10	VCC[053]		
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AE5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AF4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AE2
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]	VCCSENSE	AF7
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AE7

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VCC_CORE

C237 C189 C193 C199 — 10U-6.3V_8
C213 C217 C230 C238 — 10U-6.3V_8
C185 C191 C197 C214 — 10U-6.3V_8
C220 C236 C244 C262 — 10U-6.3V_8
C263 C264 C265 C266 — 10U-6.3V_8
C613 C612 C611 C610 — 10U-6.3V_8
C608 C609 C626 C625 — 10U-6.3V_8
C624 C623 C621 C622 — 10U-6.3V_8

change to 0805

REV_3A/02-09 Change to 10U

VCC_CORE

C200 C211 C216 C225 — 10U-6.3V_8

reserve dummy cap--Allen

REV_3A/02-09 Change to 10U

+1.05V

C186 C187 C242 C243 C149 C153 — .1U/10V_4 1U/10V_4 1U/10V_4 1U/10V_4 1U/10V_4 1U/10V_4

+1.05V

C144 330U-2.5V_7343

+1.5V

C637 C639 — .01U/16V_4 10U/X5R-6.3V_8

Close CPU B26

+1.5V

CPU_VID0 [32]
CPU_VID1 [32]
CPU_VID2 [32]
CPU_VID3 [32]
CPU_VID4 [32]
CPU_VID5 [32]
CPU_VID6 [32]

VCC_CORE

R164 100/F_4

VCCSENSE [32]

R162 100/F_4

VSSSENSE [32]

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Quanta Computer Inc.

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	CPU(2 OF 2)	3A
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Note : If Use Internal VGA Please NC "EV@xxx" Parts

CLK

Close to IC <500mils

REV_3B/03-14 Add

25 mils

L21 ACB2012L-120-T_8

+3V — 120 ohms@100Mhz — VDD_SRC_CPU

C182 1U/10V_4, C235 .1U/10V_4, C233 1U/10V_4, C179 1U/10V_4, C183 10U/10V_8

R187 2.2/F_6 — VDD_A

C231 .1U/10V_4, C247 10U/10V_8

VR_PWRGD_CK410# C — C724 .1U/10V_4

REV_3A/02-05 Add

25 mils

L22 ACB2012L-120-T_8

+3V — VDD_PCI

C180 .1U/10V_4, C192 .1U/10V_4, C194 10U/10V_8

R153 2.2/F_6 — VDD_48

C181 .1U/10V_4, C169 10U/10V_8

R189 1_6 — VDD_REF

C234 .1U/10V_4, C245 10U/10V_8

[15,32] VR_PWRGD_CK410# — R540 0_4 — VR_PWRGD_CK410# C

[15] VR_PWRGD_CK410_R# — R541 *0_4

REV_3A/02-09 Add

REQ3 Latched Select
"0" : CLK Enable
"1" : CLK Disable
Control : PCIE 2,4

[24] MINI_CLKREQ3# — MINI_CLKREQ3# — R169 10K_4 — +3V

PEREQ Control Pair	
PEREQ1	PECLK Pair0, 6
PEREQ2	PECLK Pair1, 8
PEREQ3	PECLK Pair2, 4
PEREQ4	PECLK Pair3, 5, 7

C627 27P_4 — CG_XIN — C629 27P_4 — CG_XOUT — CL=20pF — Y4 14.318MHZ

VDD_A

U6 CK-410M ICS954310BGLF

X1, X2

VR_PWRGD_CK410# C — R420 *10K_4 — +3V

[15] PM_STPCPU# — PM_STPCPU#
[15] PM_STPPCI# — PM_STPPCI#

[12] SMBCK — SMBCK
[12] SMBDT — SMBDT

[15] CLKUSB_48 — R421 33_4 — CLKUSB_48_R

CLK_BSEL0 — R414 4.7K_4
CLK_BSEL1
CLK_BSEL2 — R181 4.7K_4

VDD_REF, VDD_SRC_CPU, VDD_PCI, VDD_SRC_CPU, VDD_48, MINI_CLKREQ3#

Iref=5mA, Ioh=4*Iref — R182 475/F_6 — IREF

[7] DREFCLK — DREFCLK — RP18 — R_DOT96 — R_DOT96# — [7] DREFCLK#

33_4P2R_S

T47 — INTERNAL PULL HIGH — PWRSAVE#

DOT96MHz, DOT96MHz#, 27Mfix/LCD_SSCGT/PCIE0T, 27SS/LCD_SSCGC/PCIE0C, selPCIEX0_LCD#/PCI5, PCI4, PCI3, PCICLK2/REQ_SEL, PCIF1/selLCD_27#, PCIF0/ITP_EN

GND, GND_48, GND, GND, GND_PCI_1, GND_PCI_2, GND, GND_SRC, GND

BSEL strappings need to be set for 533MHz Moby Dick (Intel?915GM - Calistoga Interposer)
(if Calistoga is designed for 667MHz board).

REV_3A/02-06 Modify

Place these termination to close CK410M.

R180 22_4 — 14M_ICH [15] — C246 *10P/50V_4

14M_REF

CPUCLKT0, CPUCLKC0 — RHCLK_CPU, RHCLK_CPU# — RP57 33_4P2R_S — CLK_CPU_BCLK, CLK_CPU_BCLK# — CLK_CPU_BCLK [2], CLK_CPU_BCLK# [2]

CPUCLKT1, CPUCLKC1 — RHCLK_MCH, RHCLK_MCH# — RP58 33_4P2R_S — CLK_MCH_BCLK, CLK_MCH_BCLK# — CLK_MCH_BCLK [5], CLK_MCH_BCLK# [5]

CPUCLKT2/PCIET8, CPUCLKC2/PCIEC8
REQ1#/PCIET7, REQ2#/PCIEC7
PCIET6, PCIEC6

PCIET5, PCIEC5 — RSRC_MCH, RSRC_MCH# — RP19 33_4P2R_S — CLK_PCIE_3GPLL, CLK_PCIE_3GPLL# — CLK_PCIE_3GPLL [7], CLK_PCIE_3GPLL# [7]

PCIET4, PCIEC4

SATA_CKT, SATA_CKC — RSRC_SATA, RSRC_SATA# — RP55 33_4P2R_S — CLK_PCIE_SATA, CLK_PCIE_SATA# — CLK_PCIE_SATA [13], CLK_PCIE_SATA# [13]

PCIET3, PCIEC3 — PECLK_VGA_R, PECLK_VGA_R# — RP16 EV@33_4P2R_S — CLK_PCIE_VGA, CLK_PCIE_VGA# — CLK_PCIE_VGA [17], CLK_PCIE_VGA# [17]

PCIET2, PCIEC2 — R_CLK_PCIE_MINI, R_CLK_PCIE_MINI# — RP56 33_4P2R_S — CLK_PCIE_MINI, CLK_PCIE_MINI# — CLK_PCIE_MINI [24], CLK_PCIE_MINI# [24]

PCIET1, PCIEC1 — RSRC_ICH, RSRC_ICH# — RP17 33_4P2R_S — CLK_PCIE_ICH, CLK_PCIE_ICH# — CLK_PCIE_ICH [14], CLK_PCIE_ICH# [14]

R_DREFSSCLK, R_DREFSSCLK# — RP54 33_4P2R_S — DREFSSCLK, DREFSSCLK# — DREFSSCLK [7], DREFSSCLK# [7]

R_PCLK_SIO — R159 10K_4
R_PCLK_LAN — R160 33_4
R_PCLK_PCM — R161 33_4
PCLK_MINI_LPC — R176 33_4
R_PCLK_ICH — R423 33_4
R_PCLK_591 — R422 33_4

PCLK_LAN [25], PCLK_PCM [26], PCLK_MINI [24], PCLK_ICH [14], PCLK_591 [30]

R177 *10K_4 — +3V
R417 10K_4
R416 10K_4

C601 *10P/50V_4, C166 *10P/50V_4, C600 *10P/50V_4, C209 *10P/50V_4, C165 *10P/50V_4

[2] CPU_BSEL0 — R412 *56.2/F_4 — R410 0_4 — R411 *1K_4 — CLK_BSEL0 — R409 1K_4 — MCH_BSEL0 [7]

FSA

[2] CPU_BSEL1 — R413 *1K_4 — R415 0_4 — R424 *0_4 — CLK_BSEL1 — R418 1K_4 — MCH_BSEL1 [7]

FSB

Stuff 0 ohm for 533MHz, NC for 667MHz

[2] CPU_BSEL2 — R179 *1K_4 — R188 0_4 — R183 *0_4 — CLK_BSEL2 — R185 1K_4 — MCH_BSEL2 [7]

FSC

+5V, +1.8V — C162 .1U/10V_4, C630 .1U/10V_4

REV_02/11-21 Modify

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

CLK_CPU_BCLK# RP59 — CLK_CPU_BCLK — 49.9_4P2R_S
CLK_MCH_BCLK# RP60 — CLK_MCH_BCLK — 49.9_4P2R_S
CLK_PCIE_MINI# RP53 — CLK_PCIE_MINI — 49.9_4P2R_S
CLK_PCIE_3GPLL RP20 — CLK_PCIE_3GPLL# — 49.9_4P2R_S
CLK_PCIE_ICH RP13 — CLK_PCIE_ICH# — 49.9_4P2R_S
CLK_PCIE_VGA RP15 — CLK_PCIE_VGA# — EV@49.9_4P2R_S
DREFSSCLK# RP51 — DREFSSCLK — IV@49.9_4P2R_S
DREFCLK RP14 — DREFCLK# — 49.9_4P2R_S
CLK_PCIE_SATA# RP52 — CLK_PCIE_SATA — 49.9_4P2R_S

+3V — Q18 RHU002N06 — R430 10K_4, R432 10K_4 — [15,24] PDAT_SMB — SMBDT

+3V — Q19 RHU002N06 — [15,24] PCLK_SMB — SMBCK

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Quanta Computer Inc.

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	CLOCK GENERATOR	3B
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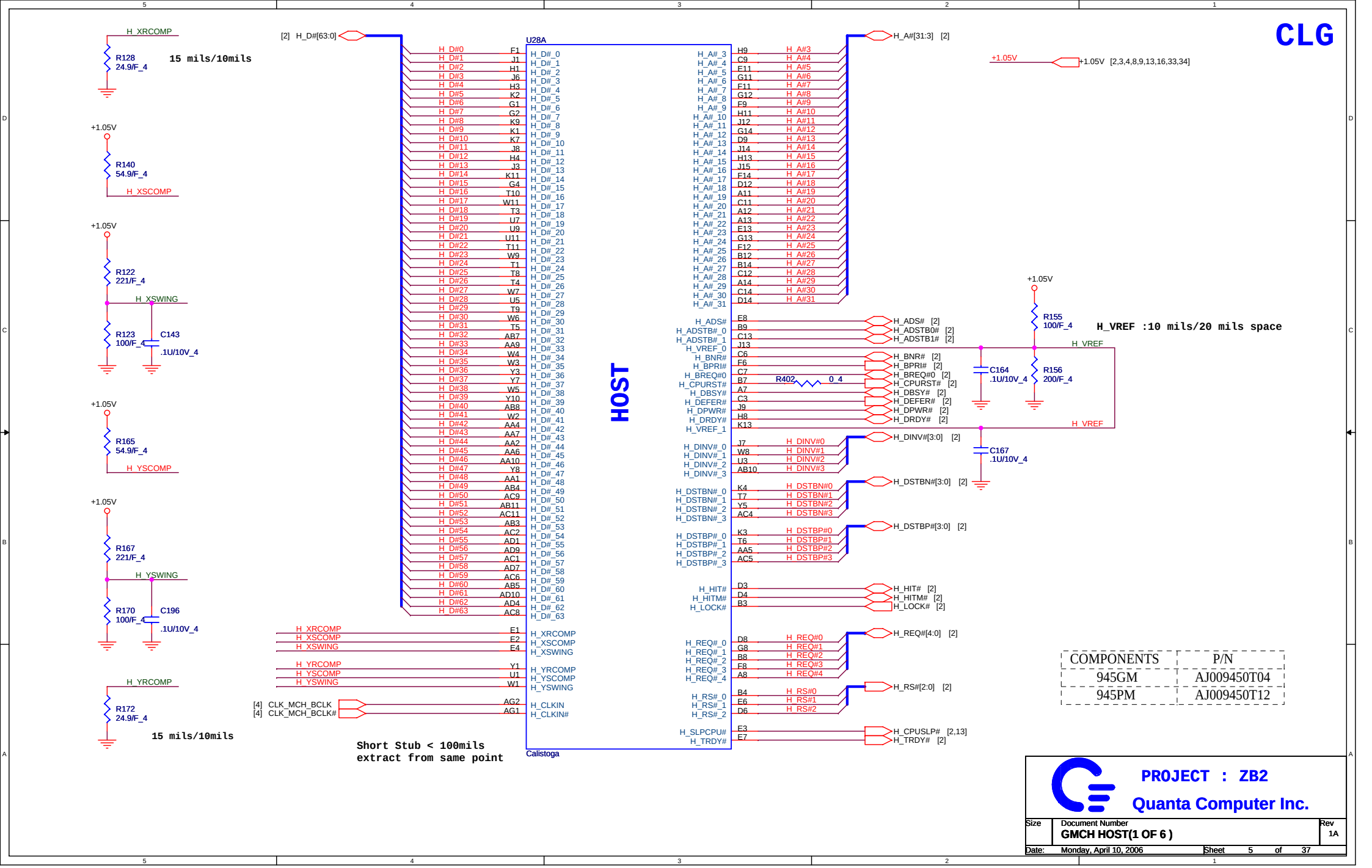
CLG
H_XRCOMP
R128
24.9/F_4
15 mils/10mils
+1.05V
R140
54.9/F_4
H_XSCOMP
+1.05V
R122
221/F_4
H_XSWING
R123
100/F_4
C143
.1U/10V_4
+1.05V
R165
54.9/F_4
H_YSCOMP
+1.05V
R167
221/F_4
H_YSWING
R170
100/F_4
C196
.1U/10V_4
H_YRCOMP
R172
24.9/F_4
15 mils/10mils
[2] H_D#[63:0]
U28A
HOST
Calistoga
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
[4] CLK_MCH_BCLK AG2
[4] CLK_MCH_BCLK# AG1
H_CLKIN
H_CLKIN#
Short Stub < 100mils
extract from same point
H_A#[31:3] [2]
H_A#_3 H9
H_A#_4 C9
H_A#_5 F11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 F9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
+1.05V
+1.05V [2,3,4,8,9,13,16,33,34]
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_VREF_0 J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_VREF_1 K13
H_ADS# [2]
H_ADSTB0# [2]
H_ADSTB1# [2]
H_BNR# [2]
H_BPRI# [2]
H_BREQ#0 [2]
H_CPURST# [2]
H_DBSY# [2]
H_DEFER# [2]
H_DPWR# [2]
H_DRDY# [2]
R402 0_4
+1.05V
R155
100/F_4
H_VREF
R156
200/F_4
C164
.1U/10V_4
H_VREF
C167
.1U/10V_4
H_VREF :10 mils/20 mils space
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DINV#[3:0] [2]
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBN#[3:0] [2]
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_DSTBP#[3:0] [2]
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# [2]
H_HITM# [2]
H_LOCK# [2]
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4:0] [2]
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] [2]
H_SLPCPU# E3
H_TRDY# E7
H_CPUSLP# [2,13]
H_TRDY# [2]
COMPONENTS P/N
945GM AJ009450T04
945PM AJ009450T12
PROJECT : ZB2
Quanta Computer Inc.
Size
Document Number
GMCH HOST(1 OF 6)
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1A
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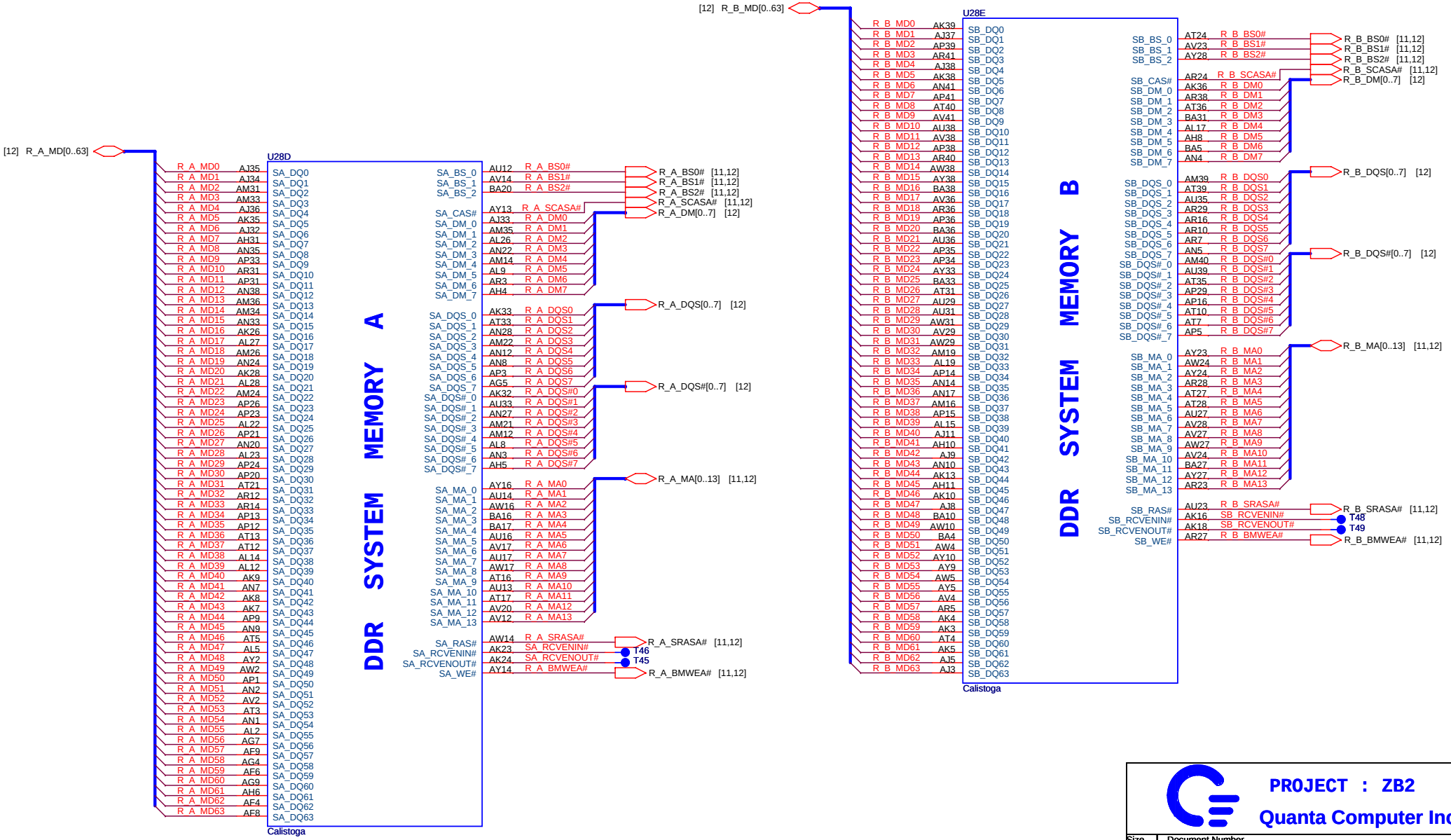
CLG



PROJECT : ZB2		
Quanta Computer Inc.		
Size	Document Number: GMCH DDR(2 OF 6)	Rev: 1A
Date: Monday, April 10, 2006	Sheet 6 of 37	

CLG

Note : If Use Internal VGA Please NC "UMA@xxx" Parts

U28B

RSVD
RSVD_0
RSVD_1
RSVD_2
RSVD_3
RSVD_4
RSVD_5
RSVD_6
RSVD_7
RSVD_8
RSVD_9
RSVD_10
RSVD_11
RSVD_12
RSVD_13
RSVD_14
RSVD_15

CFG
CFG_0
CFG_1
CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20

PM
PM_BMBUSY#
PM_EXTTS#_0
PM_EXTTS#_1
PM_THRMTRIP#
PWROK
RSTIN#

MISC
SDVO_CTRLCLK
SDVO_CTRLDATA
LT_RESET#

NC
NC0
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
NC9
NC10
NC11
NC12
NC13
NC14
NC15
NC16
NC17
NC18

DDR MUXING
SM_CK_0
SM_CK_1
SM_CK_2
SM_CK_3
SM_CK#_0
SM_CK#_1
SM_CK#_2
SM_CK#_3
SM_CKE_0
SM_CKE_1
SM_CKE_2
SM_CKE_3
SM_CS#_0
SM_CS#_1
SM_CS#_2
SM_CS#_3
SM_OCDCOMP_0
SM_OCDCOMP_1
SM_ODT_0
SM_ODT_1
SM_ODT_2
SM_ODT_3
SM_RCOMP#
SM_RCOMP
SM_VREF_0
SM_VREF_1

CLK
G_CLKIN#
G_CLKIN
D_REFCLKIN#
D_REFCLKIN
D_REFSSCLKIN#
D_REFSSCLKIN

DMI
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3

Calistoga

CFG[17:3] Internal Pull-up

CFG[2:0]=011
FSB=667M
CFG[2:0]=001
FSB=533M

CFG[18,19] Internal Pull-down

Layout as short as passable
NC from WW45
15mils/15mils
15mils/10mils
+1.8VSUS
+0.9VSUS
SMDDR_VREF_MCH
0_6

CLK_PCIE_3GPLL# [4]
CLK_PCIE_3GPLL [4]
DREFCLK# [4]
DREFCLK [4]
DREFSSCLK# [4]
DREFSSCLK [4]

DMI_TXN0 [14]
DMI_TXN1 [14]
DMI_TXN2 [14]
DMI_TXN3 [14]
DMI_TXP0 [14]
DMI_TXP1 [14]
DMI_TXP2 [14]
DMI_TXP3 [14]
DMI_RXN0 [14]
DMI_RXN1 [14]
DMI_RXN2 [14]
DMI_RXN3 [14]
DMI_RXP0 [14]
DMI_RXP1 [14]
DMI_RXP2 [14]
DMI_RXP3 [14]

< 0.1" . 15mils/15mils space
use 1% R

GMCH Strap pin

1.MCH_CFG_5 DMI Select : Low = DMI X2, High=DMIX4 (Default "1")
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap : Low=RSVD, High=Mobile CPU (Default "1")
4.MCH_CFG_9 PCI Exp Graphics Lane : Low =Reserved, High=Mobility (Default "1")
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: PSB 4x CLK ENABLE Low=Reserved, High=Calistoga
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled. (Default "1")
8.MCH_CFG_18 VCC Select : LOW=1.05V, High=1.5V (Default "0")
9.MCH_CFG_19 DMI Lane Reversal : 0=Normal operation 1=Reverse Lane (Default "0")
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.

CFG[18,19] Internal Pull-down

U28C

LVDS
L_BKLTCTL
L_BKLTEN
L_CLKCTLA
L_CLKCTLB
L_DDC_CLK
L_DDC_DATA
L_IBG
L_VBG
L_VDDEN
L_VREFH
L_VREFL
LA_CLK#
LA_CLK
LB_CLK#
LB_CLK
LA_DATA#_0
LA_DATA#_1
LA_DATA#_2
LA_DATA_0
LA_DATA_1
LA_DATA_2
LB_DATA#_0
LB_DATA#_1
LB_DATA#_2
LB_DATA_0
LB_DATA_1
LB_DATA_2

TV
TV_DACA_OUT
TV_DACB_OUT
TV_DACC_OUT
TV_IREF
TV_IRTNA
TV_IRTNB
TV_IRTNC

VGA
CRT_BLUE
CRT_BLUE#
CRT_GREEN
CRT_GREEN#
CRT_RED
CRT_RED#
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_IREF
CRT_VSYNC

Calistoga

PCI-EXPRESS GRAPHICS
EXP_A_COMPI
EXP_A_COMPO
EXP_A_COMPX
EXP_A_RXN_0 … EXP_A_RXN_15
EXP_A_RXP_0 … EXP_A_RXP_15
EXP_A_TXN_0 … EXP_A_TXN_15
EXP_A_TXP_0 … EXP_A_TXP_15

20mils/20mils space
+V1.5_PCIE
GMCHEXP_RXN[0..15] [17]
GMCHEXP_RXP[0..15] [17]
GMCHEXP_TXP[0..15] [17]
GMCHEXP_TXN[0..15] [17]

UMA@1U_4
0.1u Capacitors place at first 1/3 of trace

+V1.5_PCIE [9]
+3V [2,4,9,12,13,14,15,16,17,19,20,22,23,24,25,26,27,28,29,30,31,32,33,34,36]
+0.9VSUS [12,34]
+1.8VSUS [8,12,33,34]

PROJECT	ZB2
	Quanta Computer Inc.
Size	Document Number: GMCH DMI/VEDIO(3 OF 6)
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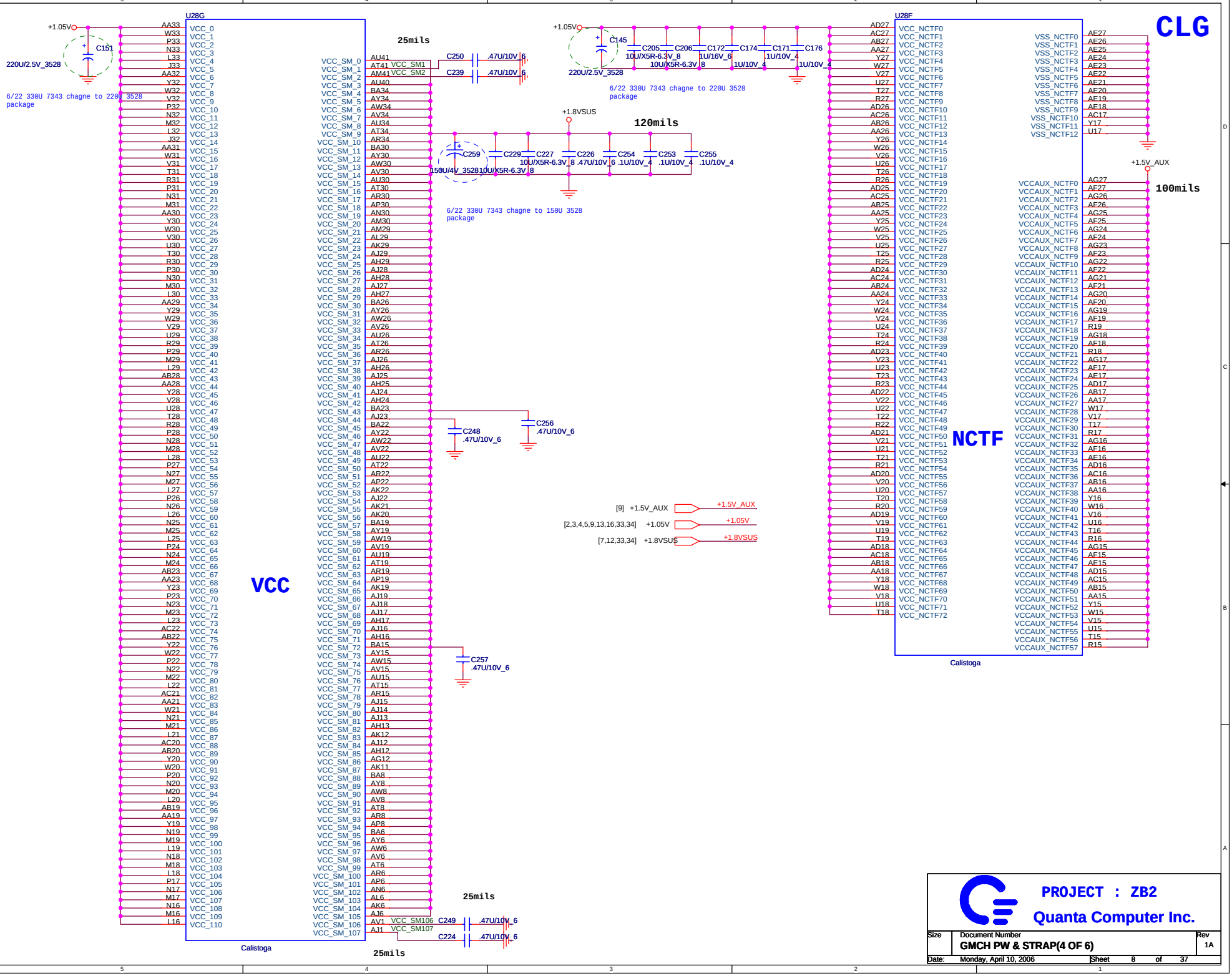
U28G
VCC
Calistoga
U28F
NCTF
Calistoga
CLG
+1.05V
C151
220U/2.5V_3528
6/22 330U 7343 chagne to 220U 3528 package
C145
C205
C206
C172
C174
C171
C176
10U/X5R-6.3V_8
1U/16V_6
1U/10V_4
6/22 330U 7343 chagne to 220U 3528 package
+1.8VSUS
120mils
C259
150U/4V_3528
C229
C227
C226
C254
C253
C255
10U/X5R-6.3V_8
.47U/10V_6
.1U/10V_4
6/22 330U 7343 chagne to 150U 3528 package
25mils
C250
C239
.47U/10V_6
C248
C256
C257
C249
C224
[9] +1.5V_AUX
[2,3,4,5,9,13,16,33,34] +1.05V
[7,12,33,34] +1.8VSUS
+1.5V_AUX
100mils
PROJECT : ZB2
Quanta Computer Inc.
Size
Document Number
GMCH PW & STRAP(4 OF 6)
Rev
1A
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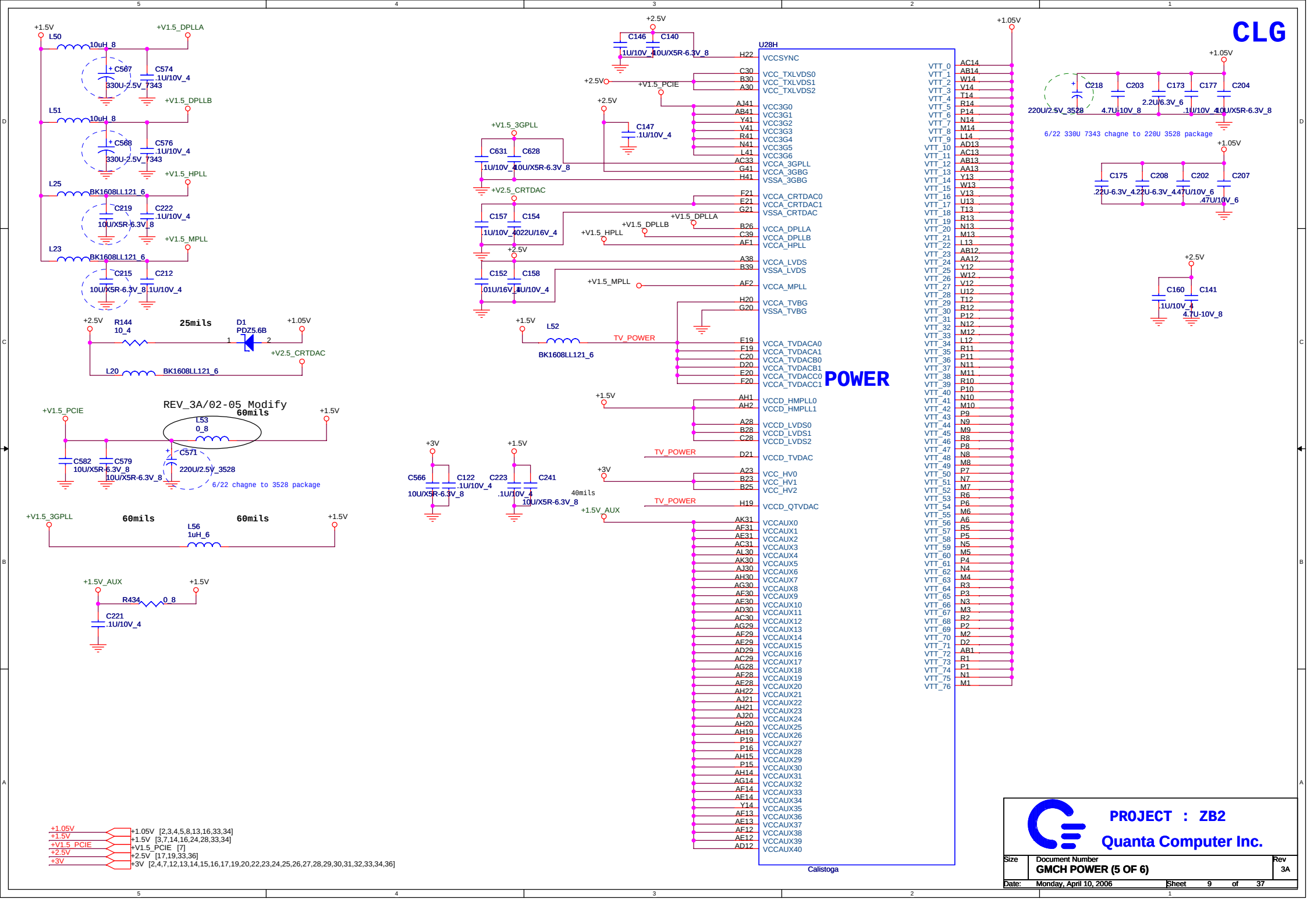
CLG
POWER
U28H
Calistoga
+1.5V
+V1.5_DPLLA
L50
10uH_8
C567
330U-2.5V_7343
C574
.1U/10V_4
+V1.5_DPLLB
L51
C568
C576
+V1.5_HPLL
L25
BK1608LL121_6
C219
10U/X5R-6.3V_8
C222
+V1.5_MPLL
L23
C215
C212
+2.5V
R144
10_4
25mils
D1
PDZ5.6B
+1.05V
+V2.5_CRTDAC
L20
REV_3A/02-05 Modify
+V1.5_PCIE
60mils
L53
0_8
C582
C579
C571
220U/2.5V_3528
6/22 chagne to 3528 package
+V1.5_3GPLL
L56
1uH_6
+1.5V_AUX
R434
C221
C146
C140
1U/10V_4
10U/X5R-6.3V_8
C147
C631
C628
C157
C154
22U/16V_4
C152
C158
01U/16V_4
L52
TV_POWER
C566
C122
C223
C241
40mils
H22 VCCSYNC
C30 VCC_TXLVDS0
B30 VCC_TXLVDS1
A30 VCC_TXLVDS2
AJ41 VCC3G0
AB41 VCC3G1
Y41 VCC3G2
V41 VCC3G3
R41 VCC3G4
N41 VCC3G5
L41 VCC3G6
AC33 VCCA_3GPLL
G41 VCCA_3GBG
H41 VSSA_3GBG
F21 VCCA_CRTDAC0
E21 VCCA_CRTDAC1
G21 VSSA_CRTDAC
B26 VCCA_DPLLA
C39 VCCA_DPLLB
AF1 VCCA_HPLL
A38 VCCA_LVDS
B39 VSSA_LVDS
AF2 VCCA_MPLL
H20 VCCA_TVBG
G20 VSSA_TVBG
E19 VCCA_TVDACA0
F19 VCCA_TVDACA1
C20 VCCA_TVDACB0
D20 VCCA_TVDACB1
E20 VCCA_TVDACC0
F20 VCCA_TVDACC1
AH1 VCCD_HMPLL0
AH2 VCCD_HMPLL1
A28 VCCD_LVDS0
B28 VCCD_LVDS1
C28 VCCD_LVDS2
D21 VCCD_TVDAC
A23 VCC_HV0
B23 VCC_HV1
B25 VCC_HV2
H19 VCCD_QTVDAC
AK31 VCCAUX0
AE31 VCCAUX1
AE31 VCCAUX2
AC31 VCCAUX3
AL30 VCCAUX4
AK30 VCCAUX5
AJ30 VCCAUX6
AH30 VCCAUX7
AG30 VCCAUX8
AF30 VCCAUX9
AE30 VCCAUX10
AD30 VCCAUX11
AC30 VCCAUX12
AG29 VCCAUX13
AF29 VCCAUX14
AE29 VCCAUX15
AD29 VCCAUX16
AC29 VCCAUX17
AG28 VCCAUX18
AF28 VCCAUX19
AE28 VCCAUX20
AH22 VCCAUX21
AJ21 VCCAUX22
AH21 VCCAUX23
AJ20 VCCAUX24
AH20 VCCAUX25
AH19 VCCAUX26
P19 VCCAUX27
P16 VCCAUX28
AH15 VCCAUX29
P15 VCCAUX30
AH14 VCCAUX31
AG14 VCCAUX32
AF14 VCCAUX33
AE14 VCCAUX34
Y14 VCCAUX35
AF13 VCCAUX36
AE13 VCCAUX37
AF12 VCCAUX38
AE12 VCCAUX39
AD12 VCCAUX40
VTT_0 AC14
VTT_1 AB14
VTT_2 W14
VTT_3 V14
VTT_4 T14
VTT_5 R14
VTT_6 P14
VTT_7 N14
VTT_8 M14
VTT_9 L14
VTT_10 AD13
VTT_11 AC13
VTT_12 AB13
VTT_13 AA13
VTT_14 Y13
VTT_15 W13
VTT_16 V13
VTT_17 U13
VTT_18 T13
VTT_19 R13
VTT_20 N13
VTT_21 M13
VTT_22 L13
VTT_23 AB12
VTT_24 AA12
VTT_25 Y12
VTT_26 W12
VTT_27 V12
VTT_28 U12
VTT_29 T12
VTT_30 R12
VTT_31 P12
VTT_32 N12
VTT_33 M12
VTT_34 L12
VTT_35 R11
VTT_36 P11
VTT_37 N11
VTT_38 M11
VTT_39 R10
VTT_40 P10
VTT_41 N10
VTT_42 M10
VTT_43 P9
VTT_44 N9
VTT_45 M9
VTT_46 R8
VTT_47 P8
VTT_48 N8
VTT_49 M8
VTT_50 P7
VTT_51 N7
VTT_52 M7
VTT_53 R6
VTT_54 P6
VTT_55 M6
VTT_56 A6
VTT_57 R5
VTT_58 P5
VTT_59 N5
VTT_60 M5
VTT_61 P4
VTT_62 N4
VTT_63 M4
VTT_64 R3
VTT_65 P3
VTT_66 N3
VTT_67 M3
VTT_68 R2
VTT_69 P2
VTT_70 M2
VTT_71 D2
VTT_72 AB1
VTT_73 R1
VTT_74 P1
VTT_75 N1
VTT_76 M1
C218
C203
C173
C177
C204
220U/2.5V_3528
4.7U-10V_8
2.2U/6.3V_6
.1U/10V_4
10U/X5R-6.3V_8
6/22 330U 7343 chagne to 220U 3528 package
C175
C208
C202
C207
.22U-6.3V_4
.22U-6.3V_4
4.47U/10V_6
.47U/10V_6
C160
C141
4.7U-10V_8
+1.05V [2,3,4,5,8,13,16,33,34]
+1.5V [3,7,14,16,24,28,33,34]
+V1.5_PCIE [7]
+2.5V [17,19,33,36]
+3V [2,4,7,12,13,14,15,16,17,19,20,22,23,24,25,26,27,28,29,30,31,32,33,34,36]
PROJECT : ZB2
Quanta Computer Inc.
Size
Document Number
GMCH POWER (5 OF 6)
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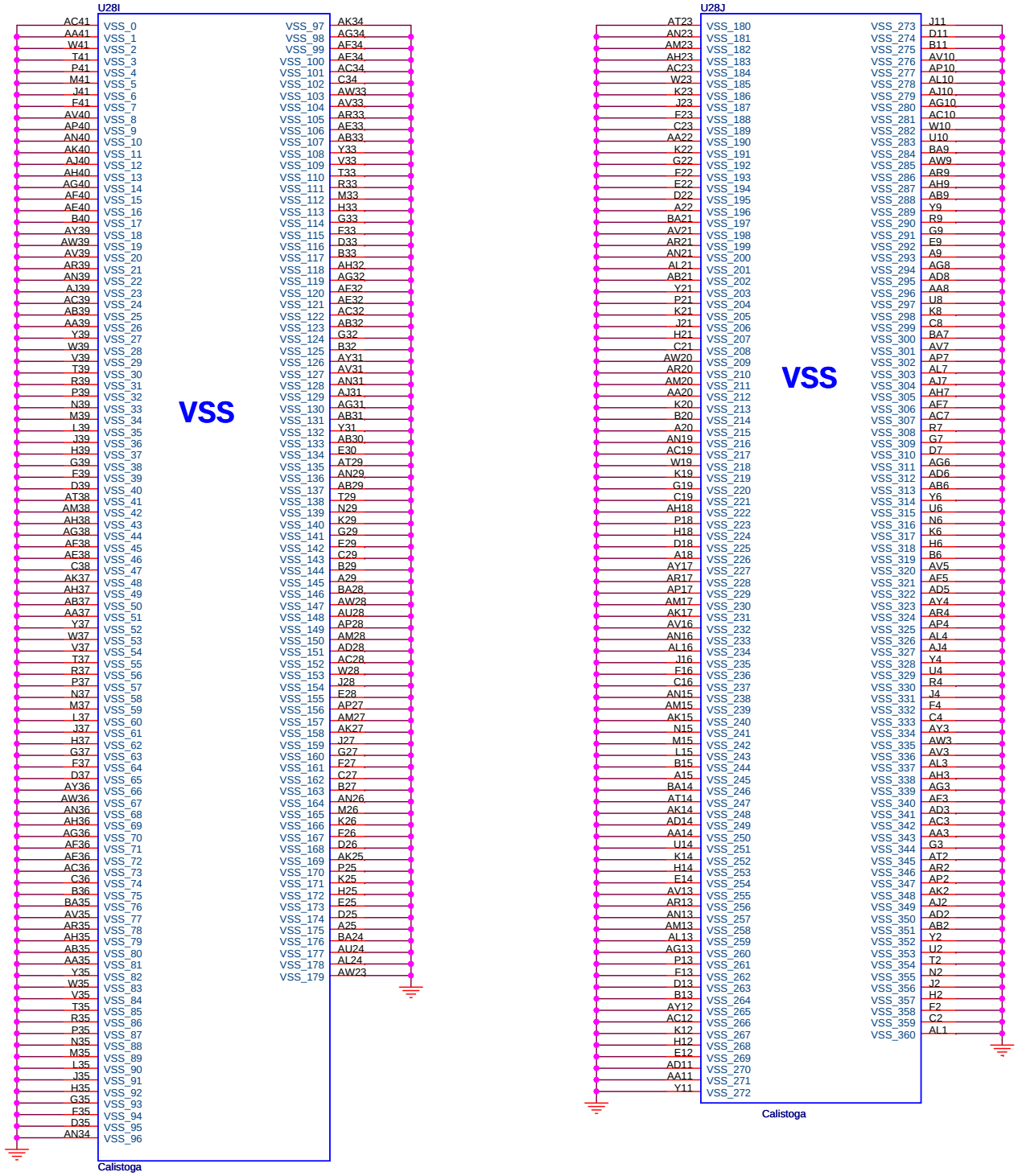

CLG

PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH GND(6 OF 6)	1A

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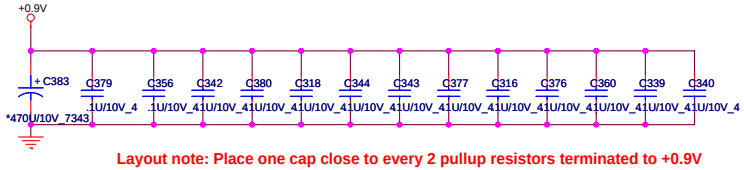
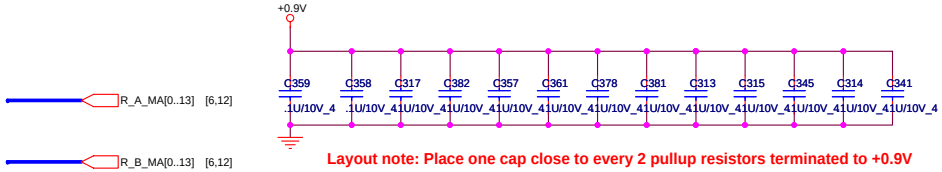
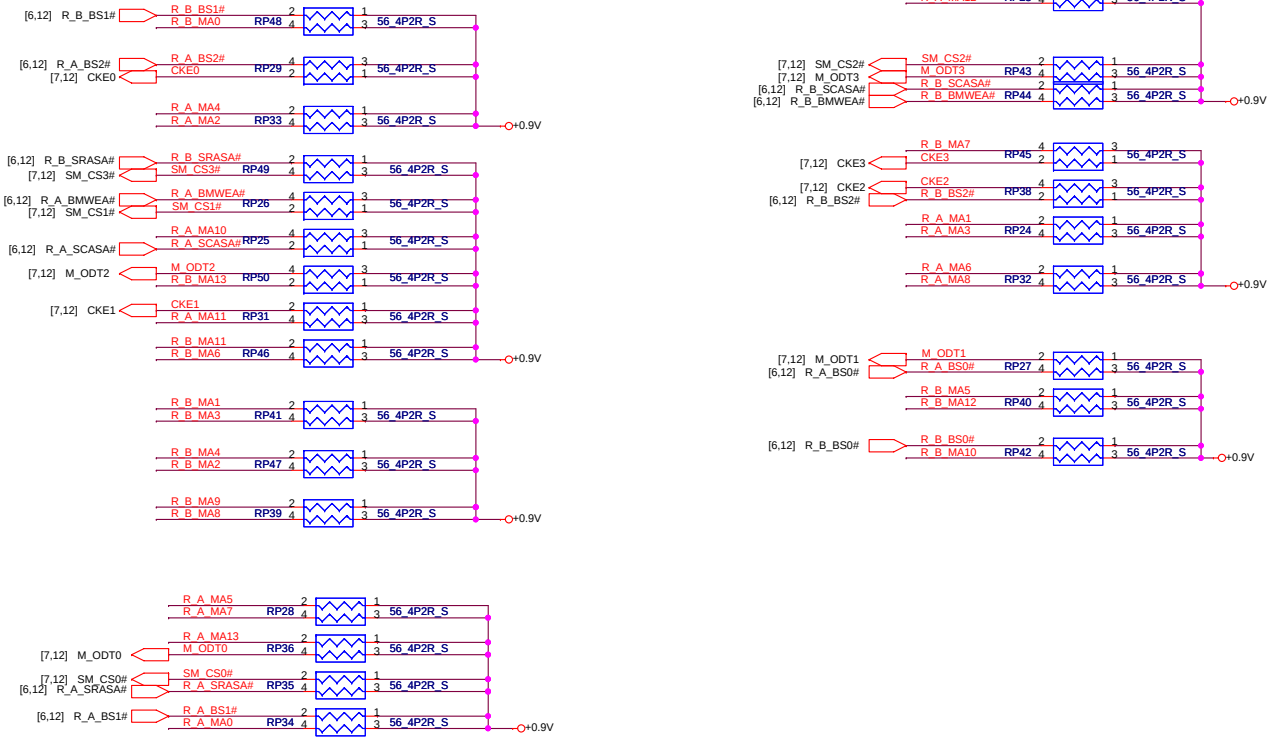


Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9V



PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 TERMINATION	1A

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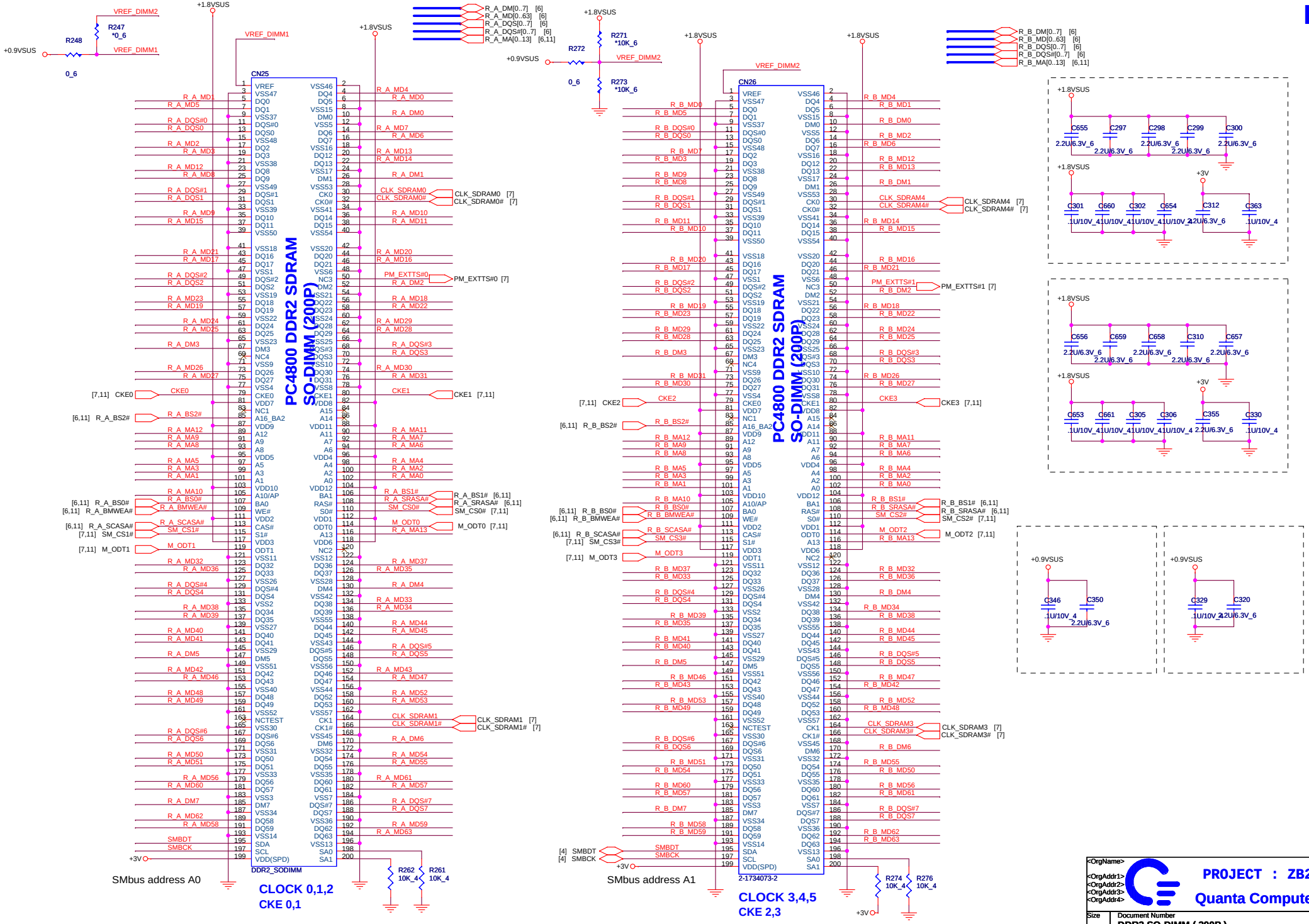
DDR



<OrgName>	PROJECT : ZB2	
<OrgAddr1> <OrgAddr2> <OrgAddr3> <OrgAddr4>	Quanta Computer Inc.	
Size	Document Number: DDR2 SO-DIMM (200P)	Rev: 1A
Date: Monday, April 10, 2006	Sheet 12 of 37	

CLG

CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF

C643 15P-50V_4 — Y5 32.768KHZ — R470 10M_6 — C651 15P-50V_4 — CLK_32KX1 / CLK_32KX2

REV_3B/03-14 Modify

ICH7 internal VR enable strap

	INTVRMEN
Enable (default)	1
Disable	0

VCCRTC — R251 332K/F_4 — R253 *0_4 — RTCRST# — SM_INTRUDER# — ICH_INTVRMEN

U34A

RTC: RTCX1, RTCX2, RTCRST#, INTRUDER#, INTVRMEN

LPC: LAD0–LAD3, LDRQ0#, LDRQ1#/GPIO23, LFRAME#

LAN: EE_CS, EE_SHCLK, EE_DOUT, EE_DIN, LAN_CLK, LAN_RSTSYNC, LAN_RXD0–2, LAN_TXD0–2

CPU: A20GATE, A20M#, CPUSLP#, TP1/DPRSTP#, TP2/DPSLP#, FERR#, GPIO49/CPUPWRGD, IGNNE#, INIT3_3V#, INIT#, INTR, RCIN#, NMI, SMI#, STPCLK#, THERMTRIP#

AC-97/AZALIA: ACZ_BIT_CLK, ACZ_SYNC, ACZ_RST#, ACZ_SDIN0–2, ACZ_SDOUT

SATA: SATA0RXN/RXP, SATA0TXN/TXP, SATA2RXN/RXP, SATA2TXN/TXP, SATA_CLKN/CLKP, SATARBIASN/P

IDE: DD0–DD15, DA0–DA2, DIOR#, DIOW#, DDACK#, IDEIRQ, IORDY, DDREQ, DCS1#, DCS3#

ICH7-M

+3V — R256 10K_4 — LPC_DRQ0# — R249 10K_4 — LPC_DRQ1#

+3V — R211 10K_4 — RCIN# — R227 10K_4 — GATEA20

R267 39_4 — C354 *22P_4 — CD_BITCLKA_MDC [28] — CD_BITCLKA_SB — R469 39_4 — C649 *22P_4 — CD_BITCLKA [28]

[28] CD_SYNC_MDC — R244 39_4 — C284 *22P_4

[28] CD_SYNC — R270 39_4 — C367 *22P_4 — CD_SYNC_SB

[28] CD_RESET#_MDC — R240 39_4 — C280 *22P_4

[28] CD_RESET# — R275 39_4 — C368 *22P_4 — CD_RESET#_SB

[28] CD_SDOUTA_MDC — R268 39_4 — C365 *22P_4

[28] CD_SDOUTA — R269 39_4 — C366 *22P_4 — CD_SDOUTA_SB

[28] CD_SDIN0 / [28] CD_SDIN1 — T154 — ACZ_SDIN2

CD_SDOUTA_SB — CD_SYNC_SB — CD_RESET#_SB — CD_BITCLKA_SB — SATA_LED#

[31] SATA_LED#

[23] SATA_RXN0 / [23] SATA_RXP0 / [23] SATA_TXN0 / [23] SATA_TXP0 — C646 *SH_SP@.01U-16V_4 SATA_TXN0_C — C647 *SH_SP@.01U-16V_4 SATA_TXP0_C

T148 / T76 / T152 / T149

[4] CLK_PCIE_SATA# / [4] CLK_PCIE_SATA

R246 24.9/F_4 SATA_BIAS — Place within 500 mils of ICH7 — 25mils/15mils

[23] PDIOR# / [23] PDIOW# / [23] PDDACK# / [23] IRQ14 / [23] PHDRDY / [23] PDDREQ — IRQ14 / PHDRDY

LAD0–LAD3 → LAD0/FWH0 [30] … LAD3/FWH3 [30]

LDRQ0# LPC_DRQ0# / LDRQ1# LPC_DRQ1#

LFRAME# → LFRAME#/FWH4 [30]

A20GATE GATEA20 → GATEA20 [30] / H_A20M# [2]

CPUSLP# — TP_H_CPUSLP# — R210 *0_4 — H_CPUSLP# [2,5]

TP1/DPRSTP# — H_DPRSTP#_R — R203 0_4 — ICH_DPRSTP# [2,32]

TP2/DPSLP# — H_DPSLP#_R — R202 0_4 — H_DPSLP# [2]

FERR# → H_FERR# [2]

GPIO49/CPUPWRGD — R214 0_4 — H_PWRGD [2]

+1.05V — R199 *56.2/F_4 — R200 *56.2/F_4 — R217 56.2/F_4

IGNNE# → H_IGNNE# [2]

INIT3_3V# — T60

INIT# → H_INIT# [2]

INTR → H_INTR [2]

RCIN# → RCIN# [30]

+1.05V — R201 56.2/F_4

NMI → H_NMI [2]

SMI# — H_SMI#_R — R216 0_4 — H_SMI# [2]

STPCLK# → H_STPCLK# [2]

THERMTRIP# — H_THERMTRIP_R — R204 24.9/F_4 — PM_THRMTRIP# [2,7]

Should be 2" close ICH7

PDD[15:0] [23]

PDA[2:0] [23]

PDCS1# [23] / PDCS3# [23]

RTC

+3VPCU — D3 CH500H-40 — VCCRTC — C349 1U/16V_6

+5VPCU — 20MIL — 20MIL

R382 1.2K_6 — VCCRTC_1 — R385 1K_4 — VCCRTC_2 — Q15 MMBT3904 — VCCRTC_4

R384 4.7K_4

R381 15K_6

VCCRTC_3 — D5 CH500H-40 — R263 20K_6 — RTCRST#

R266 1K_4

R250 1M/F_6

C348 1U/16V_6

JP2 *SHORT_ PAD1

SM_INTRUDER# — Internal PU

CN19 BATCON

REV_2A/12-23 Modify

PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M HOST (1 OF 4)	3B
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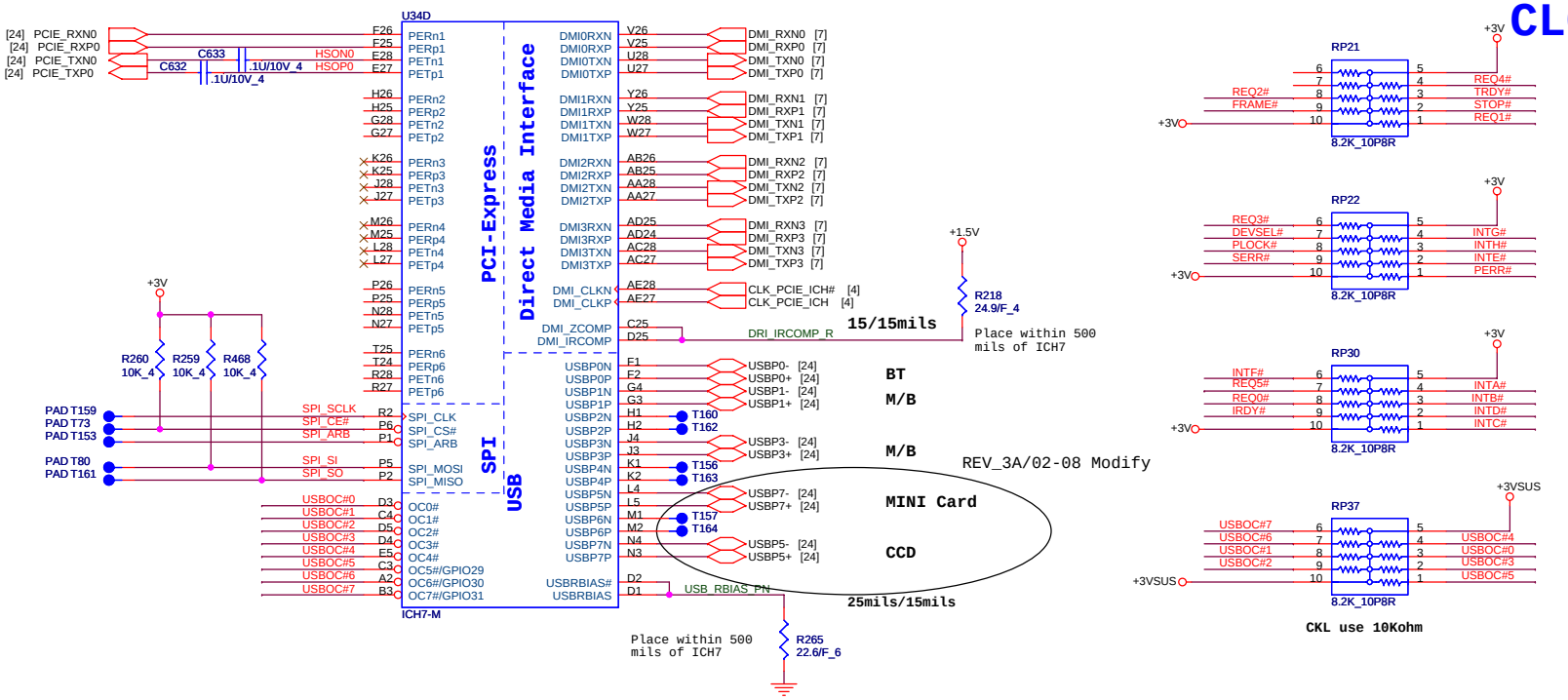

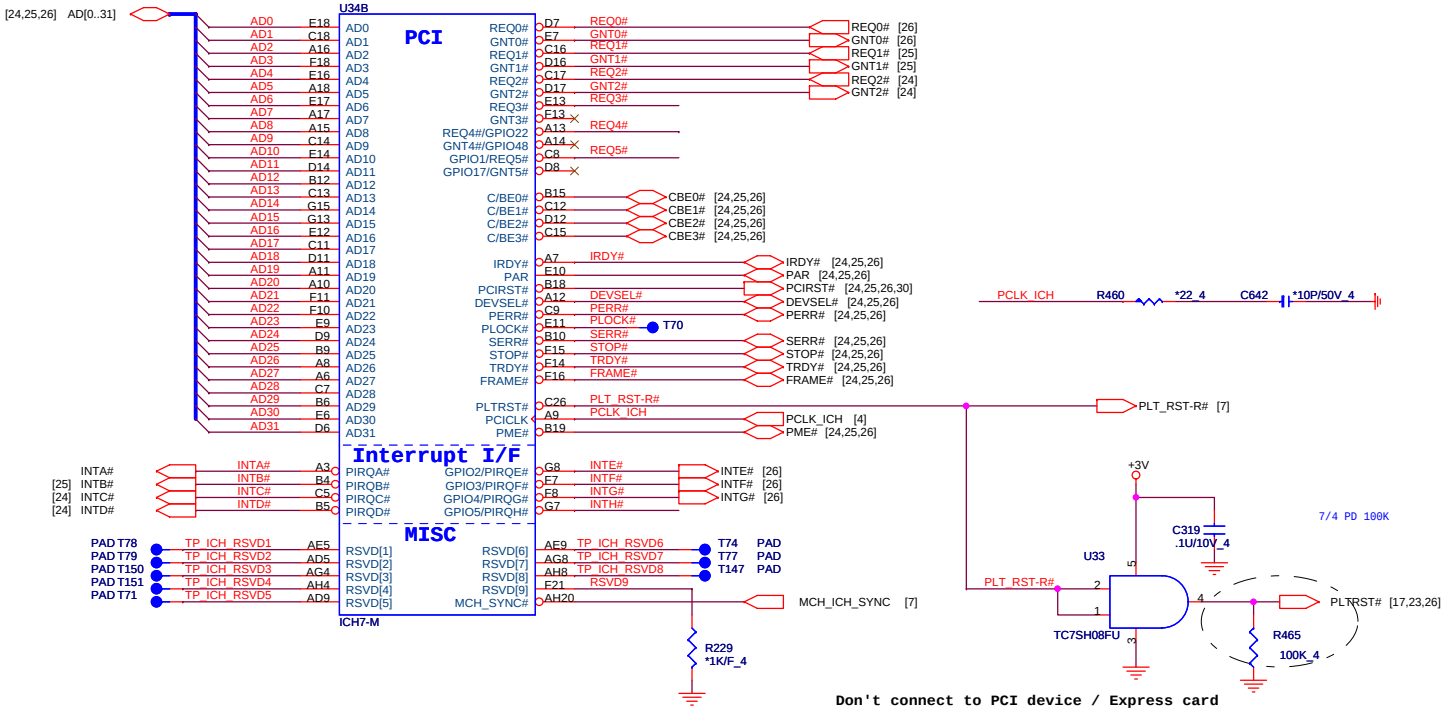

ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCCARD	AD25	REQ0# / GNT0#	INT E/F/G#
MINIPCI	AD19	REQ2# / GNT2#	INT C/D#
LAN	AD16	REQ1# / GNT1#	INT B#

PROJECT : ZB2

Quanta Computer Inc.

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CardReader

CLG

PM_DPRSLPVR
C730
*.1U-10V_4
REV_3A/02-08 Modify

to Clock Gen & DIMM

U34C
ICH7-M

SMB
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1

SATA GPIO
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP

Clocks
CLK14
CLK48
SUSCLK

SYS Power MGT
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#

GPIO
SPKR
SUS_STAT#
SYS_RST#
RI#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39

R453 *1K/F_4
[4,24] PCLK_SMB
[4,24] PDAT_SMB
PCLK_SMB C22
PDAT_SMB B22
SMB_LINK_ALERT# A26
SMLINK0 B25
SMLINK1 A25
T140 T141 T142
[28] PCSPK
[26] RI#
RI# A28
[26] LPC_PD#
[2] SYS_RST#
LPC_PD# A19
SYS_RST# A27
A22
R449 *10K_4
R237 0_4
[7] PM_BMBUSY# AB18
R219 *10K/F_4
R236 *10K/F_4
+3V_S5
R443 10K_4
B23
[4] PM_STPPCI#
[4] PM_STPCPU#
R235 0_4
R221 0_4
PM_STPPCI_ICH# AC20
PM_STPCPU_ICH# AF21
REV_2A/12-20 Add Pull-Up
Note: Connect to EC; Reserve PH/3V
T144 A21
T143 B21
T59 E23
[24,25,26,30] CLKRUN#
CLKRUN# AG18
R223 10K/F_4
T68 AC19
T155 U2
[24] PCIE_WAKE#
[24,26,30] SERIRQ
PCIE_WAKE# F20
SERIRQ AH21
AF20
[2] THERM_ALERT#
VR_PWRGD_CK410 AD22
R228 10K_4
[22] MONITOR_PLUG#
[30] SCI#
[30] KBSMI#
R239 0_4
R456 0_4
RUNTIME_SCI#_R AC21
EXTSMI#_R AC18 E21

R454 *8.2K_4
R457 33_4
AF19 AH18 AH19 AE19
AC1 B2
14M_ICH [4]
CLKUSB_48 [4]
C20 T65
B24 D23 F22
R220 100/F_4
R224 100/F_4
SUSB# [30]
SUSC# [30]
T61
AA4 ICH_PWROK
AC22 PM_DPRSLPVR
PM_DPRSLPVR [32]
C21 PM_BATLOW#_R
C23 DNBSWON#
DNBSWON# [30]
C19 R257 0_4 R258 10K_4
Y4 R255 10_4
RSMRST#
RSMRST# [30]
E20 A20 E19 R4 E22 R3 D20 AD21 AD20 AE20
T63 T145 T64 T62 T66 T67 T146
EMAIL_LED#
WAKE_SCI#_R
EMAIL_LED# [31]
LID591#_SB [22]
BOARD_ID1
BOARD_ID0

GPIO25 /Suspend rail is a HW strap , don't pull down .

CLKRUN# R234 8.2K_4
SERIRQ R225 8.2K_4
RUNTIME_SCI#_R R238 10K_4

DNBSWON# R222 10K_4
SYS_RST# R448 10K_4
PM_BATLOW#_R R230 10K_4

RI# R436 10K_4
SMB_LINK_ALERT# R437 10K_4
SMLINK0 R439 10K_4
SMLINK1 R440 10K_4
EXTSMI#_R R455 10K_4
WAKE_SCI#_R R527 10K_4
REV_2A/12-20 Add Pull-Up

PCLK_SMB R447 2.2K_4
PDAT_SMB R442 2.2K_4
PCIE_WAKE# R233 1K_4

R452 *10K_4
BOARD_ID0
R450 10K_4
R441 *10K_4
BOARD_ID1
R444 10K_4
+3VSUS
C352 .022U/16V_4
U31
[30] EC_PWRGD
[7,32] IMVP_PWRGD
TC7SH08FU
ICH_PWROK
R435 10K_4

A1A:Change to inverter for VR_PWRGD_CK410
R226 100K_4
U9
VR_PWRGD_CK410
VR_PWRGD_CK410# [4,32]
SN74LVC1G04DCKR
Note: External pull-up 3V

CLKUSB_48
R467 10_4
C648 10P/50V_4
14M_ICH
R466 33_4
C650 10P/50V_4

REV_3C/03-29 Modify

Board ID		CardReader	CCD
ID0 , ID1	00	X	X
ID0 , ID1	01	X	V
ID0 , ID1	10	V	X
ID0 , ID1	11	V	V

REV_3A/02-09 Add
VR_PWRGD_CK410
Q29
*2N7002
VR_PWRGD_CK410_R#
R542 *100K_4
VR_PWRGD_CK410_R# [4]

REV_3A/02-08 Add
VR_PWRGD_CK410# [4,32]
Q28
*2N7002
R534 *100K_4

PROJECT : ZB2
Quanta Computer Inc.

Size	Document Number	Rev
	ICH7-M GPIO (3 OF 4)	3C
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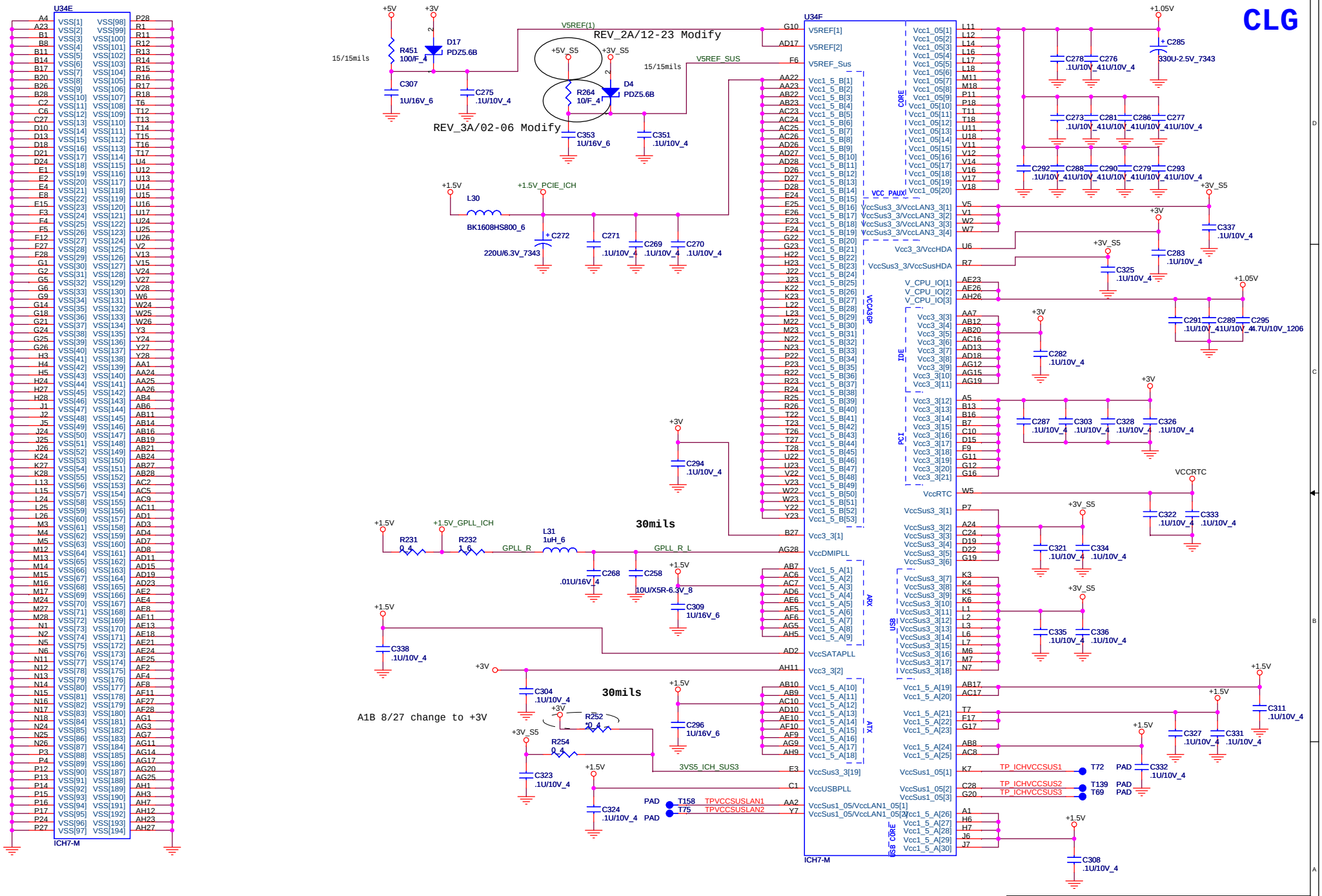
CLG
U34E
ICH7-M
U34F
ICH7-M
REV_2A/12-23 Modify
REV_3A/02-06 Modify
A1B 8/27 change to +3V
30mils
30mils
V5REF(1)
V5REF_SUS
3VS5_ICH_SUS3
TP_ICHVCCSUS1
TP_ICHVCCSUS2
TP_ICHVCCSUS3
TPVCCSUSLAN1
TPVCCSUSLAN2
PROJECT : ZB2
Quanta Computer Inc.
ICH7-M POWER (4 OF 4)
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VGA

NOTE: some of the PCIE testpoints will be available trought via on traces.

Note : If Use Internal VGA Please NC "EV@xxx" Parts

[7] GMCHEXP_TXP[0..15]
[7] GMCHEXP_TXN[0..15]
[7] GMCHEXP_RXP[0..15]
[7] GMCHEXP_RXN[0..15]

U23A — PART 1 OF 7 — PCI-EXPRESS INTERFACE

GMCHEXP_TXP0	AJ31	PCIE_RX0P	PCIE_TX0P	AK27	V_GMCHEXP_RXP0 C523 EV@.1U-10V_4 — GMCHEXP_RXP0
GMCHEXP_TXN0	AH31	PCIE_RX0N	PCIE_TX0N	AJ27	V_GMCHEXP_RXN0 C524 EV@.1U-10V_4 — GMCHEXP_RXN0
GMCHEXP_TXP1	AH30	PCIE_RX1P	PCIE_TX1P	AJ25	V_GMCHEXP_RXP1 C546 EV@.1U-10V_4 — GMCHEXP_RXP1
GMCHEXP_TXN1	AG30	PCIE_RX1N	PCIE_TX1N	AH25	V_GMCHEXP_RXN1 C547 EV@.1U-10V_4 — GMCHEXP_RXN1
GMCHEXP_TXP2	AG32	PCIE_RX2P	PCIE_TX2P	AH28	V_GMCHEXP_RXP2 C525 EV@.1U-10V_4 — GMCHEXP_RXP2
GMCHEXP_TXN2	AF32	PCIE_RX2N	PCIE_TX2N	AG28	V_GMCHEXP_RXN2 C526 EV@.1U-10V_4 — GMCHEXP_RXN2
GMCHEXP_TXP3	AF31	PCIE_RX3P	PCIE_TX3P	AG27	V_GMCHEXP_RXP3 C548 EV@.1U-10V_4 — GMCHEXP_RXP3
GMCHEXP_TXN3	AE31	PCIE_RX3N	PCIE_TX3N	AF27	V_GMCHEXP_RXN3 C549 EV@.1U-10V_4 — GMCHEXP_RXN3
GMCHEXP_TXP4	AE30	PCIE_RX4P	PCIE_TX4P	AE25	V_GMCHEXP_RXP4 C527 EV@.1U-10V_4 — GMCHEXP_RXP4
GMCHEXP_TXN4	AD30	PCIE_RX4N	PCIE_TX4N	AE25	V_GMCHEXP_RXN4 C528 EV@.1U-10V_4 — GMCHEXP_RXN4
GMCHEXP_TXP5	AD32	PCIE_RX5P	PCIE_TX5P	AE28	V_GMCHEXP_RXP5 C550 EV@.1U-10V_4 — GMCHEXP_RXP5
GMCHEXP_TXN5	AC32	PCIE_RX5N	PCIE_TX5N	AD28	V_GMCHEXP_RXN5 C551 EV@.1U-10V_4 — GMCHEXP_RXN5
GMCHEXP_TXP6	AC31	PCIE_RX6P	PCIE_TX6P	AD27	V_GMCHEXP_RXP6 C529 EV@.1U-10V_4 — GMCHEXP_RXP6
GMCHEXP_TXN6	AB31	PCIE_RX6N	PCIE_TX6N	AC27	V_GMCHEXP_RXN6 C530 EV@.1U-10V_4 — GMCHEXP_RXN6
GMCHEXP_TXP7	AB30	PCIE_RX7P	PCIE_TX7P	AC25	V_GMCHEXP_RXP7 C552 EV@.1U-10V_4 — GMCHEXP_RXP7
GMCHEXP_TXN7	AA30	PCIE_RX7N	PCIE_TX7N	AB25	V_GMCHEXP_RXN7 C553 EV@.1U-10V_4 — GMCHEXP_RXN7
GMCHEXP_TXP8	AA32	PCIE_RX8P	PCIE_TX8P	AB28	V_GMCHEXP_RXP8 C531 EV@.1U-10V_4 — GMCHEXP_RXP8
GMCHEXP_TXN8	Y32	PCIE_RX8N	PCIE_TX8N	AA28	V_GMCHEXP_RXN8 C532 EV@.1U-10V_4 — GMCHEXP_RXN8
GMCHEXP_TXP9	Y31	PCIE_RX9P	PCIE_TX9P	AA27	V_GMCHEXP_RXP9 C554 EV@.1U-10V_4 — GMCHEXP_RXP9
GMCHEXP_TXN9	W31	PCIE_RX9N	PCIE_TX9N	Y27	V_GMCHEXP_RXN9 C555 EV@.1U-10V_4 — GMCHEXP_RXN9
GMCHEXP_TXP10	W30	PCIE_RX10P	PCIE_TX10P	Y25	V_GMCHEXP_RXP10 C533 EV@.1U-10V_4 — GMCHEXP_RXP10
GMCHEXP_TXN10	V30	PCIE_RX10N	PCIE_TX10N	W25	V_GMCHEXP_RXN10 C534 EV@.1U-10V_4 — GMCHEXP_RXN10
GMCHEXP_TXP11	V32	PCIE_RX11P	PCIE_TX11P	W28	V_GMCHEXP_RXP11 C556 EV@.1U-10V_4 — GMCHEXP_RXP11
GMCHEXP_TXN11	U32	PCIE_RX11N	PCIE_TX11N	V28	V_GMCHEXP_RXN11 C557 EV@.1U-10V_4 — GMCHEXP_RXN11
GMCHEXP_TXP12	U31	PCIE_RX12P	PCIE_TX12P	V27	V_GMCHEXP_RXP12 C535 EV@.1U-10V_4 — GMCHEXP_RXP12
GMCHEXP_TXN12	T31	PCIE_RX12N	PCIE_TX12N	U27	V_GMCHEXP_RXN12 C536 EV@.1U-10V_4 — GMCHEXP_RXN12
GMCHEXP_TXP13	T30	PCIE_RX13P	PCIE_TX13P	U25	V_GMCHEXP_RXP13 C537 EV@.1U-10V_4 — GMCHEXP_RXP13
GMCHEXP_TXN13	R30	PCIE_RX13N	PCIE_TX13N	T25	V_GMCHEXP_RXN13 C538 EV@.1U-10V_4 — GMCHEXP_RXN13
GMCHEXP_TXP14	R32	PCIE_RX14P	PCIE_TX14P	T28	V_GMCHEXP_RXP14 C539 EV@.1U-10V_4 — GMCHEXP_RXP14
GMCHEXP_TXN14	P32	PCIE_RX14N	PCIE_TX14N	R28	V_GMCHEXP_RXN14 C540 EV@.1U-10V_4 — GMCHEXP_RXN14
GMCHEXP_TXP15	P31	PCIE_RX15P	PCIE_TX15P	R27	V_GMCHEXP_RXP15 C542 EV@.1U-10V_4 — GMCHEXP_RXP15
GMCHEXP_TXN15	N31	PCIE_RX15N	PCIE_TX15N	P27	V_GMCHEXP_RXN15 C541 EV@.1U-10V_4 — GMCHEXP_RXN15

Clock: [4] CLK_PCIE_VGA → AL28 PCIE_REFCLKP; [4] CLK_PCIE_VGA# → AK28 PCIE_REFCLKN
[14,23,26] PLTRST# → PLTRST# → AG24 PERSTB
AA24 PCIE_TEST
AF24 PERSTB_MASK — Tie To VSS
Calibration: AF24 PCIE_CALRN — R115 EV@2K/F_4 — +1.2V; AD24 PCIE_CALRP — R104 EV@562/F_4; AB24 PCIE_CALI — R103 EV@1.47K/F_4
EV@M56-P B11 LF
R101 EV@10K_4

REV_02/10-28 Add

MEMORY CLOCK SPREAD SPECTRUM

U25 EV@CY25819 MK1726-8
XT_IN — 1726_S0 — 1726_CKO — OSC_SPREAD R373 EV@33_4
XIN, VSS, SRS, SSCLK; XOUT, VDD, PD, REF
XT_OUT — MK1726_VDD — MK_PD — MK_27M
R386 27MOUT EV@0_4
C544 EV@.1U-10V_4; L48 EV@BLM18PG181SN1D_6 +3V; C545 EV@22U-16V_1210
+3V — R375 *EV@10K_4 — 1726_S0 — R374 *EV@10K_4
27M_IN — EV@121/F_4 R383 — C516 EV@10P/50V_4 — R380 EV@71.5/F_4
MK_PD — R391 *EV@10K_4

U23B — PART 2 OF 7 — VIDEO & MULTIMEDIA

Expand GPIO: TP11 AG8, TP4 AH7, TP13 AG9, TP5 AH8, TP12 AJ8, TP9 AH9, TP14 AG10, TP15 AF10, TP7 AH6, TP1 AF8, TP2 AE7, TP8 AE9, TP3 AE10, TP10 AG7, TP6 AF9, TP16 AF13, TP17 AE13
GPIO_34, GPIO_33, GPIO_32, GPIO_31, GPIO_30, GPIO_29, GPIO_28, GPIO_27, GPIO_26, GPIO_25, GPIO_24, GPIO_23, GPIO_22, GPIO_21, GPIO_20, GPIO_19, GPIO_18

VIP Host/External TMDS: NC_DVOVMODE_0 AK4, NC_DVOVMODE_1 AL4; DVPCNTL_0 AF2, DVPCNTL_1 AE1, DVPCNTL_2 AF3, DVPCLK AG1, DVPDATA_0 AG2 … DVPDATA_23 AG6
[20] MEMTYP_0 AG2, [20] MEMTYP_1 AG3, [20] MEMTYP_2 AH2, [20] MEMTYP_3 AH3

[20] CPIS_VDD_VCL — GPIO2
[20] DC_Strap2 — VID/DVO_R13 AF4; [20] DC_Strap3 — VID/DVO_R14 AF5; [20] DC_Strap4 — VID/DVO_R15 AG4
T92 AJ3; T93 AH4
[7,22] EDIDDATA — *EV@0_4 R364; [7,22] EDIDCLK — *EV@0_4 R365
T6 AJ5; T5 AH5; T4 AF6; T7 AG6

General Purpose I/O: GPIO_0 AD4 … GPIO_14 AB5, GPIO_15 AB8, GPIO_16 AA8, GPIO_17 AB7, NC_AB6
[20] GPIO0 — GPIO0 AD4
[20] GPIO1 — GPIO1 AD2
[20] GPIO2 — GPIO2 AD1
[20] GPIO3 — GPIO3 AD3
[20] GPIO4 — GPIO4 AC1
[20] GPIO5 — GPIO5 AC2
[20] GPIO6 — GPIO6 AC3
GPIO7 — GPIO7 AB2
[20] GPIO8 — GPIO8 AC5
[20] GPIO9 — GPIO9 AC4
[20] GPIO10 — GPIO10 AB3
[20] GPIO11 — GPIO11 AB4
[20] GPIO12 — GPIO12 AB5
[20] GPIO13 — GPIO13 AC5
T94 — GPIO7; T1 — GPIO10; T91 — GPIO11; T3 — GPIO12; T2 — GPIO13

[36] VGA_PWR_SW
OSC_SPREAD
VGA_ALERT# — R62 EV@0_4 — AB6
+3V — EV@499_4 R73; EV@499_4 R76 — VREFG AC8

Thermal Diode: VREFG, VGATHRM+ AG12, VGATHRM- AH12
PLL & XTAL: DPLUS, DMINUS, PVDD AJ14, PVSS AH14, MPVDD A6, MPVSS A5, XTALIN AL26, XTALOUT AM26, PLLTEST AG14
Test: TESTEN AG22
ROM: ROMCSb AC7

LVDS PLL and I/O GND: LVSSR_1 AK17, LVSSR_2 AJ19, LVSSR_3 AF18, LVSSR_4 AH17, LVSSR_5 AG17, LVSSR_6 AG19, LVSSR_7 AH19
External SSC: GENERICC AF23, LPVSS AF18
LVDS PLL and I/O GND: LVSSR_10 AE22, LVSSR_9 AF17, LVSSR_8 AF21

Integrated TMDS: TXCM AL9, TXCP AM9; TX0M AK10, TX0P AL10; TX1M AL11, TX1P AM11; TX2M AL12, TX2P AM12; TX3M AK9, TX3P AJ9; TX4M AK11, TX4P AJ11; TX5M AK12, TX5P AJ12
TPVDD AM8 — +TPVDD — C472 EV@.1U-10V_4; C470 EV@22U-16V_1210; L40 EV@BLM18PG181SN1D_6 +2.5V
TPVSS AL8
TXVDDR_1 AJ6, TXVDDR_2 AK6, TXVDDR_3 AL6, TXVDDR_4 AM6 — TXVDDR — L39 EV@BLM18PG181SN1D_6 +2.5V
TXVSSR_1 AJ7, TXVSSR_2 AK7, TXVSSR_3 AL7, TXVSSR_4 AM7, TXVSSR_5 AK8
C467 EV@22U-16V_1210; C468 EV@1U-16V_6; C469 EV@.1U-10V_4

DAC / CRT: R AK24, G AM24, B AL24
VGA_RED_V — EV@0_4 — R105 VGA_RED — VGA_RED [7,22]
VGA_GRN_V — EV@0_4 — R109 VGA_GRN — VGA_GRN [7,22]
VGA_BLU_V — EV@0_4 — R112 VGA_BLU — VGA_BLU [7,22]
HSYNC AJ23, VSYNC AL3, GENERICA AK22
HSYNC_V — EV@0_4 — R98 HSYNC — HSYNC [7,20,22]
VSYNC_V — EV@0_4 — R94 VSYNC — VSYNC [7,20,22]
GENERICB AF23 — VGA_ALERT# — R57 EV@0_4
RSET AL22 — R93 EV@499_4
AVDD_1 AL25, AVDD_2 AM25 — +AVDD — L47 EV@BLM18PG181SN1D_6 +2.5V
AVSSQ AK23, AVSSN_1 AK25, AVSSN_2 AJ24
C509 EV@1U-16V_6; C507 EV@.1U-10V_4; C506 EV@22U-16V_1210
VDD1DI AM23 — +VDDDI — L46 EV@BLM18PG181SN1D_6 +2.5V
VSS1DI AL23
C503 EV@1U-16V_6; C504 EV@.1U-10V_4; C502 EV@22U-16V_1210

DAC2 (TV/CRT2): R2 AK15, G2 AM15, B2 AL15
H2SYNC AF15, V2SYNC AG15
Y AJ15, C AJ13, COMP AH15
R2SET AK14 — R2SET — EV@715/F_4 — R82
A2VDD_1 AM16, A2VDD_2 AL16 — A2VDD — L41 EV@BLM18PG181SN1D_6 +2.5V
C475; C473; C474 EV@22U-16V_1210
A2VSS_1 AM17, A2VSS_2 AL17
EV@1U-16V; EV@.1U-10V_4
NC_A2VDDQ AL14 — +A2VDDQ — L44 EV@BLM18PG181SN1D_6 +2.5V
A2VSSQ AK13
VDD2DI AJ16 — +VDD2DI — L45 EV@BLM18PG181SN1D_6 +2.5V
VSS2DI AJ17
C489 EV@1U-16V_6; C486 EV@.1U-10V_4; C492 EV@22U-16V_1210
C498 EV@1U-16V_6; C496 EV@.1U-10V_4; C499 EV@22U-16V_1210

Monitor Interface: HPD1 AF11
DDC1DATA AH22, DDC1CLK AH23 — DDCDAT_V — EV@0_4 — R87 — DDCDAT [7,22]; DDCCLK_V — EV@0_4 — R89 — DDCCLK [7,22]
DDC2DATA AH13, DDC2CLK AG13
DDC3DATA AE12, DDC3CLK AF12 — EV@0_4 — R77 VTHM_DAT; EV@0_4 — R79 VTHM_CLK
GENERICC AF23 — GENERICC [20]

PLACE CLOSE TO ASIC
VGA_RED_V — R102 EV@150/F_4; VGA_GRN_V — R108 EV@150/F_4; VGA_BLU_V — R111 EV@150/F_4

Ba3: +AVDD — R93 EV@499_4; +2.5V
Ba5: +A2VDDQ; +2.5V

15 MIL

+3V — L36 3V_THM1 EV@BLM18PG181SN1D_6 — C462 EV@.1U-10V_4
R346 EV@10K_4; R70 EV@4.7K_4; R71 EV@4.7K_4
U21 EV@MAX6657/GMT-781-1: VCC, DXN, DXP, GND, ALERT#, SDA, SCLK, OVERT#
VGATHRM- — 10 mil trace / 10 mil space — VGATHRM+
C44 EV@2200P-50V_4
VGA_ALERT#, VTHM_DAT, VTHM_CLK, VGA_THERM# [31]

Close to pin ASIC **SLAVE ADDRESS: 9A**

VTHM_DAT — EV@0_4 R67 — VTHM_DAT_EC — Q13 EV@2N7002 — MBDATA [30,35]
VTHM_CLK — EV@0_4 R74 — VTHM_CLK_EC — Q14 EV@2N7002 — MBCLK [30,35]
+3V

PROJECT : ZB2
Quanta Computer Inc.
Size | Document Number: M52-P_MAIN_PCIE (1 of 4) | Rev: 1A
Date: Monday, April 10, 2006 | Sheet 17 of 37

RV410 MEMORY CHANNELS A and B

VGA

FOR M52P,M54P,M26X,
PIN B25 IS MA12(BA0)
PIN C25 IS MA13(BA1)
PIN E29 IS MA15(BA2)
PIN E27 IS MA14
M50P IS THE SAME EXCEPT
PIN E29 IS CSBb_1
FOR M56P
PIN B25 IS MA14(BA0)
PIN C25 IS MA15(BA1)
PIN E29 IS MA13(BA2)
PIN E27 IS MA12

Channel A

U23C

Part 3 of 7

MEMORY INTERFACE A

EV@M56-P B11 LF

FOR M52P,M54P,M26X,M50P
PIN H2 IS MAB12 (BA0)
PIN H3 IS MAB13 (BA1)
PIN D5 IS MAB15 (BA2)
PIN F5 IS MAB14
M50P IS THE SAME EXCEPT
PIN D5 IS CSBb_1
FOR M56P
PIN H2 IS MA14 (BA0)
PIN H3 IS MA15 (BA1)
PIN D5 IS MA13 (BA2)
PIN F5 IS MAB1

Channel B

U23D

Part 4 of 7

MEMORY INTERFACE B

EV@M56-P B11 LF

[21] MDA[0..63]

MAA[0..15] [21]

-DQMA[0..7] [21]

RDQSA[0..7] [21]

WDQSA[0..7] [21]

ODTA0 [21]
ODTA1 [21]

M_CLKA0 [21]
-M_CLKA0 [21]

CKEA [21]

-RASA [21]

-CASA [21]

-WEA [21]

-CSA0 [21]

M_CLKA1 [21]
-M_CLKA1 [21]

CKEA1 [21]

-RASA1 [21]

-CASA1 [21]

-WEA1 [21]

-CSAb0 [21]

+1.8V

R366 EV@100/F_4

R367 EV@100/F_4

C471 EV@.1U-10V_4

R60 EV@100/F_4

R59 EV@100/F_4

C35 EV@.1U-10V_4

R43 EV@4.7K_4

R61 EV@4.7K_4

R42 EV@2.2K_4

VRAM_REF0
VRAM_REF1

TEST_MCLK
TEST_YCLK

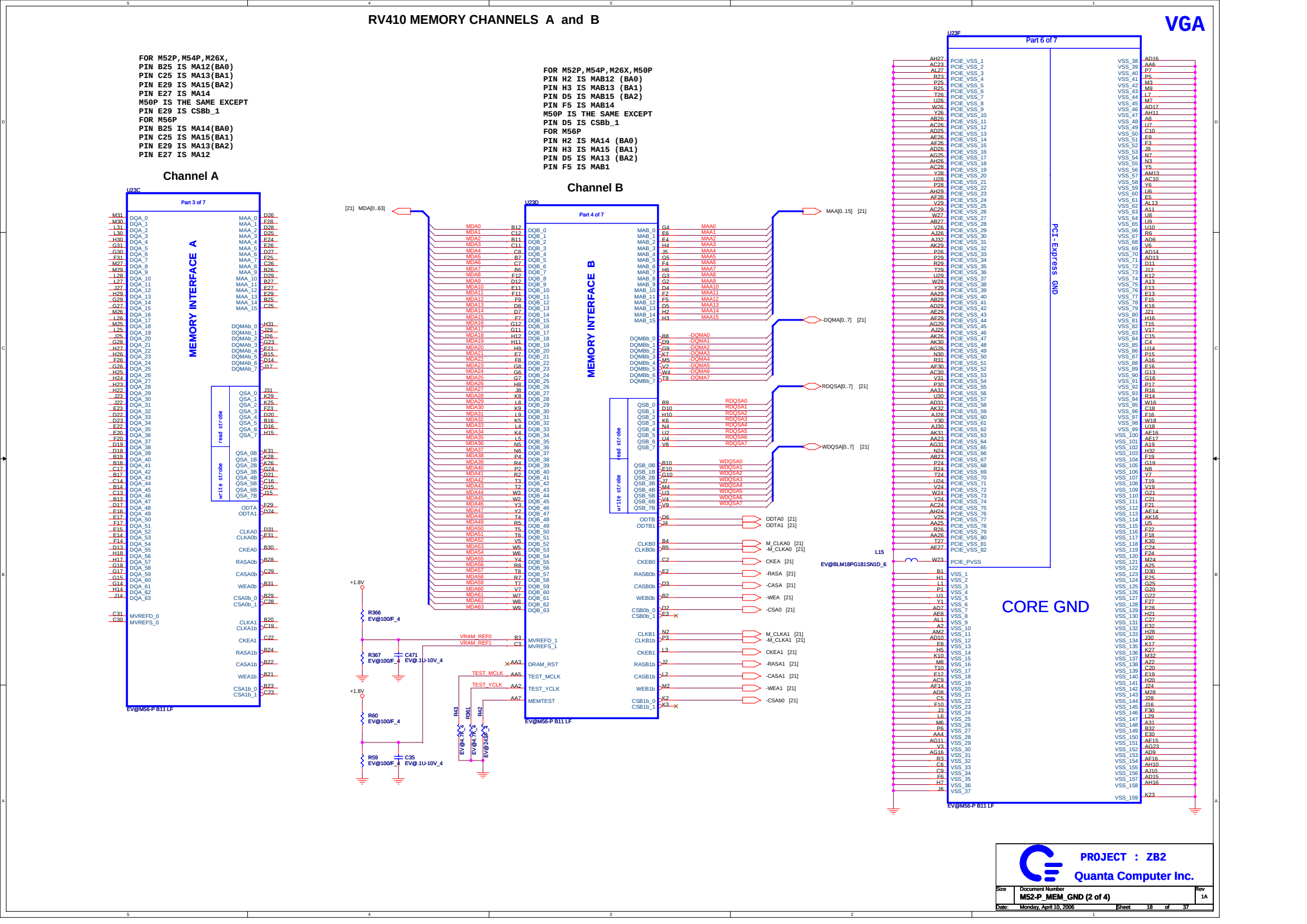
U23F

Part 6 of 7

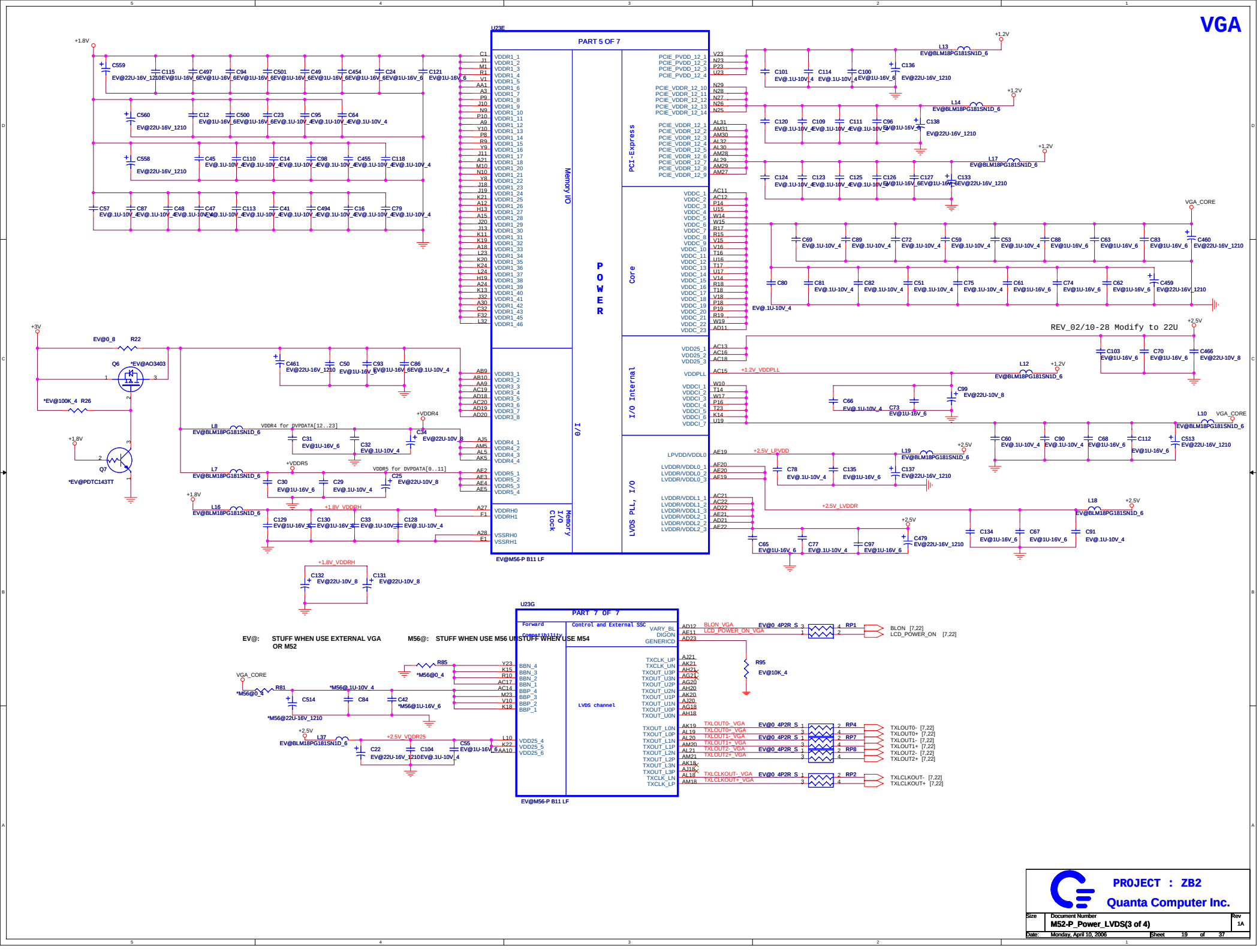
PCI-Express GND

CORE GND

L15 EV@BLM18PG181SN1D_6



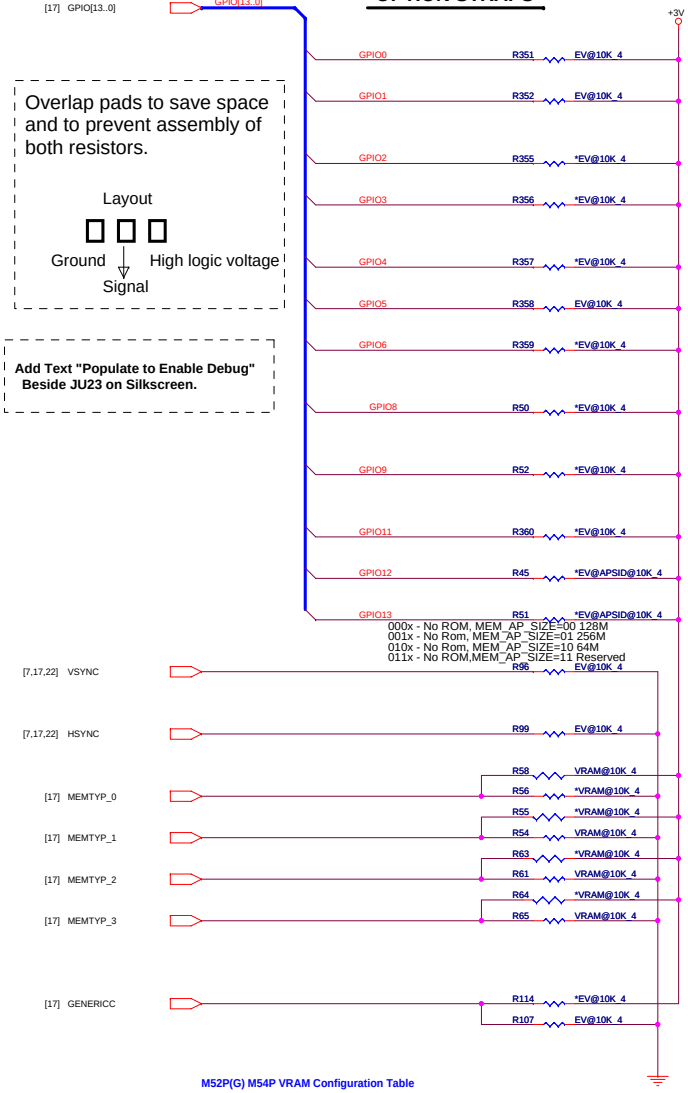
VGA


U23E
PART 5 OF 7
POWER
Memory I/O
I/O
Core
I/O Internal
LVDS PLL, I/O
Memory I/O Clock
PCI-Express
EV@M56-P B11 LF
U23G
PART 7 OF 7
Forward Compatibility
Control and External SSC
LVDS channel
EV@M56-P B11 LF
VGA_CORE
REV_02/10-28 Modify to 22U
EV@: STUFF WHEN USE EXTERNAL VGA OR M52
M56@: STUFF WHEN USE M56 UNSTUFF WHEN USE M54
PROJECT : ZB2
Quanta Computer Inc.
M52-P_Power_LVDS(3 of 4)
Monday, April 10, 2006
Sheet 19 of 37

001x - No ROM,MEM_AP_SIZE=01
256M

OPTION STRAPS

VGA



M56-P Strap

STRAPS	PIN	DESCRIPTION	Board DEFAULT
TX_PWRS_ENB	GPIO0 (Internal pull-down)	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	1
TX_DEEMPH_EN	GPIO1 (Internal pull-down)	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	1
	GPIO(3:2) (Internal pull-down)	RSVD	
DEBUG_ACCESS	GPIO4 (Internal pull-down)	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5 (Internal pull-down)	RSVD	
	GPIO6 (Internal pull-down)	RSVD	
Force_ Compliance	GPIO8 (Internal pull-down)	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13,12,11) (Internal pull-down)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128M 001x - No Rom, MEM_AP_SIZE=01 256M 010x - No Rom, MEM_AP_SIZE=10 64M 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	000
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC, GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

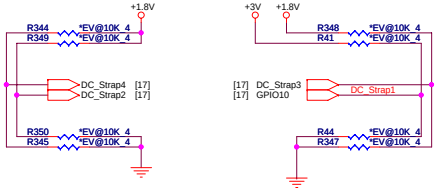
```
Memory Aperture Size Select
When no ROM is attached, GPIO_9 is set to 0
GPIO_[13:12] is used to select the memory aperture size.
GPIO_[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO_[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO_[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO_[13:12] = 11: reserved, same as ROM strap 11

Default: 128M memory aperture.
GPIO_[13:12] = 01 (256M memory aperture) recommended
for designs with 256MB or 512MB of physical memory.
```

M52P(G) M54P VRAM Configuration Table

MEMTYP_[3:0]	DESCRIPTION	Size
0000	DDR2 , 16Mx16 , 2pcs	64M
0001	DDR2 , 16Mx16 , 4pcs	128M
0010	DDR2 , 32Mx16 , 2pcs	128M
0011	DDR2 , 32Mx16 , 4pcs	256M
others	Reserved	

Default



00

Board Straps REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	GPIO25,26	Memory identification for BIOS 00 - DDR2 16X16X4pcs 128MB 01 - DDR2 32X16X4pcs 256MB 10 - DDR2 16X16X2pcs 64MB 11 - DDR2 32X16X2pcs 128MB	
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

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	M52-P_Straps (4 of 4)	1A

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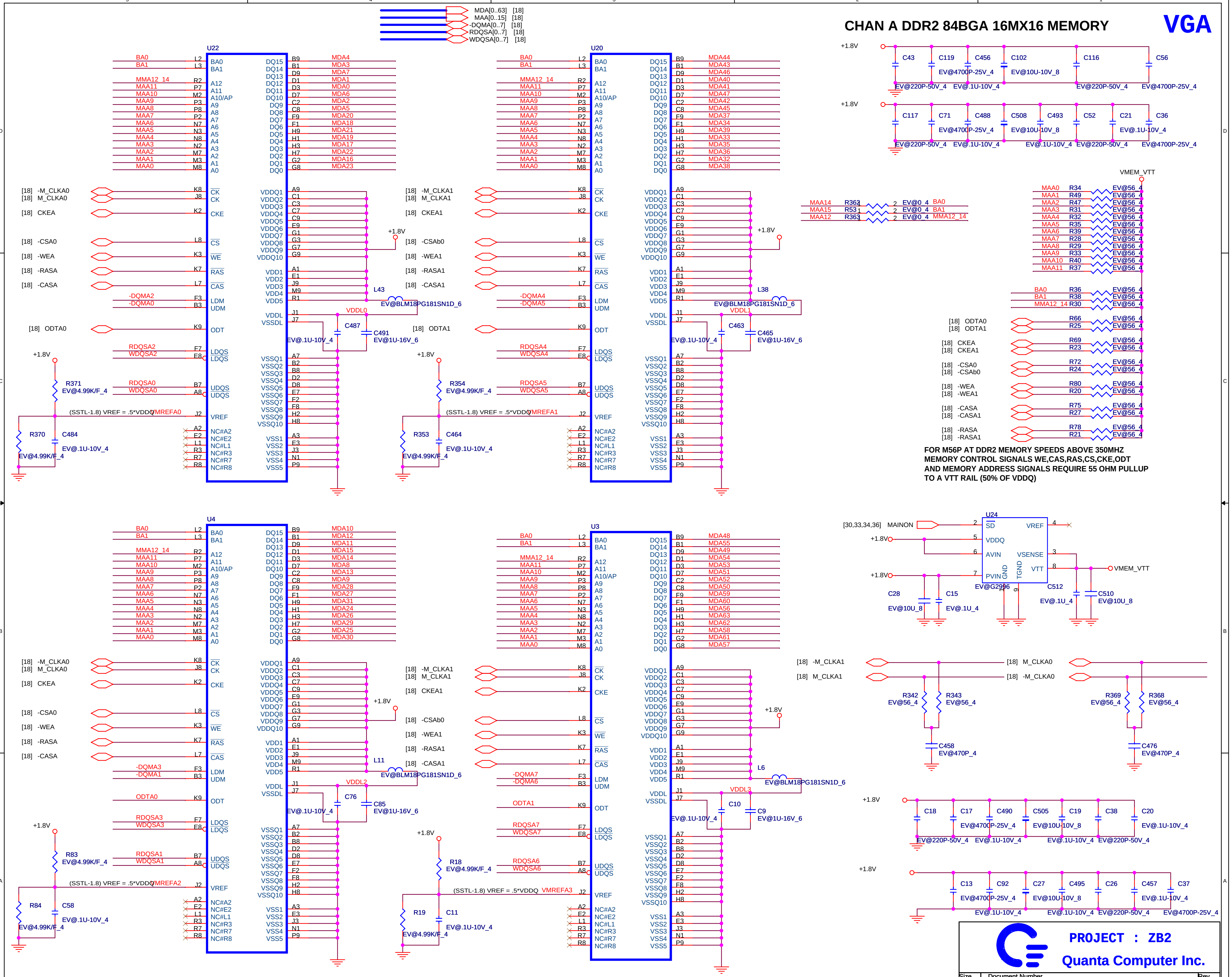
CHAN A DDR2 84BGA 16MX16 MEMORY

VGA



FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP
TO A VTT RAIL (50% OF VDDQ)

PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	VRAM DDR2	1A

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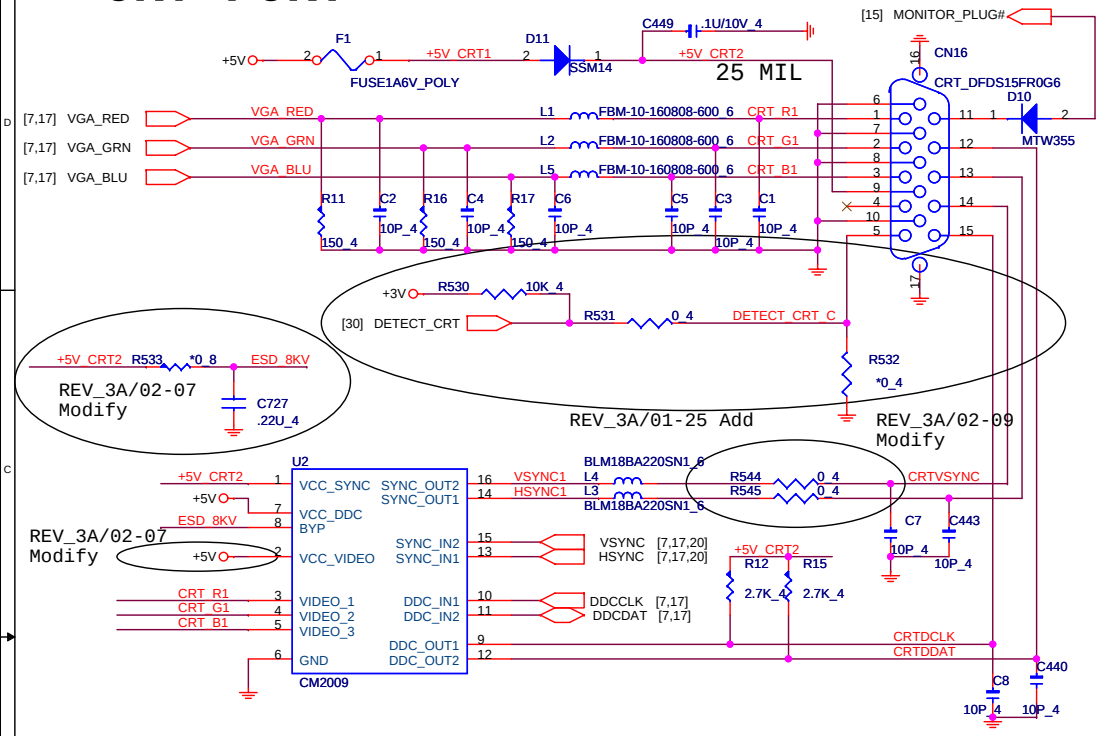
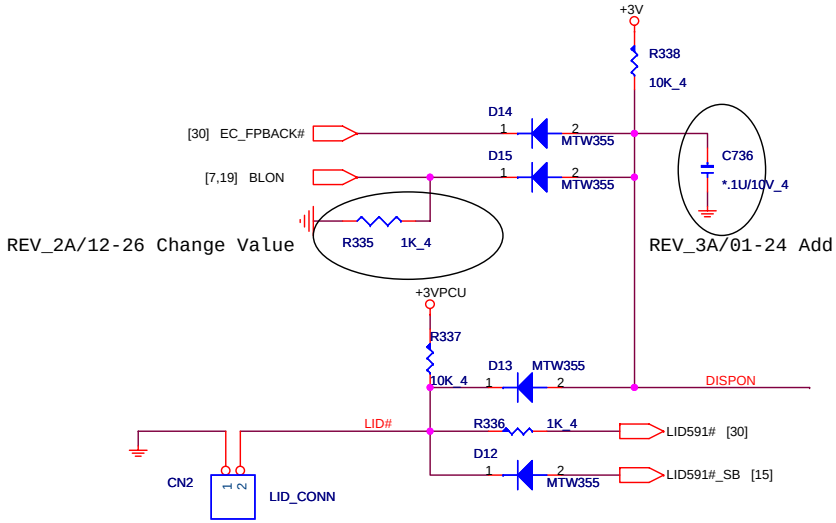
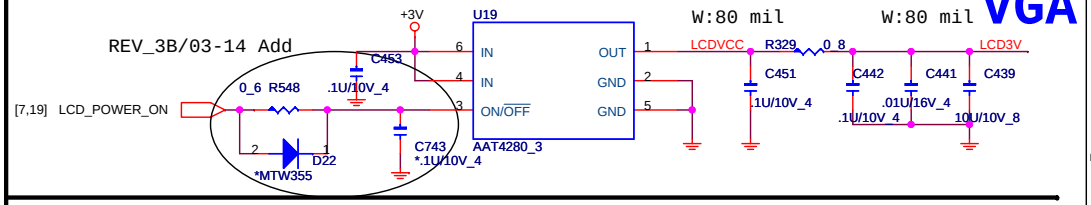
CRT PORT

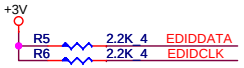


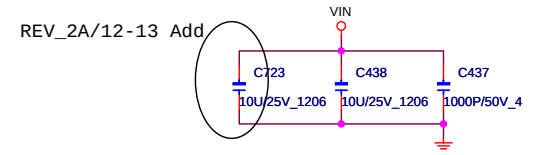


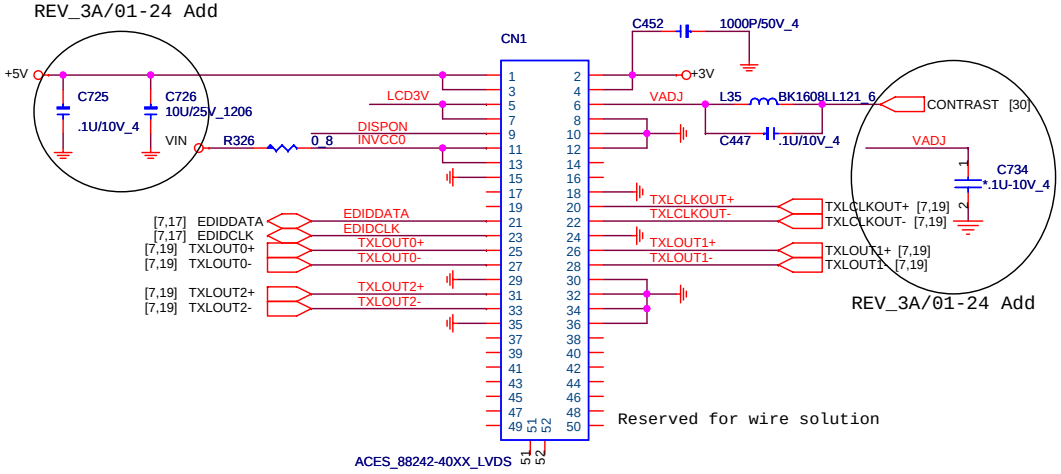
Lid Switch

VGA









PROJECT : ZB2

Quanta Computer Inc.

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	LVDS,VGA Ports, LID	3B
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IDE

[13] PDD[0..15] — PDD[0..15]

PH@HDD_CON CN29

-RST_HDD0, PDD7, PDD6, PDD5, PDD4, PDD3, PDD2, PDD1, PDD0, PDD8, PDD9, PDD10, PDD11, PDD12, PDD13, PDD14, PDD15

PDD7 R464 *10K_4

PDDREQ R471 *5.6K_4

PDDREQ

[13] PDDREQ
[13] PDIOW#
[13] PDIOR#
[13] PHDRDY
[13] PDDACK#
[13] IRQ14
[13] PDA1
[13] PDA0
[13] PDCS1#
[31] IDELED#

PHDRDY

IRQ14

PSEL R474 470_4

-PDIAG R481 *10K_4 +5V

PDA2 [13]
PDCS3# [13]

IDELED#

+5V

C412 .1U/10V_4
C694 .1U/10V_4
C692 *100P_4
C693 .1U/10V_4
C695 1000P/50V_4
C413 .1U/10V_4
C414 150U/6.3V_7343
C741 10U/25V_1206

REV_3B/03-13 Add

+5V
+5V
R463 *10K_4
Q23 *DTC144EU
-RST_HDD0
R462 0_4
R461 22_4
PLTRST# [14,17,26]

REV_3B/03-13 Modify

+3V R478 8.2K_4 IRQ14
+3V R546 4.7K_4 PHDRDY

REV_3B/03-01 Add

CN18

-RST_HDD0, PDD7, PDD6, PDD5, PDD4, PDD3, PDD2, PDD1, PDD0, PDD8, PDD9, PDD10, PDD11, PDD12, PDD13, PDD14, PDD15, PDDREQ, PDIOR#, PDDACK#, -PDIAG, PDA2, PDCS3#, RBAYVCC

PDIOW#
PHDRDY
IRQ14
PDA1
PDA0
PDCS1#
IDELED#
RBAYVCC

RCSEL_R
R372 *470_4
NC FOR SLAVE

NS@ODD_CONN

+5V
C105 .1U/10V_4
C108 .1U/10V_4
C106 .1U/10V_4
C107 .1U/10V_4

+5V
RBAYVCC
R91 0_8
R92 0_8
C740 10U/25V_1206
C477 1000P/50V_4
C54 50U/6.3V_7343
C478 .1U/10V_4
C483 .1U/10V_4
C482 .1U/10V_4

REV_3B/03-13 Add

OTH

PAD14 PAD21 PAD8 PAD16 PAD2 PAD20 PAD19 PAD3 PAD7 PAD10 PAD15 PAD23 PAD24 PAD17 PAD18 PAD6 PAD11 PAD4 PAD12

*EMIPAD

*MODEM PAD

REV_3A/02-07 NC

REV_3A/02-07
Add for EMI

HOLE18 H-C236I182D142P2
HOLE25 H-TC197BC98D59P2
HOLE26 H-TC197BC98D59P2
HOLE19 H-C276I158D118P2

PAD28 EMIPAD

REV_3C/03-29 Add

PAD5 PAD13 PAD1 PAD25 PAD26 PAD27

EMIPAD

HOLE16 H-C276D118P2-8
HOLE3 H-C276D118P2-8
HOLE20 H-C276D118P2-8
HOLE27 H-C276D118P2-8
HOLE1 H-C276D118P2-8
HOLE29 H-C276D118P2-8
HOLE8 H-C276D118P2-8
HOLE24 H-C276D118P2-8

HOLE4 H-C276D118P2-8
HOLE22 H-C276D118P2-8
HOLE23 H-C276D118P2-8
HOLE2 H-C276D118P2-8
HOLE5 H-C276D118P2-8
HOLE15 H-C197D63P2-8
HOLE21 H-C217D118P2-8
HOLE10 H-C276I182D142P2-8
HOLE6 H-C276I182D142P2-8

HOLE7 H-C276I158D118P2-8
HOLE9 H-C276I158D118P2-8
HOLE12 H-C276I158D118P2-8
HOLE28 H-C276I158D118P2-8
HOLE13 H-C236D142P2-8
HOLE14 H-C236D142P2-8
HOLE17 H-C236D142P2-8

CN28

GND1 RXP RXN GND2 TXN TXP GND3
3.3V 3.3V 3.3V GND GND GND 5V 5V 5V GND RSVD GND 12V 12V 12V

SATA_TXP0 [13]
SATA_TXN0 [13]
SATA_RXN0_C C645 *SH_SP@.01U-16V_4
SATA_RXP0_C C644 *SH_SP@.01U-16V_4
SATA_RXN0 [13]
SATA_RXP0 [13]

+3.3VSATA R292 *SH@0_8 +3V
HDD_VDD R298 *SH@0_8 +5V

*SH@Serial_ATA

+3.3VSATA
C390 *SH@4.7U-10V_8
C398 *SH@4.7U-10V_8
C387 *SH@.1U-10V_4

RST GND 02 GND
1 2
43 44
2 1
44 43

Reserve SATA

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Quanta Computer Inc.

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	HDD & CDROM & Hole	3C

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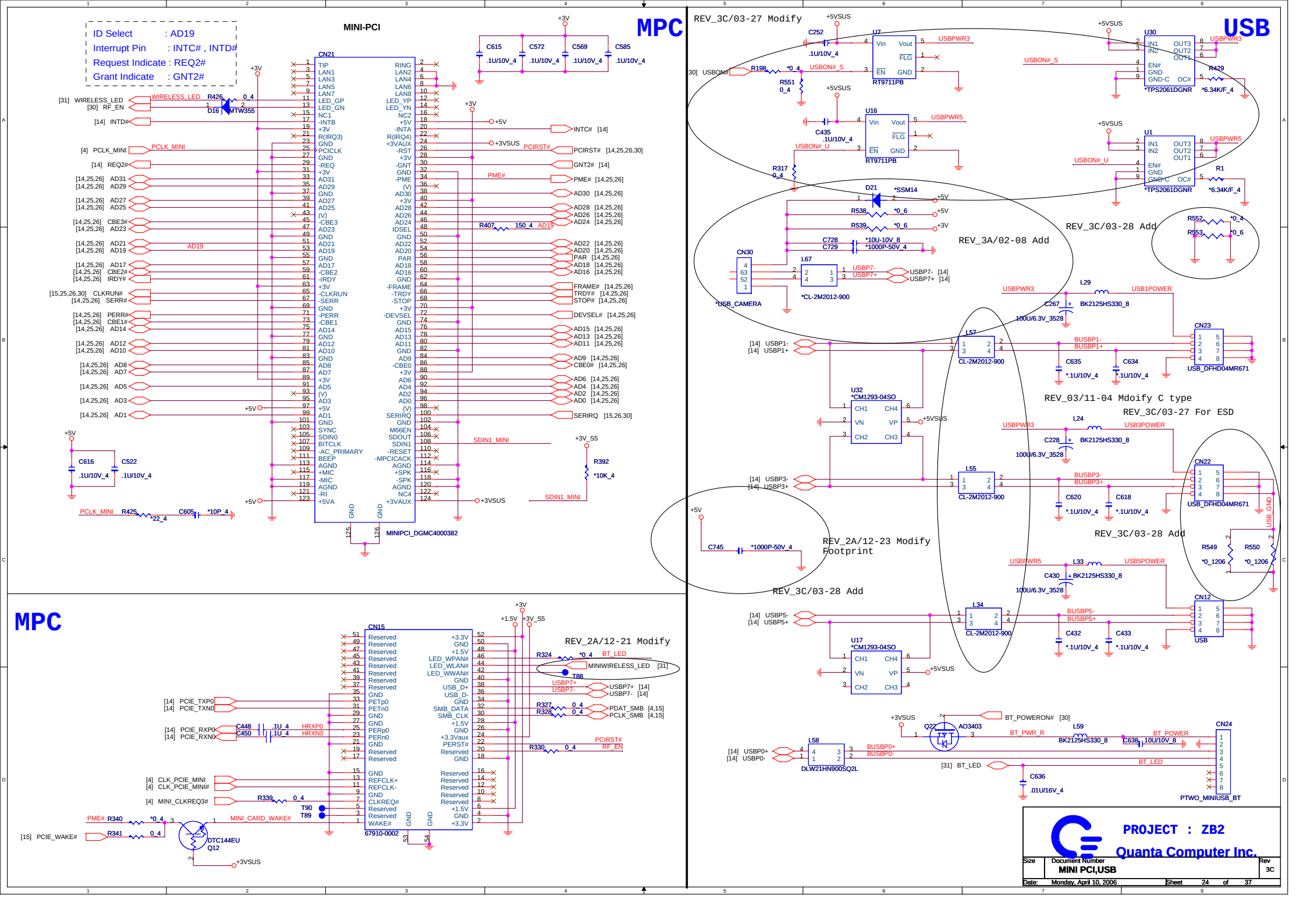
MPC
MINI-PCI
ID Select : AD19
Interrupt Pin : INTC# , INTD#
Request Indicate : REQ2#
Grant Indicate : GNT2#
CN21
MINIPCI_DGMC4000382
MPC
REV_2A/12-21 Modify
CN15
67910-0002
DTC144EU
Q12
REV_3C/03-27 Modify
USB
REV_3A/02-08 Add
REV_3C/03-28 Add
REV_03/11-04 Mdoify C type
REV_3C/03-27 For ESD
REV_2A/12-23 Modify
Footprint
*USB_CAMERA
*CL-2M2012-900
RT9711PB
*TPS2061DGNR
USB_DFHD04MR671
*CM1293-04SO
DLW21HN900SQ2L
AO3403
PTWO_MINIUSB_BT
PROJECT : ZB2
Quanta Computer Inc.
MINI PCI,USB
Monday, April 10, 2006

LAN

ID Select : AD16
Interrupt Pin : INTB#
Request Indicate : REQ1#
Grant Indicate : GNT1#

U27

RTL8110SBL/8100CL

RTL8110SBL
VDD33---+3.3V DIGITAL
AVDDH------+3.3V ANALOG
AVDDL-----+2.5V ANALOG
DVDD-----+1.2V DIGITAL
DVDD_A----+1.2V ANALOG

RTL8100CL
VDD33---+3.3V DIGITAL
AVDDL-----+3.3V ANALOG
DVDD-----+2.5V DIGITAL
AVDDH------+2.5V ANALOG

Near Lan chipset

REV_2A/12-26 Add

REV_3B/03-14 Add

REV_2A/12-26 Delete

U18 NS681688

CN11 RJ-45&RJ-11

U26 93C46-3GR

CN14 ACES-MDC

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Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8110SBL/8100CL	3B
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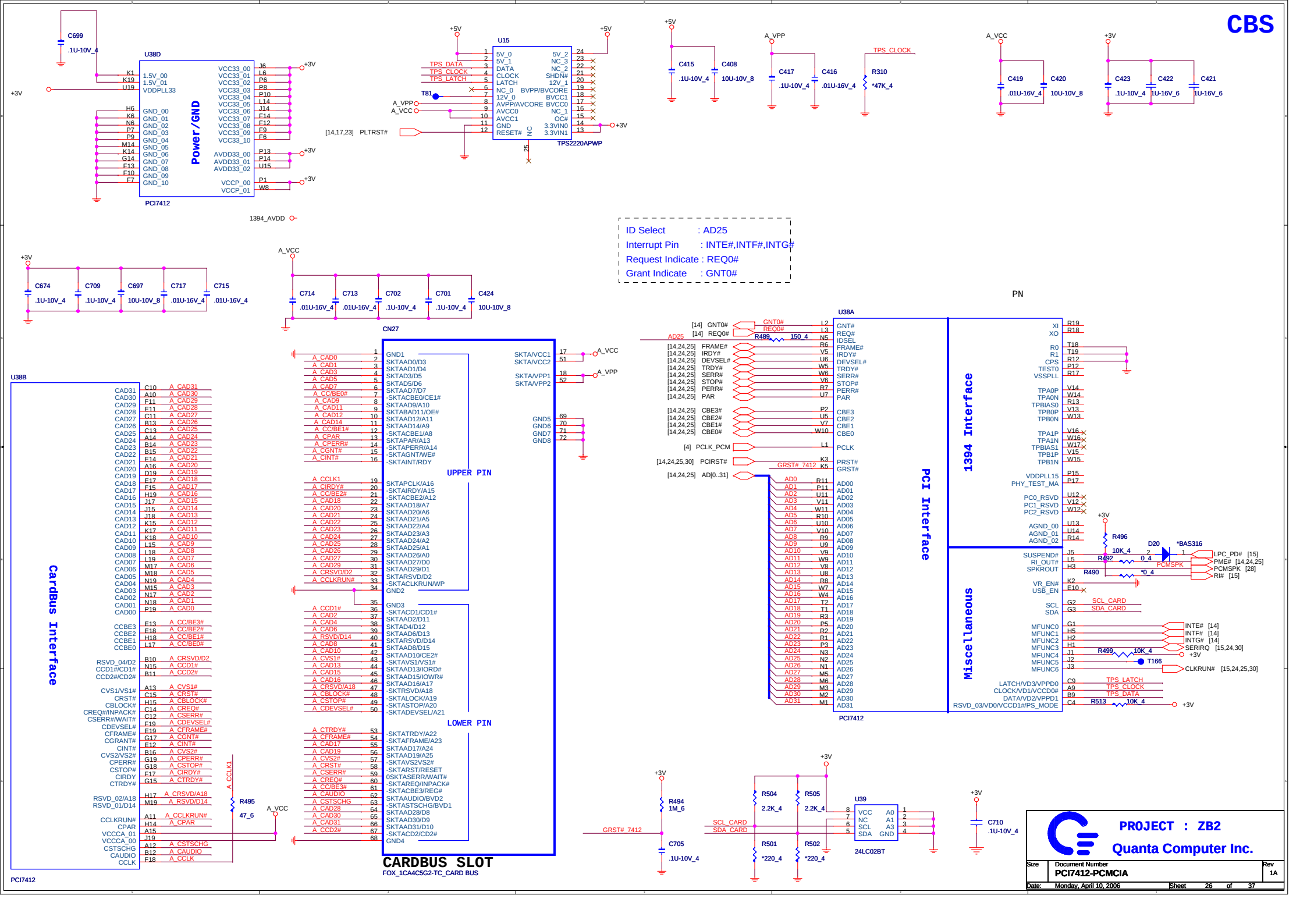
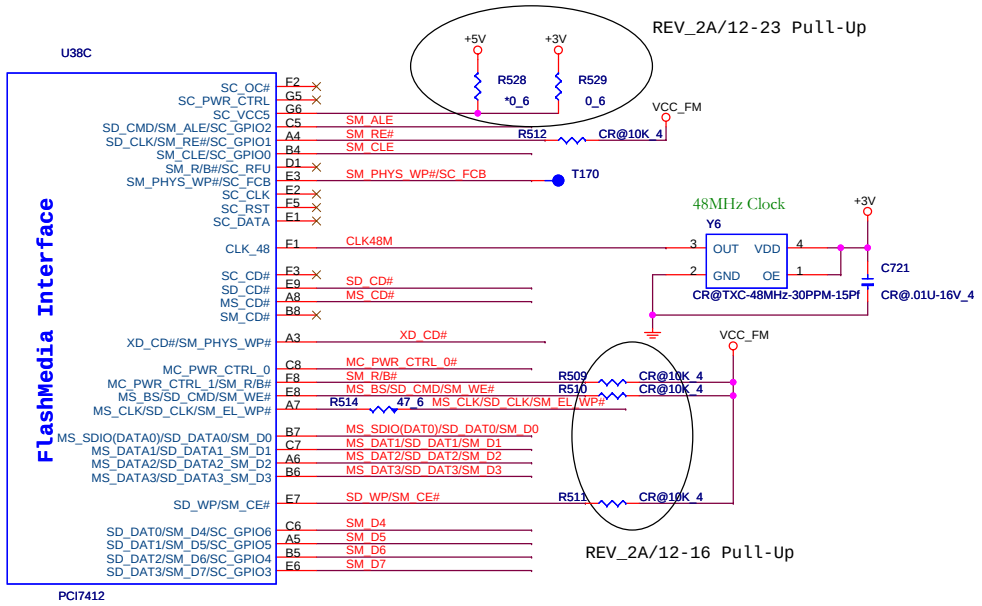
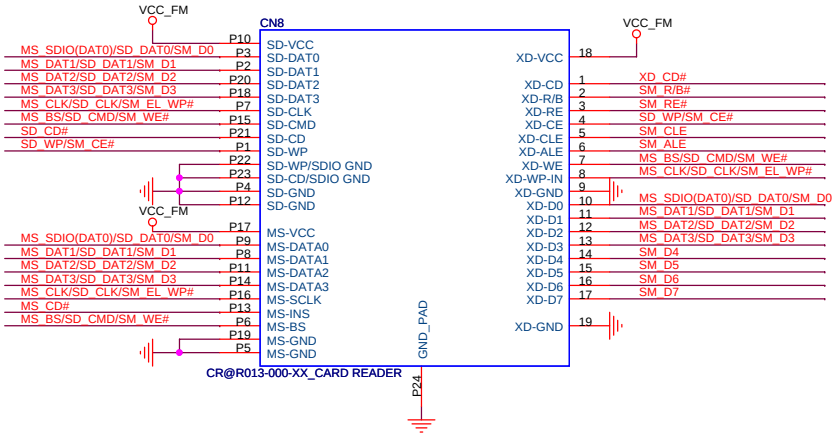

CBS
C699
.1U-10V_4
U38D
Power/GND
PCI7412
U15
TPS2220APWP
T81
C415
C408
C417
C416
R310
*47K_4
TPS_CLOCK
A_VPP
A_VCC
C419
C420
C423
C422
C421
1394_AVDD
C674
C709
C697
C717
C715
C714
C713
C702
C701
C424
CN27
ID Select : AD25
Interrupt Pin : INTE#,INTF#,INTG#
Request Indicate : REQ0#
Grant Indicate : GNT0#
PN
U38A
1394 Interface
PCI Interface
Miscellaneous
U38B
CardBus Interface
UPPER PIN
LOWER PIN
R495
47_6
R494
1M_6
C705
.1U-10V_4
R504
R505
R501
R502
2.2K_4
*220_4
U39
24LC02BT
C710
.1U-10V_4
CARDBUS SLOT
FOX_1CA4C5G2-TC_CARD BUS
PROJECT : ZB2
Quanta Computer Inc.
PCI7412-PCMCIA
Monday, April 10, 2006
Sheet 26 of 37

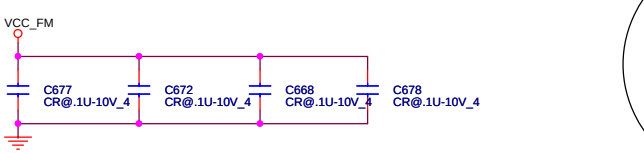
MMC

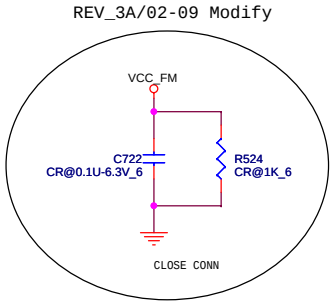
DO NOT INSERT SD/MMC, MEMORYSTICK AND XD SIMULTANEOUSLY.

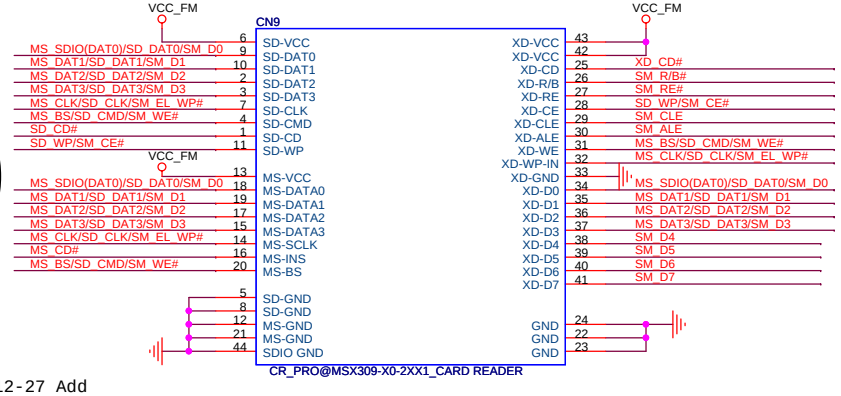


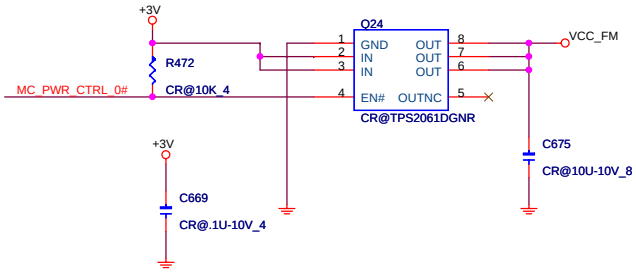


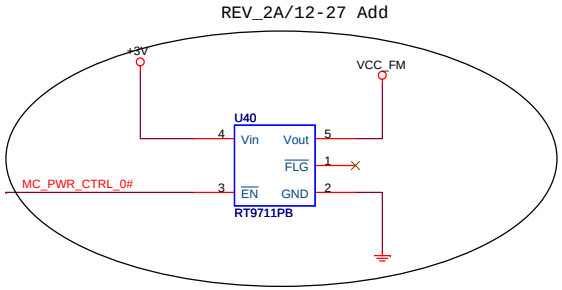
5 IN1 CARD READER









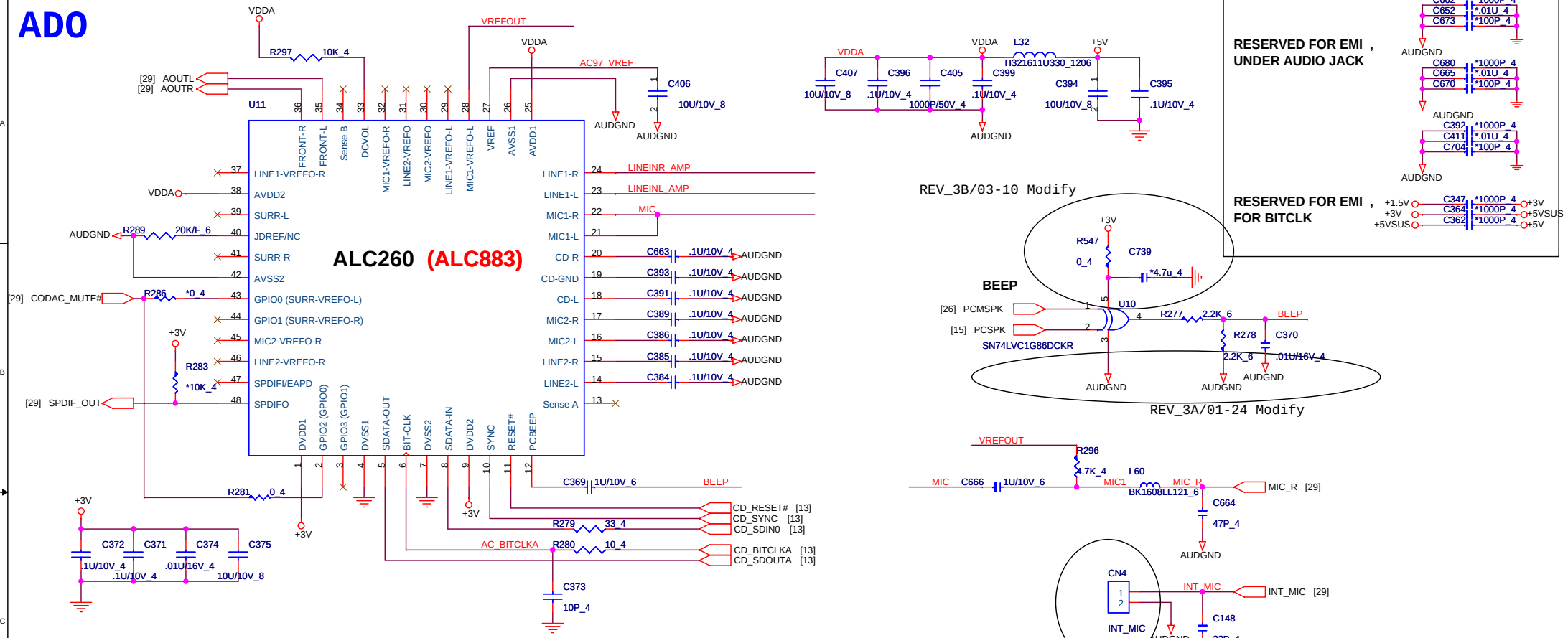


PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	PCI7412-CARD READER	3A
Date: Monday, April 10, 2006	Sheet 27 of 37	

ADO



REV_3B/03-10 Modify

RESERVED FOR EMI , UNDER AUDIO JACK

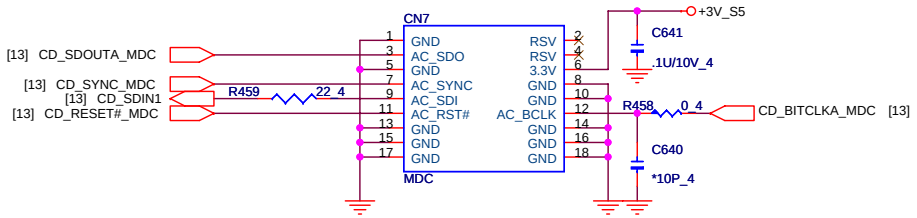
RESERVED FOR EMI , FOR BITCLK

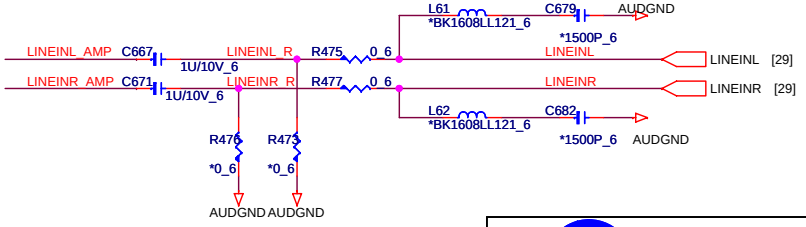
BEEP

REV_3A/01-24 Modify

REV_3A/02-07 Modify Type

MDM



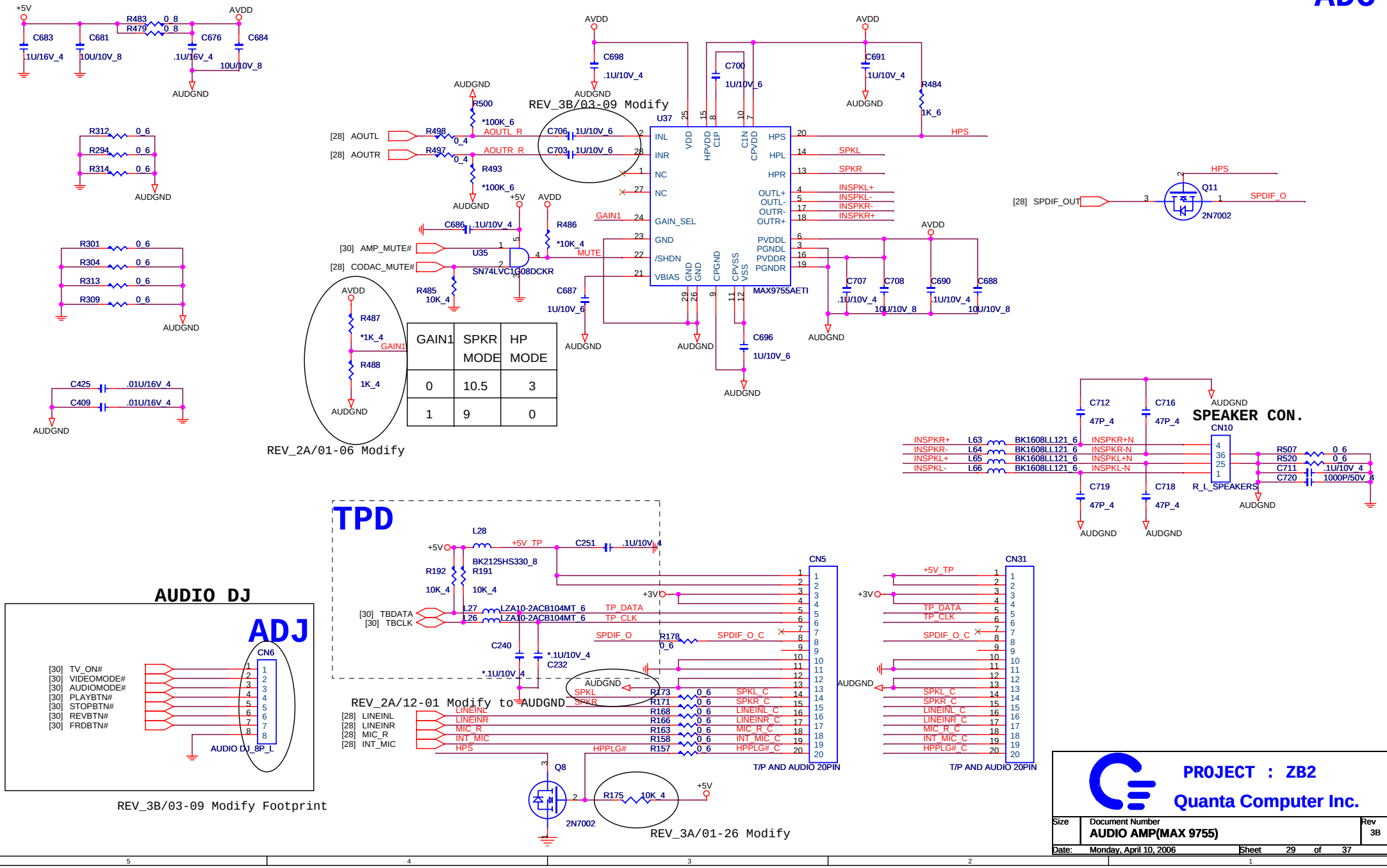


PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	REALTEK ALC883	3B
Date: Monday, April 10, 2006	Sheet 28 of 37	

ADO



GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO AMP(MAX 9755)	3B

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KBC

U12 AT24C08AN — MBCLK, MBDATA, SCL, SDA, A0, A1, A2, WP, VCC, GND

C427 10U/10V_8, C404 .1U/10V_4, C403 .1U/10V_4, C685 .1U/10V_4, C388 .1U/10V_4

C429 .1U/10V_4, C402 .1U/10V_4, R316 0_6, C428 .1U/10V_4, C689 .1U/10V_4

U41 *SN74LVC1G14DBVR — FANSIG_C, R535 *8.2K_4, R536 *22K_4, R537 0_4, FANSIG [31]

REV_3A/02-08 Add

ENV1 R515 10K_4; BADDR0 R516 *10K_4; BADDR1 R517 *10K_4; BT_POWERON# R491 *10K_4; SHBM R518 10K_4

SHBM=1: Enable shared memory with host BIOS

I/O Address		
BADDR1-0	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

U36 PC97551

Host interface: SERIRQ, LDRQ, LFRAME, LAD0, LAD1, LAD2, LAD3, LCLK, LRESET, SMI, PWUREQ

AD Input: AD0 TEMP_MBAT, AD1 T167, AD2 T169, AD3 T168, IOPE0/AD4 WIRELESS_SW#, IOPE1/AD5 BLUETOOTH_SW#, IOPE2/AD6 SUSC#, IOPE3/AD7 SUSB#, DP/AD8, DN/AD9

DA output: DA0 CC-SET, DA1 CV-SET, DA2 CONTRAST, DA3 VFAN

PWM or PORTA: IOPA0/PWM0 8724CELLS, IOPA1/PWM1, IOPA2/PWM2, IOPA3/PWM3 AMP_MUTE# [29], IOPA4/PWM4 HWPG_591, IOPA5/PWM5 REVBTN# [29], IOPA6/PWM6 STOPBTN# [29], IOPA7/PWM7 FRDBTN# [29]

Battery Cells Select

REV_3A/01-25 Add

PORTB: IOPB0/URXD DETECT_CRT [22], IOPB1/UTXD TX_551 T165, IOPB2/USCLK LID591# [22], IOPB3/SCL1 MBCLK [17,35], IOPB4/SDA1 MBDATA [17,35], IOPB7/RING/PFAIL PCIRST# [14,24,25,26]

PORTC: IOPC0 591_PME#, IOPC1/SCL2 CPU_MBCLK [2], IOPC2/SDA2 CPU_MBDATA [2], IOPC3/TA1 FANSIG_C, IOPC4/TB1/EXWINT22 EC_FPBACK# [22], IOPC5/TA2 H_PROCHOT# [2], IOPC6/TB2/EXWINT23 PWROK_1 R290 0_6 EC_PWRGD [15], IOPC7/CLKOUT

D19 MTW355 — DNBSWON# [15]

PORTD-1: IOPD0/RI1/EXWINT20 AUDIOMODE# [29], IOPD1/RI2/EXWINT21 ACIN [35], IOPD2/EXWINT24 VIDEOMODE# [29]

PORTE: IOPE4/SWIN NBSWON#, IOPE5/EXWINT40 TV_ON# [29], IOPE6/LPCPD/EXWIN45 PLAYBTN# [29], IOPE7/CLKRUN/EXWINT46 CLKRUN# [15,24,25,26]; R287 0_4

PORTH: IOPH0/A0/ENV0 ENV0, IOPH1/A1/ENV1 ENV1, IOPH2/A2/BADDR0 BADDR0, IOPH3/A3/BADDR1 BADDR1, IOPH4/A4/TRIS TRIS, IOPH5/A5/SHBM SHBM, IOPH6/A6 A6, IOPH7/A7 A7

PORTI: IOPI0/D0 D0, IOPI1/D1 D1, IOPI2/D2 D2, IOPI3/D3 D3, IOPI4/D4 D4, IOPI5/D5 D5, IOPI6/D6 D6, IOPI7/D7 D7

PORTJ-1: IOPJ0/RD RD#, IOPJ1/WR0 WR#

SELIO

PORTD-2: IOPD4 CELL-SET, IOPD5 D/C# [35], IOPD6 BL/C# [35], IOPD7

PORTK: IOPK0/A8 A8, IOPK1/A9 A9, IOPK2/A10 A10, IOPK3/A11 A11, IOPK4/A12 A12, IOPK5/A13/BE0 A13, IOPK6/A14/BE1 A14, IOPK7/A15/CBRD A15

PORTL: IOPL0/A16 A16, IOPL1/A17 A17, IOPL2/A18 A18, IOPL3/A19 A19, IOPL4/WR1

Key matrix scan: KBSIN0–KBSIN7, KBSOUT0–KBSOUT15

JTAG debug port: TINT T86, TCK T84, TDO T87, TDI T85, TMS T83

PS2 interface: PSCLK1/IOPF0, PSDAT1/IOPF1, PSCLK2/IOPF2, PSDAT2/IOPF3, PSCLK3/IOPF4, PSDAT3/IOPF5, PSCLK4/IOPF6, PSDAT4/IOPF7

32KX1/32KCLKOUT, 32KX2

PORTJ-2: IOPJ2/BST0, IOPJ3/BST1, IOPJ4/BST2, IOPJ5/PFS, IOPJ6/PLI, IOPJ7/BRKI_RSTO

PORTM: IOPM0/D8, IOPM1/D9, IOPM2/D10, IOPM3/D11, IOPM4/D12, IOPM5/D13, IOPM6/D14, IOPM7/D15

SEL0, SEL1, CLK

GND1–GND7, AGND, NC1–NC10

C397 1U/10V_6 — FOR 97551 ONLY

Switch Signal between main and 2'nd Battery

MBCLK R295 4.7K_4; MBDATA R300 4.7K_4; CPU_MBCLK R482 4.7K_4; CPU_MBDATA R480 4.7K_4

WIRELESS_SW# R503 4.7K_4; BLUETOOTH_SW# R506 4.7K_4

R284 *4.7K_4, Q10 PDTC143TT, R288 10K_4, 591_PME# — LAN_PME# [25]

R282 470K_4, D7 MTW355 — SERIRQ [15,24,26]

D6 MTW355 — KBSMI# [15]

PCLK_591 R291 *22_4 C400 *10P_4 — SCI# [15]

D18 MTW355 — IOPD3/ECSCI

D9 MTW355 — GATEA20 [13]

D8 MTW355 — RCIN# [13]

LFRAME#/FWH4 [13], LAD0/FWH0 [13], LAD1/FWH1 [13], LAD2/FWH2 [13], LAD3/FWH3 [13], PCLK_591 [4]

GA20/IOPB5, KBRST/IOPB6

MX0–MX7 [31], MY0–MY15 [31]

VGA_MAINON — MAINON; C732 *.1U-10V_4, C731 *.1U-10V_4

TBCLK [29], TBDATA [29], CAPSLED# [31], NUMLED# [31]

Y1 32.768KHZ; R311 20M_6, R308 121K/F_6, C418 10P_4, C410 10P_4

USBON# [24,31], BT_POWERON# [24], RF_EN [24], RSMRST# [15], SUSLED# [31], BATLED0# [31], BATLED1# [31]

VRON [32,34], MAINON [21,33,34,36], SUSON [33,34], S5_ON [33]

REV_2A/12-02 Modify

R293 10K_6 — +3V

HWPG_SYS [33] R303 0_4; HWPG_1.8V [34] R307 0_4; HWPG_1.5V [34] R302 0_4

REV_3A/02-08 Add

HWPG_VGA [36] R305 0_4; HWPG_1.05V [34] R299 0_4 — HWPG_591

USBON# R285 10K_4 +3VPCU

LID591# — C738 *.1U-10V_4; EC_FPBACK# — C733 .1U-10V_4

REV_3A/02-08 Add

U14 *ST Micro M29W008AB/AMD-29LV081B/SST39VF080

ENV0, ENV1, BADDR0, BADDR1, TRIS, SHBM, A6, A7, A8, A9, A10, A11, A12, A13, A14, A15, A16, A17, A18, A19; CS# 22, RD# 24, WR# 9; D0–D7; RESET#/NC 10, RY/BY#/NC 12, NC1 29, NC2 38, NC3 11; VCC1_PWROK — T82; R315 *10K_4; C426 *.1U-10V_4

U13 PLCC32

A0–A19; CS# 22, RD# 24, WR# 31; D0–D7; VPP 1 — A18; C401 .1U/10V_4

BIU configuration should match flash speed used

FWH

PROJECT : ZB2

Quanta Computer Inc.

Size	Document Number	Rev
	97551 & FLASH	3A
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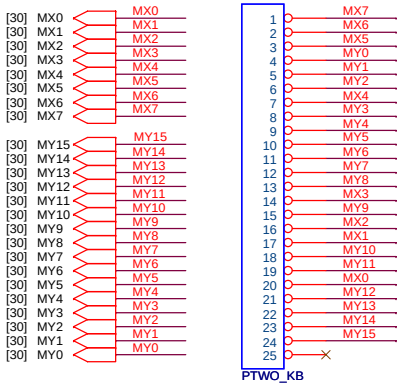
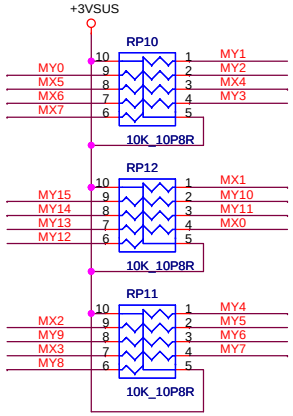
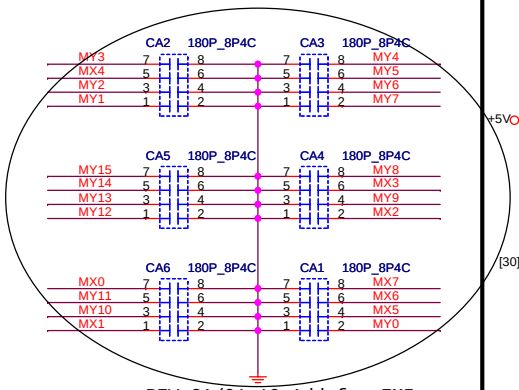
KBC

INT K/B





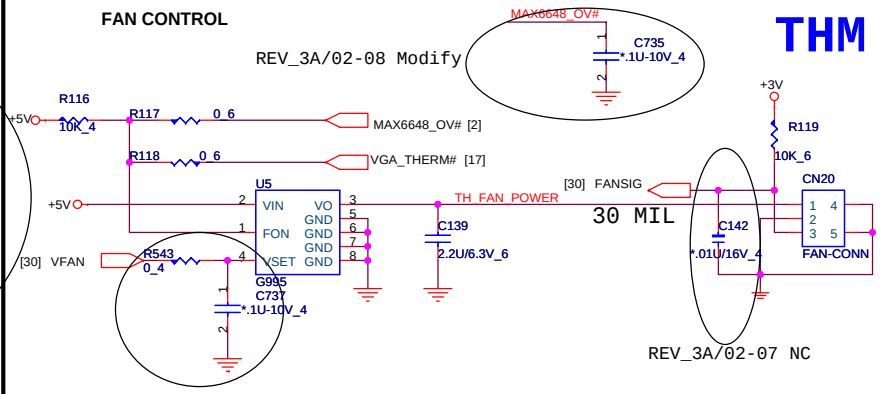


REV_2A/01-10 Add for EMI

THM

FAN CONTROL

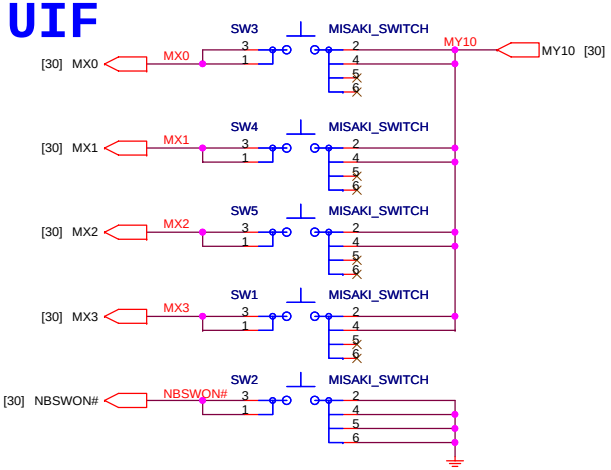
REV_3A/02-08 Modify

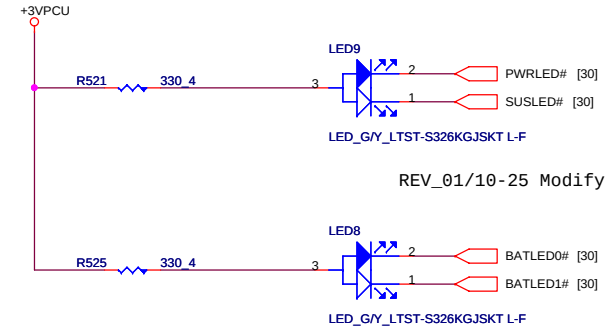


REV_3A/02-08 Modify

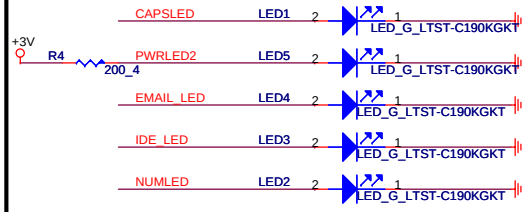
REV_3A/02-07 NC

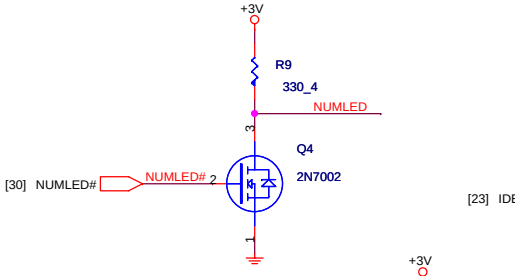
UIF

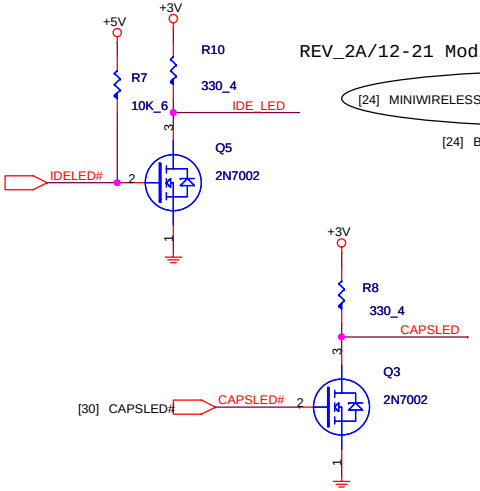




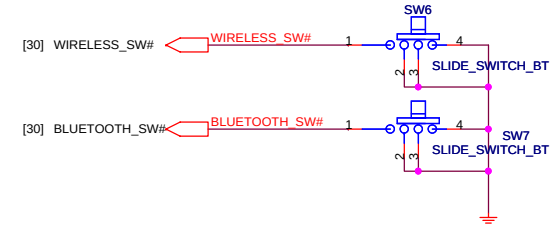
REV_01/10-25 Modify LED type

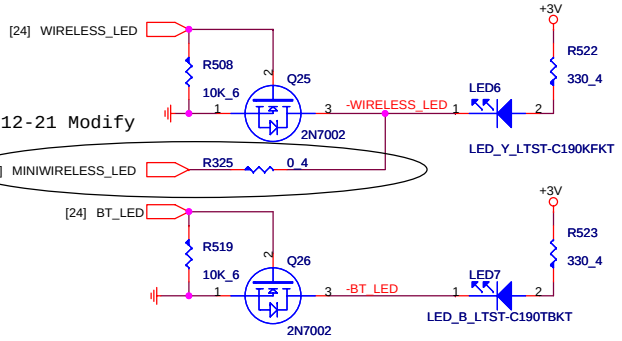






UIF





REV_2A/12-21 Modify

PROJECT : ZB2		
Quanta Computer Inc.		
Size	Document Number: T/P,FAN,SWITCH,LED,K/B	Rev: 3A
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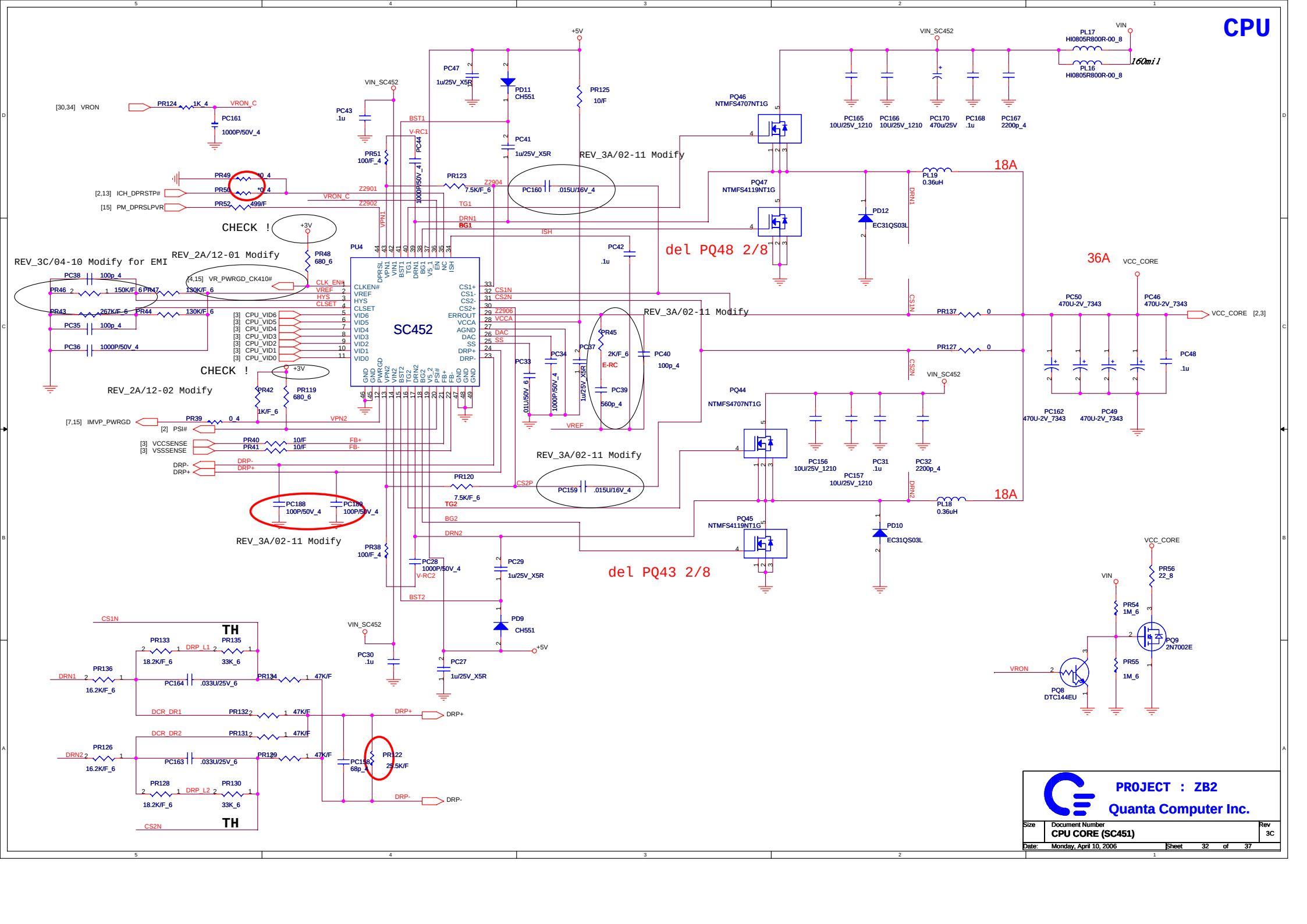
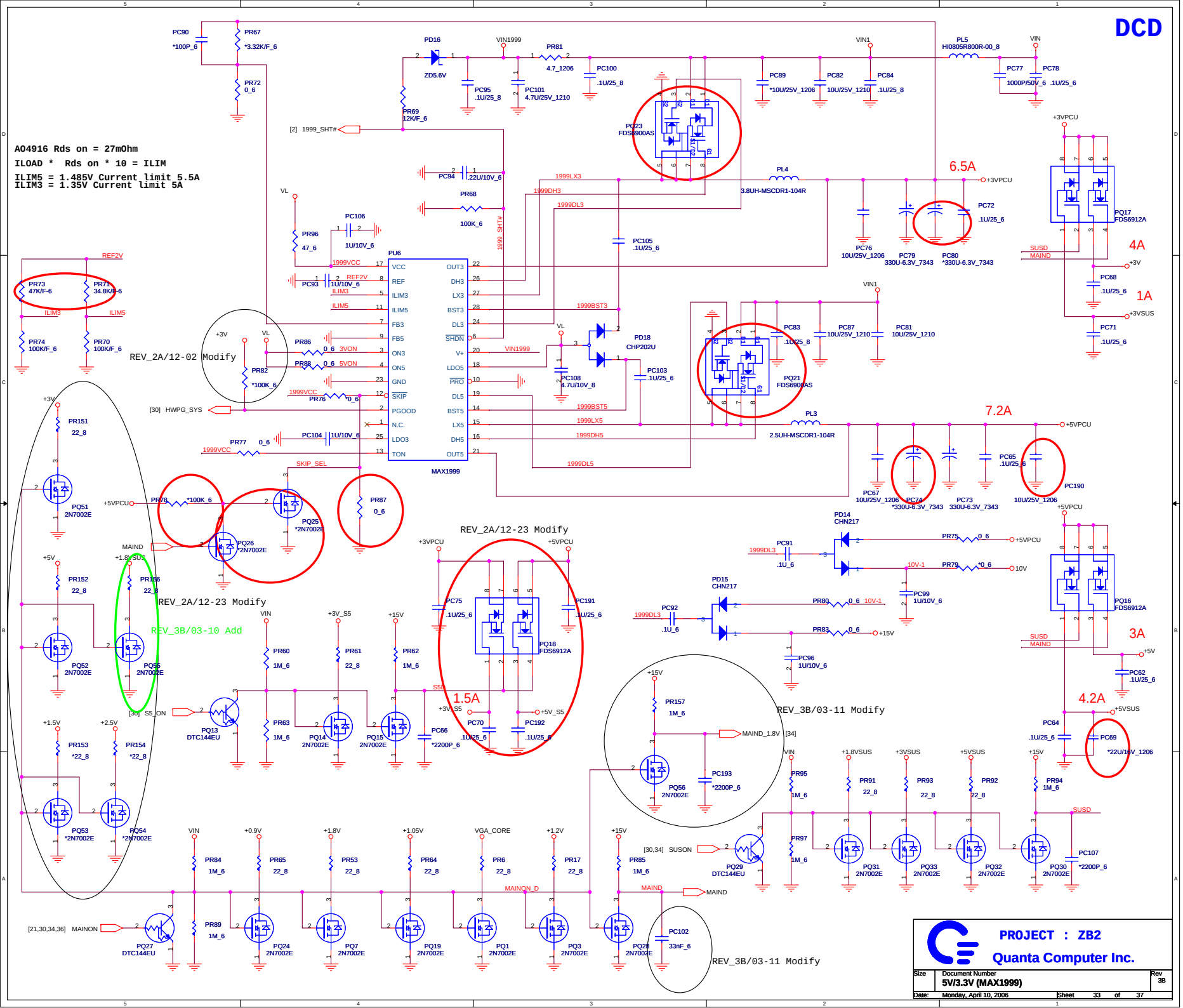

CPU
SC452
PU4
REV_3A/02-11 Modify
REV_2A/12-01 Modify
REV_3C/04-10 Modify for EMI
REV_2A/12-02 Modify
CHECK !
del PQ48 2/8
del PQ43 2/8
18A
36A
PROJECT : ZB2
Quanta Computer Inc.
CPU CORE (SC451)
Monday, April 10, 2006


DCD
AO4916 Rds on = 27mOhm
ILOAD * Rds on * 10 = ILIM
ILIM5 = 1.485V Current limit 5.5A
ILIM3 = 1.35V Current limit 5A
REV_2A/12-02 Modify
REV_2A/12-23 Modify
REV_2A/12-23 Modify
REV_3B/03-10 Add
REV_3B/03-11 Modify
REV_3B/03-11 Modify
MAX1999
6.5A
4A
1A
7.2A
1.5A
3A
4.2A
PROJECT : ZB2
Quanta Computer Inc.
5V/3.3V (MAX1999)
Monday, April 10, 2006
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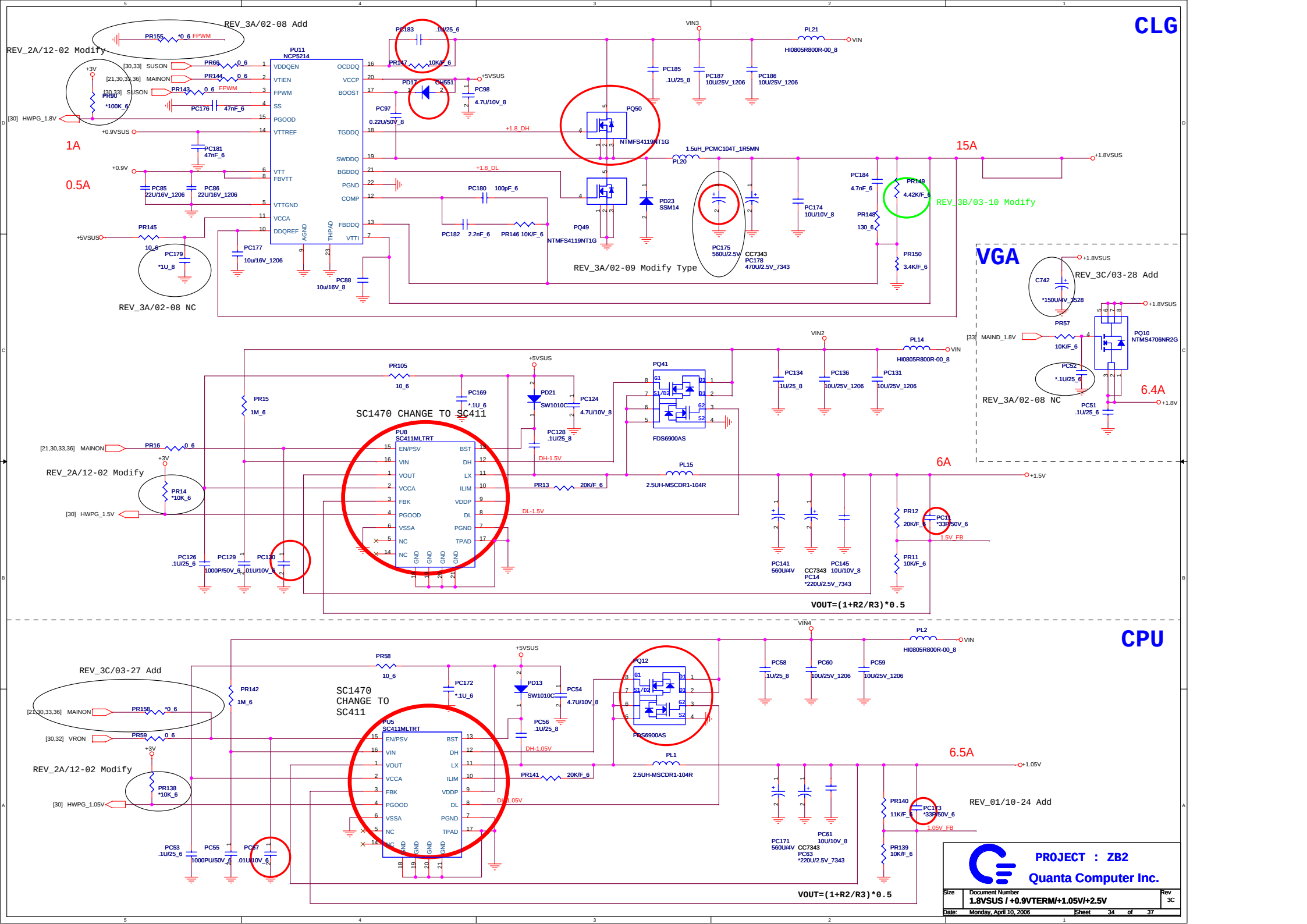
CLG
REV_3A/02-08 Add
REV_2A/12-02 Modify
PU11
NCP5214
1A
0.5A
REV_3A/02-08 NC
REV_3A/02-09 Modify Type
15A
REV_3B/03-10 Modify
VGA
REV_3C/03-28 Add
REV_3A/02-08 NC
6.4A
SC1470 CHANGE TO SC411
PU8
SC411MLTRT
FDS6900AS
6A
VOUT=(1+R2/R3)*0.5
CPU
REV_3C/03-27 Add
SC1470
CHANGE TO
SC411
PU5
SC411MLTRT
FDS6900AS
6.5A
REV_01/10-24 Add
VOUT=(1+R2/R3)*0.5
PROJECT : ZB2
Quanta Computer Inc.
1.8VSUS / +0.9VTERM/+1.05V/+2.5V
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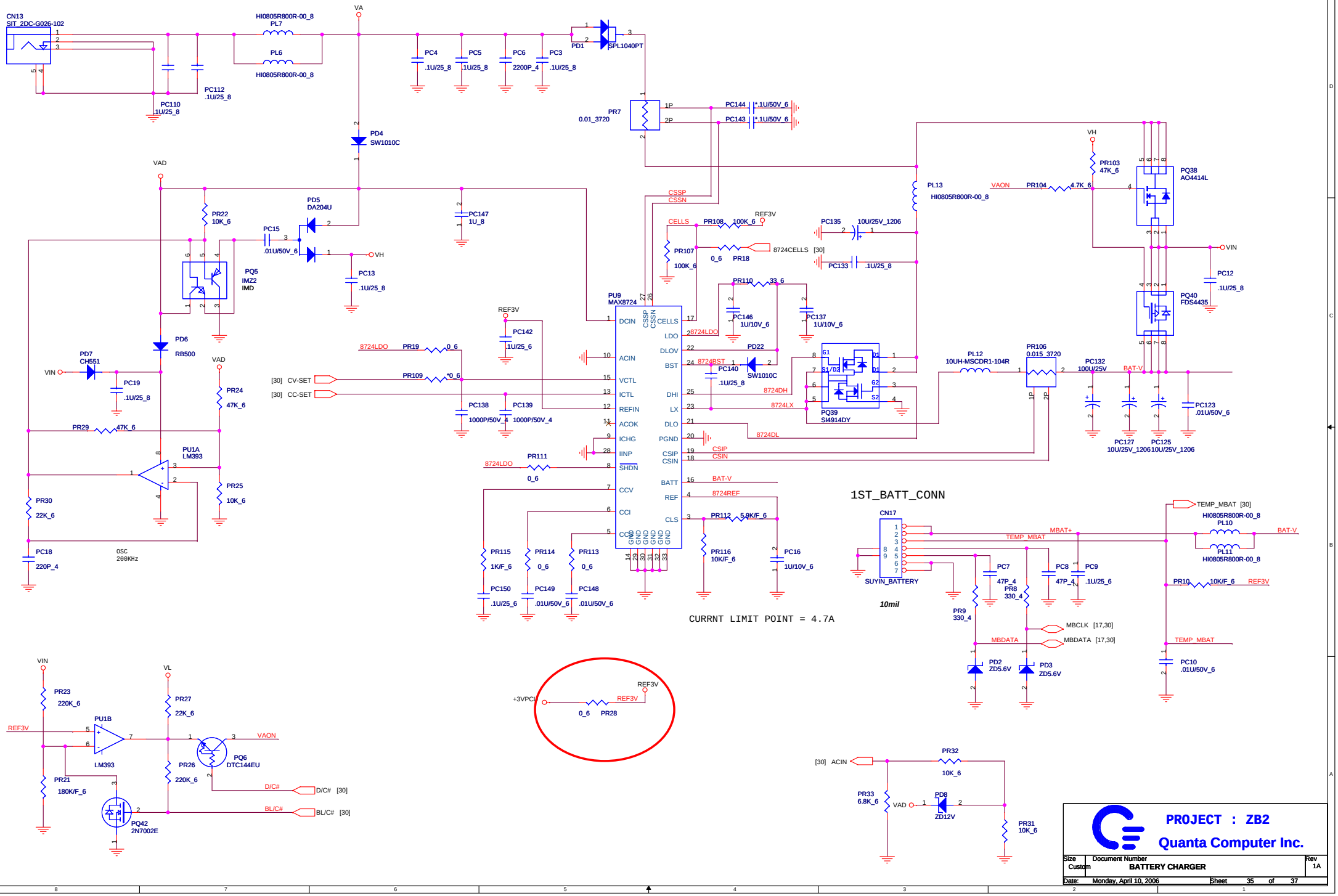
PBC


CN13
SIT_2DC-G026-102
HI0805R800R-00_8
PL7
PL6
HI0805R800R-00_8
VA
PC4 .1U/25_8
PC5 .1U/25_8
PC6 2200P_4
PC3 .1U/25_8
PD1
SPL1040PT
PC110 .1U/25_8
PC112 .1U/25_8
PD4
SW1010C
PR7
0.01_3720
PC144 *.1U/50V_6
PC143 *.1U/50V_6
VAD
PR22 10K_6
PD5
DA204U
PC15 .01U/50V_6
VH
PC13 .1U/25_8
PC147 1U_8
PQ5
IMZ2
IMD
CSSP
CSSN
CELLS
PR108 100K_6
REF3V
PR107 100K_6
0_6 PR18
8724CELLS [30]
PC135 10U/25V_1206
PC133 .1U/25_8
PR110 33_6
PC146 1U/10V_6
PC137 1U/10V_6
PU9
MAX8724
DCIN
CSSP
CSSN
CELLS
LDO
8724LDO
DLOV
BST
8724BST
PD22
SW1010C
PC140 .1U/25_8
8724DH
8724LX
PQ39
SI4914DY
PL12
10UH-MSCDR1-104R
PR106
0.015_3720
PC132 100U/25V
BAT-V
PC123 .01U/50V_6
PC127 10U/25V_1206
PC125 10U/25V_1206
PL13
HI0805R800R-00_8
VAON
PR104 4.7K_6
PR103 47K_6
VH
PQ38
AO4414L
PQ40
FDS4435
VIN
PC12 .1U/25_8
PD6
RB500
PD7
CH551
VIN
PC19 .1U/25_8
VAD
PR24 47K_6
PR29 47K_6
PU1A
LM393
PR30 22K_6
PR25 10K_6
PC18 220P_4
OSC
200KHz
8724LDO
PR19 0_6
PR109 *0_6
[30] CV-SET
[30] CC-SET
PC142 .1U/25_6
PC138 1000P/50V_4
PC139 1000P/50V_4
ACIN
VCTL
ICTL
REFIN
ACOK
ICHG
IINP
SHDN
CCV
CCI
CCO
DHI
LX
DLO
PGND
CSIP
CSIN
BATT
REF
CLS
8724DL
8724REF
PR111 0_6
PR112 5.9K/F_6
PR116 10K/F_6
PC16 1U/10V_6
PR115 1K/F_6
PR114 0_6
PR113 0_6
PC150 .1U/25_6
PC149 .01U/50V_6
PC148 .01U/50V_6
CURRNT LIMIT POINT = 4.7A
1ST_BATT_CONN
CN17
SUYIN_BATTERY
10mil
MBAT+
TEMP_MBAT
PC7 47P_4
PC8 47P_4
PC9 .1U/25_6
PR8 330_4
PR9 330_4
MBCLK [17,30]
MBDATA [17,30]
PD2 ZD5.6V
PD3 ZD5.6V
TEMP_MBAT [30]
HI0805R800R-00_8
PL10
PL11
HI0805R800R-00_8
BAT-V
PR10 10K/F_6
REF3V
TEMP_MBAT
PC10 .01U/50V_6
VIN
PR23 220K_6
REF3V
PU1B
LM393
PR21 180K/F_6
VL
PR27 22K_6
PR26 220K_6
PQ6
DTC144EU
VAON
D/C#
D/C# [30]
BL/C#
BL/C# [30]
PQ42
2N7002E
+3VPCU
REF3V
0_6 PR28
[30] ACIN
PR32 10K_6
PR33 6.8K_6
VAD
PD8
ZD12V
PR31 10K_6
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VGA

REV_3A/02-08 Modify to 0 Ohm

REV_2A/12-02 Modify

SC1470 CHANGE TO SC470

REV_3A/02-08 NC

15A

2.2A

HI-->VOUT=(1+R2/R3)*0.5

LO-->VOUT=(1+R2/(R3//R4))*0.5

M52P(G)

PR1 : 10K

PR4 : 11K

PR2 : 110K

M54P

PR1 : 12K

PR4 : 12K

PR2 : 60.4K

Vo=0.8(R1+R2)/R2

1.2*(PR137+PR136)/PR136=Vout

CLG

1A

Power Play Mode		
VGA_PWR_SW	VGA_CORE	
HI	0.95V--M52P(G)	1.0V --M54P
Default LO	1.0V--M52P(G)	1.1V--M54P

PROJECT : ZB2

Quanta Computer Inc.

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	VGA CORE/+1.2V	3A

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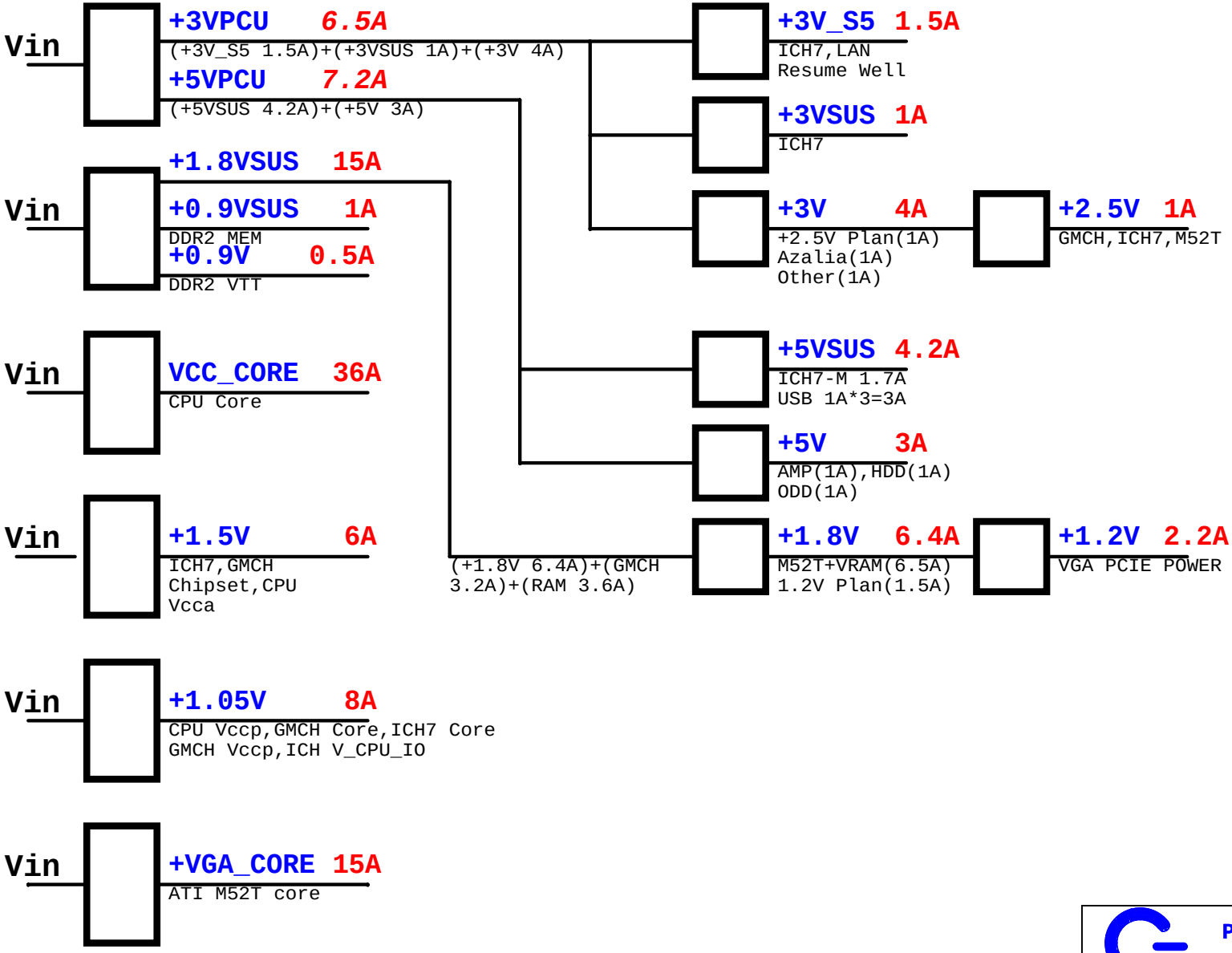

PROJECT : ZB2

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	POWER DIAGRAM	1A
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