Garda-D Block Diagram

(Discrete)

Project code: 91.4A901.001
PCB P/N : 55.4A901.XXX
REVISION : 05217-1
(Hannstar, ACCL)

-1M-0111

CLK GEN.
IDT CV125PA
(ICS 954206) 3

Mobile CPU
Yonah 478
1.83G/2G/2.16G 4, 5

G792 19

HOST BUS 400/533/667MHz

DDR2 533 MHz 11,12
DDR2 533 MHz 11,12
533/667MHz
533/667MHz

Calistoga
Ver.:A3 :71.945PM.A0U / QK58
6,7,8,9,10

PCI Express x16
M56 Ver.: B24
M52 Ver.: A12
M54 Ver.: A12

ATI M54P / M52P 45,46,47,48,49
VRAM x4 128/256M 50,51

LVDS
TVO 14
14"WSXGA LCD 13
RGB CRT
CRT 14

DMI I/F 100MHz

ICH7M
Ver. : B0, 71.ICH7M.A0U / QK65
KI.80101.017
15,16,17,18

Line In 29
MIC In 29
INT.MIC
Codec ALC883 28
AZALIA

Line Out (SPDIF) 29
OP AMP G1421B 29
INT.SPKR 29

RJ11
MODEM MDC Card 21

PCI Express
New card 30
PWR SW TPS2231 30

SATA
PATA
HDD 20
CDROM 18

USB 3 PORT 21
MINI USB Blue-tooth 21

PCI BUS
TI PCI 7412
CARDBUS 1394 CardReader 24,25
PCMCIA I/F
PWR SW TSP2220A 27
PCMCIA SLOT Support TypeII 27
1394 CONN 26
MS/MS Pro/xD/ MMC/SD/SDIO 6 in 1 26
Mini-PCI 802.11A/B/G 30

LAN 10/100 BCM4401-E 22
TXFM 23
RJ45 23
BCM5787MKFBG-A1
BCM5789KFBG-C1
BCM4401EKFBG-B0

PCIEx1
Mini Card*1 802.11A/B/G 26
Giga LAN BCM5789/5787M 35

SPI I/F
BIOS SST25LF080A 34

LPC BUS
SIO NS87381 32
FIR 32
KBC Renesas RE144B 31
Touch Pad 33
INT. KB 33
LPC DEBUG CONN. 34

PCB STACKUP

TOP	
GND	
S	
S	
VCC	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51120 40

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 41

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

TPS51100 43

1D8V_S3	DDR_VREF_S0

APL5332KAC 43

3D3V_S0	2D5V_S0

APL5912-U 43

1D8V_S3	1D5V_S0

MAXIM CHARGER MAX8725 42

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6262 38,39

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 44A

ATI M54 DC/DC FAN5234 52

INPUTS	OUTPUTS
DCBATOUT	VGA_CORE_S0

APL5331KAC 43

1D8V_S0	1D2V_S0

<Variant Name>

緯創資通 **Wistron Corporation**
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Title: **BLOCK DIAGRAM**
Size: A3 | Document Number: AG1 | Rev: -1M
Date: Wednesday, January 11, 2006 | Sheet 1 of 53

ICH7M Integrated Pull-up and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN, EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT, ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS, SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

ICH7M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

954305D 27Mhz/LCDCLK Spread and Frequency Selection Table

page 3

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+-0.25 Center
1	0	0	1	+-0.5 Center
1	0	1	0	+-0.75 Center
1	0	1	1	+-1.0 Center
1	1	0	0	+-0.25 Center
1	1	0	1	+-0.5 Center
1	1	1	0	+-0.75 Center
1	1	1	1	+-1.0 Center

PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
7412	22	A->G, B->B, C->F, D->G	0
MiniPCI	21	A/C -> E B/D -> E	1
LAN	23	A -> H	2

Calistoga Strapping Signals and Configuration

EDS 17050 0.71

page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 **1 = DMI x4** (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved **1 =Mobile CPU(Default)**
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable **1 = Normal Operation (Default)**
CFG18	VCC Select	**0 = 1.05V** (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL_DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

History

<Variant Name>

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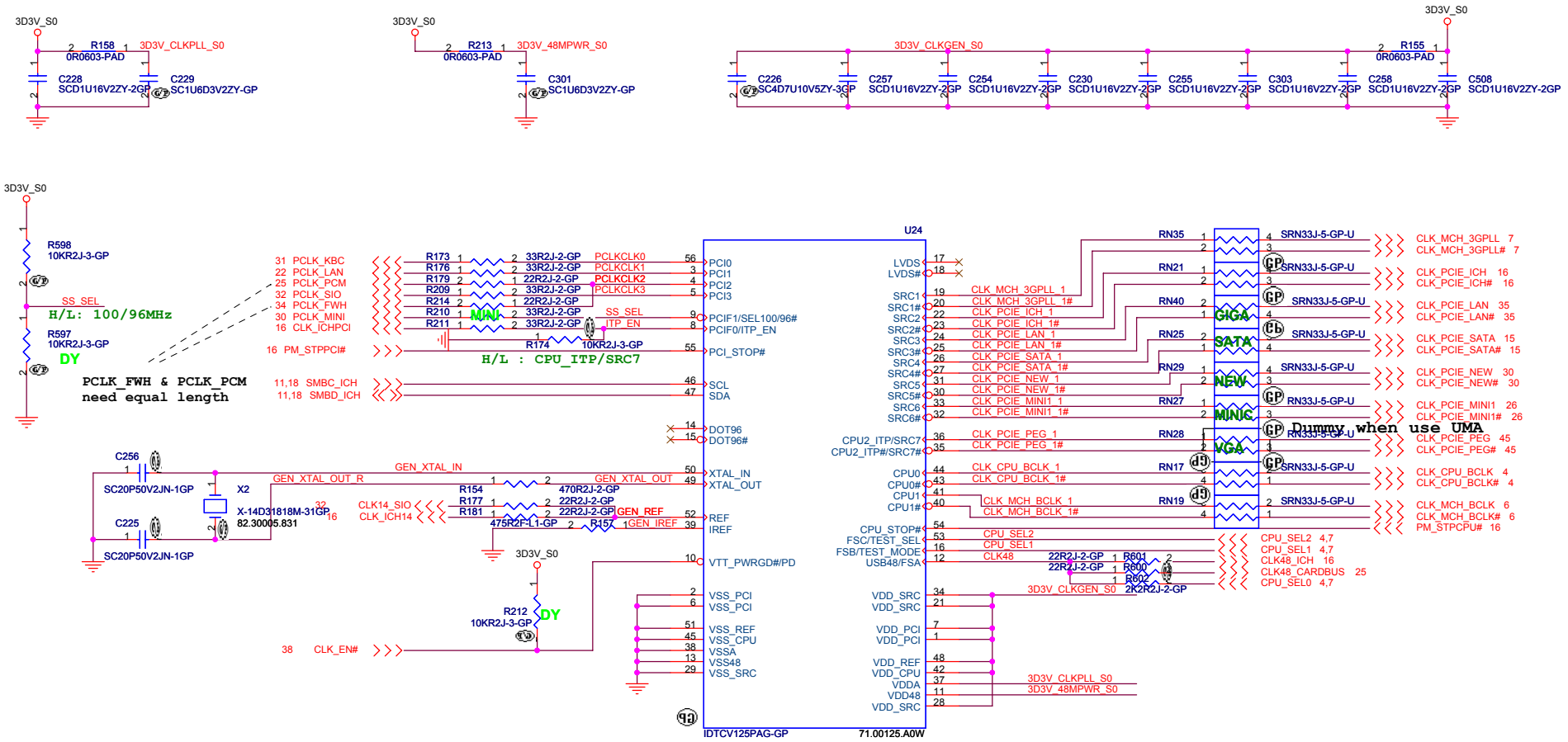
Title: Reference

Size: A3 | Document Number: AG1 | Rev: SD

Date: Tuesday, January 10, 2006 | Sheet 2 of 53



SEL2	SEL1	SEL0	CPU	FSB
0	0	0	266M	X
0	0	1	133M	533M
0	1	0	200M	X
0	1	1	166M	667M
1	0	0	333M	X
1	0	1	100M	X
1	1	0	400M	X
1	1	1	Reserved	X

<Variant Name>

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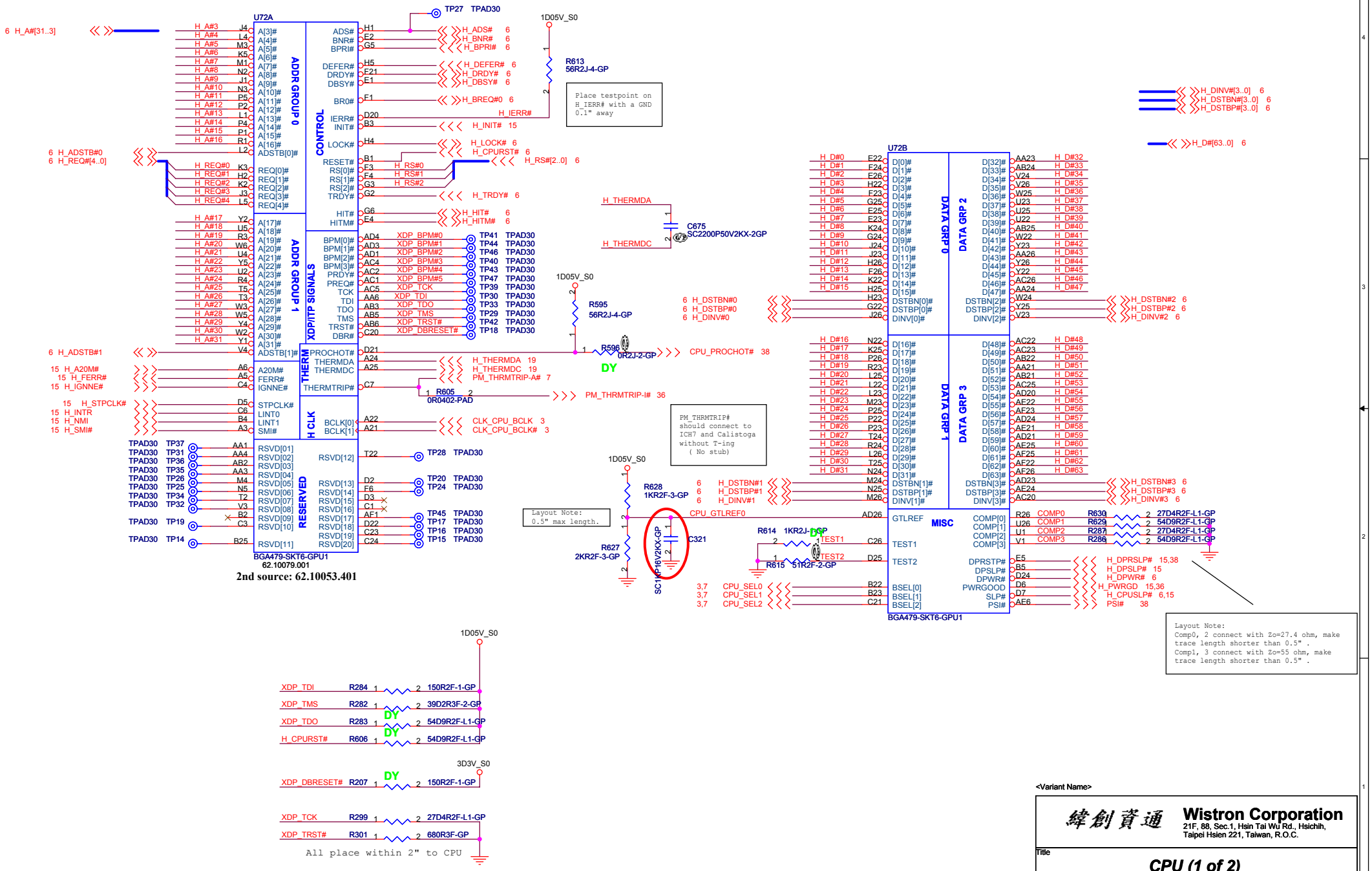
Title: Clock Generator IDT CVT125PAG

Size	Document Number	Rev
A3	AG1	-1

Date: Tuesday, January 10, 2006 Sheet 3 of 53



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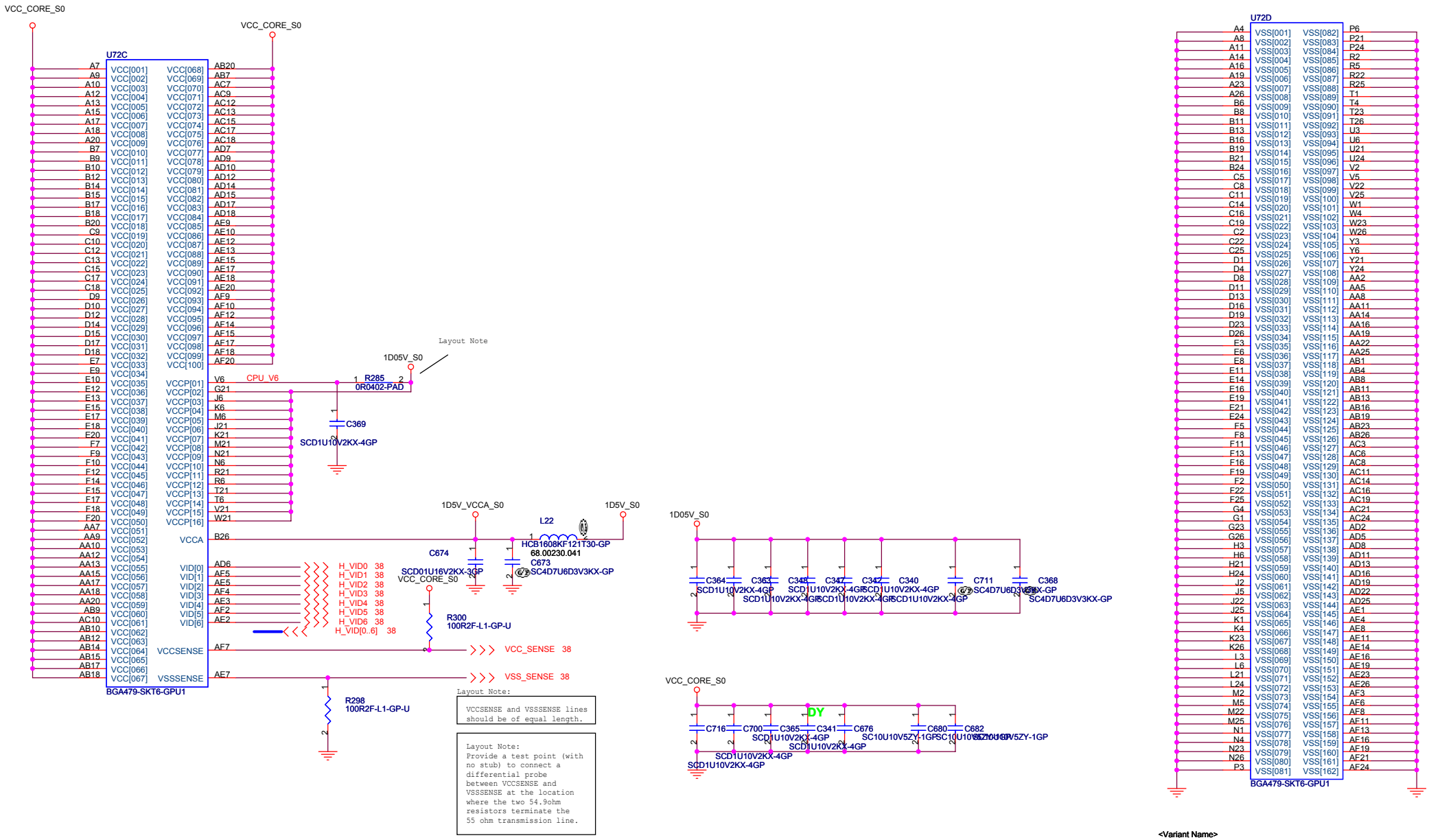
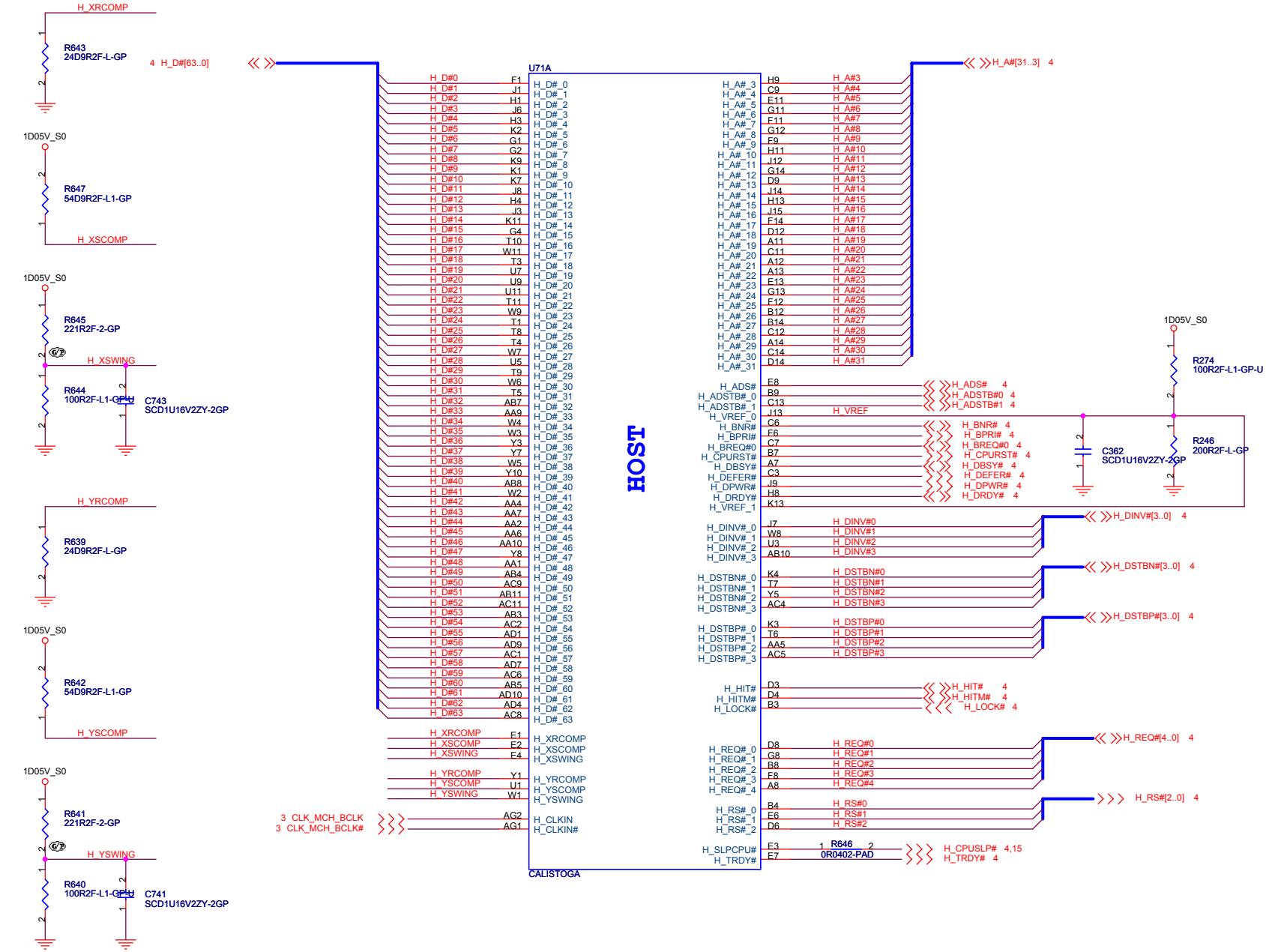
<variant_name>

Title: CPU (1 of 2)

Size: A3 | Document Number: AG1 | Rev: SC

Date: Tuesday, January 10, 2006 | Sheet 4 of 53


VCC_CORE_S0
U72C
BGA479-SKT6-GPU1
CPU_V6
R285
0R0402-PAD
1D05V_S0
Layout Note
C369
SCD1U10V2KX-4GP
1D5V_VCCA_S0
1D5V_S0
L22
HCB1608KF121T30-GP
68.00230.041
C674
SCD01U16V2KX-3GP
C673
SC4D7U6D3V3KX-GP
R300
100R2F-L1-GP-U
VCC_SENSE 38
VSS_SENSE 38
R298
100R2F-L1-GP-U
Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.
Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.
U72D
BGA479-SKT6-GPU1
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2 of 2)
Size A3
Document Number AG1
Rev SA
Date: Tuesday, January 10, 2006
Sheet 5 of 53



Place them near to the chip (< 0.5")

<Variant Name>

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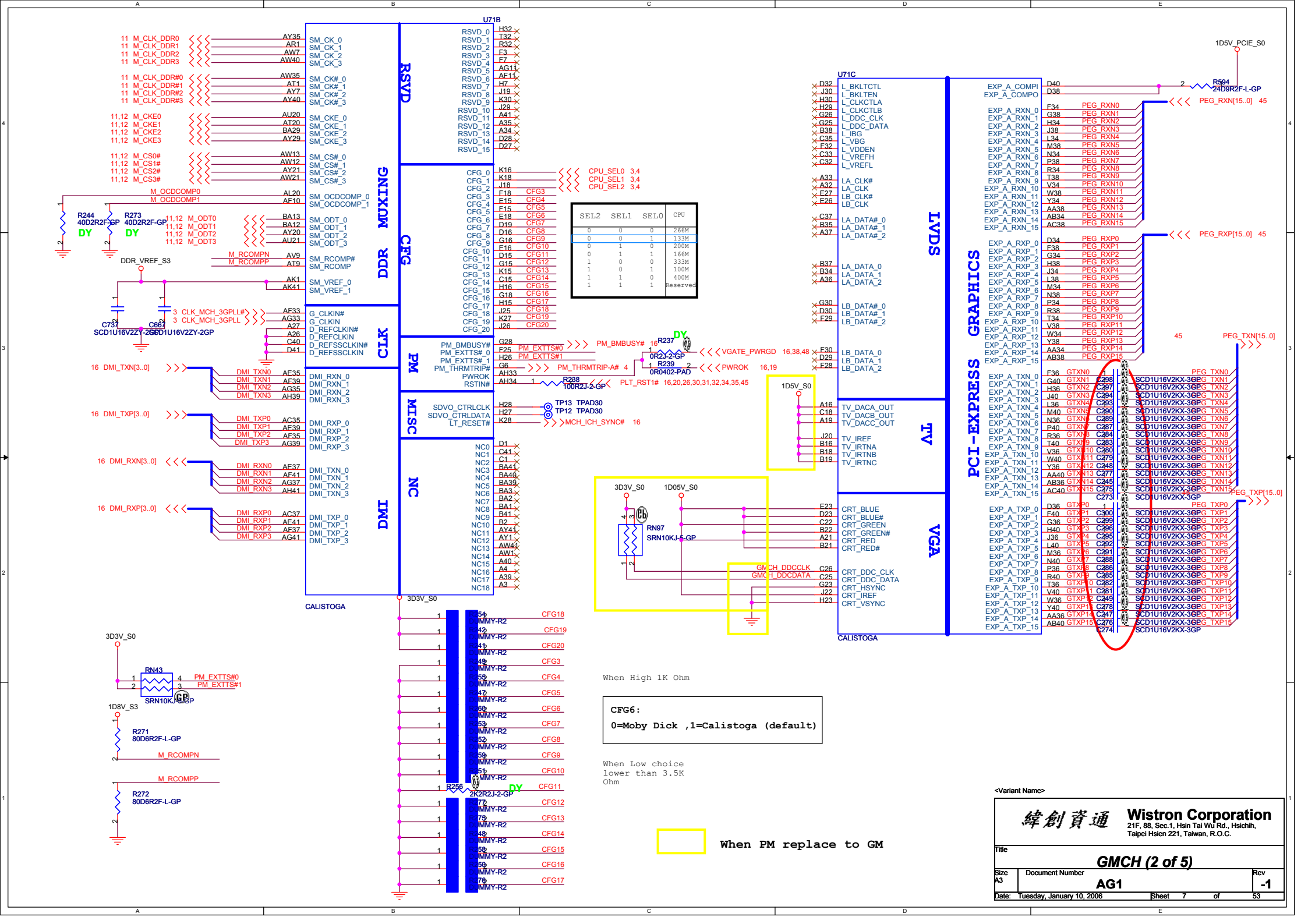
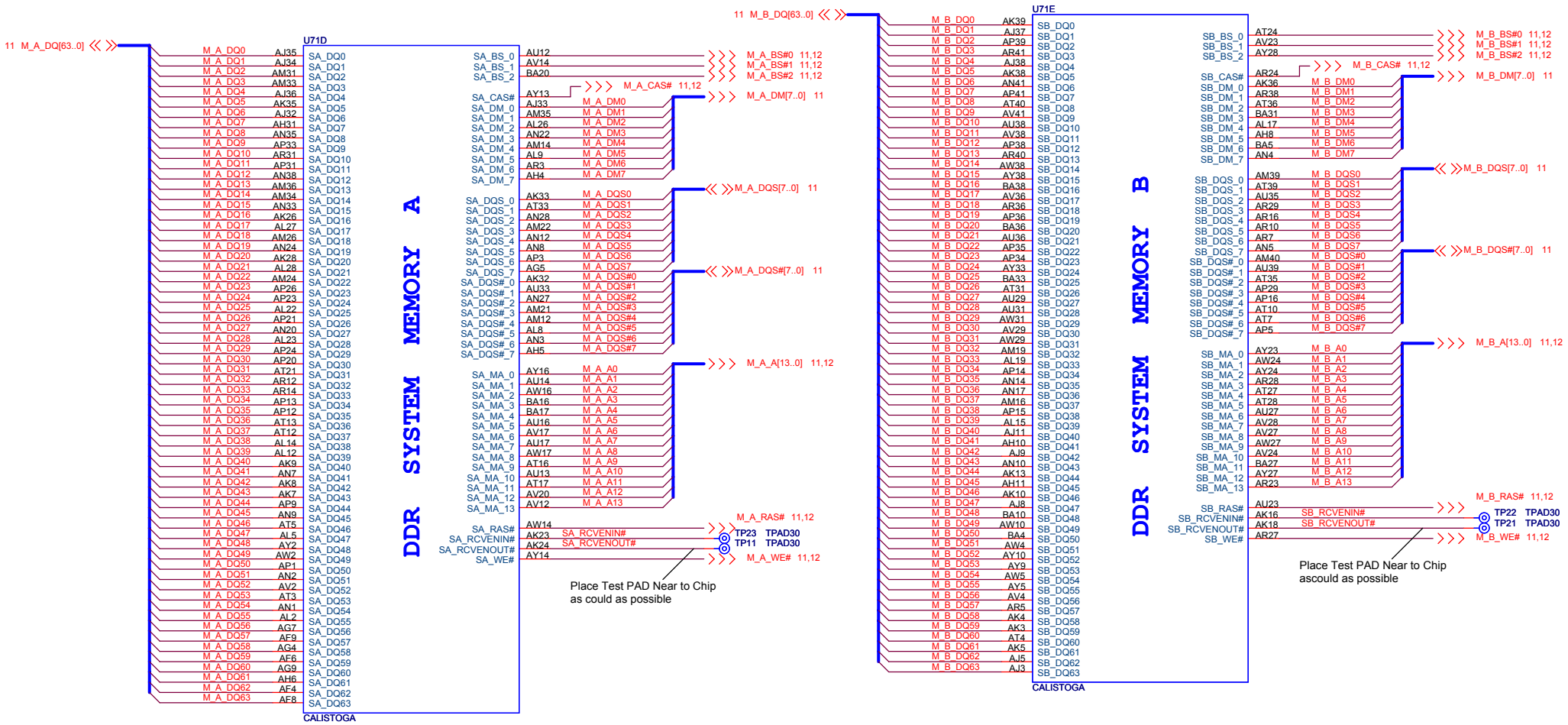
Title: **GMCH (1 of 5)**

Size	Document Number	Rev
A3	AG1	SA

Date: Tuesday, January 10, 2006 Sheet 6 of 53


U71B
RSVD
DDR MUXING
CFG
CLK
PM
MISC
NC
DMI
CALISTOGA
U71C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA
SEL2 SEL1 SEL0 CPU
0 0 0 266M
0 0 1 133M
0 1 0 200M
0 1 1 166M
1 0 0 333M
1 0 1 100M
1 1 0 400M
1 1 1 Reserved
When High 1K Ohm
CFG6:
0=Moby Dick ,1=Calistoga (default)
When Low choice lower than 3.5K Ohm
When PM replace to GM
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
GMCH (2 of 5)
AG1
Tuesday, January 10, 2006
Sheet 7 of 53



<Variant Name>

緯創資通 **Wistron Corporation**
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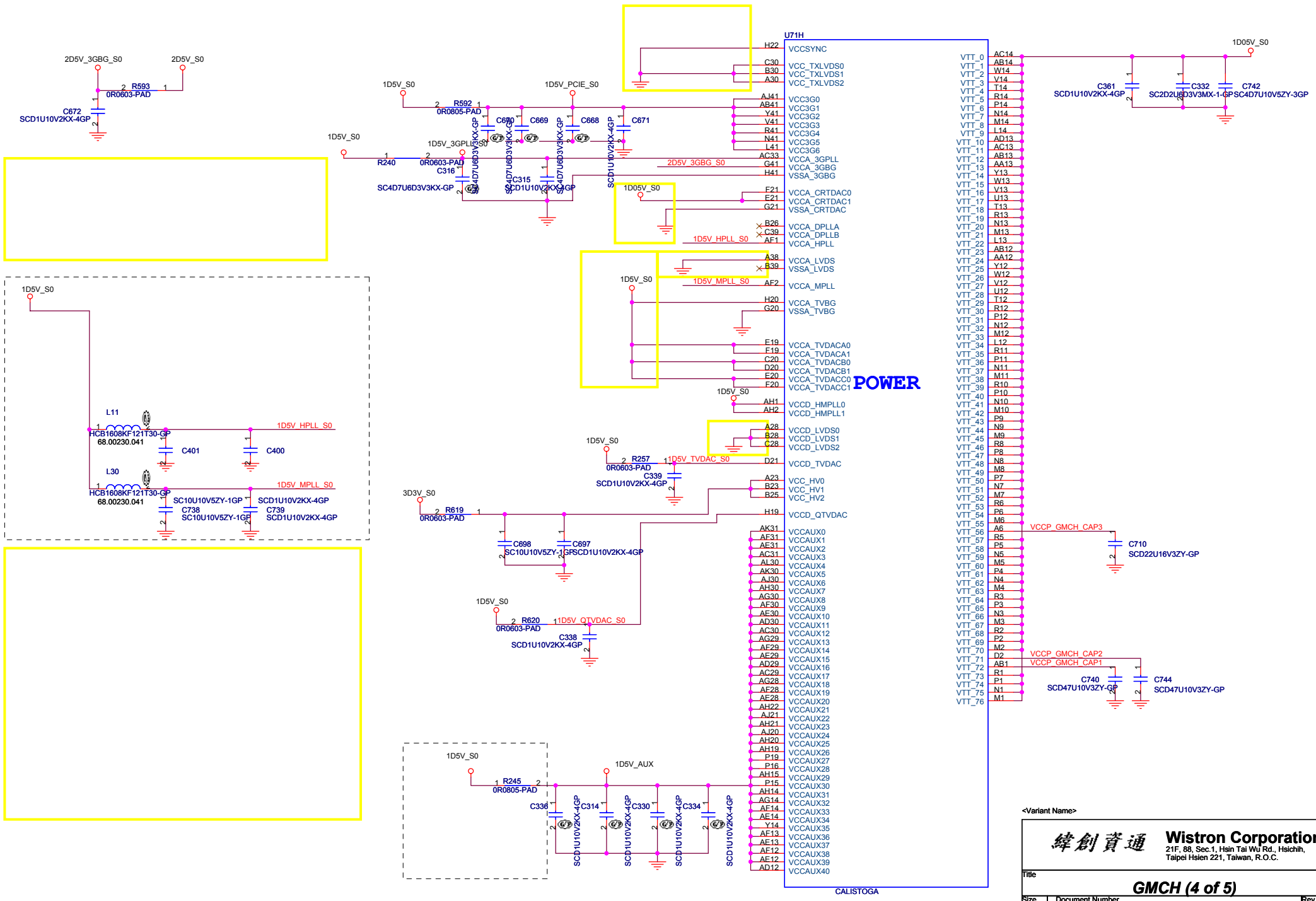
Title: **GMCH (3 of 5)**

Size	Document Number	Rev
A3	AG1	SA

Date: Tuesday, January 10, 2006 Sheet 8 of 53



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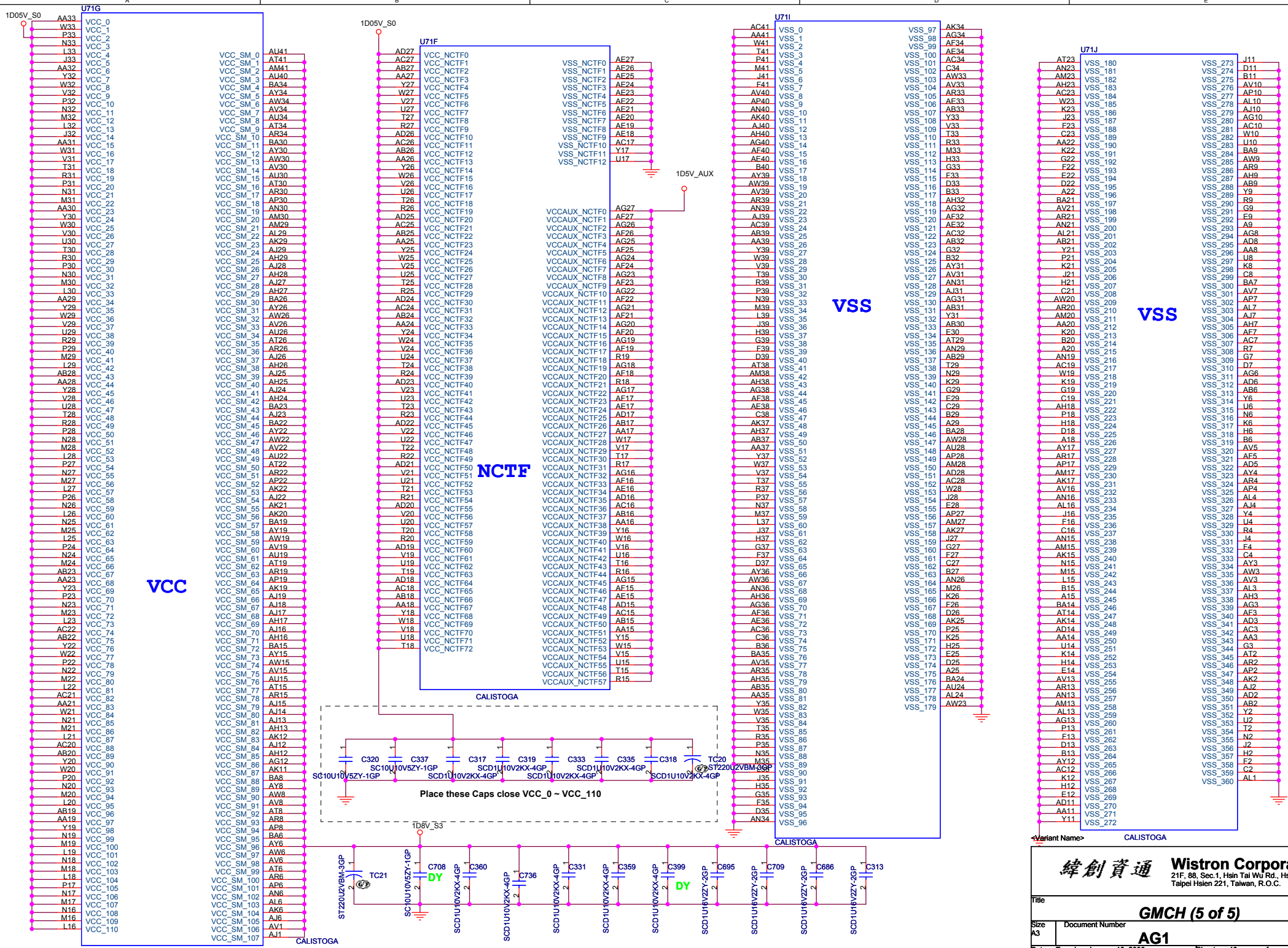
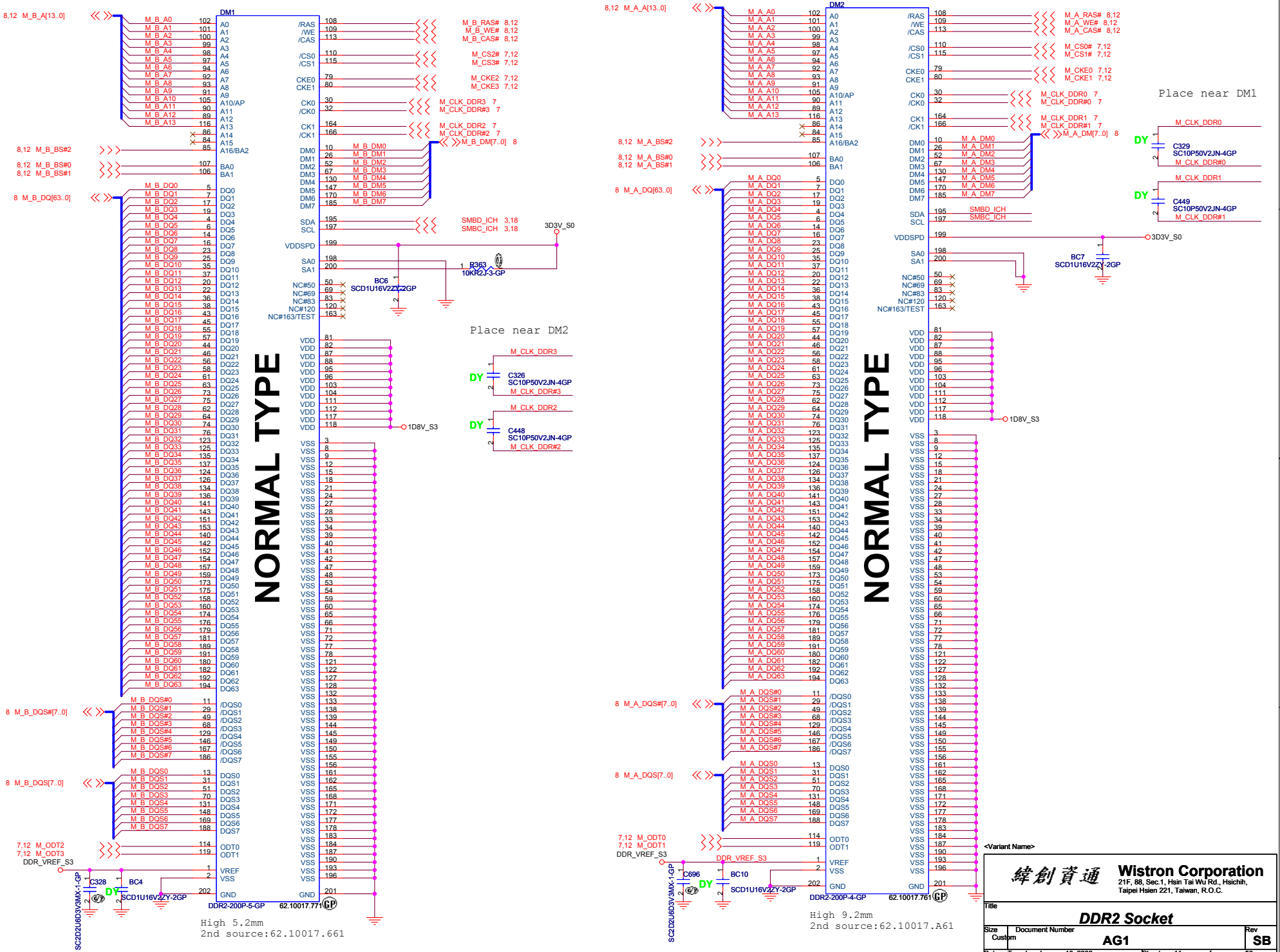
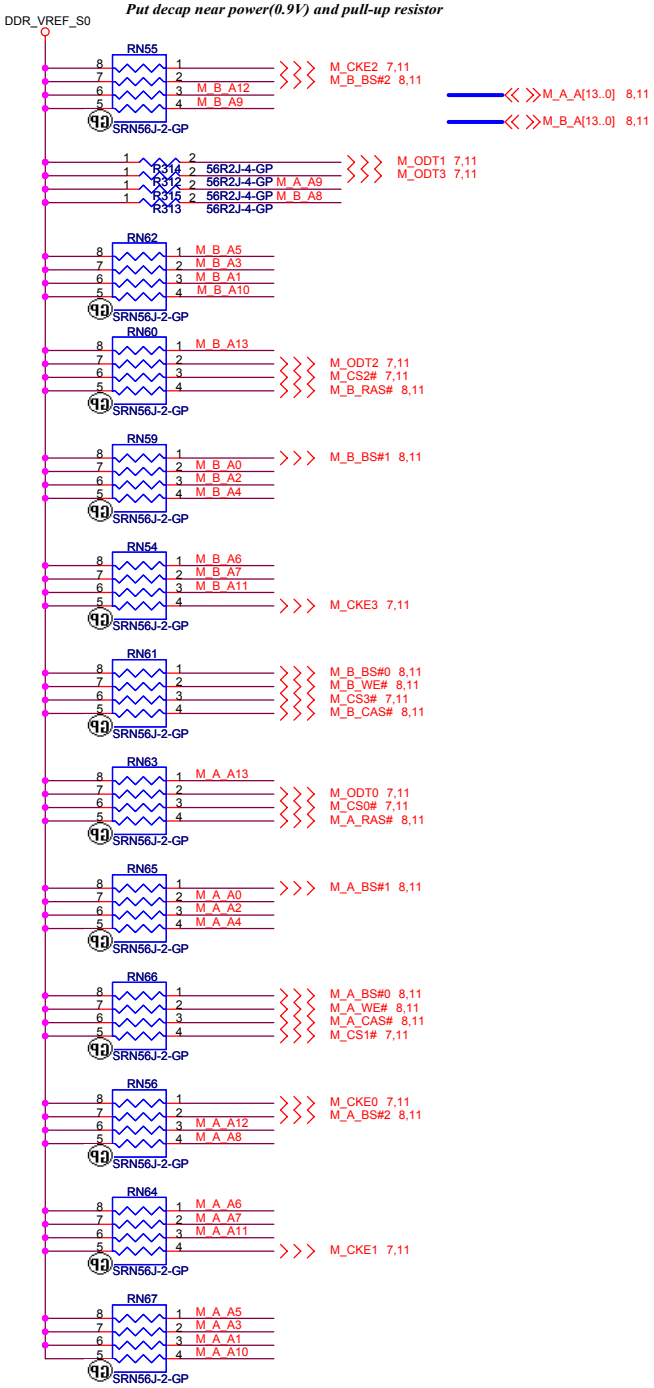
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***GMCH (4 of 5)***	
Size A3	Document Number **AG1**	Rev **SA**
Date: Tuesday, January 10, 2006	Sheet 9 of 53	



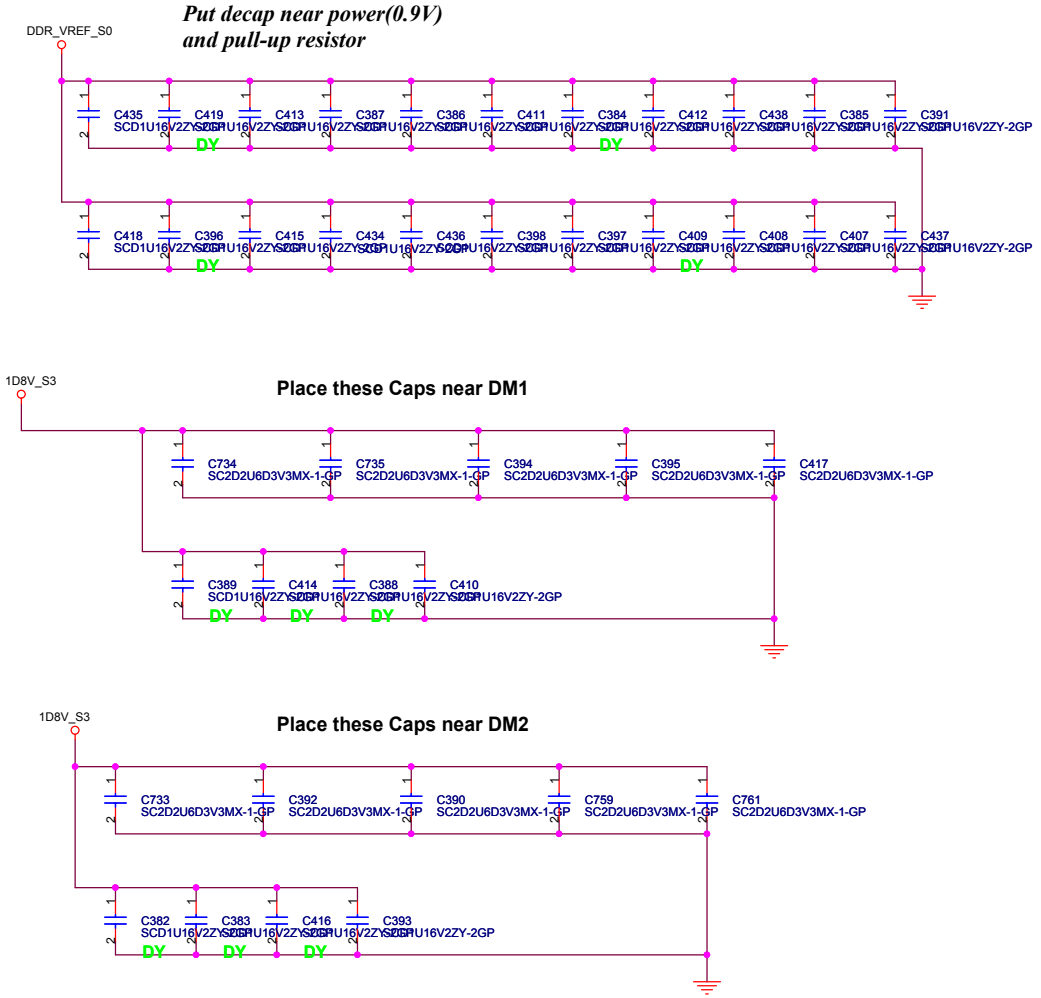
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	GMCH (5 of 5)
Size A3	Document Number AG1
Rev	SA
Date: Tuesday, January 10, 2006	Sheet 10 of 53


DM1
NORMAL TYPE
DDR2-200P-5-GP
62.10017.771
High 5.2mm
2nd source:62.10017.661
Place near DM2
M_CLK_DDR3
C326
SC10P50V2JN-4GP
M_CLK_DDR#3
M_CLK_DDR2
C448
SC10P50V2JN-4GP
M_CLK_DDR#2
BC6
SCD1U16V2ZY-2GP
R363
10KR2J-3-GP
C328
BC4
SCD1U16V2ZY-2GP
SC202U6D3V3MX-1-GP
DM2
NORMAL TYPE
DDR2-200P-4-GP
62.10017.761
High 9.2mm
2nd source:62.10017.A61
Place near DM1
M_CLK_DDR0
C329
SC10P50V2JN-4GP
M_CLK_DDR#0
M_CLK_DDR1
C449
SC10P50V2JN-4GP
M_CLK_DDR#1
BC7
SCD1U16V2ZY-2GP
C696
BC10
SCD1U16V2ZY-2GP
SC202U6D3V3MX-1-GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDR2 Socket
Size
Custom
Document Number
AG1
Rev
SB
Date: Tuesday, January 10, 2006
Sheet 11 of 53

PARALLEL TERMINATION



Decoupling Capacitor



<Variant Name>

緯創資通 **Wistron Corporation**
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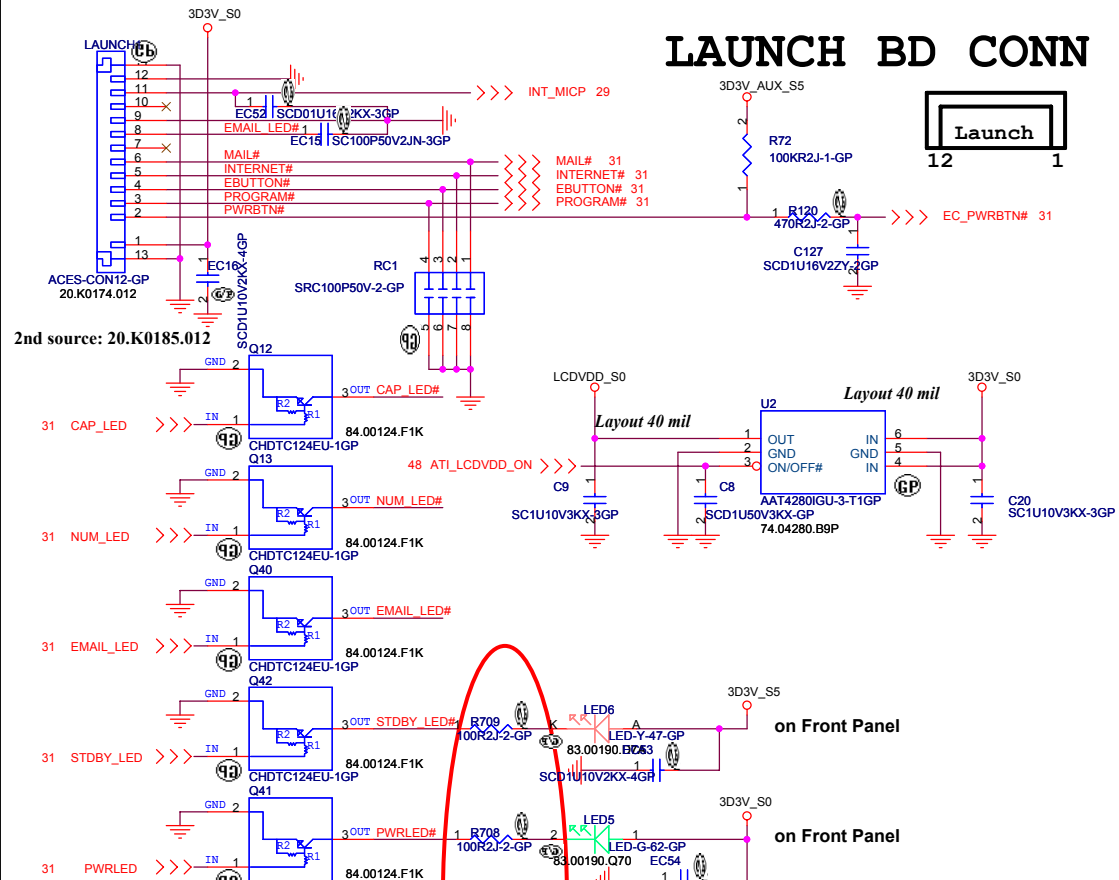
Title: ***DDR2 Termination Resistor***

Size	Document Number	Rev
A3	AG1	SA

Date: Tuesday, January 10, 2006 Sheet 12 of 53

LAUNCH BD CONN



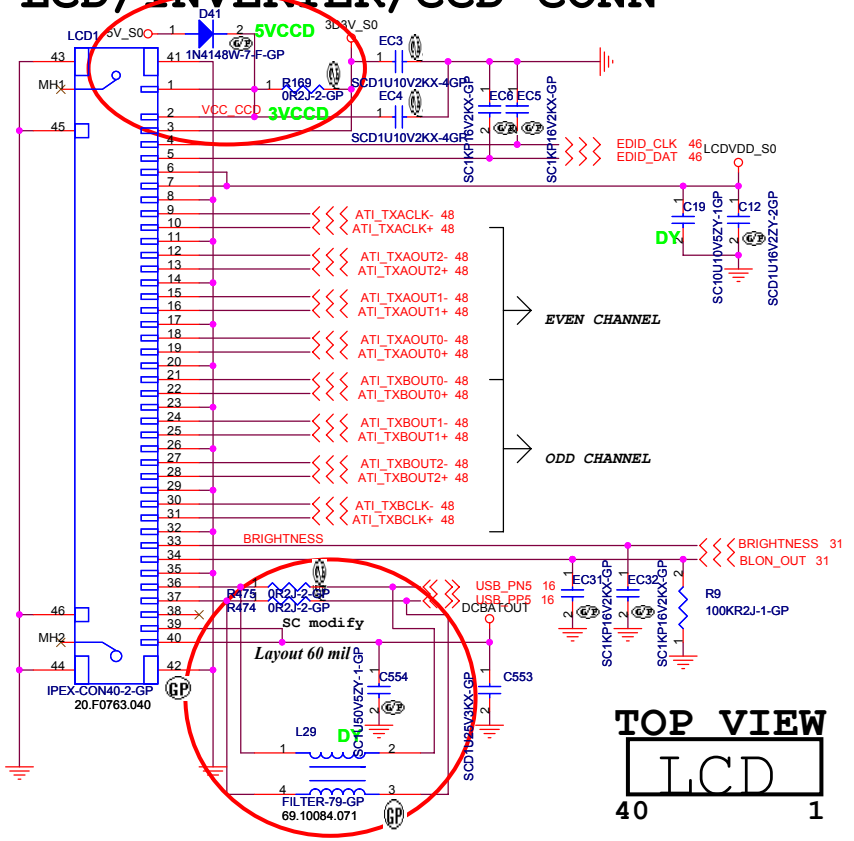
Launch
12 1

CCD Pin	
Pin	Symbol
1	5V
2	USB-
3	USB+
4	GND
5	GND

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Launch BD	
Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN

LCD/INVERTER/CCD CONN

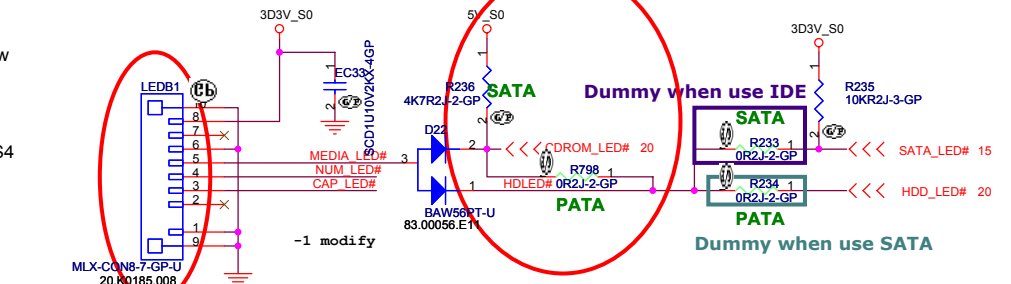


TOP VIEW
LCD
40 1

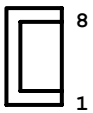
Charger:
OFF : Battery or DC only
Orange : Charging
Orange Blink : Battery low

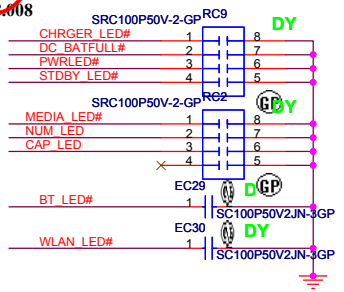
Power:
Green : S0
Orange : S3
Orange Blinking : Enter S4

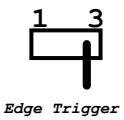
LED BD CONN



1st source: 20.K0228.008







Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

<Variant Name>

緯創資通 **Wistron Corporation**
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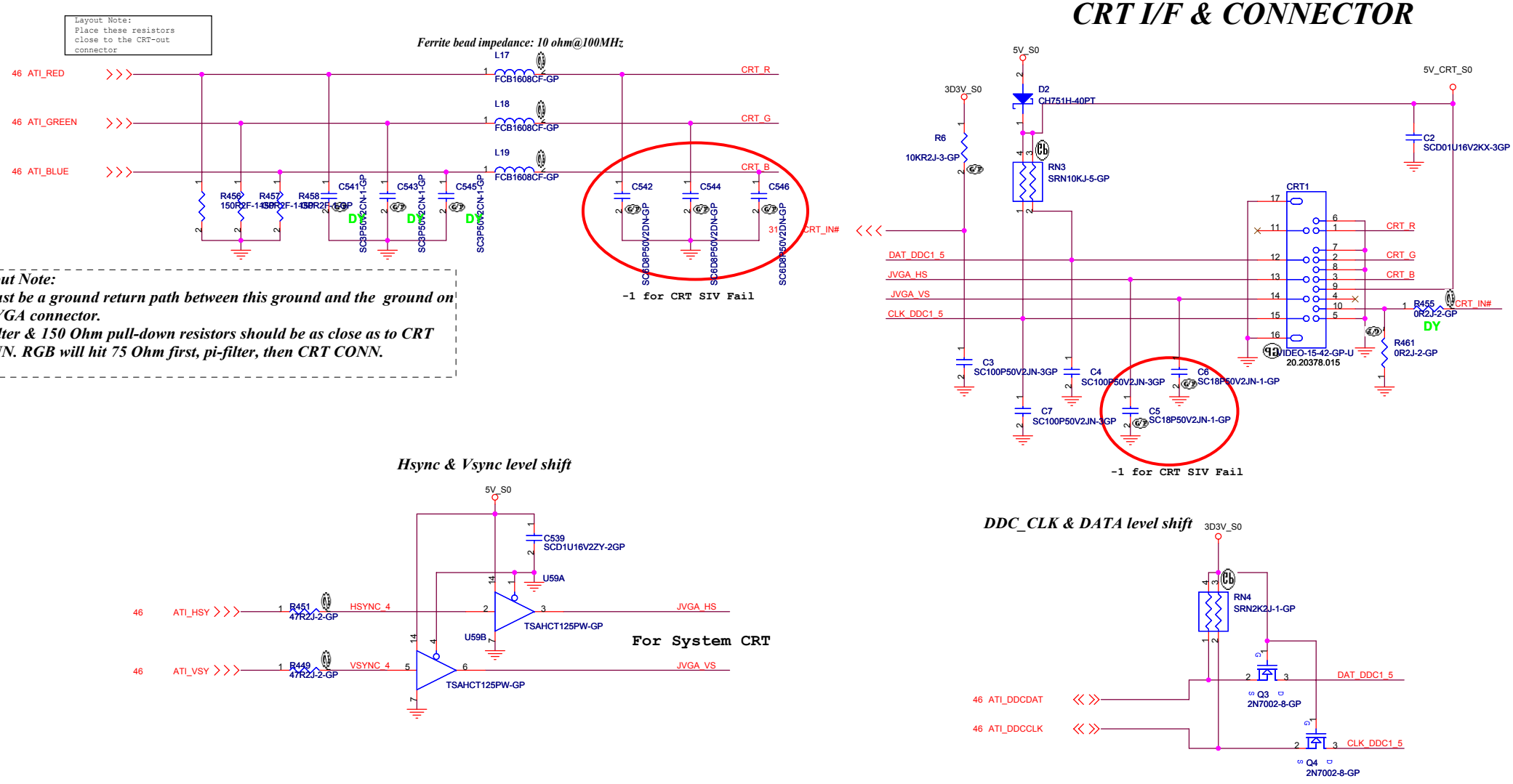
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LAUNCH / LEDs**

Size	Document Number	Rev
Custom	AG1	-1

Date: Tuesday, January 10, 2006 Sheet 13 of 53

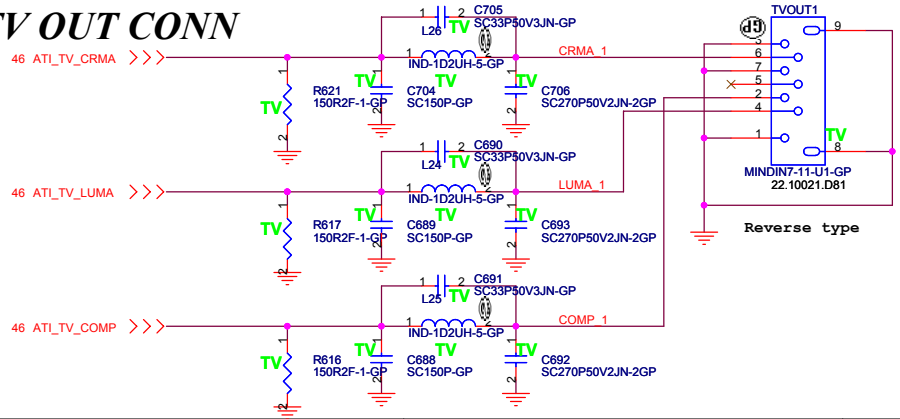
CRT I/F & CONNECTOR

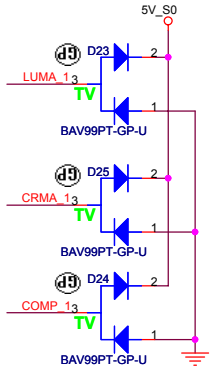


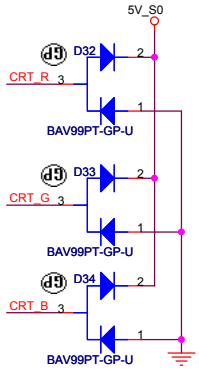
Hsync & Vsync level shift

DDC_CLK & DATA level shift

TV OUT CONN







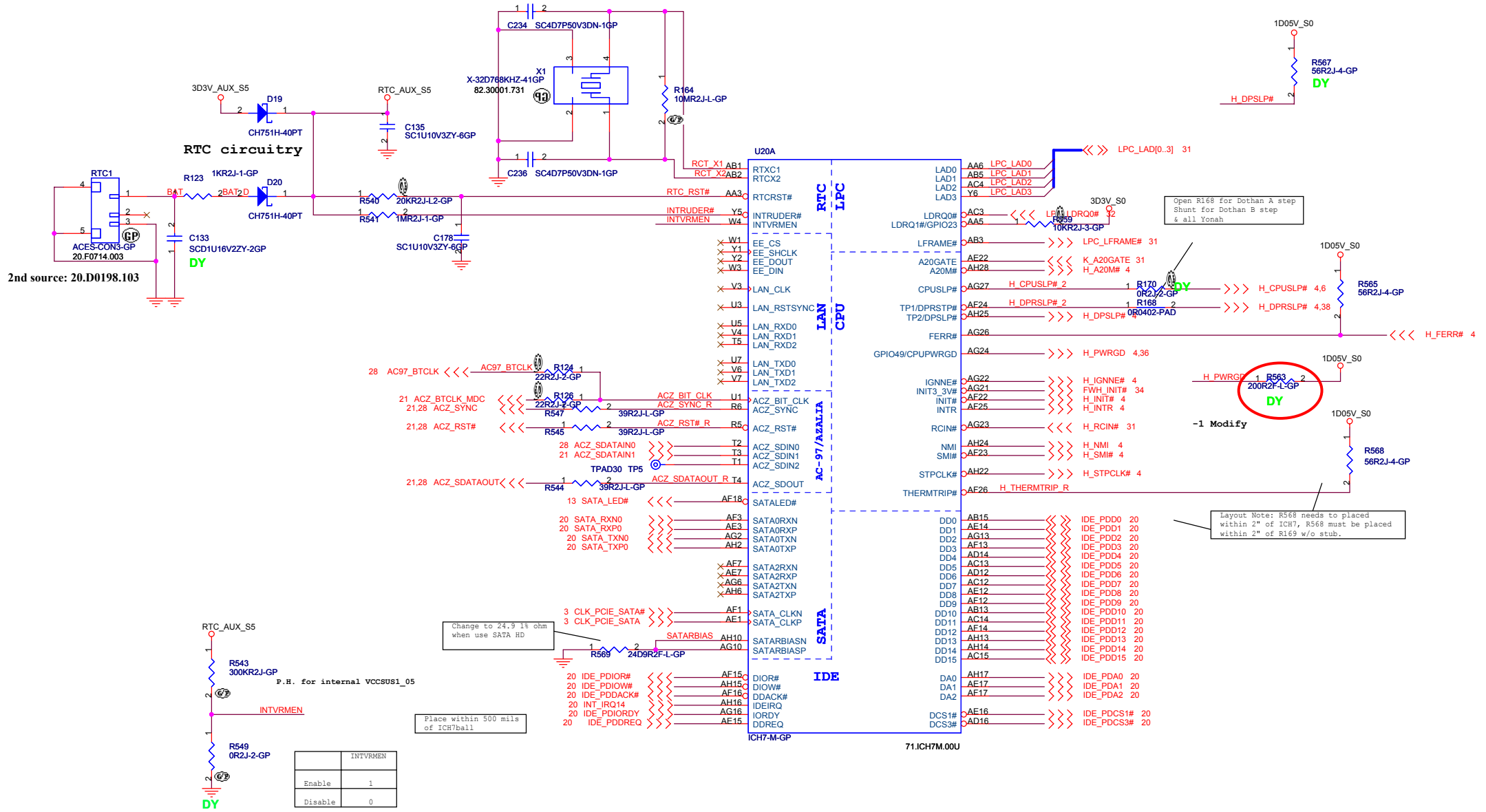
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT/TV Connector**

Size	Document Number	Rev
A3	AG1	-1

Date: Tuesday, January 10, 2006 Sheet 14 of 53



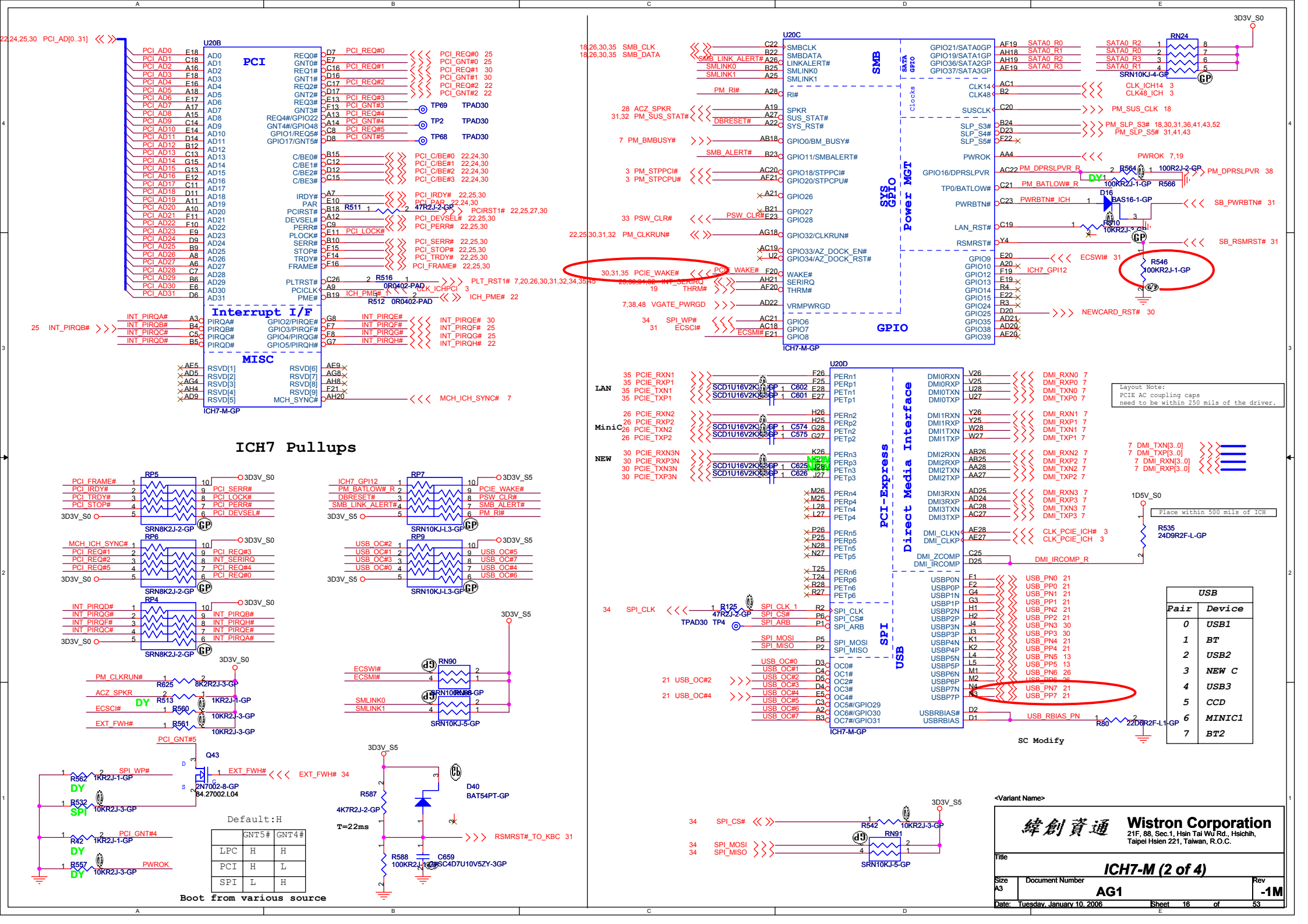
<Variant Name>

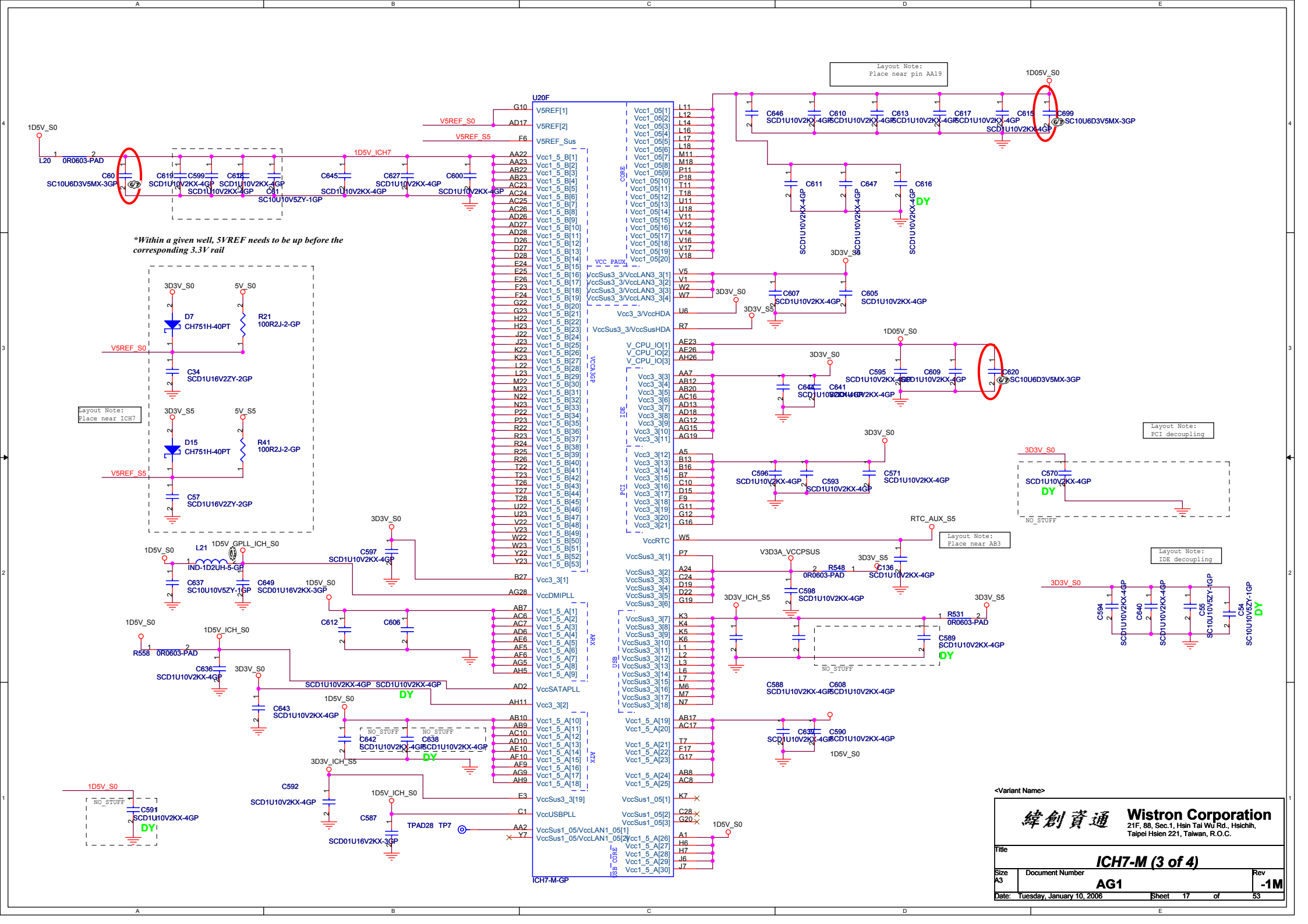
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

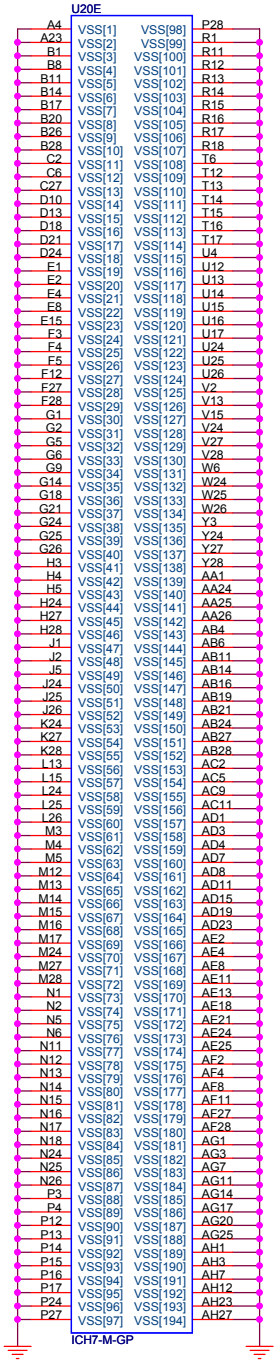
Title: ICH7-M (1 of 4)

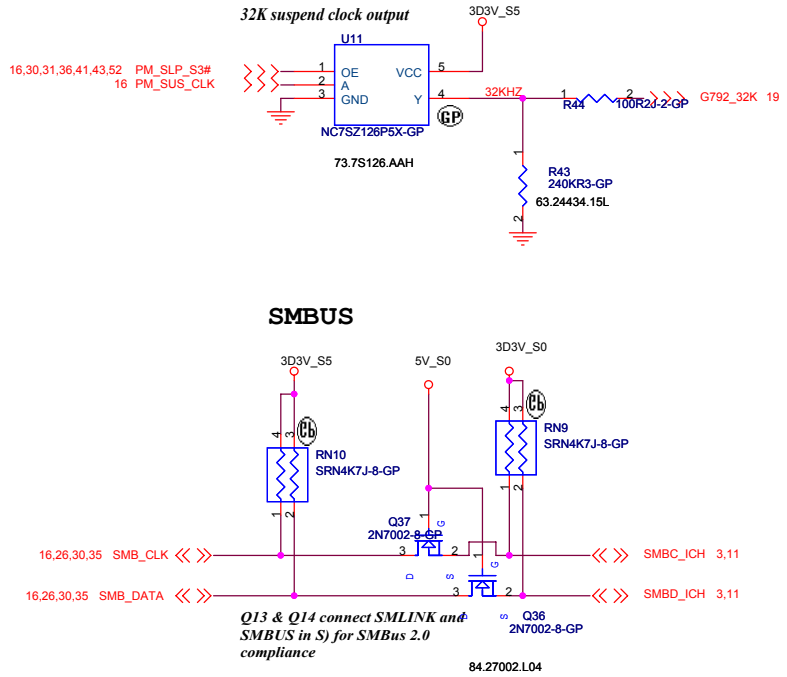
Size: A3 | Document Number: AG1 | Rev: -1

Date: Tuesday, January 10, 2006 | Sheet 15 of 53


U20B
PCI
Interrupt I/F
MISC
ICH7-M-GP
U20C
SMB
SYS GPIO
Power MGT
GPIO
ICH7-M-GP
U20D
PCI-Express
Direct Media Interface
SPI
USB
ICH7-M-GP
ICH7 Pullups
Default:H
Boot from various source
SC Modify
Layout Note:
PCIE AC coupling caps
need to be within 250 mils of the driver.
USB
Pair Device
0 USB1
1 BT
2 USB2
3 NEW C
4 USB3
5 CCD
6 MINIC1
7 BT2
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (2 of 4)
Size A3
Document Number AG1
Rev -1M
Date: Tuesday, January 10, 2006
Sheet 16 of 53


U20F
ICH7-M-GP
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note: Place near pin AA19
Layout Note: Place near ICH7
Layout Note: PCI decoupling
Layout Note: Place near AB3
Layout Note: IDE decoupling
1D5V_S0
1D05V_S0
3D3V_S0
3D3V_S5
5V_S0
5V_S5
V5REF_S0
V5REF_S5
1D5V_ICH7
1D5V_GPLL_ICH_S0
1D5V_ICH_S0
3D3V_ICH_S5
V3D3A_VCCPSUS
RTC_AUX_S5
L20 0R0603-PAD
L21 IND-1D2UH-5-GP
C60 SC10U6D3V5MX-3GP
C81 SC10U10V5ZY-1GP
C637 SC10U10V5ZY-1GP
C649 SCD01U16V2KX-3GP
C699 SC10U6D3V5MX-3GP
C620 SC10U6D3V5MX-3GP
C54 SC10U10V5ZY-1GP
C55 SC10U10V5ZY-1GP
D7 CH751H-40PT
D15 CH751H-40PT
R21 100R2J-2-GP
R41 100R2J-2-GP
C34 SCD1U16V2ZY-2GP
C57 SCD1U16V2ZY-2GP
SCD1U10V2KX-4GP
SCD1U10V2KX-4GP DY
SCD01U16V2KX-3GP
R548 0R0603-PAD
R558 0R0603-PAD
R531 0R0603-PAD
C136 SCD1U10V2KX-4GP
C588 SCD1U10V2KX-4GP
C589 SCD1U10V2KX-4GP DY
C590 SCD1U10V2KX-4GP
C591 SCD1U10V2KX-4GP DY
C592 SCD1U10V2KX-4GP
C587 SCD01U16V2KX-3GP
TPAD28 TP7
NO_STUFF
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH7-M (3 of 4)
Size A3
Document Number AG1
Rev -1M
Date: Tuesday, January 10, 2006
Sheet 17 of 53





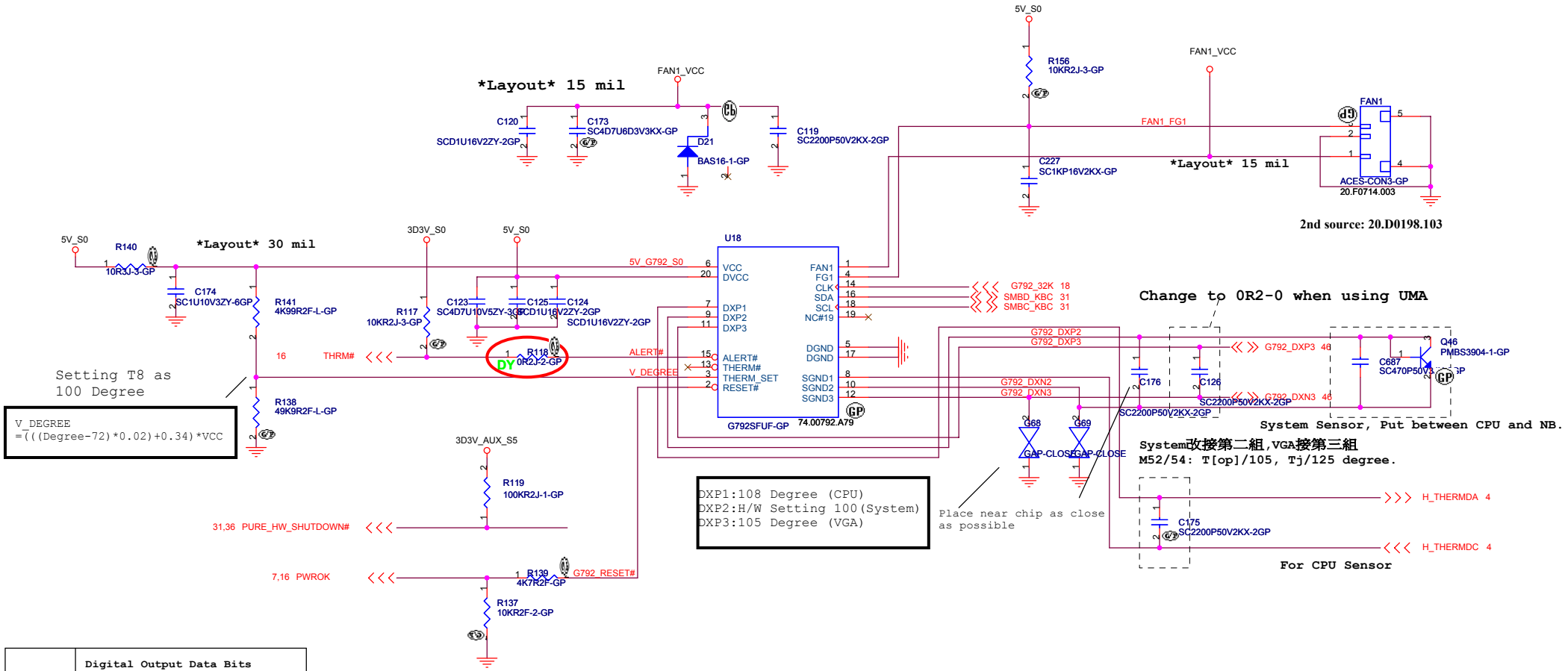
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH7-M (4 of 4)

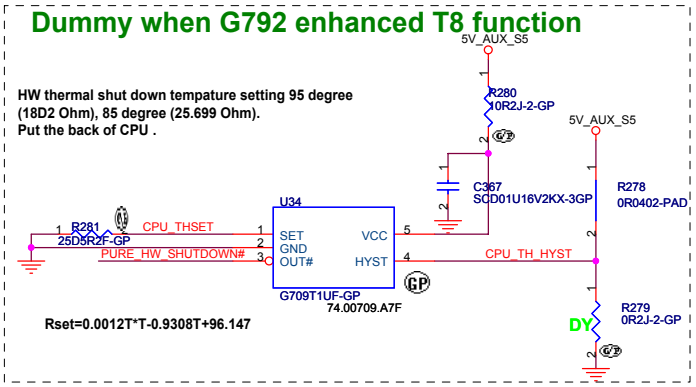
Size	Document Number	Rev
A3	AG1	SD

Date: Tuesday, January 10, 2006 Sheet 18 of 53



TEMP.	Digital Output Data Bits			
	Sign	MSB	LSB	EXT
+127.875	0	111	1111	111
+126.375	0	111	1110	011
+25.5	0	001	1001	100
+1.75	0	000	0001	110
+0.5	0	000	0000	100
+0.125	0	000	0000	001
-0.125	1	111	1111	111
-1.125	1	111	1110	111
-25.5	1	110	0110	100
-55.25	1	100	1000	110
-65.000	1	011	1111	000

Dummy when G792 enhanced T8 function



Thermal Get Setting

		T6	T7
Sencor 0	CPU DTS	98	100
Sencor 1	G792-1 CPU	98	100
Sencor 2	G792-2 System	78	83
Sencor 3	G792-3 VGA	110	115

<Variant Name>

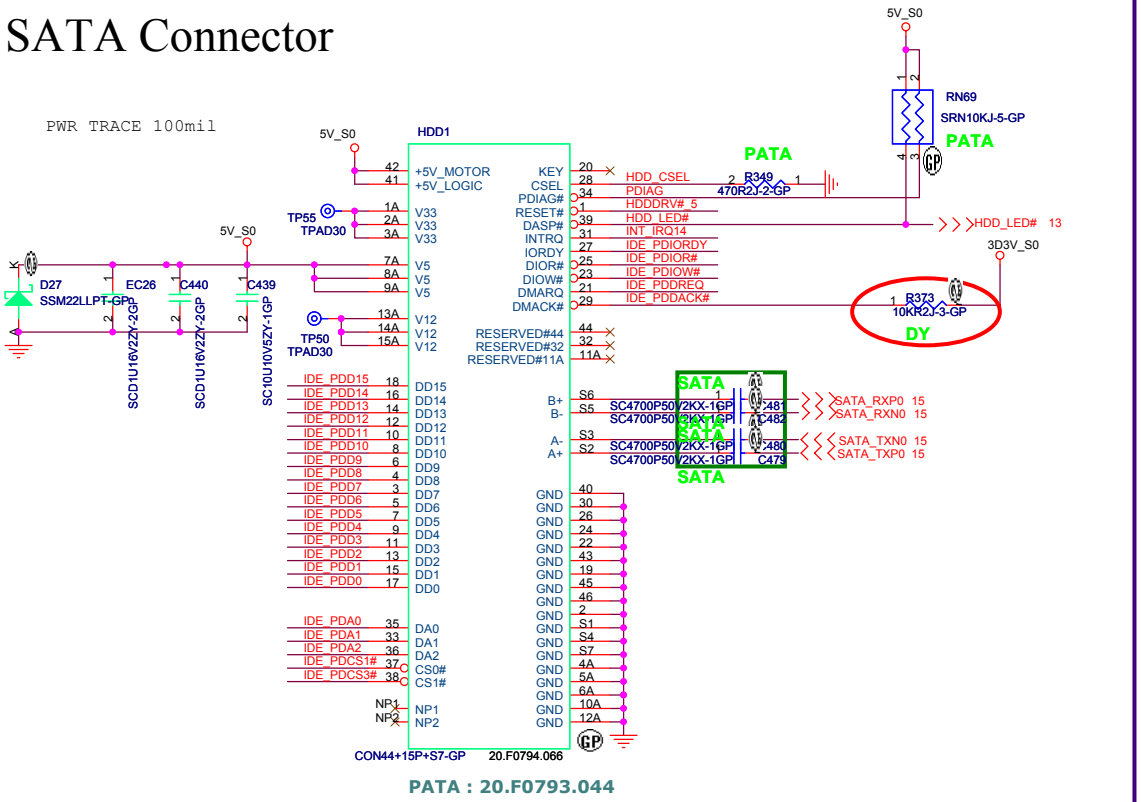
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Thermal/Fan Controllor G792

Size	Document Number	Rev
Custom	AG1	SC

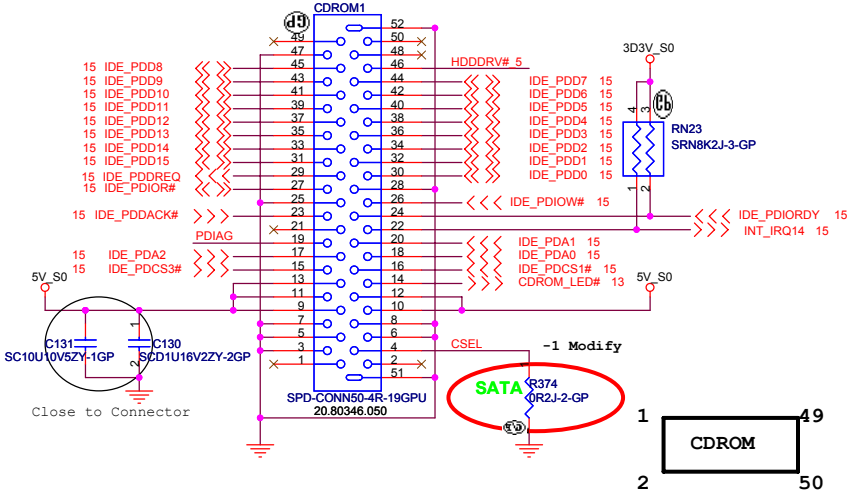
Date: Tuesday, January 10, 2006 Sheet 19 of 53

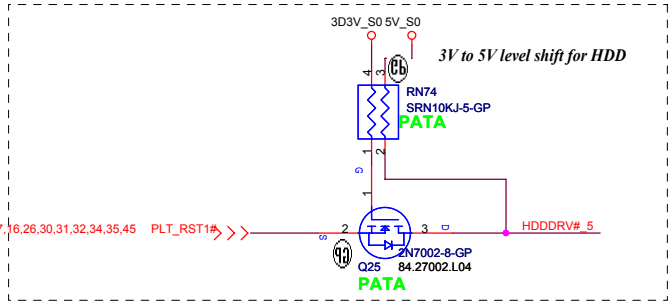
SATA Connector



PATA : 20.F0793.044

CDROM Connector



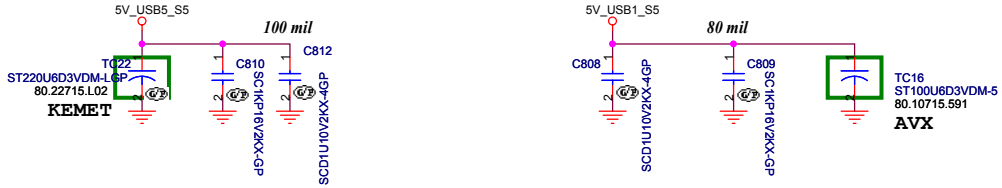


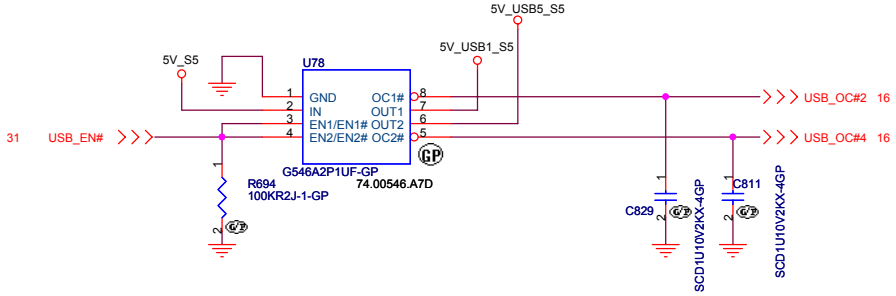
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

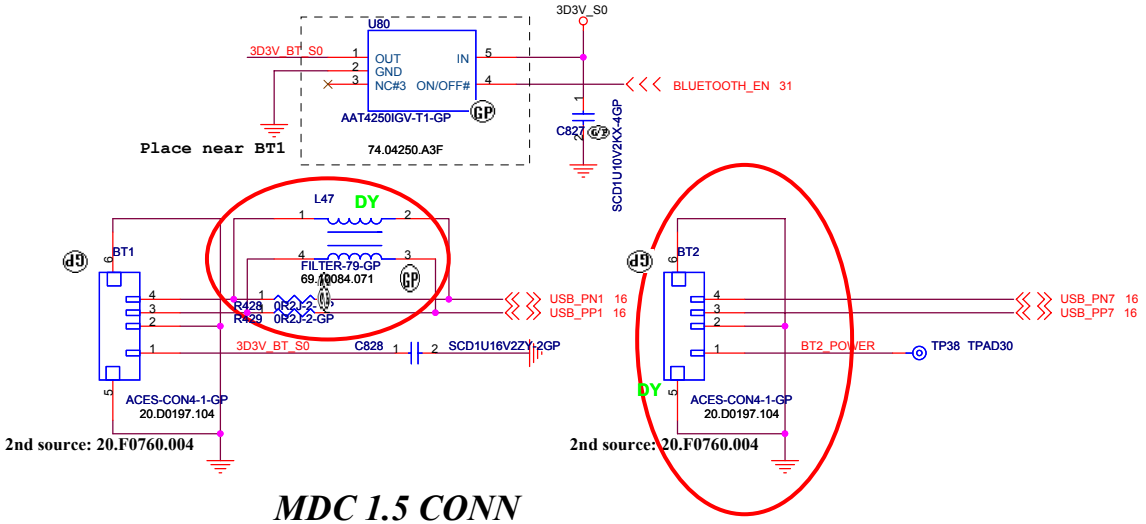
Title	**SATA/PATA HDD / ODD**	
Size A3	Document Number **AG1**	Rev **-1**
Date: Tuesday, January 10, 2006	Sheet 20 of 53	

USB PORT

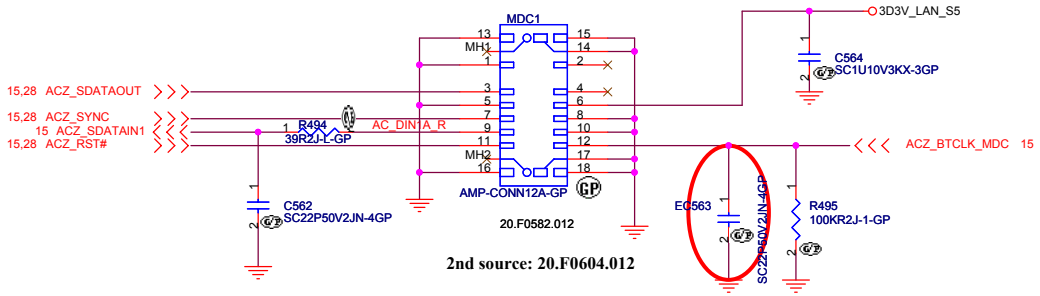


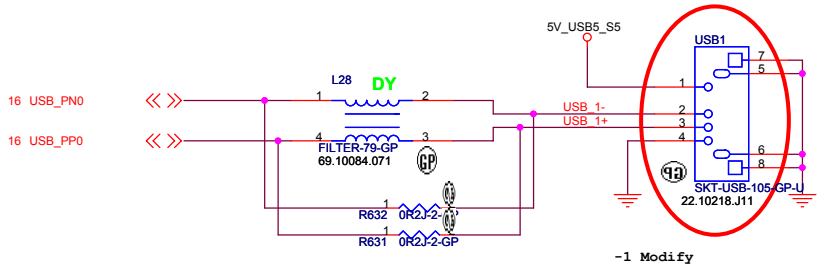


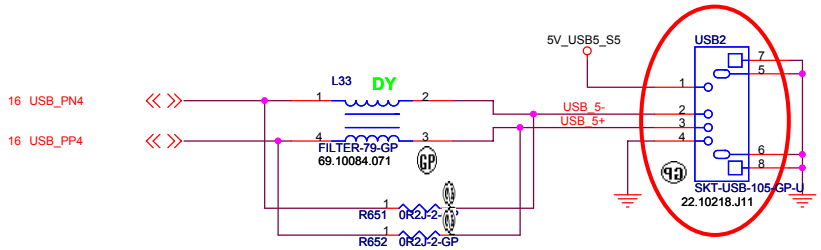
BLUETOOTH MODULE CONNECTOR

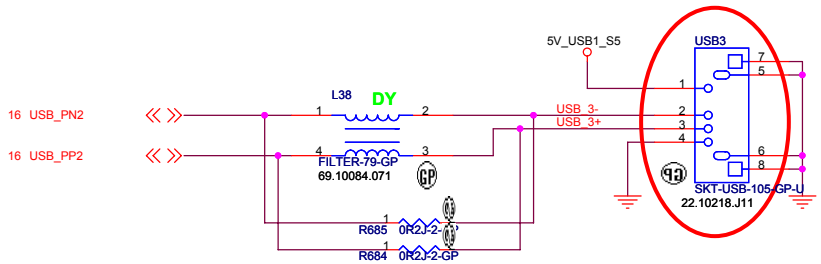


MDC 1.5 CONN









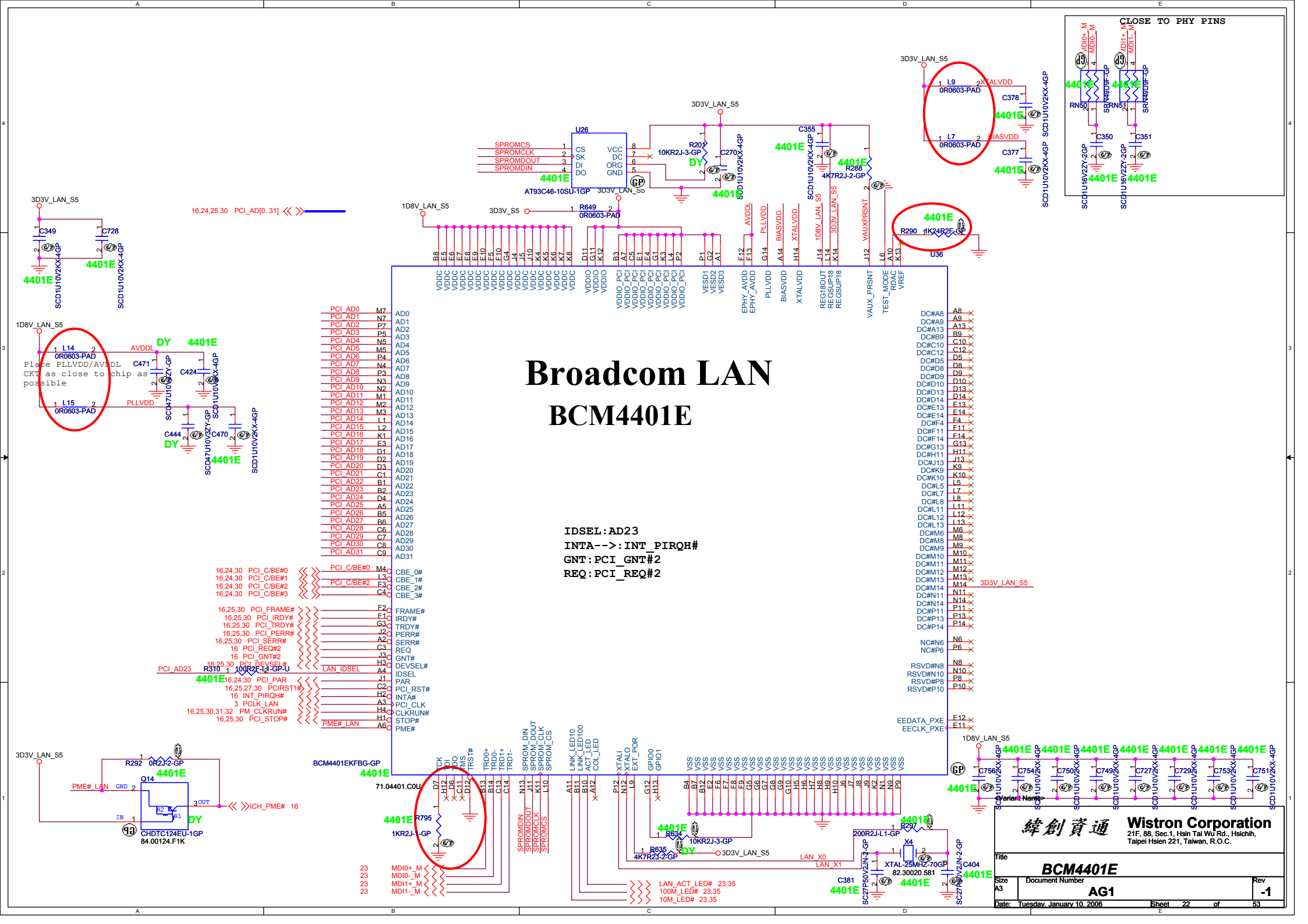
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC I/F

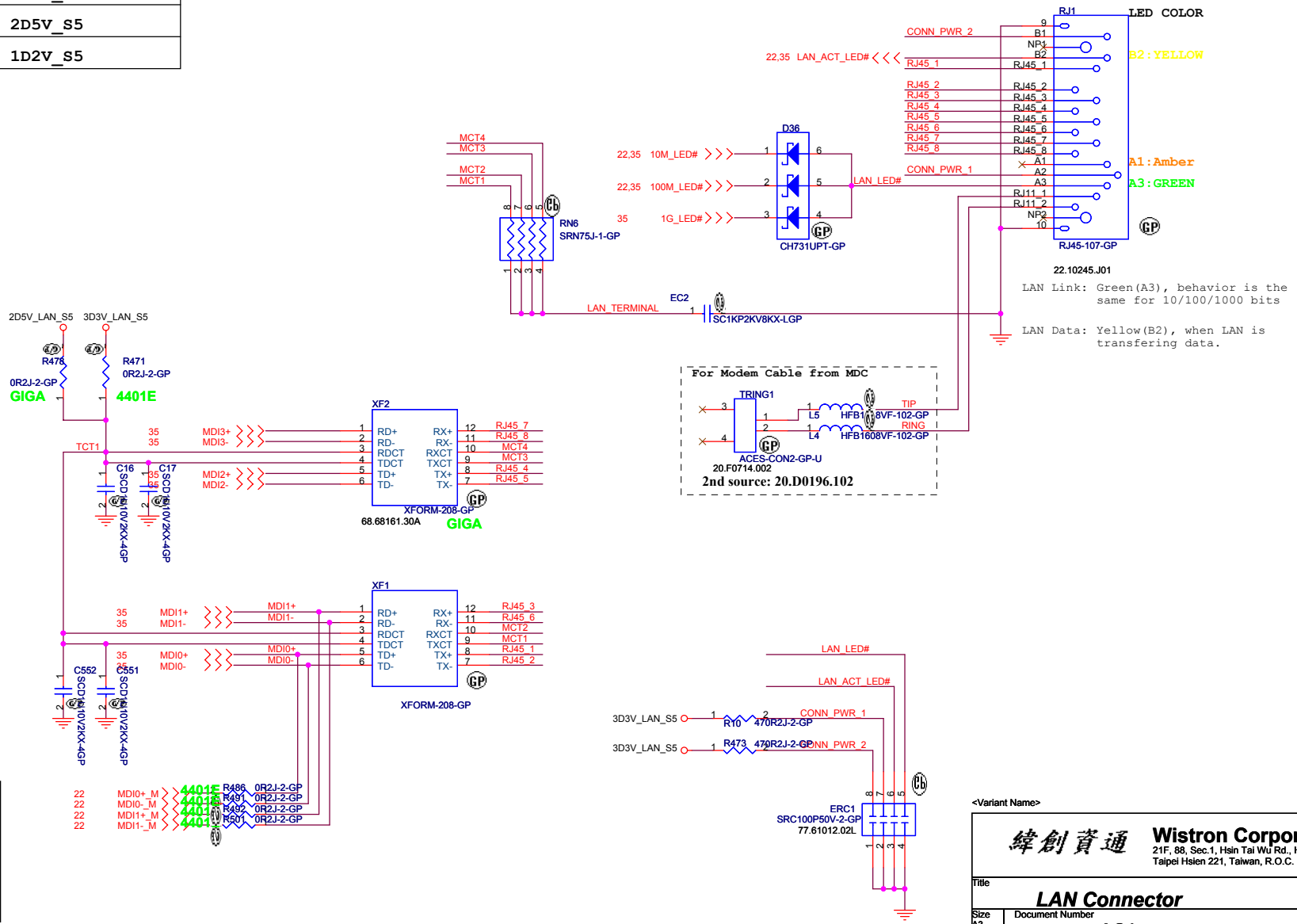
Size	Document Number	Rev
A3	AG1	-1

Date: Tuesday, January 10, 2006 Sheet 21 of 53


CLOSE TO PHY PINS
Broadcom LAN
BCM4401E
IDSEL:AD23
INTA-->:INT_PIRQH#
GNT:PCI_GNT#2
REQ:PCI_REQ#2
Place PLLVDD/AVDDL CKT as close to chip as possible
BCM4401EKFBG-GP
AT93C46-10SU-1GP
CHDTC124EU-1GP
84.00124.F1K
71.04401.C0U
XTAL-25MHZ-70GP
82.30020.581
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM4401E
Size A3
Document Number AG1
Rev -1
Date: Tuesday, January 10, 2006
Sheet 22 of 53

LAN Connector

Voltage Rail	4401E	5789	5787
VDDIO_PCI	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDC	1D8V_LAN_S5	1D2V_LAN_S5	
VDDIO	3D3V_LAN_S5	3D3V_LAN_S5	
VESD	3D3V_LAN_S5	3D3V_S0	Don't Care
VDDP	Don't Care	2D5V_S5	
3D3V_2D5V_S5	3D3V_S5	2D5V_S5	
1D8V_1D2V_S5	1D8V_LAN_S5	1D2V_S5	



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN Connector**

Size	Document Number	Rev
A3	AG1	SD

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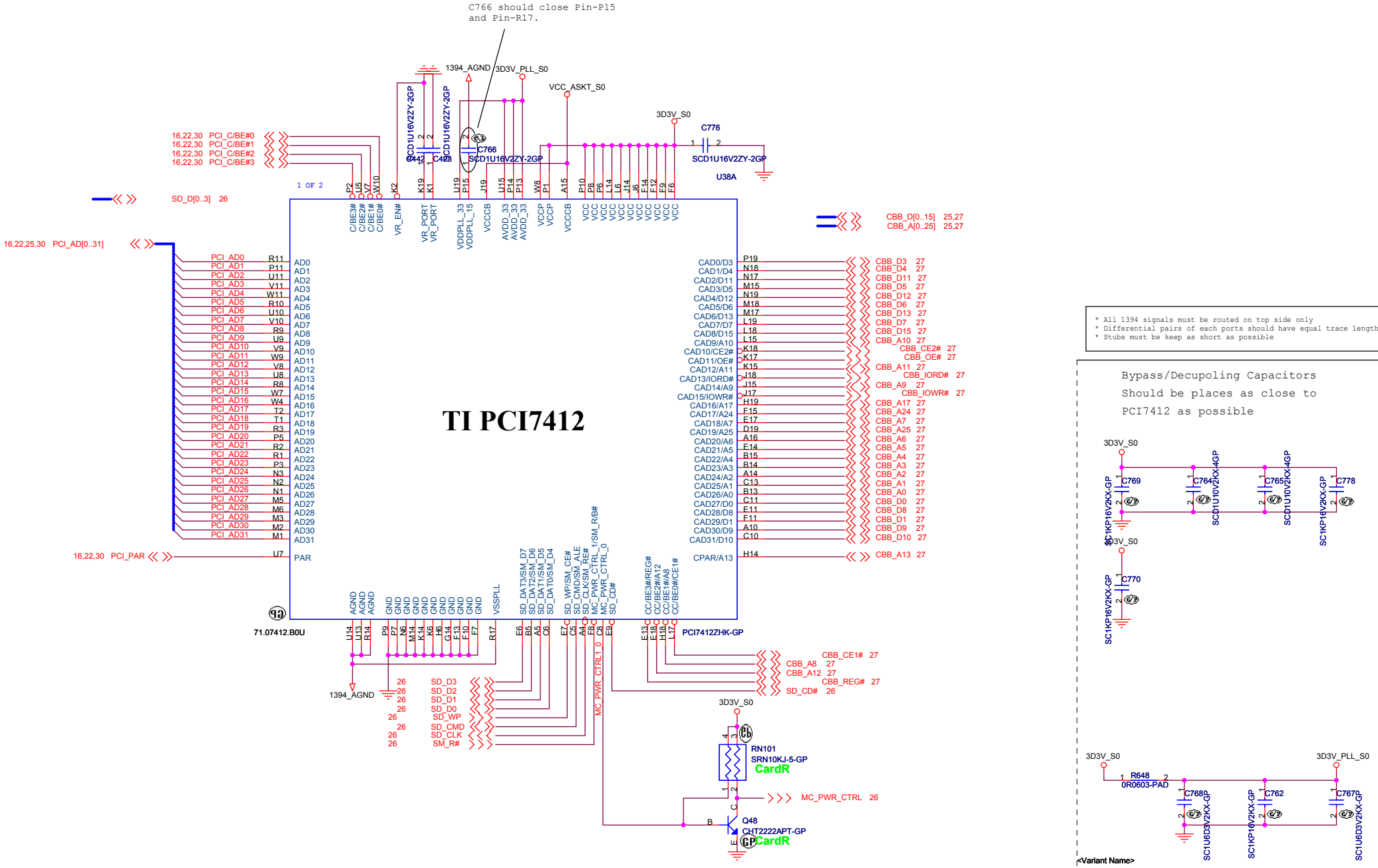
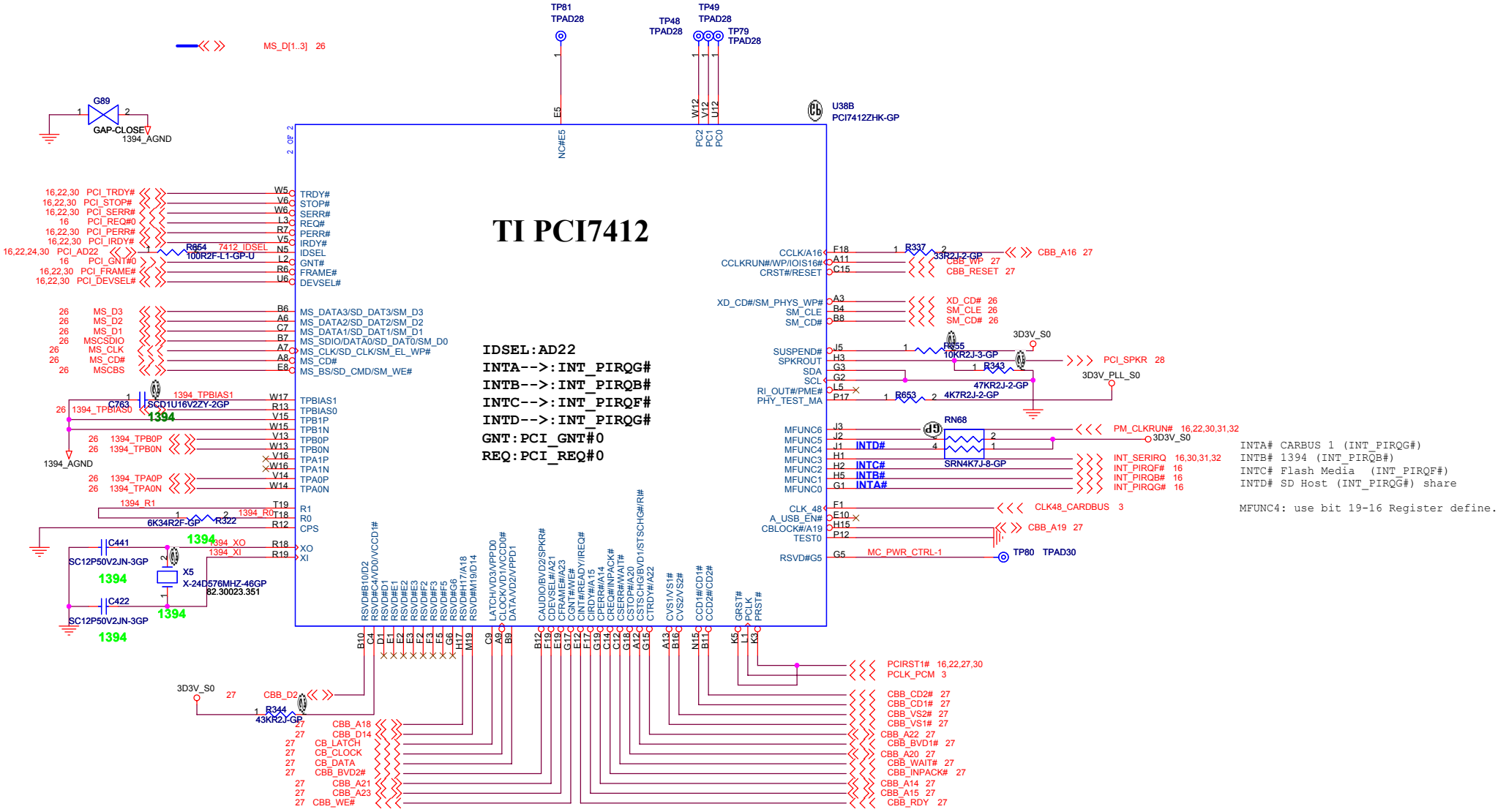
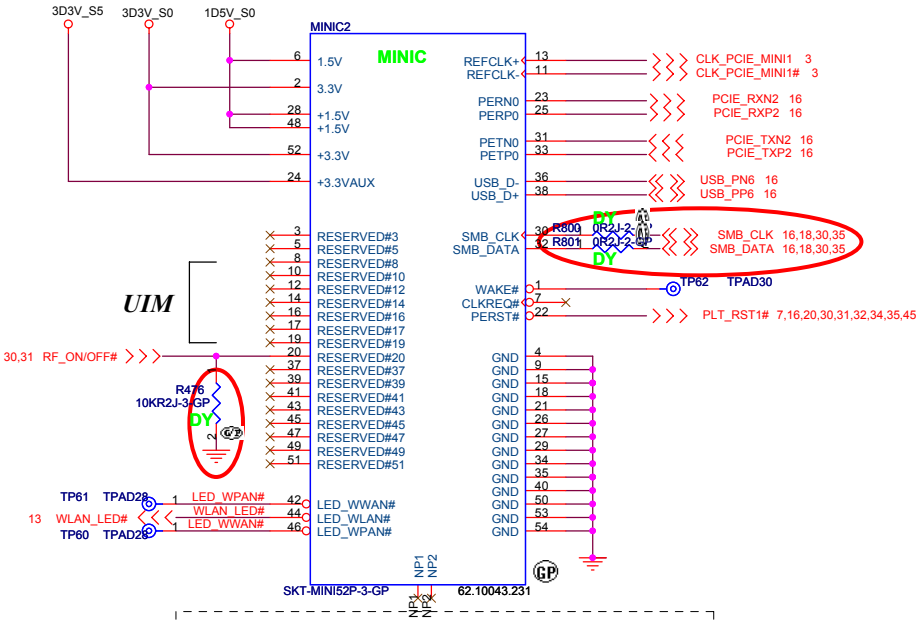

C766 should close Pin-P15
and Pin-R17.
TI PCI7412
1 OF 2
U38A
71.07412.B0U
PCI7412ZHK-GP
SD_D[0..3] 26
16,22,25,30 PCI_AD[0..31]
16,22,30 PCI_PAR
16,22,30 PCI_C/BE#0
16,22,30 PCI_C/BE#1
16,22,30 PCI_C/BE#2
16,22,30 PCI_C/BE#3
CBB_D[0..15] 25,27
CBB_A[0..25] 25,27
1394_AGND
3D3V_PLL_S0
VCC_ASKT_S0
3D3V_S0
C776
SCD1U16V2ZY-2GP
C766
C442
C428
RN101
SRN10KJ-5-GP
CardR
Q48
CHT2222APT-GP
MC_PWR_CTRL 26
* All 1394 signals must be routed on top side only
* Differential pairs of each ports should have equal trace length
* Stubs must be keep as short as possible
Bypass/Decupoling Capacitors
Should be places as close to
PCI7412 as possible
C769
C764
C765
C778
C770
C768
C762
C767
SC1KP16V2KX-GP
SC1KP16V2KX-4GP
SCD1U10V2KX-4GP
SC1U6D3V2KX-GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI PCI7412 (1 of 2)
Size A3
Document Number AG1
Rev SB
Date: Tuesday, January 10, 2006
Sheet 24 of 53

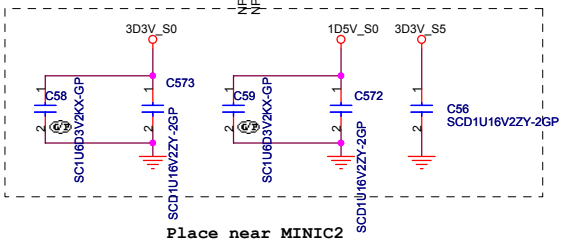


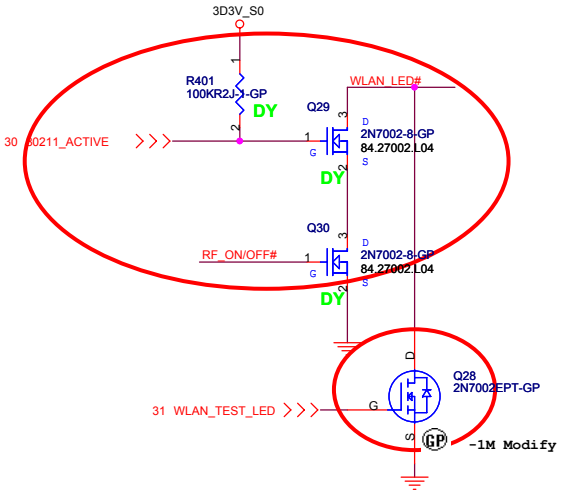
<variant_name>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	TI PCI7412 (2 of 2)	
Size A3	Document Number AG1	Rev SA
Date: Tuesday, January 10, 2006	Sheet 25 of 53	

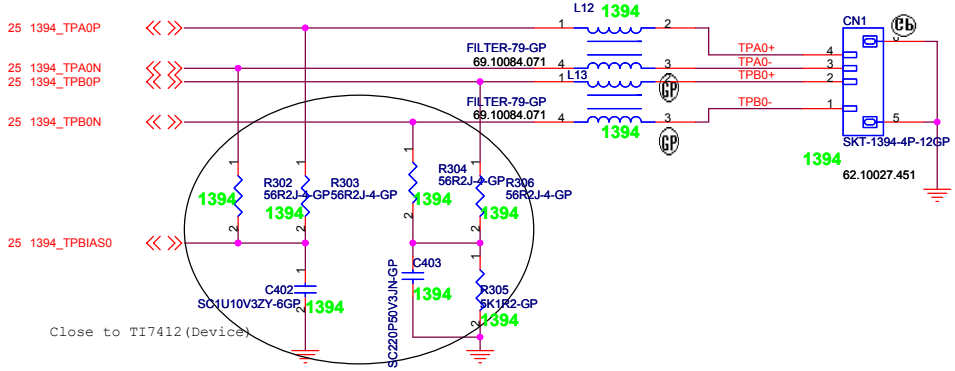
Mini Card Connector

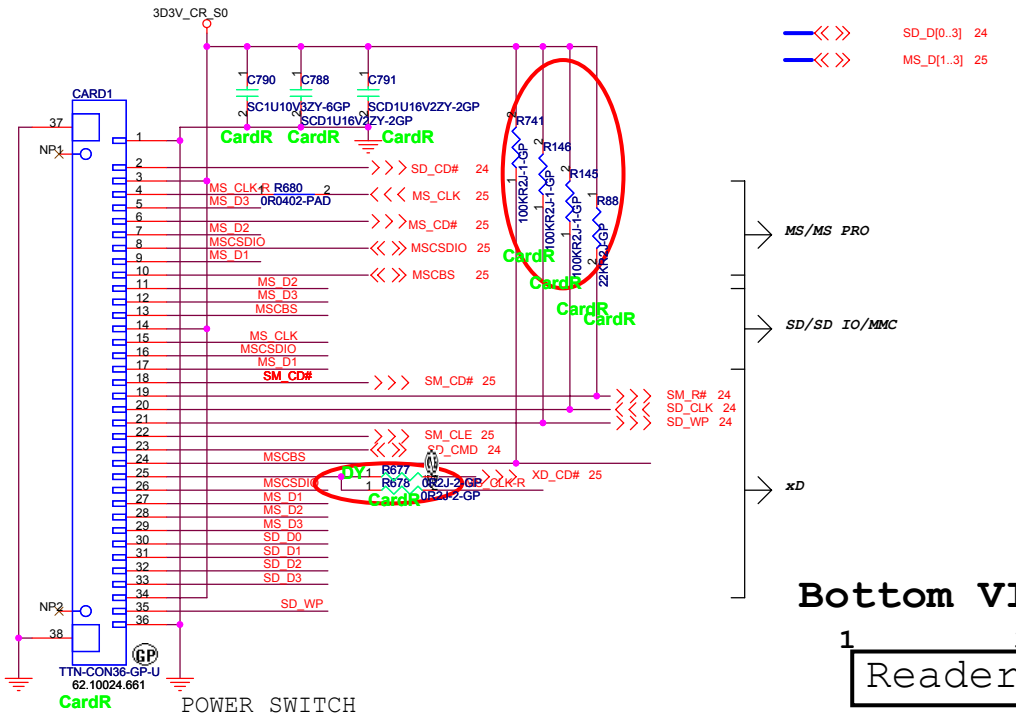






1394 Connector





Bottom VIEW

1 36

Reader

<Variant Name>

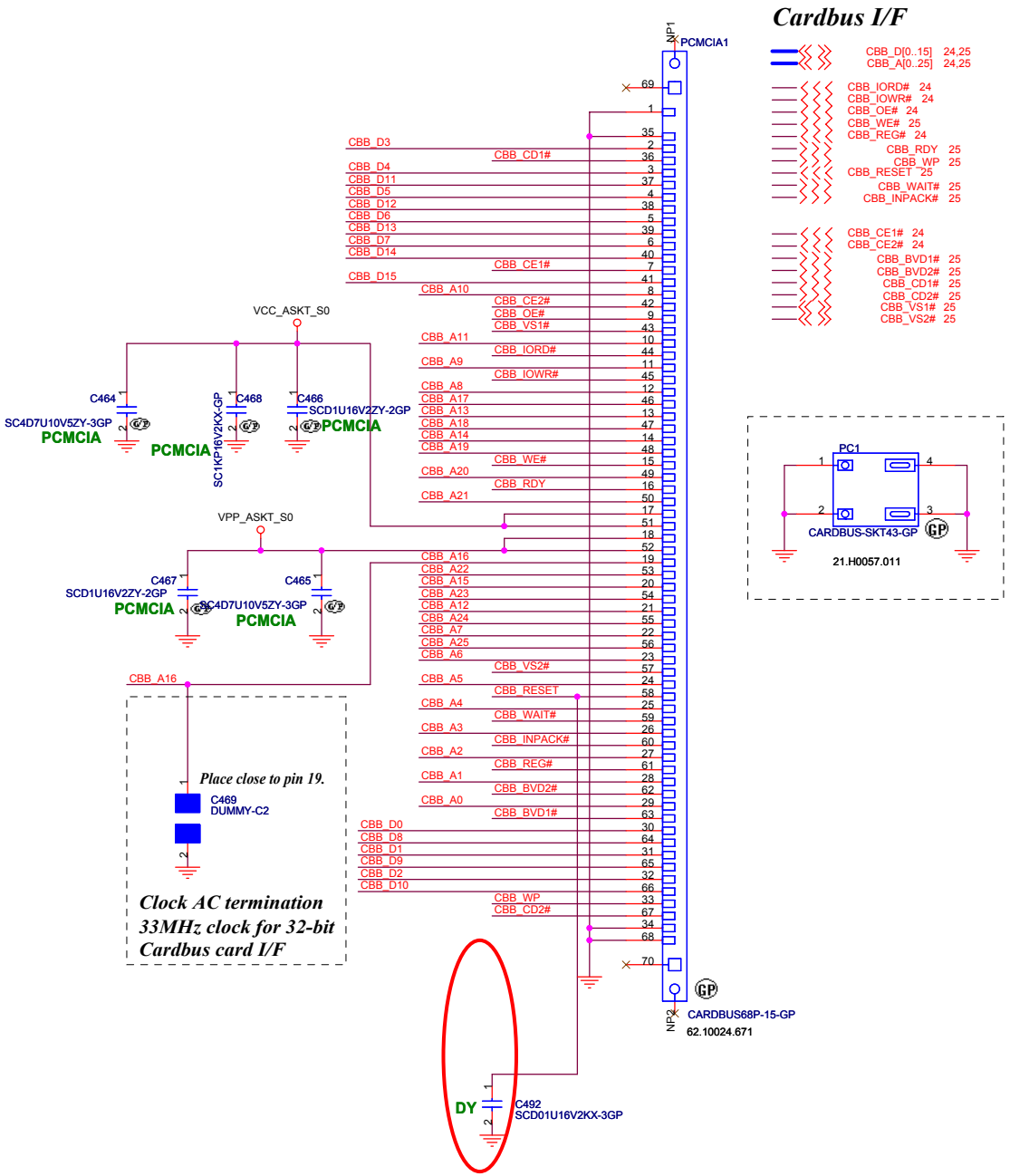
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI CARD / 1394

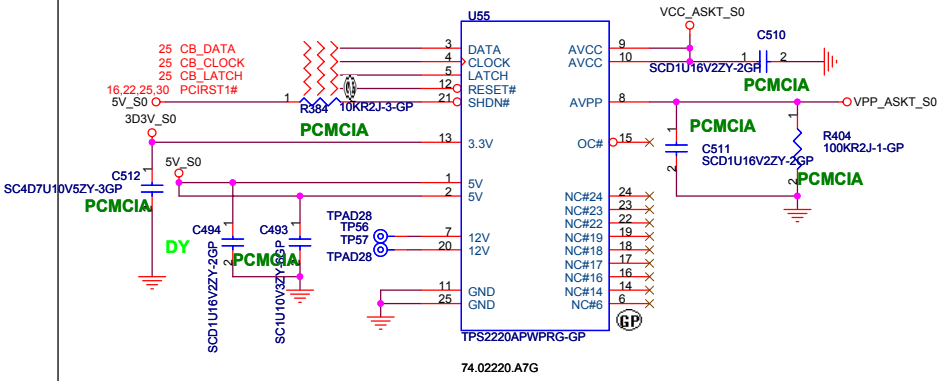
Size	Document Number	Rev
A3	AG1	-1M

Date: Tuesday, January 10, 2006 Sheet 26 of 53

PCMCIA Socket



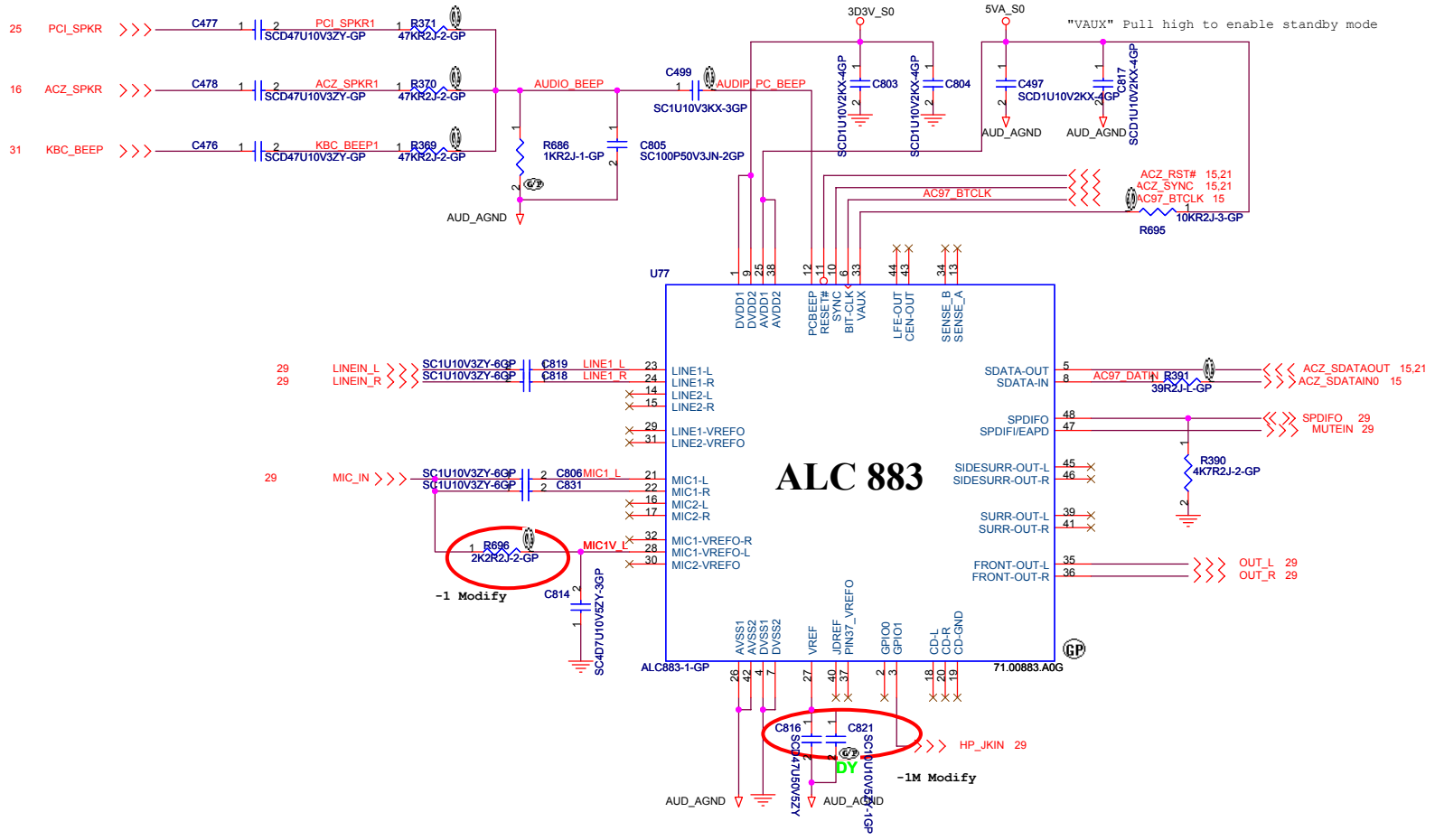
Power switch



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

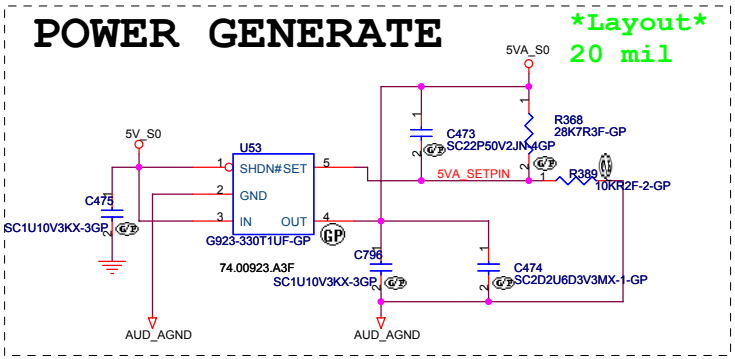
Title	PCMCIA	
Size A3	Document Number AG1	Rev SC
Date: Tuesday, January 10, 2006	Sheet 27 of 53	



1) When GPIO0 is assered, AMP should be muted.
2) SPDIFO should be turned off when not used.

Configuation:
(3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP,Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



<Variant Name>

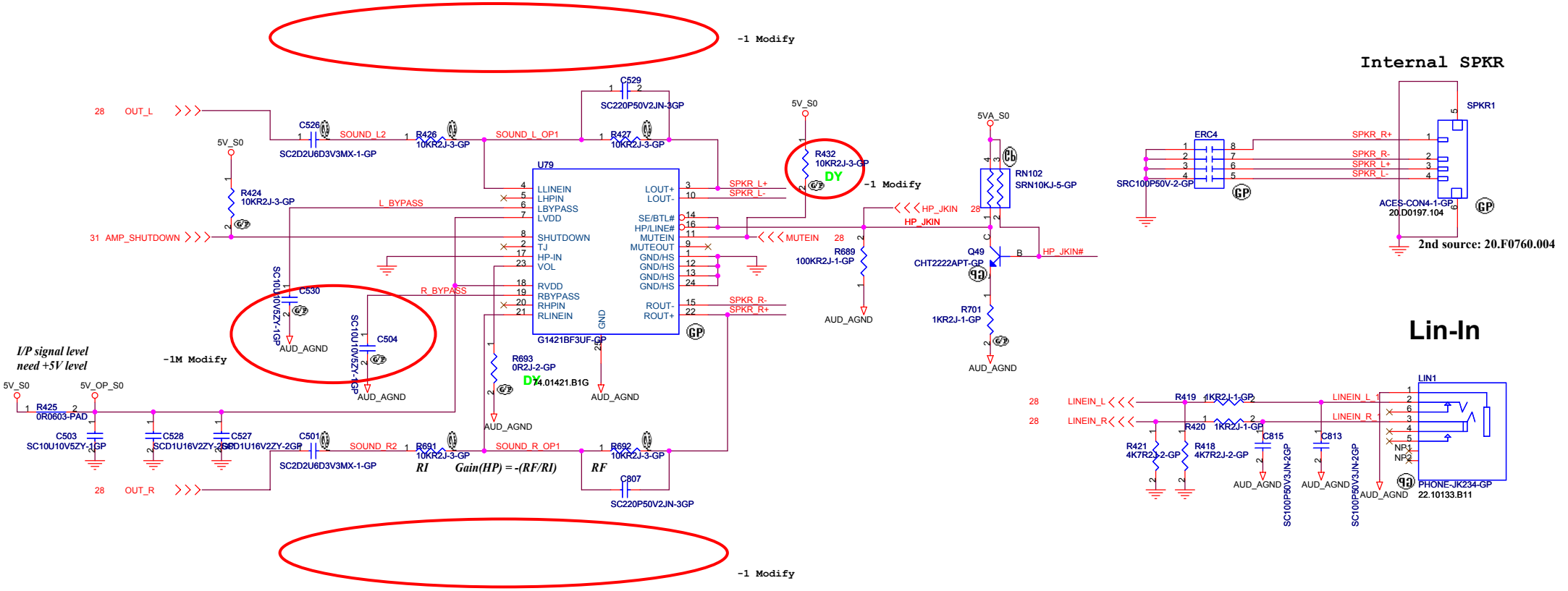
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

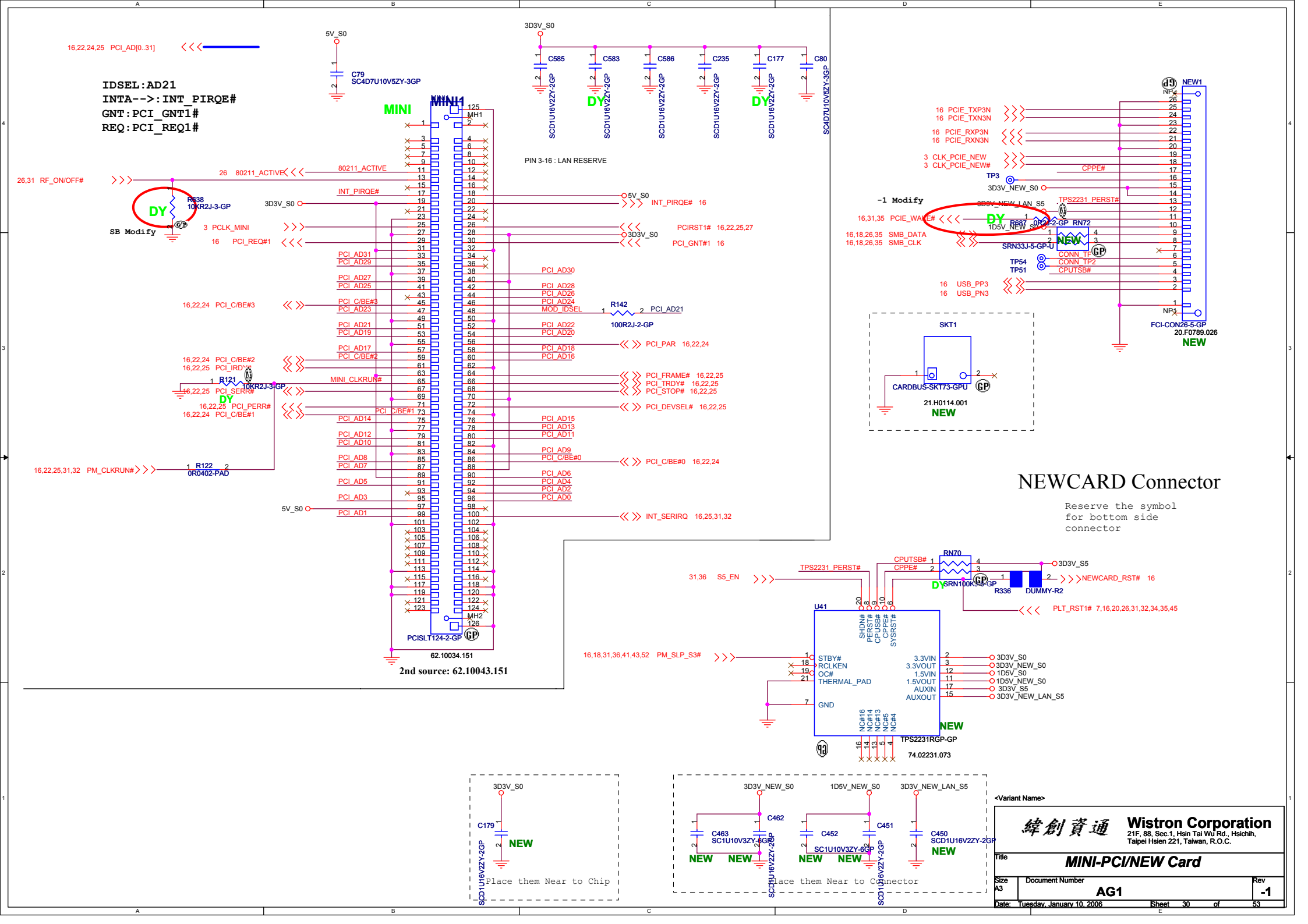
Title: **Azalia codec ALC883**

Size	Document Number	Rev
A3	AG1	-1M

Date: Tuesday, January 10, 2006 Sheet 28 of 53

AUDIO OP AMPLIFIER




IDSEL:AD21
INTA-->:INT_PIRQE#
GNT:PCI_GNT1#
REQ:PCI_REQ1#
MINI
MINI1
PCISLT124-2-GP
62.10034.151
2nd source: 62.10043.151
PIN 3-16 : LAN RESERVE
SB Modify
DY
NEW
-1 Modify
SKT1
CARDBUS-SKT73-GPU
21.H0114.001
FCI-CON26-5-GP
20.F0789.026
NEWCARD Connector
Reserve the symbol
for bottom side
connector
U41
TPS2231RGP-GP
74.02231.073
Place them Near to Chip
Place them Near to Connector
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
MINI-PCI/NEW Card
AG1
-1
Tuesday, January 10, 2006
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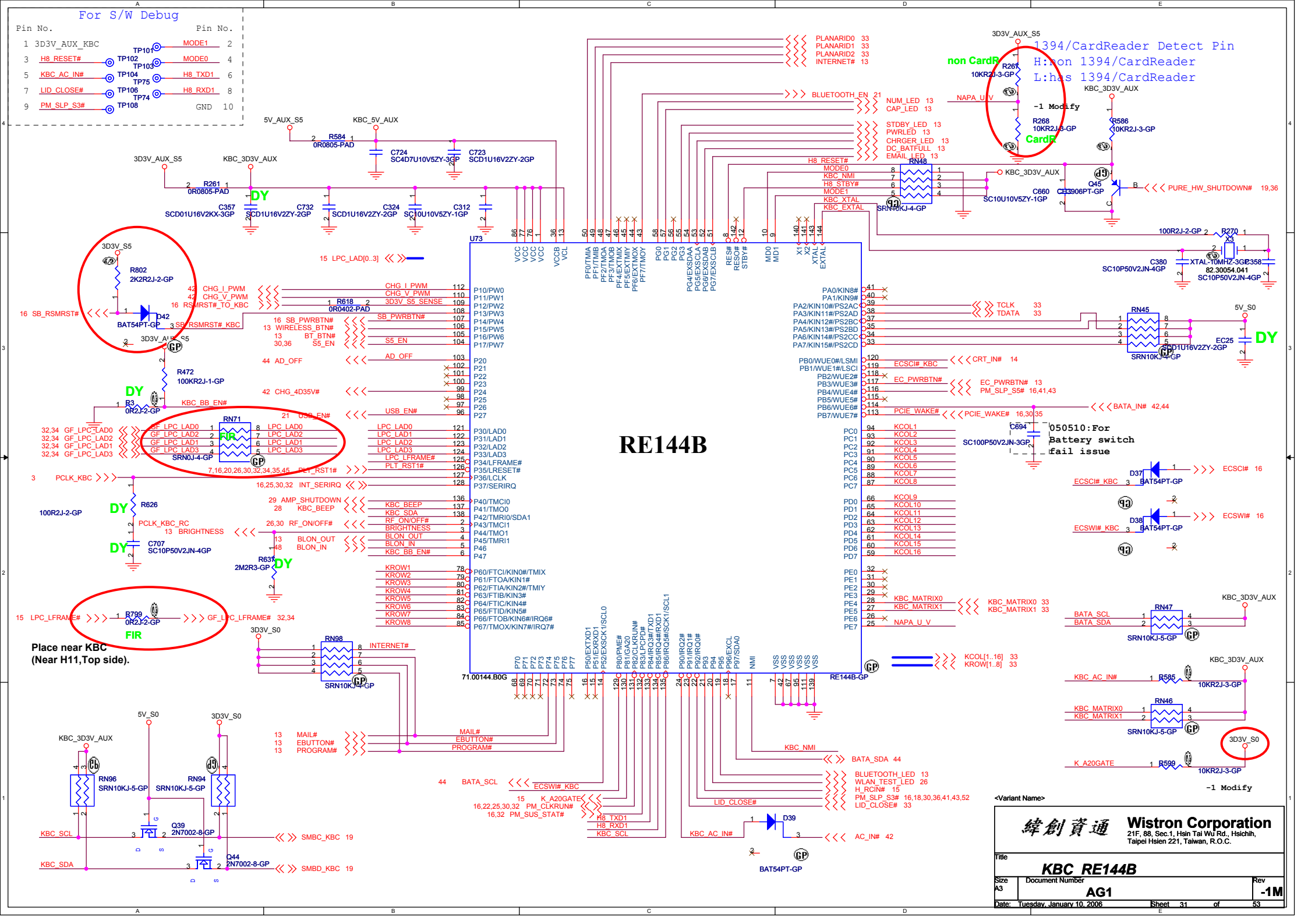
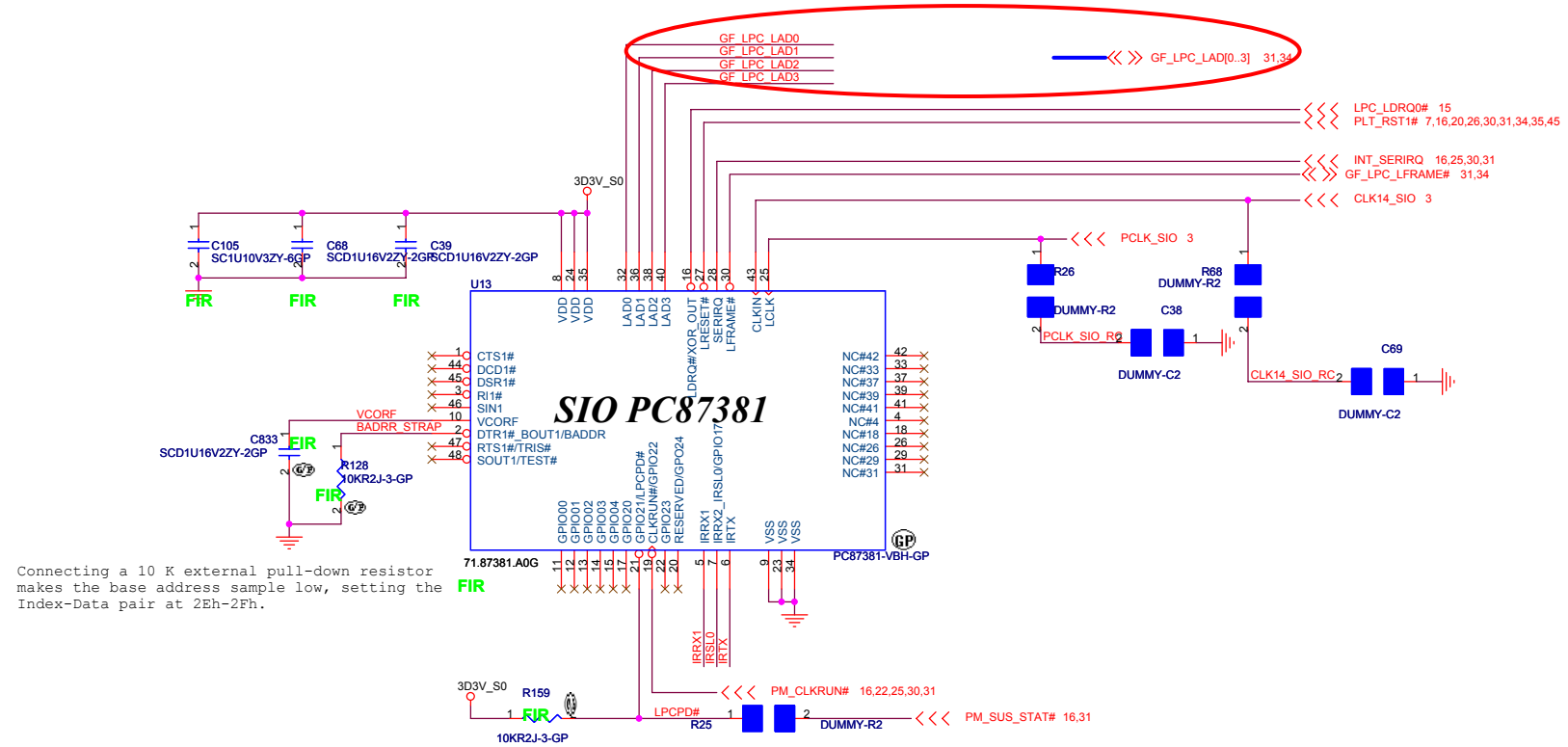
53

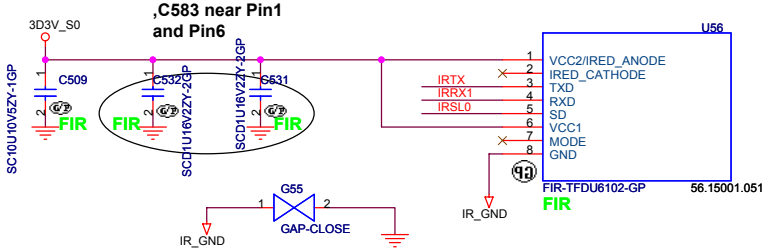

For S/W Debug
Pin No.
Pin No.
1 3D3V_AUX_KBC
TP101
MODE1 2
3 H8_RESET#
TP102
TP103
MODE0 4
5 KBC_AC_IN#
TP104
TP75
H8_TXD1 6
7 LID_CLOSE#
TP106
TP74
H8_RXD1 8
9 PM_SLP_S3#
TP108
GND 10
RE144B
U73
71.00144.B0G
RE144B-GP
1394/CardReader Detect Pin
H:non 1394/CardReader
L:has 1394/CardReader
non CardR
CardR
-1 Modify
050510:For
Battery switch
fail issue
Place near KBC
(Near H11,Top side).
FIR
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_RE144B
AG1
-1M
Tuesday, January 10, 2006
31
53



VISHAY FIR/CIR Module

Layout Guide:
(1) FIR_3D3V : 30 mils,
(2) C583, C581 close to U32

Place C581 ,C583 near Pin1 and Pin6



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **SIO 87381 / FIR**

Size	Document Number	Rev
A3	AG1	-1

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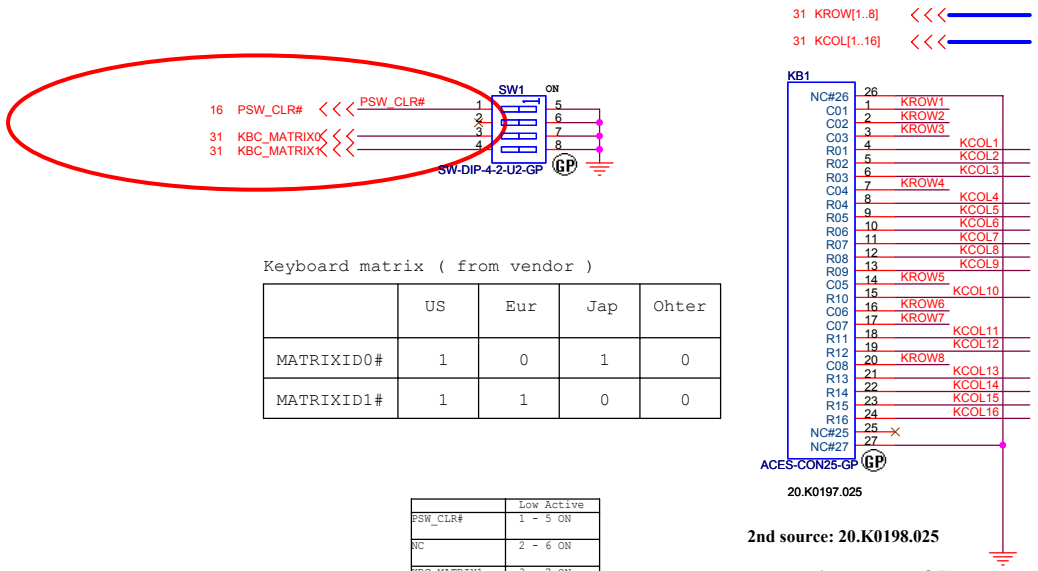
Internal KeyBoard Connector

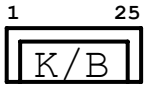


Keyboard matrix (from vendor)

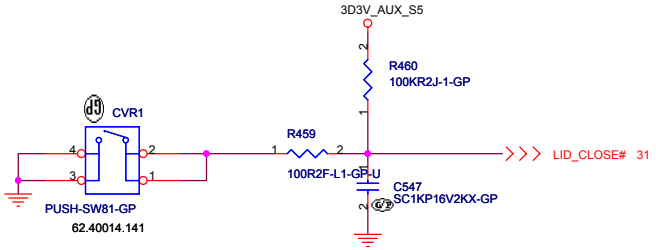
	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

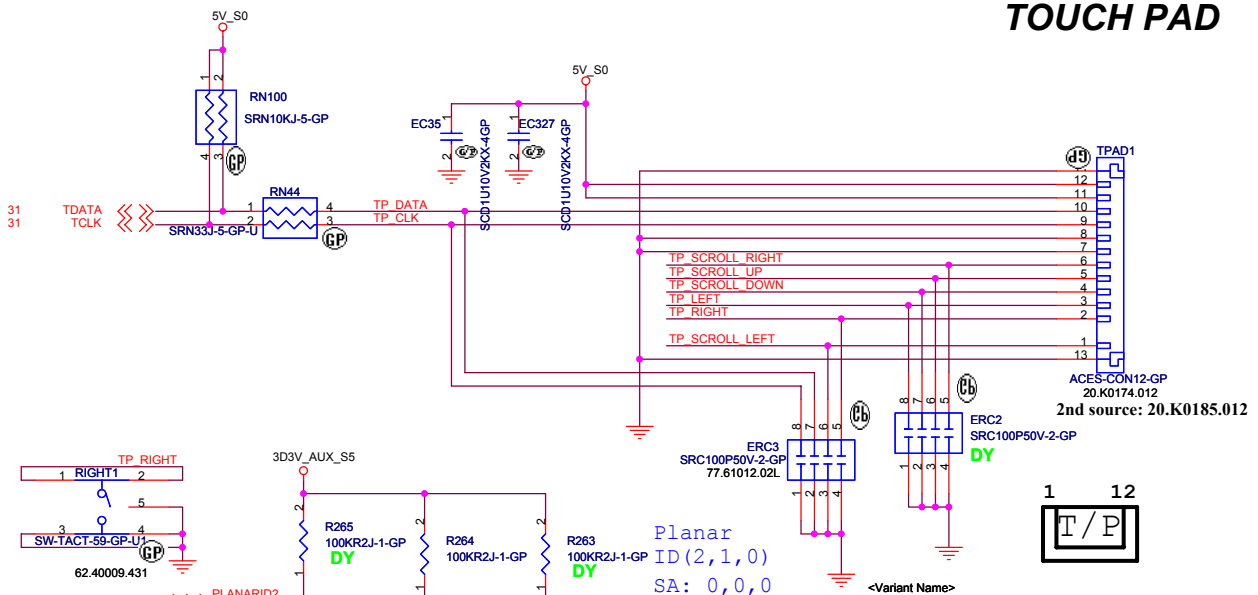
2nd source: 20.K0198.025



COVER SWITCH

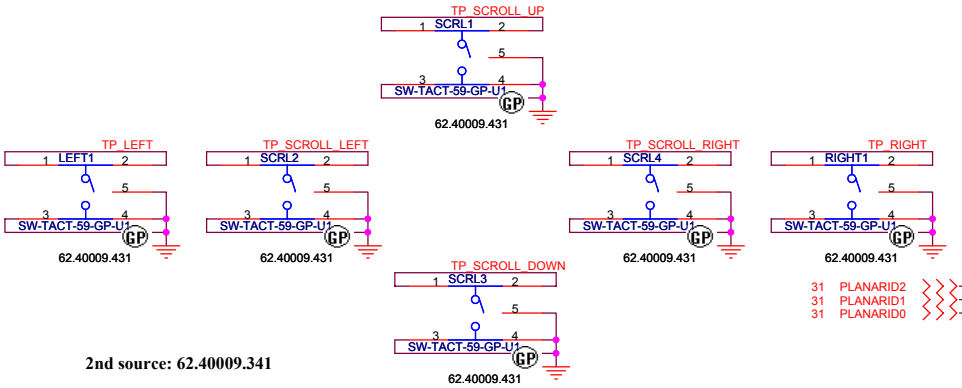


TOUCH PAD

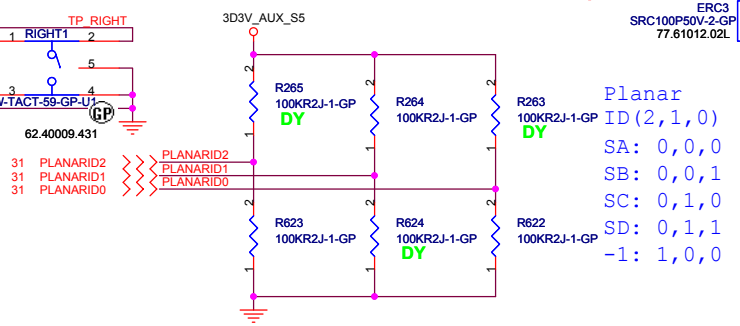


2nd source: 20.K0185.012

SCROLL KEY



2nd source: 62.40009.341



<Variant Name>

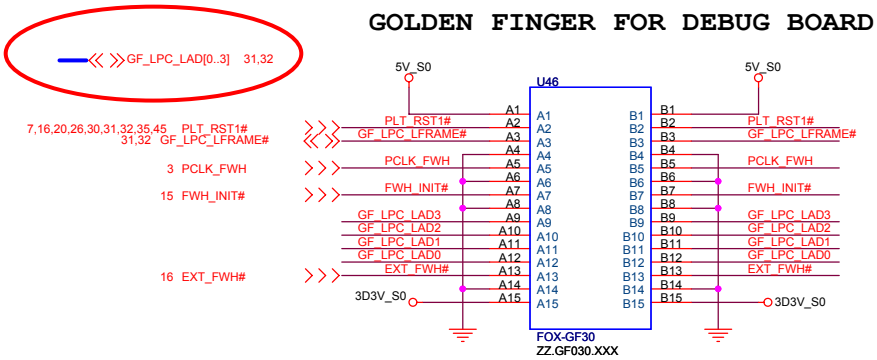
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TOUCHPAD

Size: A3 | Document Number: AG1 | Rev: SC

Date: Tuesday, January 10, 2006 | Sheet 33 of 53

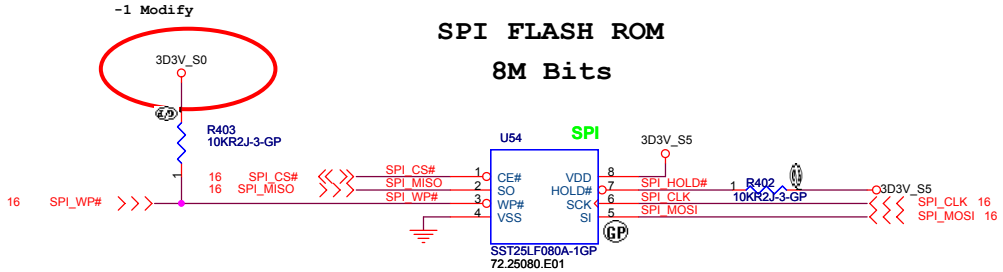
GOLDEN FINGER FOR DEBUG BOARD



Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SPI FLASH ROM

8M Bits



SOIC 200 Socket P/N:
Wieson: 62.10076.001
SPI ROM:
SST25LF080A: 72.25080.E01
SST25VF080B : 72.25080.G01
ST M25P80: 72.25P80.001

TOP VIEW

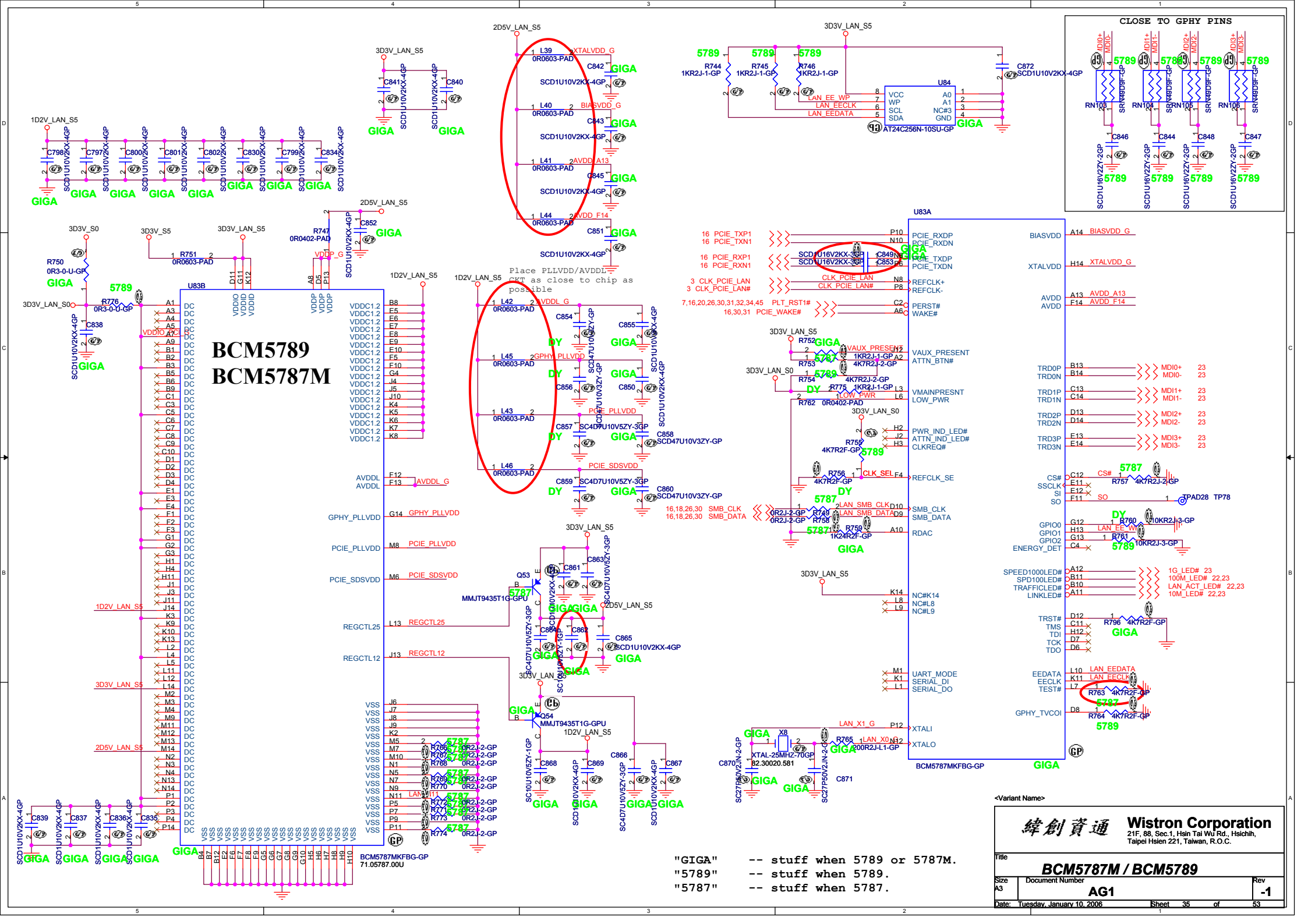
A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

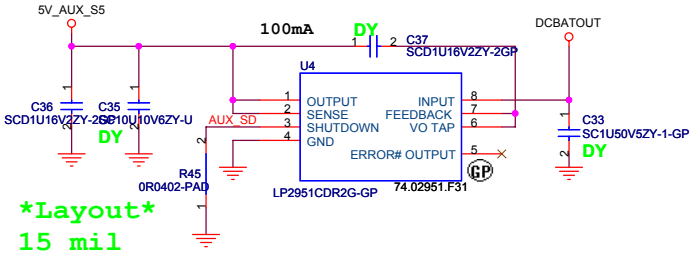
<Variant Name>

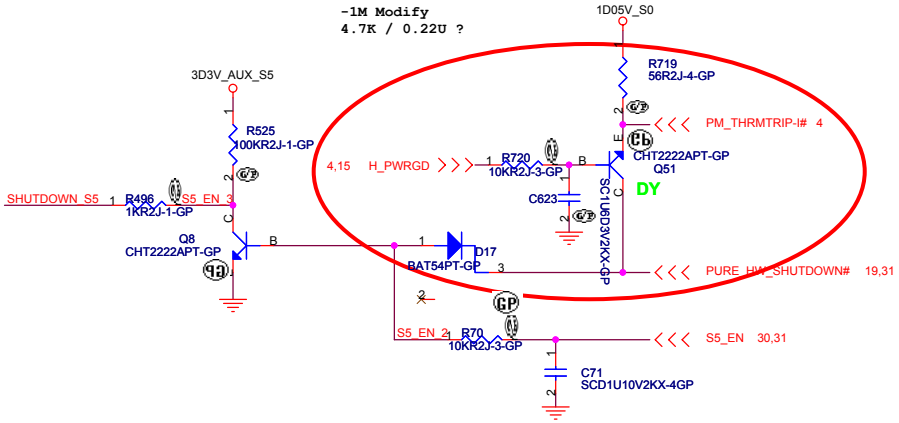
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

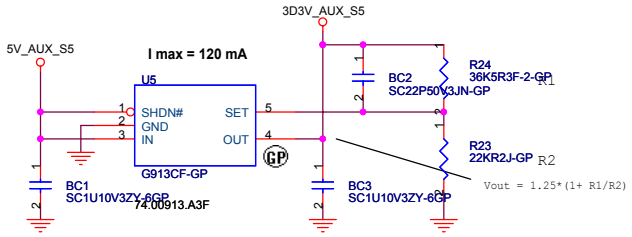
Title	***BIOS : SPI***	
Size A3	Document Number **AG1**	Rev **-1**
Date: Tuesday, January 10, 2006	Sheet 34 of 53	

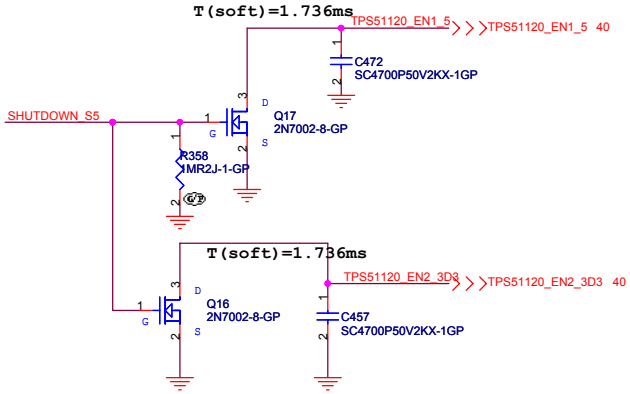

BCM5789
BCM5787M
CLOSE TO GPHY PINS
Place PLLVDD/AVDDL CKT as close to chip as possible
U83B
BCM5787MKFBG-GP
71.05787.00U
U83A
BCM5787MKFBG-GP
"GIGA" -- stuff when 5789 or 5787M.
"5789" -- stuff when 5789.
"5787" -- stuff when 5787.
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5787M / BCM5789
Size A3
Document Number AG1
Rev -1
Date: Tuesday, January 10, 2006
Sheet 35 of 53

Aux Power

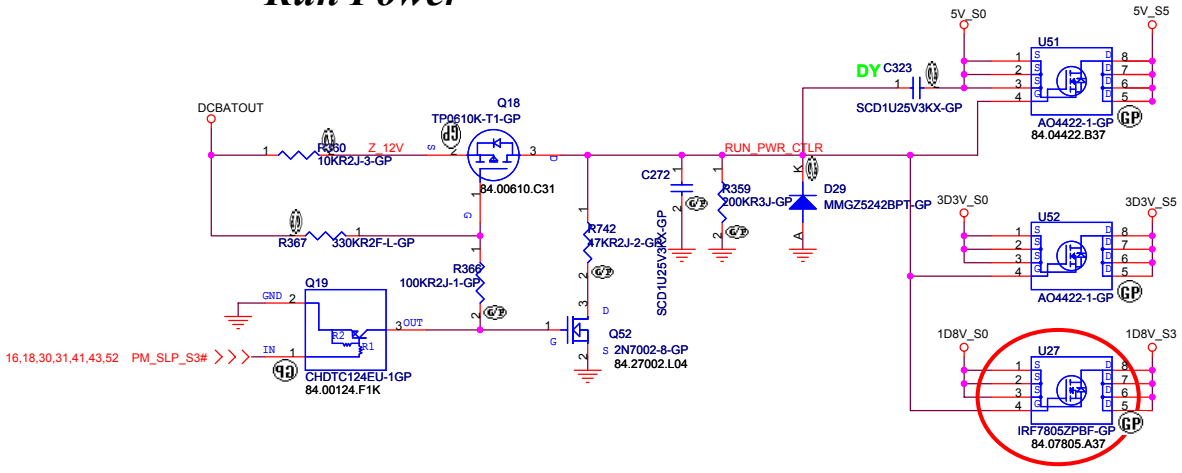








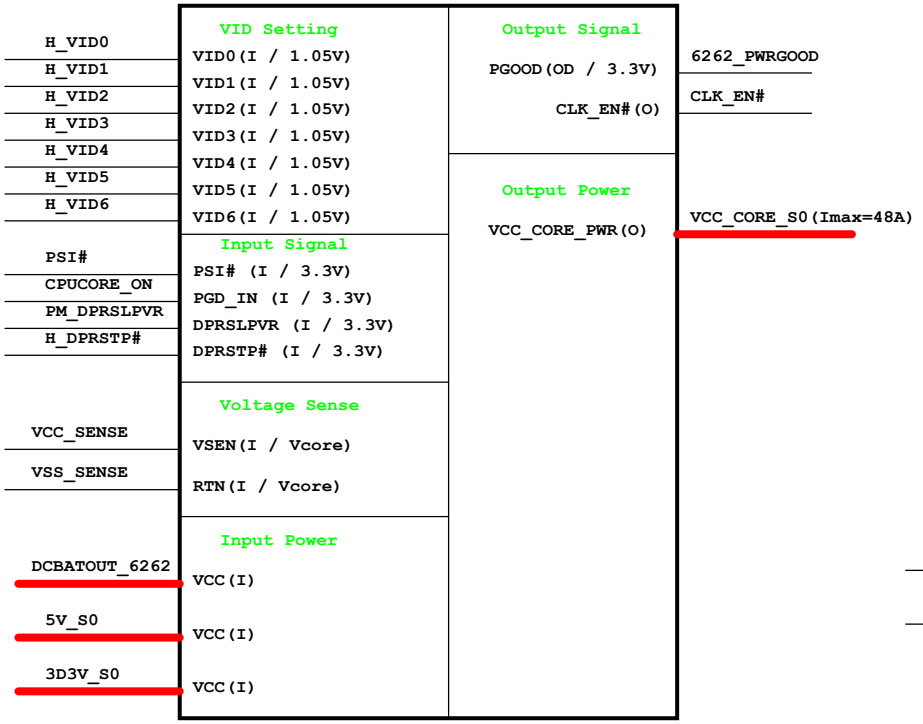
Run Power



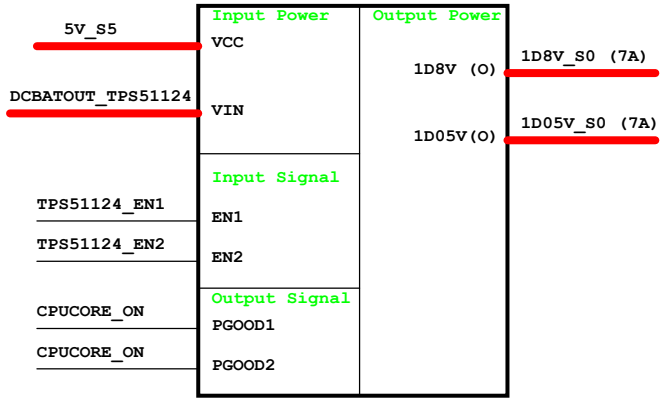
<Variant Name>

緯創資通 Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RUN and AUX POWER
Size A3 / Document Number	AG1 / Rev -1M
Date: Tuesday, January 10, 2006	Sheet 36 of 53

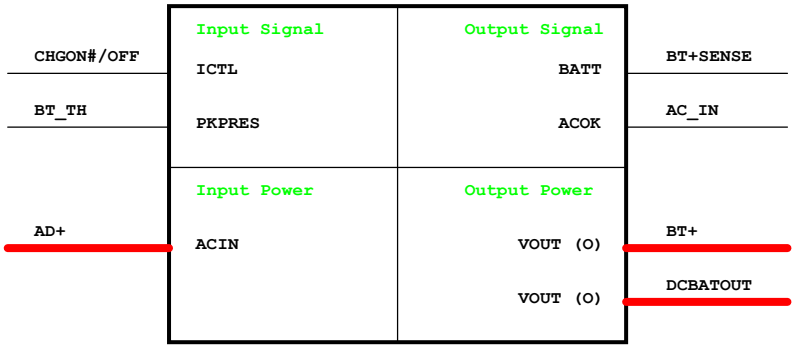
CPU_CORE
Intersil ISL6262



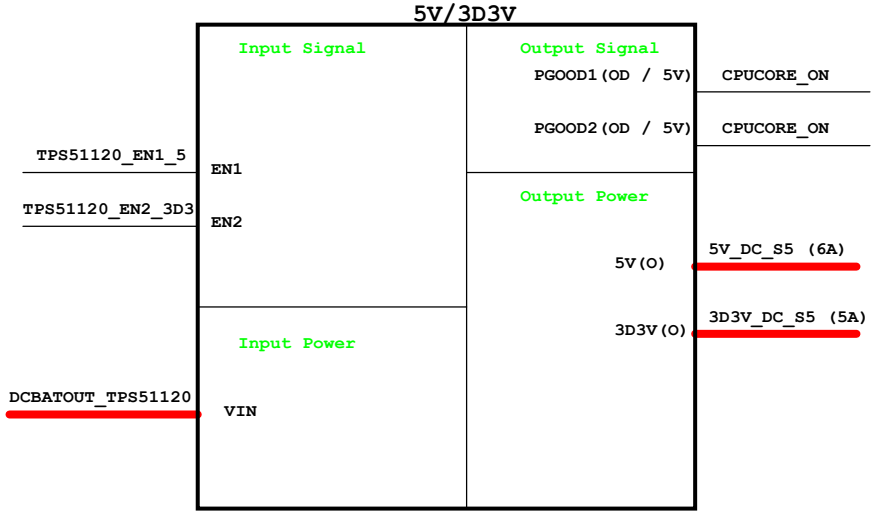
TPS51124
1D8V/1D05V



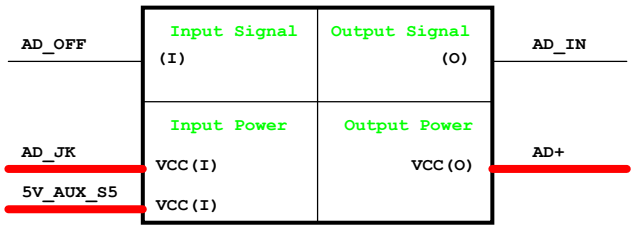
Charger Max8725



TPS51120
5V/3D3V



Adapter



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	AG1	SA

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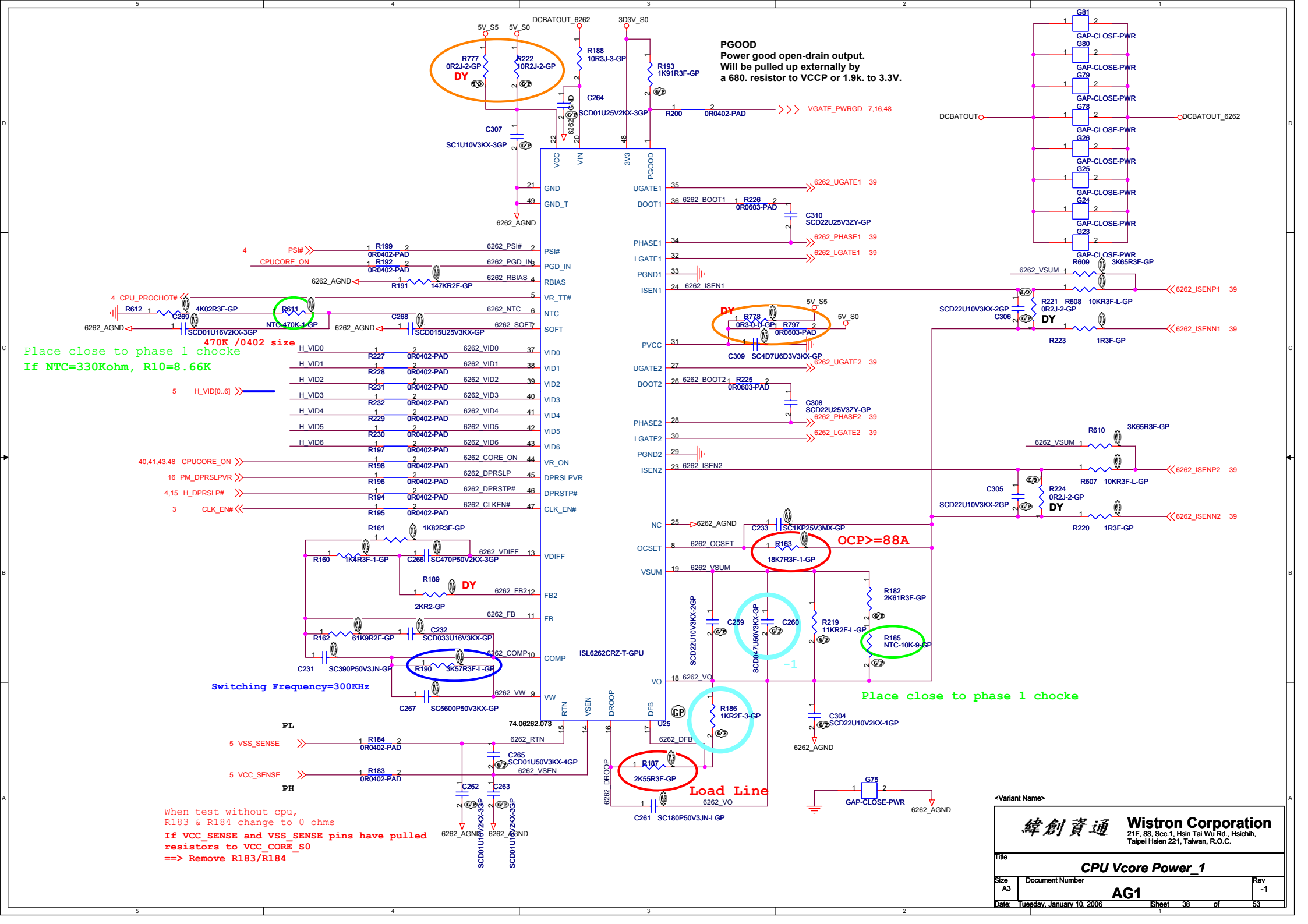
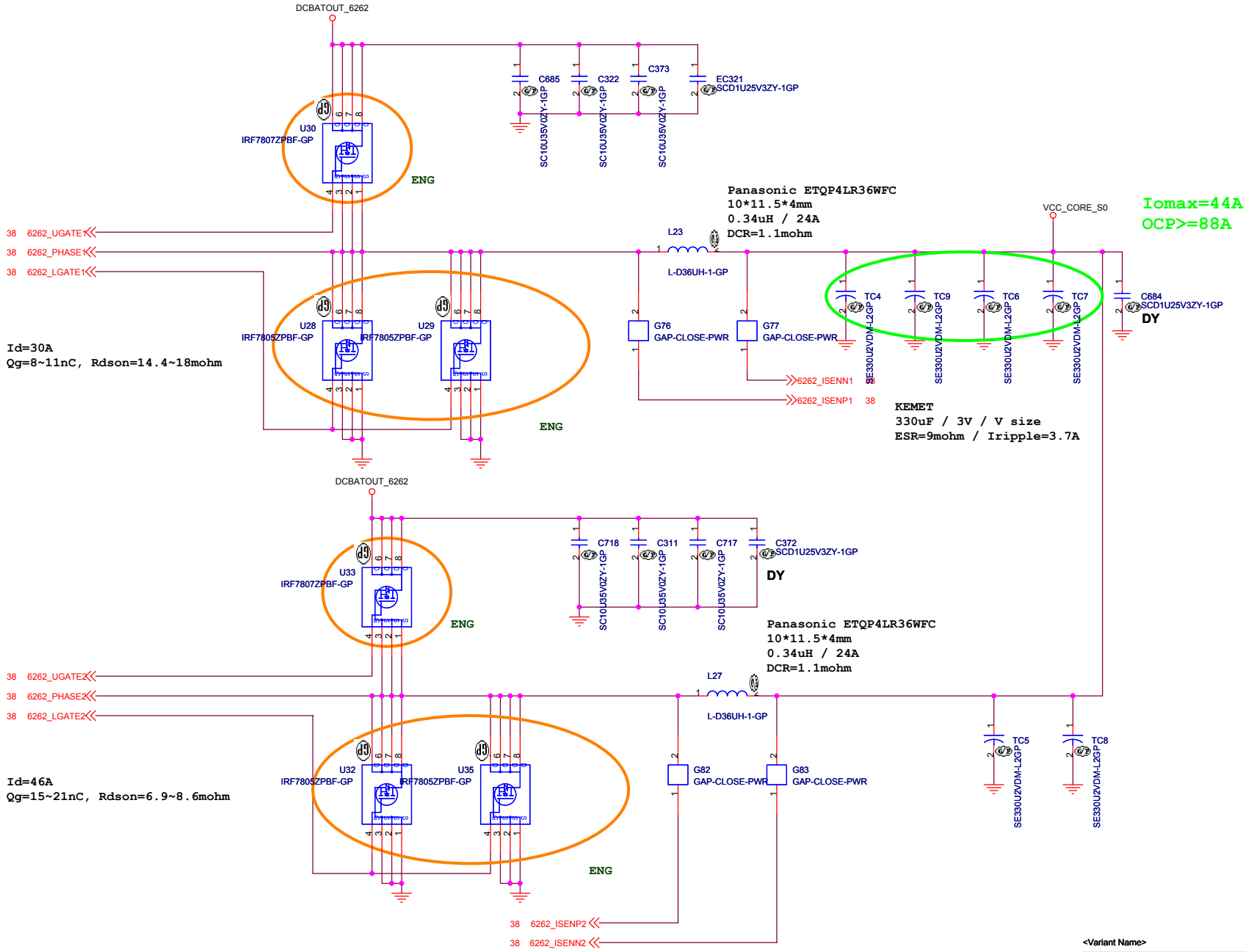

PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.
470K /0402 size
Place close to phase 1 chocke
If NTC=330Kohm, R10=8.66K
Switching Frequency=300KHz
OCP>=88A
Load Line
Place close to phase 1 chocke
When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184
ISL6262CRZ-T-GPU
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore Power_1
AG1
Tuesday, January 10, 2006



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_2

Size	Document Number	Rev
A3	AG1	SD

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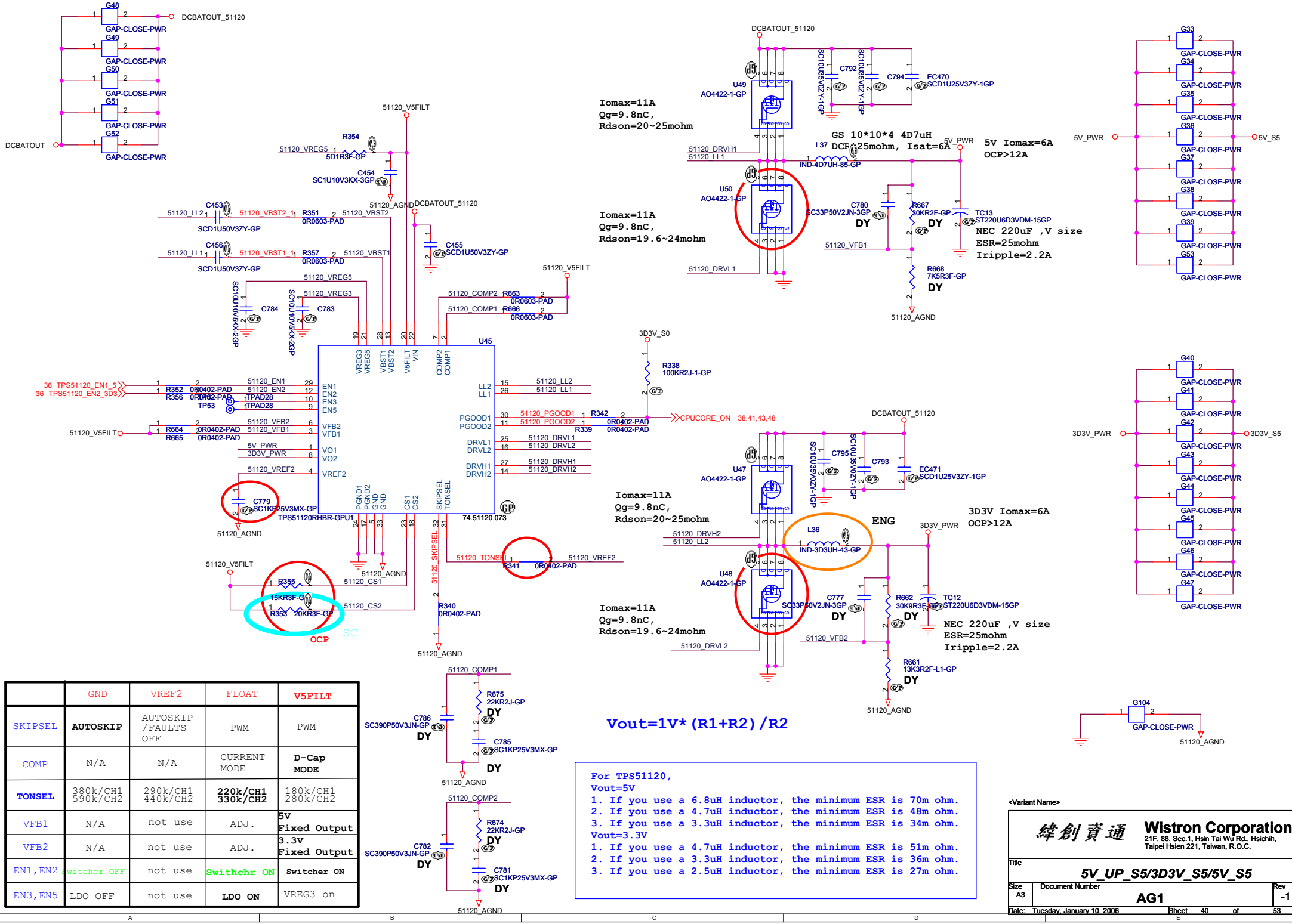

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **5V_UP_S5/3D3V_S5/5V_S5**

Size: A3 | Document Number: **AG1** | Rev: -1

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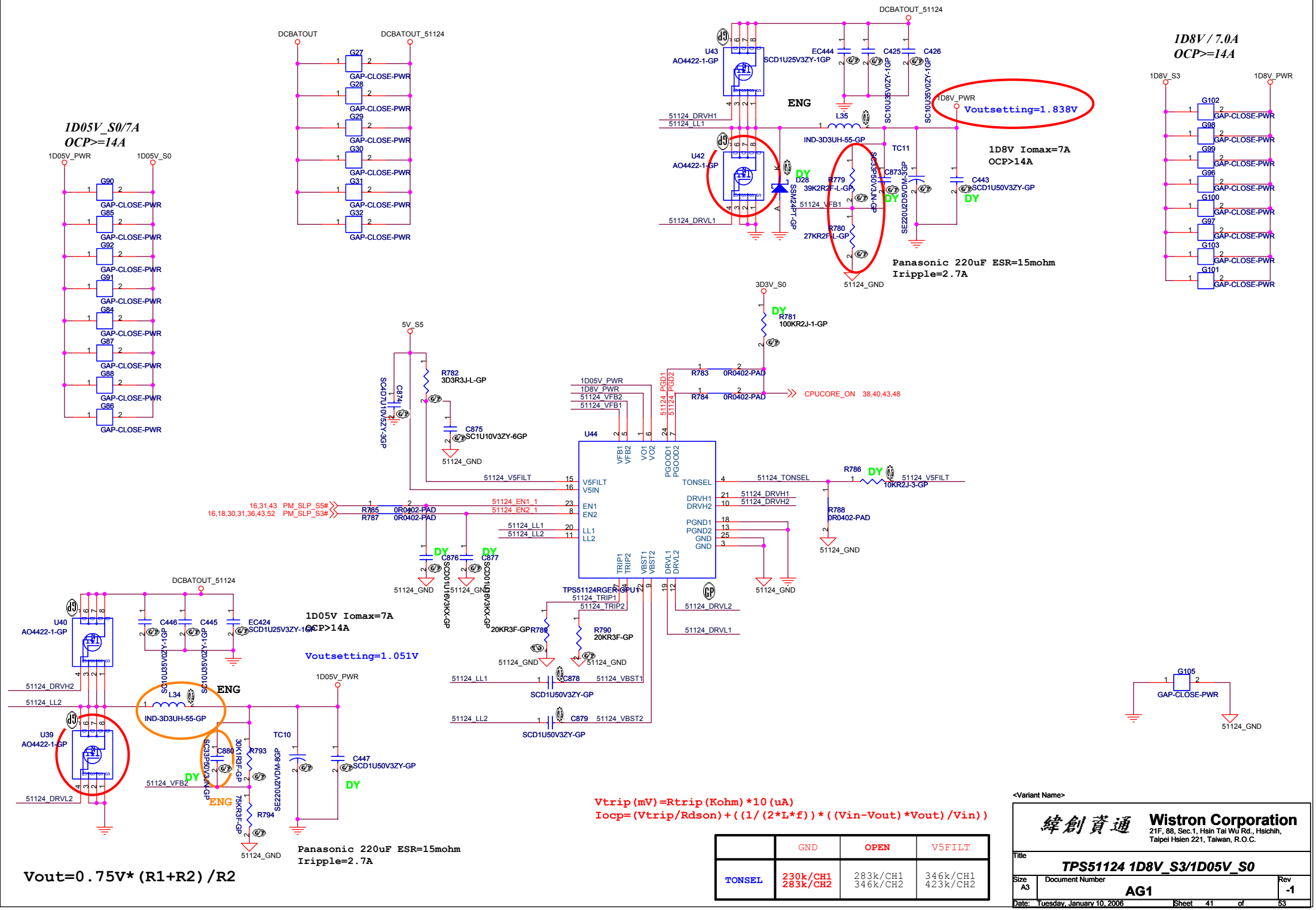
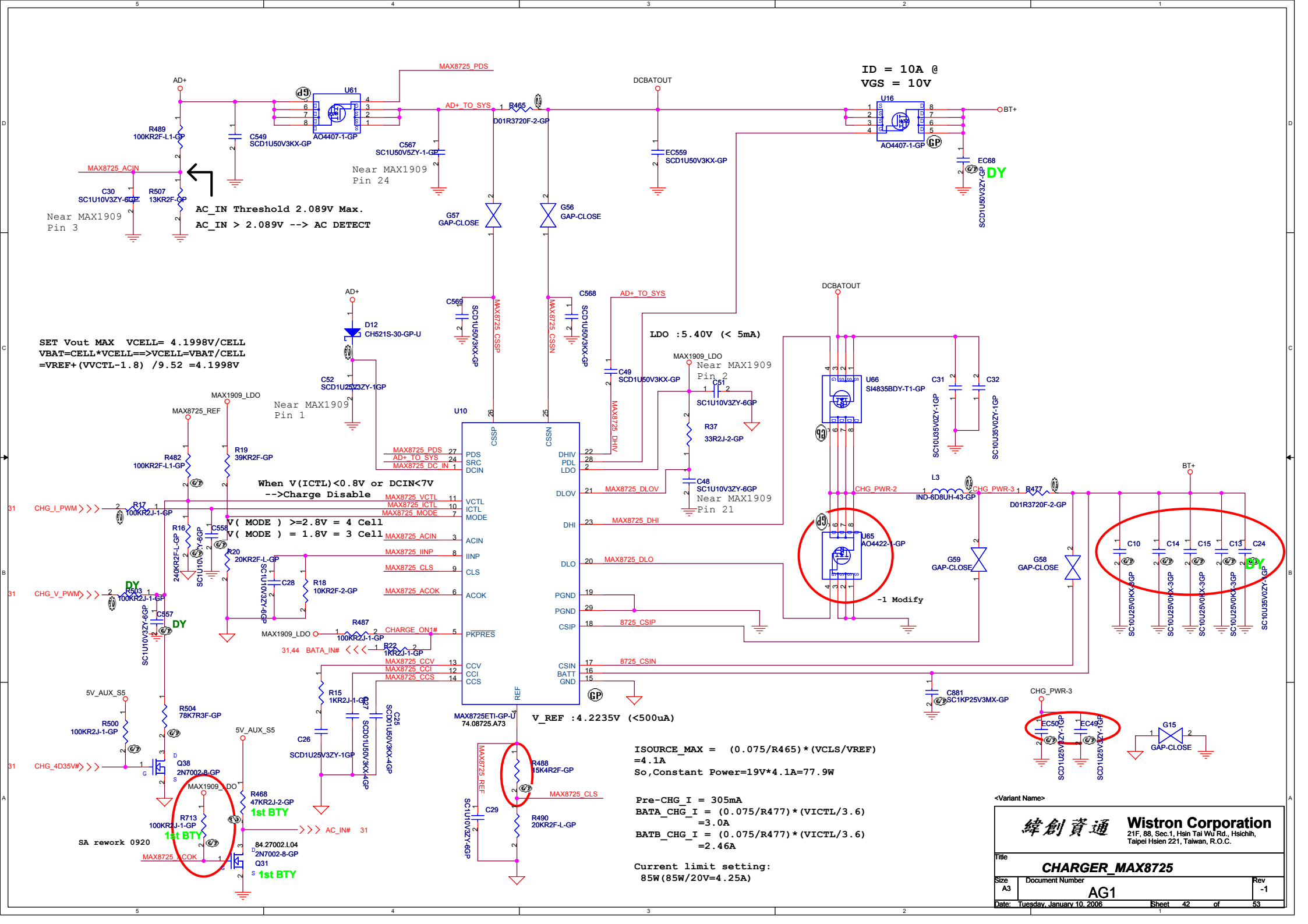
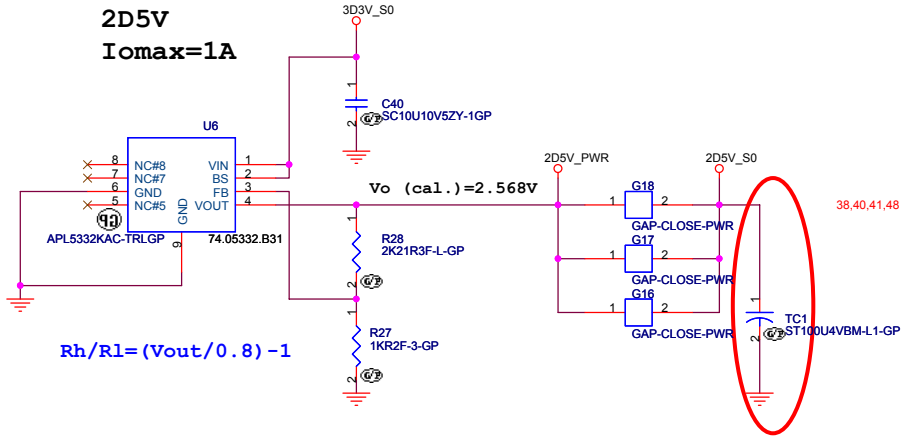
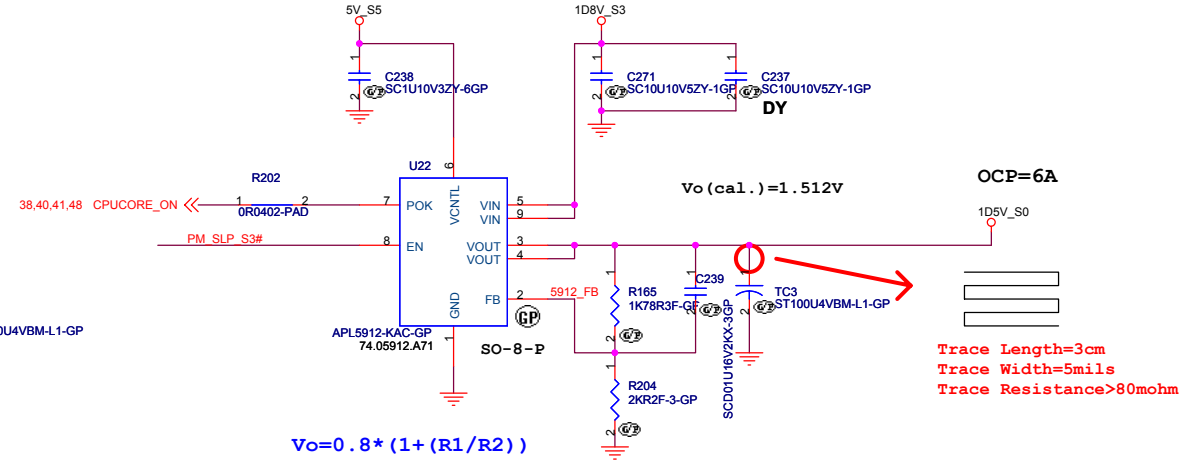

1D05V_S0/7A
OCP>=14A
1D05V_PWR
1D05V_S0
DCBATOUT
DCBATOUT_51124
GAP-CLOSE-PWR
1D8V / 7.0A
OCP>=14A
1D8V_S3
1D8V_PWR
U43
AO4422-1-GP
SCD1U25V3ZY-1GP
EC444
C425
C426
ENG
L35
IND-3D3UH-55-GP
Voutsetting=1.838V
1D8V Iomax=7A
OCP>14A
U42
AO4422-1-GP
D28
SSM24PT-GP
DY
R779
39K2R2F-L-GP
C873
R780
27KR2F-L-GP
C443
SCD1U50V3ZY-GP
Panasonic 220uF ESR=15mohm
Iripple=2.7A
51124_GND
3D3V_S0
R781
100KR2J-1-GP
5V_S5
R782
3D3R3J-L-GP
C874
C875
SC1U10V3ZY-6GP
U44
R783
R784
0R0402-PAD
CPUCORE_ON 38,40,43,48
1D05V_PWR
1D8V_PWR
51124_VFB2
51124_VFB1
51124_PGD1
51124_PGD2
VFB1
VFB2
VO1
VO2
PGOOD1
PGOOD2
V5FILT
V5IN
EN1
EN2
LL1
LL2
TONSEL
DRVH1
DRVH2
PGND1
PGND2
GND
TRIP1
TRIP2
VBST1
VBST2
DRVL1
DRVL2
R786
10KR2J-3-GP
R788
16,31,43 PM_SLP_S5#
16,18,30,31,36,43,52 PM_SLP_S3#
R785
R787
51124_EN1_1
51124_EN2_1
C876
C877
SCD1U16V3KX-GP
TPS51124RGER-GPU
51124_TRIP1
51124_TRIP2
20KR3F-GP
R789
R790
20KR3F-GP
C878
C879
SCD1U50V3ZY-GP
51124_VBST1
51124_VBST2
1D05V Iomax=7A
OCP>14A
Voutsetting=1.051V
U40
AO4422-1-GP
C446
C445
EC424
SCD1U25V3ZY-1GP
SC10U35V2ZY-1GP
L34
IND-3D3UH-55-GP
U39
AO4422-1-GP
TC10
C880
SC3300P50V2NN-GP
R793
30K1R3F-GP
R794
75KR3F-GP
C447
SE220U2VDM-8GP
Panasonic 220uF ESR=15mohm
Iripple=2.7A
Vout=0.75V*(R1+R2)/R2
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
TONSEL
GND
OPEN
V5FILT
230k/CH1
283k/CH2
283k/CH1
346k/CH2
346k/CH1
423k/CH2
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51124 1D8V_S3/1D05V_S0
Size A3
Document Number
AG1
Rev -1
Date: Tuesday, January 10, 2006
Sheet 41 of 53


ID = 10A @
VGS = 10V
AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
Near MAX1909 Pin 3
Near MAX1909 Pin 24
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
LDO :5.40V (< 5mA)
Near MAX1909 Pin 1
Near MAX1909 Pin 2
Near MAX1909 Pin 21
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
V_REF :4.2235V (<500uA)
-1 Modify
ISOURCE_MAX = (0.075/R465)*(VCLS/VREF)
=4.1A
So,Constant Power=19V*4.1A=77.9W
Pre-CHG_I = 305mA
BATA_CHG_I = (0.075/R477)*(VICTL/3.6)
=3.0A
BATB_CHG_I = (0.075/R477)*(VICTL/3.6)
=2.46A
Current limit setting:
85W(85W/20V=4.25A)
SA rework 0920
1st BTY
DY
5Y
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER_MAX8725
AG1
Tuesday, January 10, 2006

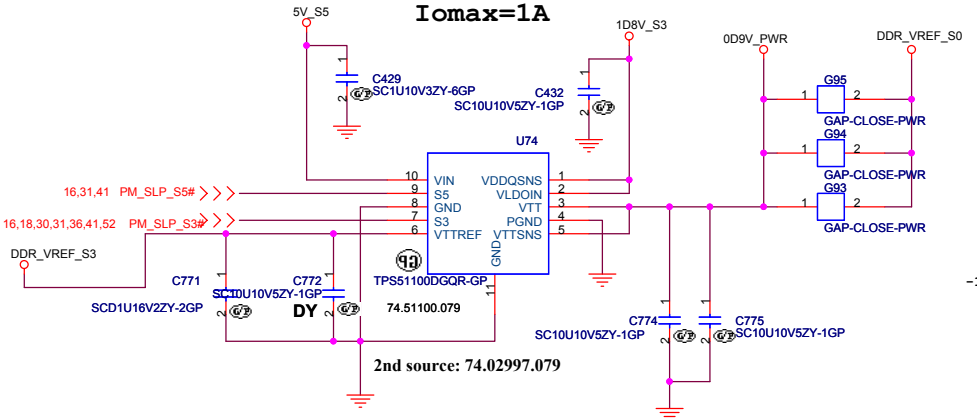
2D5V
Iomax=1A



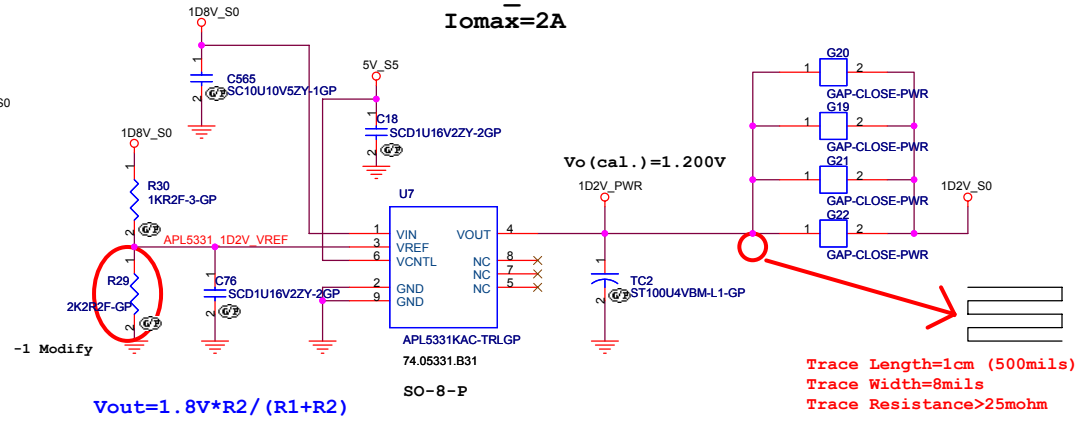
1D5V_S0
Iomax=4.0A



0D9V
Iomax=1A



1D2V_S0
Iomax=2A



<Variant Name>

緯創資通 **Wistron Corporation**
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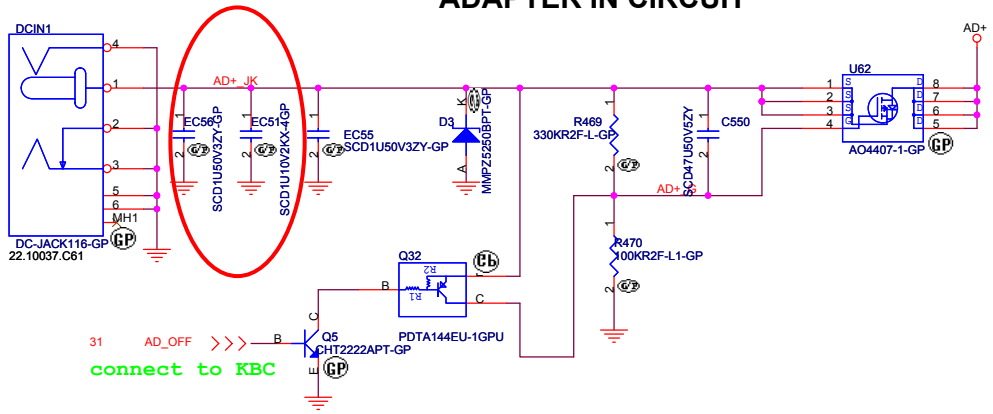
Taipei Hsien 221, Taiwan, R.O.C.

Title: *0D9V/1D2V/1D5V/2D5V*

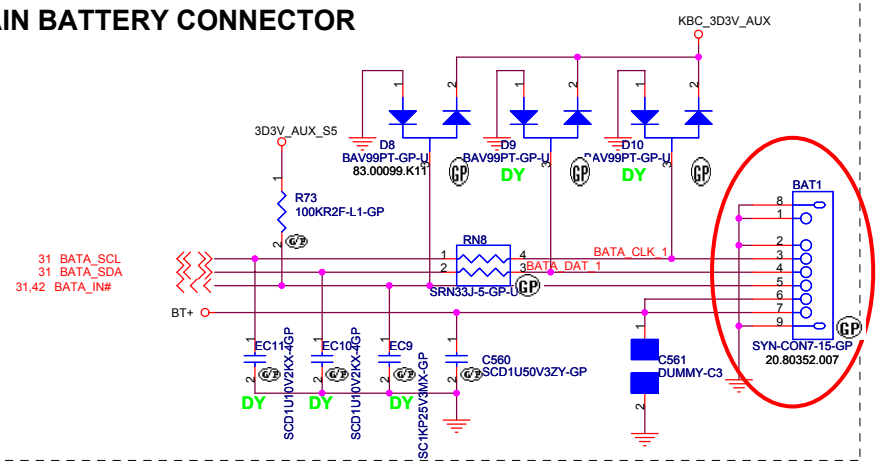
Size	Document Number	Rev
A3	AG1	-1

Date: Tuesday, January 10, 2006 Sheet 43 of 53

ADAPTER IN CIRCUIT

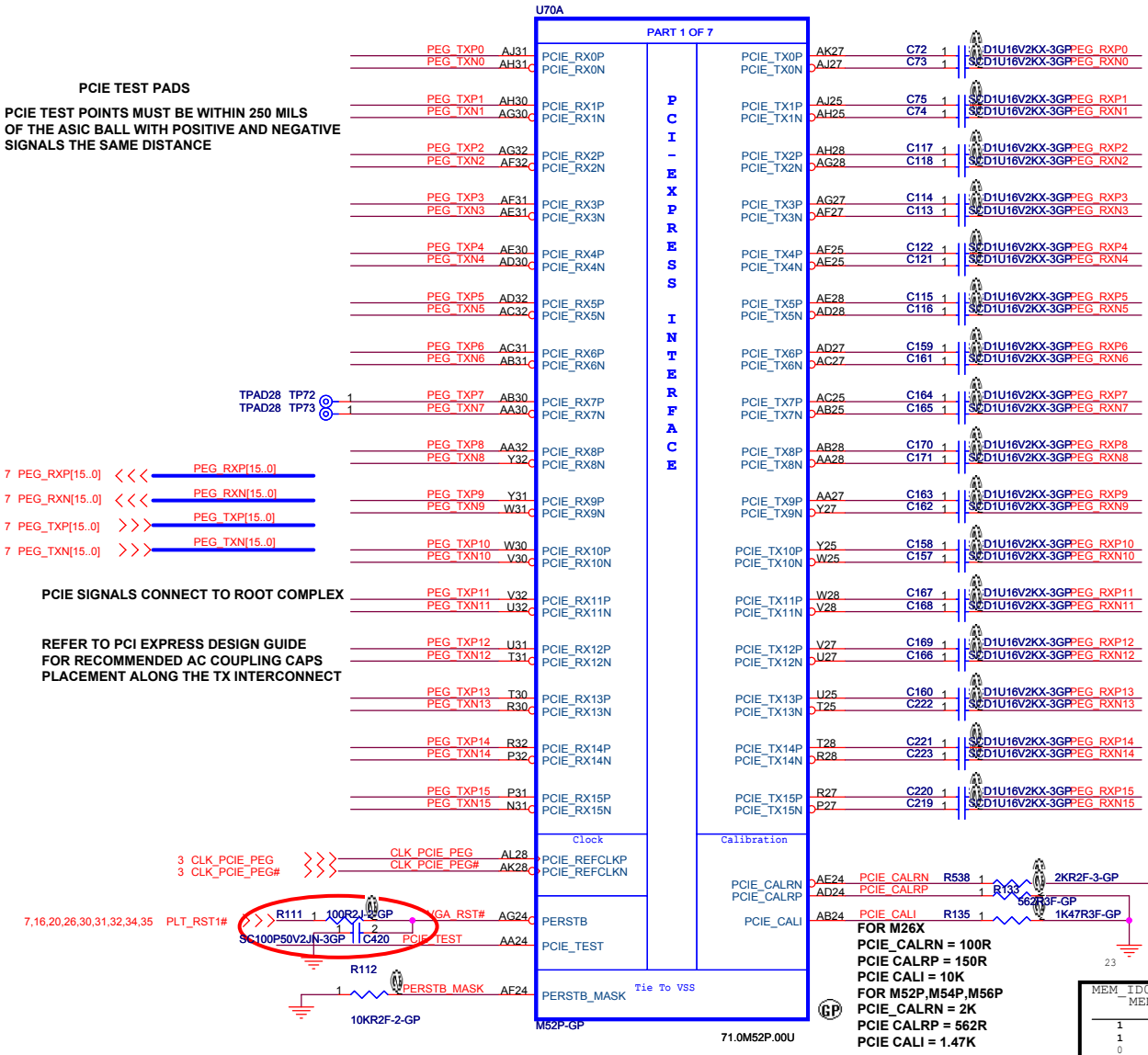


MAIN BATTERY CONNECTOR



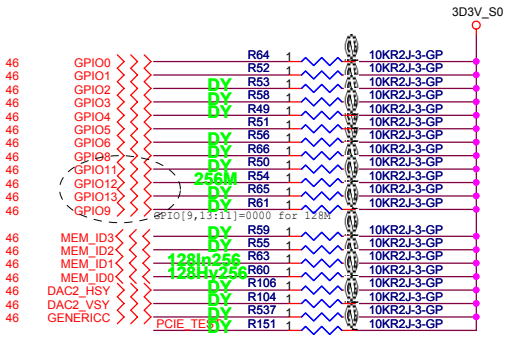
<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***AD/BATT CONN***
Size: A3	Document Number: AG1
Rev: -1	
Date: Tuesday, January 10, 2006	Sheet 44 of 53



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	GPIO[9,13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM	1011
MEMORY APERTURE SIZE	GPIO[13:11]	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPs
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4



When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

VGA THERMAL SENSOR

Place near GPU

IT IS REQUIRED TO DESIGN IN A THERMAL SENSOR
TO FACILITATE THERMAL EVALUATION AND TO PROTECT THE ASIC

<Variant Name>

緯創資通 **Wistron Corporation**
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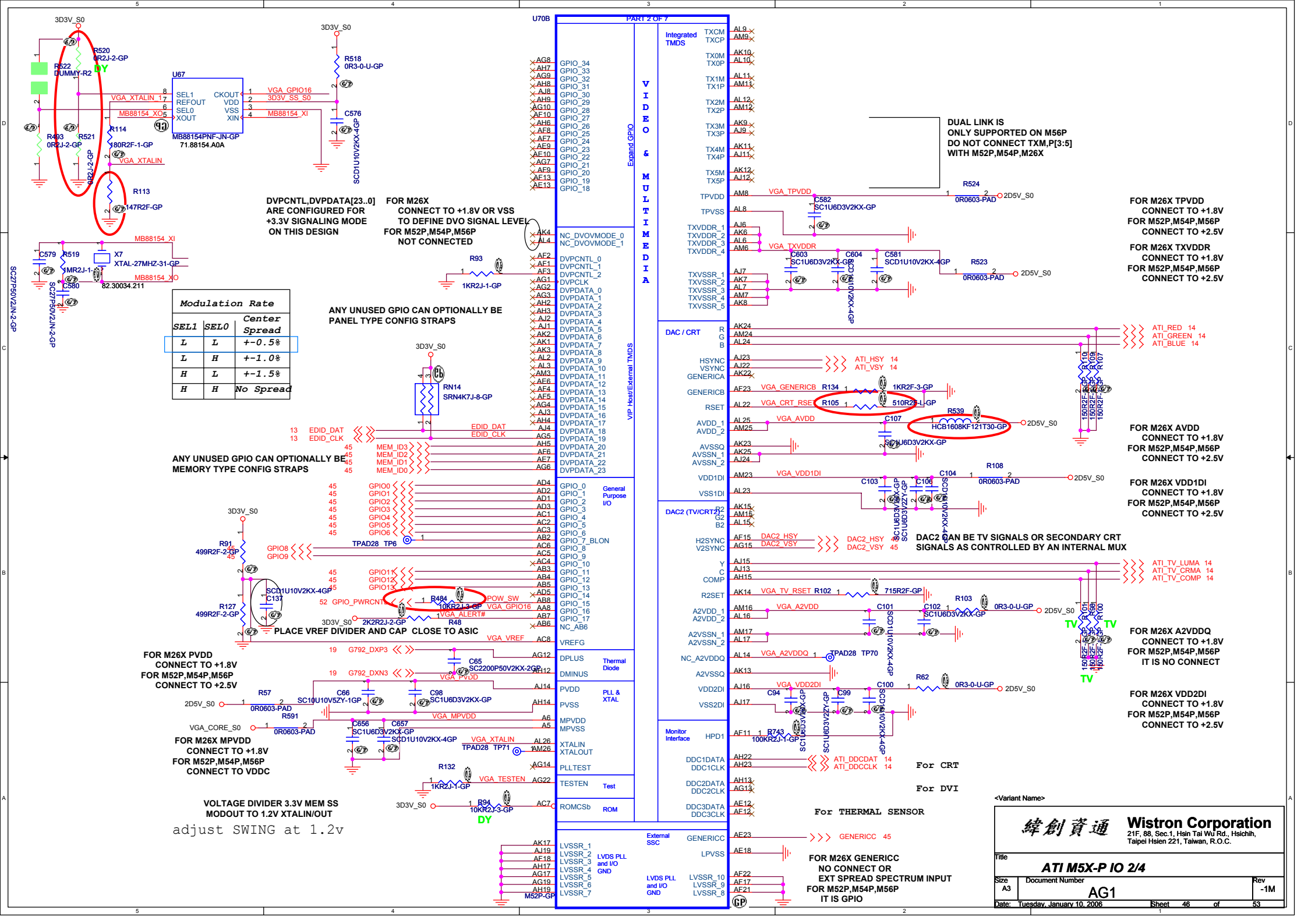
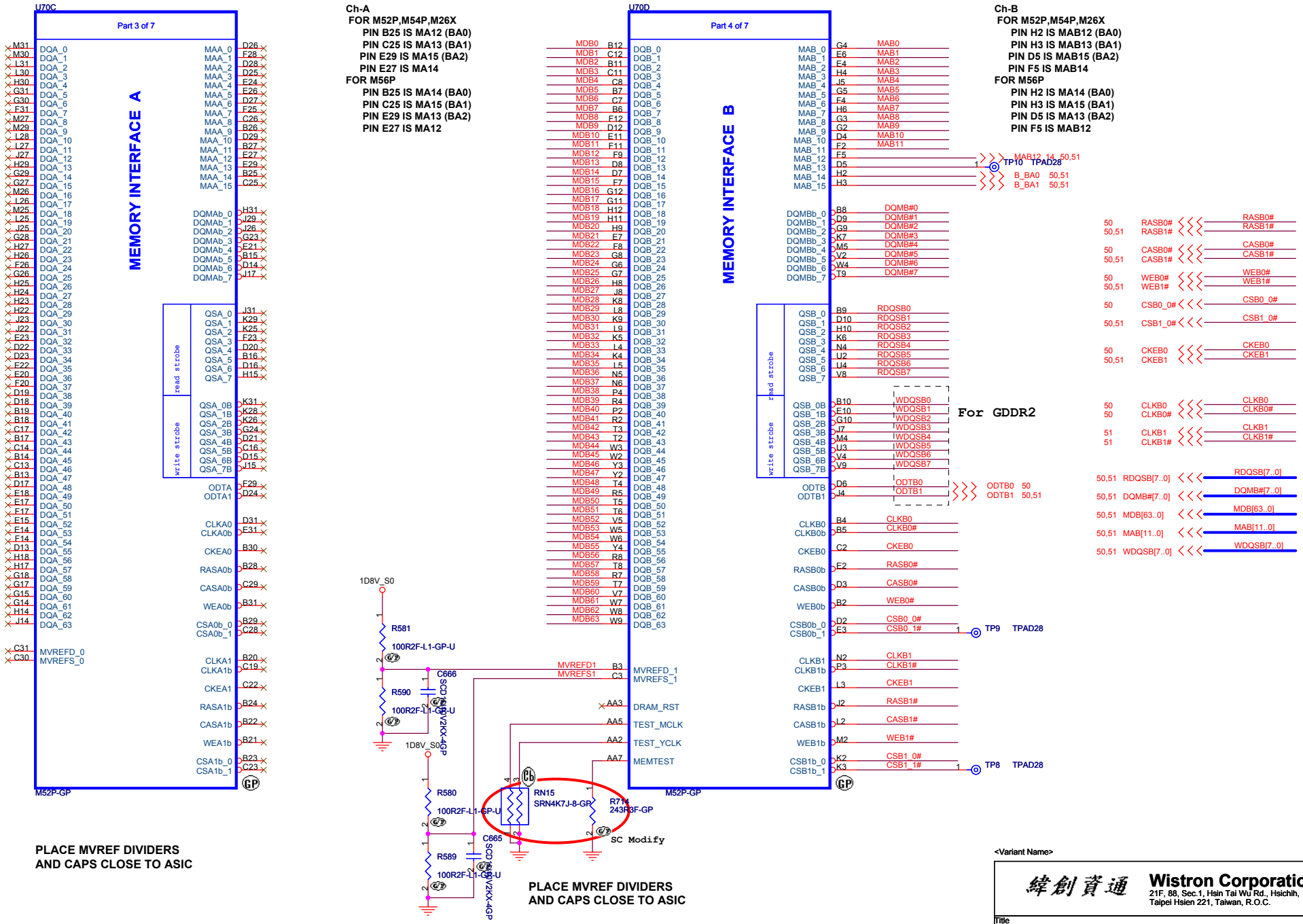
Title: **ATI M5X-P PCIE 1/4**

Size: A3 | Document Number: AG1 | Rev: SD

Date: Tuesday, January 10, 2006 | Sheet 45 of 53


U70B
PART 2 OF 7
VIDEO & MULTIMEDIA
Expand GPIO
VIP Host/External TMDS
Integrated TMDS
DAC / CRT
DAC2 (TV/CRT2)
Monitor Interface
General Purpose I/O
Thermal Diode
PLL & XTAL
Test
ROM
LVDS PLL and I/O GND
External SSC
U67
MB88154PNF-JN-GP
71.88154.A0A
SCD1U10V2KX-4GP
SC27P50V2JN-2-GP
Modulation Rate
SEL1 SEL0 Center Spread
L L +-0.5%
L H +-1.0%
H L +-1.5%
H H No Spread
DVPCNTL,DVPDATA[23..0] ARE CONFIGURED FOR +3.3V SIGNALING MODE ON THIS DESIGN
FOR M26X CONNECT TO +1.8V OR VSS TO DEFINE DVO SIGNAL LEVEL FOR M52P,M54P,M56P NOT CONNECTED
ANY UNUSED GPIO CAN OPTIONALLY BE PANEL TYPE CONFIG STRAPS
ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS
PLACE VREF DIVIDER AND CAP CLOSE TO ASIC
DUAL LINK IS ONLY SUPPORTED ON M56P DO NOT CONNECT TXM,P[3:5] WITH M52P,M54P,M26X
DAC2 CAN BE TV SIGNALS OR SECONDARY CRT SIGNALS AS CONTROLLED BY AN INTERNAL MUX
FOR M26X TPVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X TXVDDR CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X AVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X VDD1DI CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X A2VDDQ CONNECT TO +1.8V FOR M52P,M54P,M56P IT IS NO CONNECT
FOR M26X VDD2DI CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X PVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO +2.5V
FOR M26X MPVDD CONNECT TO +1.8V FOR M52P,M54P,M56P CONNECT TO VDDC
VOLTAGE DIVIDER 3.3V MEM SS MODOUT TO 1.2V XTALIN/OUT
adjust SWING at 1.2v
For CRT
For DVI
For THERMAL SENSOR
FOR M26X GENERICC NO CONNECT OR EXT SPREAD SPECTRUM INPUT FOR M52P,M54P,M56P IT IS GPIO
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M5X-P IO 2/4
Size A3
Document Number AG1
Rev -1M
Date: Tuesday, January 10, 2006
Sheet 46 of 53



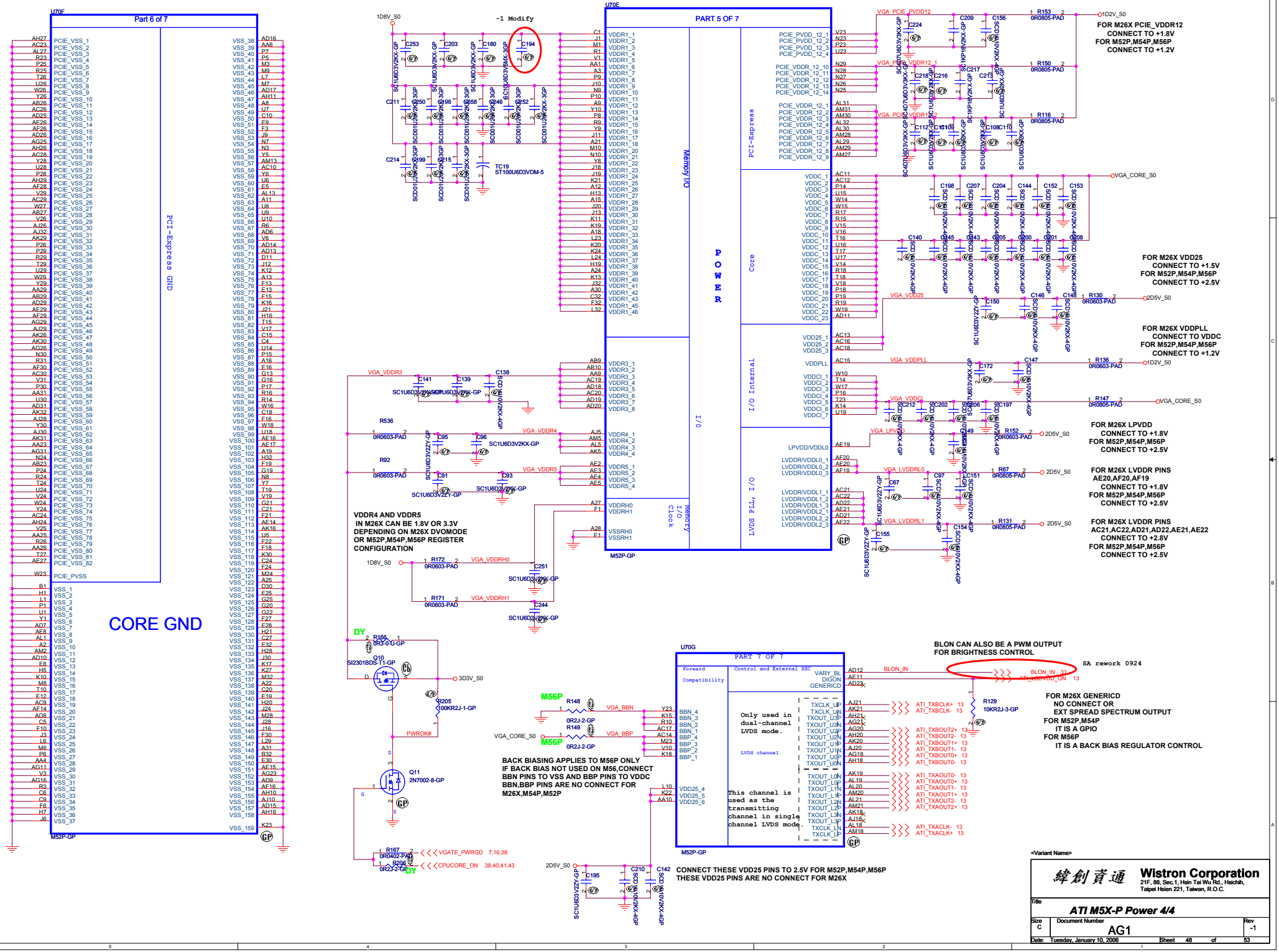
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M5X-P MEM 3/4**

Size	Document Number	Rev
A3	AG1	SC

Date: Tuesday, January 10, 2006 Sheet 47 of 53



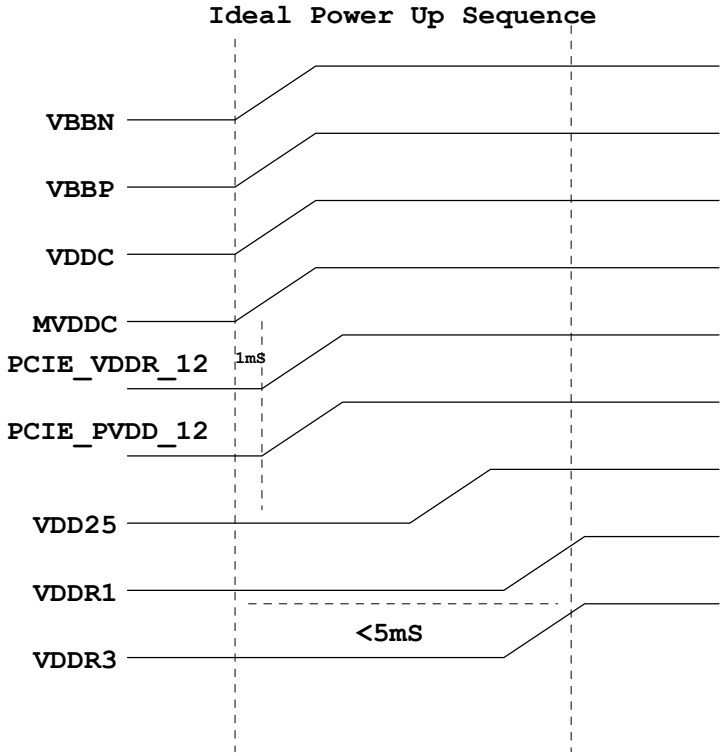
<Variant Name>

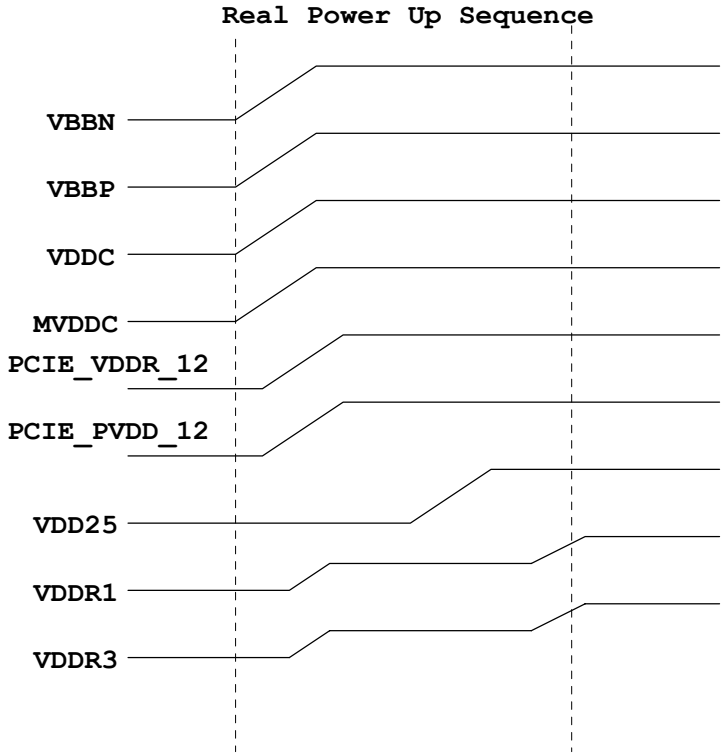
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P Power 4/4

Size: C | Document Number: AG1 | Rev: -1

Date: Tuesday, January 10, 2006 | Sheet 48 of 53





RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

General Guidelines:

- **BBN and BBP must ramp up before or at the same time as VDDC but not after.**
- **VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).**
- **All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).**
- **VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.**
- **The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.**

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

<Variant Name>

緯創資通 Wistron Corporation
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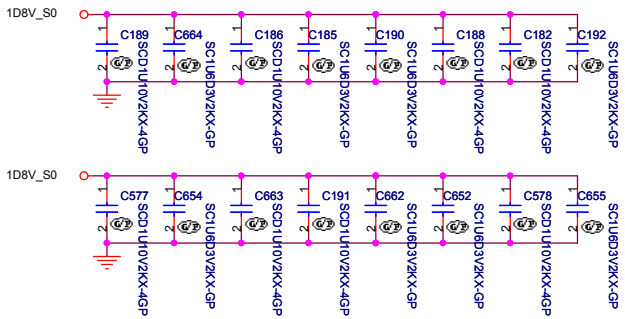
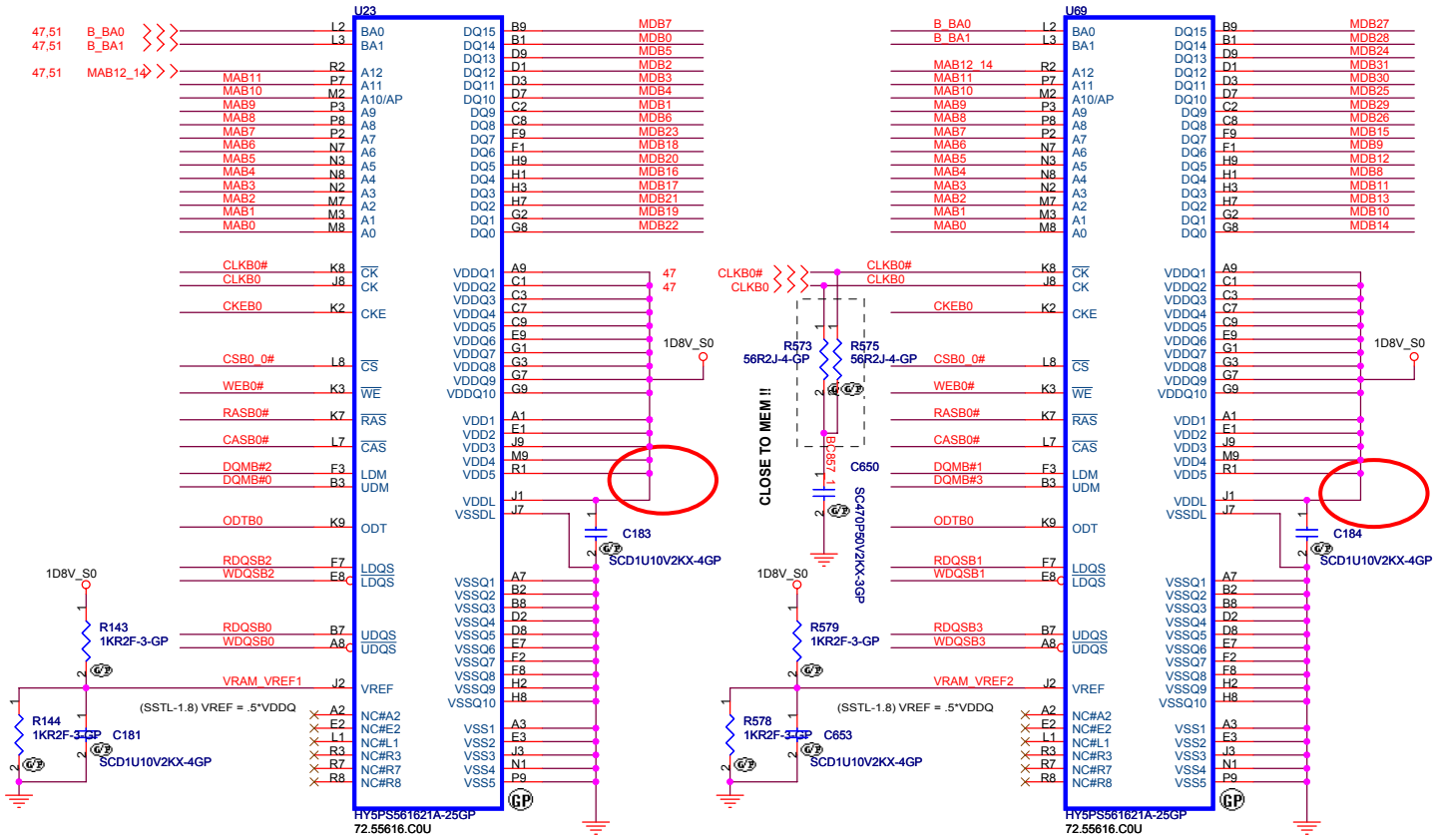
Title: ATI M5X-P POWER SEQUENCE

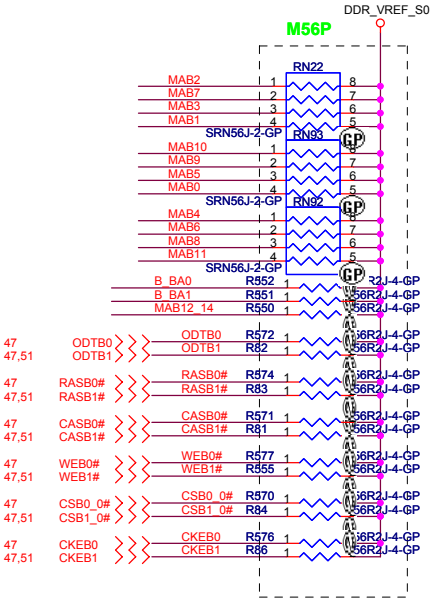
Size	Document Number	Rev
A3	AG1	SA

Date: Tuesday, January 10, 2006 Sheet 49 of 53

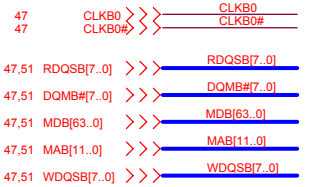
CHAN B DDR2 84BGA 32MX16 MEMORY







FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)



72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 350Mhz) Hynix-128M
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M*16, 350Mhz) Infineon-128M
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M*16, 400Mhz) Infineon-256M

<Variant Name>

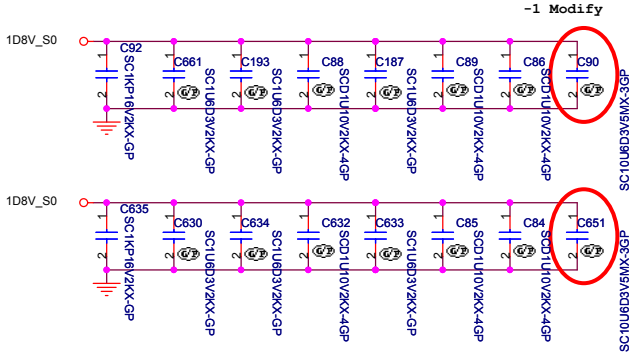
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

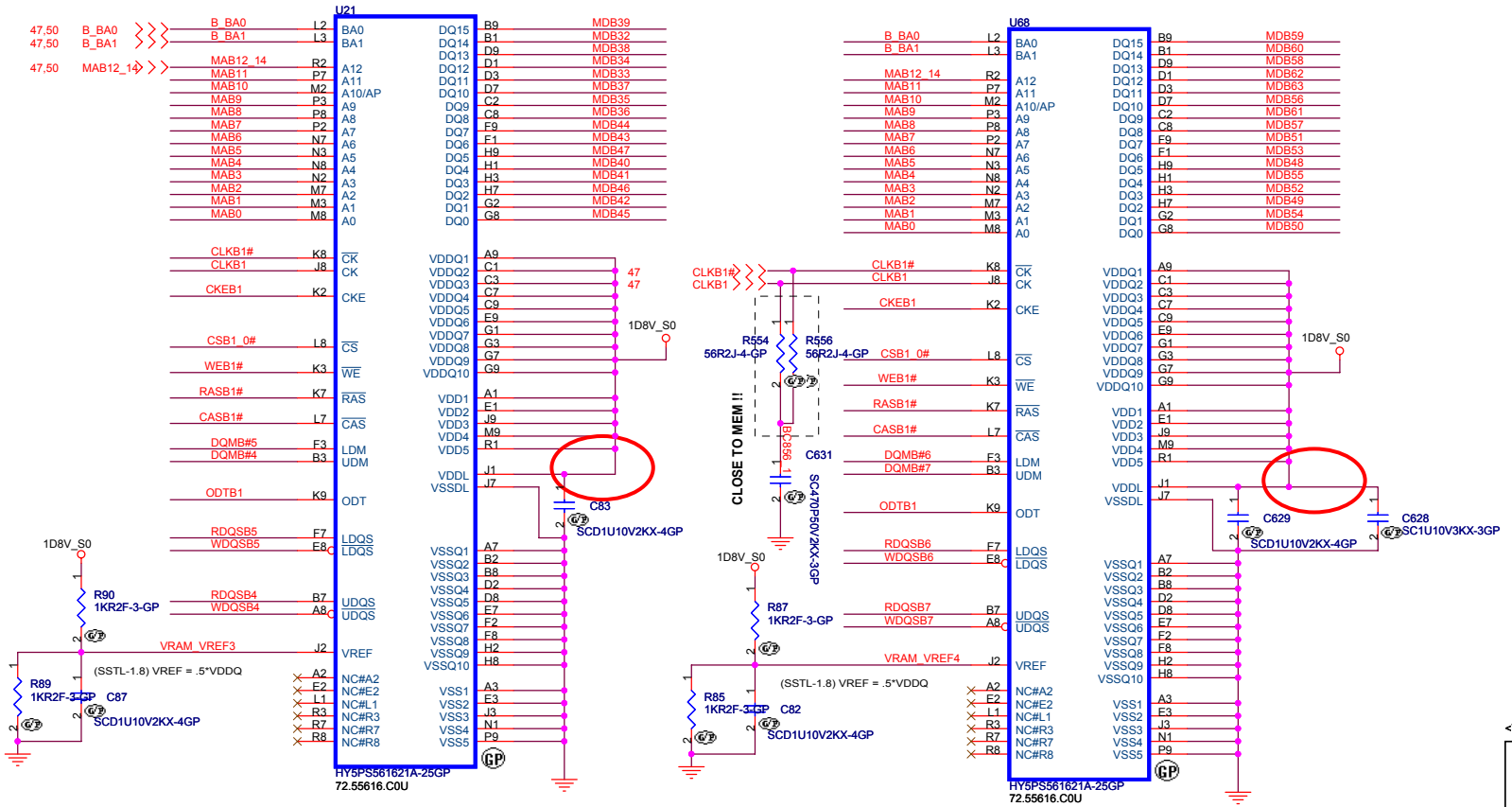
Title: ***VRAM 1/2***

Size	Document Number	Rev
A3	AG1	SC

Date: Tuesday, January 10, 2006 Sheet 50 of 53

-1 Modify





47,50 RASB1# — RASB1#
47,50 CASB1# — CASB1#
47,50 WEB1# — WEB1#
47,50 CSB1_0# — CSB1_0#
47,50 CKEB1 — CKEB1
47,50 ODTB1 — ODTB1
47 CLKB1 — CLKB1
47 CLKB1# — CLKB1#
47,50 RDQSB[7..0] — RDQSB[7..0]
47,50 DQMB#[7..0] — DQMB#[7..0]
47,50 MDB[63..0] — MDB[63..0]
47,50 MAB[11..0] — MAB[11..0]
47,50 WDQSB[7..0] — WDQSB[7..0]

<Variant Name>

緯創資通 **Wistron Corporation**
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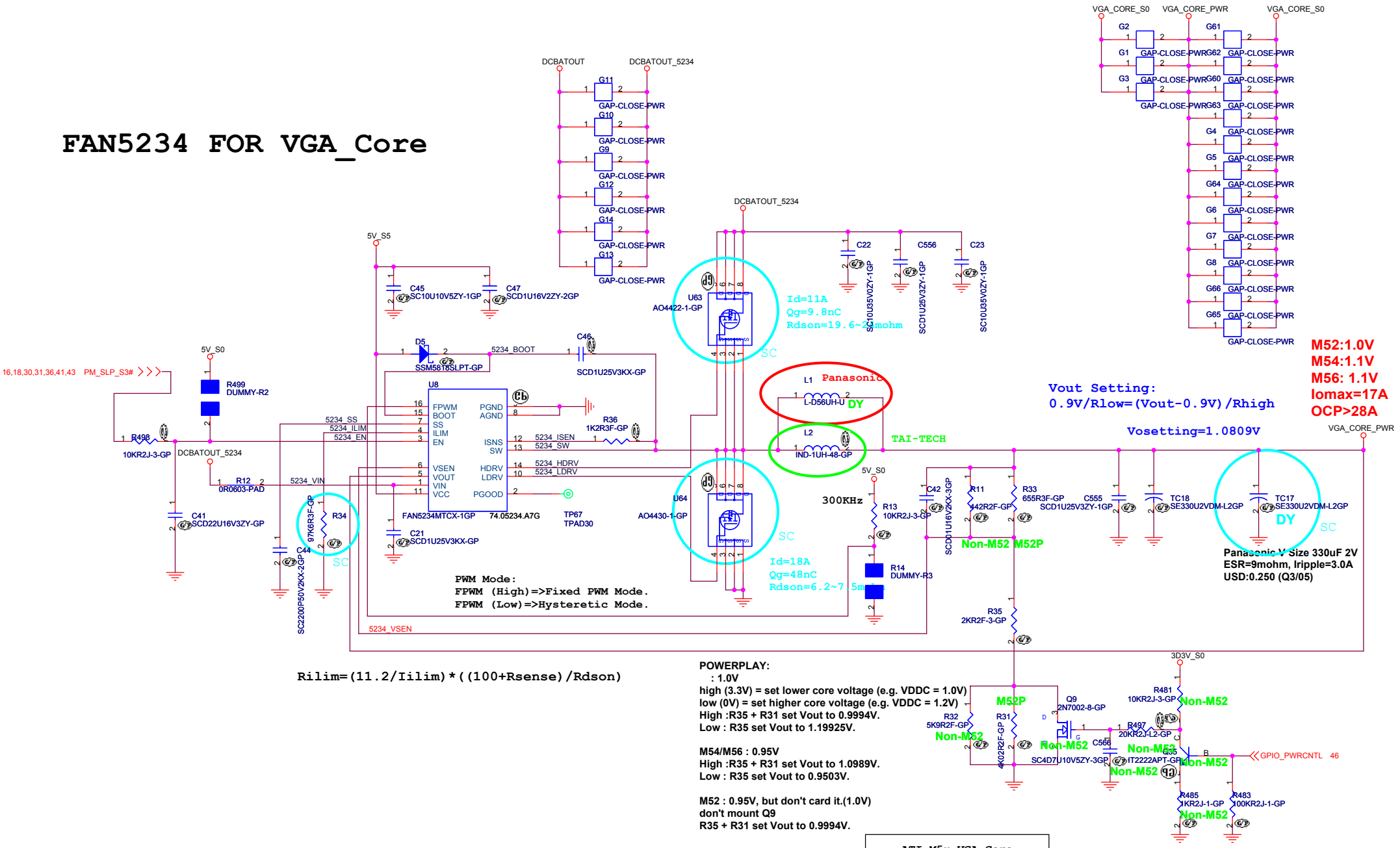
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM 2/2**

Size	Document Number	Rev
A3	AG1	-1

Date: Tuesday, January 10, 2006 Sheet 51 of 53

FAN5234 FOR VGA_Core



Rilim=(11.2/Iilim)*((100+Rsense)/Rdson)

POWERPLAY:
: 1.0V
high (3.3V) = set lower core voltage (e.g. VDDC = 1.0V)
low (0V) = set higher core voltage (e.g. VDDC = 1.2V)
High :R35 + R31 set Vout to 0.9994v.
Low : R35 set Vout to 1.19925V.

M54/M56 : 0.95V
High :R35 + R31 set Vout to 1.0989V.
Low : R35 set Vout to 0.9503V.

M52 : 0.95V, but don't card it.(1.0V)
don't mount Q9
R35 + R31 set Vout to 0.9994V.

ATI M5x VGA Core			
VGA	Ver.	Normal	PowerPlay
M52	A12	1.0	0.95/1.0
M54	A12	1.1	0.95/0.95
M56		1.2	0.95
	B24	1.1	0.95/0.95

<Variant Name>

緯創資通 Wistron Corporation
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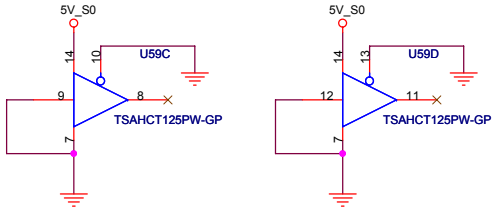
Taipei Hsien 221, Taiwan, R.O.C.

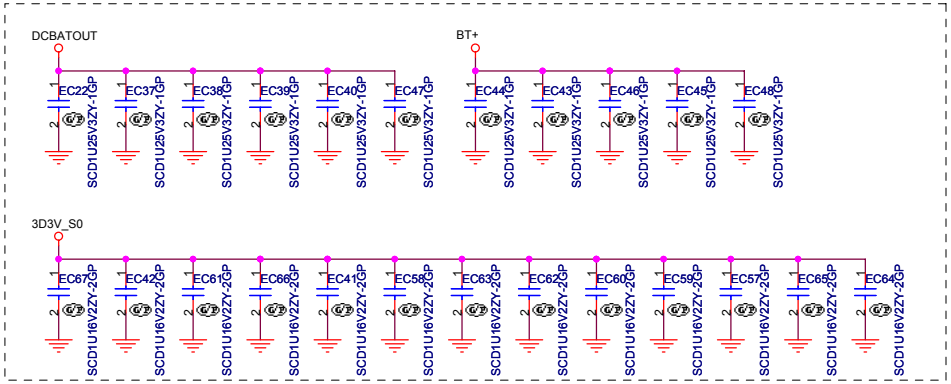
Title: VGA CORE 1D1V

Size	Document Number	Rev
A3	AG1	-1

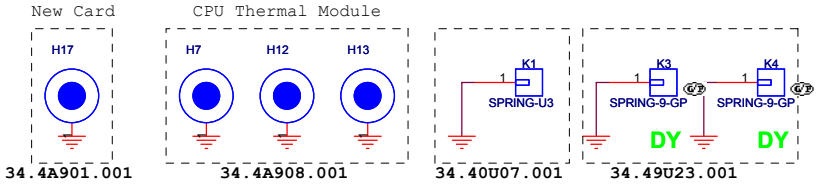
Date: Tuesday, January 10, 2006 Sheet 52 of 53

EMI CAP

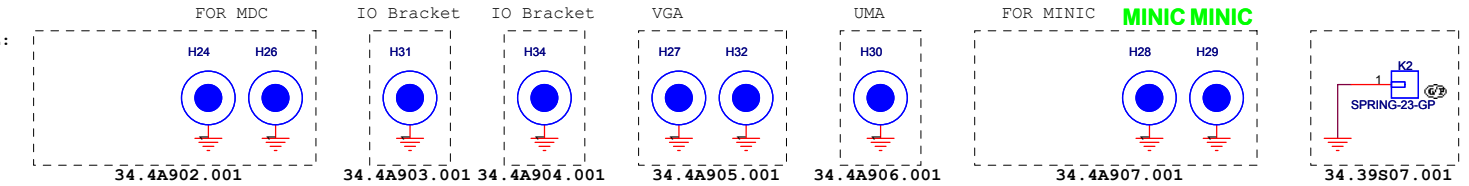


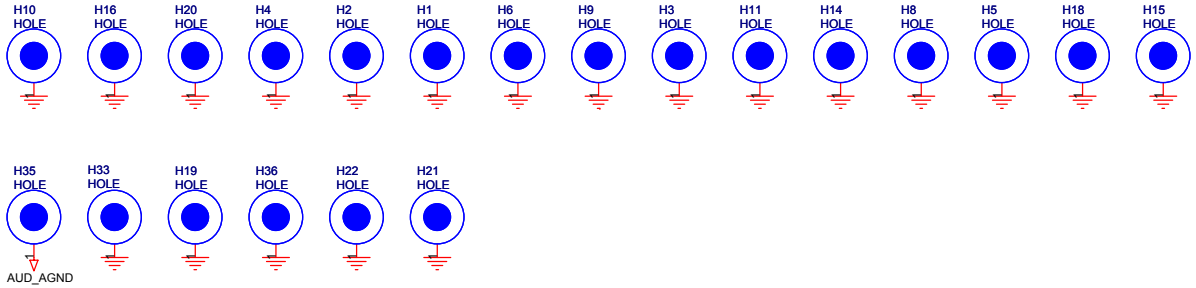


TOP SIDE:



BOTTOM SIDE:





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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