



PCB
Part Number = DAZ0FQ00100



64M512@
X76244BOL01
Part Number = X76244BOL01



64M1G@
X76244BOL03
Part Number = X76244BOL03



128M1G@
X76244BOL05
Part Number = X76244BOL05



128M2G@
X76244BOL06
Part Number = X76244BOL06

Compal Confidential

PEW76 Schematics Document

AMD Danube

Champlain Processor with RS880M/SB820/Madison VGA

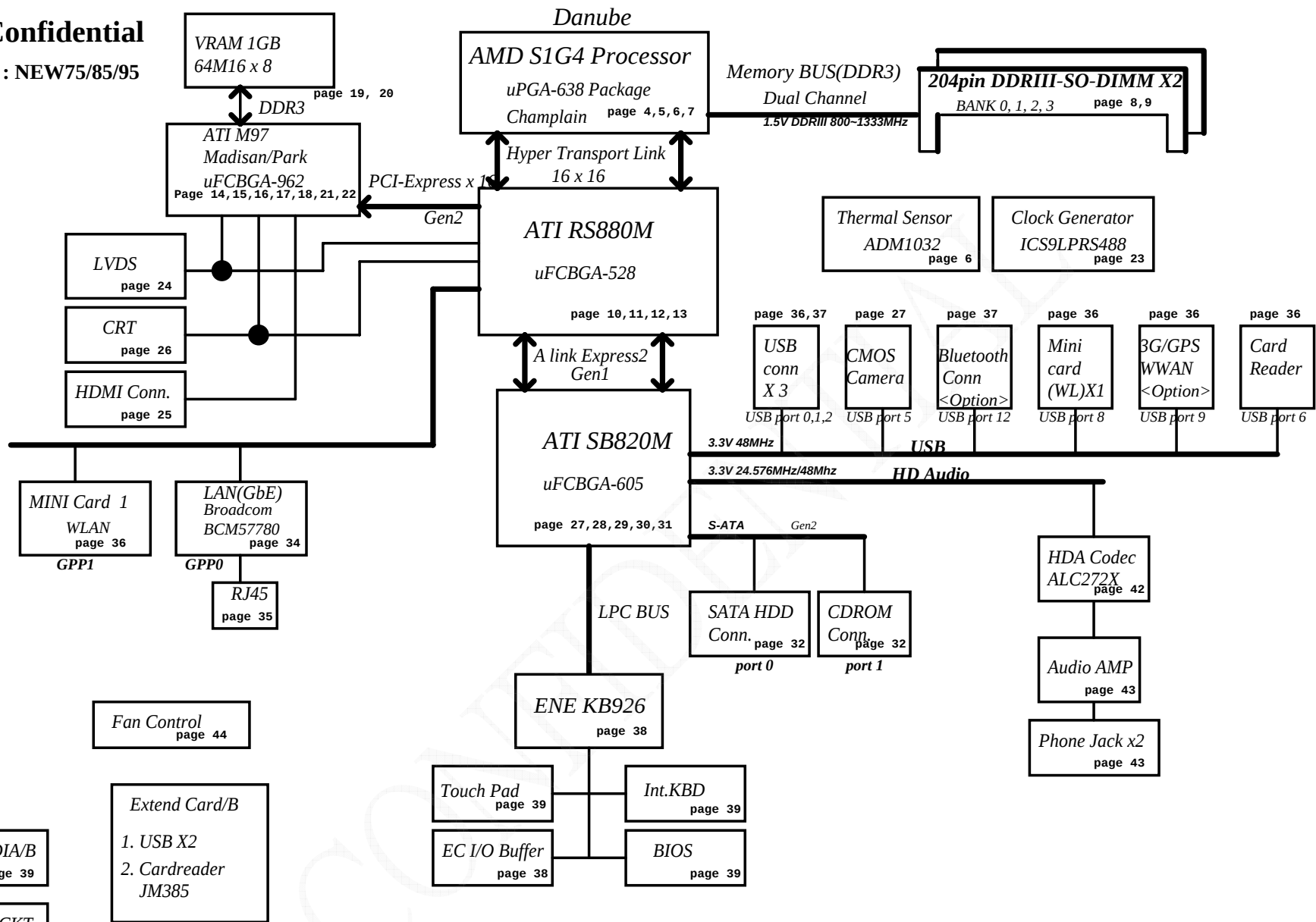
2010-06-07

LA5911P REV: 1.0

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Model Name : NEW75/85/95



LED
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RTC CKT.
page 26

LID SW / MEDIA/B
page 39

Power On/Off CKT.
page 41

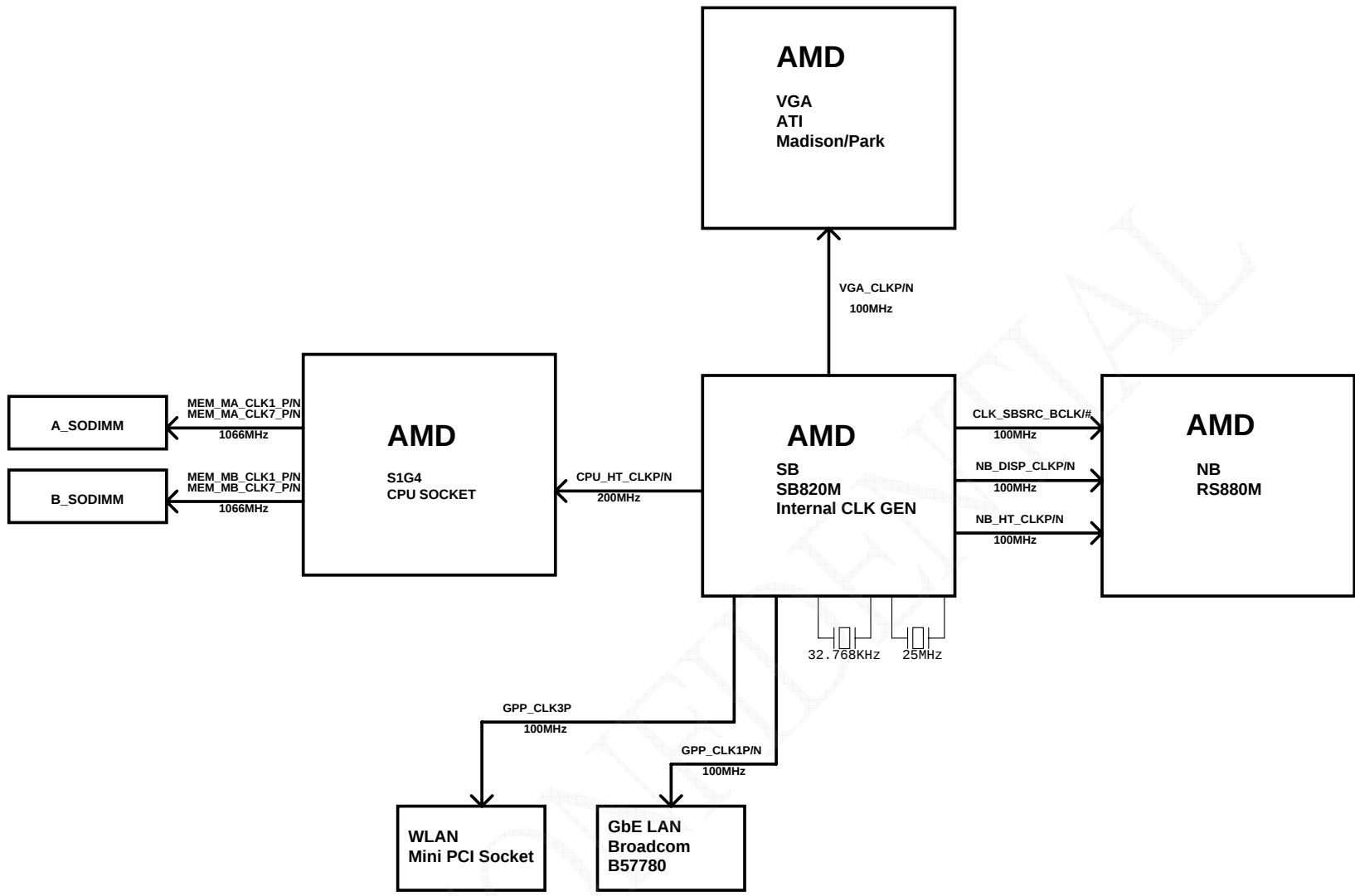
DC/DC Interface CKT.
page 45

Power Circuit
page 46, 47, 48, 49, 50, 51, 52, 53, 54

Fan Control
page 44

Extend Card/B
1. USB X2
2. Cardreader JM385

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Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	ON	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

External PCI Devices

EC SM Bus1 address

EC SM Bus2 address

SM Bus 0 address**SB820****SM Bus 1 address****EXT CLKGEN**

PowerXpress SKU(Madison): 3G@/BT@/UMA@/ VGA@/SG@/EXT@/EXTPW@/VB@/MAD@
 PowerXpress SKU(Park): 3G@/BT@/UMA@/ VGA@/SG@/EXT@/EXTPW@/VB@/PARK@
 DIS ONLY:(Park) 3G@/BT@/DISO@/ VGA@/EXT@/EXTPW@/PARK@
 UMA only SKU: 3G@/BT@/UMA@/ UMAO@/EXT@/VB@

PowerXpress SKU(Madison):3G@/BT@/UMA@/VGA@/SG@/INT@/VB@/MAD@
PowerXpress SKU(Park): 3G@/BT@/UMA@/VGA@/SG@/INT@/VB@/PARK@
DIS ONLY(PARK): 3G@/BT@/DISO@/VGA@/INT@/PARK@
UMA only SKU: 3G@/BT@/UMA@/UMAO@/INT@/VB@

Board ID / SKU ID Table for AD channel

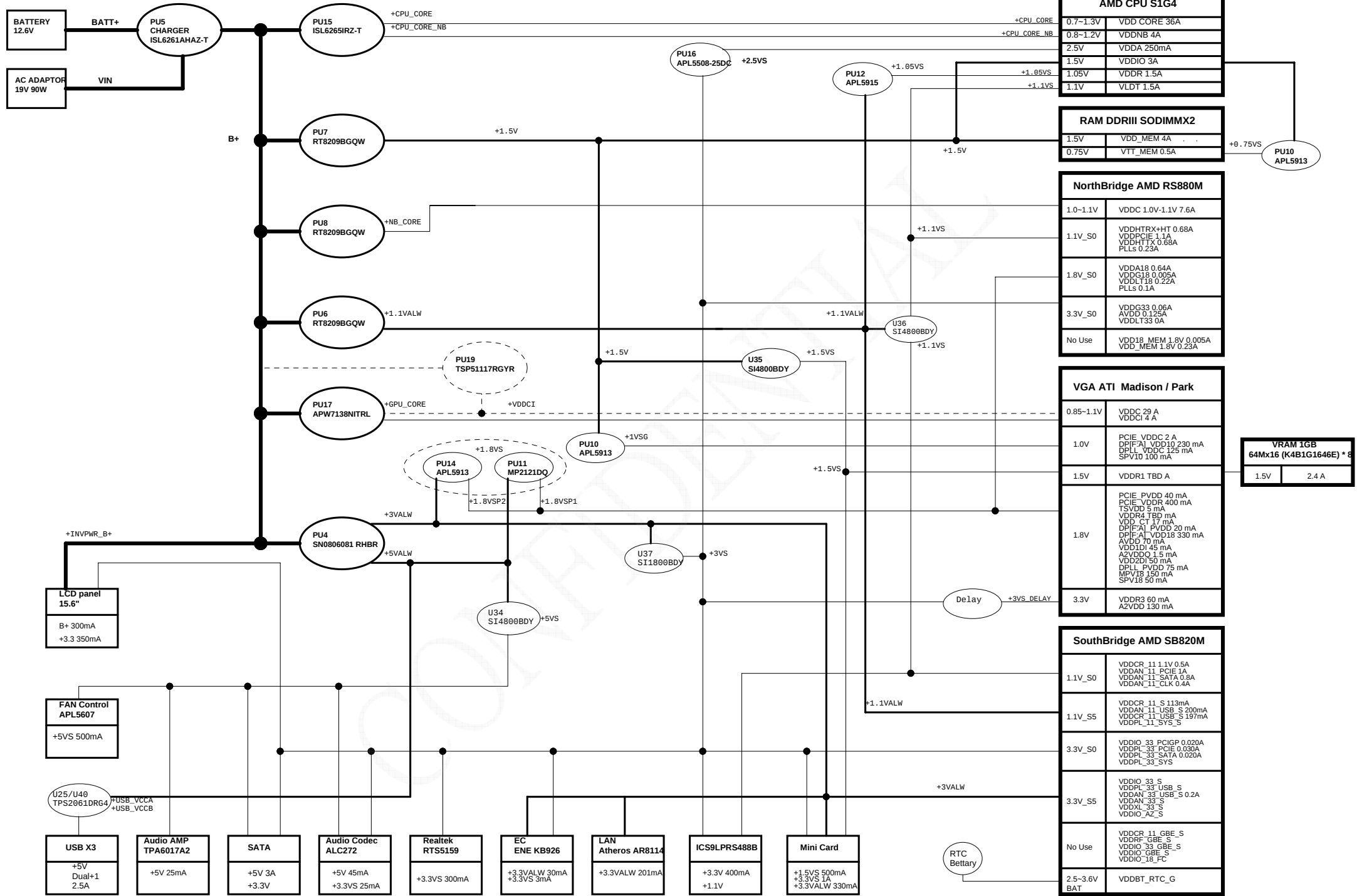
BOARD ID Table

BTO Option Table

Project ID Table

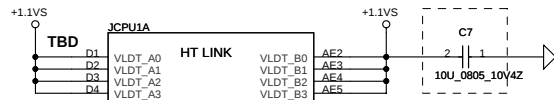
Board ID	PCB Revision
0	NEW75/85/95
1	PEW76/86/96
2	PEW56
3	
4	
5	
6	
7	

```
--For SSID define
--For TSI thermal math
```



<12> H_CADIP[0..15] H_CADIP[0..15]
<12> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <12>
H_CADON[0..15] H_CADON[0..15] <12>

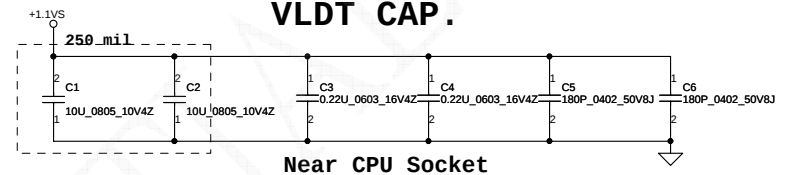


H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AA1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA2	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA3	H_CADOP3
H_CADIN3	H1	L0_CADIN_L3	L0_CADOUT_L3	W2	H_CADON3
H_CADIP4	J1	L0_CADIN_H4	L0_CADOUT_H4	W3	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	V1	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	U1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	U2	H_CADON5
H_CADIP6	M1	L0_CADIN_H6	L0_CADOUT_H6	U3	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	T1	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	R1	H_CADOP7
H_CADIN7	N2	L0_CADIN_L7	L0_CADOUT_L7	AD4	H_CADON7
H_CADIP8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD3	H_CADOP8
H_CADIN8	E5	L0_CADIN_L8	L0_CADOUT_L8	AD5	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AC5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AB4	H_CADON9
H_CADIP10	O5	L0_CADIN_H10	L0_CADOUT_H10	AB3	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB5	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AA5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	Y5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	W5	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	V4	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V3	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V5	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	U5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	T4	H_CADON14
H_CADIP15	N5	L0_CADIN_H15	L0_CADOUT_H15	T3	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15		

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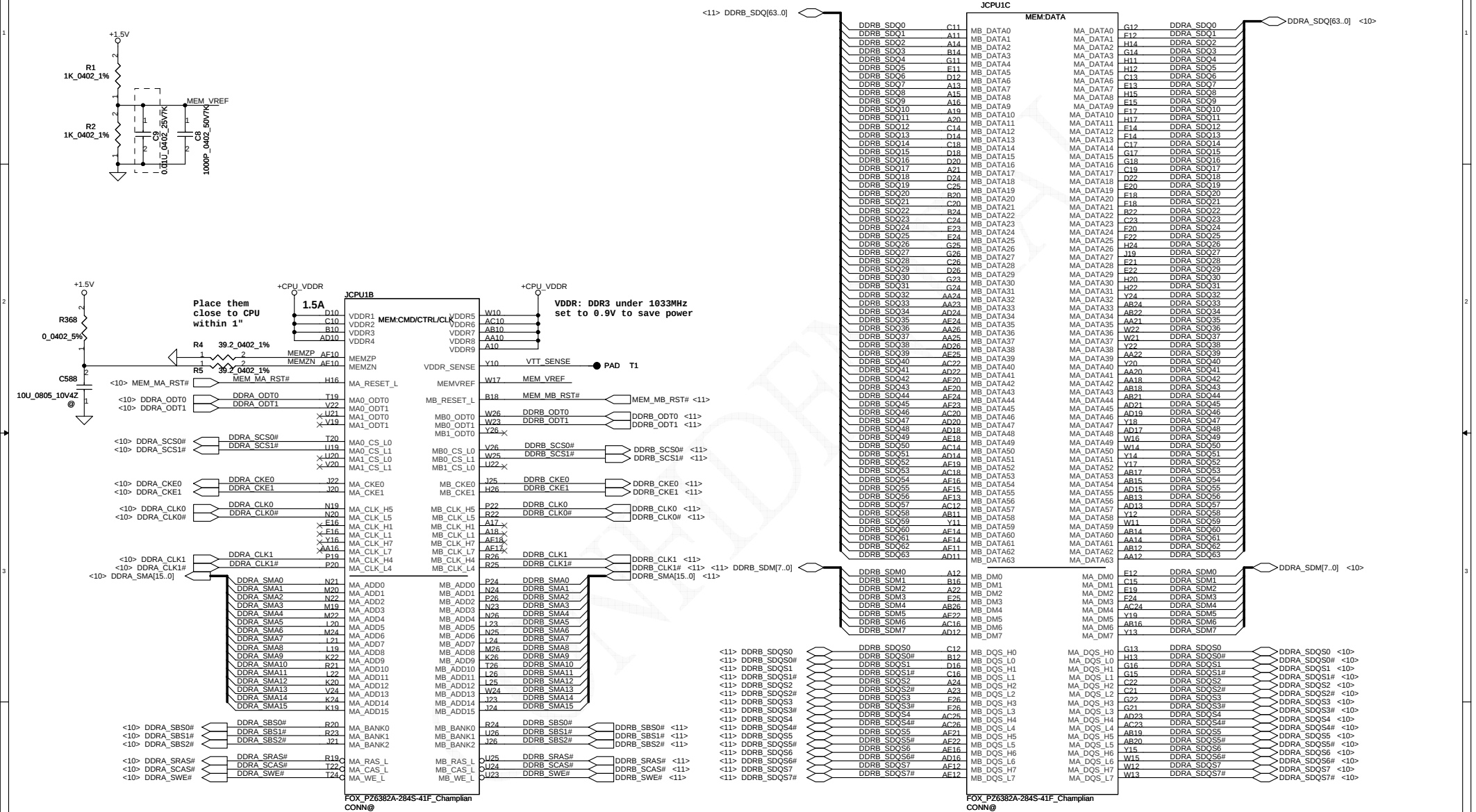
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<12> H_CTLIP1 P3 L0_CTLIN_H1 L0_CTLOUT_H1 T5 H_CTLOP1 <12>
<12> H_CTLIN1 P4 L0_CTLIN_L1 L0_CTLOUT_L1 R5 H_CTLON1 <12>

FOX_PZ6382A-2845-41F_Champion
CONN@



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Processor DDR3 Memory Interface



VDD(+CPU_CORE) decoupling.

Near CPU Socket

Under CPU Socket

Under CPU Socket

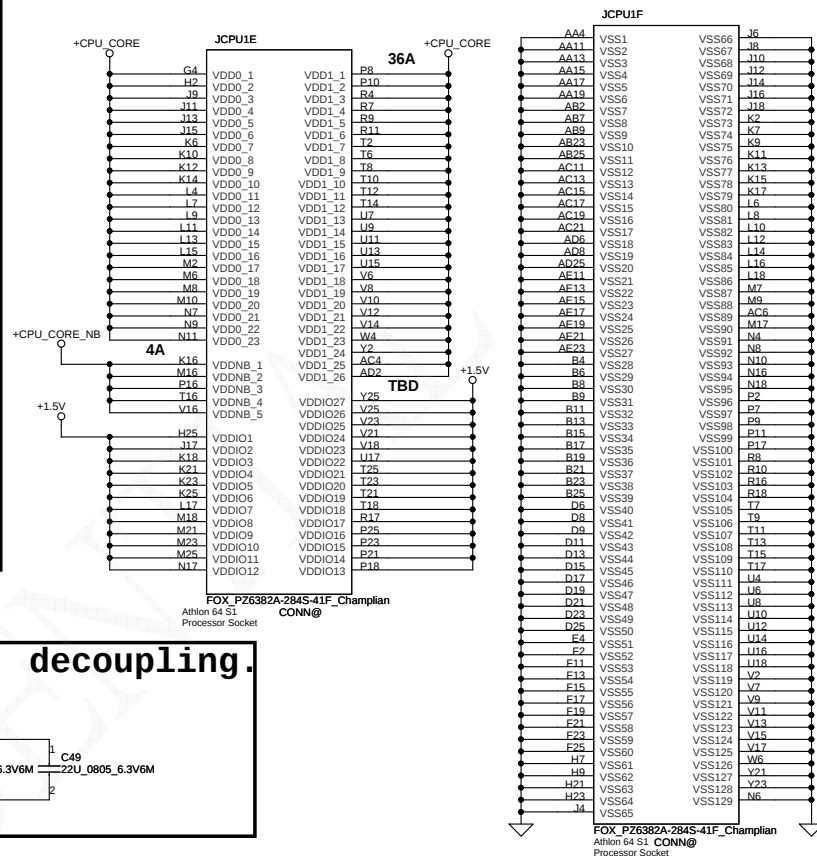
The diagrams illustrate the placement of capacitors for the CPU and DIMM power planes:

- Under CPU Socket:** A series of capacitors (C44 to C50) connected to a +1.5V supply. C44, C45, and C46 are 220µF 6.3V electrolytic capacitors. C47, C48, and C49 are 0.22µF capacitors. C50 is an 180pF capacitor. The ground reference is indicated by a triangle symbol.
- Between CPU Socket and DIMM:** A series of capacitors (C51 to C55) connected to a +1.5V supply. C51, C52, C53, C54, and C55 are 0.22µF capacitors. C354 and C355 are 0.22µF capacitors. The ground reference is indicated by a triangle symbol.
- 180PF Qt'y follow the distance between CPU socket and DIMM0. <2.5inch>** This section shows a series of capacitors (C64 to C69) connected to a +1.5V supply. C64 and C65 are 0.01µF capacitors. C66, C67, and C68 are 0.1µF capacitors. C69 is an 180pF capacitor. The ground reference is indicated by a triangle symbol.
- Bottom Diagram:** A series of capacitors (C71 to C75) connected to a +1.5V supply. C71, C72, C73, and C74 are 4.7µF 10V electrolytic capacitors. C75 is a 330µF capacitor. The ground reference is indicated by a triangle symbol.

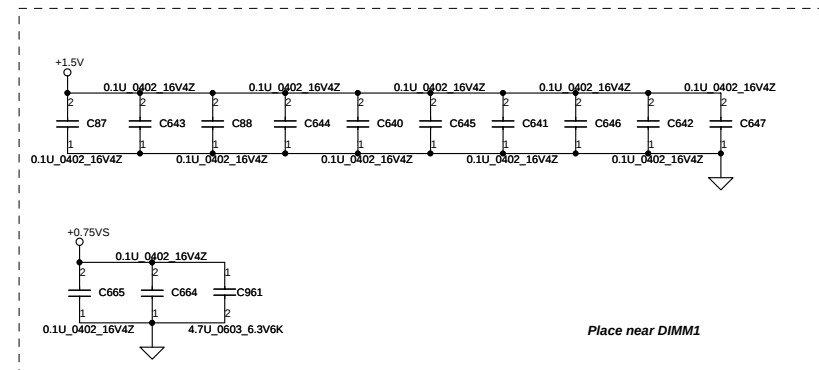
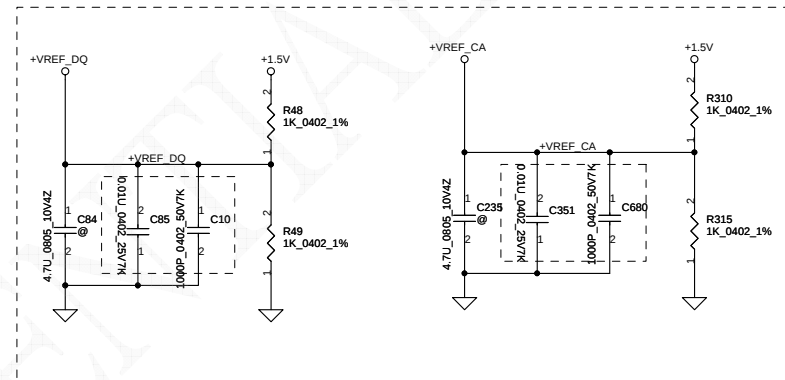
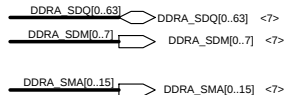
VDDR decoupling.

The diagram illustrates the VDDR decoupling layout, divided into three main sections:

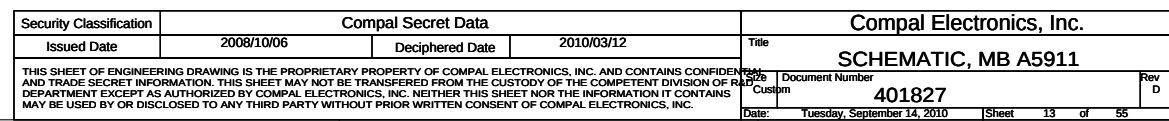
- Near Power Supply:** This section shows the connection to the +CPU_VDDR supply. It includes a callout for a change to SGA00002N80. The components shown are C56 (150U_B_6.3VM_R40M) and C55 (22U_0805_6.3V6M).
- Near CPU Socket Right side:** This section shows the decoupling network for the right side of the CPU socket. It includes components C57 (4.7U_0805_10V4Z), C58 (4.7U_0805_10V4Z), C59 (0.22U_0603_16V4Z), C60 (0.22U_0603_16V4Z), C61 (1000P_0402_50V7K), C62 (1000P_0402_50V7K), C63 (180P_0402_50V8J), and C70 (180P_0402_50V8J).
- Near CPU Socket Left side:** This section shows the decoupling network for the left side of the CPU socket. It includes components C76 (4.7U_0805_10V4Z), C77 (4.7U_0805_10V4Z), C78 (0.22U_0603_16V4Z), C79 (0.22U_0603_16V4Z), C80 (1000P_0402_50V7K), C81 (1000P_0402_50V7K), C82 (180P_0402_50V8J), and C83 (180P_0402_50V8J).

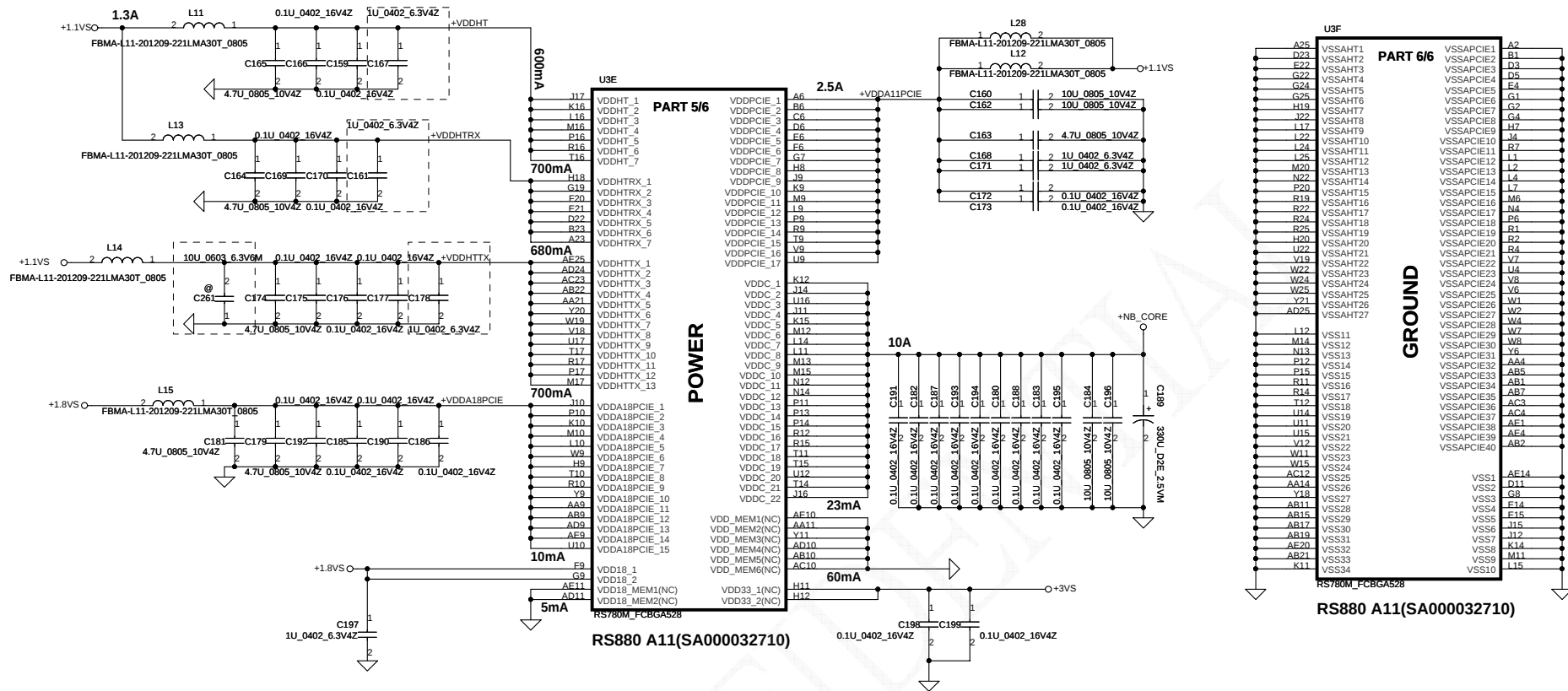


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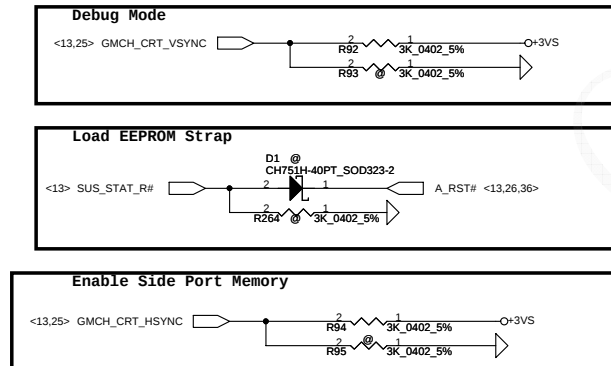


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Side port and Strap setting



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)

1 : Disable

0 : Enable

DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Enable Side Port Memory

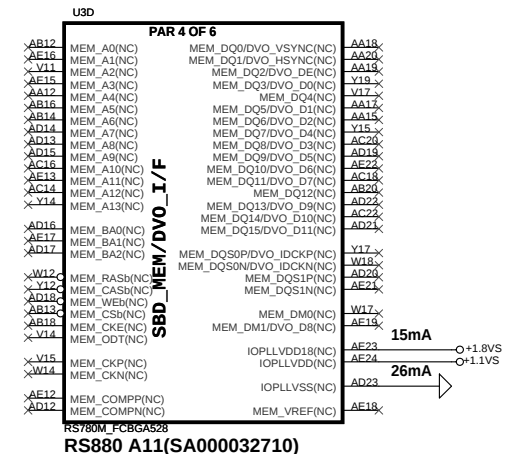
RS880: HSYN#

0: Enable

1 : Disable

Register Readback of strap:

NB_CLKCFG:CLK_TOP_SPARE_D[1]

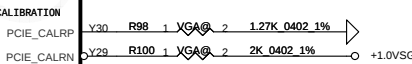
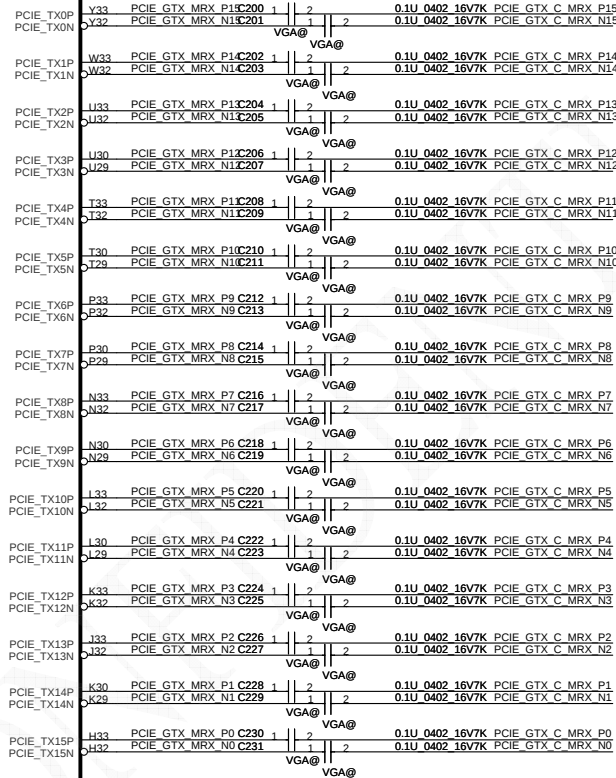
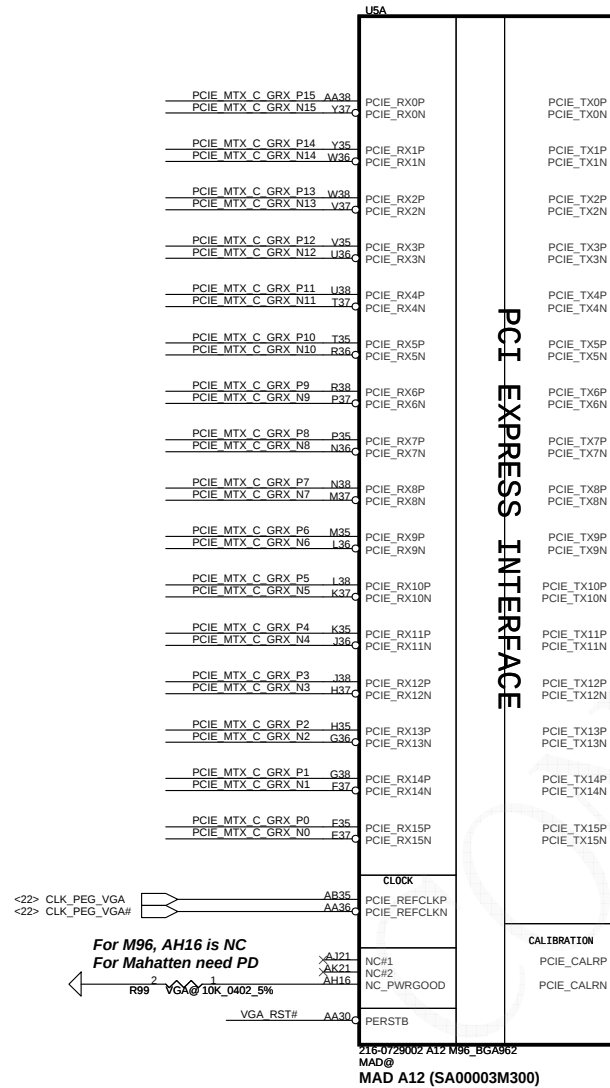


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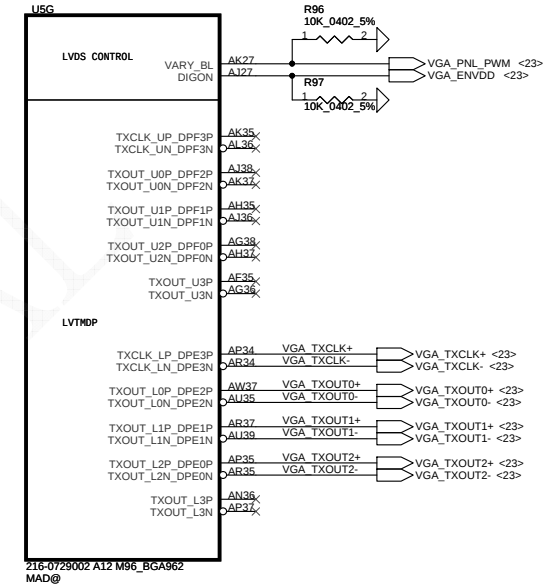
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PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] <12>

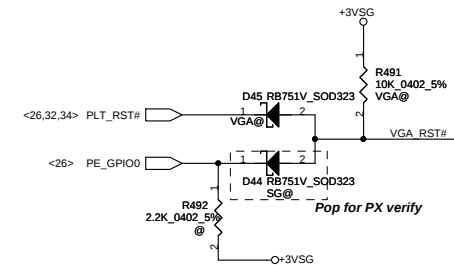
GFX PCIE LANE REVERSAL



add for VB support.

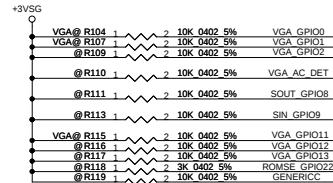


U5 PARK@
PARK XT-M2 A11
PARK A11 (SA00003MC10)



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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2.1.0): a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 256 MB 001 * b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Disable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC GPIO8 GPIO21	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	

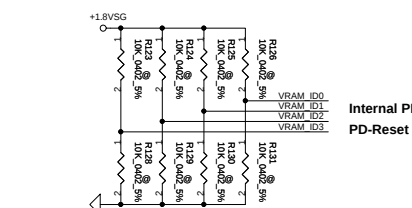


Park (XT)

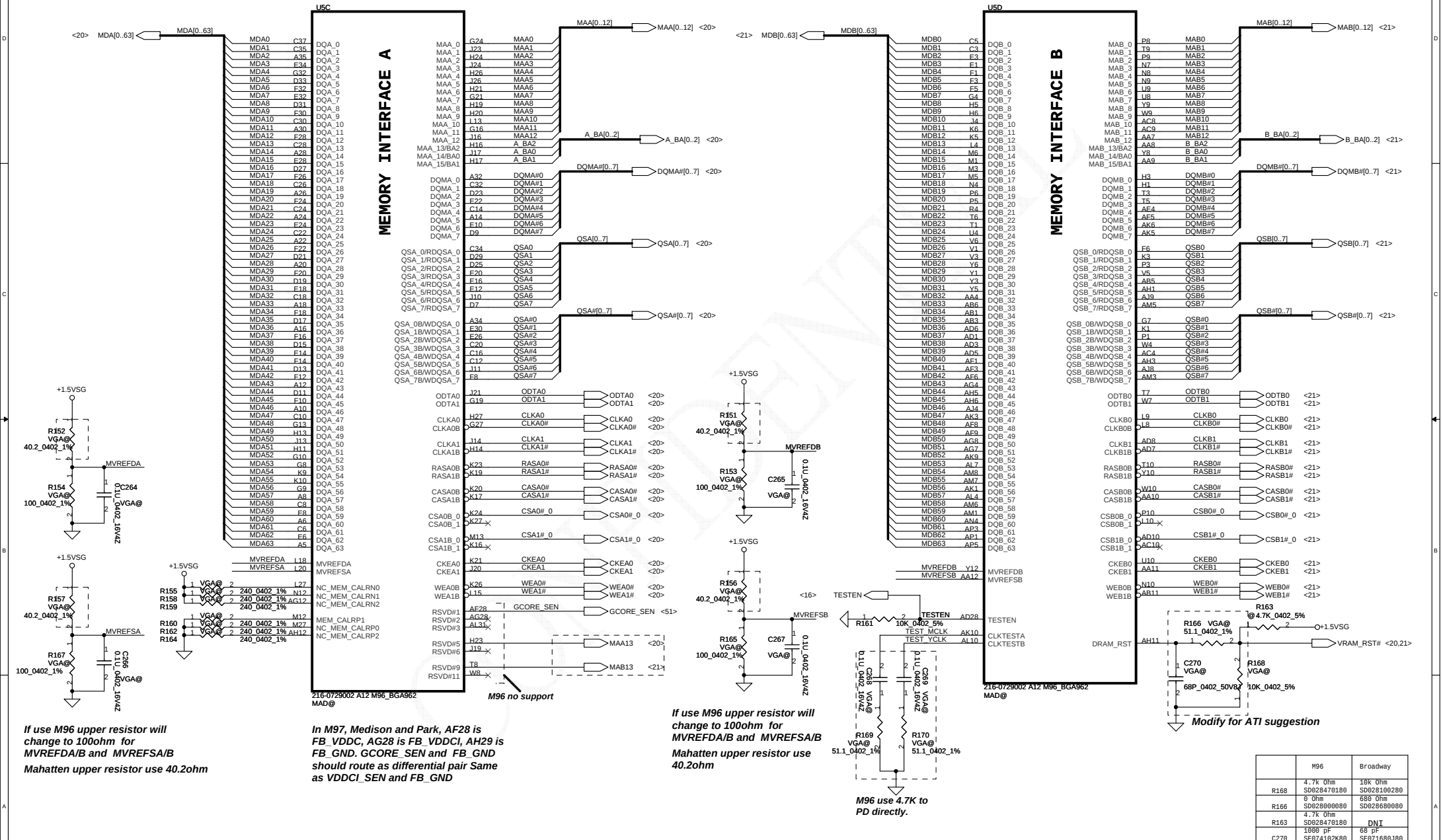
Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	<vendor1>	<pcps> 64MX16	<vendor2>	<size>
Hynix	1	1	0	0
AMD	1	1	1	0
Hynix(128MbX16)	1	1	0	1

Madsion (Pro)

Location	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	<vendor>	<size> 64MX16	0	0
Hynix	1	0	0	0
AMD	1	0	1	0
Hynix(128MbX16)	1	0	0	1

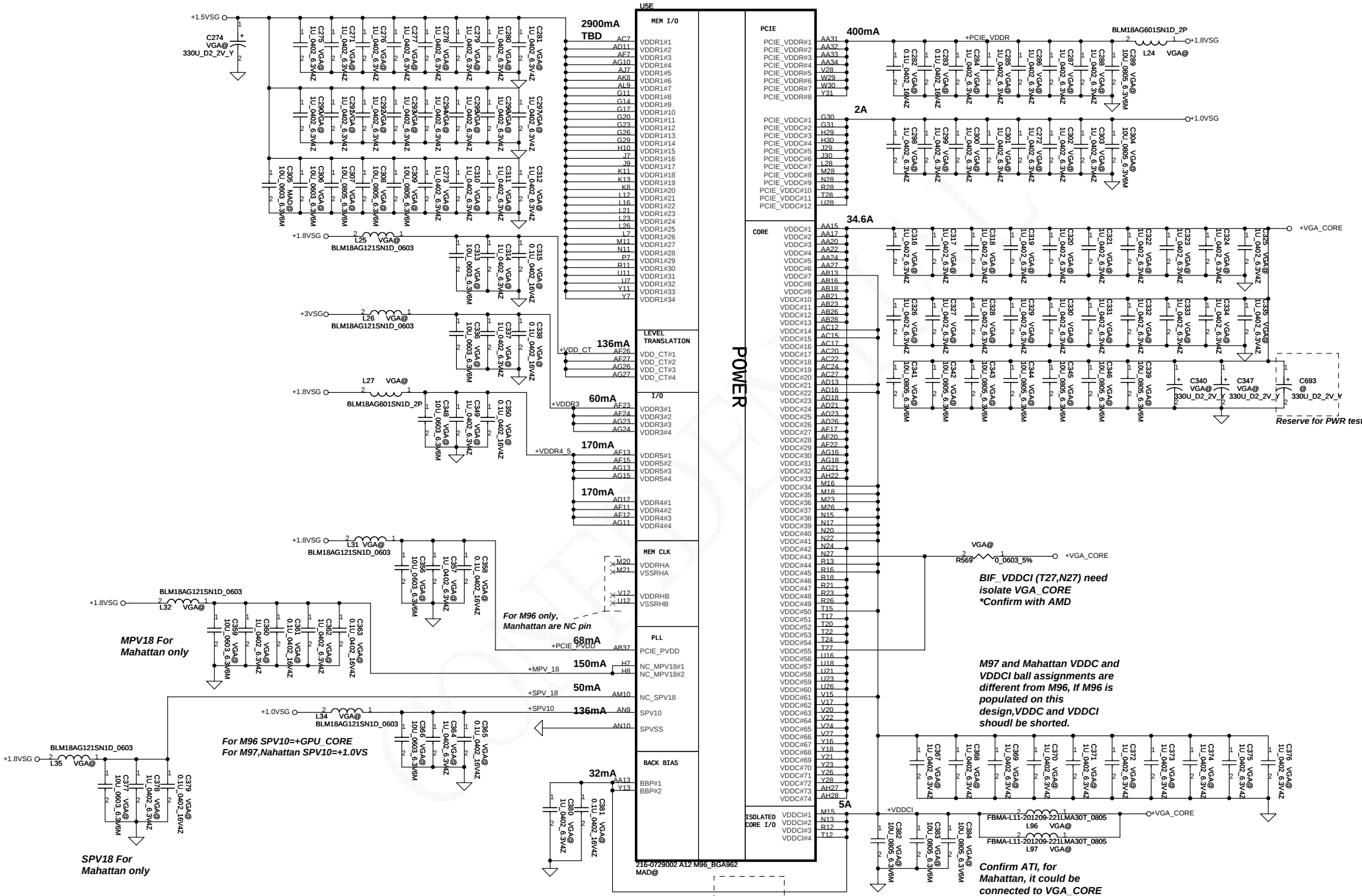


***Park only support single channel
memory (channel B only)***

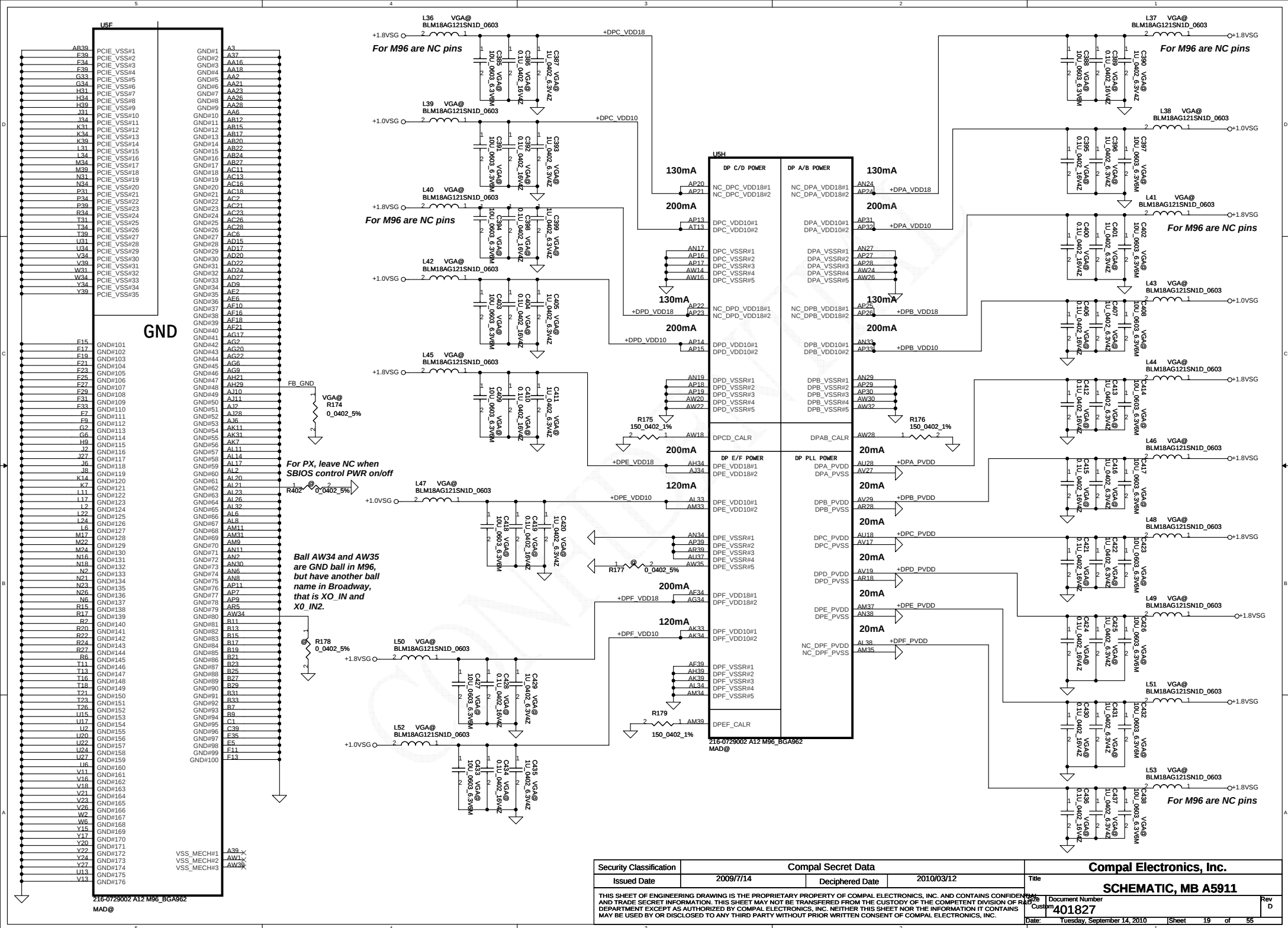


	M96	Broadway
R168	4.7k Ohm SD028470180	18k Ohm SD0281800280
R166	6 Ohm SD028000000	680 Ohm SD028680000
R163	4.7k Ohm SD028470180	DNI
C270	1000 pF SF074102K00	68 pF SFA1680180

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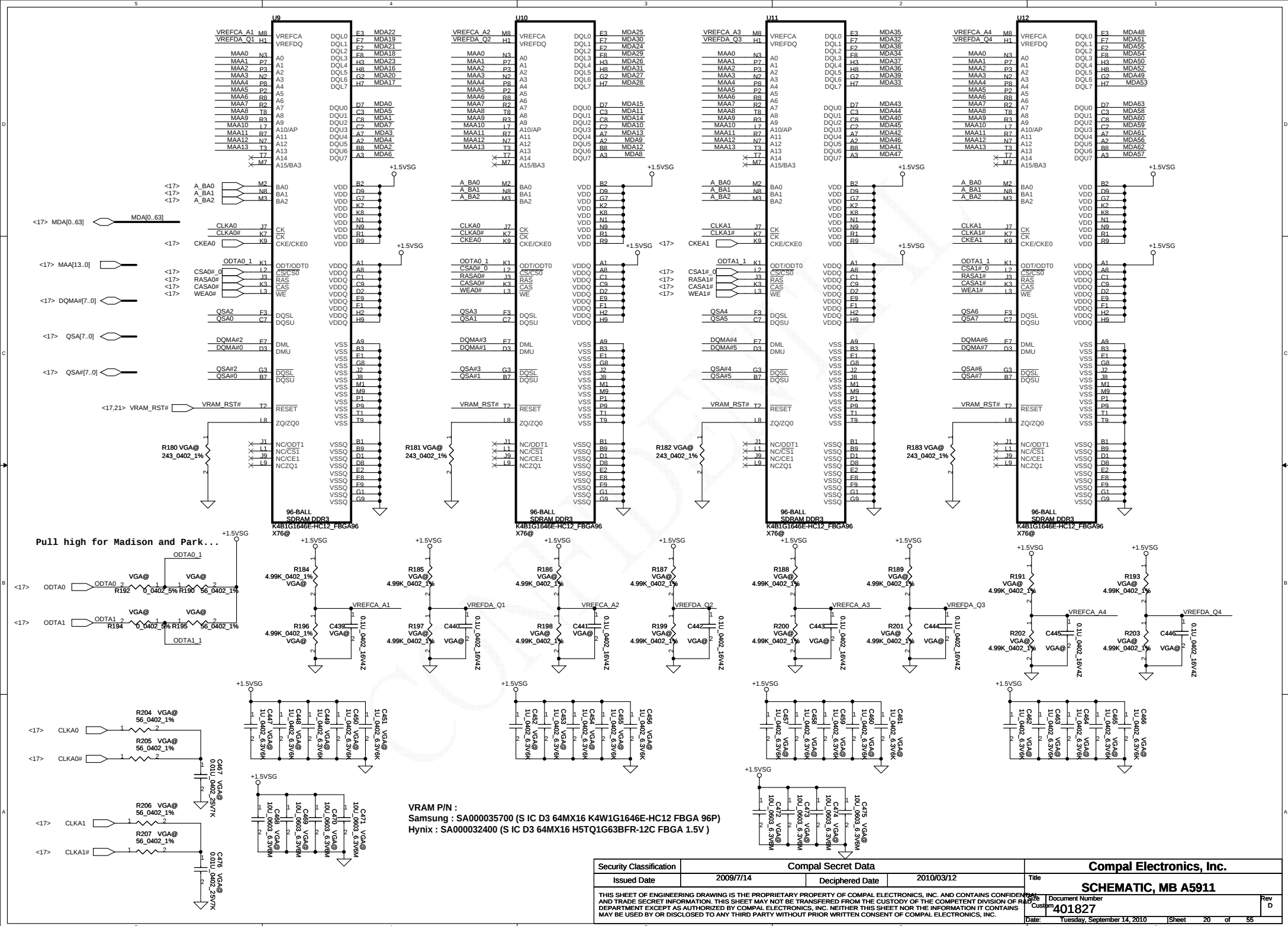


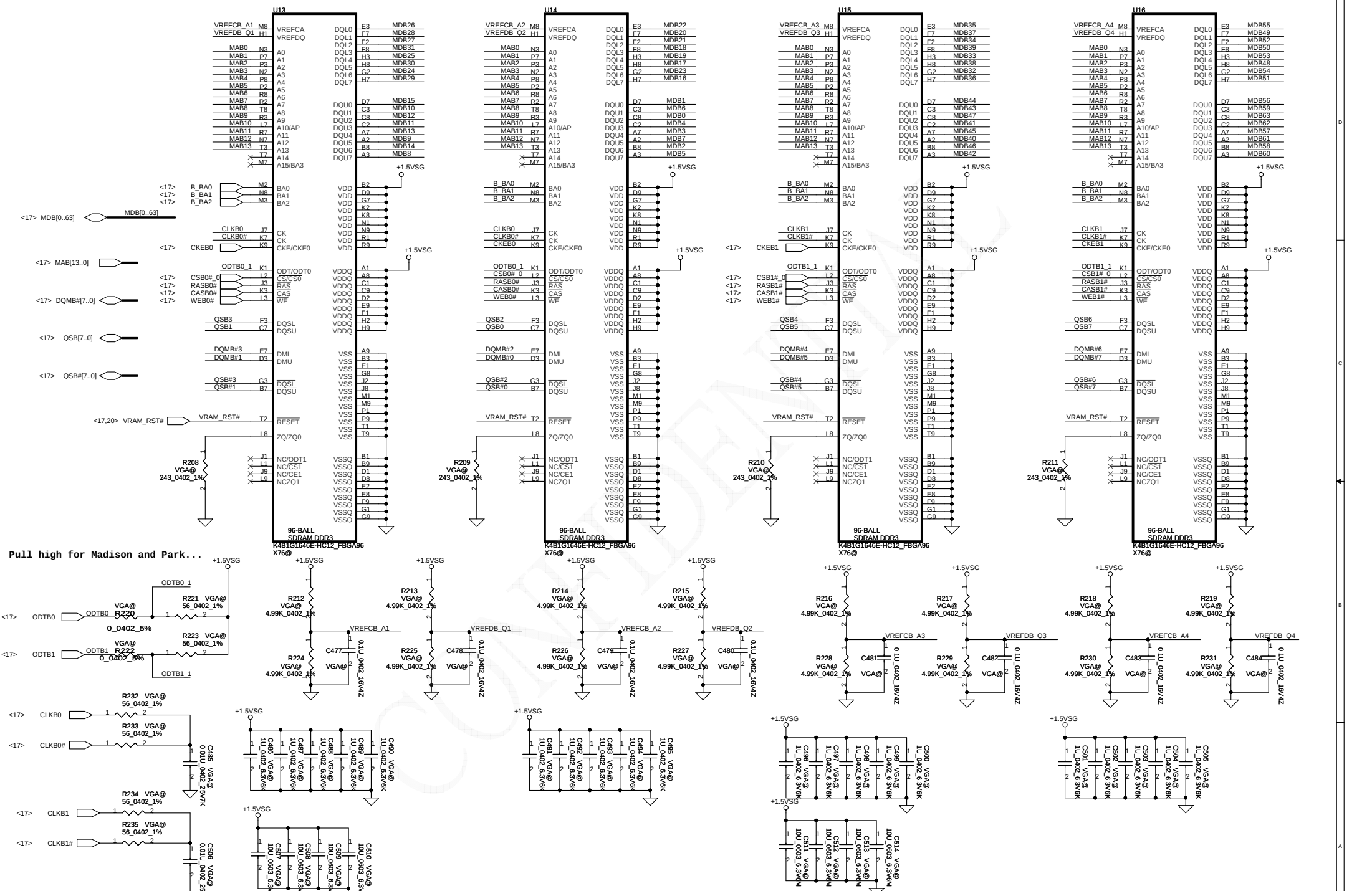
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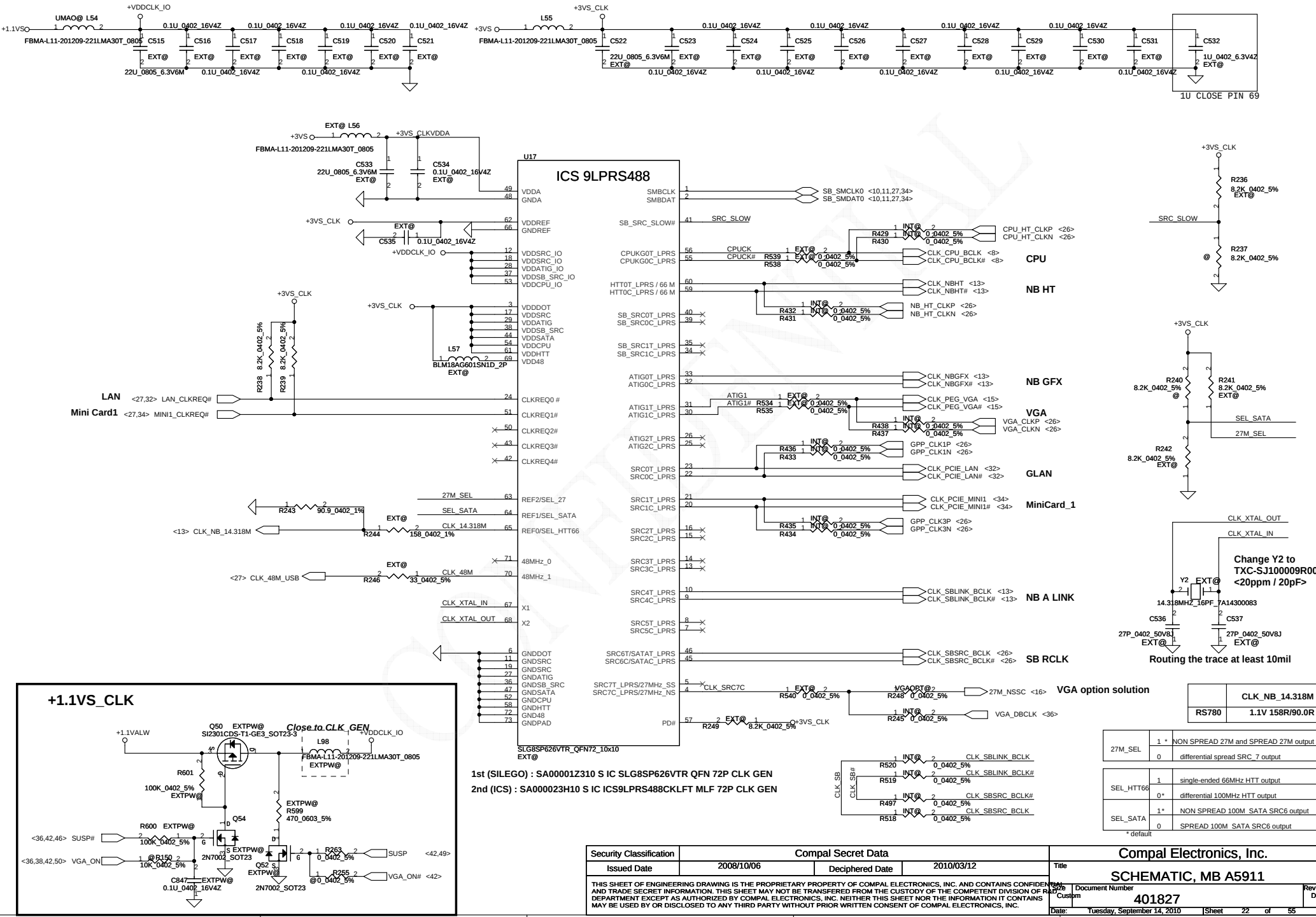


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Part No.	Document Number	Rev D	
ENG: RMD	Customer	401827	
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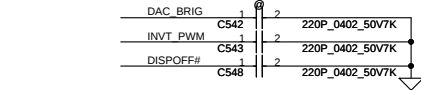
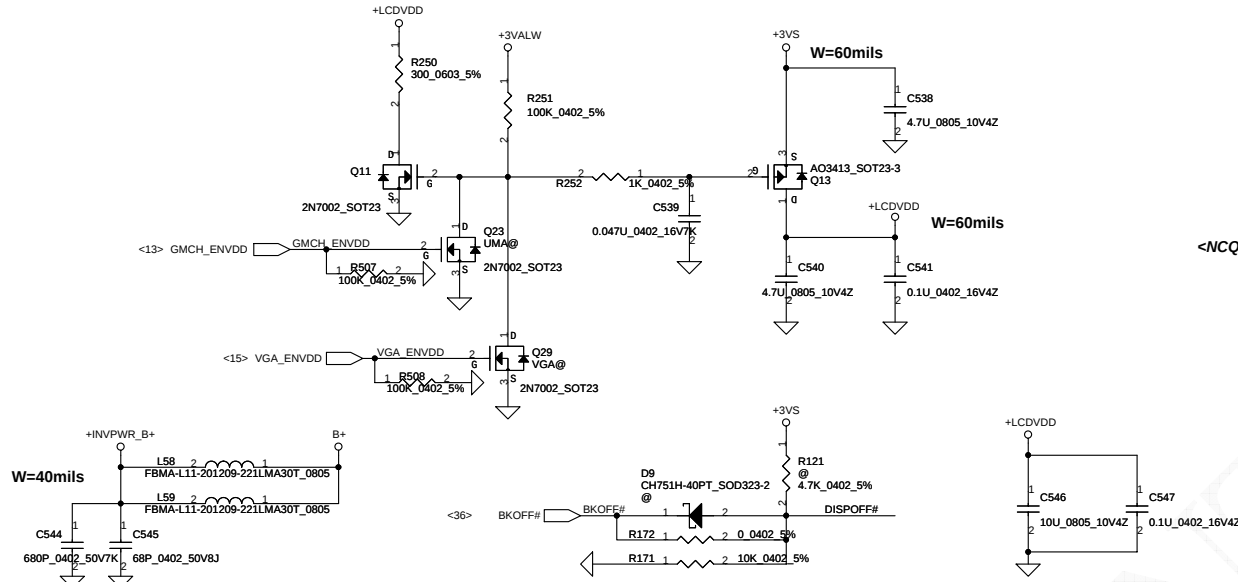




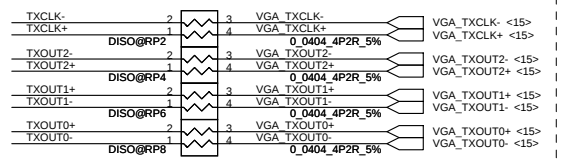


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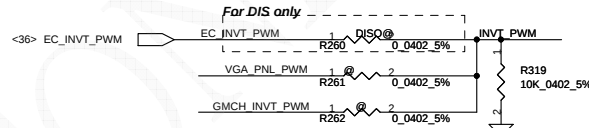
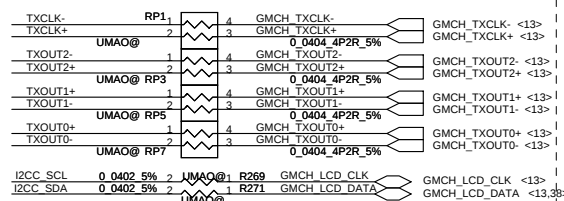
LCD POWER CIRCUIT



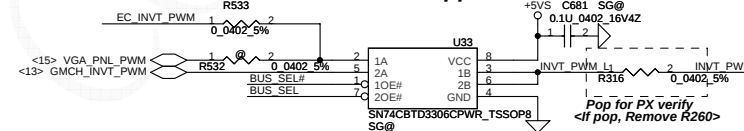
VGA ONLY



UMA ONLY

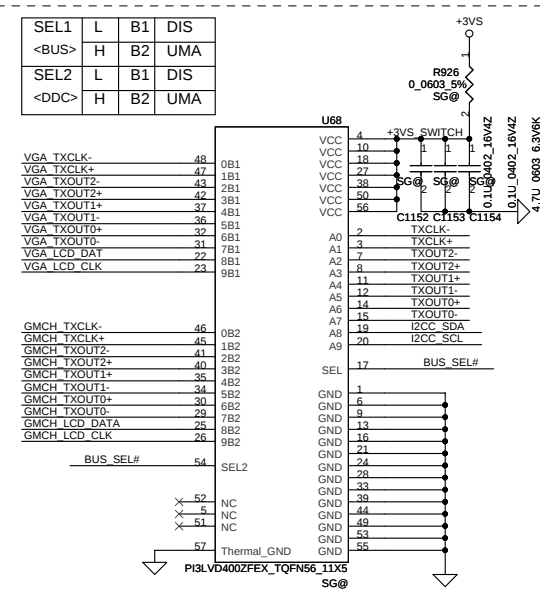
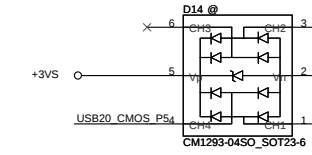
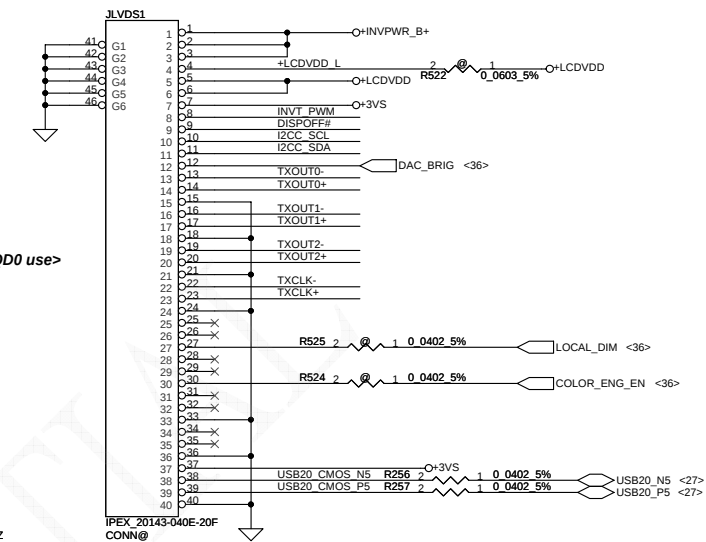


PX & VB support

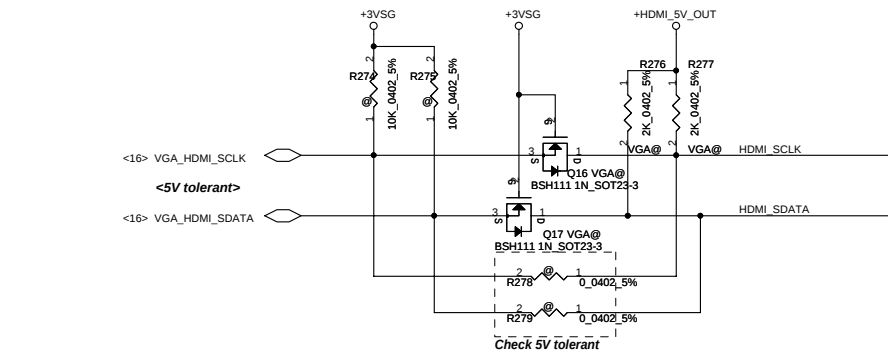


10E#	L	B1	DIS
	H	Z	
20E#	L	B1	UMA
	H	Z	

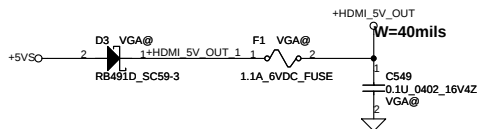
LCD/LED PANEL Conn.



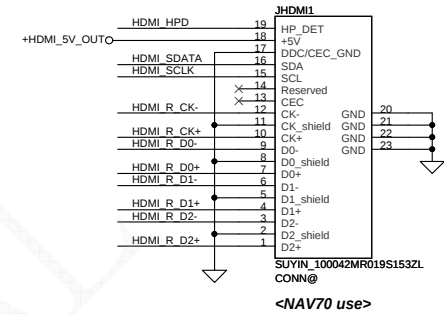
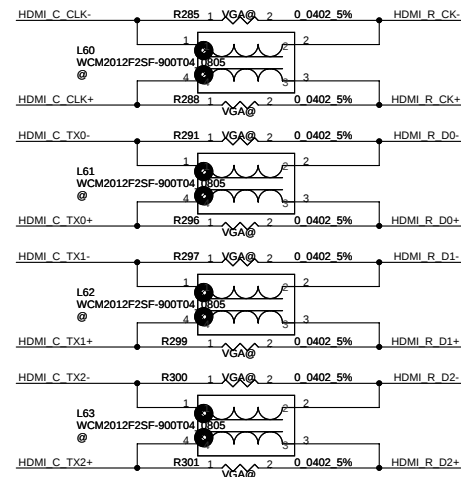
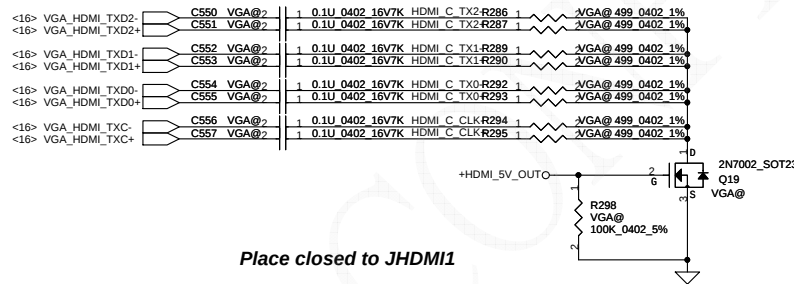
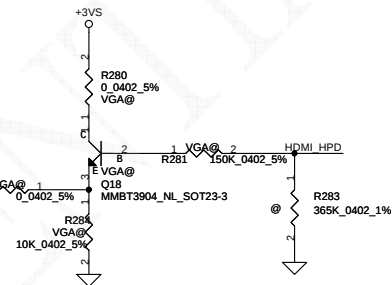
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Place closed to JHDMI1

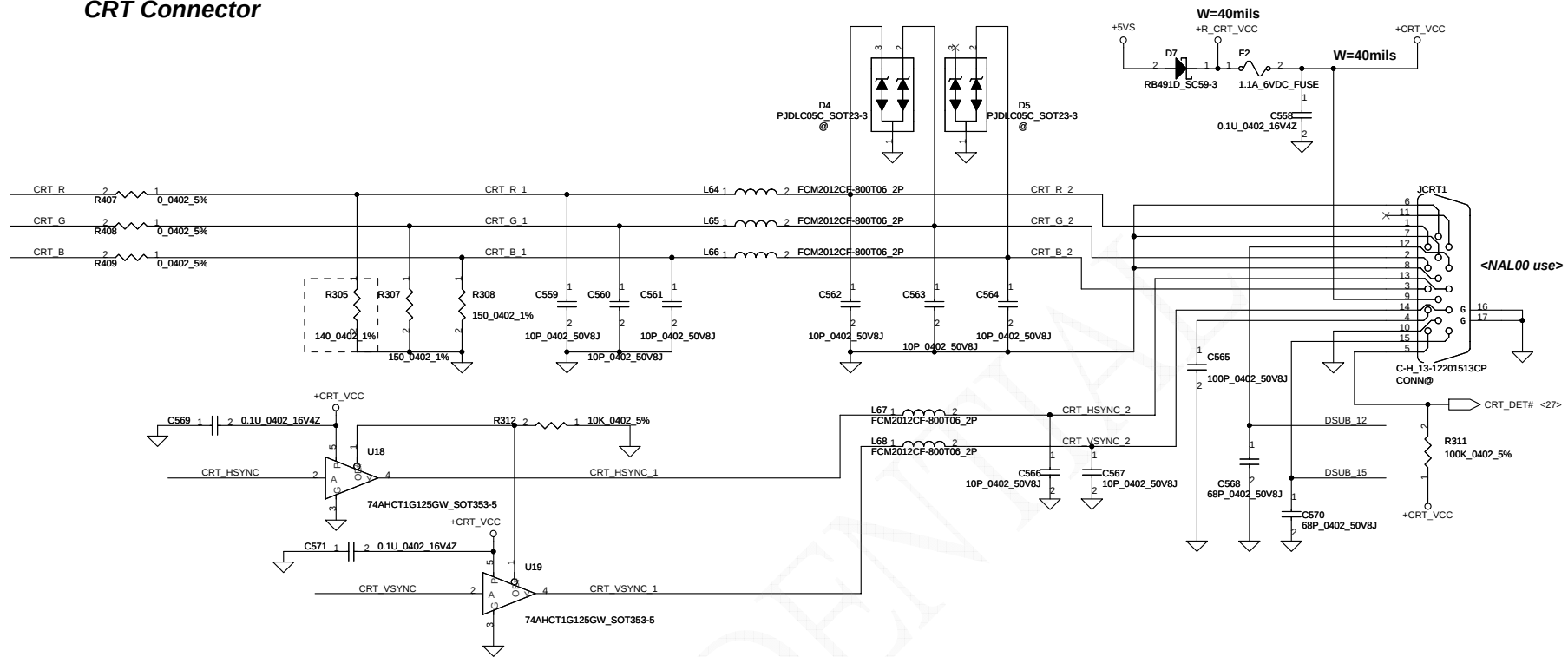


<16,27> VGA_HDMI_DET



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CRT Connector

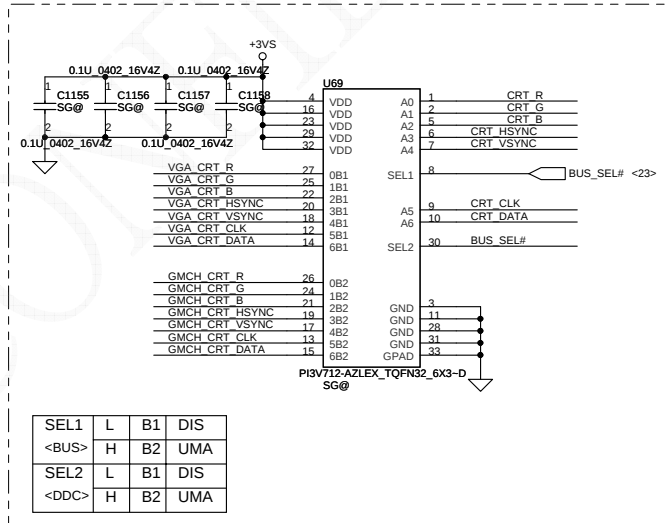


For UMA Only

<13> GMCH_CRT_R	GMCH_CRT_R	R266	2	UMA@	1	0.0402 5%	CRT_R
<13> GMCH_CRT_G	GMCH_CRT_G	R83	2	UMA@	1	0.0402 5%	CRT_G
<13> GMCH_CRT_B	GMCH_CRT_B	R268	2	UMA@	1	0.0402 5%	CRT_B
<13,14> GMCH_CRT_HSYNC	GMCH_CRT_HSYNC	R273	2	UMA@	1	0.0402 5%	CRT_HSYNC
<13,14> GMCH_CRT_VSYNC	GMCH_CRT_VSYNC	R267	2	UMA@	1	0.0402 5%	CRT_VSYNC
<13> GMCH_CRT_DATA	GMCH_CRT_DATA	R410	2	UMA@	1	0.0402 5%	CRT_DATA
<13> GMCH_CRT_CLK	GMCH_CRT_CLK	R406	2	UMA@	1	0.0402 5%	CRT_CLK

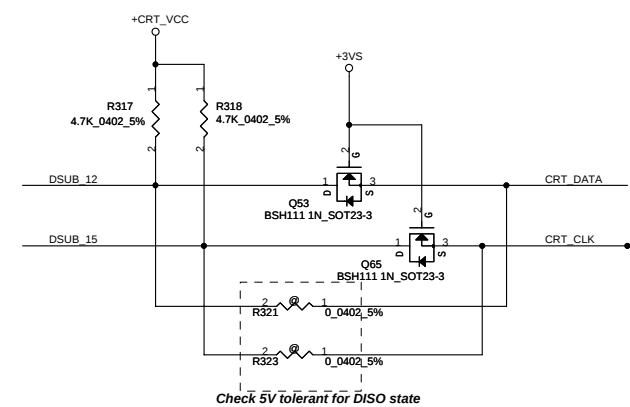
For VGA Only

<16> VGA_CRT_R	VGA_CRT_R	R306	2	DISO@	1	0.0402 5%	CRT_R
<16> VGA_CRT_G	VGA_CRT_G	R302	2	DISO@	1	0.0402 5%	CRT_G
<16> VGA_CRT_B	VGA_CRT_B	R304	2	DISO@	1	0.0402 5%	CRT_B
<16> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R303	2	DISO@	1	0.0402 5%	CRT_HSYNC
<16> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R309	2	DISO@	1	0.0402 5%	CRT_VSYNC
<16> VGA_CRT_DATA	VGA_CRT_DATA	R411	2	DISO@	1	0.0402 5%	CRT_DATA
<16> VGA_CRT_CLK	VGA_CRT_CLK	R412	2	DISO@	1	0.0402 5%	CRT_CLK



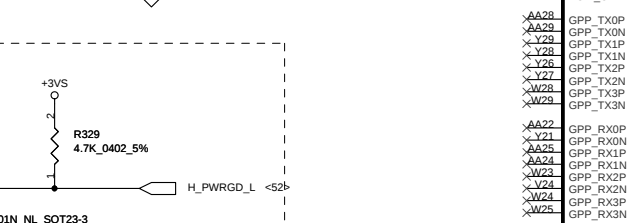
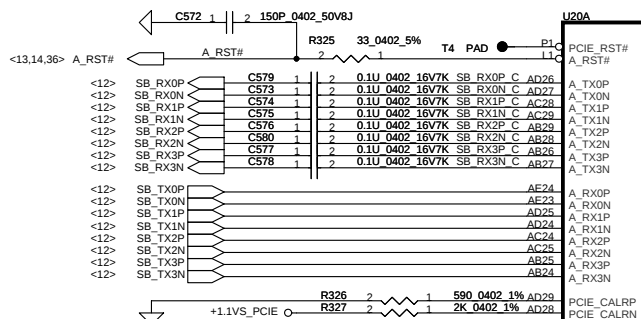
SEL1	L	B1	DIS
<BUS>	H	B2	UMA
SEL2	L	B1	DIS
<DDC>	H	B2	UMA

Close to Conn side



Check 5V Tolerant for DISO state

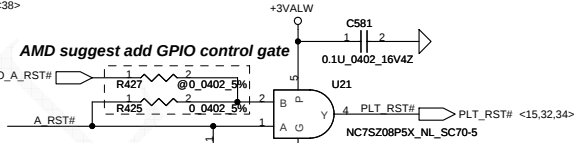
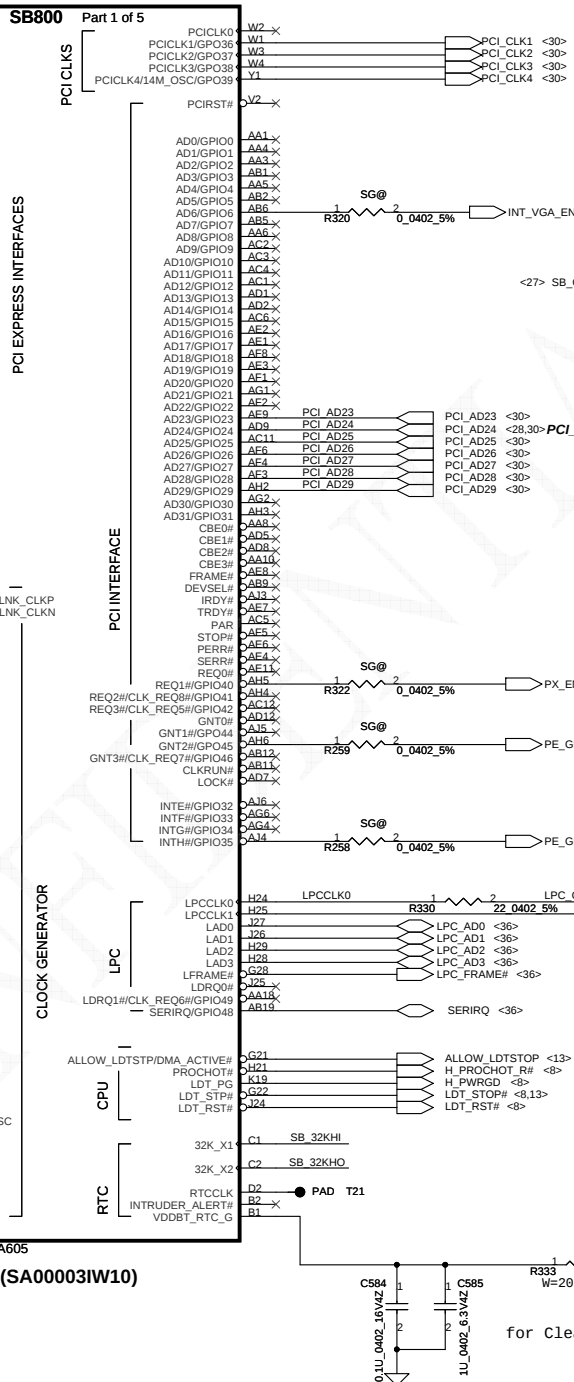
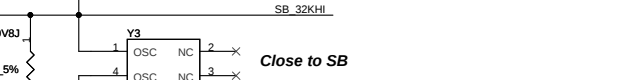
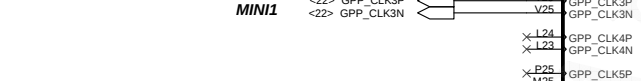
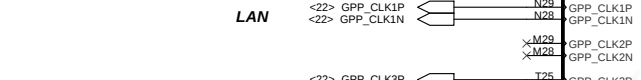
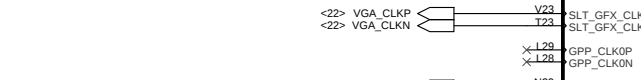
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level shift to ISL6265

ISL6265 PWROK input, TTL level: 0.8V~2.0V

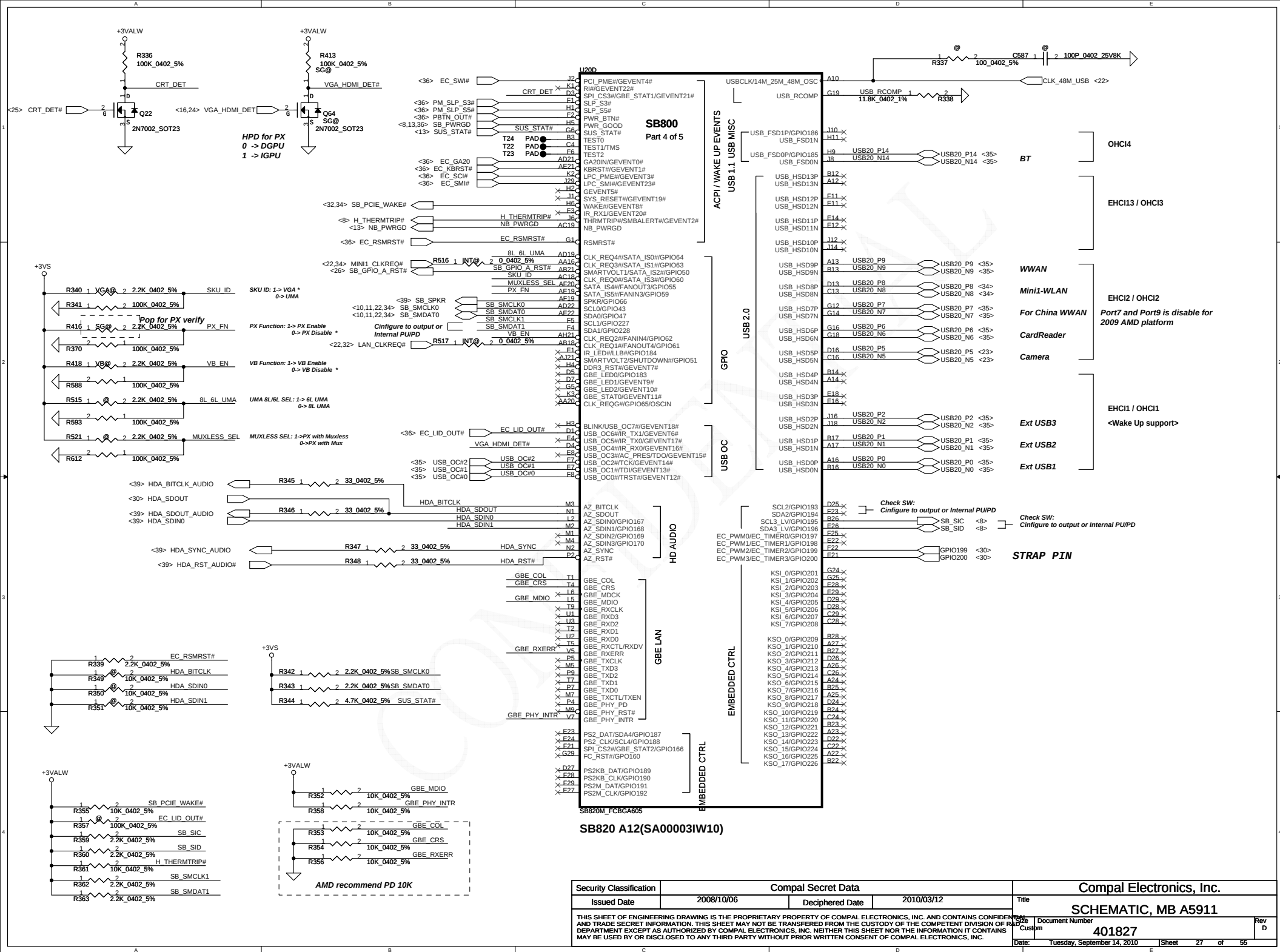
When this pin is high, the SVI interface is active and I2C protocol is running. While this pin is low, the SVC, SVD, and VFIXEN input states determine the pre-PWROK metal VID or VFIX mode voltage. This pin must be low prior to the ISL6265 PGOOD output going high



Power Xpress Support

PE_GPIO0	VGA RESET,	H: Enable
PE_GPIO1	VGA PWR Enable,	H: Enable
PE_GPIO2	MODE Switch,	H: VGA, L: NB

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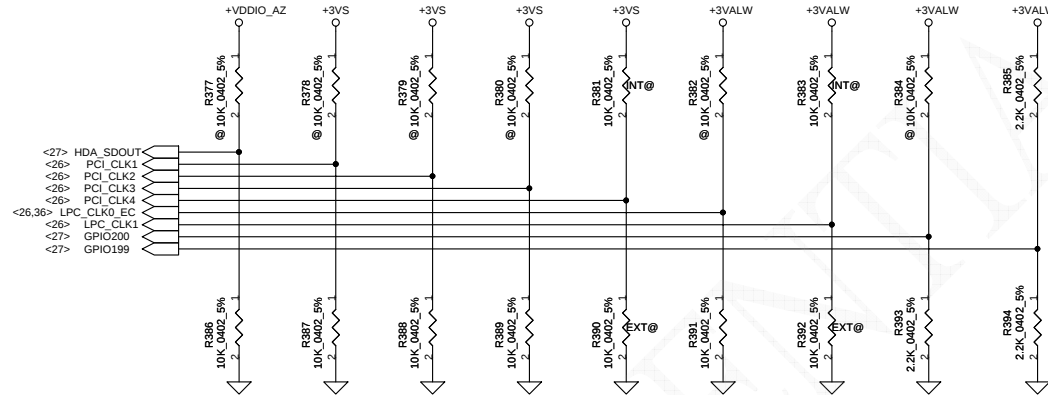


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REQUIRED STRAPS

Check Internal PU/PD

	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE GEN2	WATCHDOG TIMER ENABLE	USE DEBUG STRAP	CPU/HT CLK SEL Enable	EC ENABLE	CLOCKGEN ENABLE	H,H = Reserved H,L = SPI ROM L,H = LPC ROM (Default L,NC) L,L = FWH ROM	
PULL LOW	Performance MODE	FORCE PCIE GEN1	WATCHDOG TIMER DISABLE	IGNORE DEBUG STRAP	CPU/HT CLK SEL Disable	EC DISABLE	CLOCKGEN DISABLE		
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT		



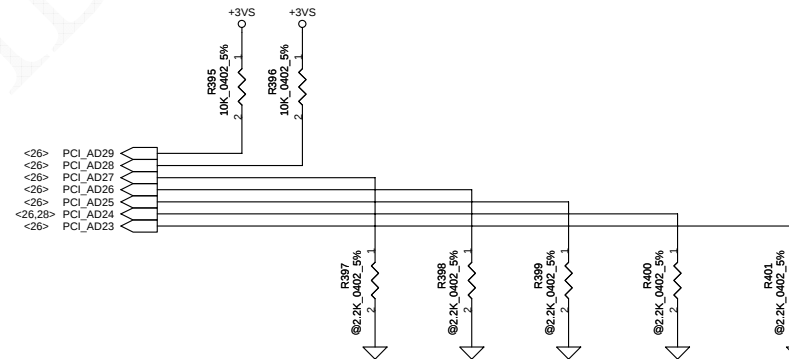
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

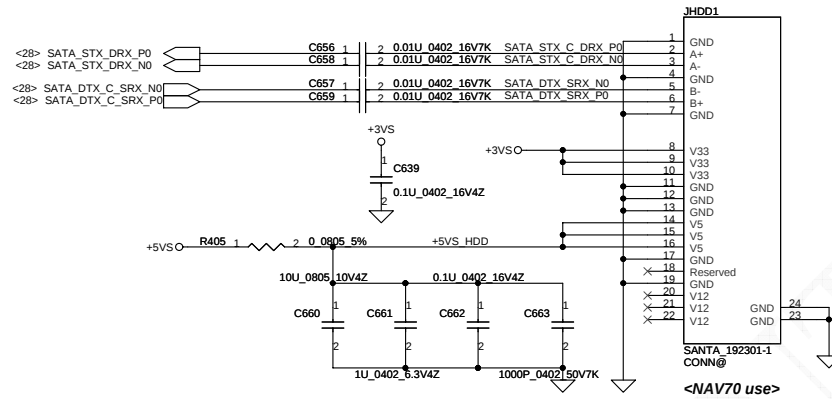
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL	DISABLE ILA AUTORUN	USE FC PLL	USE DEFAULT PCIE STRAPS	DISABLE PCI MEM BOOT
	DEFAULT	DEFAULT	DEFAULT	DEFAULT	DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

Check AD29,AD28 strap function

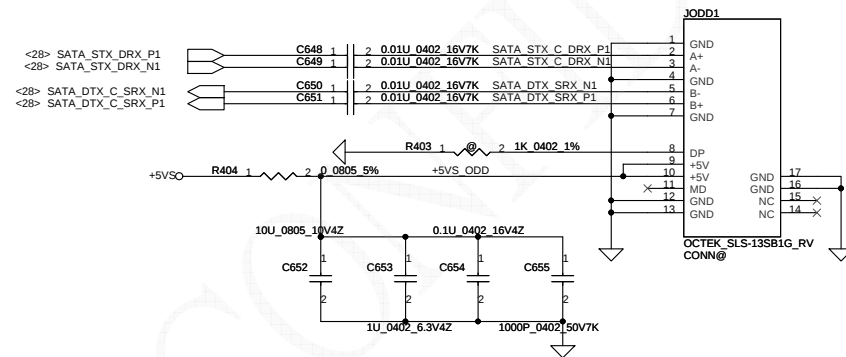
check default



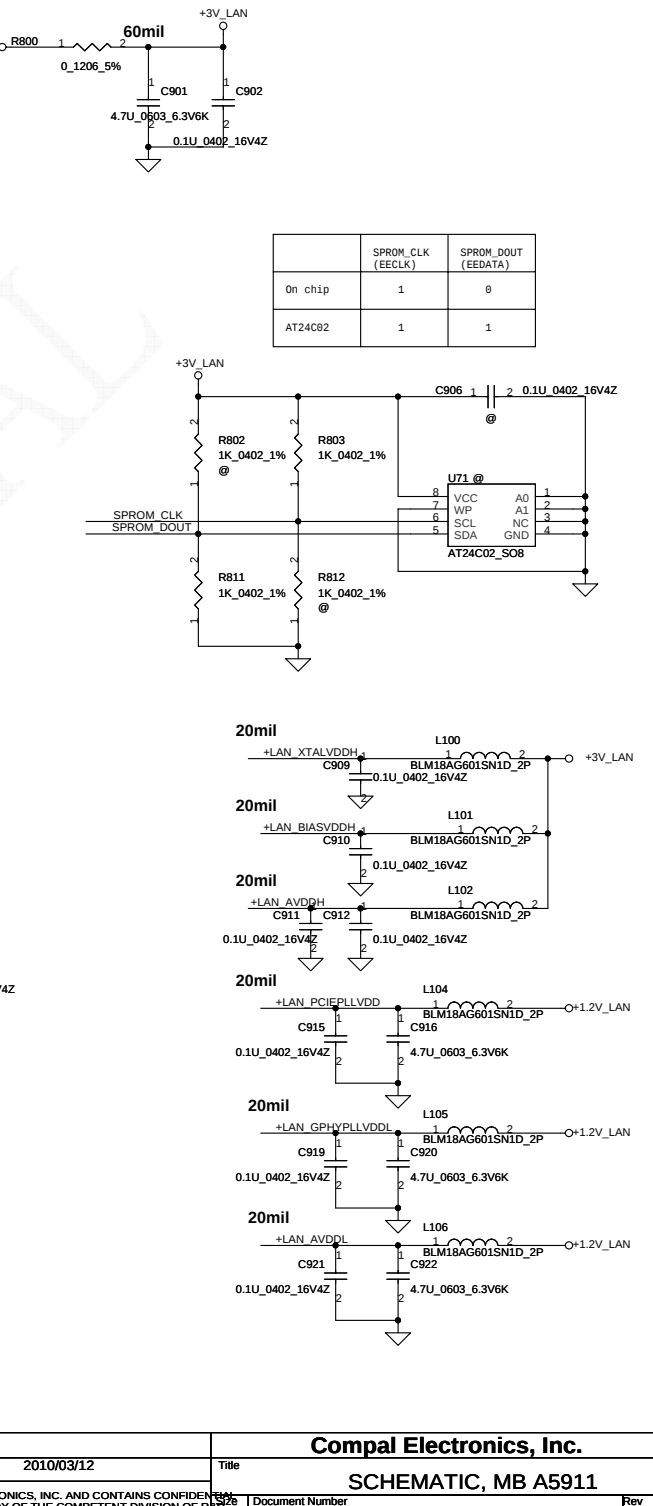
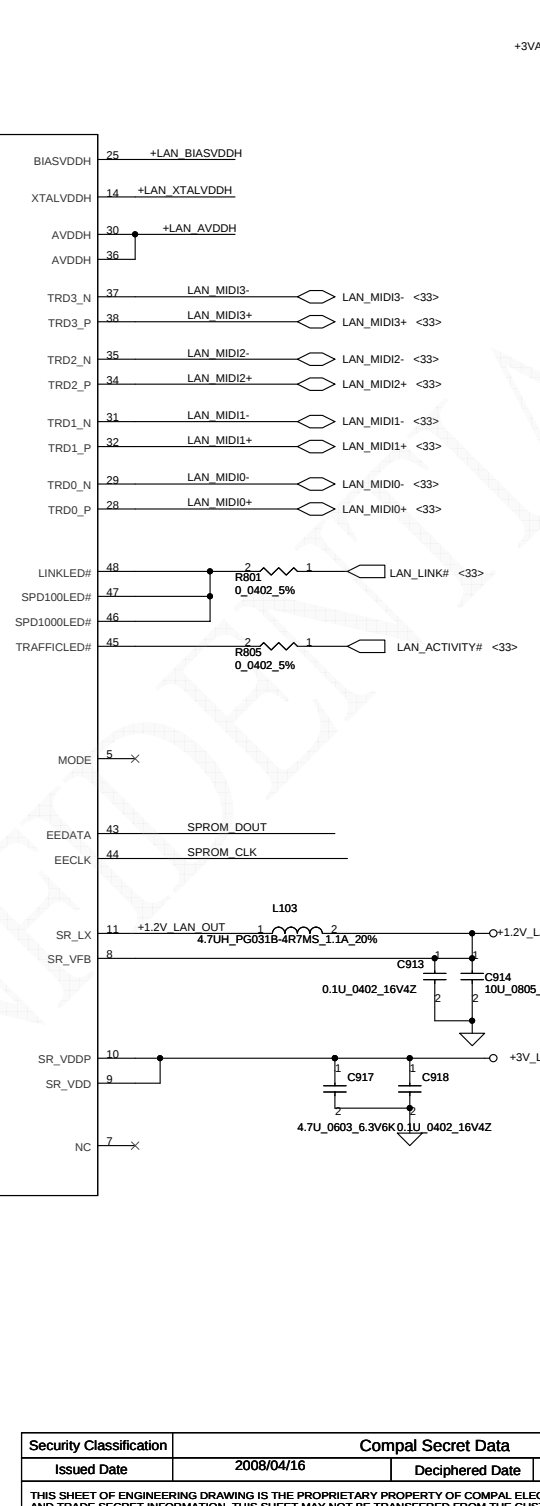
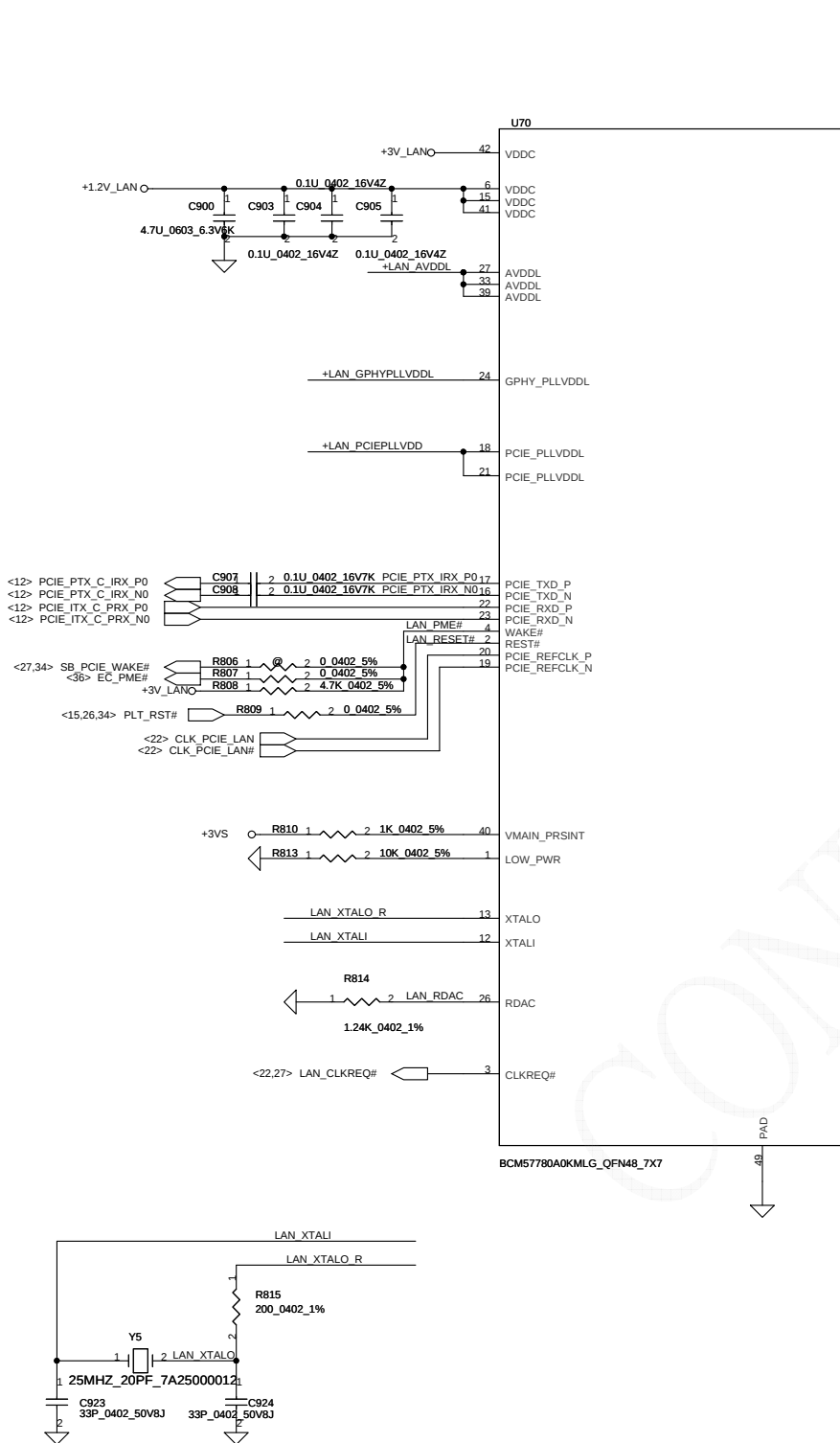
SATA HDD Conn.



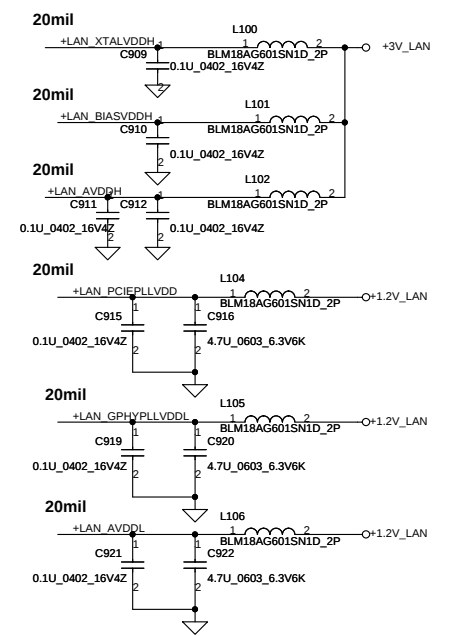
SATA ODD Conn.

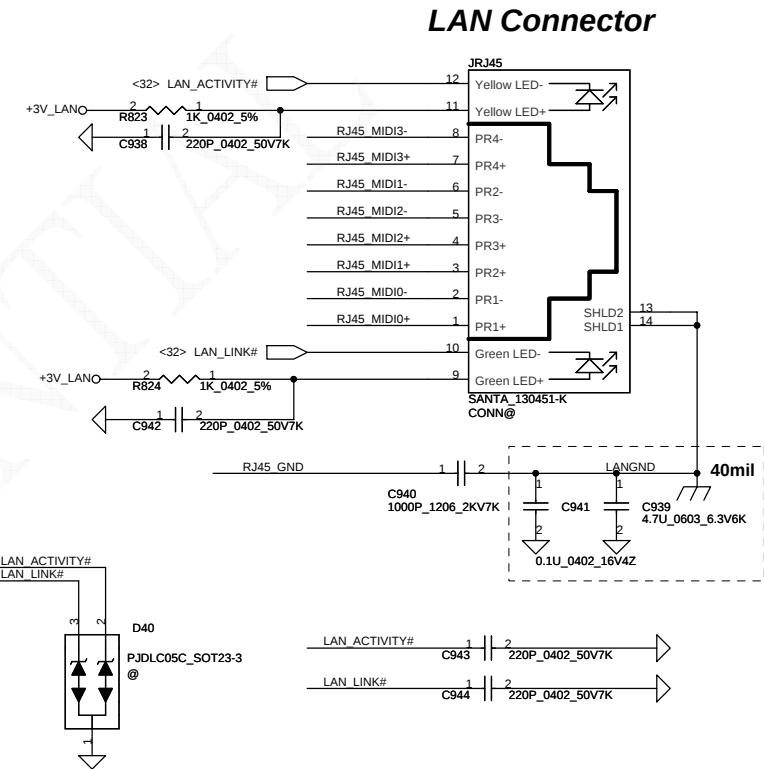
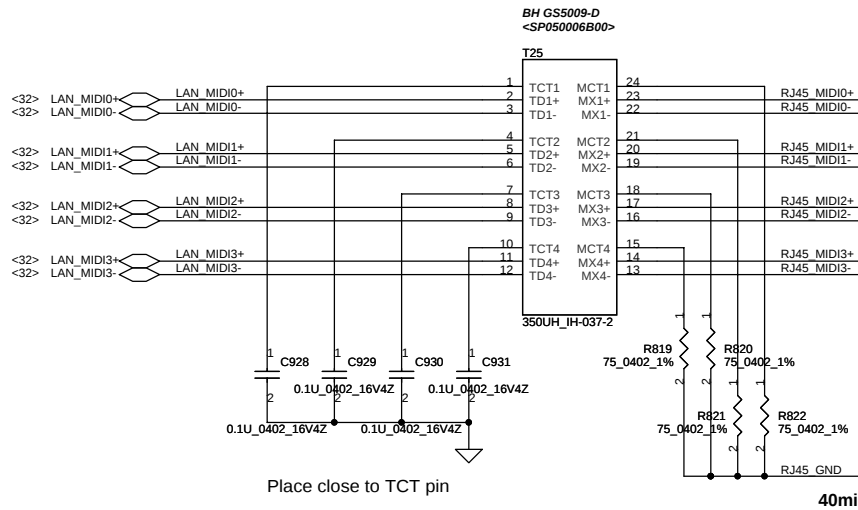


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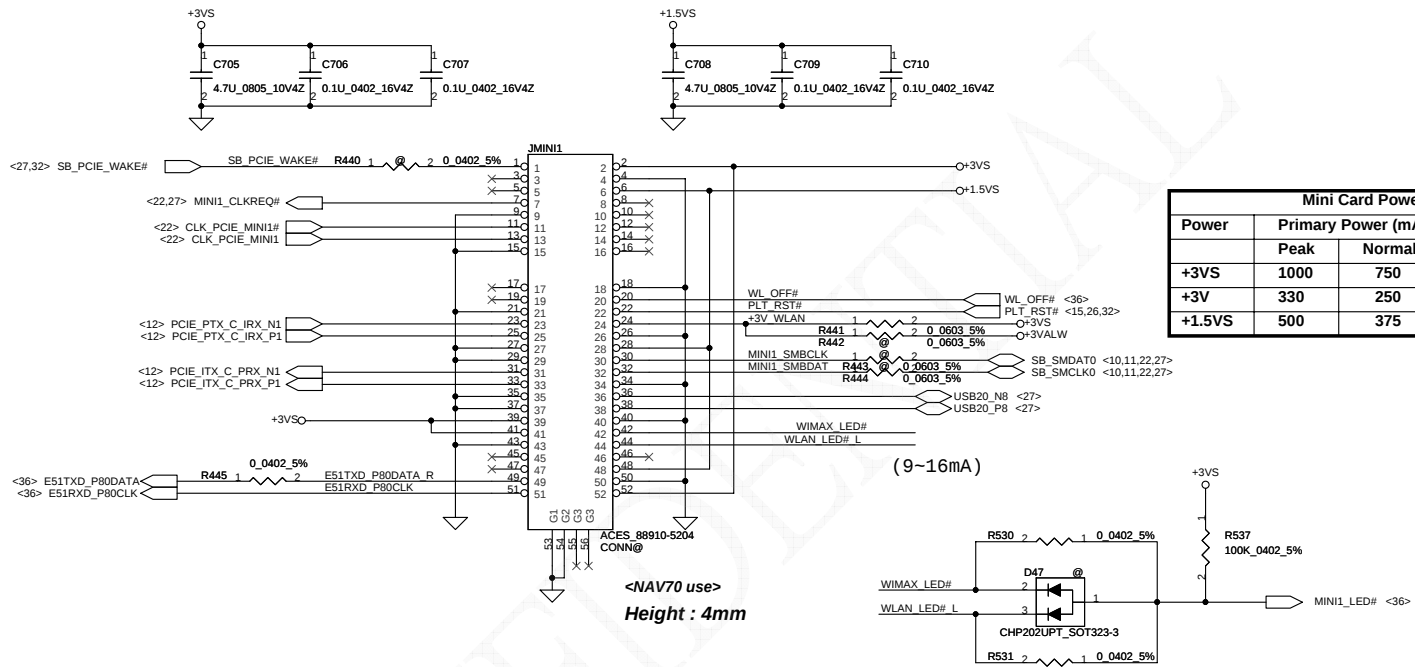
	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1



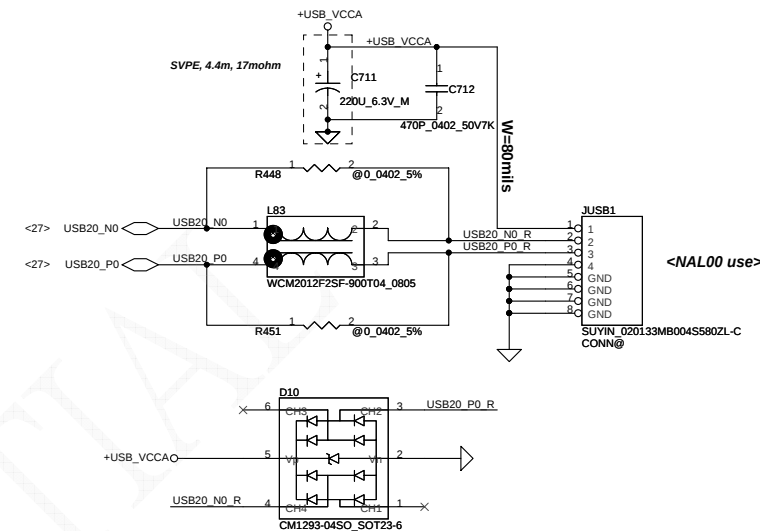
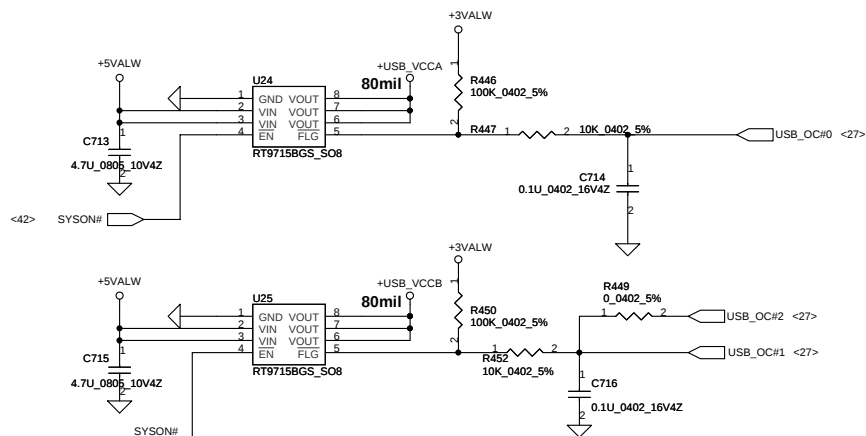


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Mini-Express Card for WLAN

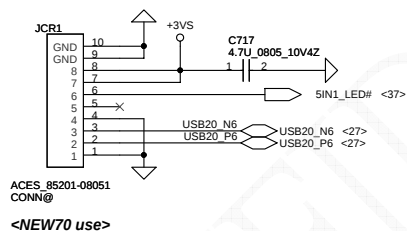
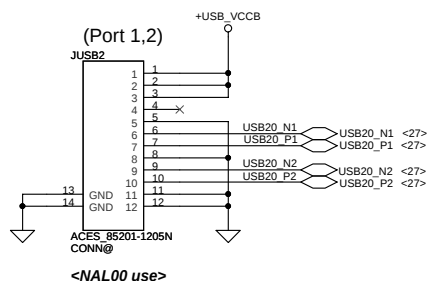


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

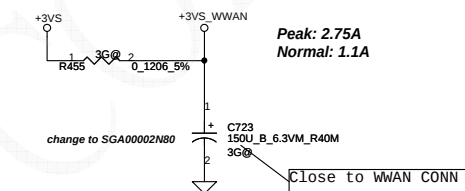
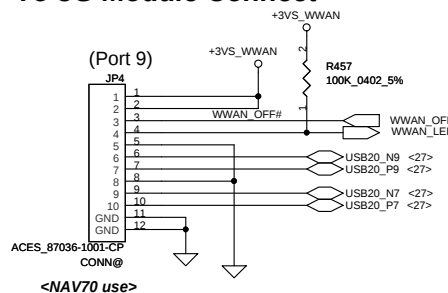


To USB/B Connector

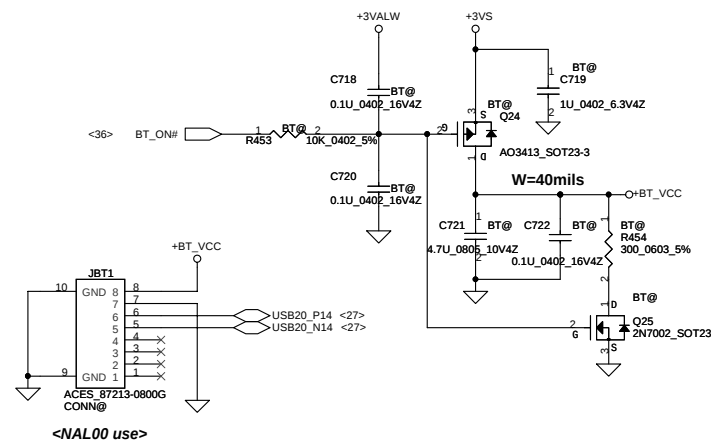
To CardReader/B Connector



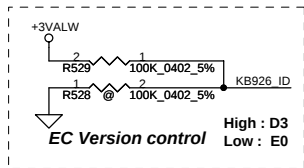
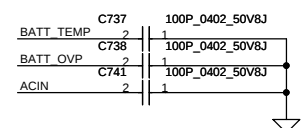
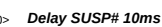
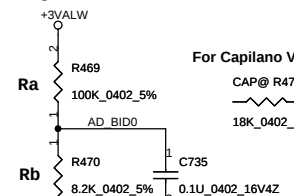
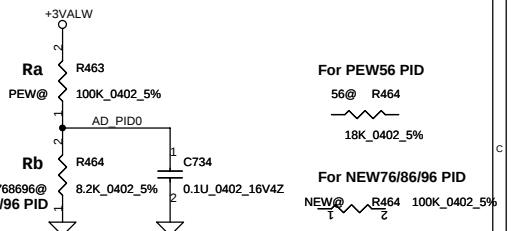
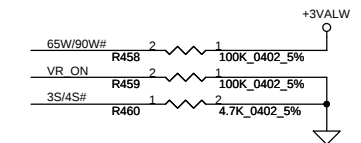
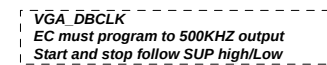
To 3G Module Connect



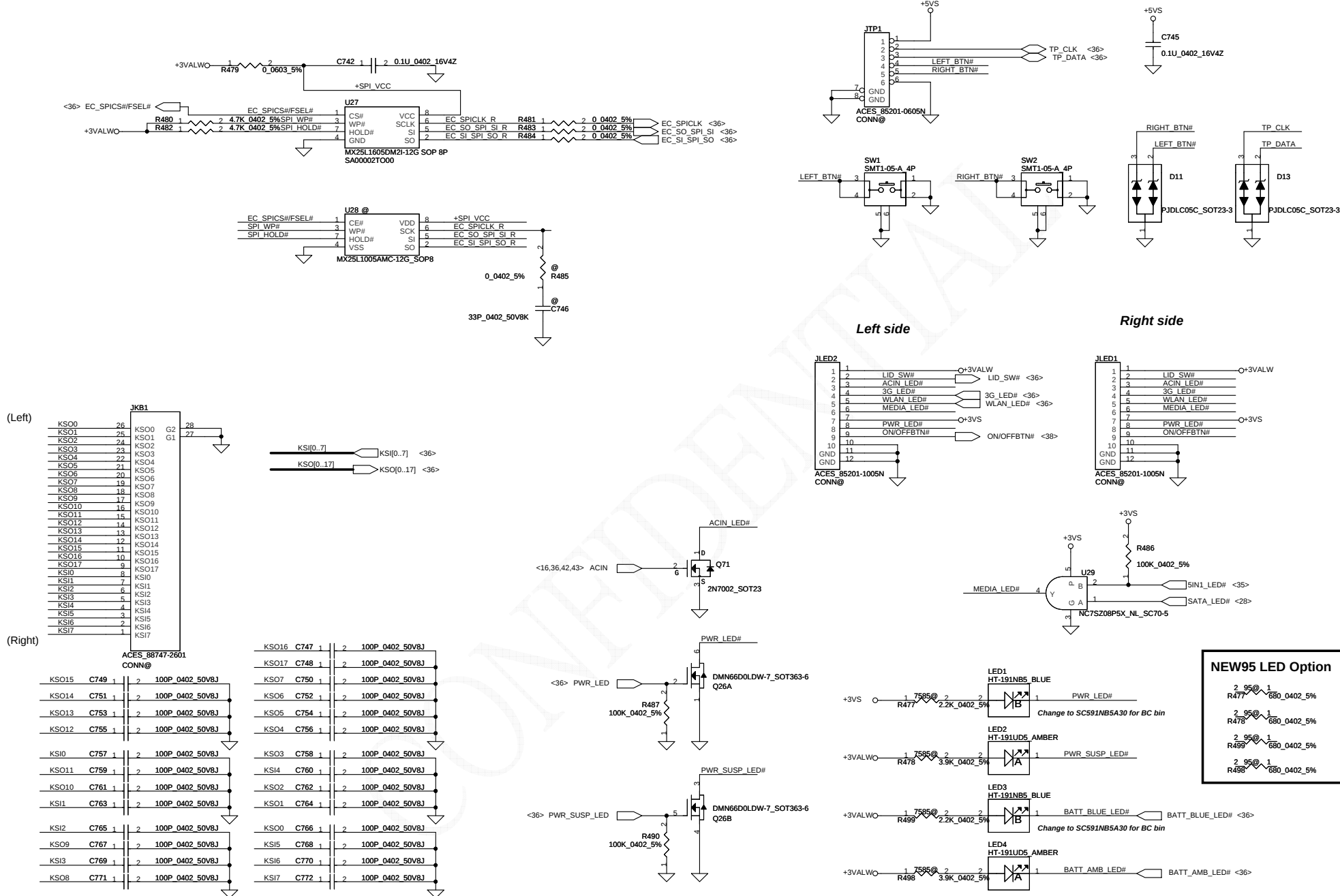
Bluetooth Conn.



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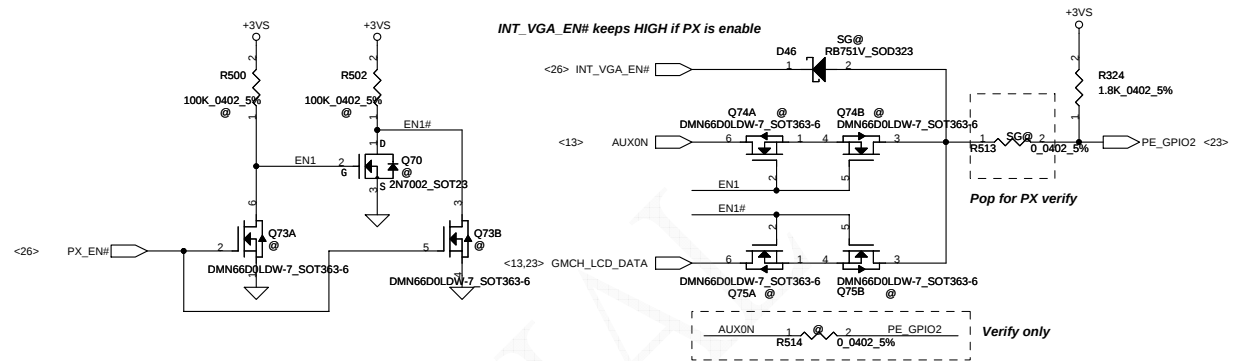
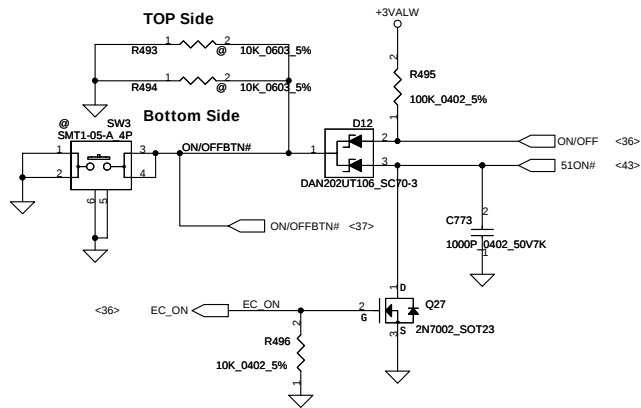
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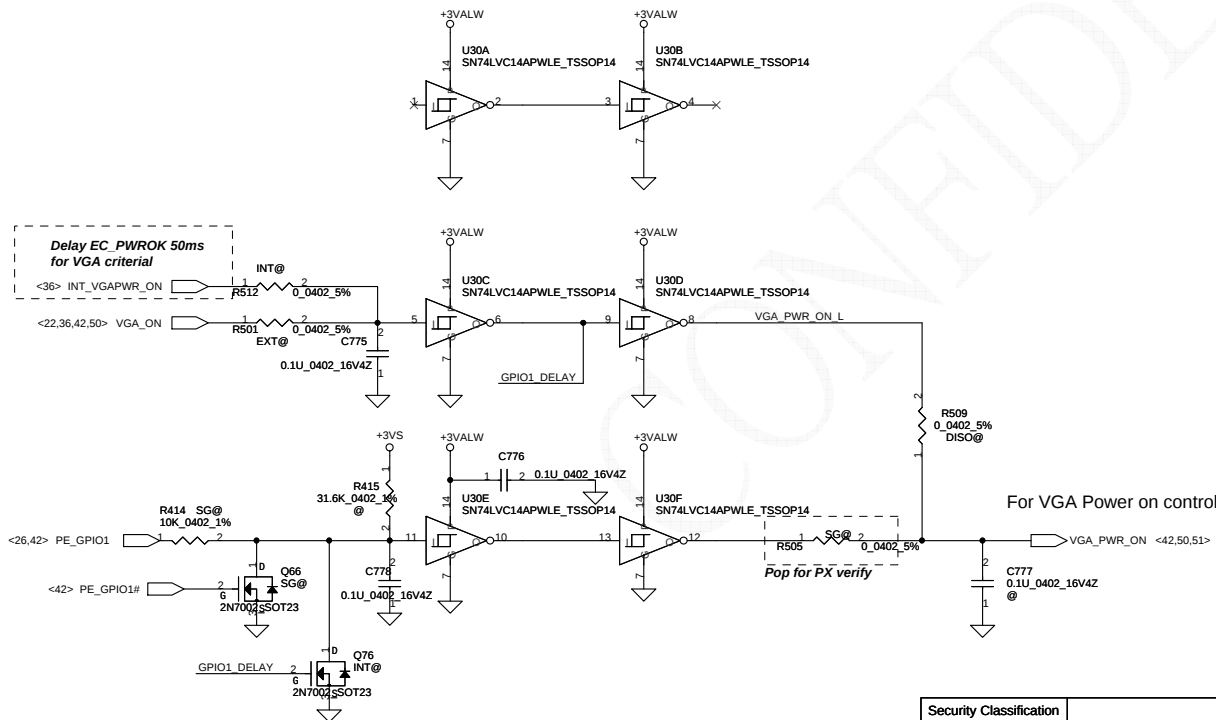
ON/OFF switch **Power Button**

PX MODE SELECT CONTROL <AMD Suggestion>

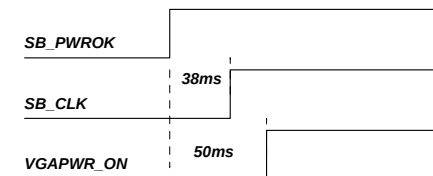


	PX_EN#	AUX0N EDP_DISABLED	I2C_DATA EDP_ENABLED	INT_VGA_EN#	DISPLAY OUTPUT
IGP only mode	1	X	X	0	IGP(LVDS,EDP,VGA,DP)
VGA only mode	1	X	X	1	VGA(LVDS,EDP,CRT,DP)
PX (MUXED)	0	0/1	0/1	1	VGA/IGP(CRT, LVDS, EDP); MXM(DP)
PX (MUXLESS)	0	X	X	0	IGP(LVDS,EDP,CRT,DP)

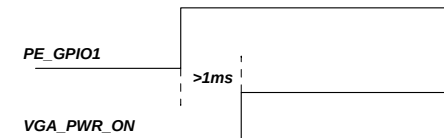
VGA Power ON Circuit



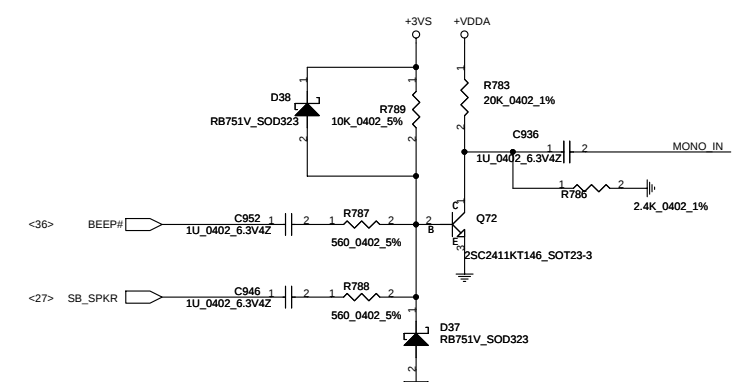
For PX sequence and internal clock mode, VGA PWR need ramp up after SB_CLK oscillate



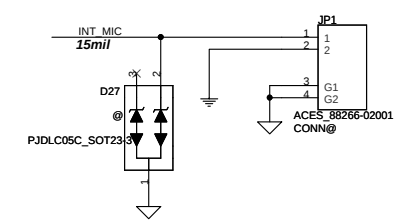
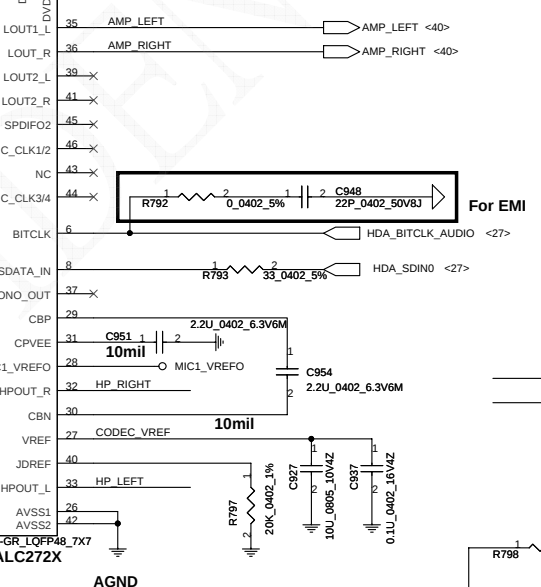
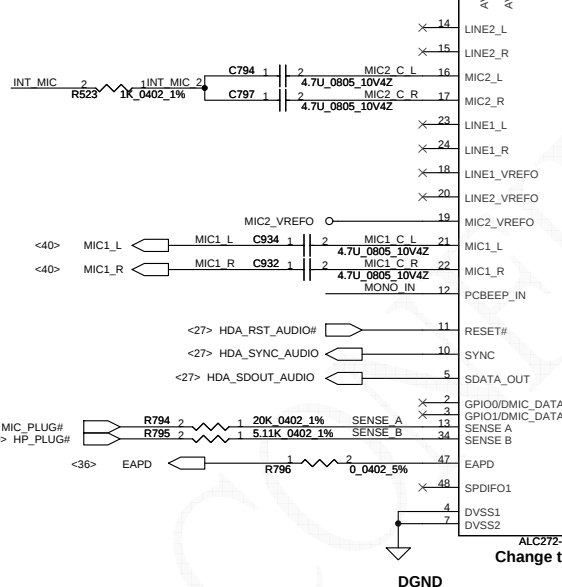
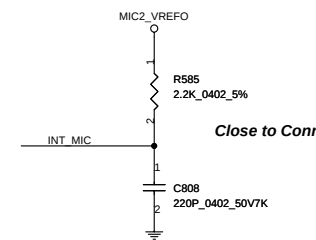
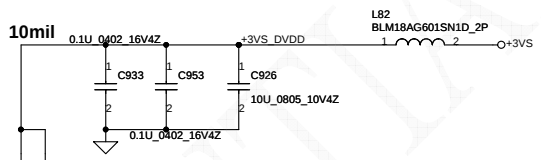
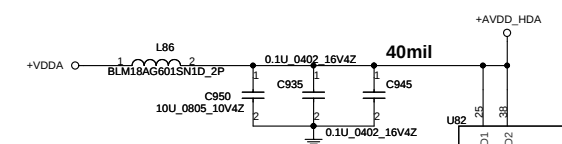
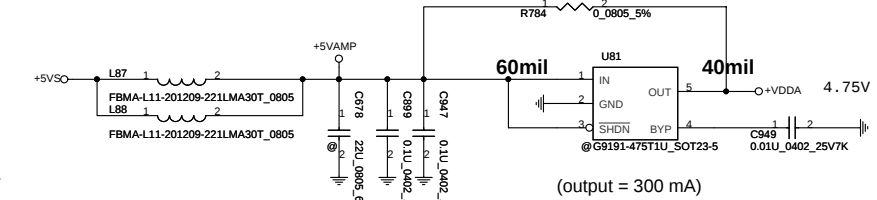
For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON



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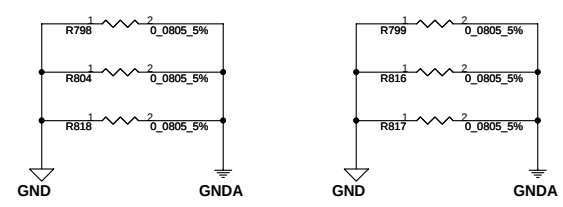


HD Audio Codec



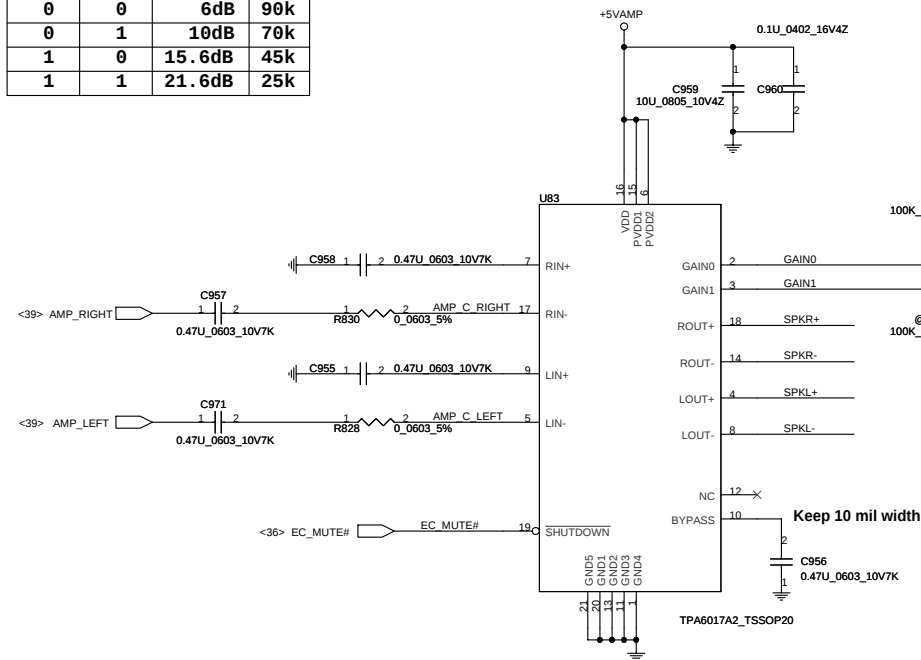
ALC272X			
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	LOUT2
	20K	PORT-B (PIN 21, 22)	MIC1
	10K	PORT-C (PIN 23, 24)	LINE1
	5.1K	PORT-D (PIN 35, 36)	LOUT1
SENSE B	39.2K	PORT-E (PIN 14, 15)	LINE2
	20K	PORT-F (PIN 16, 17)	MIC2
	10K	PORT-G (PIN 32, 33)	HP

Change to ALC272X

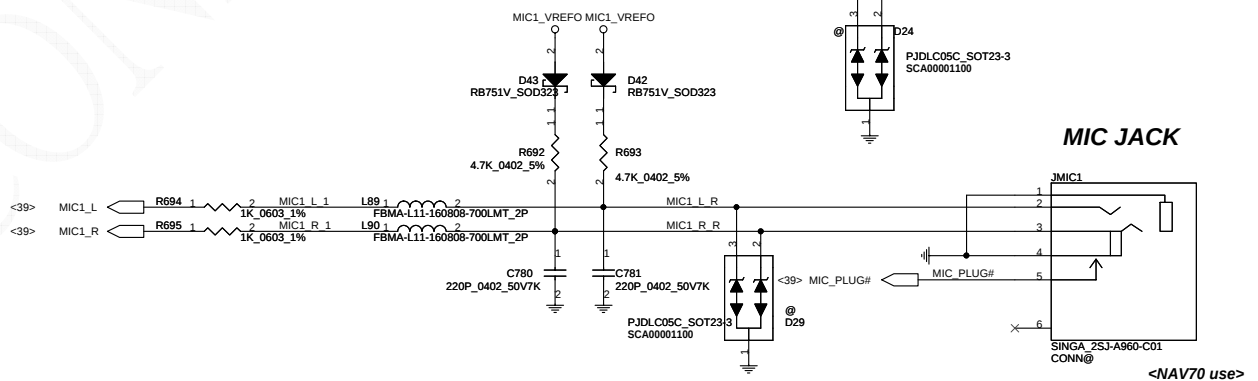
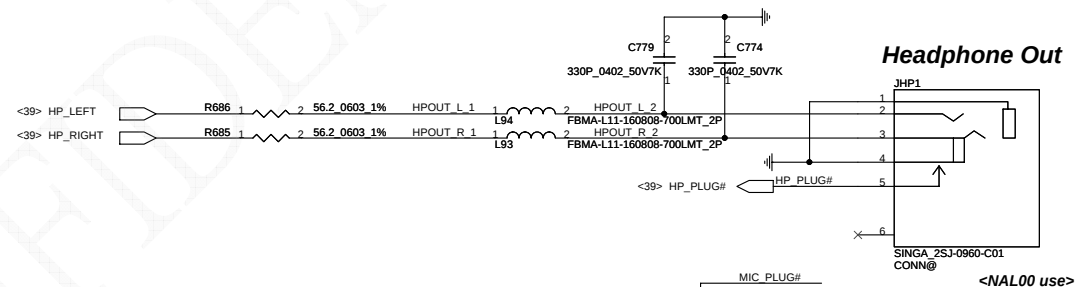
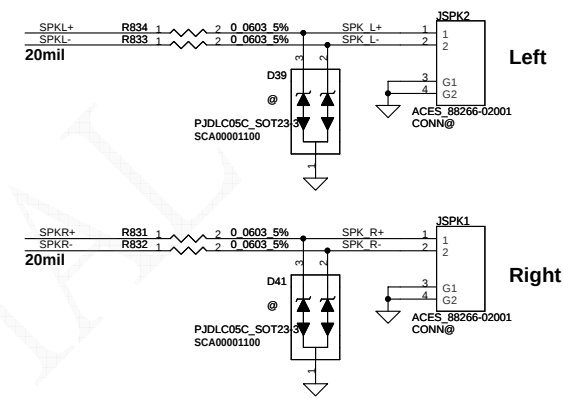


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55											

GAIN0	GAIN1	AV(inv)	Ri
0	0	6dB	90k
0	1	10dB	70k
1	0	15.6dB	45k
1	1	21.6dB	25k

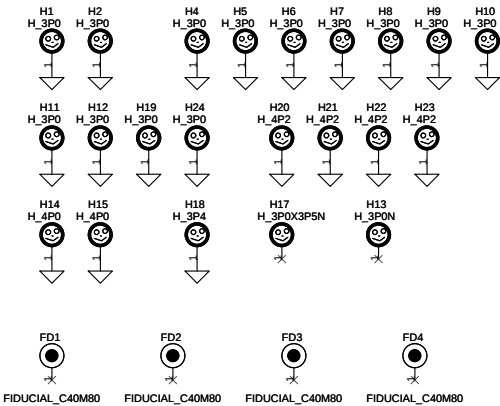
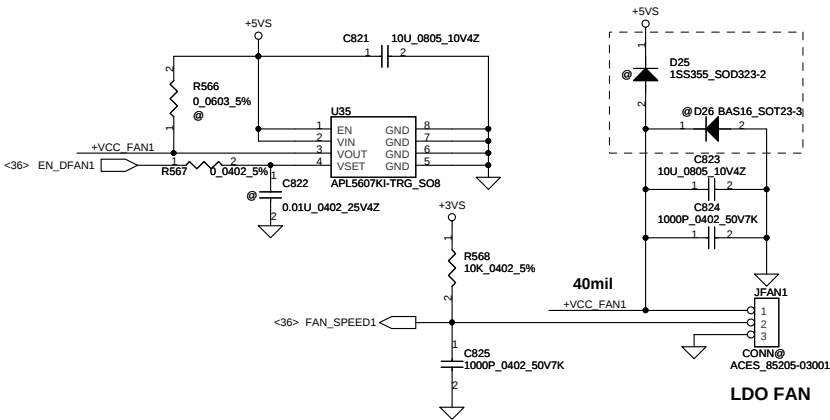


Int. Speaker Conn.



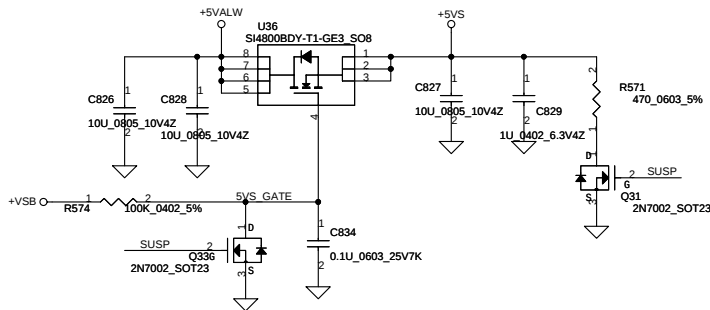
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FAN1 Conn

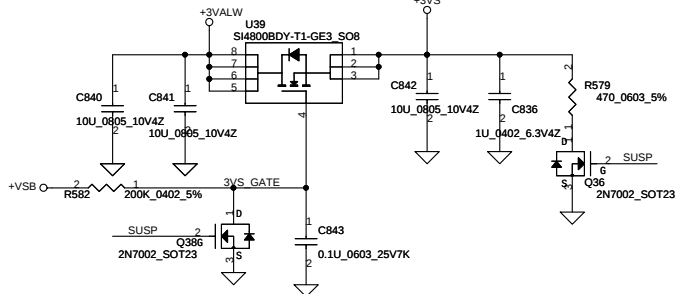


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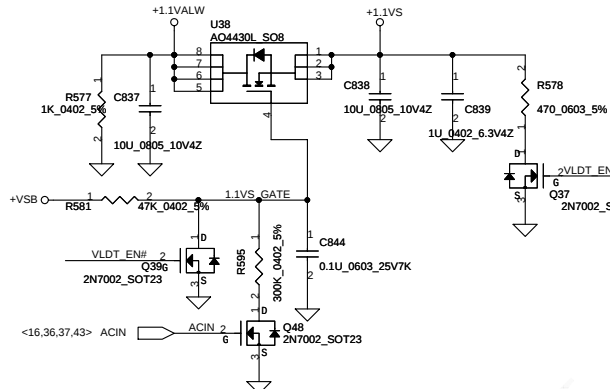
+5VALW TO +5VS



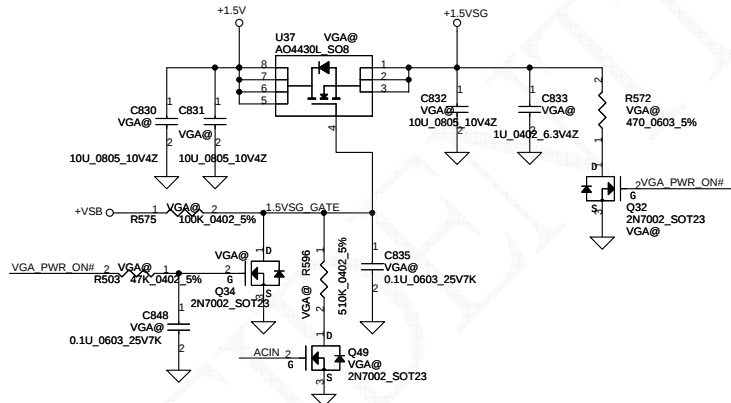
+3VALW TO +3VS



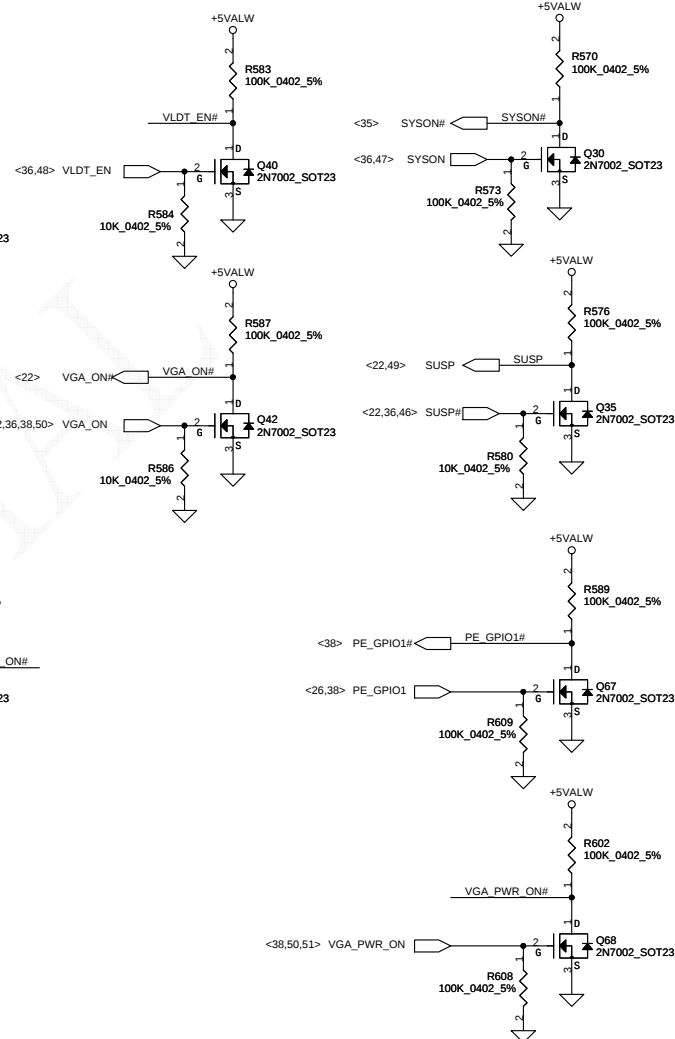
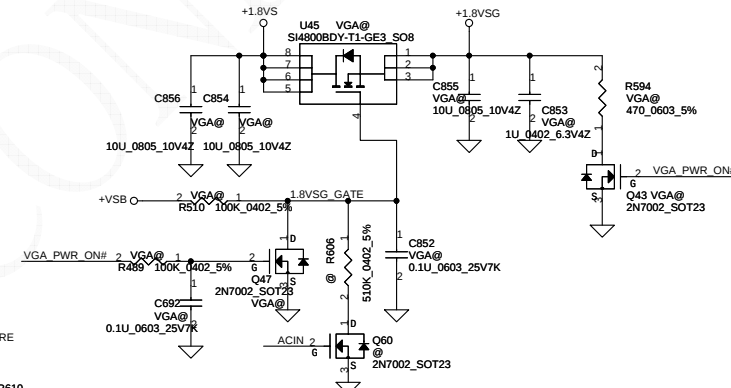
+1.1VALW TO +1.1VS



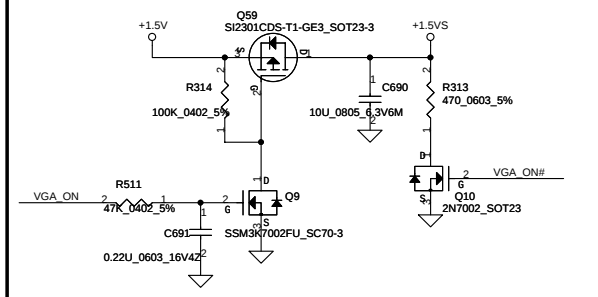
+1.5V to +1.5VSG



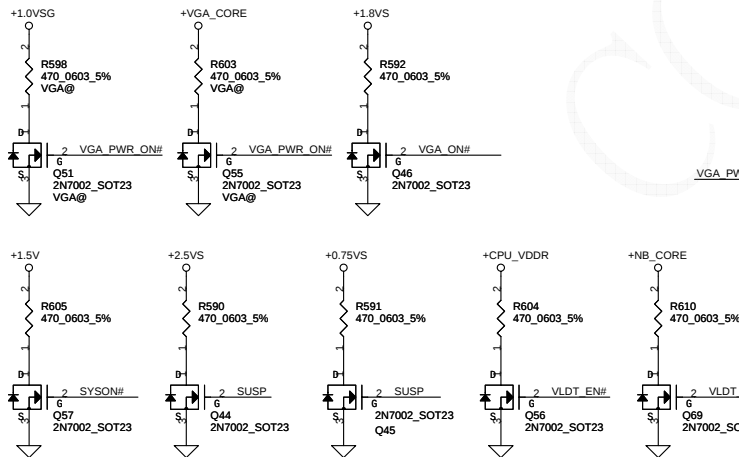
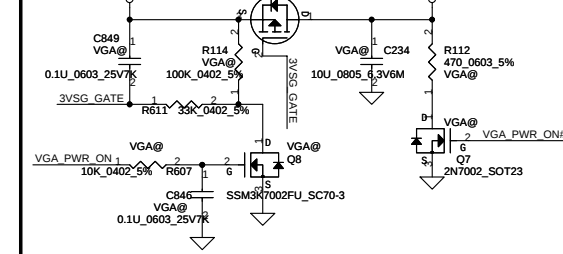
+1.8VS to +1.8VSG



+1.5VS

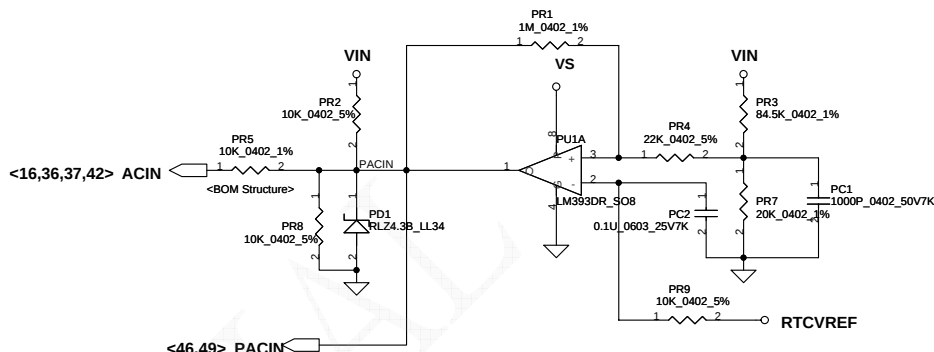
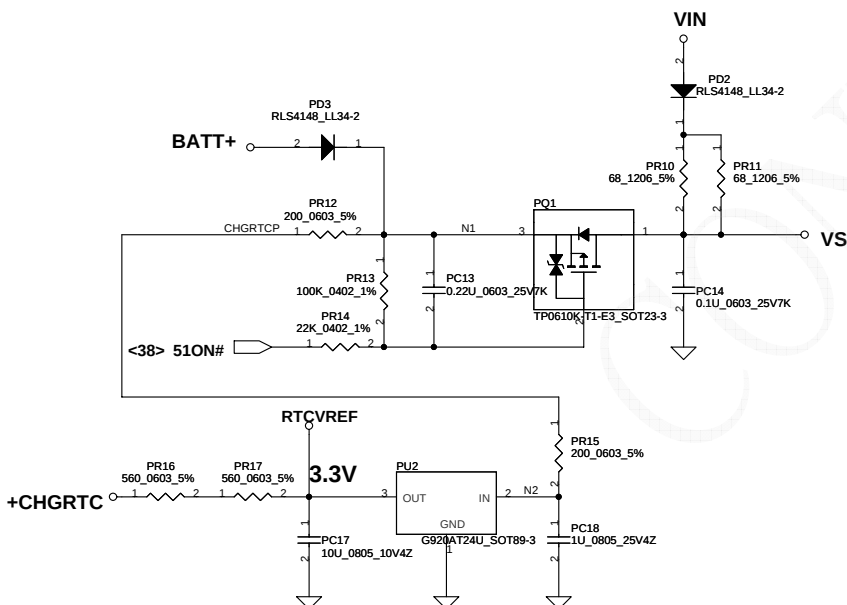
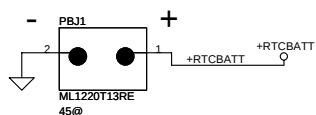
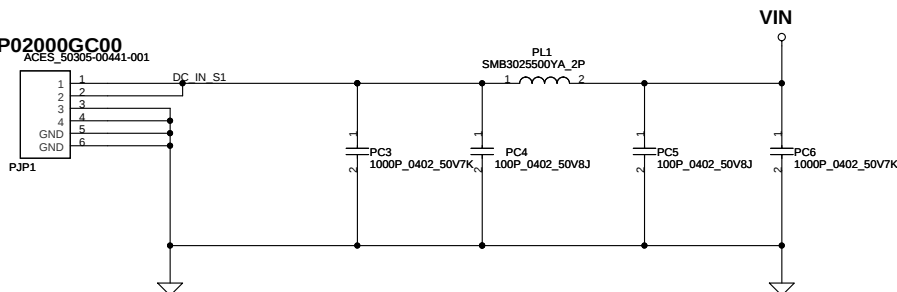


+3VSG

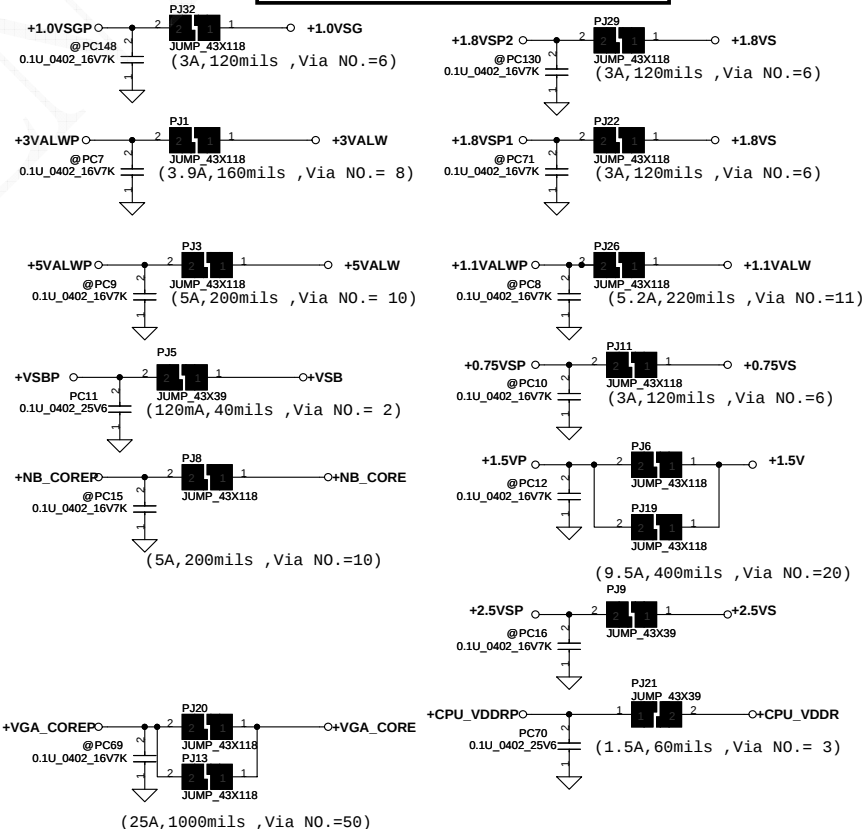


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SP02000GC00
ACES_50305-00441-001

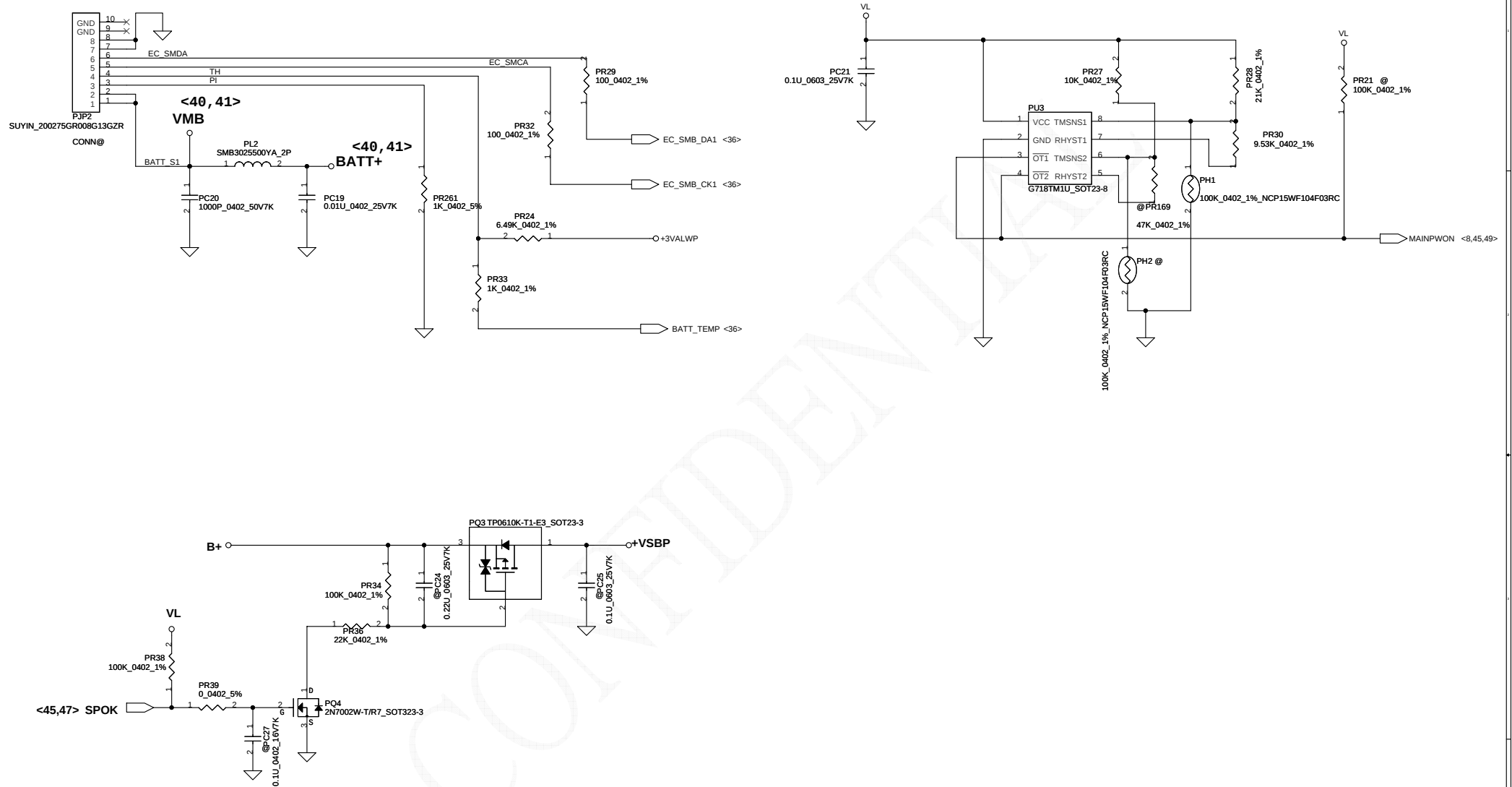


Vin Detector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

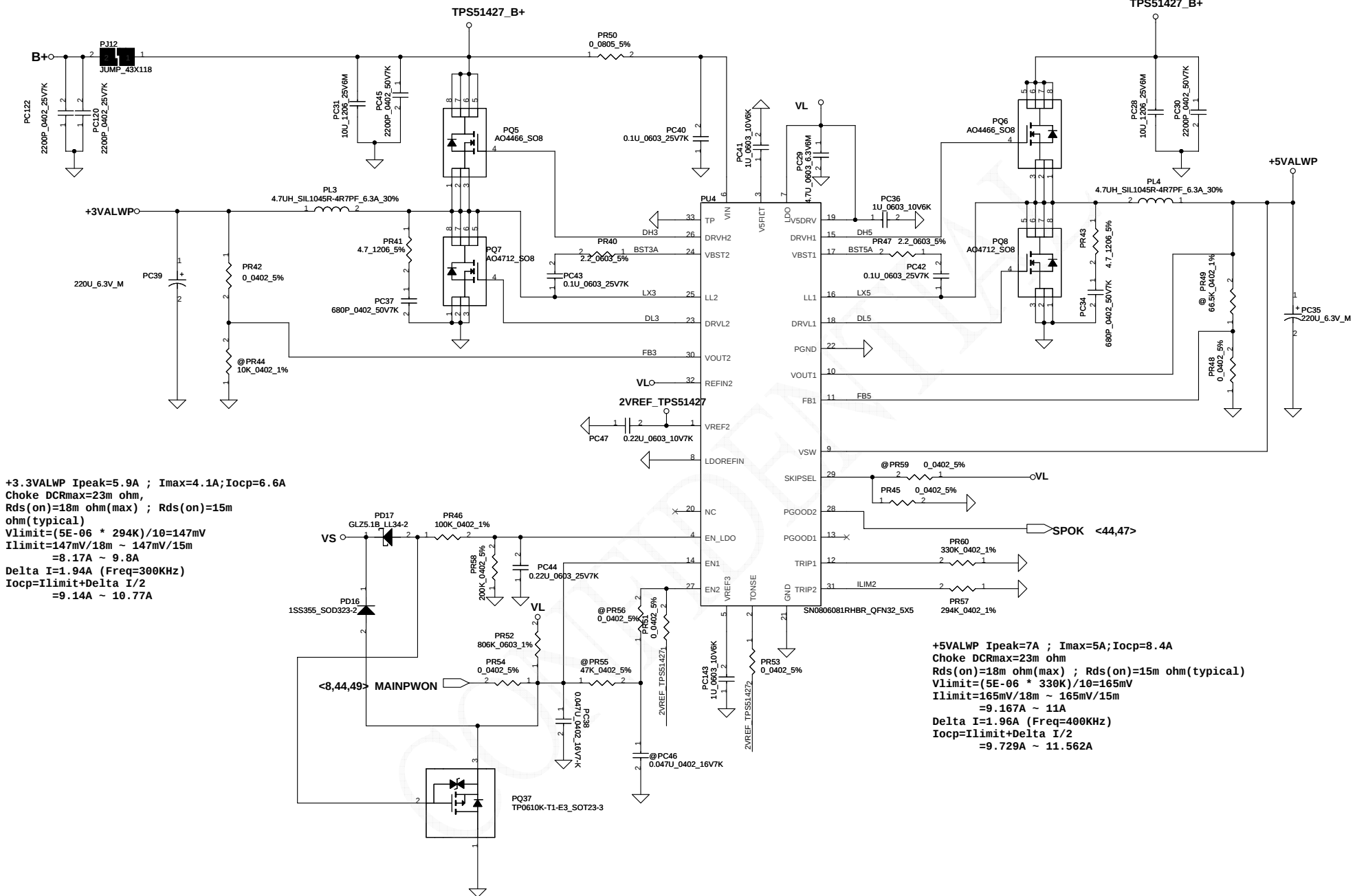


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PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

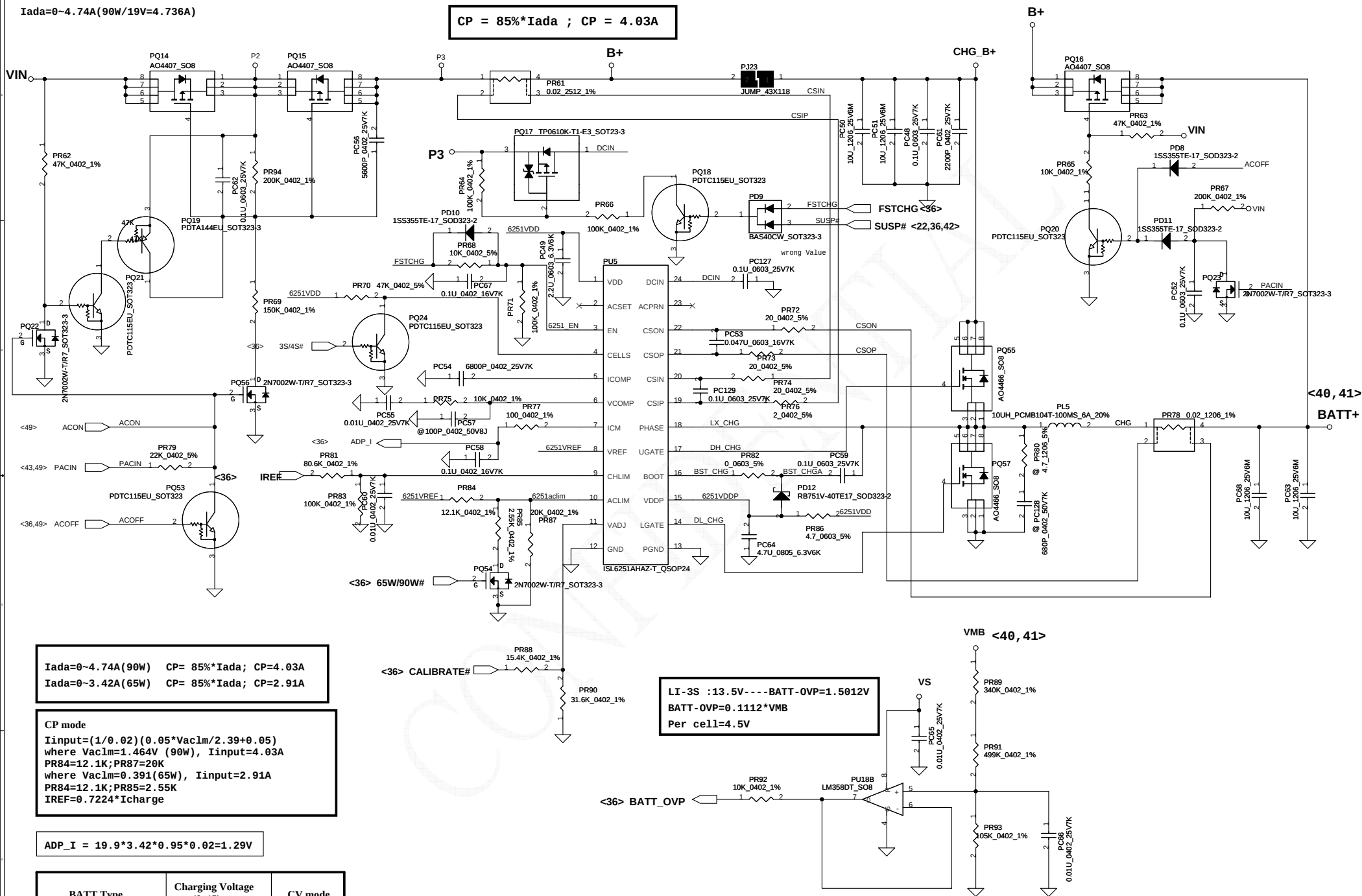


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Iada=0~4.74A(90W/19V=4.736A)

CP = 85%*Iada ; CP = 4.03A



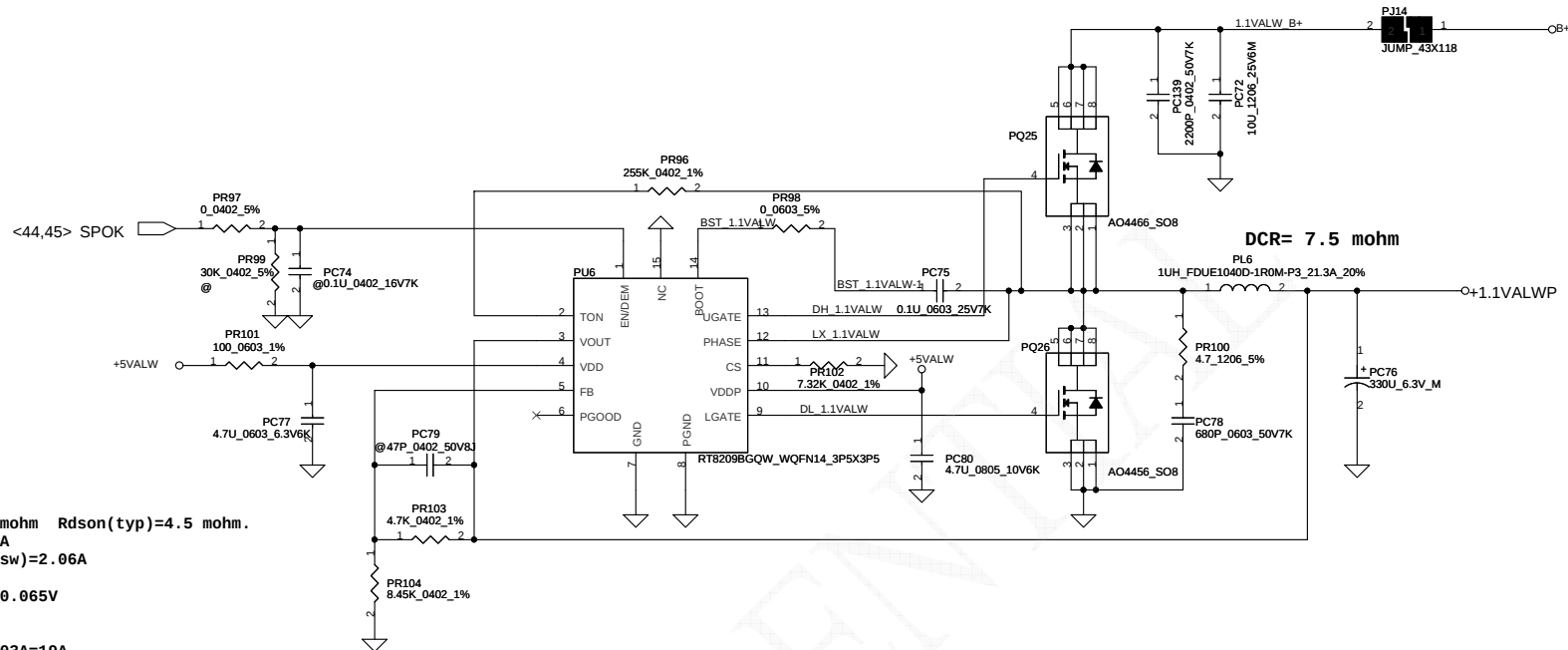
Iada=0~4.74A(90W) CP= 85%*Iada; CP=4.03A
Iada=0~3.42A(65W) CP= 85%*Iada; CP=2.91A

CP mode
Iinput=(1/0.02)*(0.05*Vaclm/2.39+0.05)
where Vaclm=1.464V (90W), Iinput=4.03A
PR84=12.1K;PR87=20K
where Vaclm=0.391(65W), Iinput=2.91A
PR84=12.1K;PR85=2.55K
IREF=0.7224*Icharge

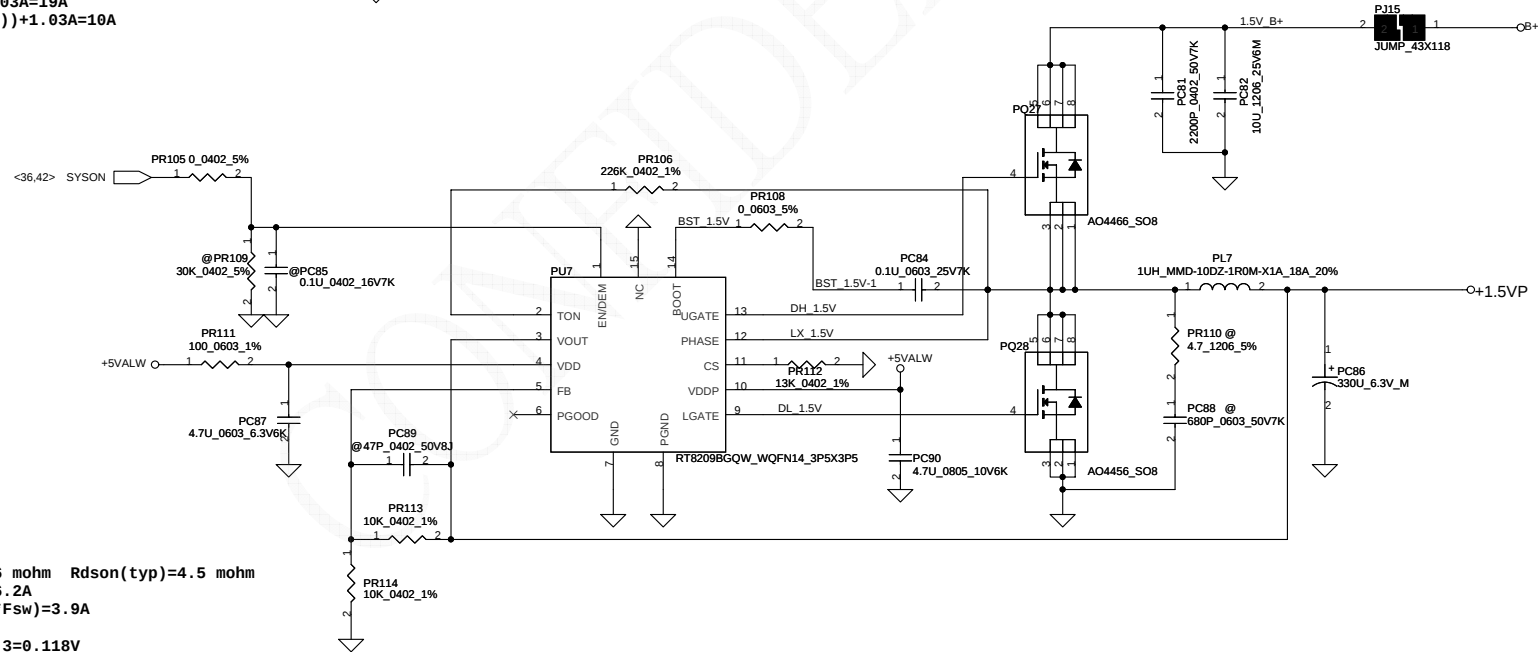
ADP_I = 19.9*3.42*0.95*0.02=1.29V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

LI-3S :13.5V---BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=4.5V



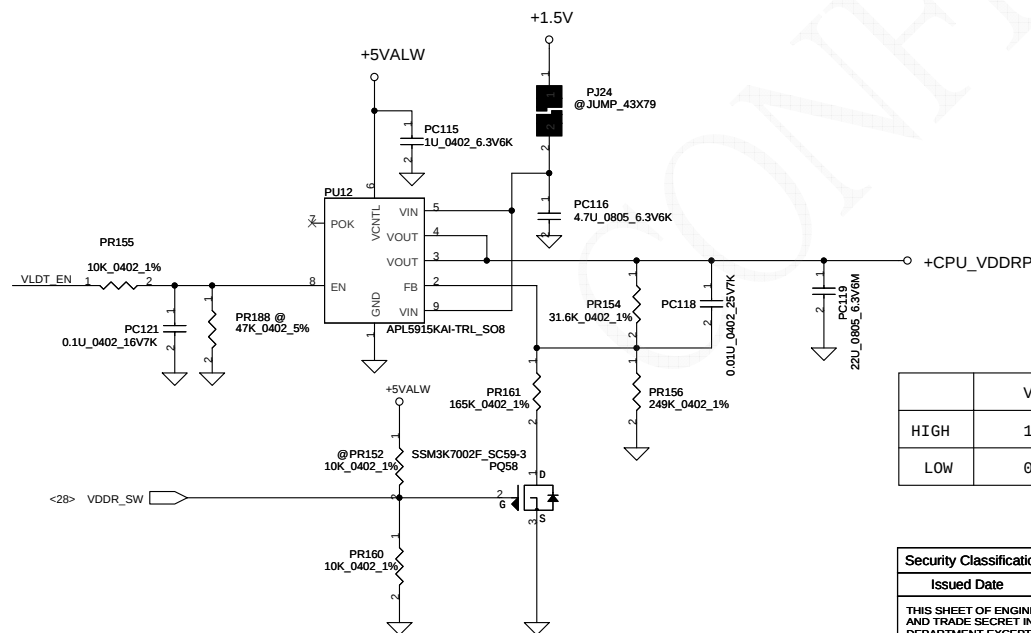
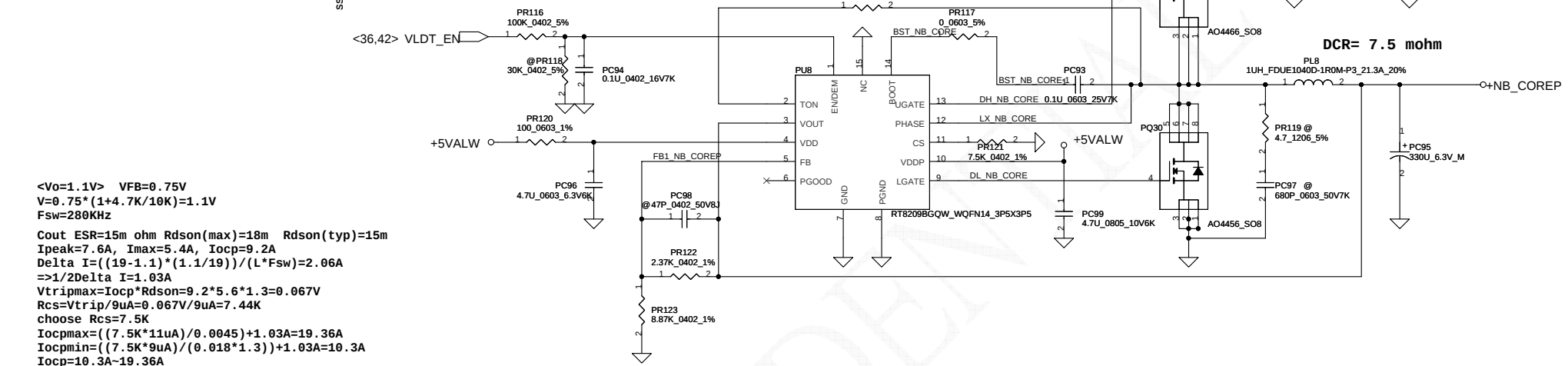
<Vo=1.1V> VFB=0.75V
 $V=0.75 \times (1 + 4.7K/10K) = 1.1V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 15m \text{ ohm}$ $R_{dson(max)} = 5.6 \text{ mohm}$ $R_{dson(typ)} = 4.5 \text{ mohm}$
 $I_{peak} = 7.42A$, $I_{max} = 5.2A$, $I_{ocp} = 8.9A$
 $\Delta I = ((19 - 1.1) \times (1.1/19)) / (L \times F_{sw}) = 2.06A$
 $\Rightarrow 1/2 \Delta I = 1.03A$
 $V_{tripmax} = I_{ocp} \times R_{dson} = 8.9 \times 5.6 \times 1.3 = 0.065V$
 $R_{cs} = V_{trip} / 9uA = 0.065V / 9uA = 7.2K$
 choose $R_{cs} = 7.32K$
 $I_{ocpmax} = ((7.32K \times 11uA) / 0.0045) + 1.03A = 19A$
 $I_{ocpmin} = ((7.32K \times 9uA) / (0.0056 \times 1.3)) + 1.03A = 10A$
 $I_{ocp} = 10A \sim 19A$



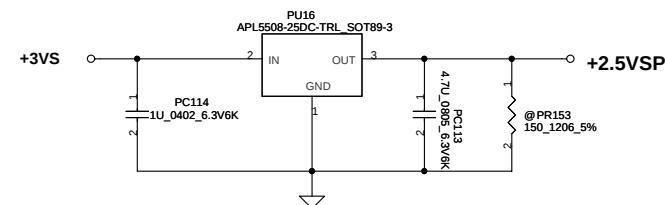
<Vo=1.5V> VFB=0.75V
 $V=0.75 \times (1 + 10K/10K) = 1.5V$
 $F_{sw} = 280KHz$
 $C_{out} ESR = 17 \text{ mohm}$ $R_{dson(max)} = 5.6 \text{ mohm}$ $R_{dson(typ)} = 4.5 \text{ mohm}$
 $I_{peak} = 13.5A$, $I_{max} = 9.5A$, $I_{ocp} = 16.2A$
 $\Delta I = ((19 - 1.5) \times (1.5/19)) / (L \times F_{sw}) = 3.9A$
 $\Rightarrow 1/2 \Delta I = 1.95A$
 $V_{tripmax} = I_{ocp} \times R_{dson} = 16.2 \times 5.6 \times 1.3 = 0.118V$
 $R_{cs} = V_{trip} / 9uA = 0.118V / 9uA = 13.1K$
 choose $R_{cs} = 13K$
 $I_{ocpmax} = ((13K \times 11uA) / 0.0045) + 1.95A = 32A$
 $I_{ocpmin} = ((13K \times 9uA) / (0.0056 \times 1.3)) + 1.95A = 18A$
 $I_{ocp} = 18A \sim 32A$

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	POWER_SEL
HIGH	0.95V
LOW	1.1V

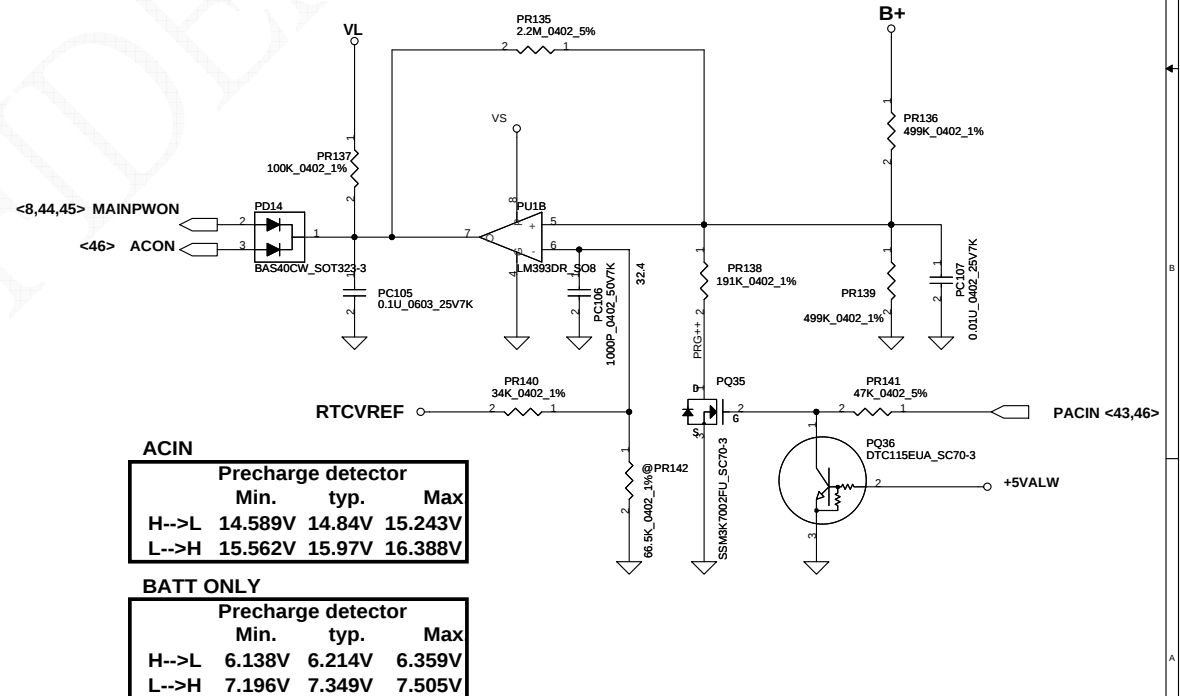
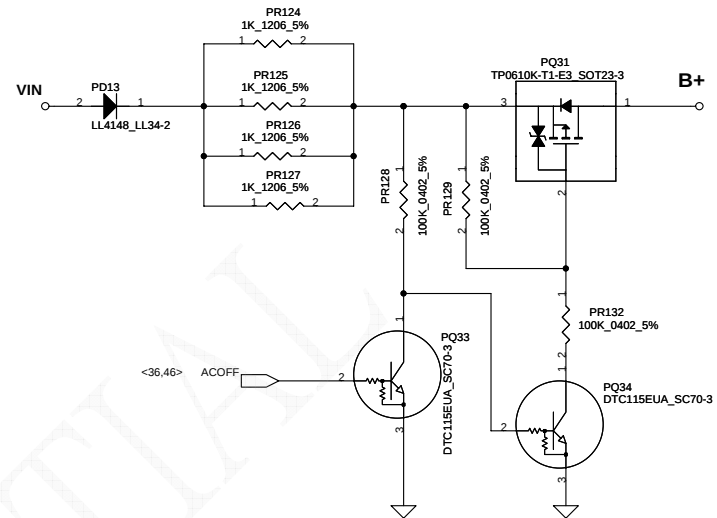
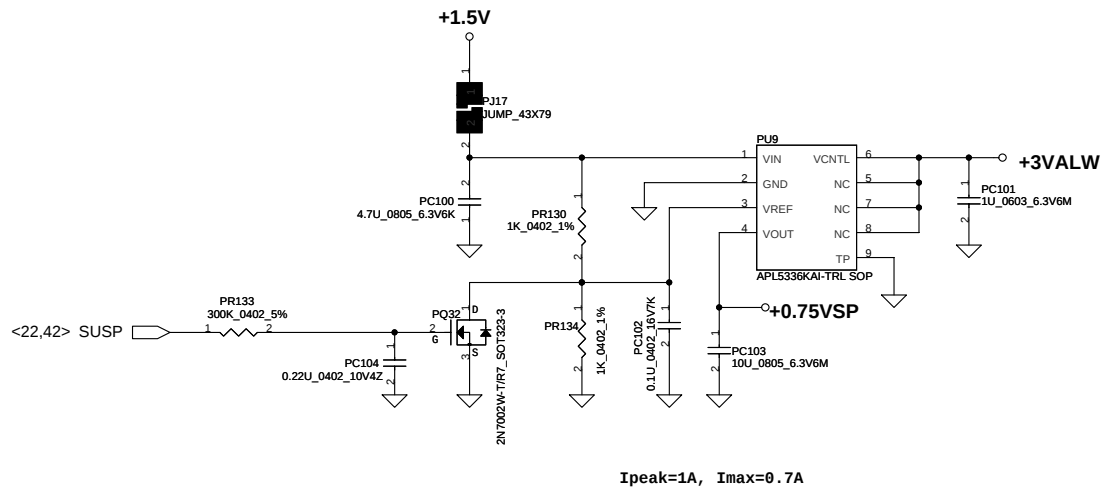


	VDDR_SW
HIGH	1.05V
LOW	0.9V

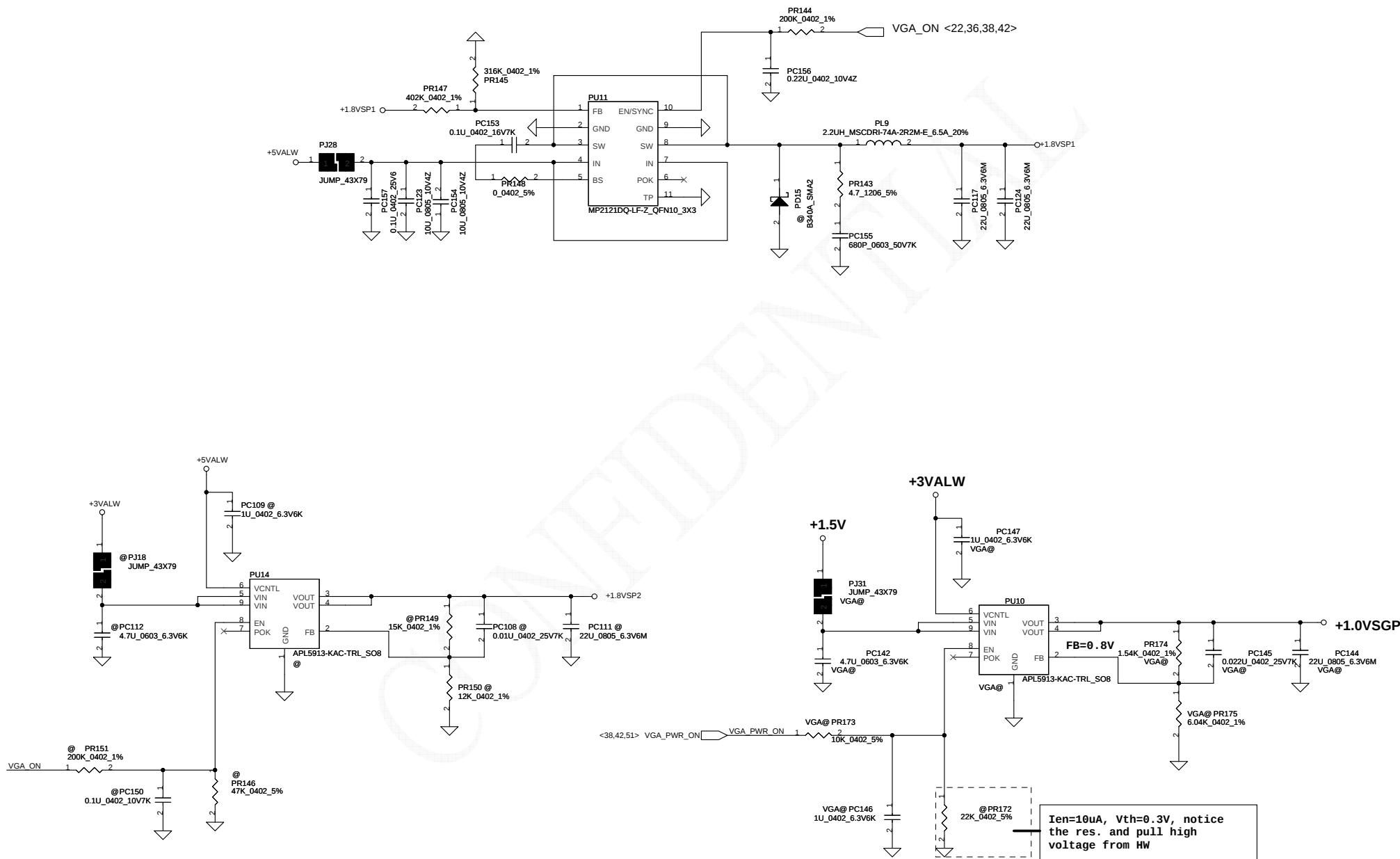


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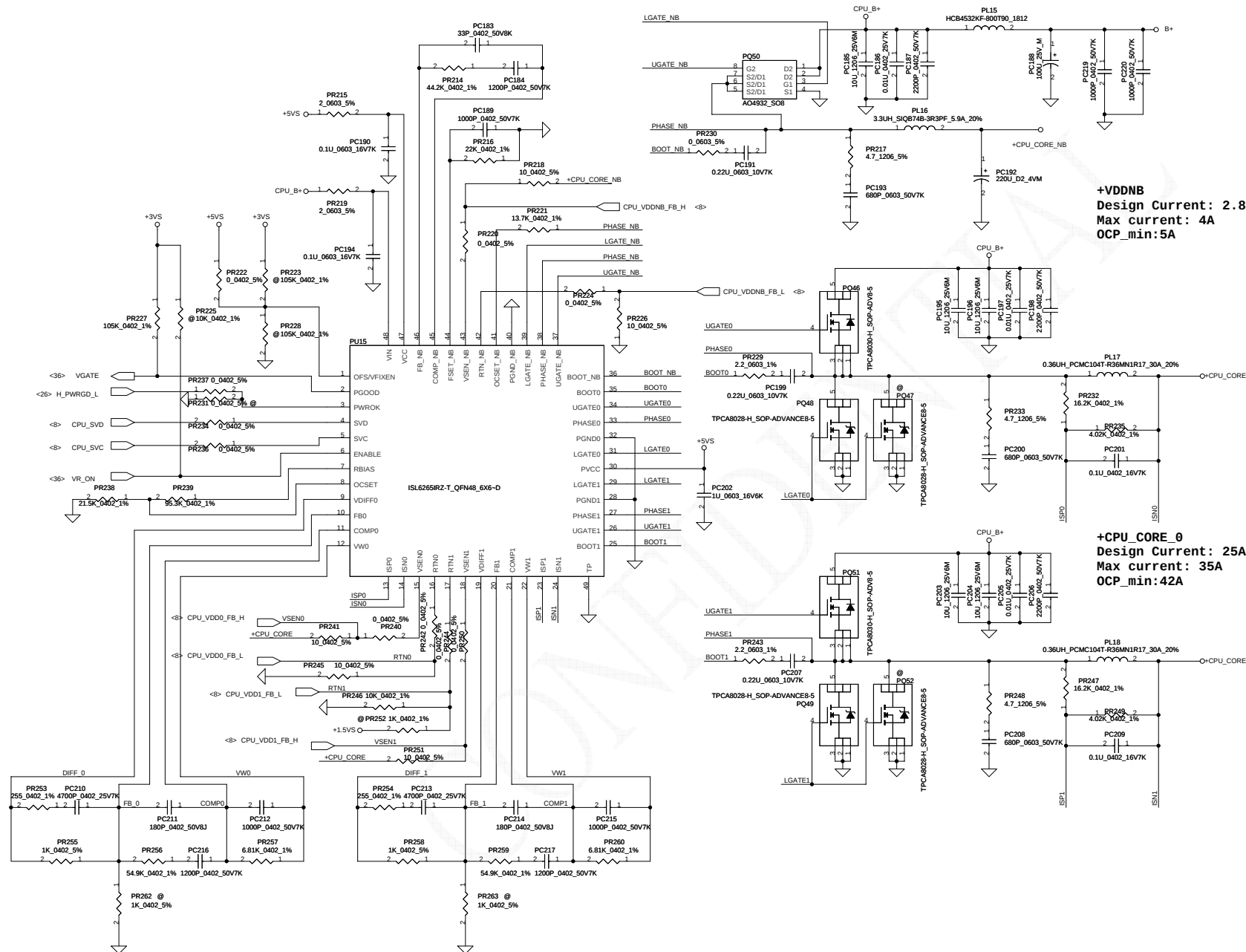
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+VDDNB
Design Current: 2.8A
Max current: 4A
OCP_min:5A

+CPU_CORE_0
Design Current: 25A
Max current: 35A
OCP_min:42A

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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	ADD 2 switch mos and remove 2 pull high resistance to modify VGA_CORE switch level	Before modify to fault, we recognize that VGAPWRSEL pin is open drain state. But after check with AMD AE regoer to clear the foul that VGAPWRSEL pin has driving ability,so i take away 2 pull high resistance and add 2 switch mos to modify the switch level.	0.1	52	ADD PQ60 and PQ61 remove PR212(10K,0402) and PR213(10K.0402)	2009/08/21	EVT_NEW75
2	change thermister , tune PH1 protection and recovery set point	change thermister from 150K to 100K	0.1	44	thermister part number SL200000V00 and PR28 change to 21K, PR30 change to 9.53K	2009/08/27	EVT_NEW75
3	Add GPU voltagr sence net	Cause GPU have GCORE_SEN and FB_GND pin so power add receive net.	0.1	51	ADD GCORE_SEN and FB_GND net, also add PR296(0_0402_1%), PR297(10_0402_5%) and PR298(0_0402_5%)	2009/09/04	EVT_NEW75
4	change DC-IN connector part number	to meet pin definition	0.1	43	change part number is SP020908120	2009/09/10	EVT_NEW75
5	change reistance PR81 value	Cause meet battery Ki value setting from 1.106 to 0.7224. change PR81 from 154K(0402_1%) to 80.6K(0402_1%)	0.1	46	change resistance PR81 value from 154K to 80.6K	2009/09/22	EVT_NEW75
6	ADD switch circuit for 1.05V	Cause follow AMD electrcial sheet, VDDIO/ VDDR voltage setting procedure. AMD processor will switch between 1.05V and 0.9V by VDDIO and VDDR	0.1	48	ADD PR161 (165K_0402_1%), PQ58, PR152(10K_0402_5%),PR160(10K_0402_5%), PC131(0.1U_25V6) , change PR161 value from 100K to 249K, and ADD enable net name -VDDR_SW	2009/09/22	EVT_NEW75
7	change resistance size	cause for component de-rating . Prevent the component break down when inrush current happen.	0.1	46	change PR61 from (0.02_1206_1%) to (0.02_2512_1%)	2009/10/06	EVT_NEW75
8	Modify VGA_CORE mapping table.	cause ATI change power play voltage, so change the table value.	0.1	51	change PR198 from 9.76_0402_1% to 9.53_0402_1%, PR197 from 37.4_0402_1% to 64.9_0402_1% and PR201 from 17.8_0402_1% to 31.6_0402_1%	2009/10/06	EVT_NEW75
9	Change 1.0VSGP enable RC value	Prevent LDO can't turn off when it should turn off	0.1	50	Change PR173 from 100K_0402_5% to 10K_0402_5%, PC146 from 0.1u_0402 to 1u_0402	2009/10/15	EVT_NEW75
10	Change lowside MOS of VGA_CORE	Cause light load efficiency result is fail, and we get result after discuss FAE. The reason is lowside mos Rdsn too less and IC will detect not very sensitive	0.1	51	Change PQ39 and PQ40 from TPCA8028(SB000006L00) to A04456(SB000009F80)	2009/11/19	EVT_NEW75
11	Change 3/5Valw boost resistance value	For EMI request	0.1	45	Change PR40 and PR47 from 0_0603_5% to 2.2_0603_5%(SD013220B80)	2009/11/19	EVT_NEW75
12	ADD two capacity	For EMI request	0.1	52	Add pc219 and pc220 are both S CER CAP 1000P 50V K X7R 0402	2009/11/23	EVT_NEW75
13	ADD three resistance	Cause madison and park need different voltage switch level so add different resistance value for the problem.	0.1	51	Add PR197(68.1K_0402_1%) , PR198 (9.53K_0402_1%) and PR201 (31.6K_0402_1%)	2009/11/23	EVT_NEW75
14	Change chock	Cause A phase put wrong chock	0.2	37,39,40	Change PL9 from SH00000FK00 to SH000009Q00	2009/11/23	EVT_NEW75

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Version change list (P.I.R. List)

DVT Stage

- 1. remove Y4 related
- 2. add a bead on +VDDA11PCIE ---ok (add L28)
- 3. use 6mohm MOS on +1.1VS ---ok (U38,U37)
- 4. +1.1VALW vlotage level --check PW rail
- 5. check EC sequence (syson/vga_on) --ok
- 6. VRAM ID --ok
- 7. VRAM_RST circuit -- check slew rate
- 8. 3G module circuit update --ok
- 9. EC 500K circuit --ok
- 10. MEMZN circuit (0ohm/10uF) --ok
- 11. check GBE PU/PD --ok
- 12. check capacitor size
- 13. TXC crystal value --ok (change X1,Y2), Y5
- 14. internal clock circuit --ok
- 15. ADD VGAPWR_ON --ok, INT_VGAPWR_ON
- 16. define PX_FN/CLK_MODE strap pin --ok
- 17. define CLK_REQ for internal CLKREQ --ok
- 18. change 4.7u_0805 type --ok
- 19. BOM change for SG --ok
- 20. add VGAPWR_ON for SG&int clock use --ok
- 21. add PJ25 --ok
- 22. LED1/3 680ohm, LED2/4 3.9Kohm --ok
- 23. add MUXLESS strap --ok (R521,R612)
- 24. add LPW planel feature --ok (LOCAL_DIM / COLOY_ENG_EN)
- 25. EC version control--ok (R529,R528)
- 26. WiMAX LED combine circuit --ok (R530,R531,D47)
- 27. change INT_VGAPWR_ON to EC_pin91 --ok
- 28. add VB function --ok (R533,R532)
- 29. Add R534,R535,R536 for layout --ok
- 30. change Y5 to 33p cap
- 31. pop ESD diode --ok
- 32. set T25 to BH for main --ok
- 33. Define Board file ID for SW req. --ok

For PEW change list

- 1. Change Strap/PID/BID for SW
- 2. Change EC version to E0
- 3. Change thermal sensor to SB-TSI
- 4. Define 8L_6L_UMA strap on SB
- 5. Change EC version to D3 06/29

PVT Stage

- 1. un-pop D39,D41 p.40
- 2. pop D27 p.39
- 3. un-pop Q73,Q74,Q75,Q70,R500,R502 p.38
- 4. Change R470 to 8.2K p.36
- 5. Change R600,R510,R489 to 100K p.22/p.42
- 6. Change C847 to 0.1u p.22
- 7. Change C739,C740 to 15p p.36
- 8. Change LED resistance R477,R499 change to 2.2K p.37
- 9. Change R611 to 33K p.42
- 10. Change HDMI_HPD PU from +3VSG to +3VS p.24
- 11. Change C957,C971 to 0.47u_0603 p.40
- 12. Remove VGA option solution
unpop R147,R420,R421,R248 pop R161 p.16/p.22/p.17
- 13. Pop R595,R596,Q49,Q48 change R595 to 300k p.42
- 14. Change LED1,LED3 to SC591NB5A30 p.37
- 15. Change Q5,Q26 to SB00000DH00 p.16/p.37
- 16. Change C468-C475 to MAD@ p.20
- 17. Change C305,C306 to 0603 size p.18
- 18. Change LED control circuit, Pop R537,R457 p.34/p.35
- 19. Update AMP GAIN to 10dB p.40
- 20. Change C11,C56,C723 to SGA00002N80 p.8/p.9/p.35
- 21. Change TPC24 to TPC12 for layout

MP Stage

- 1. Add R541, R542 for TSI leakage current issue. (option) p.36
- 2. Change C21 from 3300pF to 100pF
- 3. Unpop C21
- 4. Unpop SW3
- 5. Change C305 to MAD@
- 6. Change VGA to R3 P/N 0419
- 7. Unpop ESD Diode D24 / D27 / D29 0512

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
15	Change chock	Cause NB_CORE and 1.1VALW efficiency measurement result fail. so change inductor from 1.8uH to 1.0 uH, and change the tye from ferrite to moding	0.2	47,48	Change PL6 and PL8 from SH000009680 to SH000009U00	2009/12/01	EVT_NEW75
16	Change resistance value	Cause change low side MOS from TPCA8028 to A04456. And there have different Rds(on). then OCP will different, so i need to change ocp setting resistance.	0.2	51	Change PR190 from SD000004100 (S RES 1/16W 8.2K +-1% 0402) to SD00000QM80 (S RES 1/16W 14.3K +-1% 0402)	2009/12/01	EVT_NEW75
17	ADD sunbber	Cause VGA_CORE phase ringing too strong, so add sunbber to reduce the ringing	0.2	51	ADD PR191(SD001470B80 ,S RES 1/4W 4.7 +-5% 1206) and PC171(SE025681K80 S CER CAP 6,80P 50V K X7R 0603)	2009/12/01	EVT_NEW75
18	Change resistance value	change VGA_CORE switch frequency fromm 300K to 400K, for solve efficiency fail issue	0.2	51	Change PR196 from 44.2K to 33K	2009/12/01	EVT_NEW75
19	Delete component PC73, PC83 and PC92	Cause for design resinable	0.2	47,48	Delete PC73,PC83 and PC92	2009/12/01	EVT_NEW75