

Compal Confidential

NCWG0/H0 Schematics Document

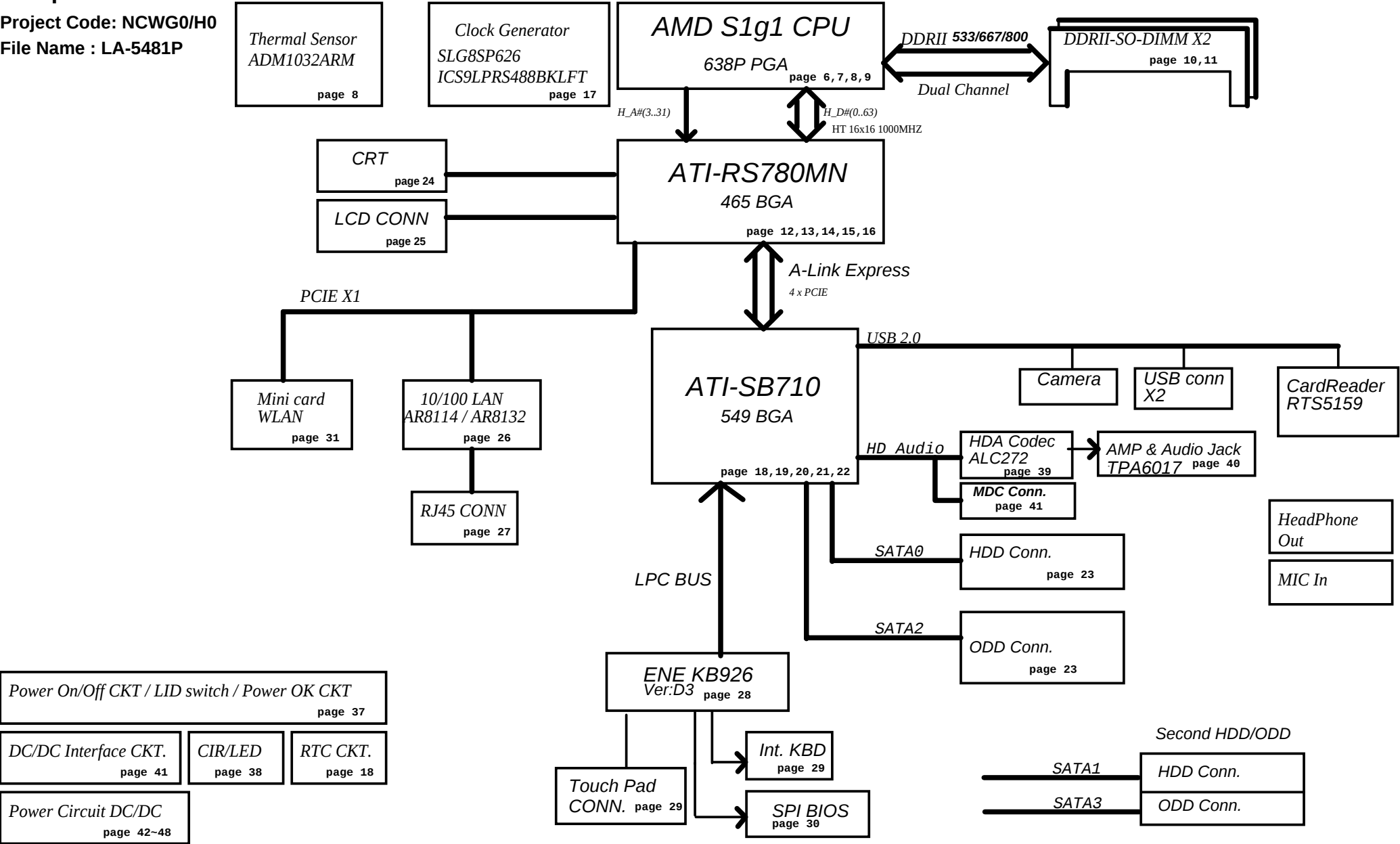
AMD S1g1 / RS780MN/ SB710

2009 / 06 / 24

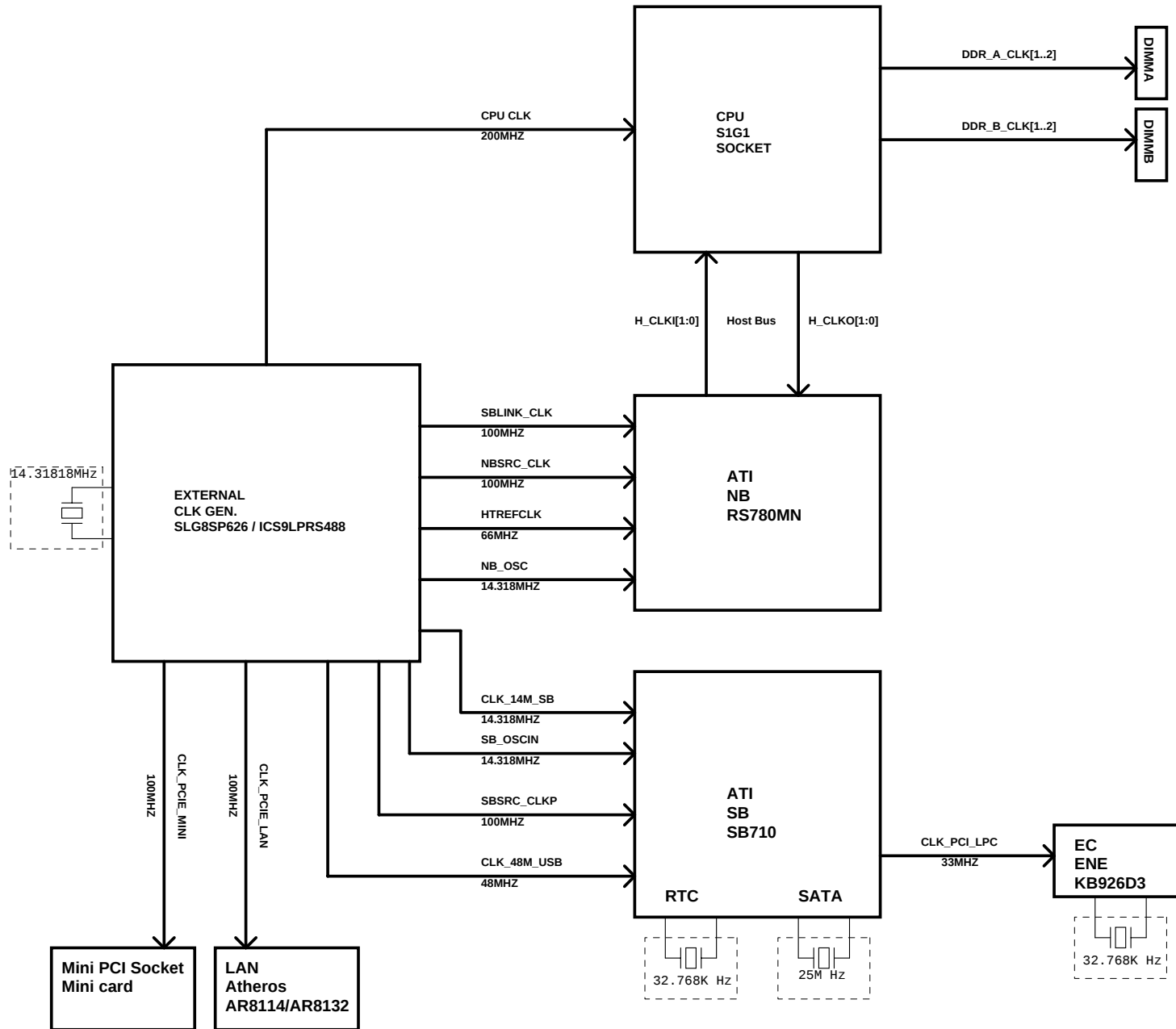
LA-5481

Rev:1.0

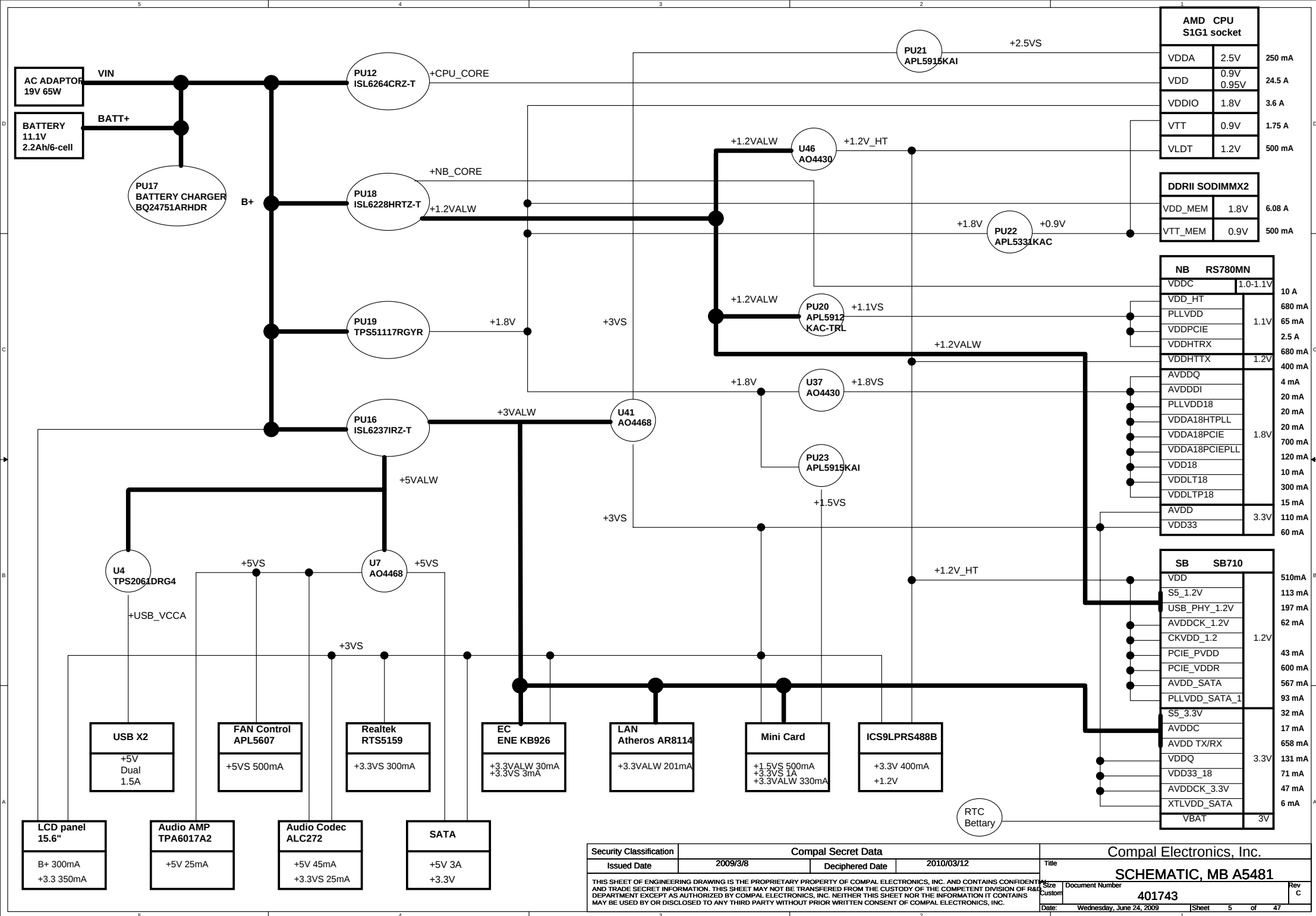
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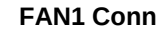
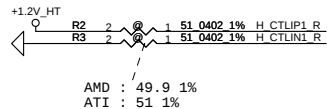
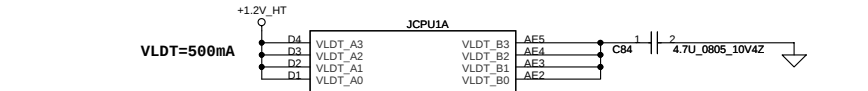


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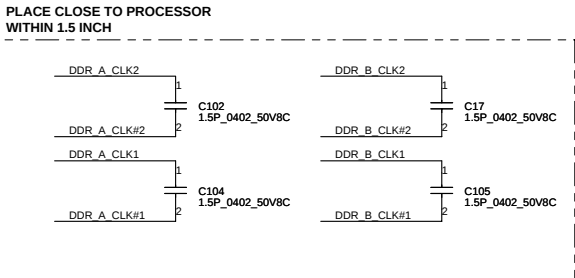
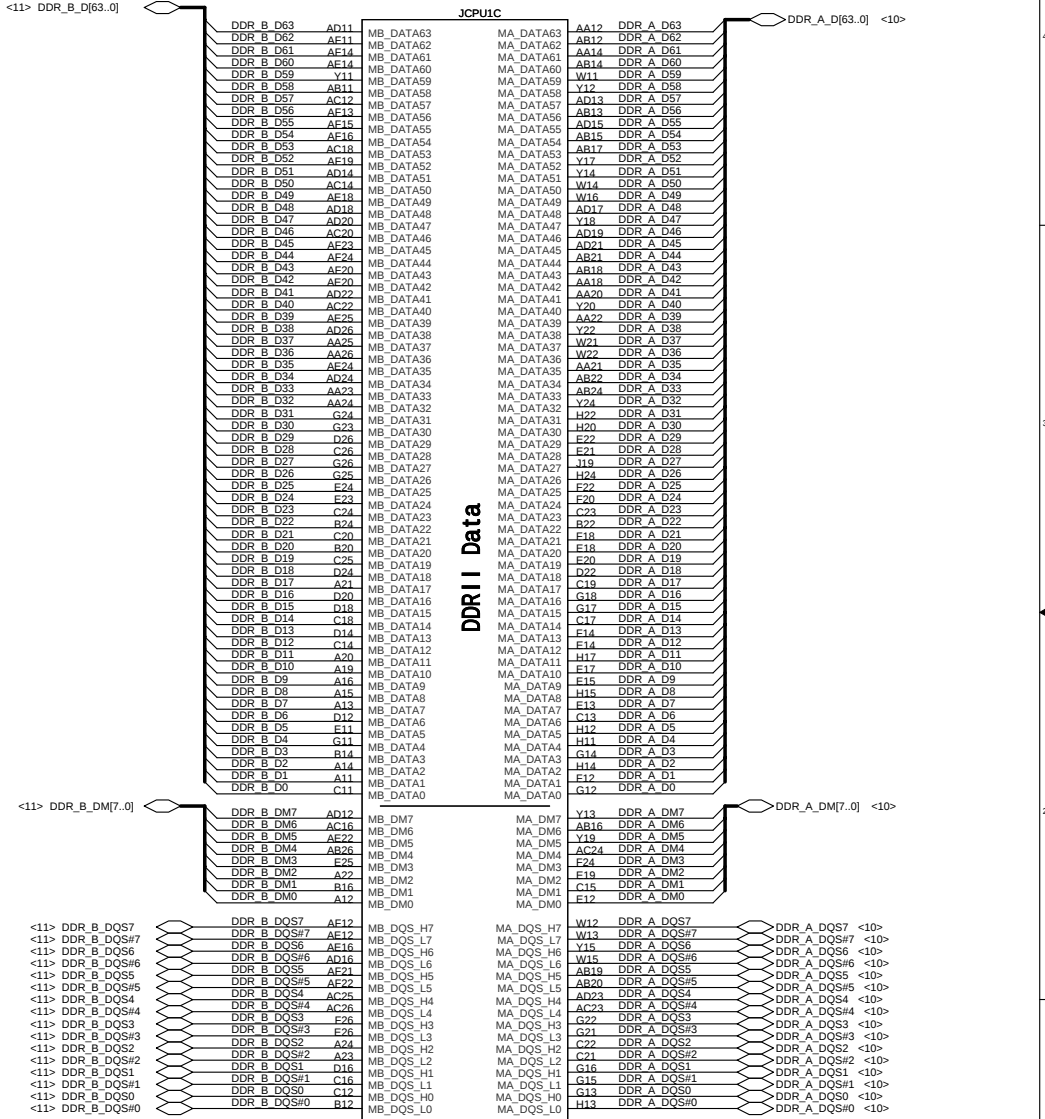
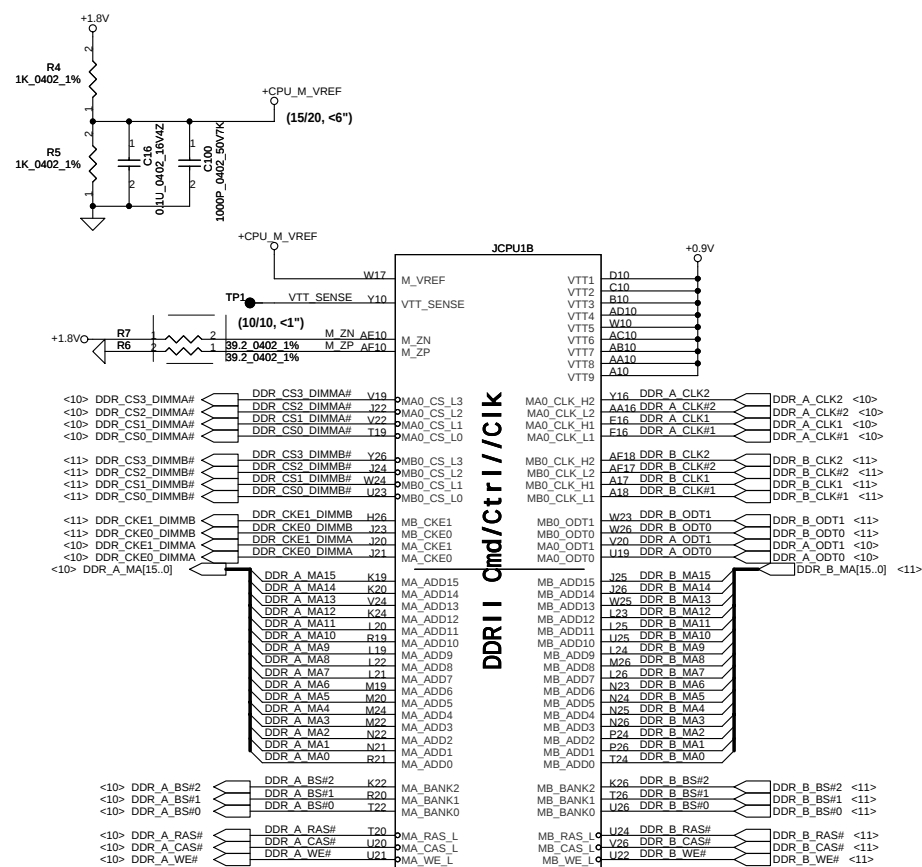
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Processor DDR2 Memory Interface



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VDD(+CPU_CORE) decoupling.

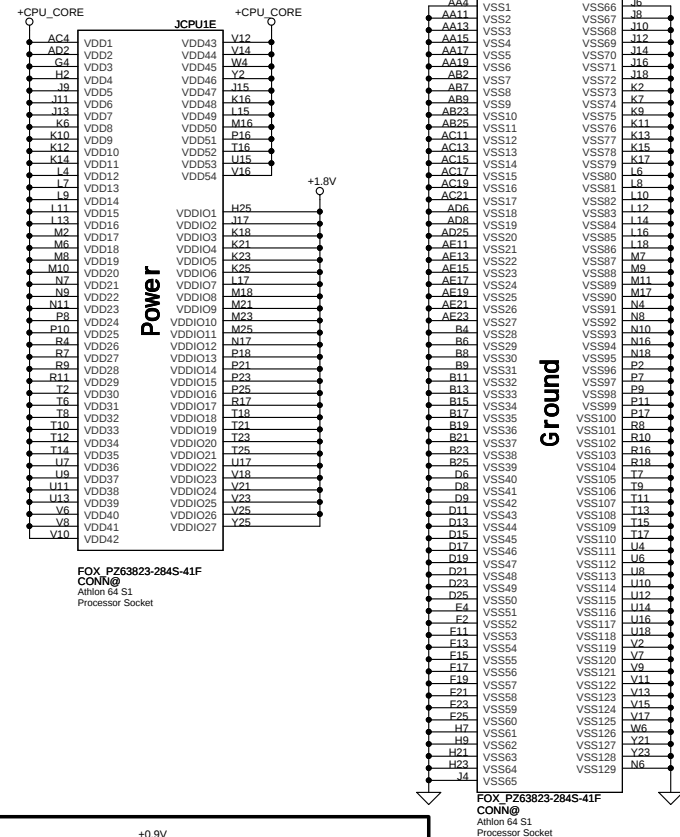
Near CPU Socket

Under CPU Socket

Under CPU Socket

Between CPU Socket and DIMM

180PF Qty follow the distance between CPU socket and DIMM0. <2.5inch>



VTT decoupling.

Near Power Supply

C: Change to NB0 CAP

150U_D2 6.3VM

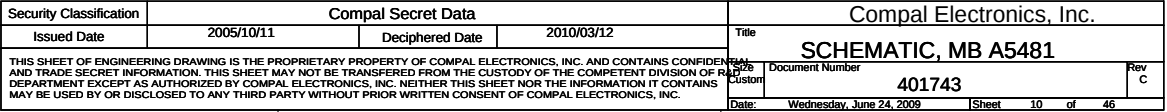
Near CPU Socket Right side.

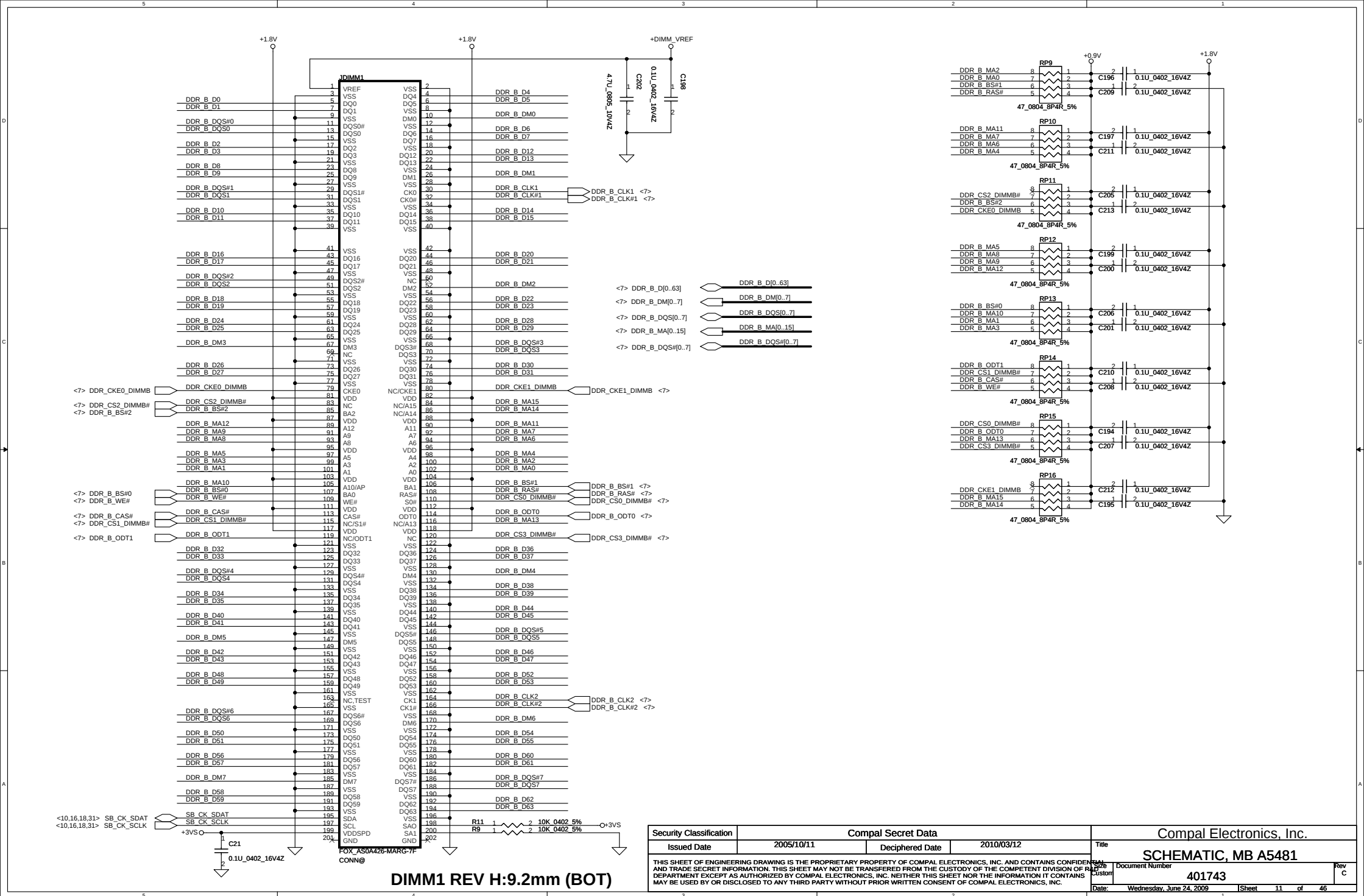
Near CPU Socket Left side.

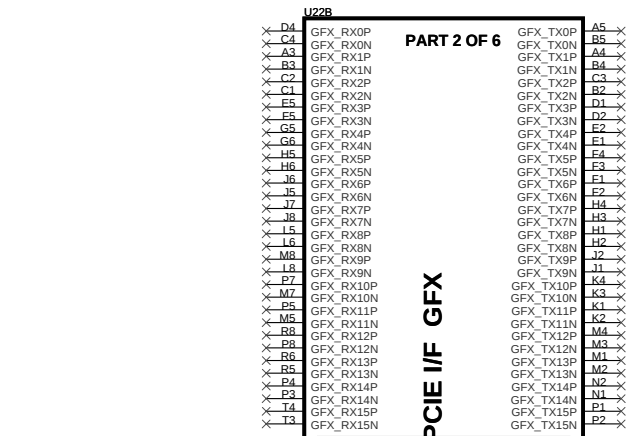
Athlon 64 S1 Processor Socket

The diagram illustrates the VTT decoupling circuit for an Athlon 64 S1 processor. It shows three main horizontal bus lines, each connected to a +0.9V supply. The top line, labeled 'Near Power Supply', includes a callout for capacitor C66, indicating a change from 150U_D2 6.3VM to NB0 CAP. The middle line, labeled 'Near CPU Socket Right side', and the bottom line, labeled 'Near CPU Socket Left side', each feature a series of capacitors (C155, C146, C184, C173, C72, C145, C180, C121 on the right; C73, C70, C127, C185, C164, C163, C152, C179 on the left) connected to the bus. The capacitors are labeled with their values and part numbers. The diagram is divided into sections labeled '<BOM Structure>'.

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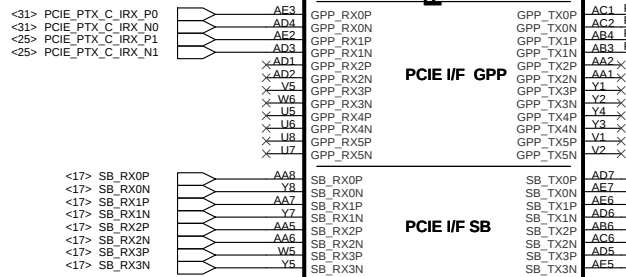






Check SW Routing

AN_RS780MN1. Only suggest pair0-3 can
usage for power save.



RS780M_FCBGA528

RS780MN-SA00002DR30 Ver:A13

RS780M Display Port Support (muxed on GFX)

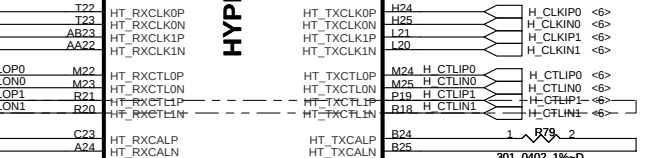
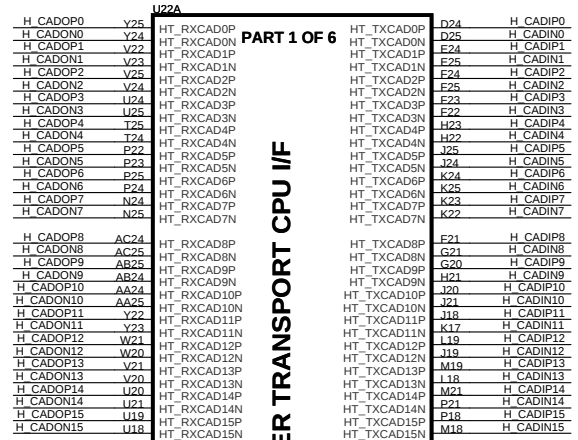
DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

HT Link

When tune trace length, must
keep 1:4 on self-trace

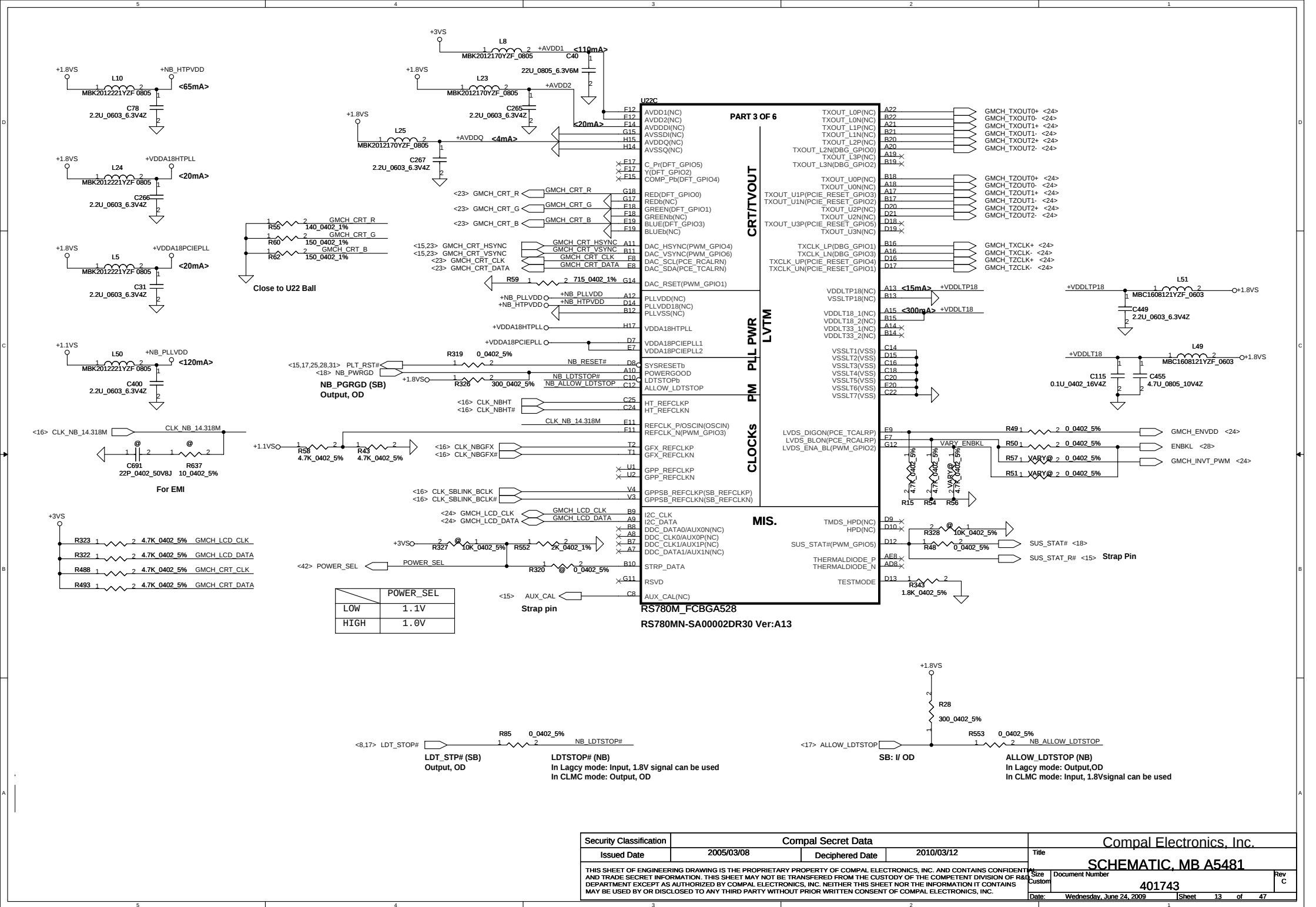
Check AMD

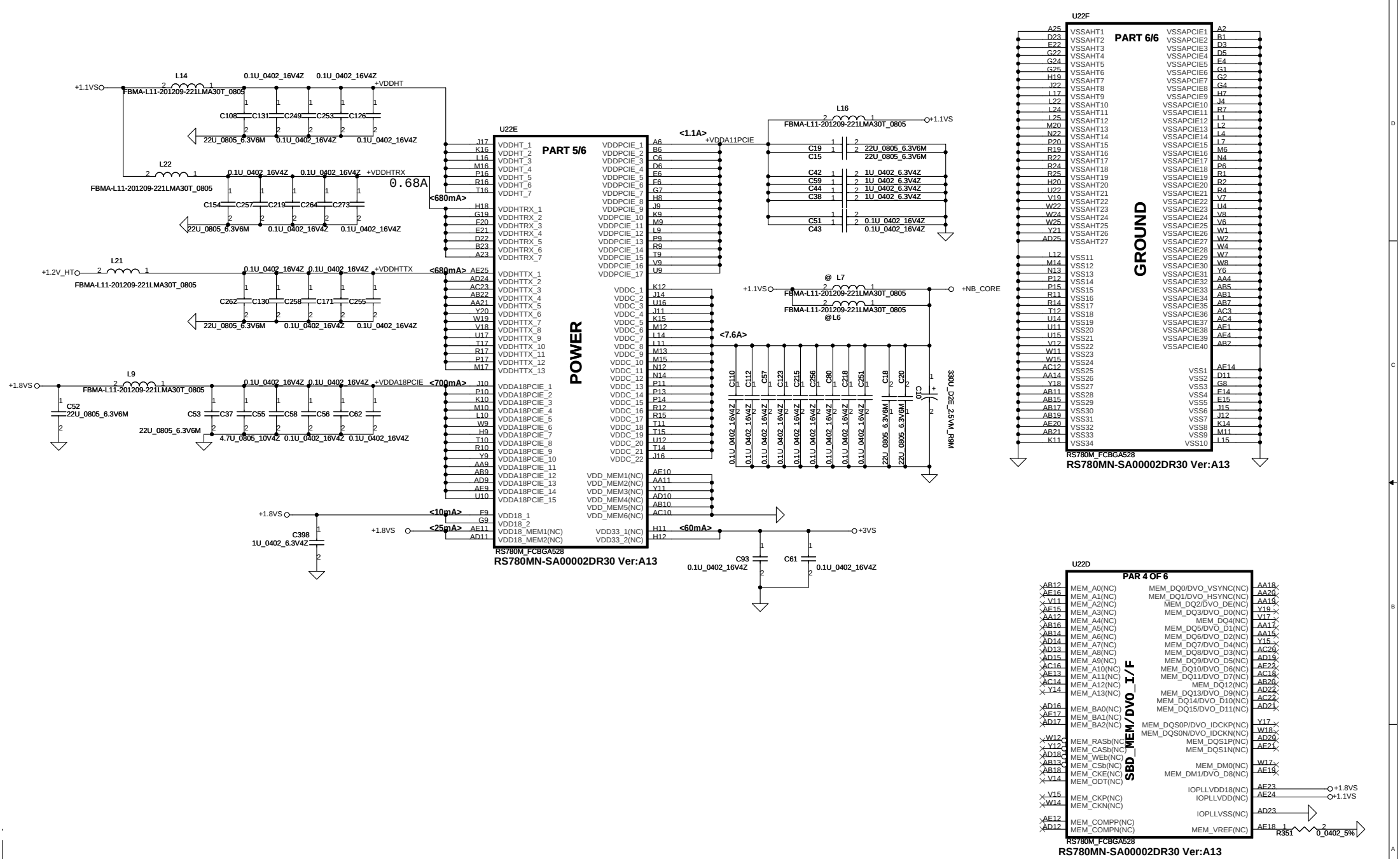
Place within 1"
layout 4/8



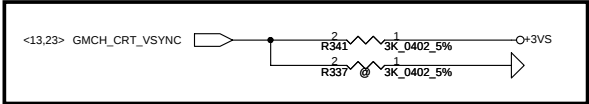
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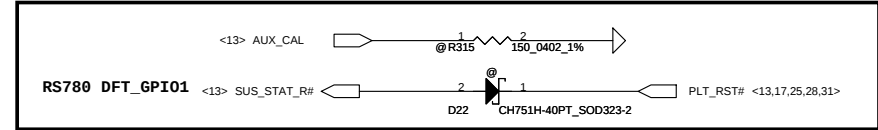


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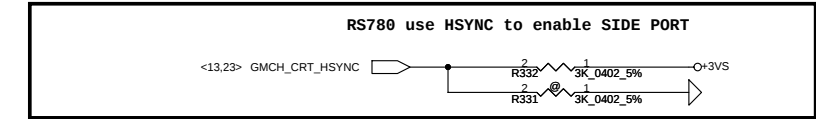
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLED

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

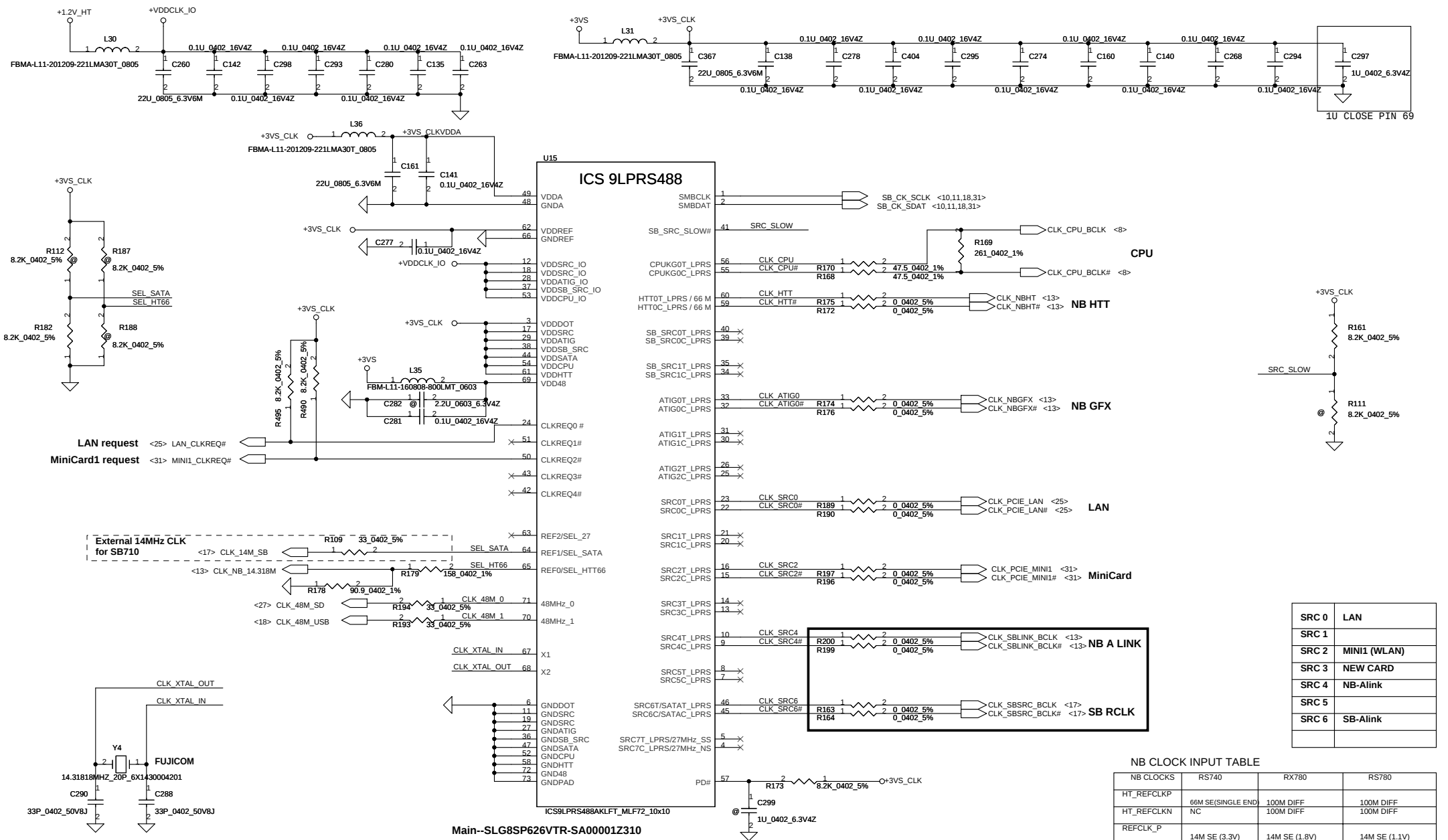
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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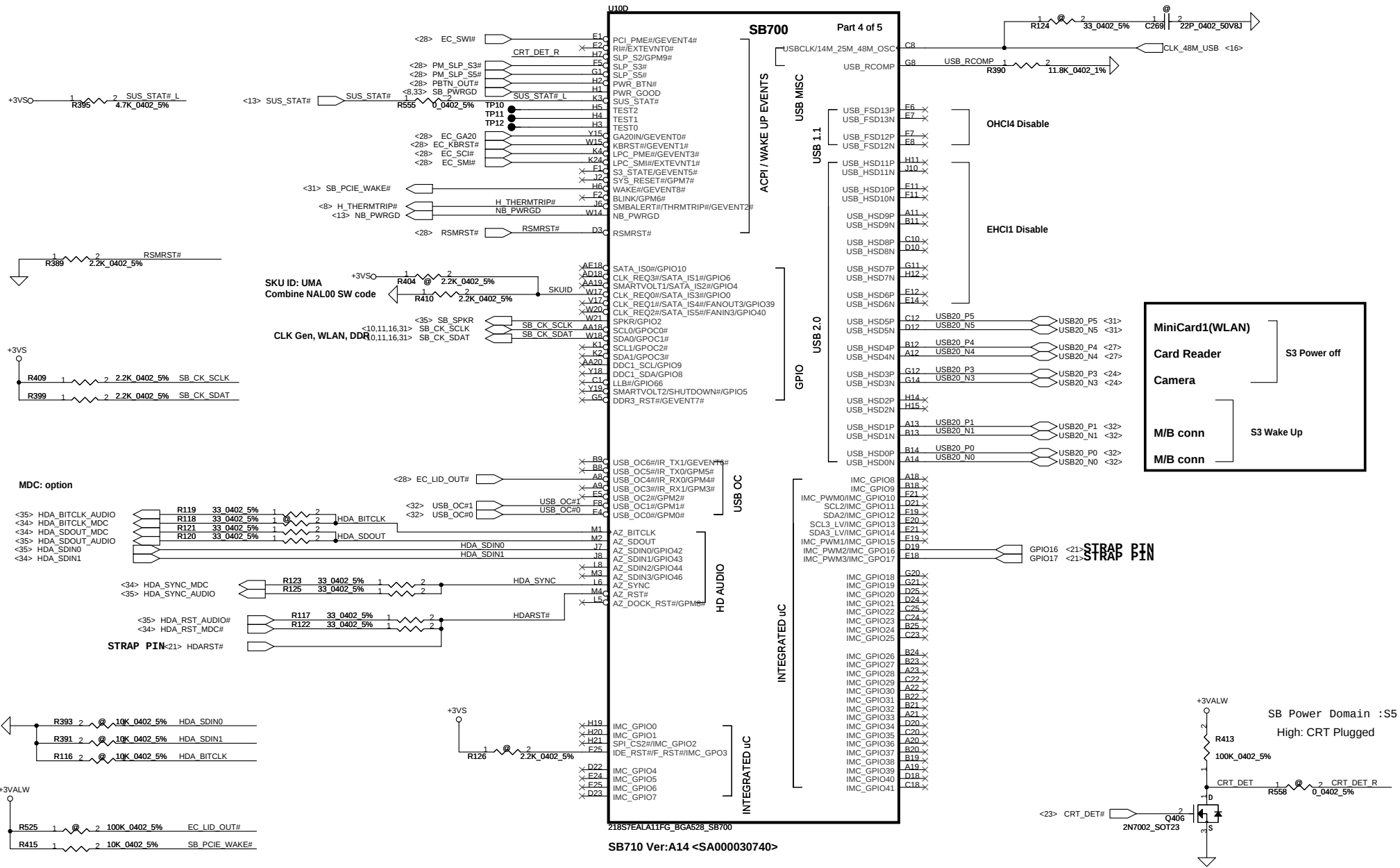
Main-SLG8SP626VTR-SA00001Z310
Second-ICS9LPRS488CKLFT-SA000023H10

SEL_HTT66	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output
SEL_SATA	1*	SS 100M SATA SRC6 output
	0	SS 100M SATA SRC6 output

* default

SEL_27M No used	1	configure as 27M and 27M_SS output
	0	configure as SRC_7 output

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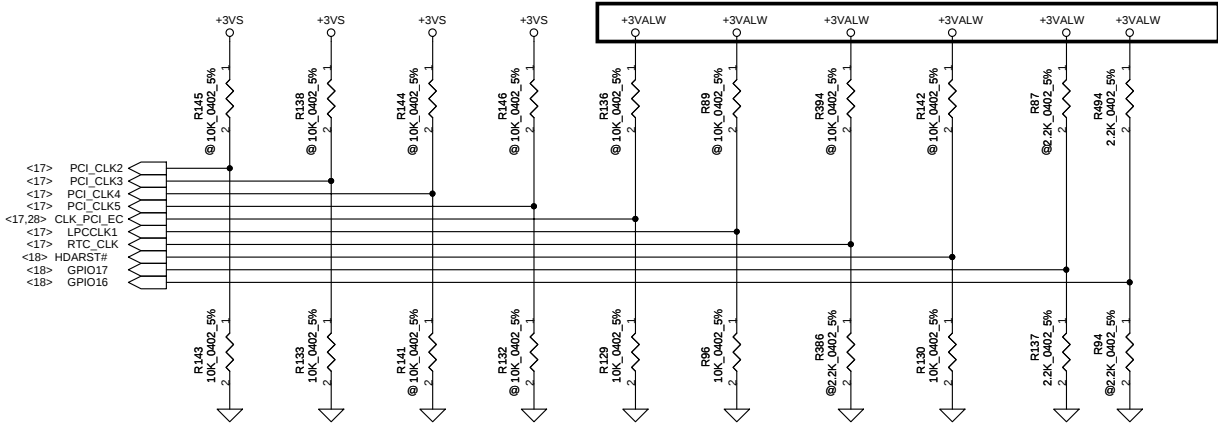


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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default L,NC) L,L = FWH ROM

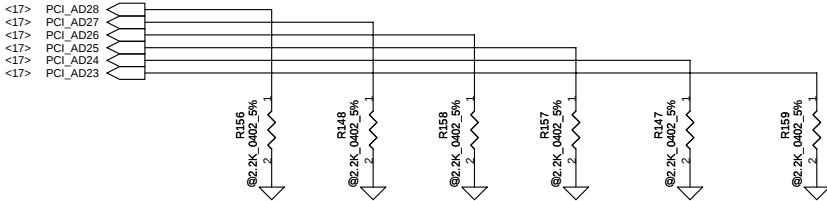


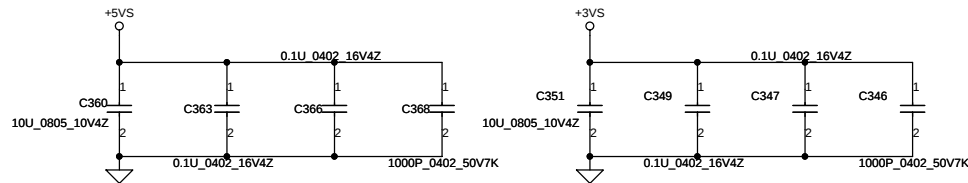
DEBUG STRAPS

DEBUG STRAPS

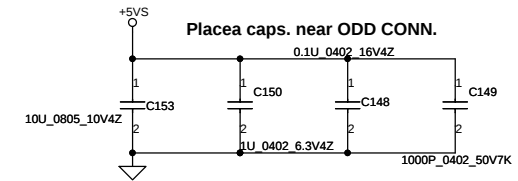
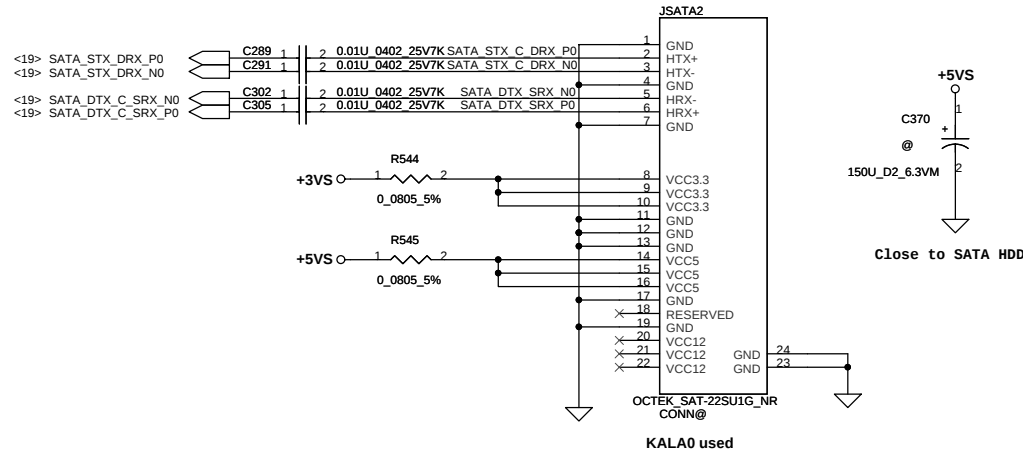
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

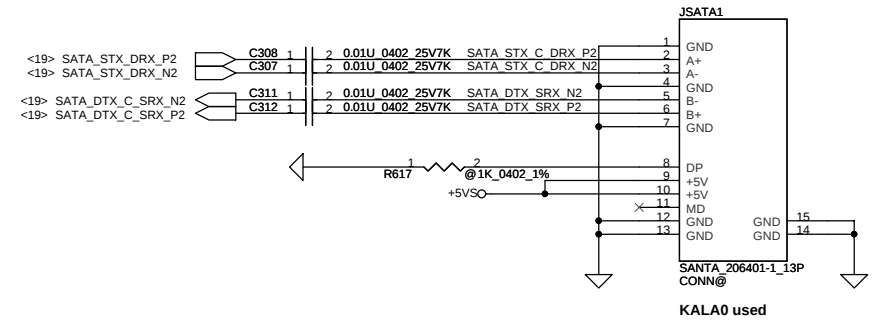




SATA HDD CONN

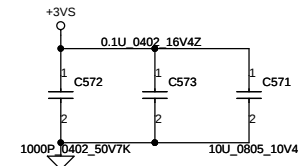
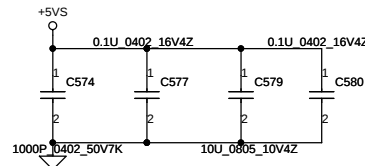
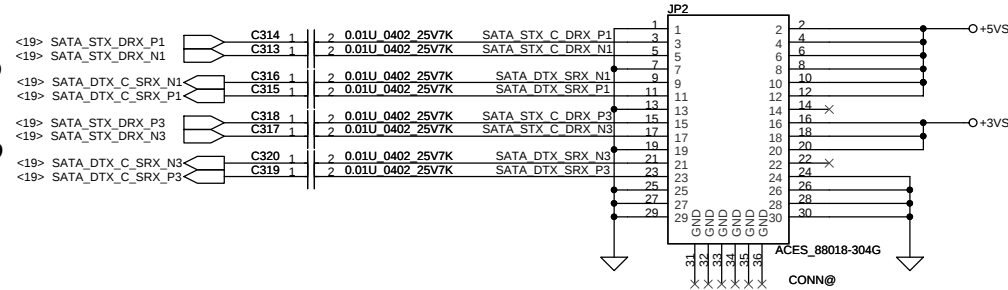


SATA ODD CONN



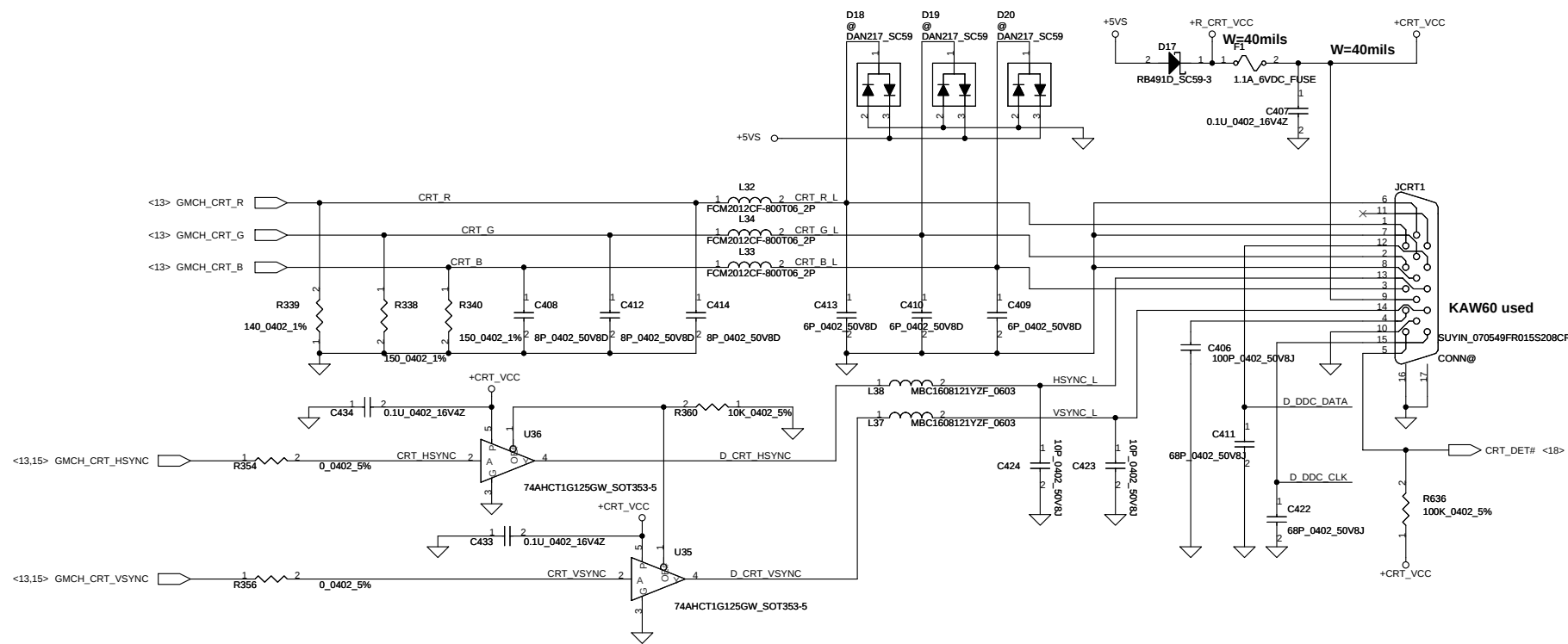
Second HDD

Second ODD

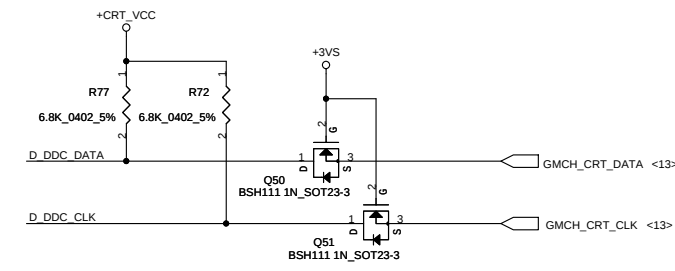


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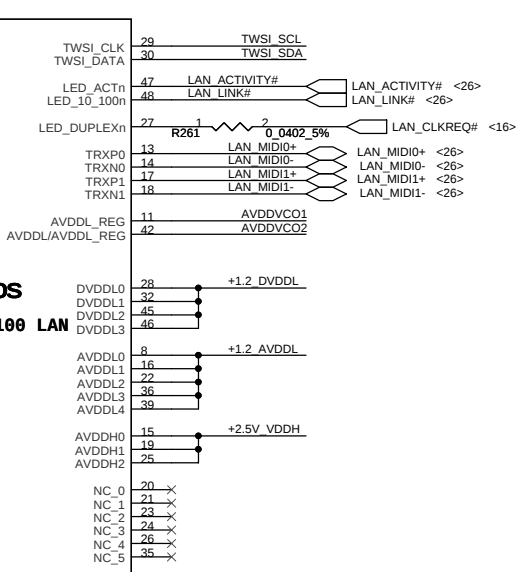
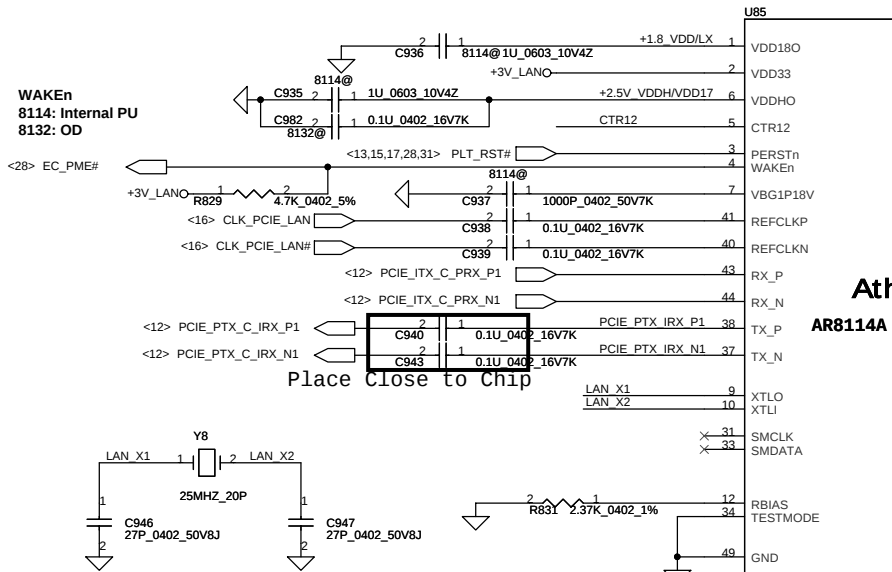
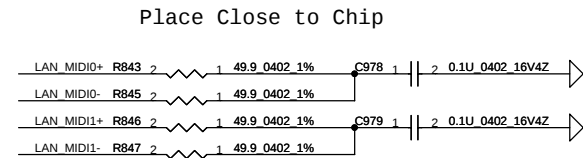
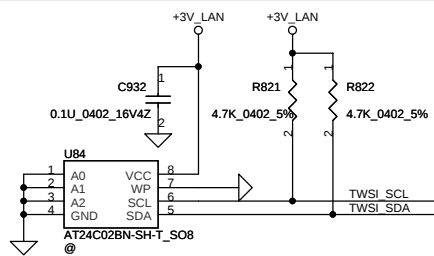
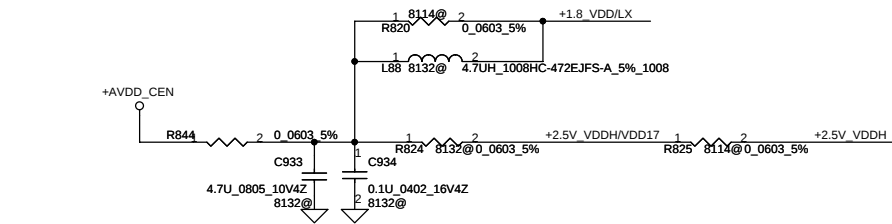
CRT Connector



Close to Conn side



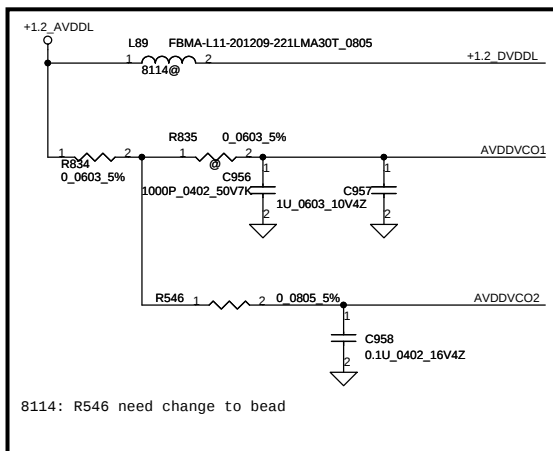
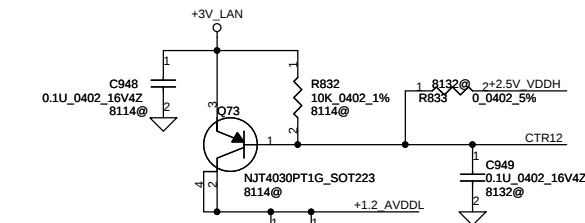
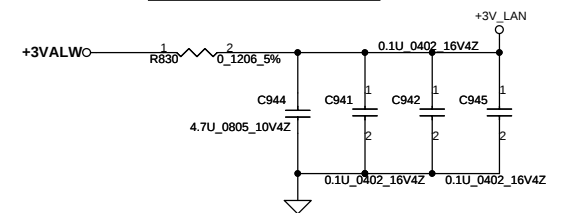
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Atheros
AR8114A 10/100 LAN

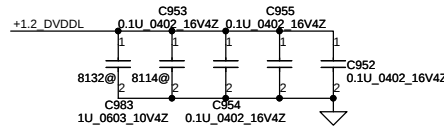
change to AR8132L-AL1E

Layout Notice : Close to chip

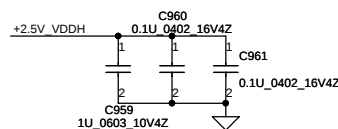


8114: R546 need change to bead

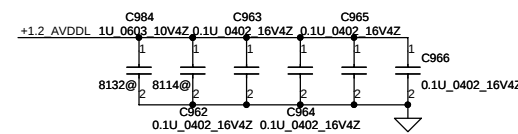
Place Close to Pin 28、32、45、46



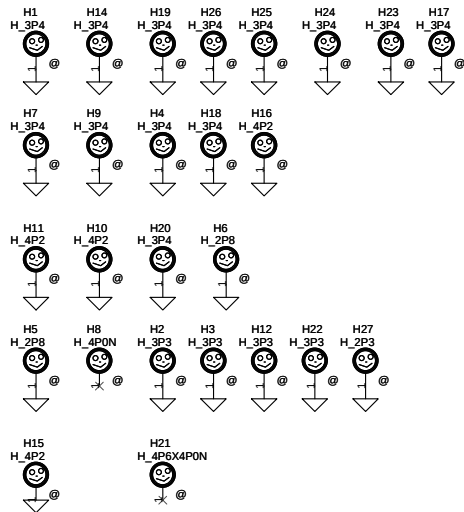
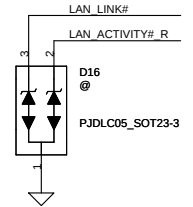
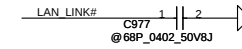
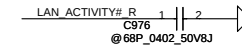
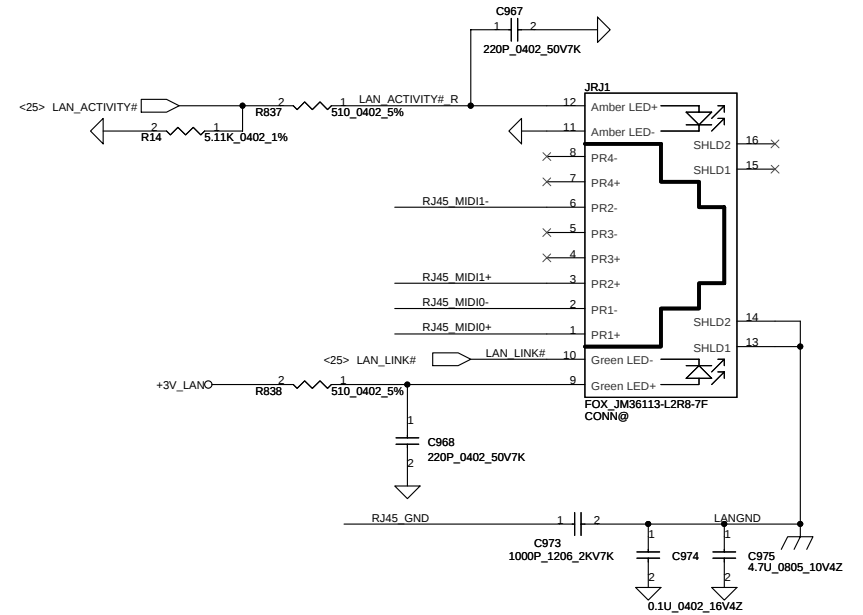
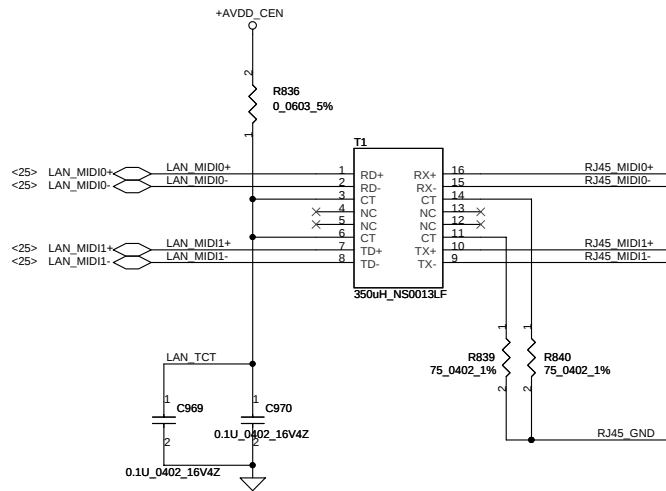
Place Close to Pin15、19、25



Place Close to Pin8、16、22、36、39

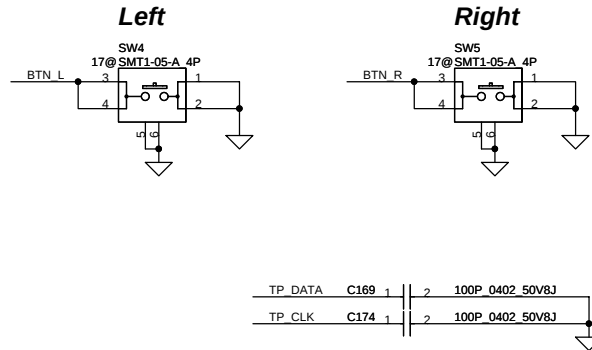


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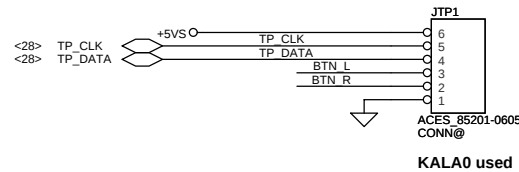


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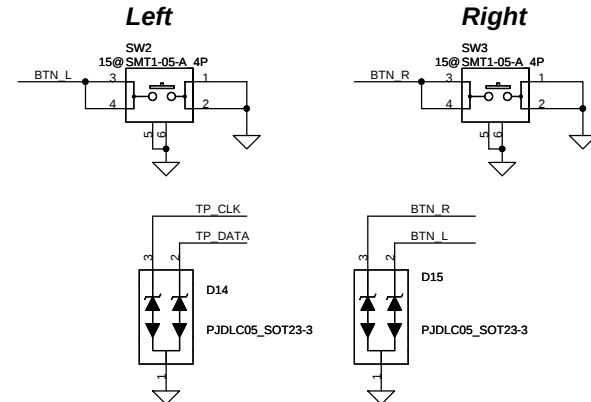
For 17"



To TP/B Conn.

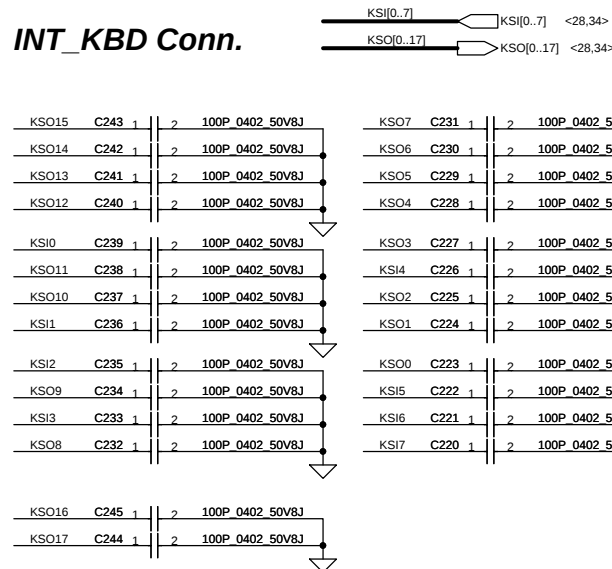


For 15"



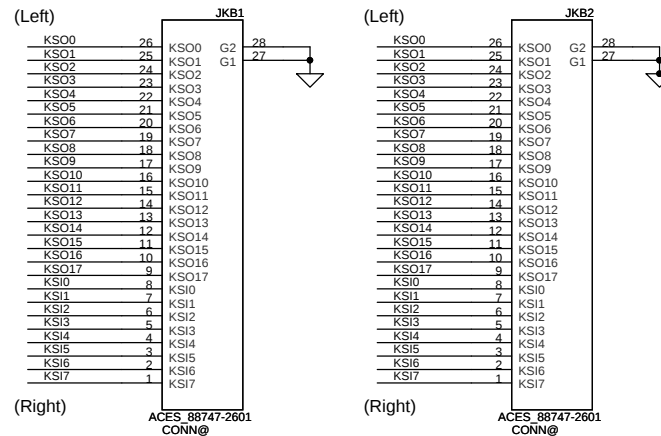
Change to SCA00000200

INT_KBD Conn.

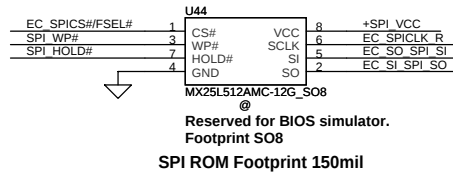
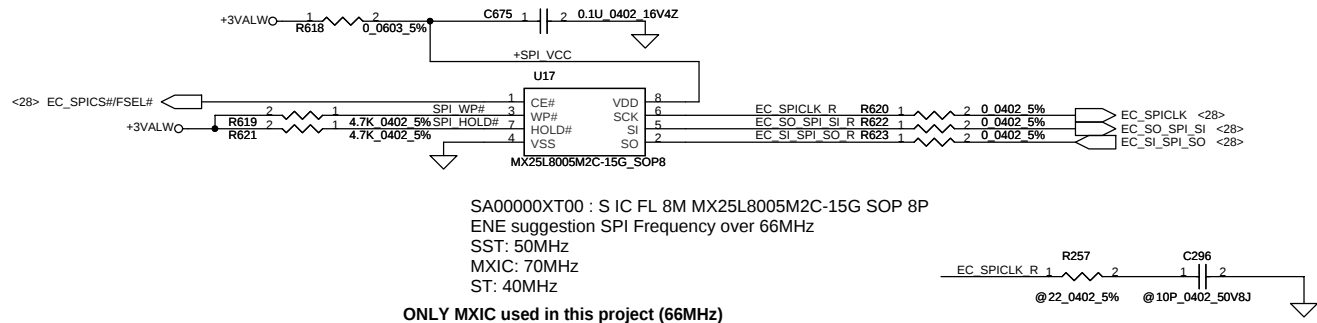


KB1 for 15"

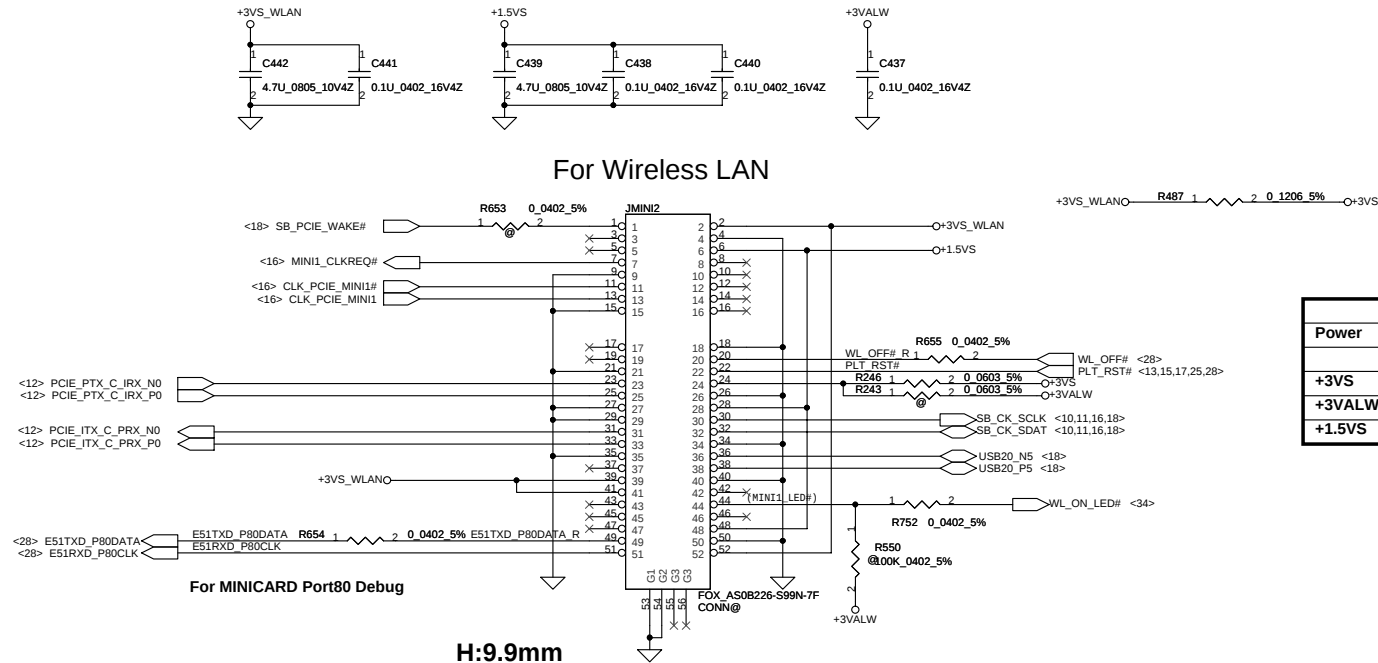
KB2 for 17"



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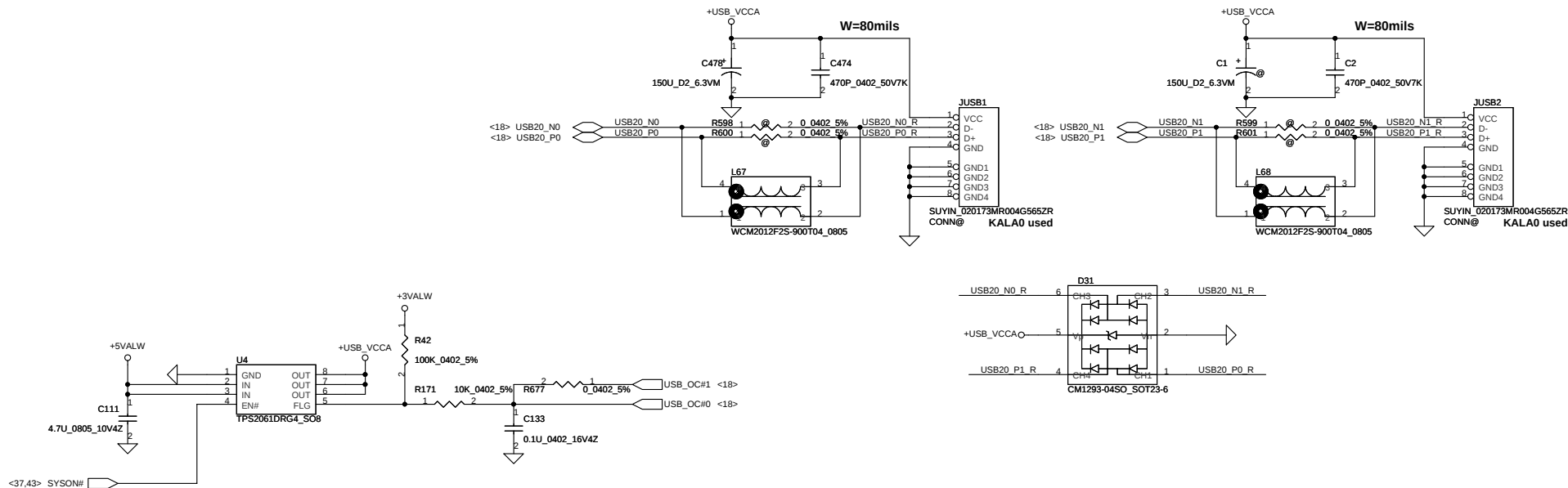
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Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3VALW	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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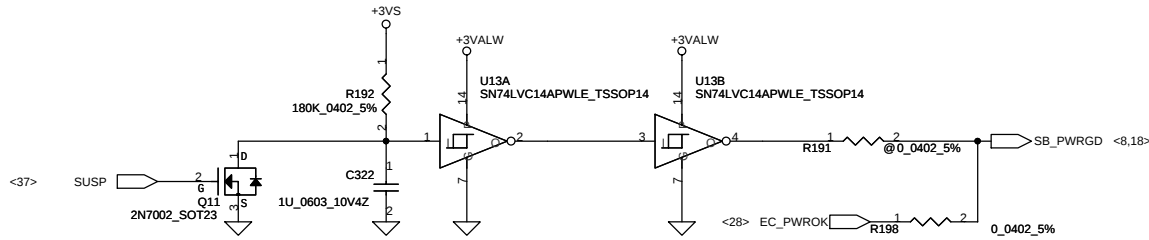
USB CONN. 1 & 2



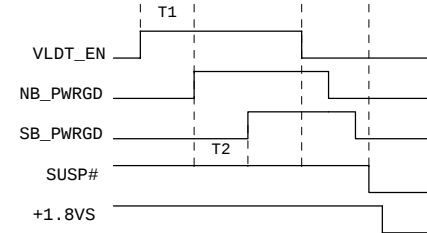
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Power ON Circuit

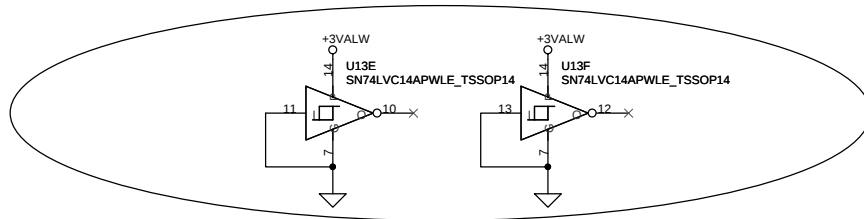
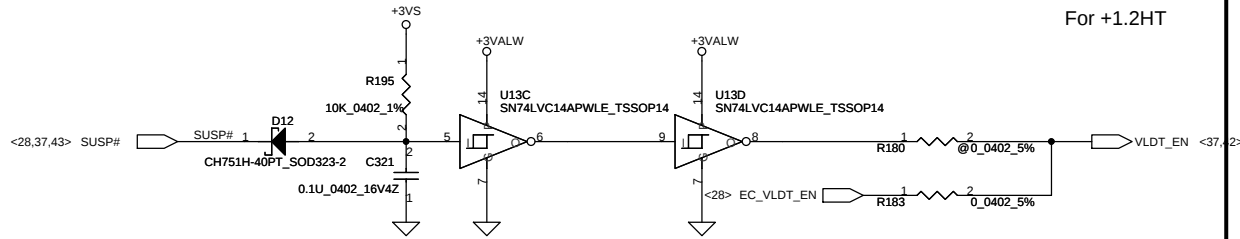
For South Bridge



note: T1 minimum 15ms, T2 minimum 33ms/maximum 500ms, SUSP# goes to low after SB_PWRGD goes to low for power down.



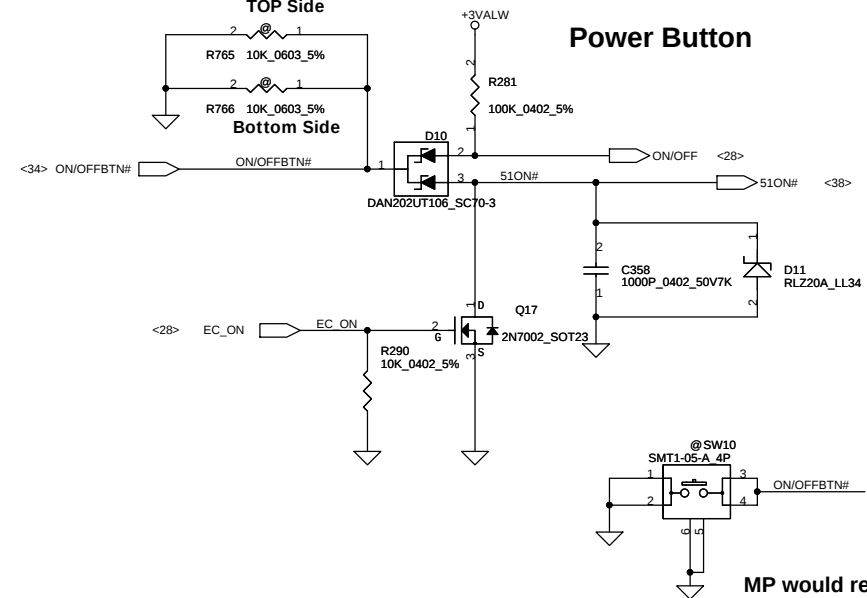
For +1.2HT



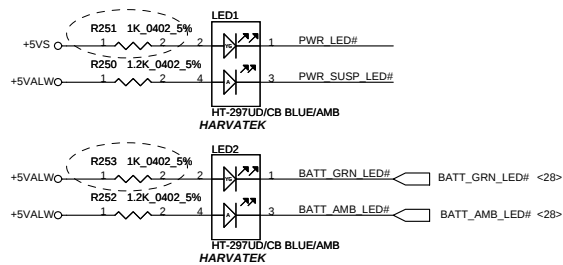
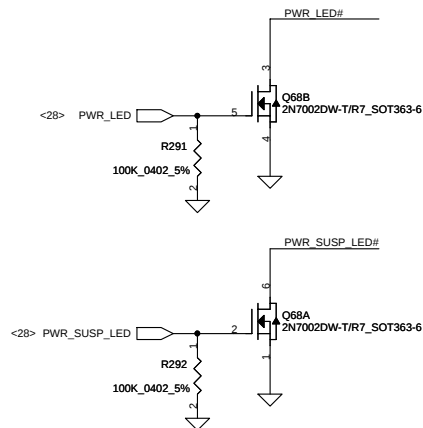
TOP Side

Bottom Side

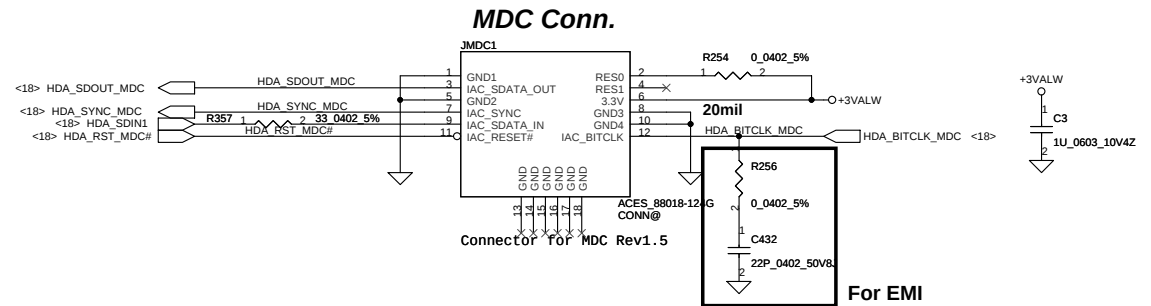
Power Button



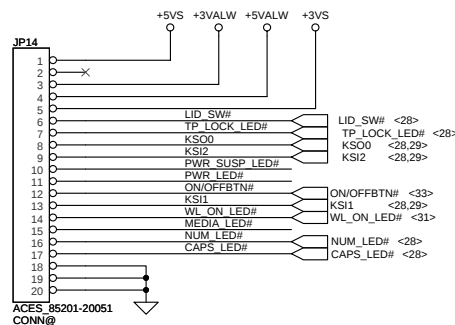
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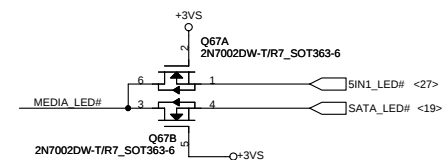
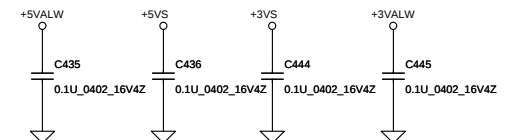
BLUE/AMB LED



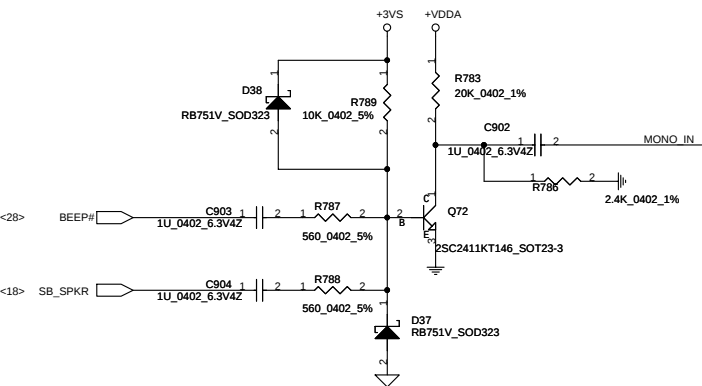
To PWR LED/B



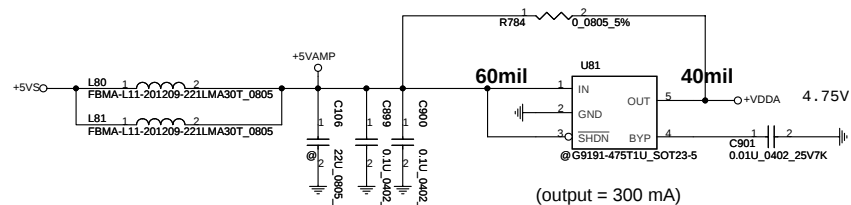
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KSI1	WL_BTN#
KSI2	TP_LOCK_BTN#
KSI3	
KSI4	
KSI5	
KSI6	



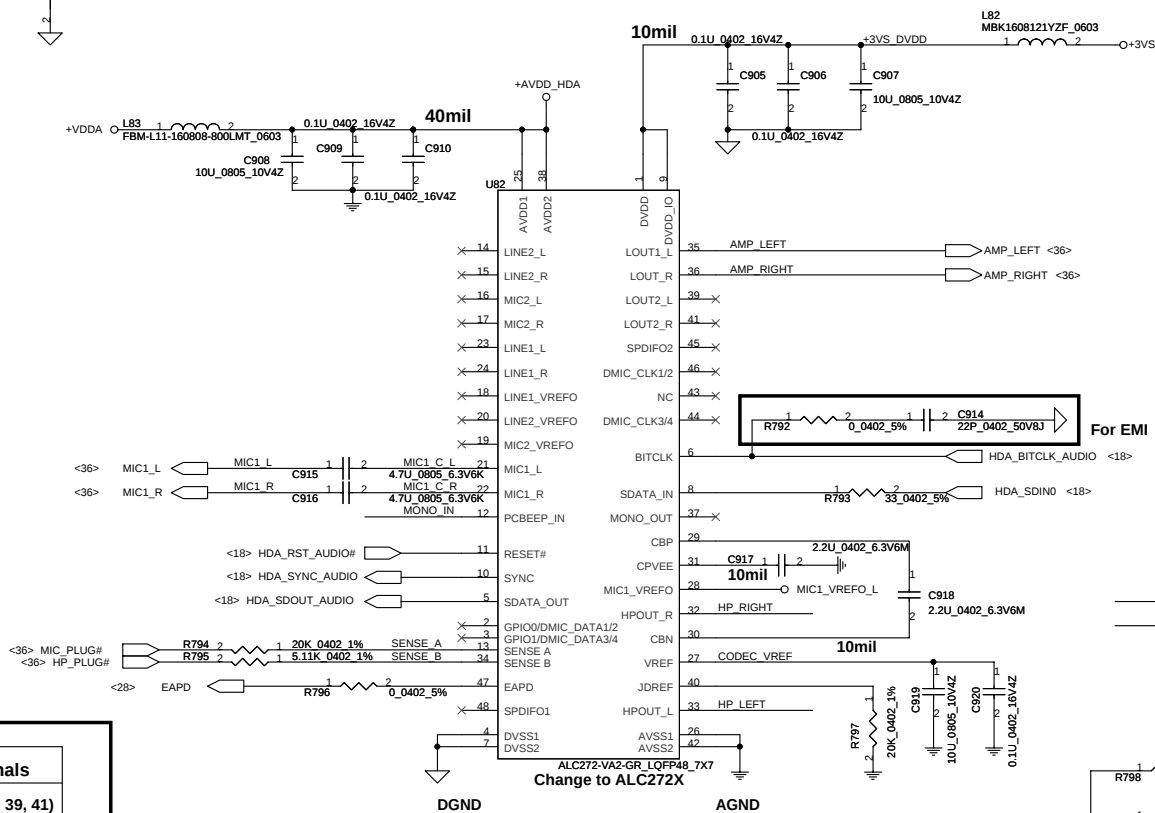
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HD Audio Codec



(output = 300 mA)



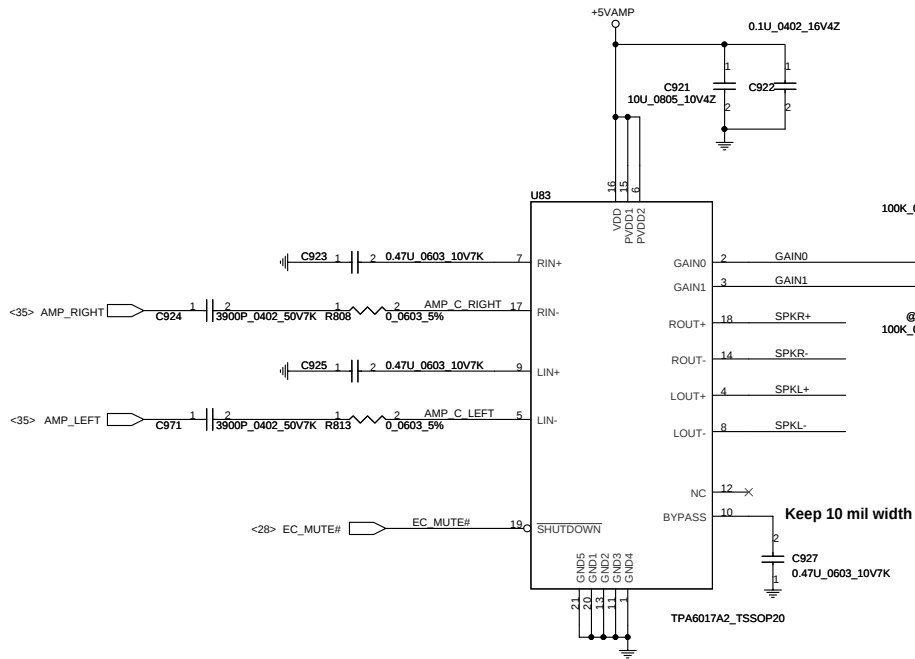
For EMI

update this table

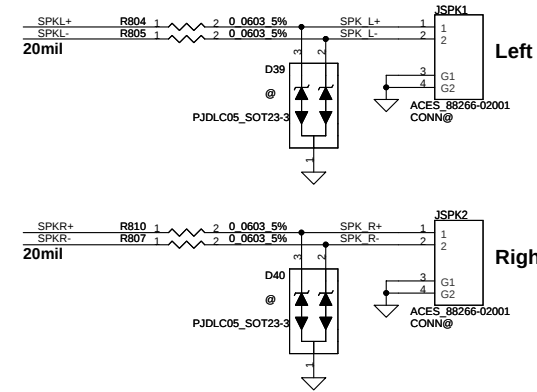
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

Change to ALC272X

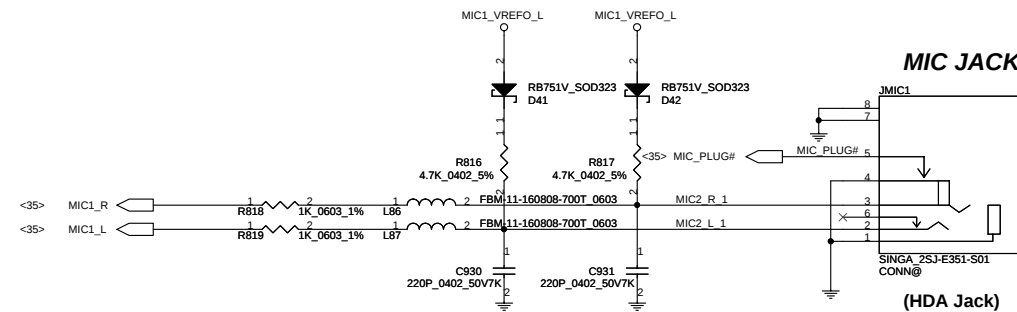
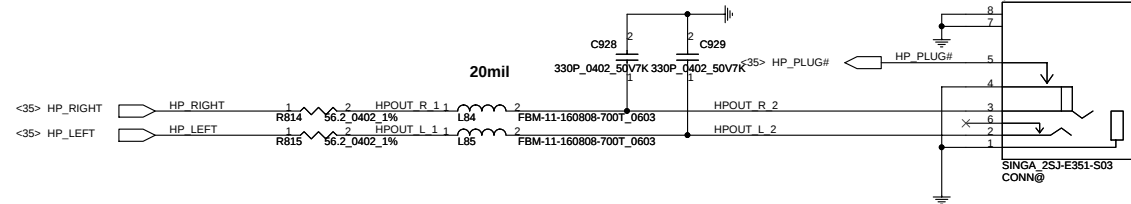
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Int. Speaker Conn.

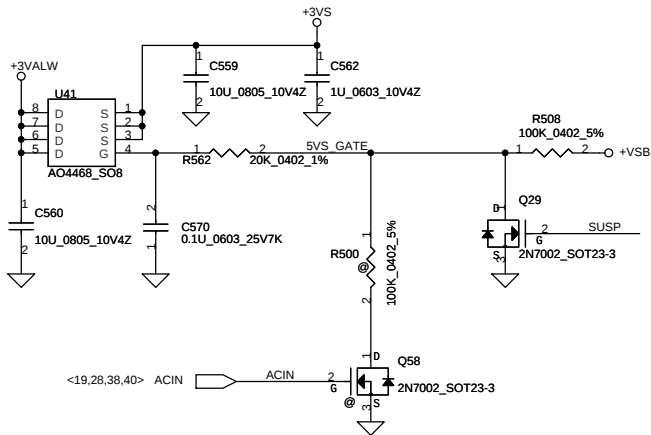


LINE Out/Headphone Out

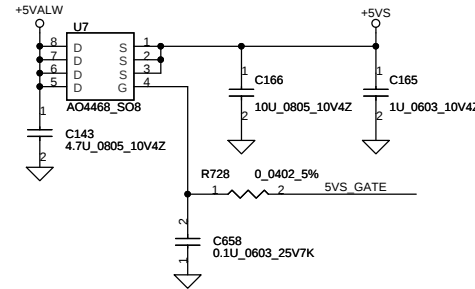


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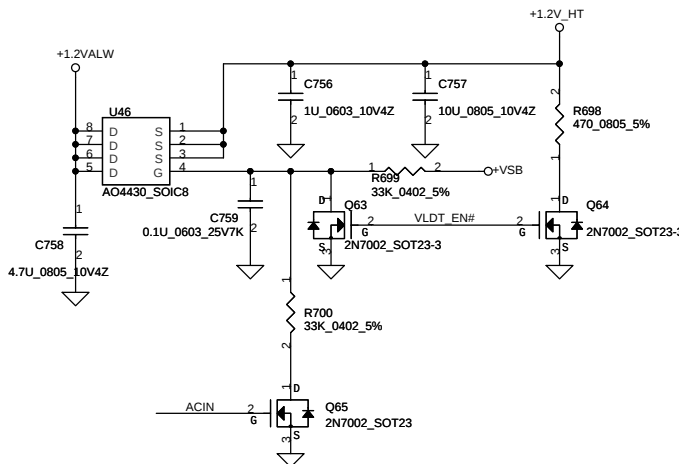
+3VALW TO +3VS



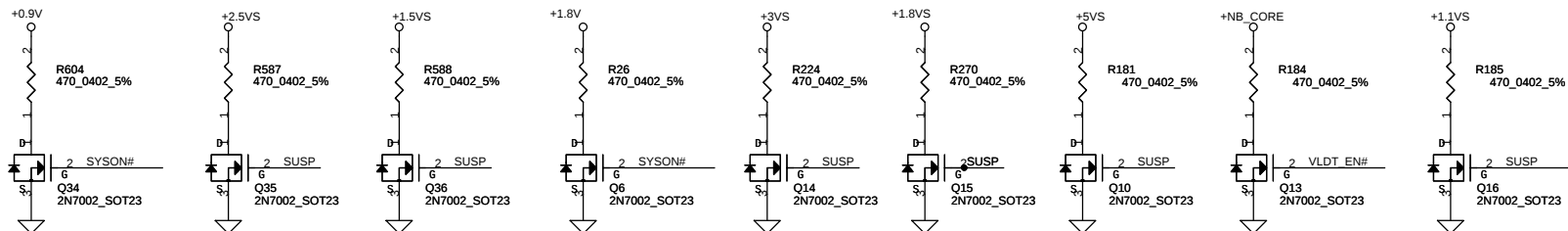
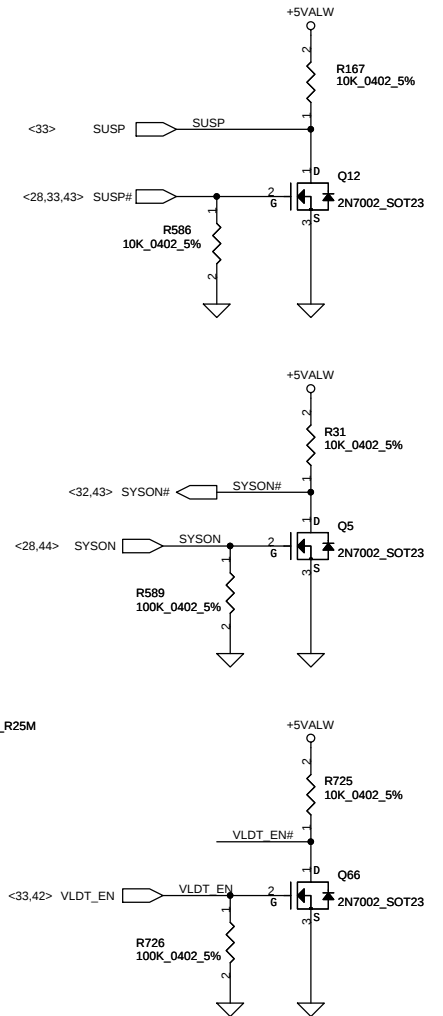
+5VALW TO +5VS



+1.2VALW TO +1.2V_HT

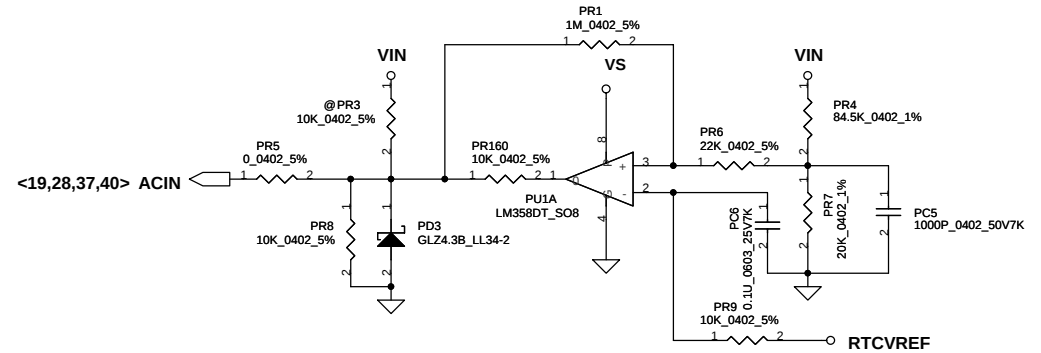
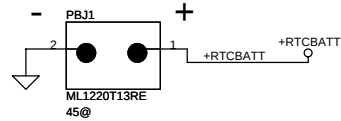
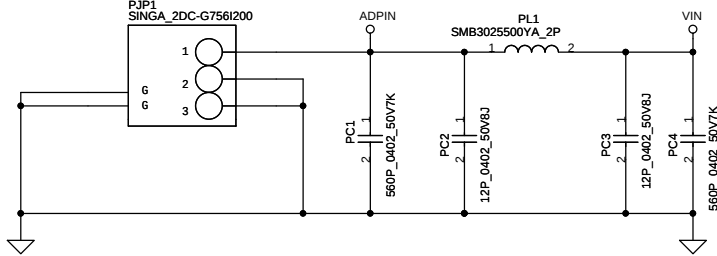


For PWR request

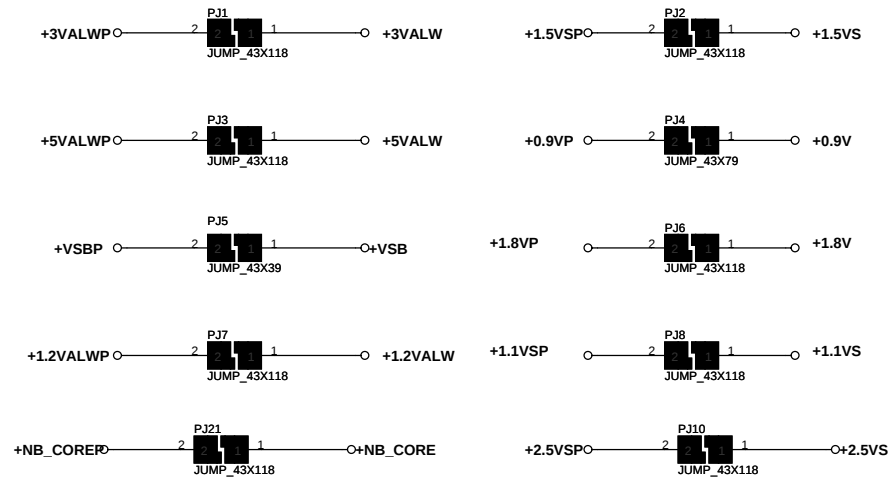
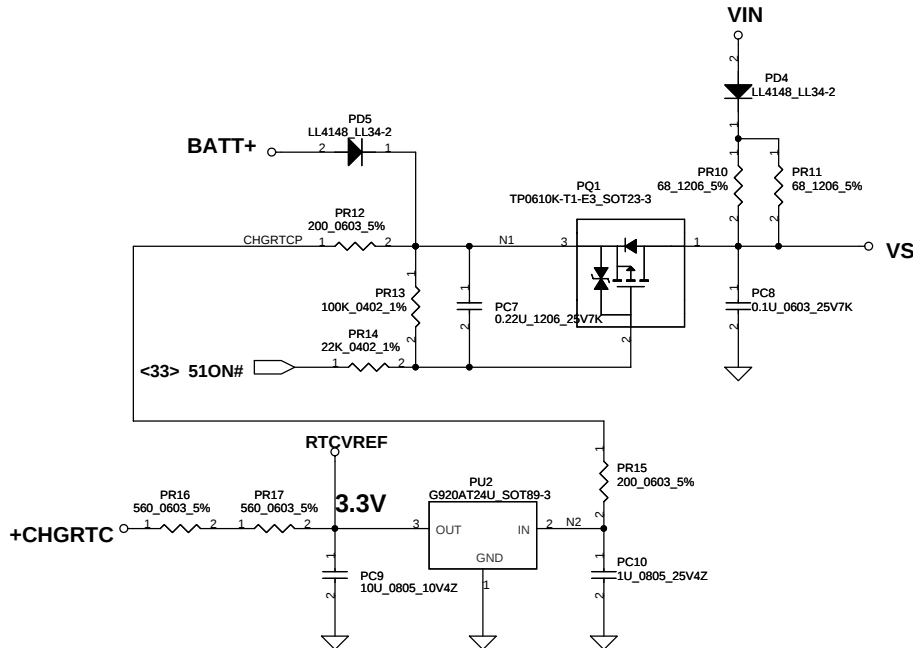


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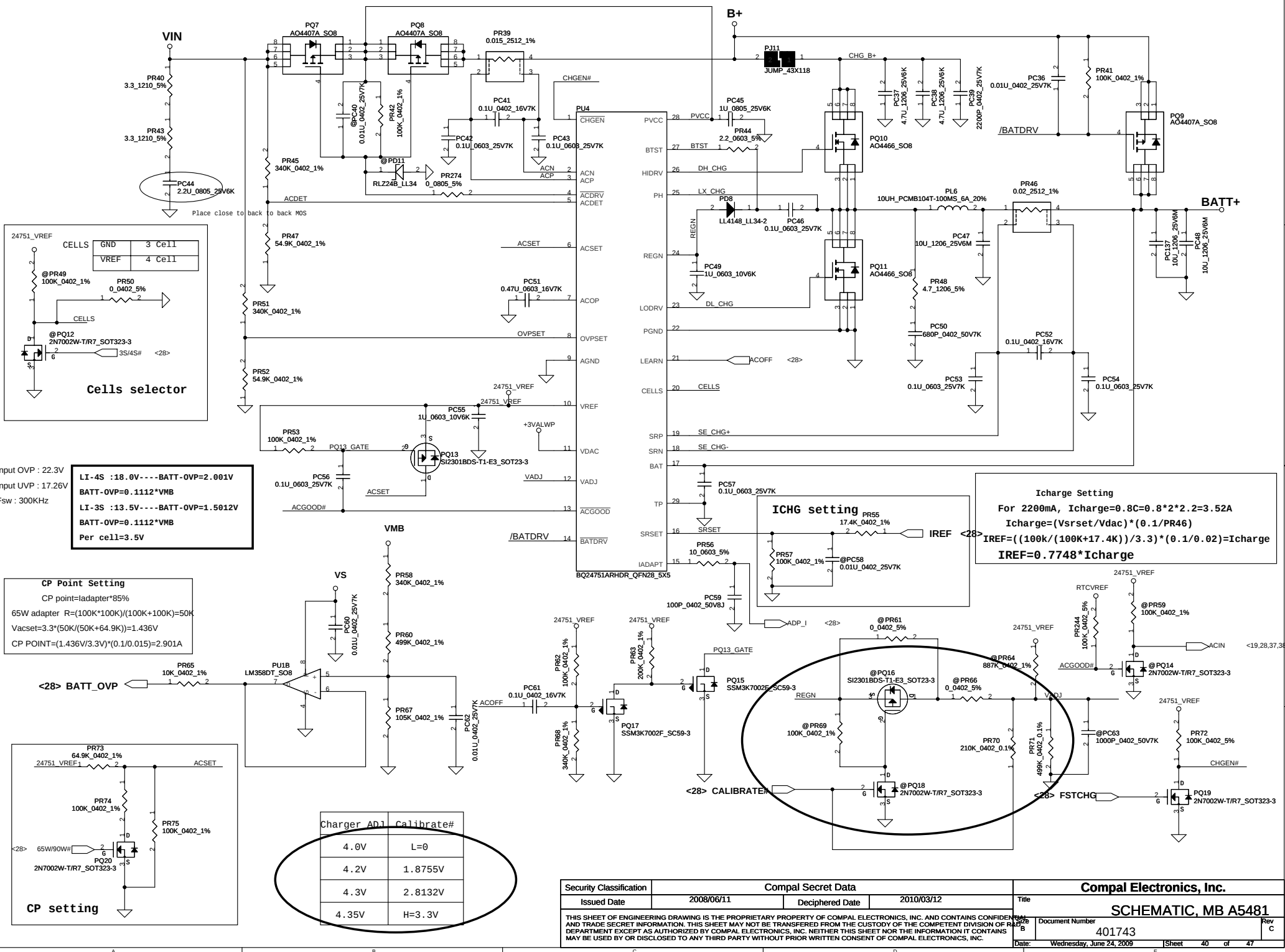
DC231000500

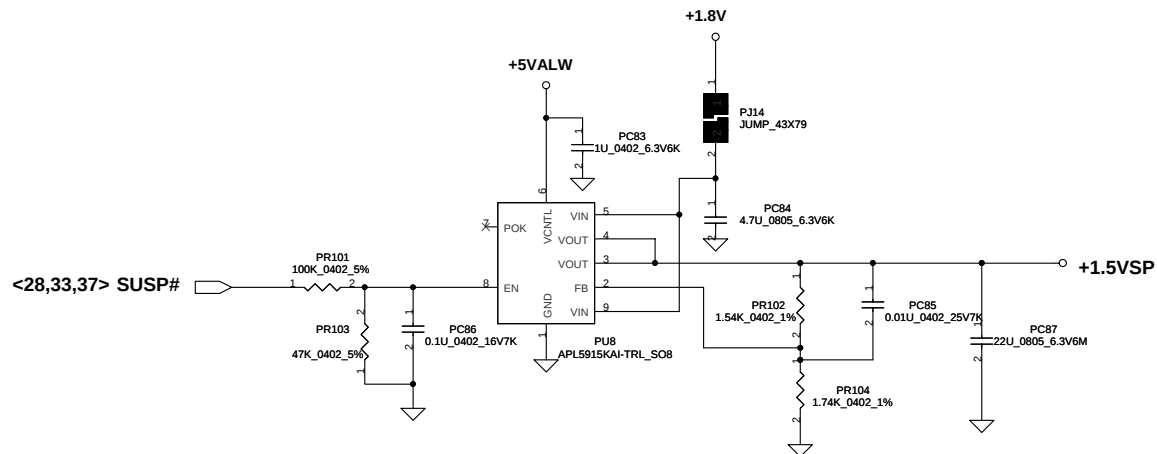
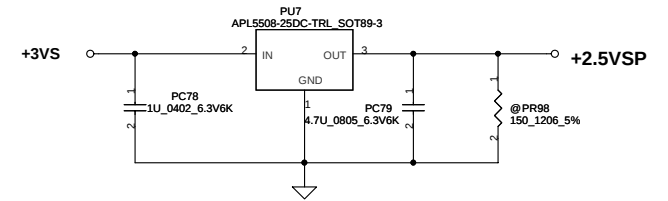
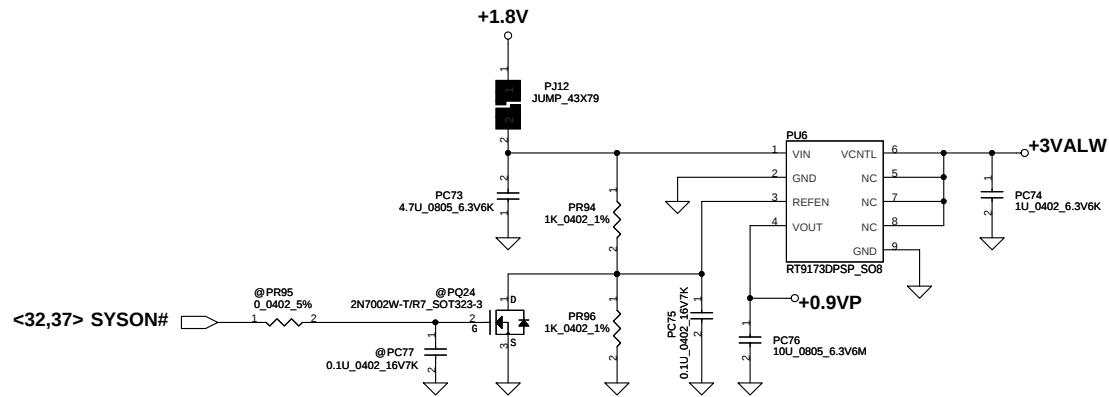


Vin Dectector			
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V

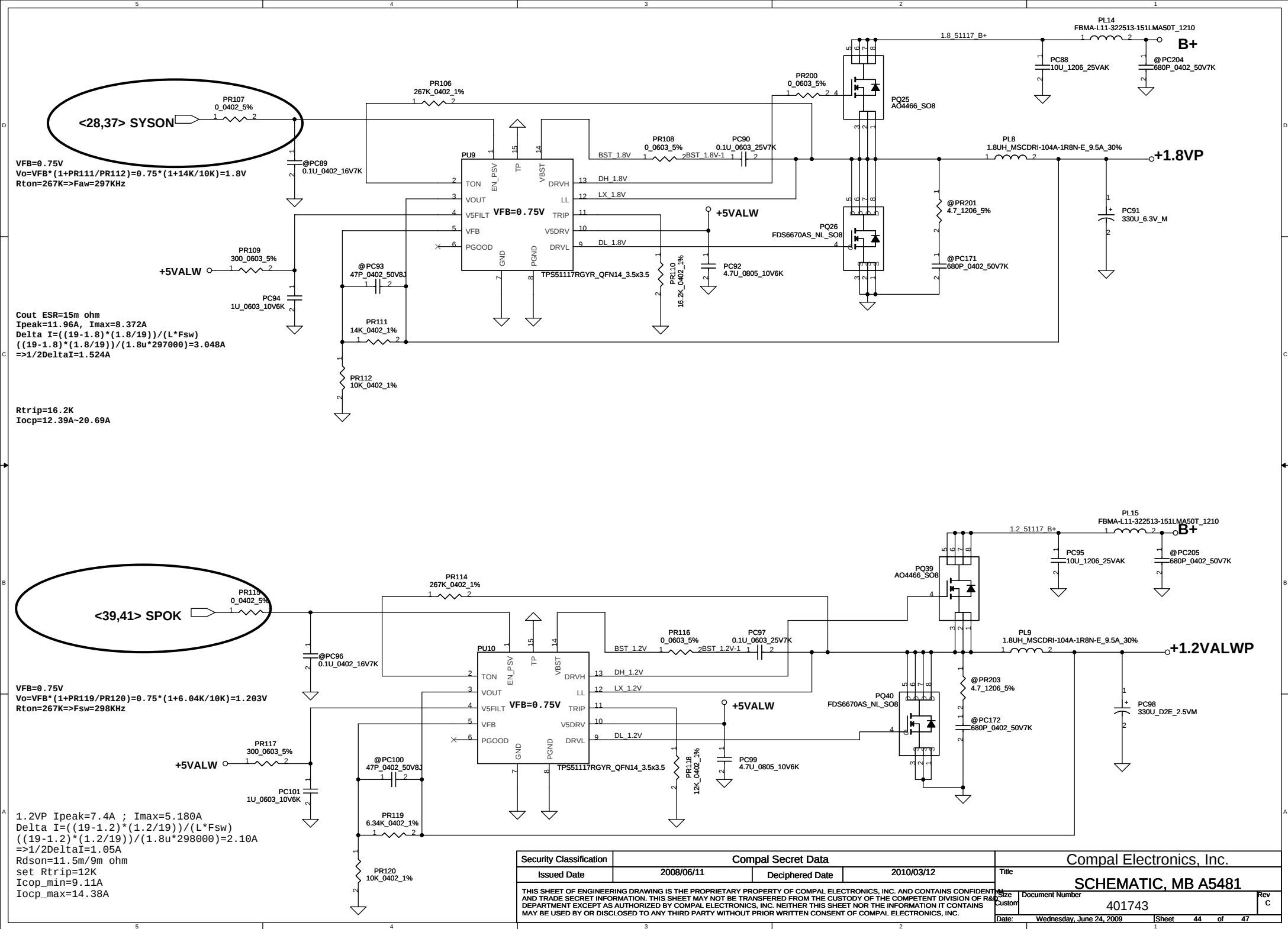


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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	HW required to adjust from 1.14V to 1.12V	HW required to adjust from 1.14V to 1.12V	0.1	42	Change PR271 from SD034300180 (S RES 1/16W 3K +-1% 0402) to SD034324180 (S RES 1/16W 3.24K 0402 1%)	09, 05/07	to PVT
2	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Add PC208 SE076104K80 (S CER CAP .1U 16V K X7R 0402)	09, 05/07	to PVT
3	Power sequense adjust.	HW required to adjust power sequense.	0.1	42	Change PR247 from SD028000080 (S RES 1/16W 0 +-5% 0402) to SD028130180 (S RES 1/16W 1.3K 0402 5%)	09, 05/07	to PVT
4	NB_COREP working frequency has issue.	Because NB_COREP working frequency will be gltfer while system at heavy loading. Change to larger ESR Cap will be solve.	0.1	42	Change PC210 from SGA19331D00 (S POLY C 330U 2.5V M D2 TPE LESR15M H1.8) to SGA00002B00 (S POLY C 330U 6.3V M D2E ESR25M TPE H1.8)	09, 05/07	to PVT
5	BOM error	BOM error	0.1	42	Add PR270 SD28100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
6	BOM error	BOM error	0.1	42	Change PR103 from SD028470280(S RES 1/16W 47K 0402 5%) to SD028100280(S RES 1/16W 10K 0402 5%)	09, 05/07	to PVT
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Version change list (P.I.R. List) for HW									
Item	Reason for change	Modify List	PG#	Date	Item	Reason for change	Modify List	Rev.	PG#
1	PWR update circuit			4/9	26				
2	BOM change	R118 reserve	P.18	4/9	27				
3	BOM change	Change R178, R179 to 90.9/158 ohm	P.16	4/9	28				
4	BOM change	R30, R39 reserve	P.24	4/9	29				
5	BOM change	Add C30	P.38	4/9	30				
6	BOM change	Add R634, R639	P.28	4/9	31				
7	BOM change	C383 Reserve	P.24	4/9	32				
8		Pop R419	P.20	4/10	33				
9	PWR update circuit			5/15					
10	For Panel flash issue	R1,D2 Reserve, pop R763	P.24	5/18					
11	For Panel flash issue	Add R414 and non-pop	P.24	5/18					
12	Lid_SW intial issue	Add R19	P.28	5/18					
13	HPET timer issue	Change C288,C290 to 33P	P.16	5/18					
14	BOM change	change C276,C279 10P to 27P	P.19	5/19					
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Version change list (P.I.R. List) for HW									
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