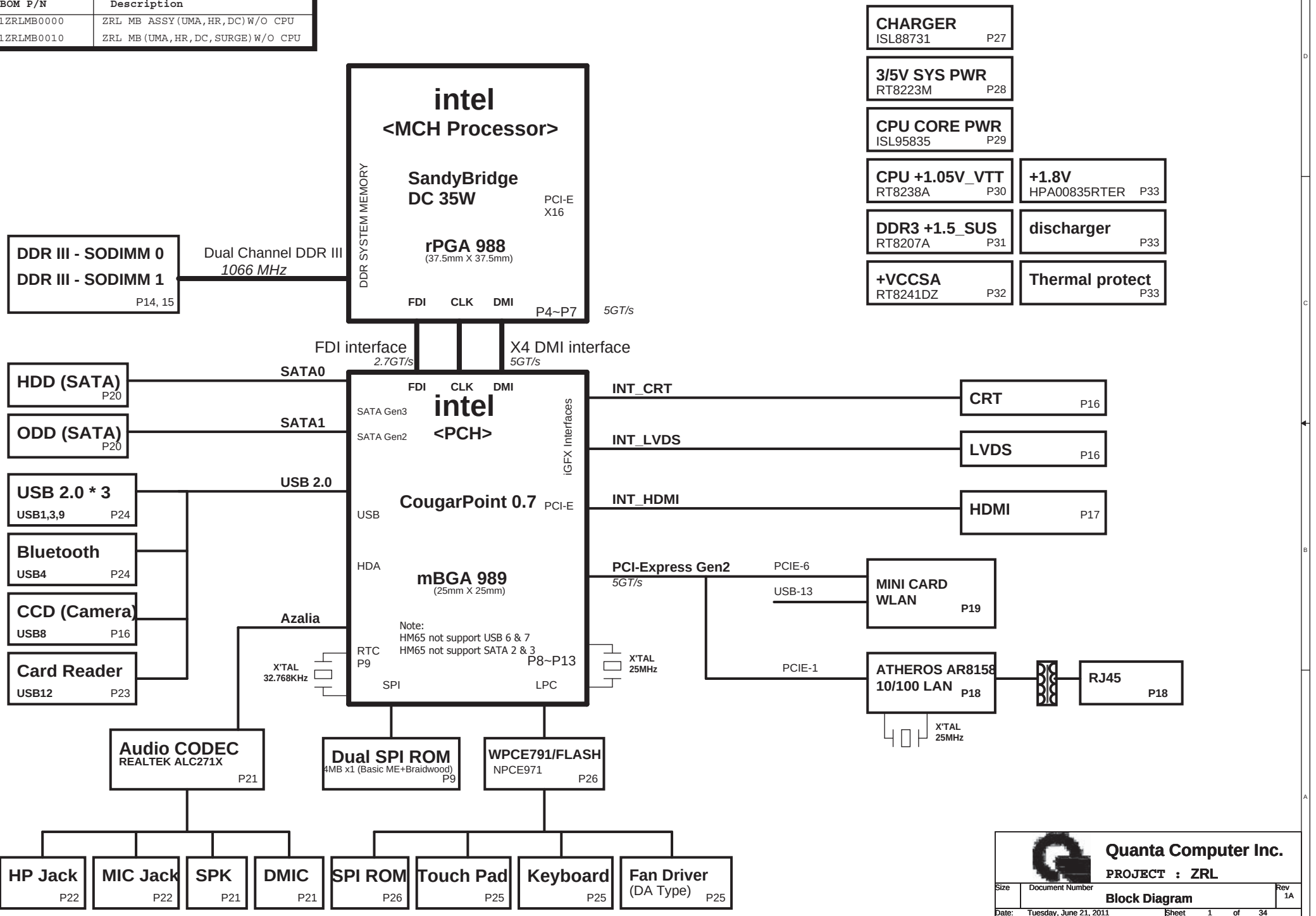
ZRL BLOCK DIAGRAM

VER : 1A	
BOM P/N	Description
31ZRLMB0000	ZRL MB ASSY(UMA,HR,DC)W/O CPU
31ZRLMB0010	ZRL MB(UMA,HR,DC,SURGE)W/O CPU



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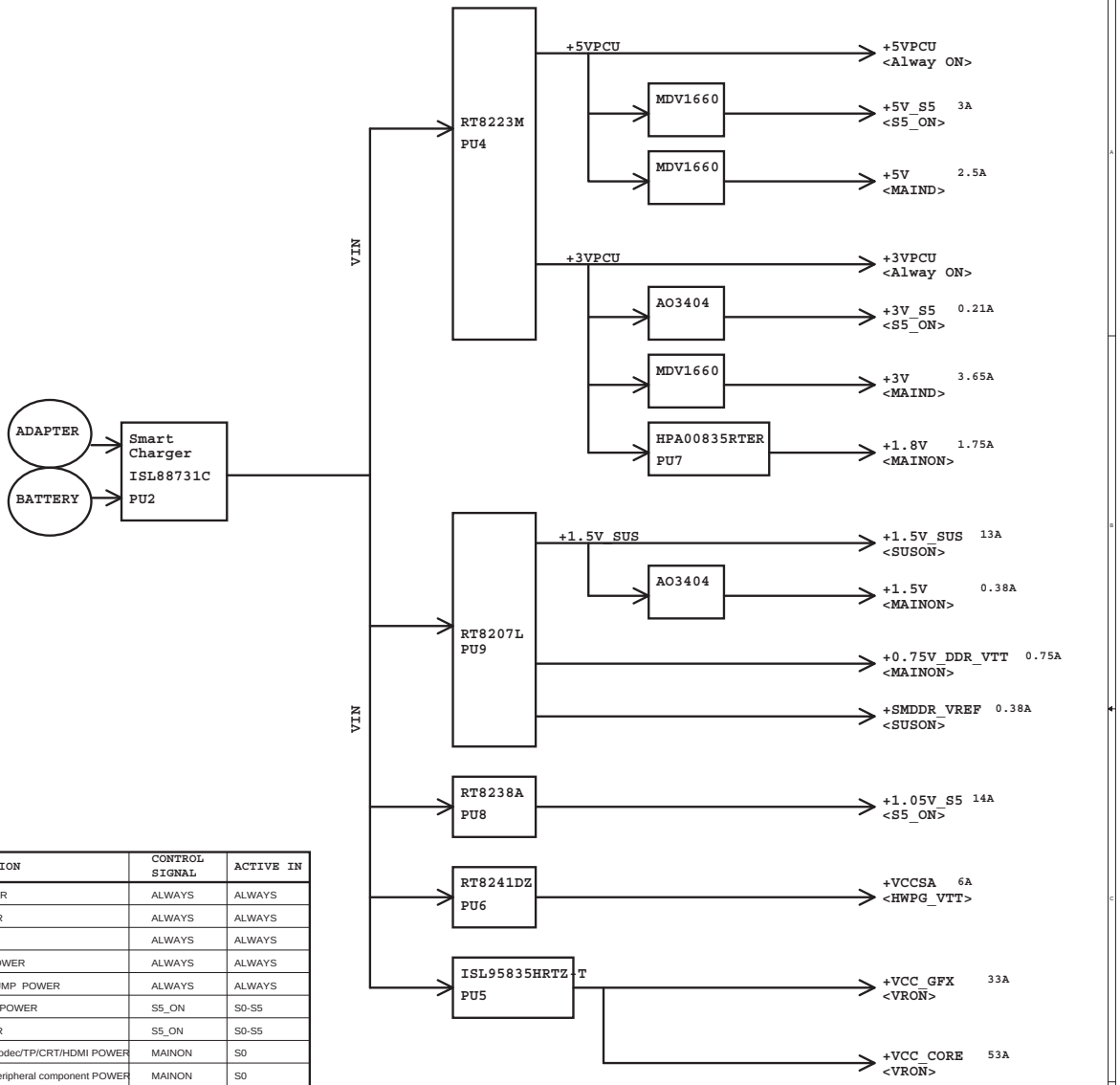
PROJECT : ZRL

Size	Document Number	Rev
	Block Diagram	1A

Date: Tuesday, June 21, 2011 Sheet 1 of 34

ZRL power tree



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Quanta Computer Inc.
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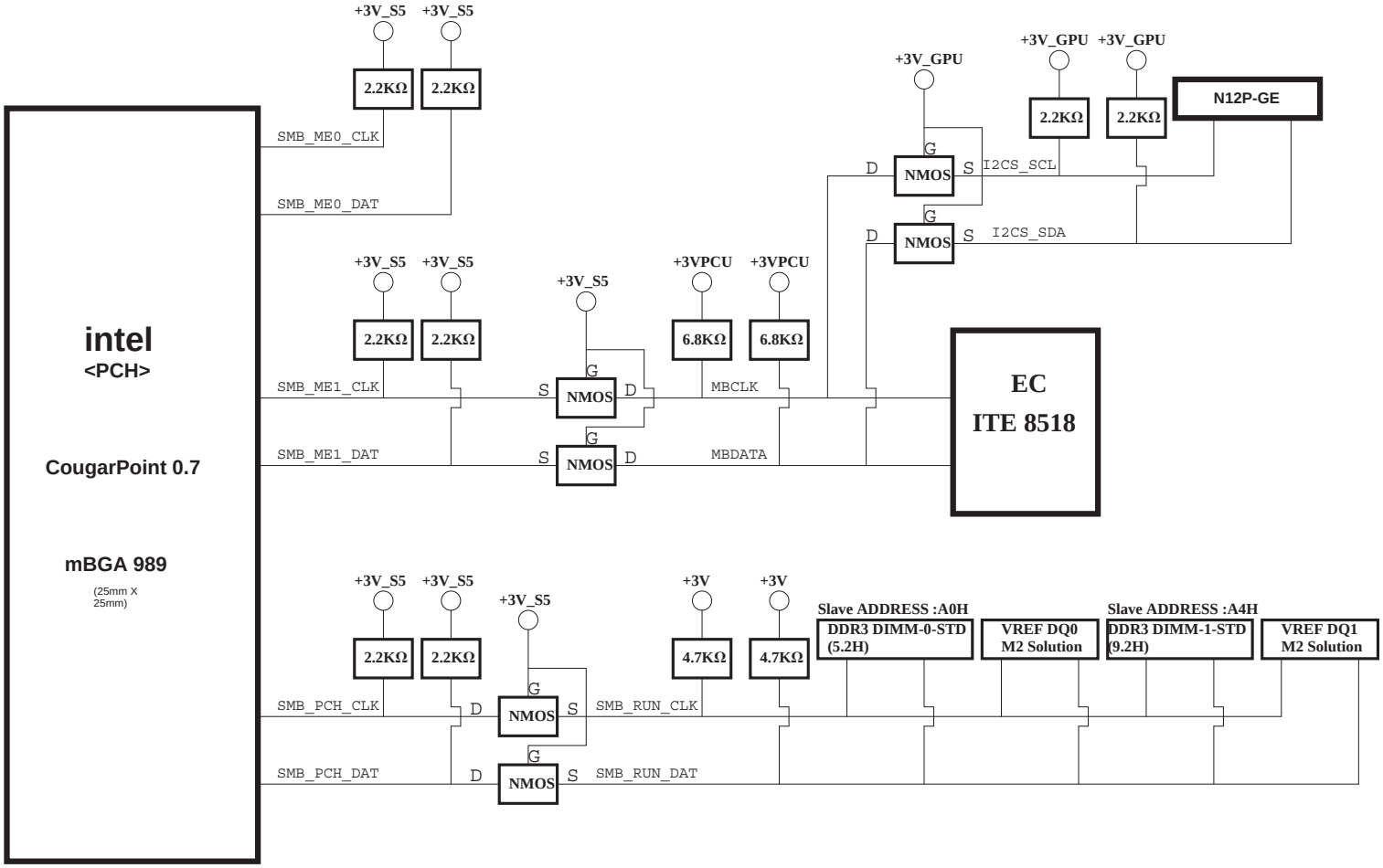


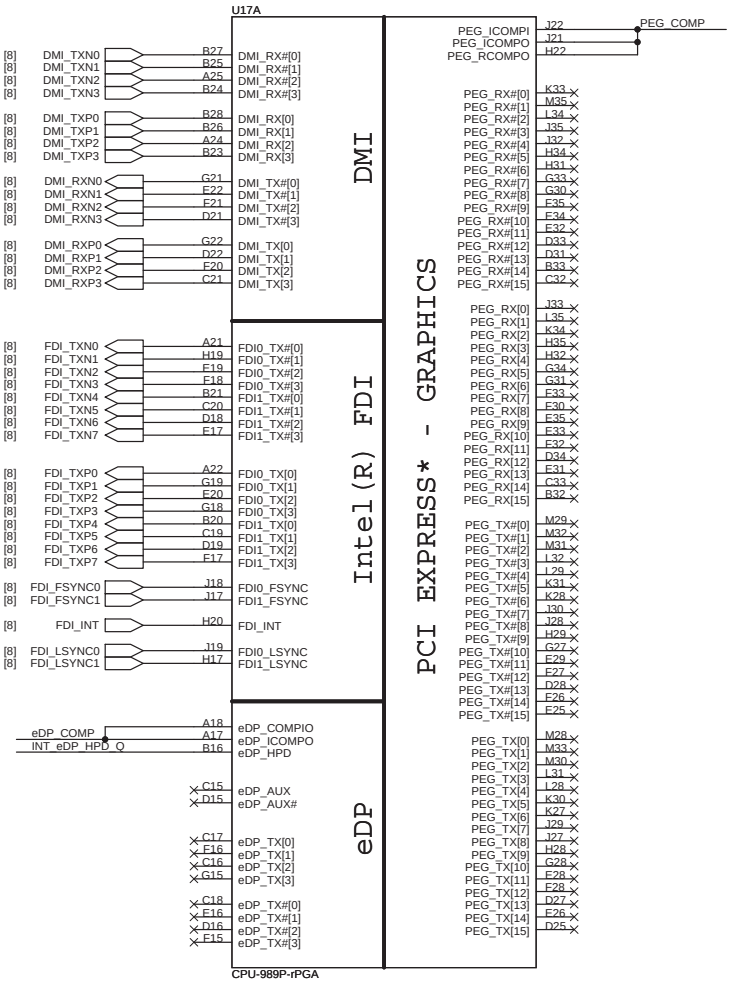
Quanta Computer Inc.
PROJECT : ZRL

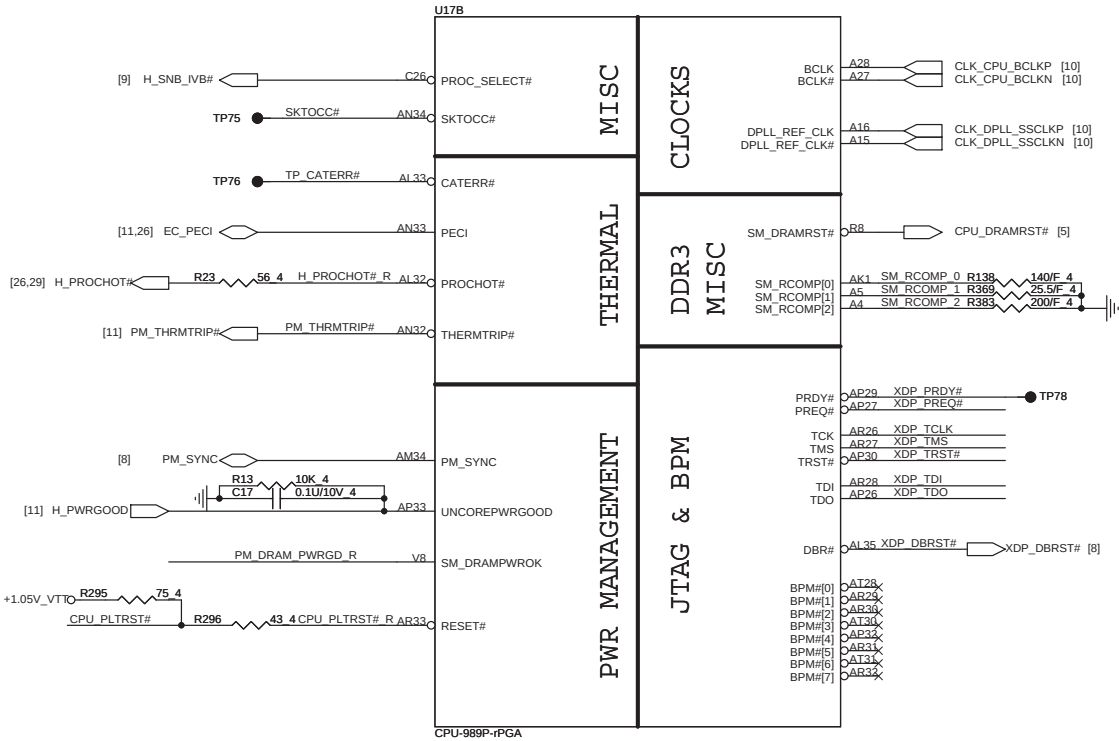
Size	Document Number	Rev
	SMBus Address	1A
Date: Tuesday, June 21, 2011	Sheet 3 of 34	

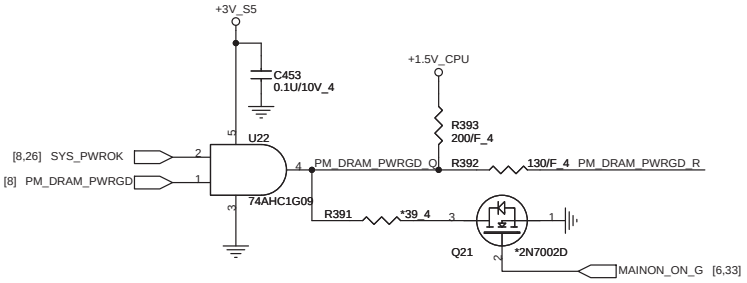
Sandy Bridge Processor (DMI,PEG,FDI)

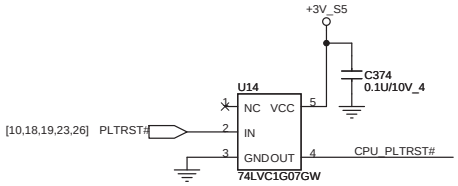
Sandy Bridge Processor (CLK,MISC,JTAG)

04

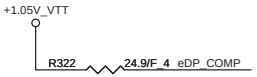




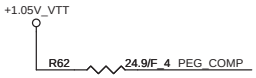




DP & PEG Compensation



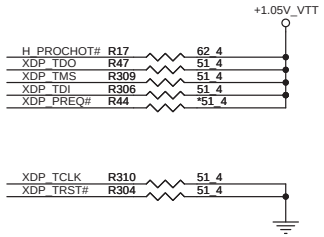
eDP_COMPIO and ICOMPO signals should
be shorted near balls and routed with
typical impedance <25 mohms

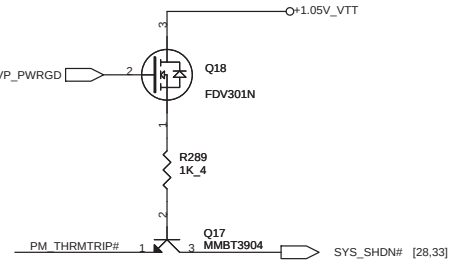


PEG_ICOMPI and RCOMPO signals should
be routed within 500 mils
typical impedance = 43 mohms

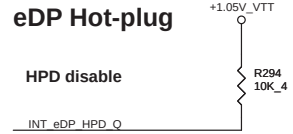
PEG_ICOMPO signals should
be routed within 500 mils
typical impedance = 14.5 mohms

Processor pull-up(CPU)





eDP Hot-plug



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Size	Document Number	Rev
	Sandy Bridge 1/4	1A
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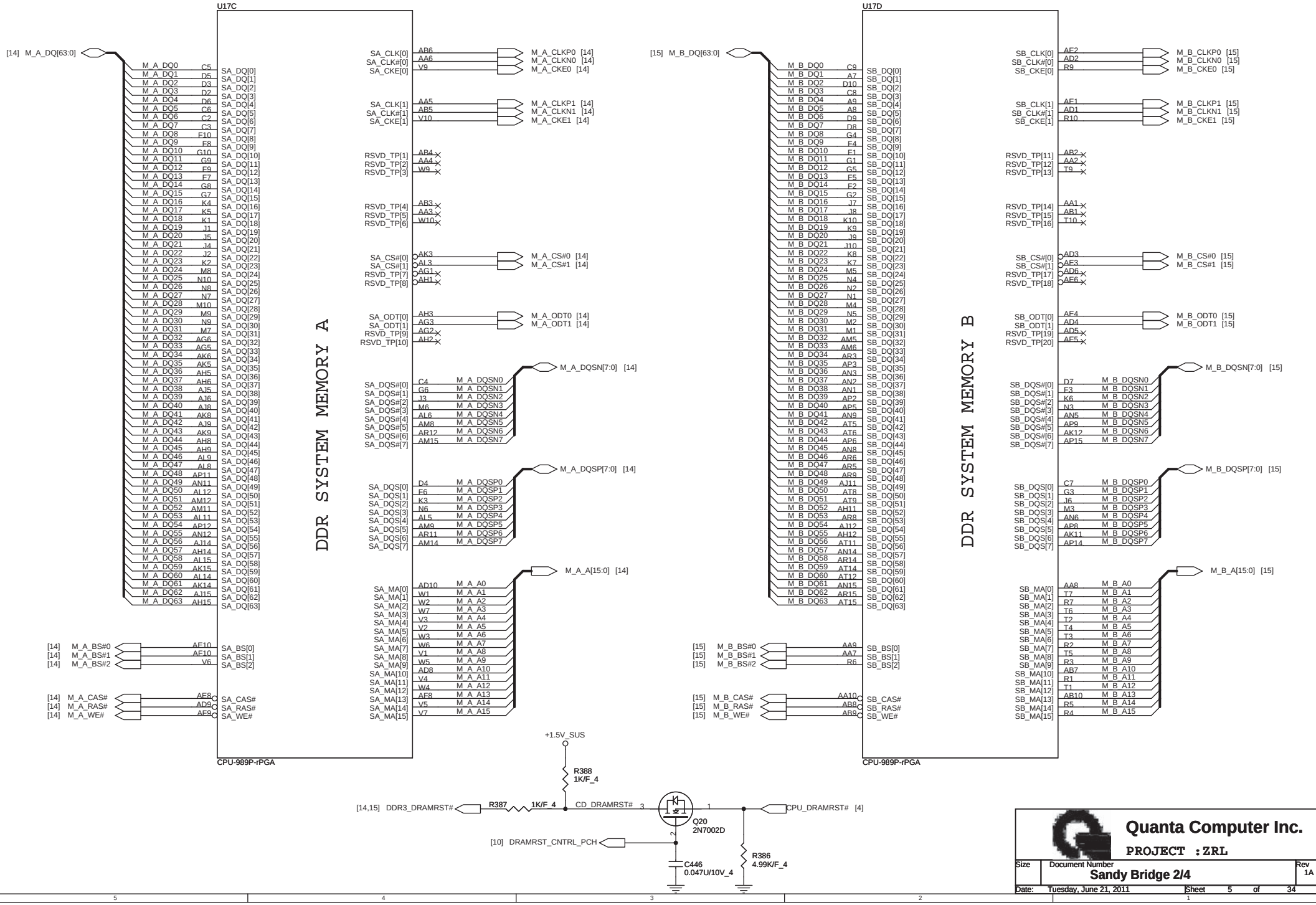
Sandy Bridge Processor (DDR3)



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Sandy Bridge Processor (POWER)

Sandy Bridge Processor (GRAPHIC POWER)

06

POWER

U17F

CPU-989P-rPGA

CPU Core Power
SNB 45W:52A

Spec
470uF/4mohm x 4
22uF x 16
10uF x 10

CPU VTT
SNB 45W:8.5A

Spec
330uF/6mohm x 2
22uF x 12
22uF x 7 (Non-stuff)

CPU VGT
SNB 45W:21.5A

Spec
470uF/4mohm x 2
22uF x 12

CPU VCCPL
SNB 45W:1.5A

Spec
330uF/7mohm x 1
10uF x 1
1uF x 2

CPU MCH
SNB 45W: 5A

Spec
330uF/6mohm x 1
10uF x 6

Real
10uF x 6

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

CPU SA
SNB 45W: 6A

Spec
330uF/7mohm x 1
10uF x 3

CORE SUPPLY

PEG AND DDR

SVID

SENSE LINES

GRAPHICS

1.8V RAIL

DDR3 -1.5V RAILS

VREF

SA RAIL

MISC

SENSE LINES

CPU-989P-rPGA

Layout note: need routing together and ALERT need between CLK and DATA

SVID CLK

SVID DATA

SVID ALERT

Place PU resistor close to CPU

Place PU resistor close to CPU

4.5A

Q7 *AO4496

Q6 *DMN601K-7

Q19 *2N7002D

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PROJECT : ZRL			
Size	Document Number: Sandy Bridge 3/4		Rev: 1A
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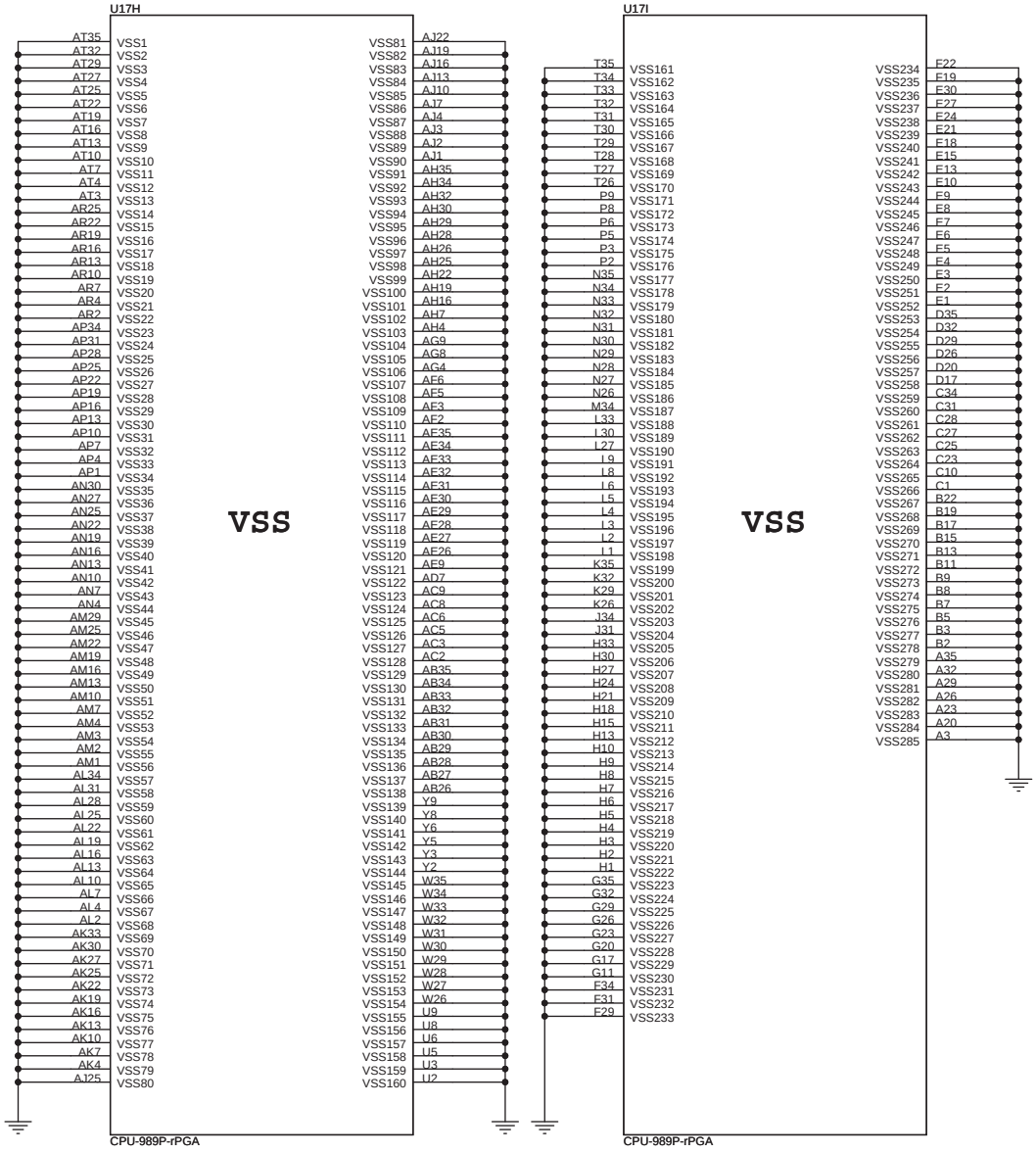
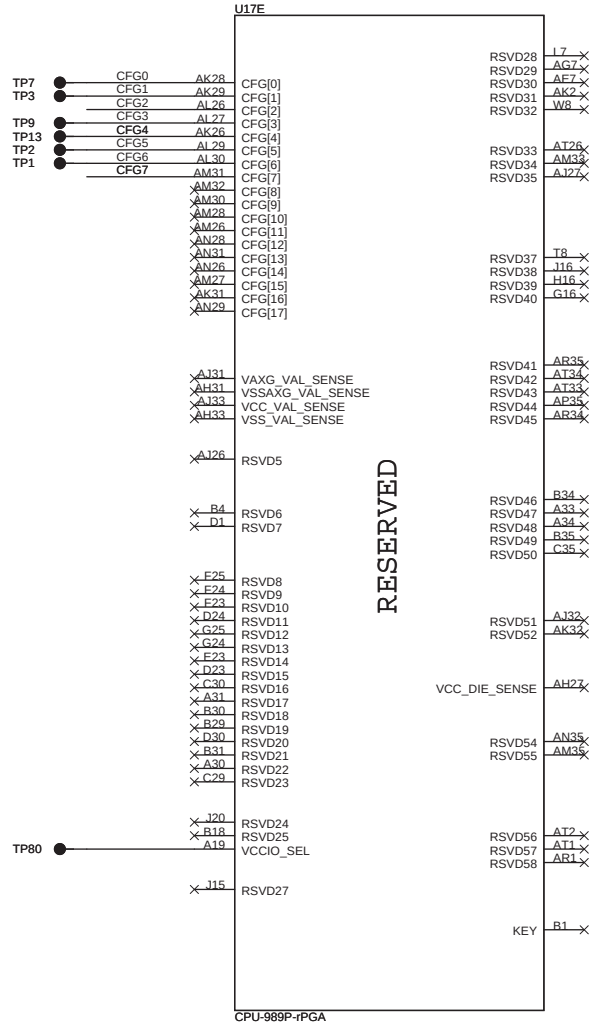
Sandy Bridge Processor (GND)



Sandy Bridge Processor (RESERVED, CFG)

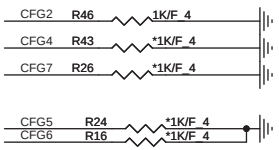
07



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xxRESETB de assertion	PEG wait for BIOS training



CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

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	Sandy Bridge 4/4	1A
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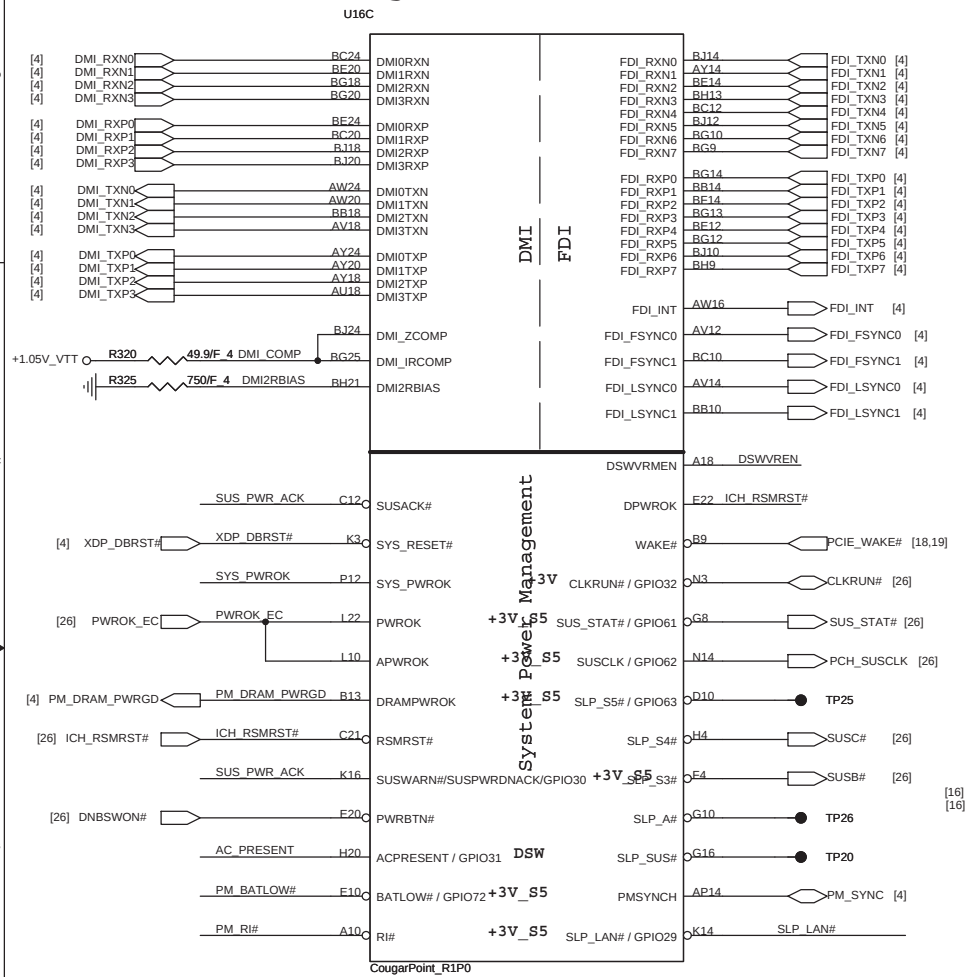
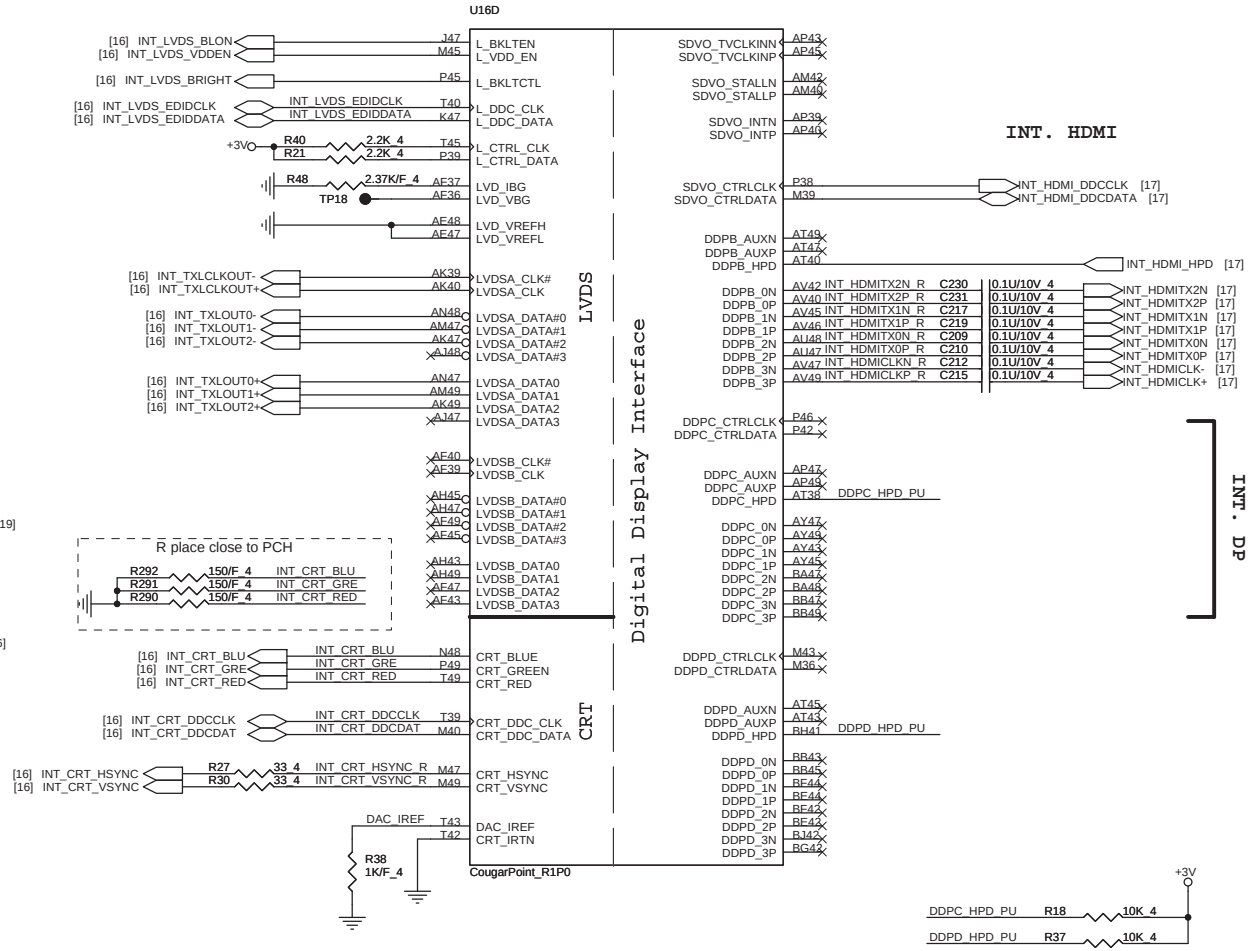
Cougar Point (DMI,FDI,PM)



Cougar Point (LVDS,DDI)

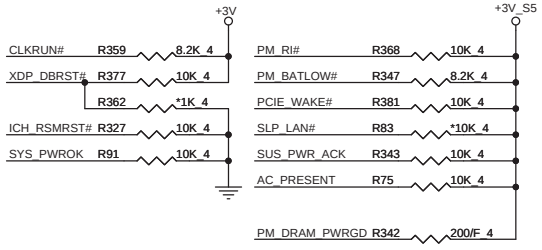


DDPC_HPD_PU R18 10K_4

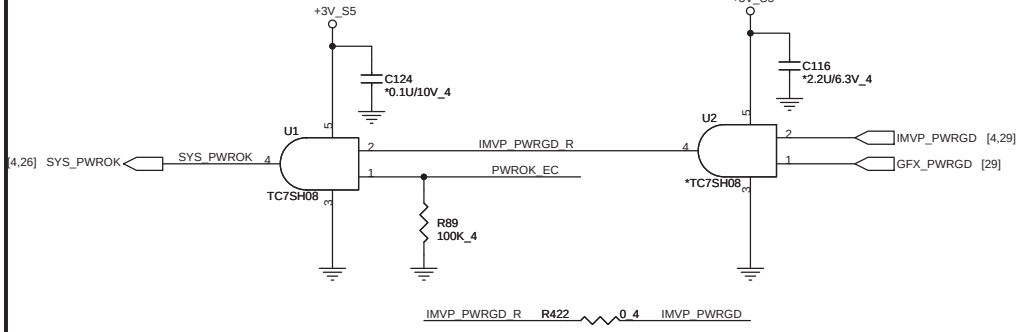
DDPD_HPD_PU R37 10K_4

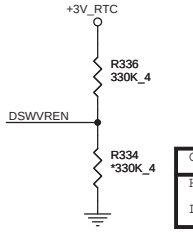
Follow PDG eDP disable guide

PCH Pull-high/low(CLG)



System PWR_OK(CLG)





On Die DSW VR Enable
High = Enable (Default)
Low = Disable

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	Cougar Point 1/6	1A
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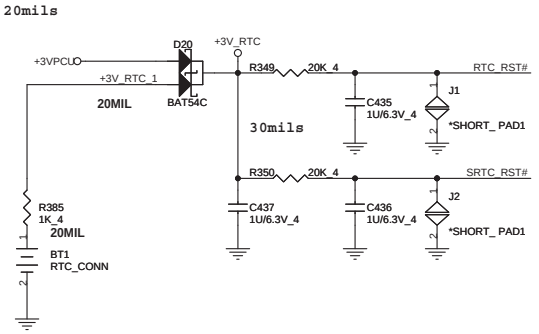
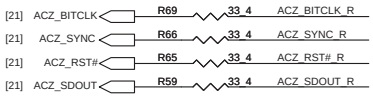
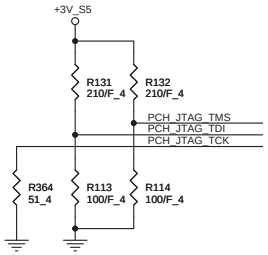
RTC Circuitry(RTC)



HDA Bus(CLG)



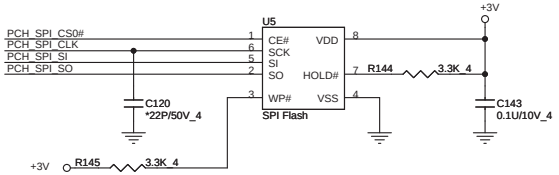
PCH JTAG Debug (CLG)



PCH Dual SPI (CLG)

MX25L3205DM2I-12G: AKE39FP0Z00

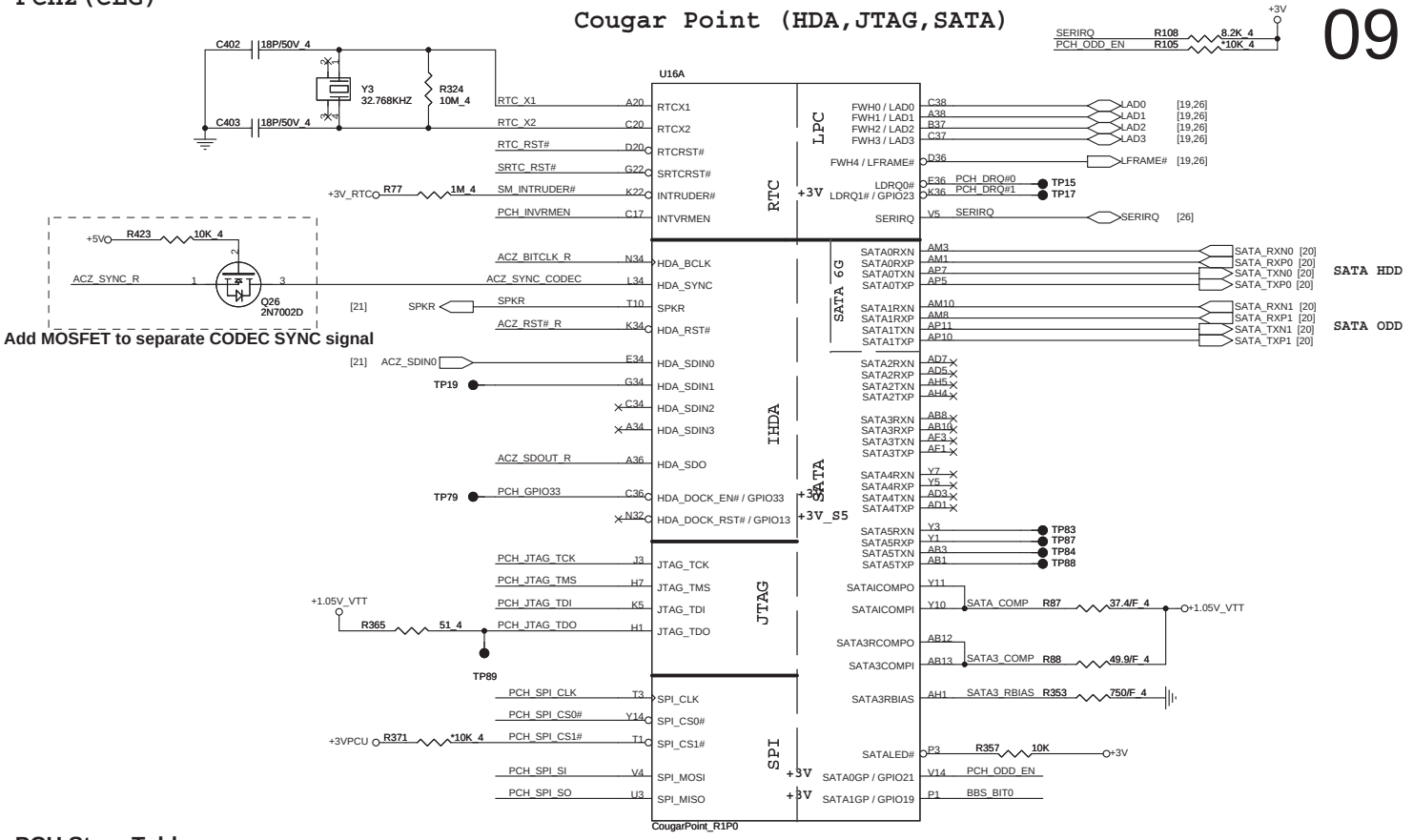
W25X32VSSIG: AKE39ZP0N00



PCH2 (CLG)

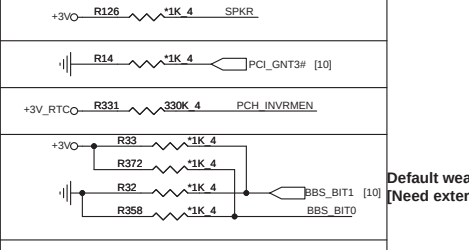
Cougar Point (HDA,JTAG,SATA)

09



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location 1 / 1 / **SPI** * 0 / 0 / LPC
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK	
HDA_SDO	Flash Descriptor Security	**RSMRST**	0 = Override 1 = Default (weak pull-up 20K)
DF_TVS	**DMI/FDI Termination voltage**	**PWROK**	**0 = Set to Vss** **1 = Set to Vcc (weak pull-down 20K)**
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	**0 = Support by 1.8V (weak pull-down)** **1 = Support by 1.5V**
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable
NV_ALE	Intel Anti-Theft HDD protection	PWROK	0 = Disable (Internal pull-down 20kohm)



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	Cougar Point 2/6	1A

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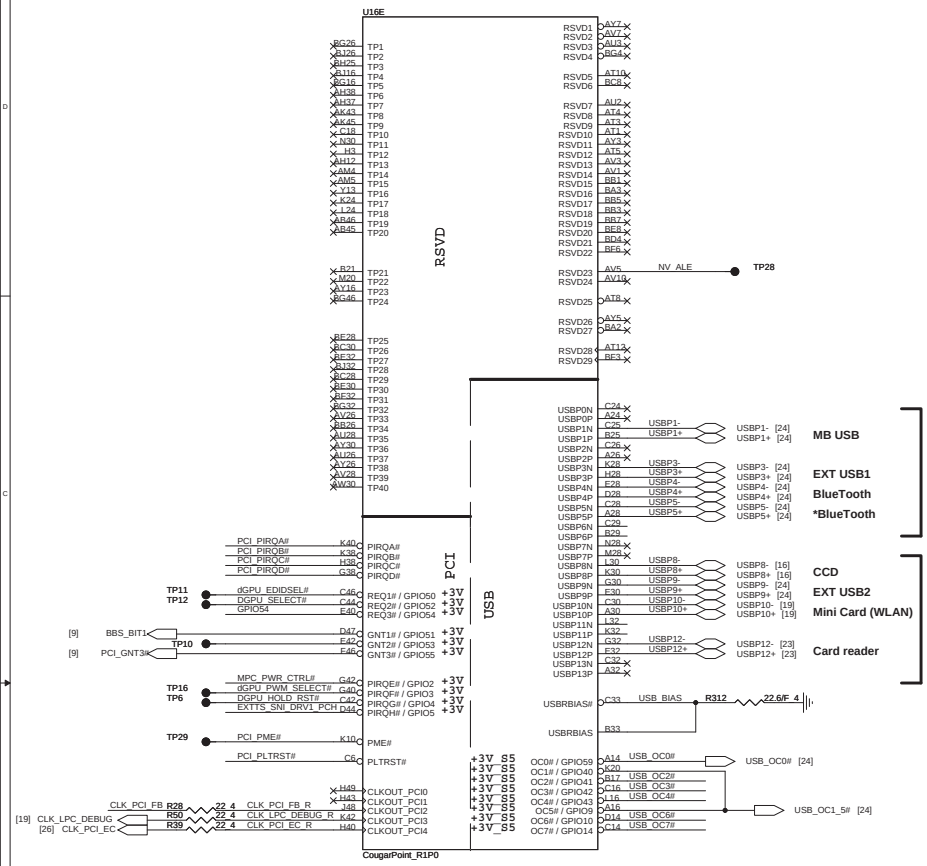
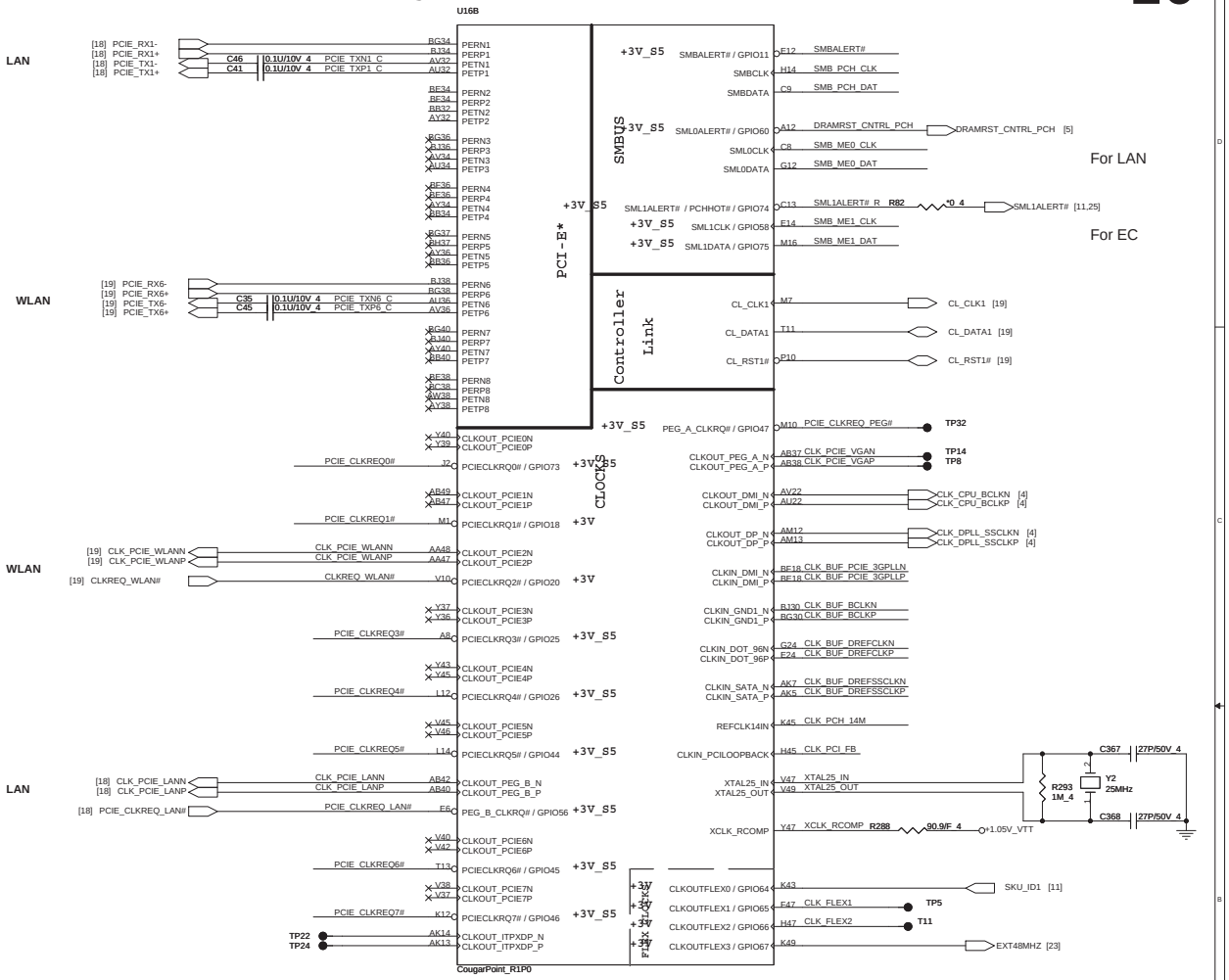
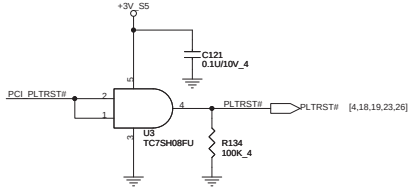
Cougar Point-M (PCI,USB,NVRAM)



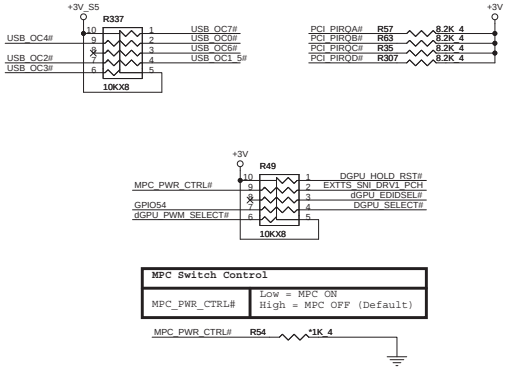
Cougar Point-M (PCI-E,SMBUS,CLK)



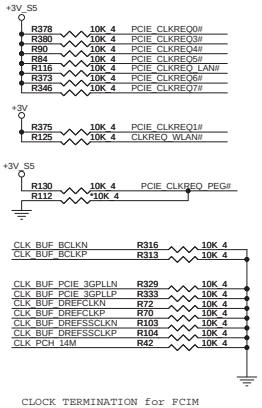
PLTRST#(CLG)



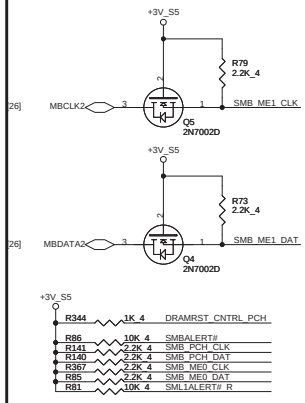
PCI/USBOC# Pull-up(CLG)



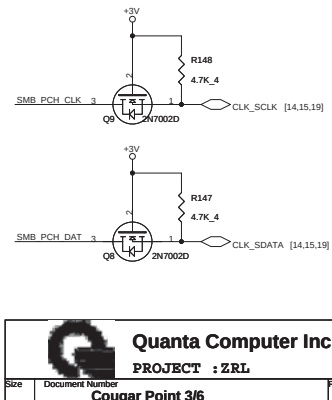
CLK_REQ/Strap Pin(CLG)



SMBus/Pull-up(CLG)



SMBus(PCH)



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	Cougar Point 3/6	1A
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Cougar Point (GPIO,VSS_NCTF,RSVD)

U16F

GPIO

S_GPIO	T7	BMBUSY# / GPIO0	+3V	+3V	TACH4 / GPIO68	C40	dGPU_PWR_CTRL#
[26] EC_EXT_SMI#	A42	EC_EXT_SMI# / TACH1 / GPIO1	+3V	+3V	TACH5 / GPIO69	B41	R298 1.5K/F_4
BOARD_ID1	H36	TACH2 / GPIO6	+3V	+3V	TACH6 / GPIO70	C41	R302 1.5K/F_4 +3V
[26] EC_EXT_SCI#	E38	EC_EXT_SCI# / TACH3 / GPIO7	+3V	+3V	TACH7 / GPIO71	A40	R303 1.5K/F_4
TP86	C10	GPIO8	+3V_S5				
SMIB#	C4	LAN_PHY_PWR_CTRL / GPIO12	+3V_S5				
PCH_GPIO15	G2	GPIO15	+3V_S5				
check VR_ON GPIO	U2	SATA4GP / GPIO16	+3V				
TP4	D40	TACH0 / GPIO17	+3V				
BIOS_REC	T5	SCLOCK / GPIO22	+3V				
CR_WAKER#	F8	GPIO24 / MEM_LED	+3V_S5				
GPIO27	E16	GPIO27	DSW				
[9] PLL_ODVR_EN	P8	PLL_ODVR_EN / GPIO28	+3V_S5				
Need Check	K1	STP_PCI# / GPIO34	+3V				
TP27	K4	dGPU_VRON / GPIO35	+3V				
TP30	V8	DMI_OVRVLTG / SATA2GP / GPIO36	+3V				
FDI_OVRVLTG	M5	SATA3GP / GPIO37	+3V				
MFG_MODE	N2	SLOAD / GPIO38	+3V				
BOARD_ID0	M3	SDATAOUT0 / GPIO39	+3V				
TEST_SET_UP	V13	SDATAOUT1 / GPIO48	+3V				
[10,25] SML1ALERT#	V3	R354 *short_4 CRIT_TEMP_REP# / SATA5GP / GPIO49	+3V				
BOARD_ID2	D6	GPIO57	+3V_S5				

CPU/MISC

A20GATE	P4	EC_A20GATE	EC_A20GATE [26]
PECI	AU16	R102 *0_4	EC_PECI [4,26]
RCIN#	P5	EC_RCIN#	EC_RCIN# [26]
PROCPWRGD	AY11	TP23	H_PWRGOOD [4]
THRMTRIP#	AY10	PCH_THRMTRIP# R101 390_4	PM_THRMTRIP# [4]
INIT3_3V#	T14		
DF_TVS	AY1		DF_TVS [9]
TS_VSS1	AH8		
TS_VSS2	AK11		
TS_VSS3	AH10		
TS_VSS4	AK10		
NC_1	P37		

NCTF

VSS_NCTF_1	A4	VSS_NCTF_15	BG2
VSS_NCTF_2	A44	VSS_NCTF_16	BG48
VSS_NCTF_3	A45	VSS_NCTF_17	BH3
VSS_NCTF_4	A46	VSS_NCTF_18	BH47
VSS_NCTF_5	A5	VSS_NCTF_19	BJ4
VSS_NCTF_6	A6	VSS_NCTF_20	BJ44
VSS_NCTF_7	B3	VSS_NCTF_21	BJ45
VSS_NCTF_8	B47	VSS_NCTF_22	BJ46
VSS_NCTF_9	BD1	VSS_NCTF_23	BJ5
VSS_NCTF_10	BD49	VSS_NCTF_24	BJ6
VSS_NCTF_11	BE1	VSS_NCTF_25	C2
VSS_NCTF_12	BF49	VSS_NCTF_26	C48
VSS_NCTF_13	BF1	VSS_NCTF_27	D1
VSS_NCTF_14	BF49	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

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R353??

GPIO27:
Un-multiplexed. Can be configured as wake input to allow wakes from Deep Sleep.
If not used then use 8.2-kΩ to 10-kΩ pull-down to GND.

	dGPU_PWR_CTRL# (GPIO68)	SKU_ID1 (GPIO64)	SKU_ID0 (GPIO16)	VGA H/W Signal	Setup Menu	
UMA Only	1	0	0	UMA	Hidden	UMA boot
Discrete Only	0 or 1	0	1	GPU	Hidden	GPU boot
Switchable (Mux)	0	1	0	UMA+GPU	DIS/SG	UMA boot
Optimize (Muxless)	0	1	1	UMA	UMA/SG	UMA boot

0 = GPU power is control by PCH GPIO (Discrete, SG or Optimize)
1 = GPU power is control by H/W (pure Discrete SKU)

SV_SET_UP

High = Strong (Default)

TEST_SET_UP R124 10K_4, R107 *0_4 +3V

SGPIO

S_GPIO R111 1K/F_4, R95 *100_4 +3V

PCH_GPIO15 R379 1K_4 +3V_S5

Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)

High = Enable

MFG-TEST

MFG_MODE R374 10K_4, R360 *0_4 +3V

FDI_OVRVLTG R129 *10K/F_4 +3V

FDI TERMINATION VOLTAGE OVERRIDE	LOW - Tx, Rx terminated to same voltage

DMI_OVRVLTG R94 *200K/F_4 +3V

DMI TERMINATION VOLTAGE OVERRIDE	Low = Tx, Rx terminated to same voltage (DC Coupling Mode) (DEFAULT)

BIOS_REC R128 10K_4, R110 *0_4 +3V

BIOS RECOVERY	High = Disable (Default) Low = Enable

GPIO Pull-up/Pull-down(CLG)

+3V_S5

CR_WAKER#	R348	10K/F_4
SMIB#	R366	10K_4
PLL_ODVR_EN	R127	*10K_4

+3V

EC_EXT_SMI#	R299	10K_4
EC_EXT_SCI#	R34	10K_4
STP_PCI#	R363	*10K_4
EC_A20GATE	R96	10K_4
EC_RCIN#	R93	10K_4
CRIT_TEMP_REP#	R355	10K_4
dGPU_PWROK	R36	*10K_4
GPIO27	R80	*10K_4

+3V

R297 10K_4, R305 *100K_4 dGPU_PWR_CTRL#

+3V

R15 *10K_4, R22 10K_4 SKU_ID1 [10]

+3V

R370 *10K_4, R356 10K_4 SKU_ID0

+3V

R361	*10K_4	BOARD_ID0	R376	10K_4	
R300	10K_4	BOARD_ID1	R301	*10K_4	
R115	10K_4	BOARD_ID2	R133	*10K_4	

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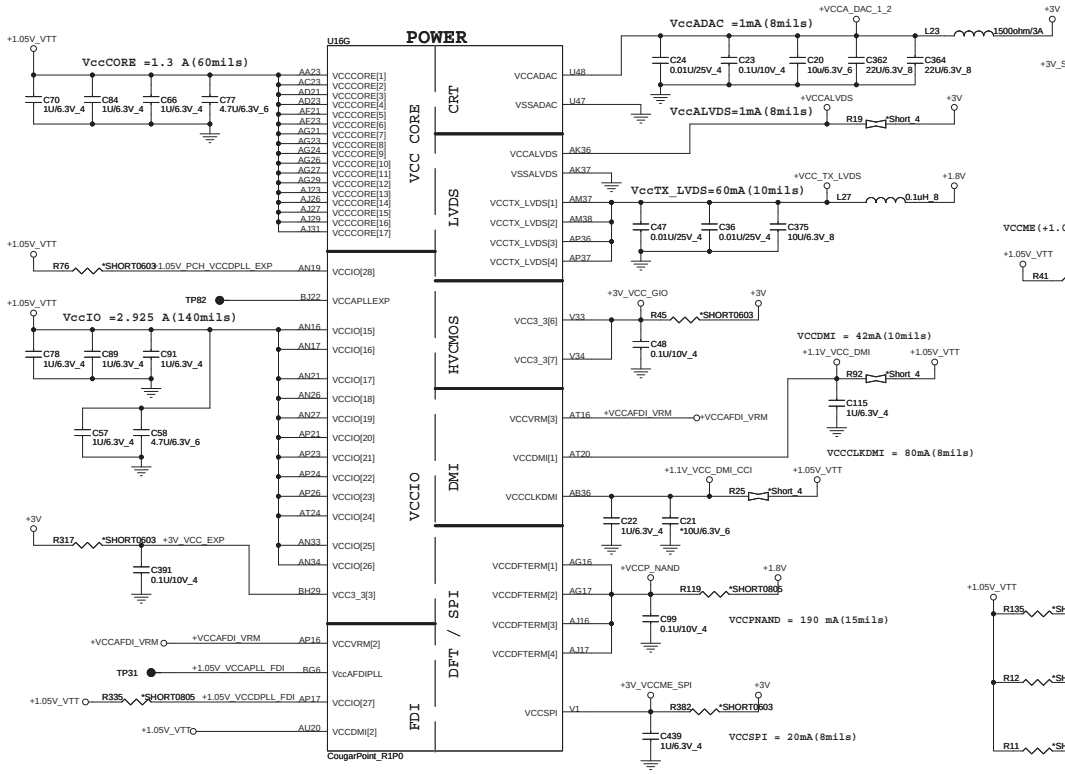
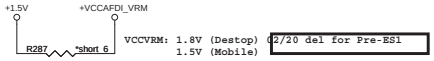
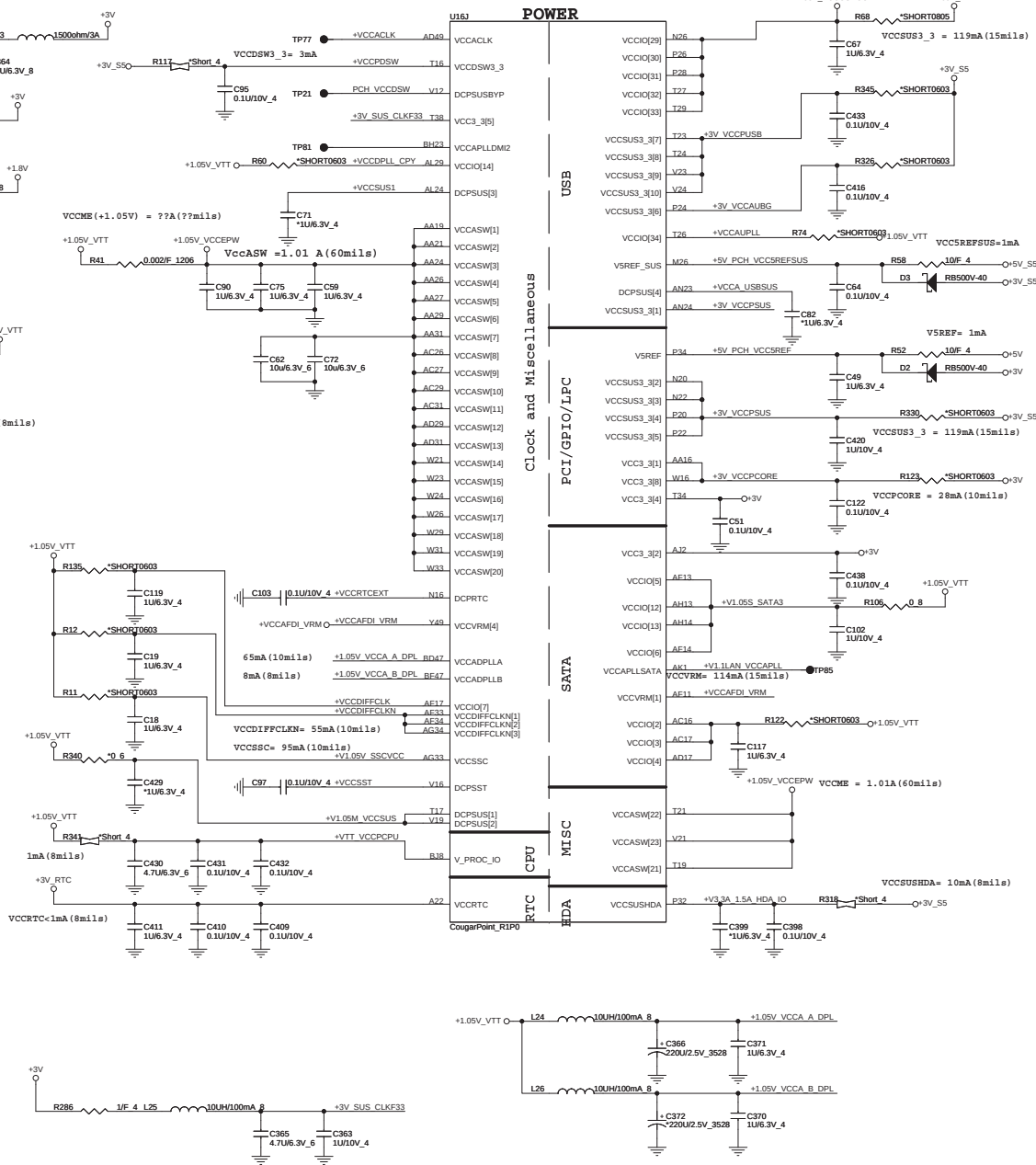
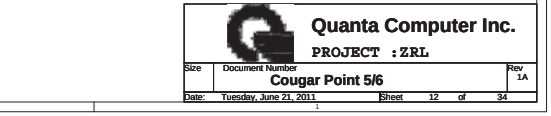
COUGAR POINT (POWER)





Cougar Point-M (POWER)





IBEX PEAK-M (GND)

U16H

H5	VSS[0]	
AA17	VSS[1]	AK38
AA2	VSS[2]	AK4
AA3	VSS[3]	AK42
AA33	VSS[4]	AK46
AA34	VSS[5]	AK8
AB11	VSS[6]	AL16
AB14	VSS[7]	AL17
AB39	VSS[8]	AL19
AB4	VSS[9]	AL2
AB43	VSS[10]	AL21
AB5	VSS[11]	AL23
AB7	VSS[12]	AL26
AC19	VSS[13]	AL27
AC2	VSS[14]	AL31
AC21	VSS[15]	AL33
AC24	VSS[16]	AL34
AC33	VSS[17]	AL48
AC34	VSS[18]	AM11
AC48	VSS[19]	AM14
AD10	VSS[20]	AM36
AD11	VSS[21]	AM39
AD12	VSS[22]	AM43
AD13	VSS[23]	AM45
AD19	VSS[24]	AM46
AD24	VSS[25]	AM7
AD26	VSS[26]	AN2
AD27	VSS[27]	AN29
AD33	VSS[28]	AN3
AD34	VSS[29]	AN31
AD36	VSS[30]	AP12
AD37	VSS[31]	AP19
AD38	VSS[32]	AP28
AD39	VSS[33]	AP30
AD4	VSS[34]	AP32
AD40	VSS[35]	AP38
AD42	VSS[36]	AP4
AD43	VSS[37]	AP42
AD45	VSS[38]	AP46
AD46	VSS[39]	AP8
AD8	VSS[40]	AR2
AE2	VSS[41]	AR48
AE3	VSS[42]	AT11
AE10	VSS[43]	AT13
AE12	VSS[44]	AT18
AE14	VSS[45]	AT22
AE16	VSS[46]	AT26
AE19	VSS[47]	AT28
AE24	VSS[48]	AT30
AE26	VSS[49]	AT32
AE27	VSS[50]	AT34
AE29	VSS[51]	AT39
AE31	VSS[52]	AT42
AE38	VSS[53]	AT46
AF4	VSS[54]	AT7
AF42	VSS[55]	AU24
AF46	VSS[56]	AU30
AF5	VSS[57]	AV16
AF7	VSS[58]	AV20
AF8	VSS[59]	AV24
AG19	VSS[60]	AV30
AG2	VSS[61]	AV38
AG31	VSS[62]	AV4
AG48	VSS[63]	AV43
AH11	VSS[64]	AV8
AH3	VSS[65]	AW14
AH36	VSS[66]	AW18
AH39	VSS[67]	AW2
AH40	VSS[68]	AW22
AH42	VSS[69]	AW26
AH46	VSS[70]	AW28
AH7	VSS[71]	AW32
AJ19	VSS[72]	AW34
AJ21	VSS[73]	AW36
AJ24	VSS[74]	AW40
AJ33	VSS[75]	AW48
AJ34	VSS[76]	AV11
AK12	VSS[77]	AY12
AK3	VSS[78]	AY22
	VSS[79]	AY28
	VSS[80]	
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	VSS[158]	

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U16I

AY4	VSS[159]	H46
AY42	VSS[160]	K18
AY46	VSS[161]	K26
AY8	VSS[162]	K39
B11	VSS[163]	K46
B15	VSS[164]	K7
B19	VSS[165]	L18
B23	VSS[166]	L2
B27	VSS[167]	L20
B31	VSS[168]	L26
B35	VSS[169]	L28
B39	VSS[170]	L36
B7	VSS[171]	L48
F45	VSS[172]	M12
BB12	VSS[173]	P16
BB16	VSS[174]	M18
BB20	VSS[175]	M22
BB22	VSS[176]	M24
BB24	VSS[177]	M30
BB28	VSS[178]	M32
BB30	VSS[179]	M34
BB38	VSS[180]	M38
BB4	VSS[181]	M4
BB46	VSS[182]	M42
BC14	VSS[183]	M46
BC18	VSS[184]	M8
BC2	VSS[185]	N18
BC22	VSS[186]	P30
BC26	VSS[187]	N47
BC32	VSS[188]	P11
BC34	VSS[189]	P18
BC36	VSS[190]	T33
BC40	VSS[191]	P40
BC42	VSS[192]	P43
BC48	VSS[193]	P47
BD46	VSS[194]	P7
BD5	VSS[195]	R2
BE22	VSS[196]	R48
BE26	VSS[197]	T12
BE40	VSS[198]	T31
BE10	VSS[199]	T37
BE12	VSS[200]	T4
BE16	VSS[201]	W34
BE20	VSS[202]	T46
BE22	VSS[203]	T47
BE24	VSS[204]	T8
BE26	VSS[205]	V11
BE28	VSS[206]	V17
BD3	VSS[207]	V26
BE30	VSS[208]	V27
BE38	VSS[209]	V29
BE40	VSS[210]	V31
BF8	VSS[211]	V36
BG17	VSS[212]	V39
BG21	VSS[213]	V43
BG33	VSS[214]	V7
BG44	VSS[215]	W17
BG8	VSS[216]	W19
BH11	VSS[217]	W2
BH15	VSS[218]	W27
BH17	VSS[219]	W48
BH19	VSS[220]	Y12
H10	VSS[221]	Y38
BH27	VSS[222]	Y4
BH31	VSS[223]	Y42
BH33	VSS[224]	Y46
BH35	VSS[225]	Y8
BH39	VSS[226]	BG29
BH43	VSS[227]	N24
BH7	VSS[228]	AJ3
D3	VSS[229]	AD47
D12	VSS[230]	B43
D16	VSS[231]	BE10
D18	VSS[232]	BG41
D22	VSS[233]	G14
D24	VSS[234]	H16
D26	VSS[235]	T36
D30	VSS[236]	BG22
D32	VSS[237]	BG24
D34	VSS[238]	C22
D38	VSS[239]	AP13
D42	VSS[240]	M14
D8	VSS[241]	AP3
E18	VSS[242]	AP1
E26	VSS[243]	BE16
G18	VSS[244]	BC16
G20	VSS[245]	BG28
G26	VSS[246]	BJ28
G28	VSS[247]	
G36	VSS[248]	
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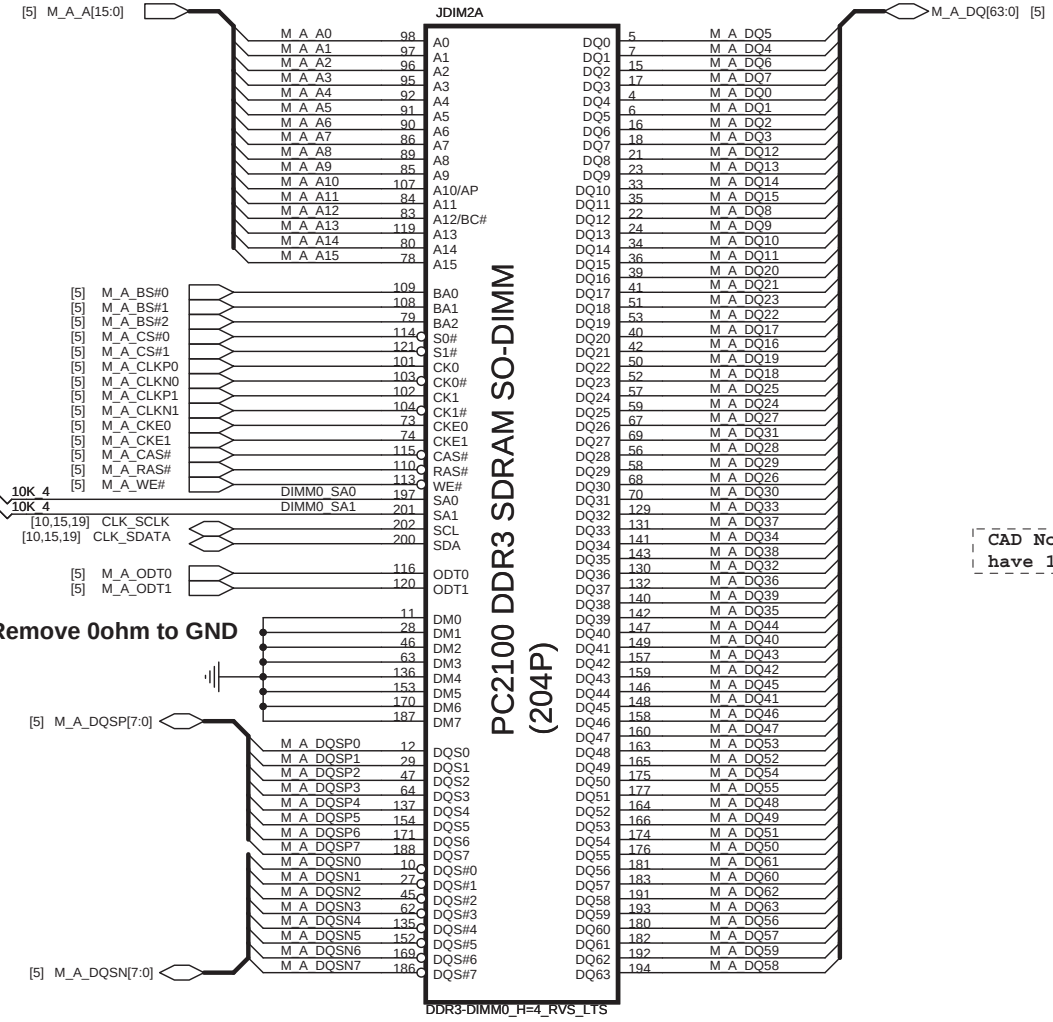
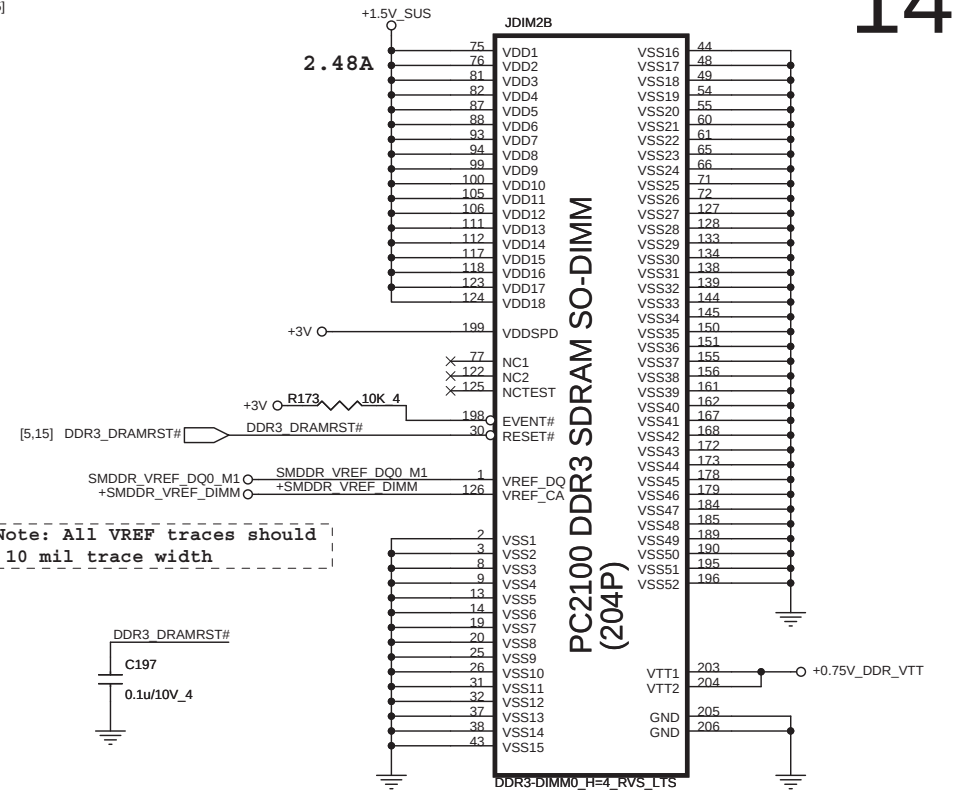
DDR RVS 4H

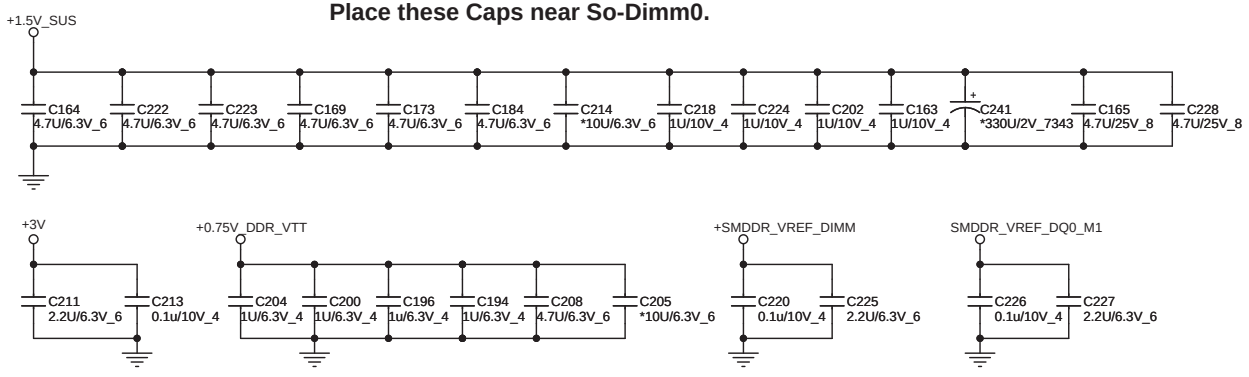


02/23 Remove 0ohm to GND

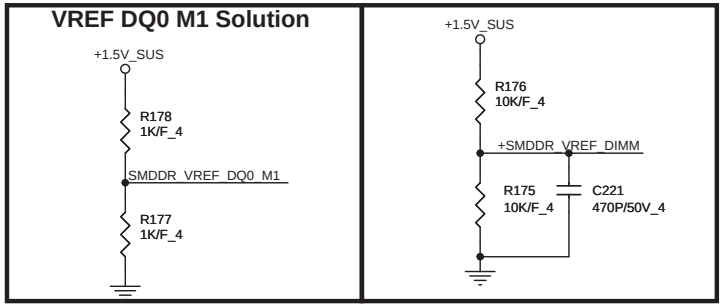


CAD Note: All VREF traces should have 10 mil trace width

Place these Caps near So-Dimm0.



VREF DQ0 M1 Solution



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	DDRIII SO-DIMM-0	1A
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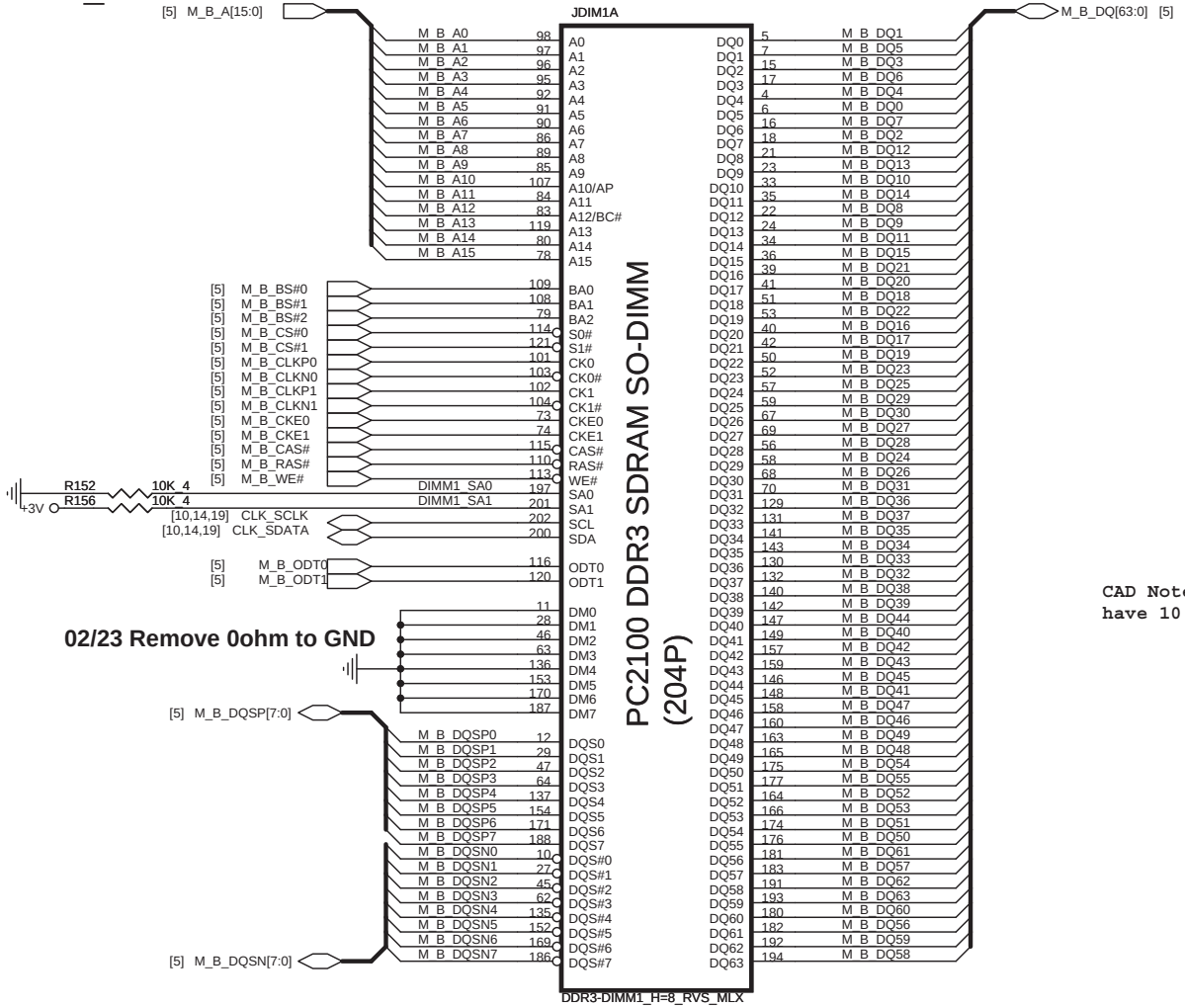
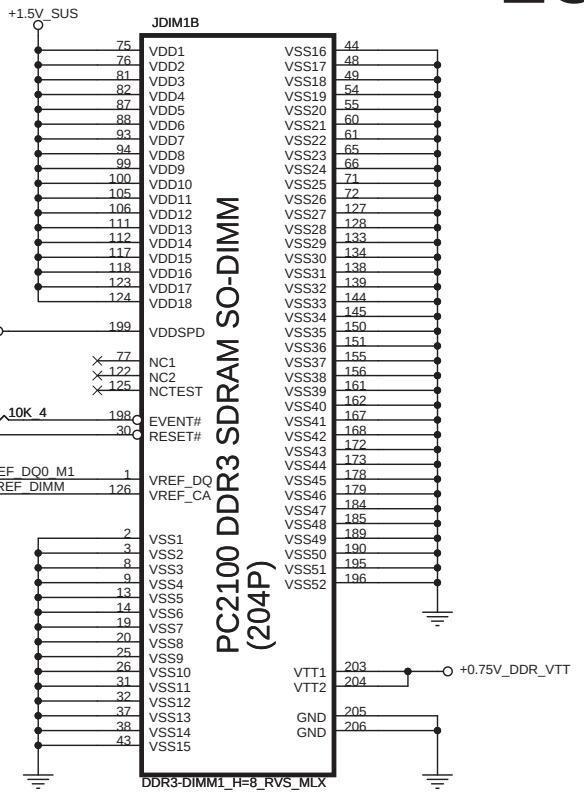
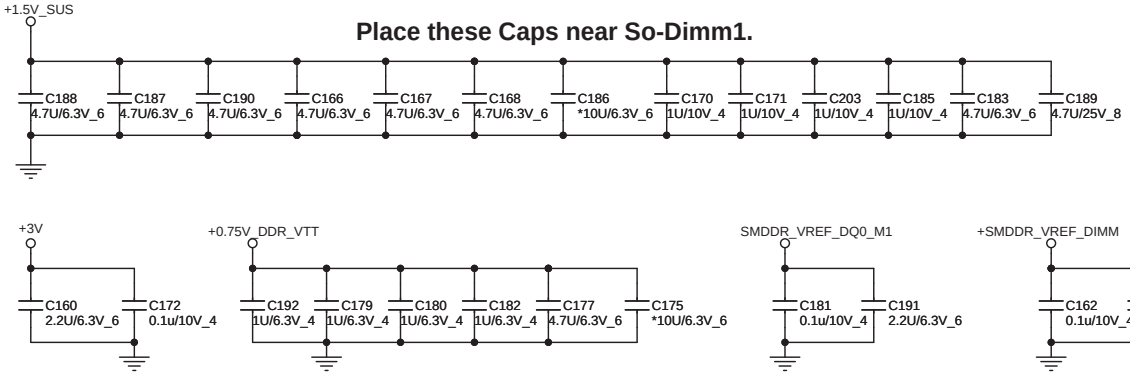
DDR_RVS(DDR)





CAD Note: All VREF traces should have 10 mil trace width



Quanta Computer Inc.

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	DDRIII SO-DIMM-1	1A
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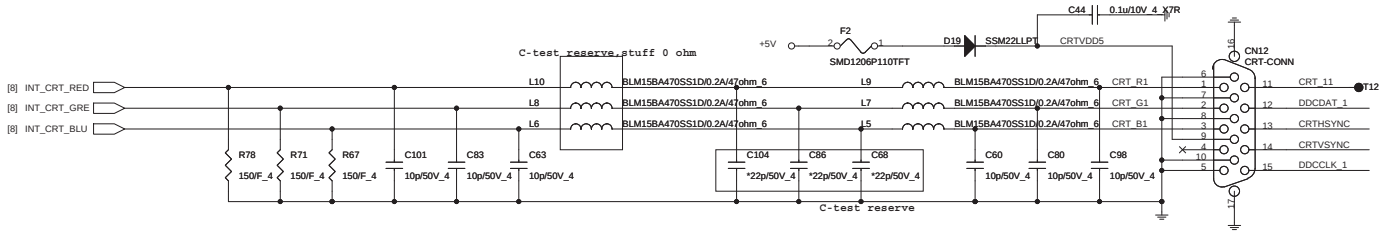
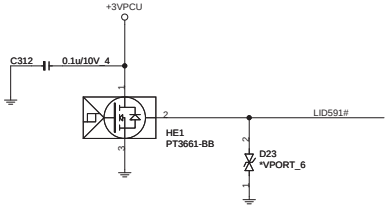
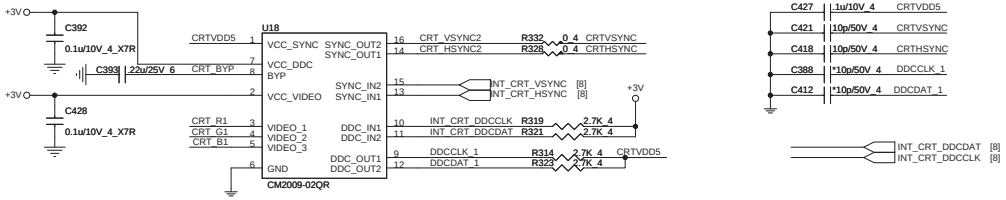
CRT

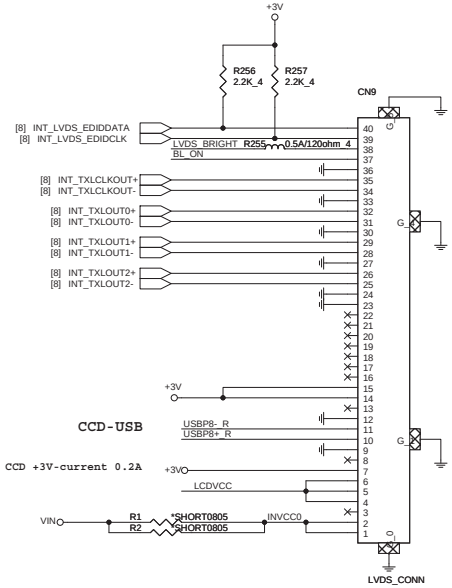


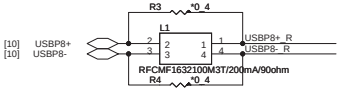
Lid Switch (Hall sensor)



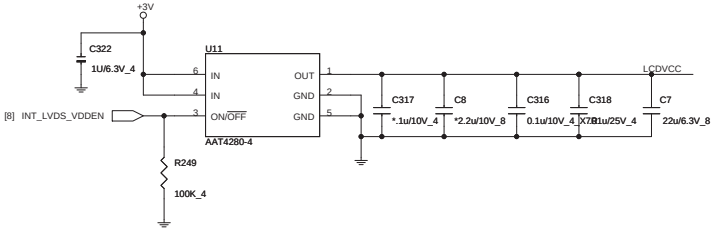


LVDS

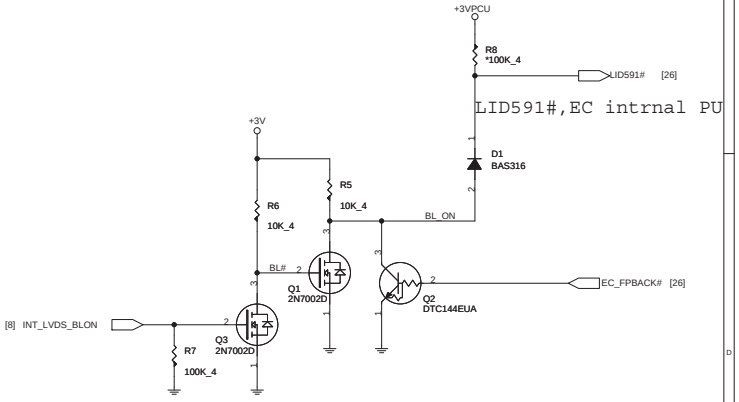




LCD Power



Backlight Control



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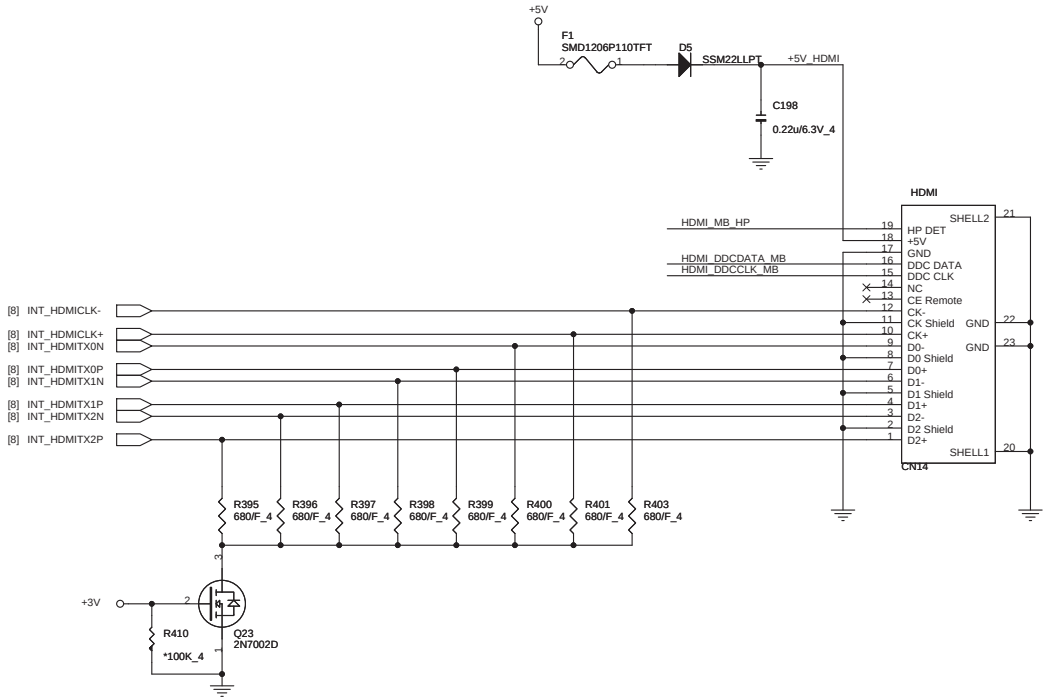
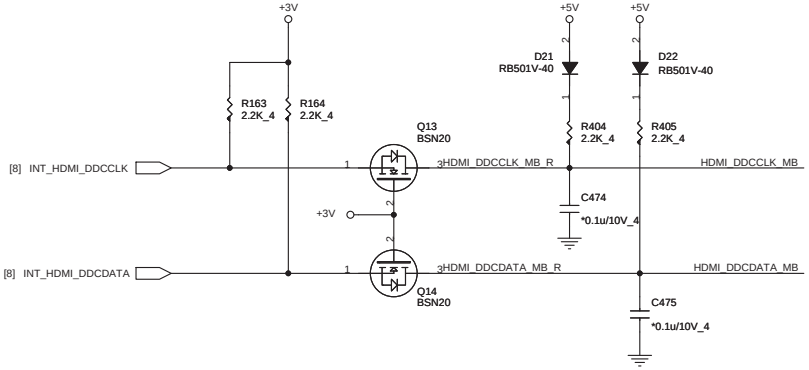
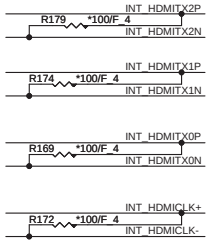
HDMI

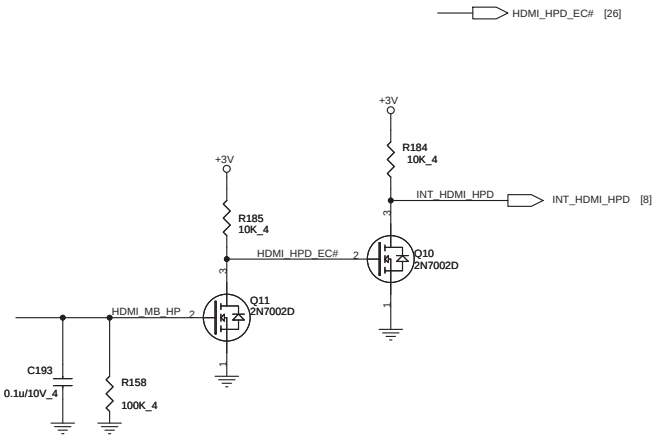




EMI



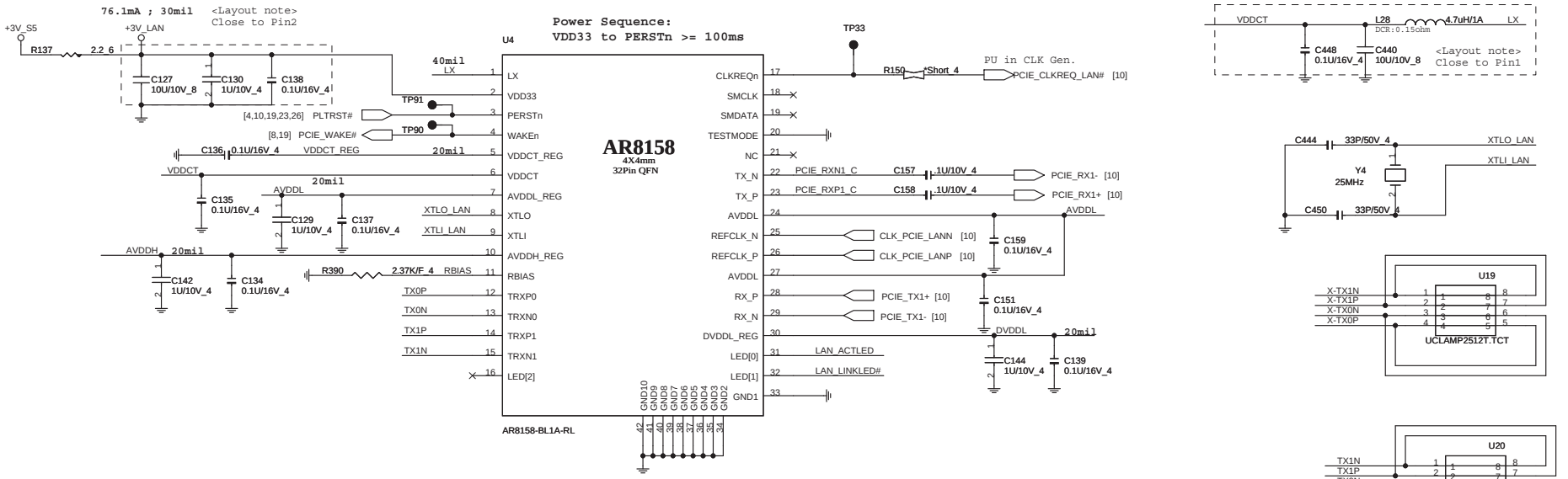
HDMI-detect



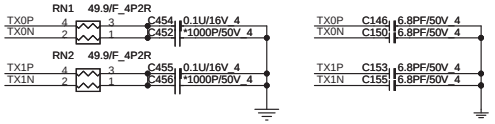
Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number: HDMI (PS8101)	Rev: 1A
Date: Tuesday, June 21, 2011	Sheet 17 of 34	

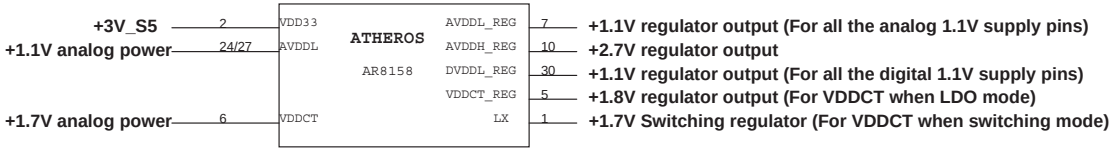
LAN

<BOM note>
If center tap power come from internal switch regulator=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO=>Stuff 52LDO@

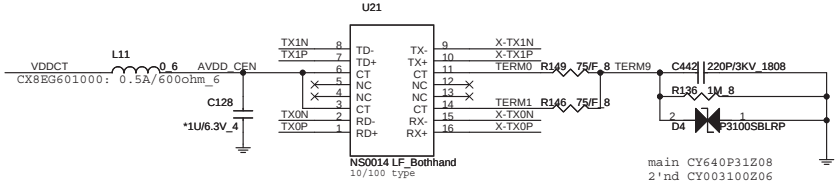


<Layout note>
Close to LAN Chip 1nF reserved for EMI

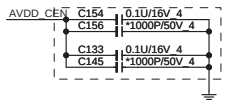




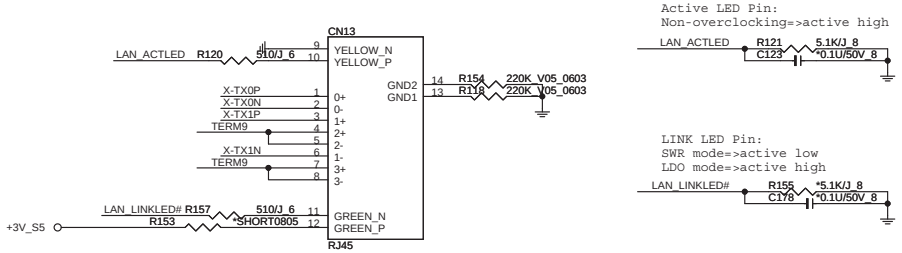
TRANSFORMER



1nF reserved for EMI



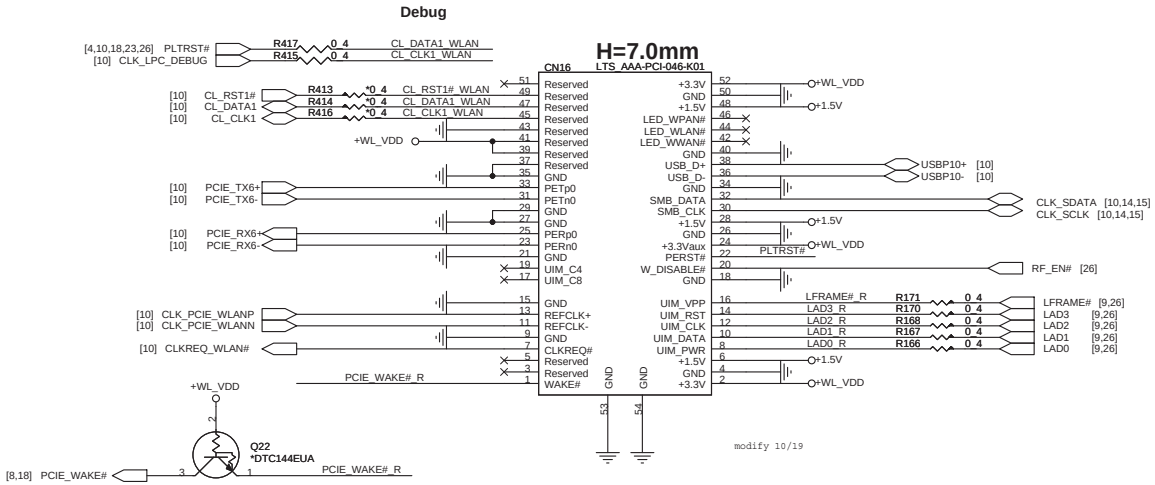
RJ45 Connector

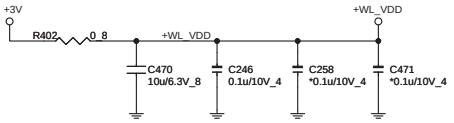


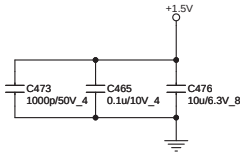
Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	LAN AR8158L		1A
Date:	Tuesday, June 21, 2011	Sheet 18 of 34	

MINI-CARD WLAN

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

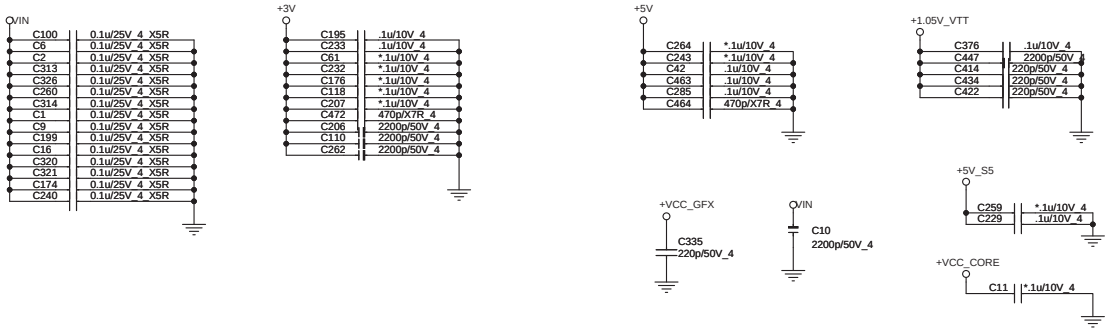






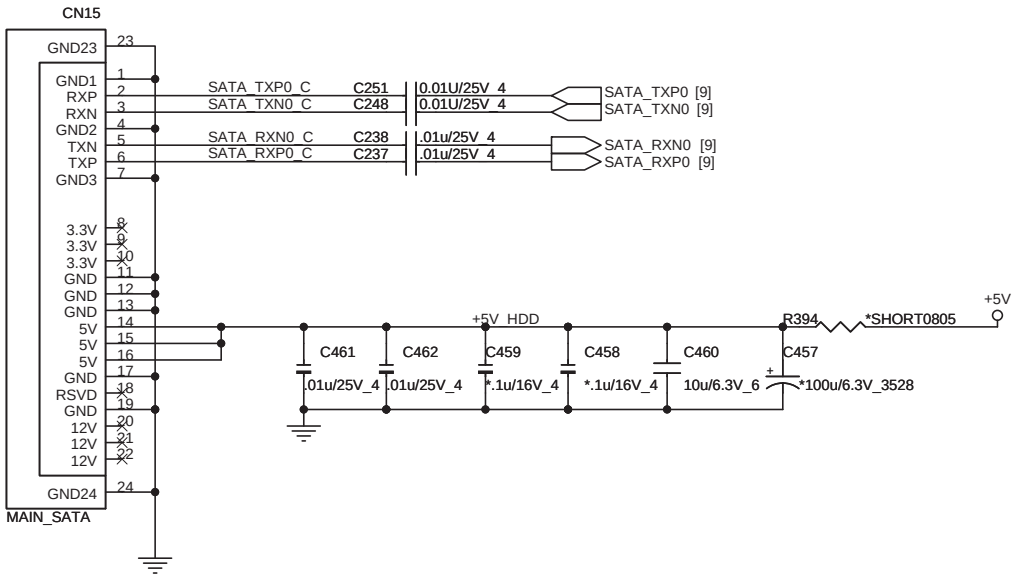
Debug

EE RETURN-PATH CAPACITORS

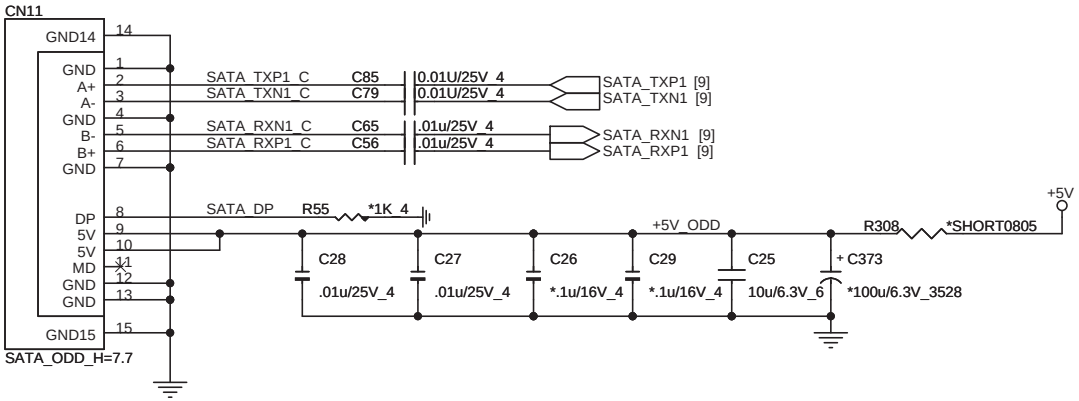


	Quanta Computer Inc.		
	PROJECT : ZRL		
Size	Document Number		Rev
	MINI PCI-E card/TV		1A
Date: Tuesday, June 21, 2011		Sheet 19 of 34	

MAIN SATA HDD



ODD (SATA)

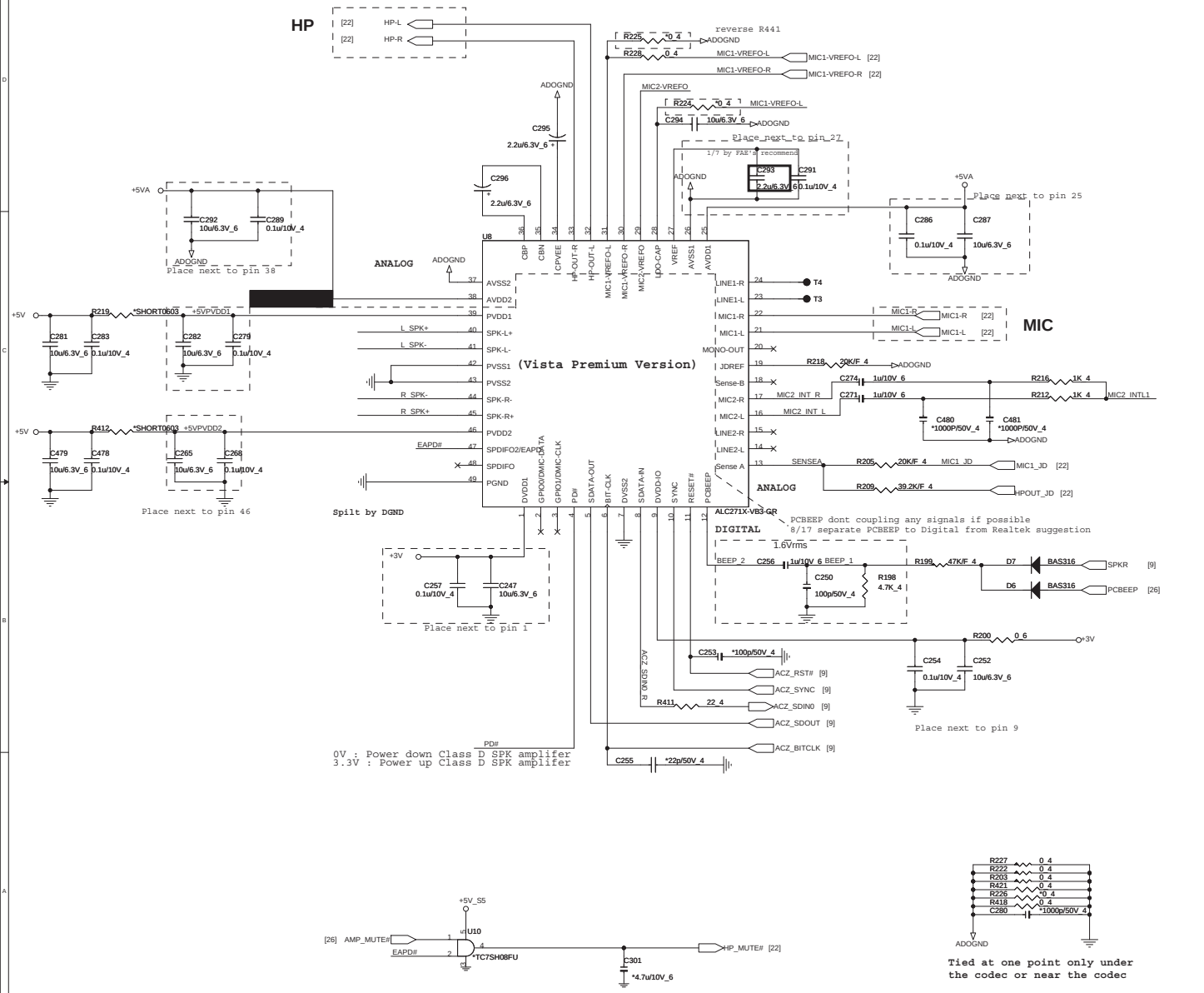


Quanta Computer Inc.

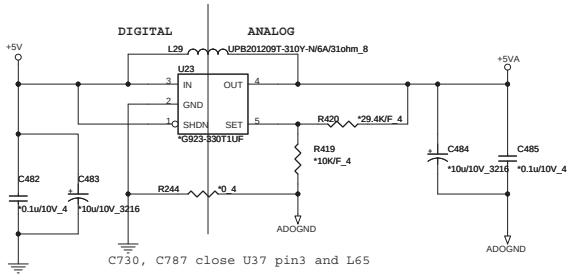
PROJECT : ZRL

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date: Tuesday, June 21, 2011	Sheet 20 of 34	

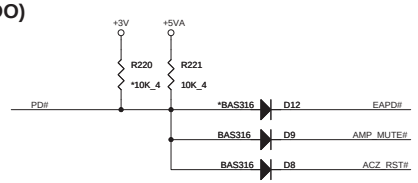
Codec



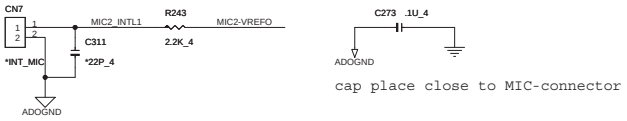
Power



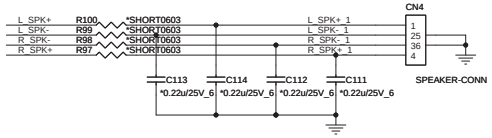
Mute(ADO)



Internal MIC

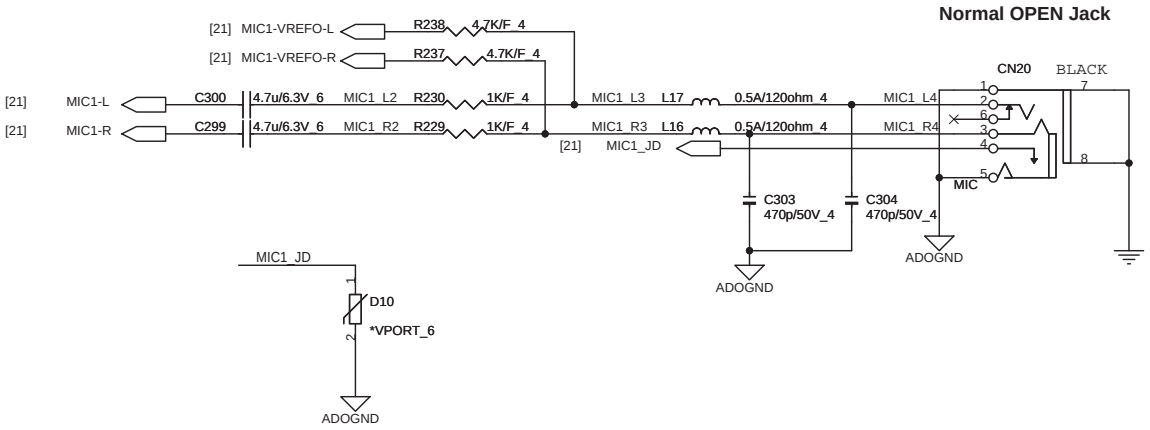


Internal Speaker

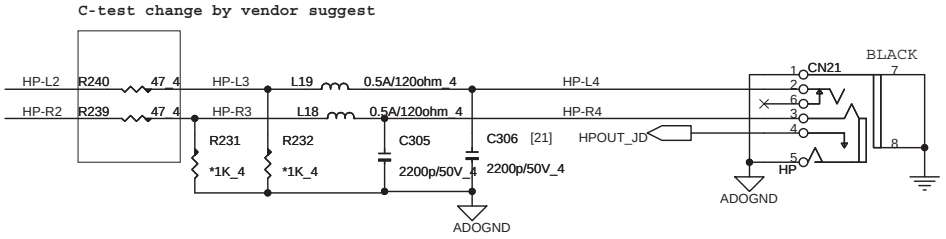


Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	REALTEK ALC271X		1A
Date: Tuesday, June 21, 2011		Sheet 21 of 34	

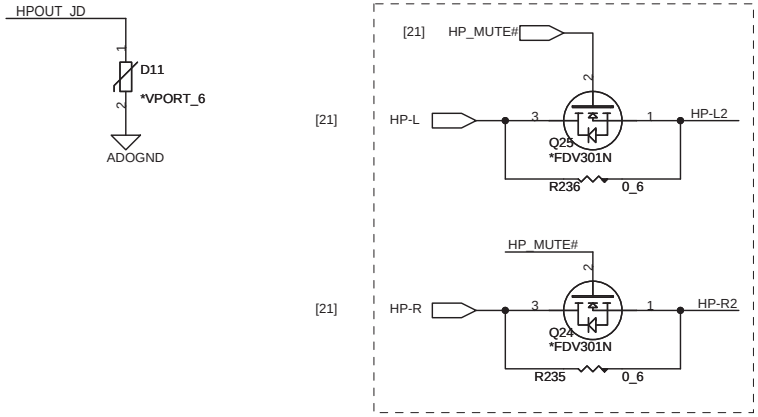
MIC



HP

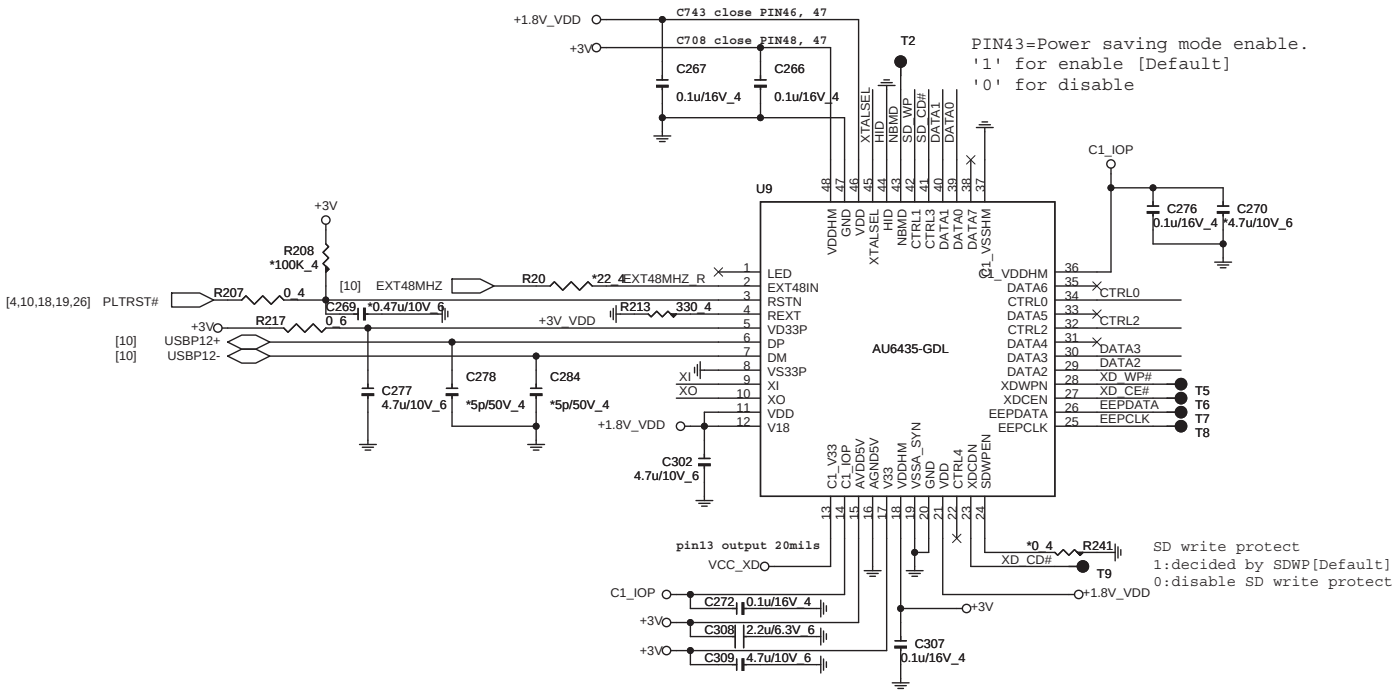


C-test , remove Q25,Q24, stuff R236,R235 fix POPO sound

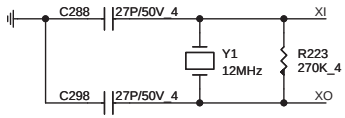


Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
Date: Tuesday, June 21, 2011	Sheet 22 of 34	

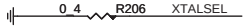
4 in 1 CARD READER IC (SD,MMC,xD,MS)



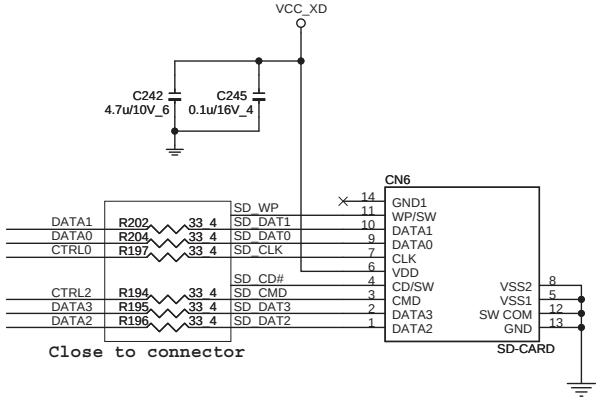
CTRL0, CRTL 1 trace length shorter ,
and surround with GND.



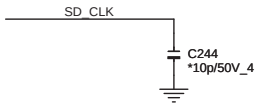
PIN45=Clock input selection
'1' for 48MHz input [Default,Internal PU]
'0' for 12MHz input



2 IN 1 CARD READER CONN (SD/MMC)



CLK Shorter than 1200 mil is good.

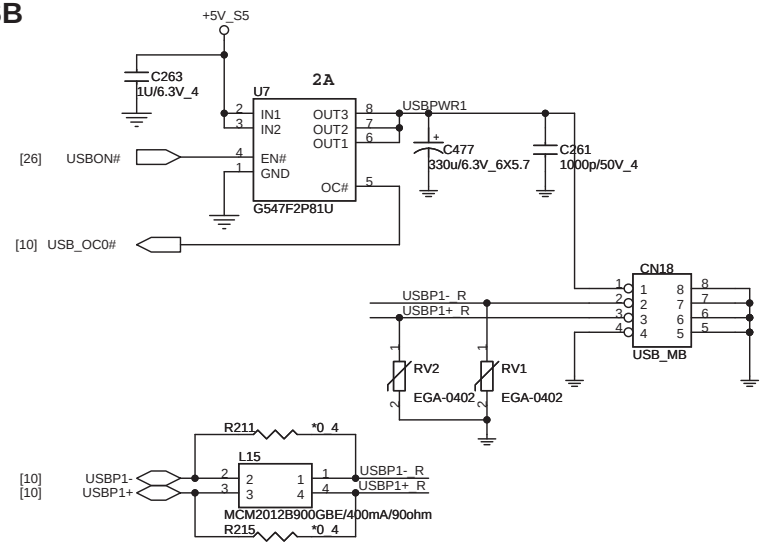


Main	DFHS11FR011
Second	DFHS11FR033

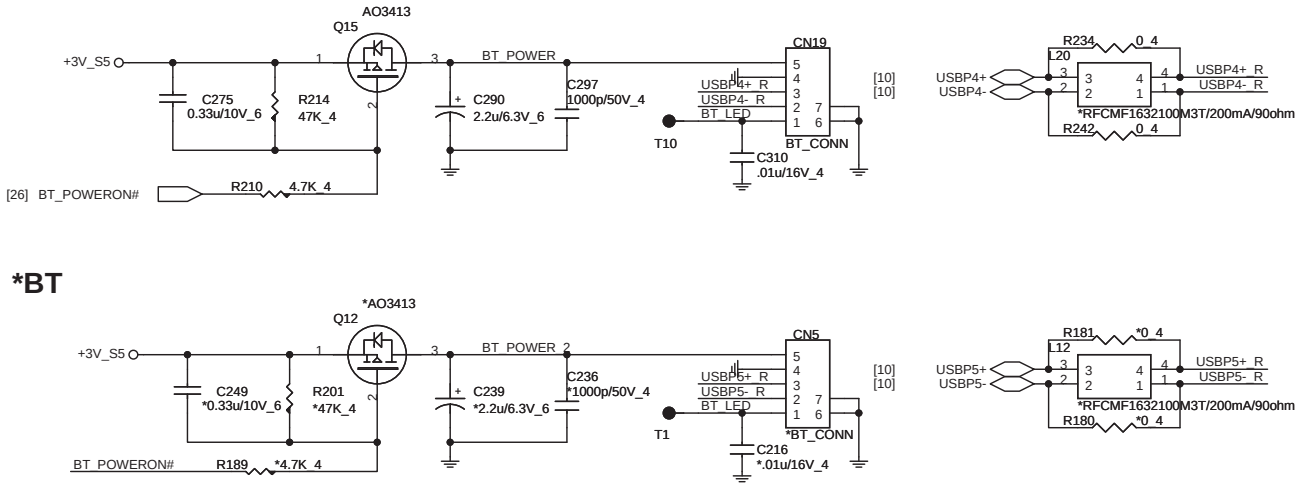
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date: Tuesday, June 21, 2011	Sheet 23 of 43	

USB

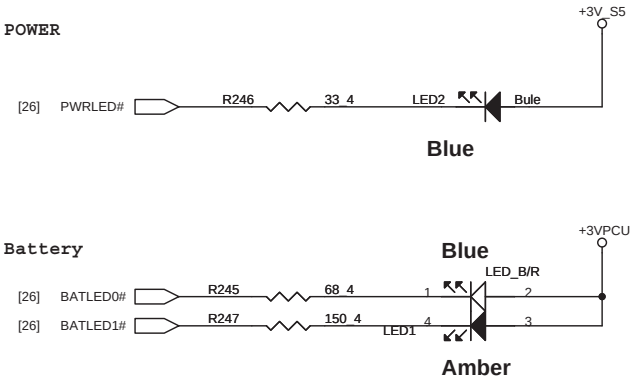


BT

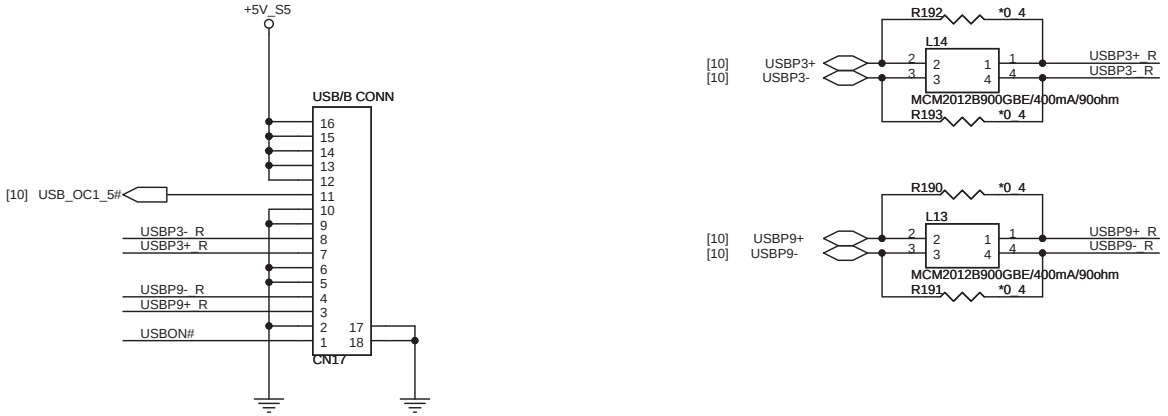


*BT

LED



USB/B

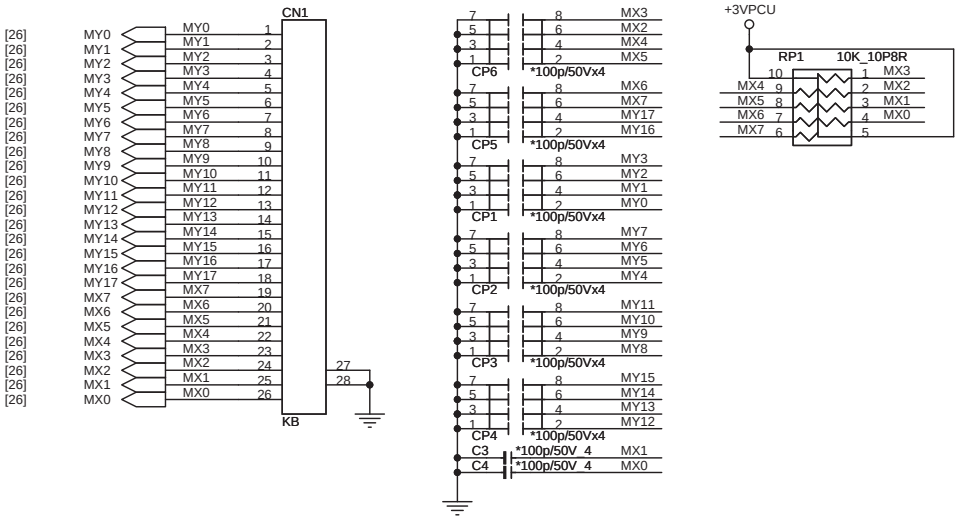


Quanta Computer Inc.

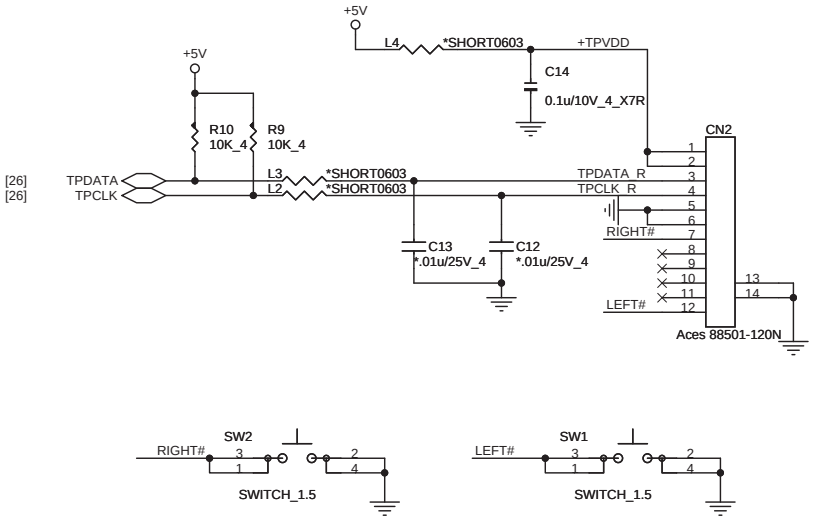
PROJECT : ZRL

Size	Document Number	Rev
	USB/ BT	1A
Date: Tuesday, June 21, 2011	Sheet 24 of 34	

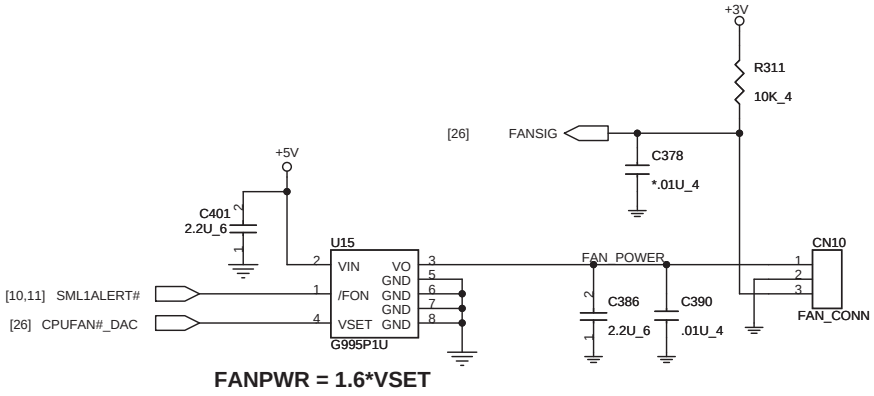
K/B



TP

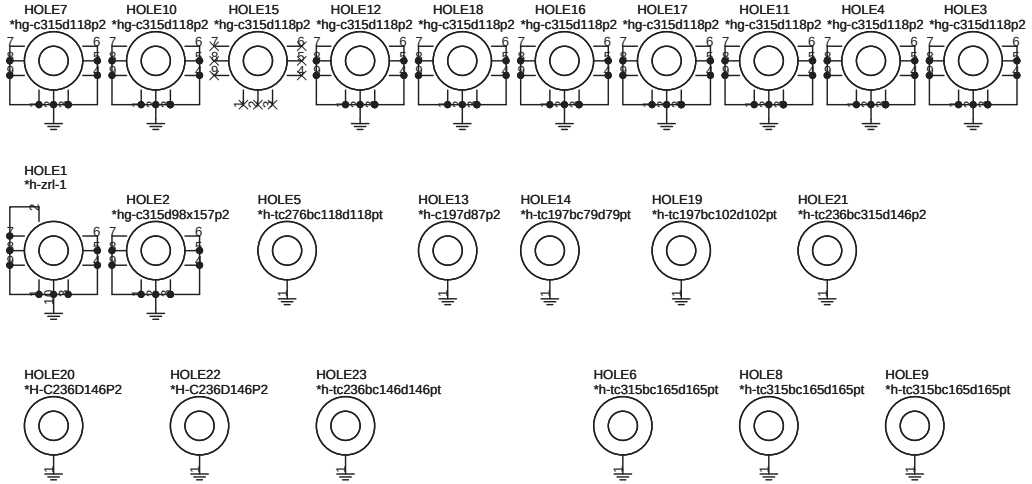


CPU FAN



FANPWR = 1.6*VSET

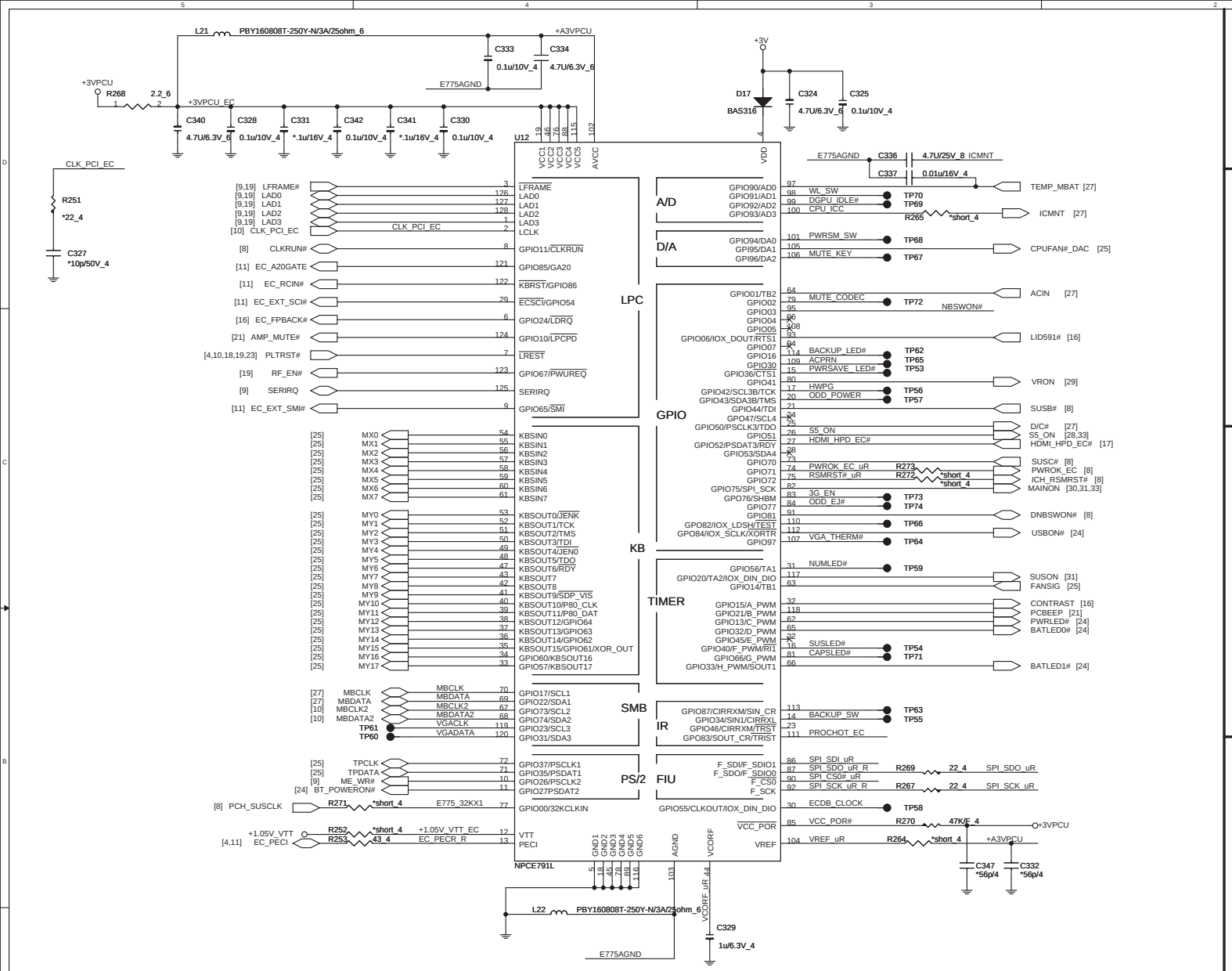
HOLE



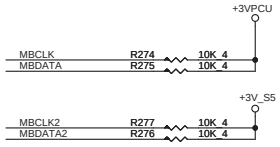
Quanta Computer Inc.

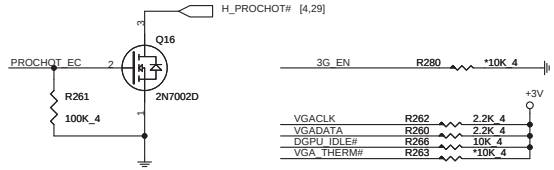
PROJECT : ZRL

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date: Tuesday, June 21, 2011	Sheet 25 of 34	

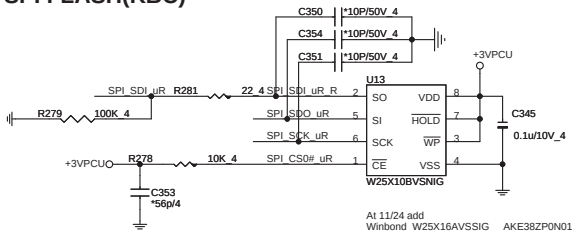


SM BUS PU(KBC)





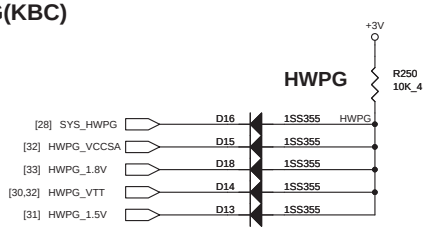
SPI FLASH(KBC)



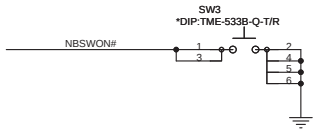
At 11/24 add

Winbond	W25X16AVSSIG	AKE38ZP0N01
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

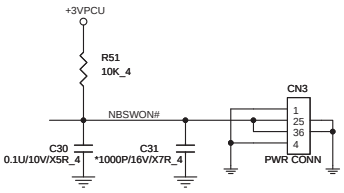
HWPG(KBC)



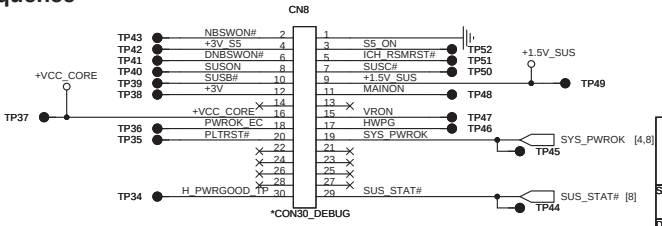
POWER-ON Switch(KBC)



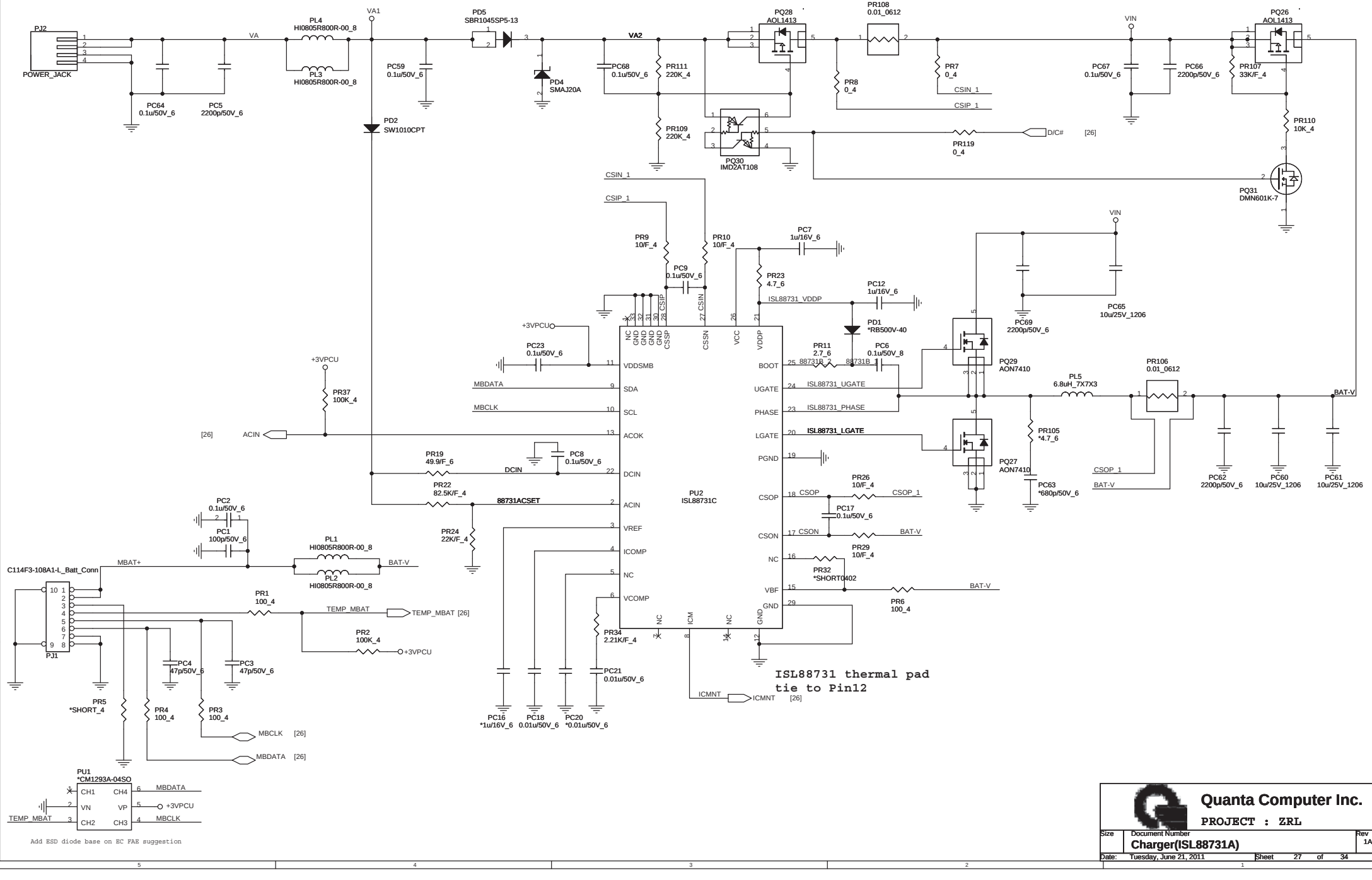
PWR/B



Power sequence



Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	WPCE791 & FLASH		1A
Date: Tuesday, June 21, 2011		Sheet 26 of 34	



Quanta Computer Inc.

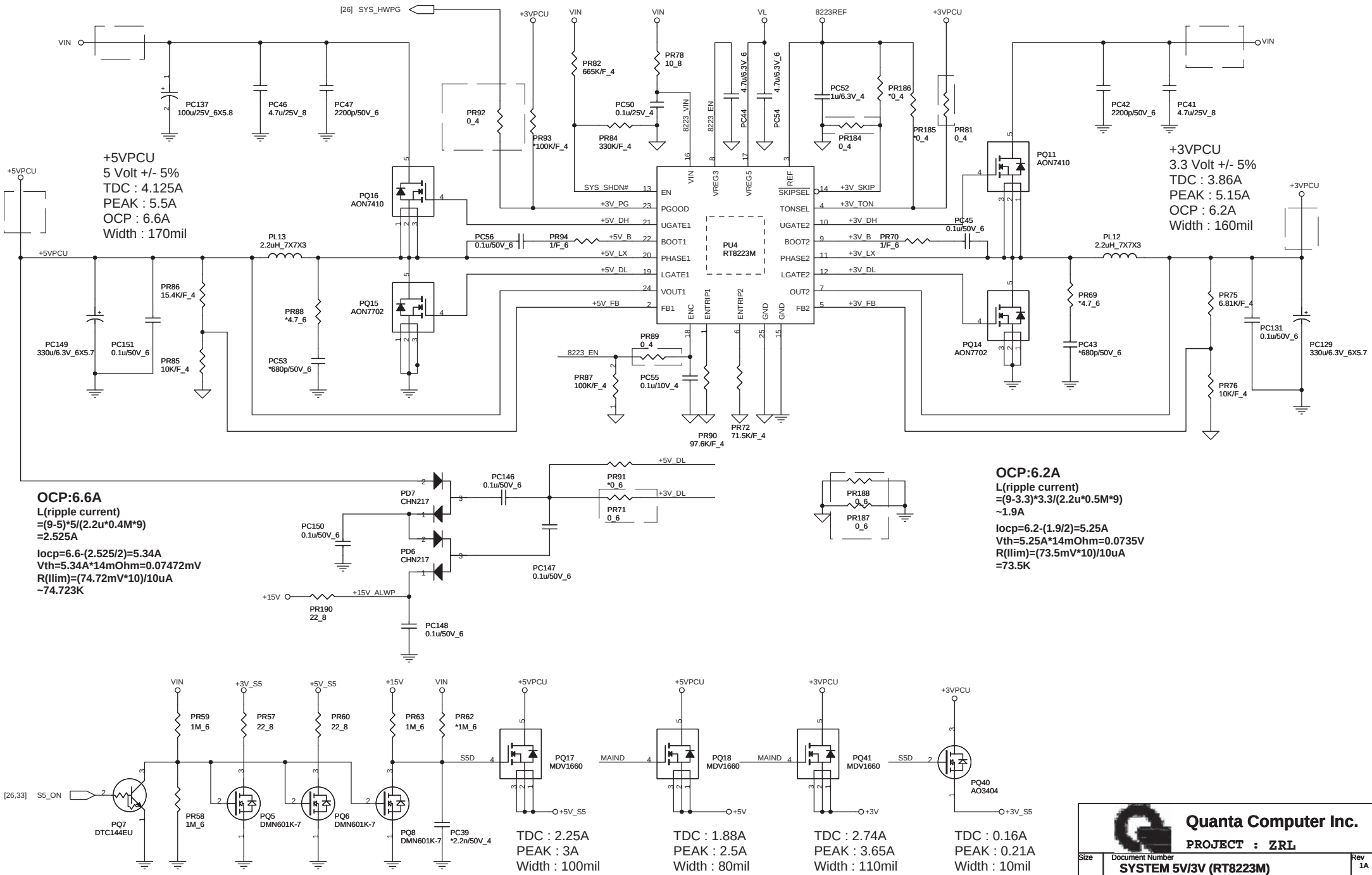
PROJECT : ZRL

Size	Document Number	Rev
	Charger(ISL88731A)	1A
Date: Tuesday, June 21, 2011	Sheet 27 of 34	

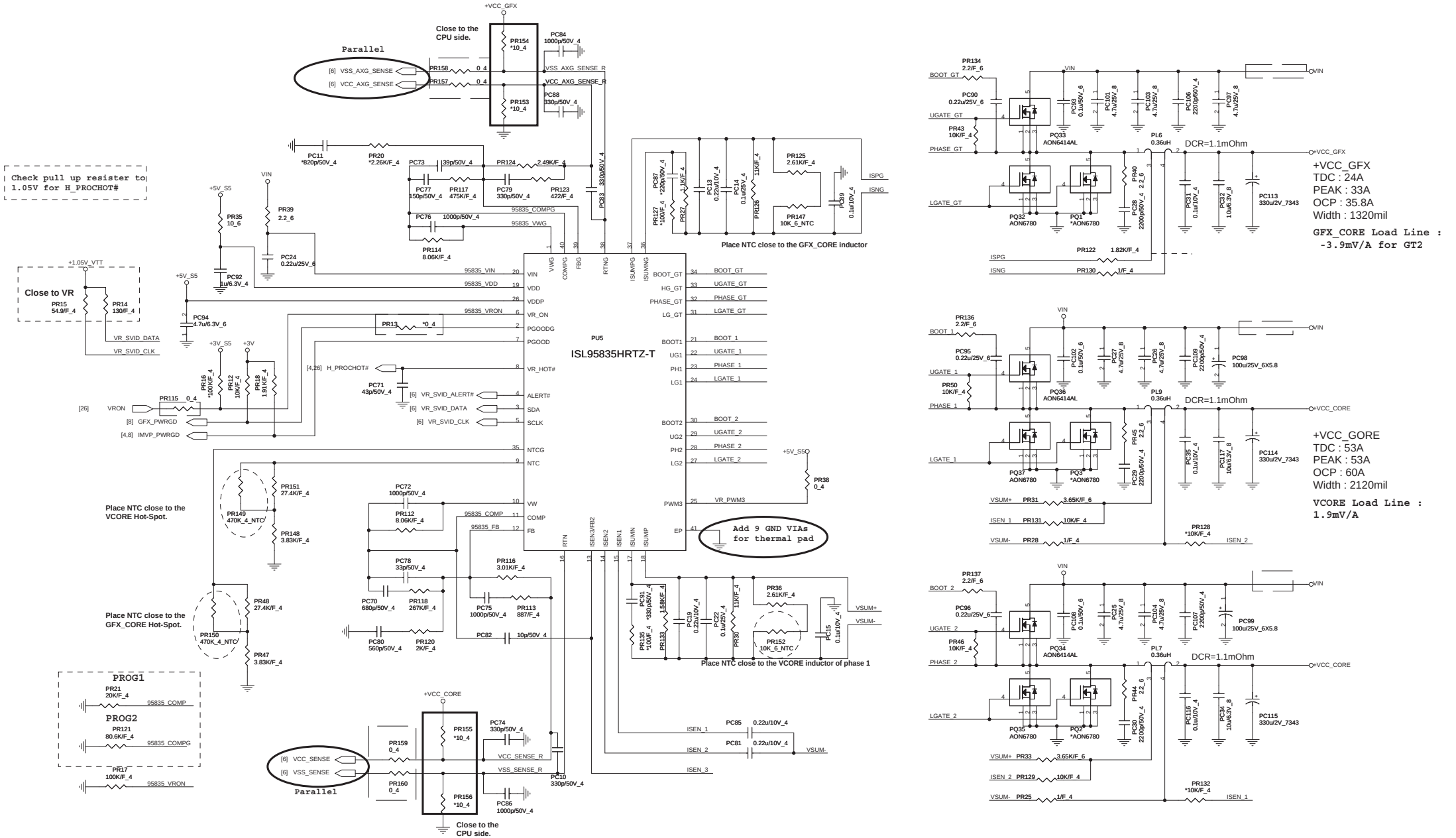
MAIND → MAIND [6,31,33]

SYS_SHDN# → SYS_SHDN# [4,33]

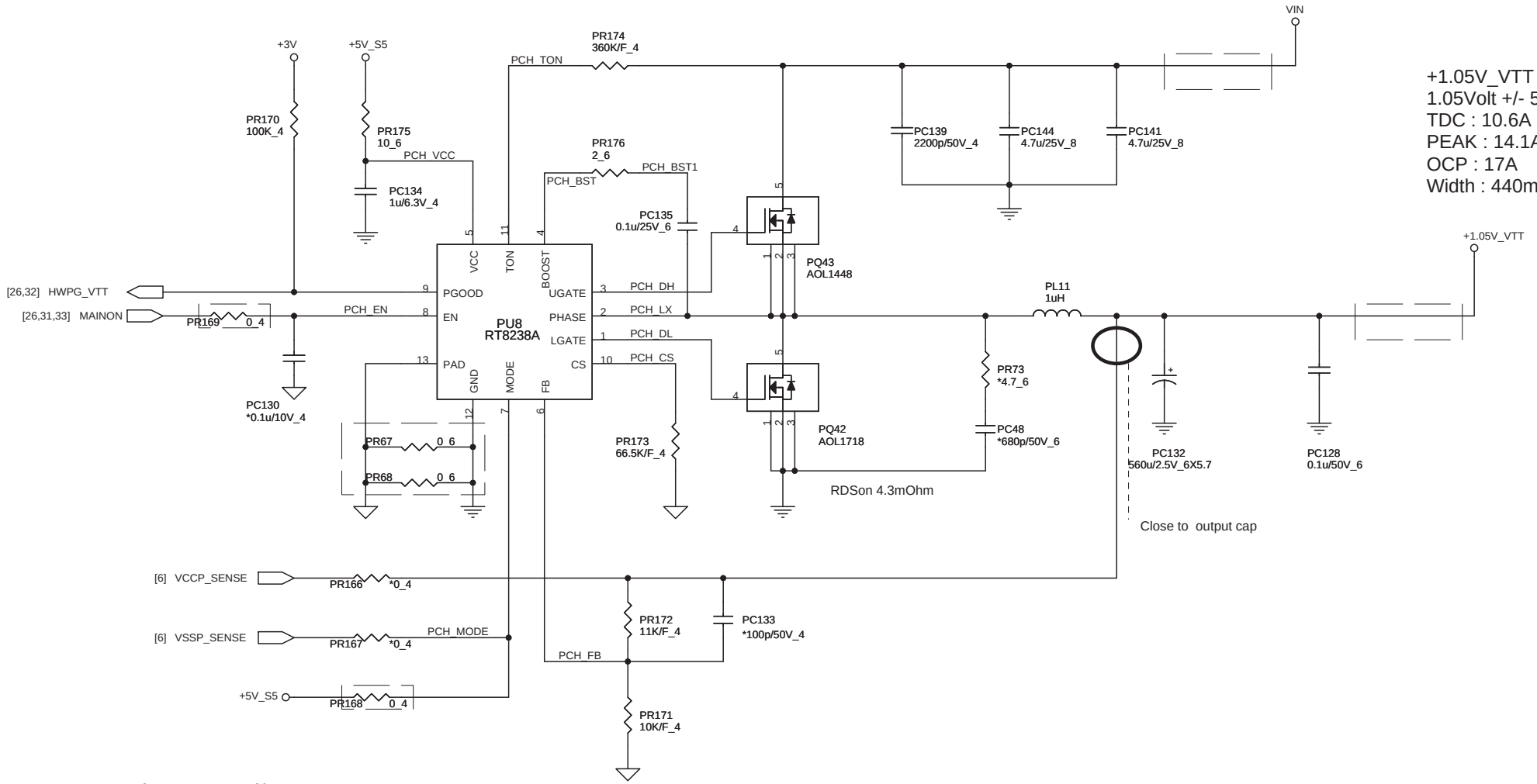
Ven=7.23V



Quanta Computer Inc.		
PROJECT : ZRL		
Size	Document Number: SYSTEM 5V/3V (RT8223M)	Rev: 1A
Date: Tuesday, June 21, 2011	Sheet 28 of 34	



Quanta Computer Inc.			
PROJECT : ZRL			
Size	Document Number		Rev
	+VCC_CORE & +VCC_GFX (ISL95835)		1A
Date: Tuesday, June 21, 2011	Sheet 29 of 34		



Ton=(8.8p*360K*1.05)/19-0.5=179.81ns
Icurrent=(19-1.05)*179ns/1uH=3.228A
Iocp=17-3.228/2=15.386A
Vcs=15.386*4.3mohm=0.06616V
Rcs=0.06616/1u=66.16Kohm

VOUT=(1+R1/R2)*0.5

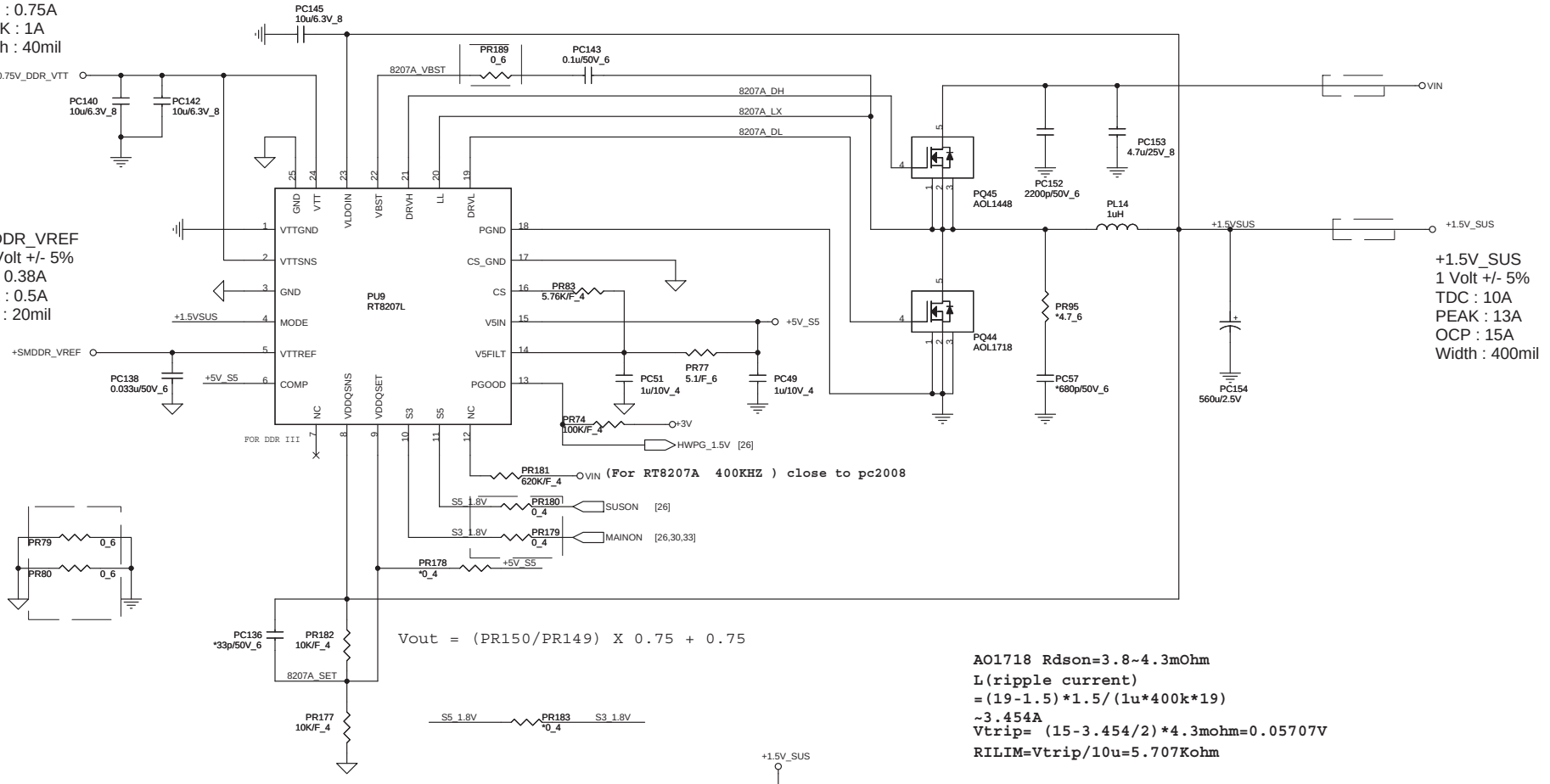
Quanta Computer Inc.

PROJECT : ZRL

Size	Document Number	Rev
	+PCH&VTT (RT8238A)	1A
Date: Tuesday, June 21, 2011	Sheet 30 of 34	

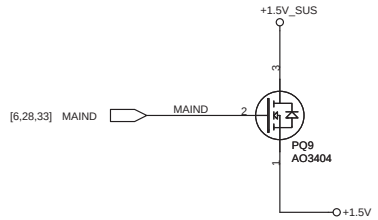
+0.75V_DDR_VTT
0.75 Volt +/- 5%
TDC : 0.75A
PEAK : 1A
Width : 40mil

+SMDDR_VREF
0.75 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil



+1.5V_SUS
1 Volt +/- 5%
TDC : 10A
PEAK : 13A
OCP : 15A
Width : 400mil

AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (15-3.454/2)*4.3mohm=0.05707V
RILIM=Vtrip/10u=5.707Kohm



+1.5V
1.5 Volt +/- 5%
TDC : 0.38A
PEAK : 0.5A
Width : 20mil

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

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	DDR 1.5V(RT8207A)	1A
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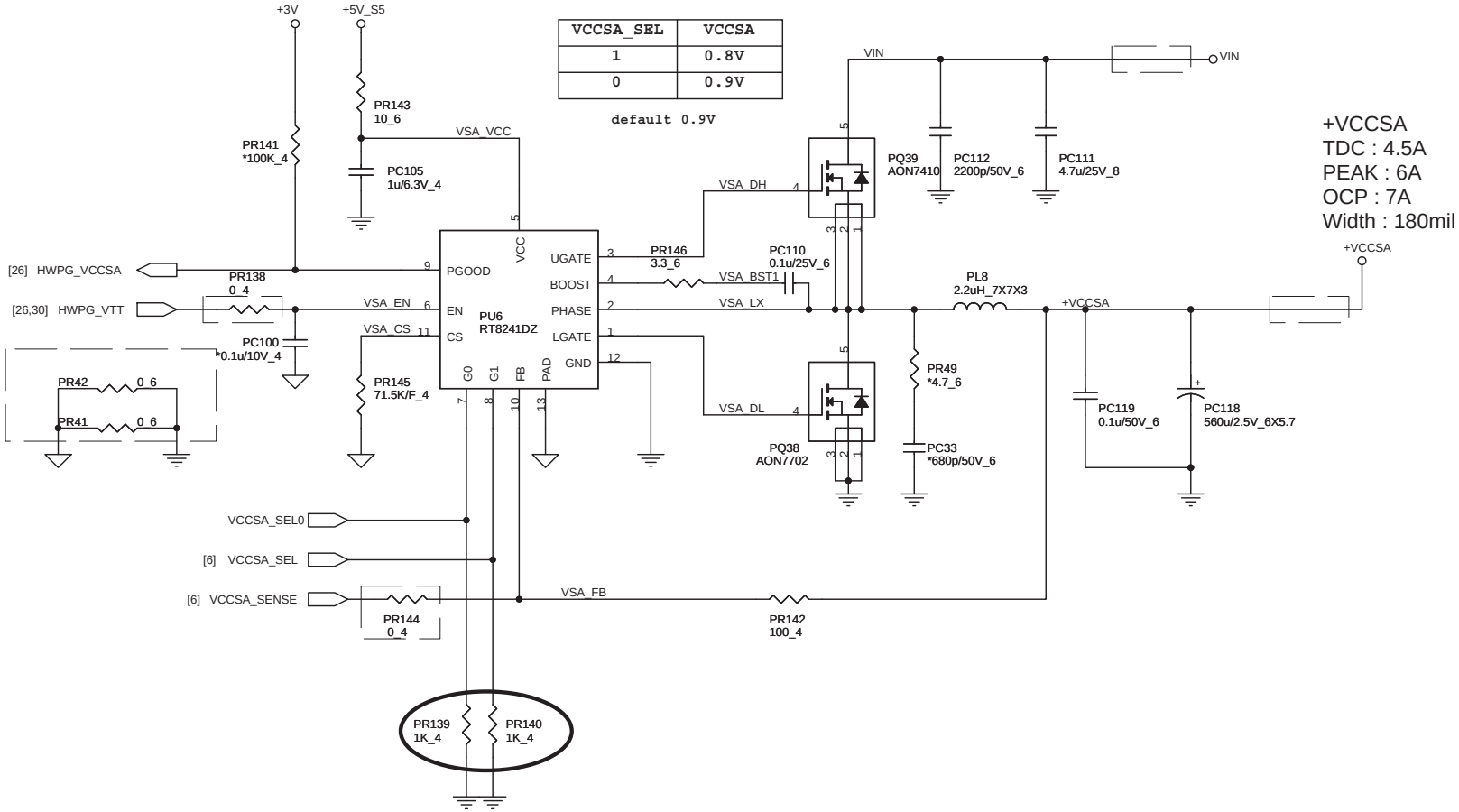
G0	G1	VCCSA
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

VCCSA_SEL	VCCSA
1	0.8V
0	0.9V

default 0.9V



+VCCSA
TDC : 4.5A
PEAK : 6A
OCP : 7A
Width : 180mil

OCP=7A
Iripple=(19-0.9)*0.9/(2.2u*300K*19)
=1.299A
Rth=14mohm*8*(7-0.65)/10uA
=71.125K
Ipeak=8.299A

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	+VCCSA	1A
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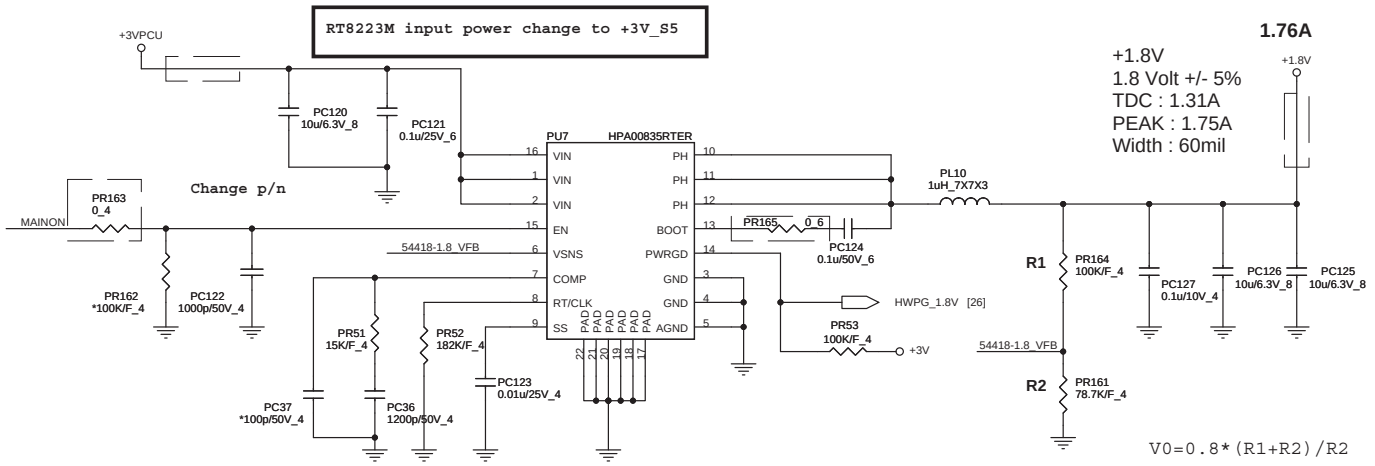
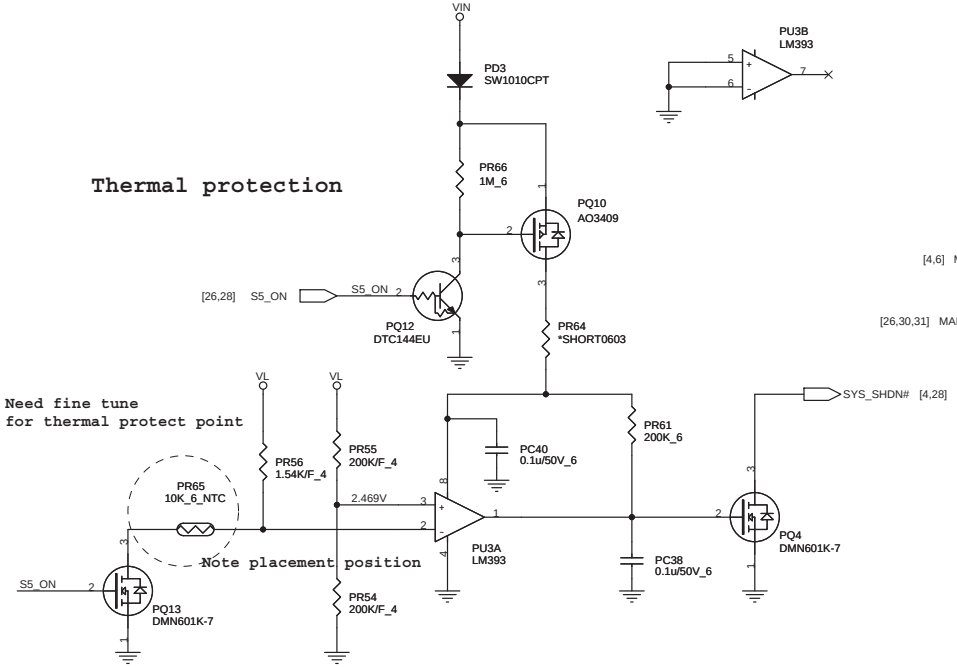
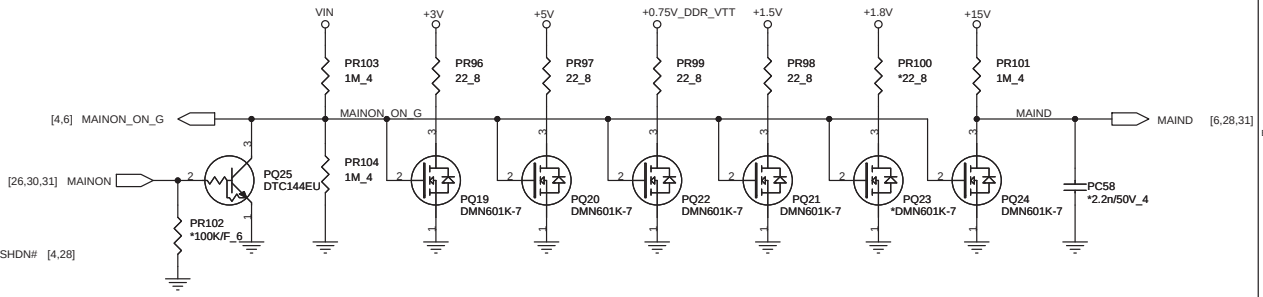


For EC control thermal protection (output 3.3V)





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Size	Document Number	Rev
	Discharge/1.8V)	1A

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1 7/7 modify

CHANGE LIST

Model	date	CHANGE LIST
ZRL	5/18	page16 : L6,L8,L10 change to 0ohm C104,C86,C68 remove for monitor issue L5,L7,L9 change to 0603 package
		page 8 : add R422 for GFX_PWRGD
		page 27 :PQ26,PQ28 change footprint
		page 17 :Remove U6 HDMI level shift
		page 9 :add Q26,R423 to separate CODEC SYNC signal
		page 22 :change R239,R240 to 47 ohm by realtek
	5/25	page 29 : change PR133 to 1.58K, PR124 to 2.49K ,PC22,PC14 to 0.1u
		page 22 : remove Q25,Q24, stuff R236,R235 fix POPO sound
	6/9	page 24 : change R246 to 33ohm,R245 to 68ohm, R247 to 150ohm for LED brightness.
	2A	

MODEL	ZRL	
	FROM	To
	X	1A
	X	1A
	X	1A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
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	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	1A	B2A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
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	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A
	B2A	C3A

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	Change list2	1A

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DOC NO.	PROJECT MODEL :	ZRL	APPROVED BY:	Spruce Wu	DATE:
	PART NUMBER:	31ZRLMB0000	DRAWING BY:	Ronnie Liu	REVISON: