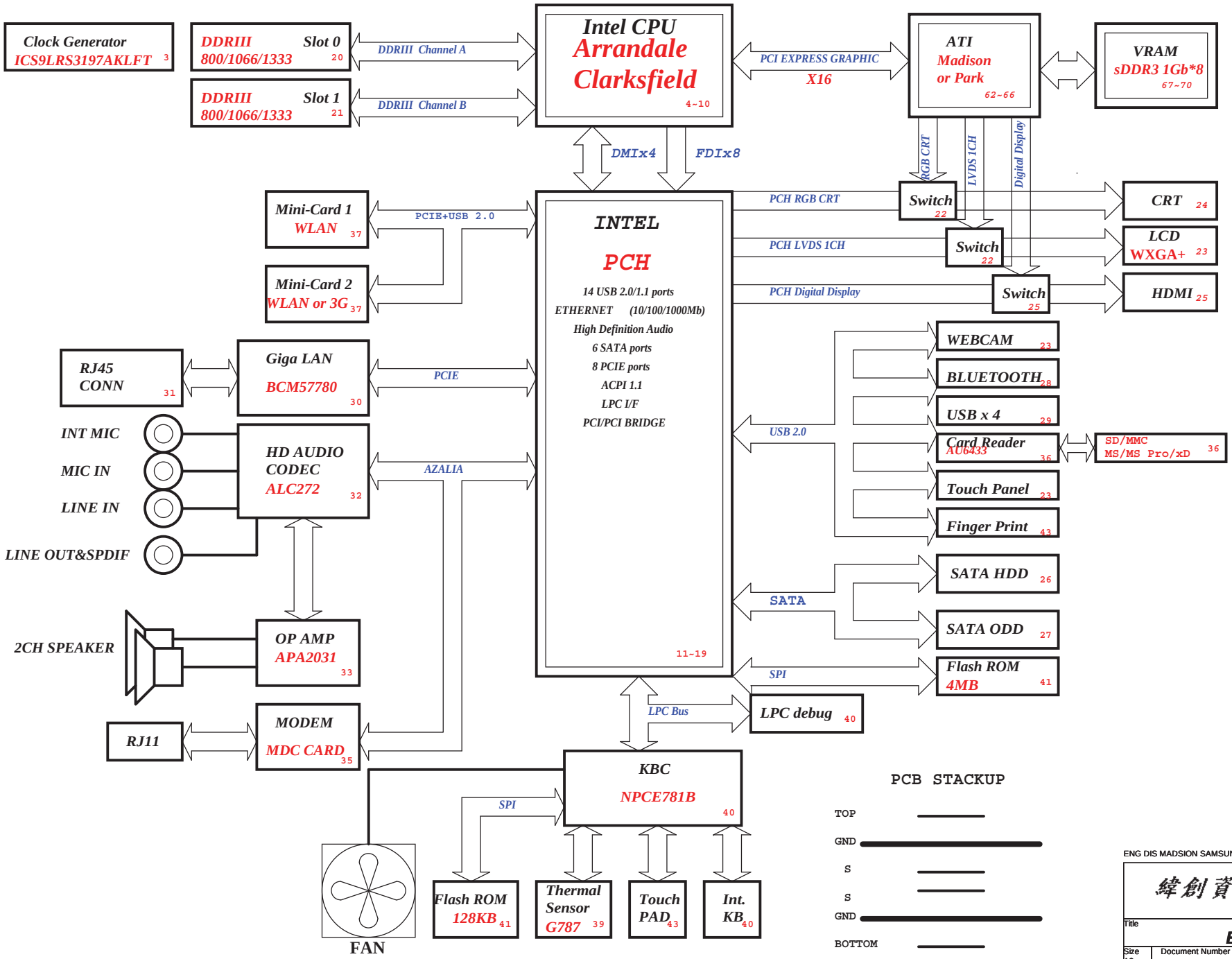
JV50-CP Block Diagram

Project code: 91.4GD01.001
PCB P/N : 48.4GD01.0SB
REVISION : SB 09285



PCB STACKUP

TOP	
GND	
S	
S	
GND	
BOTTOM	

CPU DC/DC ISL62882	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

SYSTEM DC/DC TPS51123	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 50

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 51

RT9025	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0 50

G2997	
INPUTS	OUTPUTS
1D5V_S3	0D75_S0 52

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 54

SYSTEM DC/DC TPS51117	
INPUTS	OUTPUTS
DCBATOUT	+VGA_CORE 55

CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

ENG DIS MADSION SAMSUNG

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: Block Diagram
Size: A3 | Document Number: JV50-CP | Rev: SA
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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE3	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	USB4
3	MINICARD1
4	WECAM
5	Touch Panel
6	NC
7	NC
8	NC
9	USB1(HS)
10	Finger Print
11	Blue Tooth
12	MINIC2
13	Cardreader

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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Title: **Table of Content**

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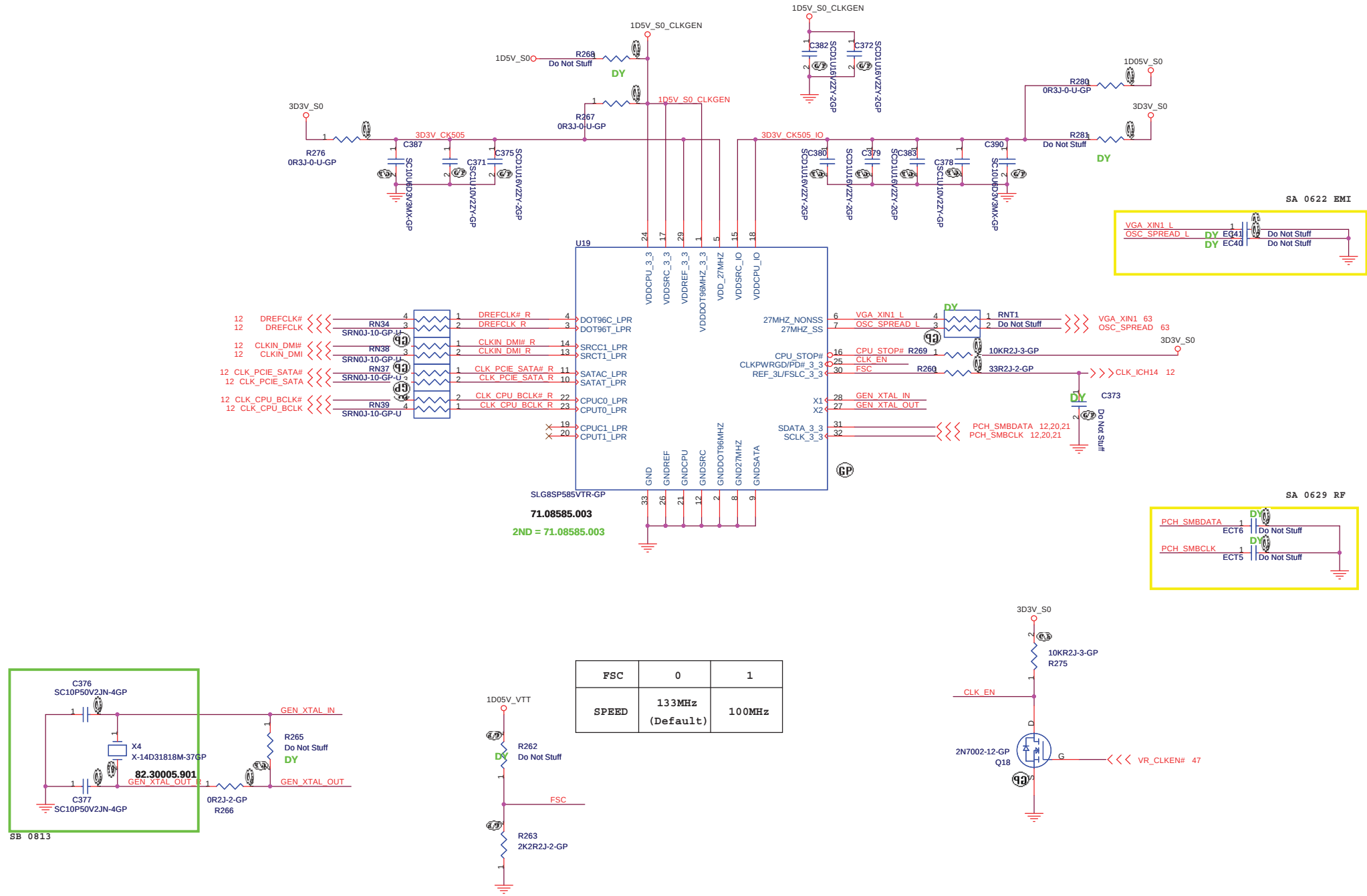

FSC	0	1
SPEED	133MHz (Default)	100MHz

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Title: **Clock Generator**

Size	Document Number	Rev
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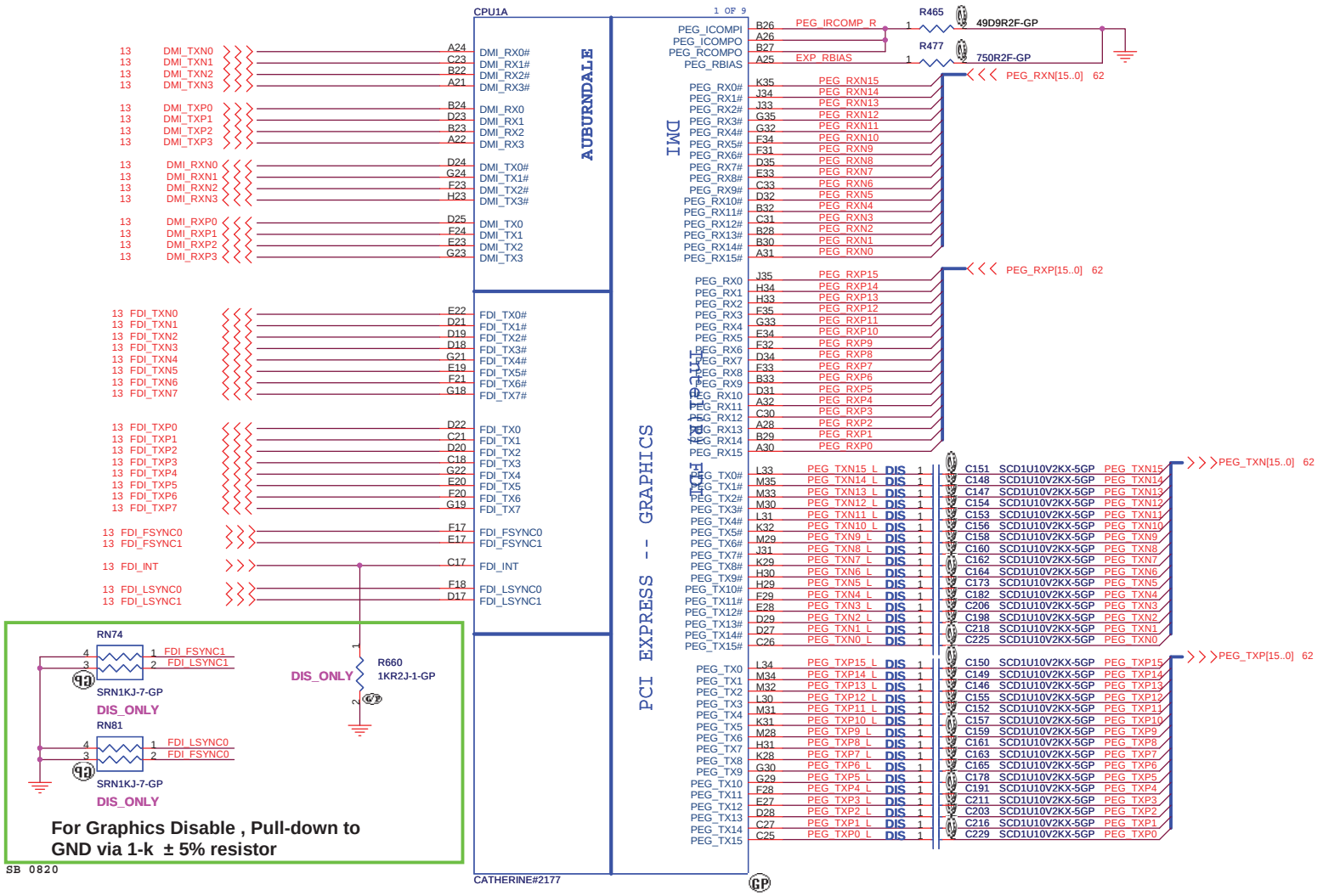

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CPU (1/7)		
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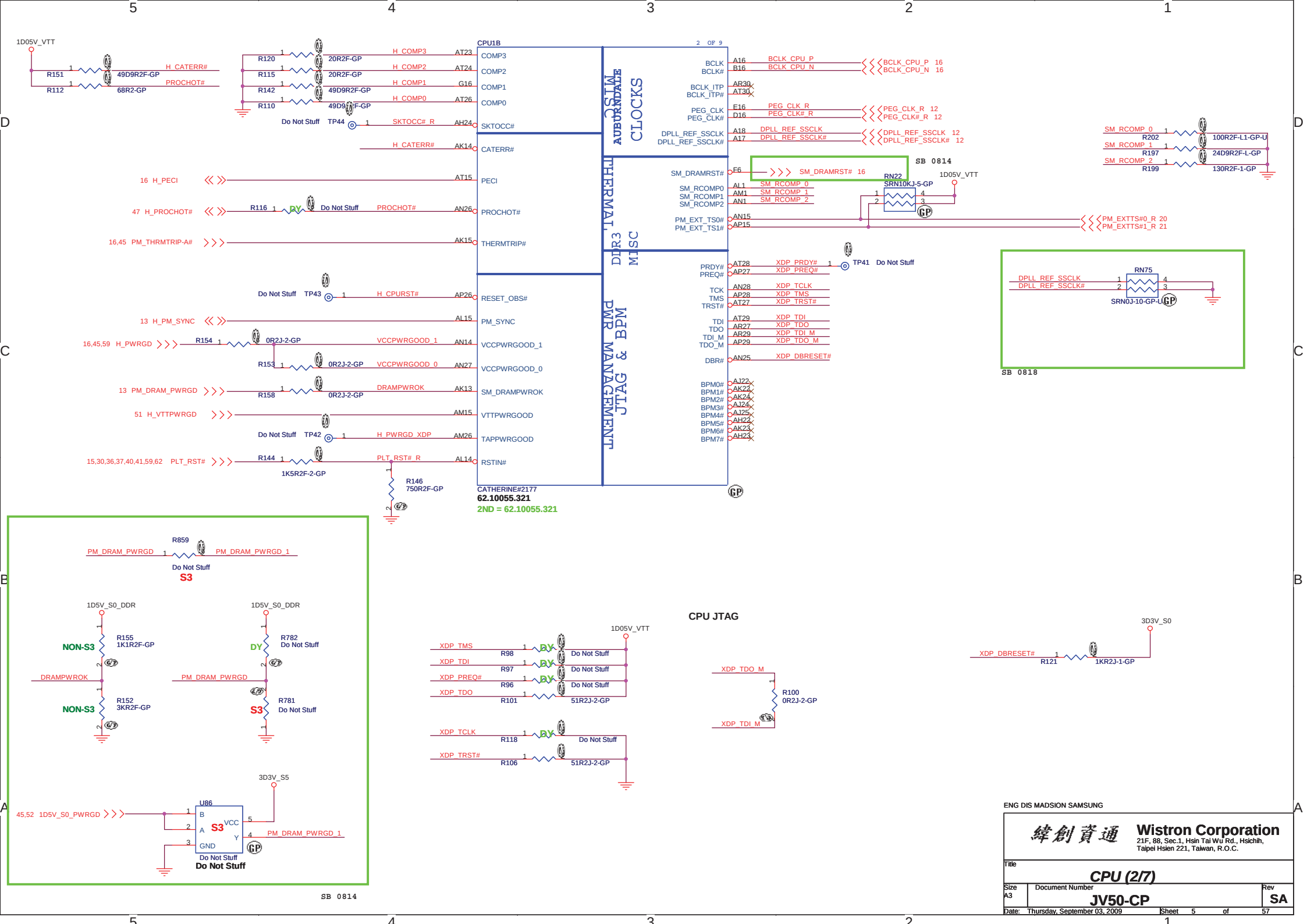
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2 OF 9
CLOCKS
MISC
THERMAL
DIR
MISC
PWR MANAGEMENT
JTAG & BPM
CATHERINE#2177
62.10055.321
2ND = 62.10055.321
SB 0814
SB 0818
CPU JTAG
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (2/7)
Size
A3
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
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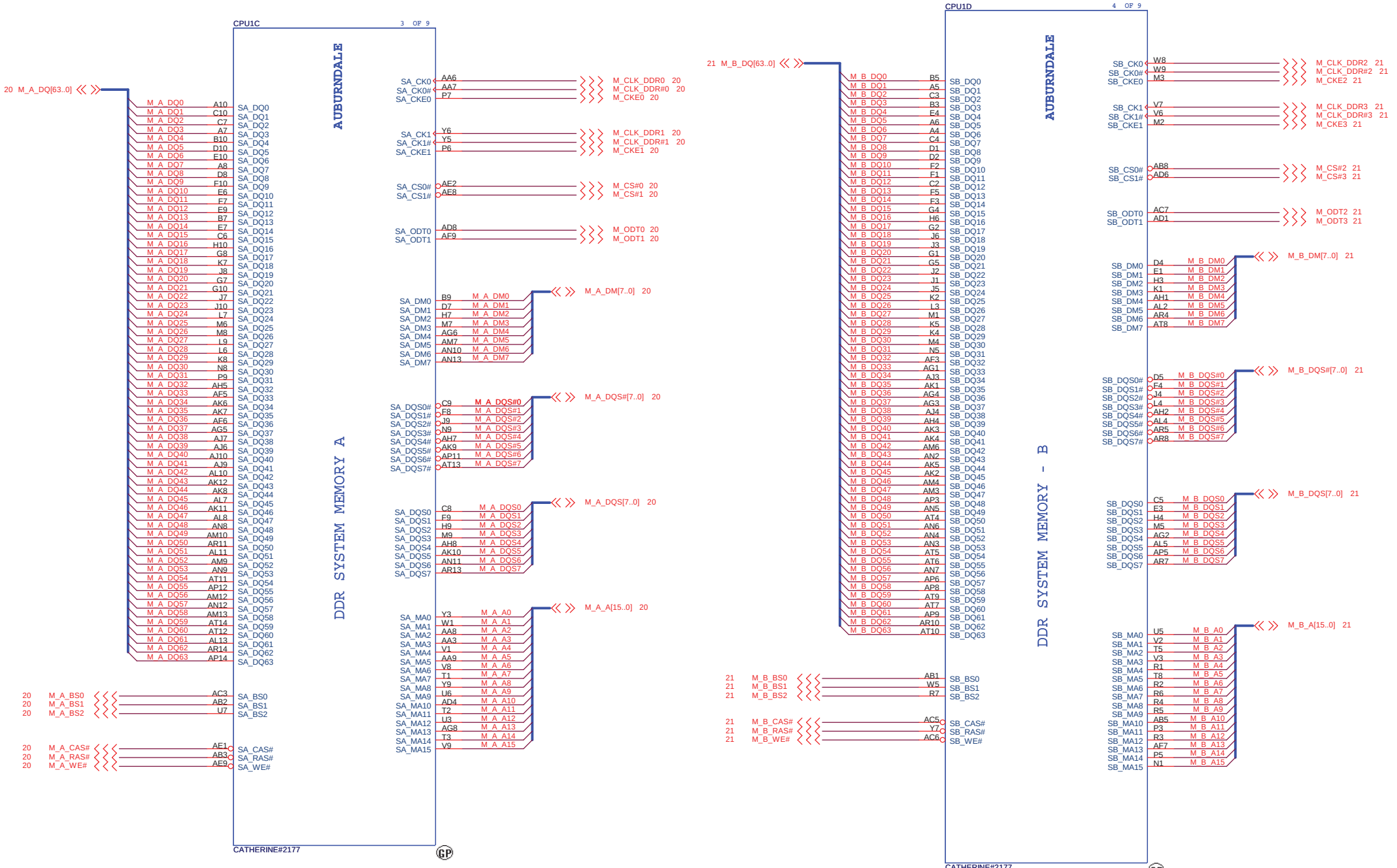
CPU1C
3 OF 9
AUBURNDALE
DDR SYSTEM MEMORY A
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M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 C7 SA_DQ2
M_A_DQ3 A7 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 E7 SA_DQ11
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M_A_DQ36 AF6 SA_DQ36
M_A_DQ37 AG5 SA_DQ37
M_A_DQ38 AJ7 SA_DQ38
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M_A_DQ40 AJ10 SA_DQ40
M_A_DQ41 AJ9 SA_DQ41
M_A_DQ42 AL10 SA_DQ42
M_A_DQ43 AK12 SA_DQ43
M_A_DQ44 AK8 SA_DQ44
M_A_DQ45 AL7 SA_DQ45
M_A_DQ46 AK11 SA_DQ46
M_A_DQ47 AL8 SA_DQ47
M_A_DQ48 AN8 SA_DQ48
M_A_DQ49 AM10 SA_DQ49
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M_A_DQ63 AP14 SA_DQ63
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20 M_A_BS2 U7 SA_BS2
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20 M_A_RAS# AB3 SA_RAS#
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SA_CK0# AA7 M_CLK_DDR#0 20
SA_CKE0 P7 M_CKE0 20
SA_CK1 Y6 M_CLK_DDR1 20
SA_CK1# Y5 M_CLK_DDR#1 20
SA_CKE1 P6 M_CKE1 20
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SA_CS1# AE8 M_CS#1 20
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SA_ODT1 AF9 M_ODT1 20
SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7
M_A_DM[7..0] 20
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SA_DQS1# F8 M_A_DQS#1
SA_DQS2# J9 M_A_DQS#2
SA_DQS3# N9 M_A_DQS#3
SA_DQS4# AH7 M_A_DQS#4
SA_DQS5# AK9 M_A_DQS#5
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SA_MA10 AD4 M_A_A10
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SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15
M_A_A[15..0] 20
CATHERINE#2177
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62.10055.321
CPU1D
4 OF 9
AUBURNDALE
DDR SYSTEM MEMORY - B
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M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
M_B_DQ5 A6 SB_DQ5
M_B_DQ6 A4 SB_DQ6
M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
M_B_DQ9 D2 SB_DQ9
M_B_DQ10 F2 SB_DQ10
M_B_DQ11 F1 SB_DQ11
M_B_DQ12 C2 SB_DQ12
M_B_DQ13 E5 SB_DQ13
M_B_DQ14 E3 SB_DQ14
M_B_DQ15 G4 SB_DQ15
M_B_DQ16 H6 SB_DQ16
M_B_DQ17 G2 SB_DQ17
M_B_DQ18 J6 SB_DQ18
M_B_DQ19 J3 SB_DQ19
M_B_DQ20 G1 SB_DQ20
M_B_DQ21 G5 SB_DQ21
M_B_DQ22 J2 SB_DQ22
M_B_DQ23 J1 SB_DQ23
M_B_DQ24 J5 SB_DQ24
M_B_DQ25 K2 SB_DQ25
M_B_DQ26 L3 SB_DQ26
M_B_DQ27 M1 SB_DQ27
M_B_DQ28 K5 SB_DQ28
M_B_DQ29 K4 SB_DQ29
M_B_DQ30 M4 SB_DQ30
M_B_DQ31 N5 SB_DQ31
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21 M_B_BS1 W5 SB_BS1
21 M_B_BS2 R7 SB_BS2
21 M_B_CAS# AC5 SB_CAS#
21 M_B_RAS# Y7 SB_RAS#
21 M_B_WE# AC6 SB_WE#
SB_CK0 W8 M_CLK_DDR2 21
SB_CK0# W9 M_CLK_DDR#2 21
SB_CKE0 M3 M_CKE2 21
SB_CK1 V7 M_CLK_DDR3 21
SB_CK1# V6 M_CLK_DDR#3 21
SB_CKE1 M2 M_CKE3 21
SB_CS0# AB8 M_CS#2 21
SB_CS1# AD6 M_CS#3 21
SB_ODT0 AC7 M_ODT2 21
SB_ODT1 AD1 M_ODT3 21
SB_DM0 D4 M_B_DM0
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SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
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SB_DQS4# AH2 M_B_DQS#4
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SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AF7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15
M_B_A[15..0] 21
CATHERINE#2177
2ND = 62.10055.321
62.10055.321
ENG DIS MAD GP SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (3/7)
Size A3
Document Number
JV50-CP
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Date: Thursday, September 03, 2009
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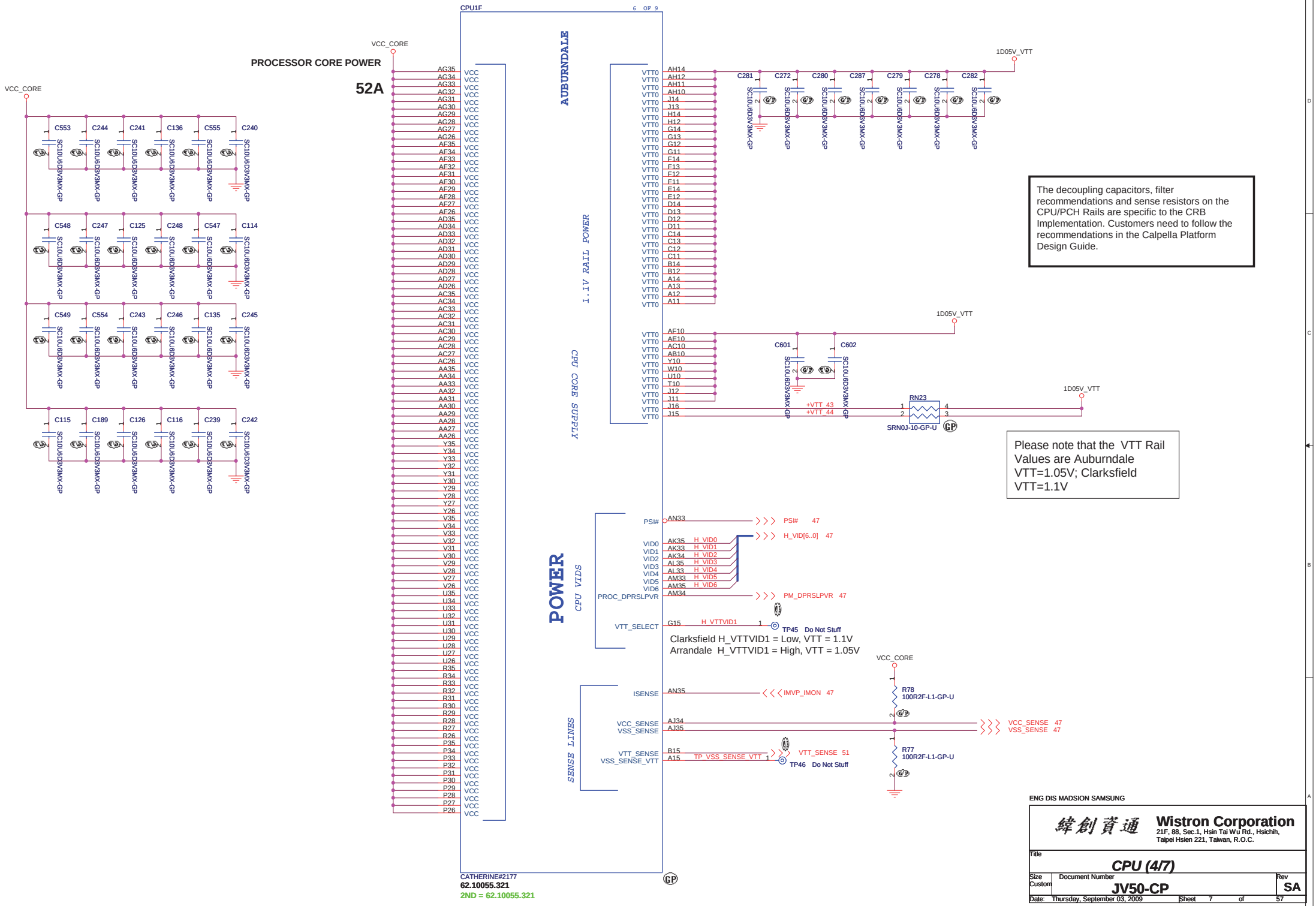
PROCESSOR CORE POWER
52A
VCC_CORE
CPU1F
6 OF 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
POWER
CPU VIDS
PSI#
VID0
VID1
VID2
VID3
VID4
VID5
VID6
PROC_DPRSLPVR
VTT_SELECT
TP45 Do Not Stuff
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
SENSE LINES
ISENSE
VCC_SENSE
VSS_SENSE
VTT_SENSE
VSS_SENSE_VTT
TP46 Do Not Stuff
R78 100R2F-L1-GP-U
R77 100R2F-L1-GP-U
RN23 SRN0J-10-GP-U
CATHERINE#2177
62.10055.321
2ND = 62.10055.321
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4/7)
Size Custom
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
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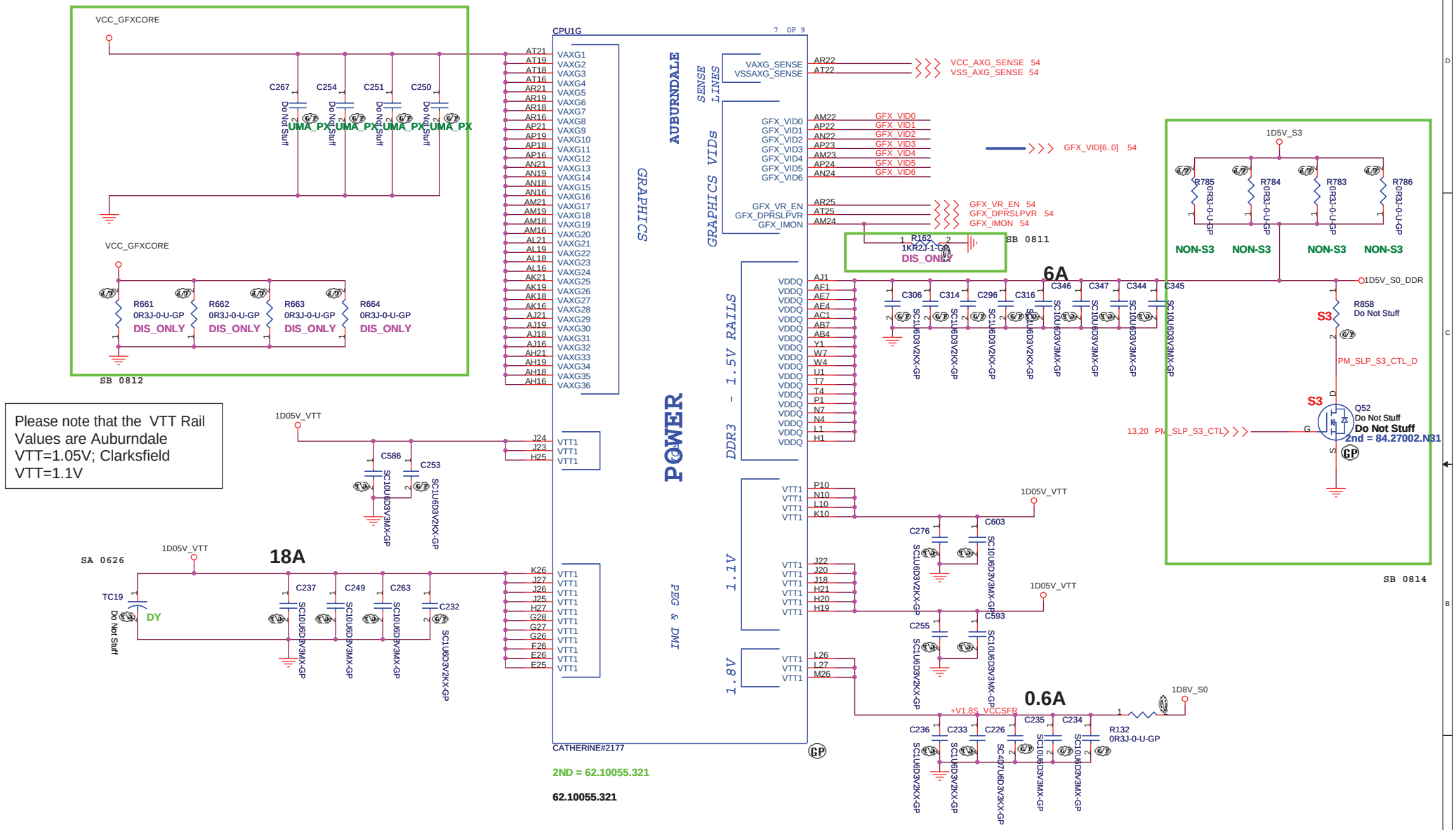

Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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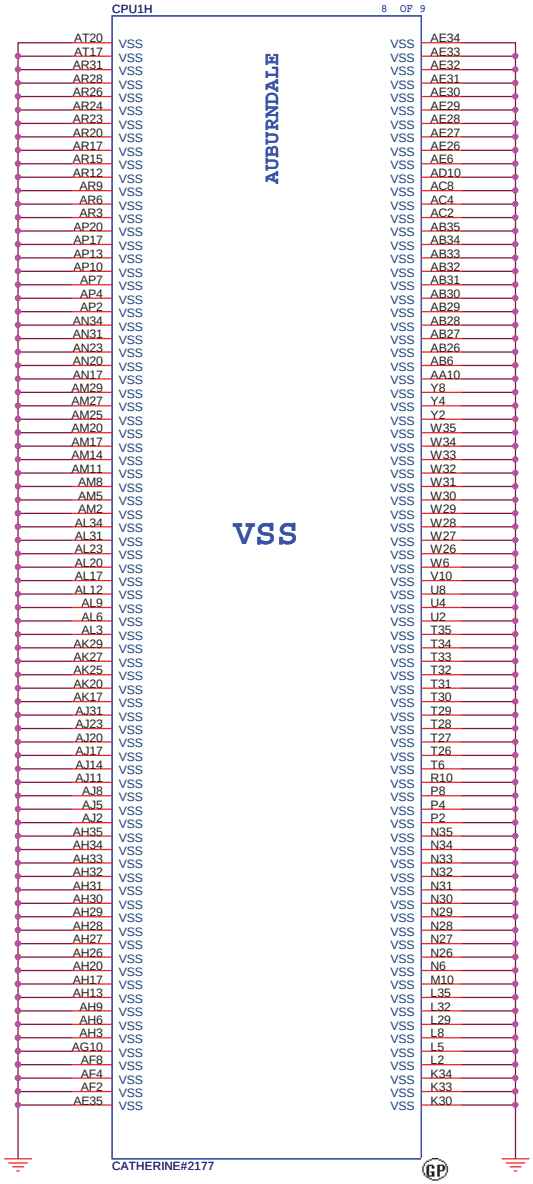
Title: **CPU (5/7)**		
Size: A3	Document Number: **JV50-CP**	Rev: **SA**
Date: Thursday, September 03, 2009	Sheet 8 of 57	



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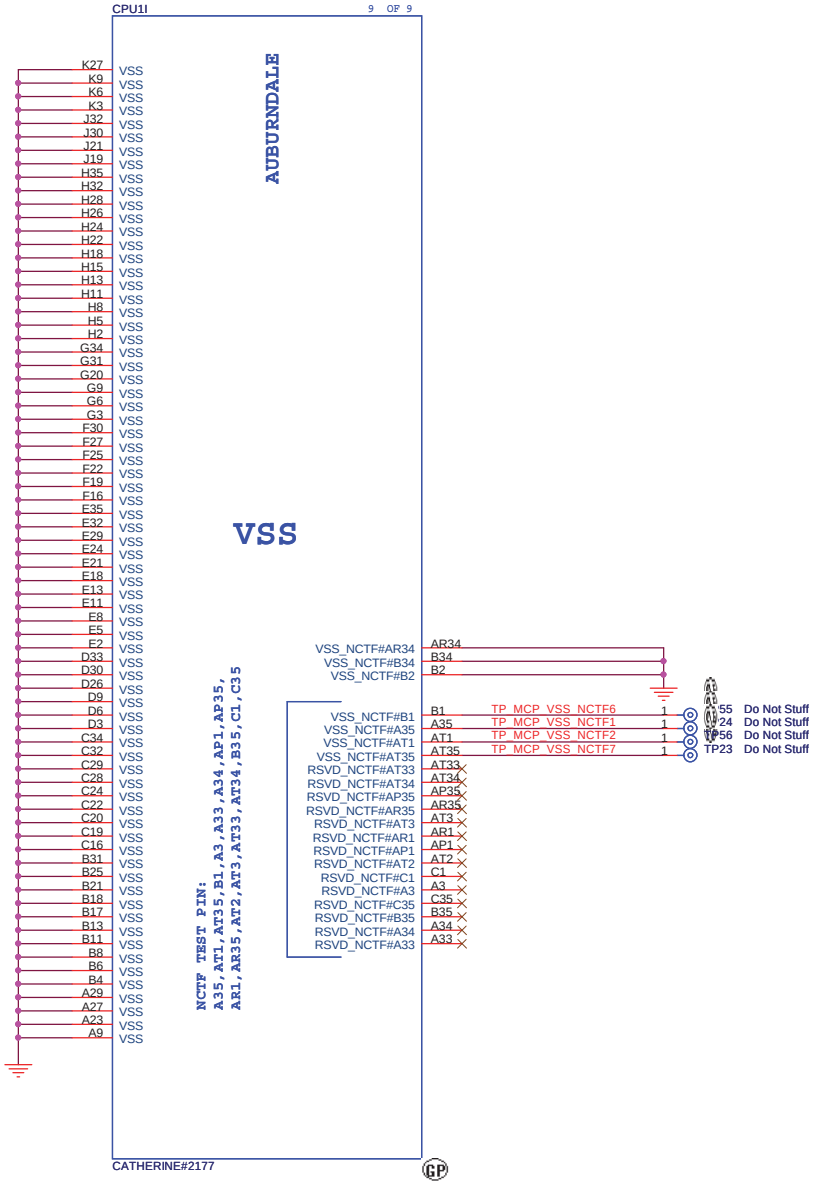
62.10055.321



2ND = 62.10055.321

62.10055.321

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (6/7)

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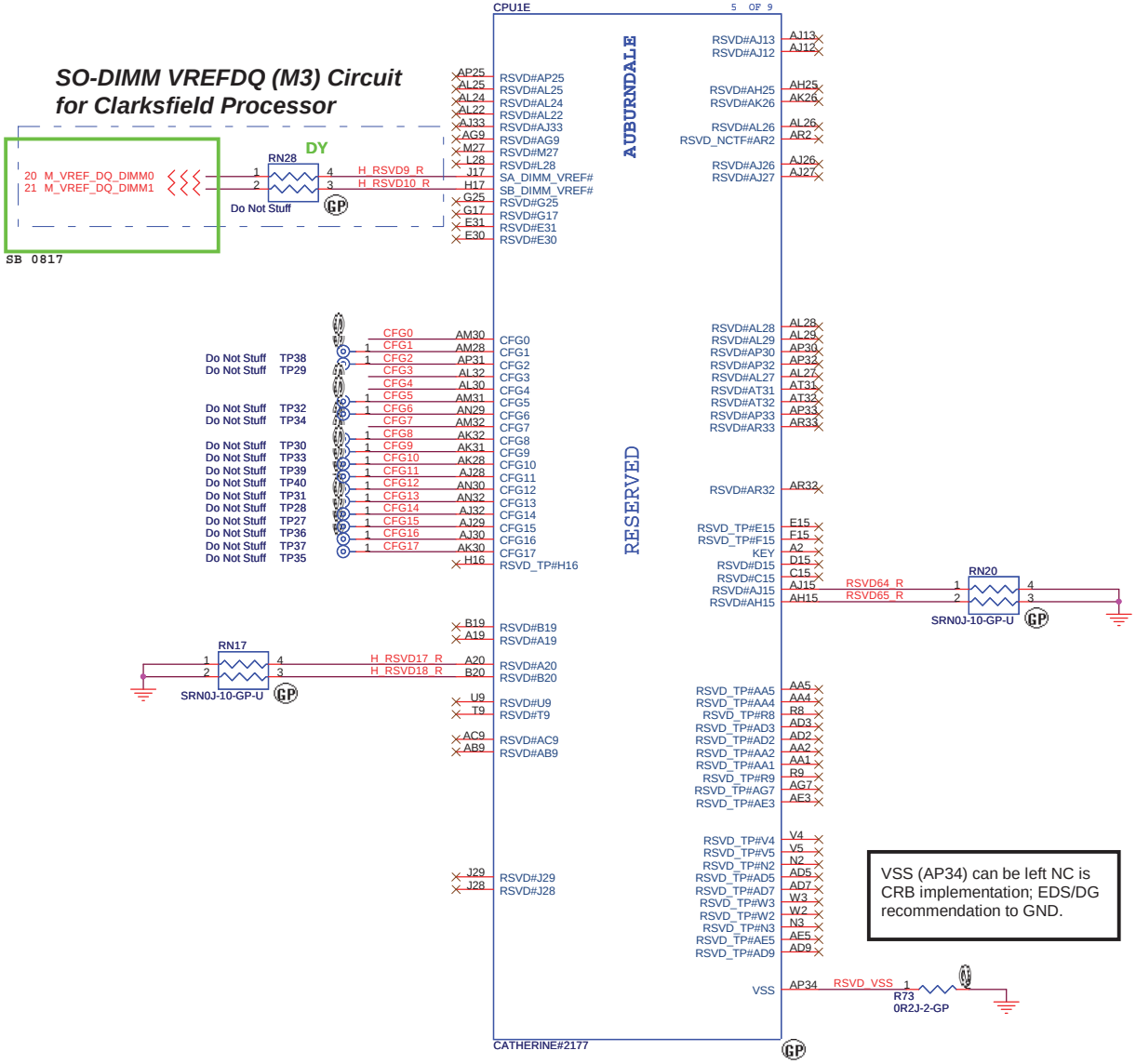
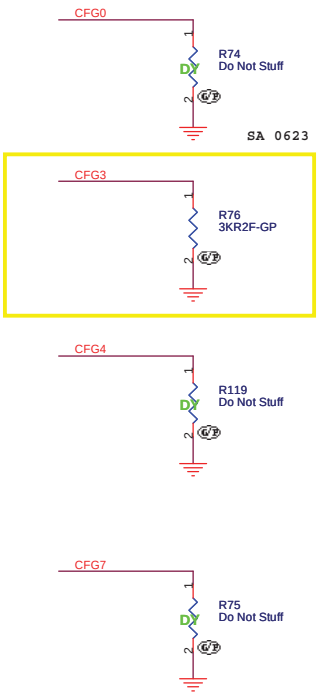
SO-DIMM VREFDQ (M3) Circuit for Clarksfield Processor



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.

2ND = 62.10055.321

62.10055.321



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (7/7)

Size: A3 | Document Number: JV50-CP | Rev: SA

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integrated VccSus1_05,VccSus1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

SA 0629 RF

SB 0825

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SA 0709

When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

HDD

ODD

ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (1/9)

Size	Document Number	Rev
A3	JV50-CP	SA

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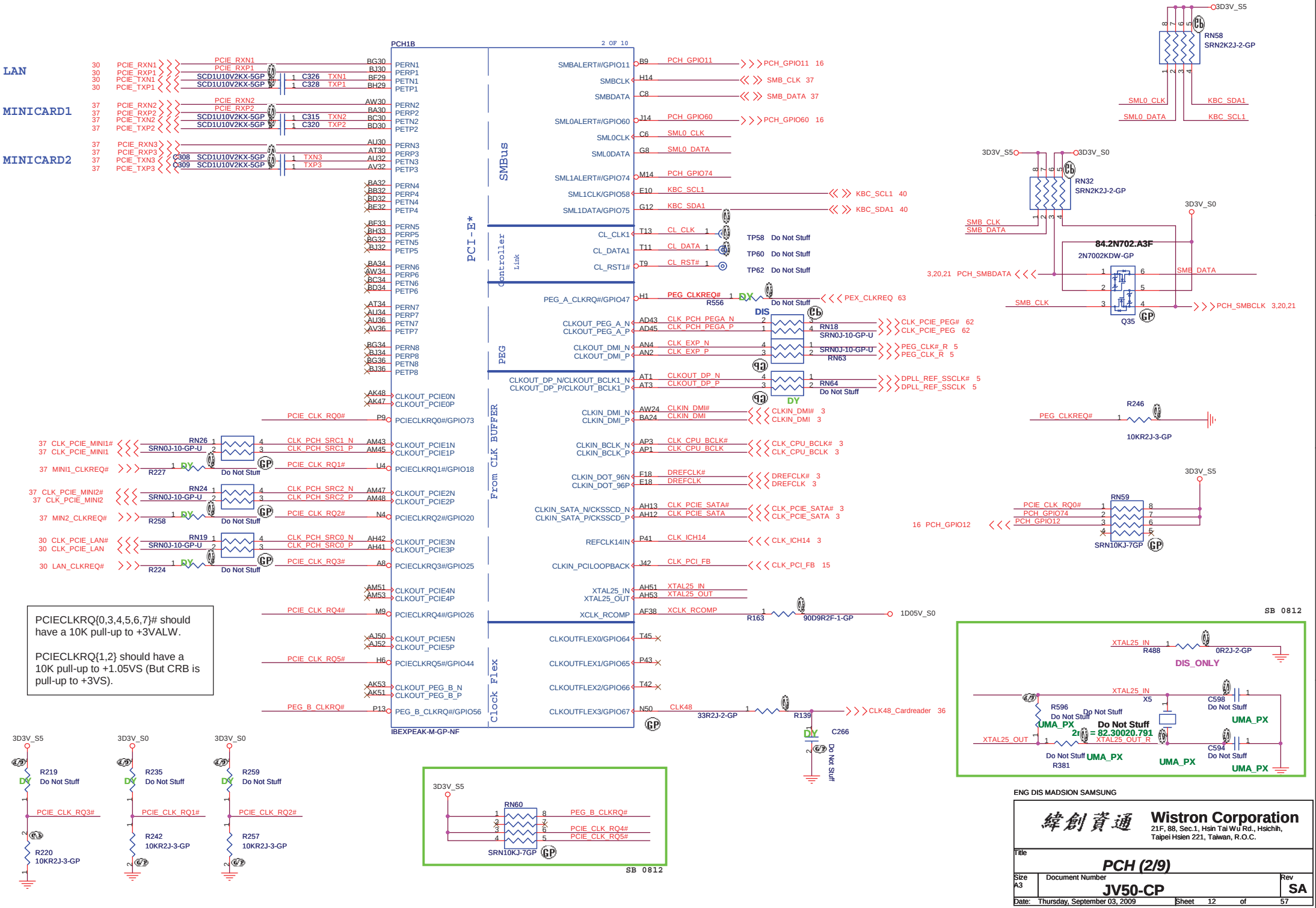
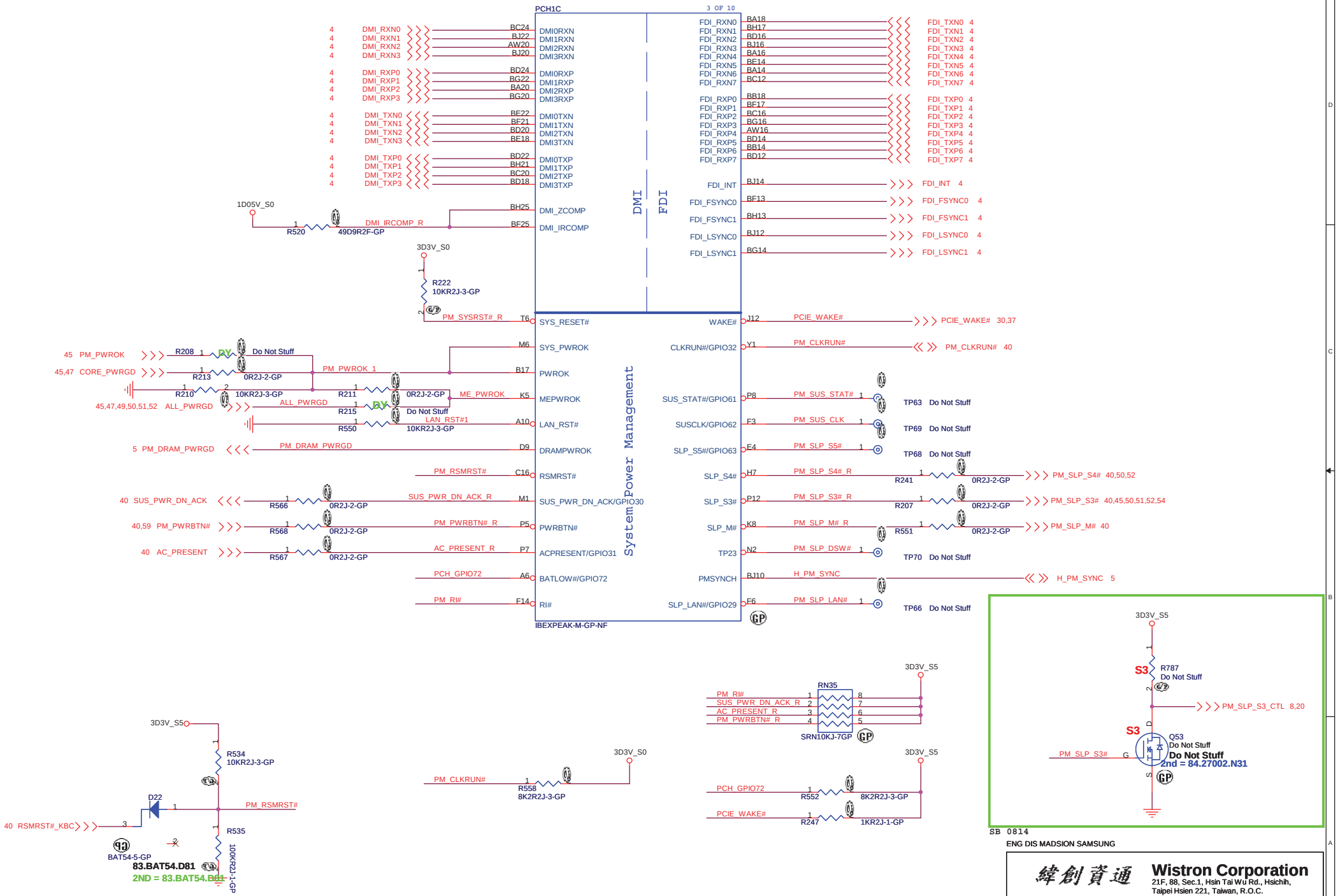

LAN
MINICARD1
MINICARD2
PCH1B
2 OF 10
PCI-E*
SMBus
Controller Link
PEG
From CLK BUFFER
Clock Flex
PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).
IBEXPEAK-M-GP-NF
SB 0812
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (2/9)
Size A3
Document Number
JV50-CP
Rev SA
Date: Thursday, September 03, 2009
Sheet 12 of 57


PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
DMI_ZCOMP
DMI_IRCOMP
R520 49D9R2F-GP
R222 10KR2J-3-GP
PM_SYSRST# R
SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_DN_ACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
WAKE#
CLKRUN#/GPIO32
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_M#
TP23
PMSYNCH
SLP_LAN#/GPIO29
R208 Do Not Stuff
R213 0R2J-2-GP
R210 10KR2J-3-GP
R211 0R2J-2-GP
R215 Do Not Stuff
R550 10KR2J-3-GP
R566 0R2J-2-GP
R568 0R2J-2-GP
R567 0R2J-2-GP
R241 0R2J-2-GP
R207 0R2J-2-GP
R551 0R2J-2-GP
TP63 Do Not Stuff
TP69 Do Not Stuff
TP68 Do Not Stuff
TP70 Do Not Stuff
TP66 Do Not Stuff
R534 10KR2J-3-GP
D22 BAT54-5-GP
R535 100KR2J-1-GP
83.BAT54.D81
2ND = 83.BAT54.D83
RN35 SRN10KJ-7GP
R558 8K2R2J-3-GP
R552 8K2R2J-3-GP
R247 1KR2J-1-GP
R787 Do Not Stuff
Q53 Do Not Stuff
Do Not Stuff
2nd = 84.27002.N31
SB 0814
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (3/9)
Size A3
Document Number
JV50-CP
Rev SA
Date: Thursday, September 03, 2009
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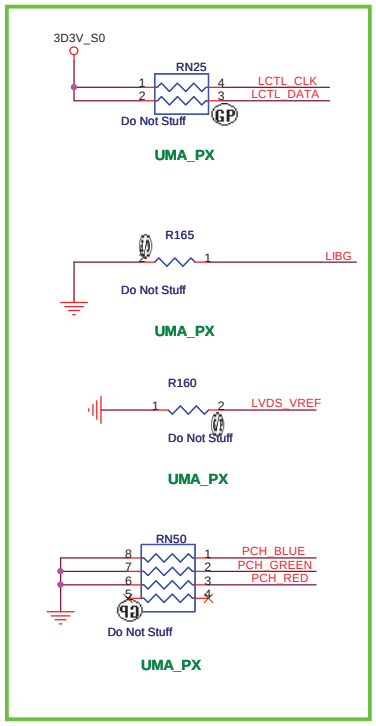
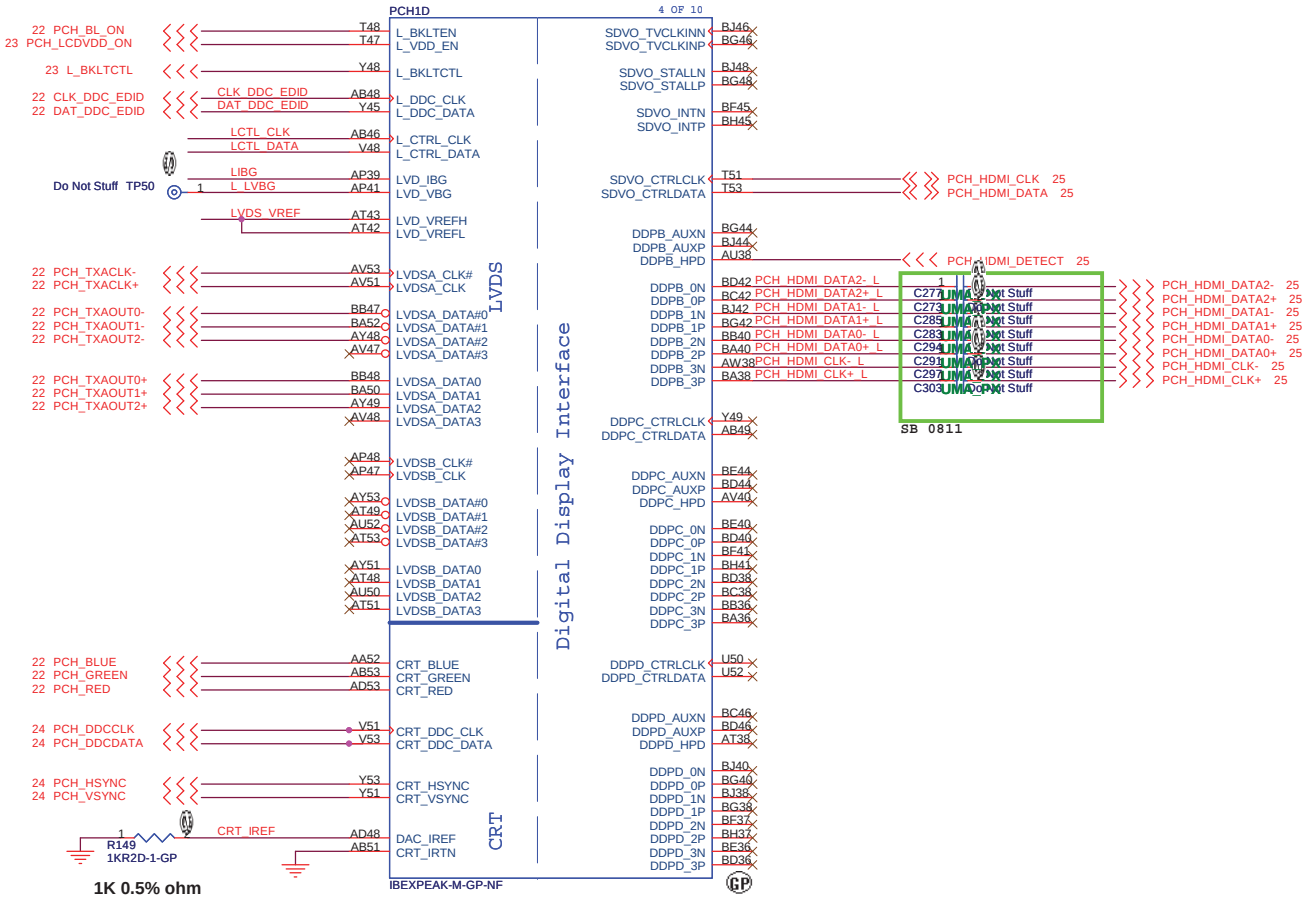


SB 0811



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (4/9)

Size	Document Number	Rev
A3	JV50-CP	SA

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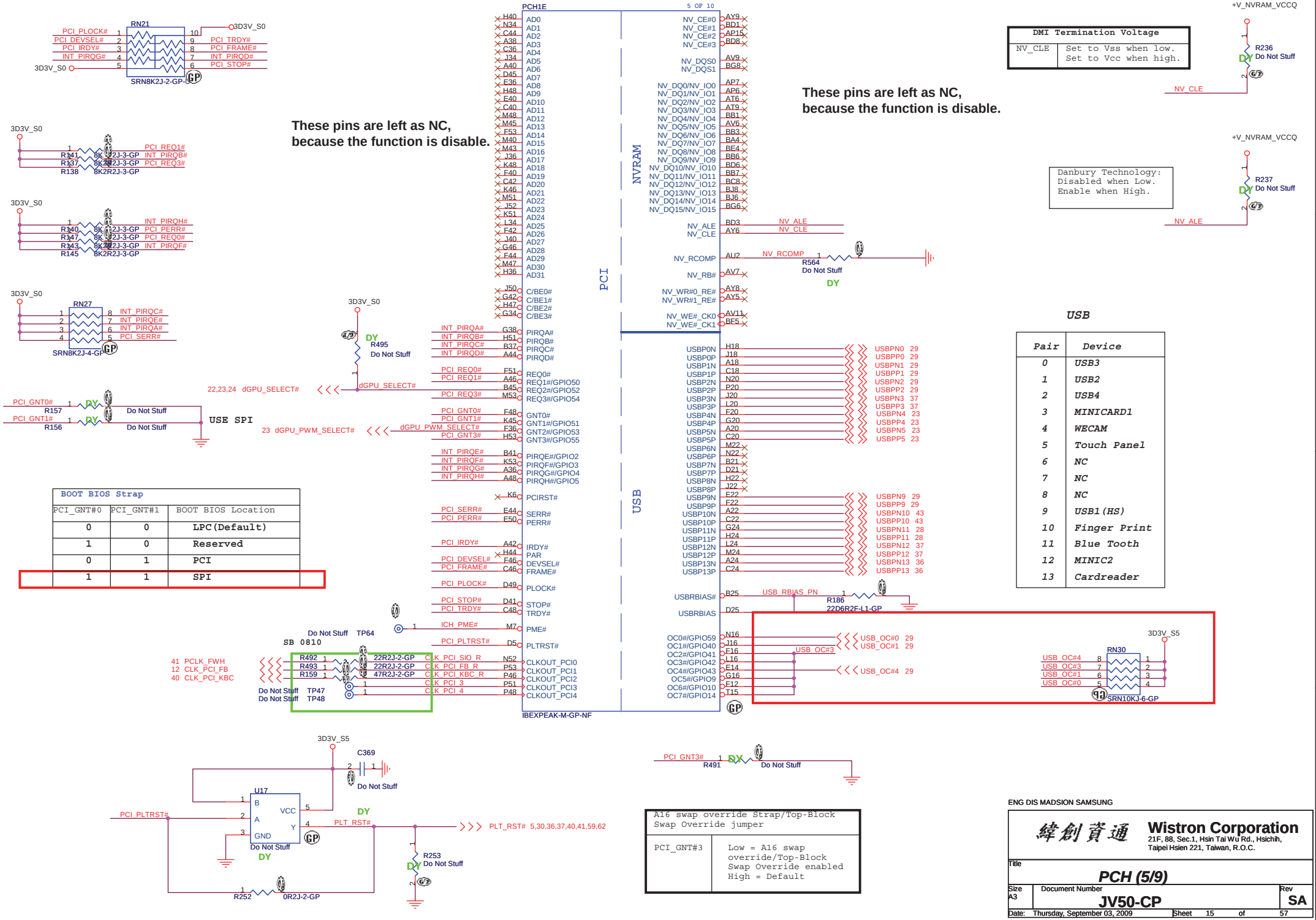
PCH1E
5 OF 10
PCI
NVRAM
USB
IBEXPEAK-M-GP-NF
These pins are left as NC, because the function is disable.
These pins are left as NC, because the function is disable.
RN21
SRN8K2J-2-GP-U
RN27
SRN8K2J-4-GP
R141 8K2R2J-3-GP
R137 8K2R2J-3-GP
R138 8K2R2J-3-GP
R140 8K2R2J-3-GP
R147 8K2R2J-3-GP
R143 8K2R2J-3-GP
R145 8K2R2J-3-GP
R495 Do Not Stuff
R157 Do Not Stuff
R156 Do Not Stuff
USE SPI
R564 Do Not Stuff
R236 Do Not Stuff
R237 Do Not Stuff
R186 22D6R2F-L1-GP
R491 Do Not Stuff
R492 22R2J-2-GP
R493 22R2J-2-GP
R159 47R2J-2-GP
R252 0R2J-2-GP
R253 Do Not Stuff
C369 Do Not Stuff
U17
RN30
SRN10KJ-6-GP
SB 0810
Do Not Stuff TP64
Do Not Stuff TP47
Do Not Stuff TP48
Danbury Technology:
Disabled when Low.
Enable when High.
DMI Termination Voltage
NV_CLE | Set to Vss when low. Set to Vcc when high.
USB
Pair | Device
0 | USB3
1 | USB2
2 | USB4
3 | MINICARD1
4 | WECAM
5 | Touch Panel
6 | NC
7 | NC
8 | NC
9 | USB1(HS)
10 | Finger Print
11 | Blue Tooth
12 | MINIC2
13 | Cardreader
BOOT BIOS Strap
PCI_GNT#0 | PCI_GNT#1 | BOOT BIOS Location
0 | 0 | LPC(Default)
1 | 0 | Reserved
0 | 1 | PCI
1 | 1 | SPI
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 | Low = A16 swap override/Top-Block Swap Override enabled
High = Default
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (5/9)
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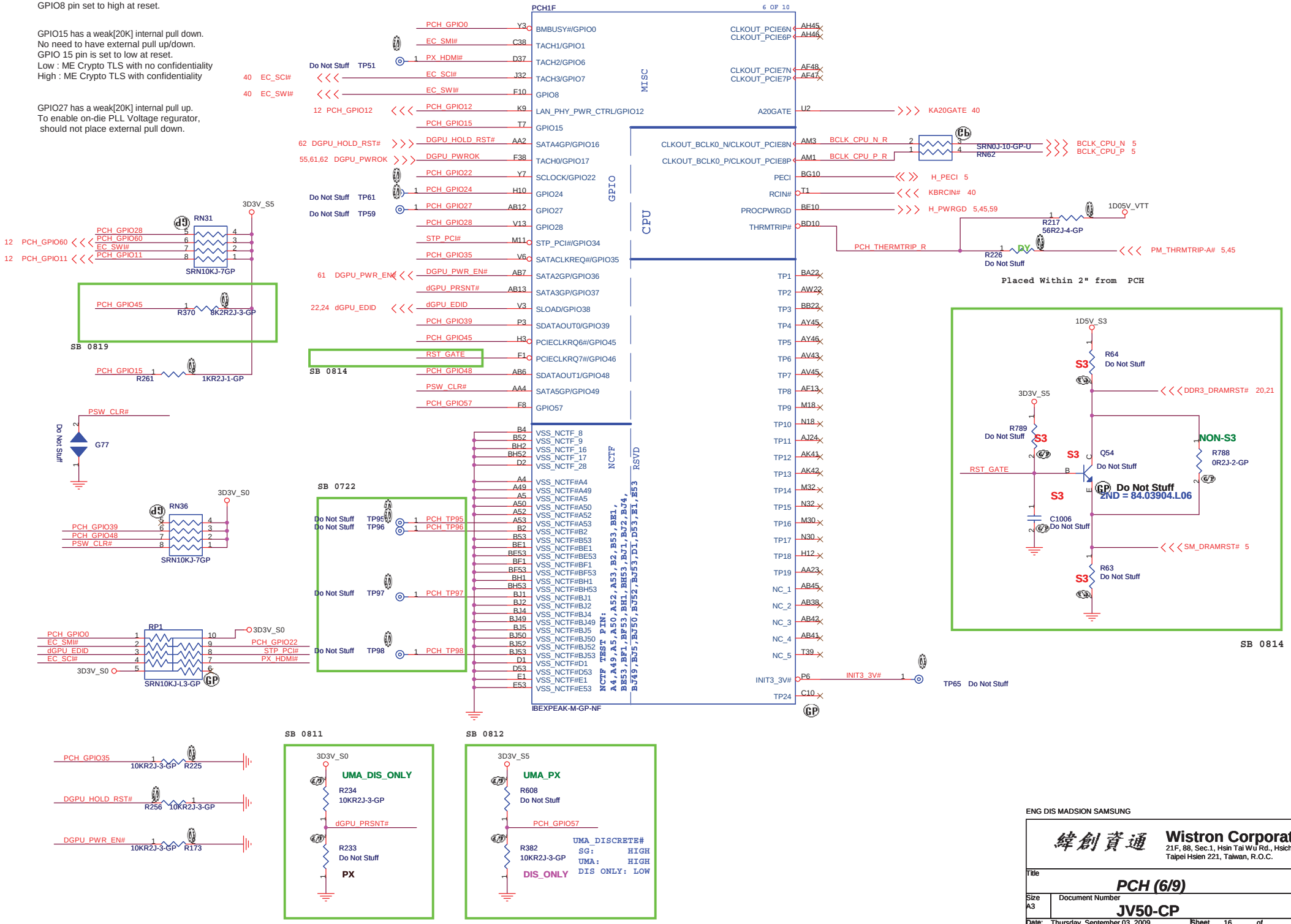
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.



ENG DIS MADSION SAMSUNG

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Title: PCH (6/9)

Size	Document Number	Rev
A3	JV50-CP	SA

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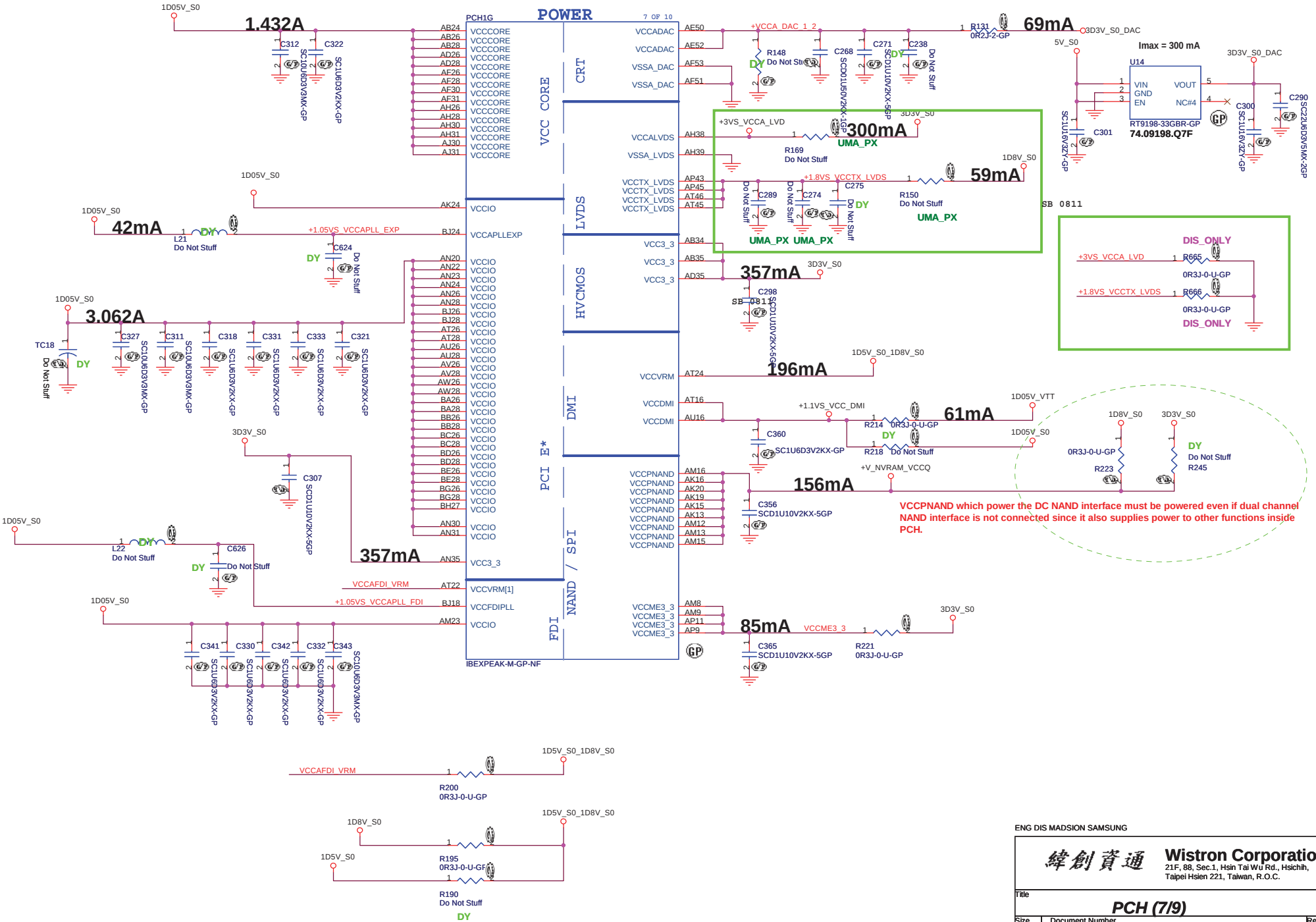
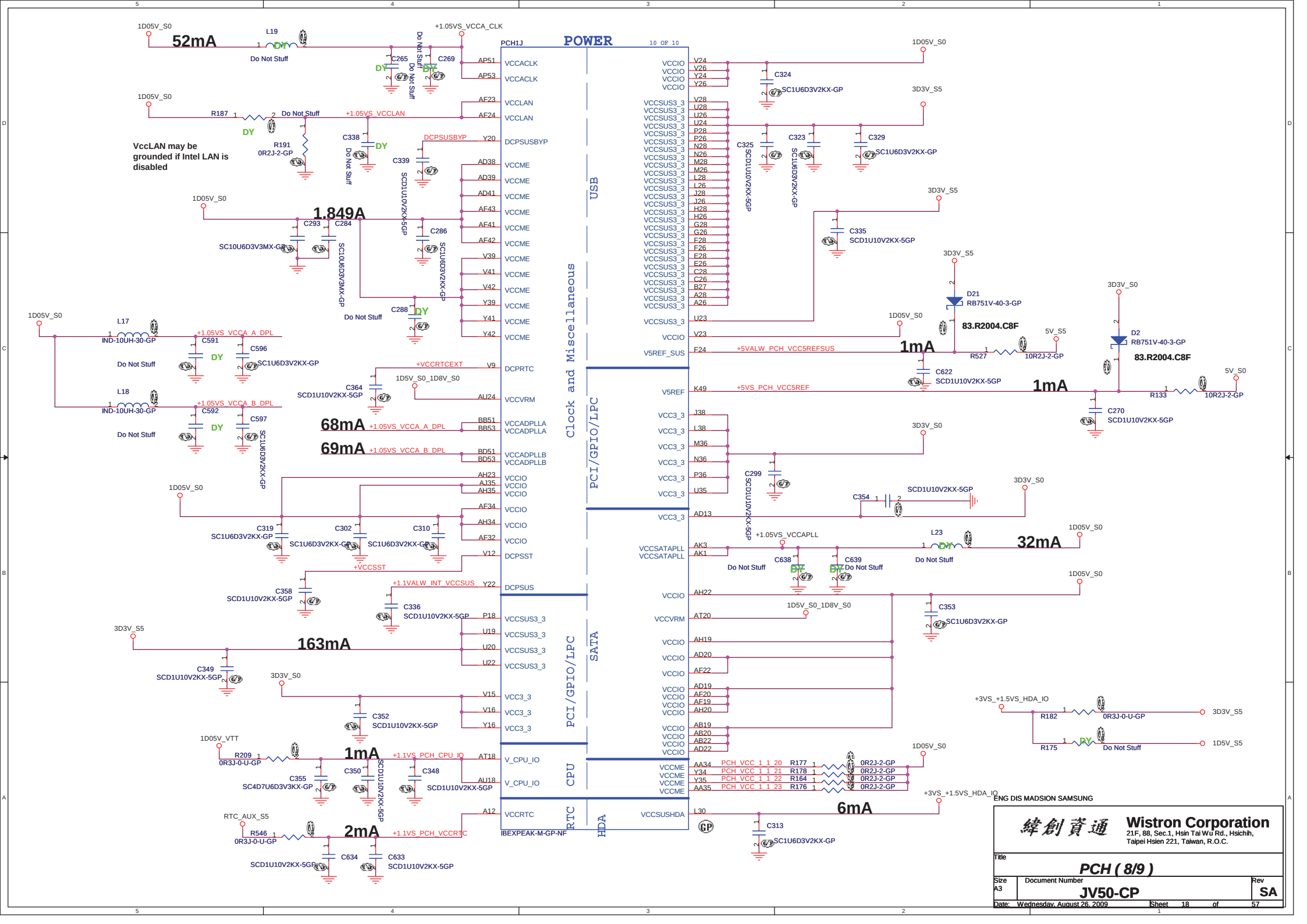


ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	PCH (7/9)	
Size A3	Document Number JV50-CP	Rev SA
Date: Wednesday, August 26, 2009	Sheet 17 of 57	


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
163mA
68mA
69mA
1mA
32mA
6mA
2mA
VccLAN may be grounded if Intel LAN is disabled
Do Not Stuff
DY
IBEXPEAK-M-GP-NF
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
Document Number
JV50-CP
Rev SA
Date: Wednesday, August 26, 2009
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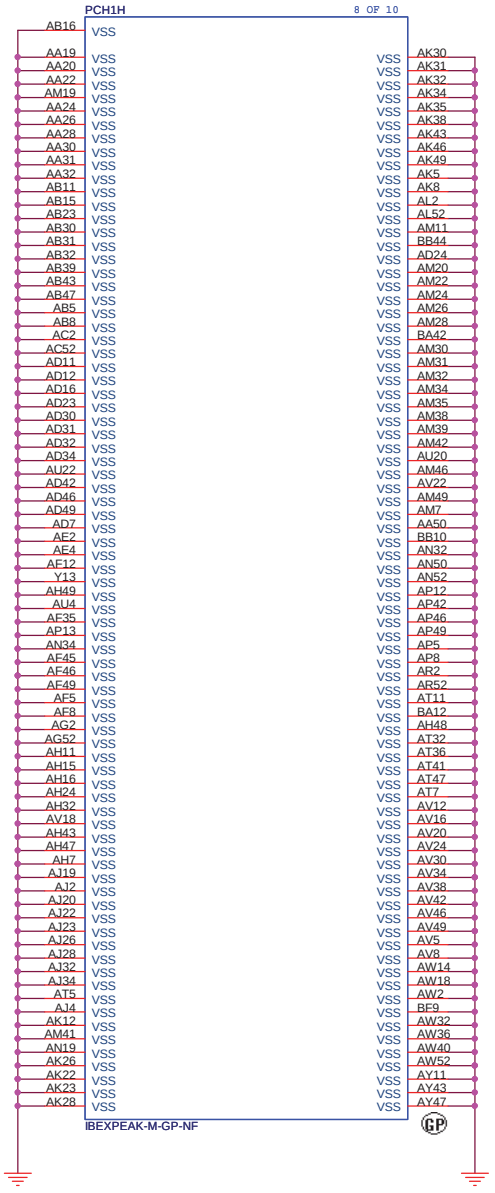
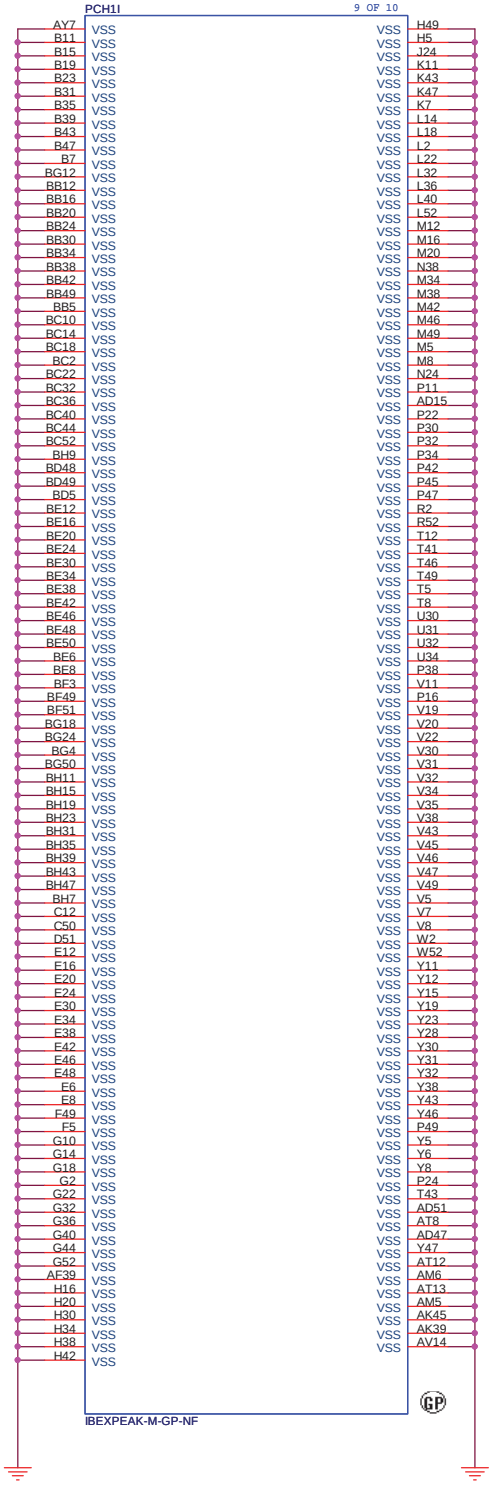




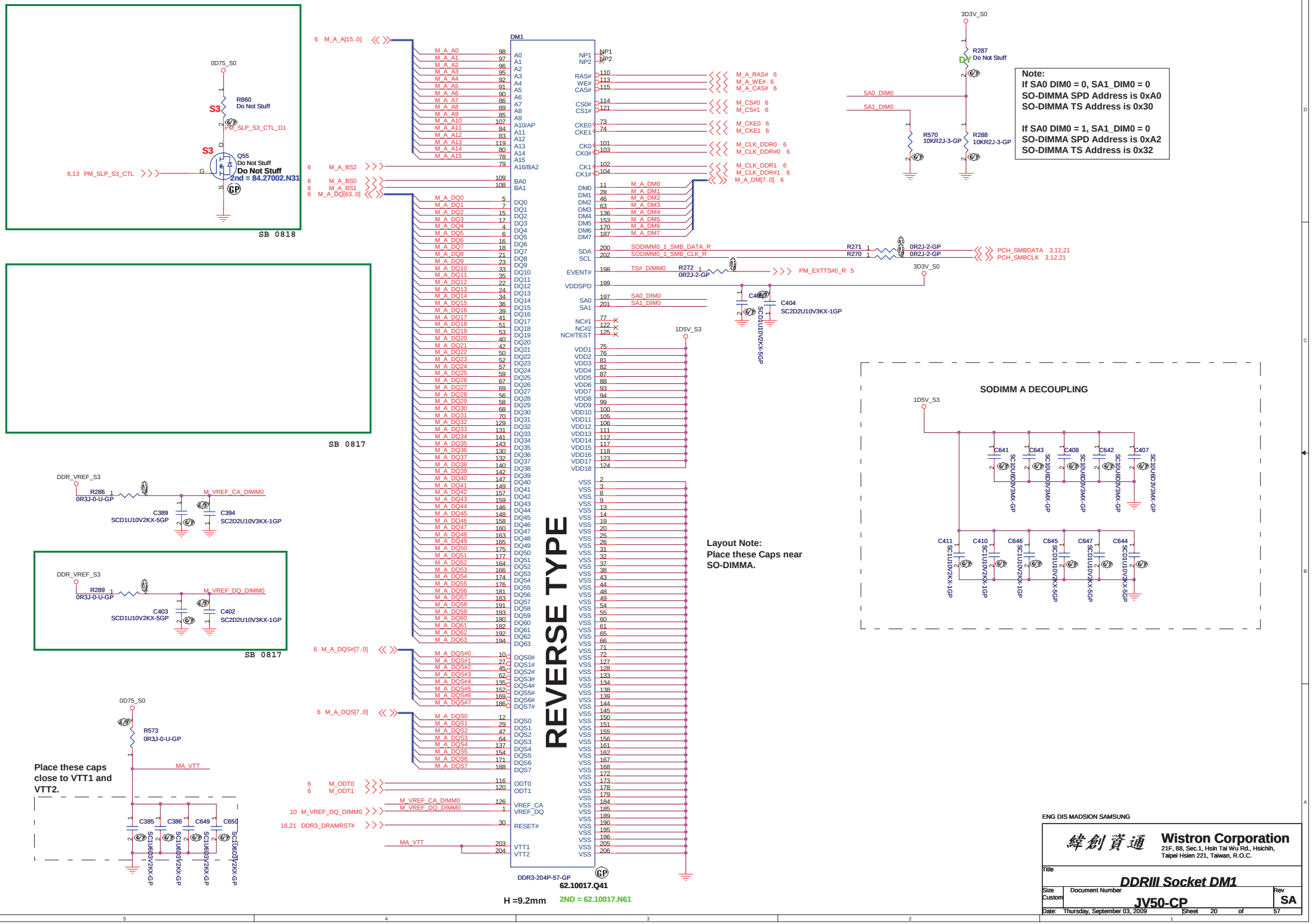
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (9/9)

Size	Document Number	Rev
A3	JV50-CP	SA

Date: Tuesday, August 18, 2009 Sheet 19 of 57



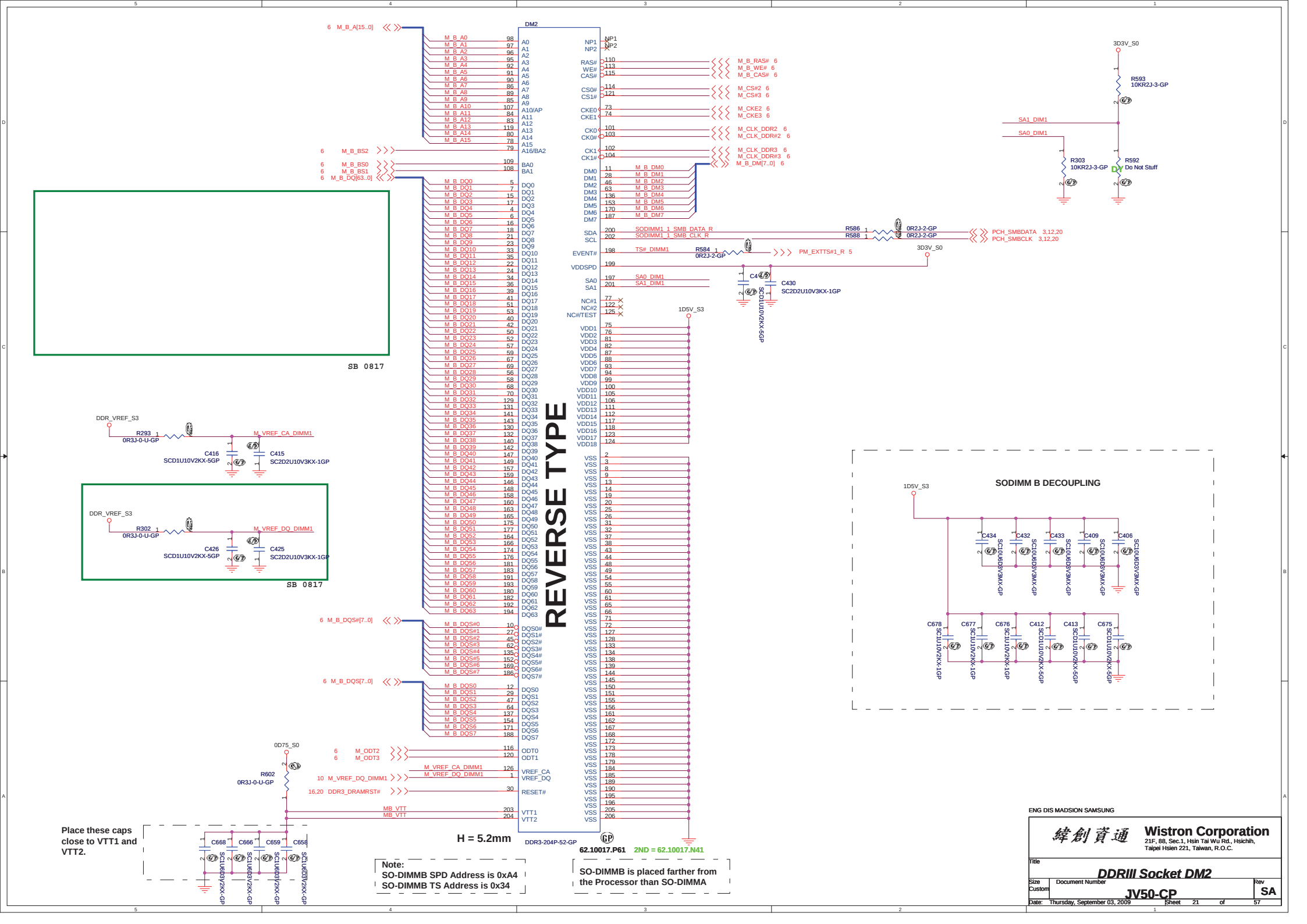
ENG DIS MADSION SAMSUNG

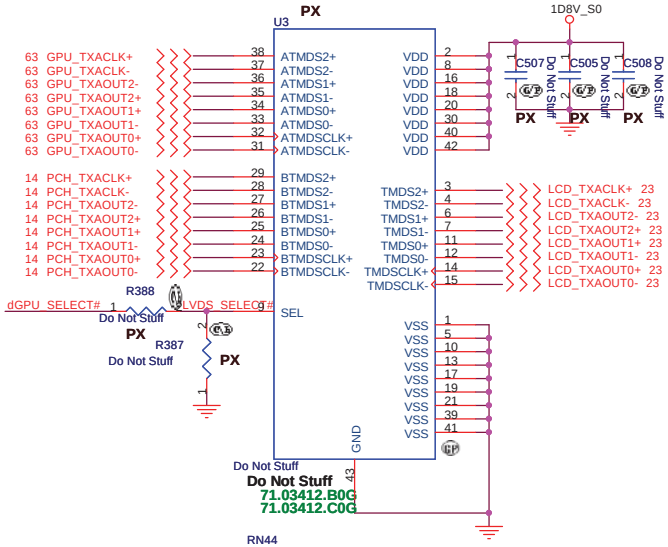
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

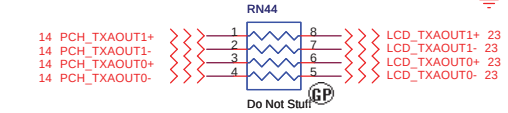
Title: DDRIII Socket DM1

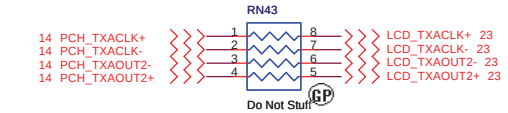
Size	Document Number	Rev
Custom	JV50-CP	SA

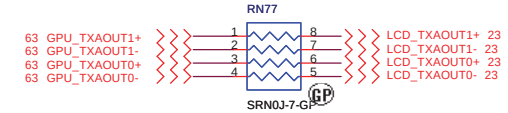
Date: Thursday, September 03, 2009 Sheet 20 of 57

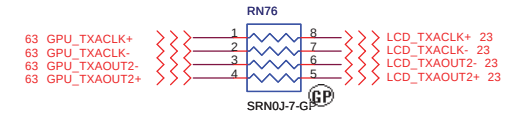

DM2
REVERSE TYPE
DDR3-204P-52-GP
62.10017.P61
2ND = 62.10017.N41
H = 5.2mm
SB 0817
SB 0817
SODIMM B DECOUPLING
Place these caps close to VTT1 and VTT2.
Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34
SO-DIMMB is placed farther from the Processor than SO-DIMMA
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM2
Size
Custom
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
Sheet 21 of 57

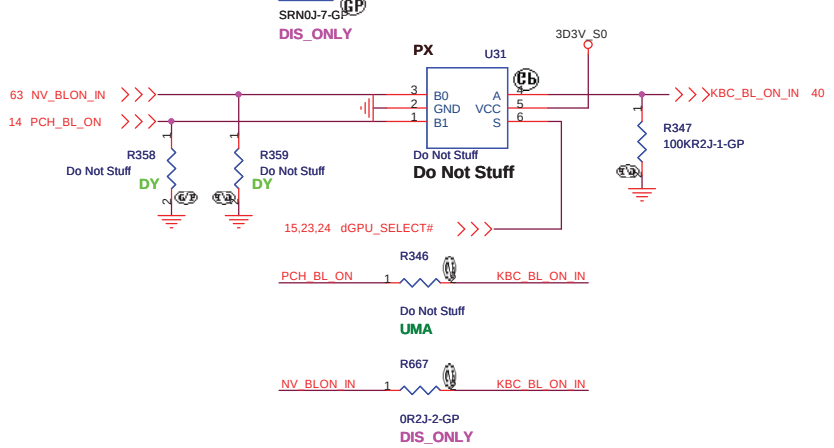






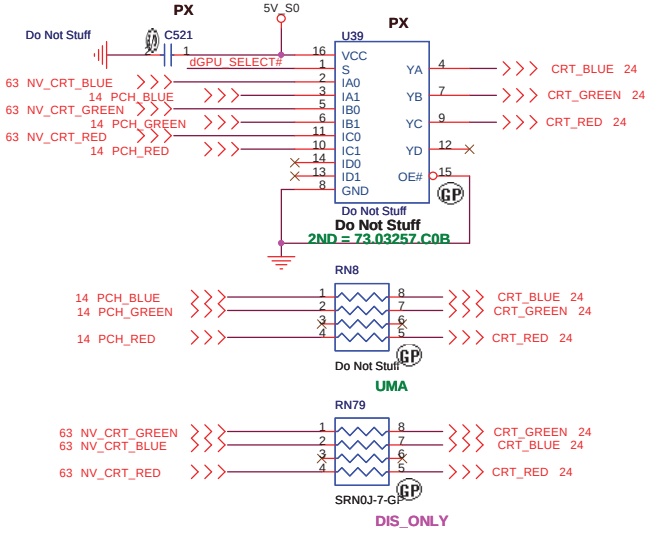


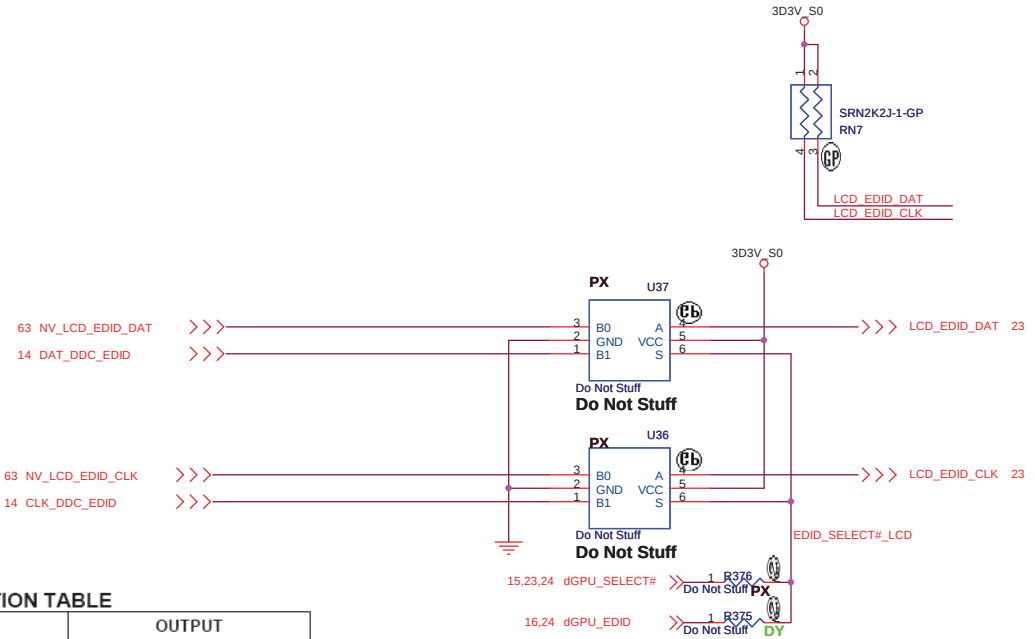




FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-





$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PX SWITCH**

Size: A3 | Document Number: **JV50-CP** | Rev: **SA**

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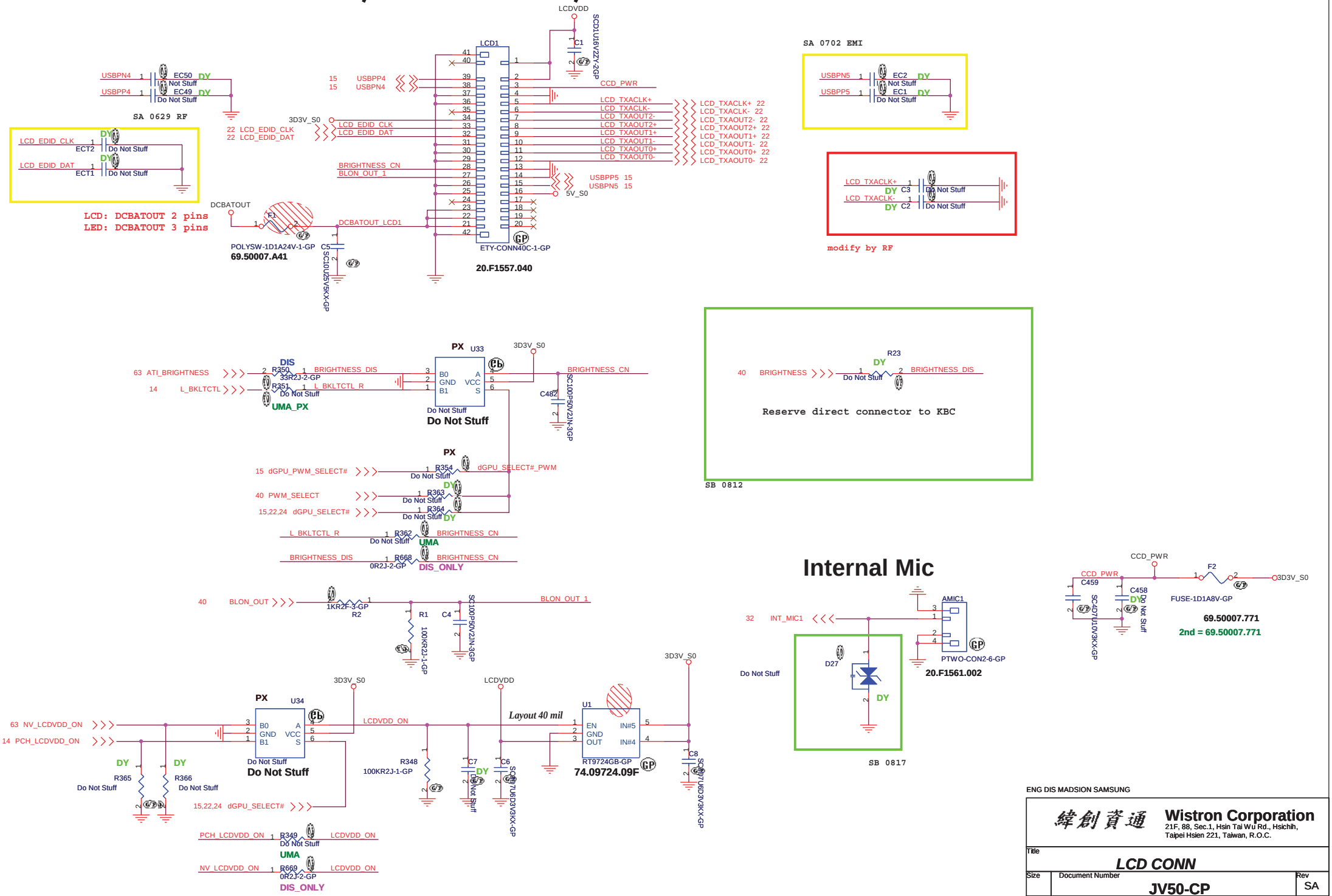
LCD/INVERTER/CCD CONN



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LCD CONN		
Size	Document Number: JV50-CP	Rev: SA
Date: Thursday, September 03, 2009	Sheet 23 of 61	

CRT I/F & CONNECTOR

Layout Note:
Place these resistors close to the CRT-out connector

22 CRT_RED
22 CRT_GREEN
22 CRT_BLUE

L9 Ferrite bead impedance: 10 ohm@100MHz
FCB1608CF-GP 68.00230.021
L7 FCB1608CF-GP 68.00230.021
L5 FCB1608CF-GP 68.00230.021

CRT_R
CRT_G
CRT_B

RN13 SRN150F-1-GP

C228 C217 C187 Do Not Stuff DY
C231 C221 C181 SC6D8P50V2DN-GP

Layout Note:
*** Must be a ground return path between this ground and the ground on the VGA connector.**
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

Hsync & Vsync level shift

L=>B0 -DIS
H=>B1 -UMA

15,22,23 dGPU_SELECT#
63,66 NV_CRT_HSYNC
63,66 NV_CRT_VSYNC
14 PCH_HSYNC
14 PCH_VSYNC

For DIS CRT
For UMA CRT

U6 DIS: 1OE# VCC 1A 2OE# 2Y 1Y GND 2A
SSLVC2G125DP-1GP 73.2G125.A07

U7 UMA_PX: 1OE# VCC 1A 2OE# 2Y 1Y GND 2A
Do Not Stuff Do Not Stuff

dGPU_SELECT

3D3V_S0
R28 10KR2J-3-GP
dGPU_SELECT
Q25 2N7002-11-GP
dGPU_SELECT# G
SC 0901

CRT_VSYNC1_1 R48 10R2J-2-GP CRT_VSYNC1_2 R47 0R3J-0-U-GP CRT_VSYNC1
CRT_HSYNC1_1 R51 10R2J-2-GP CRT_HSYNC1_2 R50 0R3J-0-U-GP CRT_HSYNC1

SB 0819

DDC_CLK & DATA level shift

5V_CRT_S0
5V_S0
3D3V_S0
3D3V_S0_DDC

FUSE-1D1A8V-GP 69.50007.771
F3
D16 RB551V-30-2GP 83.5R003.08F 500mA
5V_CRT_DDC
RN12 SRN10KJ-5-GP
RN49 SRN2K2J-1-GP
R52 10KR2J-3-GP

63 NV_CRT_DDCDATA
14 PCH_DDCDATA
63 NV_CRT_DDCCLK
14 PCH_DDCCLK

PX U42: B0 GND B1 VCC A S
PX U44: B0 GND B1 VCC A S
Do Not Stuff Do Not Stuff

Q11 2N7002KDW-GP 84.2N702.A3F
DDCDATA
DDCCLK
DAT_DDC1_5
CLK_DDC1_5

dGPU_SELECT#_DDC
15,22,23 dGPU_SELECT#
L=>B0 -DIS
H=>B1 -UMA
16,22 dGPU_EDID
R425 Do Not Stuff
R427 Do Not Stuff DY

RN11 14 PCH_DDCDATA 14 PCH_DDCCLK Do Not Stuff UMA
RN80 63 NV_CRT_DDCDATA 63 NV_CRT_DDCCLK SRN0J-6-GP DIS_ONLY

Do Not Stuff
C207 DY
C200
C172 CLK_DDC1_5
C133 DY
SC18P50V2JN-1-GP
SC18P50V2JN-1-GP
Do Not Stuff

DAT_DDC1_5
CRT_HSYNC1
CRT_VSYNC1

5V_CRT_S0
C563 SCD01U16V2KX-3GP

CRT1
CRT_R
CRT_G
CRT_B
CRT_IN#_R
VIDEO-15-142-GP
20.20813.015

40 CRT_DEC#
R61 470R2J-2-GP
C169 SC100P50V2JN-3GP
CRT_IN#_R
D20 DY
Do Not Stuff

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT CONN
Size: Document Number: JV50-CP Rev: SA
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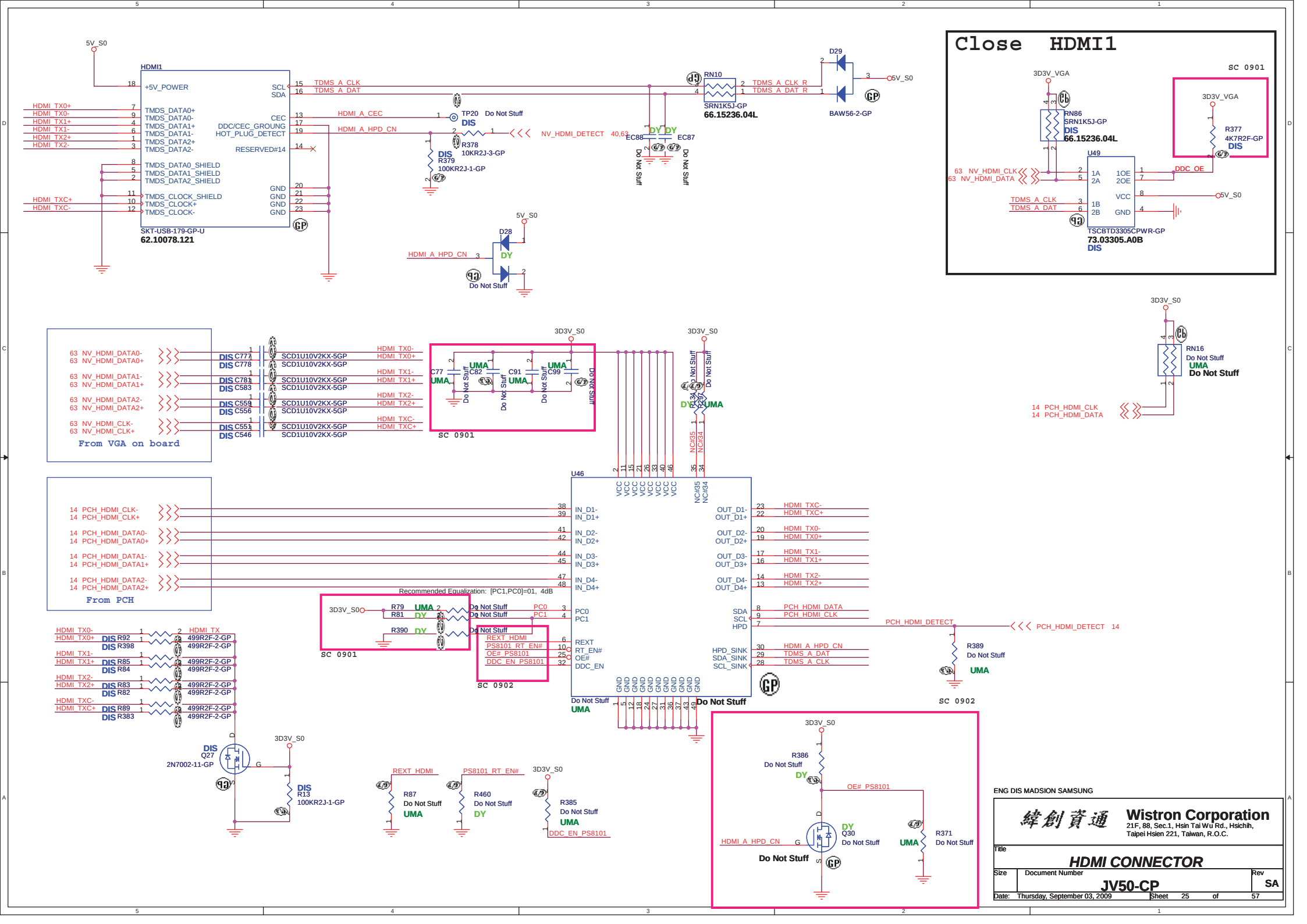
6 1 7 2 8 3 9 4 10 5


Close HDMI1
SC 0901
HDMI1
SKT-USB-179-GP-U
62.10078.121
+5V_POWER
TMDS_DATA0+
TMDS_DATA0-
TMDS_DATA1+
TMDS_DATA1-
TMDS_DATA2+
TMDS_DATA2-
TMDS_DATA0_SHIELD
TMDS_DATA1_SHIELD
TMDS_DATA2_SHIELD
TMDS_CLOCK_SHIELD
TMDS_CLOCK+
TMDS_CLOCK-
SCL
SDA
CEC
DDC/CEC_GROUNG
HOT_PLUG_DETECT
RESERVED#14
GND
TDMS_A_CLK
TDMS_A_DAT
HDMI_A_CEC
HDMI_A_HPD_CN
TP20 Do Not Stuff
DIS
R378 10KR2J-3-GP
R379 100KR2J-1-GP
NV_HDMI_DETECT 40,63
RN10
SRN1K5J-GP
66.15236.04L
TDMS_A_CLK_R
TDMS_A_DAT_R
D29
BAW56-2-GP
EC88
EC87
Do Not Stuff
3D3V_VGA
RN86
SRN1K5J-GP
DIS
66.15236.04L
R377
4K7R2F-GP
DIS
U49
TSCBTD3305CPWR-GP
73.03305.A0B
DIS
DDC_OE
63 NV_HDMI_CLK
63 NV_HDMI_DATA
TDMS_A_CLK
TDMS_A_DAT
5V_S0
D28
DY
Do Not Stuff
From VGA on board
SCD1U10V2KX-5GP
C777
C778
C781
C583
C559
C556
C551
C546
C77
C82
C91
C99
UMA
SC 0901
3D3V_S0
RN16
Do Not Stuff
UMA
14 PCH_HDMI_CLK
14 PCH_HDMI_DATA
From PCH
U46
IN_D1-
IN_D1+
IN_D2-
IN_D2+
IN_D3-
IN_D3+
IN_D4-
IN_D4+
OUT_D1-
OUT_D1+
OUT_D2-
OUT_D2+
OUT_D3-
OUT_D3+
OUT_D4-
OUT_D4+
SDA
SCL
HPD
HPD_SINK
SDA_SINK
SCL_SINK
PC0
PC1
REXT
RT_EN#
OE#
DDC_EN
REXT_HDMI
PS8101_RT_EN#
OE#_PS8101
DDC_EN_PS8101
Recommended Equalization: [PC1,PC0]=01, 4dB
R79
R81
R390
SC 0902
PCH_HDMI_DETECT
R389
Do Not Stuff
UMA
HDMI_TX
499R2F-2-GP
R92
R398
R85
R84
R83
R82
R89
R383
Q27
2N7002-11-GP
R13
100KR2J-1-GP
R87
R460
DY
R385
R386
R371
Q30
HDMI_A_HPD_CN
OE#_PS8101
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
HDMI CONNECTOR
Size
Document Number
JV50-CP
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Date: Thursday, September 03, 2009
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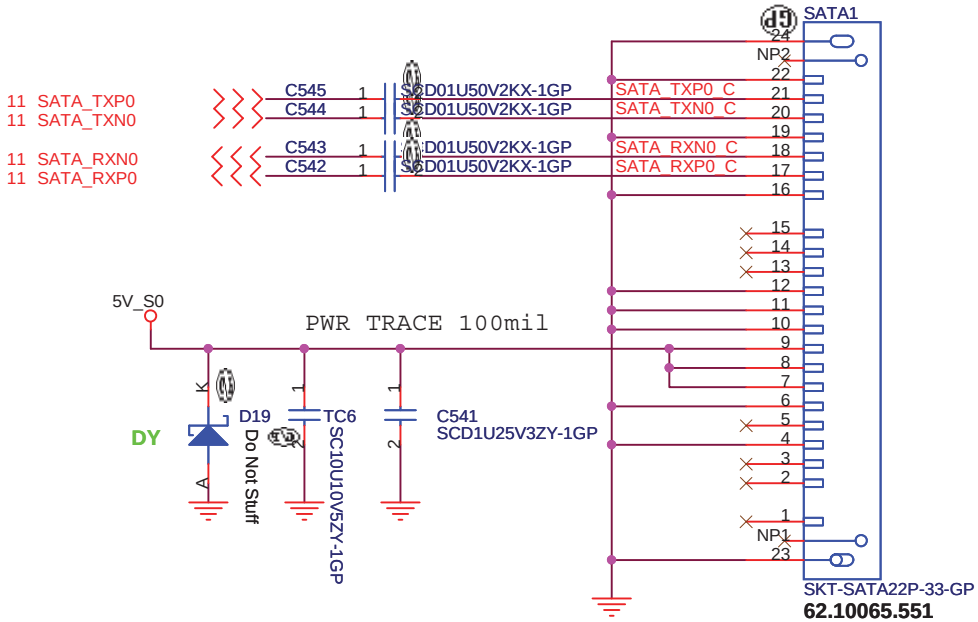
SATA Connector



ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **JV50-CP**	Rev SA
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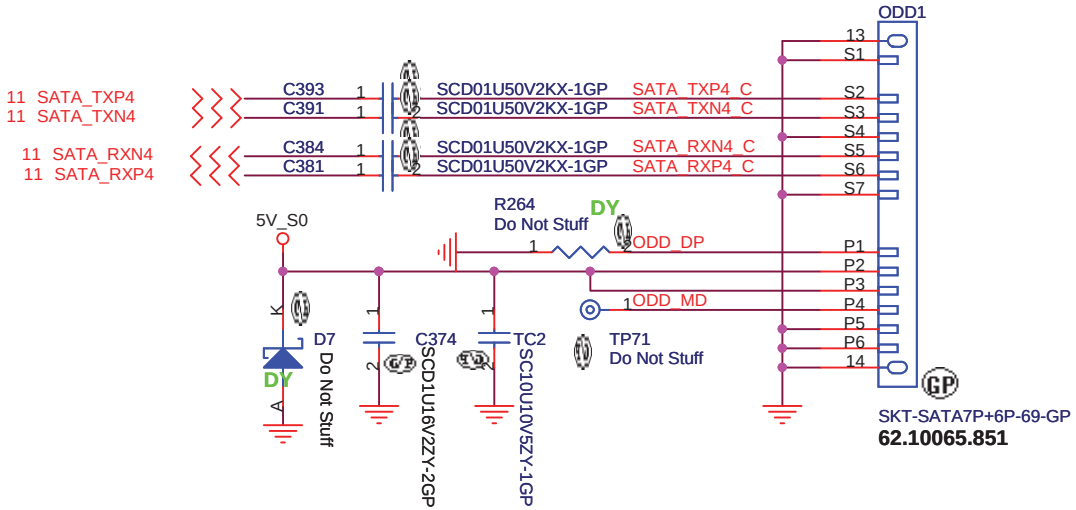
ODD Connector



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緯創資通 **Wistron Corporation**
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Title	***ODD***	
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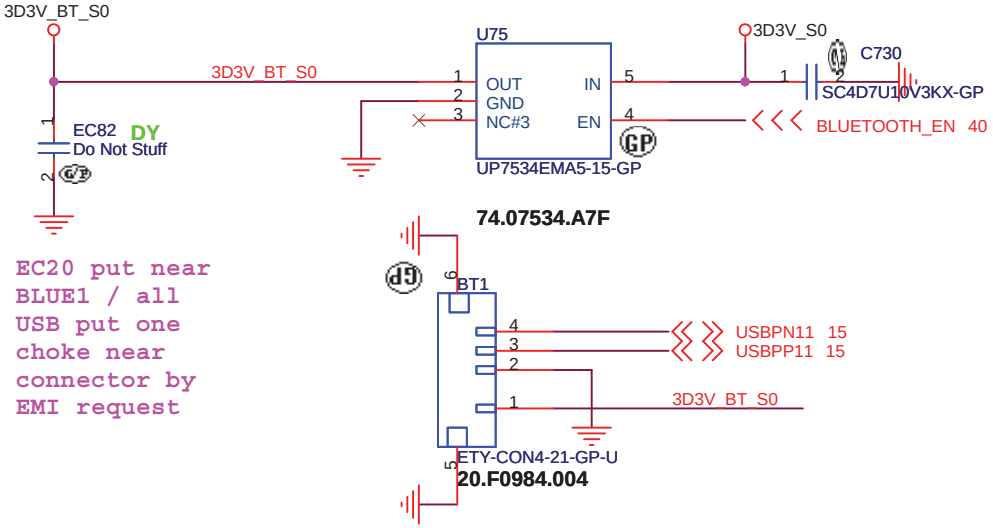
BLUETOOTH MODULE



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLUETOOTH

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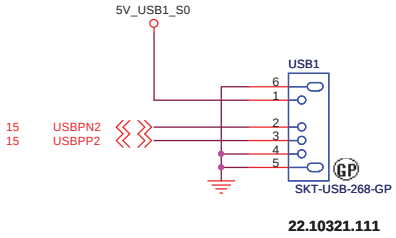

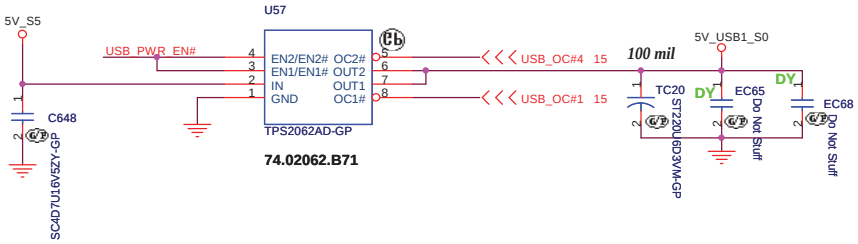

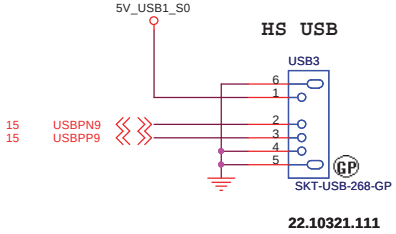

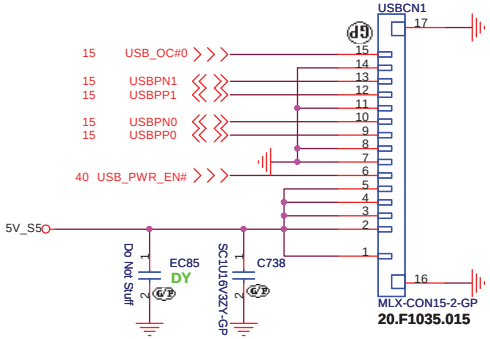

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB CONN	
Size	Document Number: JV50-CP	Rev: SA
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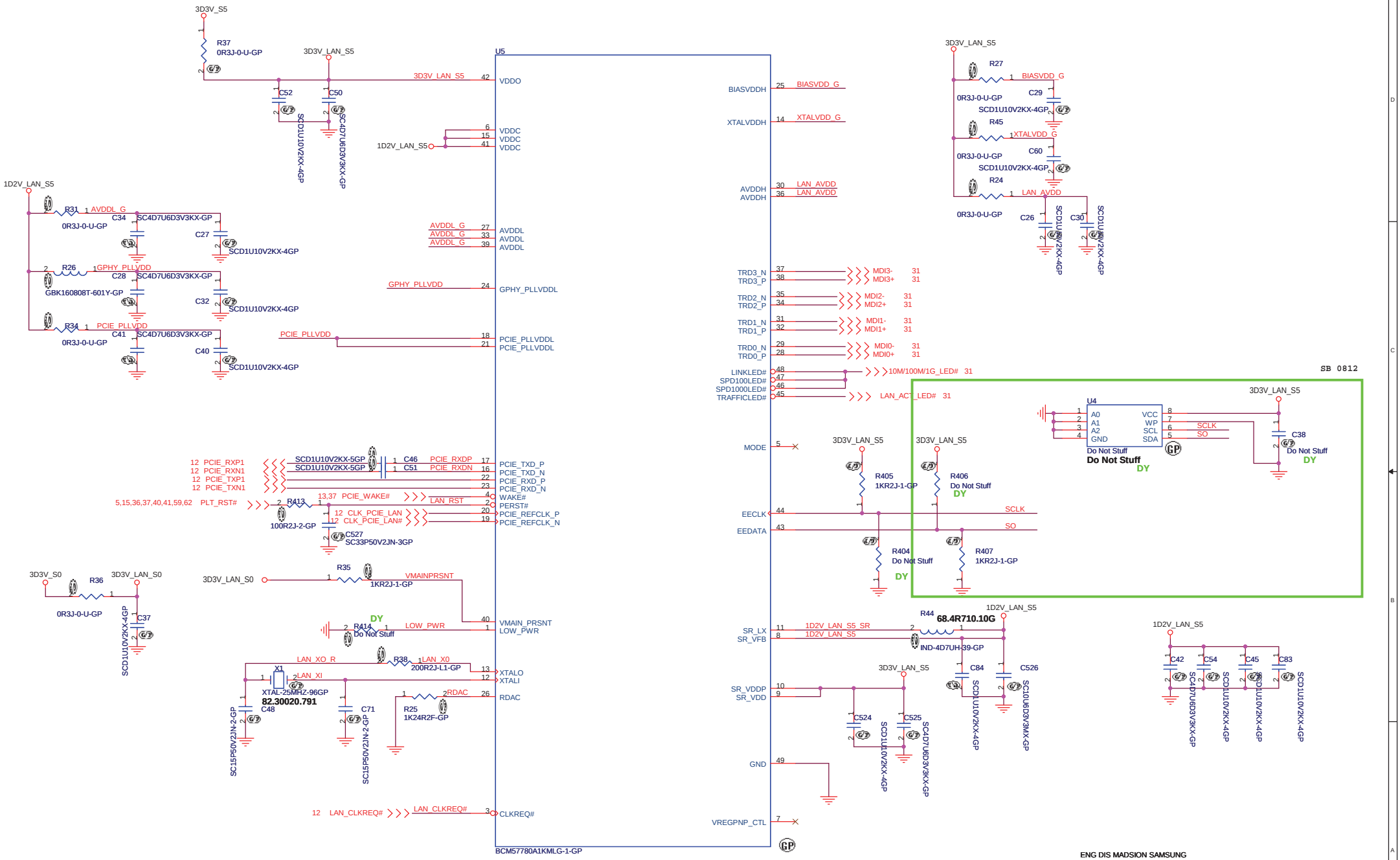
U5
BCM57780A1KMLG-1-GP
71.57780.M04
3D3V_S5
3D3V_LAN_S5
1D2V_LAN_S5
3D3V_S0
3D3V_LAN_S0
R37 0R3J-0-U-GP
R31 AVDDL_G
R26 GPHY_PLLVDD
R34 PCIE_PLLVDD
C34 SC4D7U6D3V3KX-GP
C27 SCD1U10V2KX-4GP
C28 SC4D7U6D3V3KX-GP
C32 SCD1U10V2KX-4GP
C41 SC4D7U6D3V3KX-GP
C40 SCD1U10V2KX-4GP
GBK160808T-601Y-GP
C52 SCD1U10V2KX-4GP
C50 SC4D7U6D3V3KX-GP
VDDO
VDDC
VDDC
VDDC
AVDDL
AVDDL
AVDDL
GPHY_PLLVDDL
PCIE_PLLVDDL
PCIE_PLLVDDL
BIASVDDH
XTALVDDH
AVDDH
AVDDH
LAN_AVDD
LAN_AVDD
BIASVDD_G
XTALVDD_G
R27 BIASVDD_G
R45 XTALVDD_G
R24 LAN_AVDD
C29 SCD1U10V2KX-4GP
C60 SCD1U10V2KX-4GP
C26 SCD1U10V2KX-4GP
C30 SCD1U10V2KX-4GP
0R3J-0-U-GP
TRD3_N
TRD3_P
TRD2_N
TRD2_P
TRD1_N
TRD1_P
TRD0_N
TRD0_P
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
LINKLED#
SPD100LED#
SPD1000LED#
TRAFFICLED#
10M/100M/1G_LED#
LAN_ACT_LED#
SB 0812
MODE
EECLK
EEDATA
SCLK
SO
R405 1KR2J-1-GP
R406 Do Not Stuff
R404 Do Not Stuff
R407 1KR2J-1-GP
U4
A0
A1
A2
GND
VCC
WP
SCL
SDA
C38 Do Not Stuff
Do Not Stuff
DY
PCIE_RXP1
PCIE_RXN1
PCIE_TXP1
PCIE_TXN1
SCD1U10V2KX-5GP
C46 PCIE_RXDP
C51 PCIE_RXDN
PCIE_TXD_P
PCIE_TXD_N
PCIE_RXD_P
PCIE_RXD_N
WAKE#
PERST#
PCIE_REFCLK_P
PCIE_REFCLK_N
PLT_RST#
R413 100R2J-2-GP
PCIE_WAKE#
LAN_RST
CLK_PCIE_LAN
CLK_PCIE_LAN#
C527 SC33P50V2JN-3GP
R35 1KR2J-1-GP
VMAINPRSNT
R414 Do Not Stuff
LOW_PWR
VMAIN_PRSNT
LOW_PWR
LAN_XO_R
LAN_XI
LAN_X0
R38 200R2J-L1-GP
X1 XTAL-25MHZ-96GP
82.30020.791
C48 SC15P50V2JN-2-GP
C71 SC15P50V2JN-2-GP
R25 1K24R2F-GP
XTALO
XTALI
RDAC
LAN_CLKREQ#
CLKREQ#
SR_LX
SR_VFB
SR_VDDP
SR_VDD
GND
VREGPNP_CTL
1D2V_LAN_S5_SR
R44 68.4R710.10G
IND-4D7UH-39-GP
C84 SCD1U10V2KX-4GP
C526 SC10U6D3V3MX-GP
C524 SCD1U10V2KX-4GP
C525 SC4D7U6D3V3KX-GP
C42 SC4D7U6D3V3KX-GP
C54 SCD1U10V2KX-4GP
C45 SCD1U10V2KX-4GP
C83 SCD1U10V2KX-4GP
C37 SCD1U10V2KX-4GP
R36 0R3J-0-U-GP
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM57780
Size Custom
Document Number
JV50-CP
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SA
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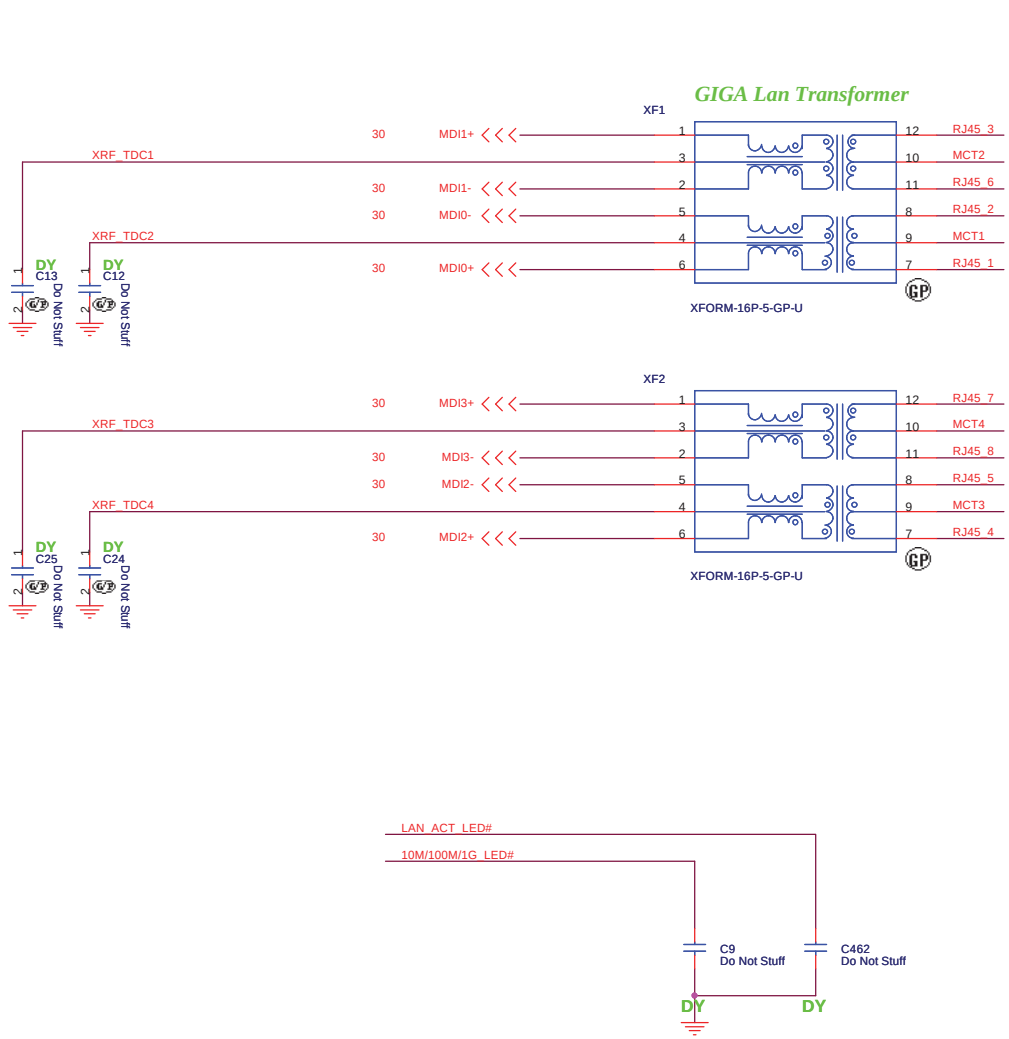
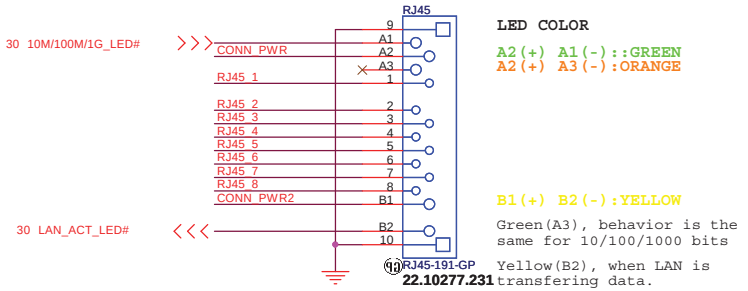
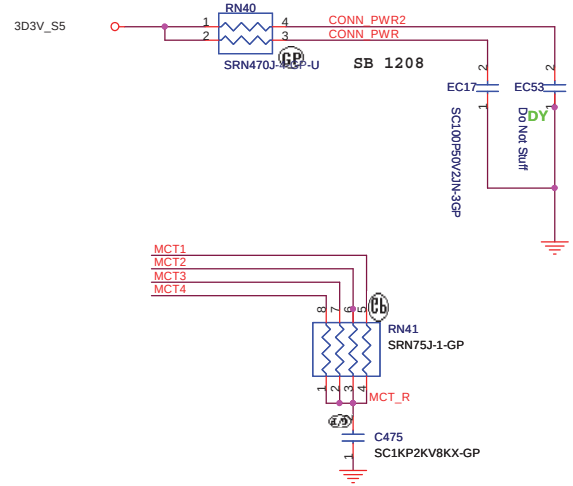
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

LAN Connector







ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	LAN CONN	
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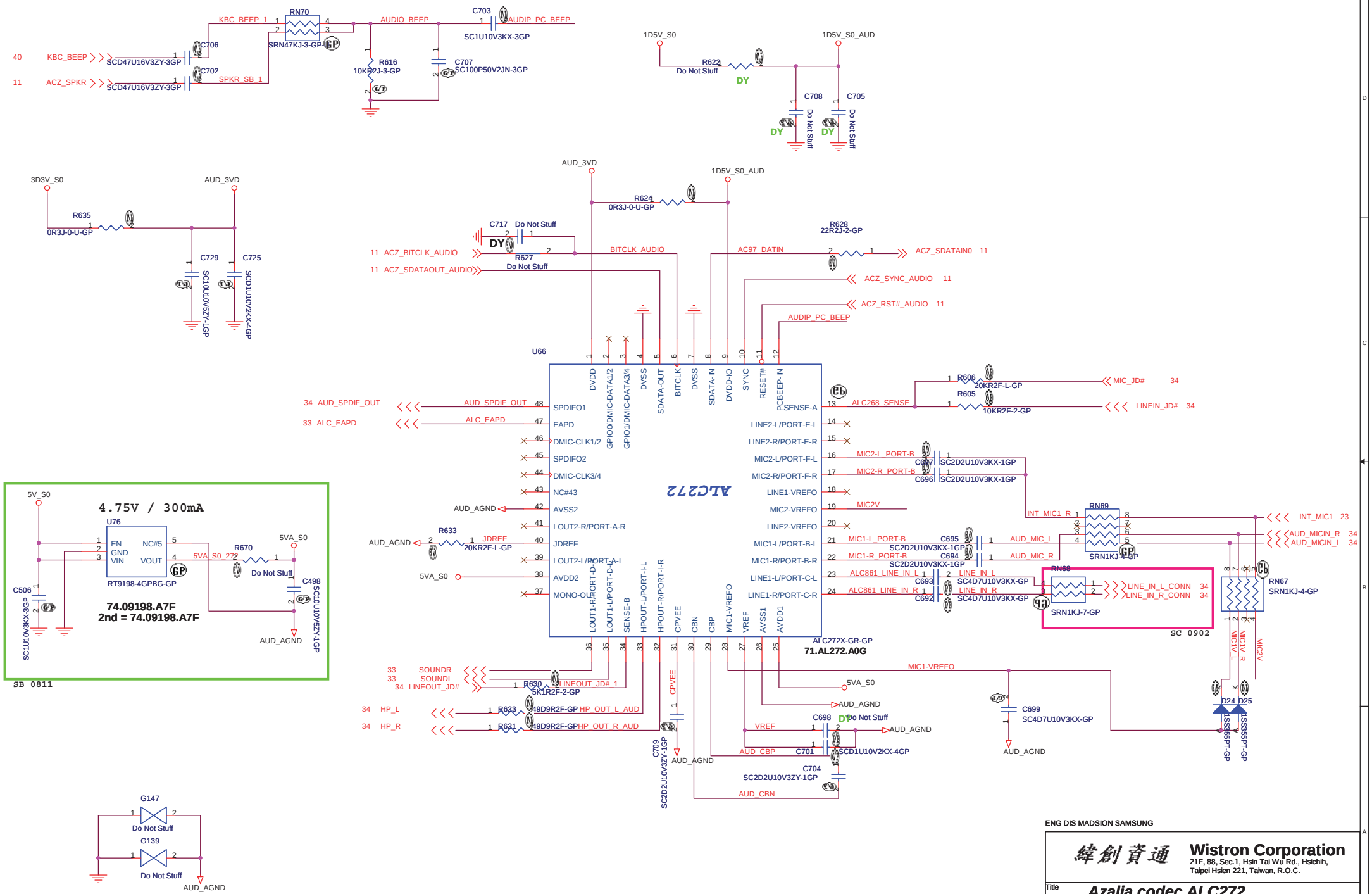
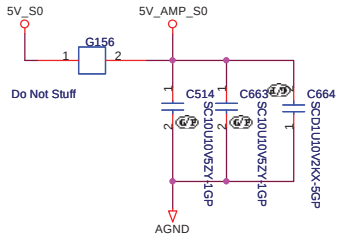
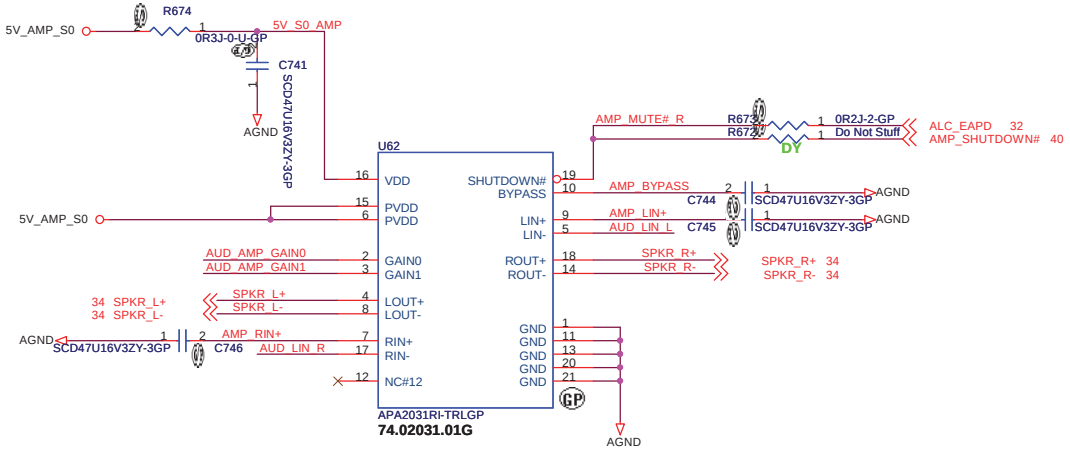


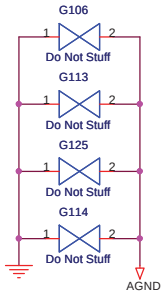
ENG DIS MADSION SAMSUNG

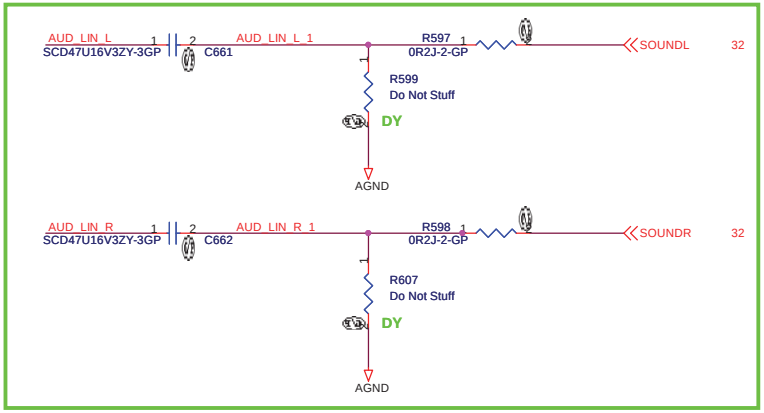
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Azalia codec ALC272**	
Size A3	Document Number **JV50-CP**	Rev **SA**
Date: Thursday, September 03, 2009	Sheet 32 of 61	



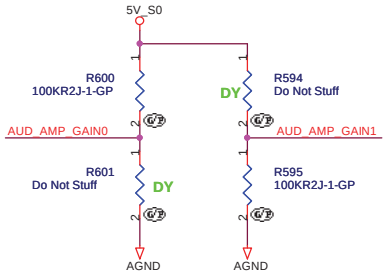






SB 0814

GAIN SETTING



GAIN0	GAIN1	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *AUDIO AMP*

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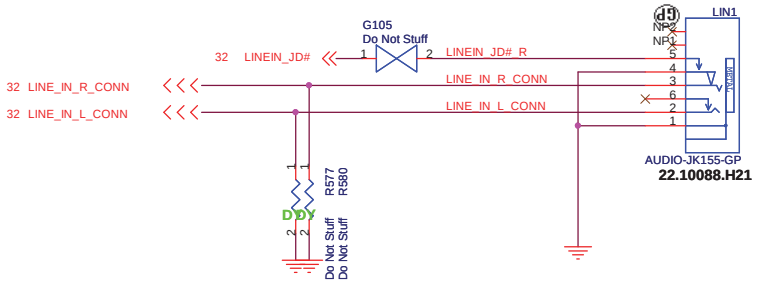
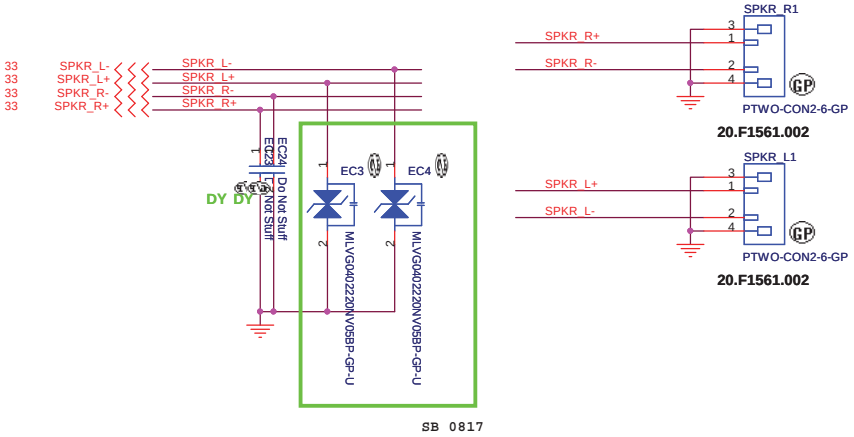
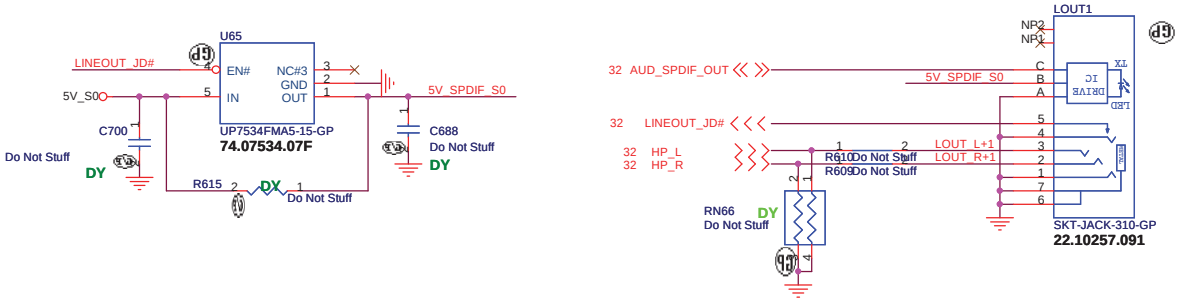
LINE IN

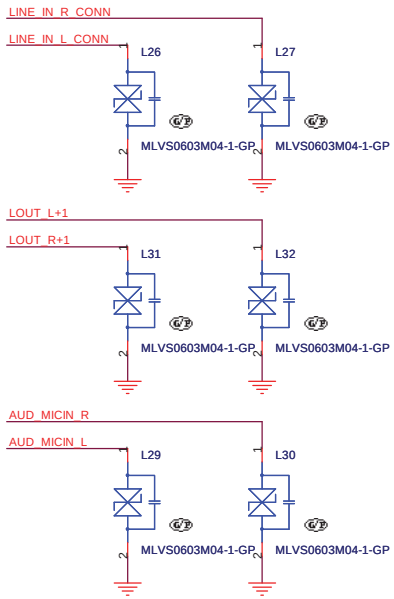


Internal Speaker



LINE OUT





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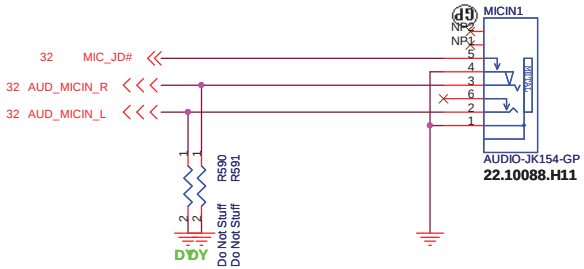

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*AUDIO jack*	
Size	Document Number: JV50-CP	Rev: SA
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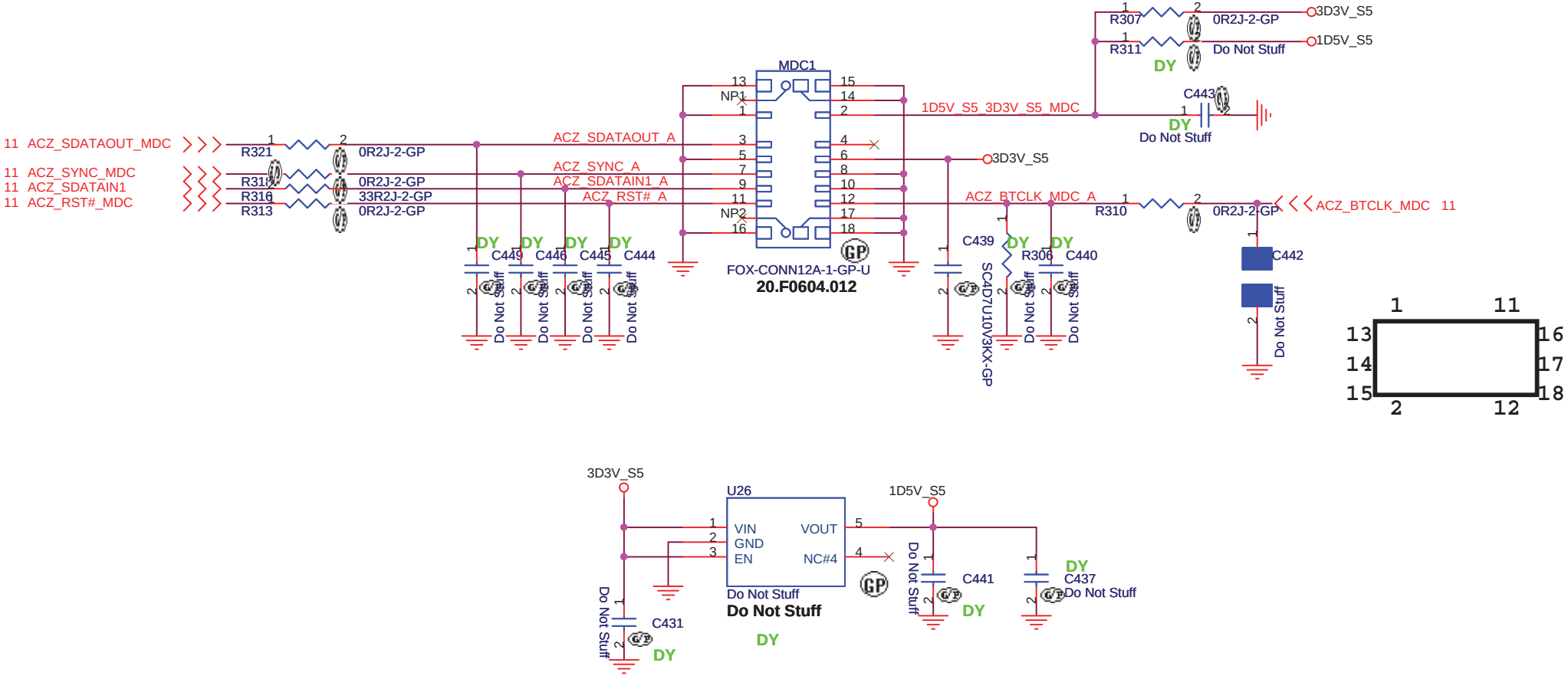
MDC 1.5 CONN



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	MDC	
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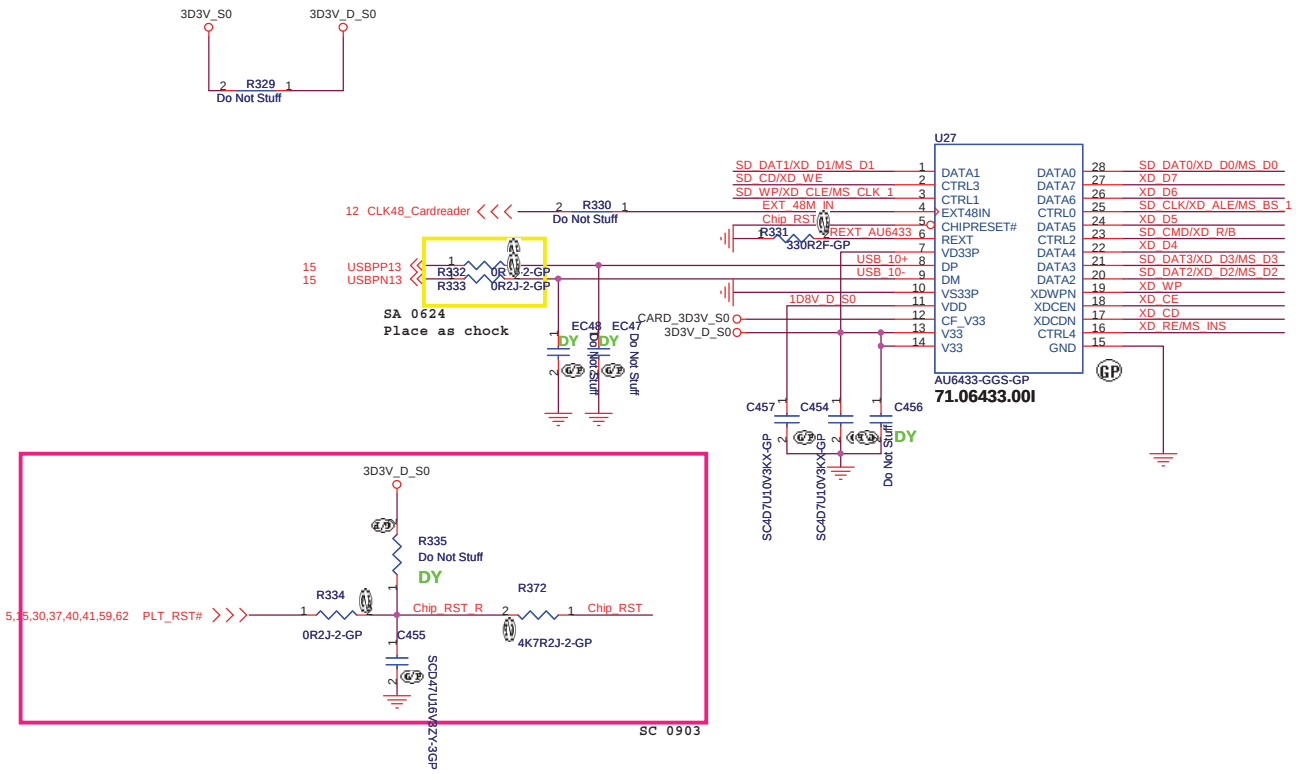
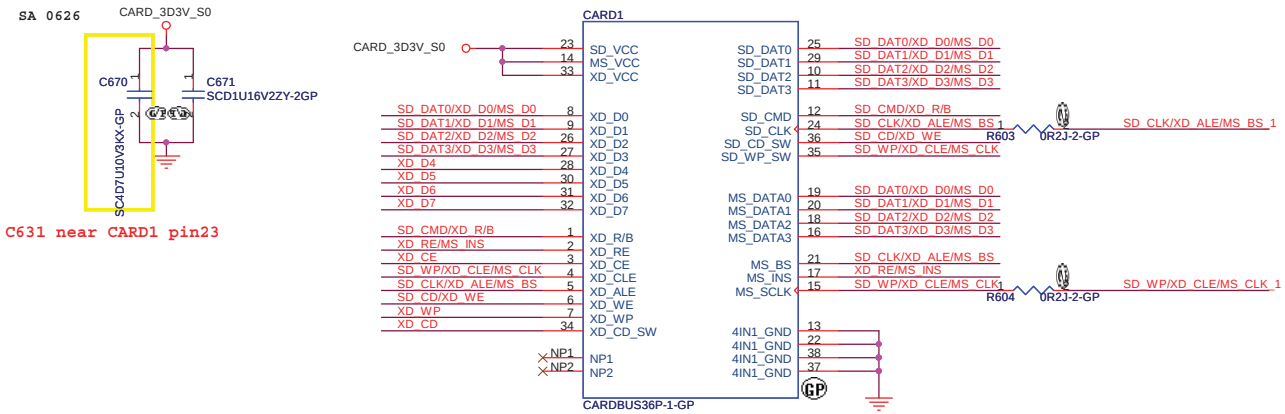


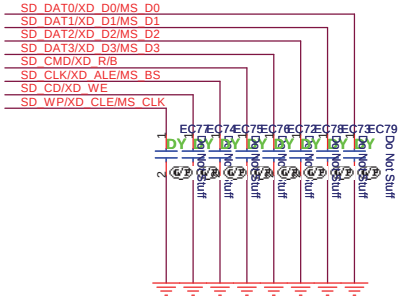
5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



2nd = 20.I0079.011

20.I0109.001

EMI capacitor



ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	Cardreader	
Size	Document Number: JV50-CP	Rev: SA
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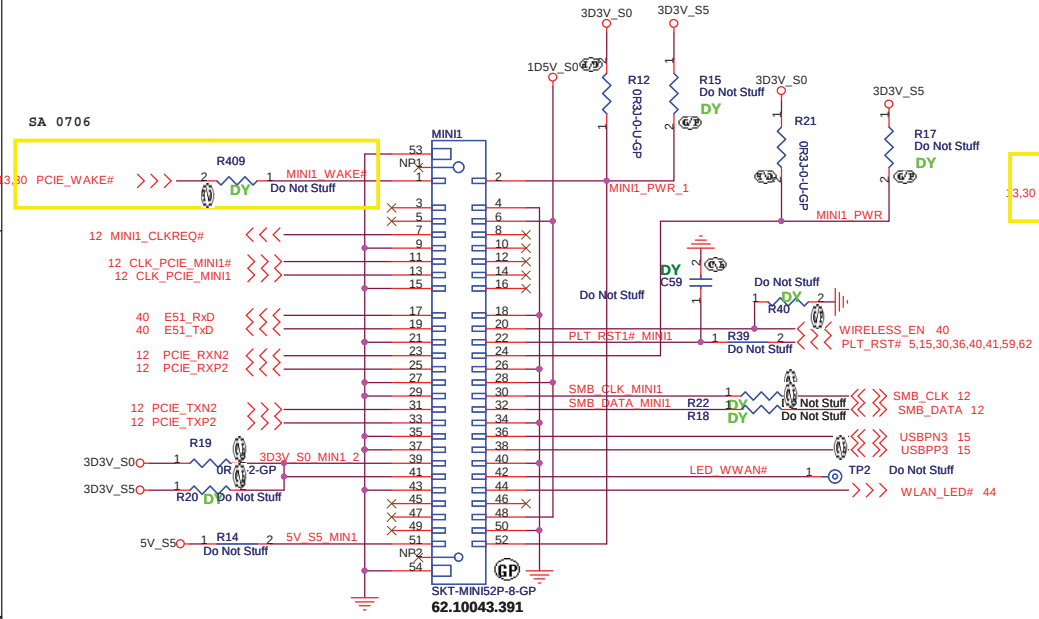
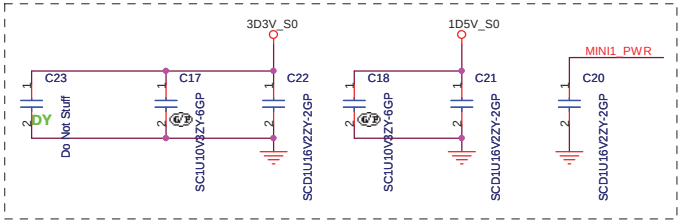
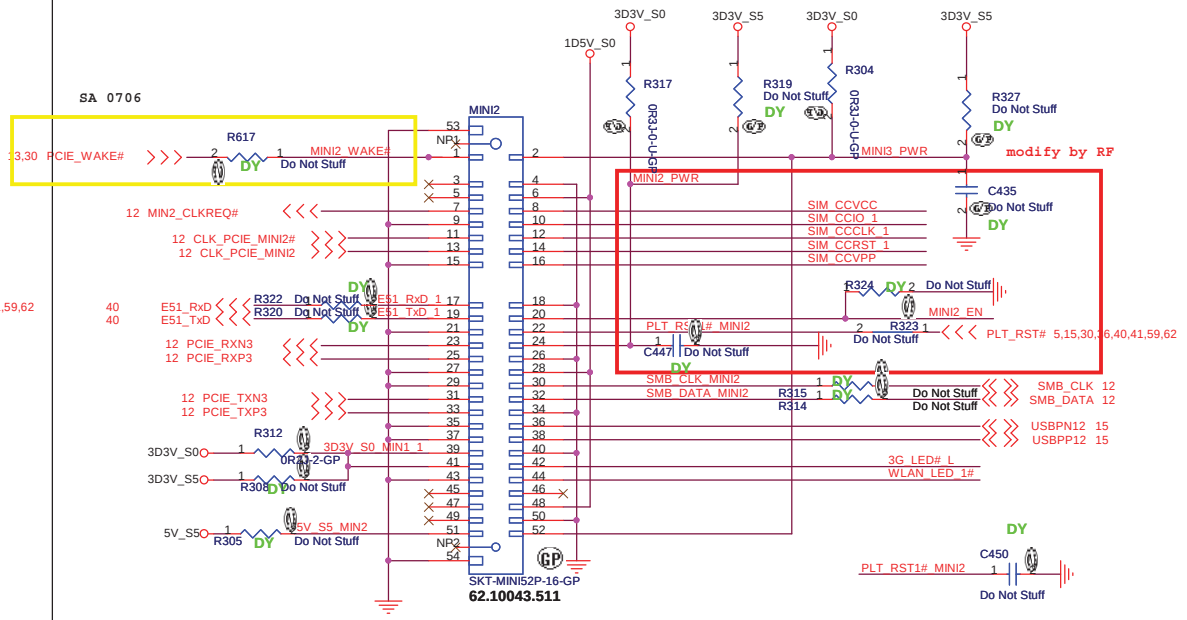
Mini Card Connector(WLAN)
Support debug-card

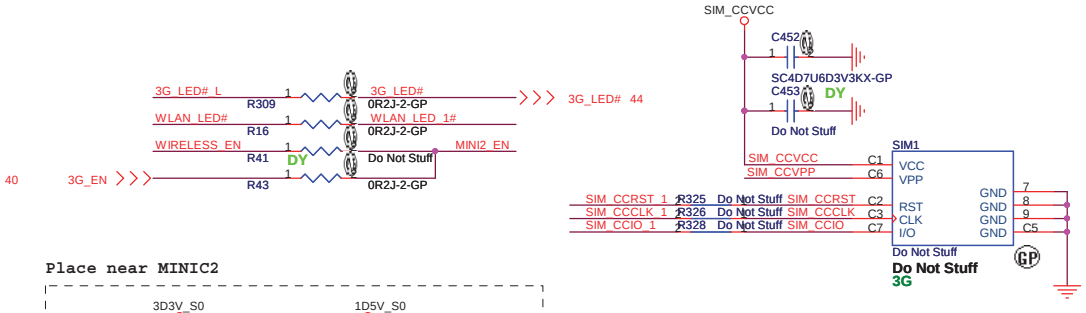


Place near MINI1

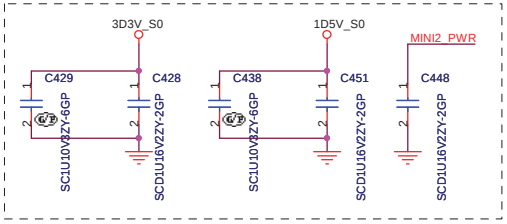


Mini Card Connector(Robson2 and 3G)





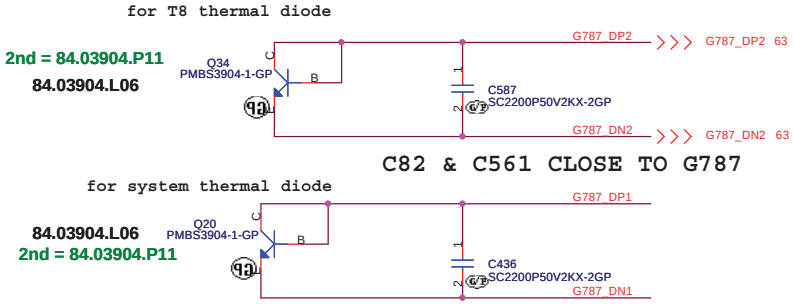
Place near MINIC2

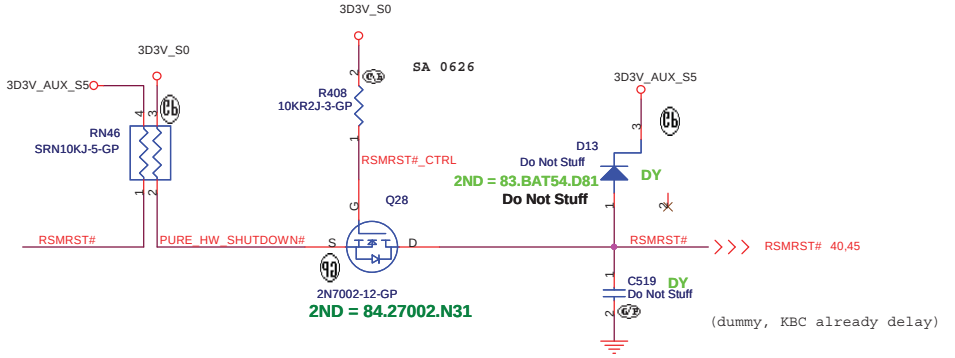


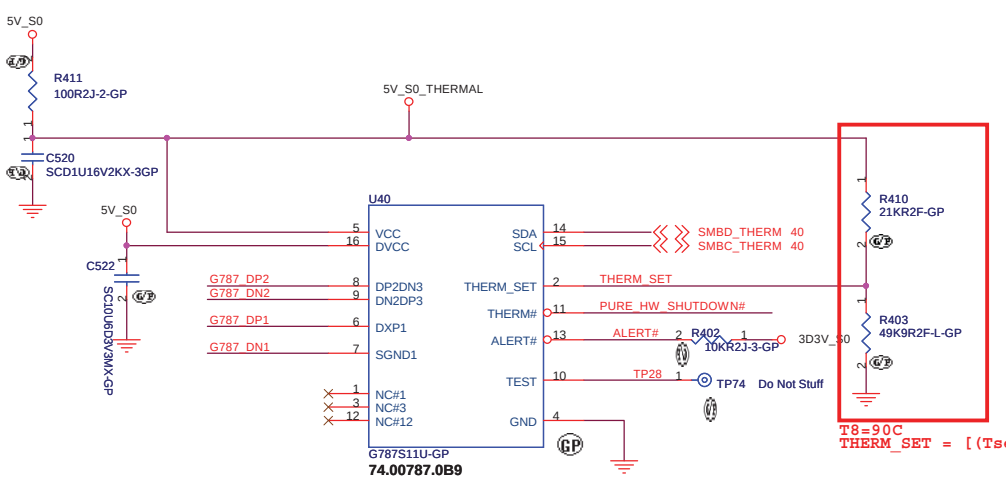
ENG DIS MADSION SAMSUNG

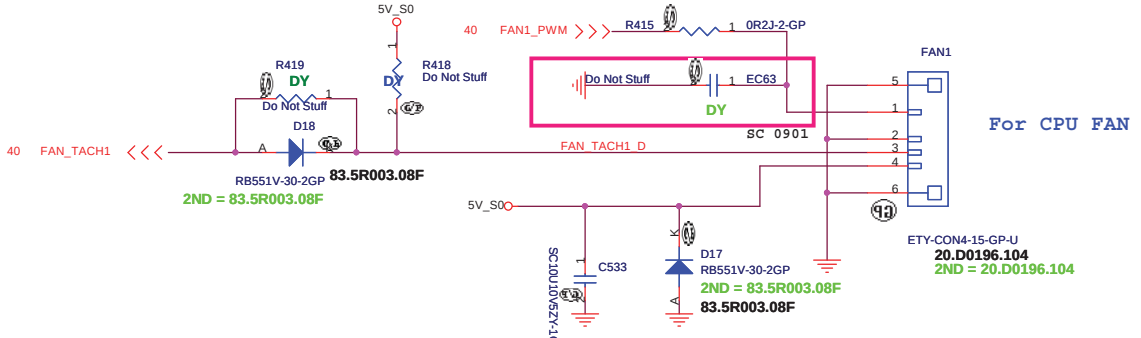
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**		
Size: A3	Document Number: **JV50-CP**	Rev: **SA**
Date: Thursday, September 03, 2009	Sheet 37 of 61	









ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thermal/Fan Connector*

Size	Document Number	Rev
	JV50-CP	SA

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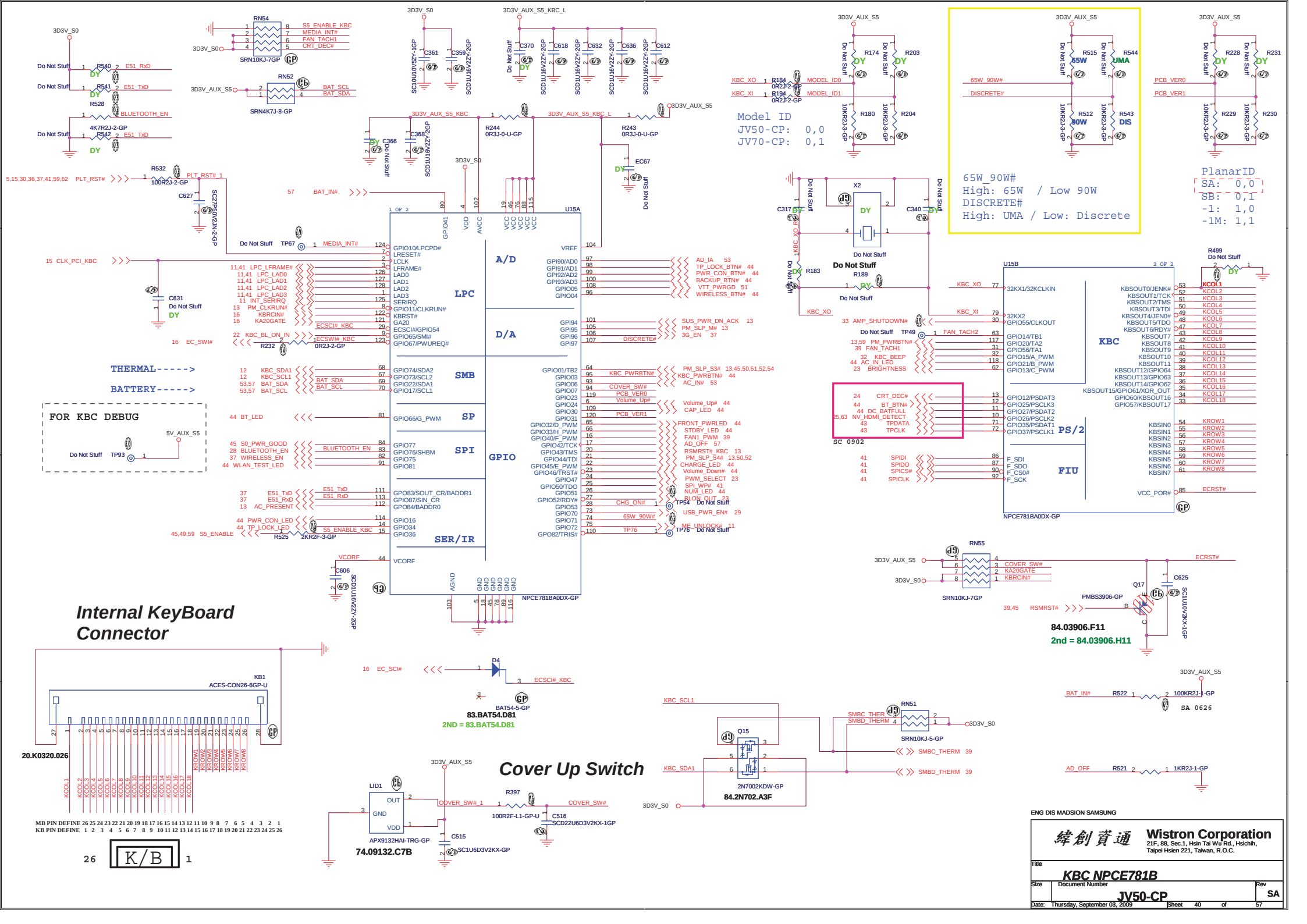
Internal KeyBoard Connector
Cover Up Switch
Model ID
JV50-CP: 0,0
JV70-CP: 0,1
65W_90W#
High: 65W / Low 90W
DISCRETE#
High: UMA / Low: Discrete
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M: 1,1
FOR KBC DEBUG
THERMAL----->
BATTERY----->
U15A
NPCE781BA0DX-GP
U15B
KBC
PS/2
FIU
SC 0902
20.K0320.026
84.03906.F11
2nd = 84.03906.H11
83.BAT54.D81
2ND = 83.BAT54.D81
84.2N702.A3F
74.09132.C7B
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
JV50-CP
SA
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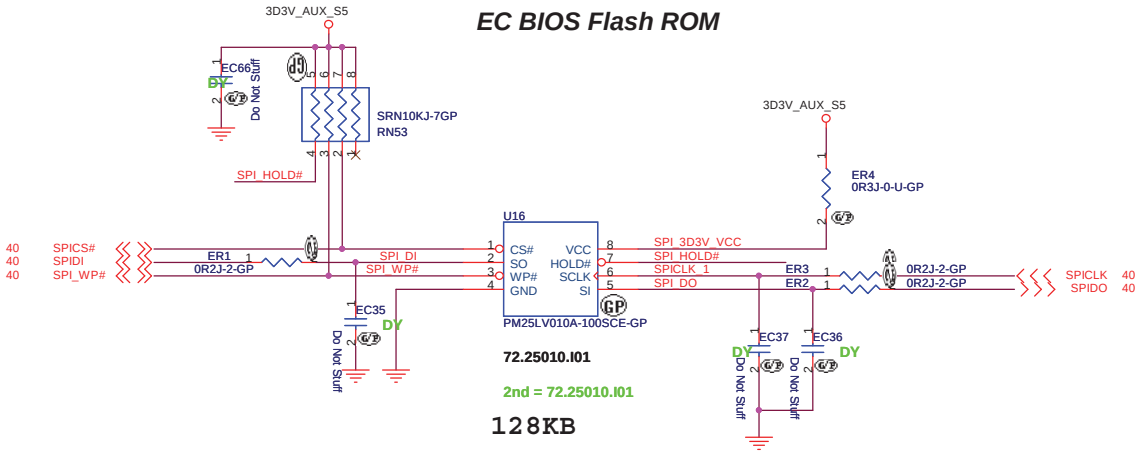
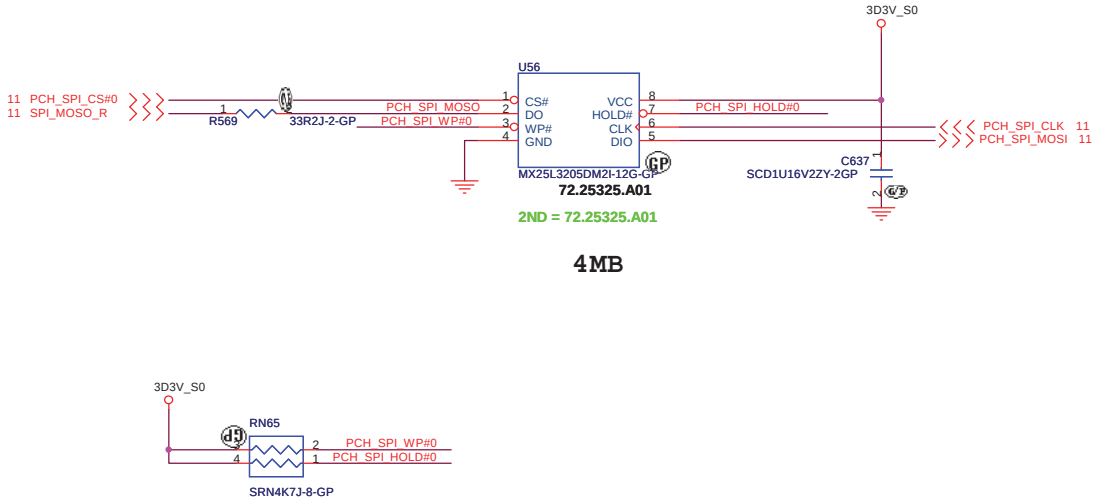
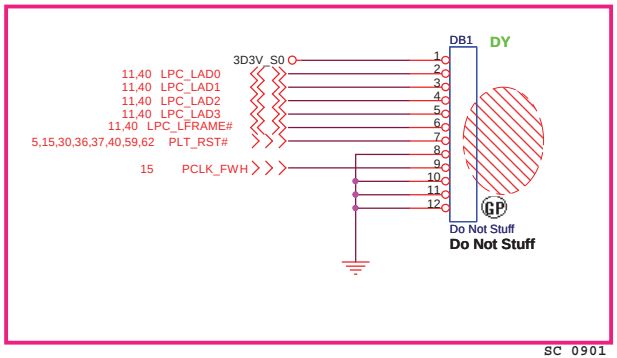
EC BIOS Flash ROM



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD



SC 0901

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

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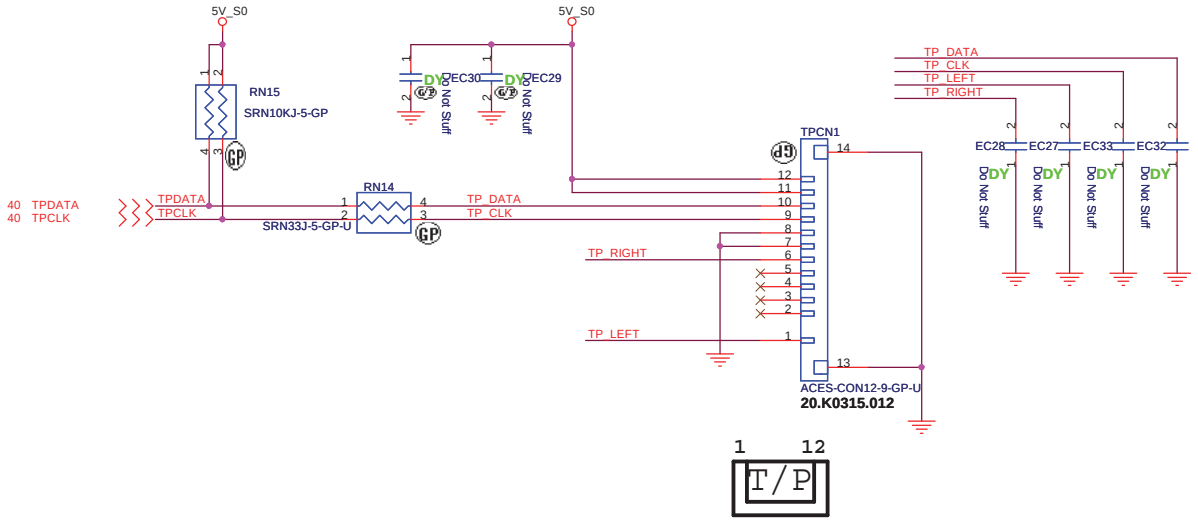
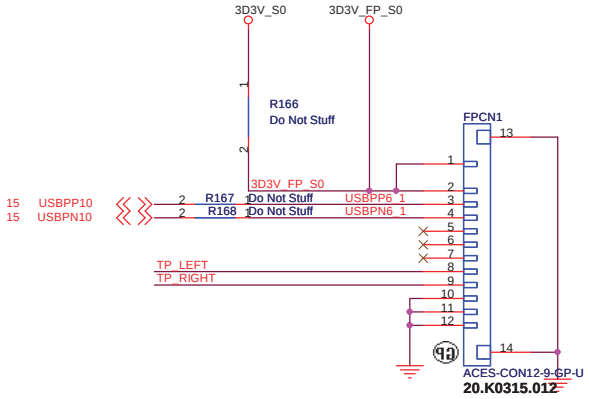
TOUCH PAD



Finger printer



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD and FP

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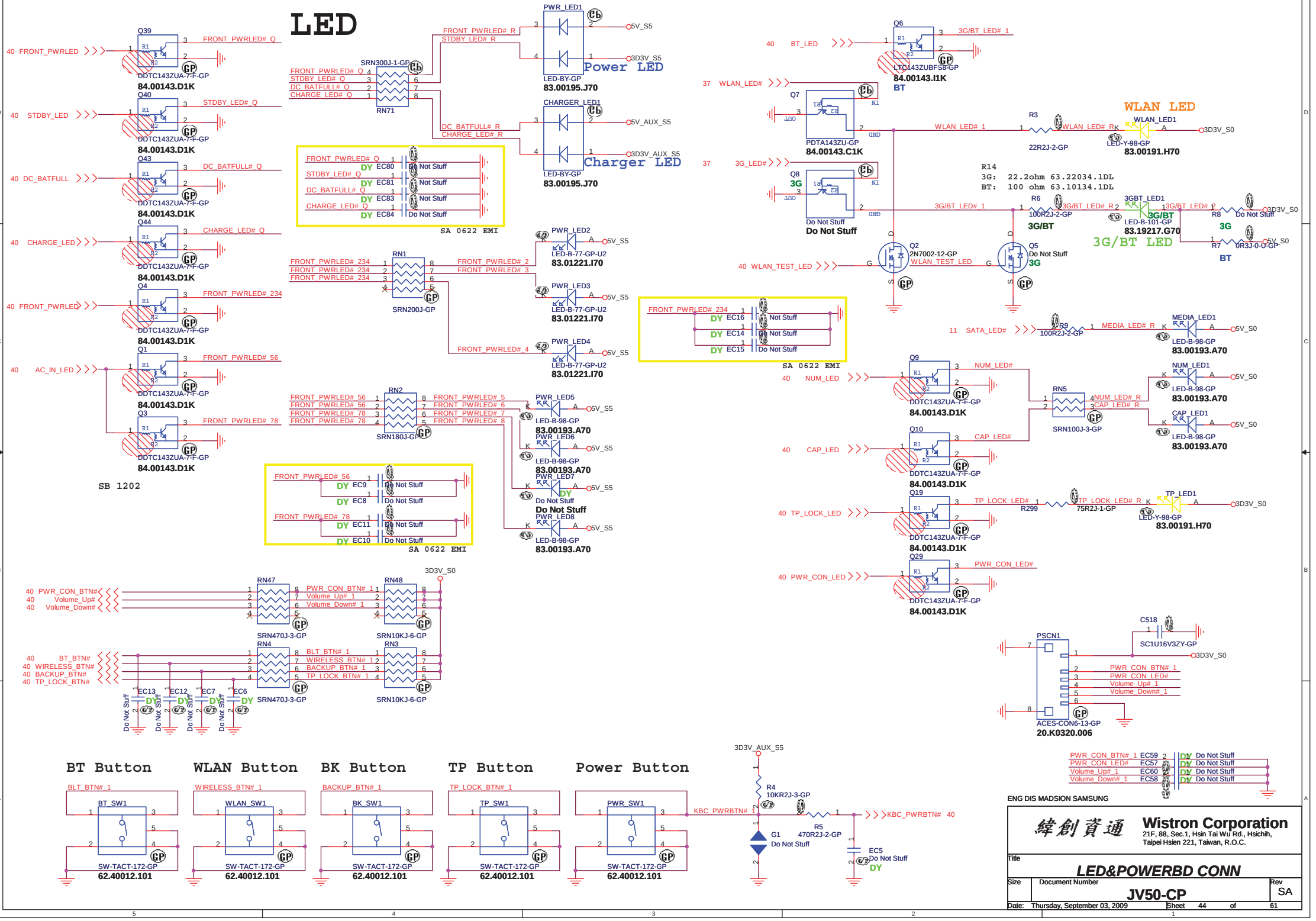
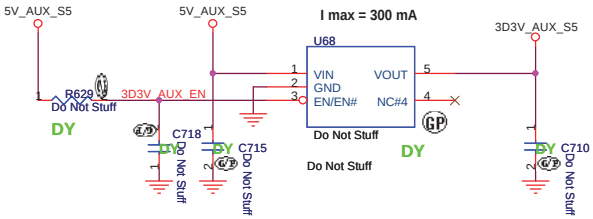
LED

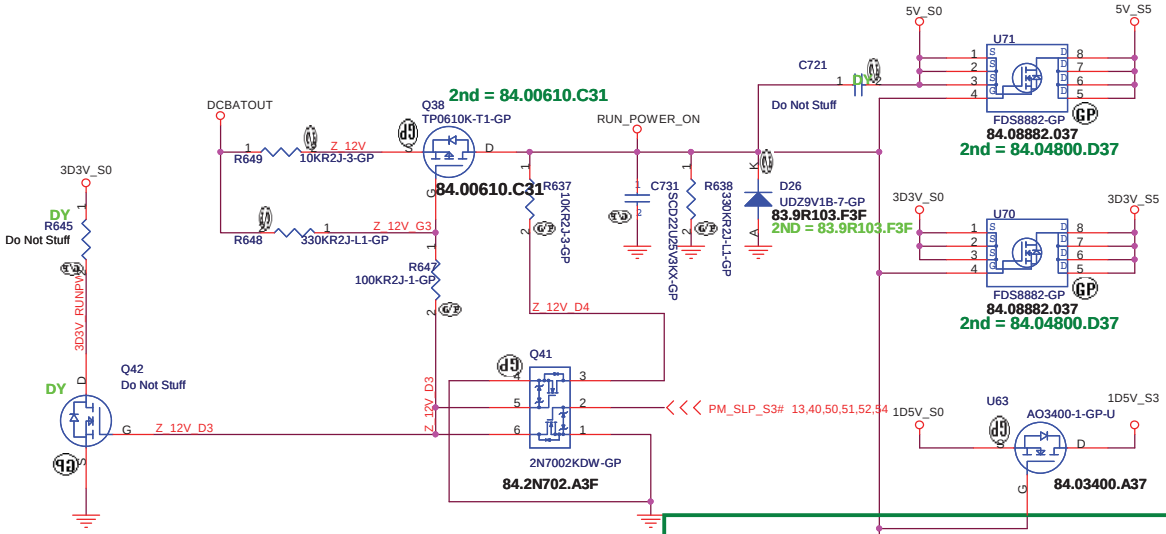

Power LED
Charger LED
WLAN LED
3G/BT LED
SA 0622 EMI
SB 1202
Do Not Stuff
BT Button
WLAN Button
BK Button
TP Button
Power Button
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LED&POWERBD CONN
JV50-CP
Thursday, September 03, 2009

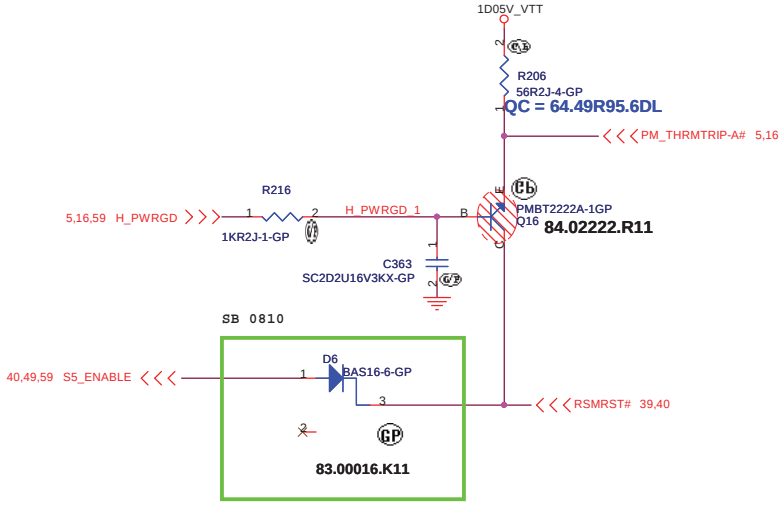
Run Power

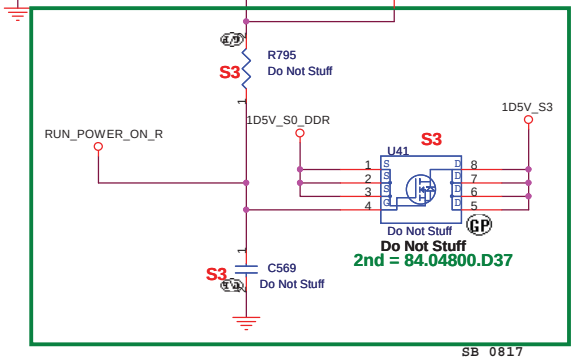
Aux Power

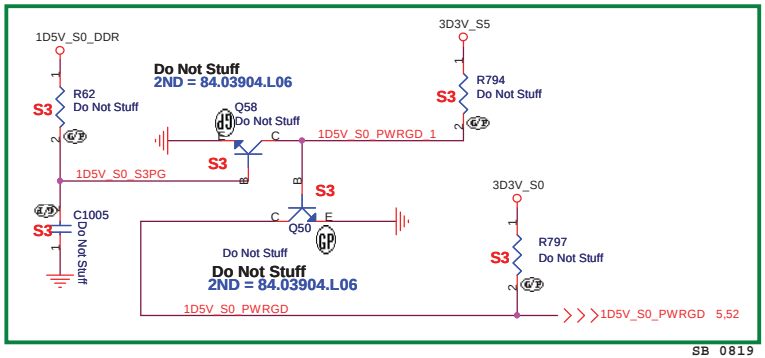
3D3V_AUX_S5

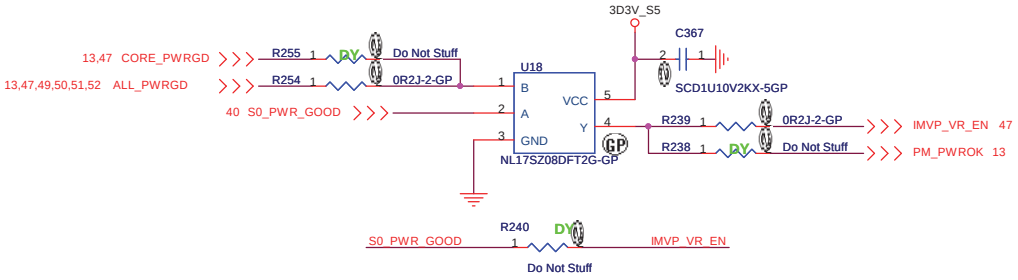












ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

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ISL62883 VCC_CORE

H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6

IMVP_VR_EN

VCC_SENSE
VSS_SENSE

DCBATOUT_62883
5V_S5
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD → CORE_PWRGD

Output Power
VCC_CORE_PWR → VCC_CORE(Imax=65A)

TPS51123 5V/3D3V

DCBATOUT_51123_1
DCBATOUT_51123_2

S5_ENABLE

ALL_PWRGD

Input Power
VIN_1
VIN_2

Input Signal
EN1
EN2

Output Signal
PGOOD

Output Power
5V(O) → 5V_S5 (8A)
3D3V(O) → 3D3V_S5 (6A)
5V_AUX(O) → 5V_AUX_S5 (100mA)
3D3V_AUX(O) → 3D3V_AUX_S5 (100mA)

RT9026 0D75V_S0

5V_S5
1D5V_S3
PM_SLP_S3#
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT → 0D75V_S0 (1.2A)
VTTREF → DDR_VREF_S3

RT9025 1D8V

5V_S5
3D3V_S0
PM_SLP_S3#
ALL_PWRGD

VIN
VLDOIN
EN
PGOOD

1D8V (O) → 1D85V_S0

RT9025 1D5V

5V_S5
DCBATOUT_7141_1D5V
PM_SLP_S4#
ALL_PWRGD

Input Power
VDD
VCC

Input Signal
EN

Output Signal
PGOOD

Output Power
1D5V (O) → 1D5V_S3 (10A)

Charger BQ24745

BATT_SENSE
AD+

Input Signal
FBS

Output Signal
ACGOOD# → AC_IN#
SRSET → AD_IA

Input Power
ACN

Output Power
VOUT (O) → BT+
VOUT (O) → DCBATOUT

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O) → AD_IN#

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O) → AD+

RT8209B 1D05V

5V_S5
DCBATOUT_RT8209B_1D05V
PM_SLP_S3#
ALL_PWRGD

Input Power
VDD
VCC

Input Signal
EN

Output Signal
PGOOD

Output Power
1D05V (O) → 1D05V_S0 (10A)

ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
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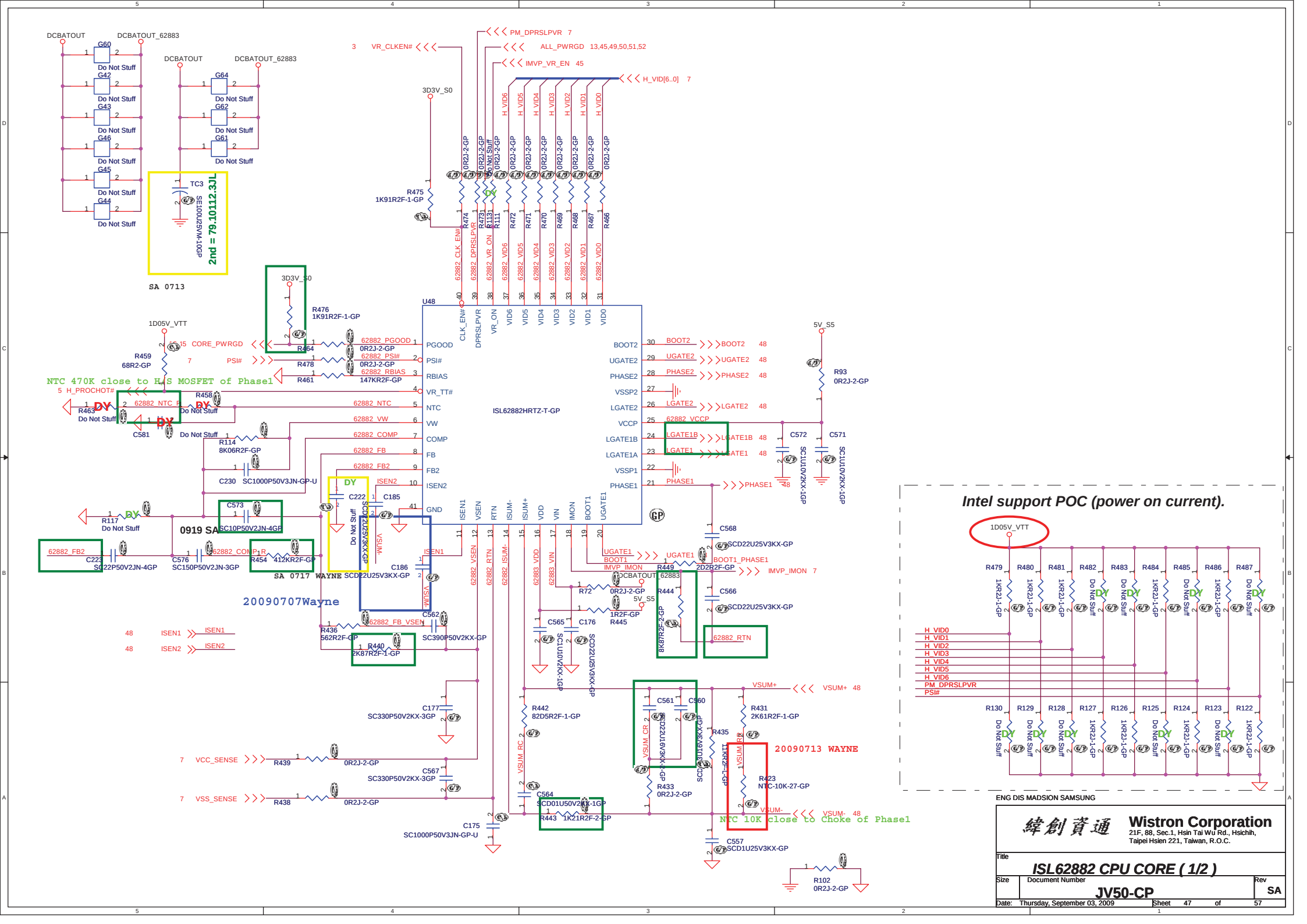
ISL62882HRTZ-T-GP
U48
SA 0713
0919 SA
SA 0717 WAYNE SCD22U25V3KX-GP
20090707Wayne
20090713 WAYNE
NTC 470K close to H_S MOSFET of Phase1
NTC 10K close to Choke of Phase1
2nd = 79.10112.33L
Intel support POC (power on current).
ENG DIS MADSION SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
JV50-CP
Rev
SA
Date: Thursday, September 03, 2009
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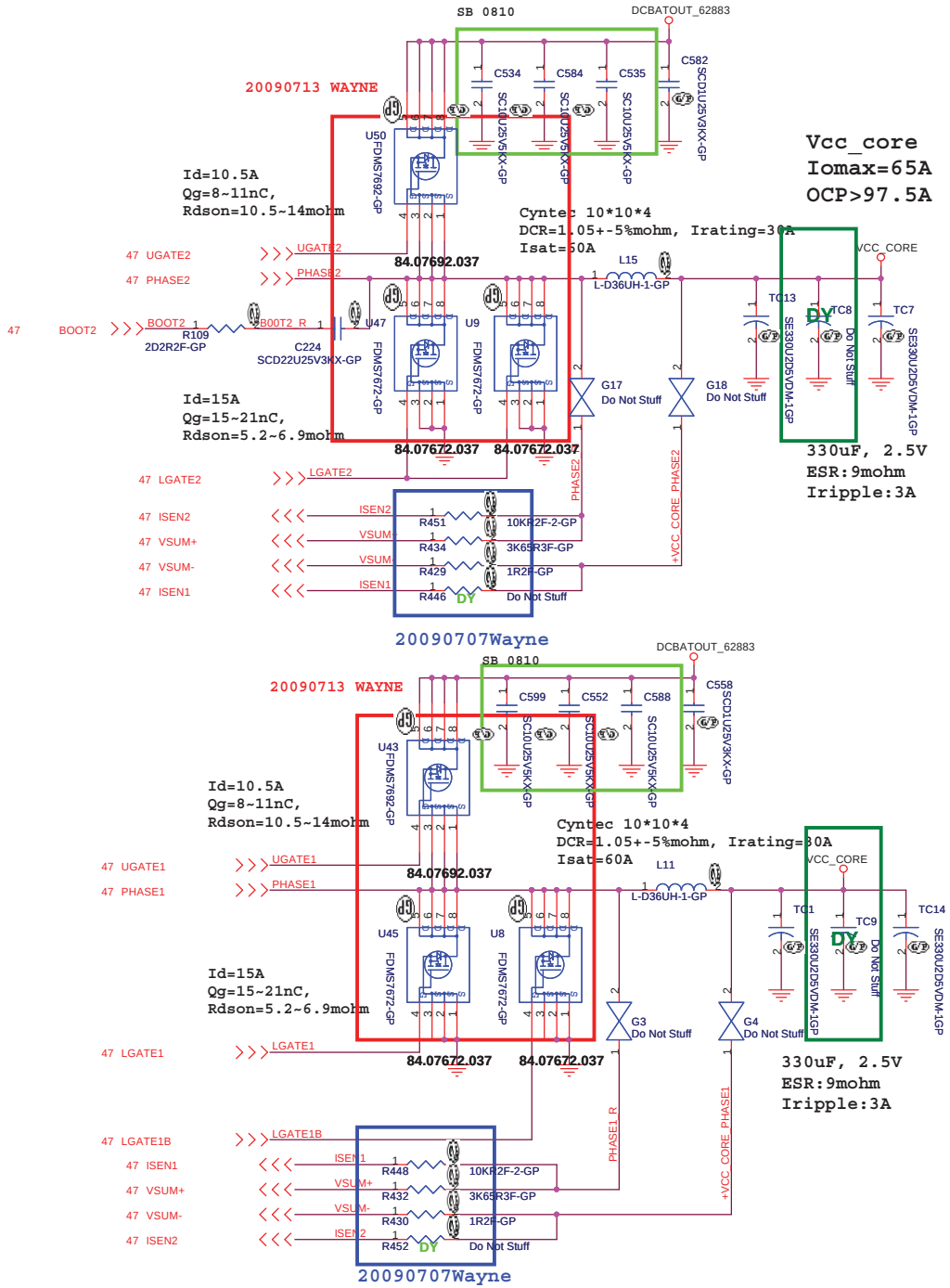

ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *ISL62882 CPU CORE (1/2)*

Size	Document Number	Rev
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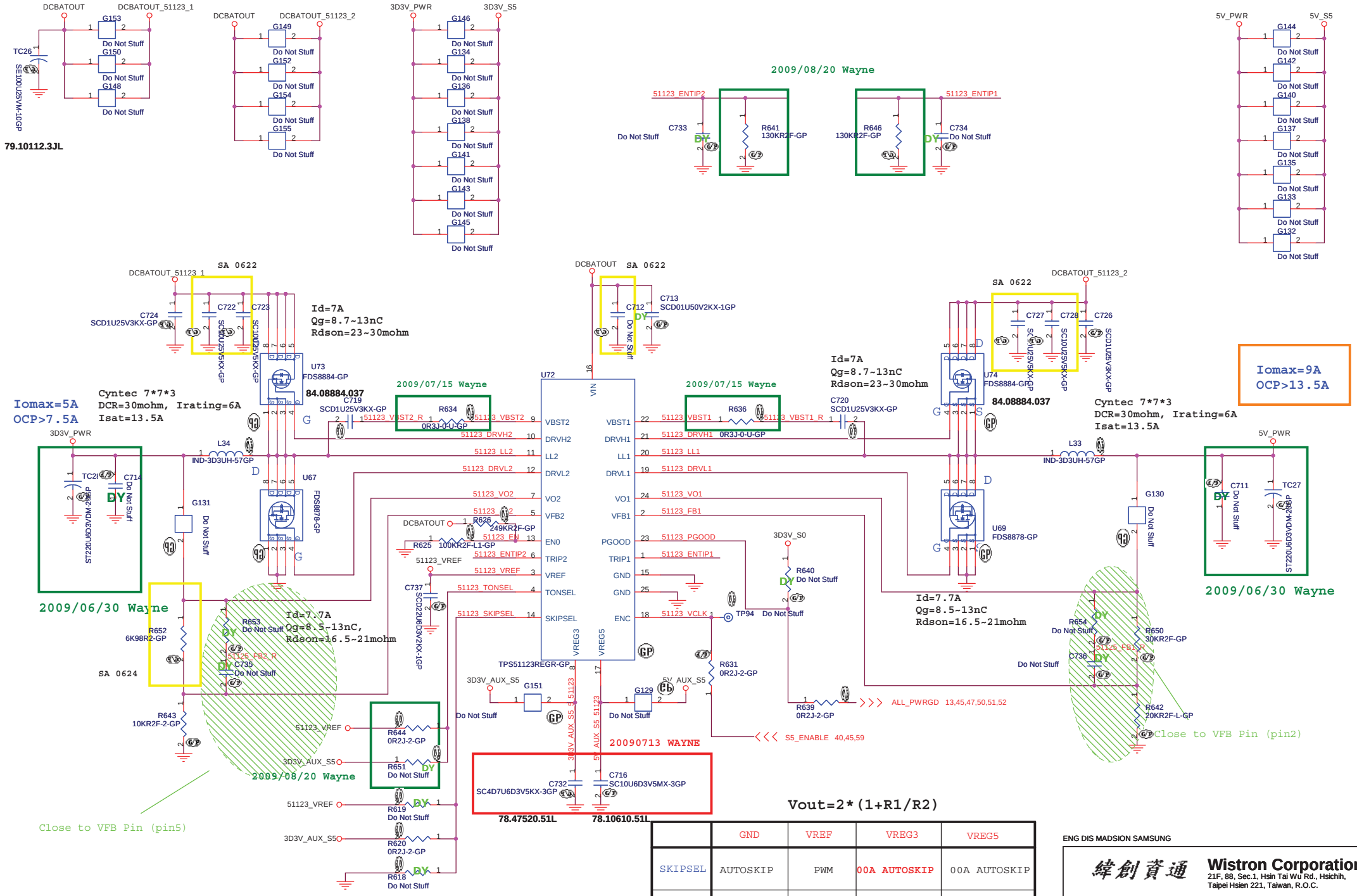
Date: Thursday, September 03, 2009 Sheet 48 of 57



	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51123 5V/3D3V

Size | Document Number: JV50-CP | Rev: SA

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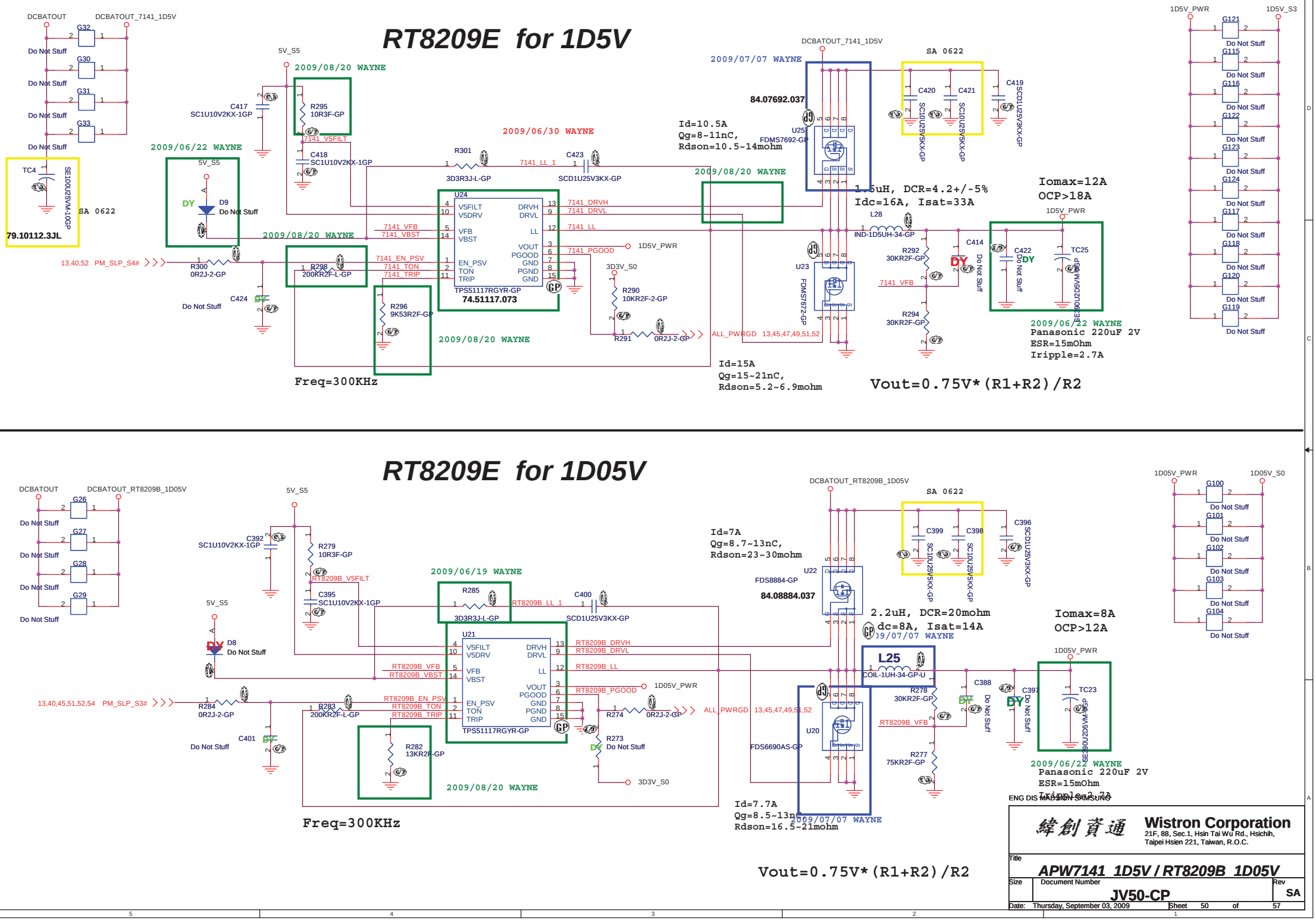
RT8209E for 1D5V
DCBATOUT
DCBATOUT_7141_1D5V
Do Not Stuff
TC4
SE100U25VM-10GP
SA 0622
79.10112.3JL
5V_S5
2009/08/20 WAYNE
C417
SC1U10V2KX-1GP
R295
10R3F-GP
7141_V5FILT
C418
SC1U10V2KX-1GP
2009/06/22 WAYNE
D9
DY
R300
0R2J-2-GP
13,40,52 PM_SLP_S4#
C424
R298
200KR2F-L-GP
R296
9K53R2F-GP
2009/06/30 WAYNE
R301
3D3R3J-L-GP
7141_LL_1
C423
SCD1U25V3KX-GP
U24
V5FILT
V5DRV
VFB
VBST
EN_PSV
TON
TRIP
DRVH
DRVL
LL
VOUT
PGOOD
GND
PGND
TPS51117RGYR-GP
74.51117.073
7141_VFB
7141_VBST
7141_EN_PSV
7141_TON
7141_TRIP
7141_DRVH
7141_DRVL
7141_LL
7141_PGOOD
1D5V_PWR
3D3V_S0
R290
10KR2F-2-GP
R291
0R2J-2-GP
ALL_PWRGD 13,45,47,49,51,52
Freq=300KHz
2009/07/07 WAYNE
DCBATOUT_7141_1D5V
84.07692.037
U25
FDMS7692-GP
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
SA 0622
C420
C421
C419
SCD1U25V3KX-GP
2009/08/20 WAYNE
1.5uH, DCR=4.2+/-5%
Idc=16A, Isat=33A
Iomax=12A
OCP>18A
L28
IND-1D5UH-34-GP
U23
FDMS7672-GP
R292
30KR2F-GP
R294
30KR2F-GP
7141_VFB
C414
C422
DO NOT STUFF
TC25
SE390U2D5GM-GP
2009/06/22 WAYNE
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
Vout=0.75V*(R1+R2)/R2
1D5V_S3
G121
G115
G116
G122
G123
G124
G117
G118
G120
G119
RT8209E for 1D05V
DCBATOUT
DCBATOUT_RT8209B_1D05V
G26
G27
G28
G29
5V_S5
C392
SC1U10V2KX-1GP
R279
10R3F-GP
RT8209B_V5FILT
C395
SC1U10V2KX-1GP
D8
2009/06/19 WAYNE
R285
3D3R3J-L-GP
RT8209B_LL_1
C400
SCD1U25V3KX-GP
U21
RT8209B_VFB
RT8209B_VBST
RT8209B_EN_PSV
RT8209B_TON
RT8209B_TRIP
RT8209B_DRVH
RT8209B_DRVL
RT8209B_LL
RT8209B_PGOOD
1D05V_PWR
13,40,45,51,52,54 PM_SLP_S3#
R284
0R2J-2-GP
R283
200KR2F-L-GP
C401
R282
13KR2F-GP
R274
0R2J-2-GP
R273
3D3V_S0
ALL_PWRGD 13,45,47,49,51,52
Freq=300KHz
DCBATOUT_RT8209B_1D05V
SA 0622
Id=7A
Qg=8.7~13nC,
Rdson=23~30mohm
U22
FDS8884-GP
84.08884.037
C399
C398
C396
SCD1U25V3KX-GP
2.2uH, DCR=20mohm
dc=8A, Isat=14A
2009/07/07 WAYNE
Iomax=8A
OCP>12A
L25
COIL-1UH-34-GP-U
U20
FDS6690AS-GP
R278
30KR2F-GP
R277
75KR2F-GP
RT8209B_VFB
C388
C397
TC23
SE390U2D5GM-GP
2009/06/22 WAYNE
Panasonic 220uF 2V
ESR=15mOhm
Iripple=2.7A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
2009/07/07 WAYNE
Vout=0.75V*(R1+R2)/R2
1D05V_S0
G100
G101
G102
G103
G104
ENG DIS MADISON SAMSUNG
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
APW7141 1D5V / RT8209B 1D05V
Size
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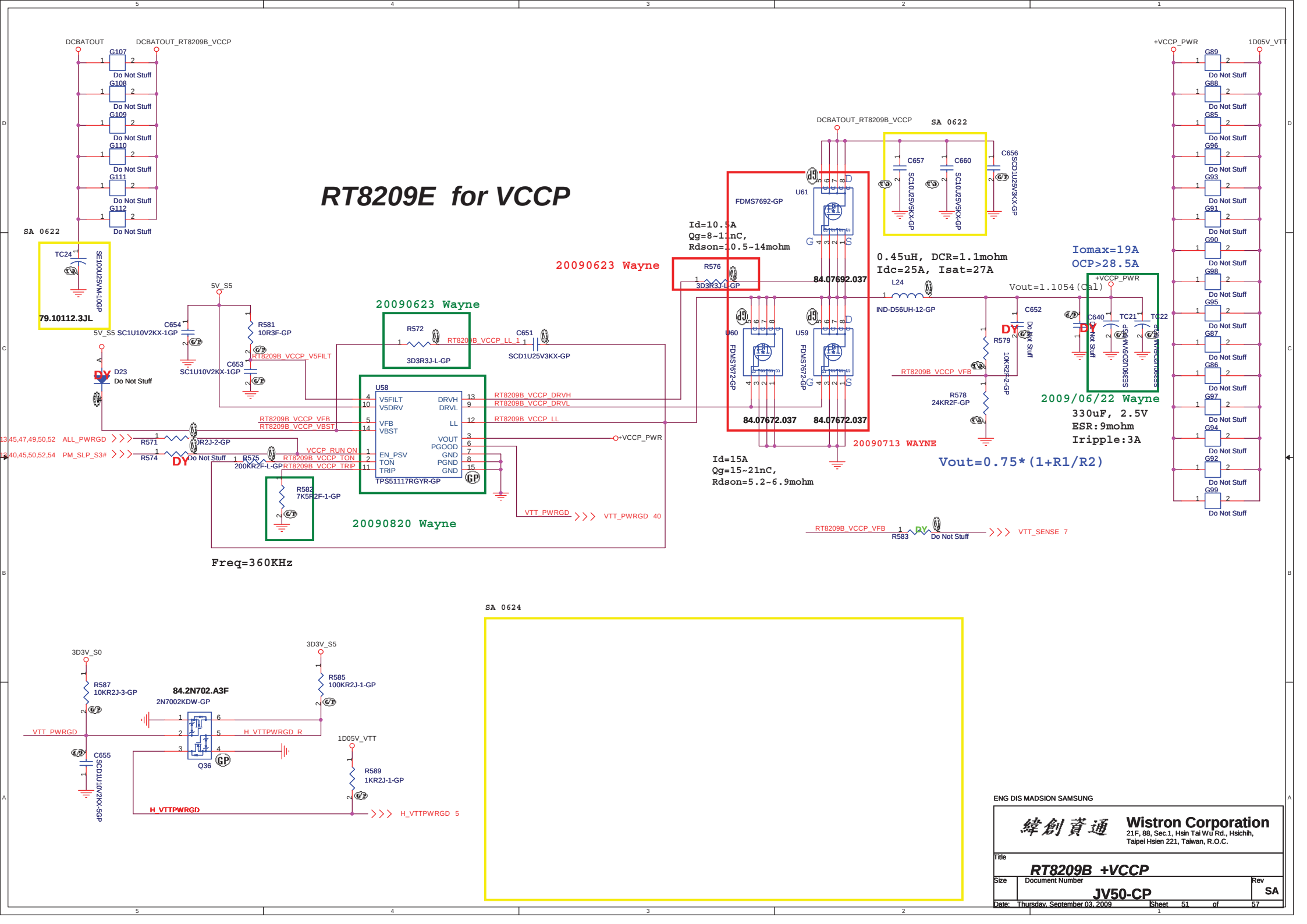
RT8209E for VCCP
DCBATOUT
DCBATOUT_RT8209B_VCCP
SA 0622
79.10112.3JL
20090623 Wayne
20090820 Wayne
20090713 WAYNE
2009/06/22 Wayne
SA 0624
U58
TPS51117RGYR-GP
U59
U60
U61
FDMS7672-GP
FDMS7692-GP
84.07692.037
84.07672.037
Id=10.5A
Qg=8~11nC,
Rdson=10.5~14mohm
Id=15A
Qg=15~21nC,
Rdson=5.2~6.9mohm
0.45uH, DCR=1.1mohm
Idc=25A, Isat=27A
Iomax=19A
OCP>28.5A
330uF, 2.5V
ESR:9mohm
Iripple:3A
Vout=0.75*(1+R1/R2)
Vout=1.1054(Cal)
Freq=360KHz
84.2N702.A3F
2N7002KDW-GP
Q36
+VCCP_PWR
1D05V_VTT
VTT_PWRGD
VTT_SENSE
H_VTTPWRGD
ENG DIS MADSION SAMSUNG
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RT8209B +VCCP
JV50-CP
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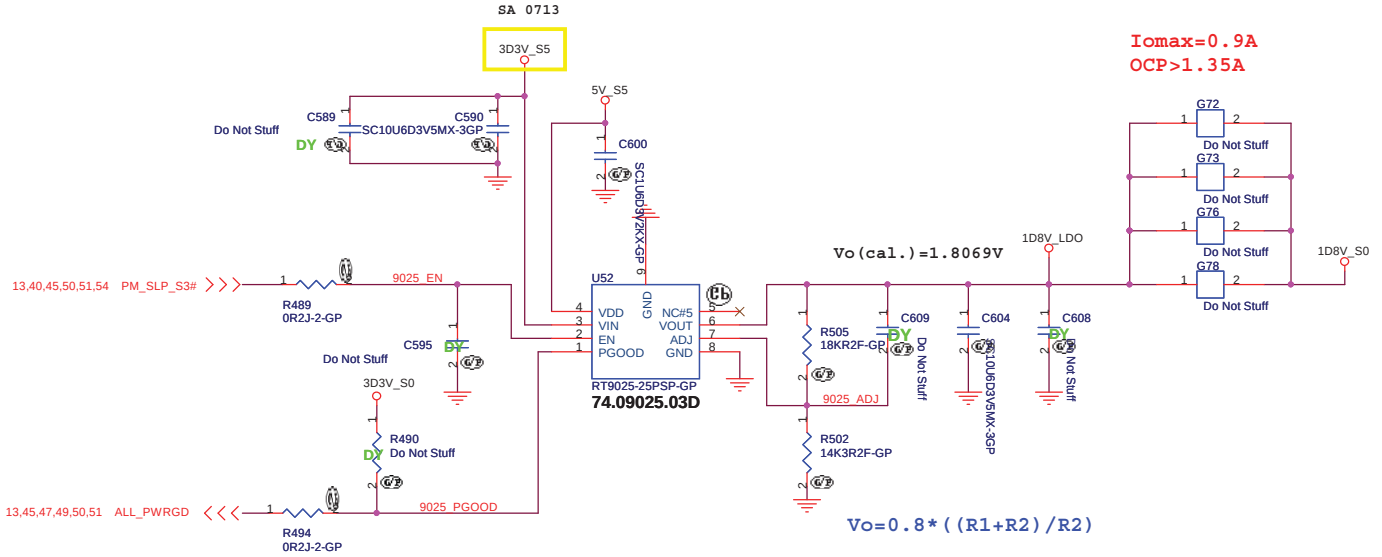
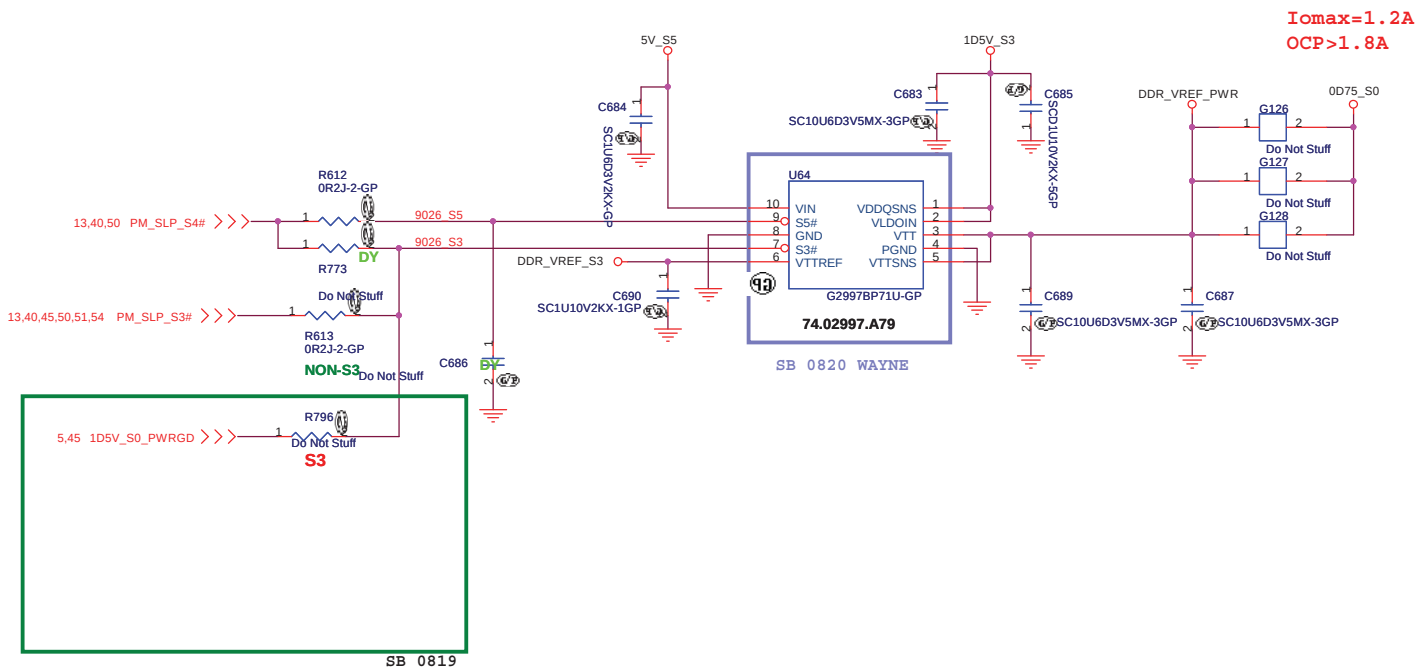
RT9025 for 1D8V_S0

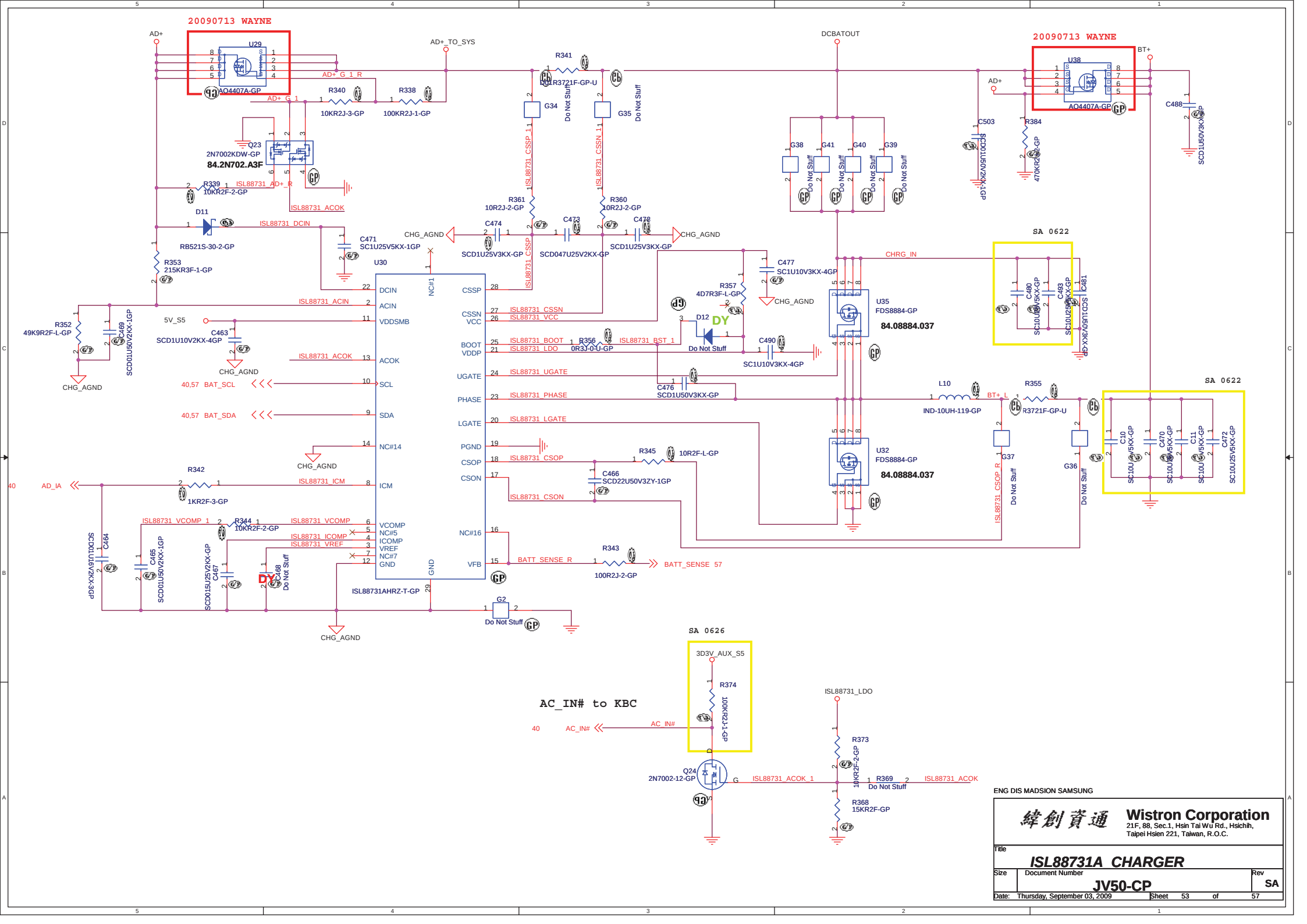


RT9026 for 0D75V_S3



ENG DIS MADSION SAMSUNG

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	RT9025_1D8V/RT9026_0D75
Size	Document Number: JV50-CP
Rev	SA
Date: Thursday, September 03, 2009	Sheet 52 of 57



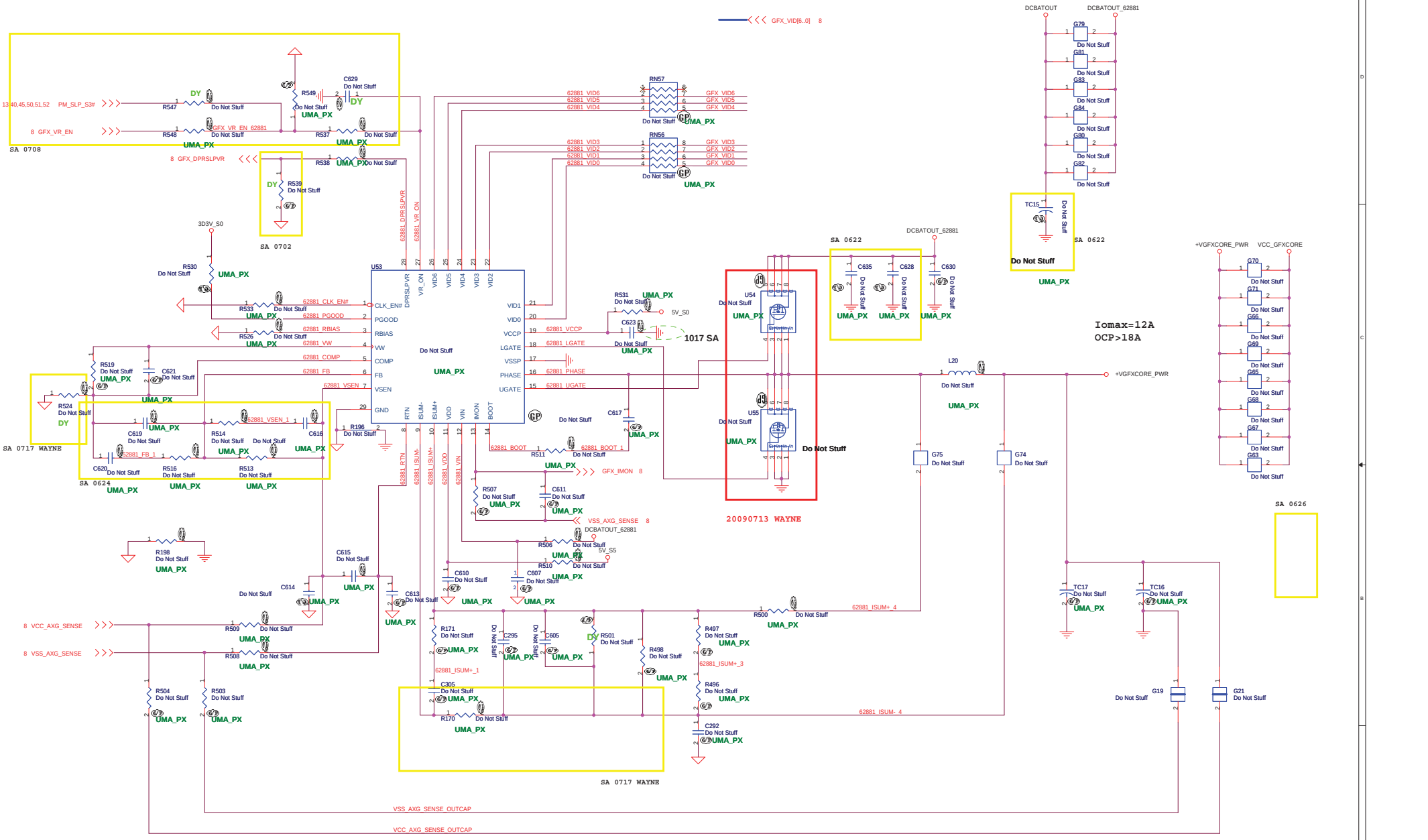
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL88731A CHARGER**

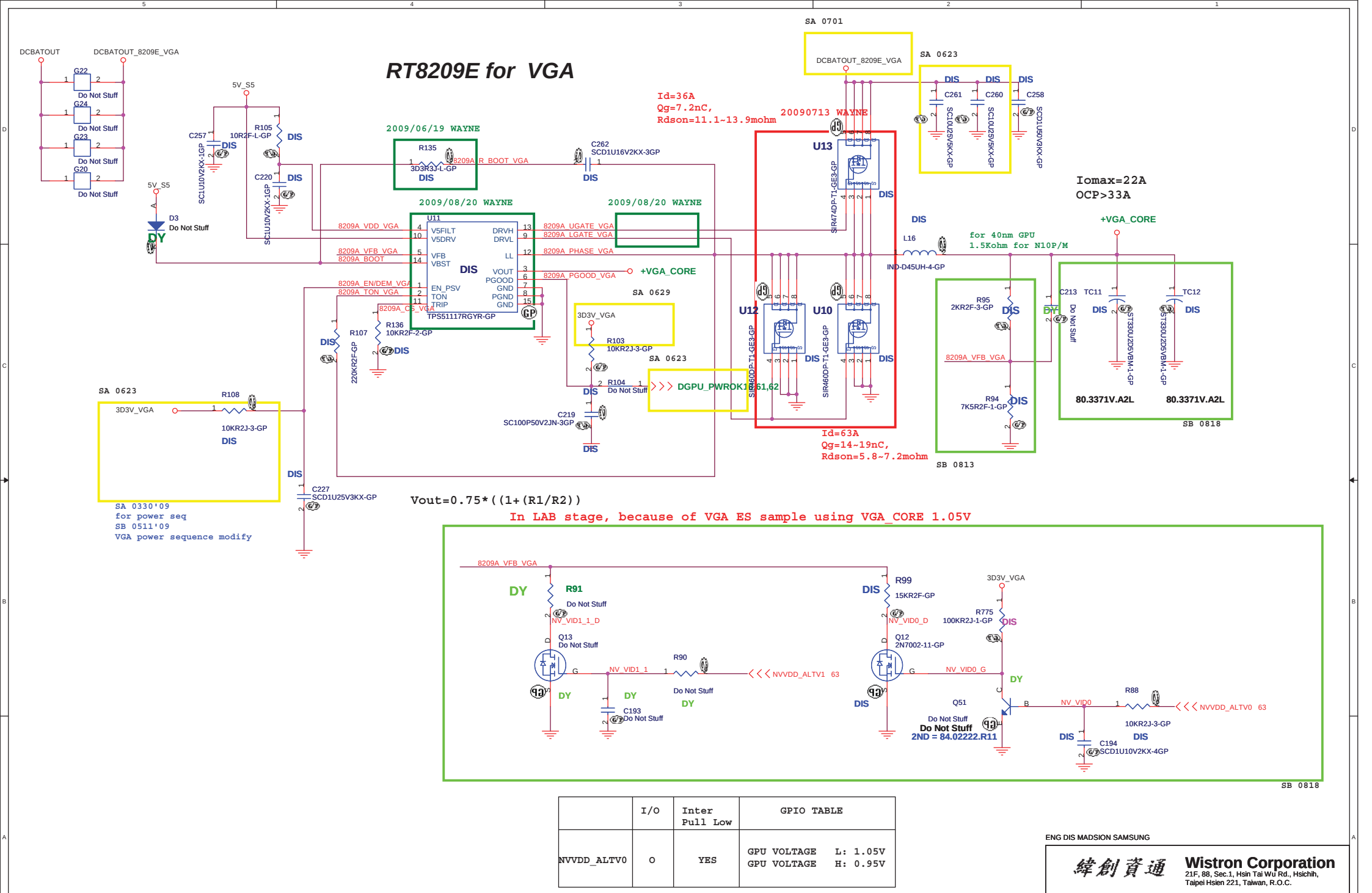
Size	Document Number	Rev
	JV50-CP	SA

Date: Thursday, September 03, 2009 Sheet 53 of 57



ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**ISL62881 +VCC_GFXCORE**	
Size: C	Document Number: **JV50-CP**	Rev: **SB**
Date: Thursday, September 03, 2009	Sheet 54 of 45	



	I/O	Inter Pull Low	GPIO TABLE
NVVDD_ALTV0	O	YES	GPU VOLTAGE L: 1.05V GPU VOLTAGE H: 0.95V

ENG DIS MADSION SAMSUNG

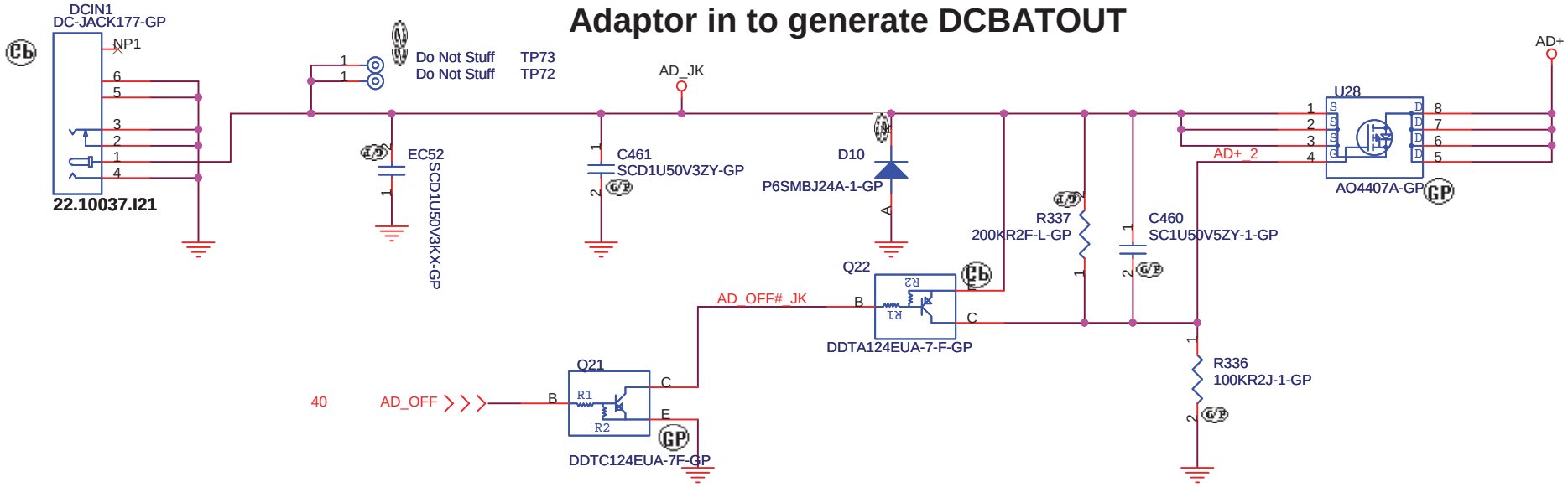
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209E VGA CORE

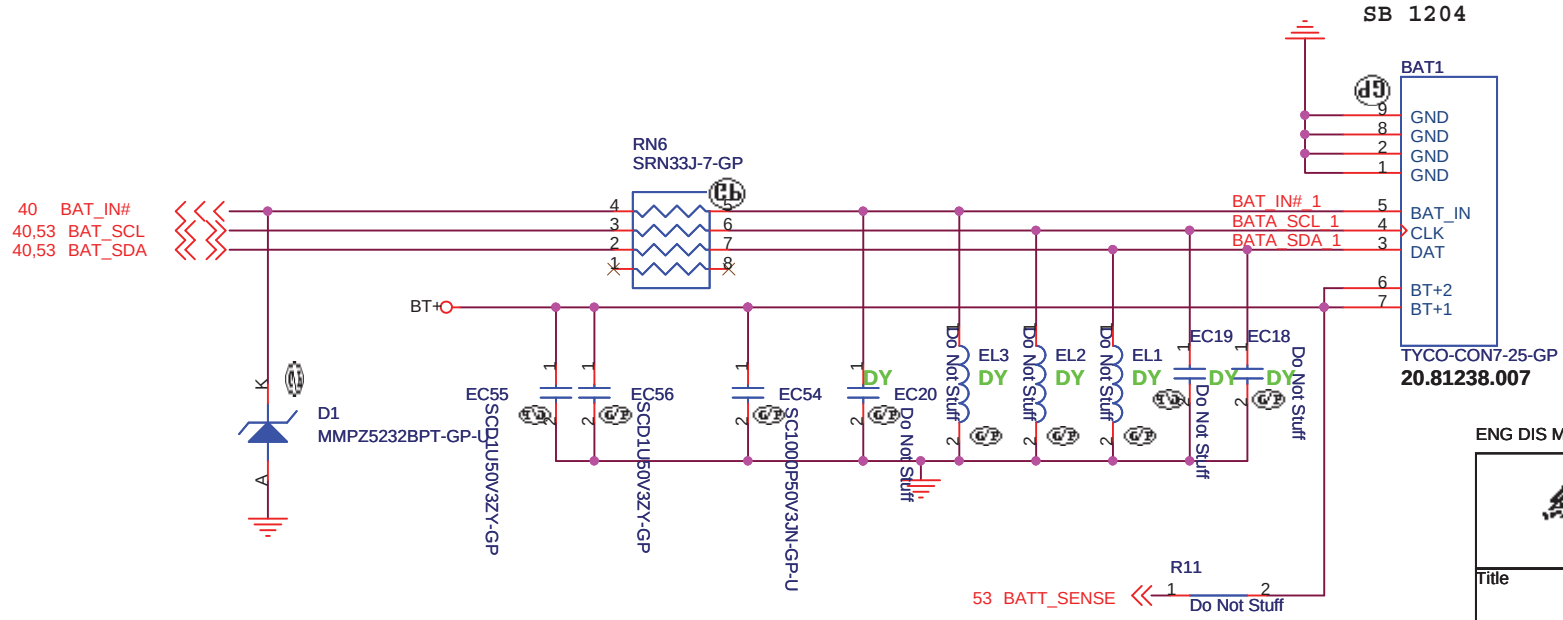
Size: A3 | Document Number: JV50-CP | Rev:

Date: Thursday, September 03, 2009 | Sheet 55 of 52

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



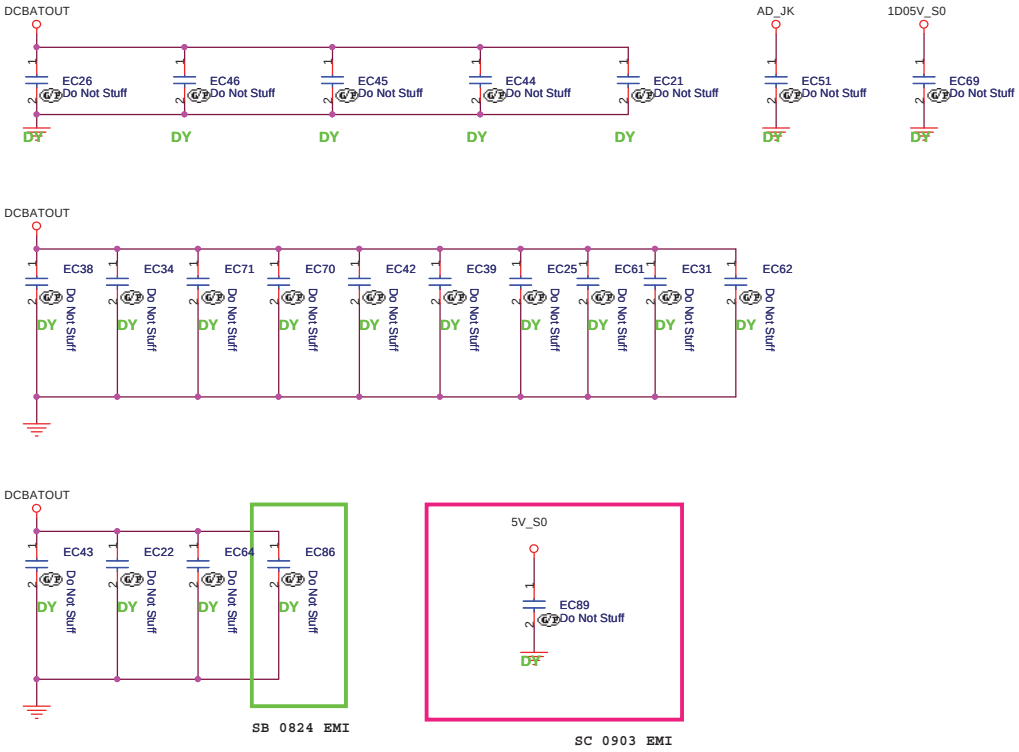
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AD/BATT CONN

Size	Document Number	Rev
	JV50-CP	SA

Date: Thursday, September 03, 2009 Sheet 57 of 61



CPU

H1 H2 H3 — STF237R125H42-GP — 34.4GD01.001 34.4GD01.001 34.4GD01.001

PCH

H4 — STF237R125H42-GP — 34.4GD01.001

VGA

H5 DIS H6 DIS H11 DIS — STF237R125H42-GP — 34.4GD01.001 34.4GD01.001 34.4GD01.001

MDC

H7 HOLE — ZZ.0HOLE.XXX — 34.42Y01.011

MINICARD

H8 HOLE — ZZ.0HOLE.XXX — 34.4P901.001

H9 Do Not Stuff H10 Do Not Stuff

GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND9 GND10 GND11 GND12 — Do Not Stuff

SPRING_GND16 SPRING_GND17 SPRING_GND18 SPRING_GND19 — Do Not Stuff

SPRING_GND14 SPRING_GND15 SPRING_GND21 SPRING_GND22 — Do Not Stuff

SPRING_GND23 SPRING_GND24 SPRING_GND25 SPRING_GND26 — Do Not Stuff

ENG DIS MADSION SAMSUNG

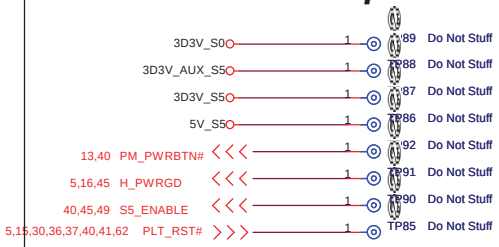
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

Size | Document Number: JV50-CP | Rev: SA

Date: Thursday, September 03, 2009 | Sheet 58 of 61

Check test point



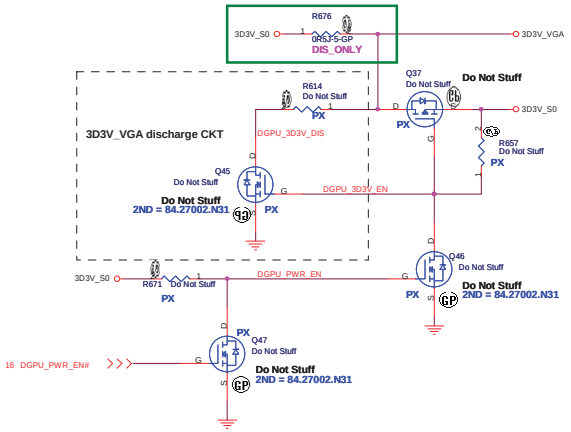
Test Point放在Dimm Door打開可量測處

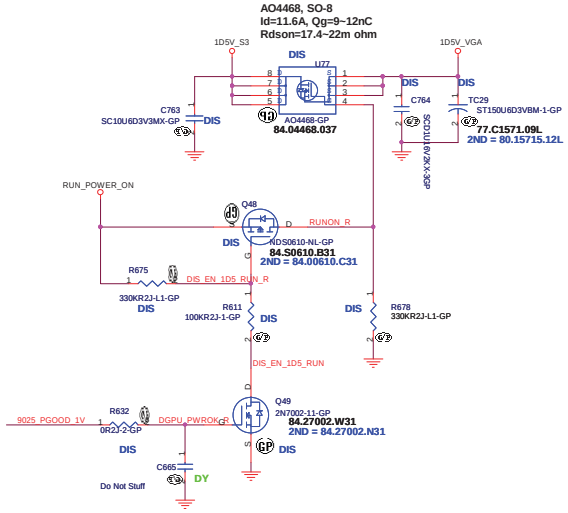
ENG DIS MADSION SAMSUNG

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

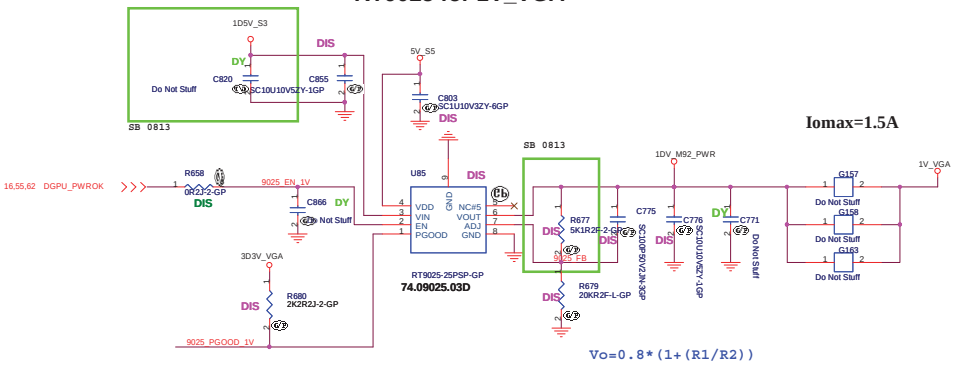
Title: AFTE_TP		
Size	Document Number: JV50-CP	Rev: SA
Date: Thursday, September 03, 2009	Sheet 59 of 57	

+3VS to 3.3V_DELAY Transfer

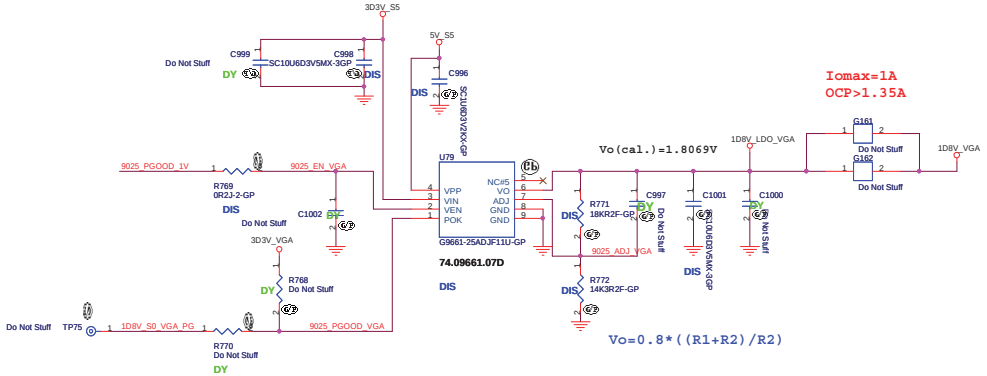




RT9025 for 1V_VGA



G9661 for 1D8V_VGA



ENG DIS MADSION SAMSUNG

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI_POWER

Size	Document Number	Rev
A2	JV50-CP	SB

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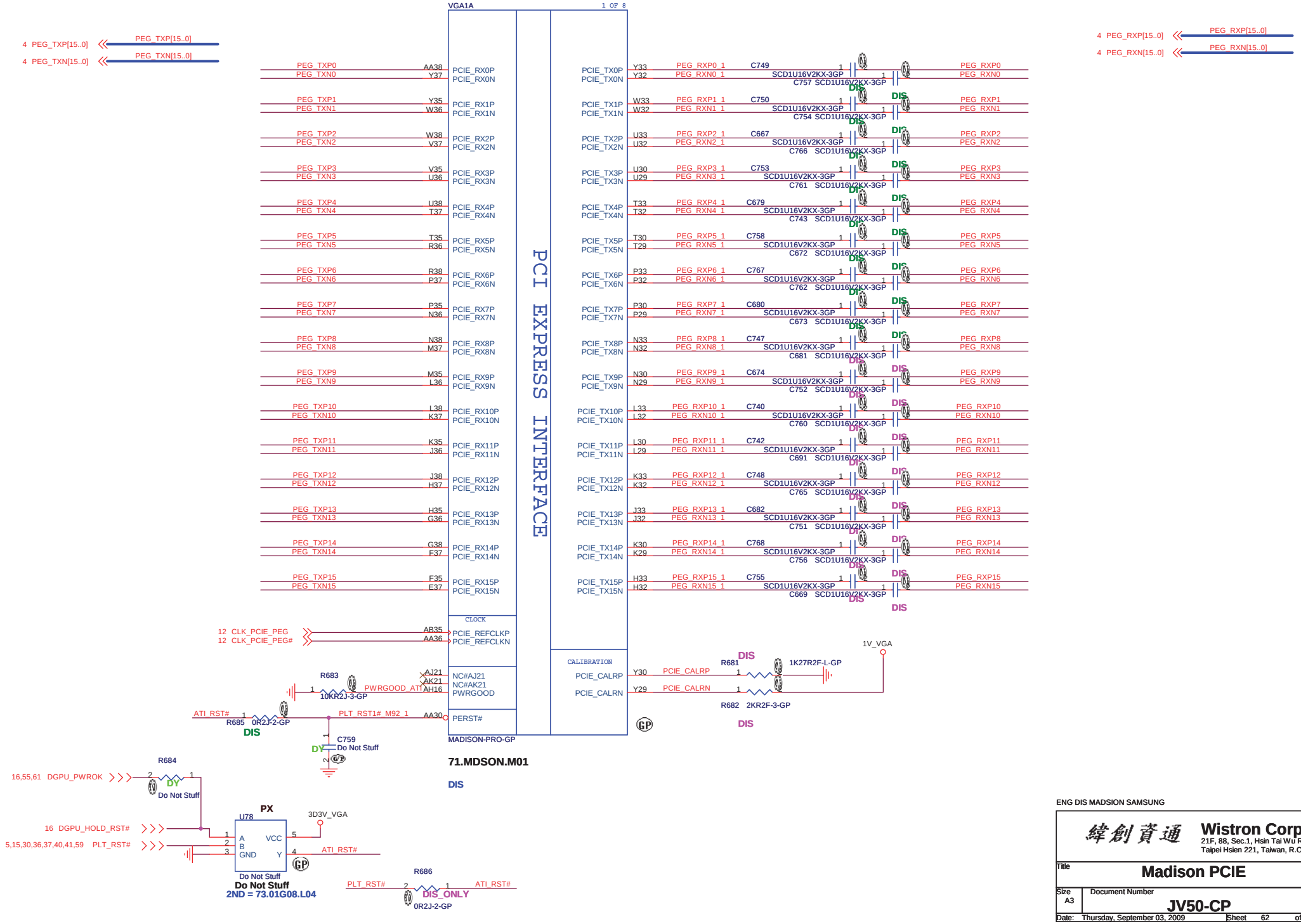
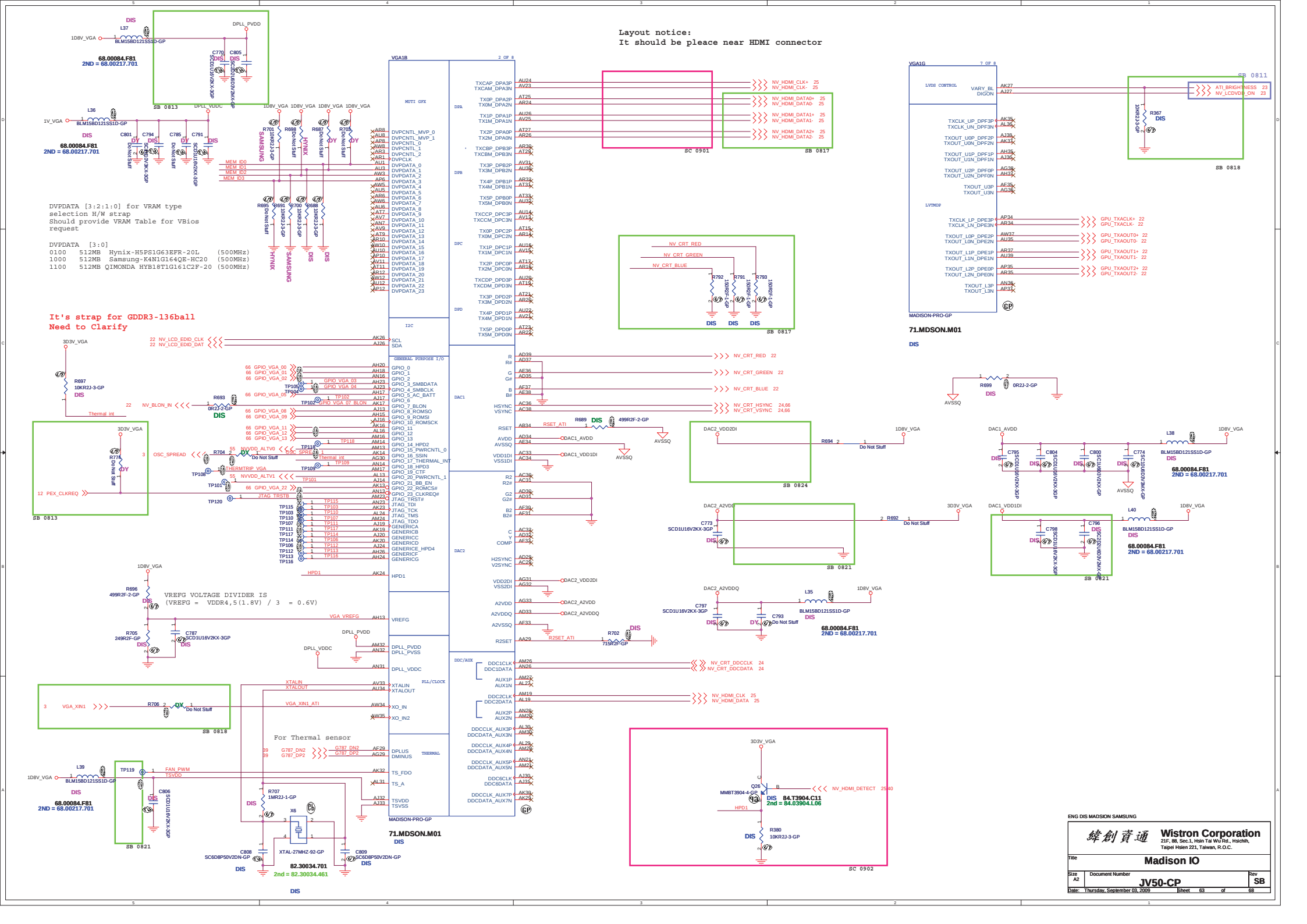
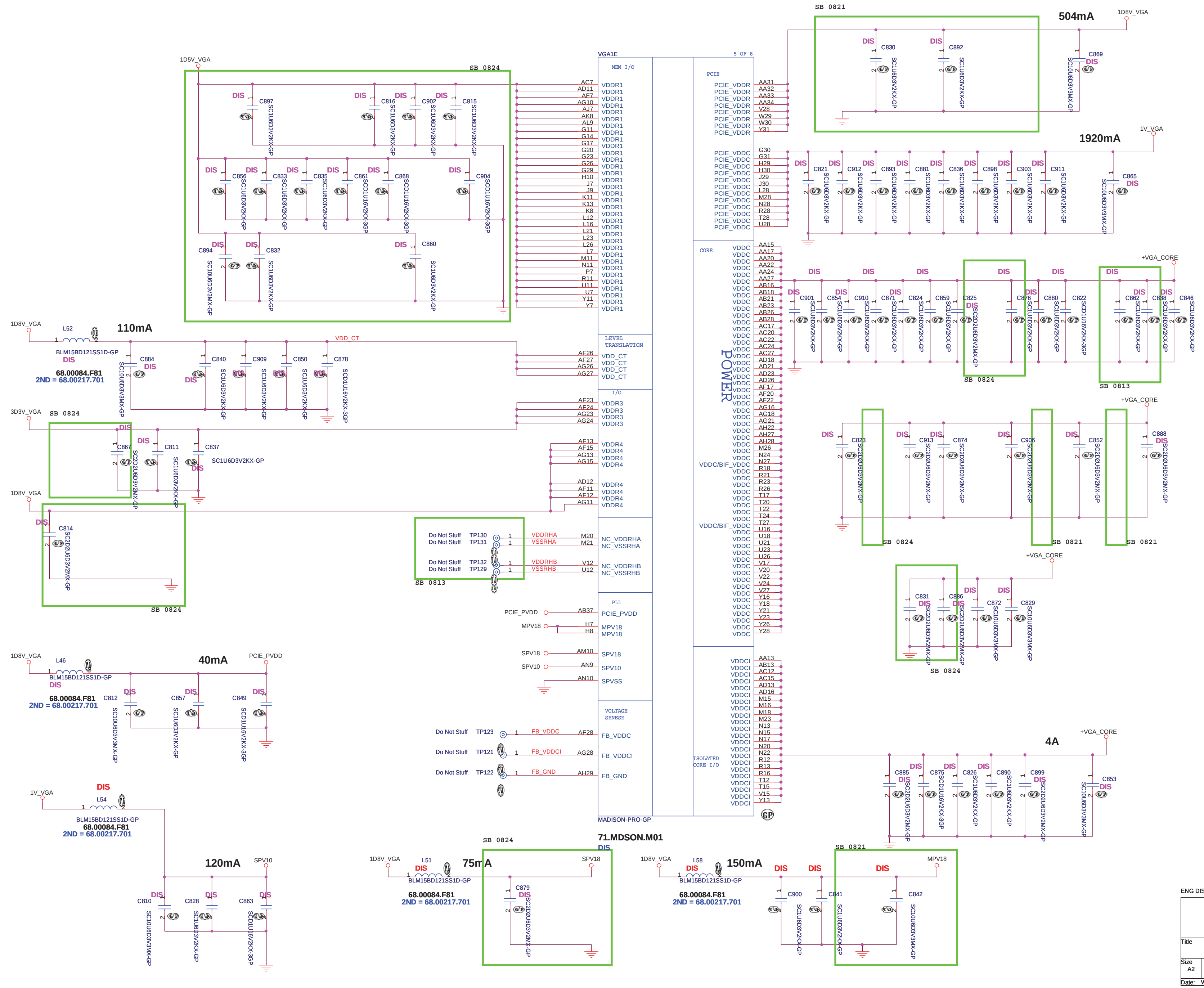


ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Madison PCIE		
Size: A3	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 62 of 68	


Layout notice:
It should be pleace near HDMI connector
DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request
DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)
It's strap for GDDR3-136ball
Need to Clarify
VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
For Thermal sensor
VGA1B
VGA1G
MADISON-PRO-GP
71.MDSON.M01
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Madison IO
JV50-CP
Thursday, September 03, 2009



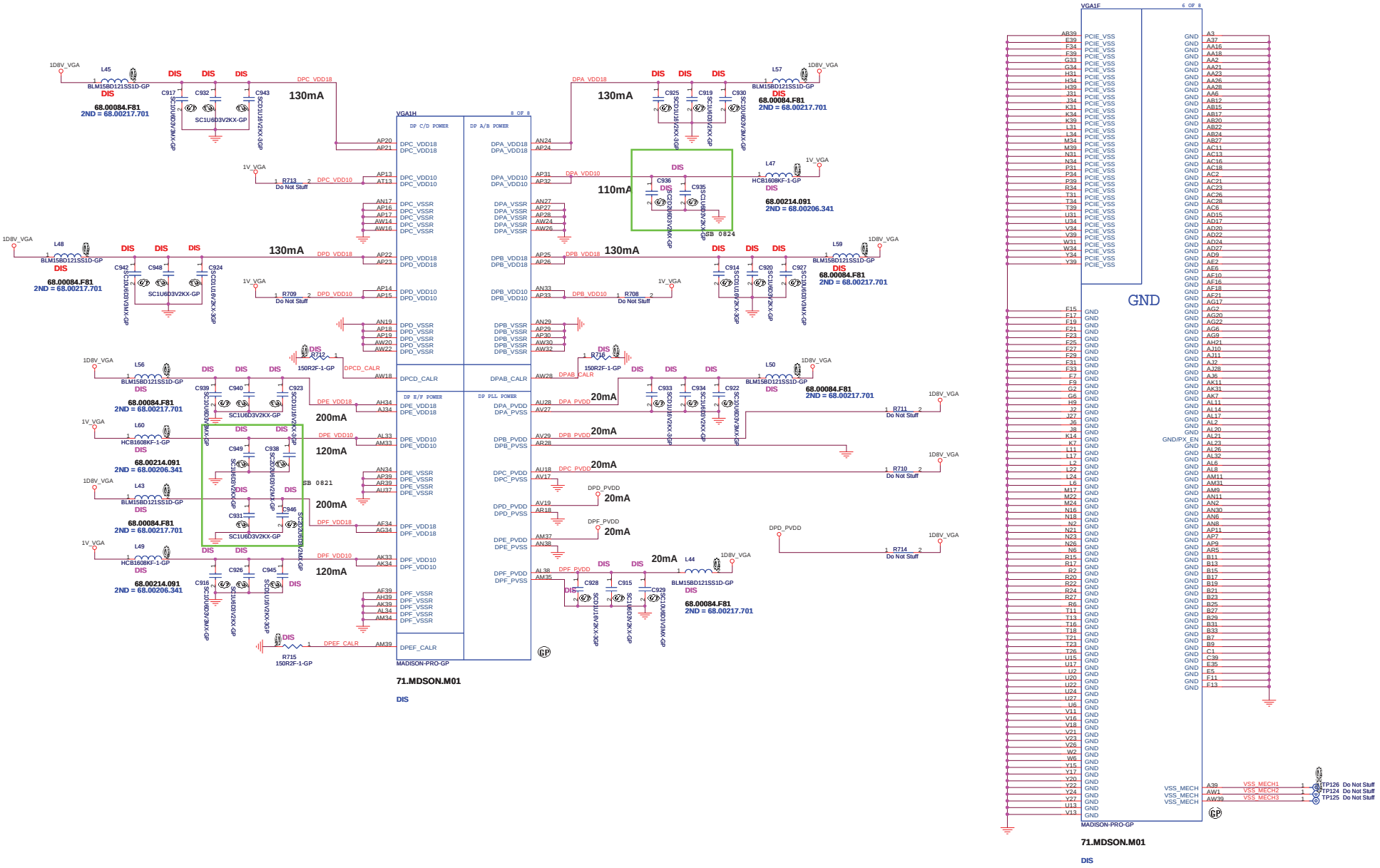
ENG DIS MADSION SAMSUNG

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Madison POWER

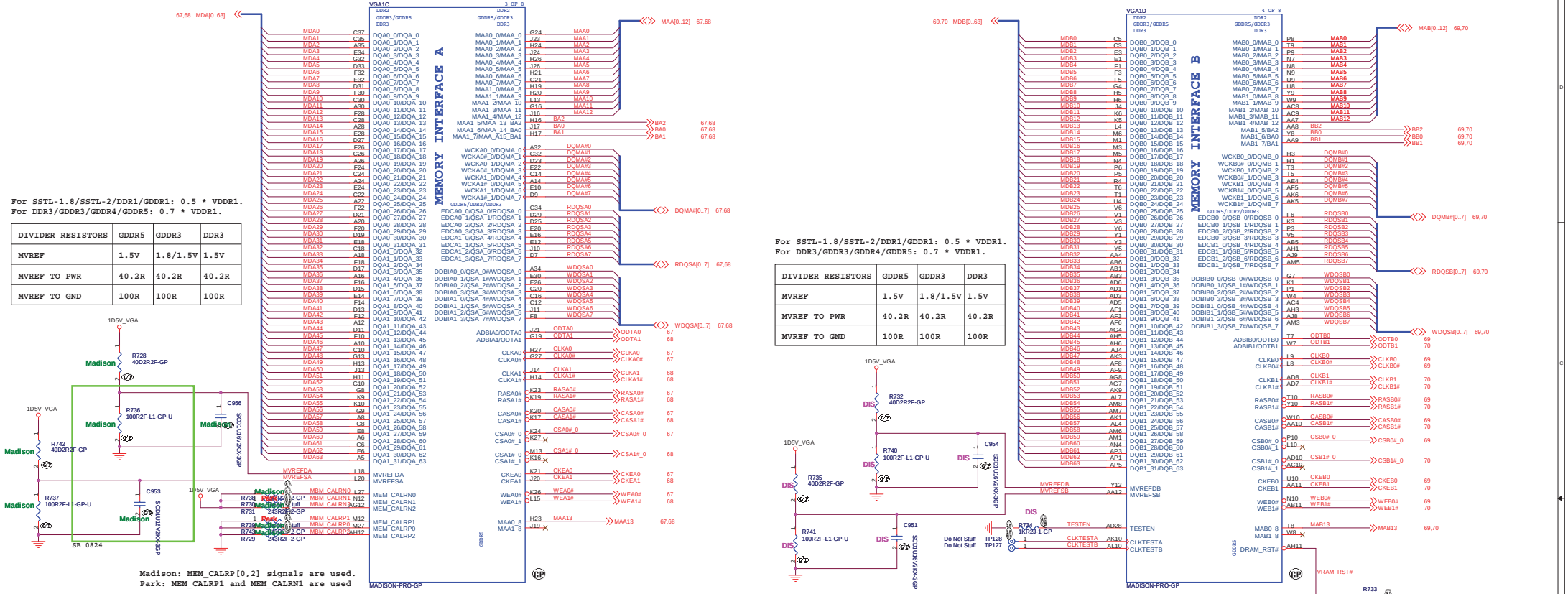
Size: A2 | Document Number: JV50-CP | Rev: SB

Date: Wednesday, August 26, 2009 | Sheet 64 of 68



ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DP POWER_GND**
Size: A2	Document Number: **JV50-CP**
Rev: **SB**	
Date: Wednesday, August 26, 2009	Sheet 65 of 68



STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	X
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	X
RESERVED	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RESERVED	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
VIP_DEVICE_STRAP_ENA (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
RSVD	V2SYNC		0
RSVD	H2SYNC		0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	X X

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC, GPIO2, GPIO21

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

Designator	For M97-M2	For Mannhatton
R_MEM_1	10K	10K
R_MEM_2	40R/Short	680R
R_MEM_3	DY	DY
C_MEM	2.2nF	68pF

ENG DIS MADSION SAMSUNG

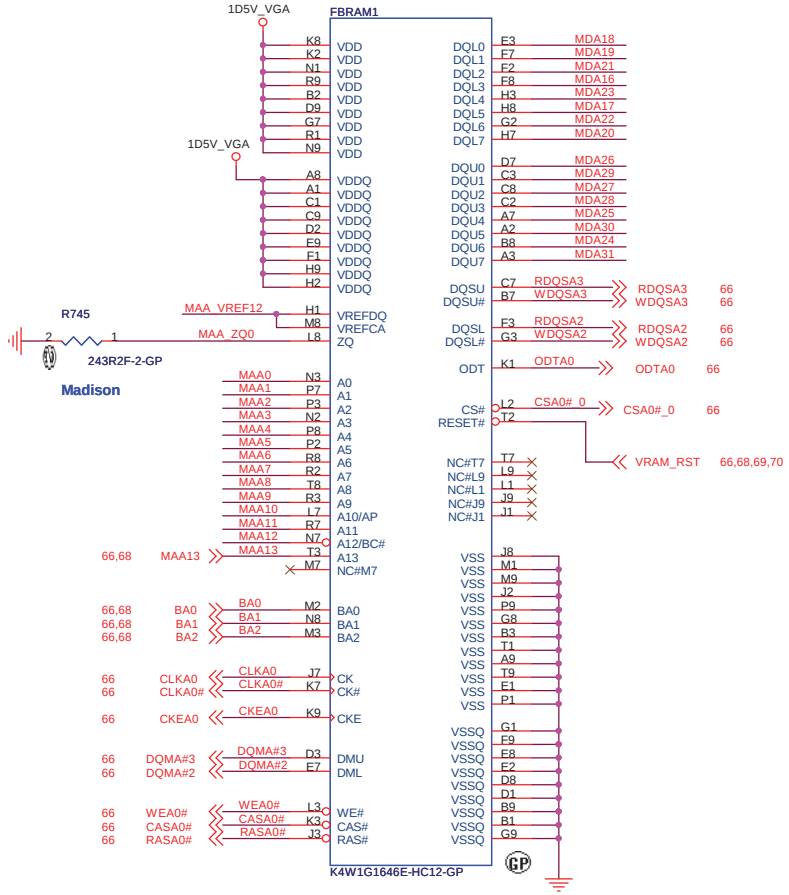
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

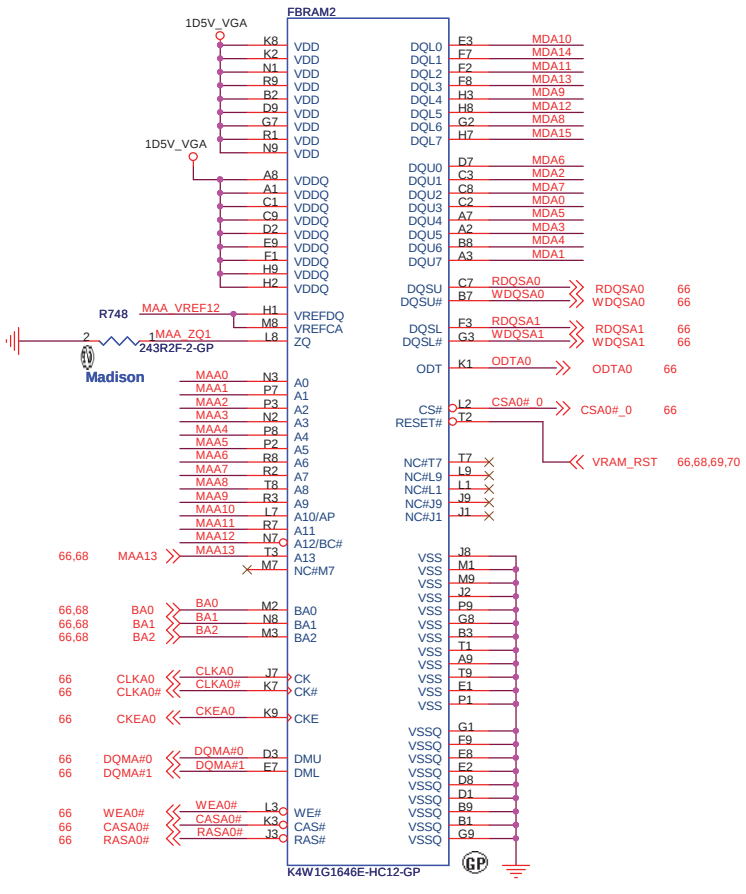
Title: Madison Memory / Straps

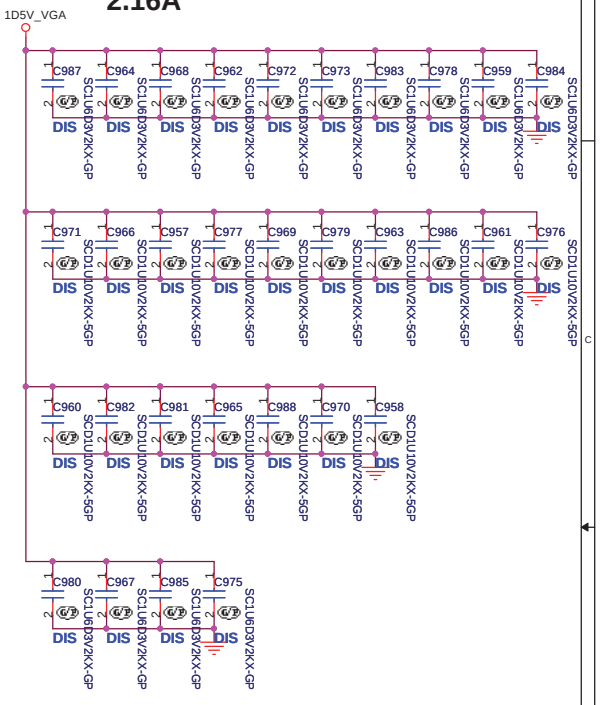
Size: A2 | Document Number: JV50-CP | Rev: SB

Date: Thursday, September 03, 2009 | Sheet 66 of 68

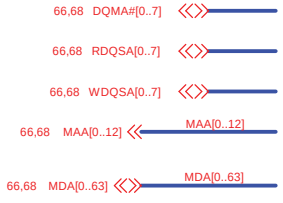
DDR3

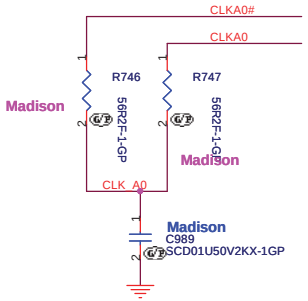


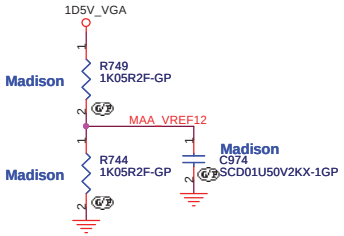




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



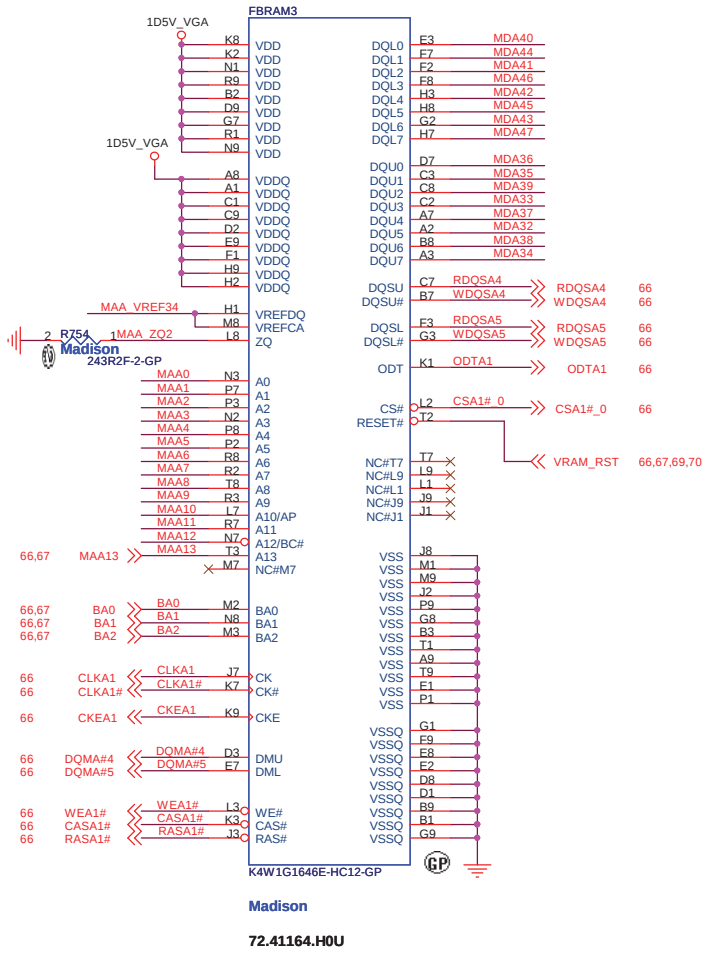


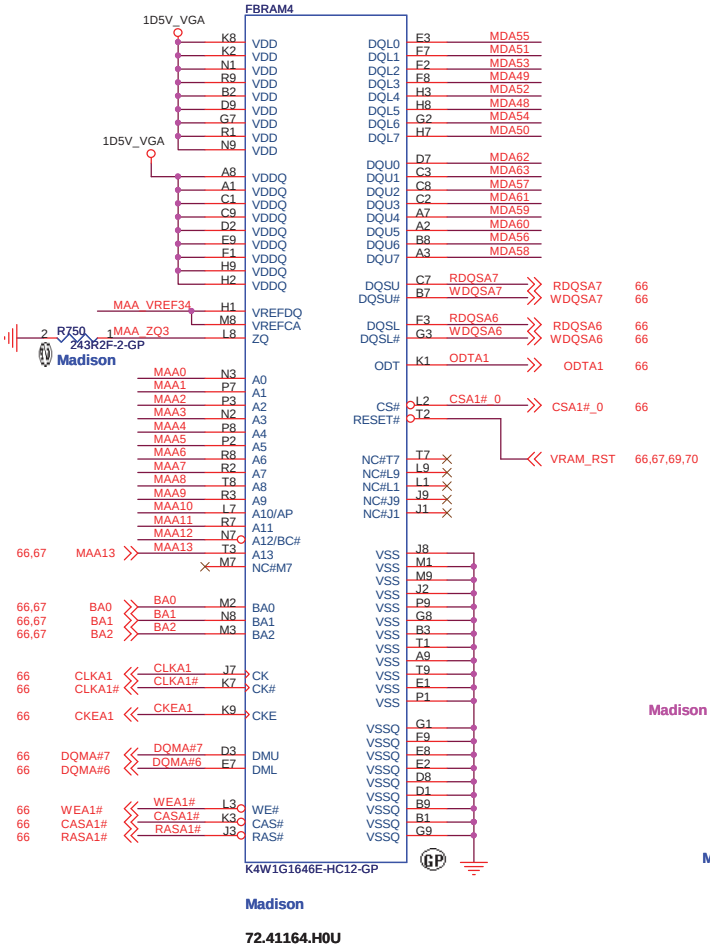


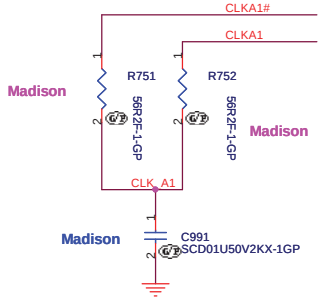
ENG DIS MADSION SAMSUNG

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VRAM(1/4)***	
Size A3	Document Number **JV50-CP**	Rev **SB**
Date: Thursday, September 03, 2009	Sheet 67 of 68	

DDR3

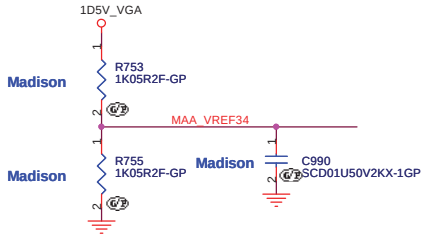






SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

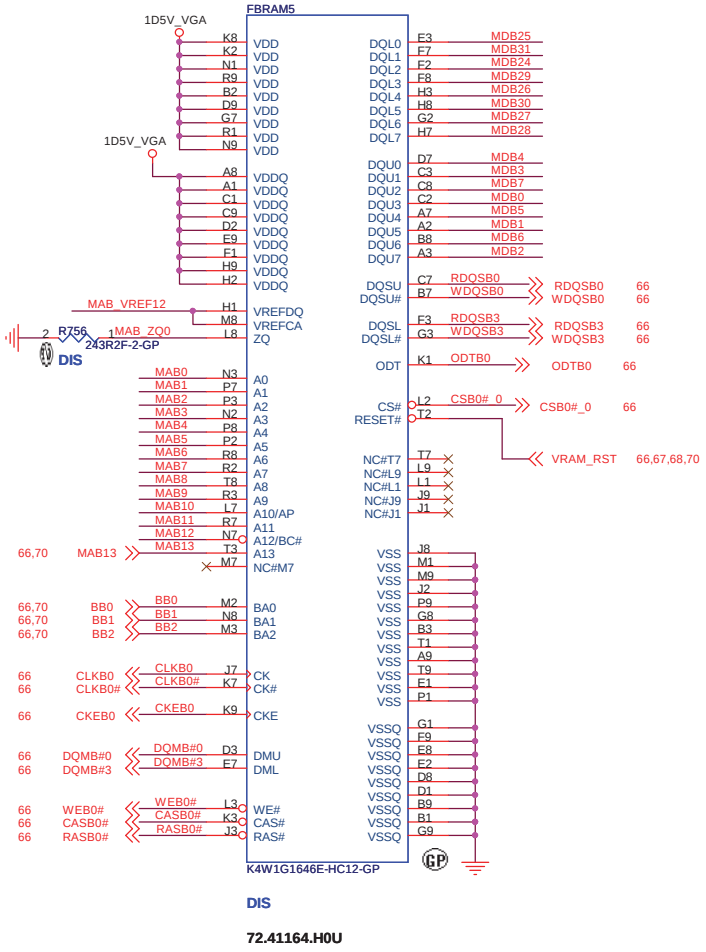
66,67 DQMA#[0..7]
66,67 RDQSA[0..7]
66,67 WDQSA[0..7]
66,67 MAA[0..12] MAA[0..12]
66,67 MDA[0..63] MDA[0..63]

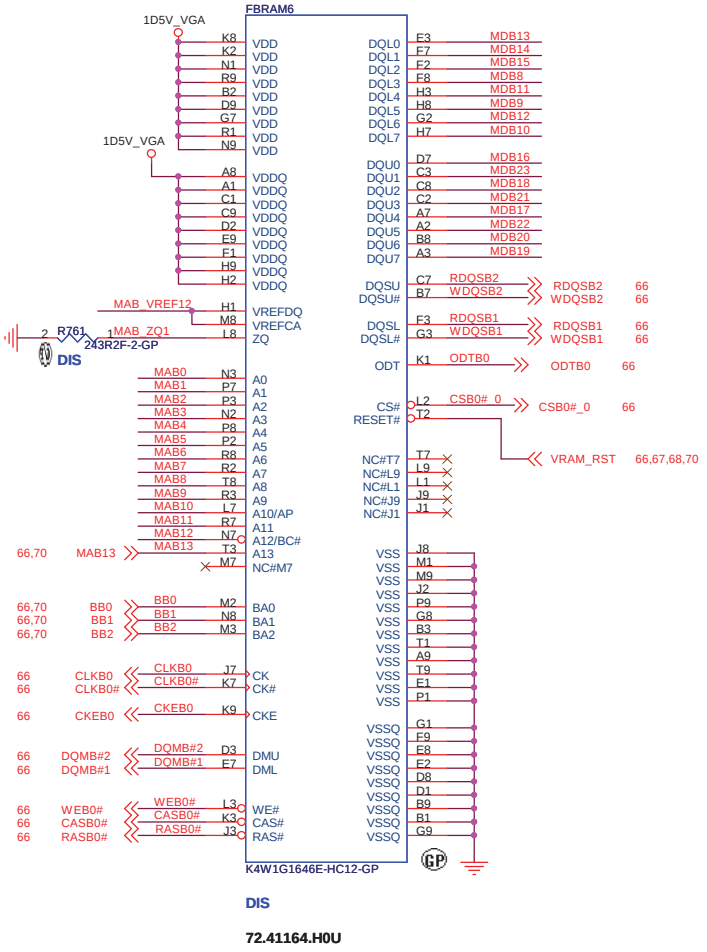


ENG DIS MADSION SAMSUNG

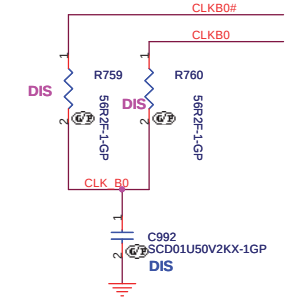
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/4)*		
Size: A3	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 68 of 68	

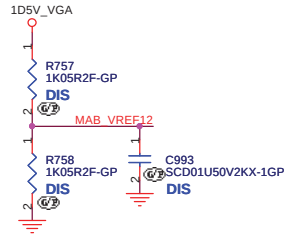
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



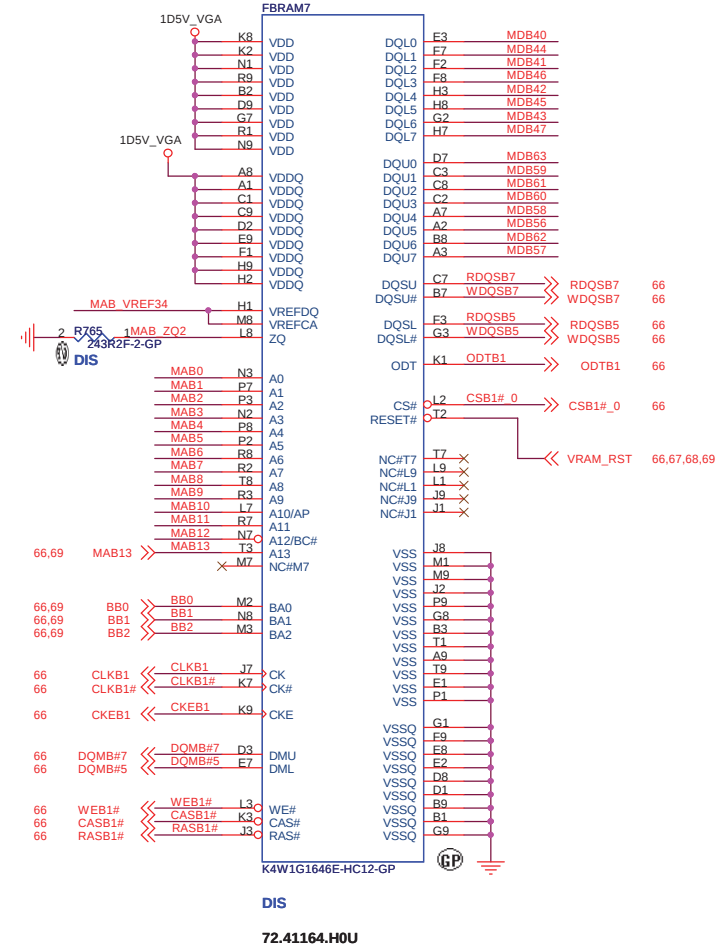


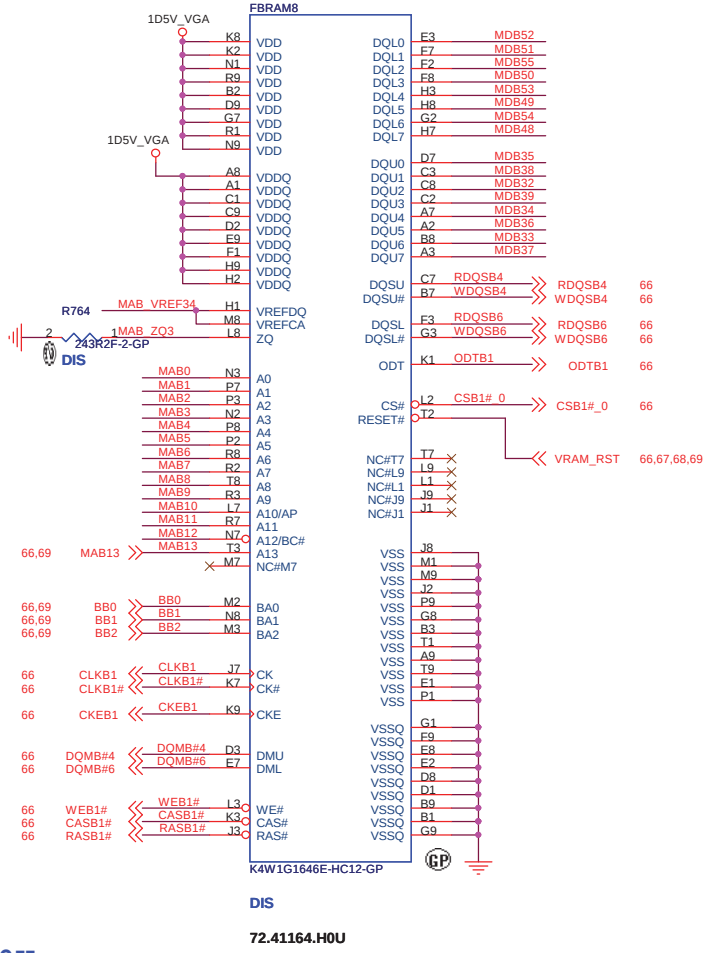
66,70 DQMB#[0..7]
66,70 RDQSB[0..7]
66,70 WDQSB[0..7]
66,70 MAB[0..12] MAB[0..12]
66,70 MDB[0..63] MDB[0..63]

ENG DIS MADSION SAMSUNG

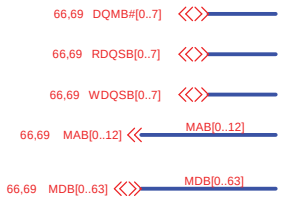
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(3/4)		
Size: A3	Document Number: JV50-CP	Rev: SB
Date: Thursday, September 03, 2009	Sheet 69 of 68	

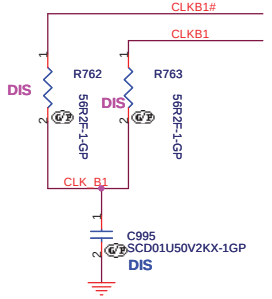
DDR3

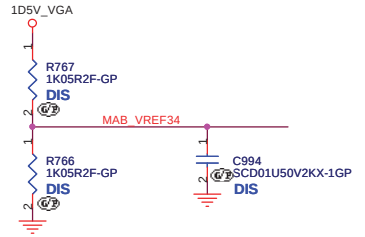




SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U







ENG DIS MADSION SAMSUNG

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