

Compal Confidential

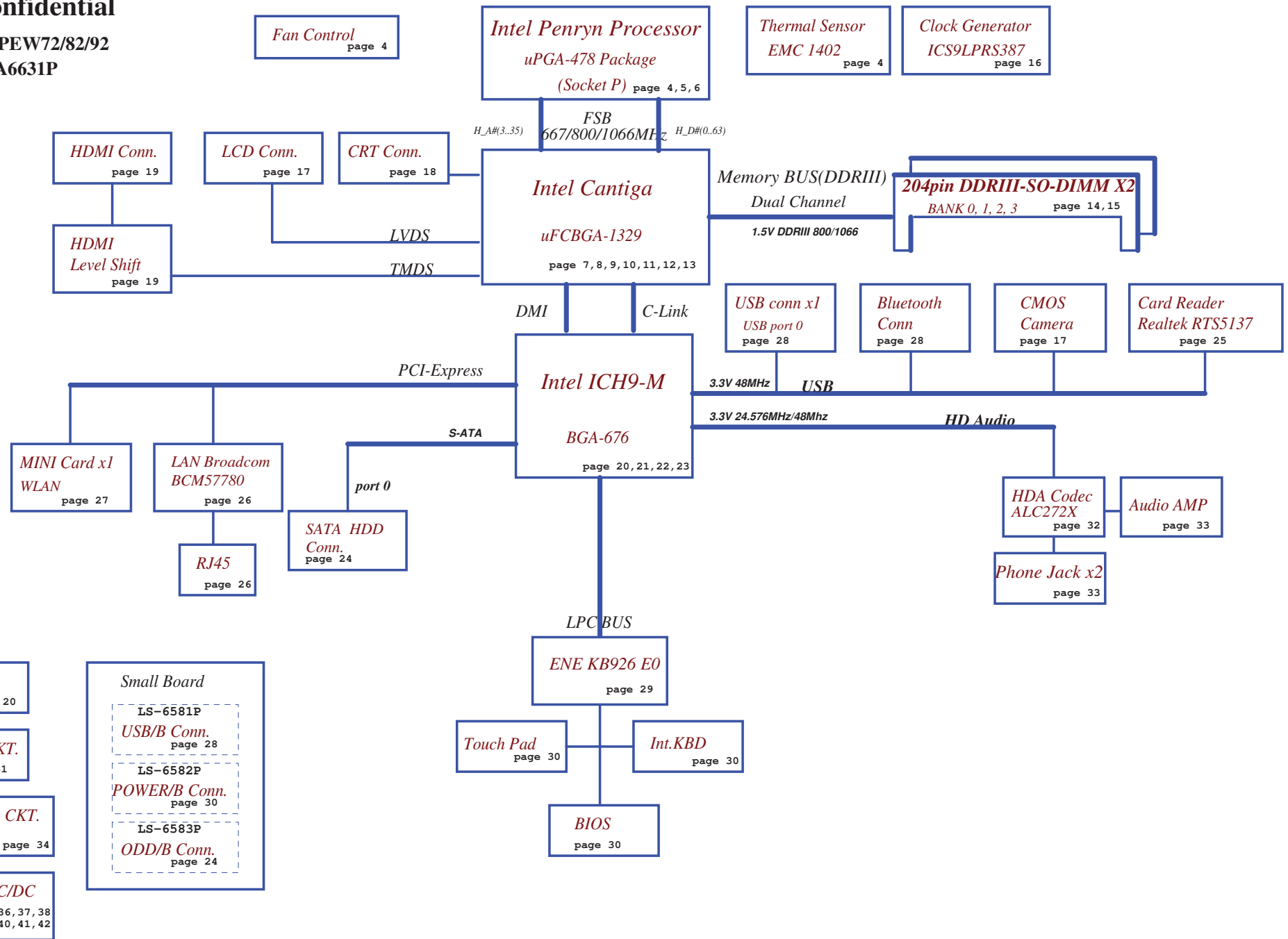
PEW72/82/92 M/B Schematics Document

Intel Penryn Processor with Cantiga + DDRIII + ICH9M

2010-07-09
REV: 1.0

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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	Cover Page
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				PEW72/82 M/B LA-6631P Schematic	1.0
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Model Name : PEW72/82/92
File Name : LA6631P



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.75VS	0.75V power rail for DDR	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for DDR	ON	ON	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for LVDS	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSb always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
--------	--------	-----------	------------

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	SMSC EMC1402	100 1100 b

EC SM Bus2 address

ICH9M SM Bus address

Device	Address
Clock Generator (ICS9LVRS367, RTM890N)	1101 001Xb
DDR DIMM1	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
GM45 B3	GM@
GM45 A1	GMA1@
GL40 B3	GL@
GM40 A1	GLA1@
Bluetooth	BT@

PCIE table

PCIE port1	
PCIE port2	Wireless Card
PCIE port3	PCIE LAN
PCIE port4	
PCIE port5	
PCIE port6	

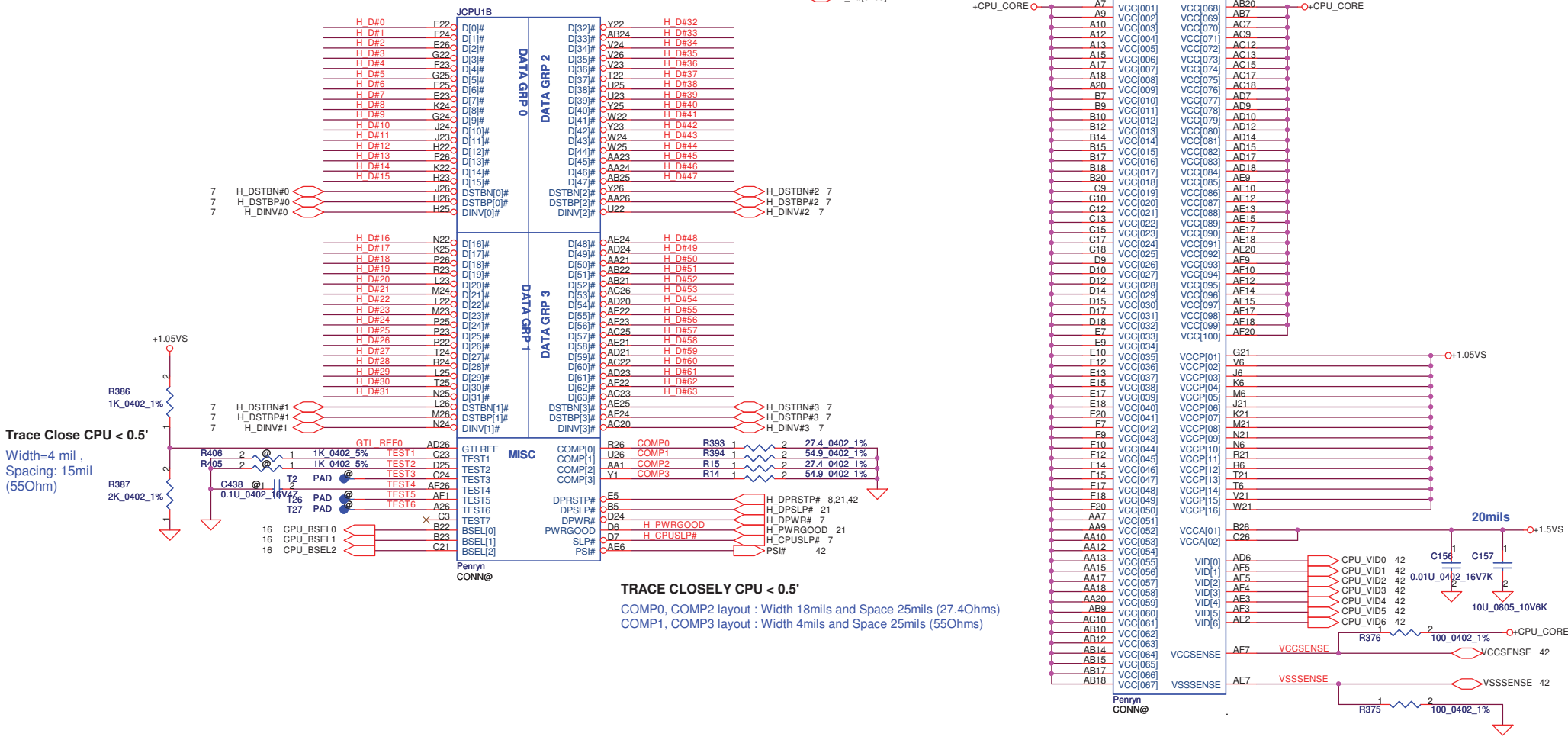
SATA table

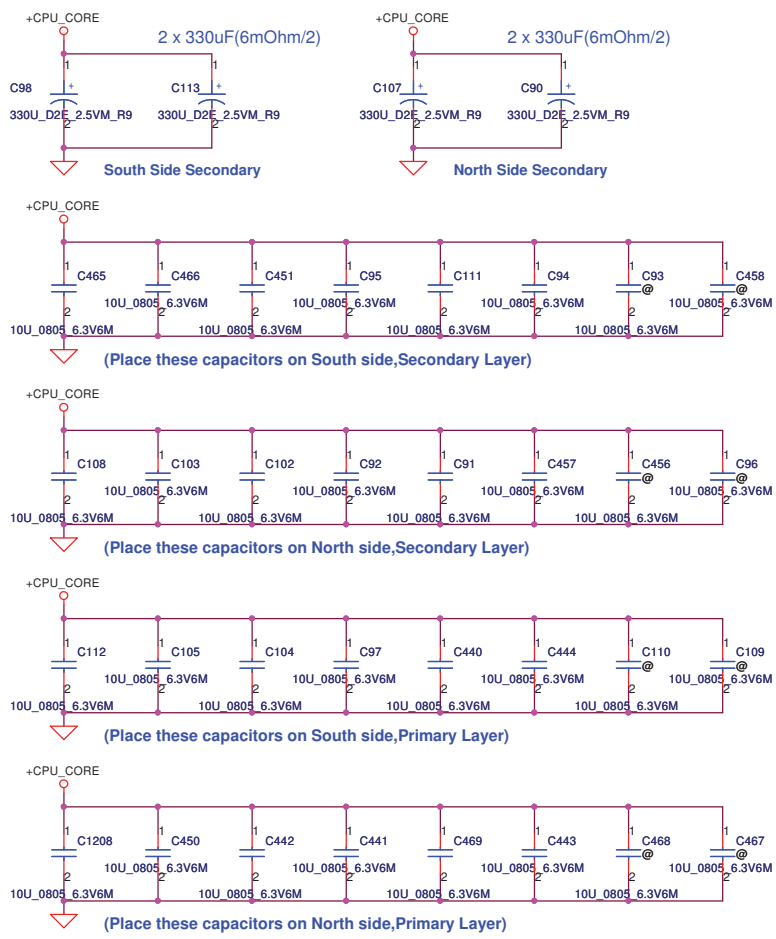
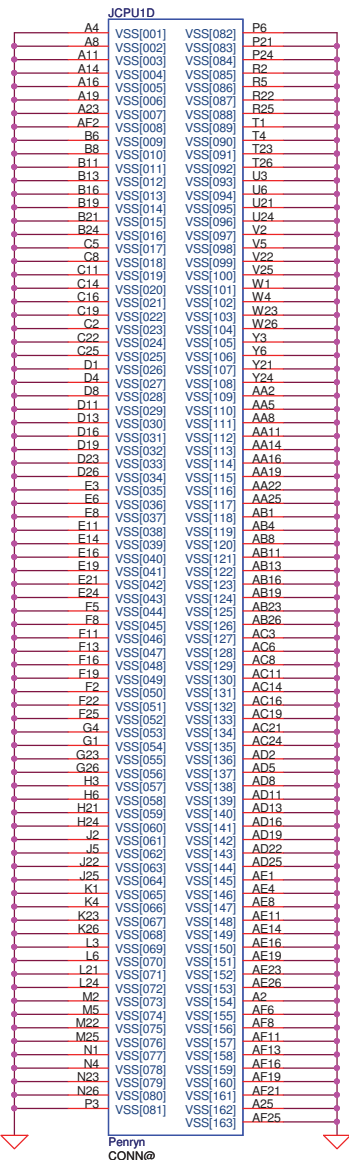
SATA port0	HDD
SATA port1	ODD
SATA port2	
SATA port3	
SATA port4	
SATA port5	

USB table

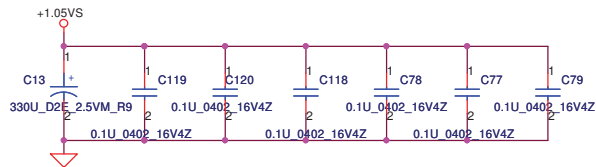
EHCI1	UHCI1	Port0	MB USB Conn.
		Port1	USB/B Conn.
		Port2	
	UHCI2	Port3	CMOS Camera
		Port4	Card Reader
EHCI2	UHCI3	Port5	
		Port6	USB/B Conn.
	UHCI4	Port7	
		Port8	Blue Tooth
	UHCI5	Port9	
		Port10	Wireless Card
	UHCI6	Port11	

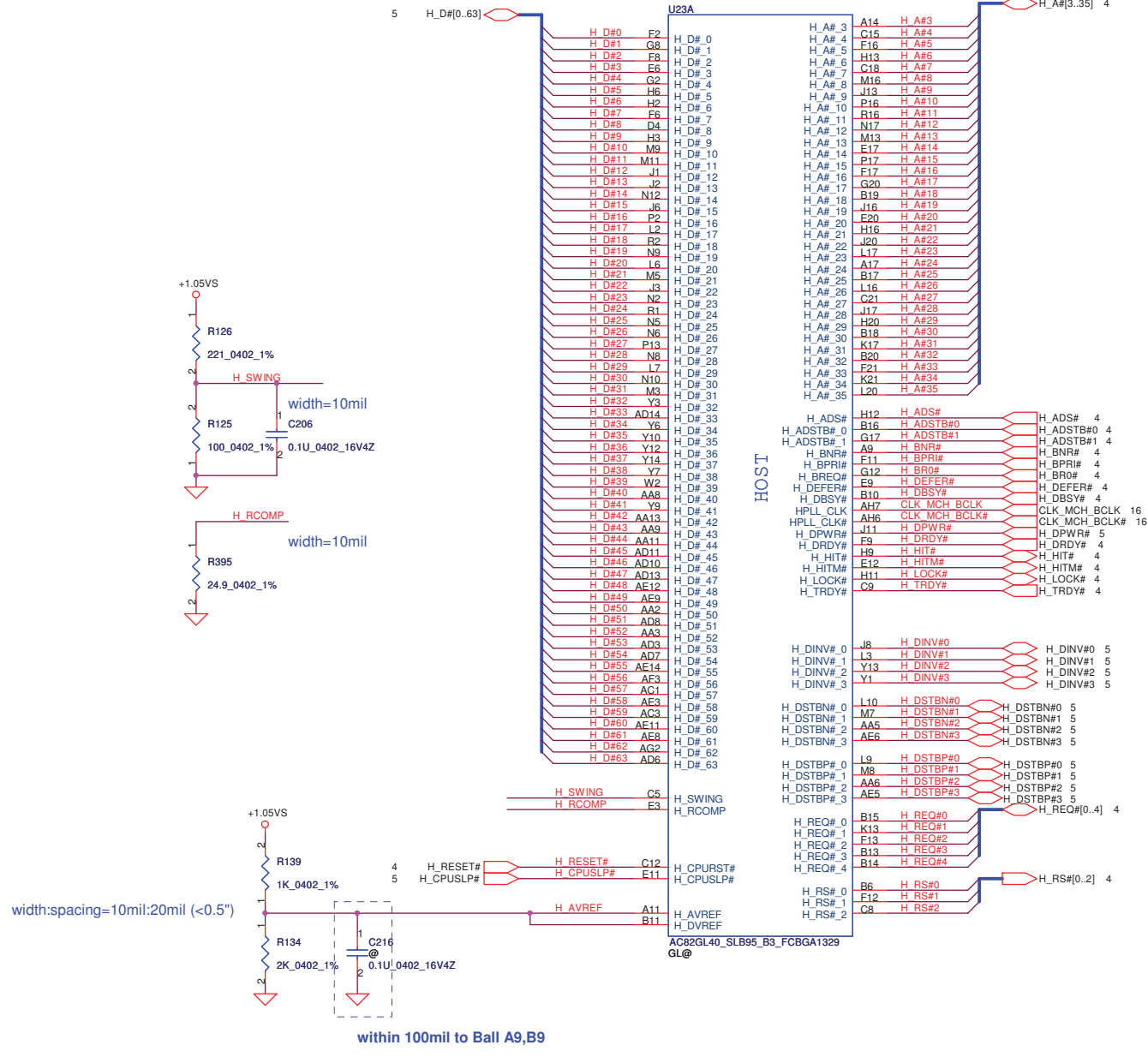
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+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP, Polymer	4X330uF	6m ohm/4	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32
	32X10uF	3m ohm/32	0.6nH/32



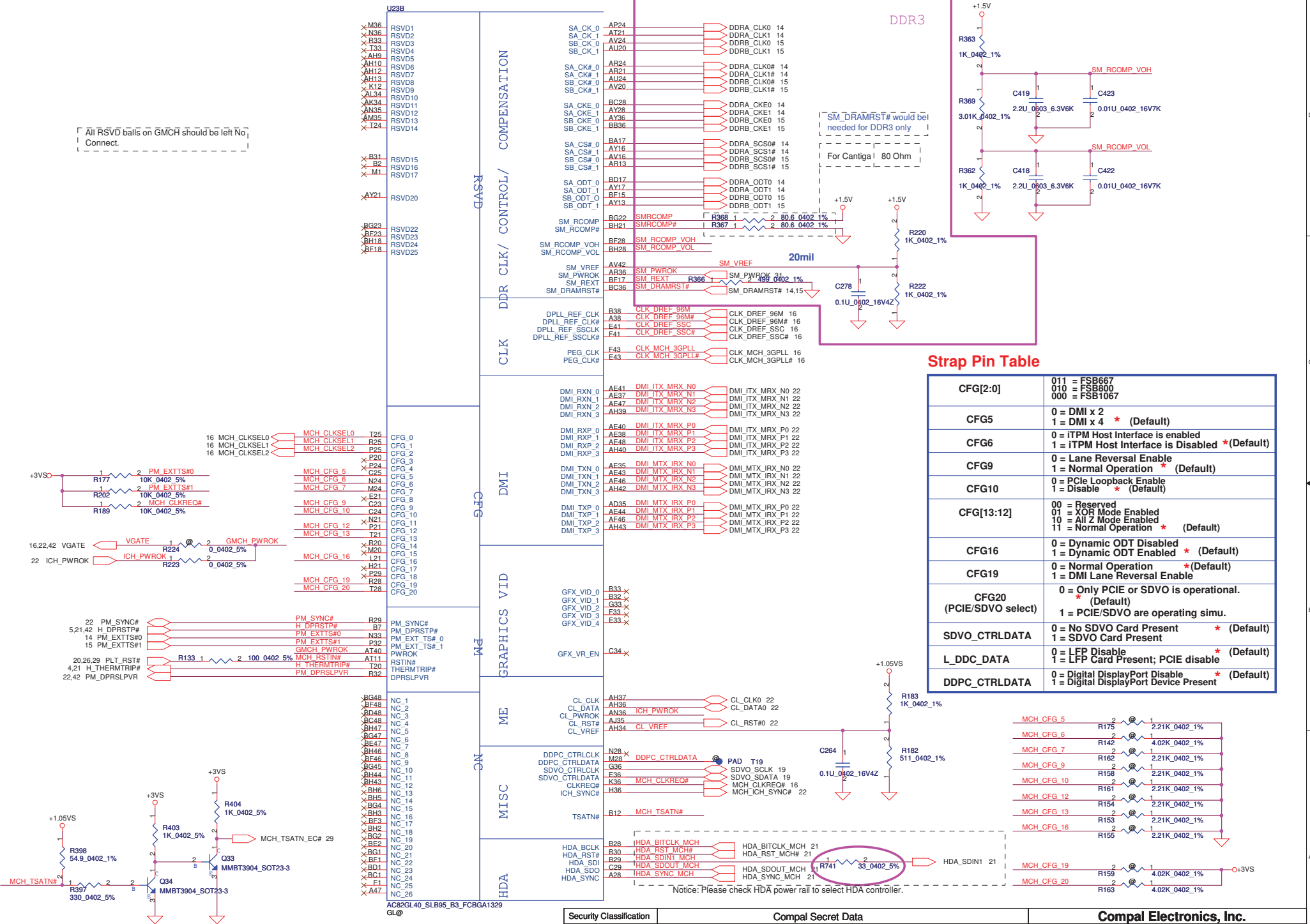


U23
AC82GM45_SLB94_B3_FCBGA1329
GM@

U23
AC82GL40_SLGGM_A1_FCBGA1329
GLA1@

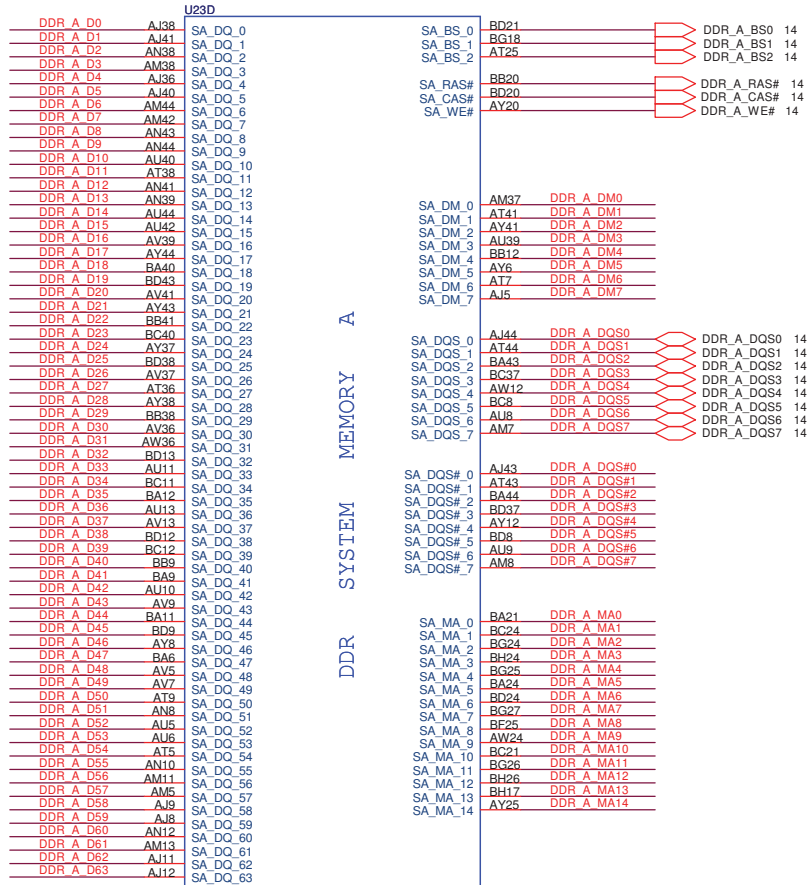
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All RSVD balls on GMCH should be left No Connect.

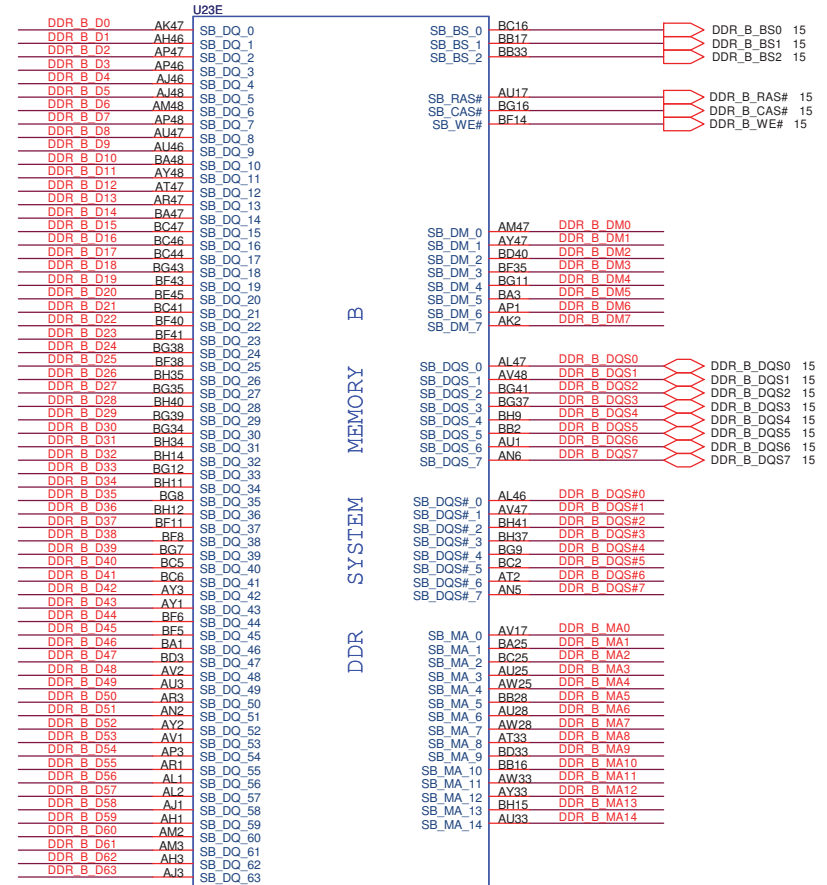


Strap Pin Table

CFG[2:0]	011 = FSB667 010 = FSB800 000 = FSB1067
CFG5	0 = DMI x 2 1 = DMI x 4 * (Default)
CFG6	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is Disabled * (Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation * (Default)
CFG10	0 = PCIe Loopback Enable 1 = Disable * (Default)
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation * (Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled * (Default)
CFG19	0 = Normal Operation 1 = DMI Lane Reversal Enable
CFG20 (PCIe/SDVO select)	0 = Only PCIe or SDVO is operational. (Default) 1 = PCIe/SDVO are operating simu.
SDVO_CTRLDATA	0 = No SDVO Card Present 1 = SDVO Card Present * (Default)
L_DDC_DATA	0 = LFP Disable 1 = LFP Card Present; PCIe disable * (Default)
DDPC_CTRLDATA	0 = Digital DisplayPort Disable 1 = Digital DisplayPort Device Present * (Default)

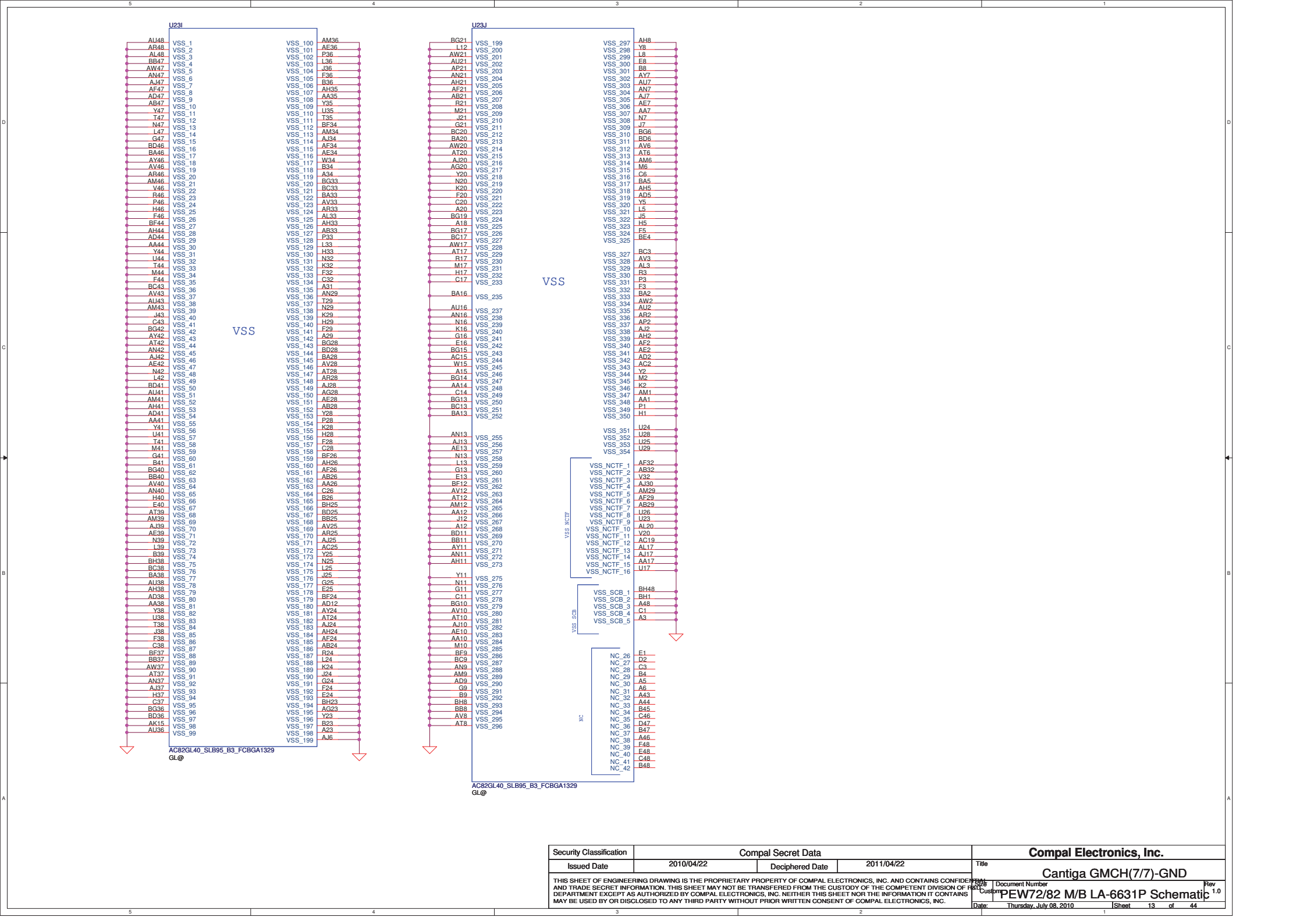


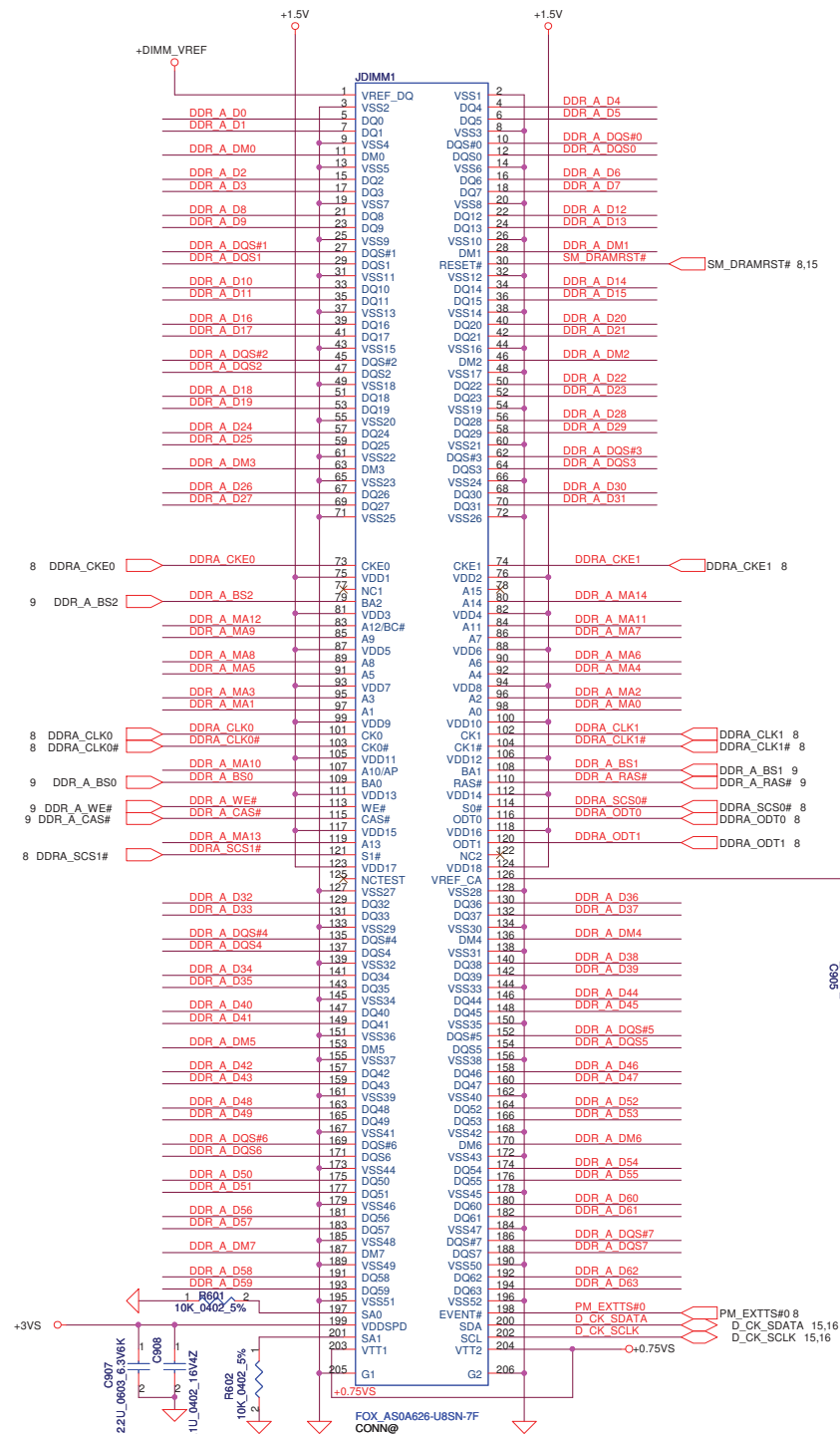
AC82GL40_SLB95_B3_FCBGA1329
GL@



AC82GL40_SLB95_B3_FCBGA1329
GL@

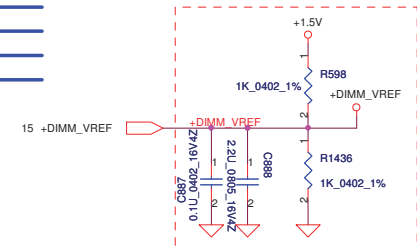
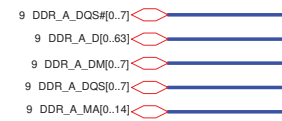
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								Cantiga GMCH(3/7)-DDR	
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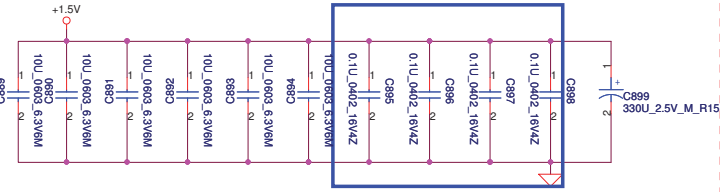
DIMM_A STD H:8mm

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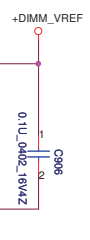
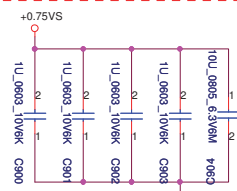


Layout Note:
Place near JDIMM2

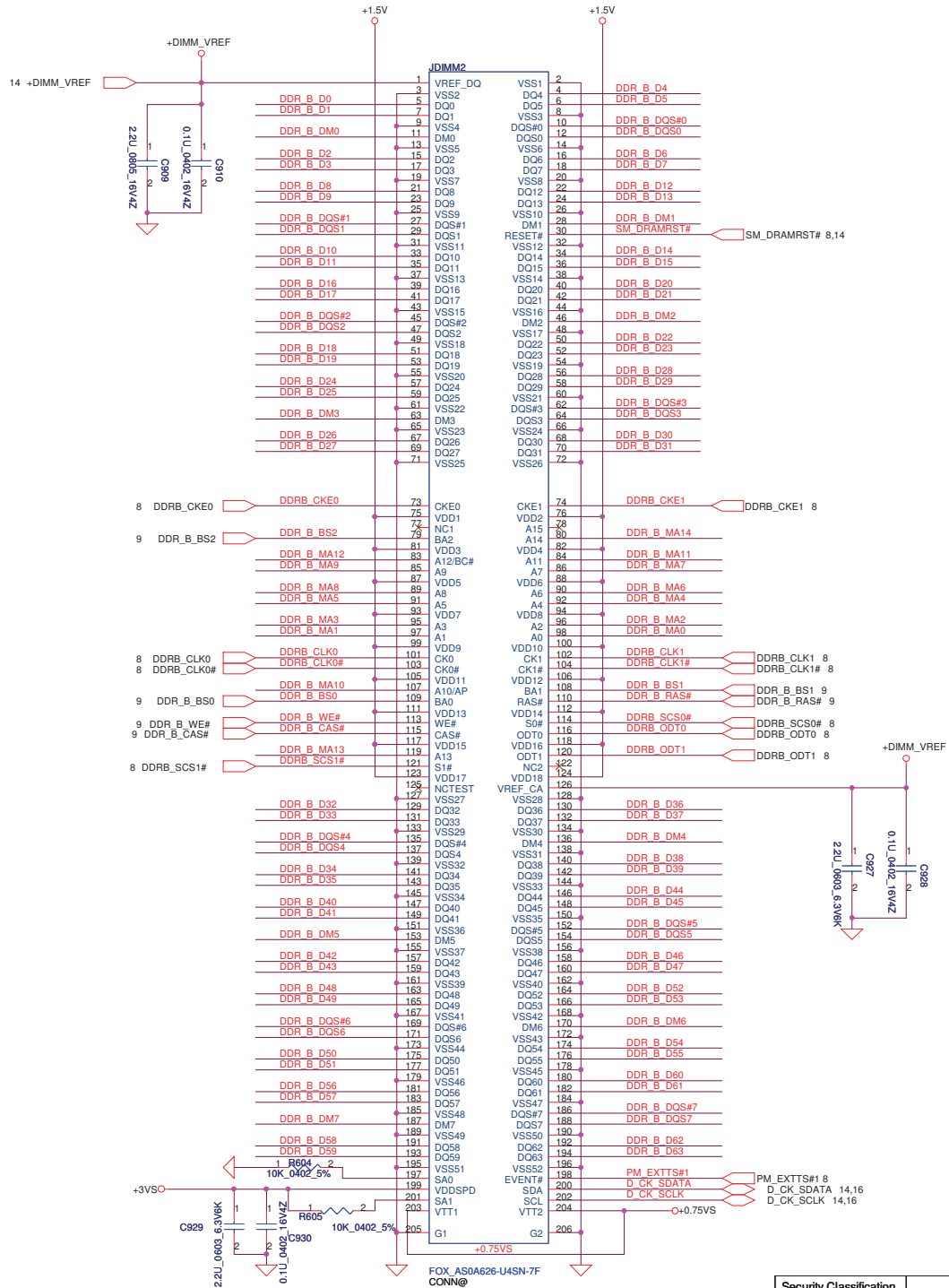
Layout Note: Place these 4 Caps near Command and Control signals of DIMM



Layout Note:
Place near JDIMM2.203 & JDIMM2.204



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Layout Note:
Place near JDIMM1

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

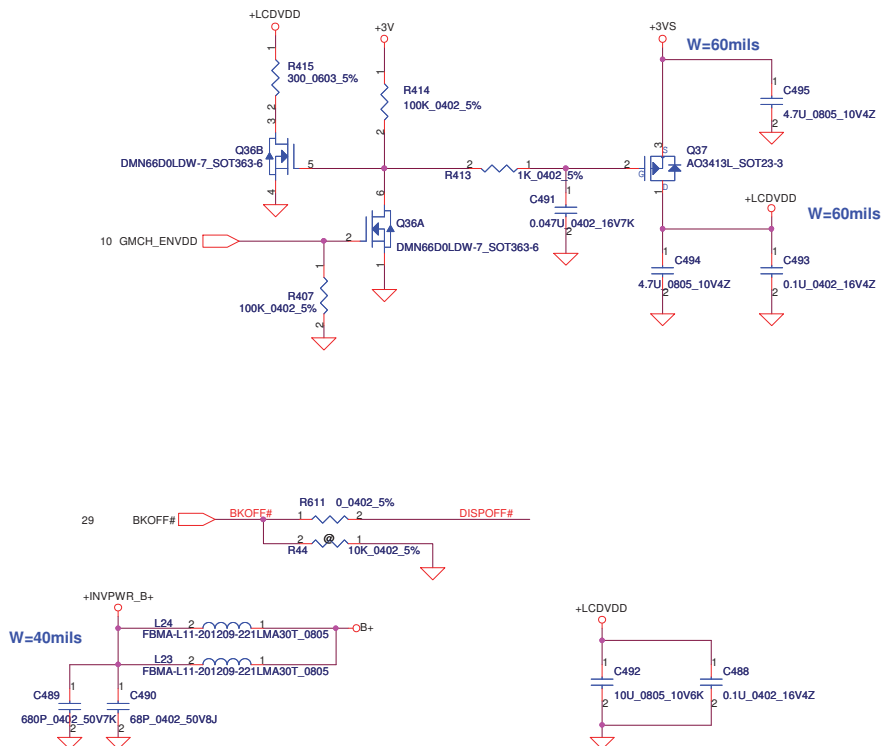
Layout Note:
Place near JDIMM1.203 & JDIMM1.204

9 DDR_B_DQS#[0..7]
9 DDR_B_D[0..63]
9 DDR_B_DM[0..7]
9 DDR_B_DQS#[0..7]
9 DDR_B_MA[0..14]

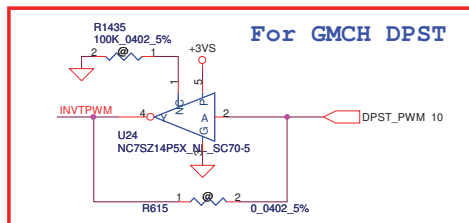
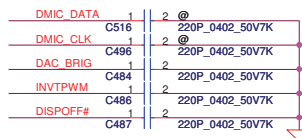
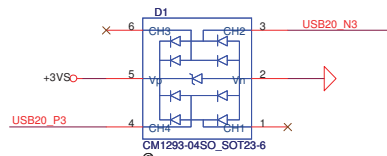
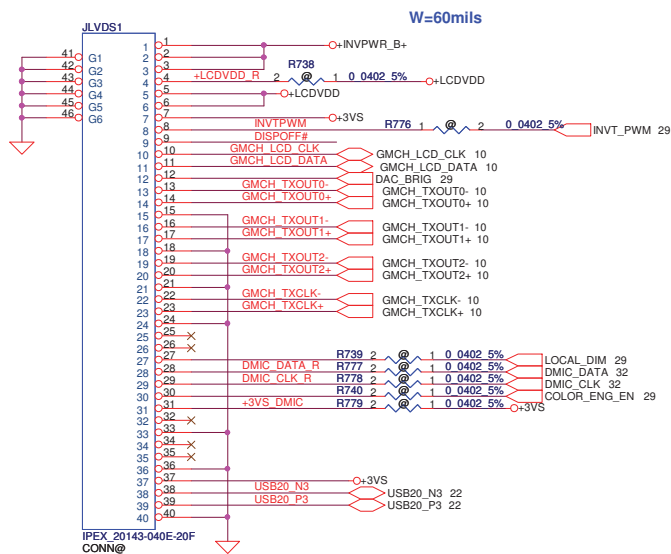
DIMM_B STD H:4mm
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LCD POWER CIRCUIT

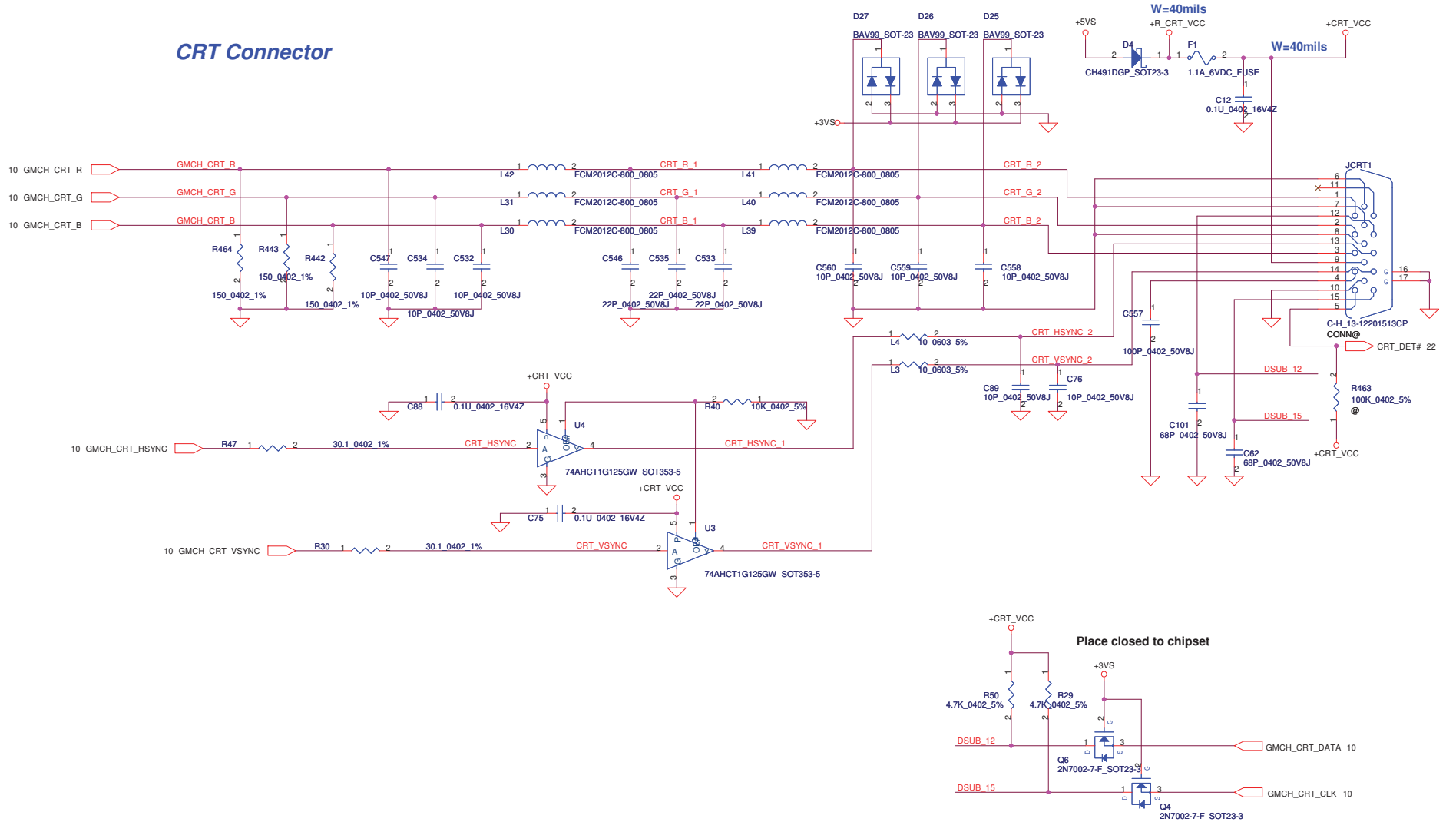


LCD/PANEL BD. Conn.

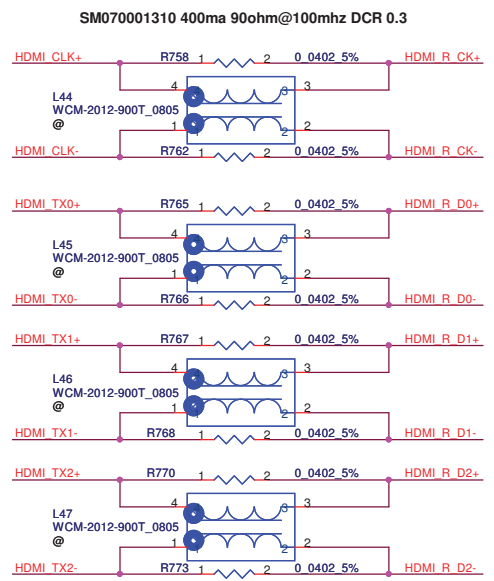
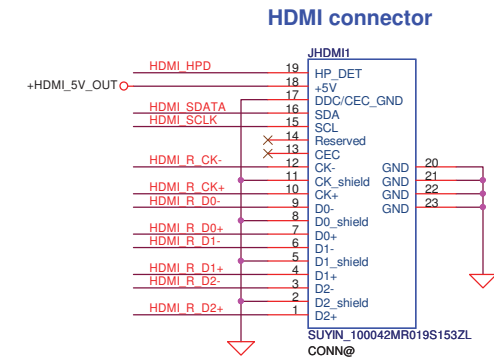
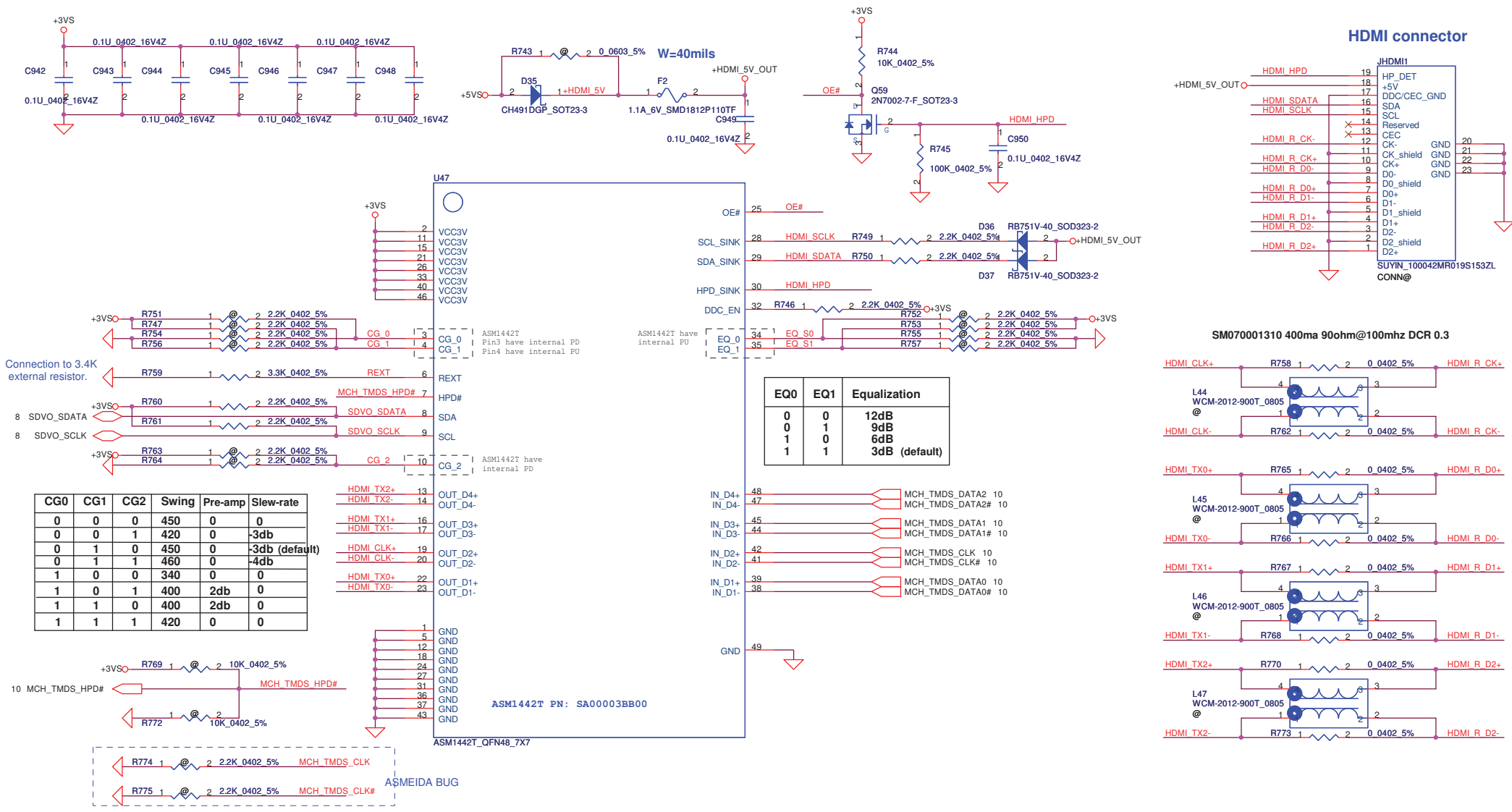


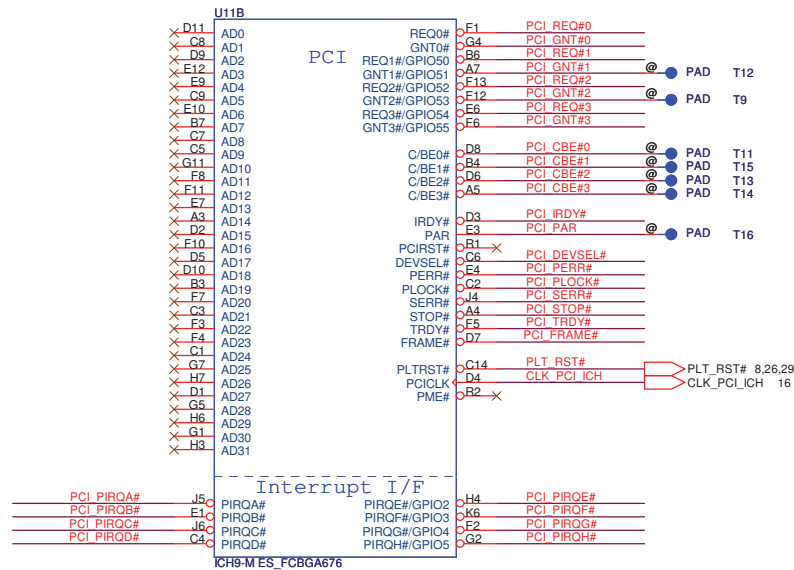
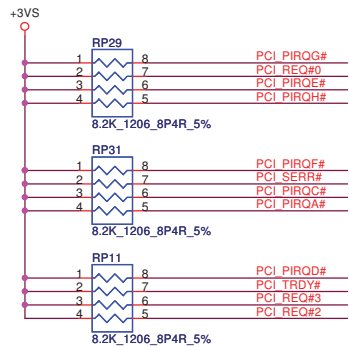
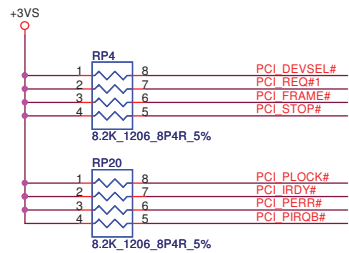
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CRT Connector

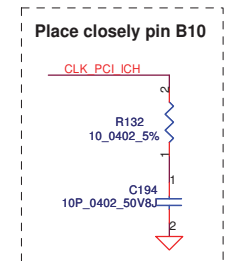


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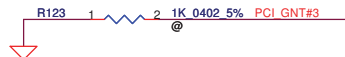




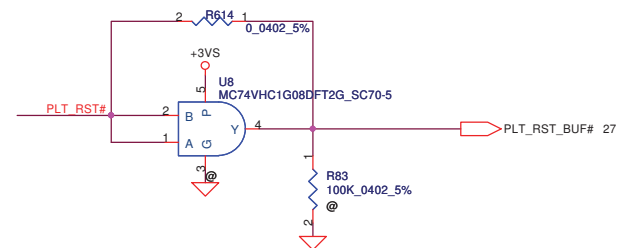
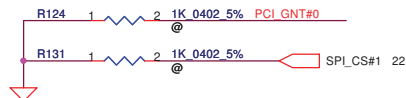
DMI for ESI-compatible operation
PCI_GNT#1 Low= DMI for ESI-compatible operation
 High= Default* (Internal pull-up)

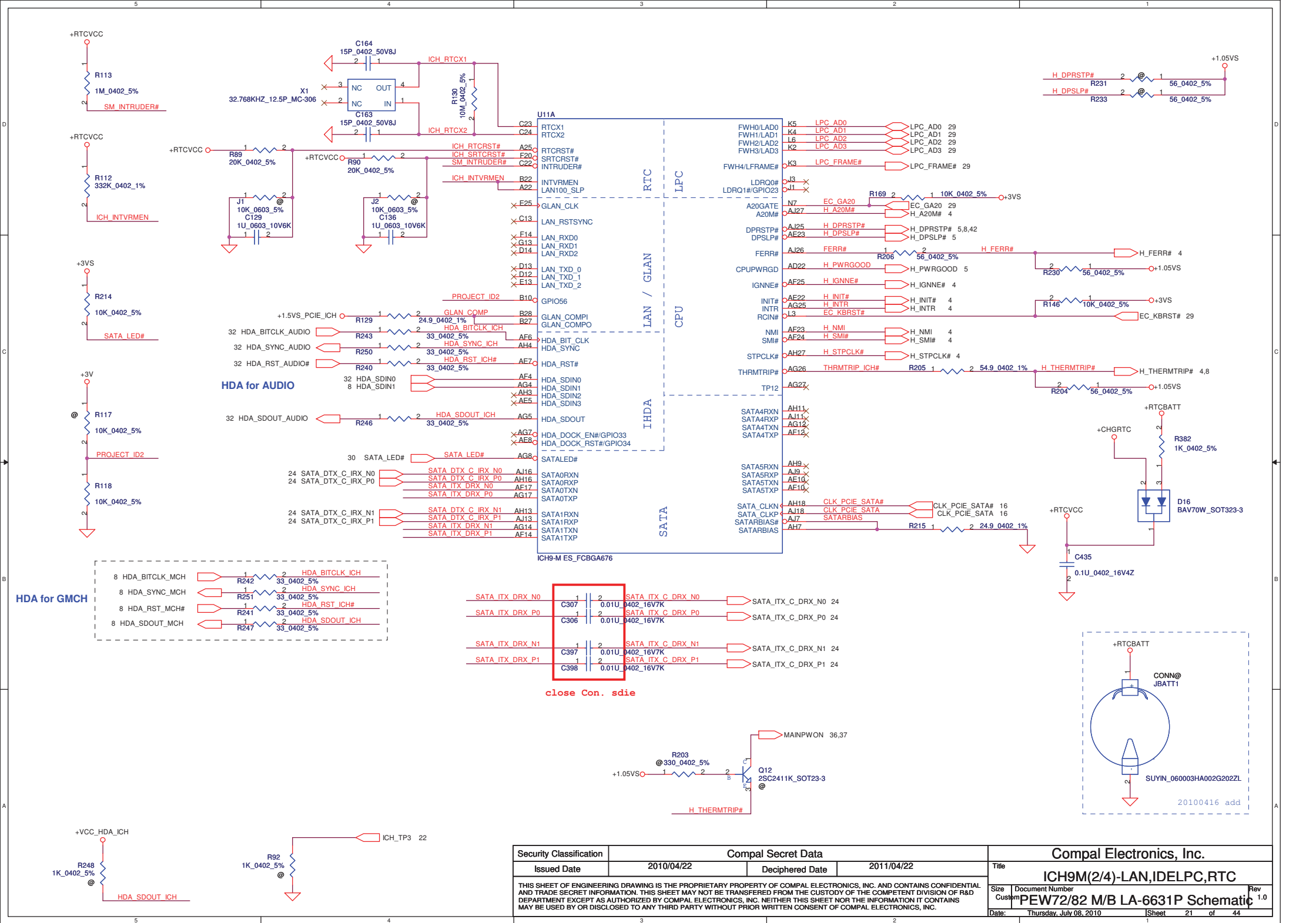


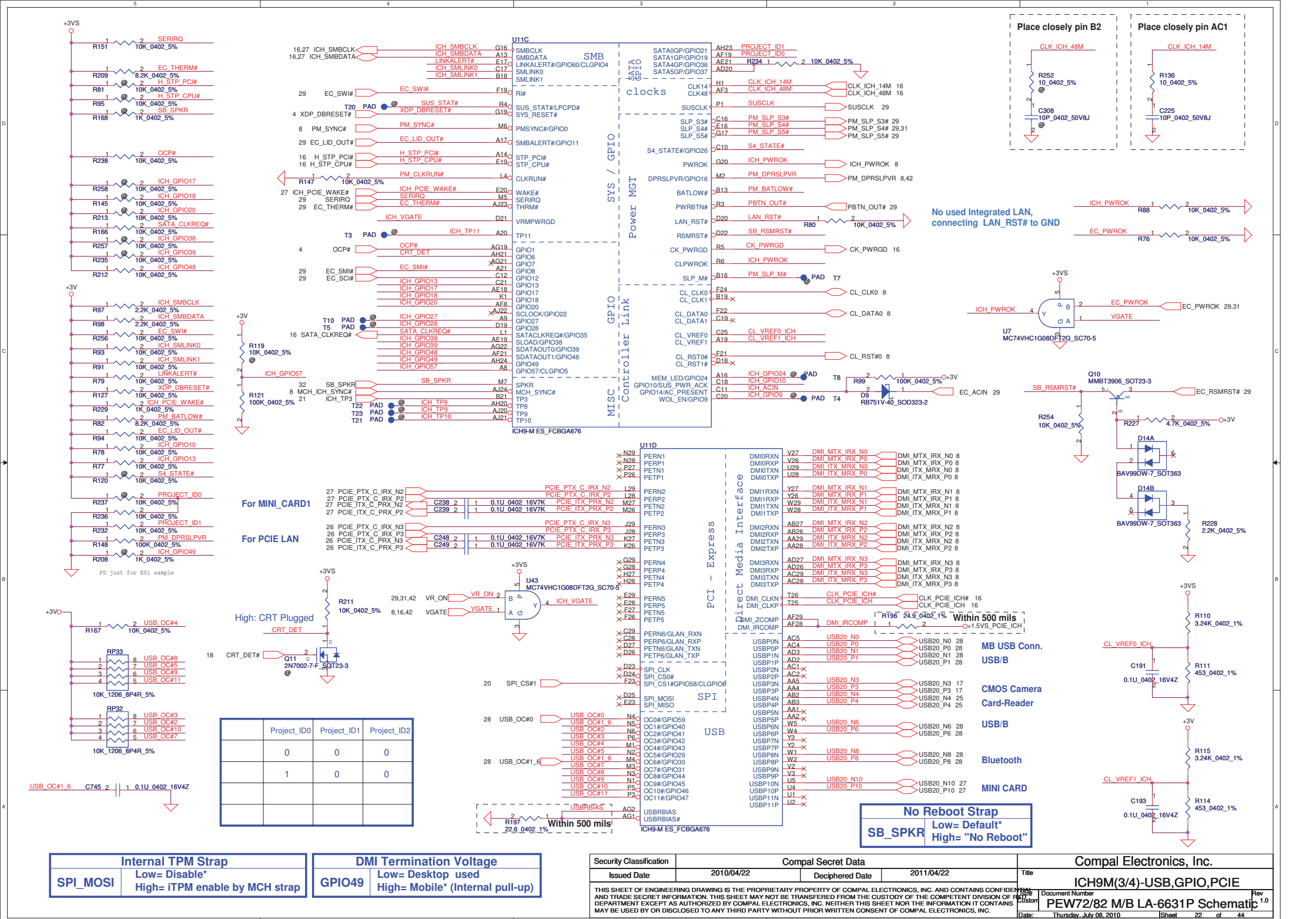
A16 Swap Override Strap
PCI_GNT#3 Low= A16 swap override Enable
 High= Default*

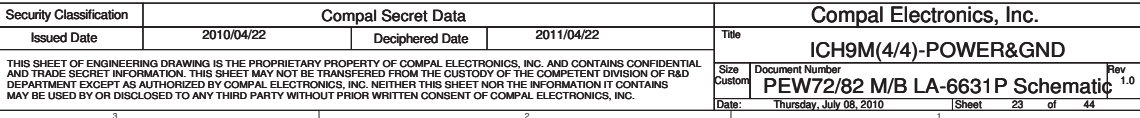


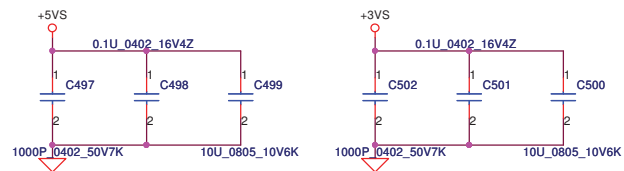
Boot BIOS Strap		
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC*



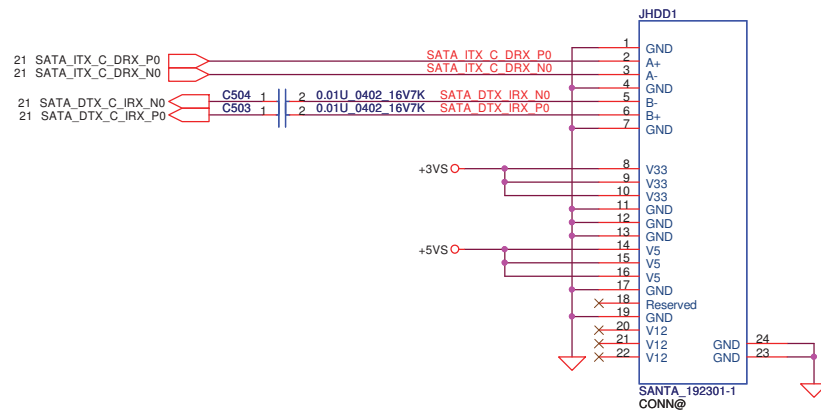




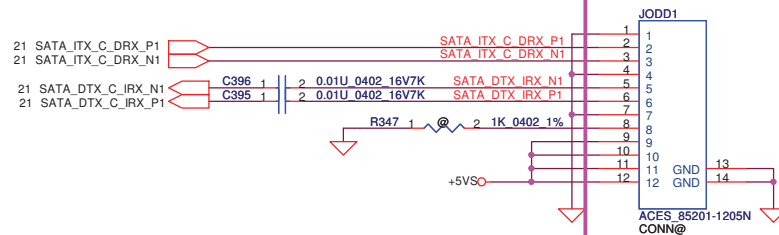




SATA HDD Conn.

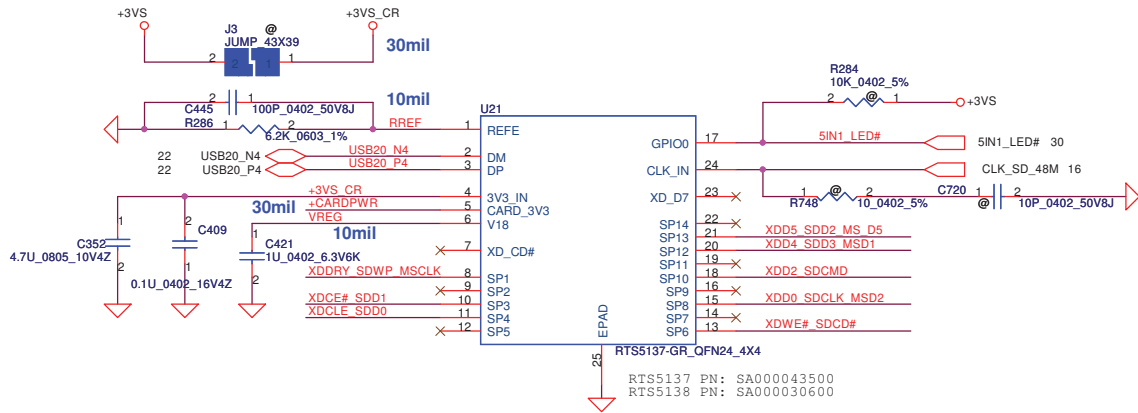


SATA ODD Conn. LS-6583

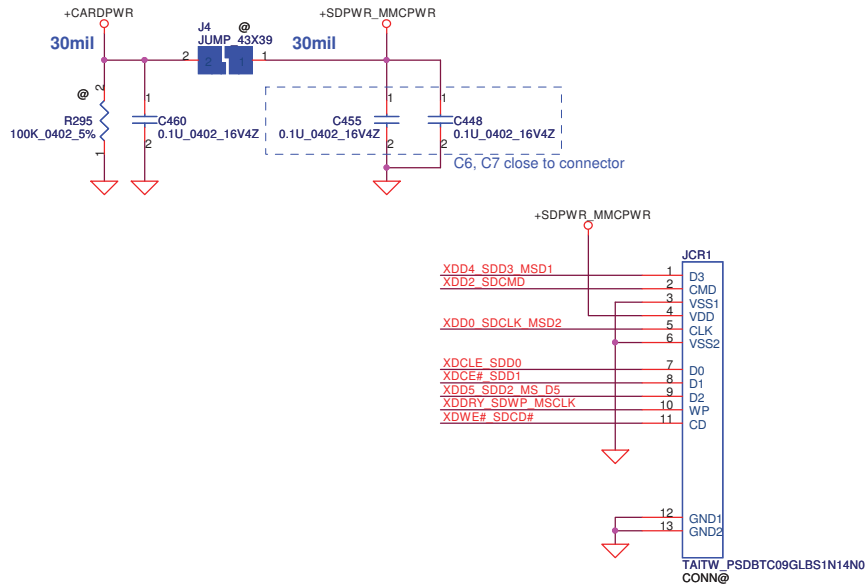


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				Custom		PEW72/82 M/B LA-6631P Schematic		1.0		Thursday, July 08, 2010	
										Sheet 24 of 44	

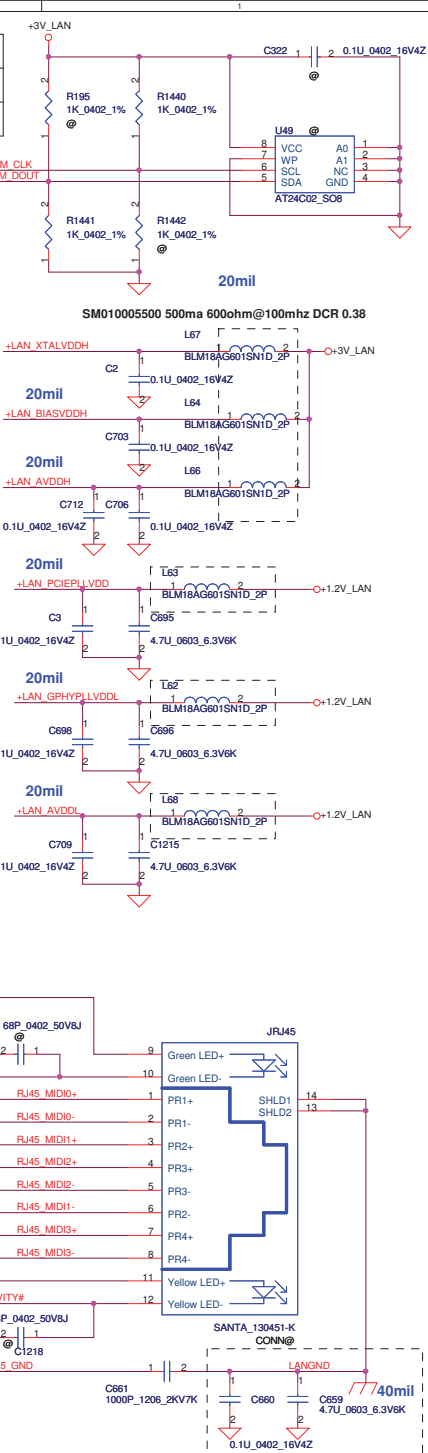
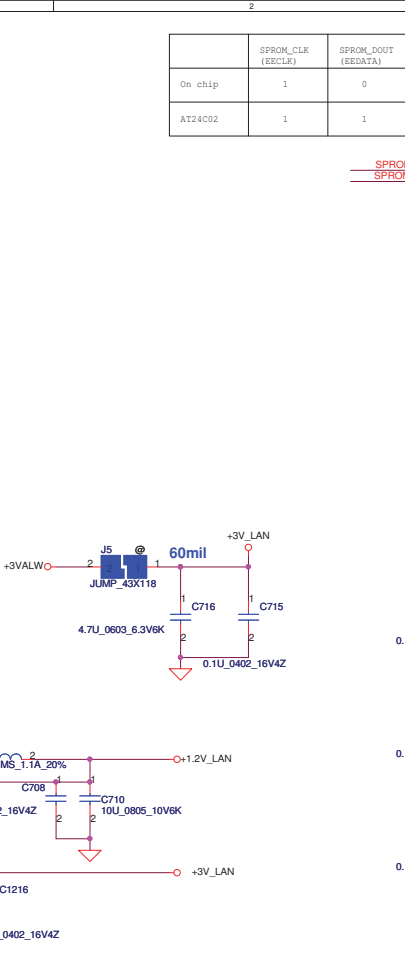
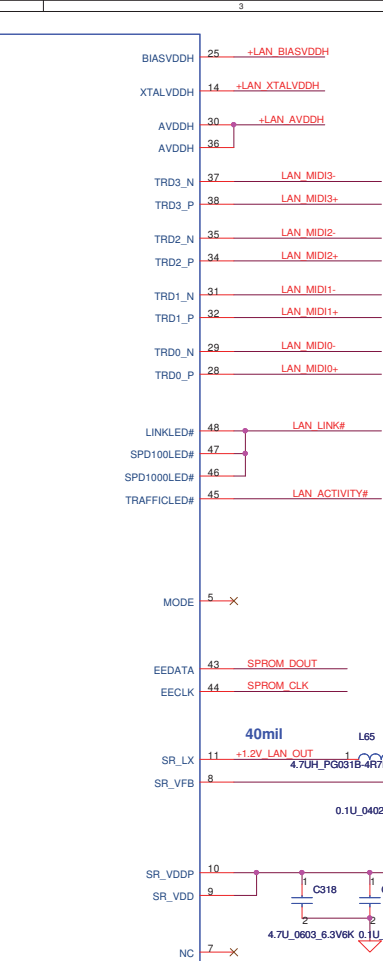
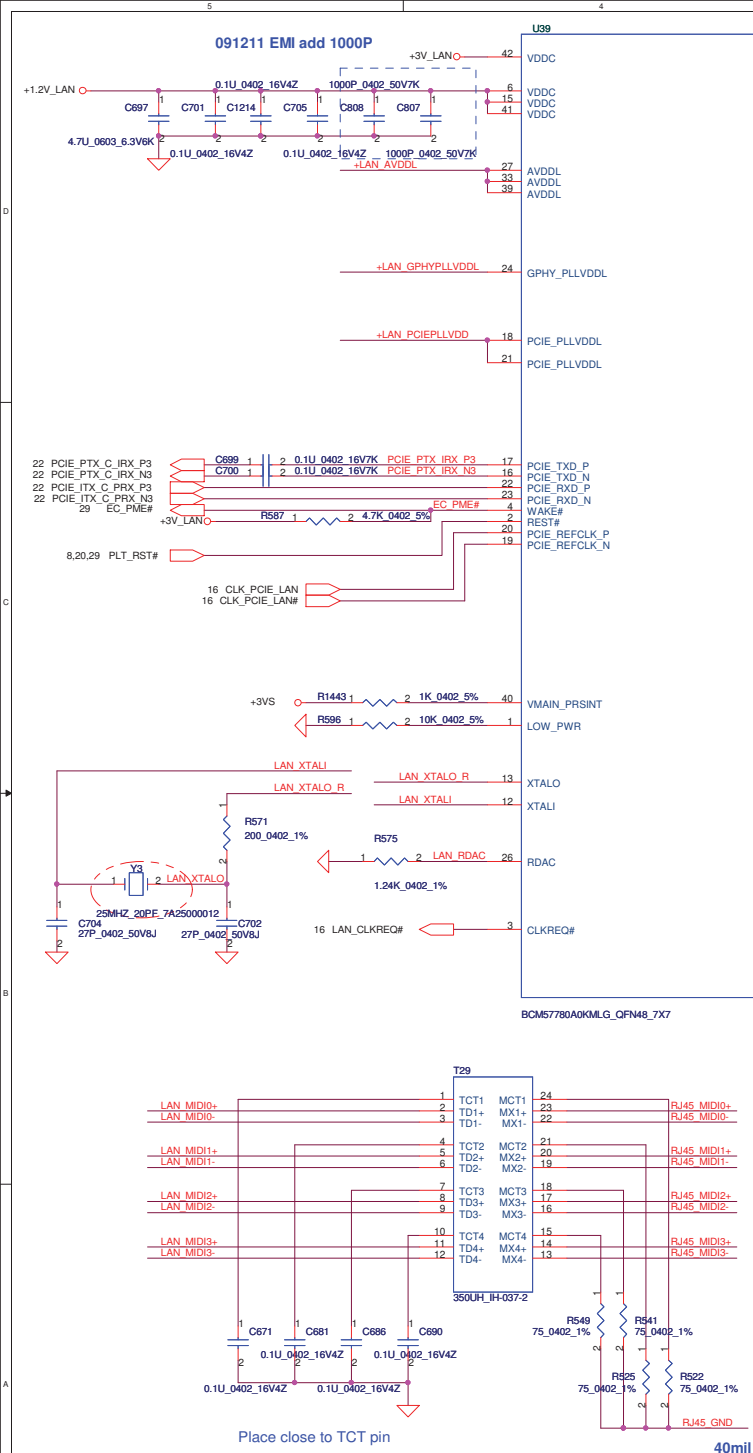
Card Reader RTS5138 / RTS5137
(only SD+MMC function)



Card Reader Connector



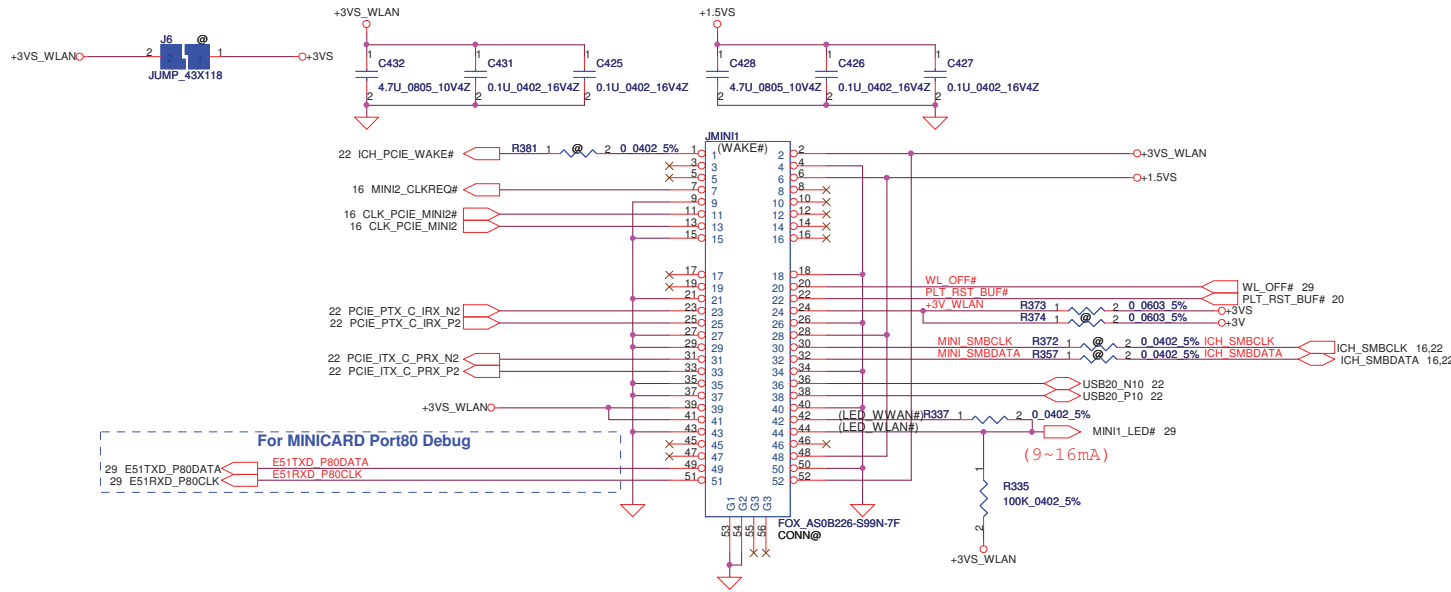
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Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title CardReader RTS5137		
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				Customer	PEW72/82 M/B LA-6631P Schematic	1.0
				Date:	Thursday, July 08, 2010	Sheet 25 of 44



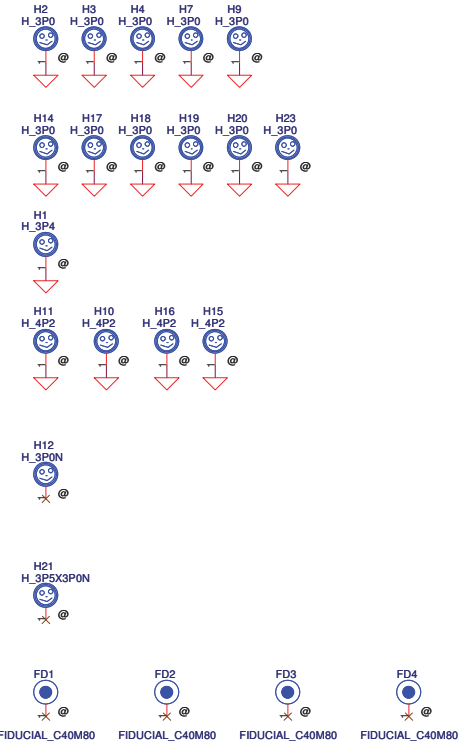
BOTH HAND: S X'FORM_GST5009-D LF LAN, SP050006B00
TIMAG: S X'FORM_IH-160 LAN, SP050006F00

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					Document Number	
					PEW72/82 M/B LA-6631P Schematic	
					Date: Thursday, July 08, 2010	
					Sheet 26 of 44	Rev 1.0

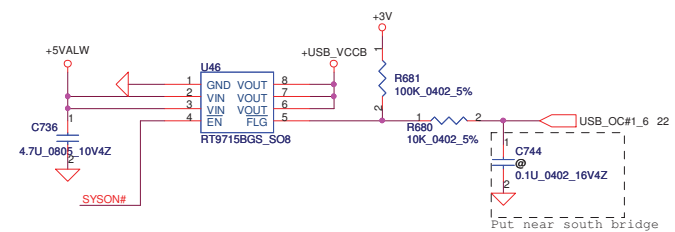
For Wireless LAN



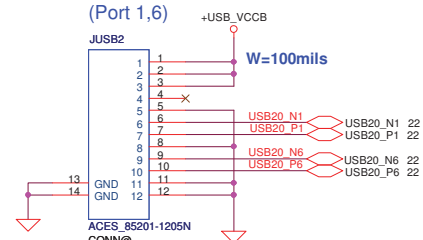
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



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								Rev		Document Number				Rev			
								PEW72/82 M/B LA-6631P Schematic								1.0	
								Date		Thursday, July 08, 2010		Sheet		27 of 44			

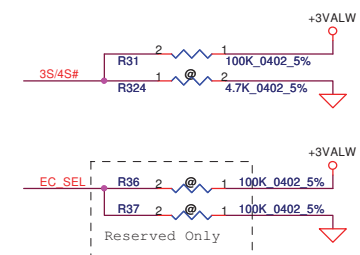
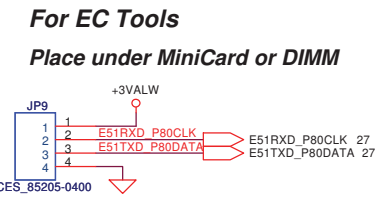
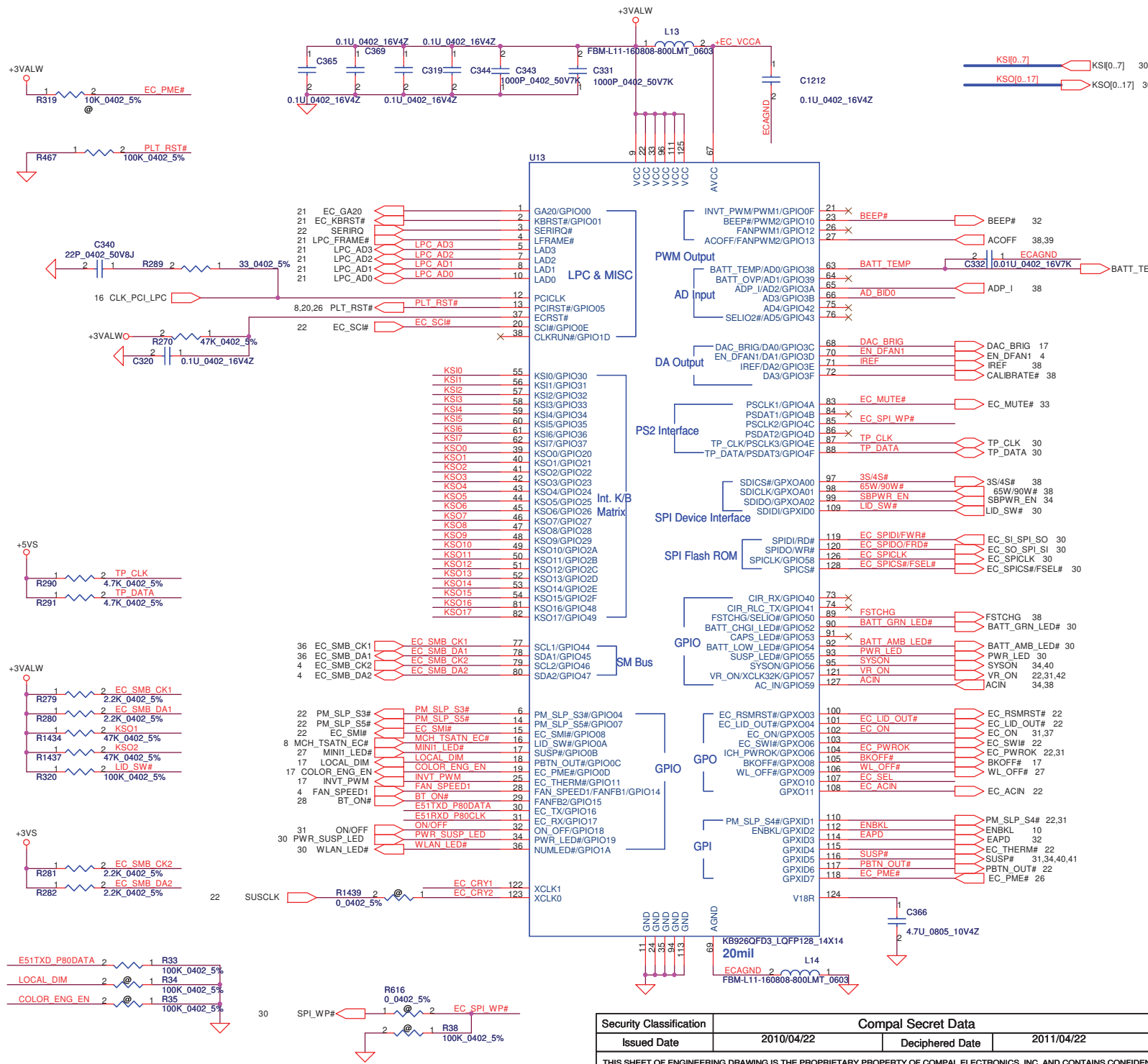


USB/B Conn. LS-6581
(Port 1,6) +USB_VCCB

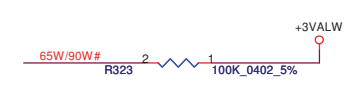


The schematic diagram illustrates the BT module circuit. It features a +3VSW supply connected to a network of capacitors (C324, C330) and a resistor (R274) leading to a BT module input. A +3VMS supply is connected to a transistor (Q20) and a capacitor (C323). The transistor (Q20) is an AQ3413L, and its gate is connected to a +BT_VCC supply. The output of Q20 is connected to a capacitor (C317) and a resistor (R269). The circuit also includes a transistor (Q21) which is a 2N7002-7-F, connected to a +BT_VCC supply and a capacitor (C316). The output of Q21 is connected to a capacitor (C316) and a resistor (R269). The circuit is connected to a USB module (jBT1) and a BT module (ACES_B7213-0800G).

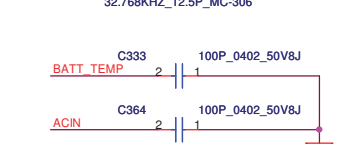
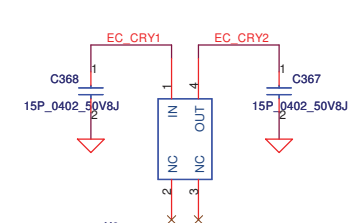
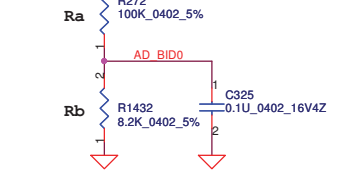
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/04/22	Deciphered Date	2011/04/22	Title	BT & USB Connector
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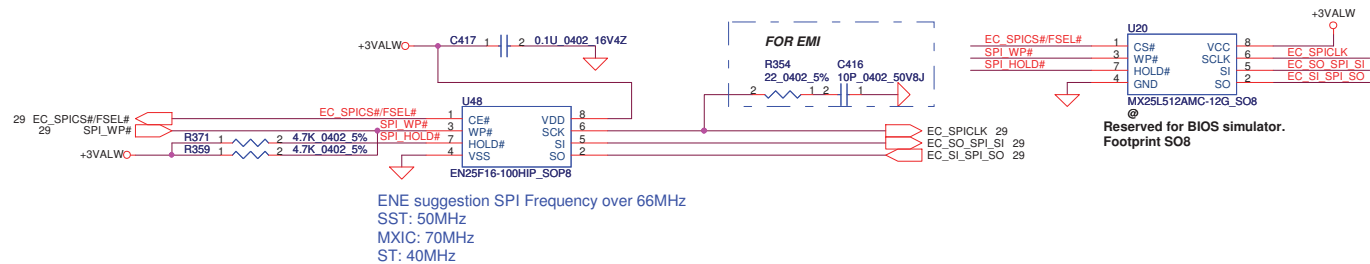
EC_SEL	EC_VERSION
HIGH	KB926D3
LOW	KB926E0



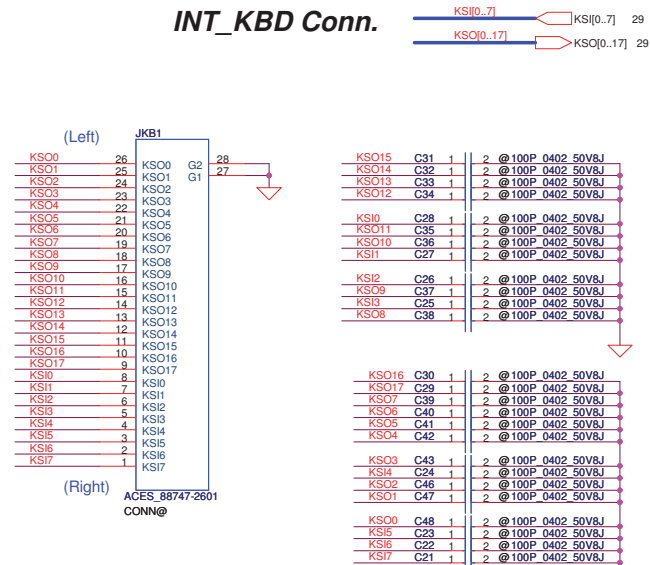
Analog Board ID definition, Please see page 3.



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										B		PEW72/82 M/B LA-6631P Schematic		1.0	
										Date:		Thursday, July 08, 2010		Sheet 29 of 44	

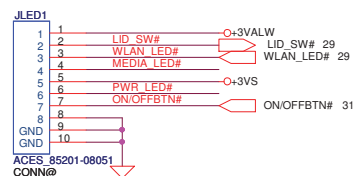


INT_KBD Conn.

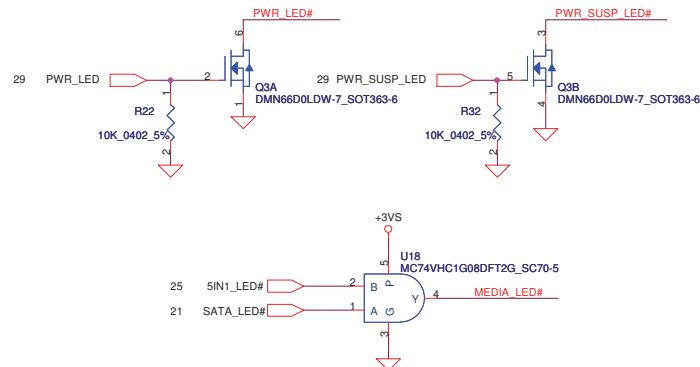
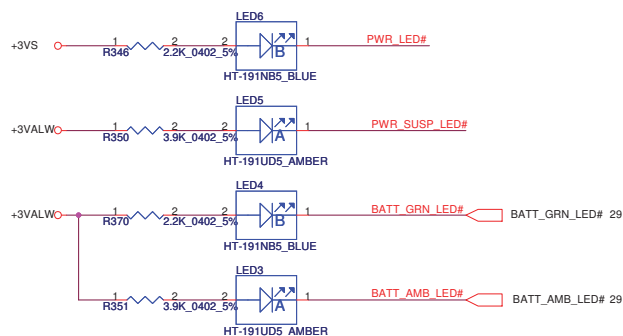
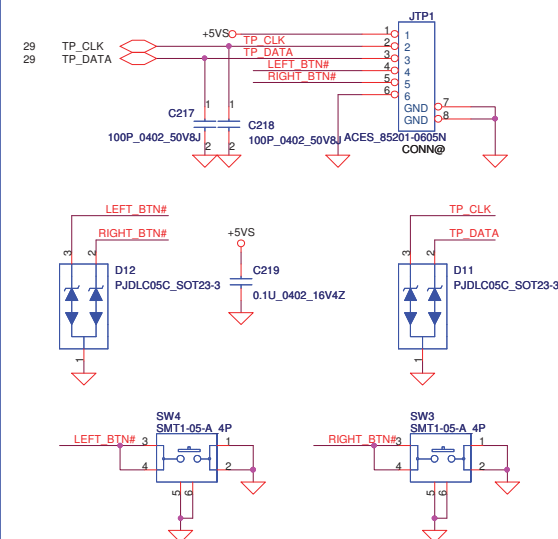


LS-6582

Power/B



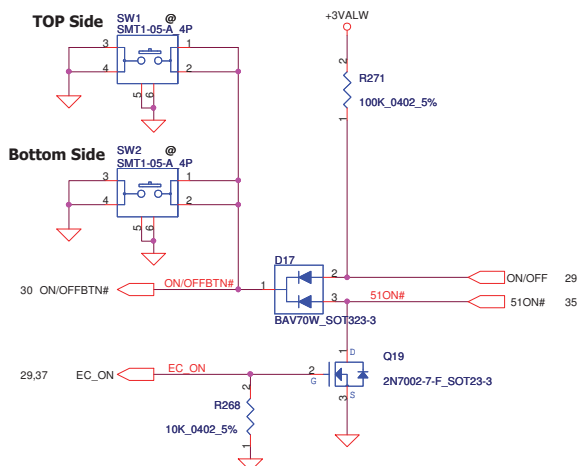
To TP/B Conn.



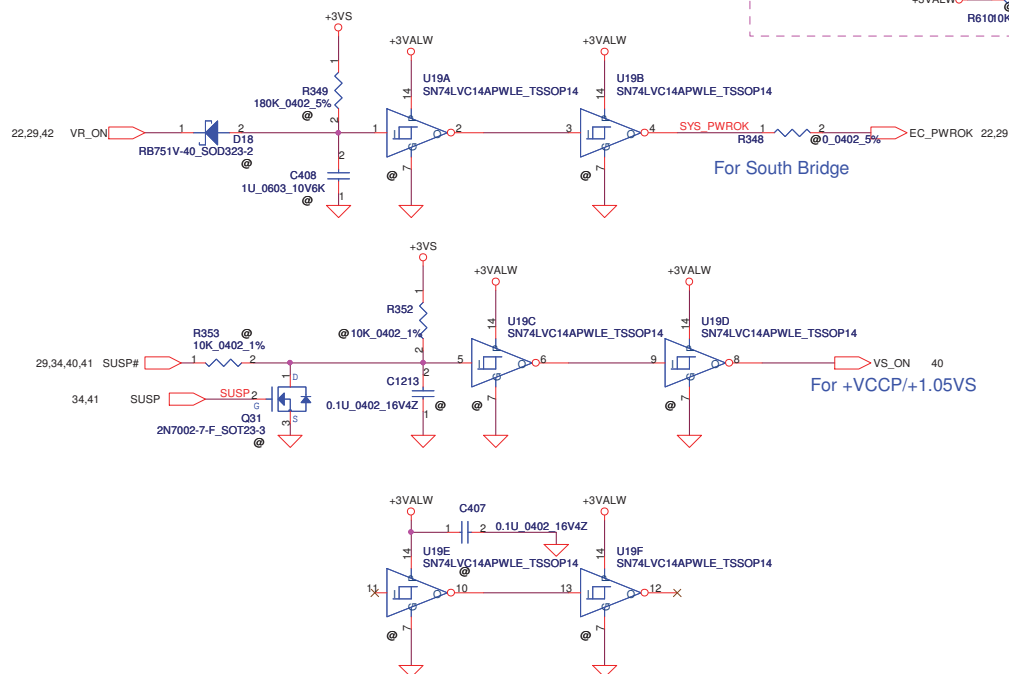
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Issued Date		2010/04/22	Deciphered Date	2011/04/22	Title	BIOS, I/O Port & K/B Connector		
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					PEW72/82 M/B LA-6631P Schematic	1.0		
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Power Button

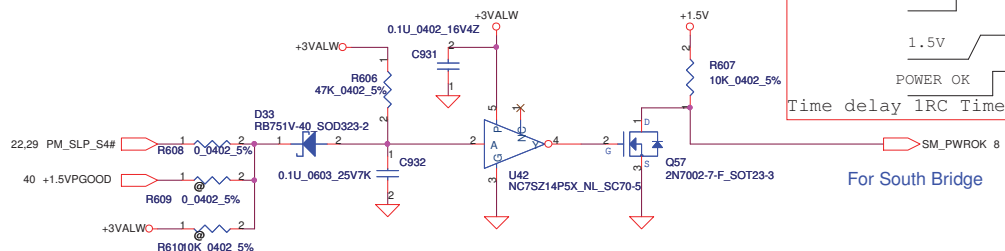
ON/OFF switch



Power ON Circuit

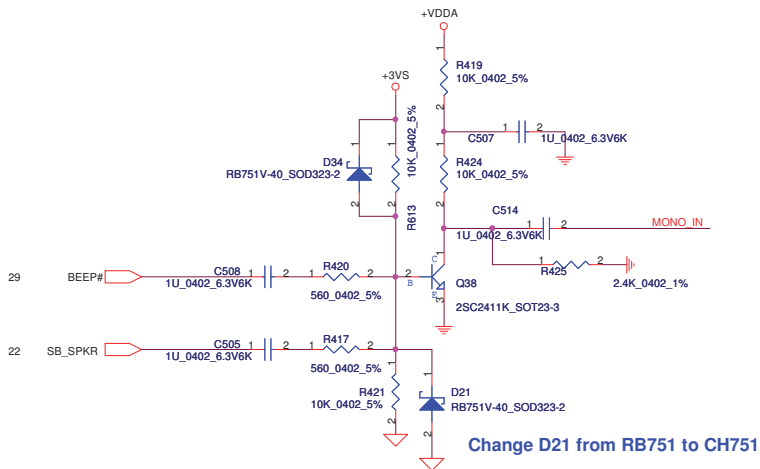


DDR3



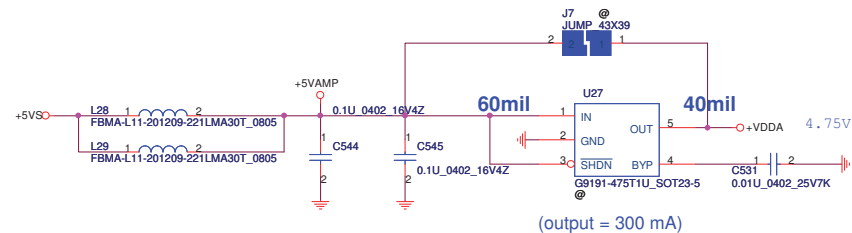
For South Bridge

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2010/04/22				2011/04/22				Title			
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PEW72/82 M/B LA-6631P Schematic				1.0				Date			
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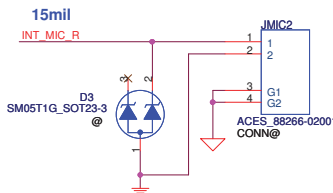
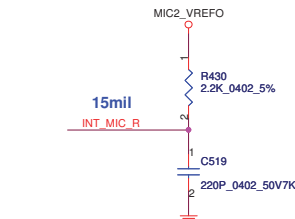
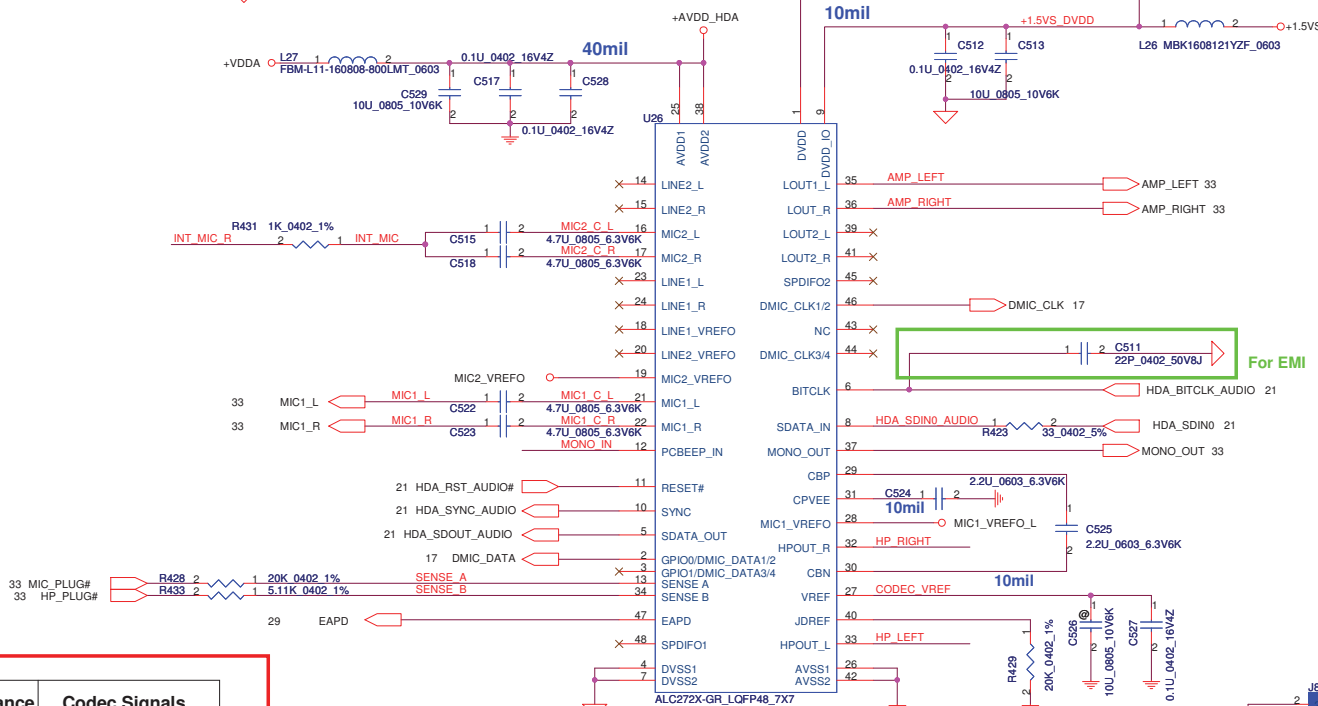


Change D21 from RB751 to CH751

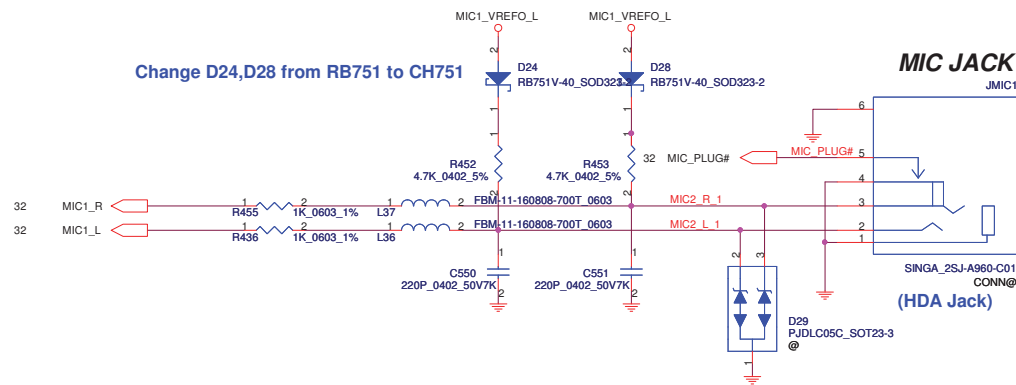
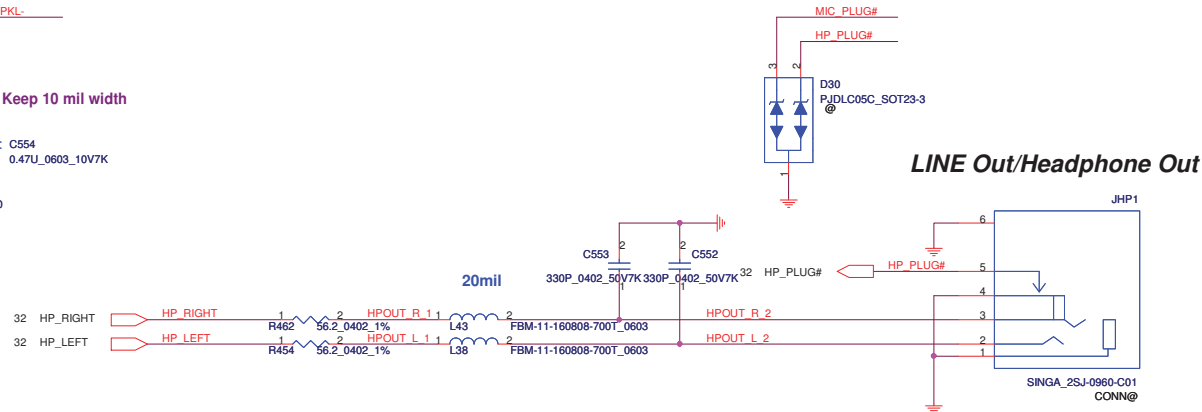
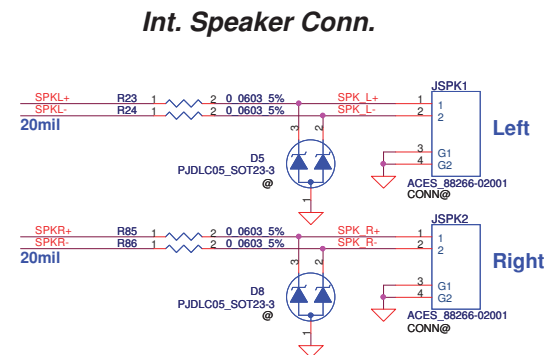
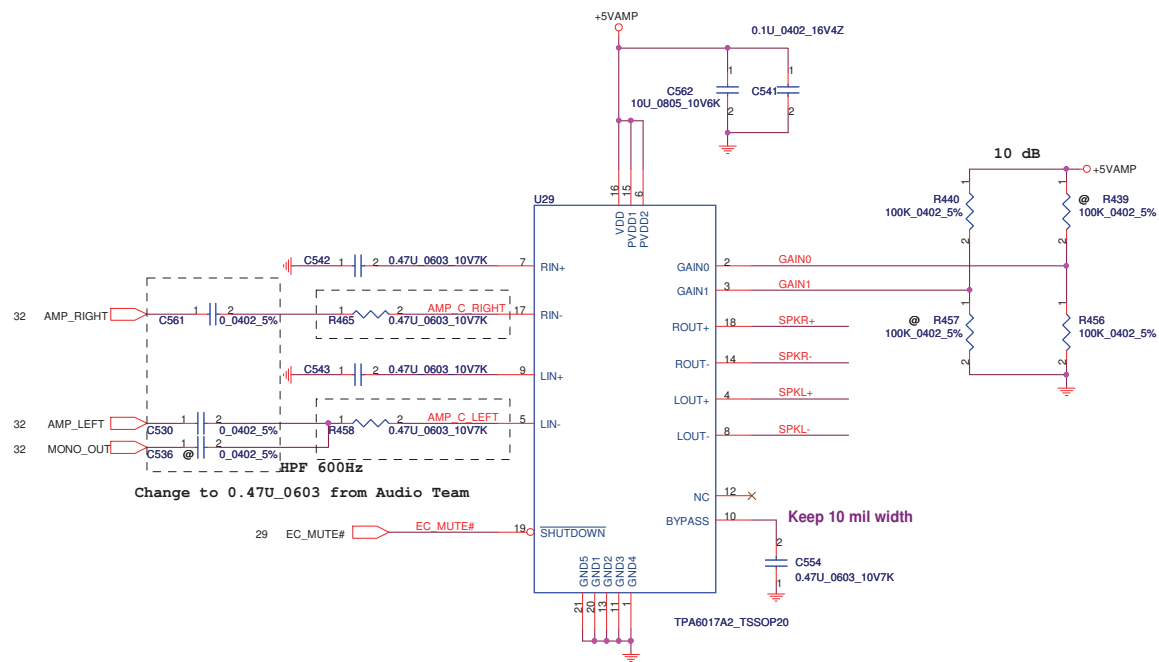
HD Audio Codec



(output = 300 mA)

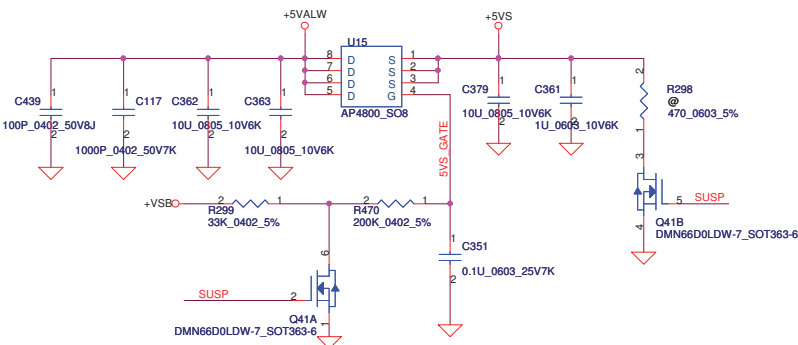


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-B (PIN 21, 22)
	20K	
	10K	
	5.1K	
SENSE B	39.2K	PORT-H (PIN 32,33)
	20K	
	10K	
	5.1K	

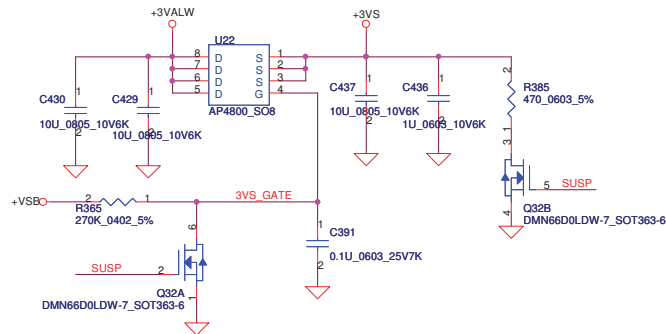


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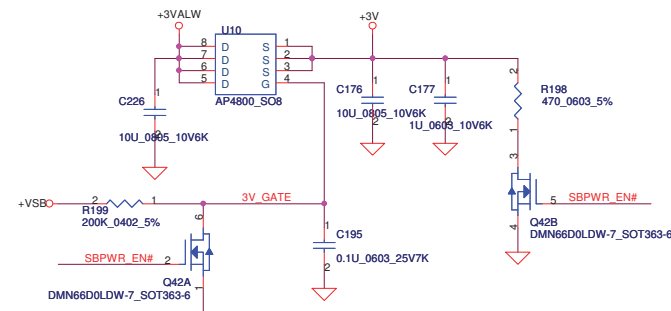
+5VALW TO +5VS



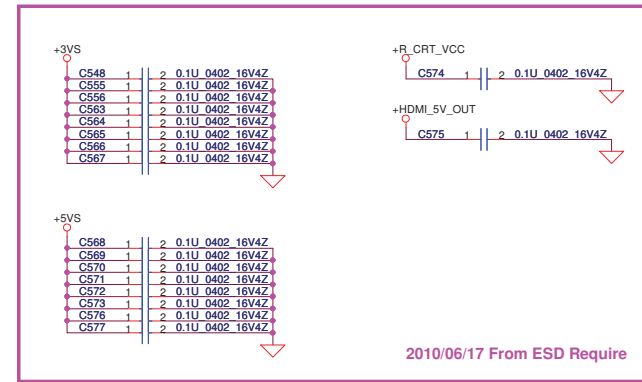
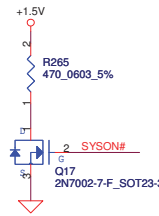
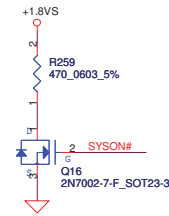
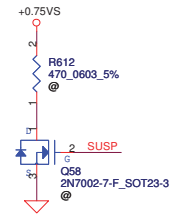
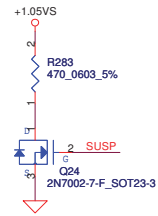
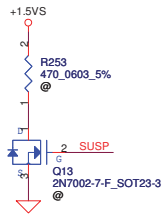
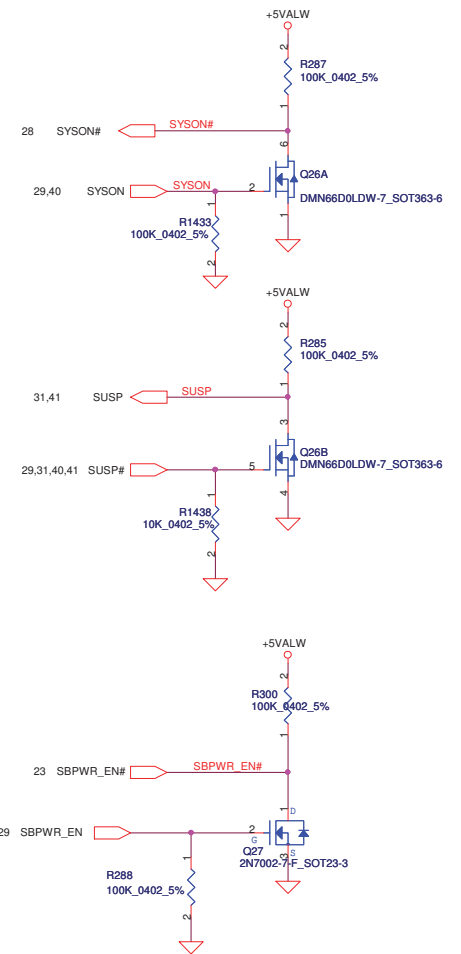
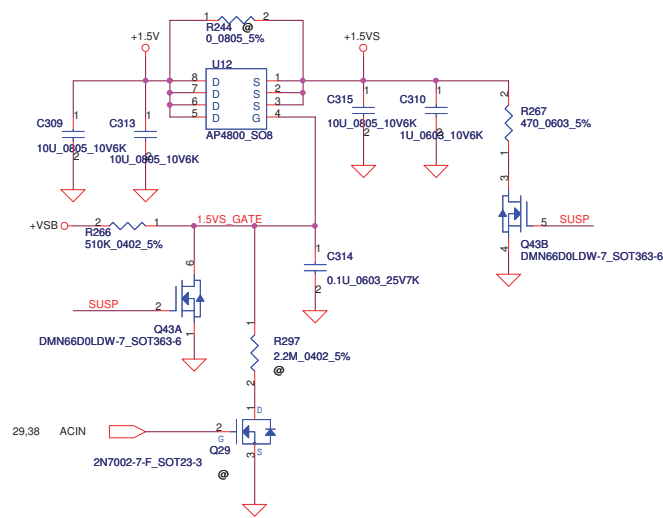
+3VALW TO +3VS



+3VALW TO +3V_SB(ICH8M AUX Power)

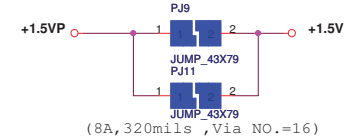
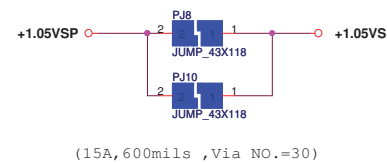
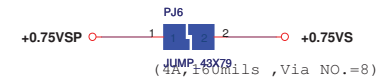
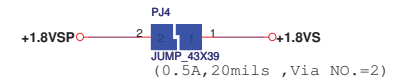
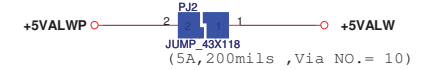
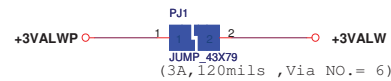
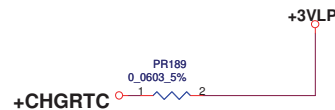
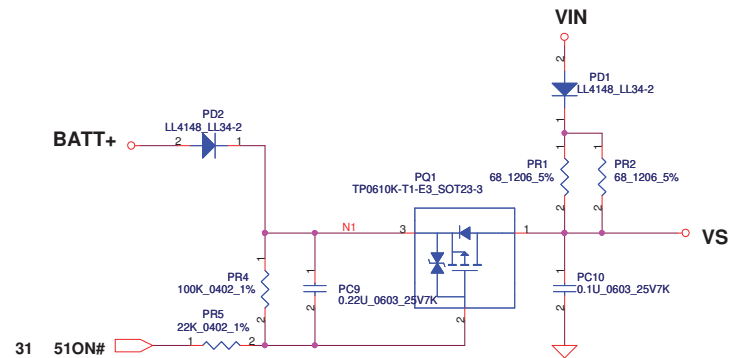
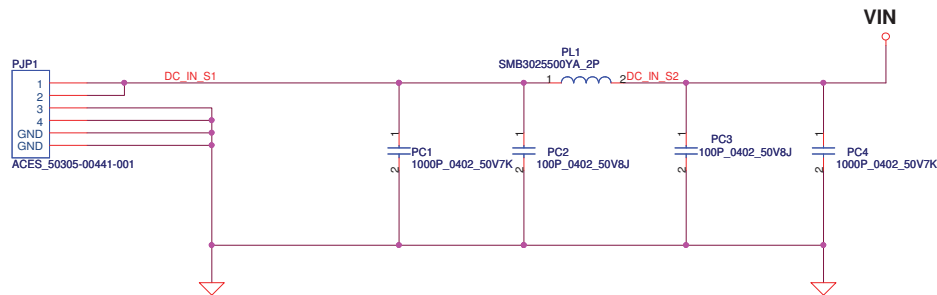


+1.5V to +1.5VS

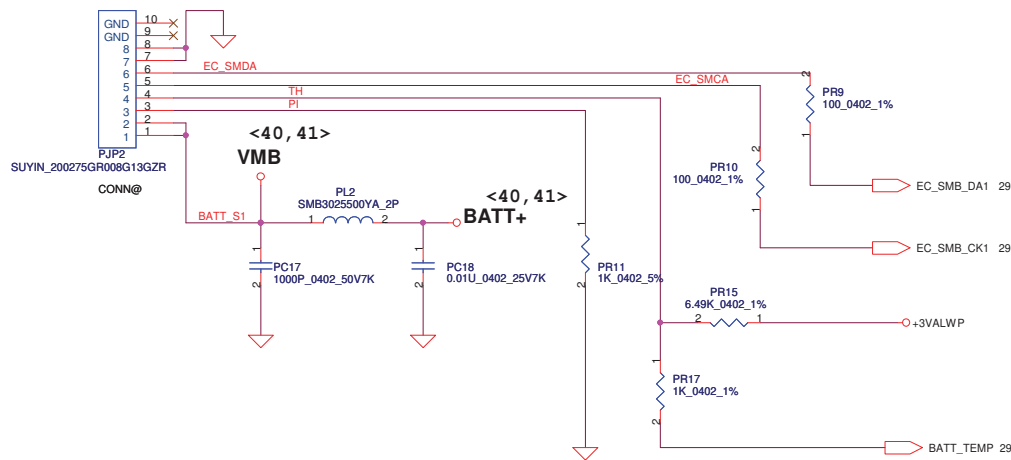


2010/06/17 From ESD Require

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				Document Number	Rev
				PEW72/82 M/B LA-6631P Schematic	1.0
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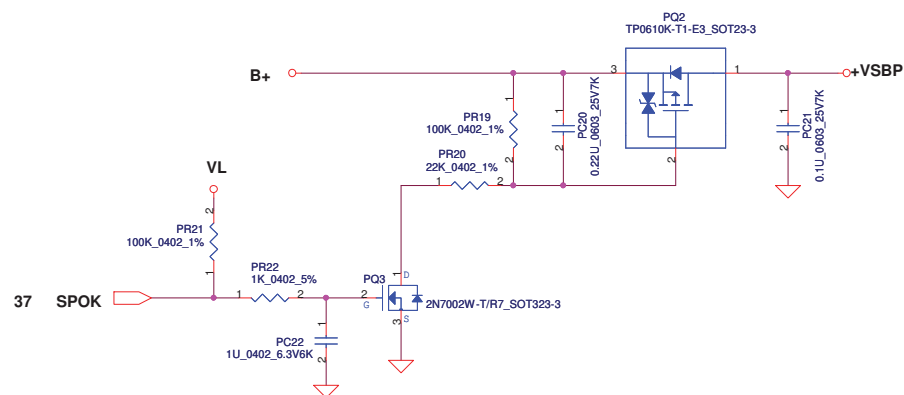
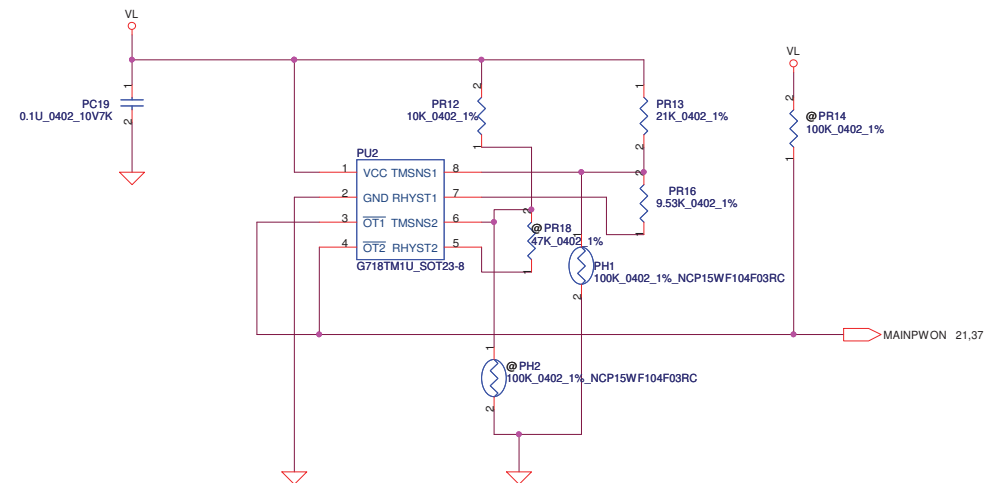
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PH1 under CPU botten side :

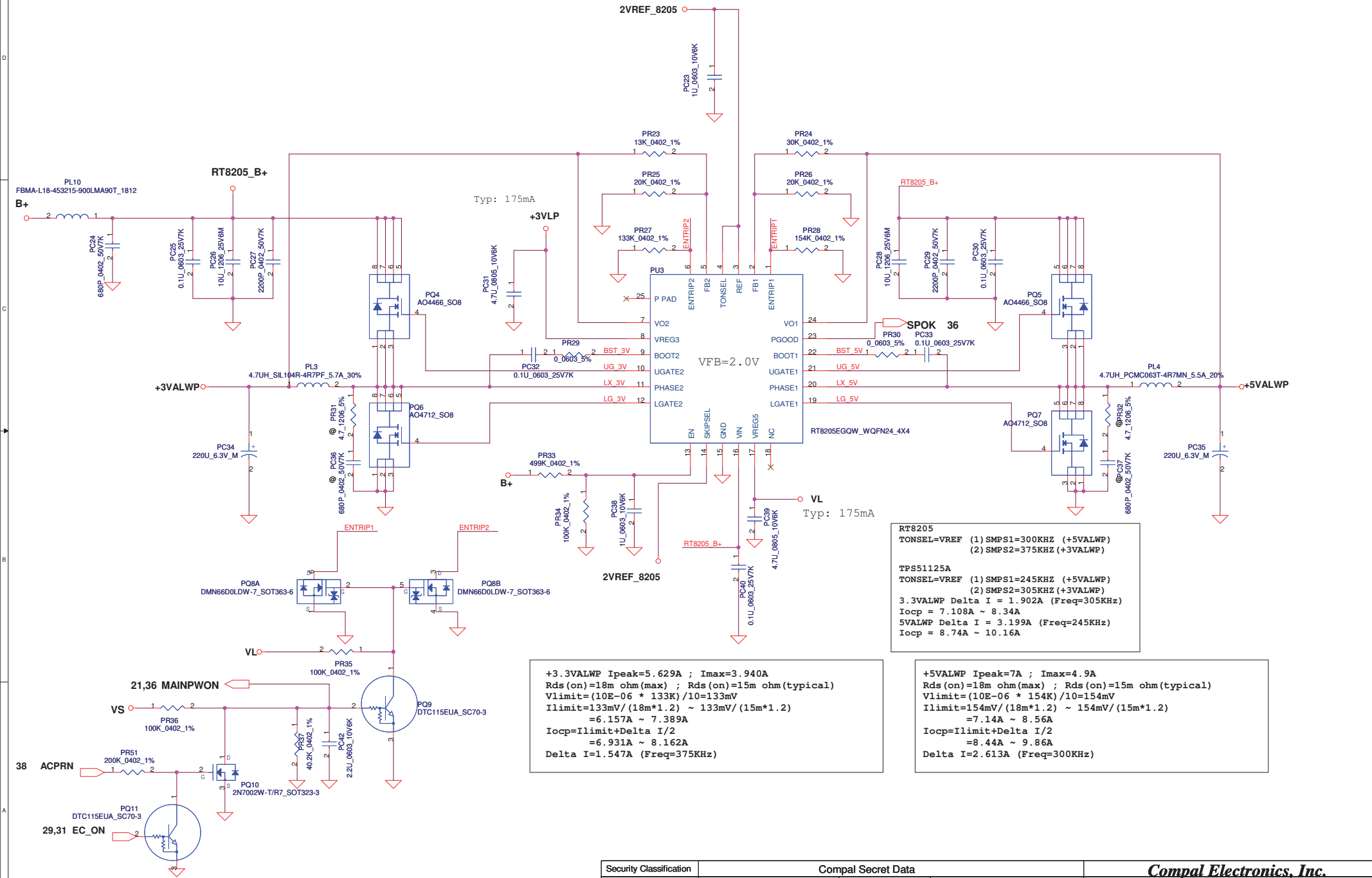
CPU thermal protection at 92 degree C

Recovery at 56 degree C



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Note:
 Use TPS51125 IC can remove RTC refernece LDO
 Use TPS51427 IC must keep RTC refernece LDO



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3VALW/5VALW

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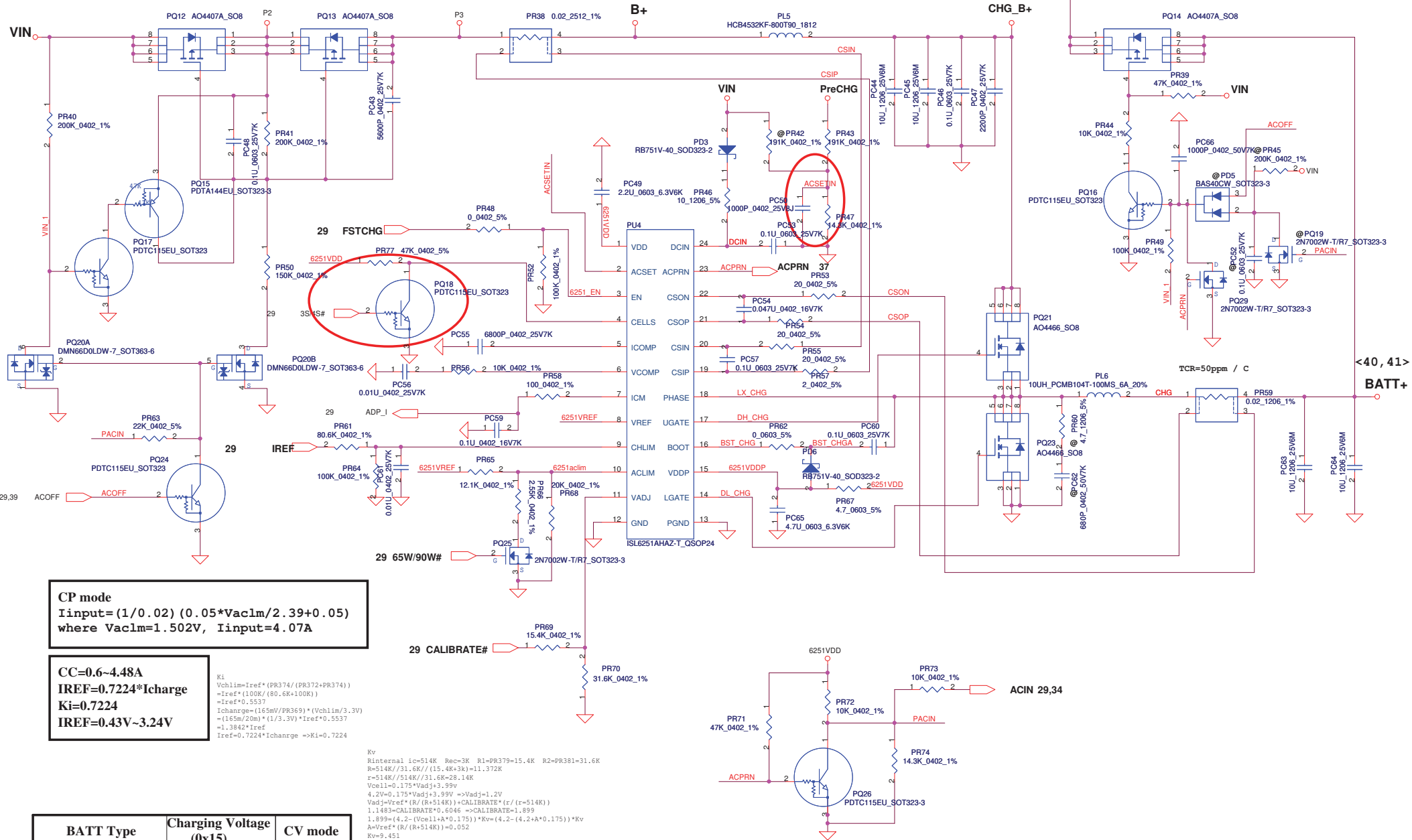
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1.0

I_{ada}=0~4.74A (90W/19V=4.736A)
I_{ada}=0~3.42A (90W/19V=3.421A)

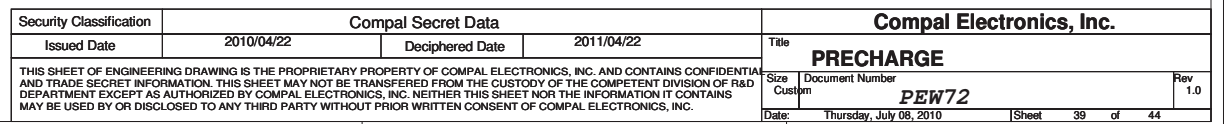
ADP_I = 19.9*I_{adapter}*R_{sense}

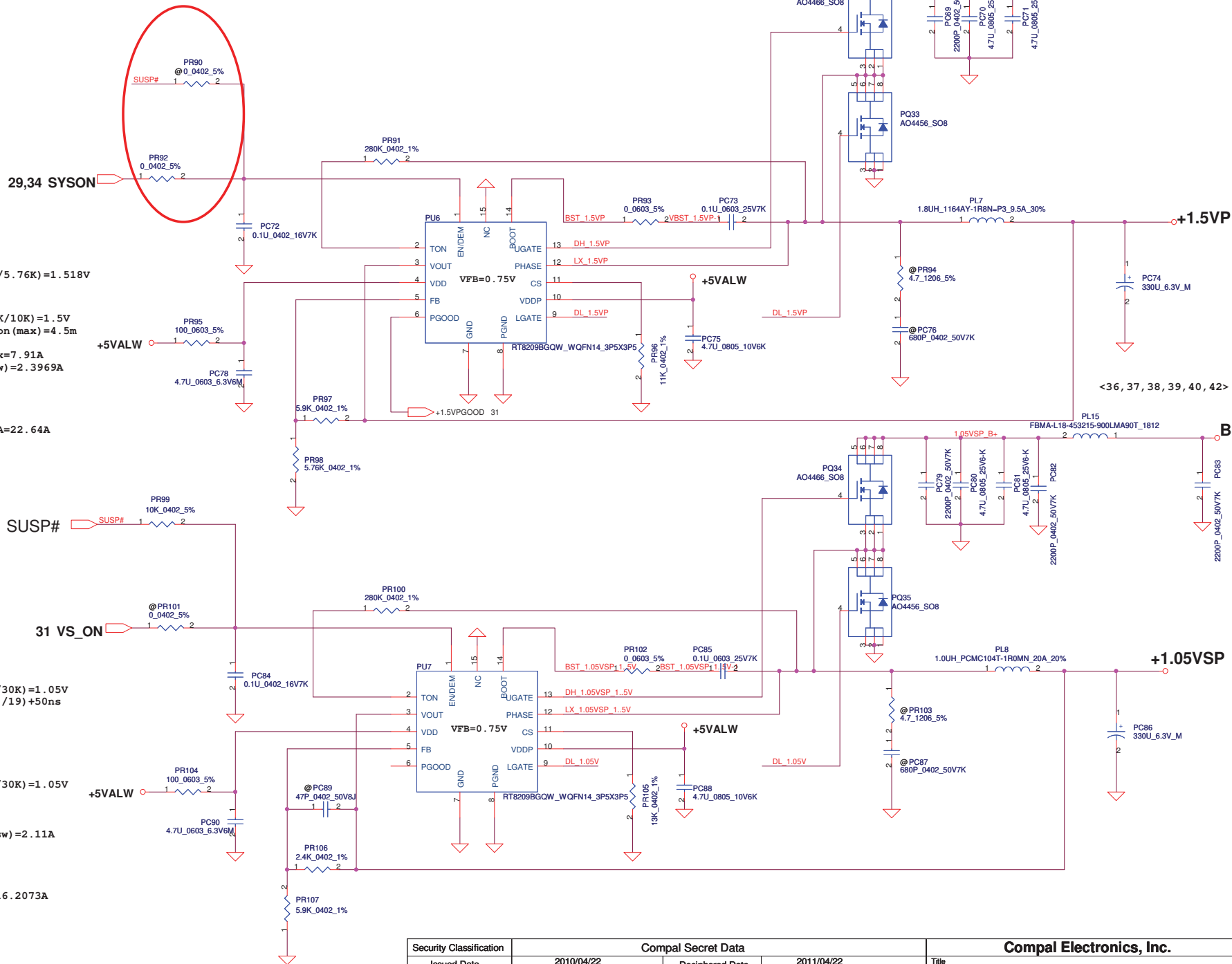
CP = 85%*I_{ada} ; CP = 4.07A
CP = 85%*I_{ada} ; CP = 2.91A



BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

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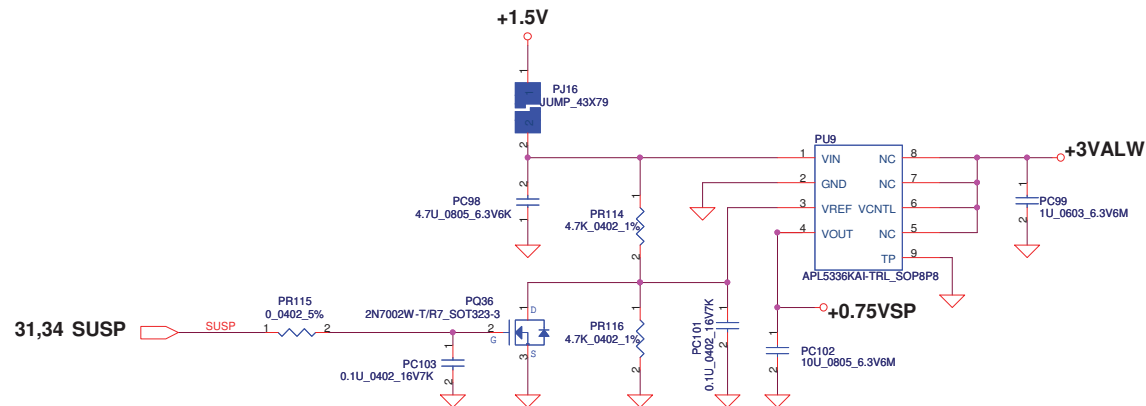
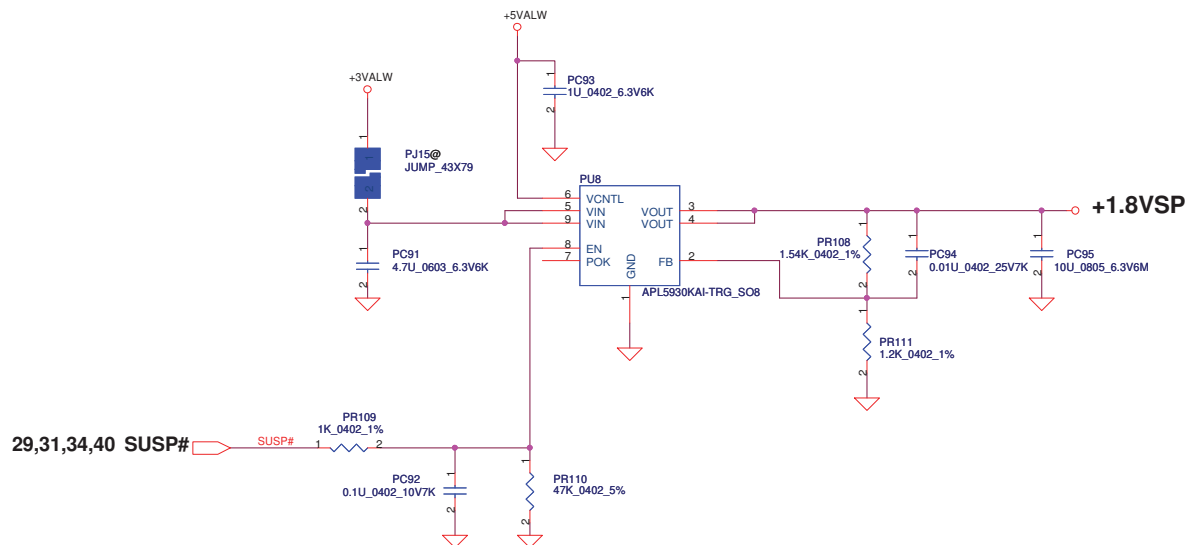


VFB=0.75V
 $V_o = VFB * (1 + PR97 / PR98) = 0.75 * (1 + 5.9K / 5.76K) = 1.518V$
 $F_{sw} = 282KHz$
 $<V_o = 1.5V>$ VFB=0.75V
 $V_o = VFB * (1 + PR116 / PR117) = 0.75 * (1 + 10K / 10K) = 1.5V$
 $F_{sw} = 262KHz$ Cout ESR=15m ohm Rdson(max)=4.5m
 Rdson(min)=5.6m
 $I_{peak} = 11.3A$, $1.2I_{peak} = 13.56A$, $I_{max} = 7.91A$
 $\Delta I = ((19 - 1.5) * (1.5 / 19)) / (L * F_{sw}) = 2.3969A$
 $\Rightarrow 1/2 \Delta I = 1.198A$
 $V_{trip} = R_{trip} * I_{0uA} = 18K * 10uA = 0.18V$
 $I_{ocpmin} = V_{trip} / Rdsonmax * 1.2 + 1.198 = 0.075 / (0.018 * 1.3) + 1.198 = 13.98A$
 $I_{ocpmax} = (0.075 / (0.015 * 1.1)) + 1.198A = 22.64A$
 $I_{ocp} = 13.98 \sim 22.64A$

VFB=0.75V
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$
 $Ton = 19 * e^{-12 * 143000} ((2/3) * V_o + 100mV) / 19 + 50ns = 2.645e-7 us$
 $\Rightarrow V_o / Vin = D = Ton / Ts \Rightarrow Ts = 3.35us$
 $F_{sw} = 261KHz$ (by calculation tool)

$<V_o = 1.05V>$ VFB=0.75V
 $V_o = VFB * (1 + PR108 / PR109) = 0.75 * (1 + 12K / 30K) = 1.05V$
 $F_{sw} = 261KHz$ Cout ESR=15m ohm
 Rdson(max.)=11.5m Rdson(min)=9m
 $I_{peak} = 9A$, $I_{max} = I_{peak} * 0.7 = 6.3A$
 $\Delta I = ((19 - 1.05) * (1.05 / 19)) / (L * F_{sw}) = 2.11A$
 $\Rightarrow 1/2 \Delta I = 1.055A$
 $V_{trip} = R_{trip} * I_{0uA} = 15K * 10uA = 0.15V$
 $I_{ocpmin} = V_{trip} / Rdsonmax * 1.3 + 1.055 = 0.15 / (0.011 * 1.3) + 1.055 = 11.0892A$
 $I_{ocpmax} = (0.15 / (0.009 * 1.1)) + 1.055A = 16.2073A$
 $I_{ocp} = 11.0892A \sim 16.2073A$

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	add 3S/4S pin function	add 4 cell battery	0.2	45	add PQ18 PUTC115EU_SOT323 (SB301150200) and PR77 47K +-5% 0402 (SD028470280)	2010/06/11	EVT
2	ACSETIN net	ACSETIN net no connect	0.2	45		2010/06/11	EVT
3	1.5V enable	1.5V enable BOM error	0.2	45	add PR92 and delete PR90 0_0402_5% (SD028000080)	2010/06/11	EVT
4							
5							
6							
7							
8							
9							
10							
11							
12							
13							
16							
17							

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A --> C Change List

- 20100622-----
1. Change U48 to SA00002KI00 (EON EN25F16-100HIP)
2. Populate D11, D12
3. Populate R132, C194, R136, C225, R354, C416
- 20100618-----
1. Page 30, For EMI reuqire populate C31, C32, C33, C34, C28, C35, C36, C27, C30, C29, C39, C40, C41, C42, C43, C24, C46, C47, C48 C23, C22, C21
2. Page 12, Populate C483
- 20100617-----
1. Add T19, T25 for boundary scan (CIT Factory)
2. Page 34, Add 0.1U_0402_16V4Z x 16 for +3VS/+5VS/+R_CRT_VCC/+HDMI_5V_OUT
C548, C555, C556, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577
3. Page 29, Reserved R38, R616 for SPI_WP#
- 20100615-----
1. Page22, Add C745 for USB_OC#1_6 at chipset side.
2. Page28, Change C744 BOM Structure to @
- 20100614-----
1. Page29, Change U13 to KB926QFD3 (SA00001J580)
Change R1432 to 8.2K_0402_5% (SD028820180)
2. Page16, Change U16 to ICS9LPRS387 (SA000020H10)
Change BOM Structure of L33 and R401 to @
Populate L32 and R400
3. Page31, Change BOM Structure of SW1 and SW2 to @
4. Change U7, U8, U43 to MC74VHC1G08DFT2G (SA000000H00)
5. Update Power Schematics

C --> MP Change List

- 20100709-----
1. Page33, Change C561, C530, C536 to 0 ohm (SD028000080)
Change R465, R458 to 0.47U_0603 (SE080474K80)
- 20100708-----
1. Page28, Unpopulate D23 (follow ESD suggestion)
- 20100706-----
1. Page29, Populate R289 and C340.
2. Page30, Unpopulate C21 ~ C43 and C46 ~ C48.

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