Cathedral Peak Block Diagram

Project code: 91.4J501.001
PCB P/N : 48.4J501.001
REVISION : 07261

CLK GEN.
ICS 9LPRS365BKLFT (71.09365.A03)
RTM 875N-606-LFT (71.00875.003)
3

Mobile CPU
Penryn 479
4, 5

THERMAL EMC2102
21

HOST BUS 667/800/1067MHz@1.05V

DDR2 DIMM1
667/800 MHz
12

DDR2 DIMM2
667/800 MHz
13

667/800MHz

667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

CRT 15

LCD 14

X4 DMI 400MHz

C-Link0

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
17,18,19,20

INT.MIC 29
Line In
29
Codec ALC268 28
AZALIA
MIC In
29
29
OP AMP APA2057 29
INT.SPKR
29
Line Out
(NO SPDIF)
RJ11
MODEM MDC Card 23

PCIex1 **LAN** Giga LAN 88E8071 25 — TXFM 26 — RJ45 26

PCIex1 **New card** 27 — PWR SW G577BR91U 27

PCIex1 **Mini Card** Kedron a/b/g/n 27

LPC BUS

KBC ENE3310 30 — BIOS Winbond W25X80 8M Bits 31 — Launch Buttom 16

LPC DEBUG CONN 31

USB

Blue Tooth (USB) 23 — Camera (USB) 14 — Touch Pad 30 — INT. KB 30

SATA

HDD SATA 22
ODD SATA 22

USB 2 Port 23

USB

CardReader Realtek RTS5158E 27 — MS/MS Pro/xD /MMC/SD 5 in 1 27

SATA

Daughter Board
LED Board
07950 16

Daughter Board
USB Board
2 Port + e-Key
07951 23

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 43

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 45

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 44

1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 44

1D8V_S3	1D5V_S0

CFXCORE DC/DC ISL6263 35,36

INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 42

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24750 47

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

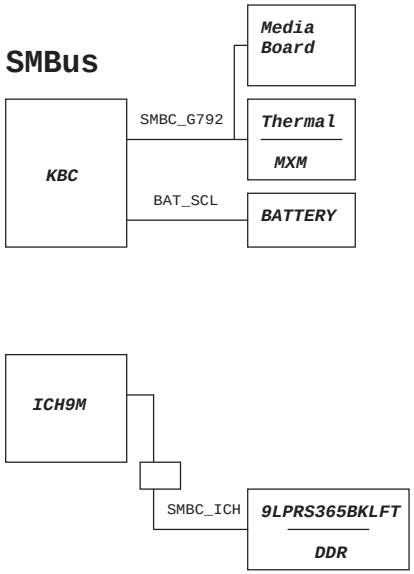
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	*NC*
LANE4	*NC*
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*USB4*
2	*USB2*
3	*NC*
4	*USB3*
5	*Bluetooth*
6	*NC*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	Card Reader
11	*NC*

SMBus



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Title: Reference

Size: A3 | Document Number: Cathedral Peak | Rev: SB

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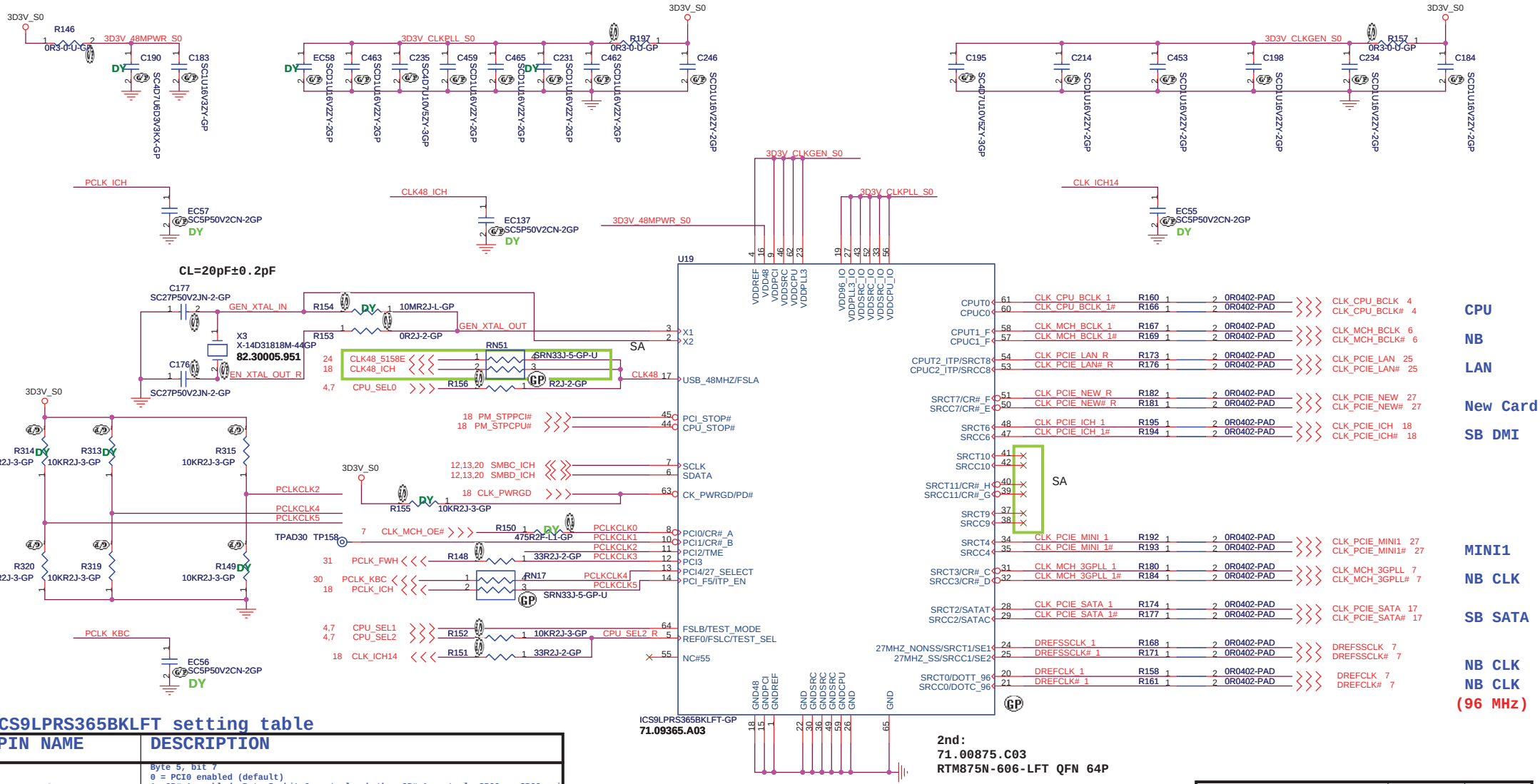

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title: Clock Generator

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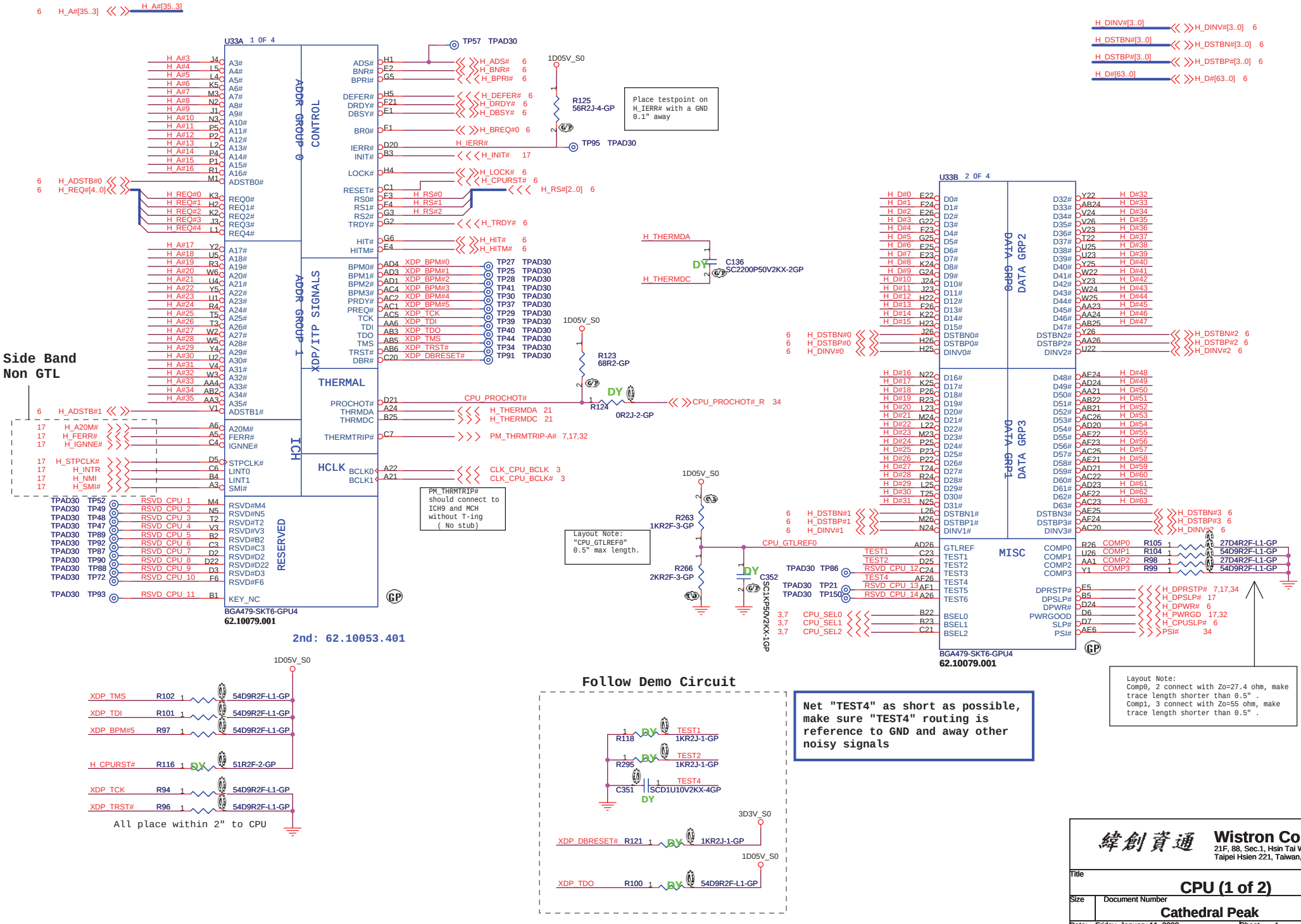

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Title: CPU (1 of 2)	
Size	Document Number: Cathedral Peak — Rev: SA
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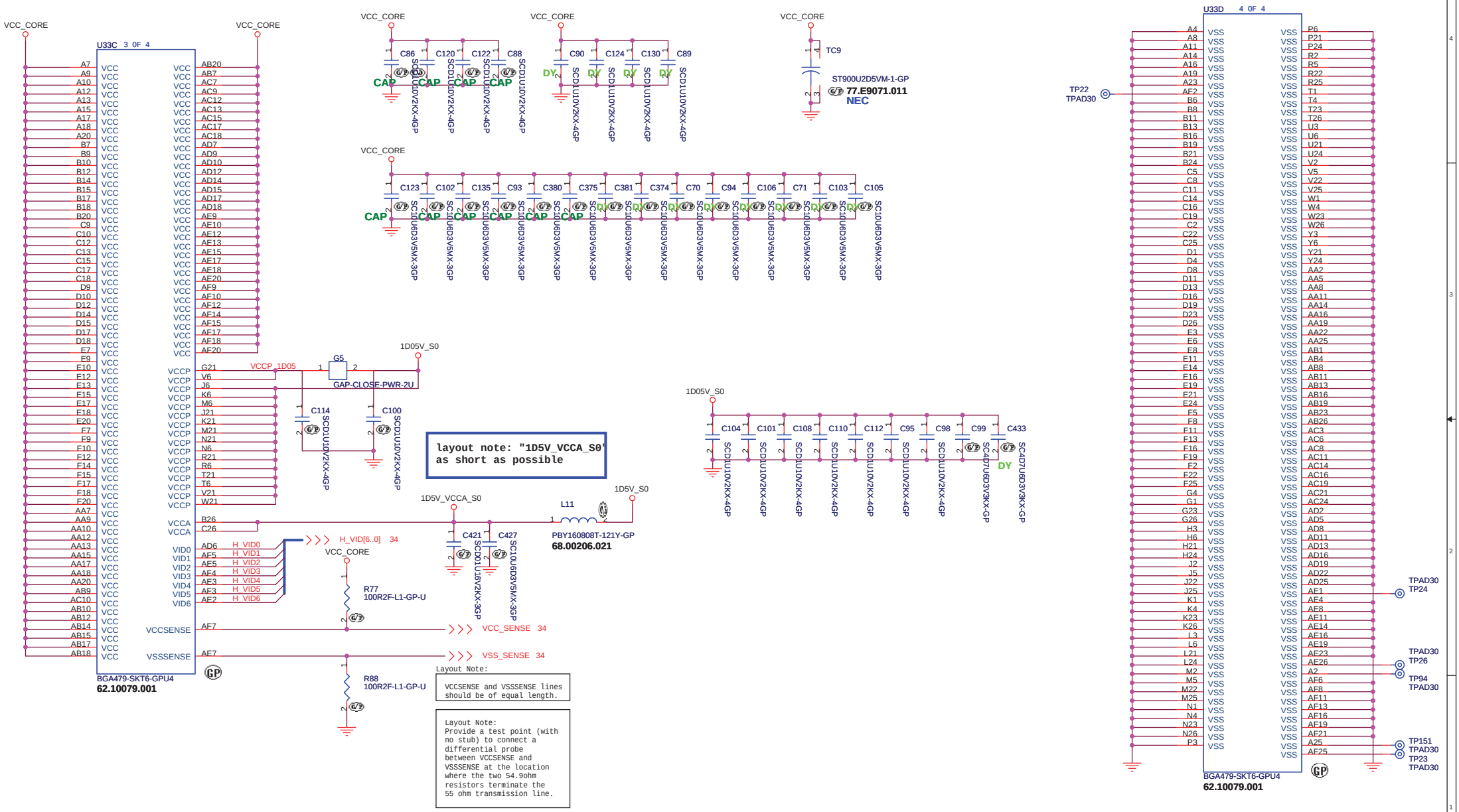

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Title	CPU (2 of 2)	
Size	Document Number: Cathedral Peak	Rev: SA
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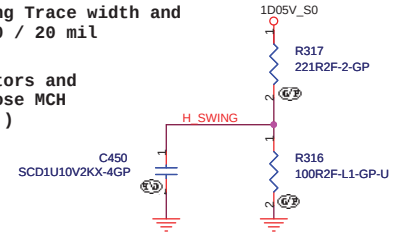
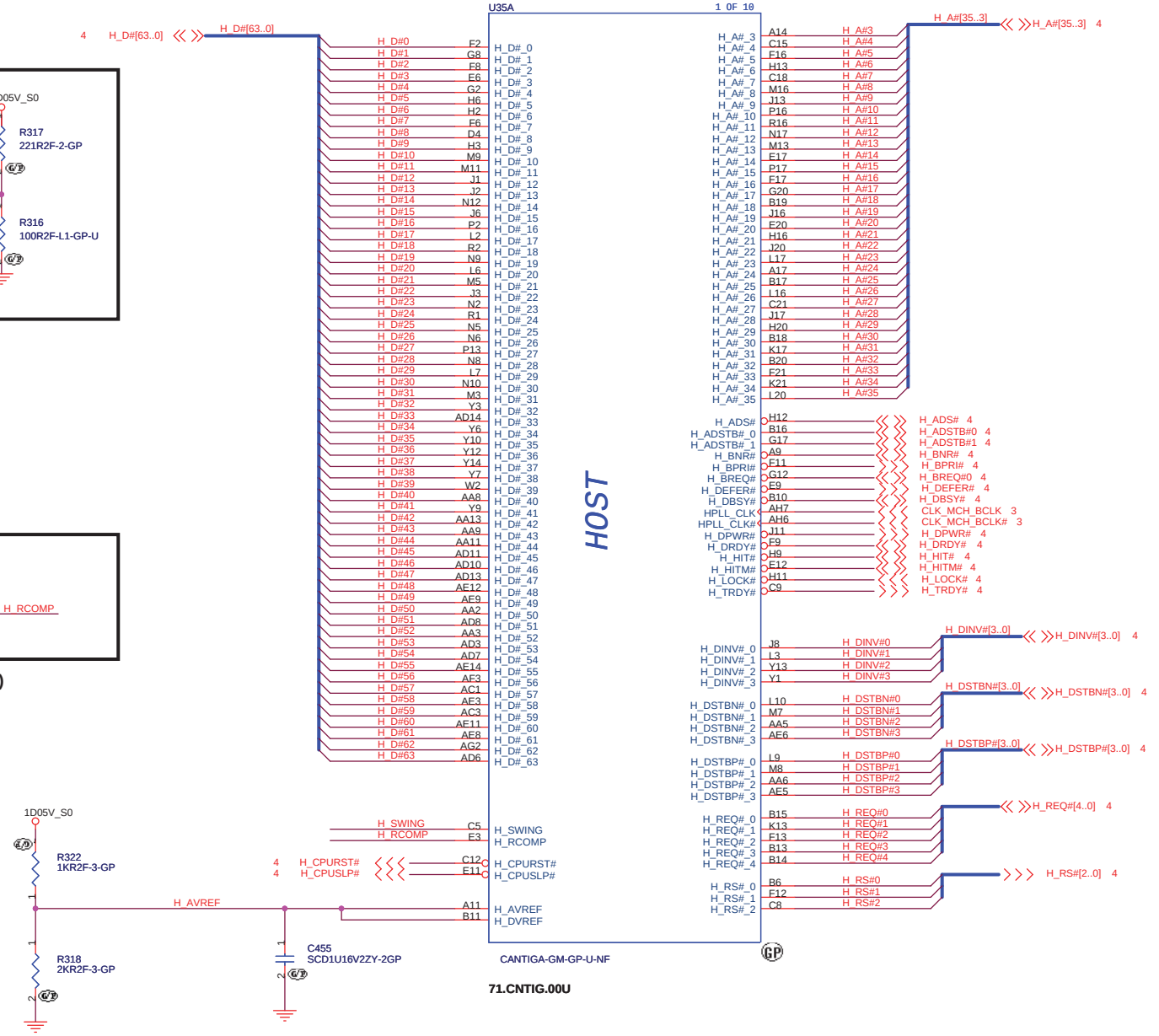
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**Cantiga (1 of 6)**
Size	Document Number: **Cathedral Peak** Rev: SA
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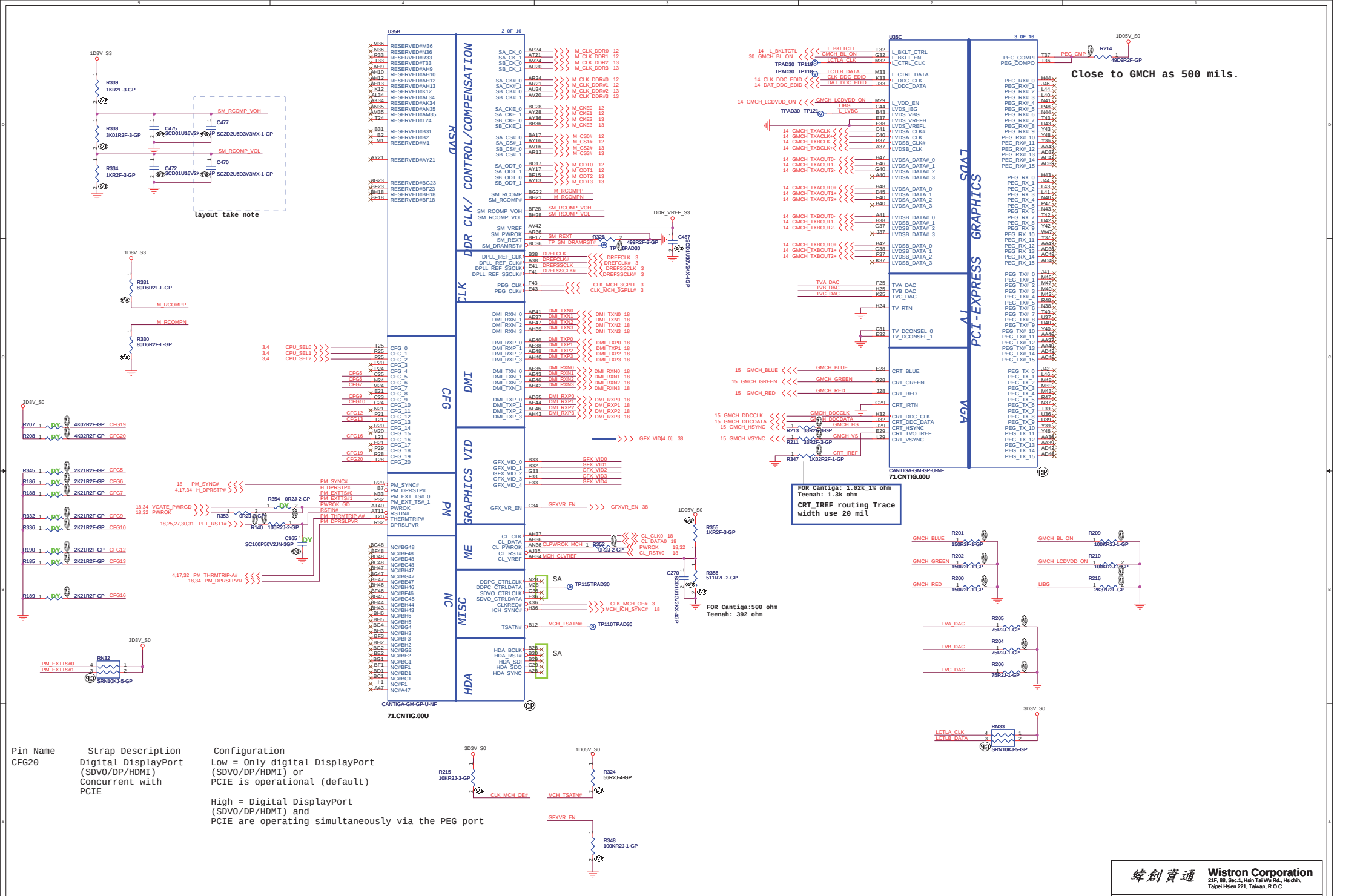
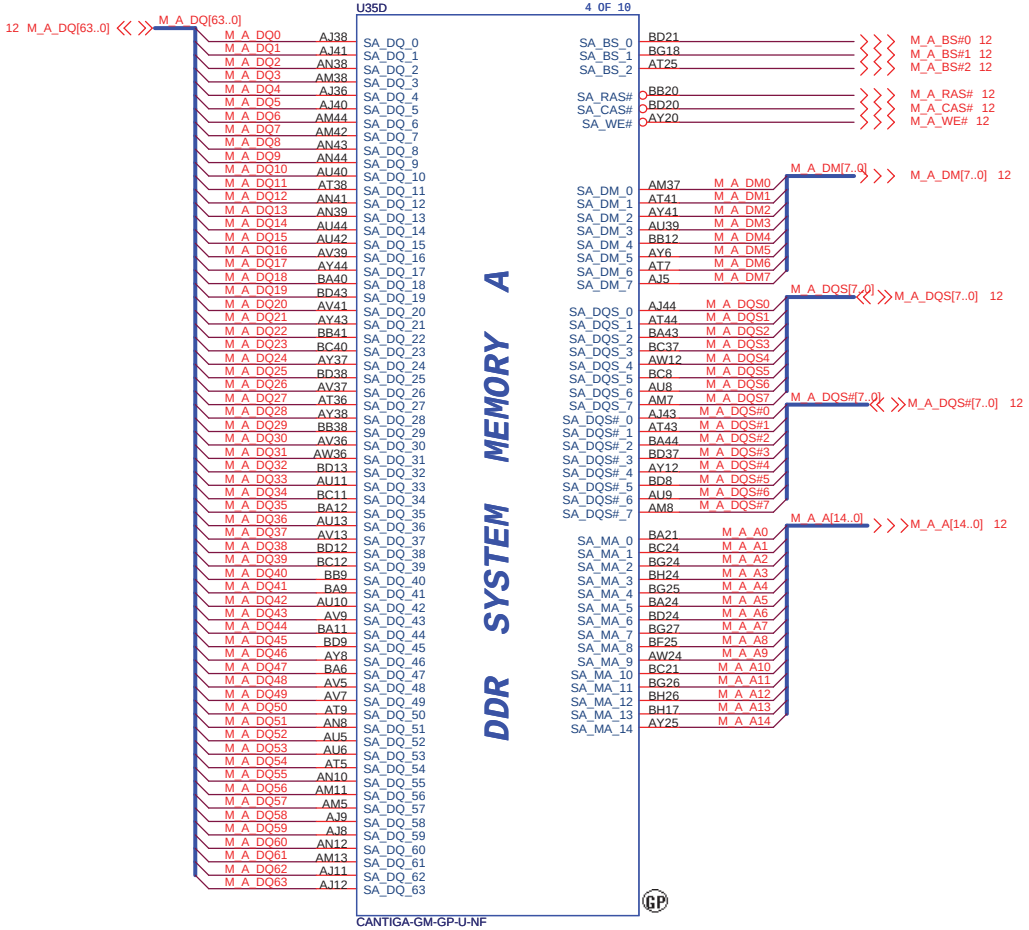
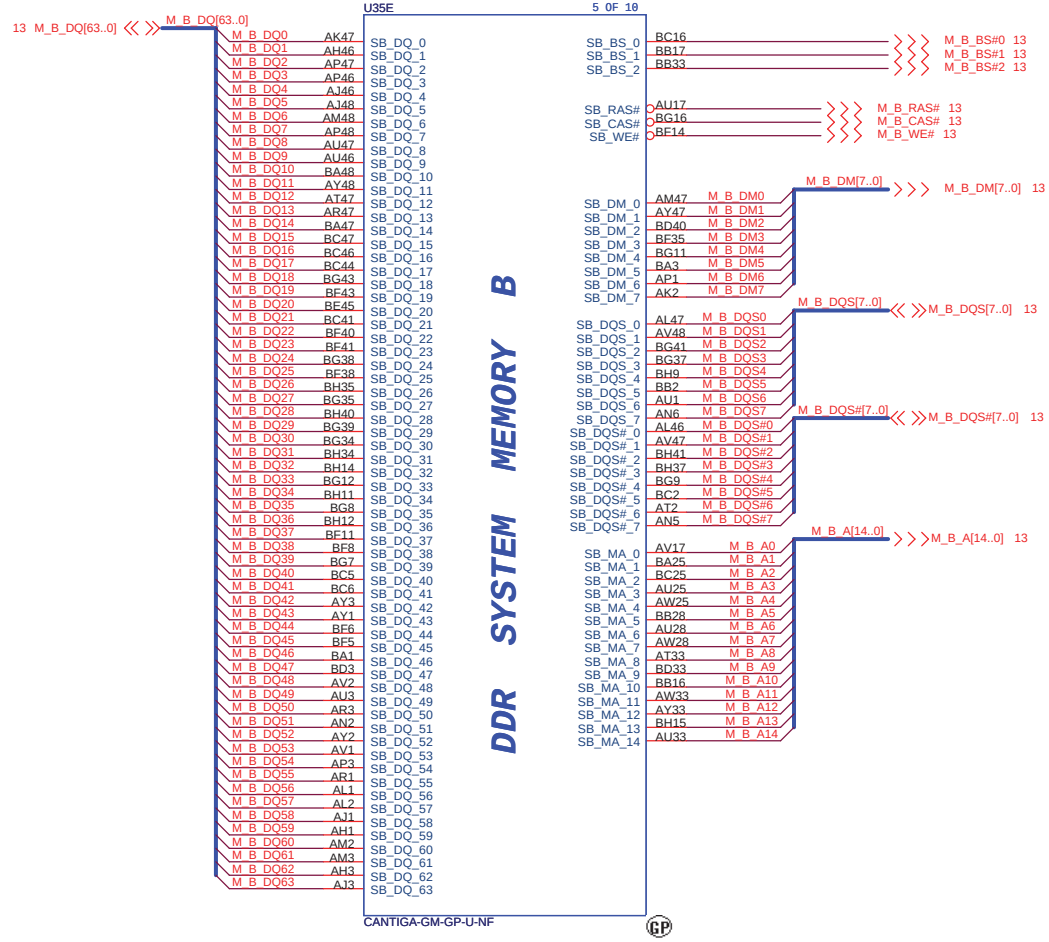


Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default)
		High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port





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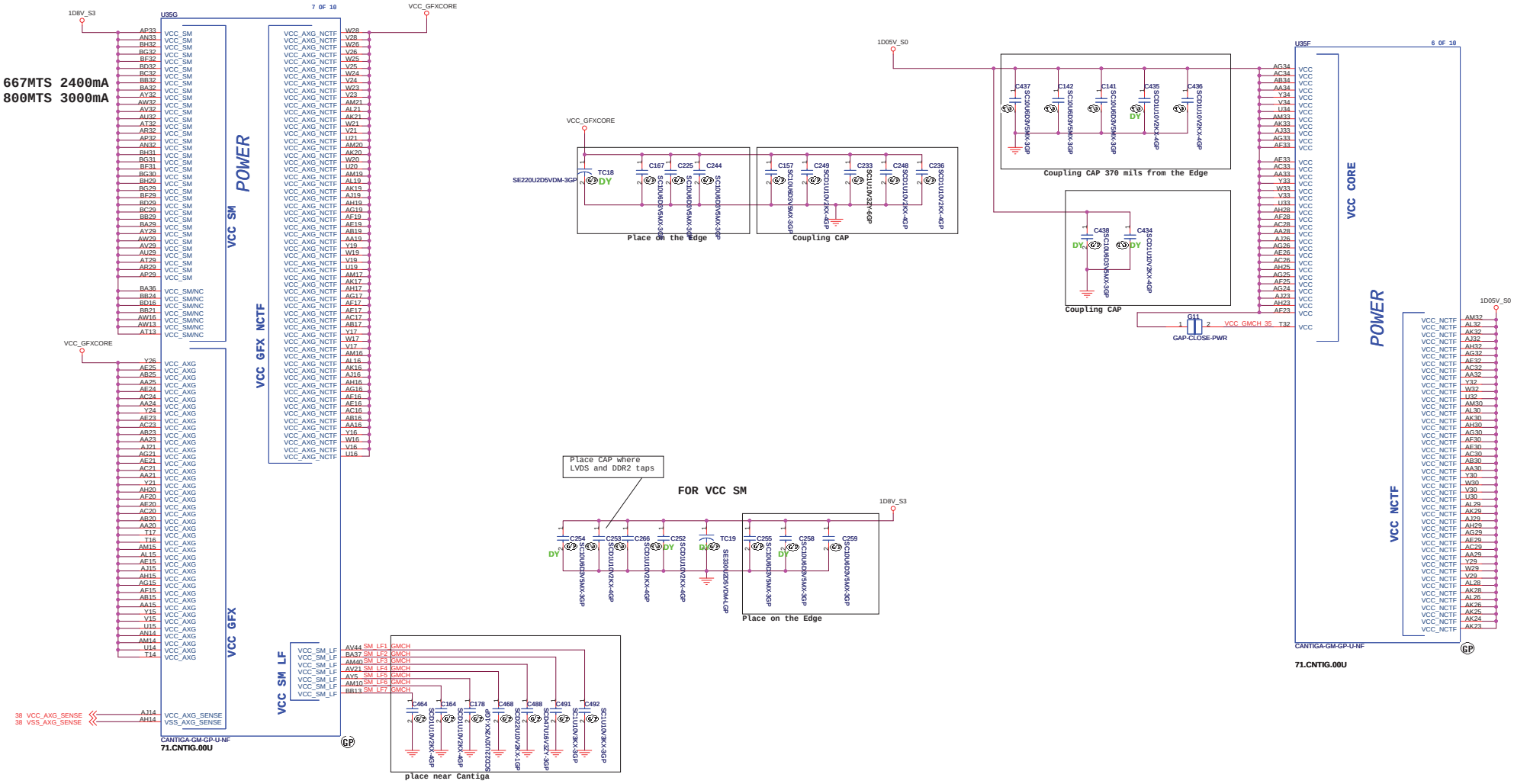
667MTS 2400mA
800MTS 3000mA



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Title: Cantiga (4 of 6)

Size | Document Number: Cathedral Peak | Rev: SA

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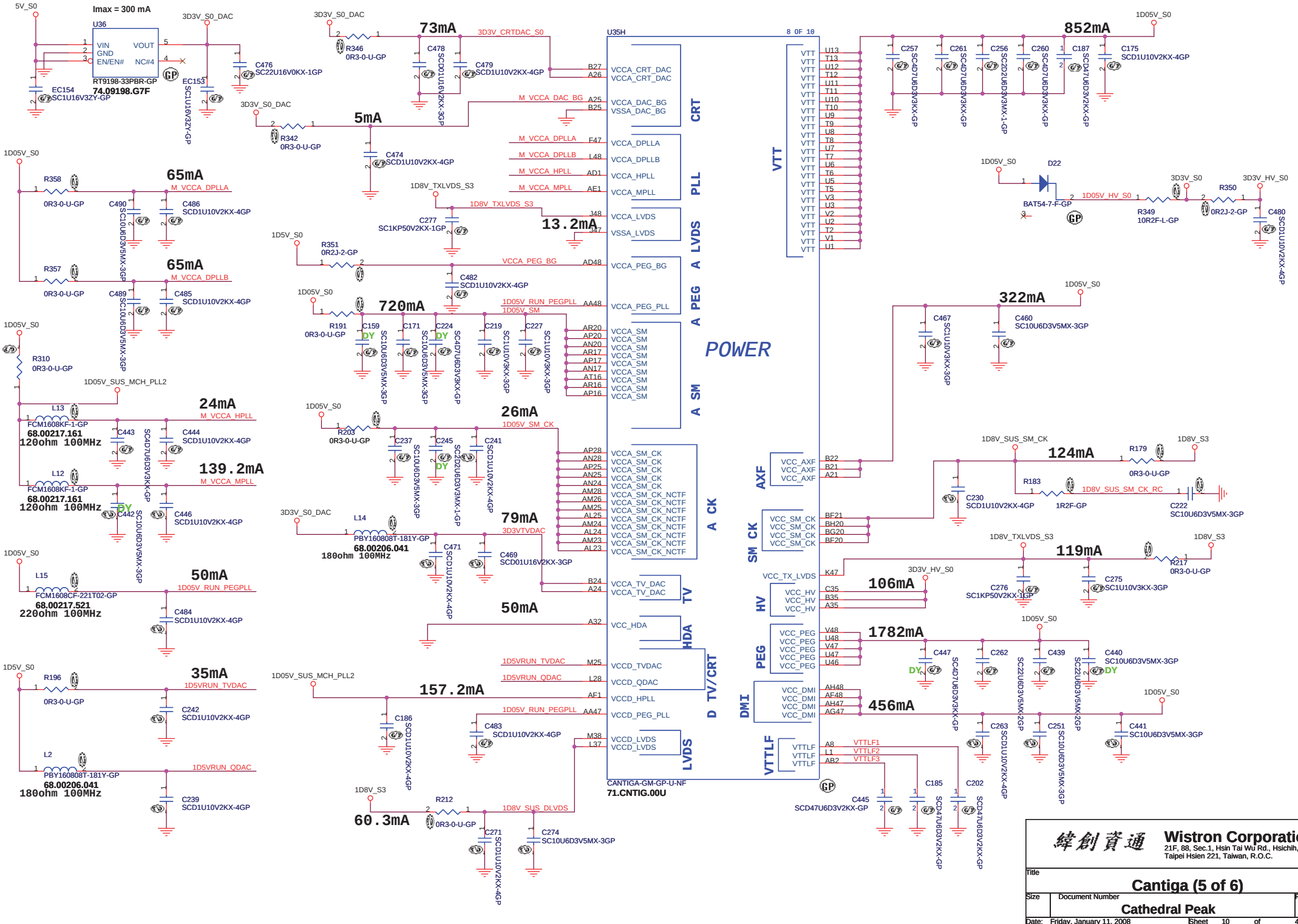

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Title: Cantiga (5 of 6)
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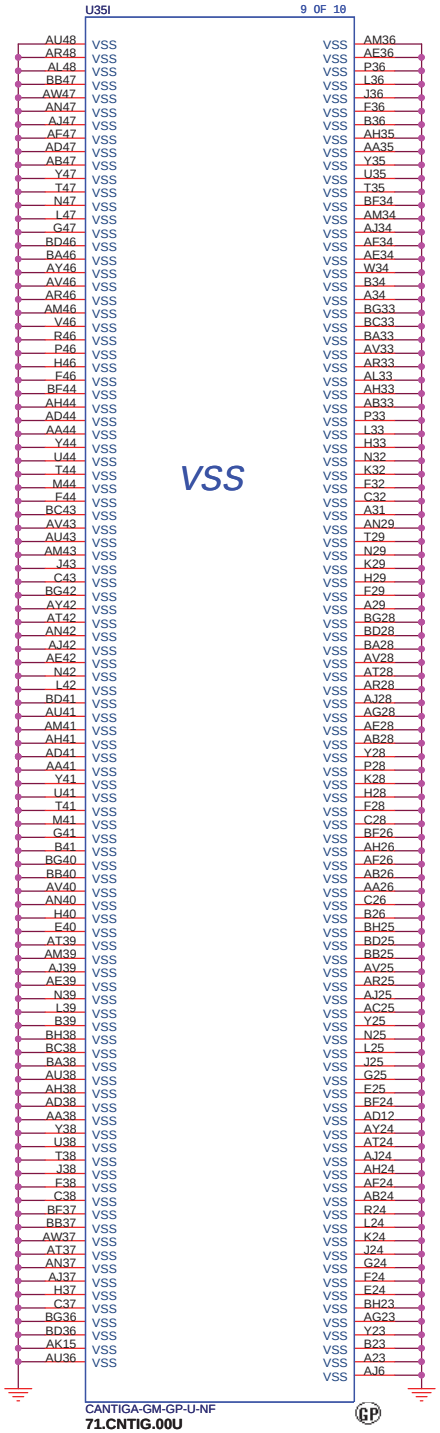

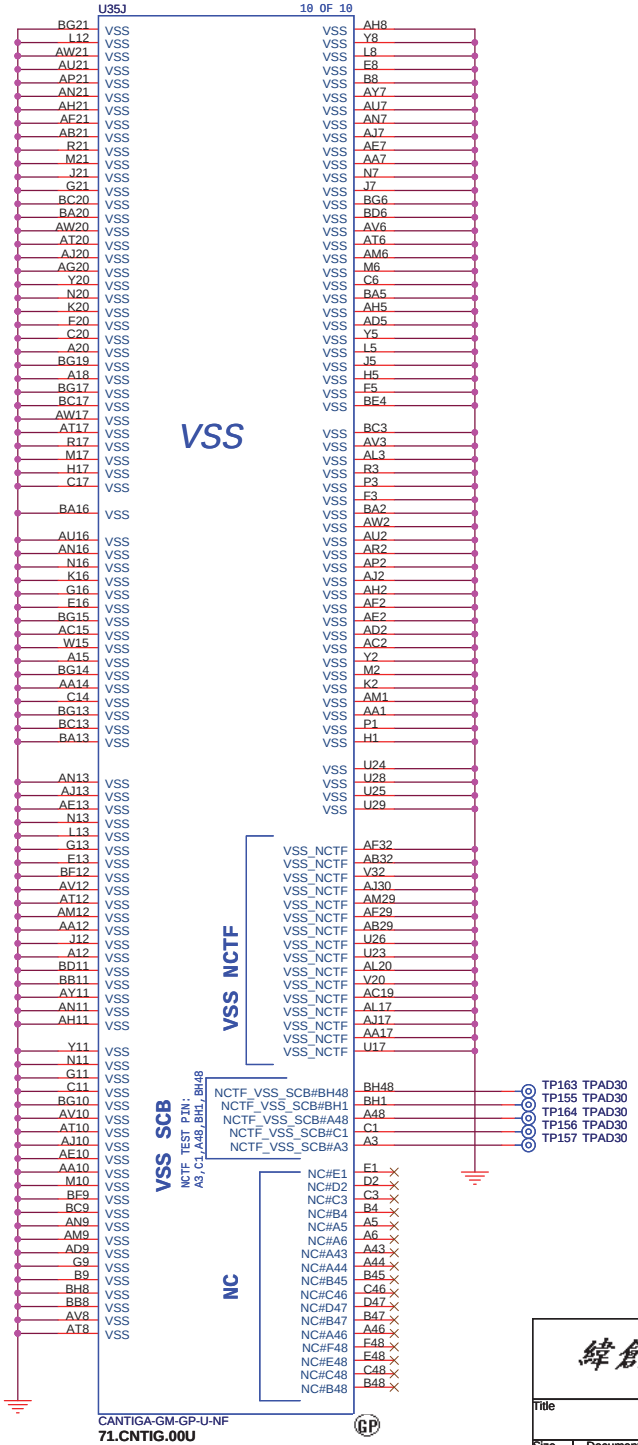

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Title	**Cantiga (6 of 6)**	
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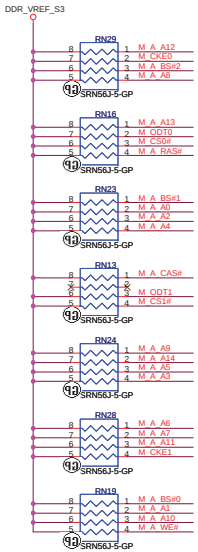
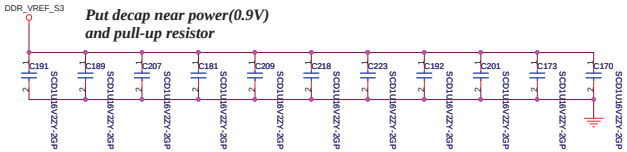
PARALLEL TERMINATION

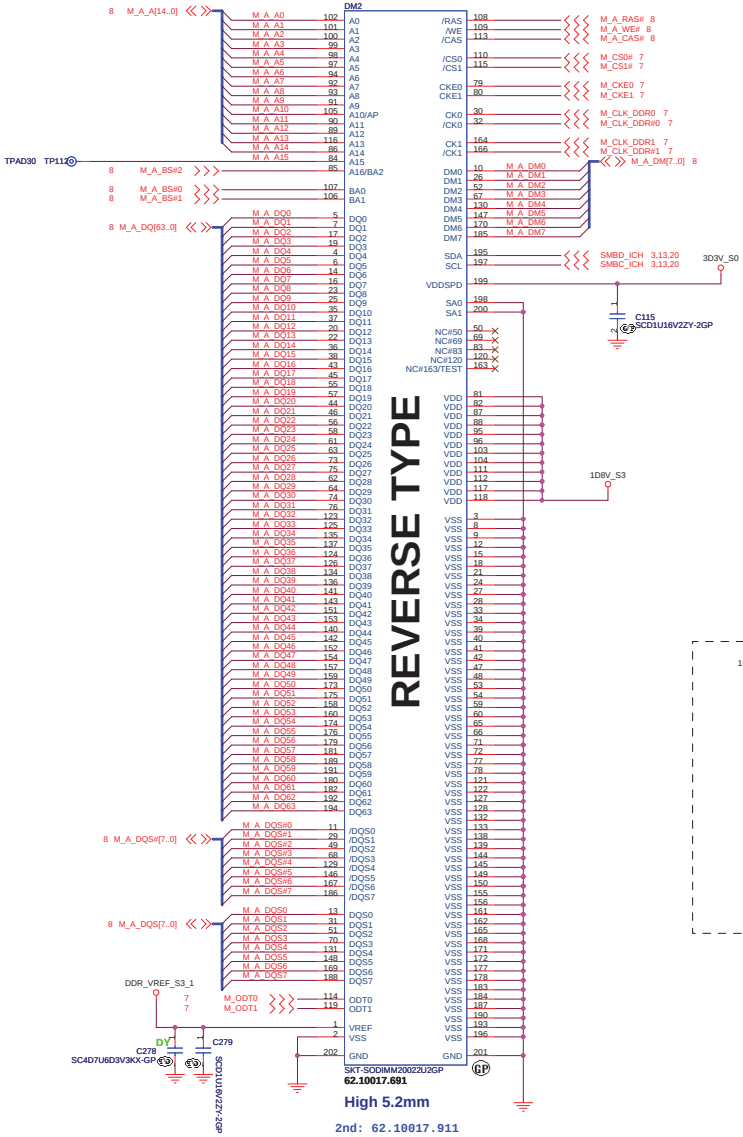
Put decap near power(0.9V) and pull-up resistor

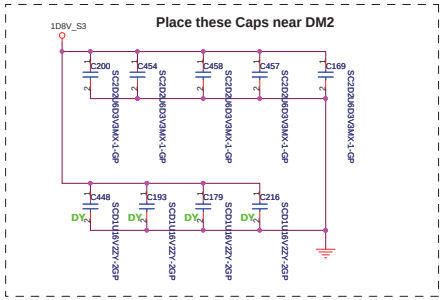


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor







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Title	DDR2 Socket 1 (DM2)	
Size	Document Number: Cathedral Peak	Rev: SA
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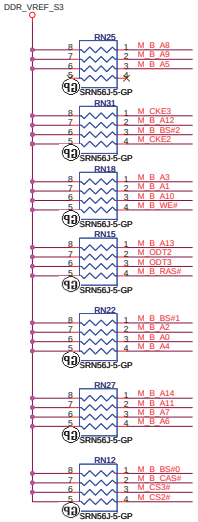
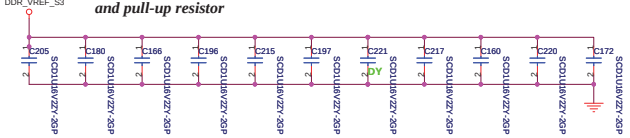
PARALLEL TERMINATION

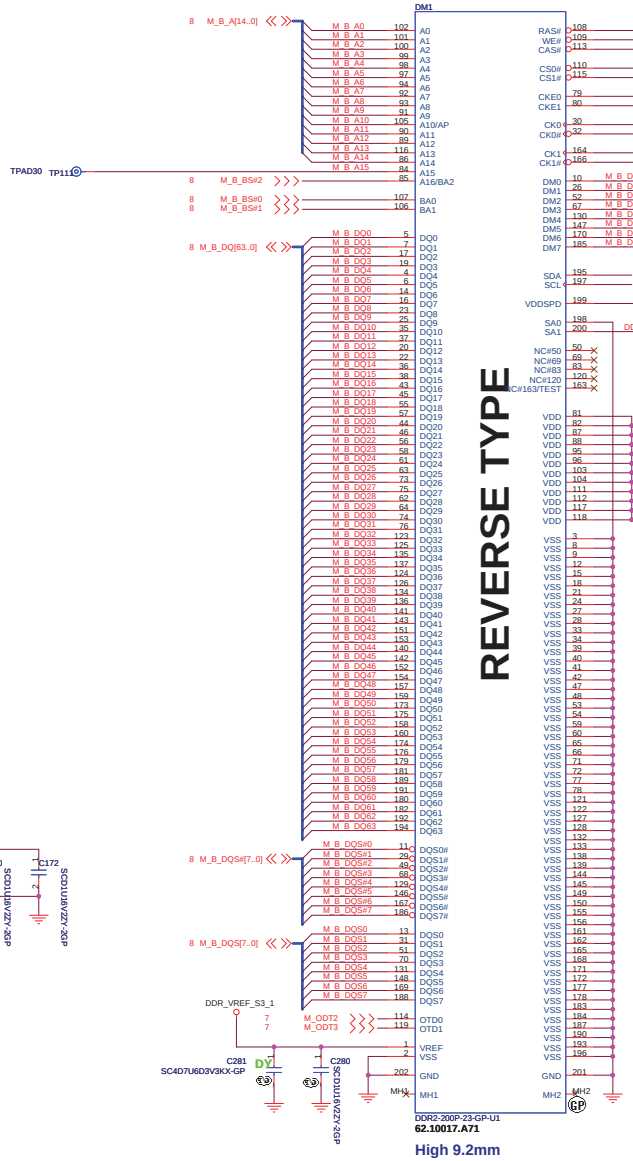
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

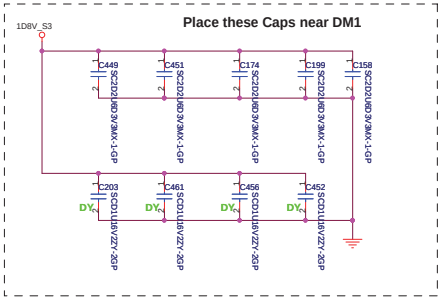
Put decap near power(0.9V) and pull-up resistor





High 9.2mm

2nd: 62.10017.B51



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Title: **DDR2 Socket 0 (DM1)**

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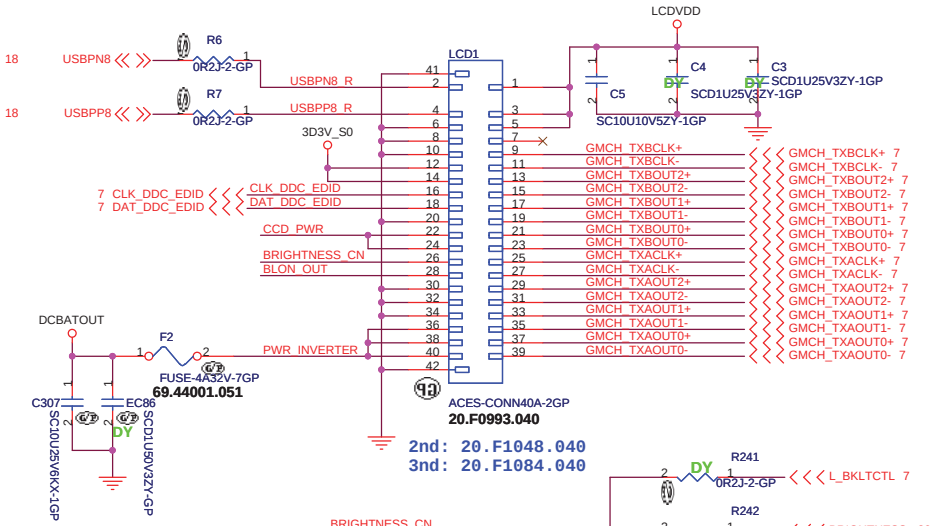
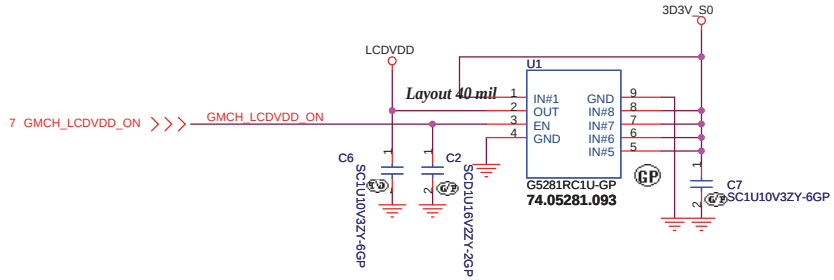
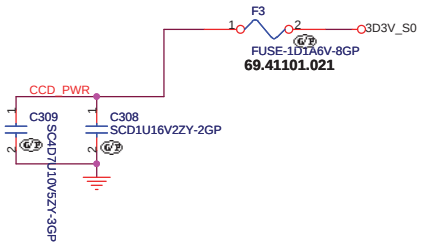
LCD/INVERTER/CCD CONN



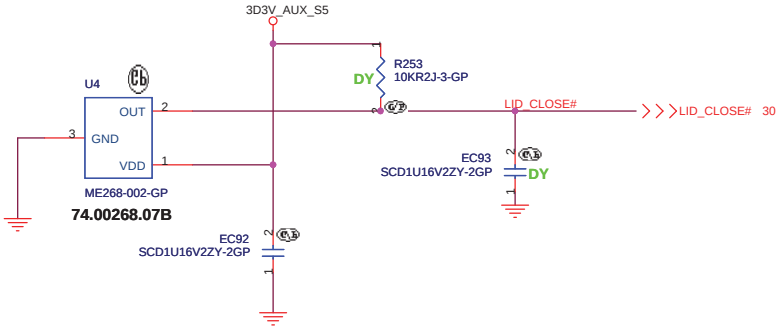




Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch

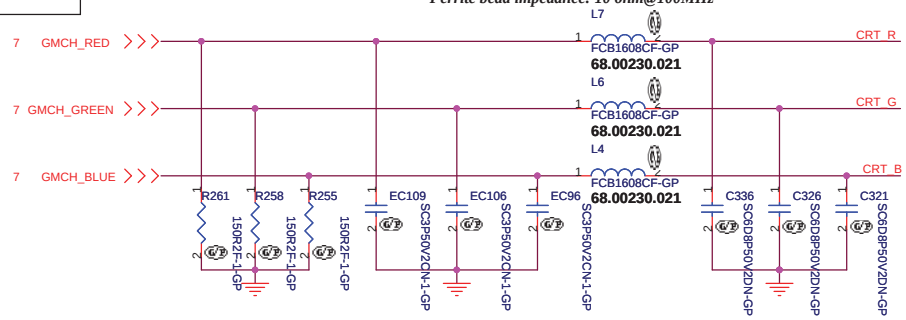


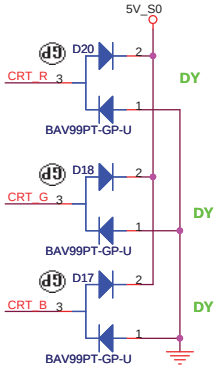
74.00268.A7B
74.00268.C7B

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: LCD CONN			
Size	Document Number: Cathedral Peak		Rev: SA
Date: Friday, January 11, 2008	Sheet 14 of 41		

Layout Note:
Place these resistors close to the CRT-out connector

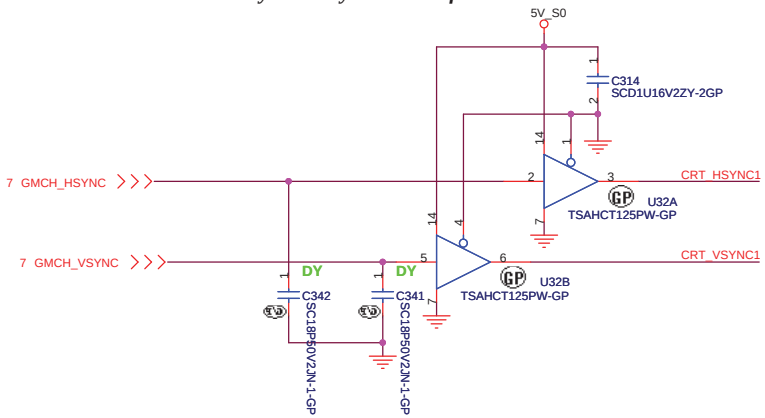
Ferrite bead impedance: 10 ohm@100MHz



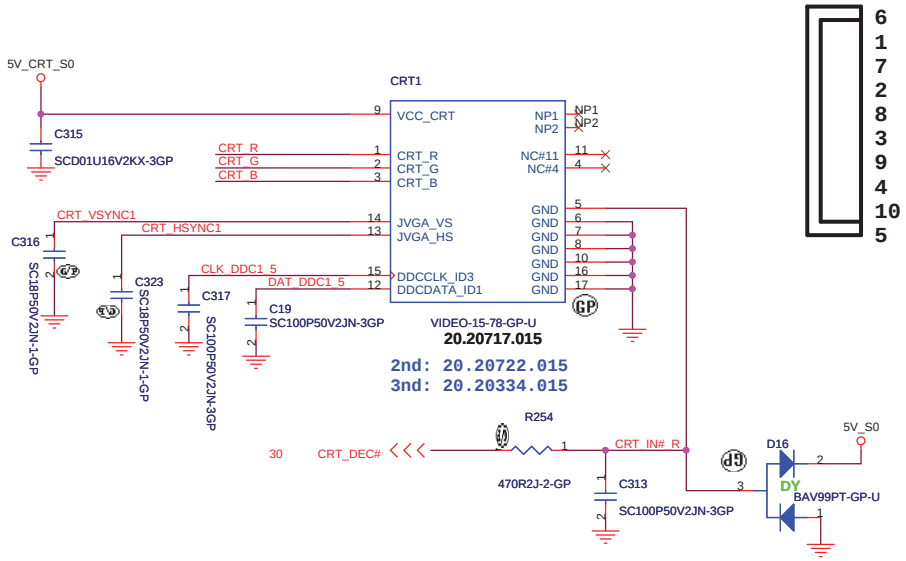


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

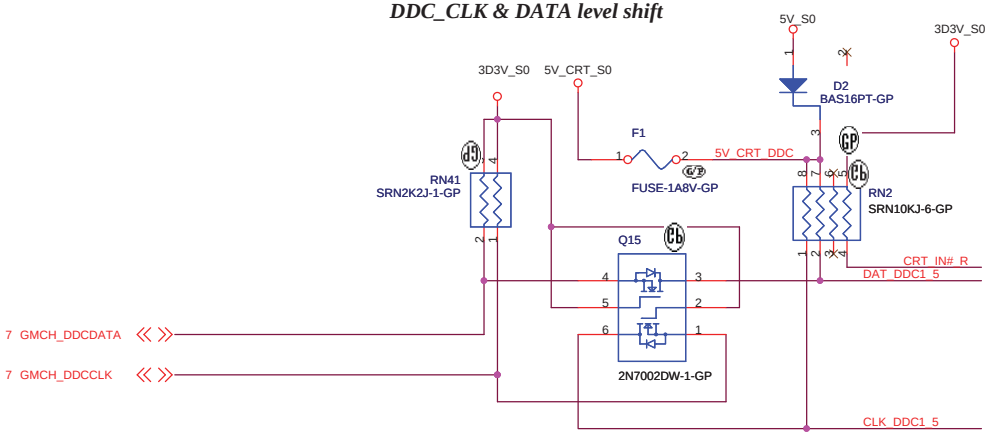
Hsync & Vsync level shift



CRT I/F & CONNECTOR



DDC_CLK & DATA level shift



緯創資通 **Wistron Corporation**
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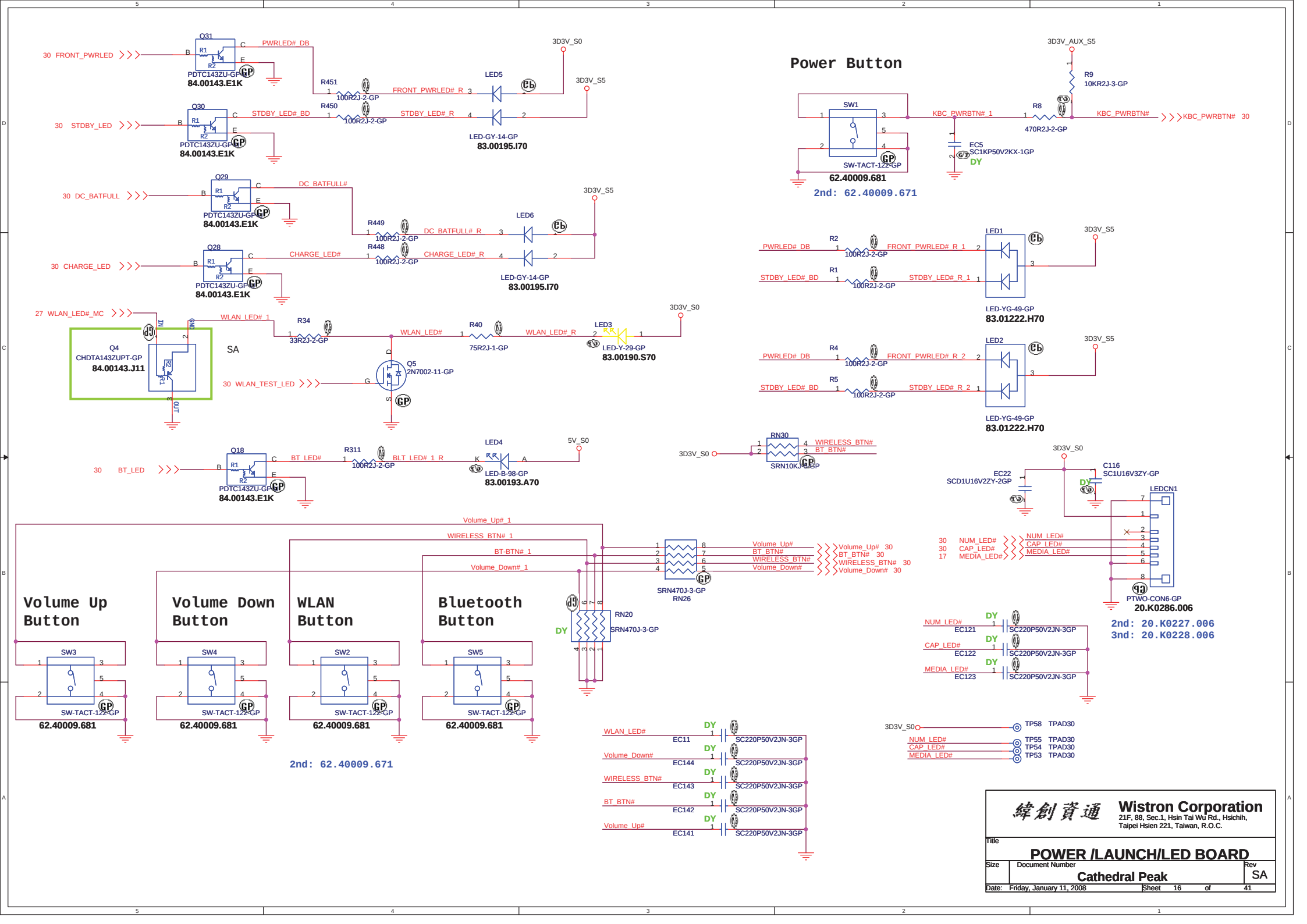
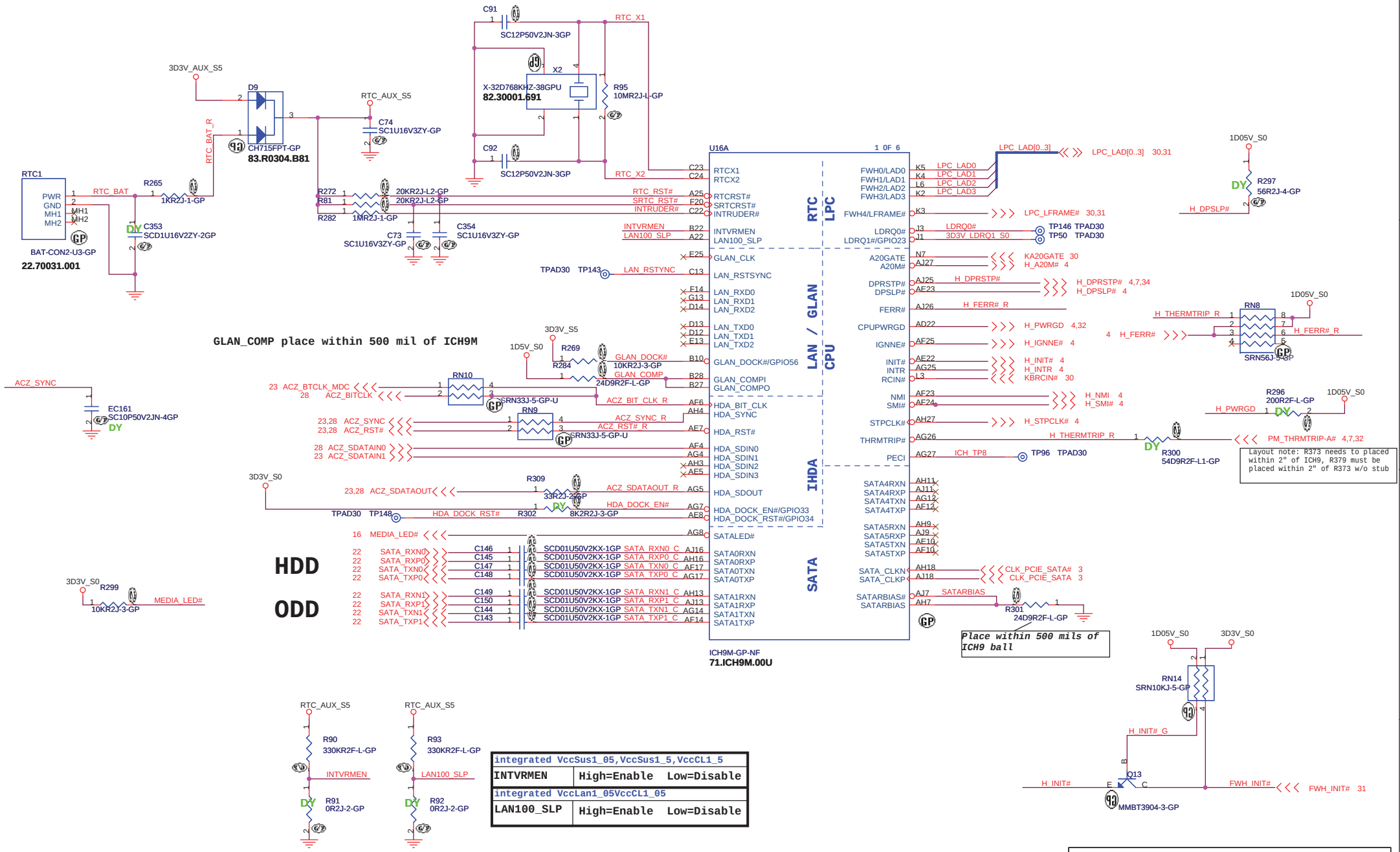
Title	**CRT Connector**	
Size	Document Number: **Cathedral Peak**	Rev: SA
Date: Friday, January 11, 2008	Sheet 15 of 41	


Power Button
Volume Up Button
Volume Down Button
WLAN Button
Bluetooth Button
Q31
PDTC143ZU-GP
84.00143.E1K
Q30
Q29
Q28
Q18
Q4
CHDTA143ZUPT-GP
84.00143.J11
SA
Q5
2N7002-11-GP
LED5
LED6
LED1
LED2
LED3
LED4
LED-GY-14-GP
83.00195.I70
LED-YG-49-GP
83.01222.H70
LED-Y-29-GP
83.00190.S70
LED-B-98-GP
83.00193.A70
SW1
SW-TACT-122-GP
62.40009.681
2nd: 62.40009.671
SW2
SW3
SW4
SW5
RN20
RN26
SRN470J-3-GP
RN30
SRN10KJ-3-GP
LEDCN1
PTWO-CON6-GP
20.K0286.006
2nd: 20.K0227.006
3rd: 20.K0228.006
EC5
SC1KP50V2KX-1GP
EC22
SCD1U16V2ZY-2GP
C116
SC1U16V3ZY-GP
EC11
EC121
EC122
EC123
EC141
EC142
EC143
EC144
SC220P50V2JN-3GP
TP58
TP55
TP54
TP53
TPAD30
R9
10KR2J-3-GP
R8
470R2J-2-GP
100R2J-2-GP
33R2J-1-GP
75R2J-1-GP
3D3V_S0
3D3V_S5
3D3V_AUX_S5
5V_S0
FRONT_PWRLED# R
STDBY_LED# R
DC_BATFULL# R
CHARGE_LED# R
WLAN_LED# R
BLT_LED# 1 R
FRONT_PWRLED# R 1
STDBY_LED# R 1
FRONT_PWRLED# R 2
STDBY_LED# R 2
KBC_PWRBTN# 1
KBC_PWRBTN#
WIRELESS_BTN# 1
BT-BTN# 1
Volume_Up# 1
Volume_Down# 1
WIRELESS_BTN#
BT_BTN#
Volume_Up#
Volume_Down#
NUM_LED#
CAP_LED#
MEDIA_LED#
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER /LAUNCH/LED BOARD
Size
Document Number
Cathedral Peak
Rev
SA
Date: Friday, January 11, 2008
Sheet 16 of 41


GLAN_COMP place within 500 mil of ICH9M
HDD
ODD
U16A
ICH9M-GP-NF
71.ICH9M.00U
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
Place within 500 mils of ICH9 ball
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
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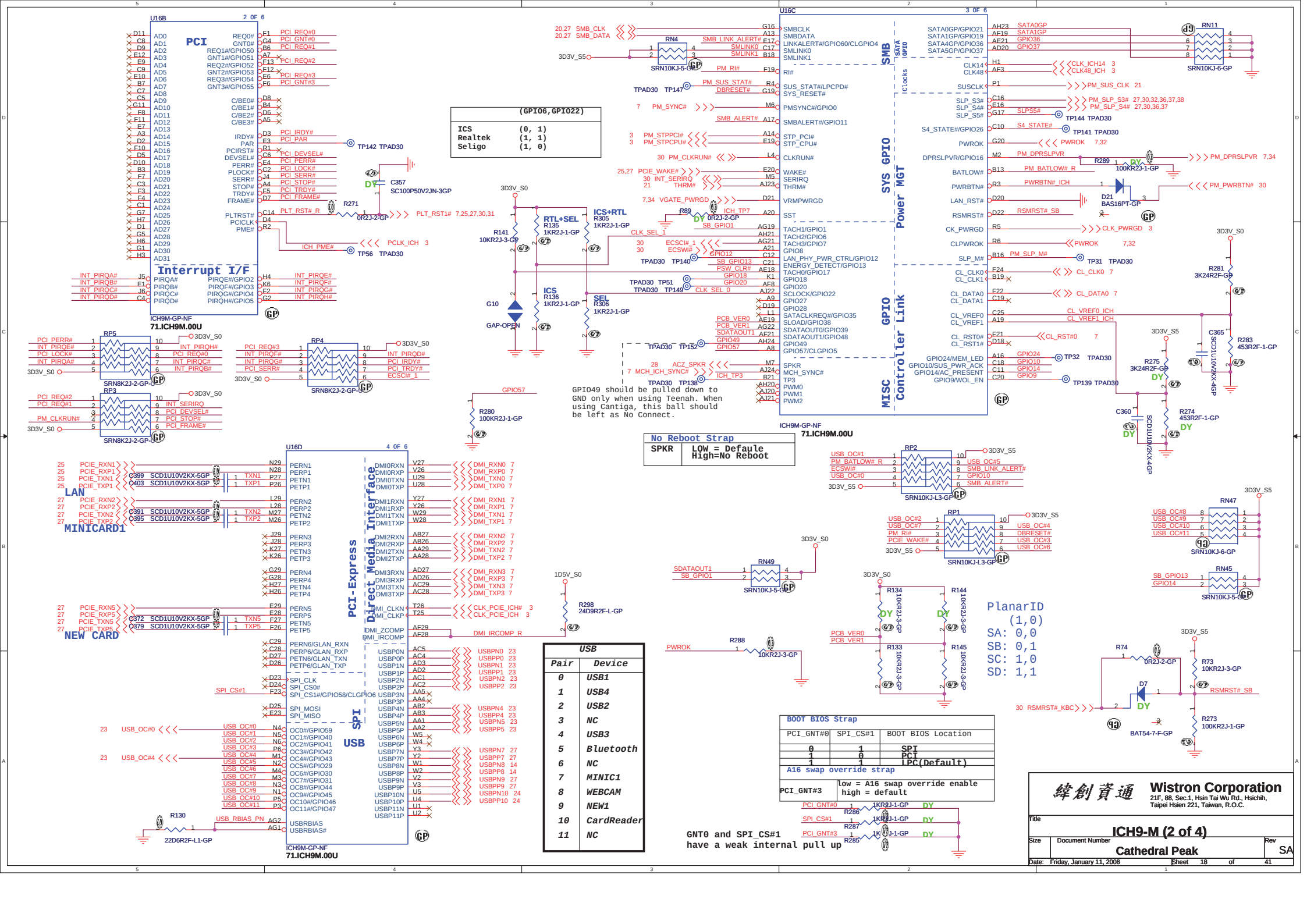
ICH9-M (1 of 4)
Cathedral Peak
SA
Date: Friday, January 11, 2008
Sheet 17 of 41


U16B
2 0F 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
U16C
3 0F 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
U16D
4 0F 6
PCI-Express
Direct Media Interface
SPI
USB
ICH9M-GP-NF
71.ICH9M.00U
(GPIO6,GPIO22)
ICS (0, 1)
Realtek (1, 0)
Seligo (0, 0)
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
USB
Pair Device
0 USB1
1 USB4
2 USB2
3 NC
4 USB3
5 Bluetooth
6 NC
7 MINIC1
8 WEBCAM
9 NEW1
10 CardReader
11 NC
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
GNT0 and SPI_CS#1 have a weak internal pull up
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
Wistron Corporation
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Title
ICH9-M (2 of 4)
Size
Document Number
Cathedral Peak
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SA
Date: Friday, January 11, 2008
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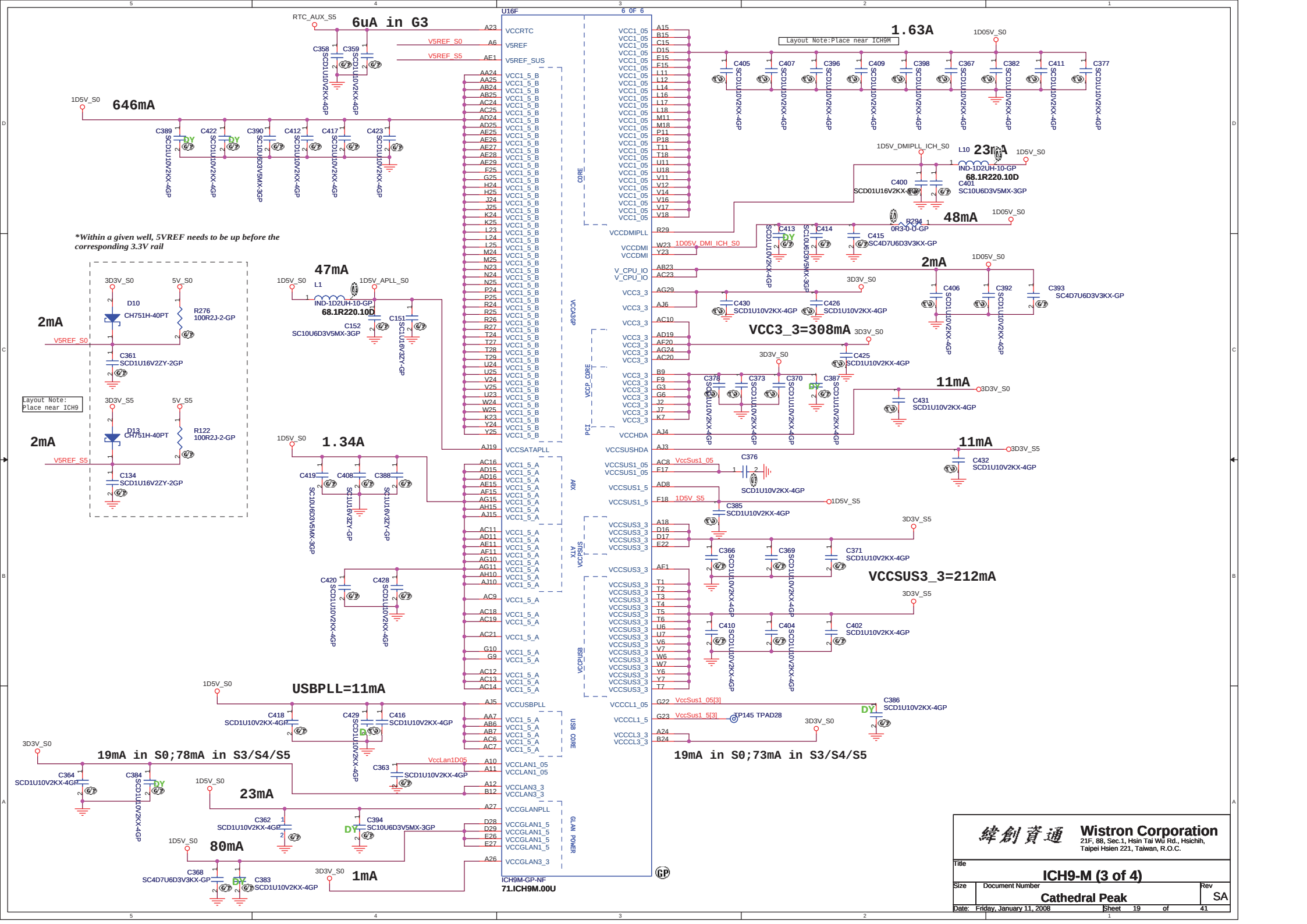
U16F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
6uA in G3
RTC_AUX_S5
V5REF_S0
V5REF_S5
646mA
1D5V_S0
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
2mA
3D3V_S0
5V_S0
D10
CH751H-40PT
R276
100R2J-2-GP
V5REF_S0
C361
SCD1U16V2ZY-2GP
Layout Note:
Place near ICH9
3D3V_S5
5V_S5
D13
CH751H-40PT
R122
100R2J-2-GP
V5REF_S5
C134
SCD1U16V2ZY-2GP
47mA
1D5V_APLL_S0
L1
IND-1D2UH-10-GP
68.1R220.10D
C152
SC10U6D3V5MX-3GP
C151
SC1U16V2ZY-GP
1.34A
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
VccLan1D05
1.63A
Layout Note:Place near ICH9M
23mA
1D5V_DMIPLL_ICH_S0
L10
IND-1D2UH-10-GP
68.1R220.10D
48mA
R294
0R3-0-U-GP
1D5V_DMI_ICH_S0
2mA
VCC3_3=308mA
11mA
11mA
VccSus1_05
VCCSUS3_3=212mA
VccSus1_05[3]
VccSus1_5[3]
TP145 TPAD28
19mA in S0;73mA in S3/S4/S5
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Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH9-M (3 of 4)
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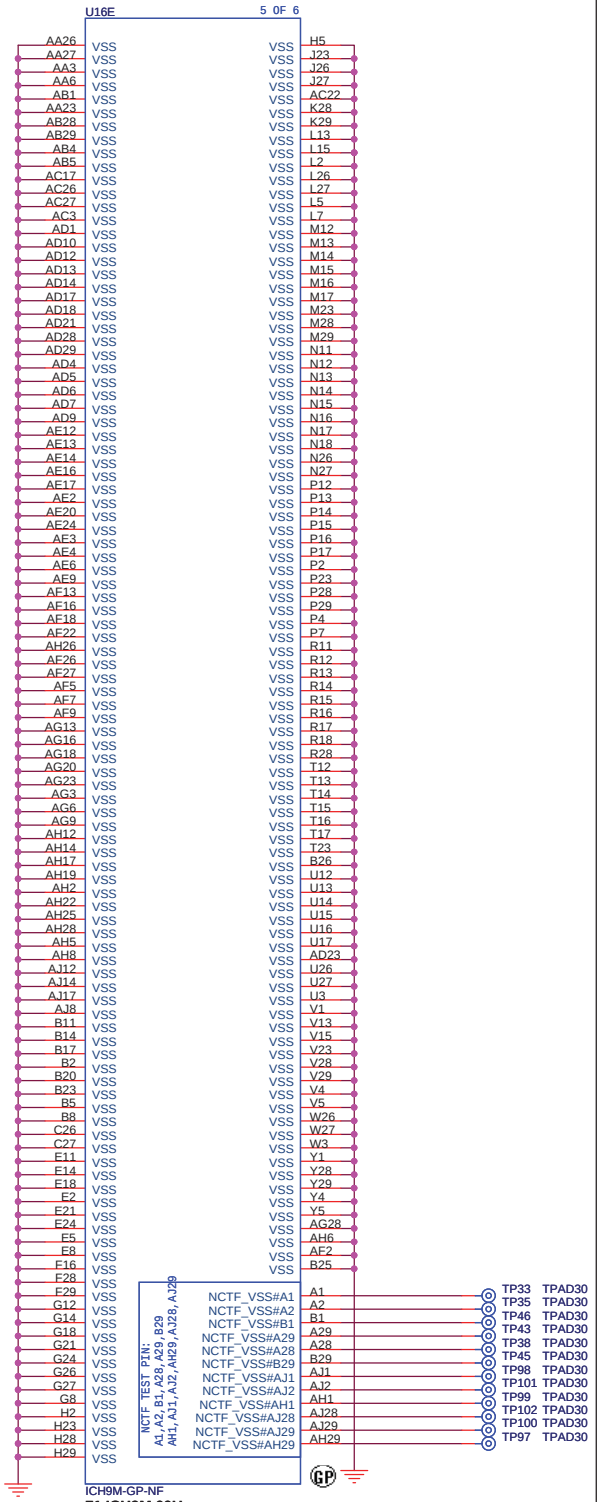

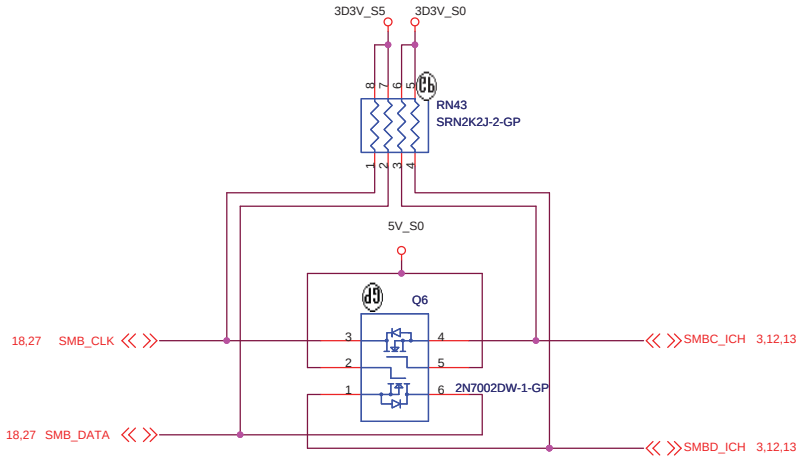

SMBUS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **ICH9-M (4 of 4)**

Size | Document Number: **Cathedral Peak** | Rev: SA

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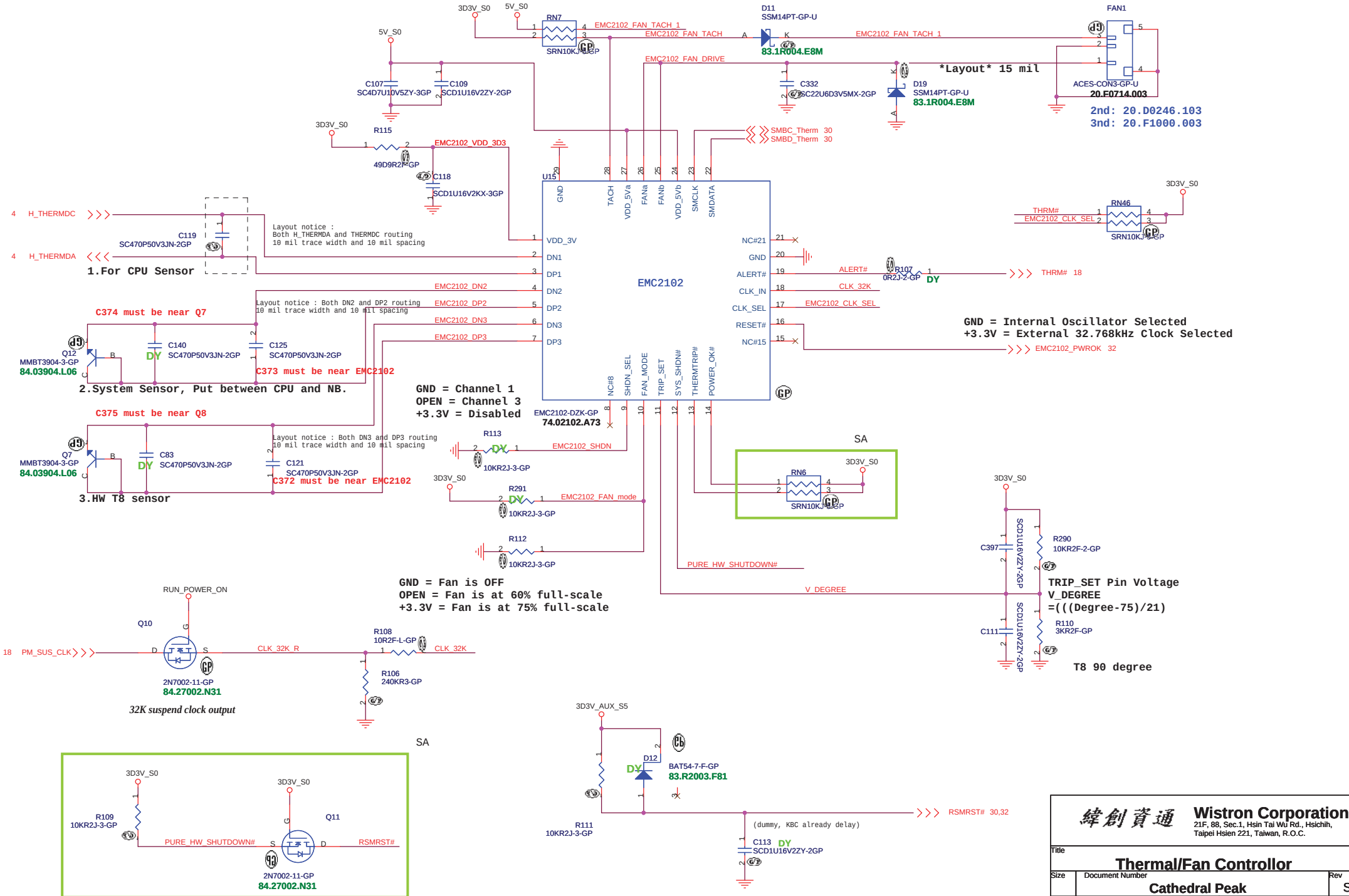

緯創資通 **Wistron Corporation**
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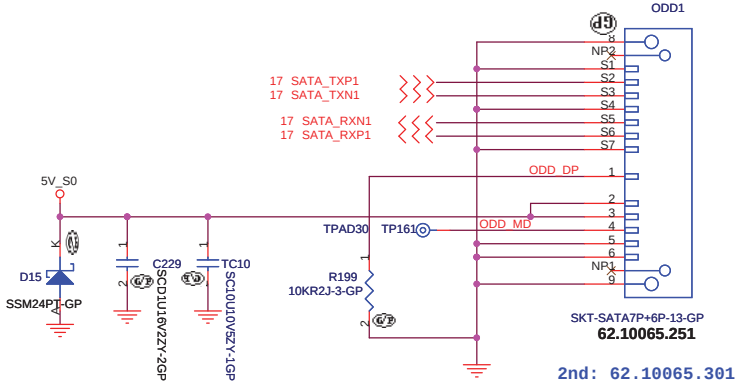
Taipei Hsien 221, Taiwan, R.O.C.

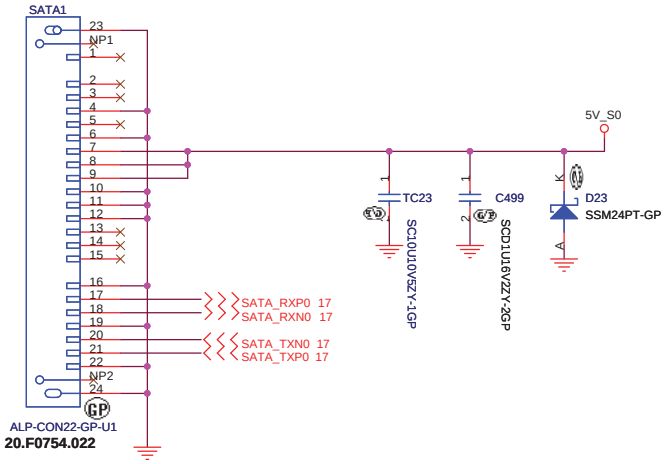
Title	**Thermal/Fan Controllor**	
Size	Document Number: **Cathedral Peak**	Rev: SA
Date: Friday, January 11, 2008	Sheet 21 of 41	

SATA ODD Connector



2nd: 62.10065.301

SATA Connector



2nd: 62.10065.151

緯創資通 **Wistron Corporation**
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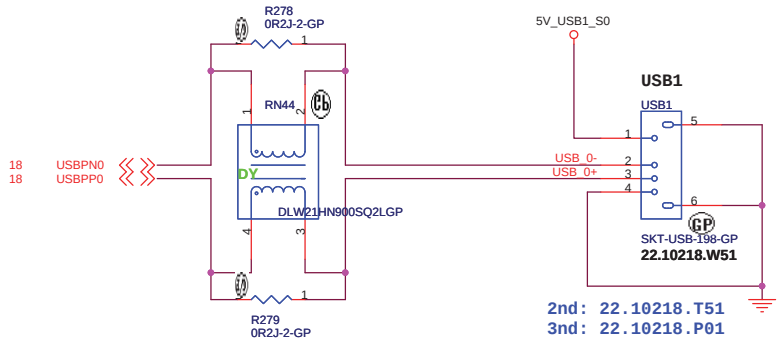
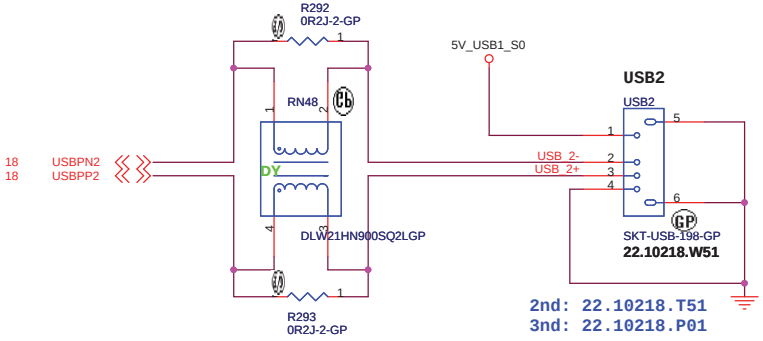
Taipei Hsien 221, Taiwan, R.O.C.

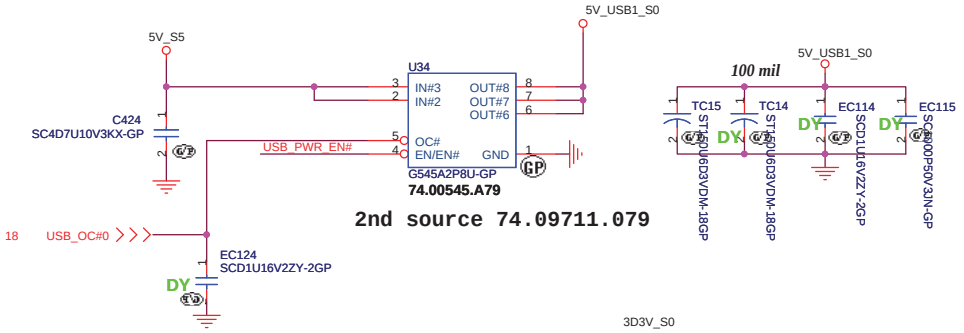
Title: HDD & CDROM		
Size	Document Number: Cathedral Peak	Rev: SA
Date: Friday, January 11, 2008	Sheet 22 of 41	

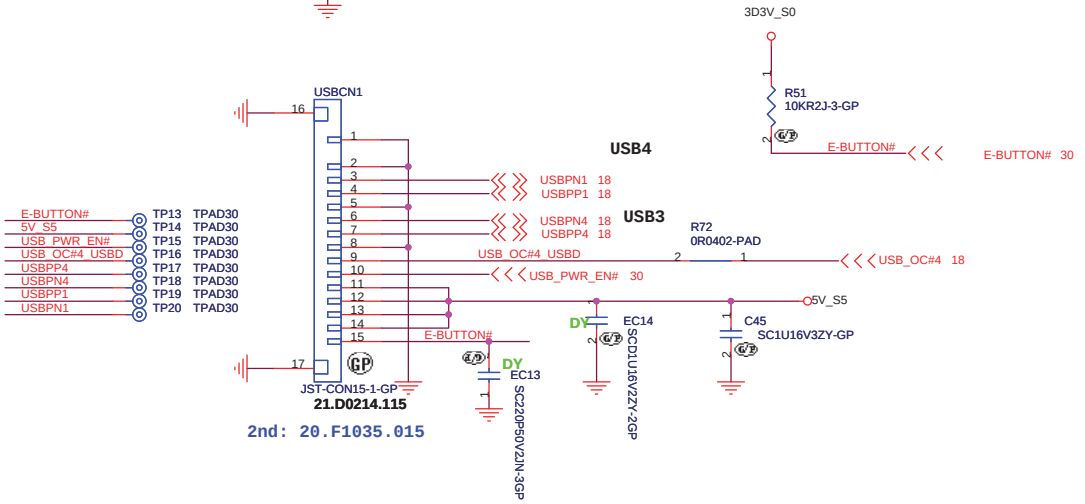
Co-Layout Common Mode Choke and 0 Ohm





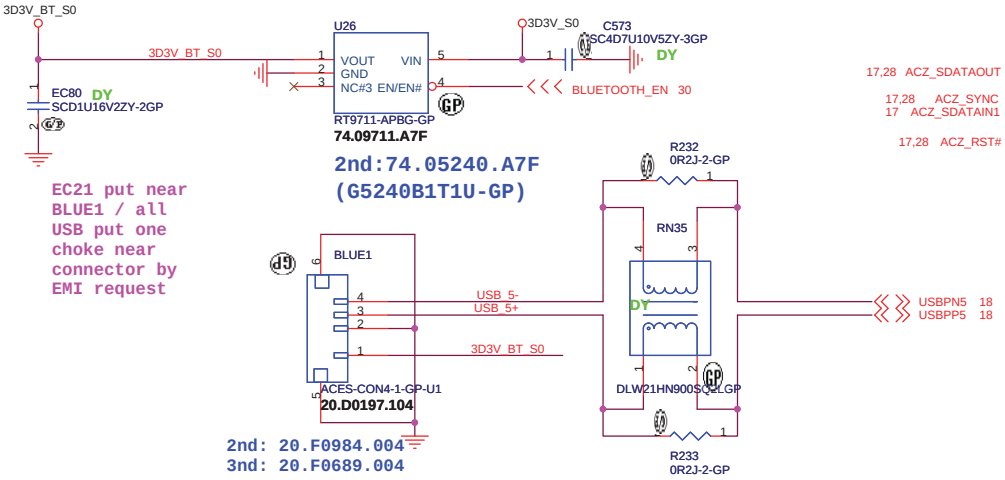
Co-Layout Common Mode Choke and 0 Ohm



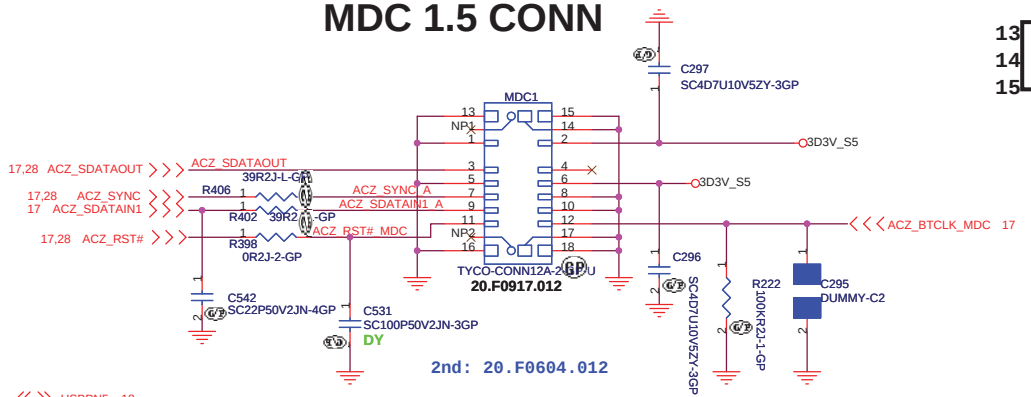


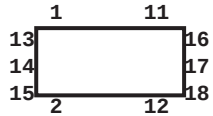
BLUETOOTH MODULE

1.5A / High Active Voltage 2V



MDC 1.5 CONN





USB_5-
USB_5+
3D3V_BT_S0
TP134 TPAD30
TP136 TPAD30
TP133 TPAD30

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB/BLUETOOTH/MDC

Size	Document Number	Rev
	Cathedral Peak	SA

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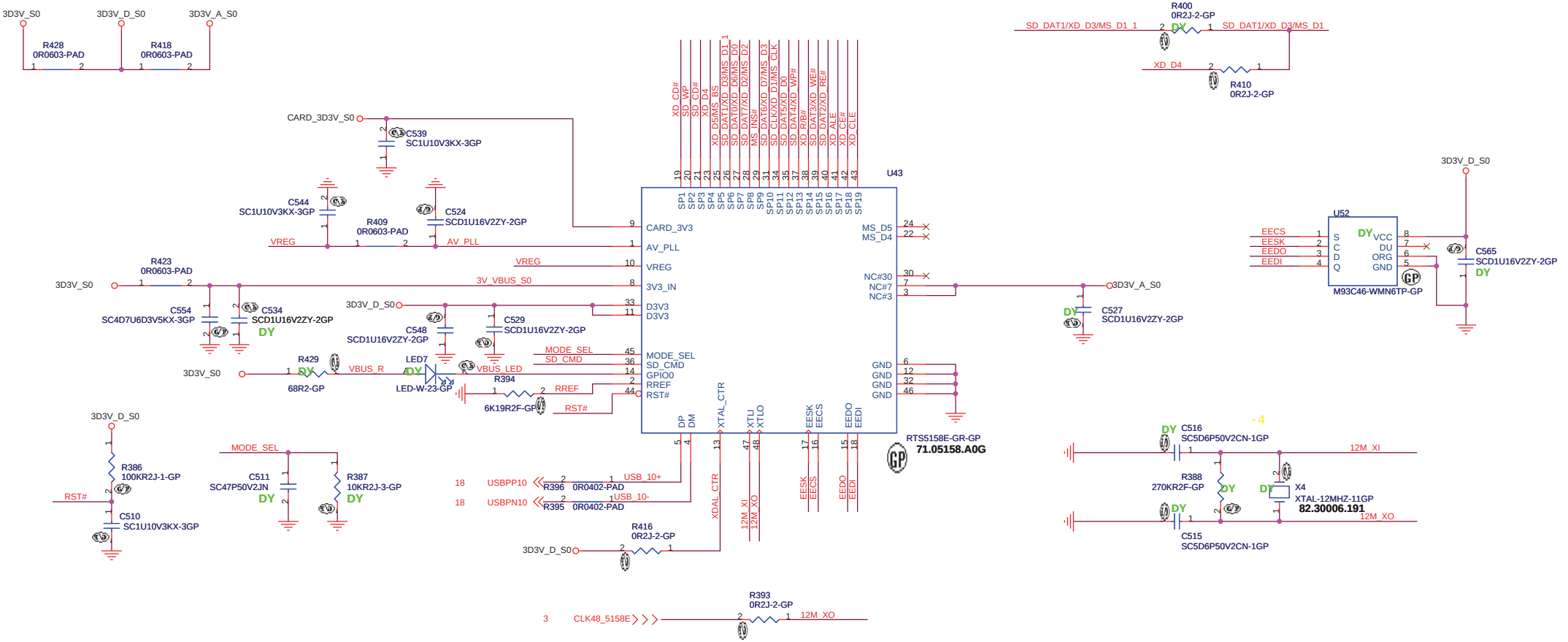
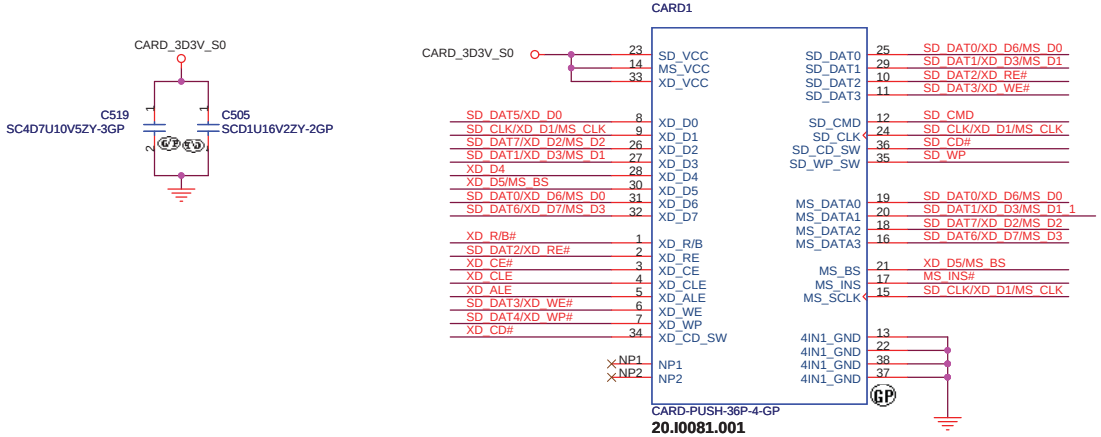


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



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Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER- RTS5158E

Size | Document Number: Cathedral Peak | Rev: SA

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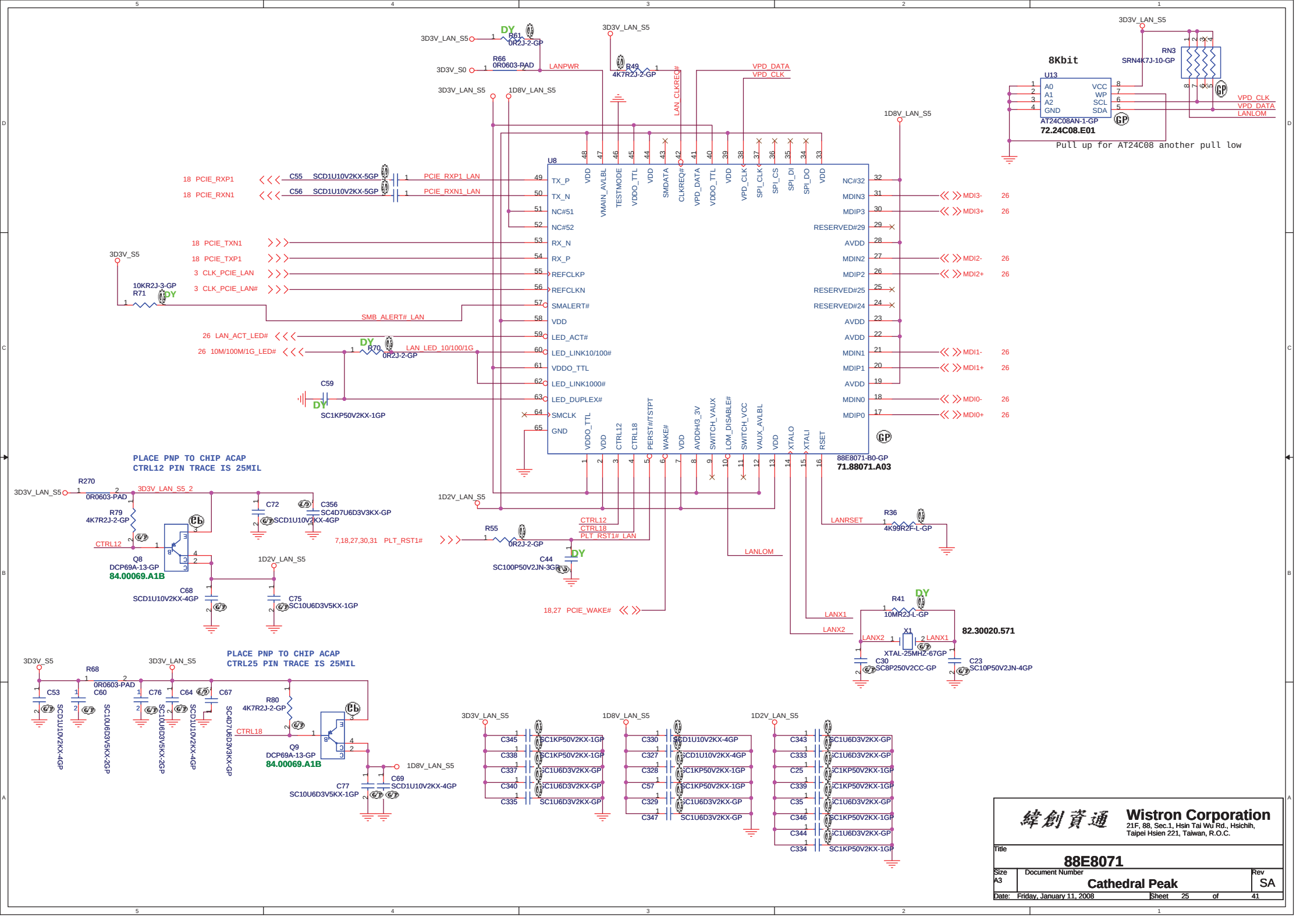
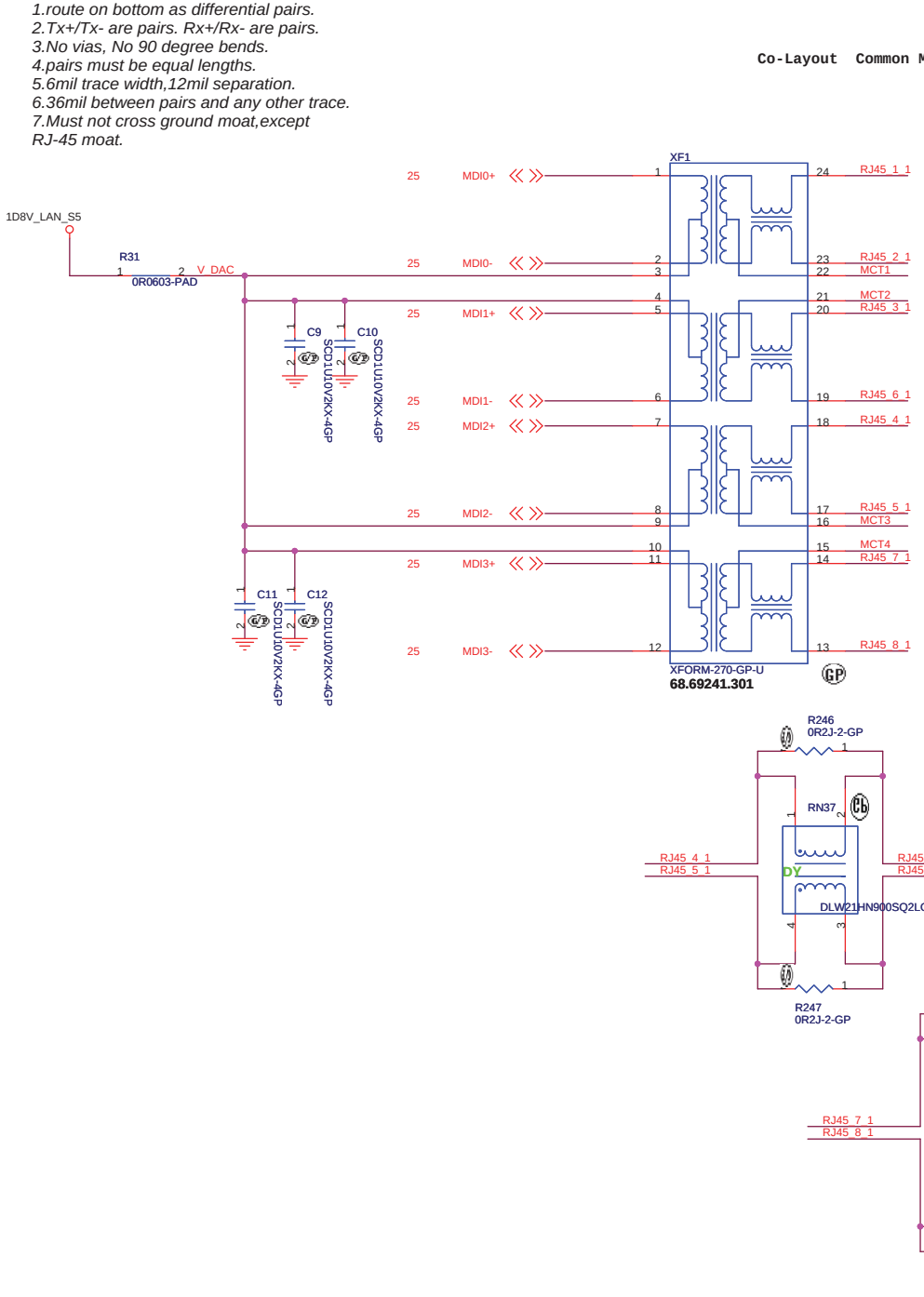
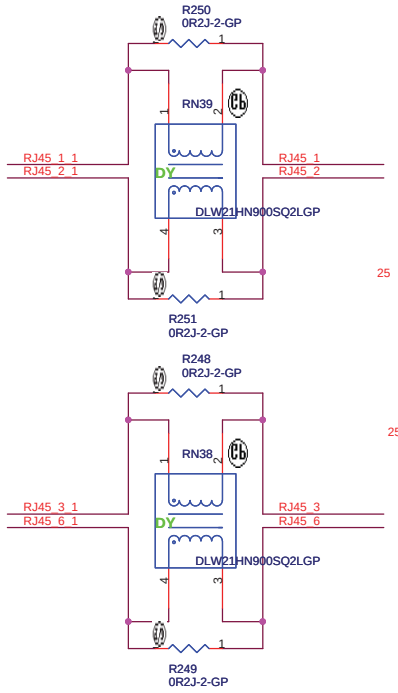

3D3V_LAN_S5
R61
0R2J-2-GP
DY
3D3V_S0
R66
0R0603-PAD
LANPWR
R49
4K7R2J-2-GP
VPD_DATA
VPD_CLK
LAN_CLKREQ#
1D8V_LAN_S5
8Kbit
U13
A0
A1
A2
GND
VCC
WP
SCL
SDA
AT24C08AN-1-GP
72.24C08.E01
RN3
SRN4K7J-10-GP
Pull up for AT24C08 another pull low
U8
TX_P
TX_N
NC#51
NC#52
RX_N
RX_P
REFCLKP
REFCLKN
SMALERT#
LED_ACT#
LED_LINK10/100#
VDDO_TTL
LED_LINK1000#
LED_DUPLEX#
SMCLK
GND
NC#32
MDIN3
MDIP3
RESERVED#29
AVDD
MDIN2
MDIP2
RESERVED#25
RESERVED#24
MDIN1
MDIP1
MDIN0
MDIP0
88E8071-B0-GP
71.88071.A03
18 PCIE_RXP1
18 PCIE_RXN1
C55 SCD1U10V2KX-5GP
C56 SCD1U10V2KX-5GP
PCIE_RXP1_LAN
PCIE_RXN1_LAN
18 PCIE_TXN1
18 PCIE_TXP1
3 CLK_PCIE_LAN
3 CLK_PCIE_LAN#
10KR2J-3-GP
R71
SMB_ALERT# LAN
26 LAN_ACT_LED#
26 10M/100M/1G_LED#
R70
0R2J-2-GP
LAN_LED_10/100/1G
C59
SC1KP50V2KX-1GP
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
R270
0R0603-PAD
3D3V_LAN_S5_2
R79
4K7R2J-2-GP
CTRL12
Q8
DCP69A-13-GP
84.00069.A1B
C72
SCD1U10V2KX-4GP
C356
SC4D7U6D3V3KX-GP
C68
SCD1U10V2KX-4GP
C75
SC10U6D3V5KX-1GP
1D2V_LAN_S5
7,18,27,30,31 PLT_RST1#
R55
0R2J-2-GP
C44
SC100P50V2JN-3GP
CTRL12
CTRL18
PLT_RST1# LAN
LANLOM
18,27 PCIE_WAKE#
LANRSET
R36
4K99R2F-L-GP
R41
10MR2J-L-GP
LANX1
LANX2
X1
XTAL-25MHZ-67GP
82.30020.571
C30
SC8P250V2CC-GP
C23
SC10P50V2JN-4GP
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
R68
0R0603-PAD
C53
C60
C76
C64
C67
R80
4K7R2J-2-GP
CTRL18
Q9
DCP69A-13-GP
84.00069.A1B
C77
SC10U6D3V5KX-1GP
C69
SCD1U10V2KX-4GP
C345
C338
C337
C340
C335
C330
C327
C328
C57
C329
C347
C343
C333
C25
C339
C35
C346
C344
C334
SC1KP50V2KX-1GP
SC1U6D3V2KX-GP
SCD1U10V2KX-4GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
88E8071
Size A3
Document Number
Cathedral Peak
Rev SA
Date: Friday, January 11, 2008
Sheet 25 of 41

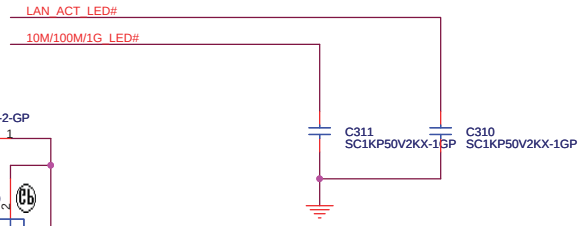
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

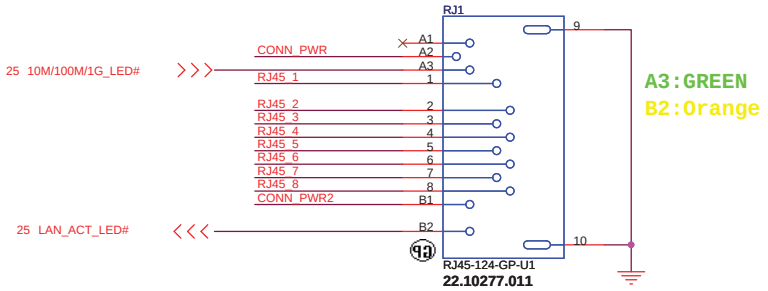
Co-Layout Common Mode Choke and 0 Ohm







LAN Connector

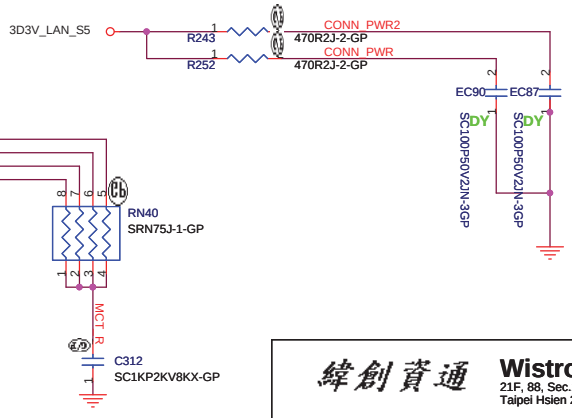


2nd: 22.10277.061

LAN Link: Green(A3), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(B2), when LAN is transfering data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



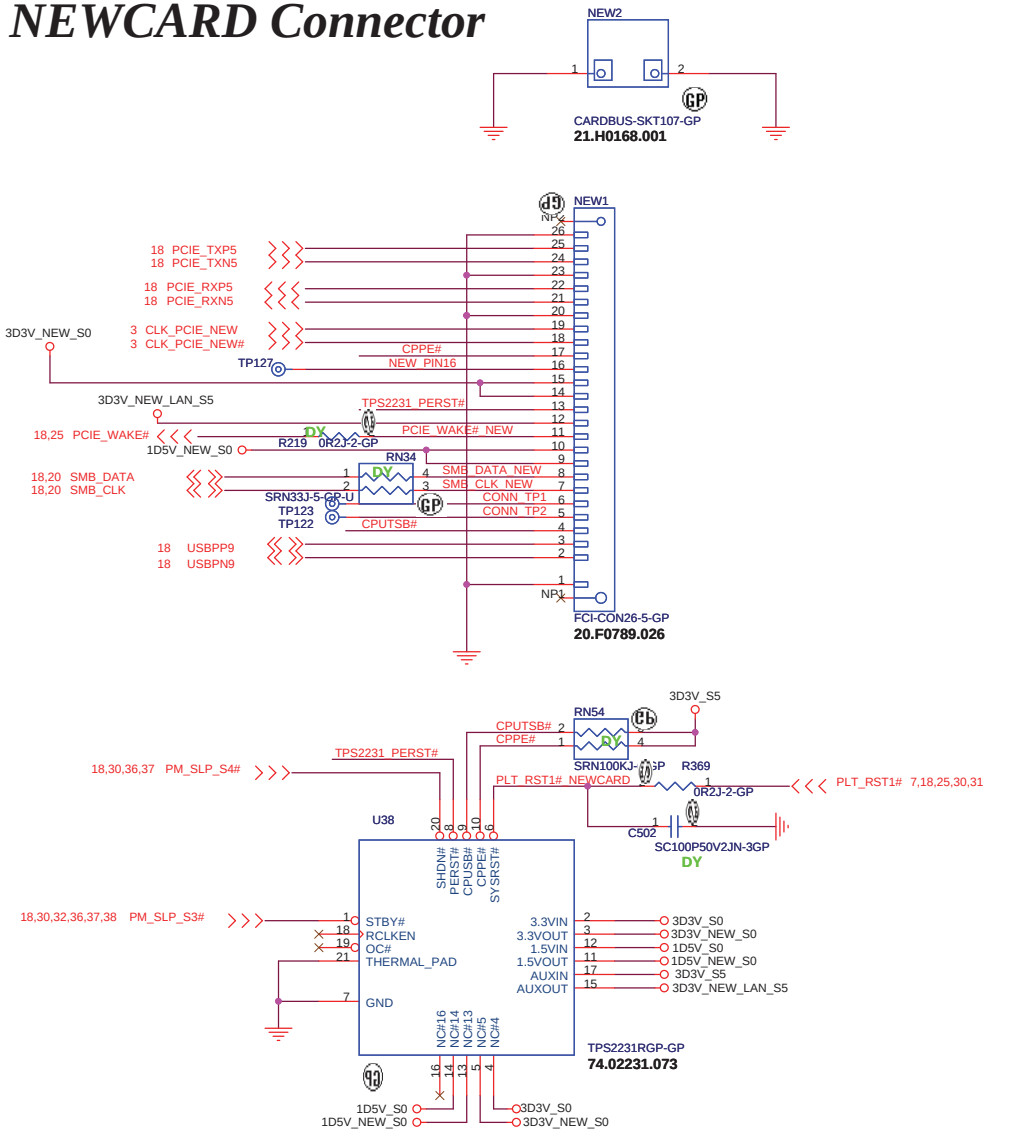
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

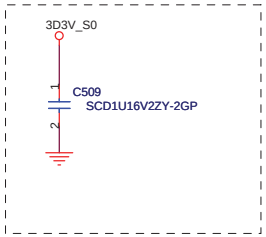
Size: A3 | Document Number: Cathedral Peak | Rev: SA

Date: Friday, January 11, 2008 | Sheet 26 of 41

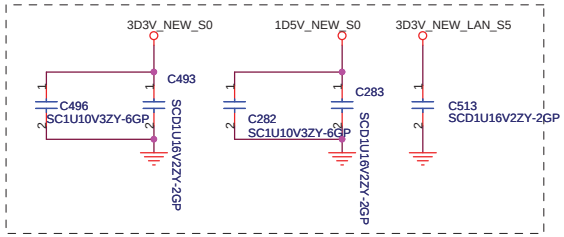
NEWCARD Connector



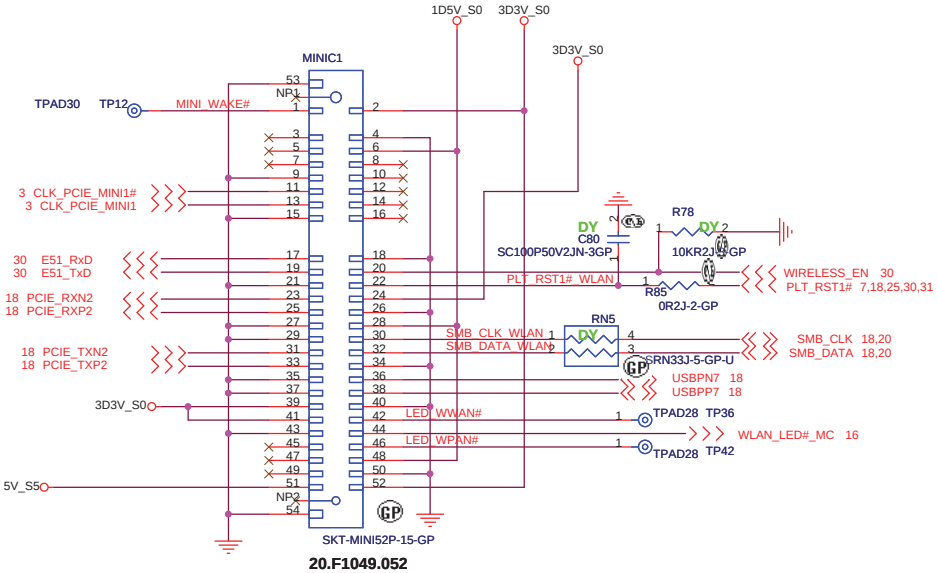
Place them Near to Chip



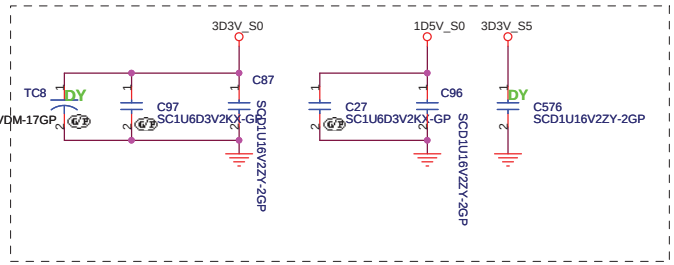
Place them Near to Connector



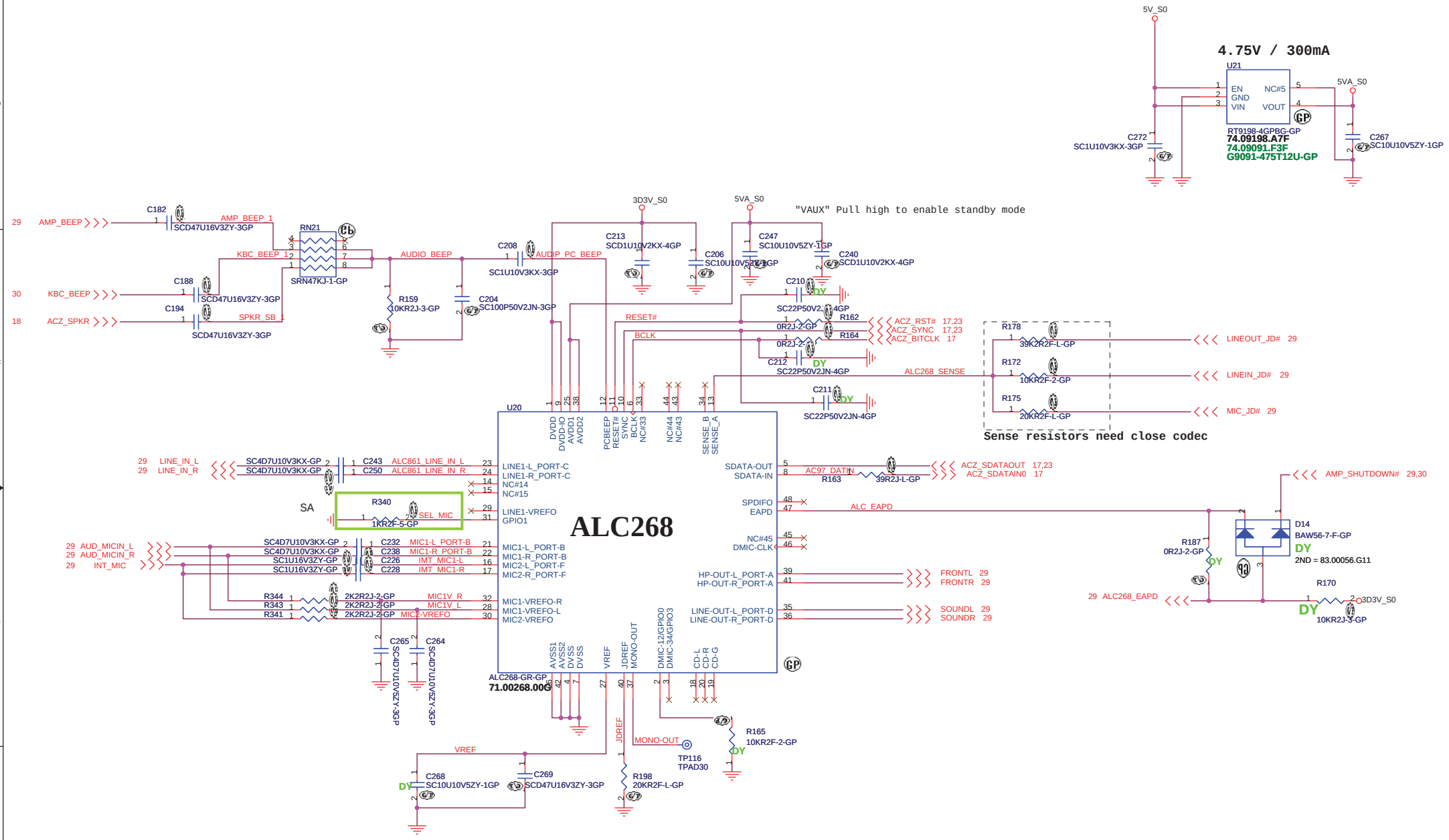
Mini Card Connector(WLAN)



Place near MINIC1

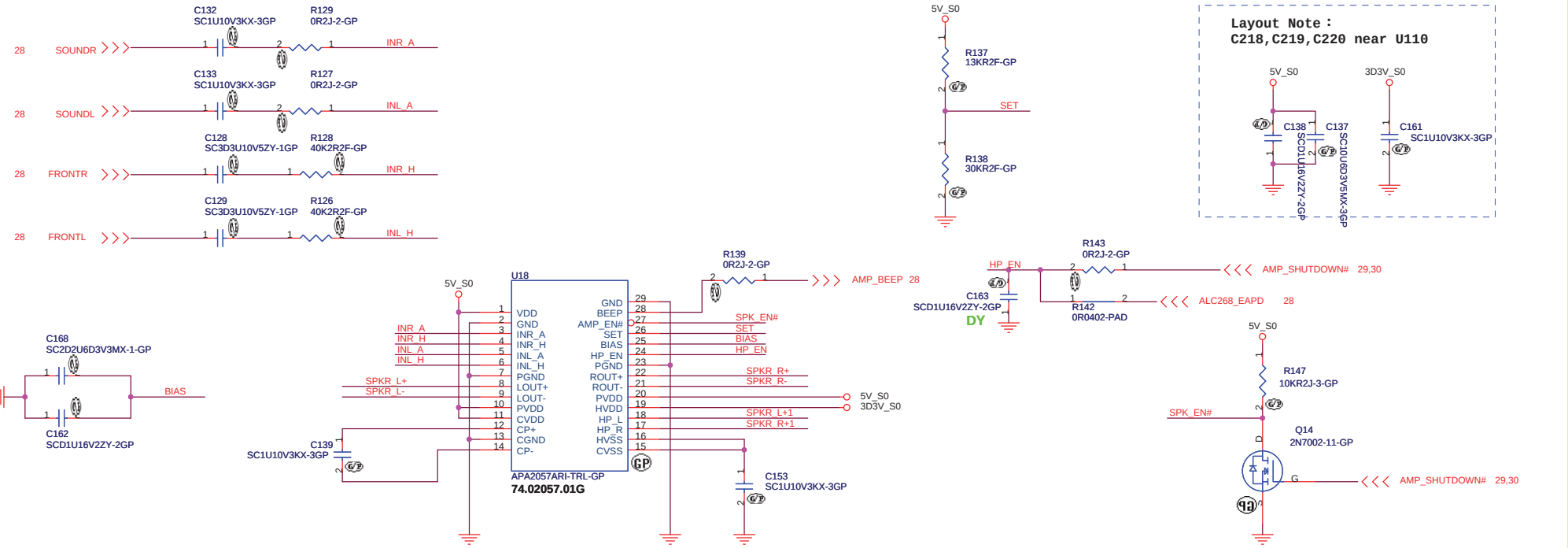


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: NEW CARD/MINI CARD		
Size	Document Number: Cathedral Peak	Rev: SA
Date: Friday, January 11, 2008	Sheet 27 of 41	

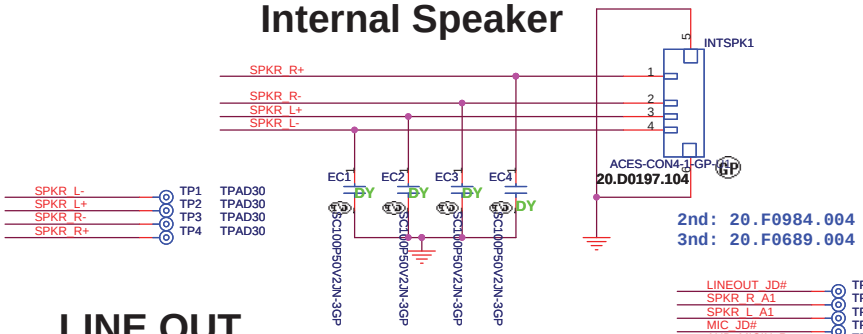

4.75V / 300mA
U21
RT9198-4GPBG-GP
74.09198.A7F
74.09091.F3F
G9091-475T12U-GP
5V_S0
5VA_S0
3D3V_S0
C272
SC1U10V3KX-3GP
C267
SC10U10V5ZY-1GP
"VAUX" Pull high to enable standby mode
AMP_BEEP
KBC_BEEP
ACZ_SPKR
C182
SCD47U16V3ZY-3GP
C188
C194
RN21
SRN47KJ-1-GP
AUDIO_BEEP
AUDIP_PC_BEEP
C208
SC1U10V3KX-3GP
R159
10KR2J-3-GP
C204
SC100P50V2JN-3GP
C213
SCD1U10V2KX-4GP
C206
SC10U10V5ZY-1GP
C247
SC10U10V5ZY-1GP
C240
SCD1U10V2KX-4GP
C210
SC22P50V2JN-4GP
R162
0R2J-2-GP
R164
C212
SC22P50V2JN-4GP
C211
SC22P50V2JN-4GP
RESET#
BCLK
ALC268_SENSE
ACZ_RST# 17,23
ACZ_SYNC 17,23
ACZ_BITCLK 17
R178
39KR2F-L-GP
R172
10KR2F-2-GP
R175
20KR2F-L-GP
LINEOUT_JD# 29
LINEIN_JD# 29
MIC_JD# 29
Sense resistors need close codec
U20
ALC268
ALC268-GR-GP
71.00268.006
LINE_IN_L
LINE_IN_R
C243 ALC861_LINE_IN_L
C250 ALC861_LINE_IN_R
SA
R340
SEL_MIC
1KR2F-5-GP
AUD_MICIN_L
AUD_MICIN_R
INT_MIC
C232 MIC1-L_PORT-B
C238 MIC1-R_PORT-B
C226 IMT_MIC1-L
C228 IMT_MIC1-R
R344
R343
R341
2K2R2J-2-GP
MIC1V_R
MIC1V_L
MIC2-VREFO
C265
C264
SC4D7U10V3KX-3GP
LINE1-L_PORT-C
LINE1-R_PORT-C
NC#14
NC#15
LINE1-VREFO
GPIO1
MIC1-L_PORT-B
MIC1-R_PORT-B
MIC2-L_PORT-F
MIC2-R_PORT-F
MIC1-VREFO-R
MIC1-VREFO-L
MIC2-VREFO
SDATA-OUT
SDATA-IN
AC97_DATIN
R163
39R2J-L-GP
ACZ_SDATAOUT 17,23
ACZ_SDATAIN0 17
SPDIFO
EAPD
ALC_EAPD
NC#45
DMIC-CLK
HP-OUT-L_PORT-A
HP-OUT-R_PORT-A
FRONTL 29
FRONTR 29
LINE-OUT-L_PORT-D
LINE-OUT-R_PORT-D
SOUNDL 29
SOUNDR 29
DVDD
DVDD-IO
AVDD1
AVDD2
PCBEEP
RESET#
SYNC
BCLK
NC#33
NC#44
NC#43
SENSE_B
SENSE_A
AVSS1
AVSS2
DVSS
DVSS
VREF
JDREF
MONO-OUT
DMIC-12/GPIO0
DMIC-34/GPIO3
CD-L
CD-R
CD-G
VREF
C268
SC10U10V5ZY-1GP
C269
SCD47U16V3ZY-3GP
JDREF
R198
20KR2F-L-GP
MONO-OUT
TP116
TPAD30
R165
10KR2F-2-GP
AMP_SHUTDOWN# 29,30
D14
BAW56-7-F-GP
2ND = 83.00056.G11
R187
0R2J-2-GP
R170
10KR2J-3-GP
29 ALC268_EAPD
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Azalia codec ALC268
Size
A3
Document Number
Cathedral Peak
Rev
SA
Date: Friday, January 11, 2008
Sheet 28 of 41

AUDIO OP AMPLIFIER

SA

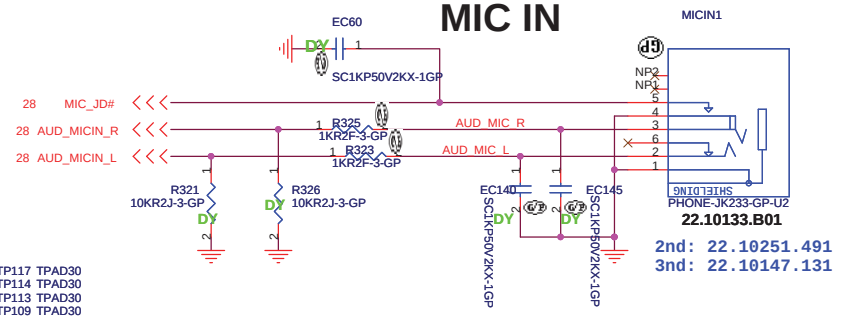


Internal Speaker



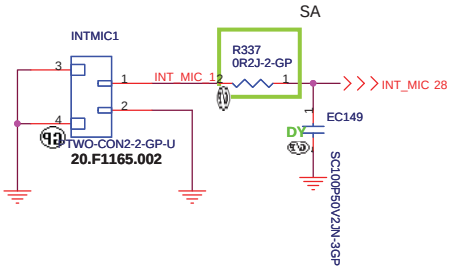
2nd: 20.F0984.004
3nd: 20.F0689.004

MIC IN

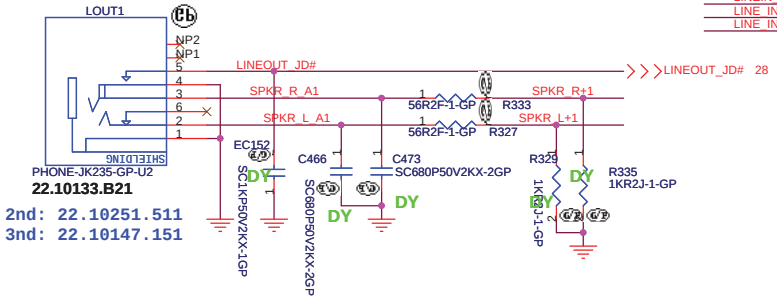


2nd: 22.10251.491
3nd: 22.10147.131

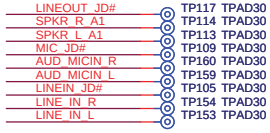
Analog Int. Mic



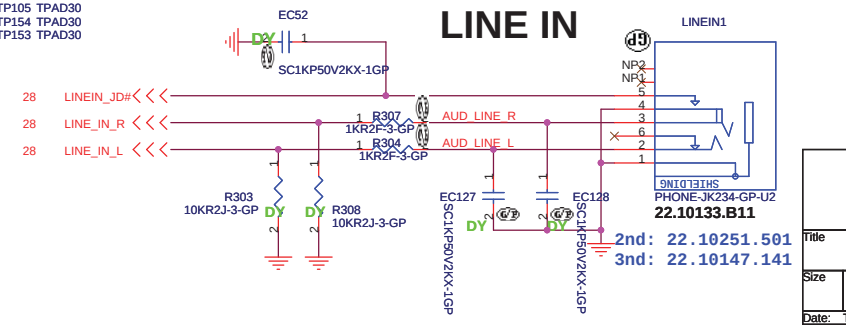
LINE OUT



2nd: 22.10251.511
3nd: 22.10147.151



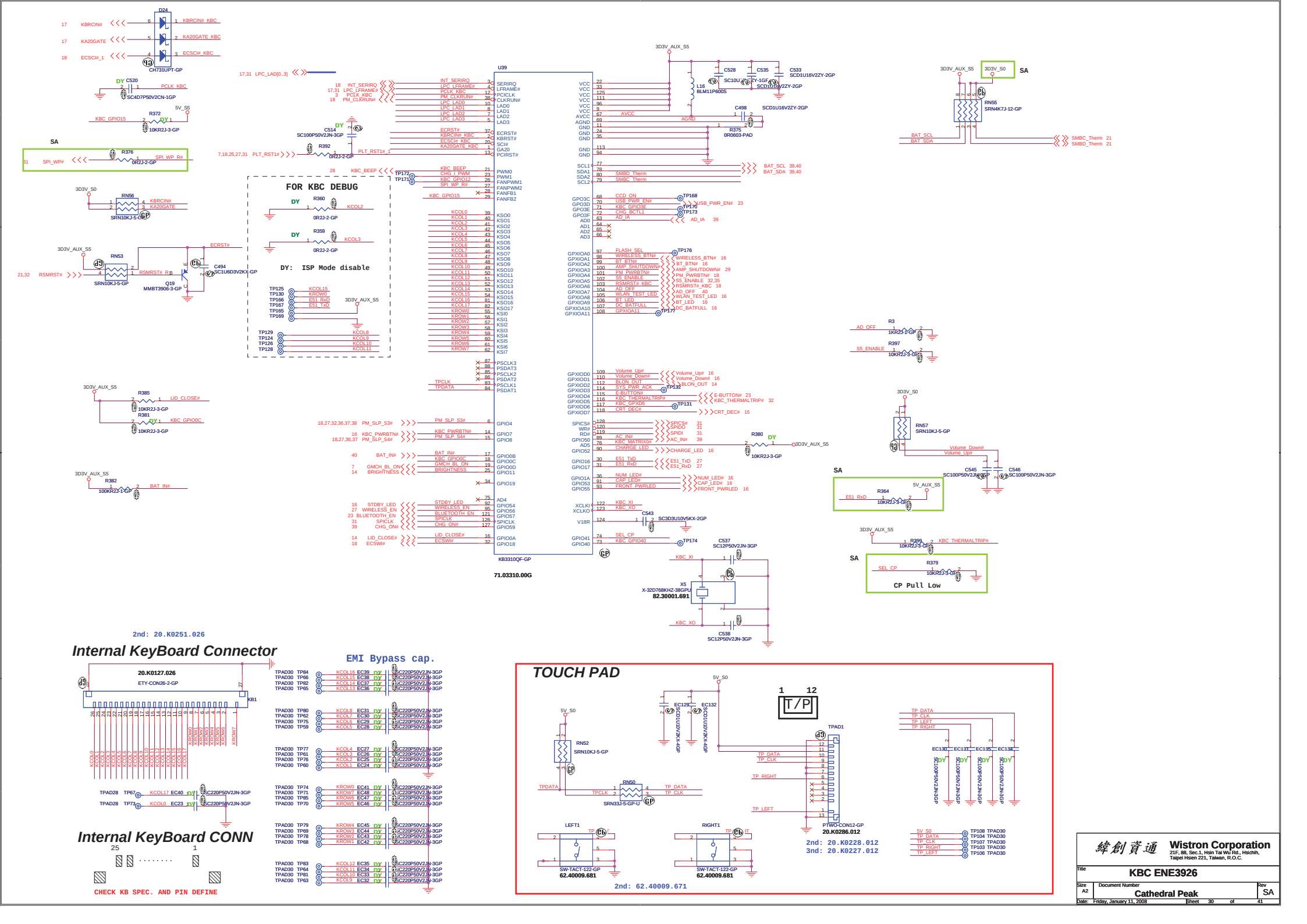
LINE IN

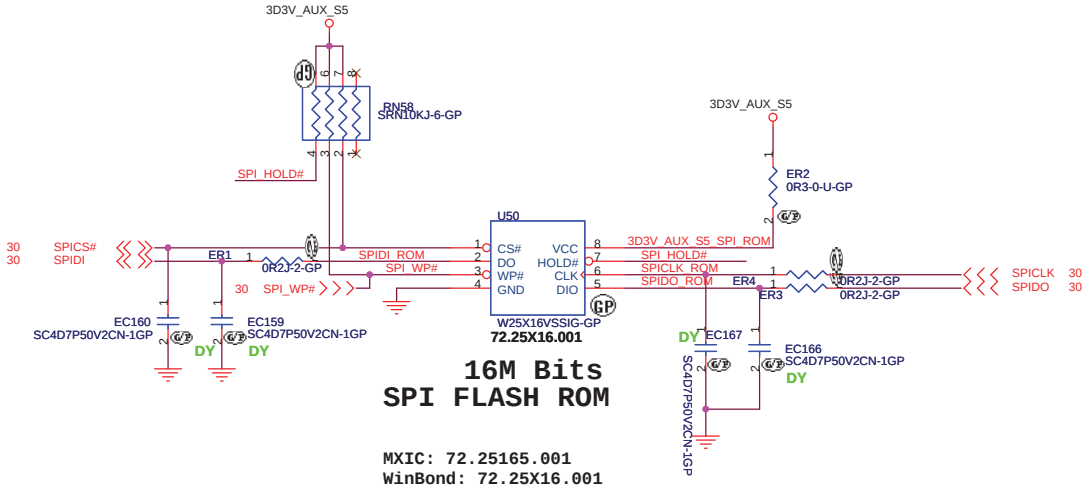


2nd: 22.10251.501
3nd: 22.10147.141

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO AMP AND JACK	
Size	Document Number: Cathedral Peak	Rev: SA
Date: Tuesday, January 15, 2008	Sheet 29 of 41	


FOR KBC DEBUG
DY: ISP Mode disable
SA
CP Pull Low
U39
KB3310QF-GP
71.03310.00G
Internal KeyBoard Connector
20.K0127.026
ETY-CON26-2-GP
2nd: 20.K0251.026
EMI Bypass cap.
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
T/P
PTWO-CON12-GP
20.K0286.012
2nd: 20.K0228.012
3nd: 20.K0227.012
SW-TACT-122-GP
62.40009.681
2nd: 62.40009.671
X5
X-32D768KHZ-38GPU
82.30001.691
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ENE3926
Cathedral Peak
SA
Friday, January 11, 2008
30
41



16M Bits
SPI FLASH ROM

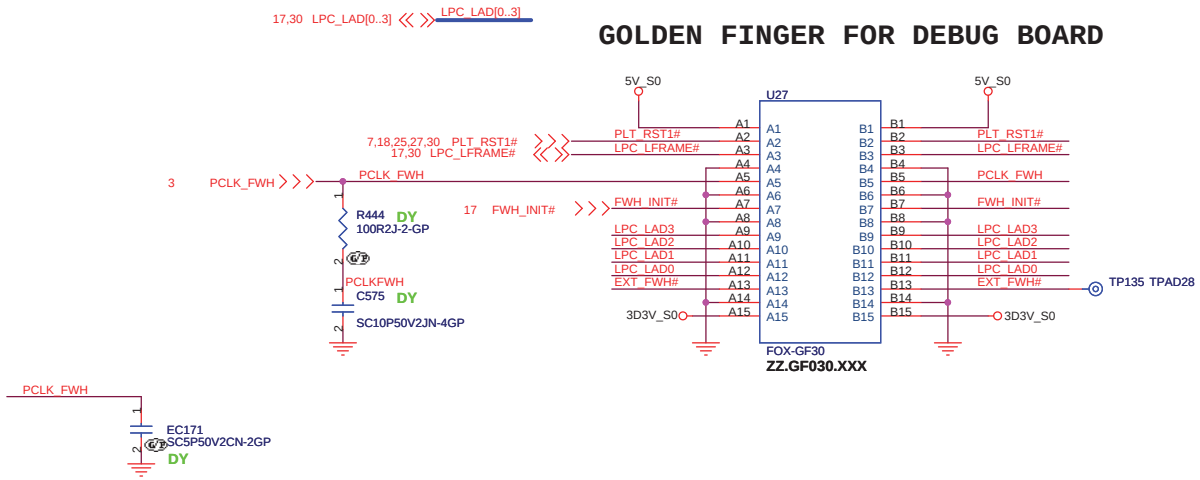
MXIC: 72.25165.001
WinBond: 72.25X16.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**BIOS/GOLDEN FINGER**	
Size	Document Number: **Cathedral Peak**	Rev: SA
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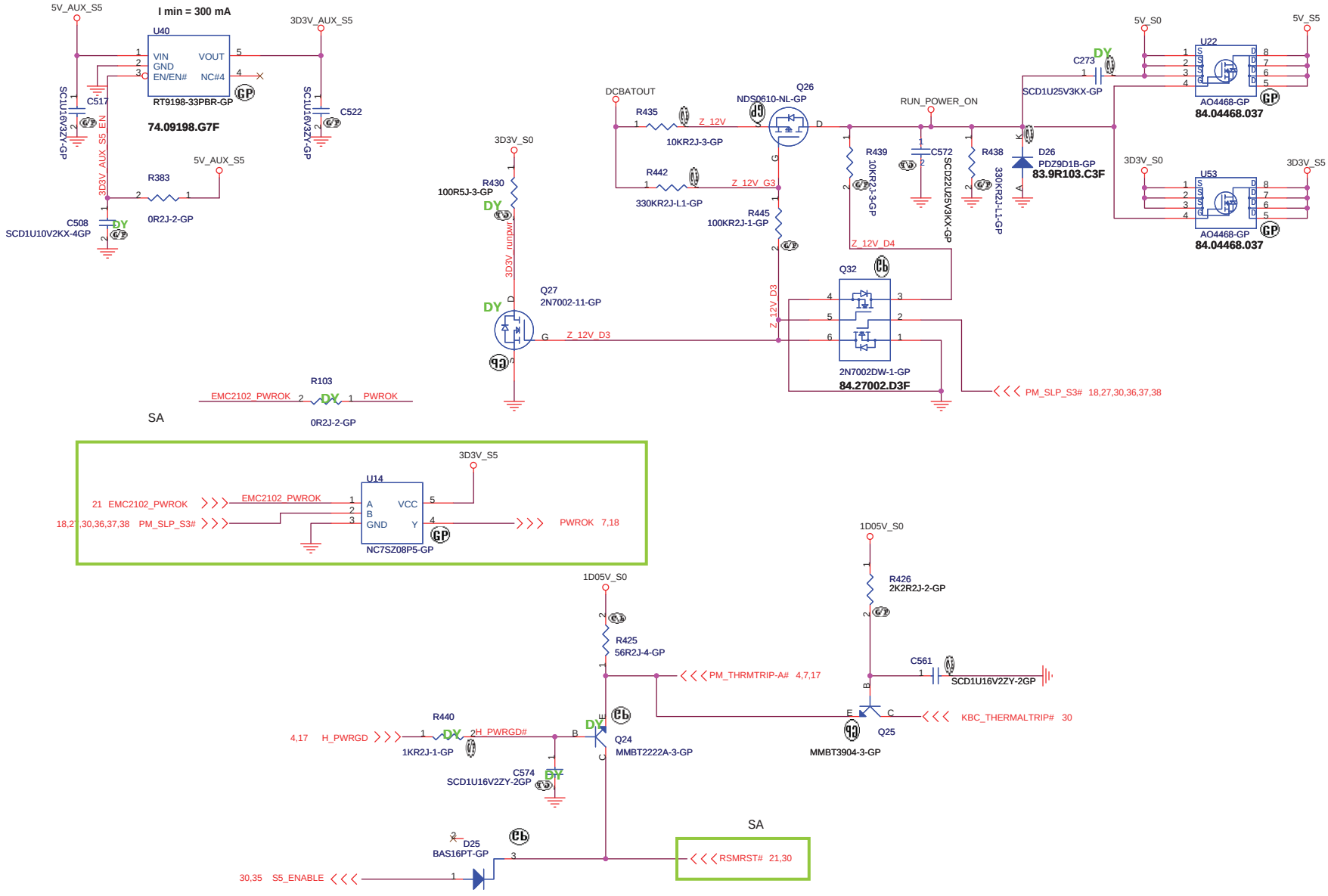
Aux Power

3D3V_AUX_S5

Run Power



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RUN POWER and 3D3V_AUX_S5	
Size	Document Number: Cathedral Peak	Rev: SA
Date: Monday, January 14, 2008	Sheet 32 of 41	

CPU_CORE
ISL6266A

VID0
VID1
VID2
VID3
VID4
VID5
VID6

CPUCORE_ON

VCC_SENSE
VSS_SENSE

DCBATOUT_6266A
5V_S0
3D3V_S0

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)

Input Signal
EN (I / 3.3V)

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Input Power
VCC(I)
VCC(I)
VCC(I)

Output Signal
PGOOD

Output Power
VCC_CORE_PWR(O)

VGATE_PWRGD
VCC_CORE(Imax=38A)

TPS51125
5V/3D3V

DCBATOUT_51125
PM_SLP_S4#
ALW_PWRGD_3V_5V

Input Power
VIN

Input Signal
EN0

Output Signal
PGOOD

Output Power
5V(O)
3D3V(O)

5V_S5 (6A)
3D3V_S5 (6A)

RT9018A
1D5V_S0

1D8V_S3
PM_SLP_S3#

VIN
EN

1D5V(O)
PGOOD

1D5V_S0 (2.5A)
CPUCORE_ON

RT9026
0D9V_S0

5V_S5
1D8V_S3
PM_SLP_S4#

VIN
VLDOIN
S3
S5

VTT
VTTREF

0D9V_S3 (1A)
0D9V_S3_1

G9131
2D5V_S0

3D3V_S0

INPUT

OUT

2D5V_S0(0.3A)

GFX_CORE
ISL6263A

VID0
VID1
VID2
VID3
VID4

5V_S0
DCBATOUT

PM_SLP_S3#
GFXVR_EN

VCC_AXG_SENSE
VSS_AXG_SENSE

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Input Power
VDD
VIN

Input Signal
VR_ON

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

Output Signal
PGOOD

Output Power
VGFXCORE (O)

CPUCORE_ON
VCC_GFXCORE(5.5A)

TPS51124
1D8V/1D05V

5V_S5
DCBATOUT_51124

PM_SLP_S4#
PM_SLP_S3#

CPUCORE_ON

Input Power
VDD
VCC

Input Signal
EN1
EN2

Output Signal
PGOOD1
PGOOD2

Output Power
1D8V (O)
1D05V(O)

1D8V_S3 (10A)
1D05V_S0 (15A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN#
AD+

Charger BQ24750

CHG_ON#
24750_CELLS

AD+

Input Signal
CHGEN#
CELLS

Input Power
ACN

Output Signal
ACGOOD#
SRSET

Output Power
VOUT (O)
VOUT (O)

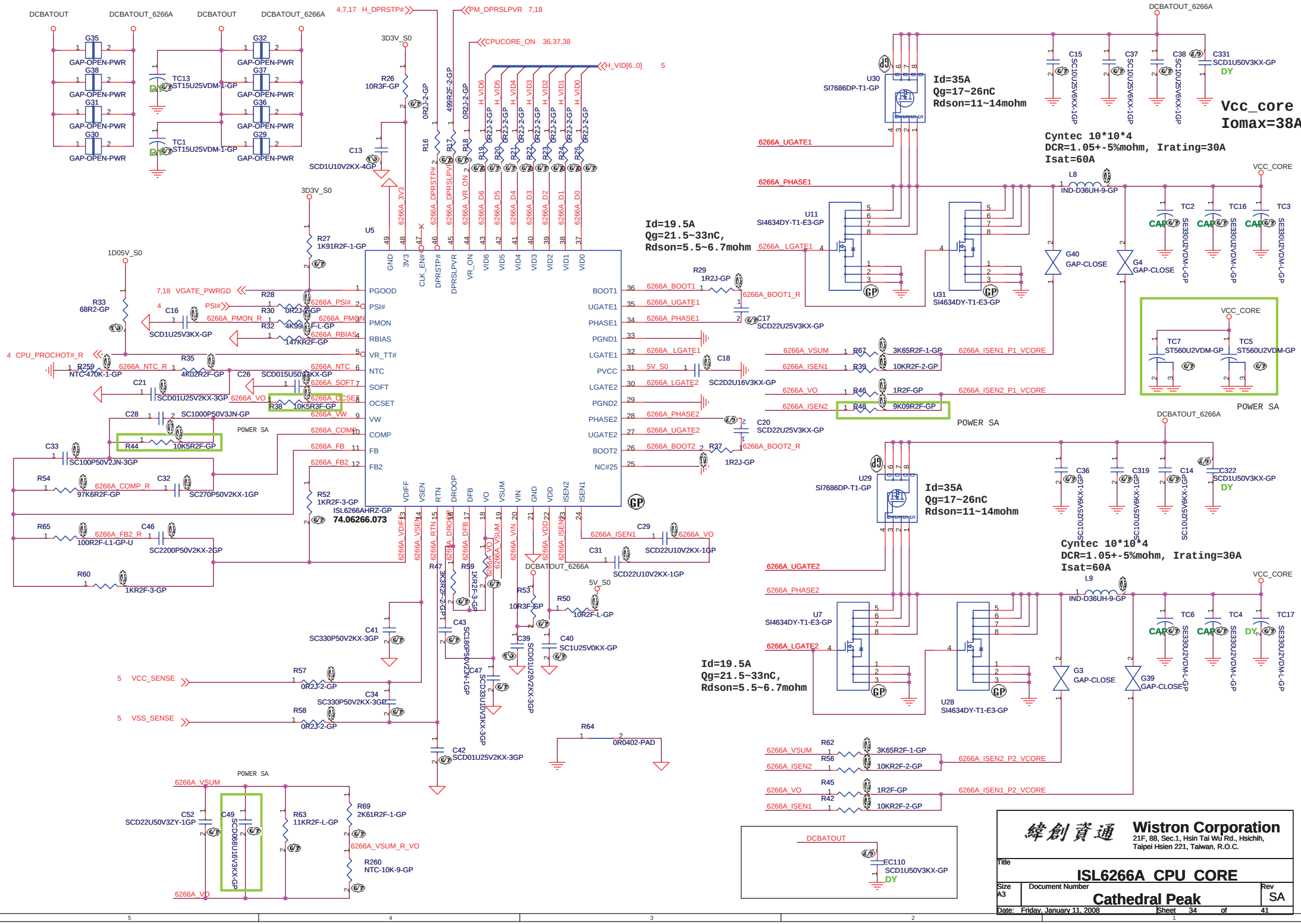
AC_IN#
AD_IA
BT+
DCBATOUT

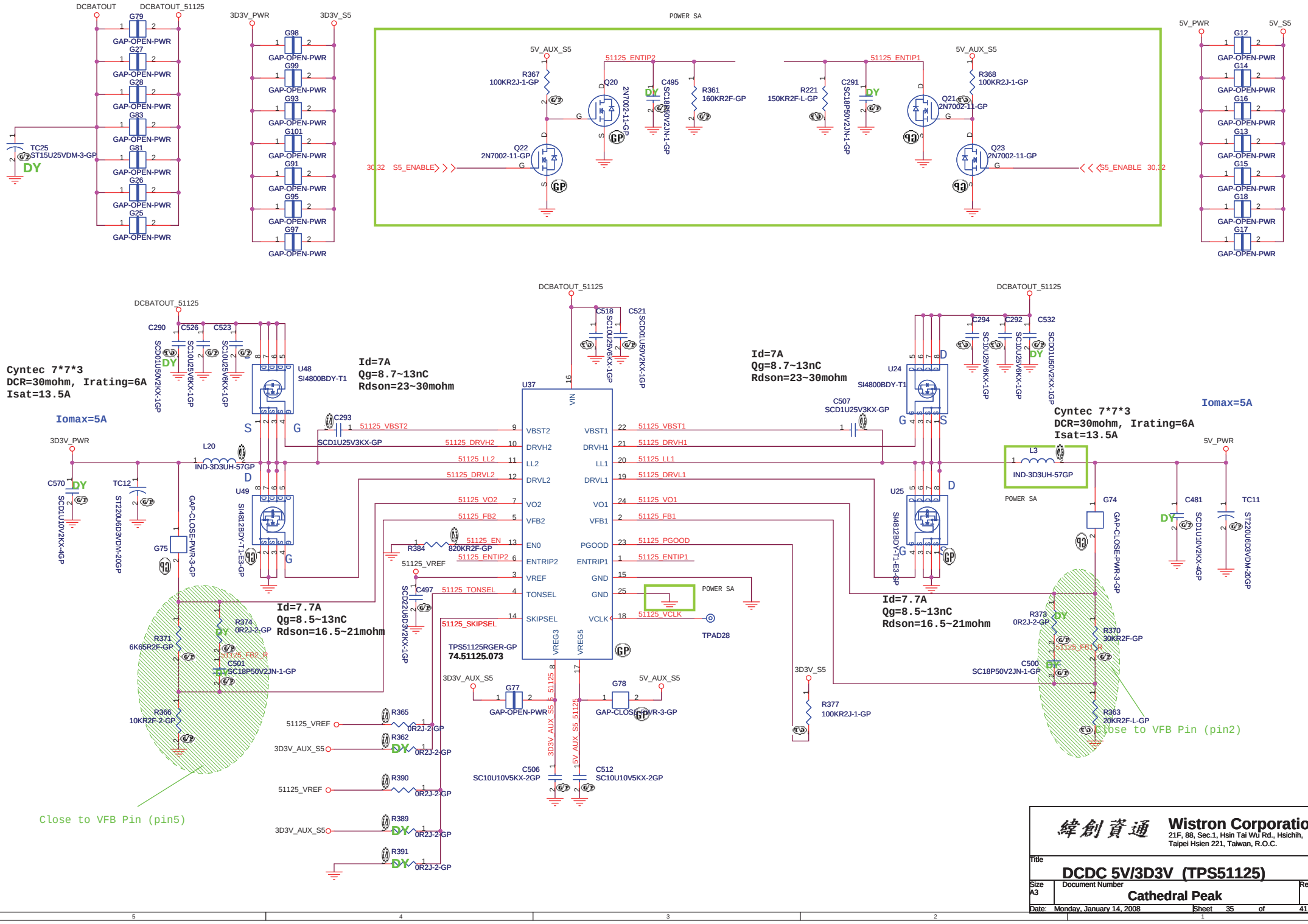
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Sequence Logic

Size: B | Document Number: Cathedral Peak | Rev: SA

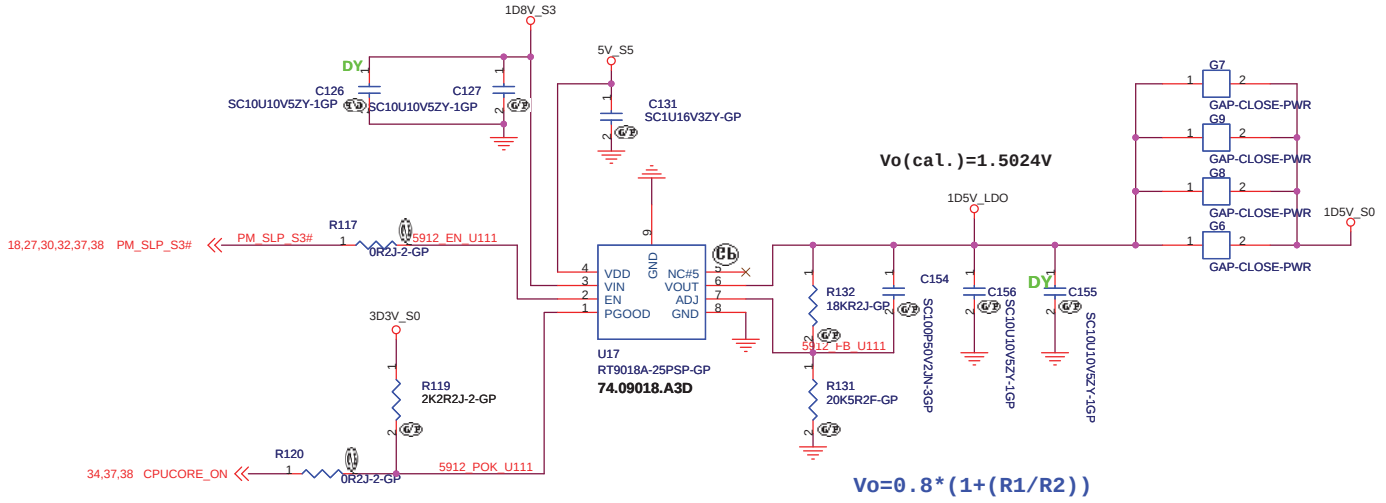
Date: Wednesday, November 14, 2007 | Sheet 33 of 41

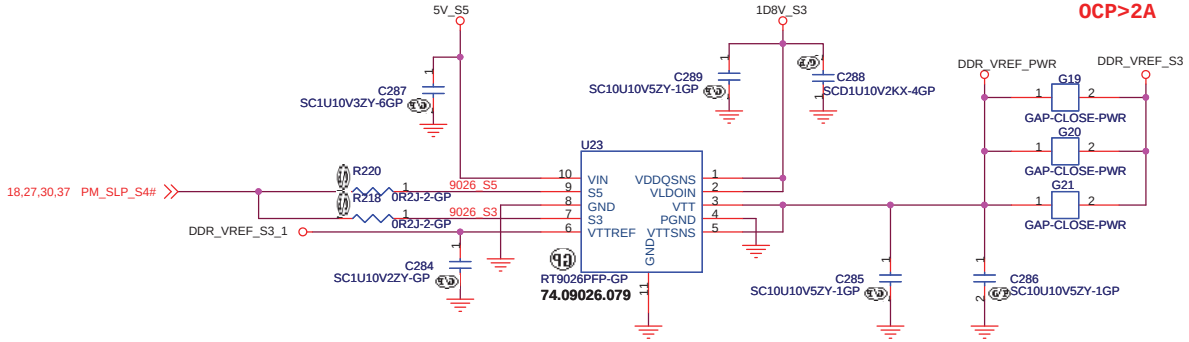

U5
ISL6266AHRZ-GP
74.06266.073
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
U30
SI7686DP-T1-GP
U11
SI4634DY-T1-E3-GP
U31
SI4634DY-T1-E3-GP
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
POWER SA
U29
SI7686DP-T1-GP
U7
SI4634DY-T1-E3-GP
U28
SI4634DY-T1-E3-GP
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
Id=35A
Qg=17~26nC
Rdson=11~14mohm
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6266A CPU CORE
Size A3
Document Number
Cathedral Peak
Rev SA
Date: Friday, January 11, 2008
Sheet 34 of 41



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DCDC 5V/3D3V (TPS51125)**
Size A3	Document Number **Cathedral Peak** Rev SA
Date: Monday, January 14, 2008	Sheet 35 of 41

1D5V_S0
Iomax=2.5A

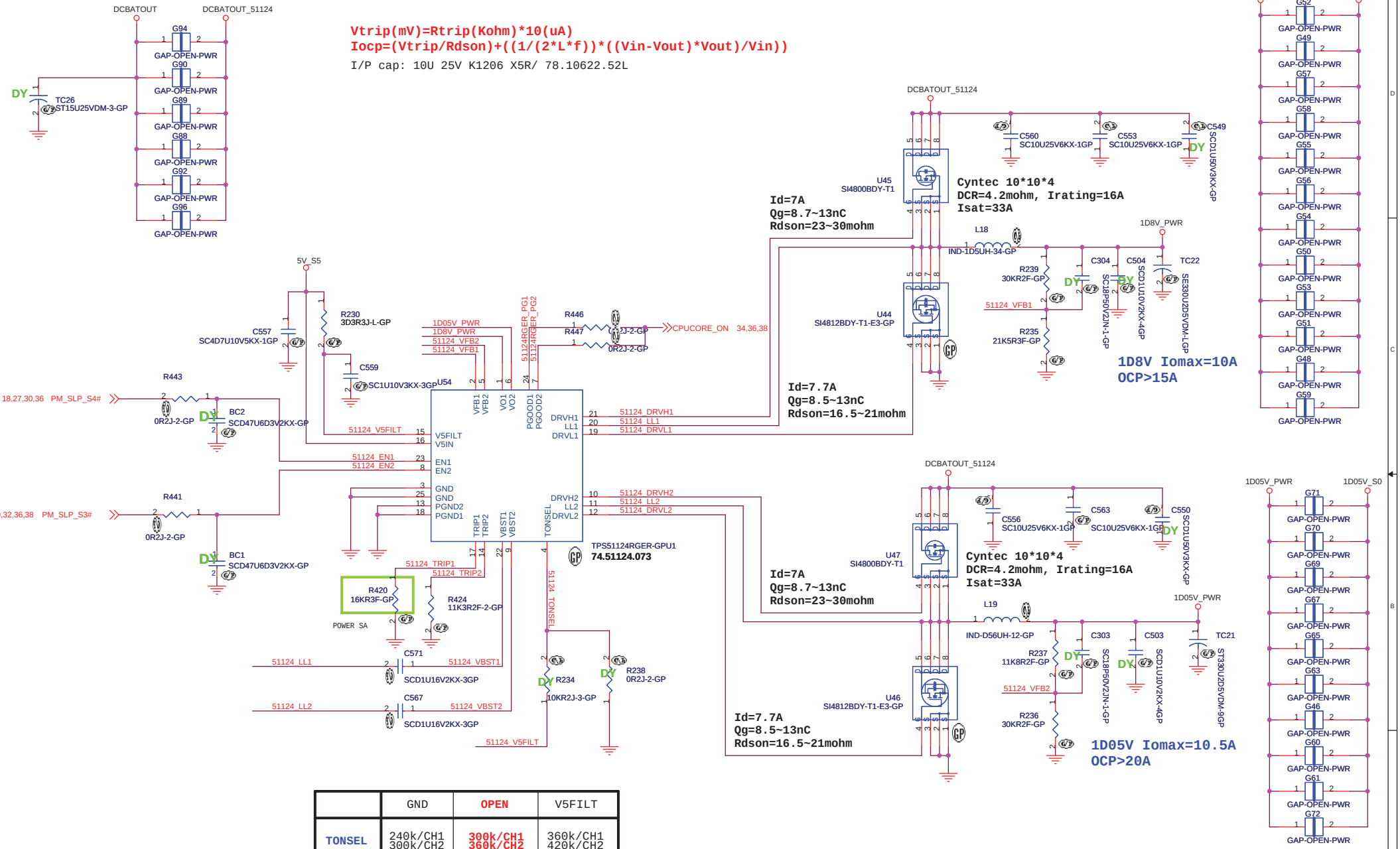




緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V & 0D9V		
Size: A3	Document Number: Cathedral Peak	Rev: SA
Date: Friday, January 11, 2008	Sheet 36 of 41	

Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

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Title: TPS51124 1D8V 1D05V

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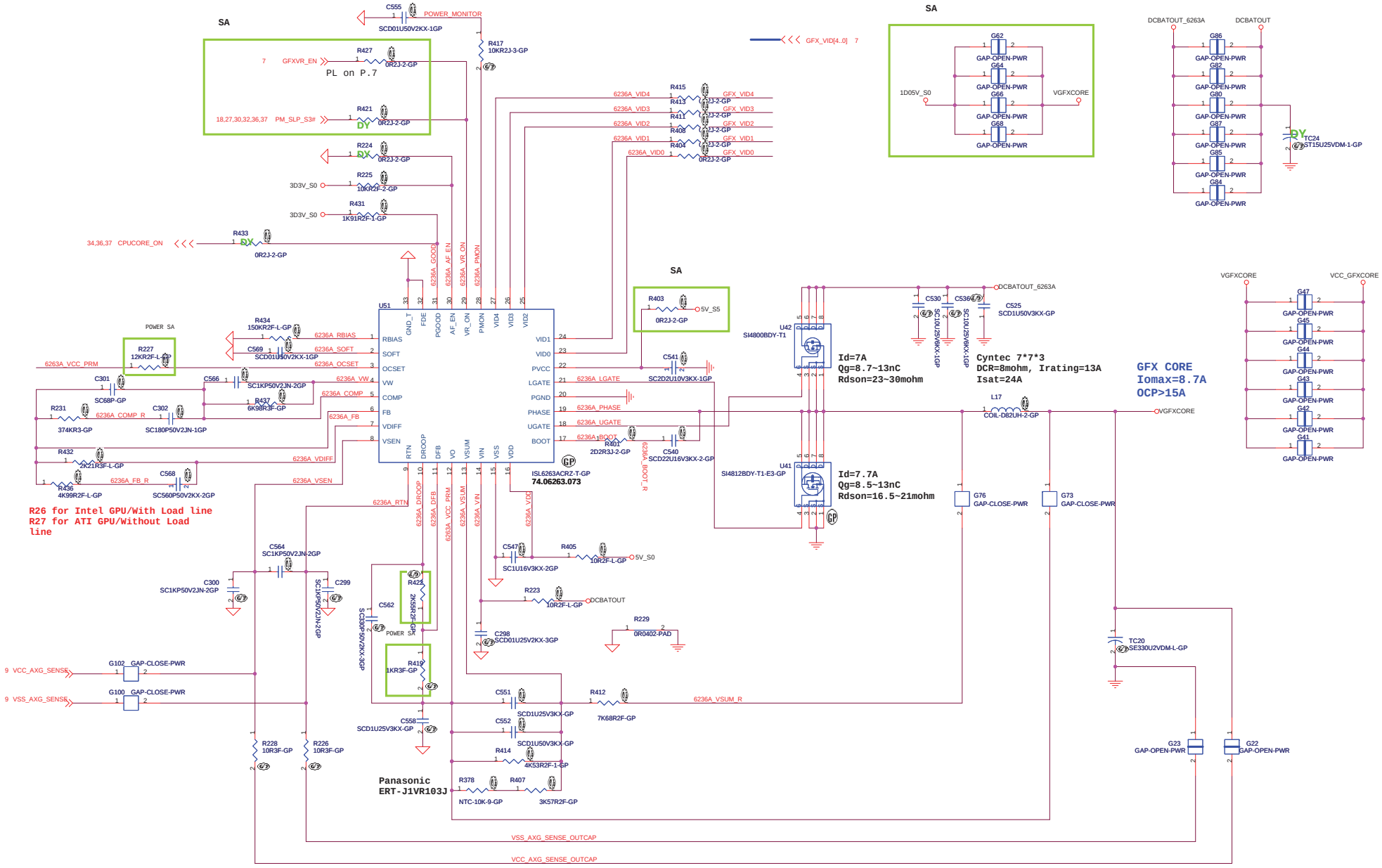
SA
PL on P.7
POWER_MONITOR
SCD01U50V2KX-1GP
GFXVR_EN
PM_SLP_S3#
GFX_VID[4..0]
1D05V_S0
VGFXCORE
GAP-OPEN-PWR
DCBATOUT_6263A
DCBATOUT
TC24
ST15U25VDM-1-GP
3D3V_S0
CPUCORE_ON
5V_S5
U51
ISL6263ACRZ-T-GP
74.06263.073
SI4800BDY-T1
SI4812BDY-T1-E3-GP
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Cyntec 7*7*3
DCR=8mohm, Irating=13A
Isat=24A
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
GFX CORE
Iomax=8.7A
OCP>15A
L17
COIL-D82UH-2-GP
R26 for Intel GPU/With Load line
R27 for ATI GPU/Without Load line
Panasonic
ERT-J1VR103J
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
Eiger
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ISL6263A_GFX CORE
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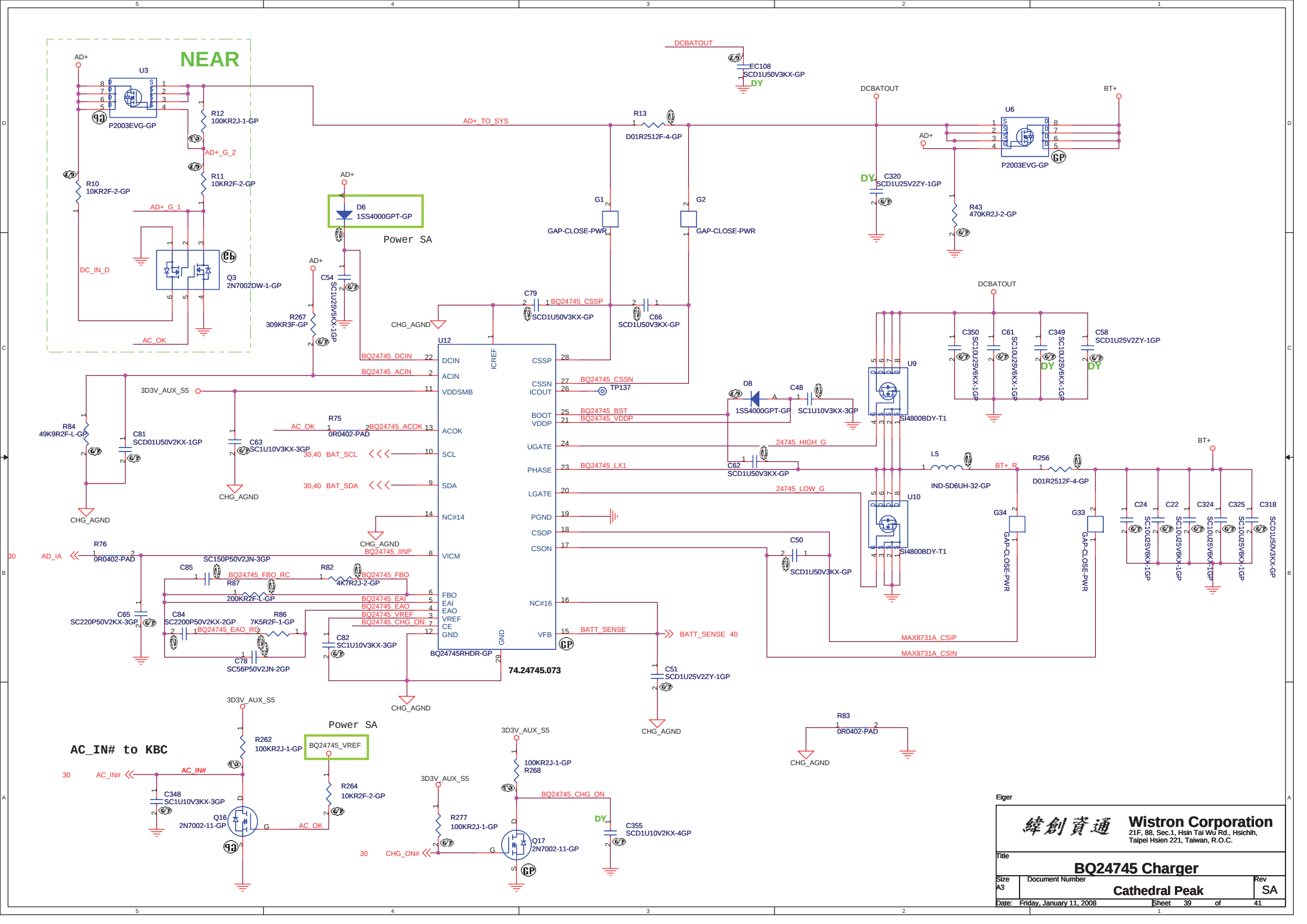
NEAR
U3
P2003EVG-GP
R12
100KR2J-1-GP
R10
10KR2F-2-GP
R11
10KR2F-2-GP
Q3
2N7002DW-1-GP
AD+_G_1
AD+_G_2
DC_IN_D
AC_OK
AD+
D6
1SS4000GPT-GP
Power SA
C54
SC1U25V6KX-1GP
R267
309KR3F-GP
CHG_AGND
AD+_TO_SYS
R13
D01R2512F-4-GP
DCBATOUT
EC108
SCD1U50V3KX-GP
DY
U6
P2003EVG-GP
BT+
C320
SCD1U25V2ZY-1GP
R43
470KR2J-2-GP
G1
G2
GAP-CLOSE-PWR
C79
SCD1U50V3KX-GP
C66
SCD1U50V3KX-GP
BQ24745_CSSP
U12
BQ24745RHDR-GP
74.24745.073
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ICREF
BQ24745_DCIN
BQ24745_ACIN
BQ24745_CSSN
TP137
BQ24745_BST
BQ24745_VDDP
24745_HIGH_G
BQ24745_LX1
24745_LOW_G
BQ24745_ACOK
BQ24745_IINP
BQ24745_FBO_RC
BQ24745_FBO
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_EAO_RC
BATT_SENSE
BATT_SENSE_40
MAX8731A_CSIP
MAX8731A_CSIN
3D3V_AUX_S5
R84
49K9R2F-L-GP
C81
SCD01U50V2KX-1GP
C63
SC1U10V3KX-3GP
R75
0R0402-PAD
AC_OK
30,40 BAT_SCL
30,40 BAT_SDA
R76
0R0402-PAD
AD_IA
SC150P50V2JN-3GP
C85
R87
200KR2F-L-GP
R82
4K7R2J-2-GP
C65
SC220P50V2KX-3GP
C84
SC2200P50V2KX-2GP
R86
7K5R2F-1-GP
C82
SC1U10V3KX-3GP
C78
SC56P50V2JN-2GP
C50
SCD1U50V3KX-GP
C51
SCD1U25V2ZY-1GP
R83
0R0402-PAD
D8
1SS4000GPT-GP
C48
SC1U10V3KX-3GP
C62
SCD1U50V3KX-GP
U9
U10
SI4800BDY-T1
L5
IND-5D6UH-32-GP
BT+_R
R256
D01R2512F-4-GP
G34
G33
GAP-CLOSE-PWR
C350
C61
C349
C58
SCD1U25V2ZY-1GP
SC10U25V6KX-1GP
C24
C22
C324
C325
C318
SCD1U50V3KX-GP
AC_IN# to KBC
R262
100KR2J-1-GP
BQ24745_VREF
R264
10KR2F-2-GP
C348
SC1U10V3KX-3GP
Q16
2N7002-11-GP
AC_IN#
R277
100KR2J-1-GP
R268
100KR2J-1-GP
Q17
2N7002-11-GP
CHG_ON#
C355
SCD1U10V2KX-4GP
Eiger
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BQ24745 Charger
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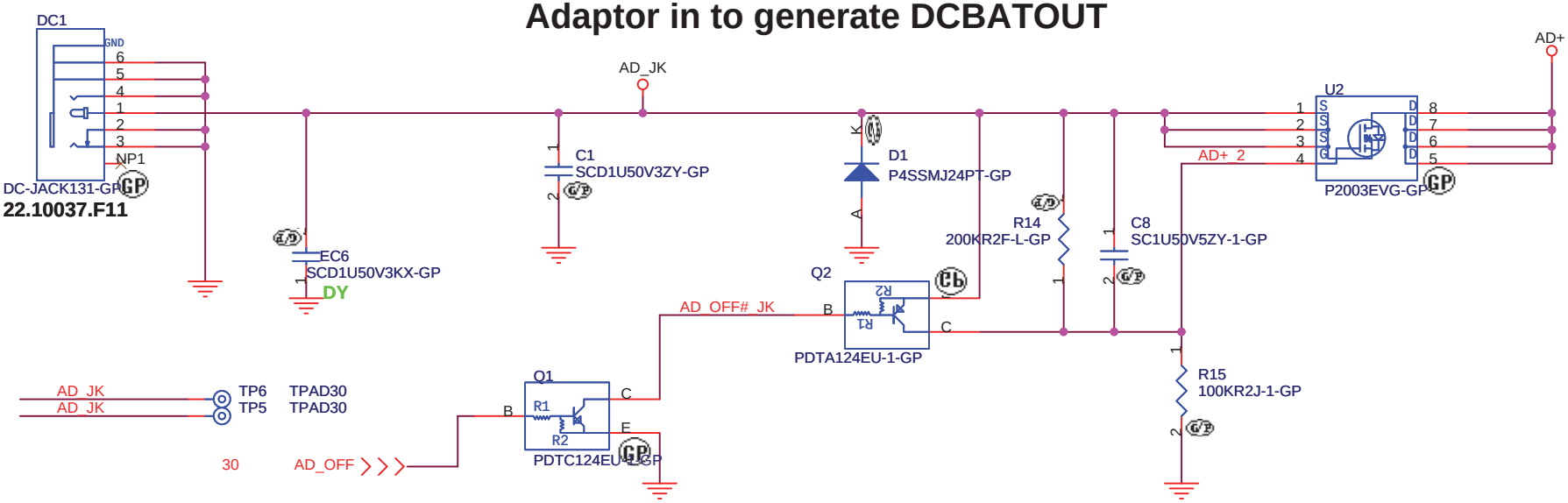
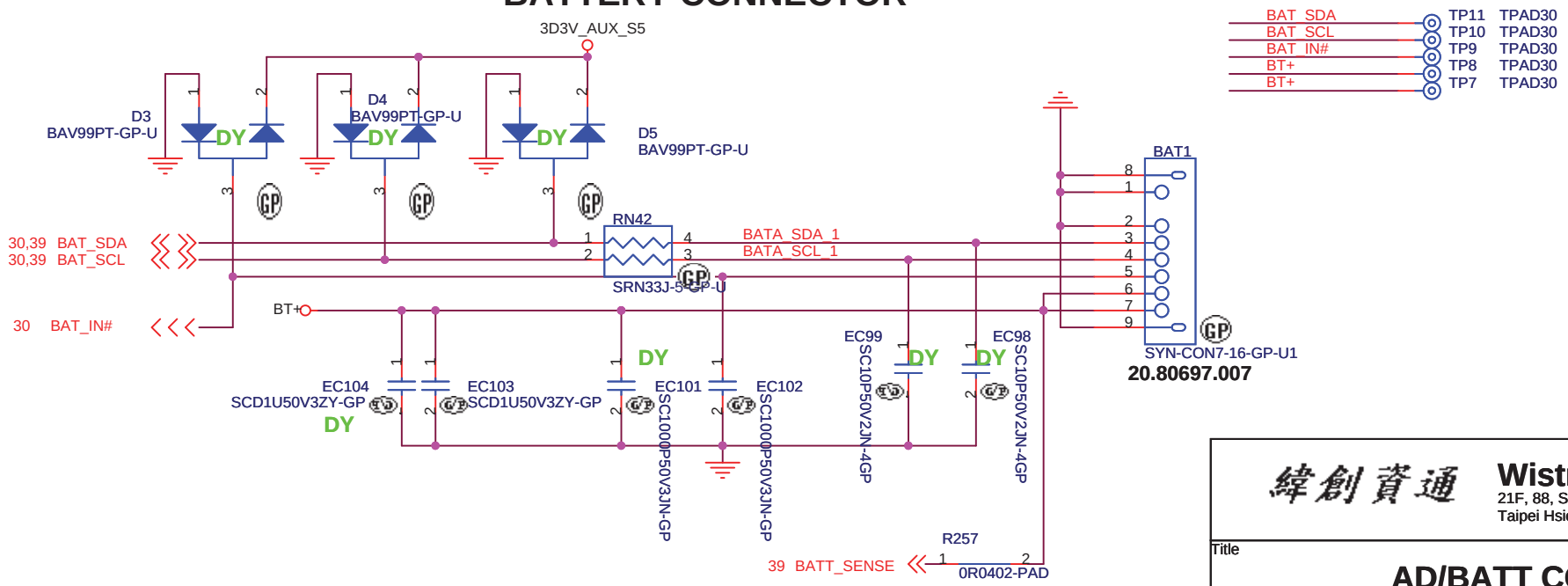
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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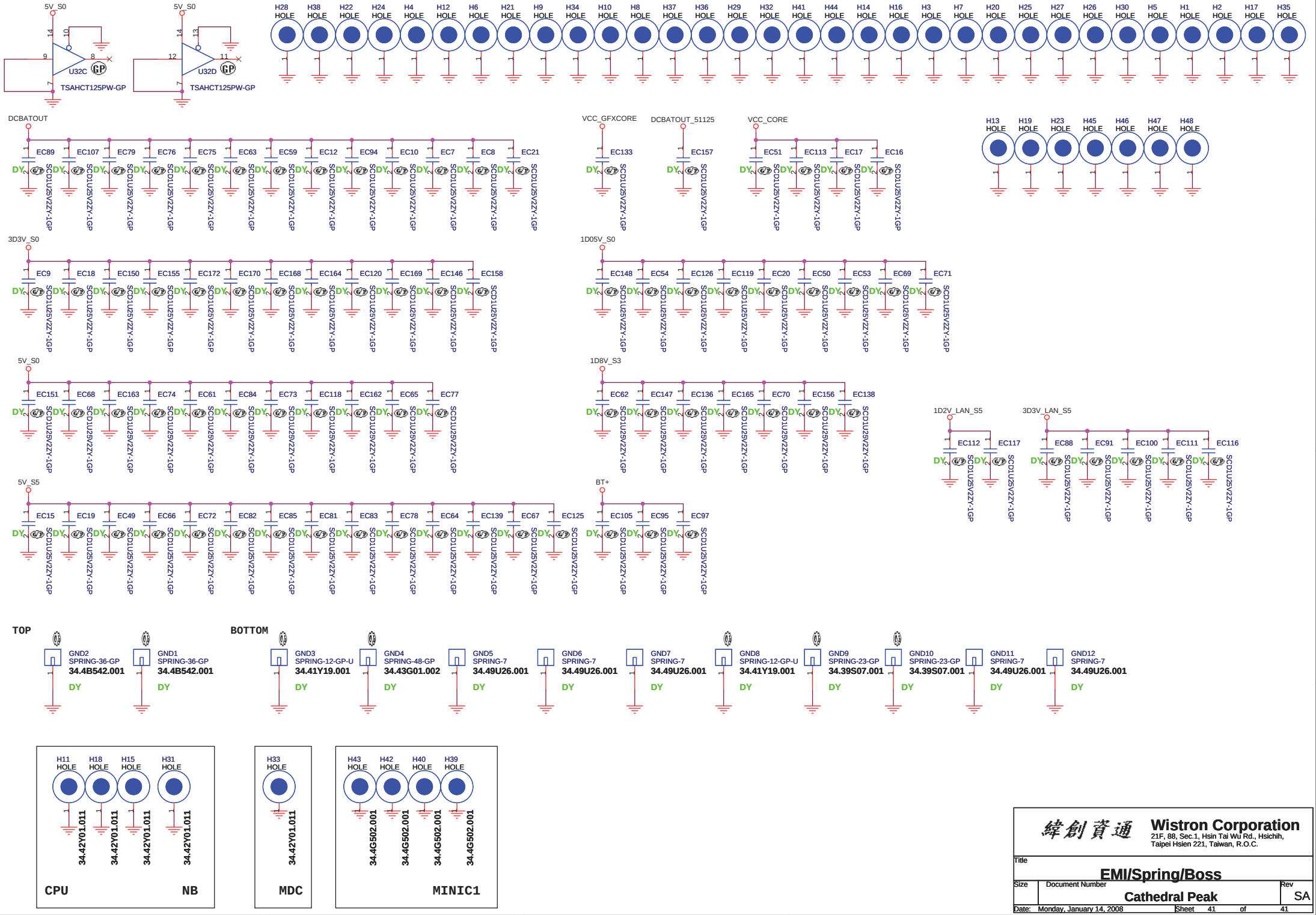

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Title: **EMI/Spring/Boss**

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