Compal Confidential

JDW50/JDY70 Schematics Document

Intel Merom Processor with Crestline(PM945/GM945) + DDRII + ICH7M
(With ATI MXM/B)

2007-4-12

REV: 0.3

Security Classification	Compal Secret Data		
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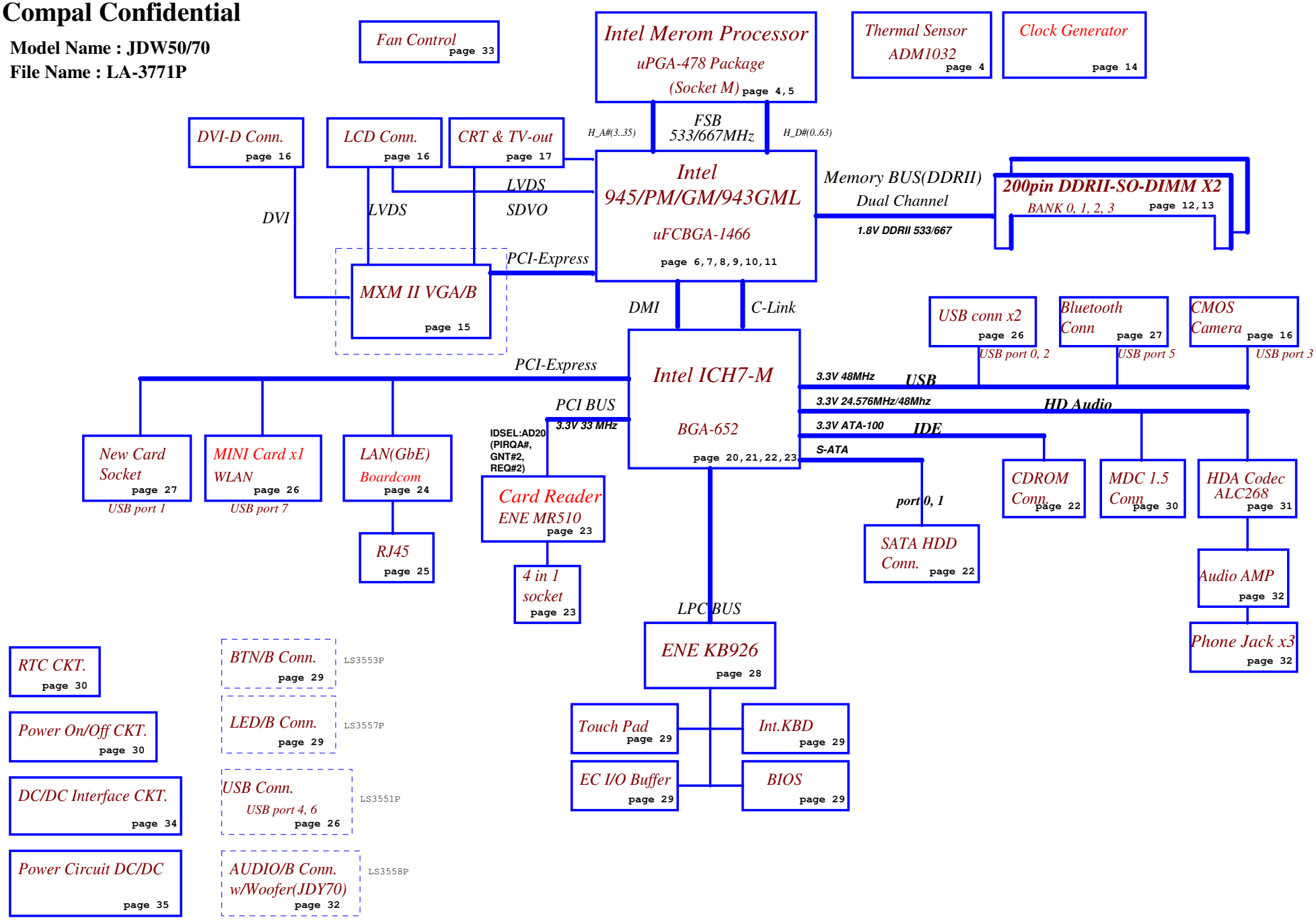
Model Name : JDW50/70
File Name : LA-3771P



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Title: Block Diagrams

Size	Document Number	Rev
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.9VS	0.9V switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8V	1.8V power rail for DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail for SB	ON	ON	X
+3V_LAN	3.3V power rail for LAN	ON	ON	X
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Card Reader	AD16	0	PIRQE

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
GMT G781-1	1001 101X b

EC SM Bus2 address

Device	Address
ADI ADM1032	1001 100X b

ICH7M SM Bus address

Device	Address
Clock Generator (ICS9LPRS365)	1101 001Xb
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	PM@
UMA	GM@
DVI	DVI@
SATA*1	SATA*1@
SATA*2	SATA*2@
Dbg	Dbg@

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Title: Notes List

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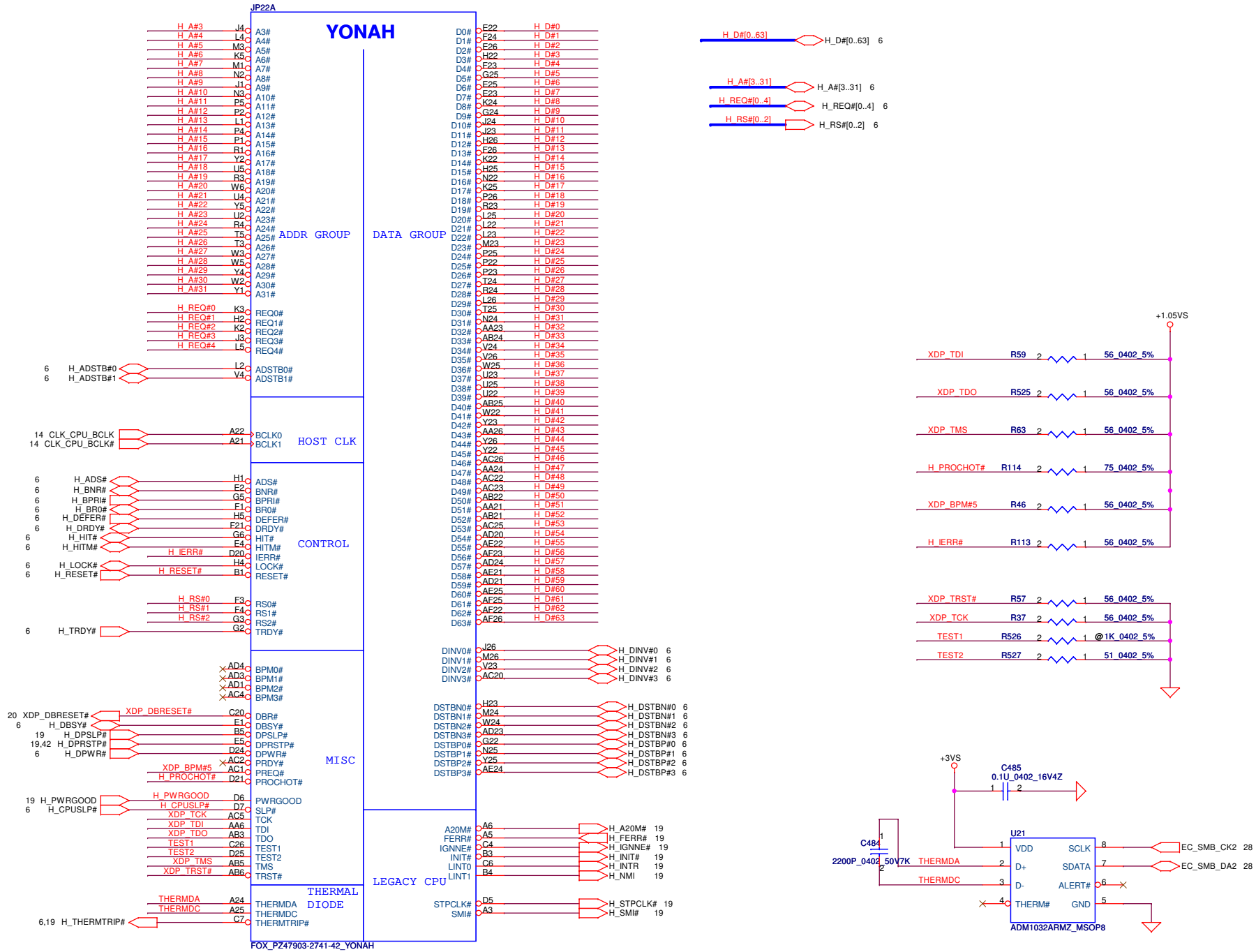

Layout Note:
THERMDA & THERMDC Trace / Space = 10 / 10 mil

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Title: Merom (1/2)

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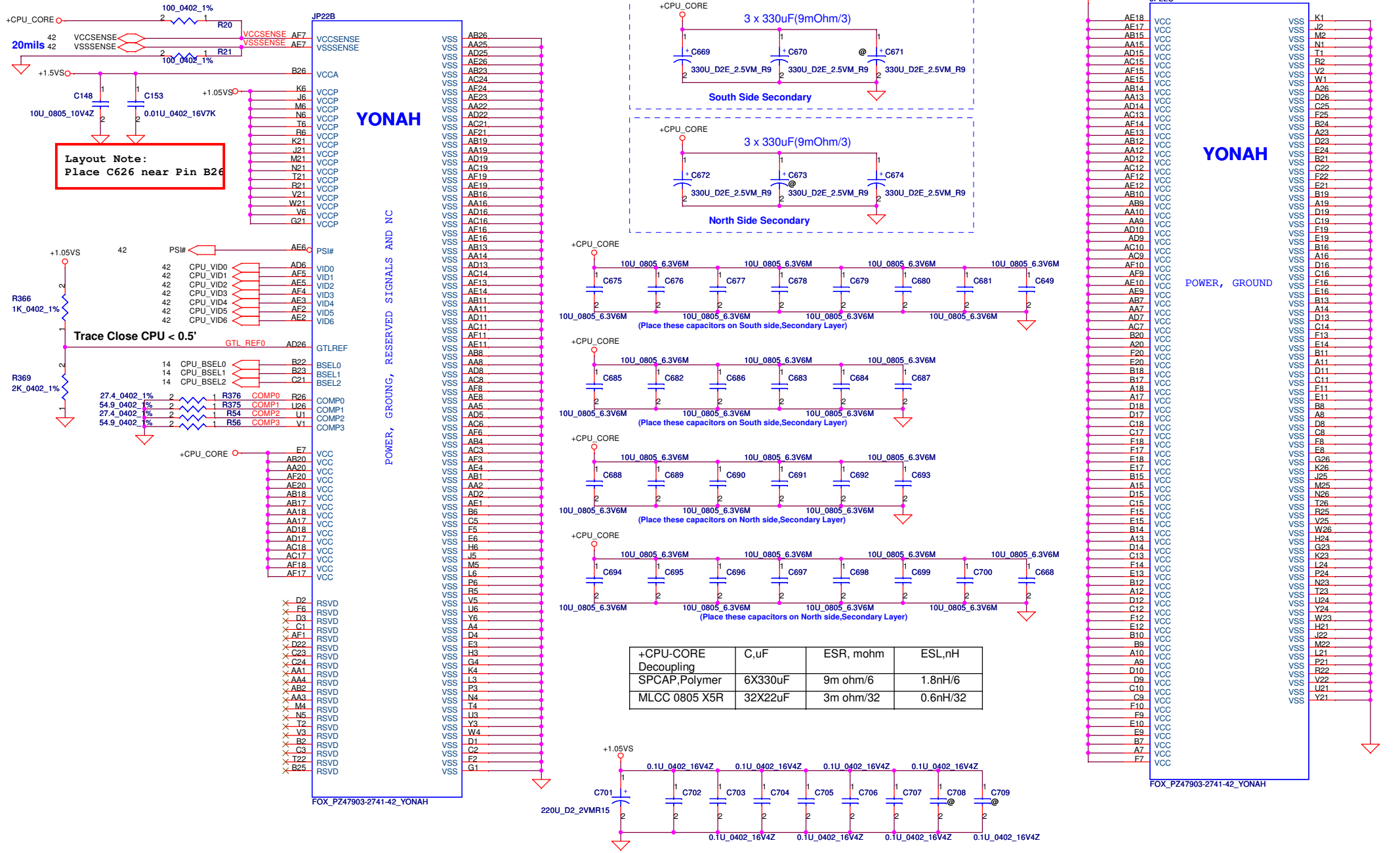

+CPU-CORE Decoupling	C,uF	ESR, mohm	ESL,nH
SPCAP,Polymer	6X330uF	9m ohm/6	1.8nH/6
MLCC 0805 X5R	32X22uF	3m ohm/32	0.6nH/32

TRACE CLOSELY CPU < 0.5'

COMP0, COMP2 layout : Width 18mils and Space 25mils (27.4Ohms)
COMP1, COMP3 layout : Space 25mils (55Ohms)

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Title	Merom (2/2)
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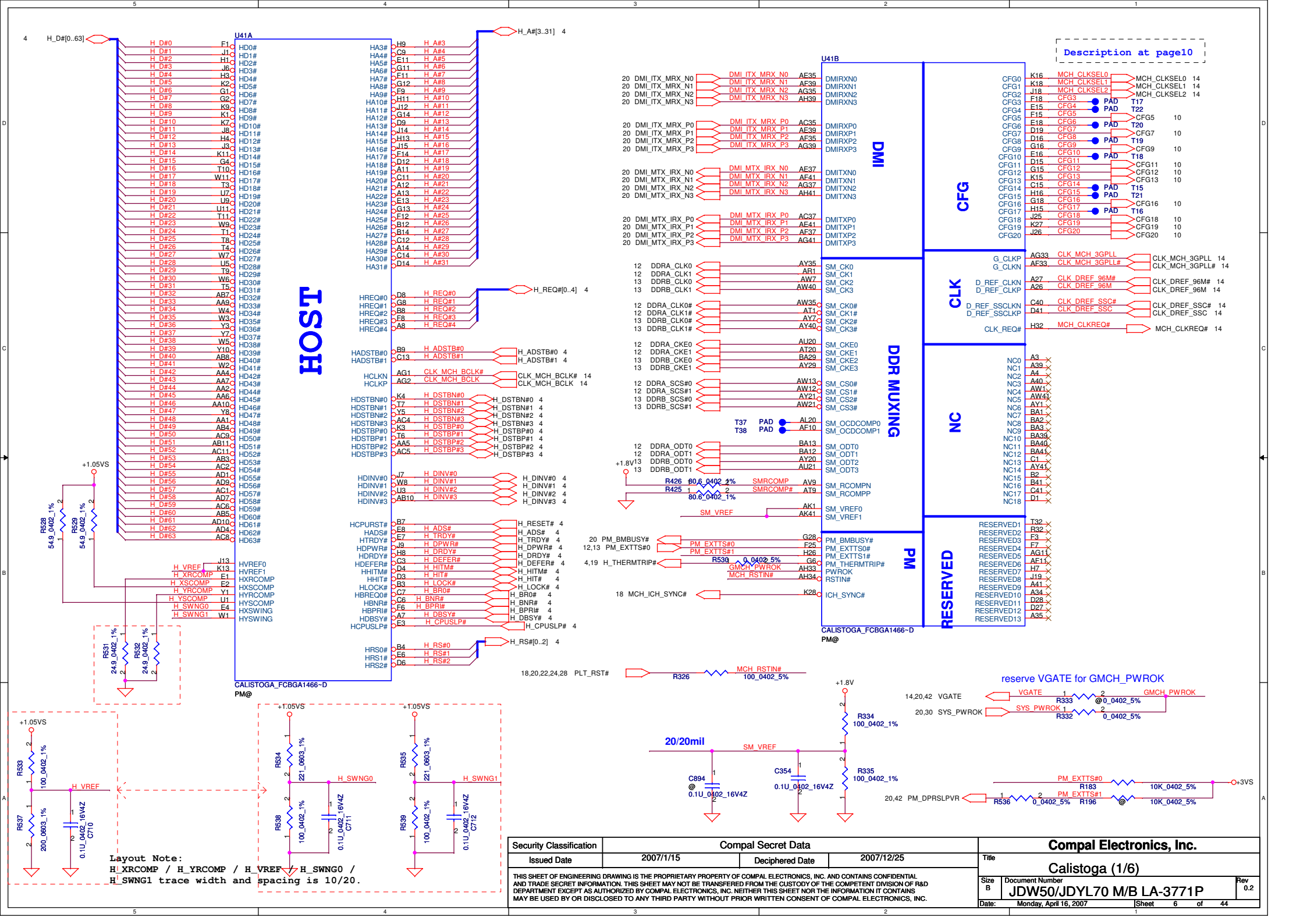

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Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title	Calistoga (1/6)	
Size B	Document Number JDW50/JDYL70 M/B LA-3771P	Rev 0.2
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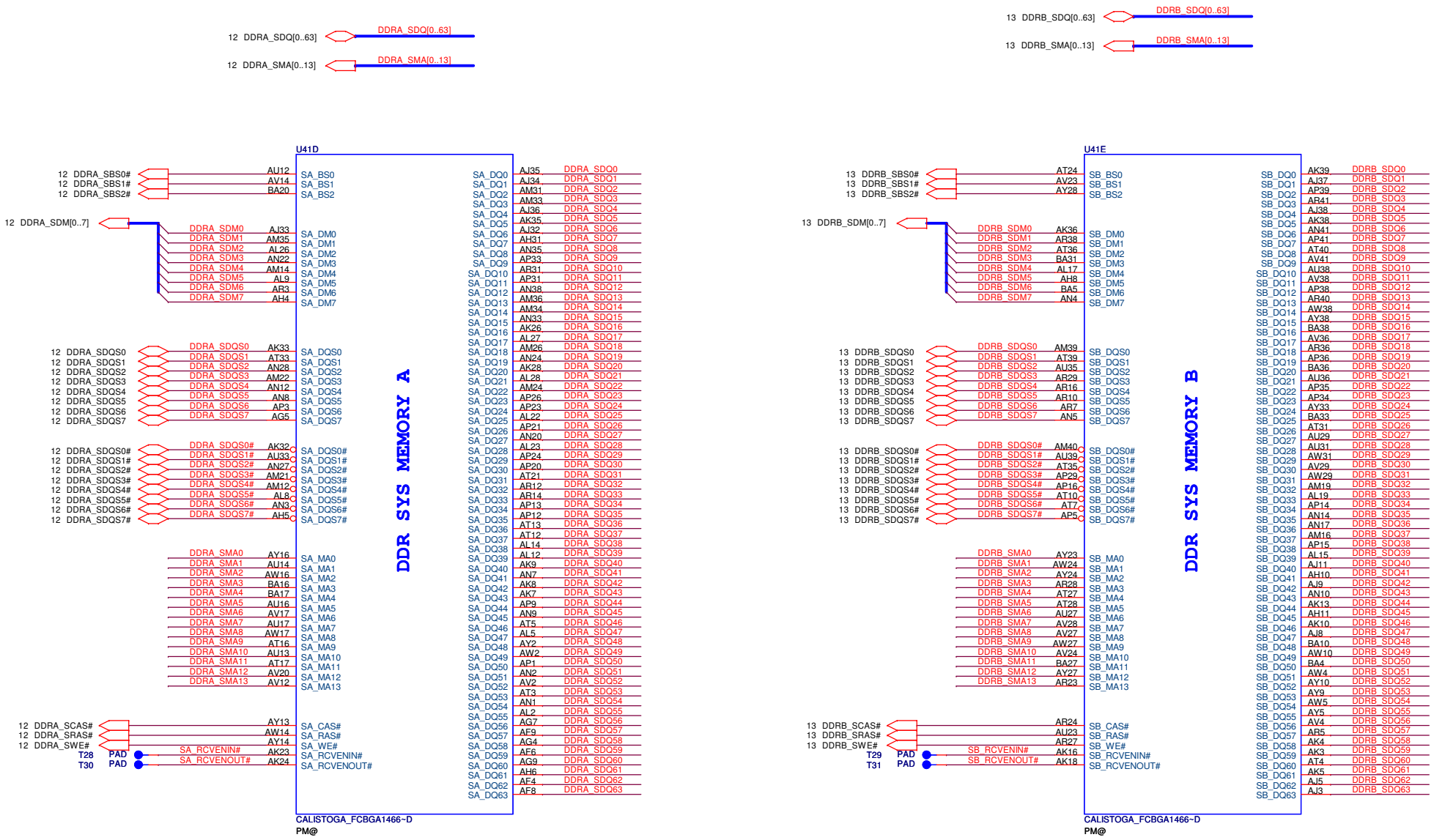

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Compal Electronics, Inc.

Title: Calistoga (2/6)

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

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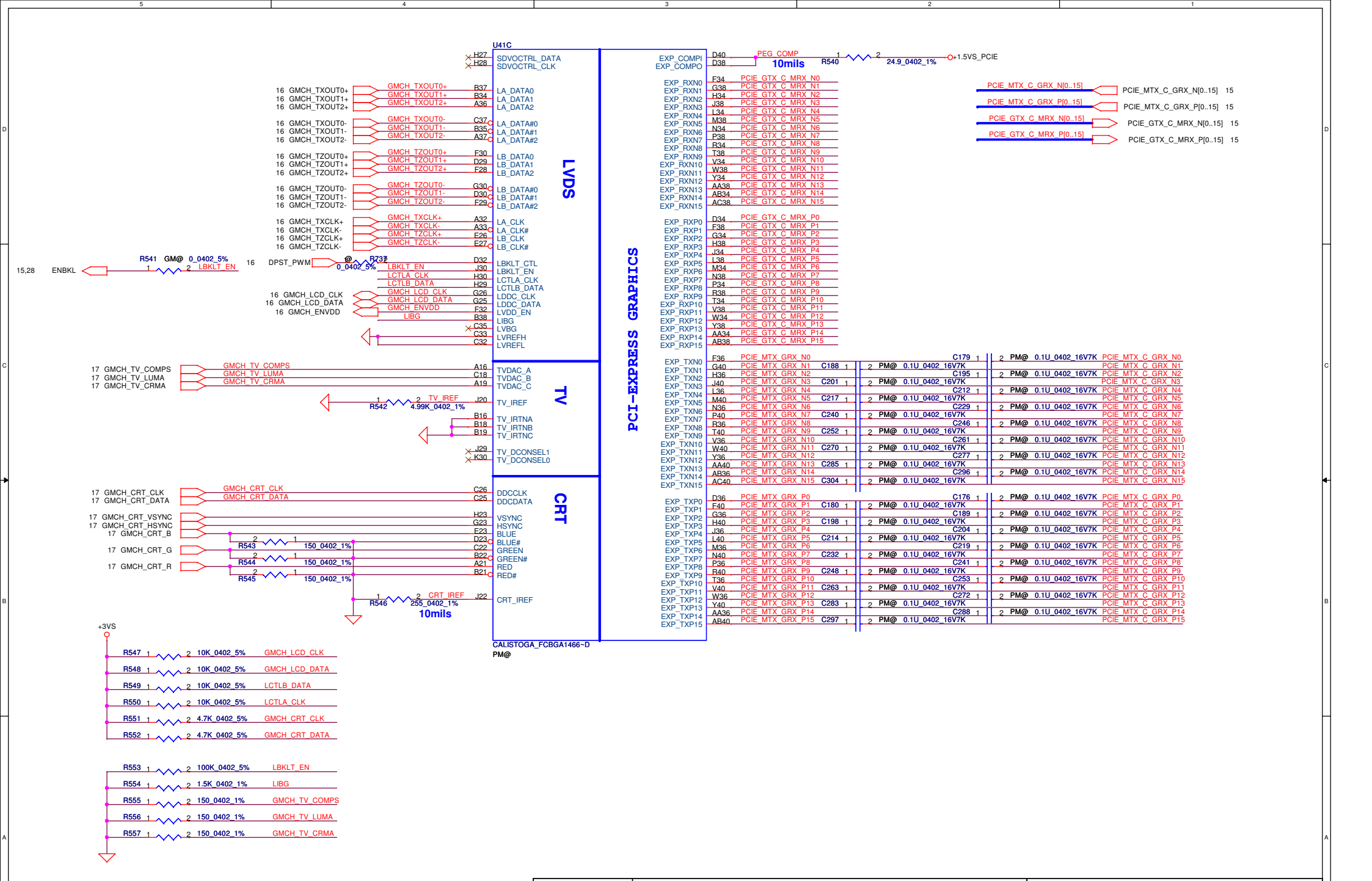

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: Calistoga (3/6)

Size: Custom | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

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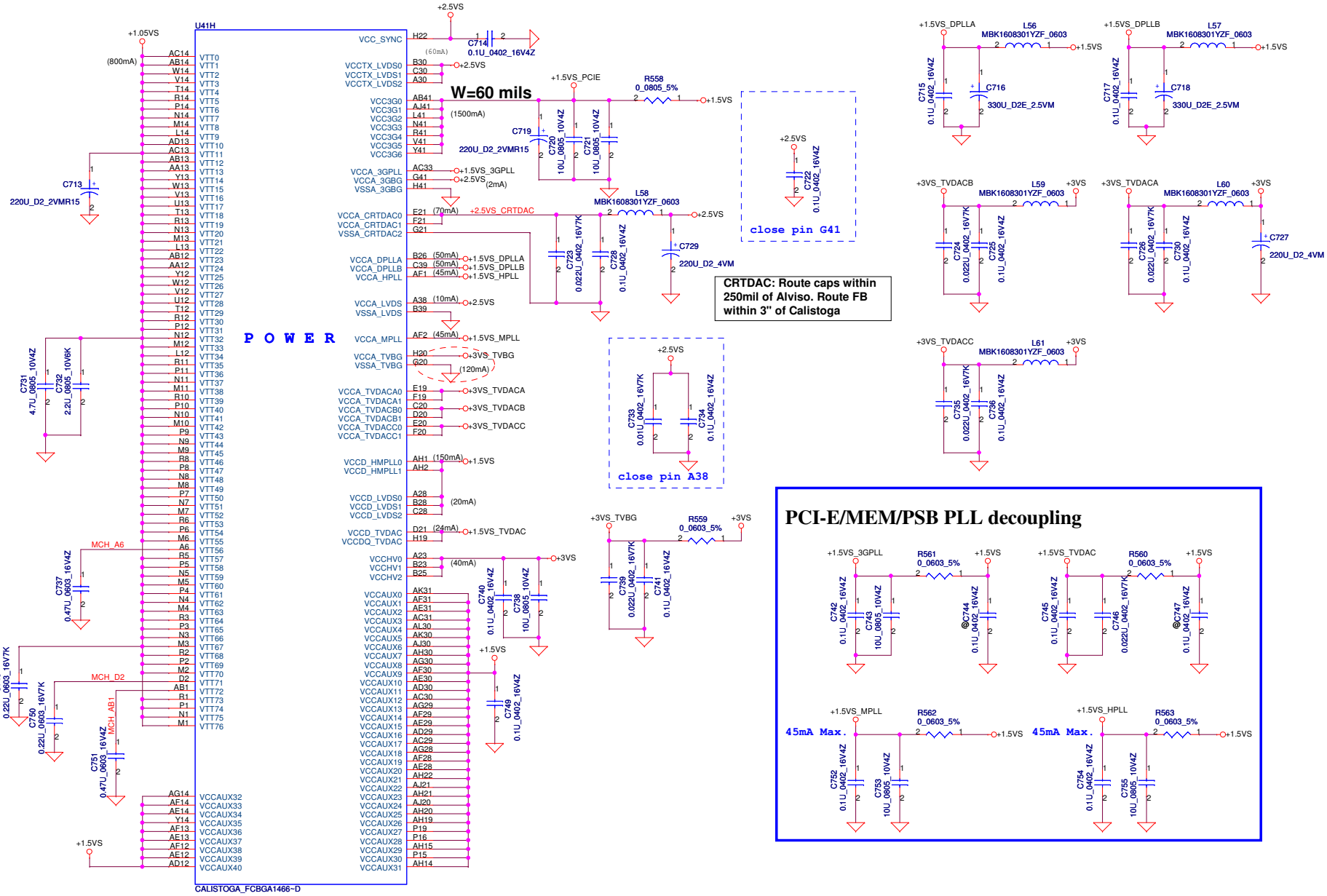

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Compal Electronics, Inc.

Title: Calistoga (4/6)

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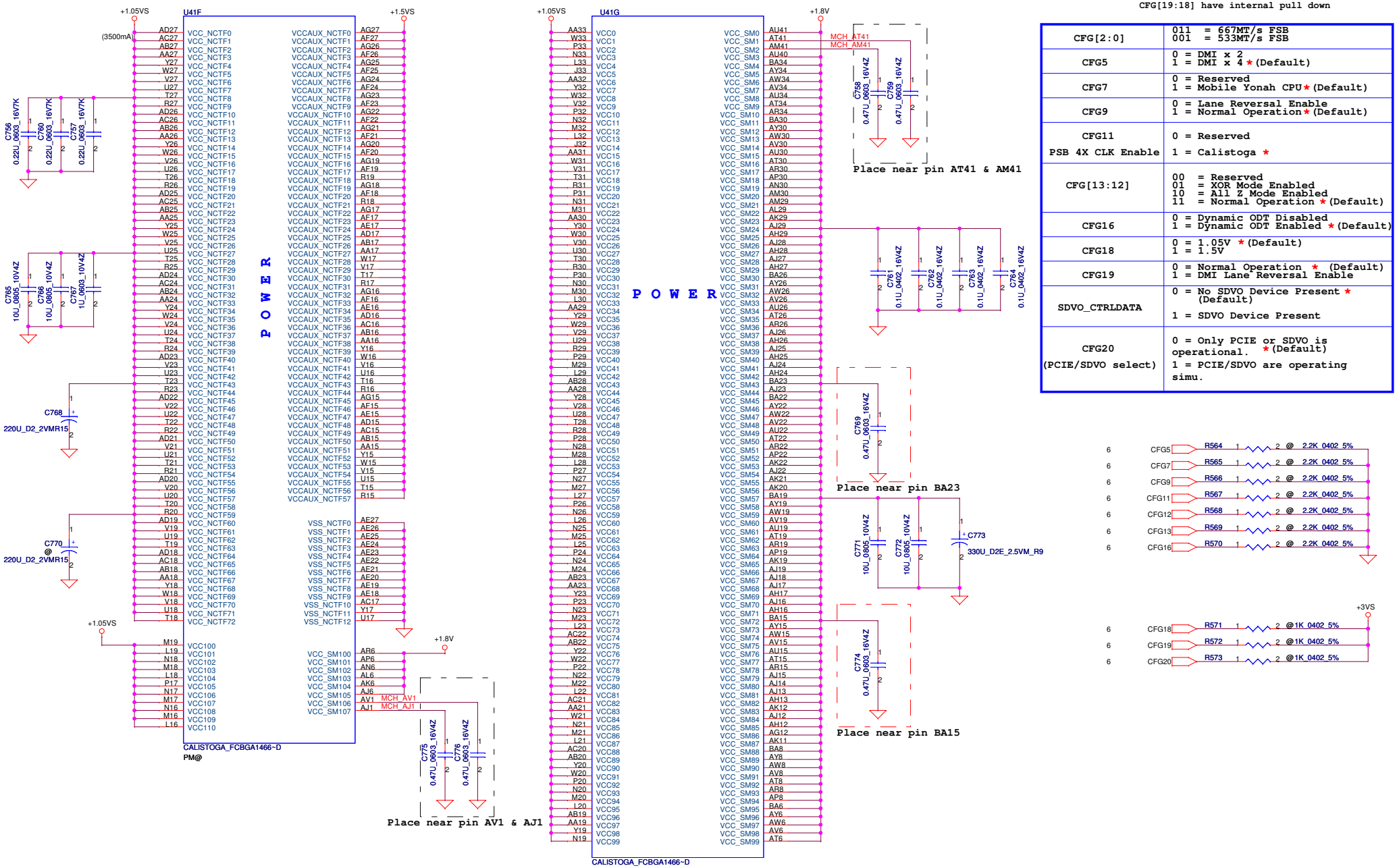

Strap Pin Table

CFG[3:17] have internal pull up

CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU *(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation *(Default)
CFG11 PSB 4X CLK Enable	0 = Reserved 1 = Calistoga *
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG18	0 = 1.05V *(Default) 1 = 1.5V
CFG19	0 = Normal Operation * (Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present * (Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.

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Compal Electronics, Inc.

Title: Calistoga (5/6)

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

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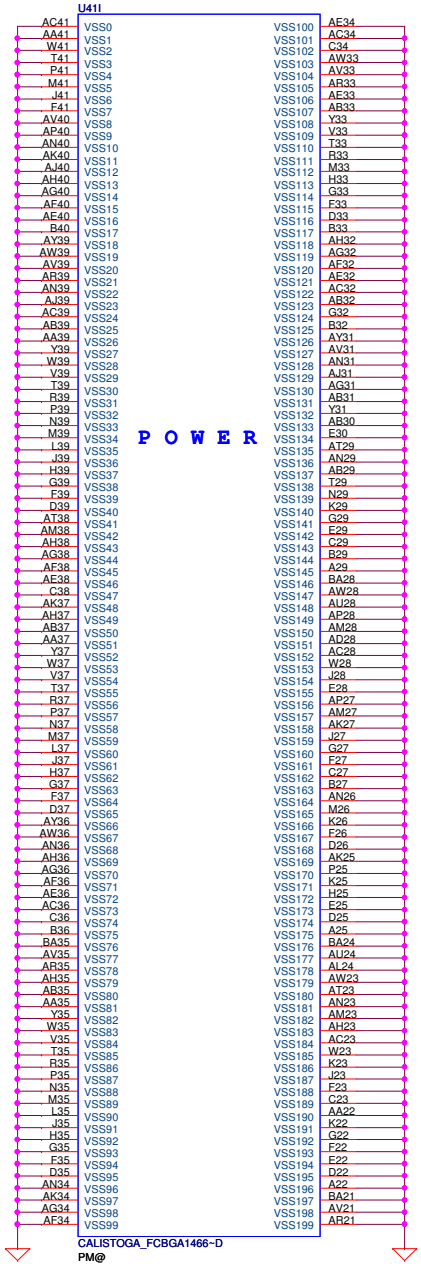

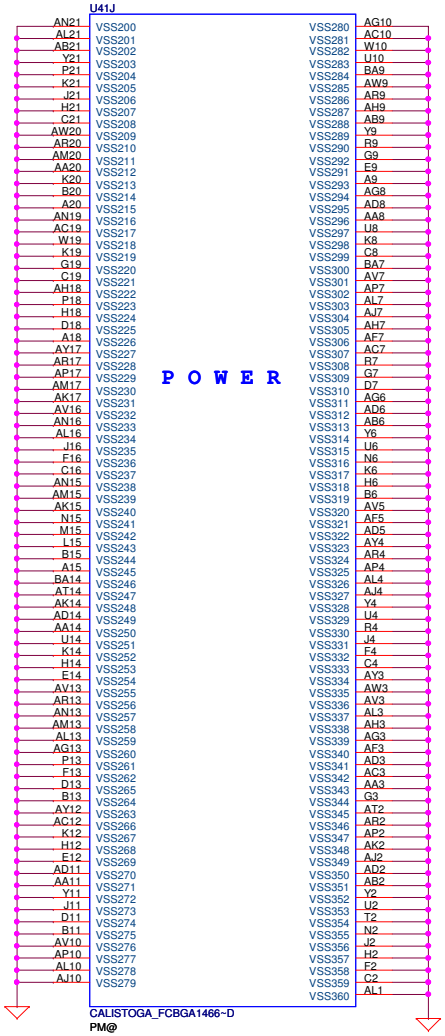

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Compal Electronics, Inc.

Title: Calistoga (6/6)

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B	JDW50/JDYL70 M/B LA-3771P	0.2

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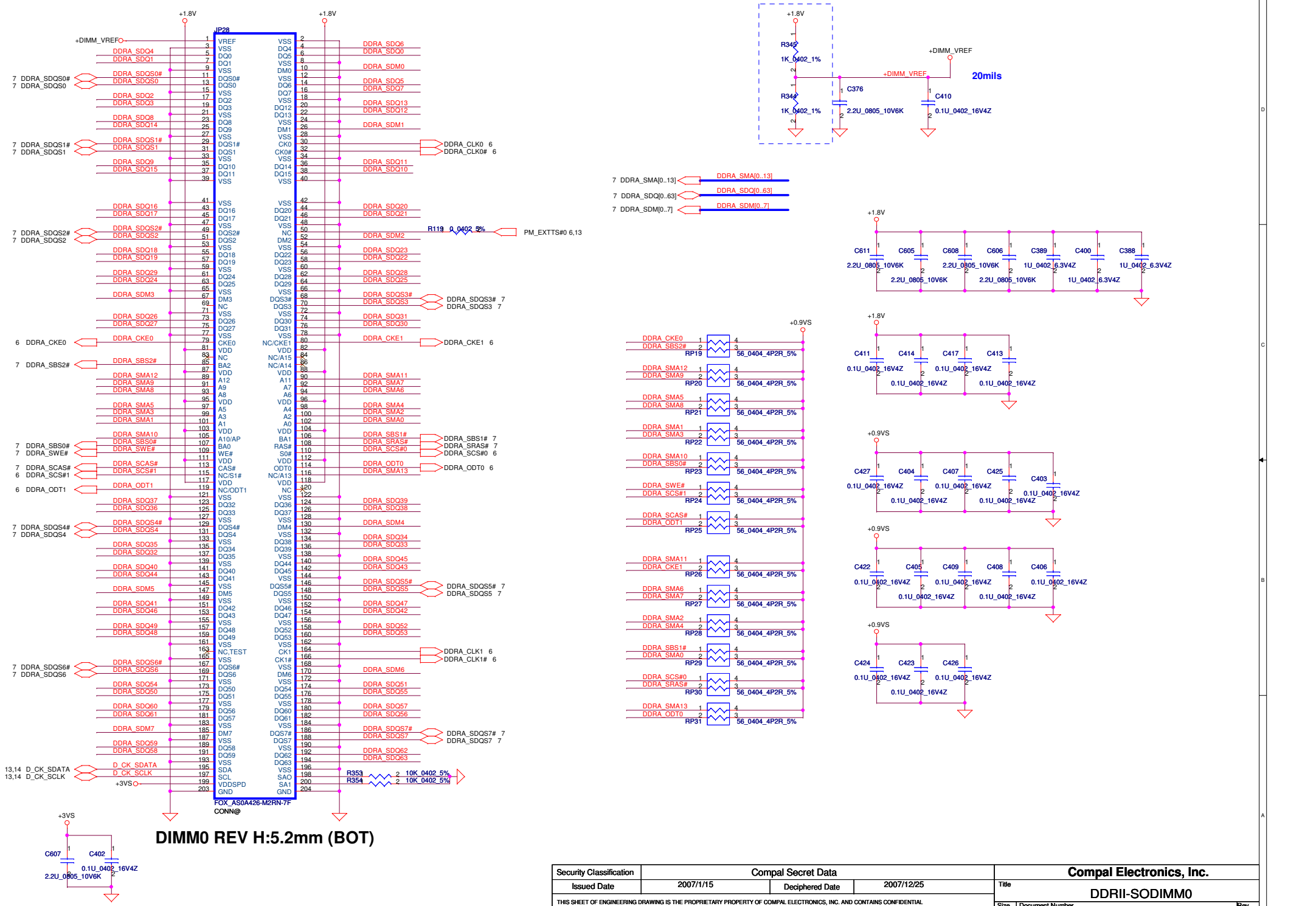

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Compal Electronics, Inc.

Title: DDRII-SODIMM0

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B	JDW50/JDYL70 M/B LA-3771P	0.2

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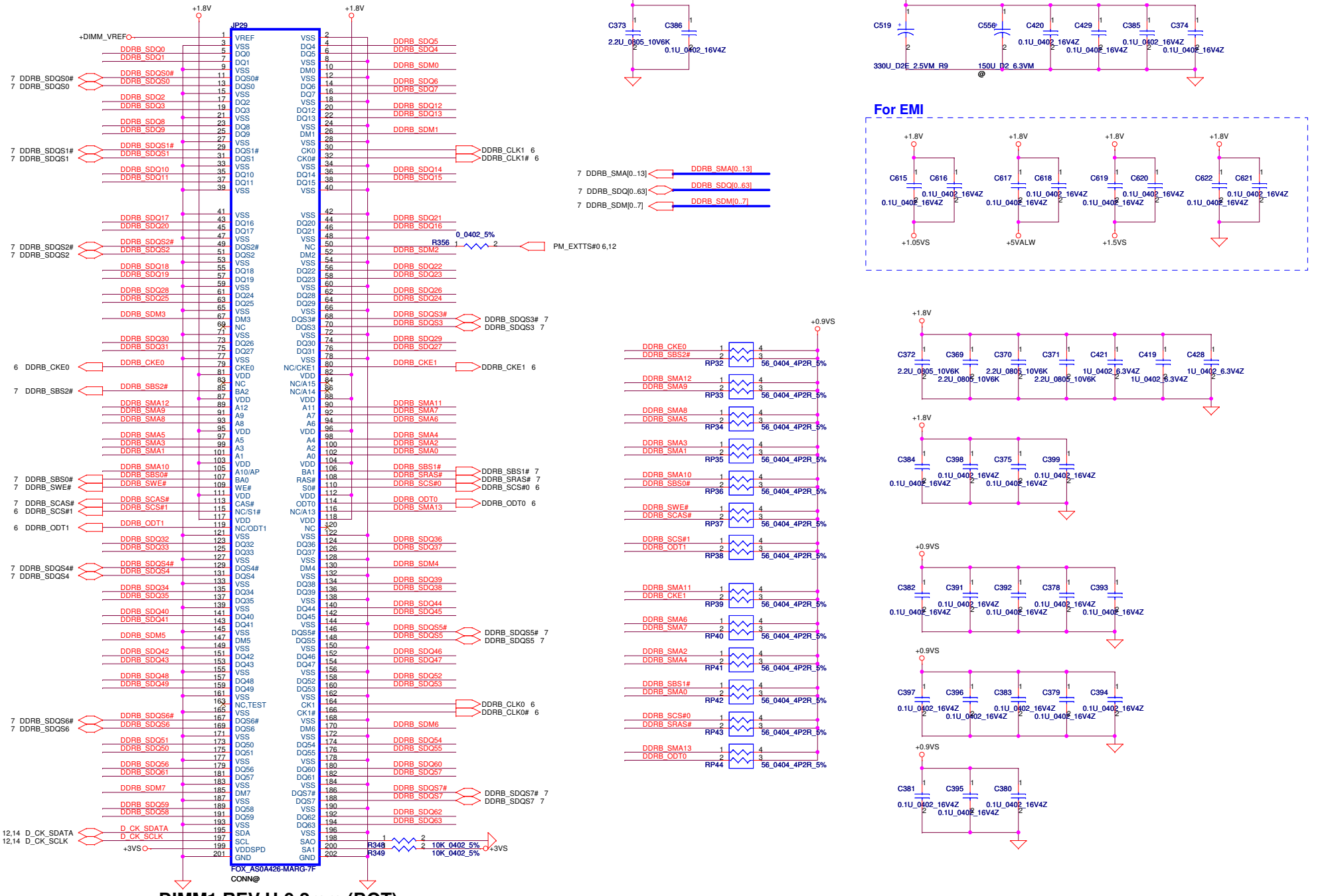

DIMM1 REV H:9.2mm (BOT)

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Compal Electronics, Inc.

Title: DDRII-SODIMM1

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Clock Generator

FSLC CLKSEL2	FSLB CLKSEL1	FSLA CLKSEL0	CPU MHz	SRC MHz	PCI MHz
0	0	1	133	100	33.3
0	1	1	166	100	33.3

Table : ICS9LPR325

	0	1
**SEL_PCI5/REF1	CLKREQ3#	33.3MHz PCICLK5
**SEL_PCI6/PCICLK1	CLKREQ5#	33.3MHz PCICLK6
**SEL_24M/PCICLK2	TESTMODE	24MHz Output
**SEL_48M/PCICLK3	CLKREQ7#	48MHz_1 Output
ITP_EN/PCICLK_F0	SRC pair	CPU_ITP pair

**SEL_24M/PCICLK2=0=TESTMODE
**SEL_PCI6/PCICLK1=0=CLKREQ5#

**SEL_PCI5=1=PCICLK5

ITP_EN/PCICLK_F0=0=SRC pair

U1 — ICS9LPR325AKLFT_MLF72

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Compal Electronics, Inc.

Title: Clock Generator

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8 PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15]
8 PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15]
8 PCIE_GTX_C_MRX_N[0..15] PCIE_GTX_C_MRX_N[0..15]
8 PCIE_GTX_C_MRX_P[0..15] PCIE_GTX_C_MRX_P[0..15]

JP19A

+MXM_B+
1 PWR_SRC
3 PWR_SRC
5 PWR_SRC
7 PWR_SRC
9 PWR_SRC
11 PWR_SRC
13 PWR_SRC
15 PWR_SRC
17 GND
19 GND
21 GND
23 GND

2 1V8RUN → +1.8VS
4 1V8RUN
6 1V8RUN
8 1V8RUN
10 1V8RUN
12 1V8RUN
14 1V8RUN
140mil(3.5A)
16 RUNPWROK → VGA_ON 30
18 5VRUN → +5VS
20 GND
22 GND
24 GND

PCIE_GTX_C_MRX_N15 25 PEX_RX15# — 26 PRSNT2#
PCIE_GTX_C_MRX_P15 27 PEX_RX15 — 28 PEX_TX15# → PCIE_MTX_C_GRX_N15
29 GND — 30 PEX_TX15 → PCIE_MTX_C_GRX_P15
PCIE_GTX_C_MRX_N14 31 PEX_RX14# — 32 GND
PCIE_GTX_C_MRX_P14 33 PEX_RX14 — 34 PEX_TX14# → PCIE_MTX_C_GRX_N14
35 GND — 36 PEX_TX14 → PCIE_MTX_C_GRX_P14
PCIE_GTX_C_MRX_N13 37 PEX_RX13# — 38 GND
PCIE_GTX_C_MRX_P13 39 PEX_RX13 — 40 PEX_TX13# → PCIE_MTX_C_GRX_N13
41 GND — 42 PEX_TX13 → PCIE_MTX_C_GRX_P13
PCIE_GTX_C_MRX_N12 43 PEX_RX12# — 44 GND
PCIE_GTX_C_MRX_P12 45 PEX_RX12 — 46 PEX_TX12# → PCIE_MTX_C_GRX_N12
47 GND — 48 PEX_TX12 → PCIE_MTX_C_GRX_P12
PCIE_GTX_C_MRX_N11 49 PEX_RX11# — 50 GND
PCIE_GTX_C_MRX_P11 51 PEX_RX11 — 52 PEX_TX11# → PCIE_MTX_C_GRX_N11
53 GND — 54 PEX_TX11 → PCIE_MTX_C_GRX_P11
PCIE_GTX_C_MRX_N10 55 PEX_RX10# — 56 GND
PCIE_GTX_C_MRX_P10 57 PEX_RX10 — 58 PEX_TX10# → PCIE_MTX_C_GRX_N10
59 GND — 60 PEX_TX10 → PCIE_MTX_C_GRX_P10
PCIE_GTX_C_MRX_N9 61 PEX_RX9# — 62 GND
PCIE_GTX_C_MRX_P9 63 PEX_RX9 — 64 PEX_TX9# → PCIE_MTX_C_GRX_N9
65 GND — 66 PEX_TX9 → PCIE_MTX_C_GRX_P9
PCIE_GTX_C_MRX_N8 67 PEX_RX8# — 68 GND
PCIE_GTX_C_MRX_P8 69 PEX_RX8 — 70 PEX_TX8# → PCIE_MTX_C_GRX_N8
71 GND — 72 PEX_TX8 → PCIE_MTX_C_GRX_P8
PCIE_GTX_C_MRX_N7 73 PEX_RX7# — 74 GND
PCIE_GTX_C_MRX_P7 75 PEX_RX7 — 76 PEX_TX7# → PCIE_MTX_C_GRX_N7
77 GND — 78 PEX_TX7 → PCIE_MTX_C_GRX_P7
PCIE_GTX_C_MRX_N6 79 PEX_RX6# — 80 GND
PCIE_GTX_C_MRX_P6 81 PEX_RX6 — 82 PEX_TX6# → PCIE_MTX_C_GRX_N6
83 GND — 84 PEX_TX6 → PCIE_MTX_C_GRX_P6
PCIE_GTX_C_MRX_N5 85 PEX_RX5# — 86 GND
PCIE_GTX_C_MRX_P5 87 PEX_RX5 — 88 PEX_TX5# → PCIE_MTX_C_GRX_N5
89 GND — 90 PEX_TX5 → PCIE_MTX_C_GRX_P5
PCIE_GTX_C_MRX_N4 91 PEX_RX4# — 92 GND
PCIE_GTX_C_MRX_P4 93 PEX_RX4 — 94 PEX_TX4# → PCIE_MTX_C_GRX_N4
95 GND — 96 PEX_TX4 → PCIE_MTX_C_GRX_P4
PCIE_GTX_C_MRX_N3 97 PEX_RX3# — 98 GND
PCIE_GTX_C_MRX_P3 99 PEX_RX3 — 100 PEX_TX3# → PCIE_MTX_C_GRX_N3
101 GND — 102 PEX_TX3 → PCIE_MTX_C_GRX_P3
PCIE_GTX_C_MRX_N2 103 PEX_RX2# — 104 GND
PCIE_GTX_C_MRX_P2 105 PEX_RX2 — 106 PEX_TX2# → PCIE_MTX_C_GRX_N2
107 GND — 108 PEX_TX2 → PCIE_MTX_C_GRX_P2

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CONN@

JP19B

PCIE_GTX_C_MRX_N1 109 PEX_RX1# — 110 GND
PCIE_GTX_C_MRX_P1 111 PEX_RX1 — 112 PEX_TX1# → PCIE_MTX_C_GRX_N1
113 GND — 114 PEX_TX1 → PCIE_MTX_C_GRX_P1
PCIE_GTX_C_MRX_N0 115 PEX_RX0# — 116 GND
PCIE_GTX_C_MRX_P0 117 PEX_RX0 — 118 PEX_TX0# → PCIE_MTX_C_GRX_N0
119 GND — 120 PEX_TX0 → PCIE_MTX_C_GRX_P0
14 CLK_PCIE_VGA# CLK_PCIE_VGA# 121 PEX_REFCLK# — 122 PRSNT1#
14 CLK_PCIE_VGA CLK_PCIE_VGA 123 PEX_REFCLK — 124 TV_C/HDTV_Pr → VGA_TV_CRMA
125 CLK_REQ# — 126 GND
18 PLTRST_VGA# 127 PEX_RST# — 128 TV_Y/HDTV_Y → VGA_TV_LUMA
129 RSVD — 130 GND
131 RSVD — 132 TV_CVBS/HDTV_Pb → VGA_TV_COMPS
D_EC_SMB_DA1 133 SMB_DAT — 134 GND
D_EC_SMB_CK1 135 SMB_CLK — 136 VGA_RED → VGA_CRT_R
137 THERM# — 138 GND
17 VGA_CRT_HSYNC VGA_CRT_HSYNC 139 VGA_HSYNC — 140 VGA_GRN → VGA_CRT_G
17 VGA_CRT_VSYNC VGA_CRT_VSYNC 141 VGA_VSYNC — 142 GND
17 VGA_DDC_CLK VGA_DDC_CLK 143 DDCA_CLK — 144 VGA_BLU → VGA_CRT_B
17 VGA_DDC_DATA VGA_DDC_DATA 145 DDCA_DAT — 146 GND
147 IGP_UCLK# — 148 LVDS_UCLK# → VGA_TZCLK-
149 IGP_UCLK — 150 LVDS_UCLK → VGA_TZCLK+
151 GND — 152 GND
153 RSVD — 154 LVDS_UTX3#
155 RSVD — 156 LVDS_UTX3
157 RSVD — 158 GND
159 IGP_UTX2# — 160 LVDS_UTX2# → VGA_TZOUT2-
161 IGP_UTX2 — 162 LVDS_UTX2 → VGA_TZOUT2+
163 GND — 164 GND
165 IGP_UTX1# — 166 LVDS_UTX1# → VGA_TZOUT1-
167 IGP_UTX1 — 168 LVDS_UTX1 → VGA_TZOUT1+
169 GND — 170 GND
171 IGP_UTX0# — 172 LVDS_UTX0# → VGA_TZOUT0-
173 IGP_UTX0 — 174 LVDS_UTX0 → VGA_TZOUT0+
175 GND — 176 GND
177 IGP_LCLK#/DVI_B_CLK# — 178 LVDS_LCLK# → VGA_TXCLK-
179 IGP_LCLK/DVI_B_CLK — 180 LVDS_LCLK → VGA_TXCLK+
181 DVI_B_HPD/GND — 182 GND
183 RSVD — 184 LVDS_LTX3#
185 RSVD — 186 LVDS_LTX3
187 GND — 188 GND
189 IGP_LTX2#/DVI_B_TX2# — 190 LVDS_LTX2# → VGA_TXOUT2-
191 IGP_LTX2/DVI_B_TX2 — 192 LVDS_LTX2 → VGA_TXOUT2+
193 GND — 194 GND
195 IGP_LTX1#/DVI_B_TX1# — 196 LVDS_LTX1# → VGA_TXOUT1-
197 IGP_LTX1/DVI_B_TX1 — 198 LVDS_LTX1 → VGA_TXOUT1+
199 GND — 200 GND
201 IGP_LTX0#/DVI_B_TX0# — 202 LVDS_LTX0# → VGA_TXOUT0-
203 IGP_LTX0/DVI_B_TX0 — 204 LVDS_LTX0 → VGA_TXOUT0+
205 DVI_A_HPD — 206 GND
16 DVI_DET DVI_DET 207 DVI_A_CLK# — 208 DDCC_DAT → I2CC_SDA
16 VGA_DVI_TXC- VGA_DVI_TXC- 209 DVI_A_CLK — 210 DDCC_CLK → I2CC_SCL
16 VGA_DVI_TXC+ VGA_DVI_TXC+ 211 GND — 212 LVDS_PPEN → ENVDD
16 VGA_DVI_TXD2- VGA_DVI_TXD2- 213 DVI_A_TX2# — 214 LVDS_BL_BRGHT
16 VGA_DVI_TXD2+ VGA_DVI_TXD2+ 215 DVI_A_TX2 — 216 LVDS_BLEN → ENBKL
217 GND — 218 DDCB_DAT → VGA_DVI_SDATA
16 VGA_DVI_TXD1- VGA_DVI_TXD1- 219 DVI_A_TX1# — 220 DDCB_CLK → VGA_DVI_SCLK
16 VGA_DVI_TXD1+ VGA_DVI_TXD1+ 221 DVI_A_TX1 — 222 2V5RUN → +2.5VS
223 GND — 224 GND
16 VGA_DVI_TXD0- VGA_DVI_TXD0- 225 DVI_A_TX0# — 226 3V3RUN → +3VS
16 VGA_DVI_TXD0+ VGA_DVI_TXD0+ 227 DVI_A_TX0 — 228 3V3RUN
229 GND — 230 3V3RUN
231 GND — 232 GND

ACES_88990-2D08
CONN@

+MXM_B+
160mil(4A)
L44 2 1 KC FBM-L11-201209-221LMAT_0805 PM@
L43 2 1 KC FBM-L11-201209-221LMAT_0805 PM@
B+
160mil(4A)
C525 0.1U_0603_25V7K
C526 PM@ 680P_0603_50V7K
C527 68P_0402_50V8J

+2.5VS
C471 0.1U_0402_16V4Z PM@
+5VS
C520 0.1U_0402_16V4Z PM@

+3VS
28,29,38 EC_SMB_DA1 → D_EC_SMB_DA1
Q46 PM@ 2N7002_SOT23
28,29,38 EC_SMB_CK1 → D_EC_SMB_CK1
Q47 PM@ 2N7002_SOT23

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

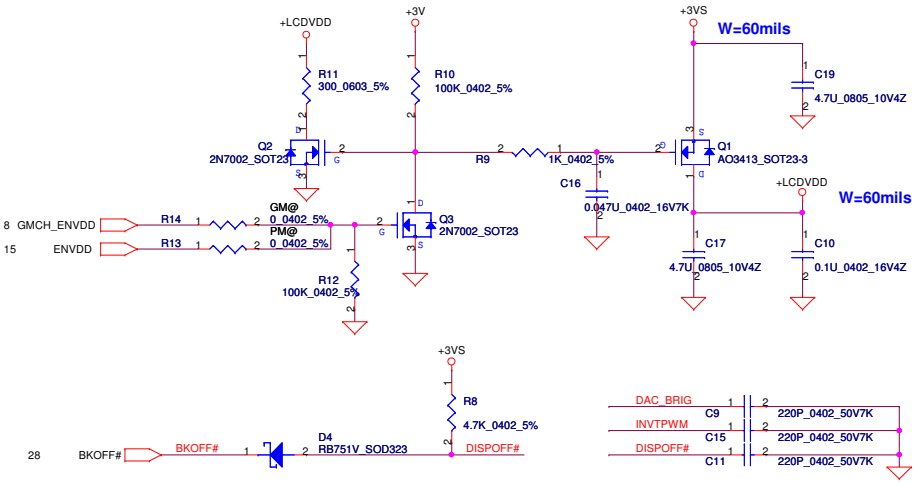
Compal Electronics, Inc.

Title: MXM Connector

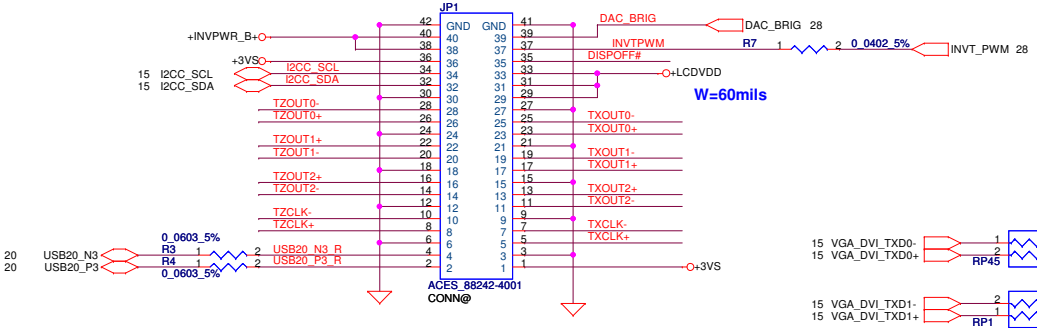
Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

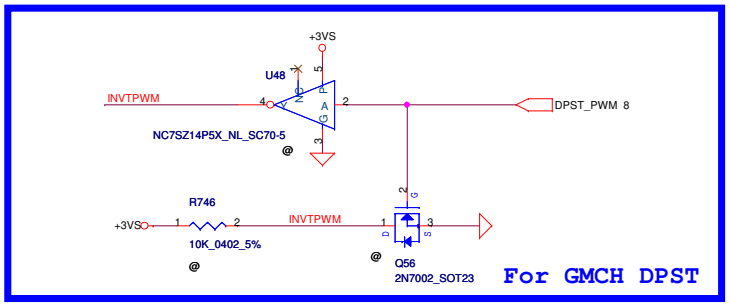
Date: Monday, April 16, 2007 Sheet 15 of 44

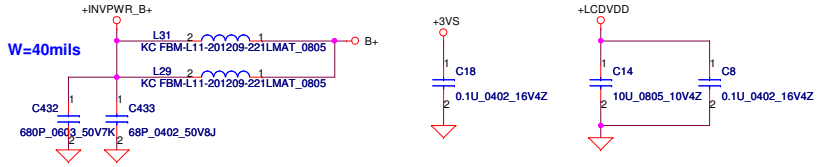
LCD POWER CIRCUIT

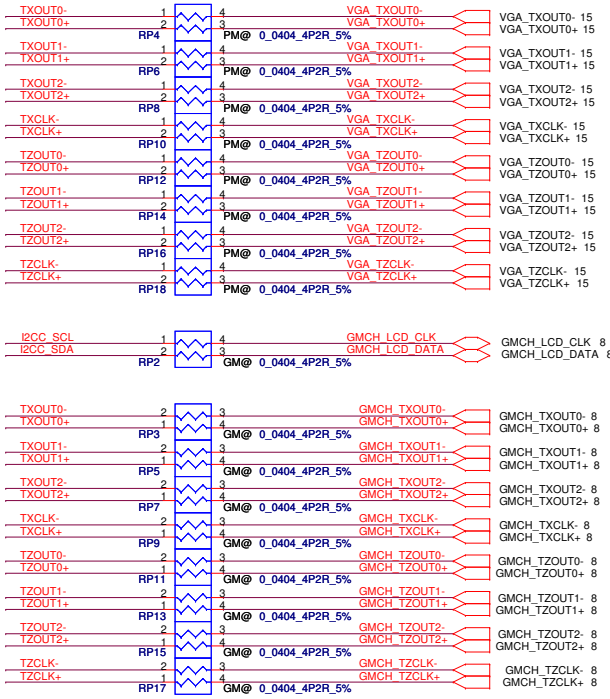


LCD/PANEL BD. Conn.

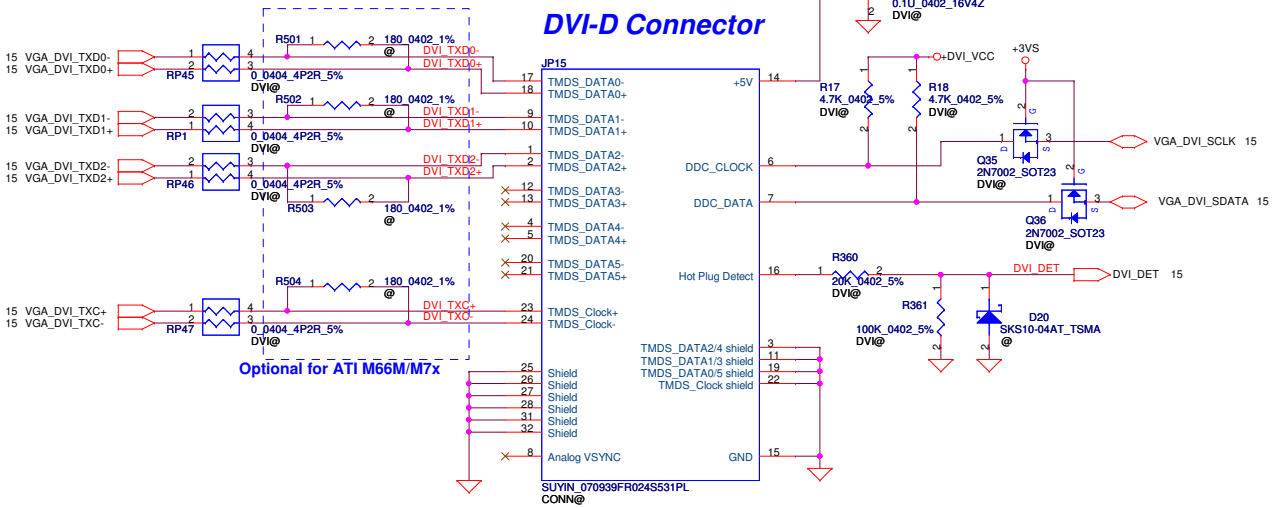








DVI-D Connector



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

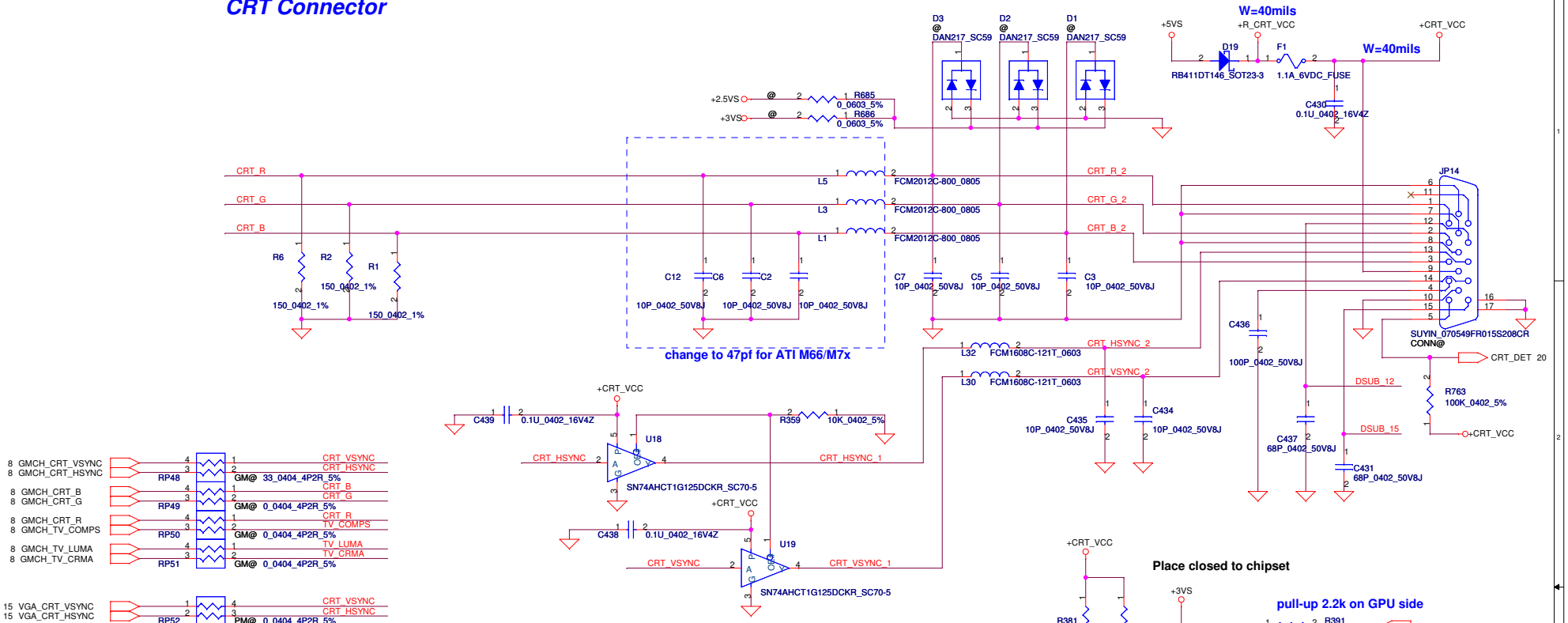
Compal Electronics, Inc.

Title: LVDS & DVI Connector

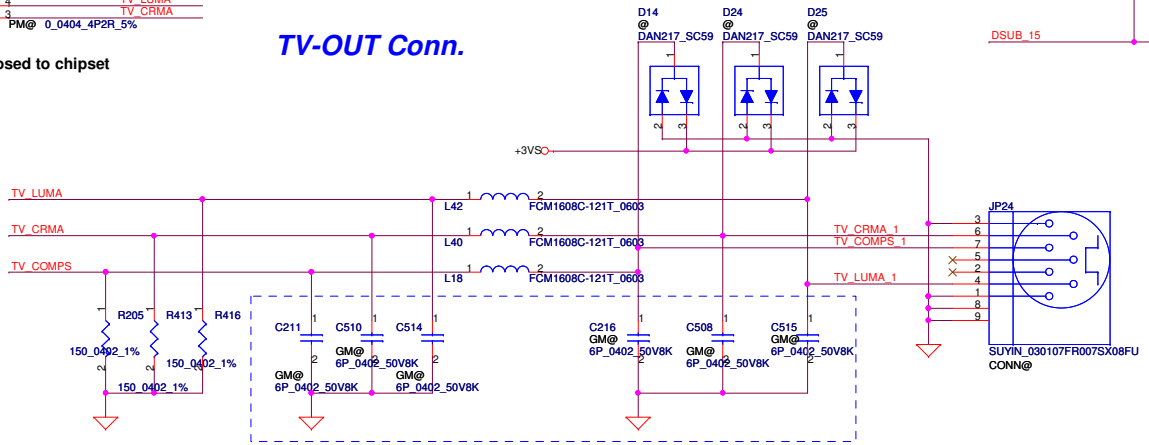
Size: B | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

Date: Monday, April 16, 2007 | Sheet 16 of 44

CRT Connector



TV-OUT Conn.



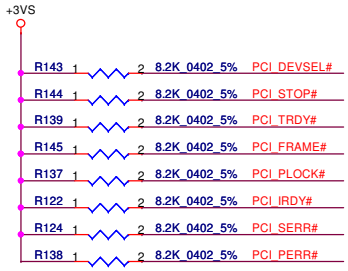
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

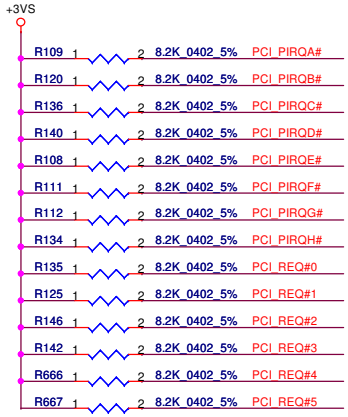
Compal Electronics, Inc.

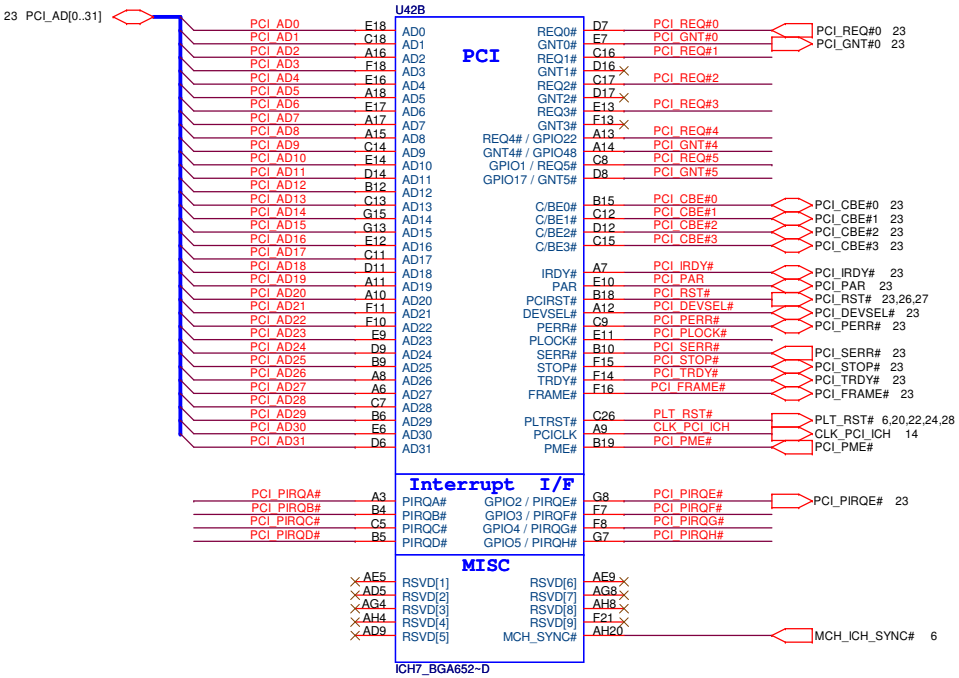
Title: CRT & TV-OUT Connector

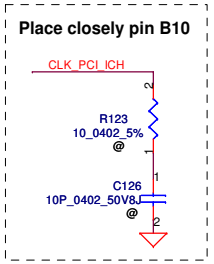
Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 | Sheet 17 of 44

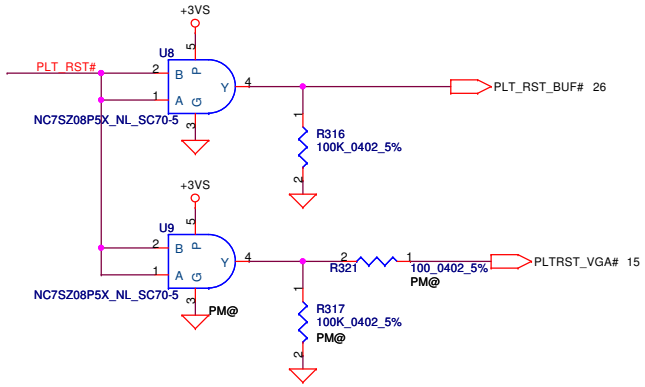








Boot BIOS Strap		
PCI_GNT#5	PCI_GNT#4	Boot BIOS Loaction
0	1	SPI
1	0	PCI
1	1	LPC*



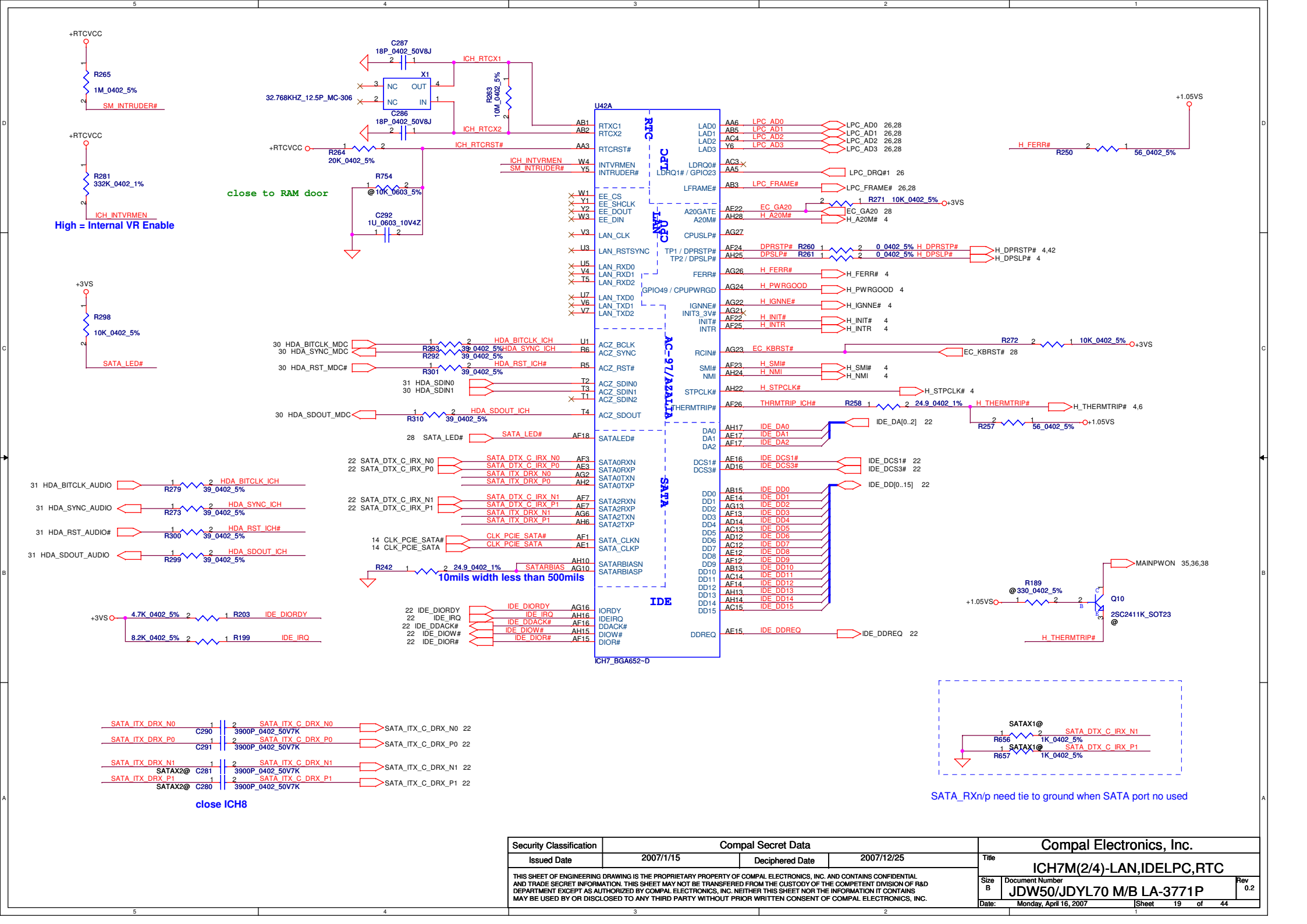
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH7M(1/4)-PCI

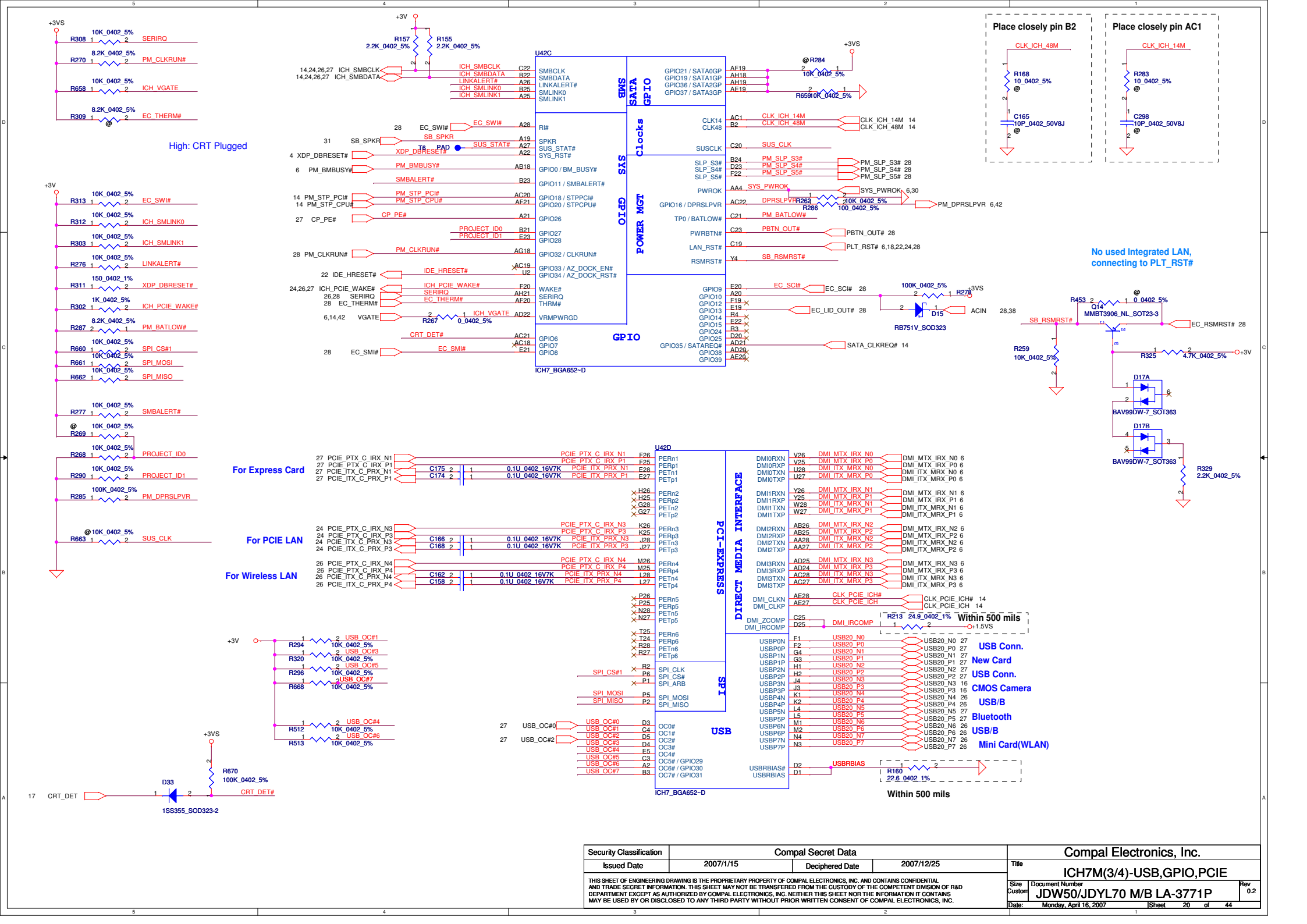
Size | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

Date: Monday, April 16, 2007 | Sheet 18 of 44



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.			
Title	ICH7M(2/4)-LAN,IDELPC,RTC		
Size B	Document Number JDW50/JDYL70 M/B LA-3771P		Rev 0.2
Date: Monday, April 16, 2007	Sheet 19 of 44		



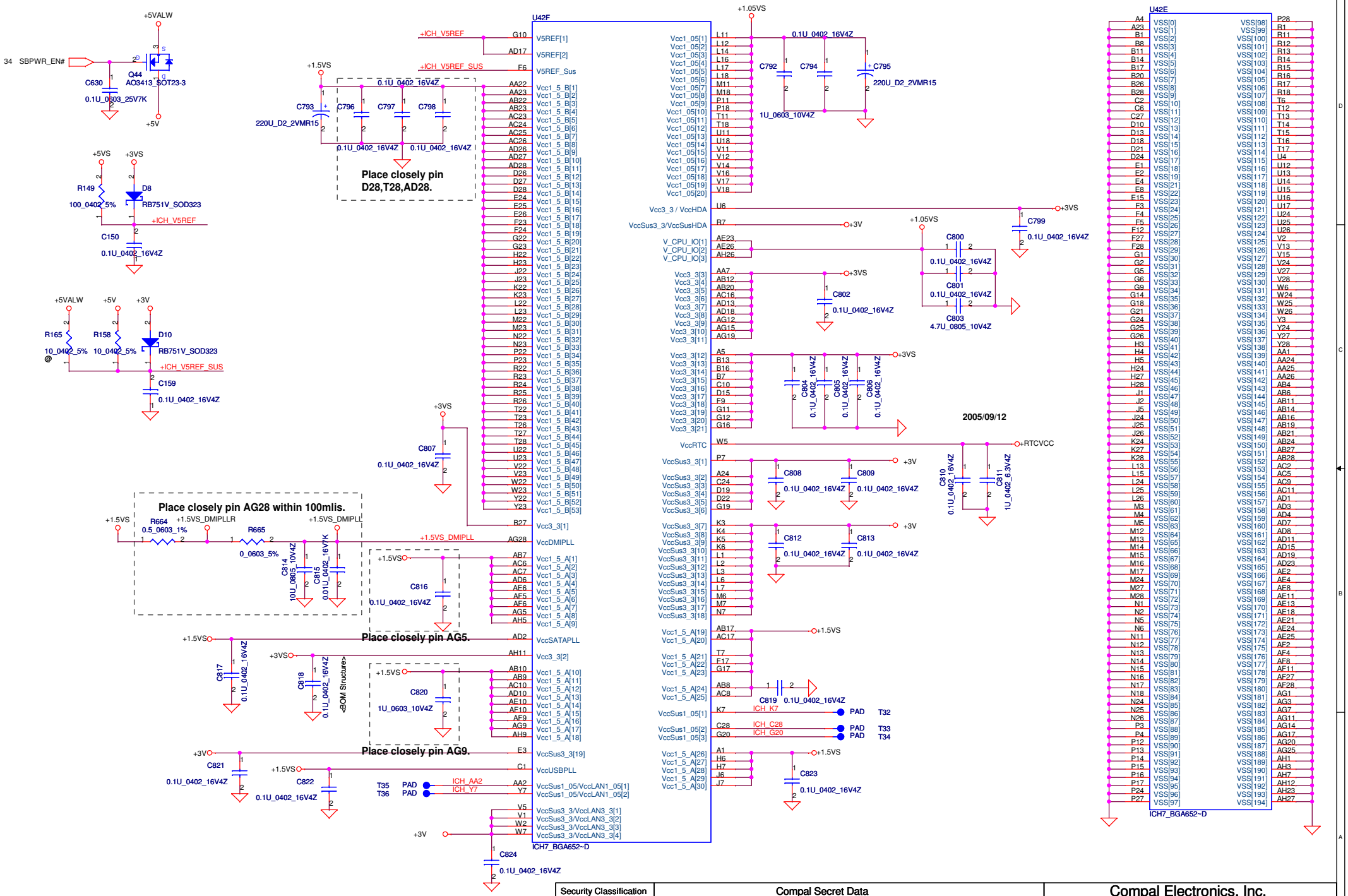
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: ICH7M(3/4)-USB,GPIO,PCIE

Size: Custom | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

Date: Monday, April 16, 2007 | Sheet 20 of 44



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

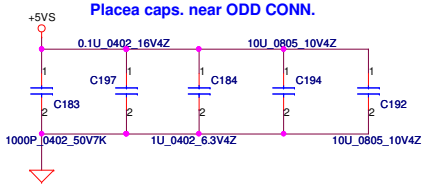
Compal Electronics, Inc.

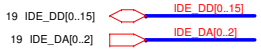
Title: ICH7M(4/4)-POWER&GND

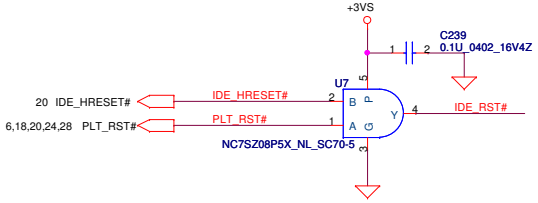
Size: Custom | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

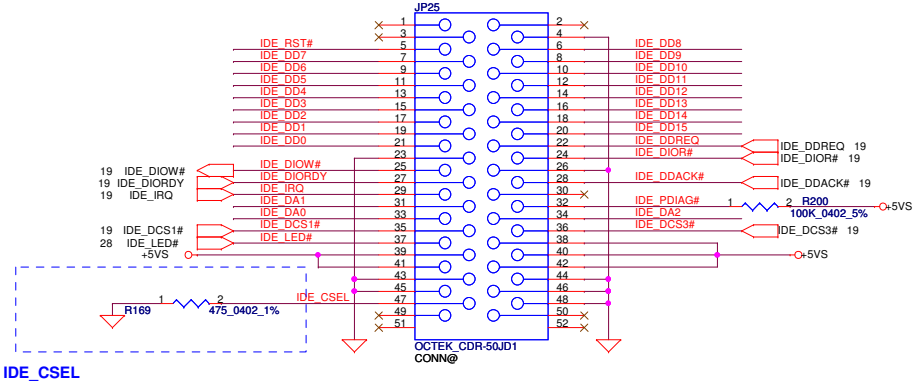
Date: Monday, April 16, 2007 | Sheet 21 of 44

Placea caps. near ODD CONN.

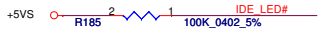


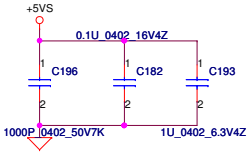


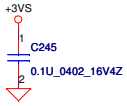




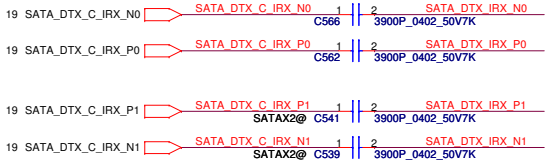
IDE_CSEL
Grounding for Master (When use SATA HDD)
Open or High for Slaver (Normal)

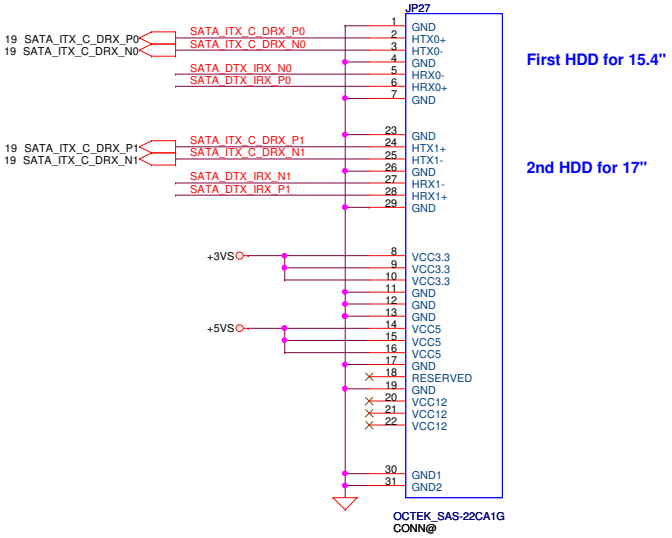






SATA HDD Conn.(SAS Connector)





Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: HDD & ODD Connector

Size: B | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

Date: Monday, April 16, 2007 | Sheet 22 of 44

PS: only below need to pull high
others have internal Pull high

pin 118 XD SMRE#
pin 7 XD SMWE#
pin 111 XD BSY#
pin 21 XD CE#

MR510

MR510QFA1_LQFP128_14X14

xD PU and PD. Close to Socket

MS signal

xd signal

SD signal

Memory Card Power Switch

4 IN 1 Socket Push Type(New)

4 IN 1 CONN

TAITW_R015-312-LM

CONN@

Reserve for SD,MS CLK. Close to Socket

MFUN0	
MFUN1	w/o eerom pull low
MFUN2	
MFUN3	
MFUN4	w/o eerom pull low
MFUN5	
MFUN6	
MFUN7	

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

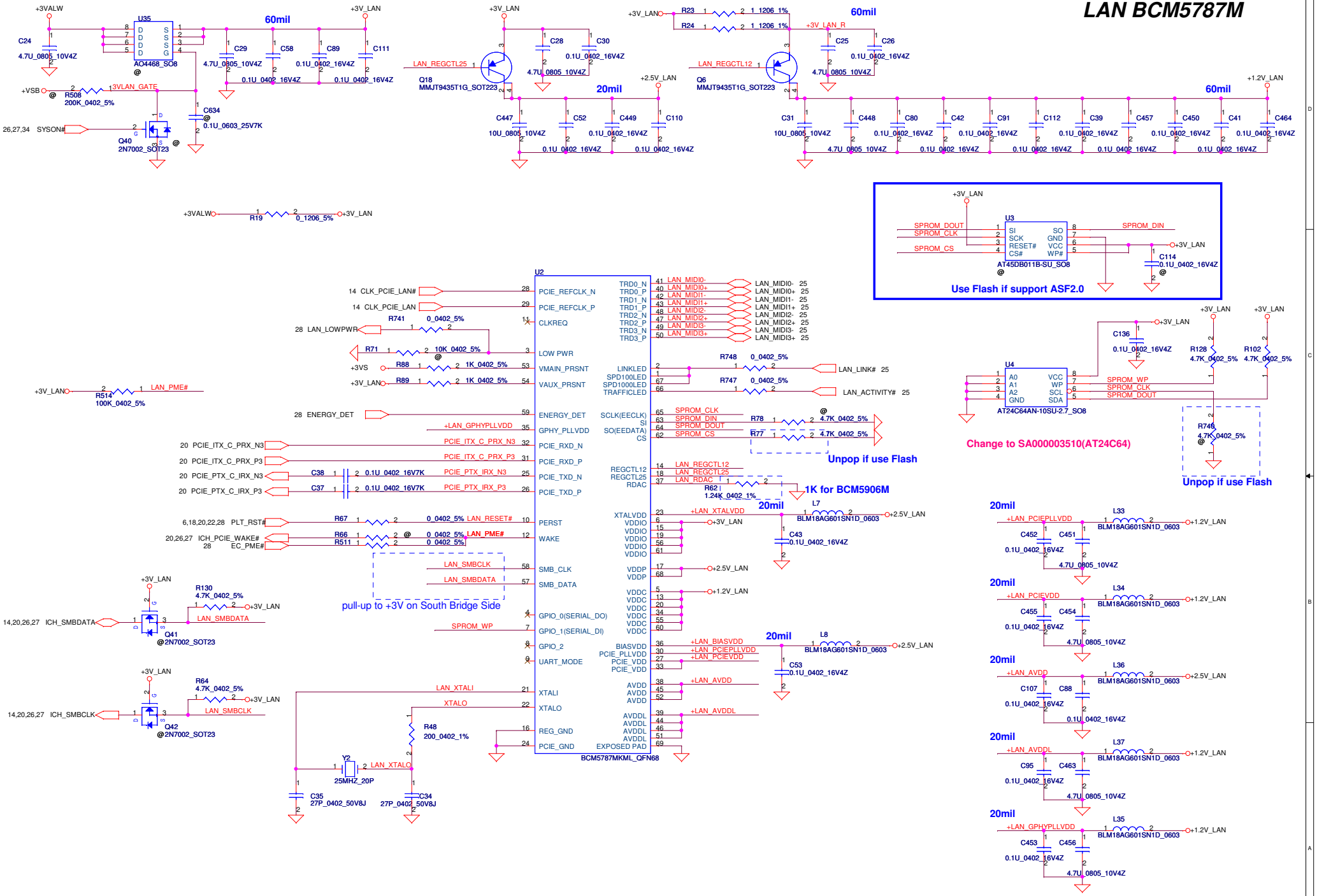
Compal Electronics, Inc.

Title: R5C833 5IN1 & IEEE1394

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 Sheet 23 of 44

LAN BCM5787M



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

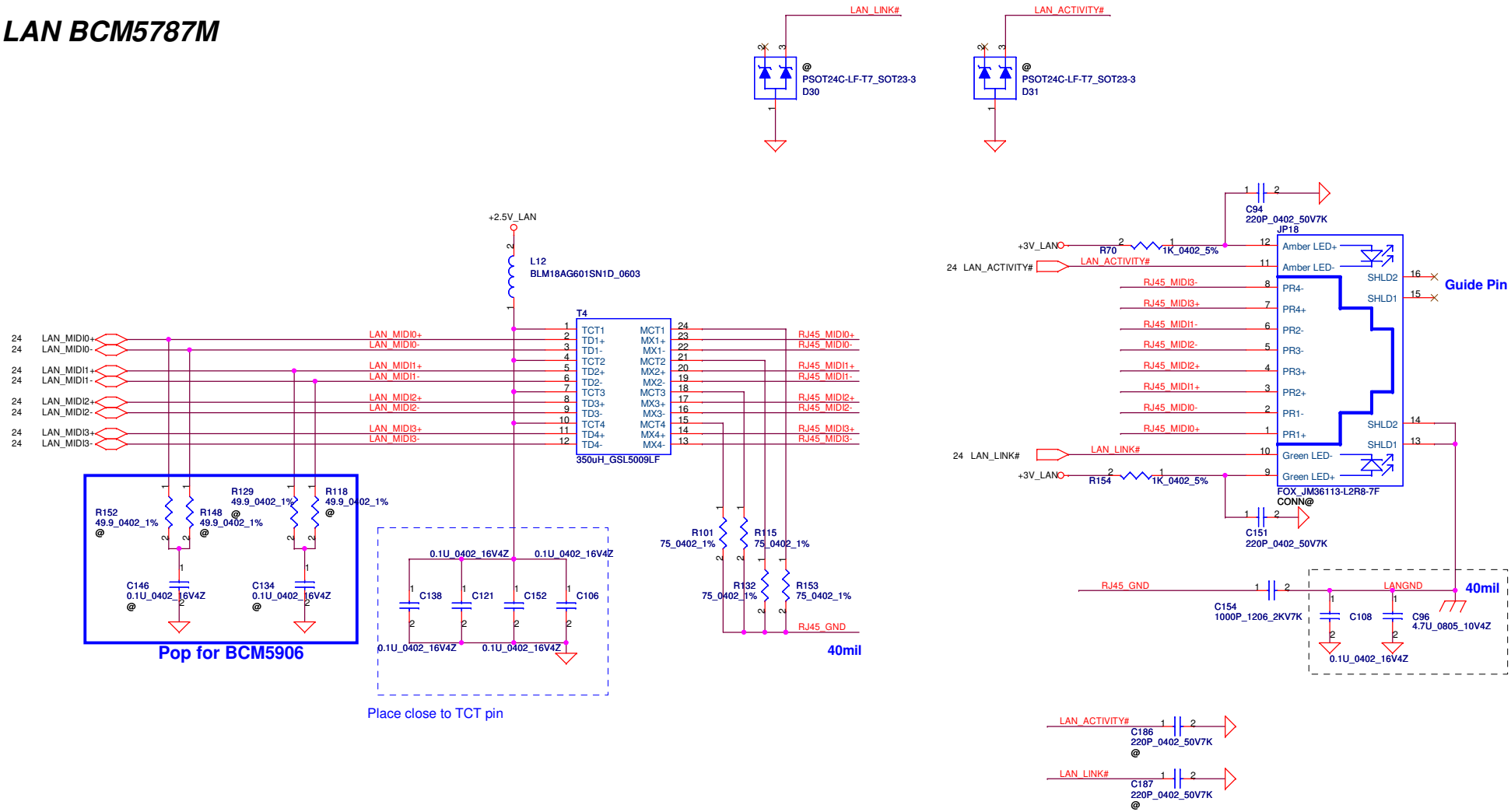
Compal Electronics, Inc.

Title: LAN BCM5787M

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 | Sheet 24 of 44

LAN BCM5787M



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

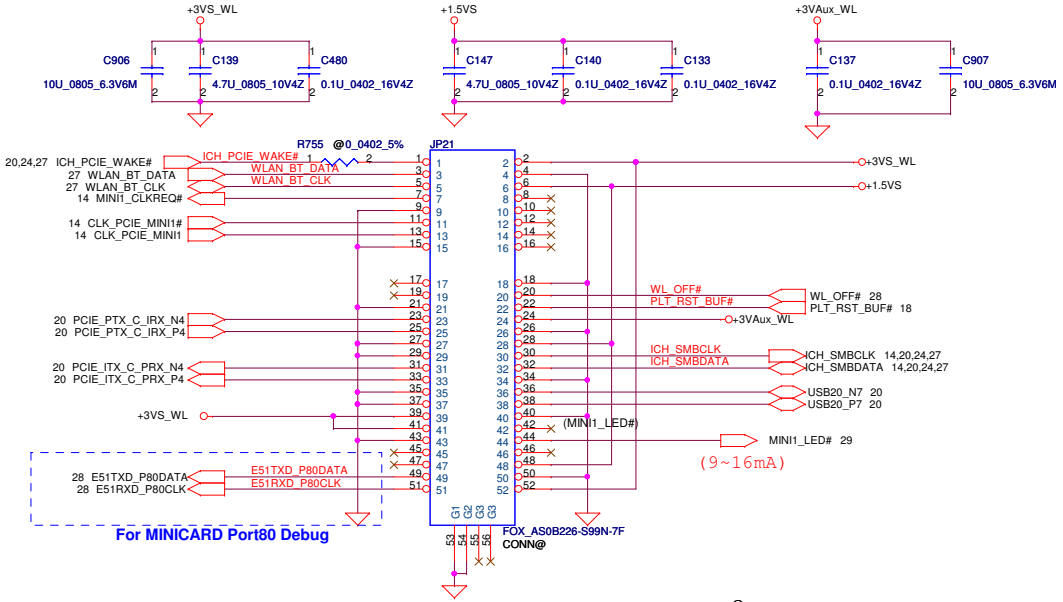
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45/RJ11

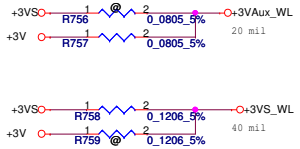
Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 Sheet 25 of 44

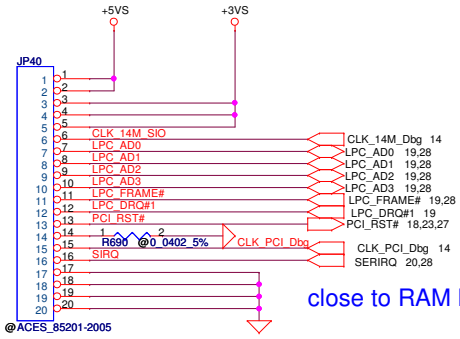
For Wireless LAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

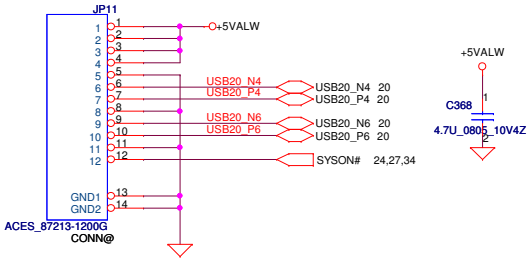


LPC Debug Port



close to RAM Door

To USB/B Connector



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

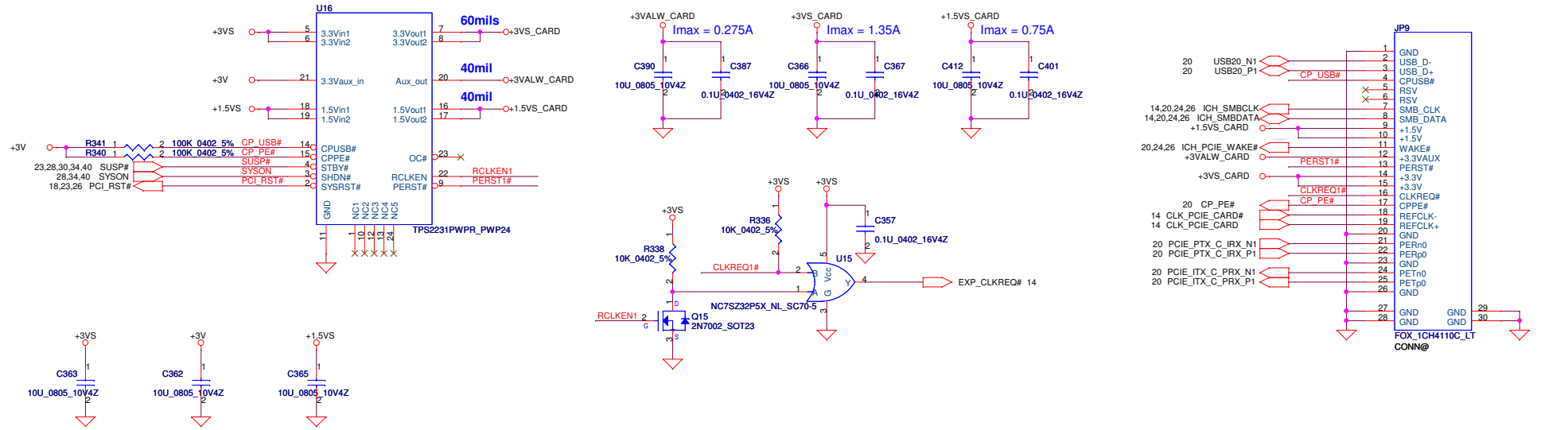
Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size: B | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

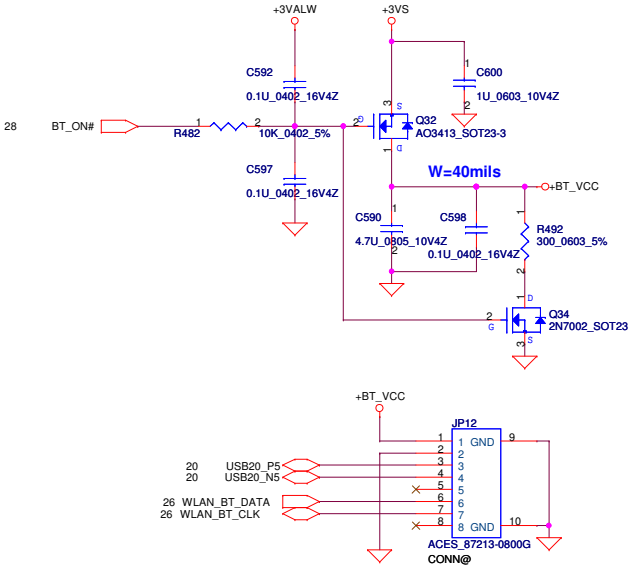
Date: Monday, April 16, 2007 | Sheet 26 of 44

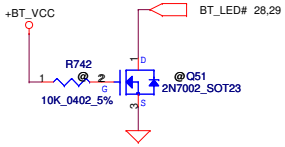
New Card Power Switch



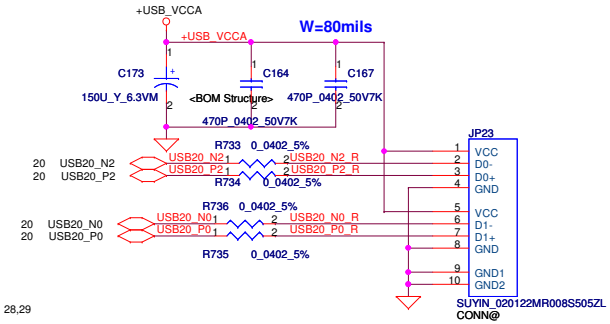
New Card Socket (Left/TOP)

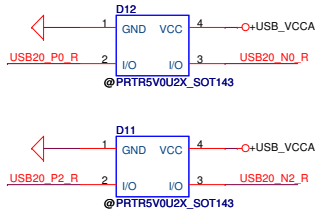
Bluetooth Conn.

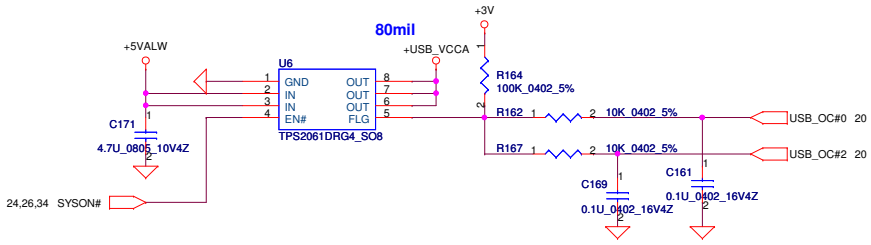




USB CONN. (Stack-up Type)







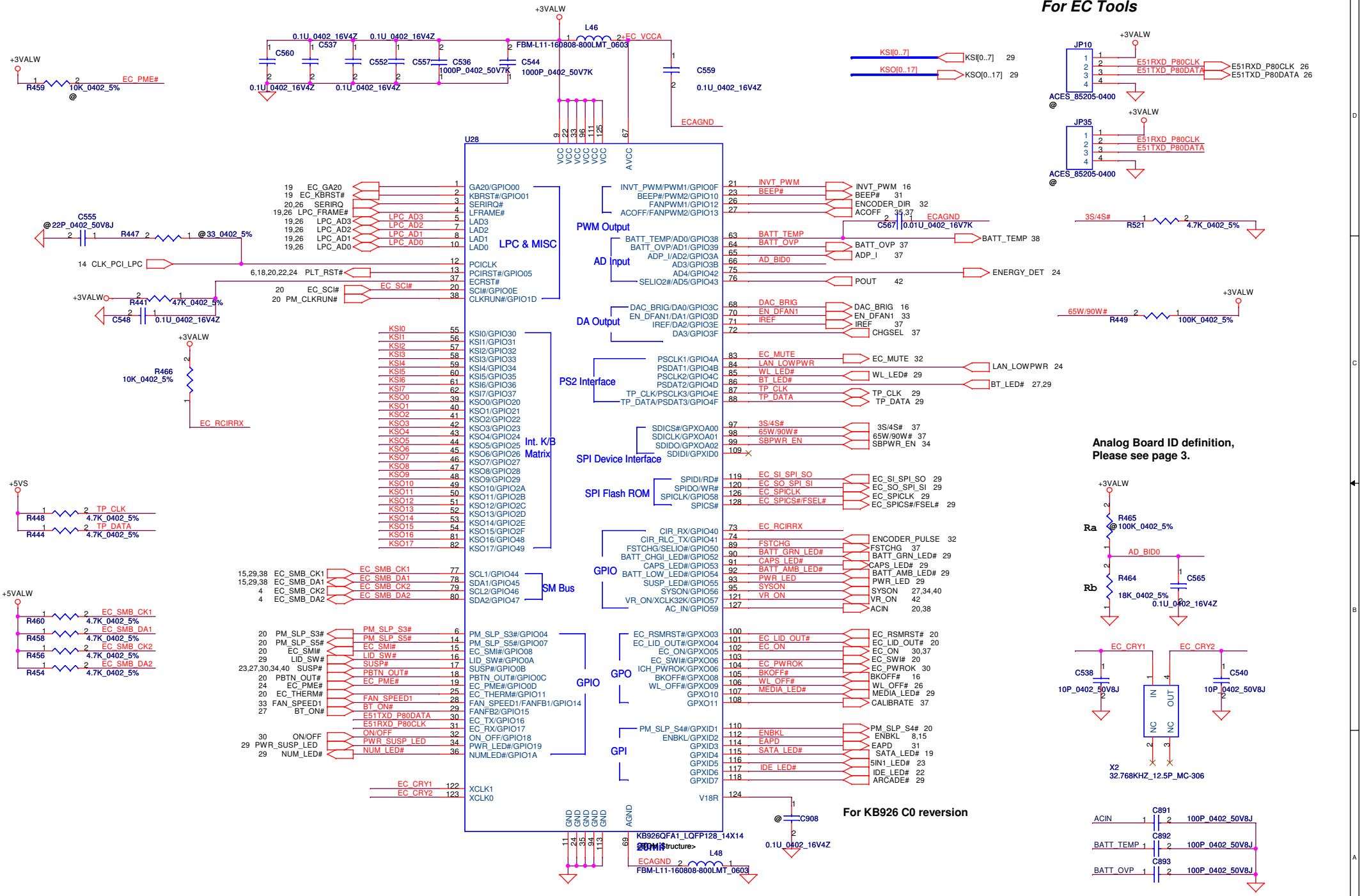
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

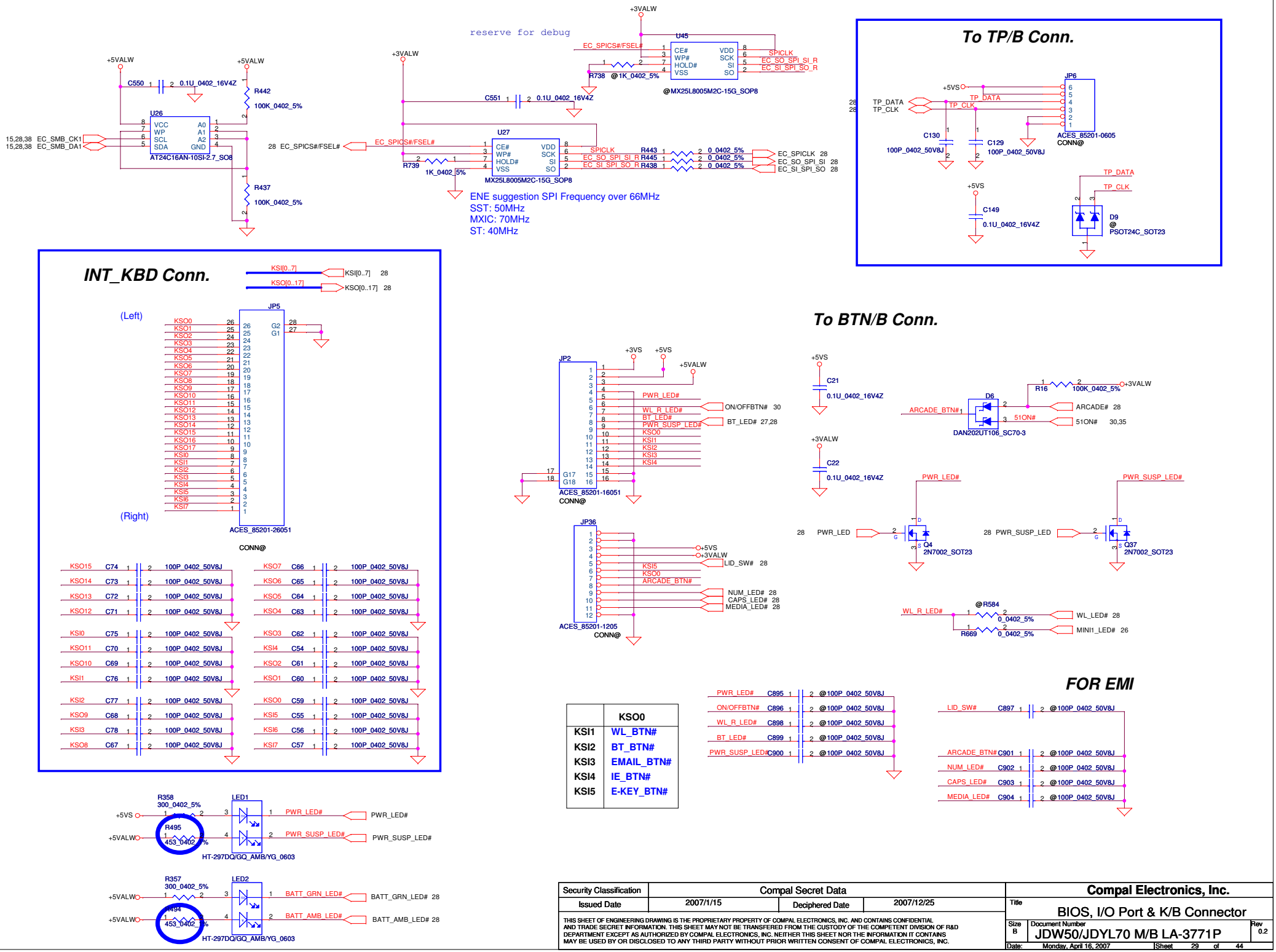
Compal Electronics, Inc.

Title: NEW CARD & USB Connector

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 Sheet 27 of 44


For EC Tools
U28
KB926QFA1_LQFP128_14X14
Int. K/B Matrix
PS2 Interface
SPI Device Interface
SPI Flash ROM
PWM Output
AD Input
DA Output
LPC & MISC
SM Bus
GPIO
GPO
GPI
Analog Board ID definition, Please see page 3.
For KB926 C0 reversion
Compal Electronics, Inc.
EC ENE KB926
JDW50/JDYL70 M/B LA-3771P
Compal Secret Data
2007/1/15
2007/12/25
Monday, April 16, 2007
Sheet 28 of 44



Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

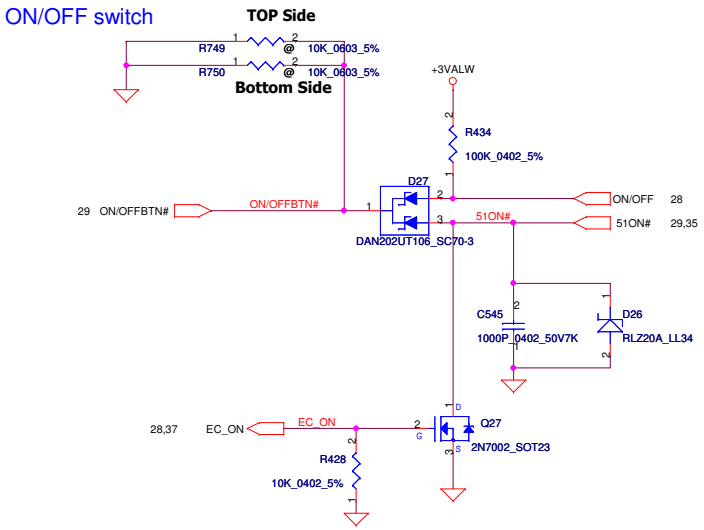
Compal Electronics, Inc.

Title: BIOS, I/O Port & K/B Connector

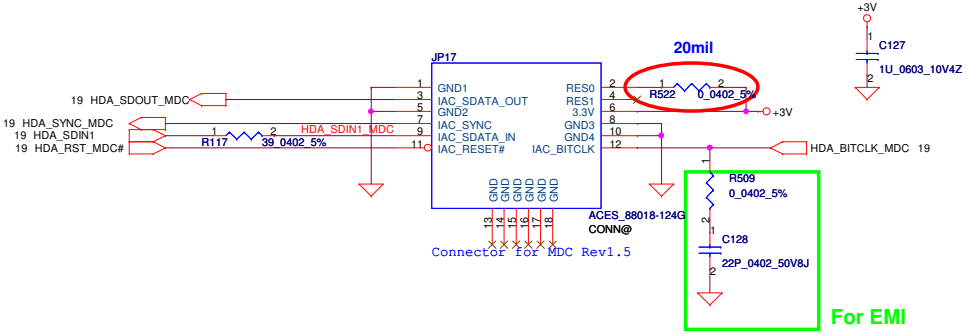
Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 | Sheet 29 of 44

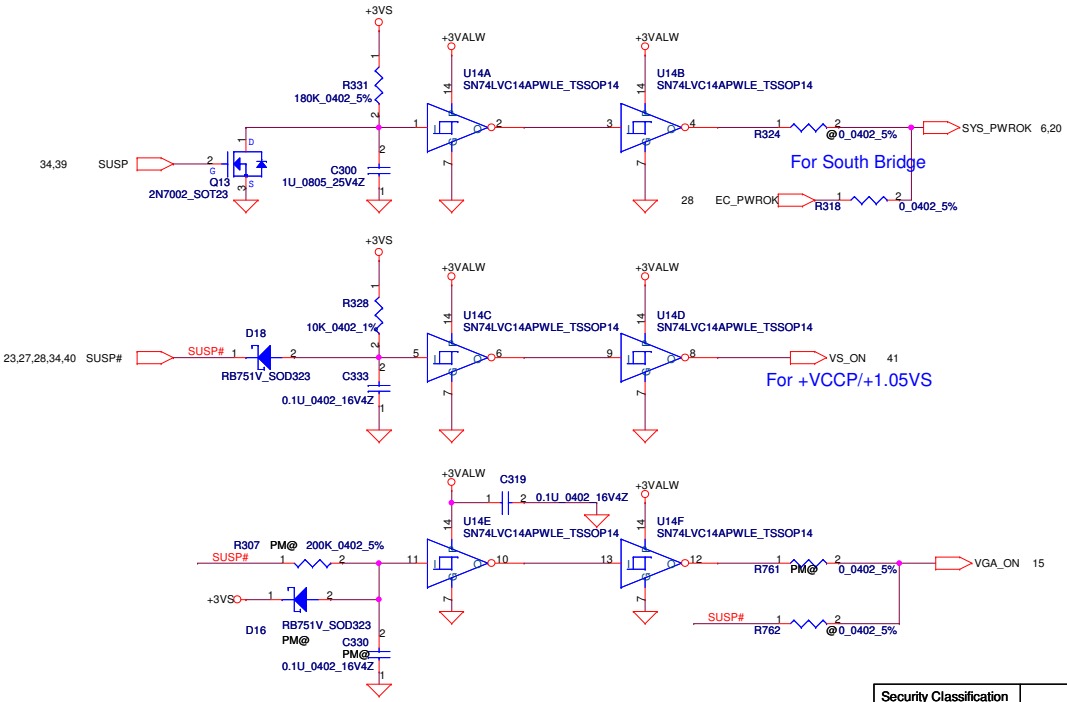
Power Button

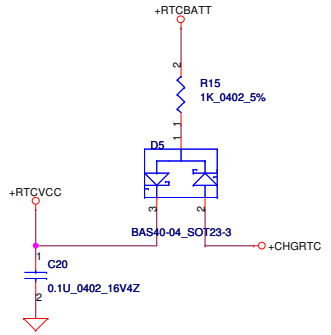


HDA MDC Conn.



Power ON Circuit





Change BATT1 P/N : SP093PA0200 (Panasonic)
SP093MX0000 (MAXELL)

Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: Power OK, Reset and RTC Circuit, TP

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

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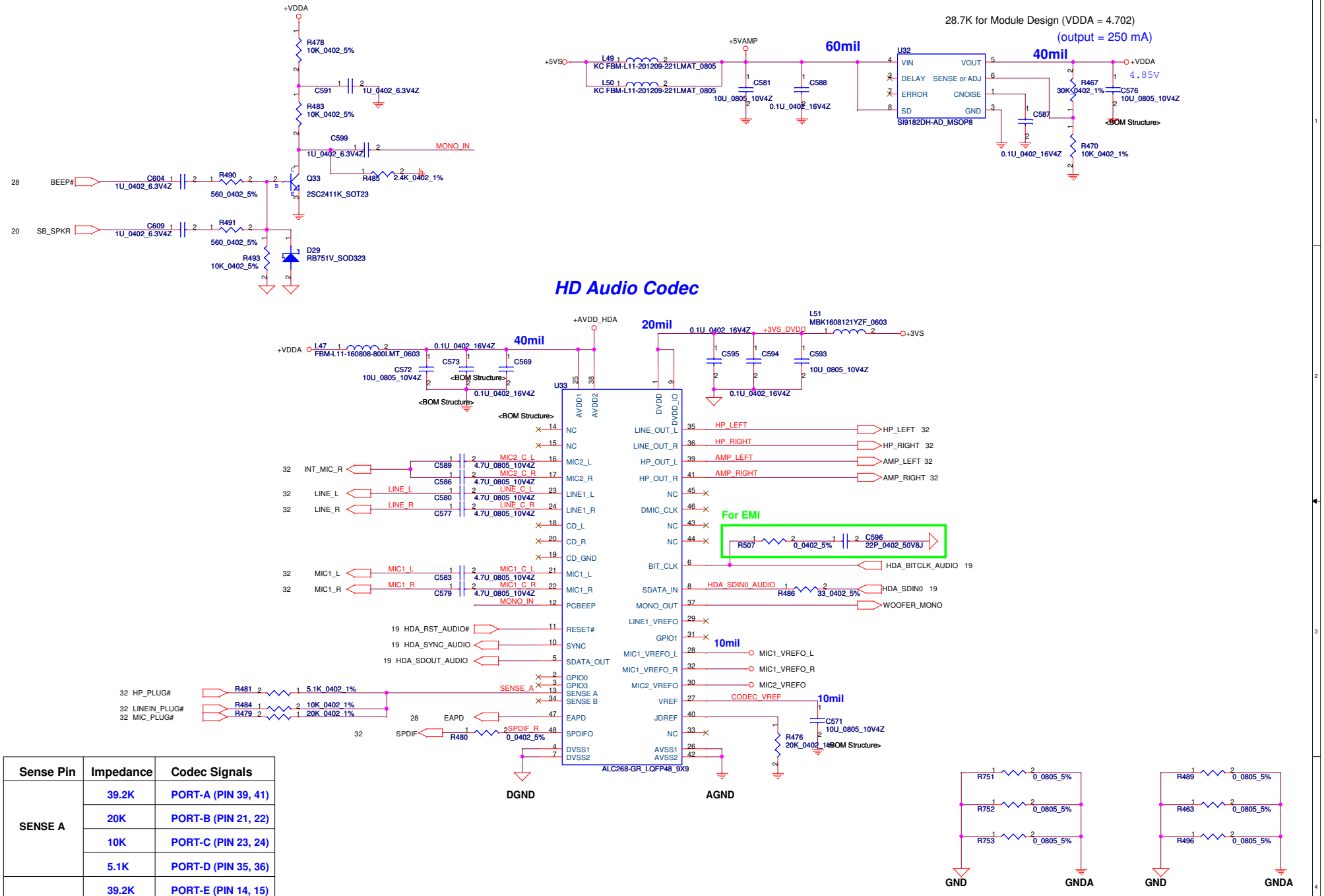


Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

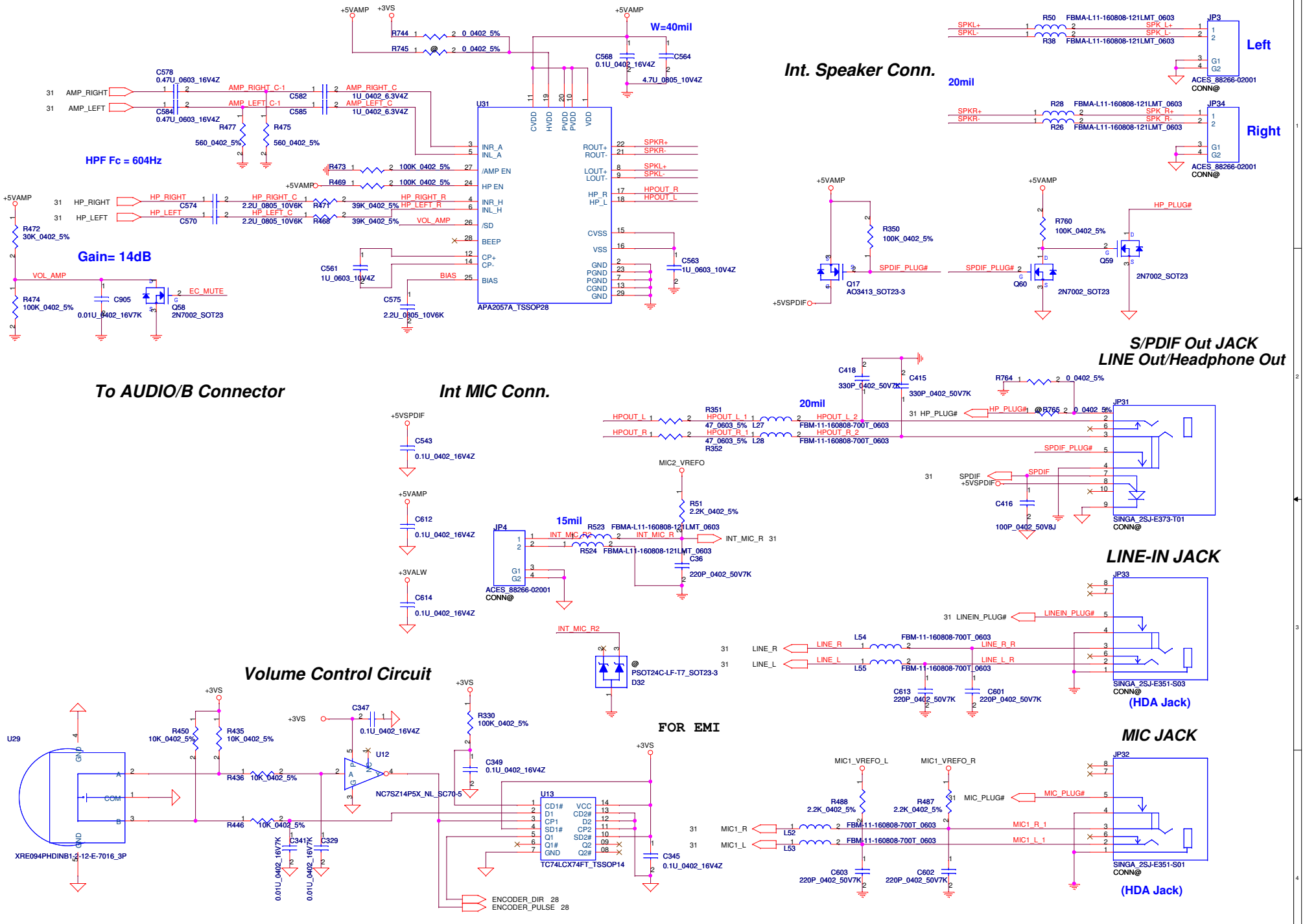
Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: HD Audio Codec ALC268

Size: B | Document Number: JDW50/JDYL70 M/B LA-3771P | Rev: 0.2

Date: Monday, April 16, 2007 | Sheet 31 of 44



Security Classification	Compal Secret Data		
Issued Date	2006/12/25	Deciphered Date	2007/12/25

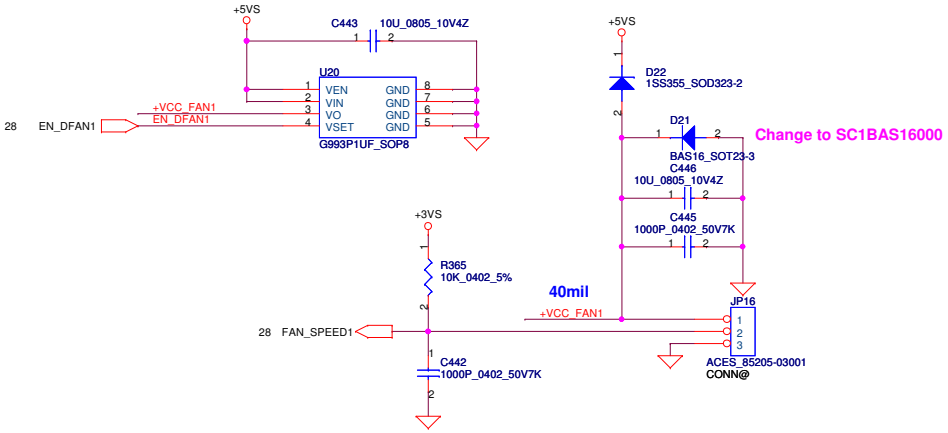
Compal Electronics, Inc.

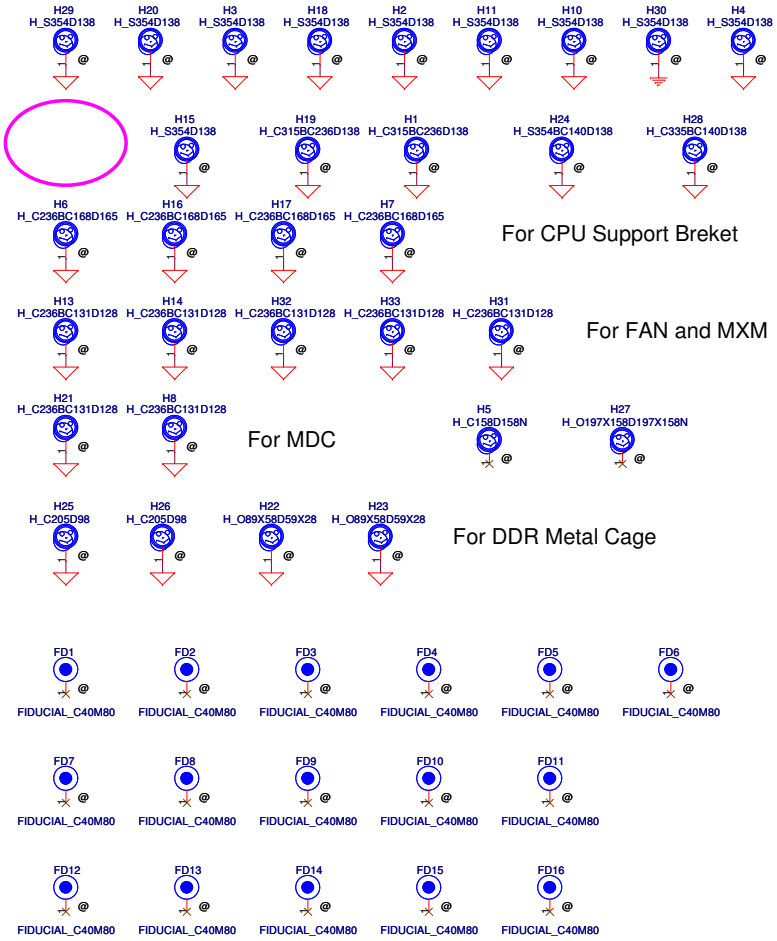
Title: Amplifier & Audio Jack

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 | Sheet 32 of 44

FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

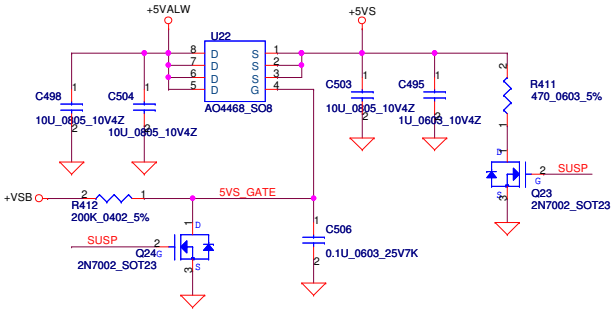
Compal Electronics, Inc.

Title: FAN & Screw Hole

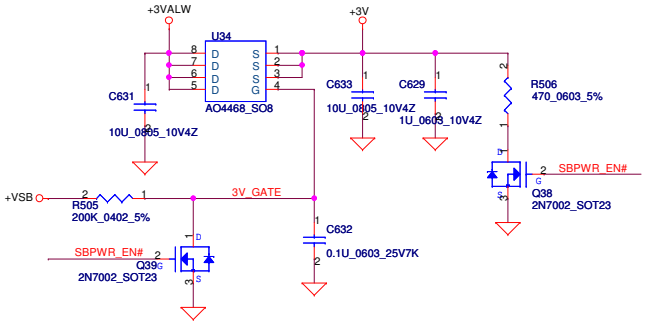
Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

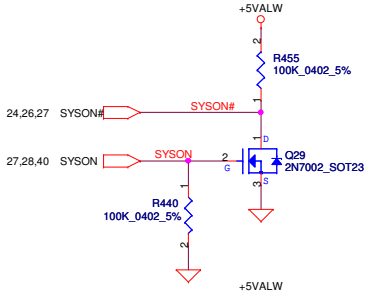
Date: Monday, April 16, 2007 | Sheet 33 of 44

+5VALW TO +5VS

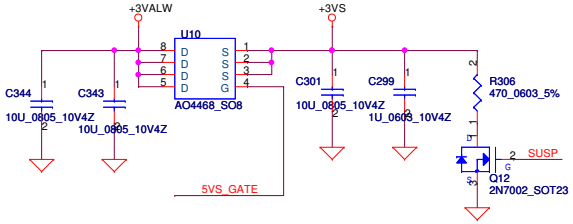


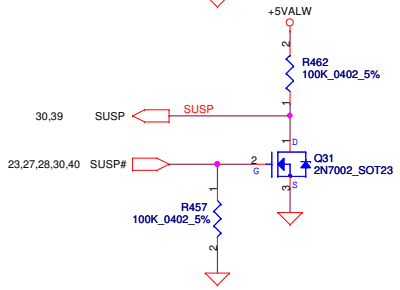
+3VALW TO +3V_SB(ICH8M AUX Power)



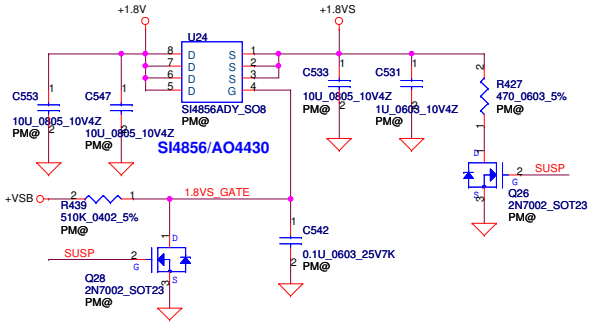


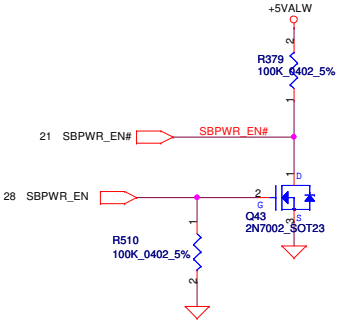
+3VALW TO +3VS

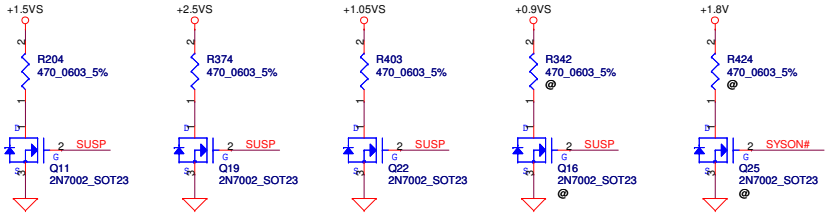




+1.8V to +1.8VS







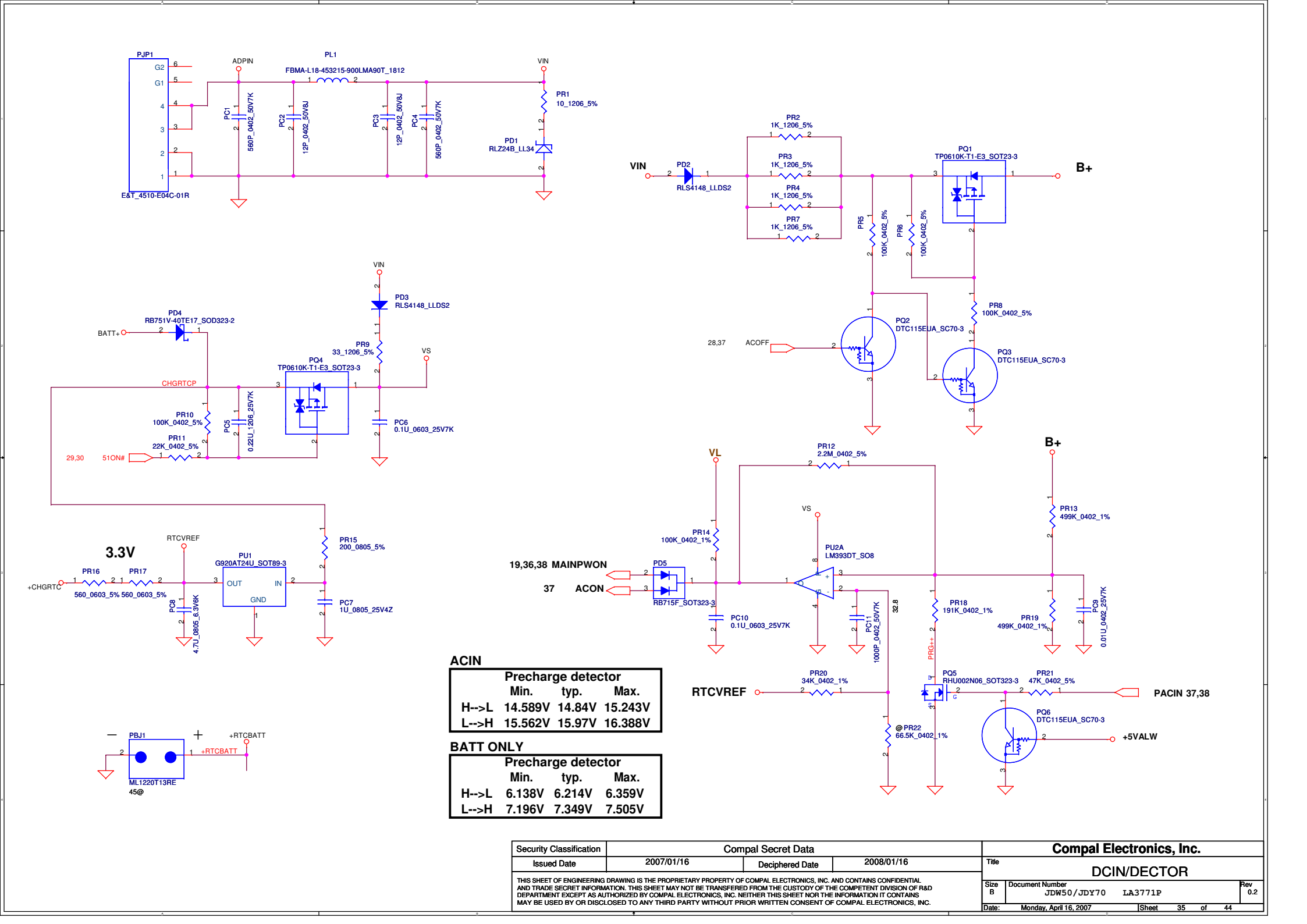
Security Classification	Compal Secret Data		
Issued Date	2007/1/15	Deciphered Date	2007/12/25

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
B	JDW50/JDYL70 M/B LA-3771P	0.2

Date: Monday, April 16, 2007 | Sheet 34 of 44



ACIN

Precharge detector	Min.	typ.	Max.
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max.
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

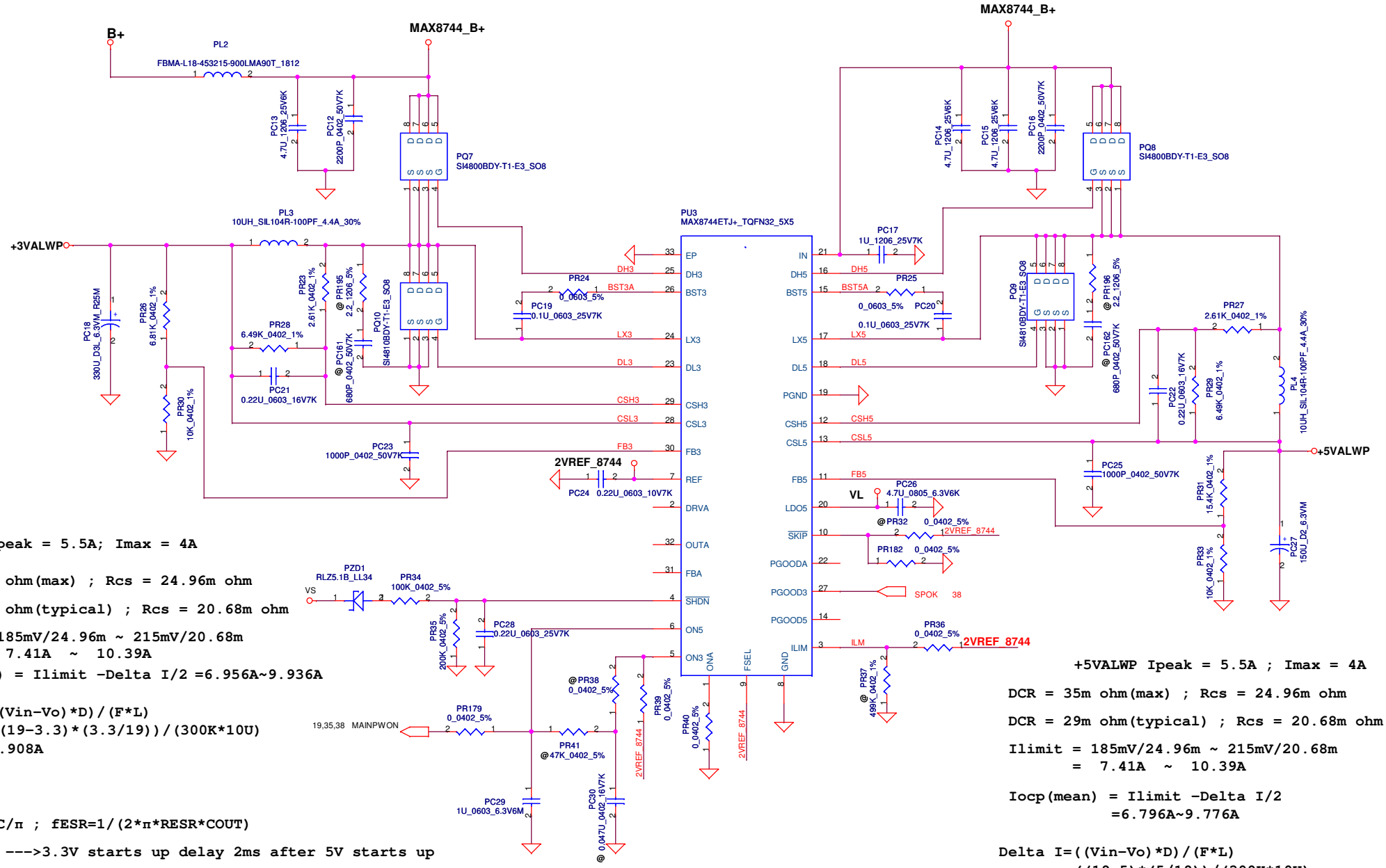
Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

Compal Electronics, Inc.

Title: DCIN/DECTOR

Size	Document Number	Rev
B	JDW50/JDY70 LA3771P	0.2

Date: Monday, April 16, 2007 | Sheet 35 of 44



+3VALWP Ipeak = 5.5A; Imax = 4A

DCR = 35m ohm(max) ; Rcs = 24.96m ohm

DCR = 29m ohm(typical) ; Rcs = 20.68m ohm

Ilimit = 185mV/24.96m ~ 215mV/20.68m
= 7.41A ~ 10.39A

Iocp(mean) = Ilimit -Delta I/2 =6.956A~9.936A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-3.3)*(3.3/19))/(300K*10U)
=0.908A

Notes :

fESR<=fOSC/π ; fESR=1/(2*π*RESR*COUT)

ON3 = REF --->3.3V starts up delay 2ms after 5V starts up

+5VALWP Ipeak = 5.5A ; Imax = 4A

DCR = 35m ohm(max) ; Rcs = 24.96m ohm

DCR = 29m ohm(typical) ; Rcs = 20.68m ohm

Ilimit = 185mV/24.96m ~ 215mV/20.68m
= 7.41A ~ 10.39A

Iocp(mean) = Ilimit -Delta I/2
=6.796A~9.776A

Delta I=((Vin-Vo)*D)/(F*L)
=((19-5)*(5/19))/(300K*10U)
1.228A

Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size	Document Number	Rev
Custom	JDW50/JDY70 LA3771P	0.1

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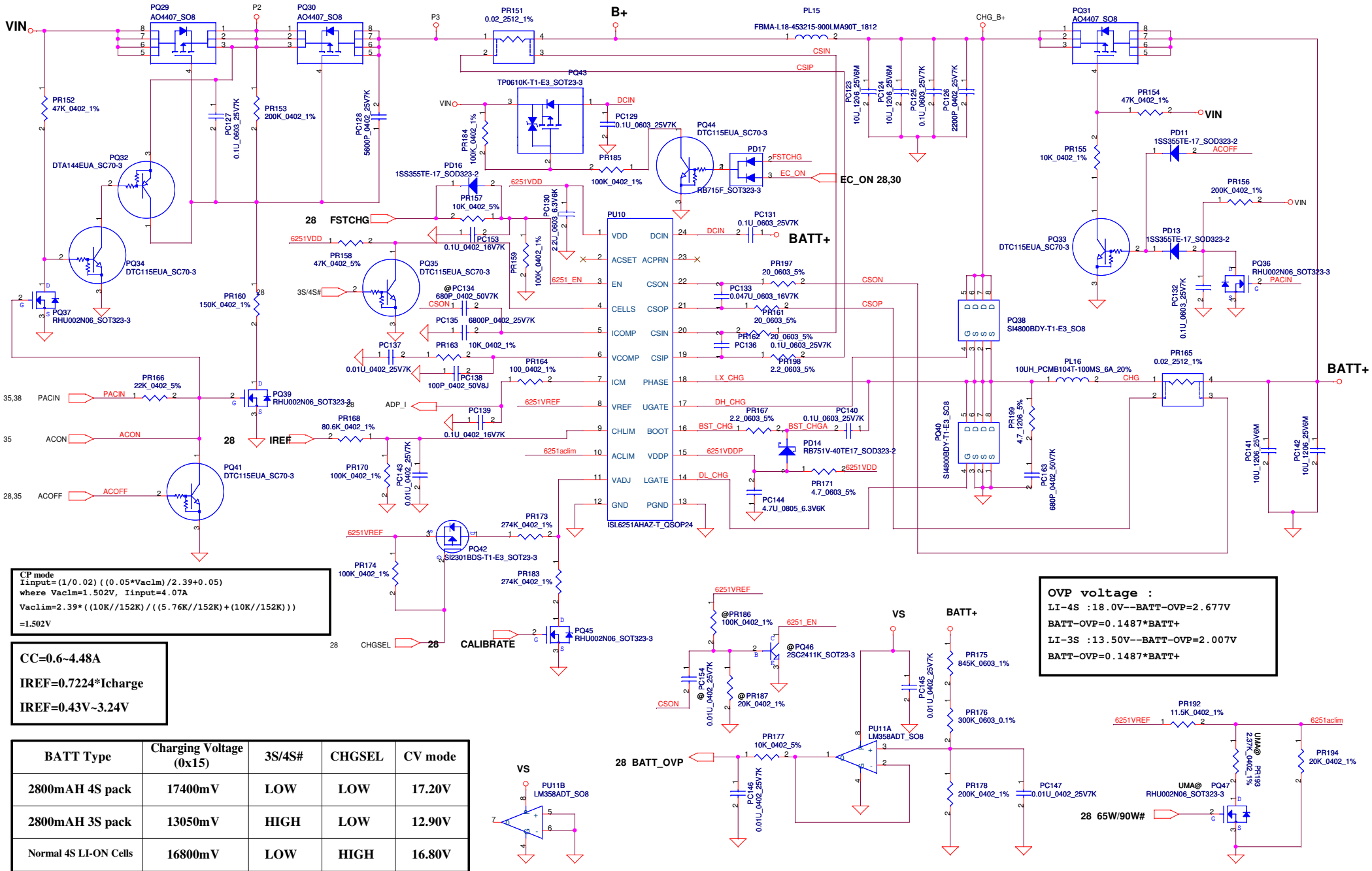
Iada=0~4.74A(90W)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode

Iinput=(1/0.02)((0.05*Vaclm)/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

Vaclim=2.39*((10K//152K)/((5.76K//152K)+(10K//152K)))

=1.502V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

OVP voltage :

LI-4S :18.0V--BATT-OVP=2.677V

BATT-OVP=0.1487*BATT+

LI-3S :13.50V--BATT-OVP=2.007V

BATT-OVP=0.1487*BATT+

BATT Type	Charging Voltage (0x15)	3S/4S#	CHGSEL	CV mode
2800mAH 4S pack	17400mV	LOW	LOW	17.20V
2800mAH 3S pack	13050mV	HIGH	LOW	12.90V
Normal 4S LI-ON Cells	16800mV	LOW	HIGH	16.80V
Normal 3S LI-ON Cells	12600mV	HIGH	HIGH	12.60V
Wake up charge while no communication	-	HIGH	HIGH	12.60V

Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

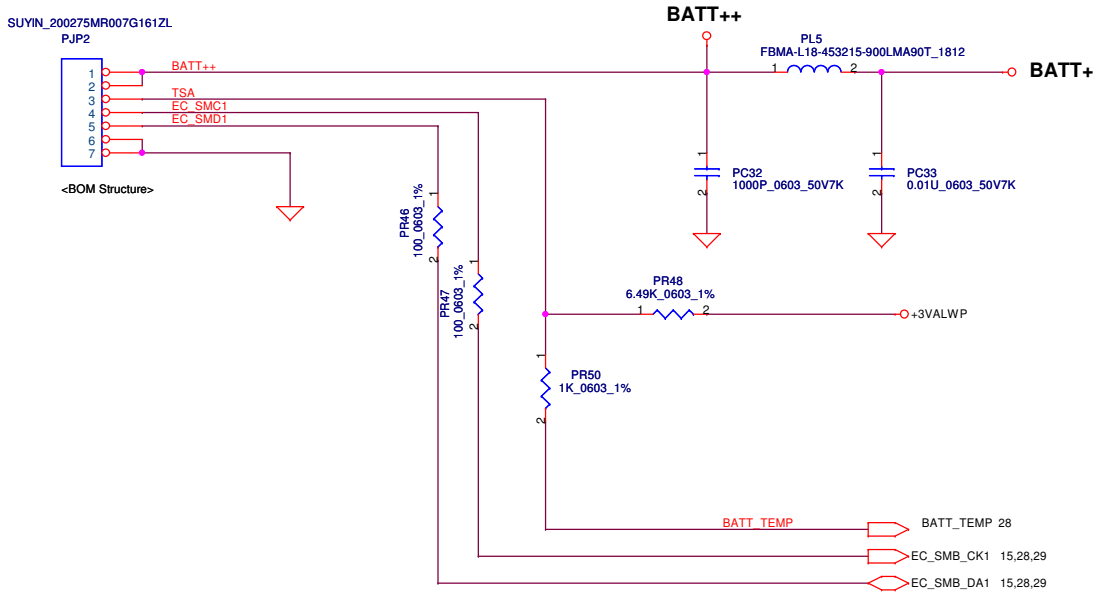
Compal Electronics, Inc.

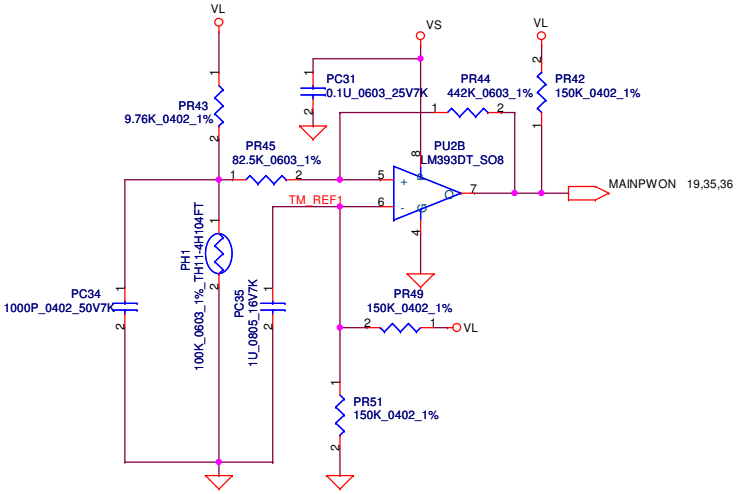
Title: CHARGER

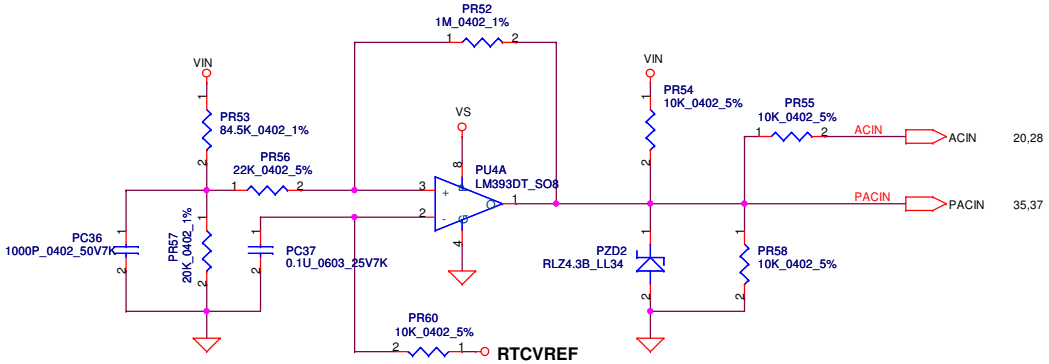
Size: | Document Number: JDW50/JDY70 LA3771P | Rev: 1.0

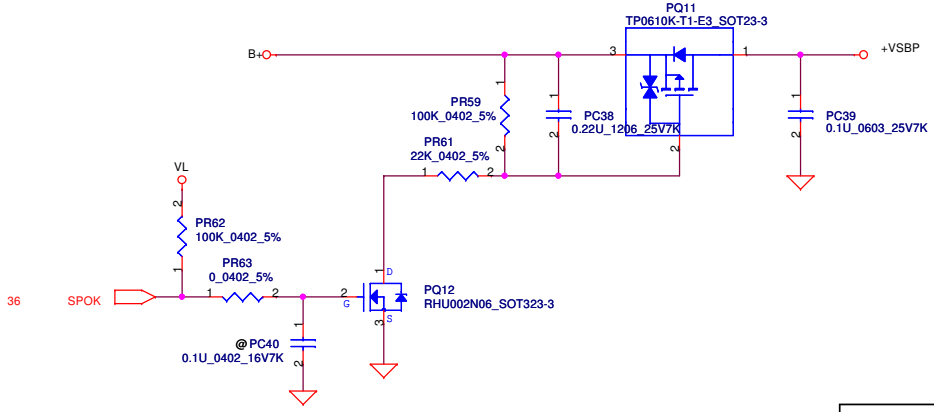
Date: Monday, April 16, 2007 | Sheet 37 of 44

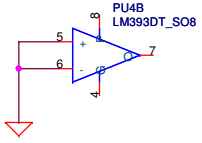
PH1 under CPU botten side :
CPU thermal protection at 90 degree C
Recovery at 70 degree C











Vin Detector

	Min.	typ.	Max.
H-->L	16.976V	17.257V	17.728V
L-->H	17.430V	17.901V	18.384V

Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

Compal Electronics, Inc.

Title: BATTERY CONN. / OTP

Size	Document Number	Rev
B	JDW50/JDY70 LA3771P	0.2

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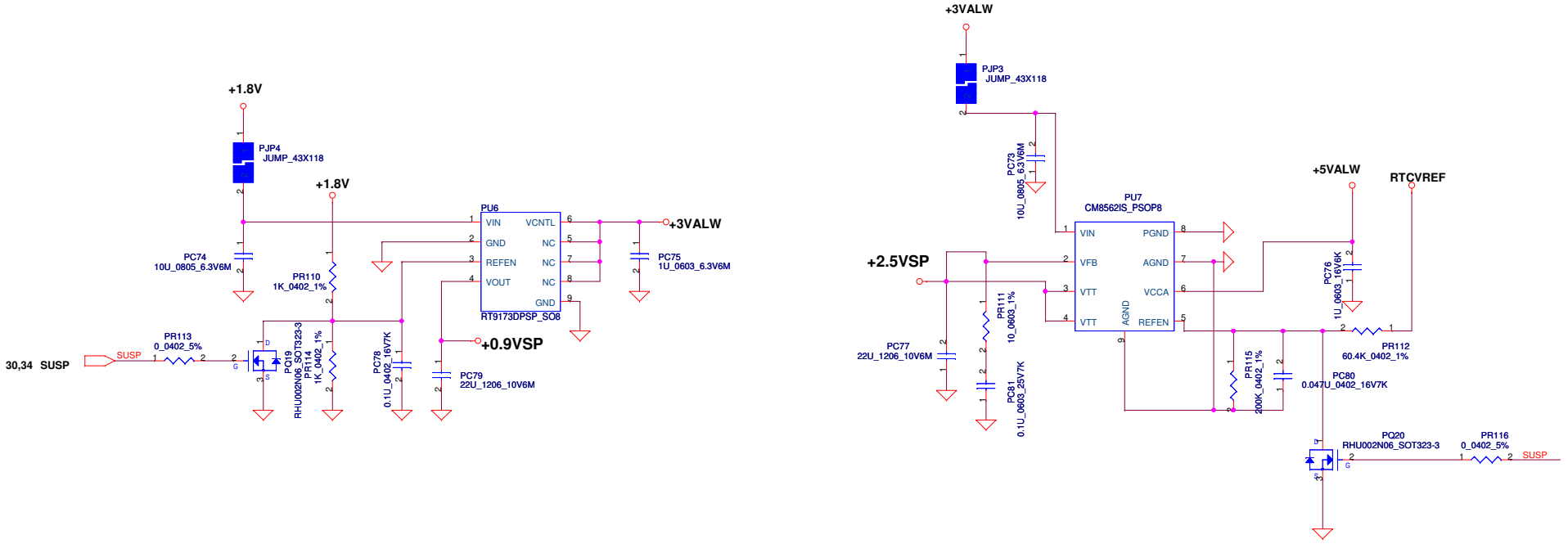

Compal Electronics, Inc.

Title: +0.9VSP/+2.5VSP

Size	Document Number	Rev
Custom	JDW50/JDY70 LA3771P	0.1

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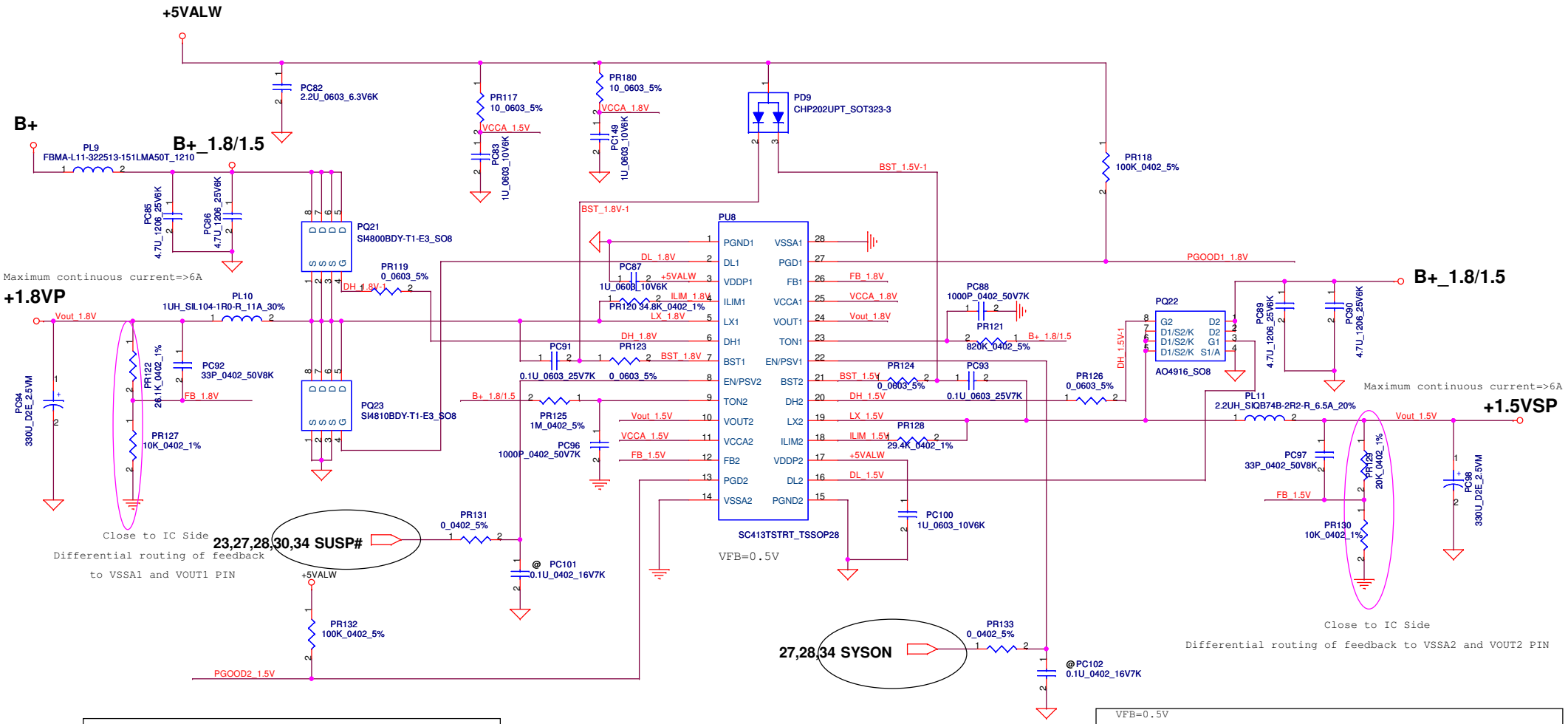

VFB=0.5V
Vo=VFB*(1+PR122/PR127)=1.805V
Ipeak=12.17A, Imax=8.519A
Ton=(3.3E-12*(PR121+37K)*(Vout/VBat))+50ns
=3.3*10e-12*(820K+37K)*(1.8/19)+50ns=0.3179us
FDS6670AS:Rds(on)=>Typ:9 mOhm
Max:11.5 mOhm
Iocp=Ivalley+ Iripple /2
Iripple=(vin-vout)*(Ton/L)=5.467A, 1/2 Iripple=2.734A.
Ivalleymin=10E-6*(PR120/Rds(ON)max*1.5)
=9*10e-6*(27.4K/0.0115*1.5)=14.295A>11.73*1.2=14.076A
Ivalleymax=10E-6*(PR120/Rds(ON)typ*1.2)
=11*10e-6*(27.4K/0.009*1.2)=27.907A.
OCP==>17.029A~30.641A

VFB=0.5V
Vo=VFB*(1+PR129/PR130)=1.5V
Ipeak=5.16A, Imax=3.612A
Ton=(3.3E-12*(PR125+37K)*(Vout/VBat))+50ns
=0.3201us
AO4916 Rds(on)=>Typ:21 mOhm
Max:27 mOhm
Ivalleymin=9*10u*(29.4K/0.027*1.4)=7A
Ivalleymax=11*E-6*(29.4K/0.021*1.1)=12.833A
Iripple=(vin-vout)*(Ton/L)=2.546A, 1/2Iriiple=1.273A
Iocp=Ivalley+ Iripple /2
OCP==>8.273A~14.106A

Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

Compal Electronics, Inc.

Title: +1.5VSP/+1.8VP

Size	Document Number	Rev
Custom	JDW50/JDY70 LA3771P	0.1

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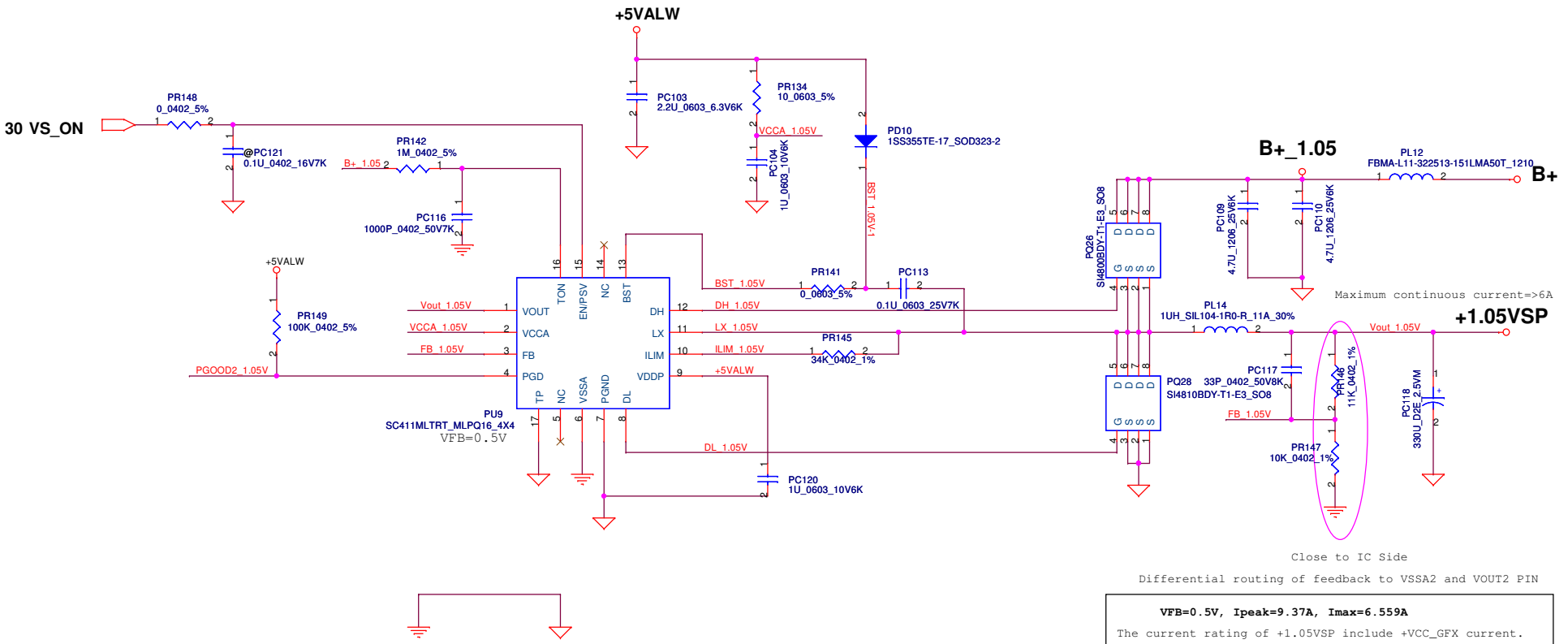
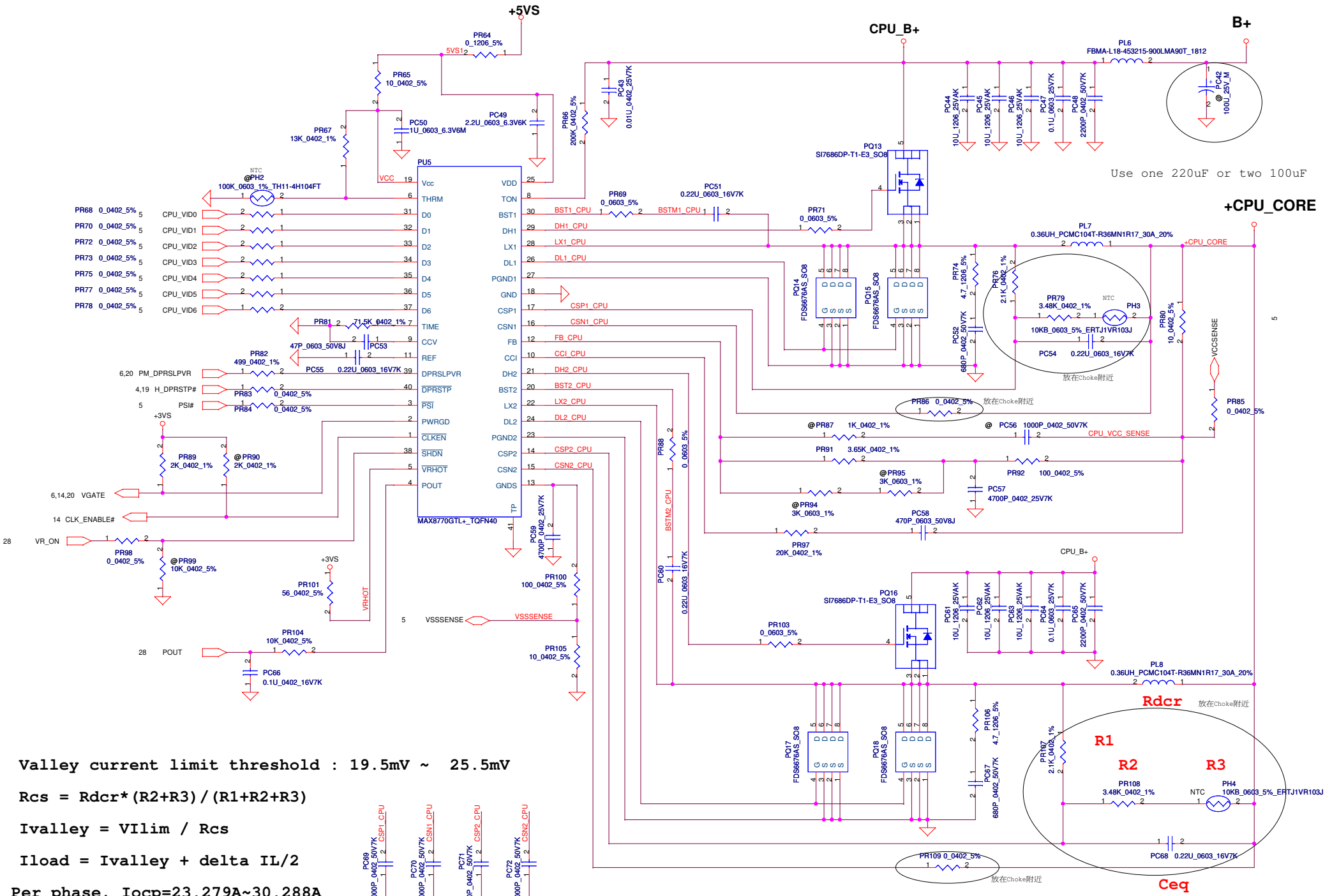


Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

Compal Electronics, Inc.

Title	+1.05VSP		
Size: Custom	Document Number: JDW50/JDY70 LA3771P		Rev: 0.1
Date: Monday, April 16, 2007	Sheet 41 of 44		



Security Classification	Compal Secret Data		
Issued Date	2007/01/16	Deciphered Date	2008/01/16

Compal Electronics, Inc.			
Title	+CPU_CORE		
Size: Custom	Document Number: JDW50/JDY70 LA3771P		Rev: 0.2
Date: Monday, April 16, 2007	Sheet 42 of 44		

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	EC GPIO pin modify	EC GPIO pin modify	0.1 ==> 0.2	8	DPST_PWM net modify	3/19	
2	clk frequency error	pin error	0.1 ==> 0.2	14	Q48,Q49,Q50 pin error		
3	EC add a GPIO pin	EC GPIO pin modify	0.1 ==> 0.2	16	del DPST_PWM net from North Bridge		
4	follow ICL50	follow ICL50	0.1 ==> 0.2	20	CRT_DET# net modify		
5	EMI request	EMI request	0.1 ==> 0.2	24	Add R477, R748		
6	ESD request	ESD request	0.1 ==> 0.2	25	reserve D30,D31		
7	test	test	0.1 ==> 0.2	26	reserve MINI1_LED#		
8	Blue LED issue	Blue LED issue	0.1 ==> 0.2	27	BT_LED# schematic modify		
9	EC GPIO pin modify	EC GPIO pin modify	0.1 ==> 0.2	28	EC GPIO pin define modify		
10	ESD request	ESD request	0.1 ==> 0.2	29	reserve C895 to C904		
11	easy short	easy short	0.1 ==> 0.2	30	change J1,J2 jumper sybmol to 0603 symbol		
12	ESD request	ESD request	0.1 ==> 0.2	31	Add R751,R752,R753		
13	chip issue	chip issue	0.1 ==> 0.2	32	U31 chip update version		
14	voice too small	modify gain value	0.1 ==> 0.2	32	change R472 form 39k to 30k ohm		
15	EMI request	EMI request	0.1 ==> 0.2	32	change R523,R524,R50,R38,R26,R28 for 0 ohm to bead		
16	DFX request	DFX request	0.1 ==> 0.2	33	del pjp15		
17	Wireless Lan S4 fail	Wireless Lan fail	0.2 ==> 0.3	26	del R756, add R757		
18	Wireless Lan S4 fail	Wireless Lan fail	0.2 ==> 0.3	26	change C906,C907 from 22u_1206 to 10u_0805		
19	Lead Free	non LF==>Lead Free	0.2 ==> 0.3	17	change C211,C510,C514,C216,C508,C515		
20	KBC version update	KBC version update	0.2 ==> 0.3	28	reserve 0.1u at pin 124		
21	SPDIF udpate	SPDIF circuit udpate	0.2 ==> 0.3	32	add q59,q60		
22	DFX	DFX issue	0.2 ==> 0.3	32	del JP13		
23							
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Compal Electronics, Inc.			
Title: PIR (HW)			
Size	Document Number: JDW50 LA-3771P		Rev: 0.2
Date: Monday, April 16, 2007		Sheet 43 of 44	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Charger IC damage issue	Charger IC damage issue	0.2	40	Change PR161 from SD013220B80 to SD013200A80		
2	Charger IC damage issue	Charger IC damage issue	0.2	40	Change PR162 from SD013180A80 to SD013200A80		
3	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PR197 SD013200A80		
4	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PR198 SD013220B80		
5	Charger IC damage issue	Charger IC damage issue	0.2	40	Add PC133 SE026473K80		
6	Add EMI solution in charger.	Add EMI solution in charger.	0.3	40	Add PR199 SD001470B80(S RES 1/4 4.7 1206 5%).	04/01/07	PVT
7	Add EMI solution in charger.	Add EMI solution in charger.	0.3	40	Add PC163 SE074681K80(S CER CAP 680P 50V K X7R 0402)	04/01/07	PVT
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