Compal Confidential

JM40-HR M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
Nvidia N12P-GS/GV-OP

2010-02-22

REV:1.0

ZZZ

Part Number	Description
DAZ0IO00100	

P4LJ0_PCB
PCB P4LJ0 LA-7231P LS-7231P/7233P/7235P/7237P

ZZZ

Part Number	Description
DC30100DT00	DC_IN_CABLE_90W

P4LJ0_DCIN_CABLE_90W
90W@

ZZZ

Part Number	Description
DC30100DS00	DC_IN_CABLE_65W

P4LJ0_DCIN_CABLE_65W
65W@

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

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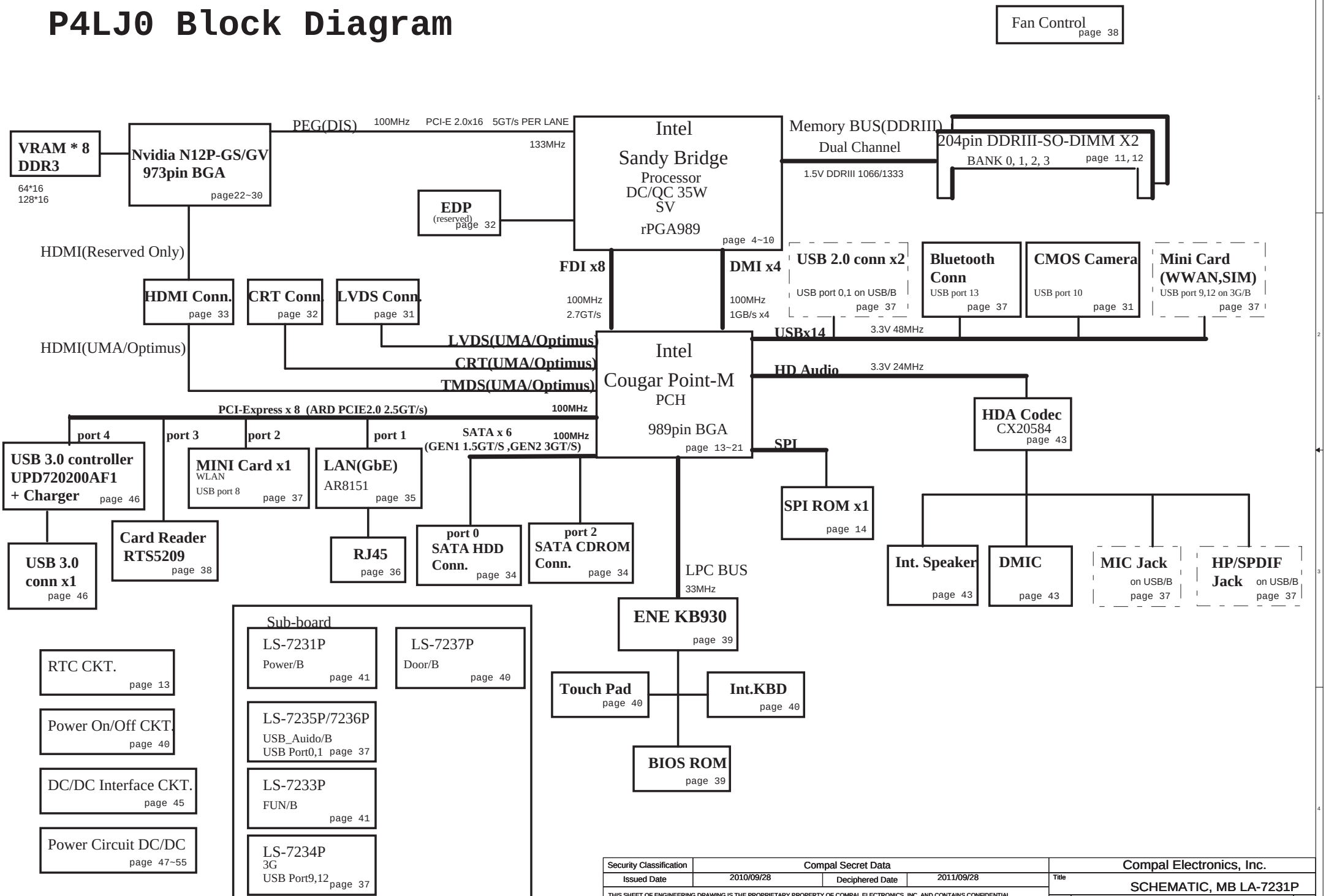
P4LJ0 Block Diagram



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+VGFX_CORE	Core voltage for UMA graphic	ON	OFF	OFF
+0.75VS	+0.75VP to +0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VSDGPU	+1.05VSDGPU power rail for GPU	ON	OFF	OFF
+1.05VS_VCCP	+1.05VS_VCCPP to +1.05VS_VCCP switched power rail for CPU	ON	OFF	OFF
+1.05VS_PCH	+1.05VS_VCCP to +1.05VS_PCH power for PCH	ON	OFF	OFF
+1.5V	+1.5VP to +1.5V power rail for DDRIII	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.5VSDGPU	+1.5VS to +1.5VSDGPU switched power rail for GPU	ON	OFF	OFF
+1.8VS	(+5VALW or +3VALW) to 1.8V switched power rail to PCH & GPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VALW_EC	+3VALW always to KBC	ON	ON	ON*
+3V_LAN	+3VALW to +3V_LAN power rail for LAN	ON	ON	ON*
+3VALW_PCH	+3VALW to +3VALW_PCH power rail for PCH (Short Jumper)	ON	ON	ON*
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VALW_PCH	+5VALW to +5VALW_PCH power rail for PCH (Short resister)	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

PCH SM Bus address

Device	Address
Clock Generator (9LVS3199AKLFT, RTM890N-631-VB-GRT)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID/ Project ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA Only	UMAO@
N12P-GS	GS@
N12P-GV	GV@
Discrete(OPTIMUS)	OPT@
VRAM	X76@
Blue Tooth	BT@
AR8151	8151@
Connector	CONN@
Unpop	@

Project ID Table

Project ID	Project Name
0	P3LJ0
1	P4LJ0
2	P5LJ0
3	P3LS0
4	P4LS0
5	P5LS0
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/B (Right Side)
		1	USB/B (Right Side)
	UHCI1	2	
		3	
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Mini Card(WLAN)
		9	Mini Card(WWAN)
	UHCI5	10	Camera
		11	
	UHCI6	12	SIM Card
		13	Blue Tooth

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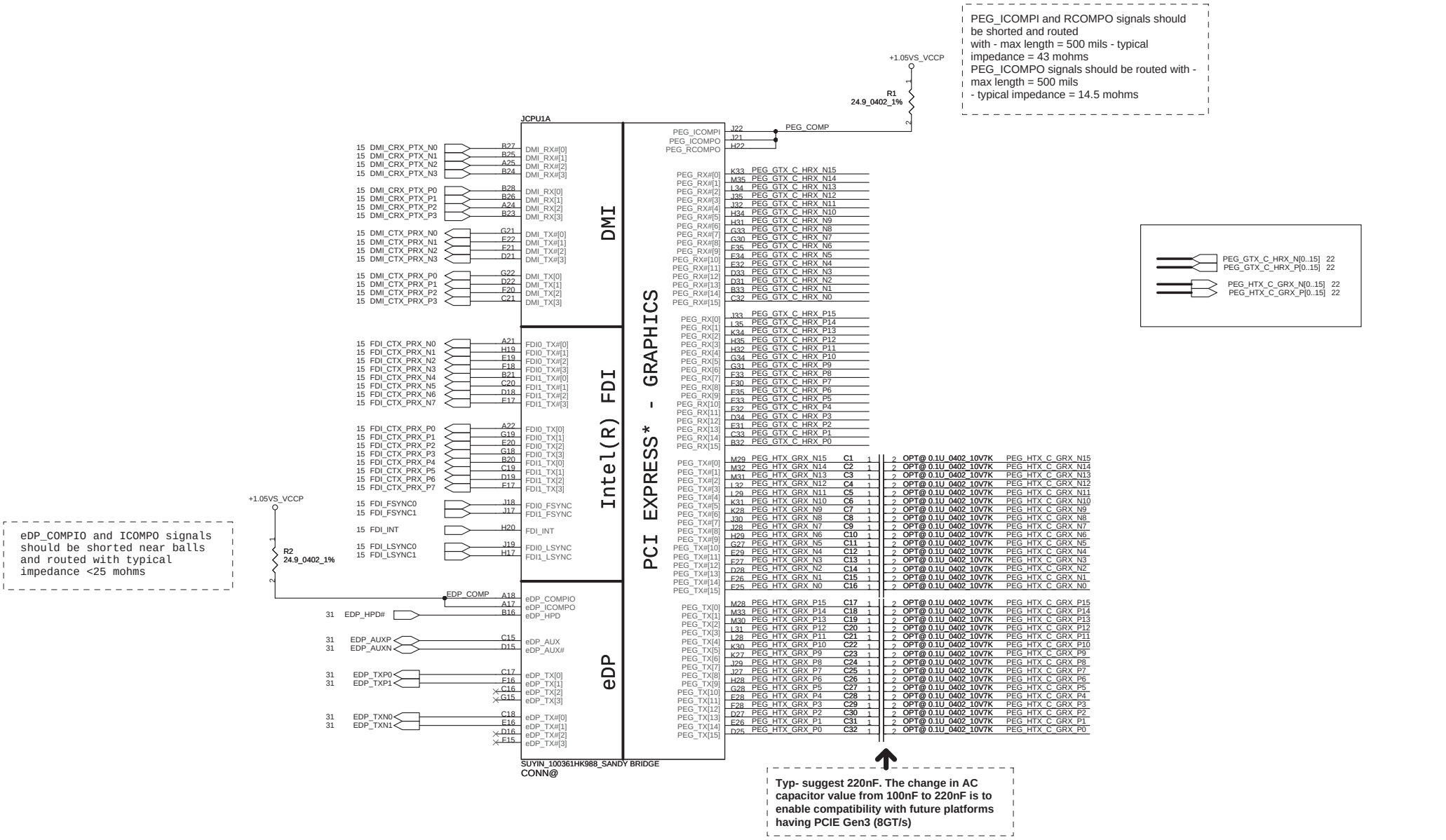

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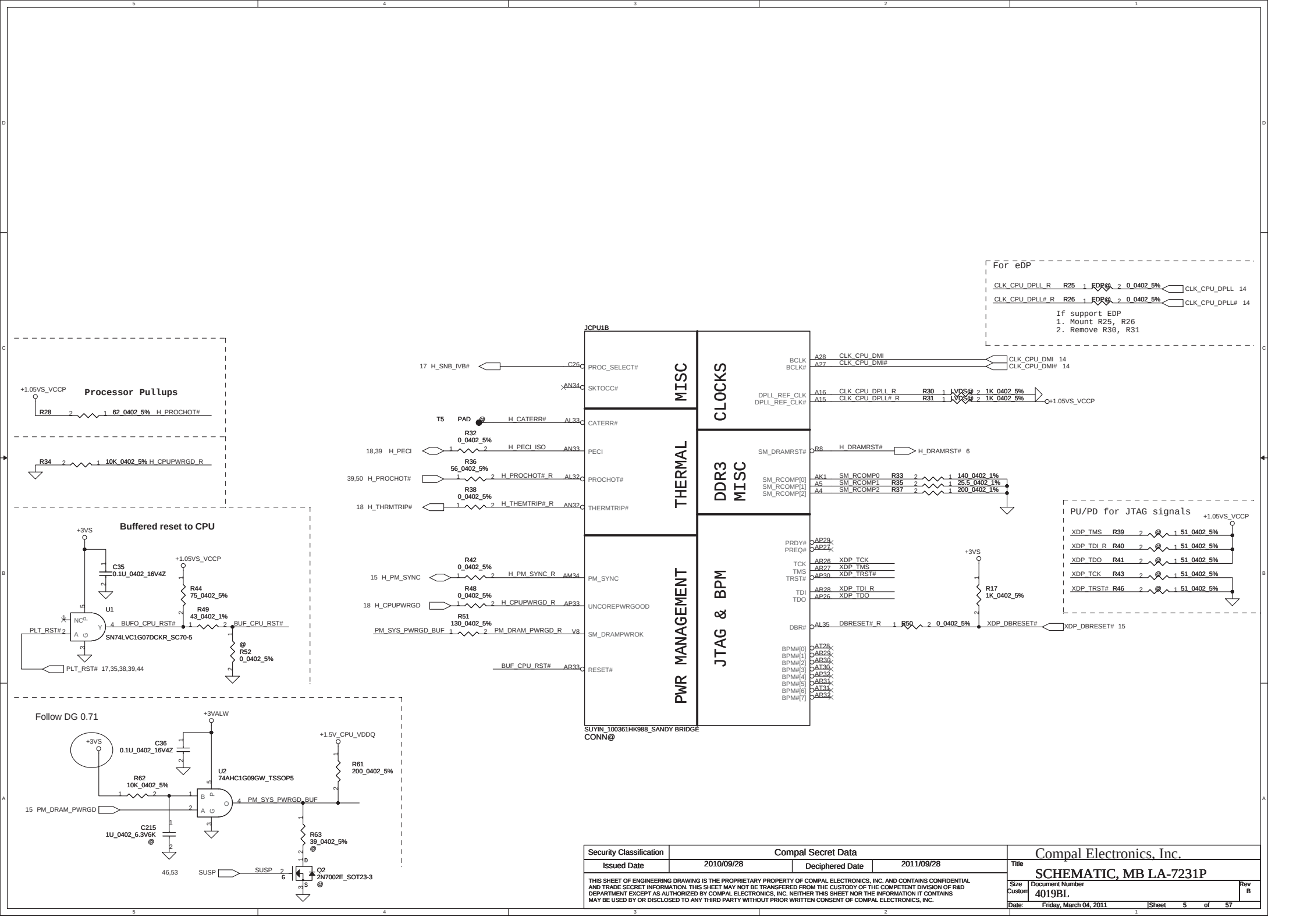

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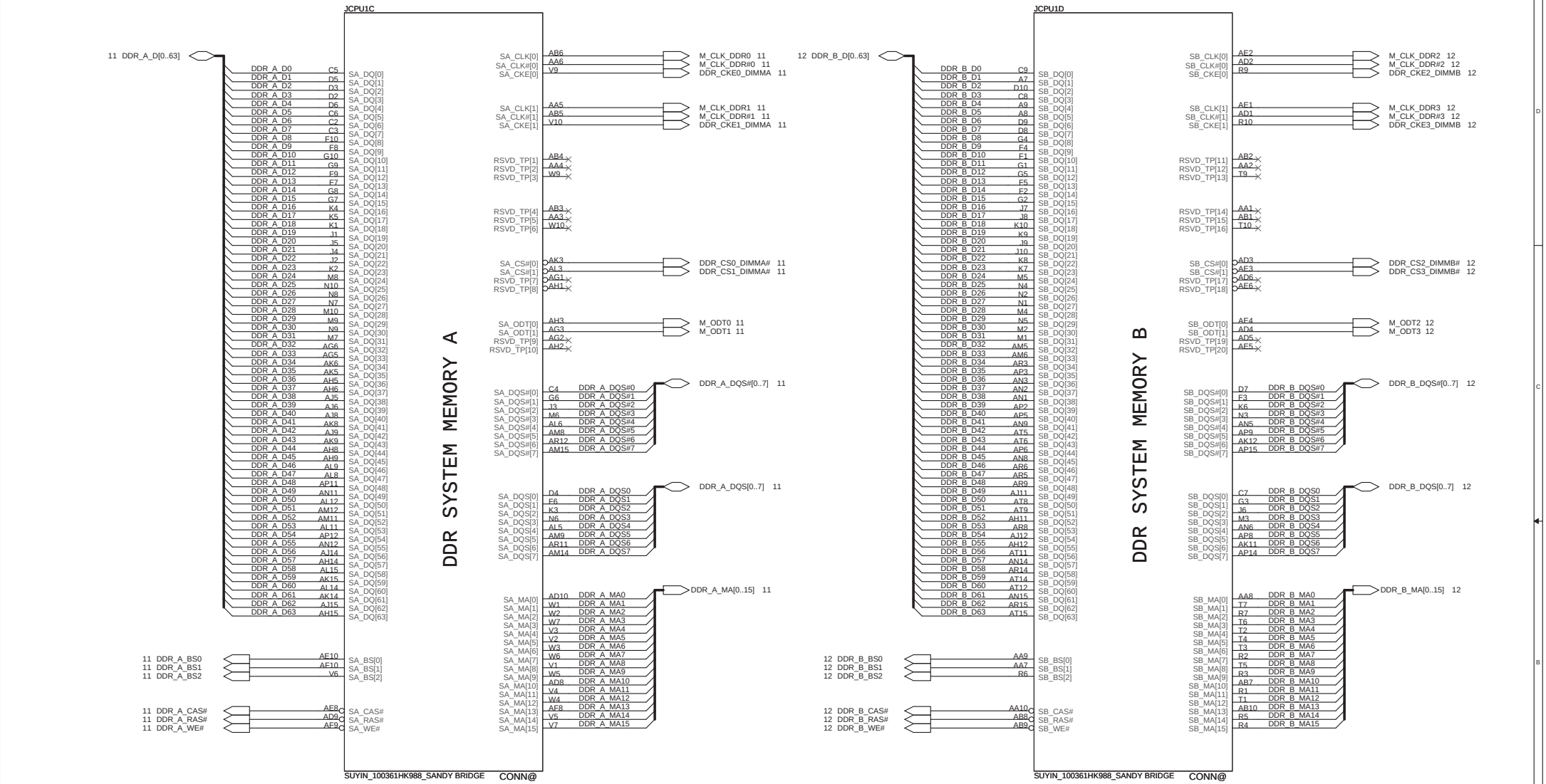

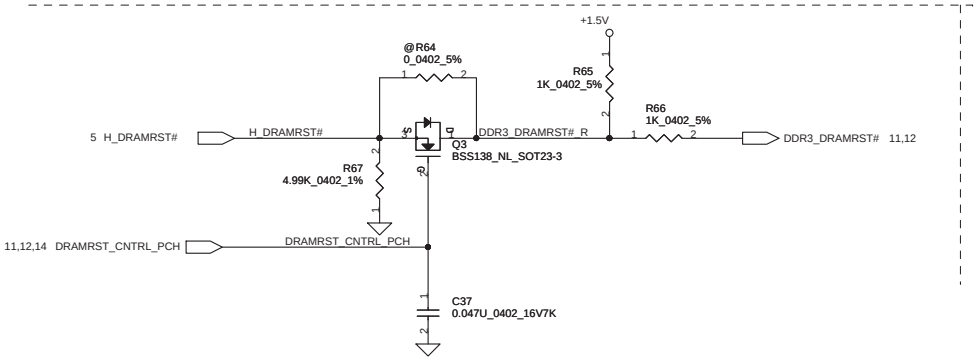

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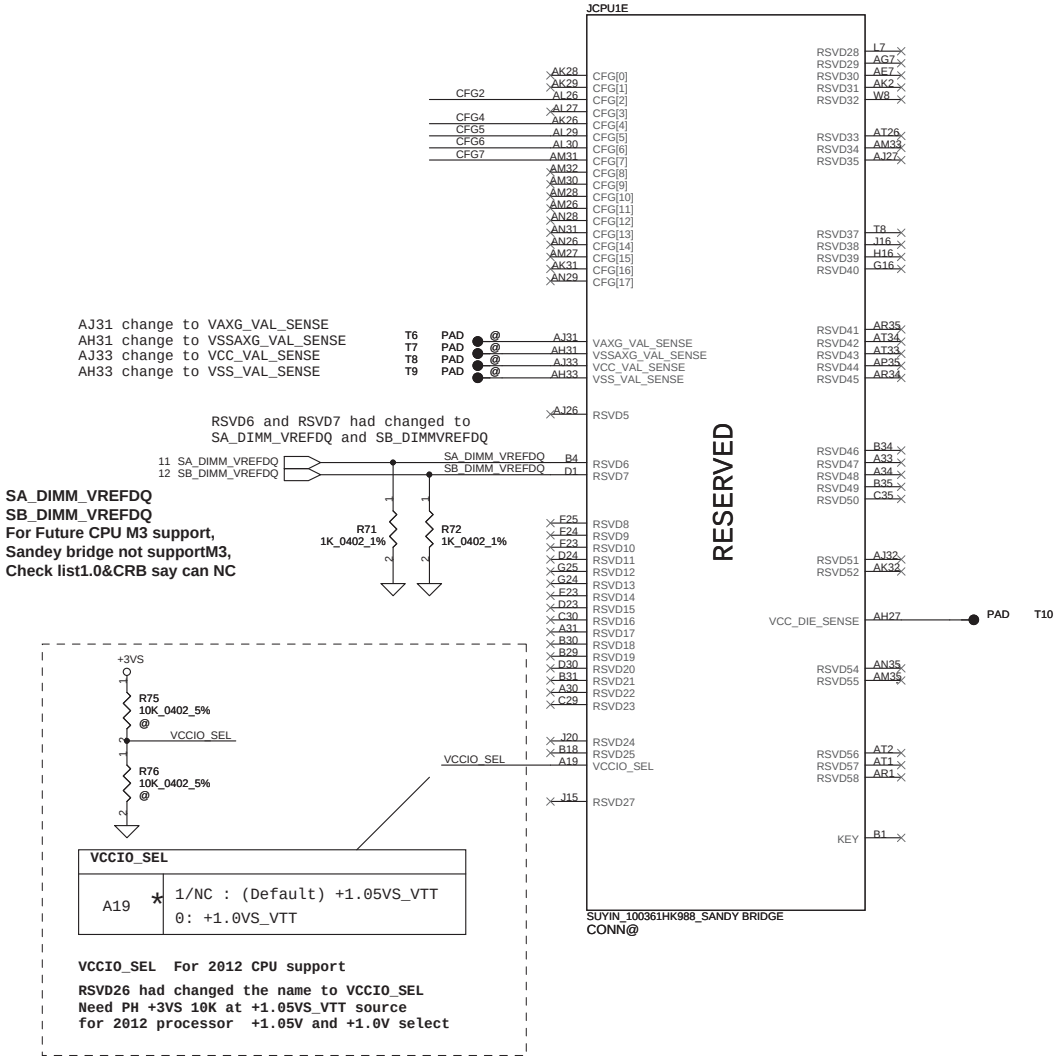
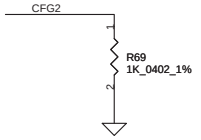
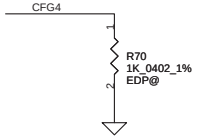
CFG Straps for Processor

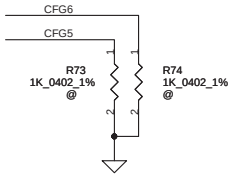




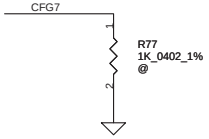
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0:Lane Reversed



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



PCIE Port Bifurcation Straps	
CFG[6:5]	*11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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POWER

SV type CPU

QC 94A
DC 53A

JCPU1F

CORE SUPPLY

+CPU_CORE

C40 10U_0805_6.3V6M
C41 10U_0805_6.3V6M
C42 10U_0805_6.3V6M
C38 10U_0805_6.3V6M
C43 10U_0805_6.3V6M
C54 10U_0805_6.3V6M
C39 10U_0805_6.3V6M
C55 10U_0805_6.3V6M
C56 10U_0805_6.3V6M
C57 10U_0805_6.3V6M

+CPU_CORE

C65 22U_0805_6.3V6M
C66 22U_0805_6.3V6M
C67 22U_0805_6.3V6M
C68 22U_0805_6.3V6M
C69 22U_0805_6.3V6M
C70 22U_0805_6.3V6M
C71 22U_0805_6.3V6M
C72 22U_0805_6.3V6M
C73 22U_0805_6.3V6M
C74 22U_0805_6.3V6M
C75 22U_0805_6.3V6M
C76 22U_0805_6.3V6M
C77 22U_0805_6.3V6M
C78 22U_0805_6.3V6M
C79 22U_0805_6.3V6M
C80 22U_0805_6.3V6M

+CPU_CORE

C81 330U_D2_2V_Y
C82 330U_D2_2V_Y
C83 330U_D2_2V_Y
C84 330U_D2_2V_Y
C85 330U_D2_2V_Y

VCC1 AG35
VCC2 AG34
VCC3 AG33
VCC4 AG32
VCC5 AG31
VCC6 AG30
VCC7 AG29
VCC8 AG28
VCC9 AG27
VCC10 AG26
VCC11 AF35
VCC12 AF34
VCC13 AF33
VCC14 AF32
VCC15 AF31
VCC16 AF30
VCC17 AF29
VCC18 AF28
VCC19 AF27
VCC20 AF26
VCC21 AD35
VCC22 AD34
VCC23 AD33
VCC24 AD32
VCC25 AD31
VCC26 AD30
VCC27 AD29
VCC28 AD28
VCC29 AD27
VCC30 AD26
VCC31 AC35
VCC32 AC34
VCC33 AC33
VCC34 AC32
VCC35 AC31
VCC36 AC30
VCC37 AC29
VCC38 AC28
VCC39 AC27
VCC40 AC26
VCC41 AA35
VCC42 AA34
VCC43 AA33
VCC44 AA32
VCC45 AA31
VCC46 AA30
VCC47 AA29
VCC48 AA28
VCC49 AA27
VCC50 AA26
VCC51 Y35
VCC52 Y34
VCC53 Y33
VCC54 Y32
VCC55 Y31
VCC56 Y30
VCC57 Y29
VCC58 Y28
VCC59 Y27
VCC60 Y26
VCC61 V35
VCC62 V34
VCC63 V33
VCC64 V32
VCC65 V31
VCC66 V30
VCC67 V29
VCC68 V28
VCC69 V27
VCC70 V26
VCC71 U35
VCC72 U34
VCC73 U33
VCC74 U32
VCC75 U31
VCC76 U30
VCC77 U29
VCC78 U28
VCC79 U27
VCC80 U26
VCC81 R35
VCC82 R34
VCC83 R33
VCC84 R32
VCC85 R31
VCC86 R30
VCC87 R29
VCC88 R28
VCC89 R27
VCC90 R26
VCC91 P35
VCC92 P34
VCC93 P33
VCC94 P32
VCC95 P31
VCC96 P30
VCC97 P29
VCC98 P28
VCC99 P27
VCC100 P26

PEG AND DDR

8.5A

+1.05VS_VCCP

VCCIO1 AH13
VCCIO2 AH10
VCCIO3 AG10
VCCIO4 AC10
VCCIO5 Y10
VCCIO6 U10
VCCIO7 P10
VCCIO8 L10
VCCIO9 J14
VCCIO10 J13
VCCIO11 J12
VCCIO12 J11
VCCIO13 H14
VCCIO14 H12
VCCIO15 H11
VCCIO16 G14
VCCIO17 G13
VCCIO18 G12
VCCIO19 F14
VCCIO20 F13
VCCIO21 F12
VCCIO22 F11
VCCIO23 E14
VCCIO24 E12
VCCIO25 E11
VCCIO26 D14
VCCIO27 D13
VCCIO28 D12
VCCIO29 D11
VCCIO30 C14
VCCIO31 C13
VCCIO32 C12
VCCIO33 C11
VCCIO34 B14
VCCIO35 B12
VCCIO36 A14
VCCIO37 A13
VCCIO38 A12
VCCIO39 A11
VCCIO40 J23

C44 22U_0805_6.3V6M
C45 22U_0805_6.3V6M
C46 22U_0805_6.3V6M
C47 22U_0805_6.3V6M
C48 22U_0805_6.3V6M
C49 22U_0805_6.3V6M
C50 22U_0805_6.3V6M
C51 22U_0805_6.3V6M
C52 22U_0805_6.3V6M
C53 22U_0805_6.3V6M
C58 22U_0805_6.3V6M
C59 22U_0805_6.3V6M
@ C60 22U_0805_6.3V6M
@ C61 22U_0805_6.3V6M
C62 330U_D2_2V_Y
C63 330U_D2_2V_Y

Cap quantity follow 43890_HR_CHKLST_Rev07

SVID

+1.05VS_VCCP

R78 130_0402_5%
R79 75_0402_5%
R80 43_0402_1%
R81 0_0402_5%
R82 0_0402_5%

VIDALERT# AJ29 H_CPU_SVIDALRT#
VIDSCLK AJ30 H_CPU_SVIDCLK
VIDSOUT AJ28 H_CPU_SVIDDAT

VR_SVID_ALRT# 54
VR_SVID_CLK 54
VR_SVID_DAT 54

Place the PU resistors close to VR

SENSE LINES

+CPU_CORE

R83 100_0402_1%
R84 0_0402_5%
R85 0_0402_5%
R86 100_0402_1%

VCC_SENSE AJ35 VCCSENSE_R
VSS_SENSE AJ34 VSSSENSE_R

VCCSENSE 54
VSSSENSE 54

VCCIO_SENSE B10
VSSIO_SENSE A10 VSSIO_SENSE

VCCIO_SENSE 53
VSSIO_SENSE 53

Place the PU resistors close to CPU

SUYIN_100361HK988_SANDY BRIDGE CONN@

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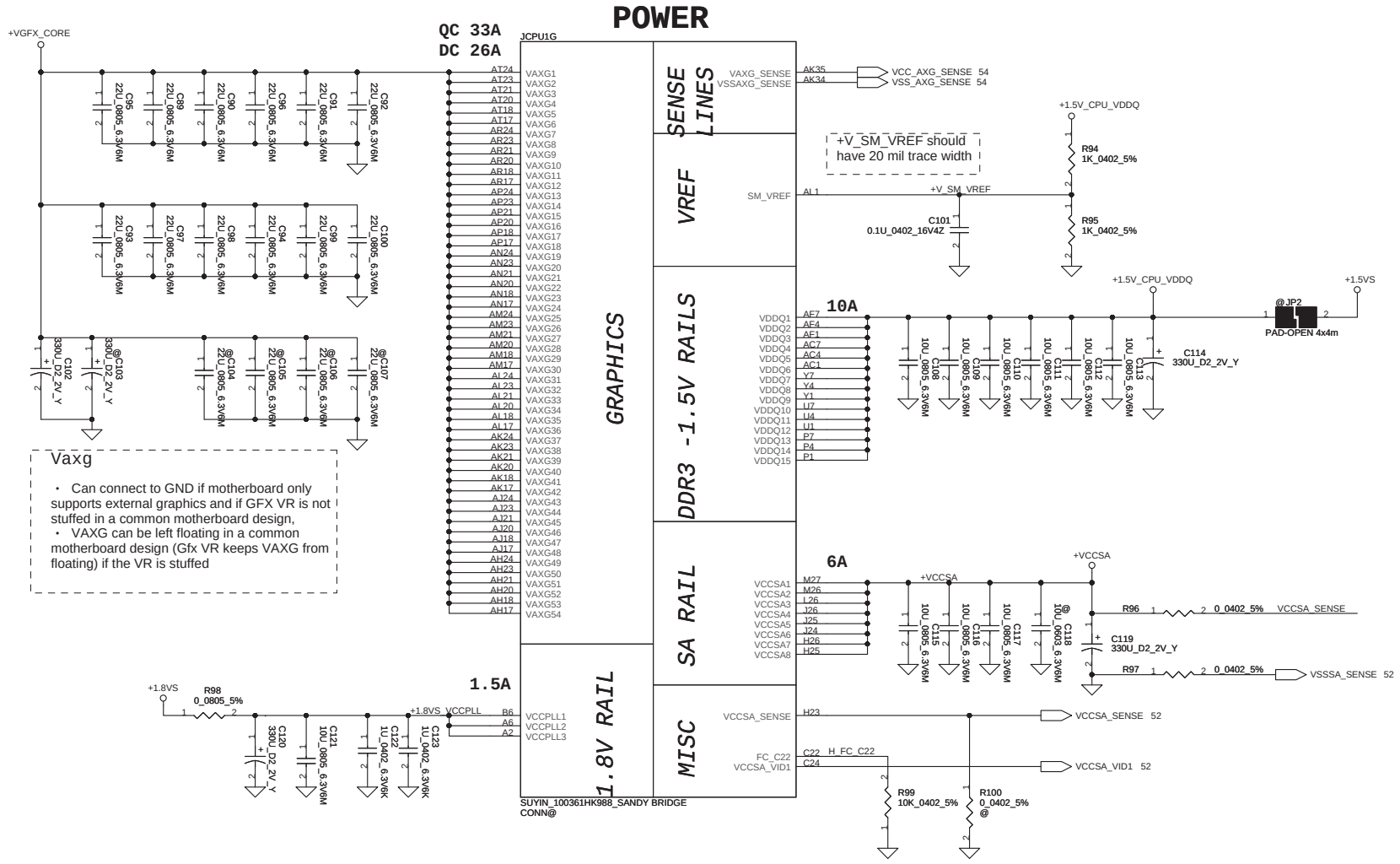
POWER



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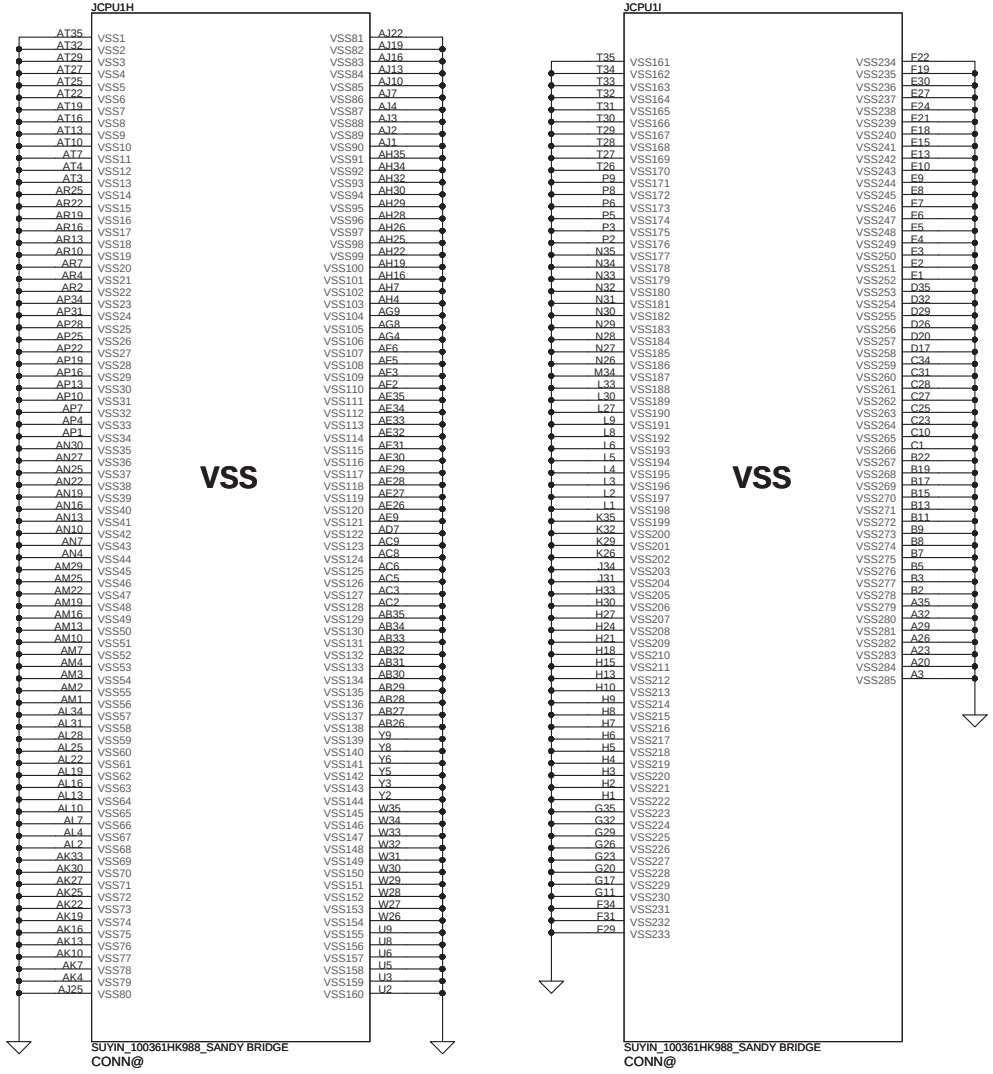

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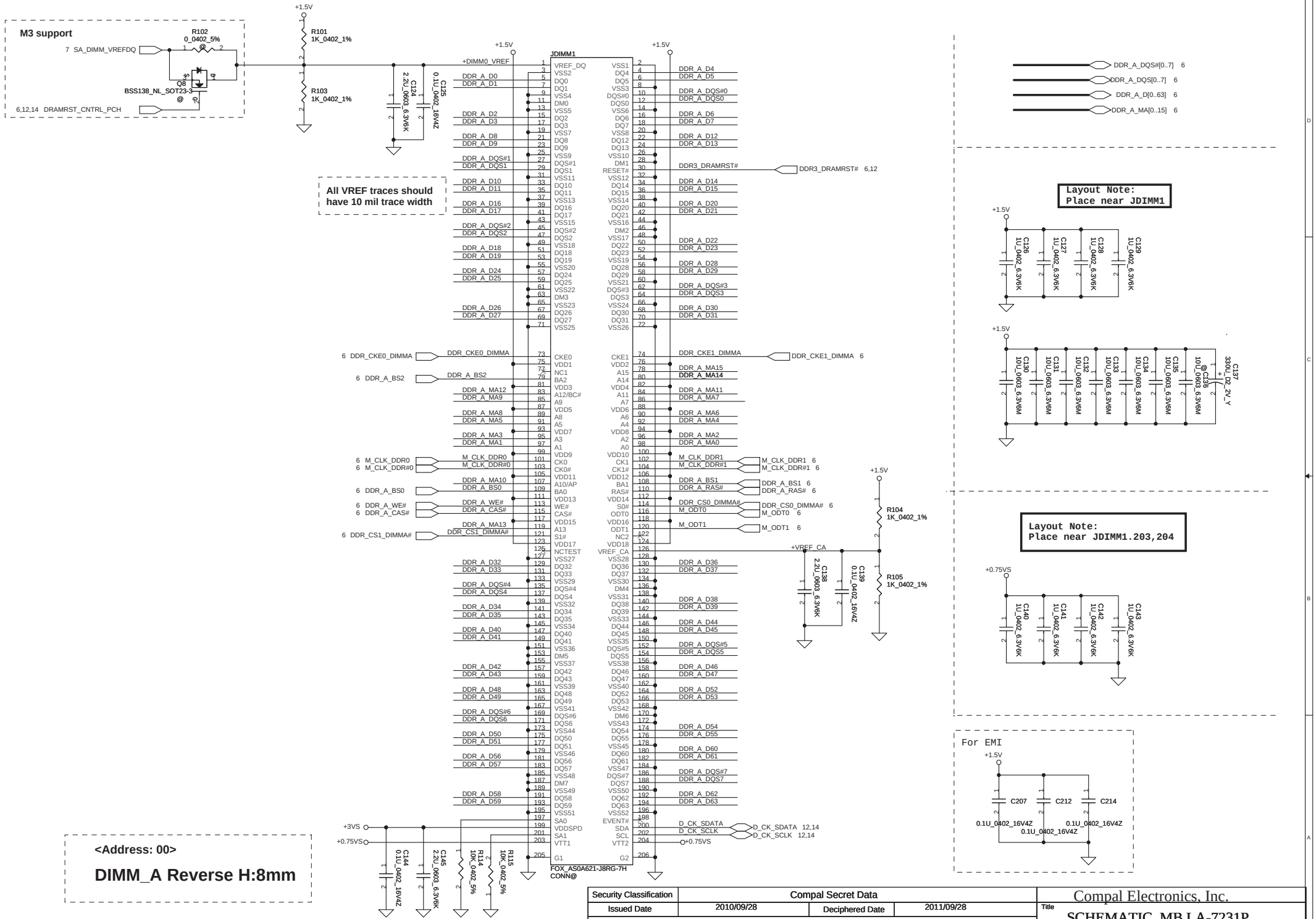

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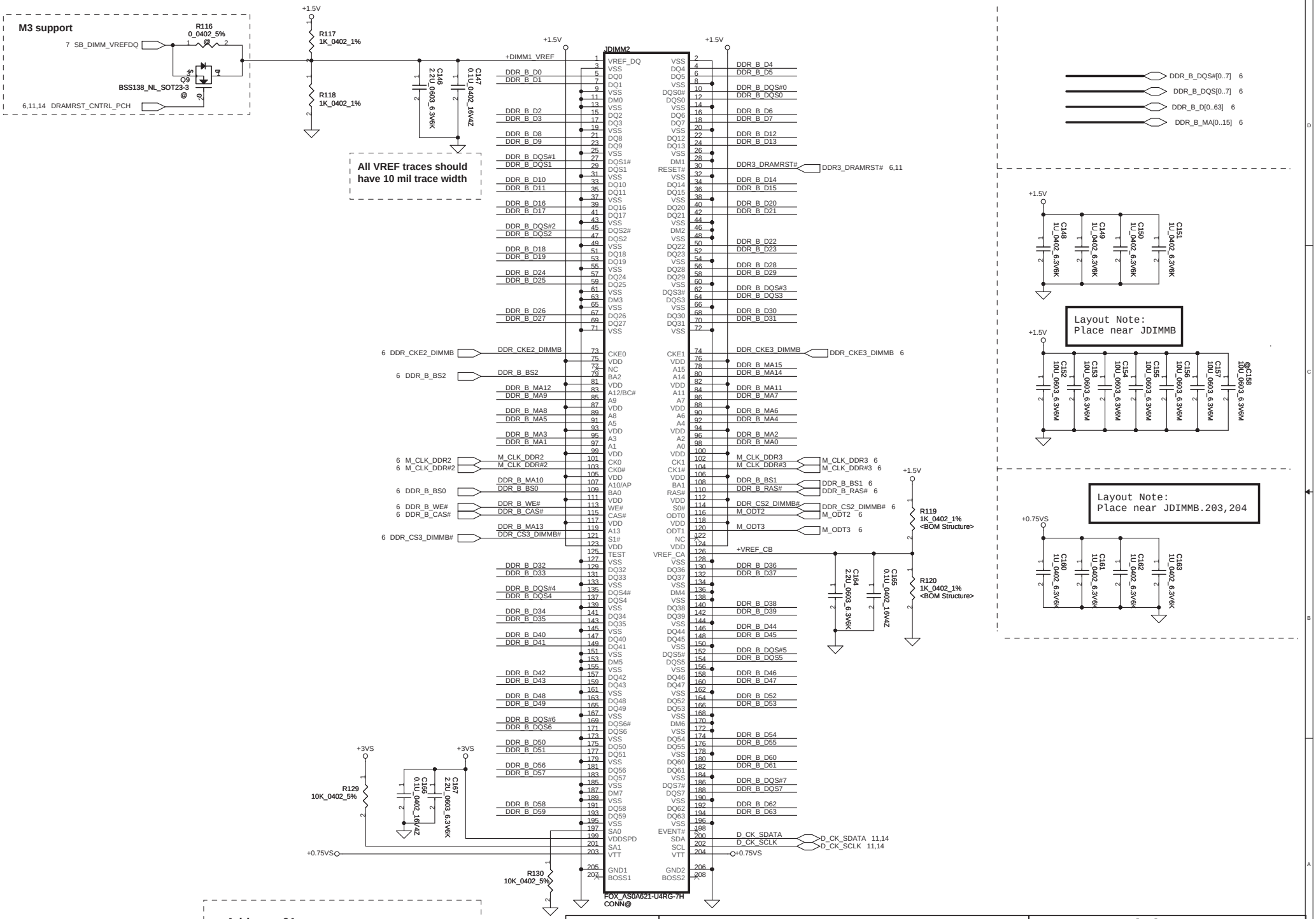

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DIMM_B Reverse type H:4mm

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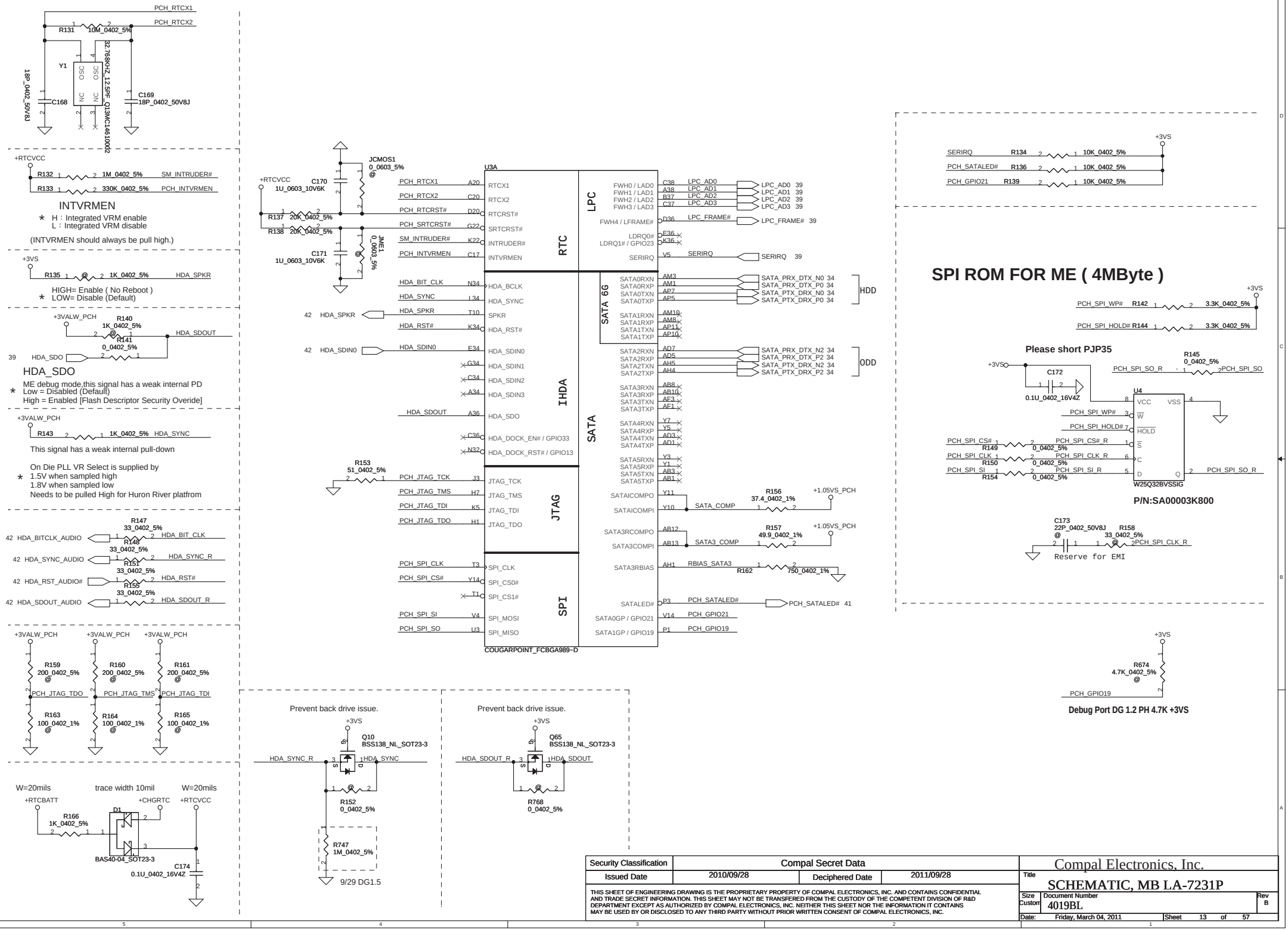

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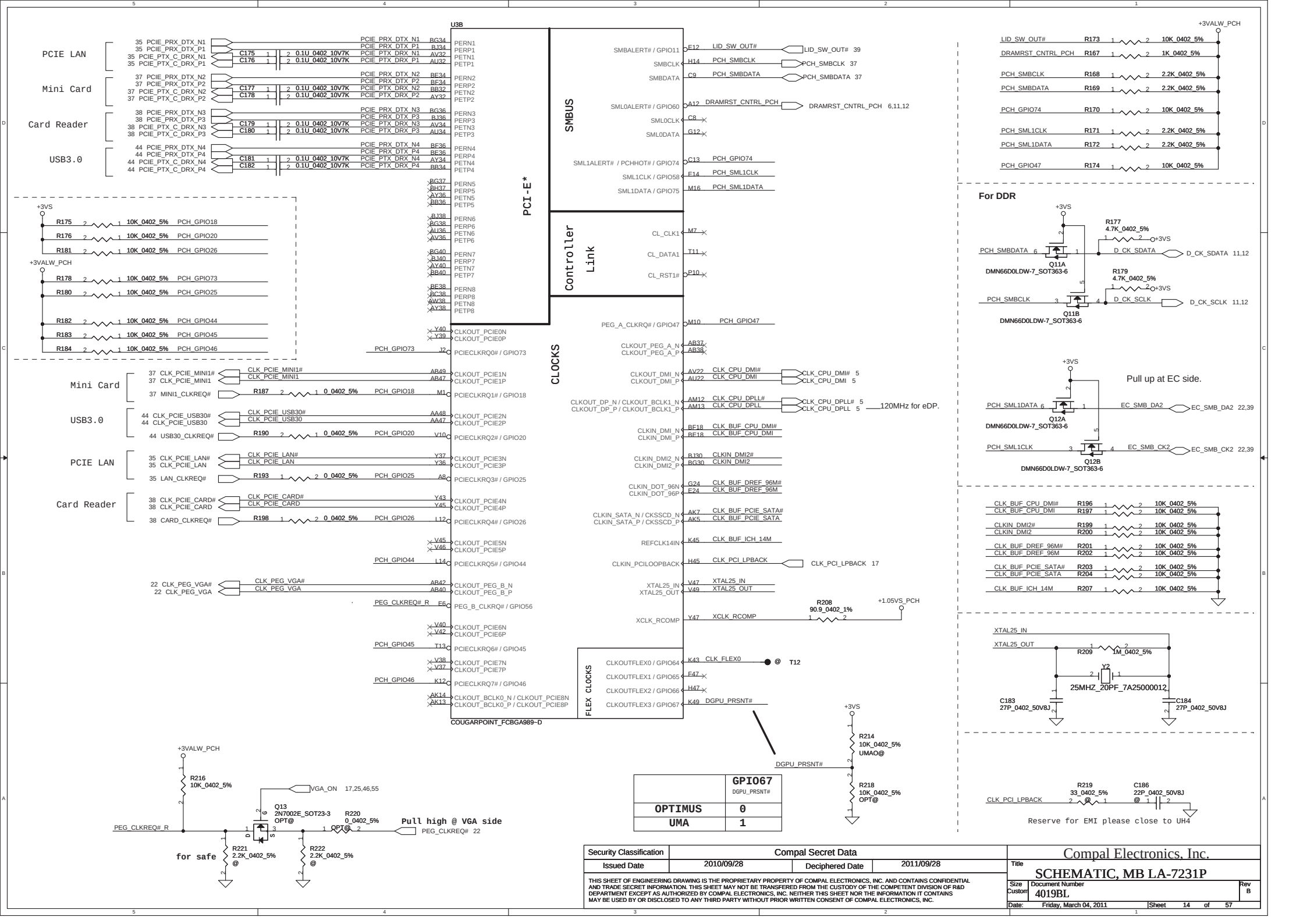

	GPIO67 DGPU_PRSNT#
OPTIMUS	0
UMA	1

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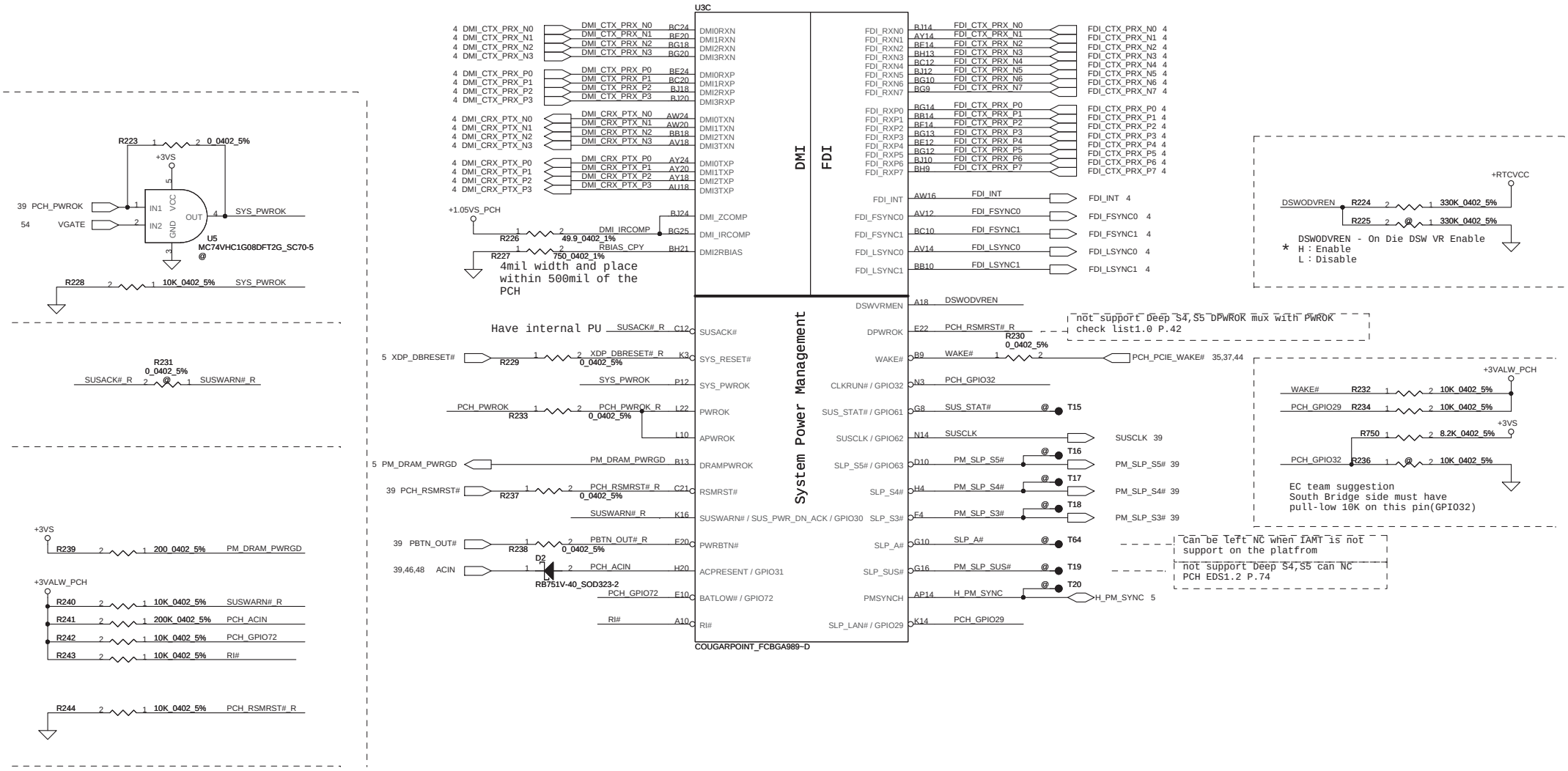

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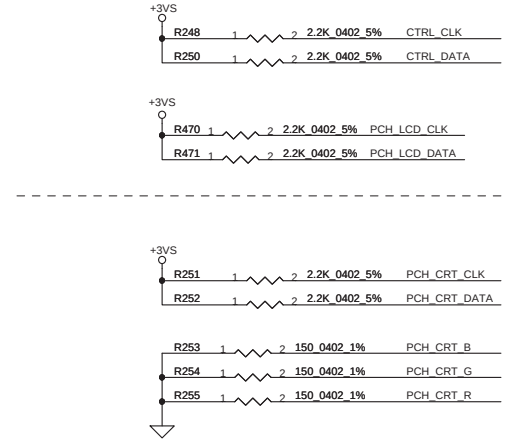

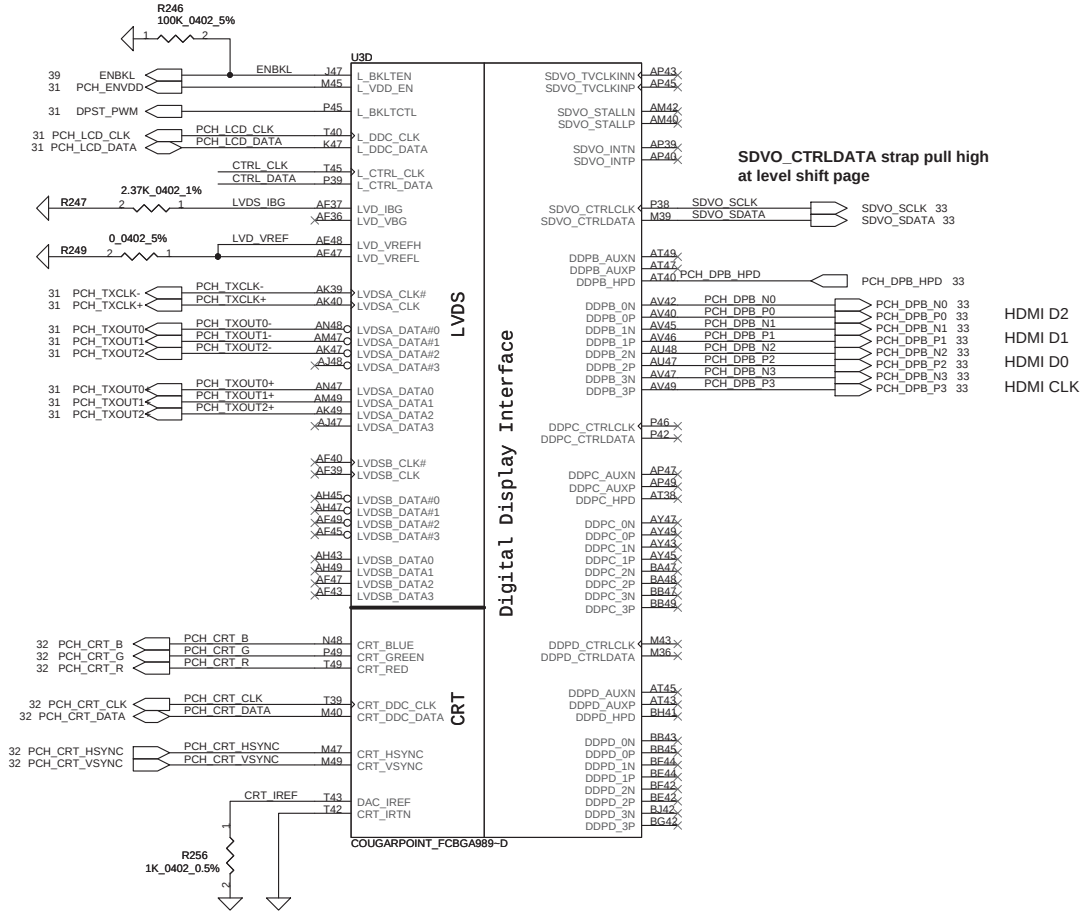

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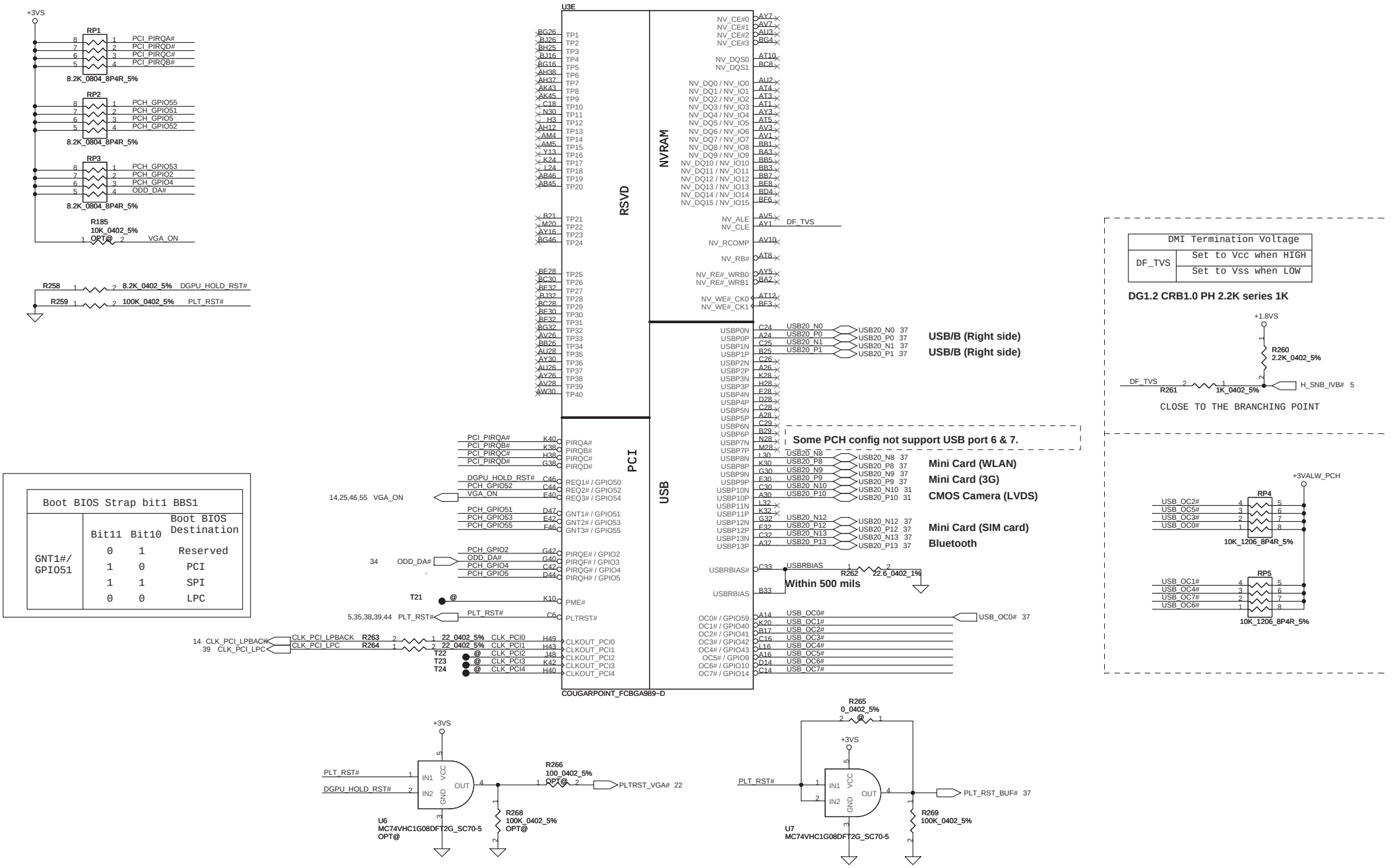

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+3VS

R279 2 UMA@ 1 10K_0402_5% OPTIMUS_EN#

R643 1 OPT@ 2 10K_0402_5%

	GPIO38 OPTIMUS_EN#
* OPTIMUS	0
Non-OPTIMUS	1

GPIO28

On-Die PLL Voltage Regulator

This signal has a weak internal pull up

*** H : On-Die PLL voltage regulator enable**
L : On-Die PLL Voltage Regulator disable

+3VALW_PCH

R485 1 @ 2 4.7K_0402_5%

R272 2 @ 1 PCH_GPIO28
1K_0402_5%

Debug Port DG 1.2 PH 4.7K +3VALW_PCH

Deep S4,S5 wake event signal
RTC alarm,Power BTN,GPIO27
PCH_GPIO27 (Have internal Pull-High)
Deep S4,S5 wake event signal
No use PD to GND Check list1.0 P.70

R277 1 2 10K_0402_5% PCH_GPIO27

+3VS

R270 2 1 10K_0402_5% PCH_GPIO0

R280 1 2 10K_0402_5% PCH_GPIO1

R281 1 2 10K_0402_5% DGPU_HPD_INT#

R282 1 2 10K_0402_5% PCH_GPIO16

R284 1 2 10K_0402_5% PCH_GPIO22

R285 1 2 100K_0402_5% WWAN_OFF#

R286 1 2 200K_0402_5% ODD_DETECT#

R287 1 2 10K_0402_5% PCH_GPIO39

R288 1 2 10K_0402_5% BT_ON#

R289 1 2 10K_0402_5% PCH_GPIO48

R290 1 2 10K_0402_5% WL_OFF#

CRB1.0 PH200K to +3VS

+3VALW_PCH

R291 1 2 10K_0402_5% PCH_GPIO12

R292 1 2 1K_0402_5% SMIB

R293 1 2 10K_0402_5% PCH_GPIO57

R294 1 2 10K_0402_5% PCH_GPIO24

CRB1.0 PH10K to +3VALW
GPIO24 Unmultiplexed
NOTE: GPIO24 configuration register bits are not cleared by CF9h reset event.

Modify R03

+3VS

R283 10K_0402_5%

+3VSDGPU

R841 10K_0402_5% OPT@

R842 100K_0402_5% OPT@

Q74A DMN66D0LDW-7_SOT363-6 OPT@

Q74B DMN66D0LDW-7_SOT363-6 OPT@

C185 1U_0402_6.3V6K OPT@

If GPIO36,37 did not use, it can not PU and reserved PD resistor for MRC0.9.

U3F

	PCH_GPIO0	T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 ODD_EN# → ODD_EN# 34
	PCH_GPIO1	A42	TACH1 / GPIO1	TACH5 / GPIO69	B41 PCH_GPIO69 → @T26
33 DGPU_HPD_INT#	DGPU_HPD_INT#	H36	TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70 → @T27
39 EC_SCI#	EC_SCI#	E38	TACH3 / GPIO7	TACH7 / GPIO71	A40 PCH_GPIO71
39 EC_SMI#	EC_SMI#	C10	GPIO8		
	PCH_GPIO12	C4	LAN_PHY_PWR_CTRL / GPIO12		
44 SMIB	SMIB	G2	GPIO15	A20GATE	P4 → GATEA20 39
	PCH_GPIO16	U2	SATA4GP / GPIO16	PECI	AU16 PCH_PECI_R 1 @ 2 0_0402_5% R274 → H_PECI 5,39
	DGPU_PWROK	D40	TACH0 / GPIO17	RCIN#	P5 EC_KBRST# → EC_KBRST# 39
	PCH_GPIO22	T5	SCLOCK / GPIO22	PROCPWRGD	AY11 → H_CPUPWRGD 5
	PCH_GPIO24	F8	GPIO24 / MEM_LED	THRMTRIP#	AY10 PCH_THRMTRIP#_R 1 2 H_THRMTRIP# R278 390_0402_5% → H_THRMTRIP# 5
	PCH_GPIO27	E16	GPIO27	INIT3_3V#	T14
	PCH_GPIO28	P8	GPIO28		
37 BT_ON#	BT_ON#	K1	STP_PCI# / GPIO34	NC_1	AH8
		K4	GPIO35	NC_2	AK11
34 ODD_DETECT#	ODD_DETECT#	V8	SATA2GP / GPIO36	NC_3	AH10
37 WWAN_OFF#	WWAN_OFF#	M5	SATA3GP / GPIO37	NC_4	AK10
	OPTIMUS_EN#	N2	SLOAD / GPIO38	NC_5	P37
	PCH_GPIO39	M3	SDATAOUT0 / GPIO39		
	PCH_GPIO48	V13	SDATAOUT1 / GPIO48		
37 WL_OFF#	WL_OFF#	V3	SATA5GP / GPIO49		
	PCH_GPIO57	D6	GPIO57		

GPIO — CPU/MISC

T32 @	A4	VSS_NCTF_1	
T34 @	A44	VSS_NCTF_2	
T36 @	A45	VSS_NCTF_3	
T38 @	A46	VSS_NCTF_4	
T40 @	A5	VSS_NCTF_5	
T42 @	A6	VSS_NCTF_6	
T44 @	B3	VSS_NCTF_7	
T46 @	B47	VSS_NCTF_8	
T47 @	BD1	VSS_NCTF_9	
T49 @	BD49	VSS_NCTF_10	
T51 @	BE1	VSS_NCTF_11	
T53 @	BE49	VSS_NCTF_12	
T54 @	BF1	VSS_NCTF_13	
T56 @	BF49	VSS_NCTF_14	
	BG2	VSS_NCTF_15	@T28
	BG48	VSS_NCTF_16	@T29
	BH3	VSS_NCTF_17	@T30
	BH47	VSS_NCTF_18	@T31
	BJ4	VSS_NCTF_19	@T33
	BJ44	VSS_NCTF_20	@T35
	BJ45	VSS_NCTF_21	@T37
	BJ46	VSS_NCTF_22	@T39
	BJ5	VSS_NCTF_23	@T41
	BJ6	VSS_NCTF_24	@T43
	C2	VSS_NCTF_25	@T45
	C48	VSS_NCTF_26	@T87
	D1	VSS_NCTF_27	@T48
	D49	VSS_NCTF_28	@T50
	E1	VSS_NCTF_29	@T52
	F49	VSS_NCTF_30	@T88
	F1	VSS_NCTF_31	@T55
	F49	VSS_NCTF_32	@T89

NCTF

COUGARPOINT_FCBGA989~D

+3VS

ODD_EN# R275 1 2 10K_0402_5%

EC_KBRST# R276 1 2 10K_0402_5%

+3VS

R273 10K_0402_5%

INIT3_3V

This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand

Follow P5WE0 R02

+3VS

R567 10K_0402_5% X76@

PCH_GPIO71

R604 10K_0402_5% X76@

	GPIO71 PCH_GPIO71
VRAM 800 MHz	0
VRAM 900 MHz	1

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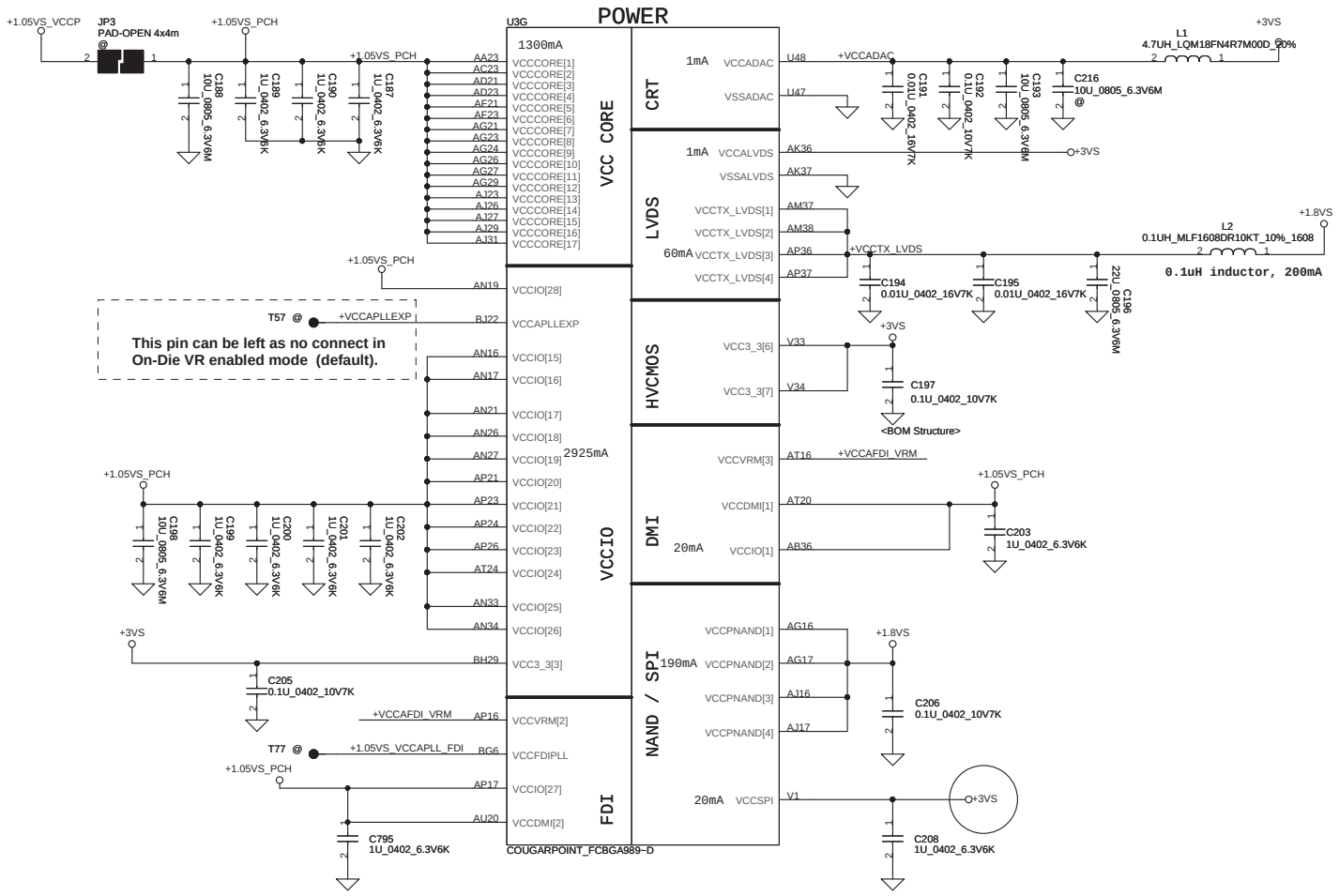

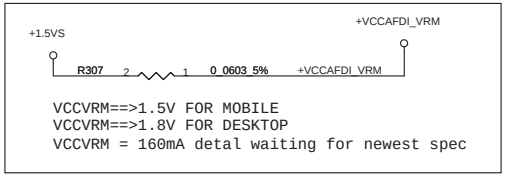

PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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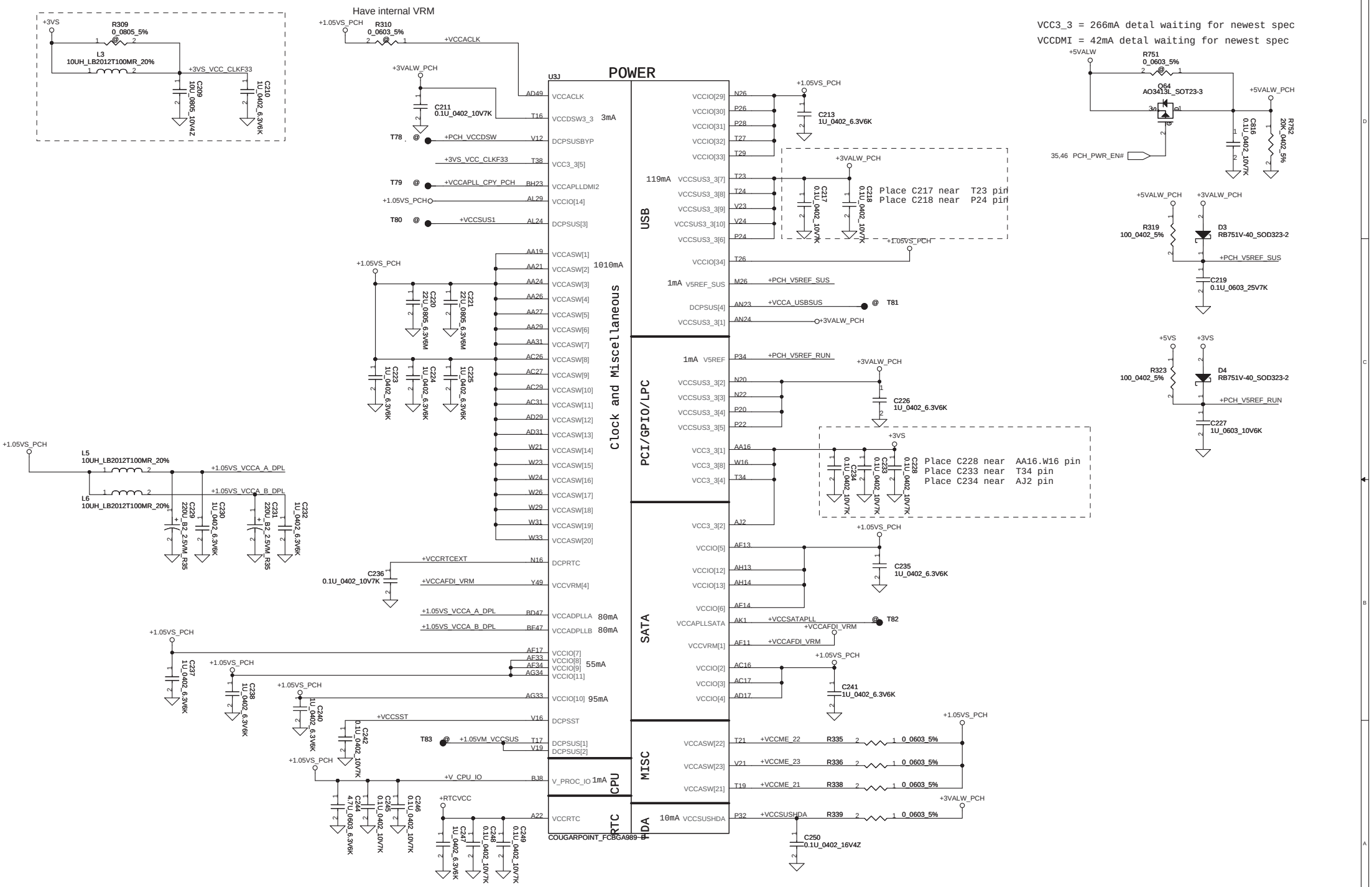

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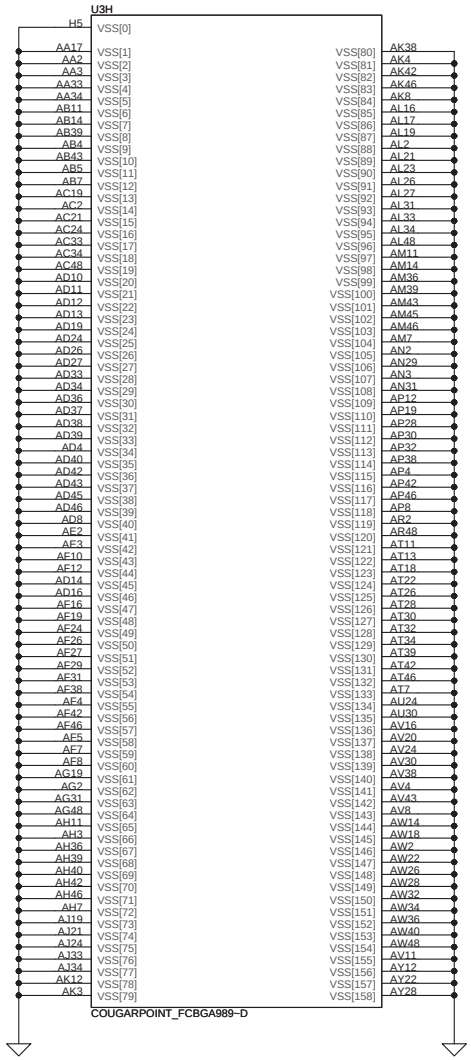

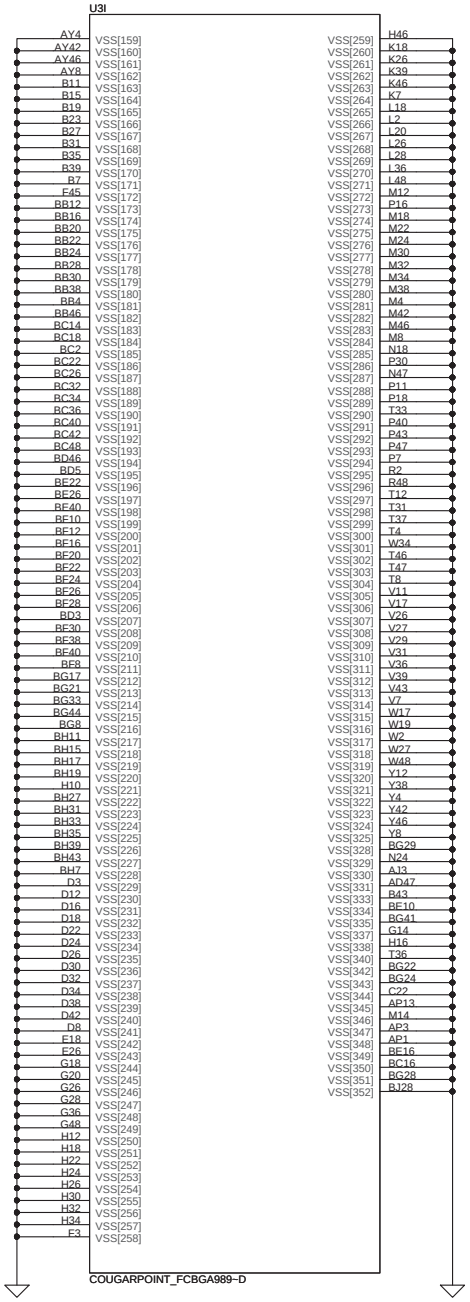

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U8A

Part 1 of 7

GPIO	I/O	FUNCTION
GPIO1	IN	HPD_C
GPIO5	OUT	GPU_VID0
GPIO6	OUT	GPU_VID1
GPIO7	OUT	GPU_VID2
GPIO8	IN	OVERT
GPIO9	IN	ALERT
GPIO12	IN	Reserve for VPS
GPIO18	IN	Reserve for VPS

External Spread Spectrum

If External Spread Spectrum not stuff then stuff resistor

Option Component

U8 N12P-GV-B-A1_BGA973 GV@ SA00004JO10

N12P-GV-B-A1_BGA973: SA00004GY00
N12P-GV-OP-B-A1_BGA973: SA00004JO10

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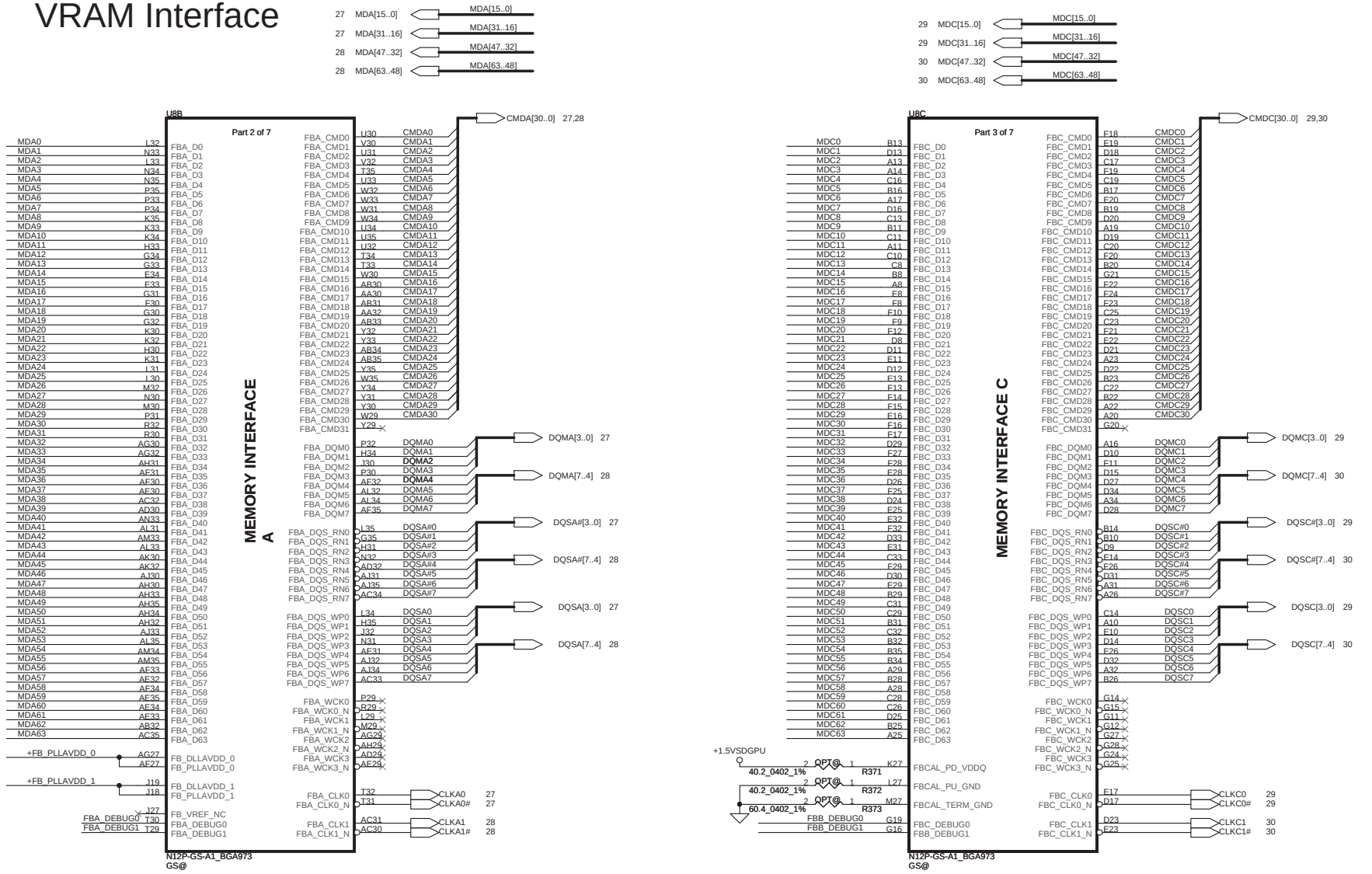
VRAM Interface



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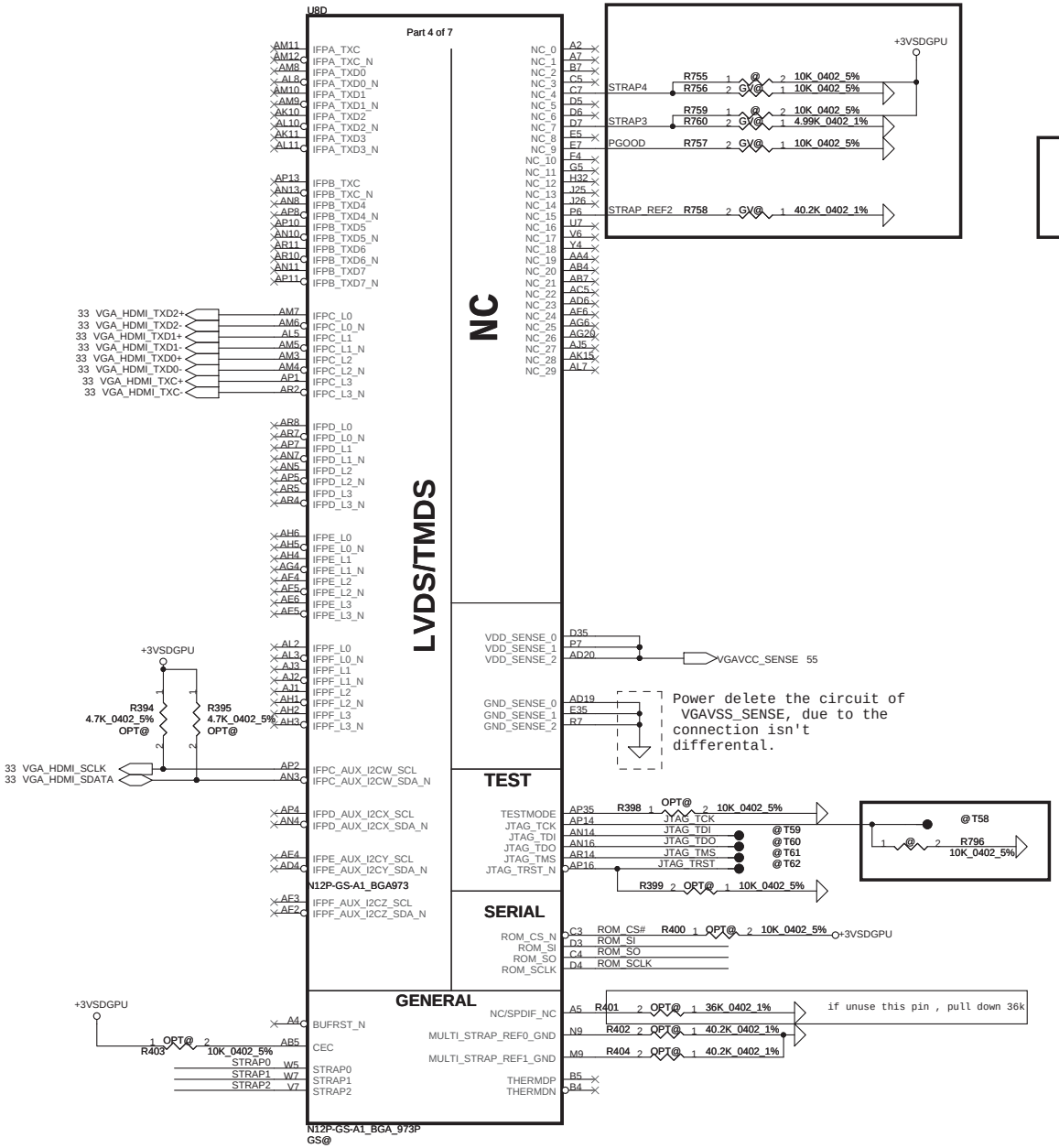
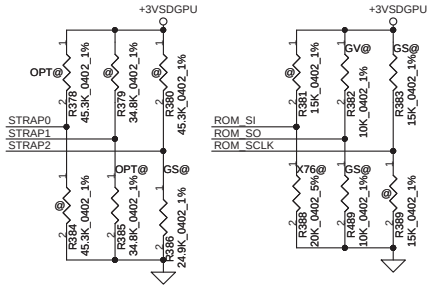
For GB2-128 & GB2b-128 colayout....



Option Component

ROM_SCLK ---> R383 2_GV@_1_4.99K_0402_1%
STRAP2 ---> R386 2_GV@_1_4.99K_0402_1%

MULTI LEVEL STRAPS



For N12P-GS strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GS	900 MHz	64M* 16* 8 1GB	Hynix SA000041S40	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 15K	R489 PD 10K	R383 PU 15K
N12P-GS	900 MHz	64M* 16* 8 1GB	Samsung SA00004GS10	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 20K	R489 PD 10K	R383 PU 15K
N12P-GS	900 MHz	128M* 16* 8 2GB	Hynix SA00003YO20	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 35K	R489 PD 10K	R383 PU 15K
N12P-GS	900 MHz	128M* 16* 8 2GB	Samsung SA000047Q20	R378 PU 45K	R385 PD 35K	R386 PD 25K	NC	NC	R388 PD 45K	R489 PD 10K	R383 PU 15K

For N12P-GV-OP-B-A1 strap table

GPU	Frenq.	Memory Size	Memory Config	strap0	strap1	strap2	strap3	strap4	ROM_SI	ROM_SO	ROM_SCLK
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Hynix SA000041S40	R378 PU 45K	R385 PD 35K	R386 PD 5K	R760 PD 5K	R756 PD 10K	R388 PD 15K	R382 PU 10K	R383 PU 5K
N12P-GV OP-B-A1	900 MHz	64M* 16* 4 512MB	Samsung SA00004GS10	R378 PU 45K	R385 PD 35K	R386 PD 5K	R760 PD 5K	R756 PD 10K	R388 PD 20K	R382 PU 10K	R383 PU 5K

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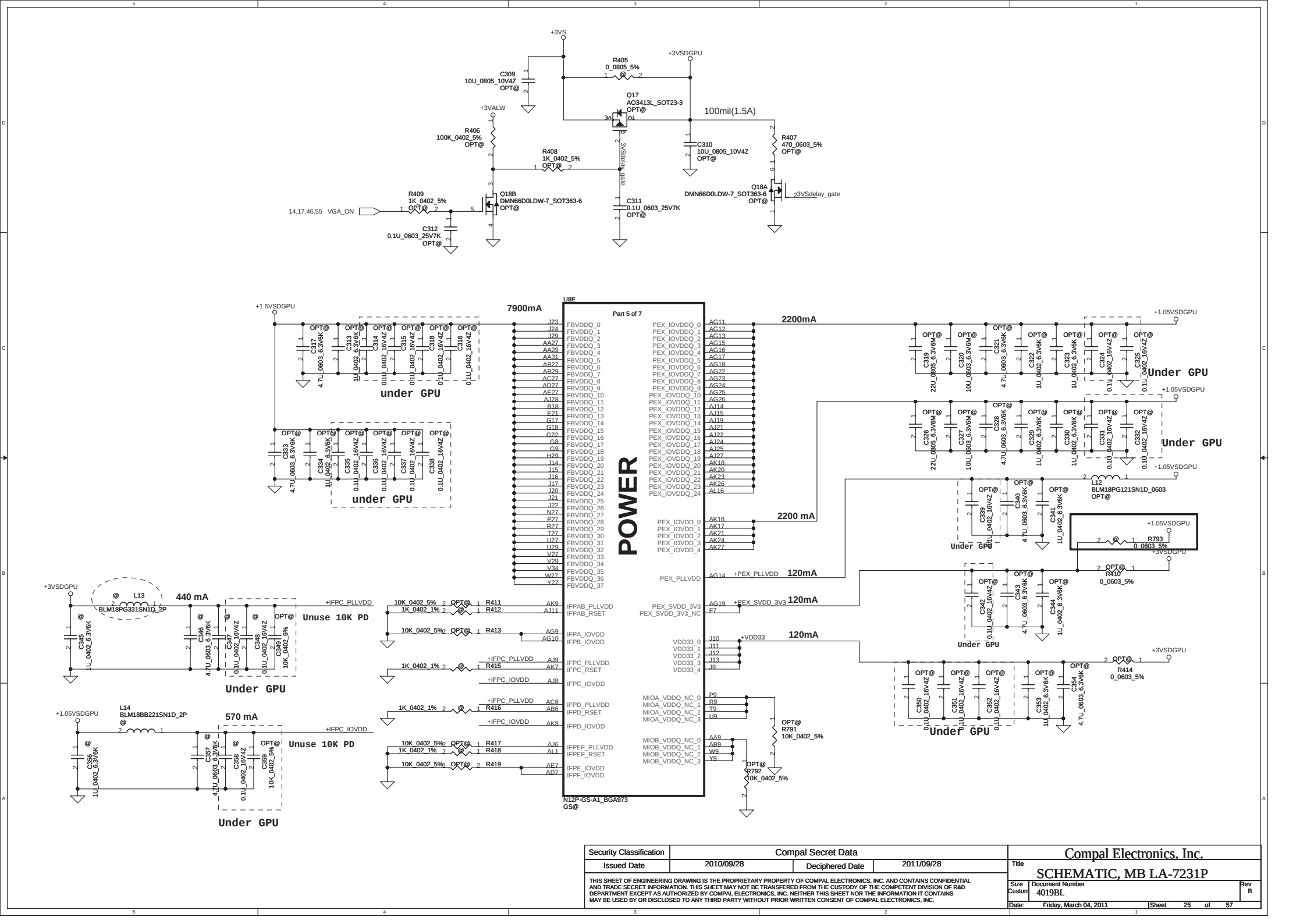

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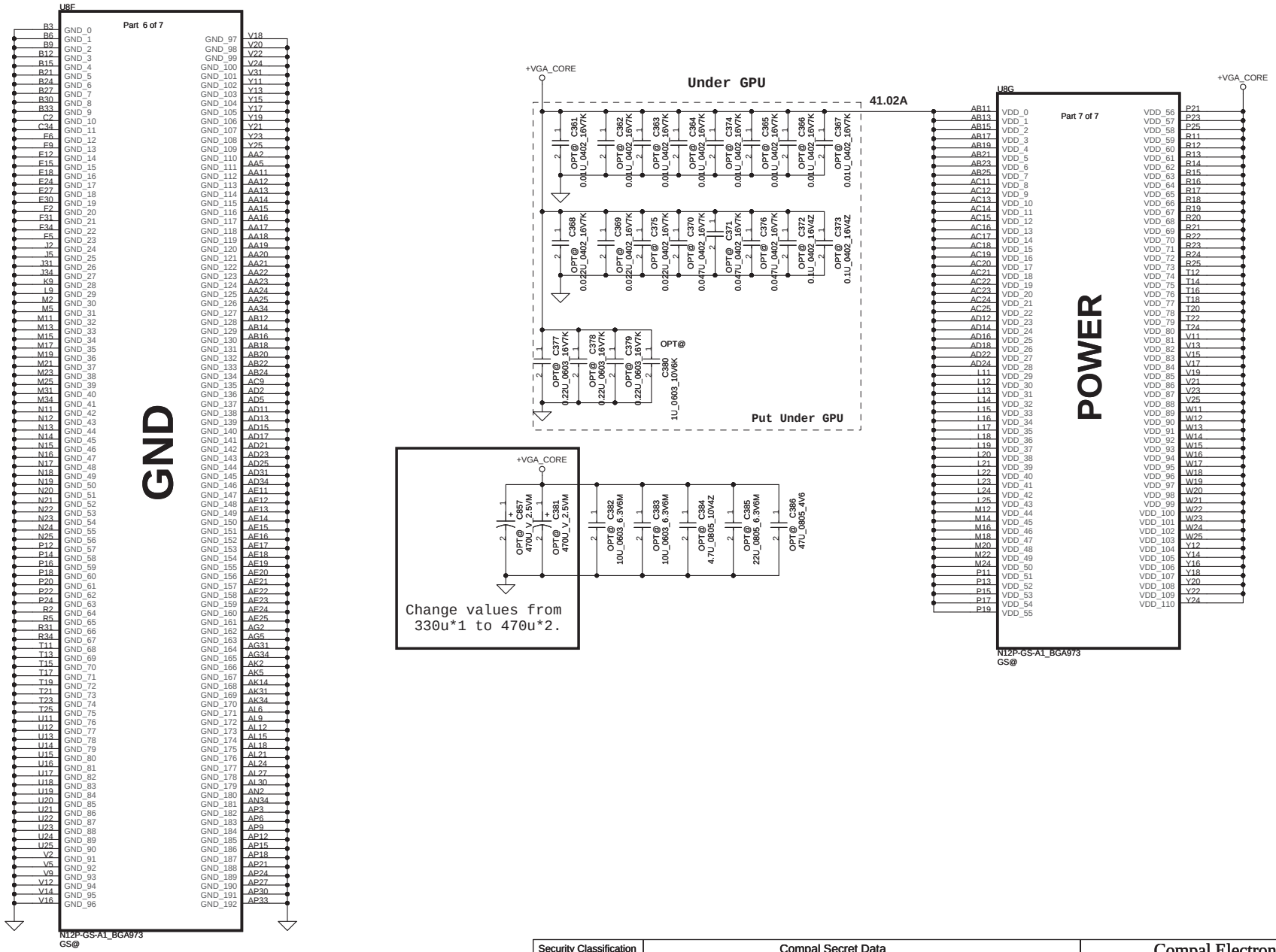

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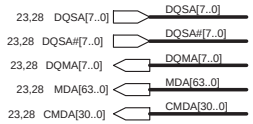
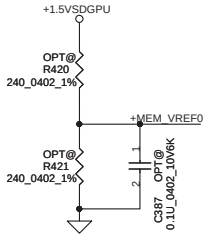
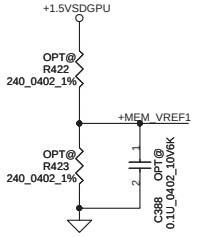
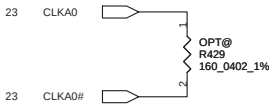
VRAM DDR3 chips (1GB)

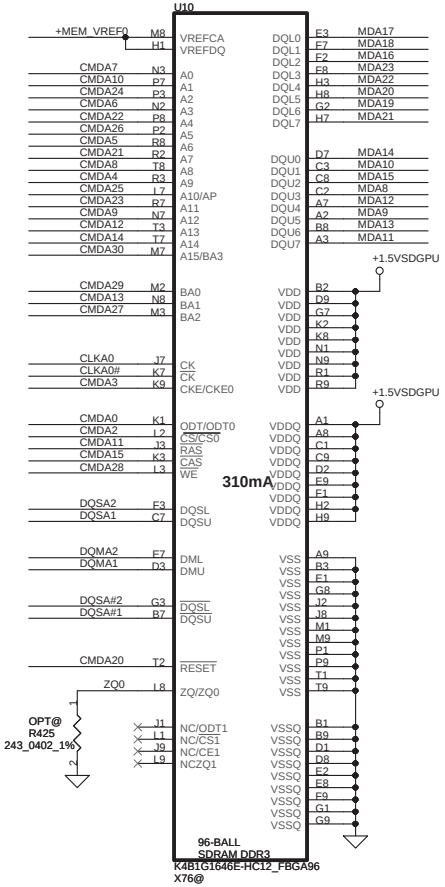
64Mx16 DDR3 *8==>1GB

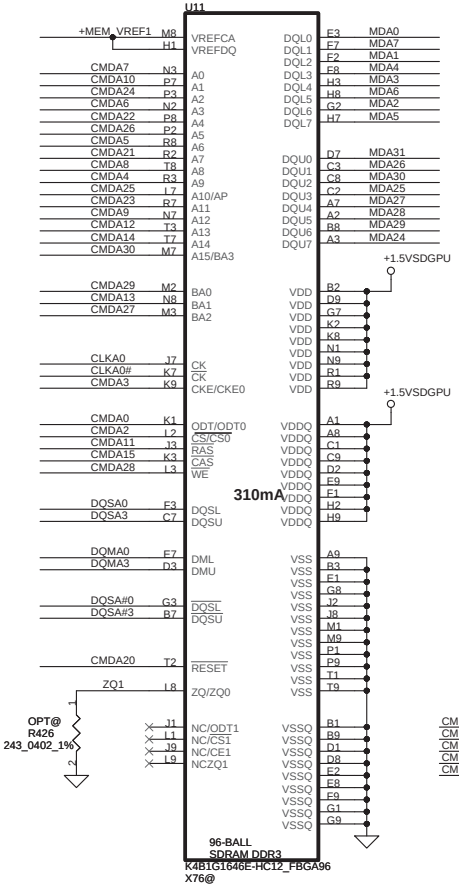




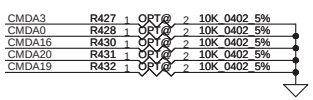




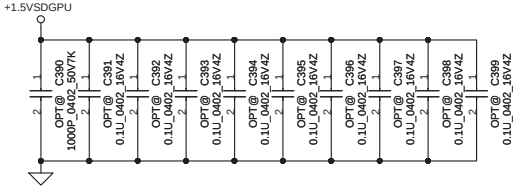


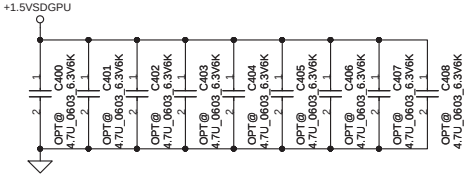


Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

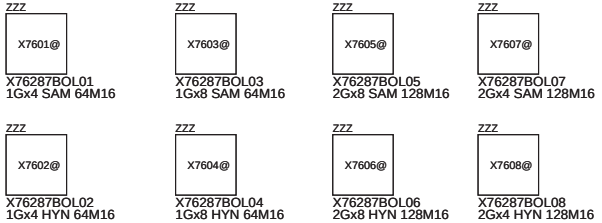


	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination





X76



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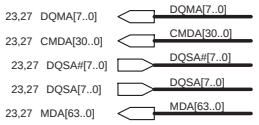
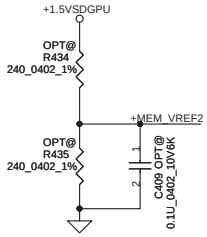
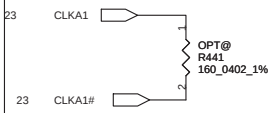
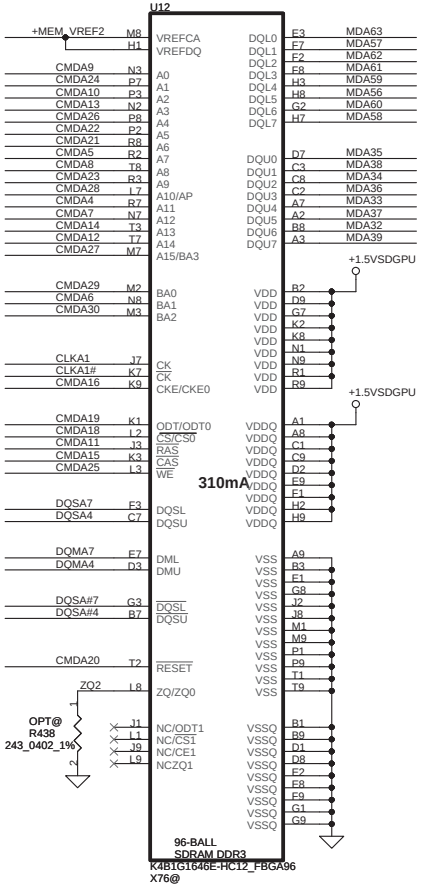
VRAM DDR3 chips (1GB)

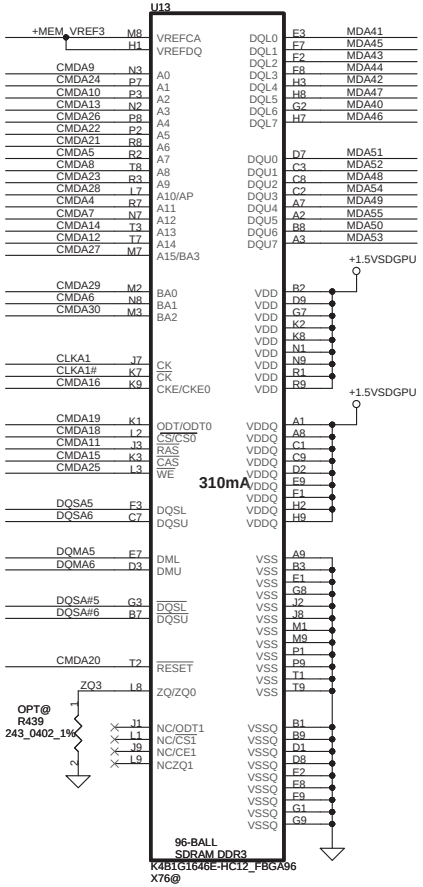
64Mx16 DDR3 *8==>1GB

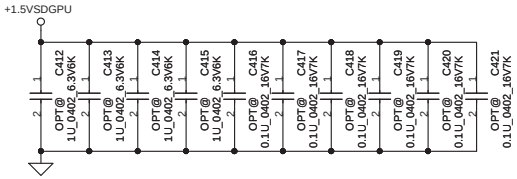


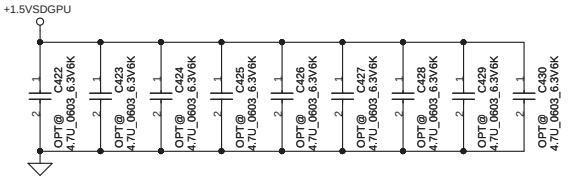












Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

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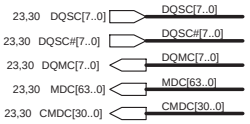
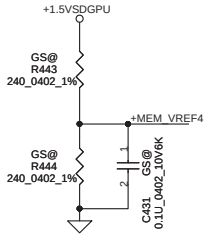
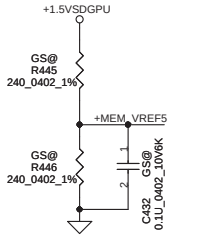
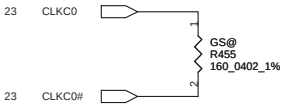
VRAM DDR3 chips (1GB)

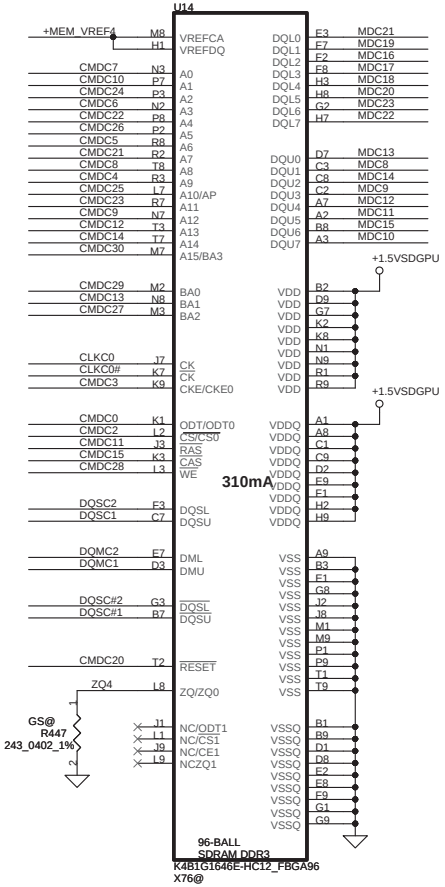
64Mx16 DDR3 *8==>1GB

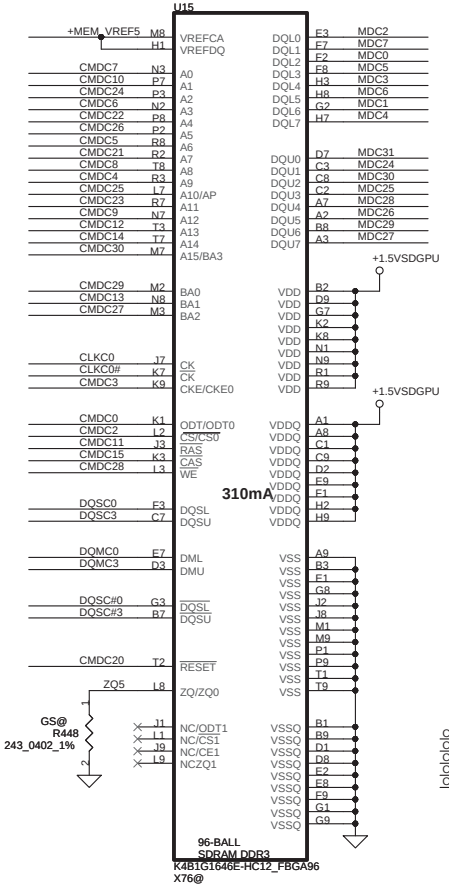


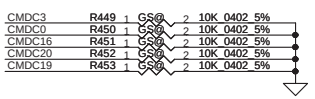


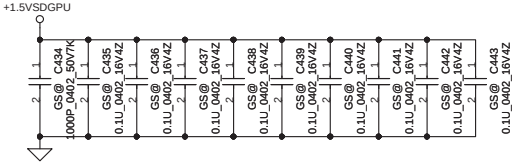


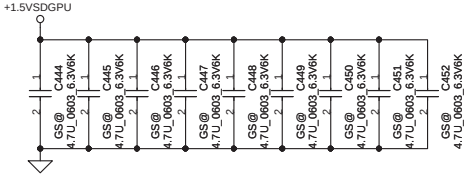












Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

	Command Bit	Default Pull-down
DDR3	ODTx	10k
	CKEx	10k
	RST	10k
	CS*	No Termination

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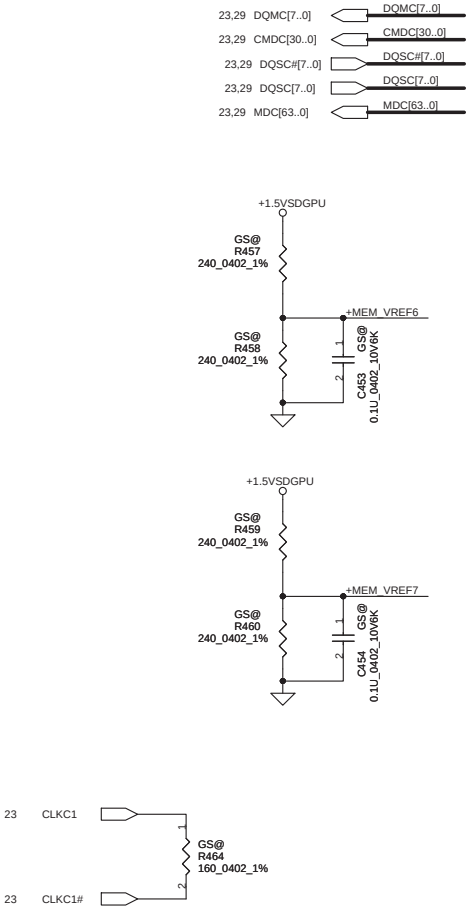
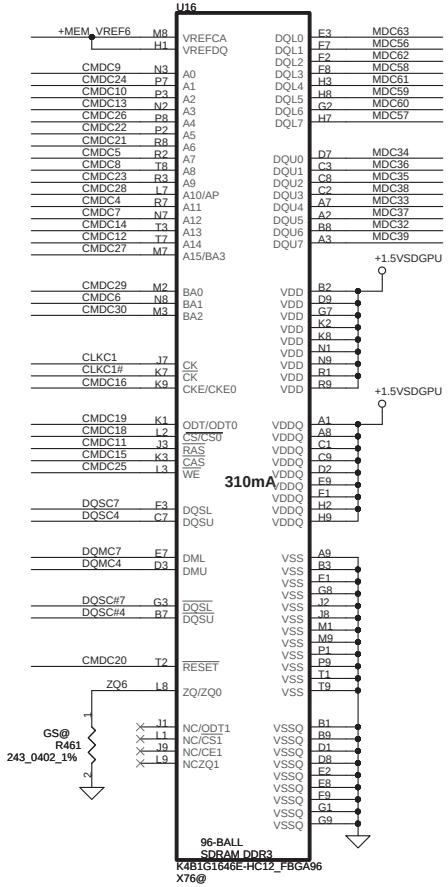
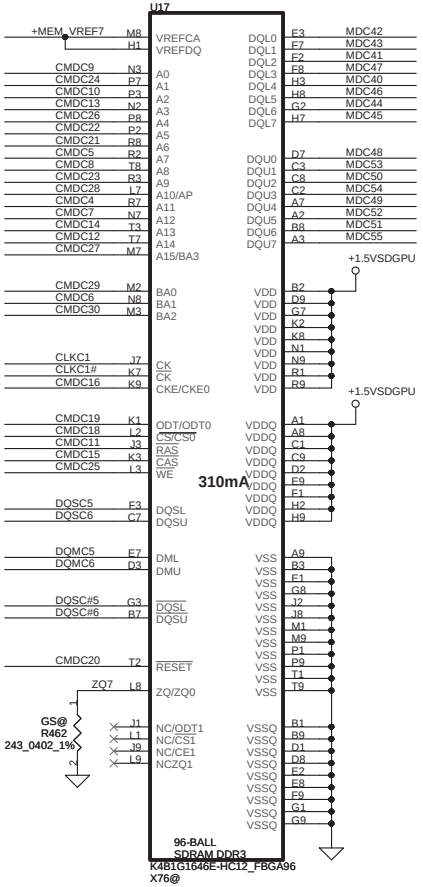
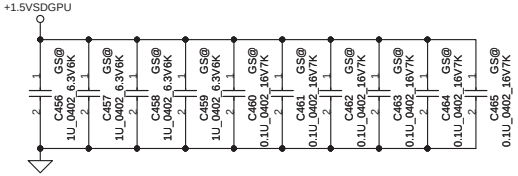
VRAM DDR3 chips (1GB)

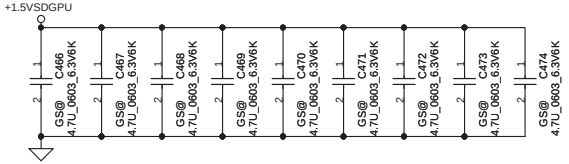
64Mx16 DDR3 *8==>1GB











Mode E Address	Mode C Address	0..31	32..63
CMD3	CMD0	CKE_L	
CMD8	CMD1	A8	A8
CMD2	CMD2	CS0_L#	
CMD21	CMD3	A7	A6
CMD24	CMD4	A2	A1
CMD23	CMD5	A11	A9
CMD26	CMD6	A5	A4
CMD7	CMD7	A0	A12
CMD15	CMD8	CAS*	CAS*
CMD13	CMD9	BA1	A3
CMD4	CMD10	A9	A11
CMD18	CMD11		CS0_H#
CMD29	CMD12	BA0	BA0
CMD27	CMD13	BA2	A15
CMD6	CMD14	A3	BA1
CMD17	CMD15		CS1_H#
CMD19	CMD16		ODT_H
CMD22	CMD17	A4	A5
CMD12	CMD18	A13	A14
CMD28	CMD19	WE*	A10
CMD10	CMD20	A1	A2
CMD25	CMD21	A10	WE*
CMD9	CMD22	A12	A0
CMD1	CMD23	CS1_L#	
CMD11	CMD24	RAS*	RAS*
CMD0	CMD25	ODT_L	
CMD5	CMD26	A6	A7
CMD16	CMD27		CKE_H
CMD20	CMD28	RST	RST
CMD14	CMD29	A14	A13
CMD30	CMD30	A15	BA2
CMD31	Not Available		
		LOW	HIGH

Compal Electronics, Inc.

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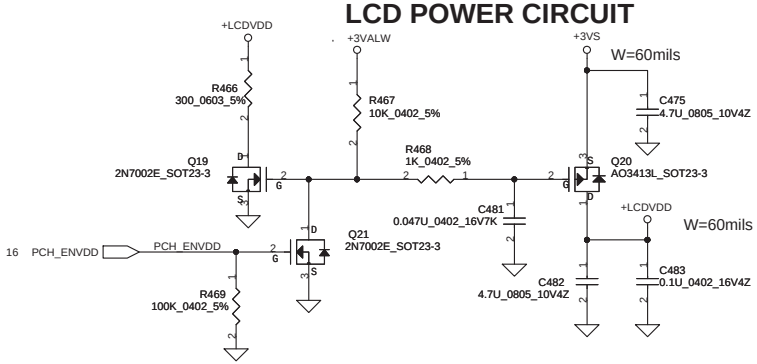
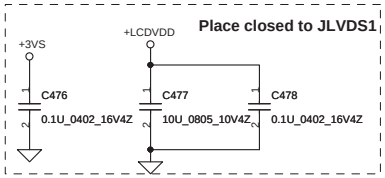
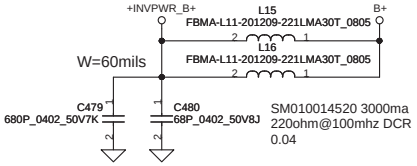
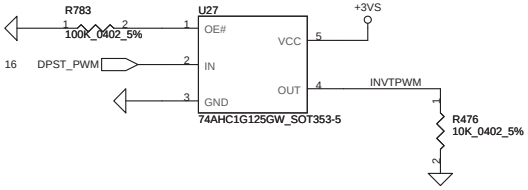
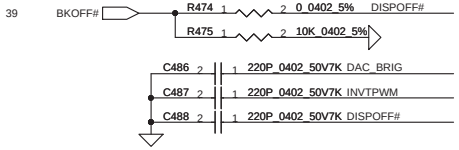
LCD POWER CIRCUIT



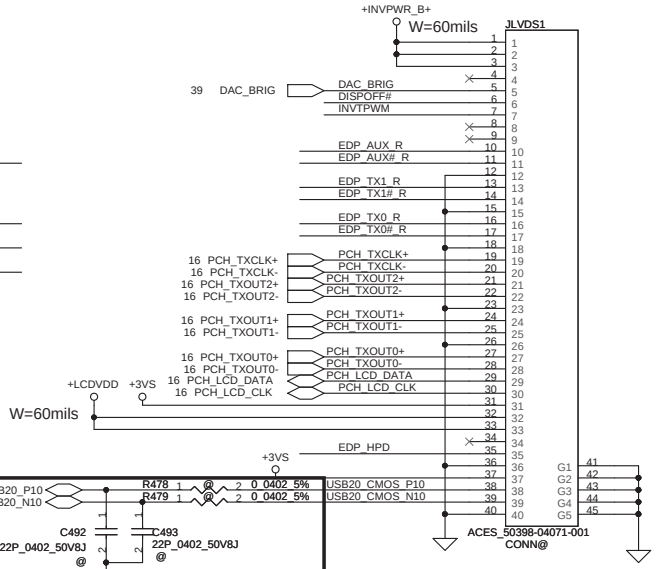




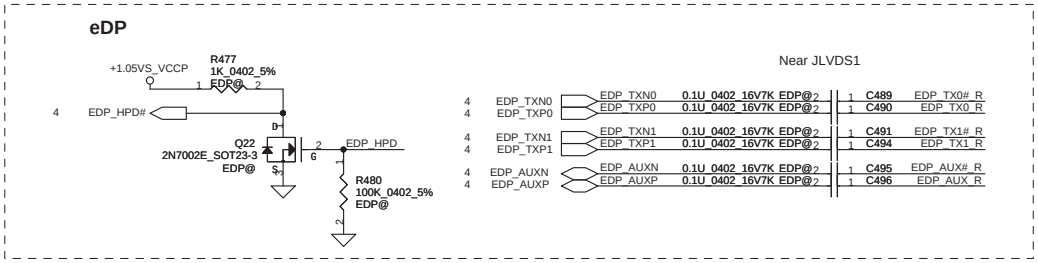




LCD/LED PANEL Conn.



Modify for LVDS Camera USB cancel twist issue



Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

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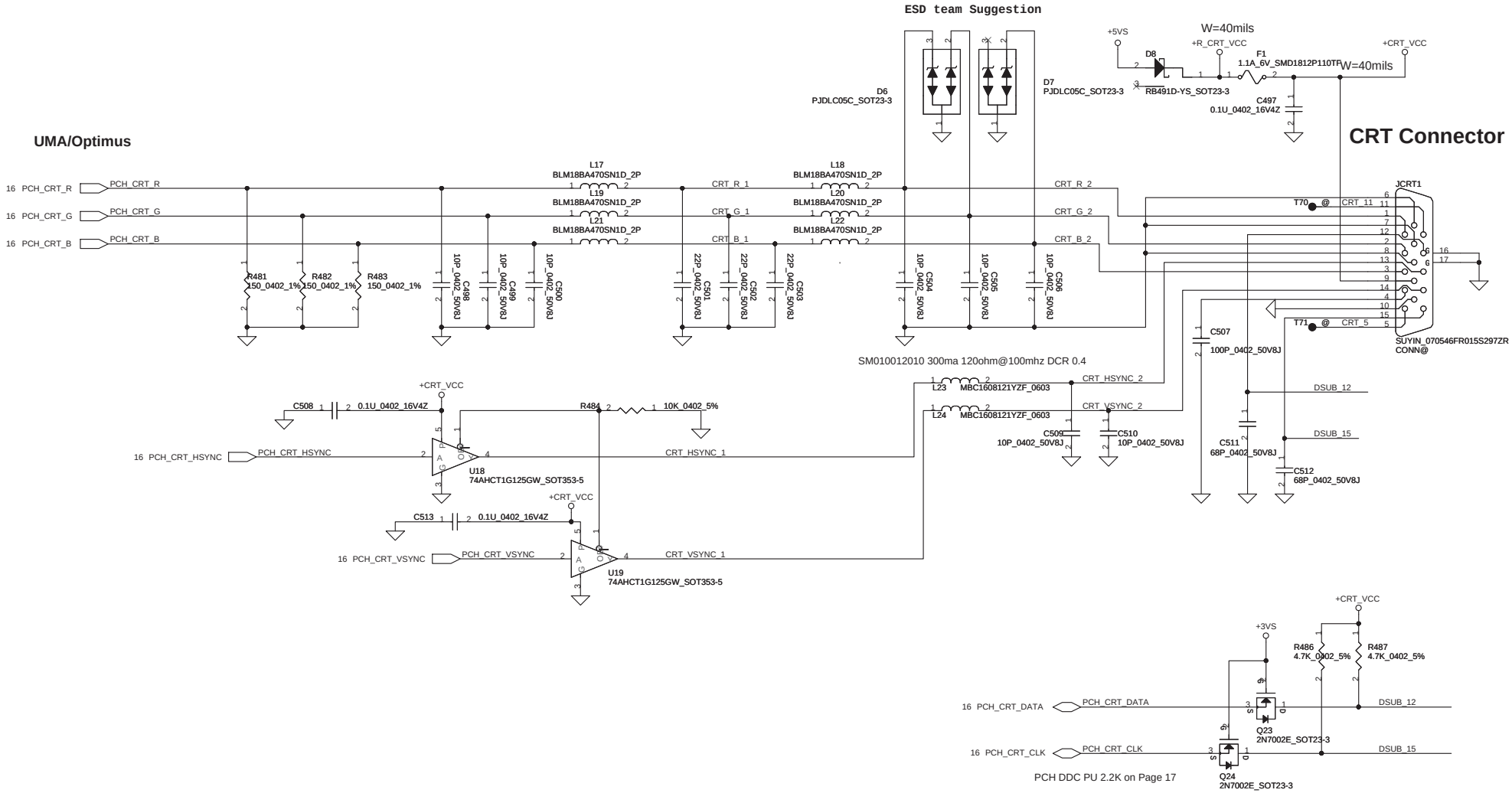

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Compal Electronics, Inc.

Title: SCHEMATIC, MB LA-7231P

Size	Document Number	Rev
Custom	4019BL	B

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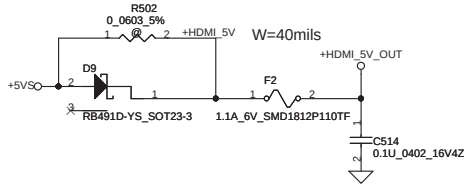
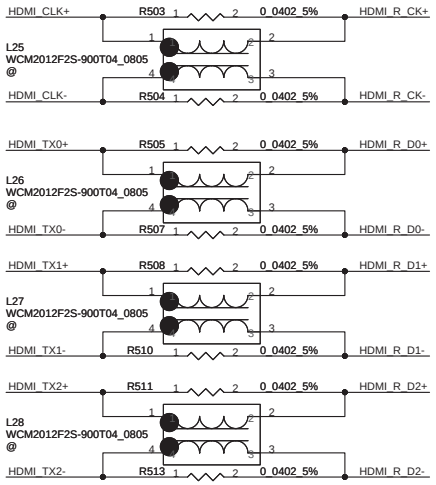
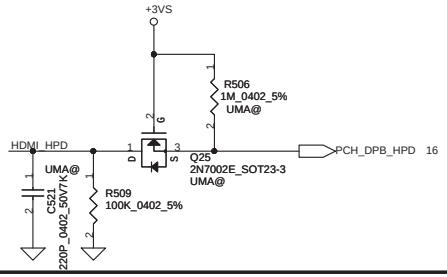
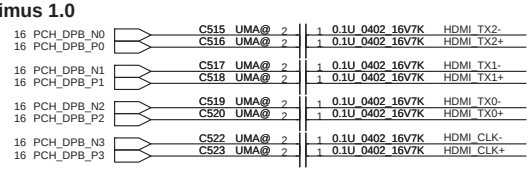


SM070001310 400ma 90ohm@100mhz DCR 0.3

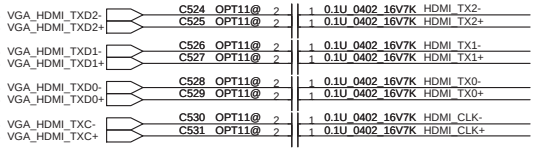


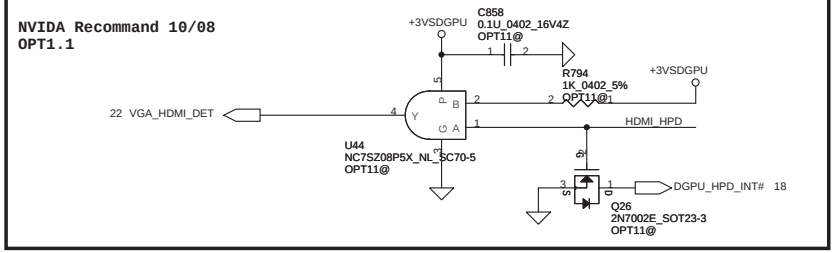


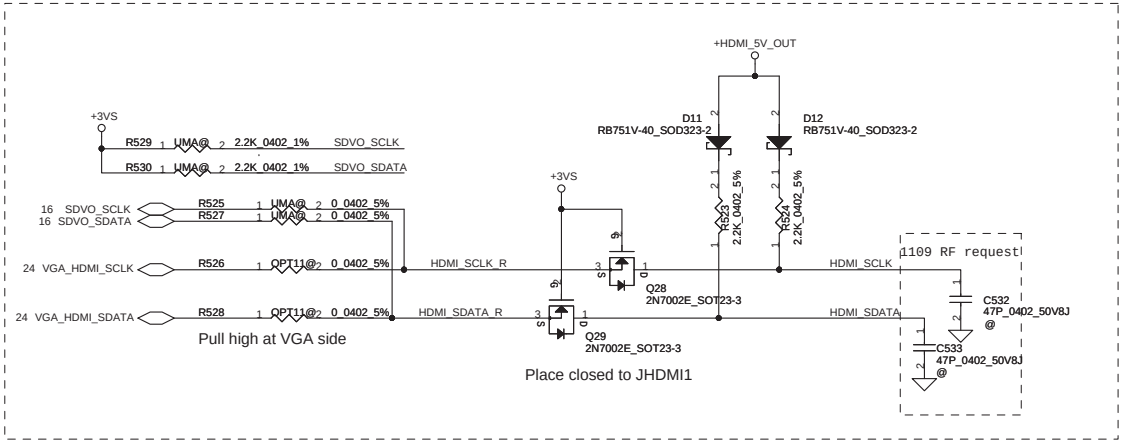
UMA & Optimus 1.0



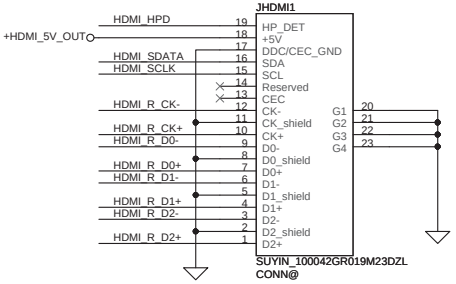
Optimus 1.1

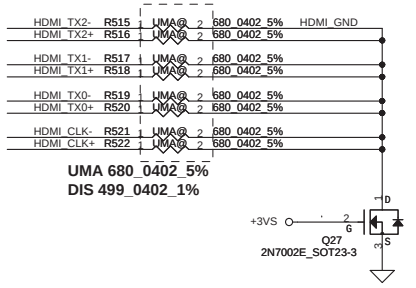




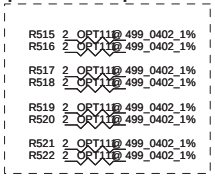


HDMI connector





Optimus 1.1 Option Component



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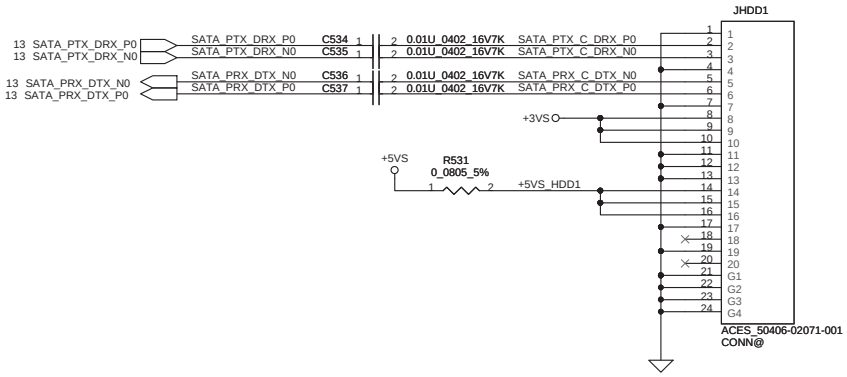
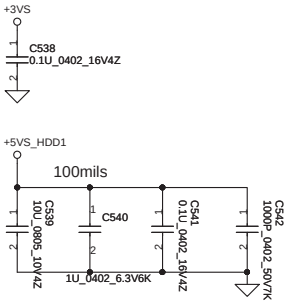
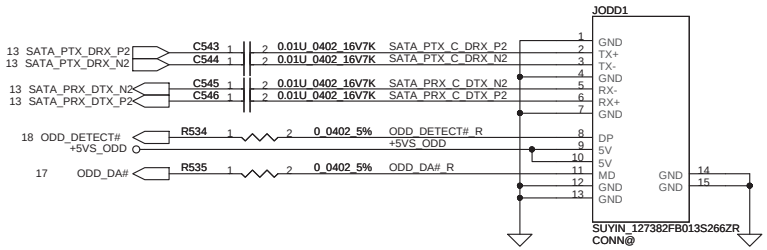
SATA HDD1 Conn.

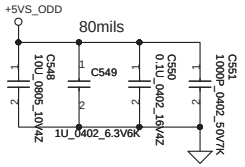
CL 4.0 mm

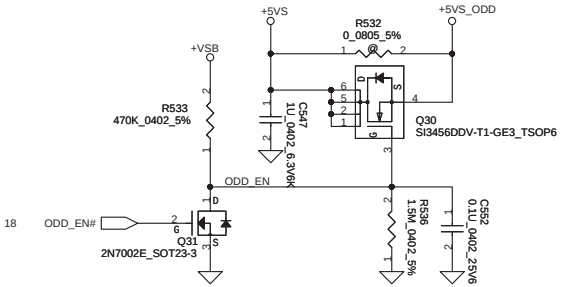




SATA ODD Conn.







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Power On strapping

Pin	Description	Chip Default
LED0	H:Over Clock Enable L:Over Clock Disable*	H
LED1	H:SWR Switch mode regulator Select AR8151 Pin39 * H: switch regulator applied. L: switch regulator isn't applied. AR8152, Pin23 is CLKREQ	AR8151-BL1A applies switch mode regulator.

+3V_LAN — *Check PU/PD on MB side*

R539 @ 4.7K_0402_5% PLT_RST#

R541 4.7K_0402_5% LAN_WAKE#

R544 4.7K_0402_5% LAN_CLKREQ#

Close to lan chip.

Place Close to LAN chip

LAN_MIDI0+	R537 49.9_0402_1%	@	C553 1000P_0402_50V7K		
LAN_MIDI0-	R538 49.9_0402_1%		C554 0.1U_0402_16V4Z		
LAN_MIDI1+	R540 49.9_0402_1%	@	C555 1000P_0402_50V7K		
LAN_MIDI1-	R542 49.9_0402_1%		C556 0.1U_0402_16V4Z		
LAN_MIDI2+	R543 49.9_0402_1%	8151@ / @	C557 1000P_0402_50V7K		
LAN_MIDI2-	R545 49.9_0402_1%	8151@	C558 0.1U_0402_16V4Z	8151@	
LAN_MIDI3+	R546 49.9_0402_1%	8151@ / @	C559 1000P_0402_50V7K		
LAN_MIDI3-	R547 49.9_0402_1%	8151@	C560 0.1U_0402_16V4Z	8151@	

Note 1 : 8152 no mount MDI3+, MDI3-, MDI2-, MDI2+ resister and cap

Note 2 : C553, C555, C557, C559 reserved for EMI.

Place Close to Chip

no overclocking
PD 5.1K

U20 — Atheros 8151-AL1A — LED0,1,2 intel Pull UP

R548 5.1K_0402_5%

LAN_ACT 36
LAN_LINK# 36
R550 0_0402_5% 8152@ LAN_CLKREQ#

LAN_MIDI0- 36
LAN_MIDI0+ 36
LAN_MIDI1- 36
LAN_MIDI1+ 36
LAN_MIDI2- 36
LAN_MIDI2+ 36
LAN_MIDI3- 36
LAN_MIDI3+ 36

R554 2.37K_0402_1% LAN_RBIAS

40mils

+3V_LAN — R557 0_1206_5% — +3VALW_PCH — R555 0_1206_5% — +3VALW

Q37 AO3413L_SOT23-3 @ — PCH_PWR_EN# — PCH_PWR_EN# 20,46

C565 0.1U_0402_16V4Z
C566
C567 10U_0805_10V4Z
C568 10U_0805_10V4Z @
1U_0402_6.3V6K

C565 & C566 Close pin1 < 200mil
C567 & C568 Close pin < 400mil

14 PCIE_PRX_DTX_N1 — PCIE_PRX_DTX_N1 C561 0.1U_0402_16V7K — PCIE_PRX_C_DTX_N1 — TX_N
14 PCIE_PRX_DTX_P1 — PCIE_PRX_DTX_P1 C562 0.1U_0402_16V7K — PCIE_PRX_C_DTX_P1 — TX_P
14 PCIE_PTX_C_DRX_N1 — PCIE_PTX_C_DRX_N1 — RX_N
14 PCIE_PTX_C_DRX_P1 — PCIE_PTX_C_DRX_P1 — RX_P
14 CLK_PCIE_LAN# — CLK_PCIE_LAN# R551 0_0402_5% — CLK_PCIE_LAN#_R — REFCLK_N
14 CLK_PCIE_LAN — CLK_PCIE_LAN R549 0_0402_5% — CLK_PCIE_LAN_R — REFCLK_P
LAN_RST# — PERST#
15,37,44 PCH_PCIE_WAKE# — PCH_PCIE_WAKE# R552 @ 0_0402_5% — LAN_WAKE# — WAKE#
39 EC_PME# — EC_PME# R553 0_0402_5% — SMCLK / SMDATA
TEST_RST / TESTMODE

8152@ C563 0.1U_0402_16V4Z — LAN_XTALO — XTLO
LAN_XTALI — XTLI

14 LAN_CLKREQ# — LAN_CLKREQ# 8151@ R556 0_0402_5% — CLKREQ#

20mils

+1.1_AVDDL ×5 — AVDDL / AVDDL / AVDDL / AVDDL / AVDDL_REG

C569 8151@ 0.1U_0402_16V4Z — Near Pin13
C570 8151@ 0.1U_0402_16V4Z — Near Pin19
C571 8151@ 0.1U_0402_16V4Z — Near Pin31
C572 0.1U_0402_16V4Z — Near Pin34
C573 C574 0.1U_0402_16V4Z — 1U_0402_6.3V6K — Near Pin6

GND — AR8151-BL1A-RL 8151@

RBIAS — VDD33 — LX — VDDCT — DVDDL / DVDDL_REG — AVDDH / AVDDH / AVDDH_REG

+1.7_LX — +1.7_LX
+1.7_VDDCT — C564 0.1U_0402_16V4Z — +1.7_VDDCT

40mils
20mils

+1.1_DVDDL ×2
+2.7_AVDDH_R — 8151@ R738 0_0402_5% — +2.7_AVDDH
+2.7_AVDDH ×3

C575 0.1U_0402_16V4Z — Near Pin9
C576 — 1U_0402_6.3V6K
C577 0.1U_0402_16V4Z — Near Pin22
C578 8151@ 0.1U_0402_16V4Z — Near Pin16
C579 0.1U_0402_16V4Z — Near Pin37
C580 — 1U_0402_6.3V6K
C581 0.1U_0402_16V4Z — Near Pin24

8152 is LED2 Function (NC)

Y4 25MHZ_20PF_7A25000012
LAN_XTALI — C582 33P_0402_50V8J
LAN_XTALO — C583 33P_0402_50V8J

Note: Place Close to LAN chip
L2 DCR< 0.15 ohm
Rate current > 1A

+1.7_VDDCT — C585 1000P_0402_50V7K @ — C586 0.1U_0402_16V4Z — L30 4.7UH_SIA4012-4R7M_20% — C587 10U_0805_10V4Z — +1.7_LX

40mils

Close to Pin40

+3V_LAN — C584 0.1U_0402_16V4Z @ — U21 NC7SZ08P5X_NL_SC70-5

5,17,38,39,44 PLT_RST# — PLT_RST# — LAN_RST#

Pull low 100K at PCH side(P17)

R558 0_0402_5%

Reserve for 8151A/B PERST# leakage issue

	Pin4	Configure R556	Configure C563		Pin23	Configure R550
AR8152	VDDCT_REG		*		CLKREQn	*
AR8151	CLKREQn	*			LED[2]	

Security Classification	Compal Secret Data		
Issued Date	2010/09/28	Deciphered Date	2011/09/28

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Size: Custom | Document Number: 4019BL | Rev: B

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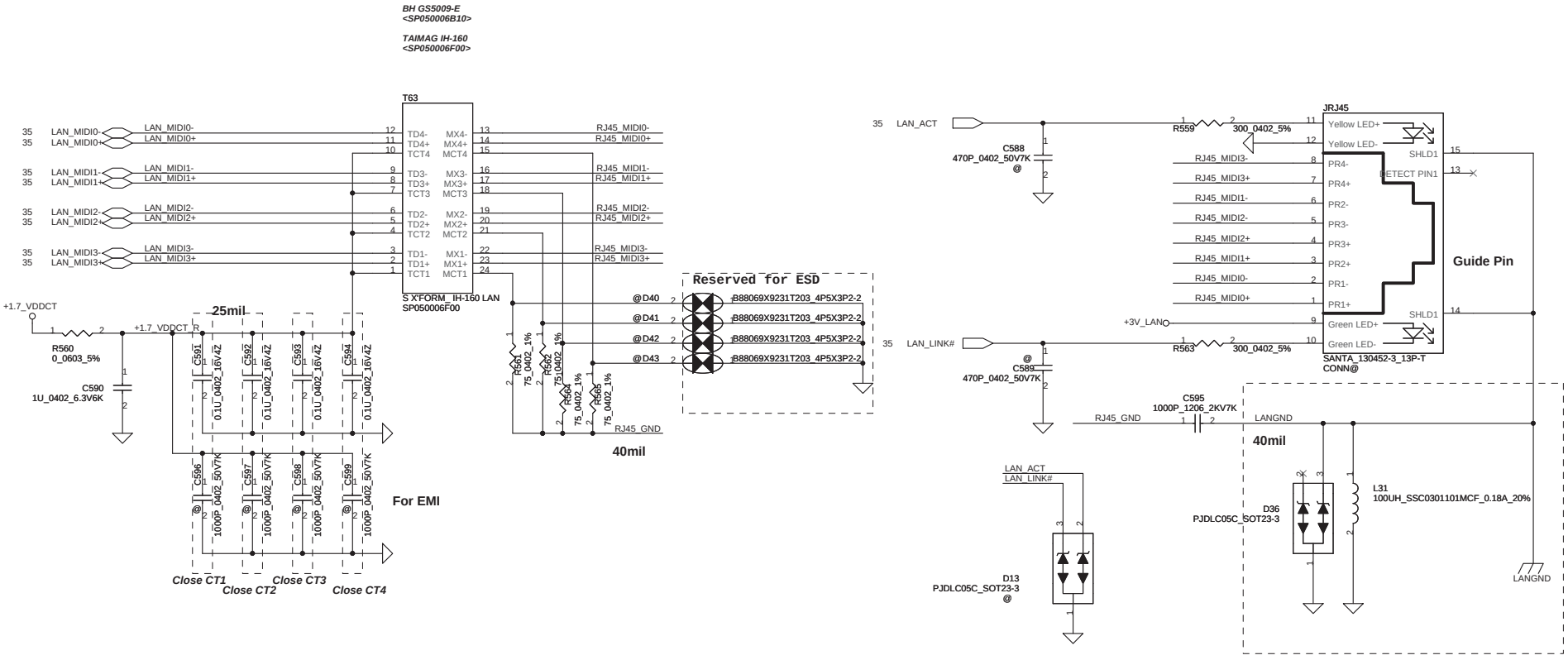

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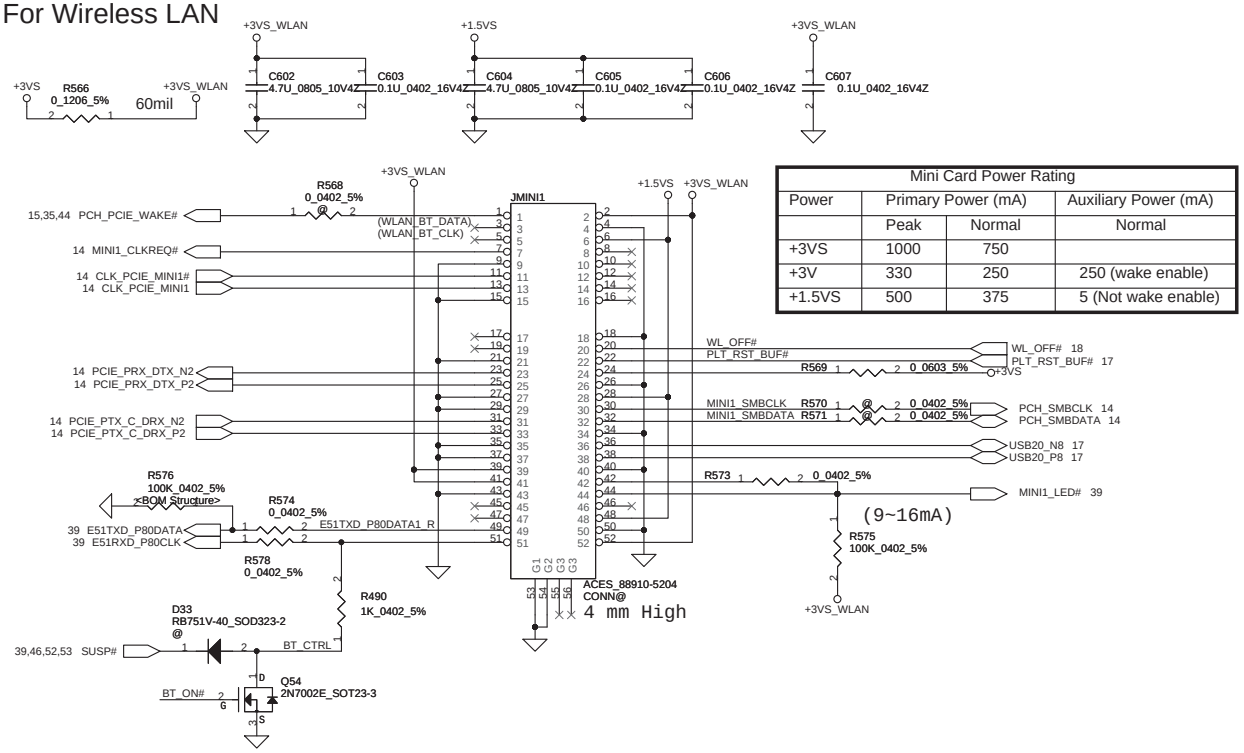
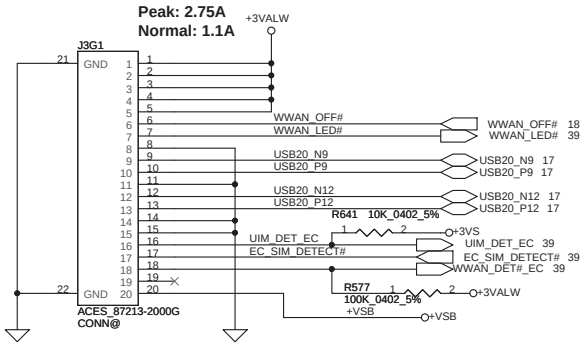
For Wireless LAN

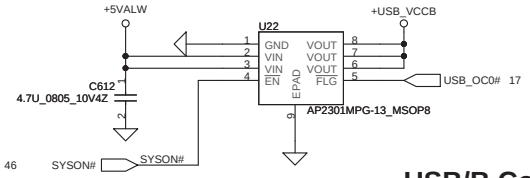


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

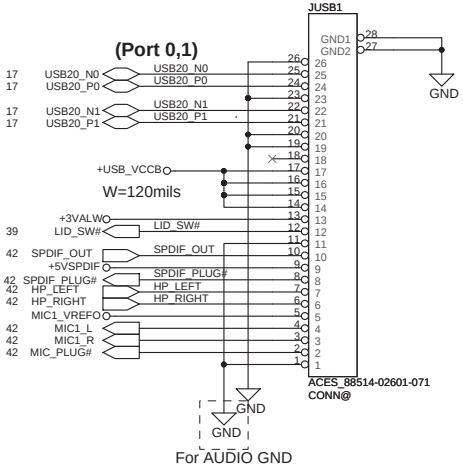
For 3G / GPS

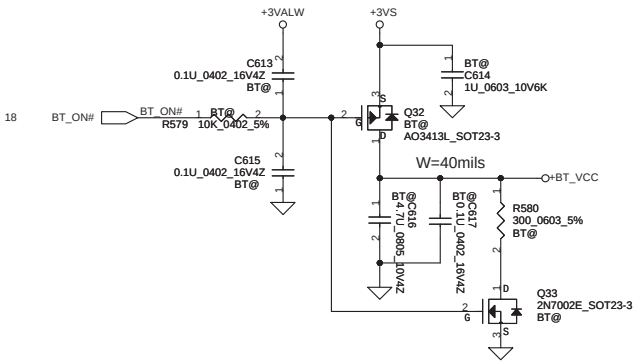
To 3G Module Connect





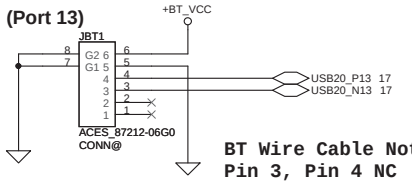
USB/B Conn.





BT Conn.

(Port 13)



BT Wire Cable Note:
Pin 3, Pin 4 NC

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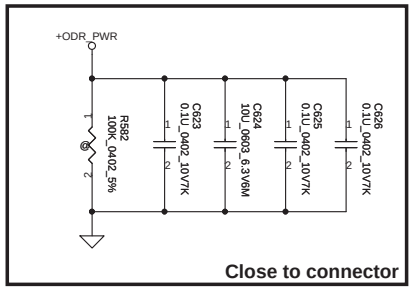
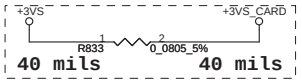
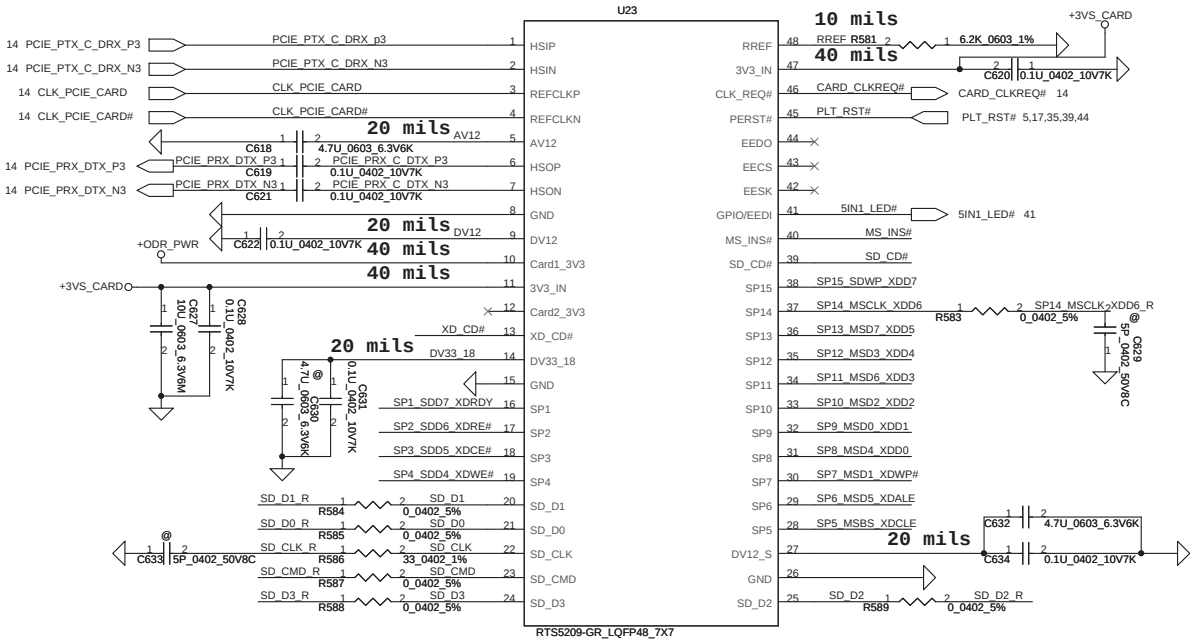
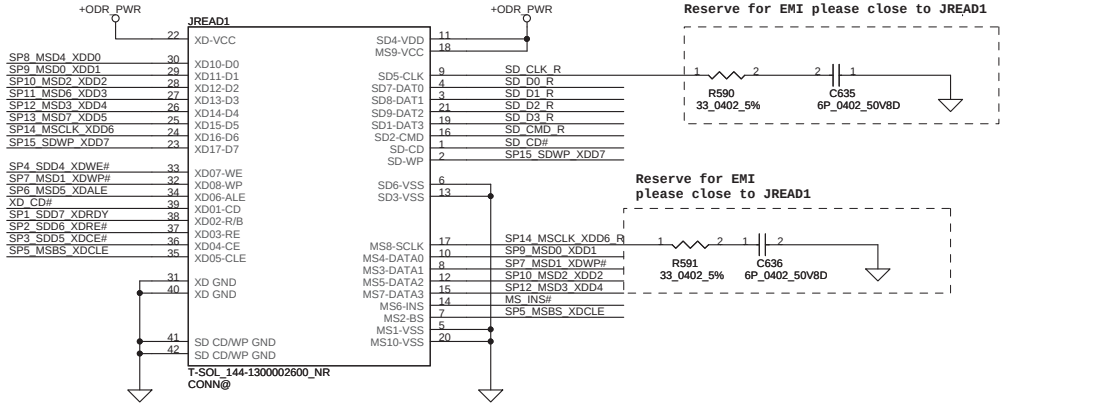
Card Reader





Modify R02, Add 0R between +3VS and +3VS_CARD





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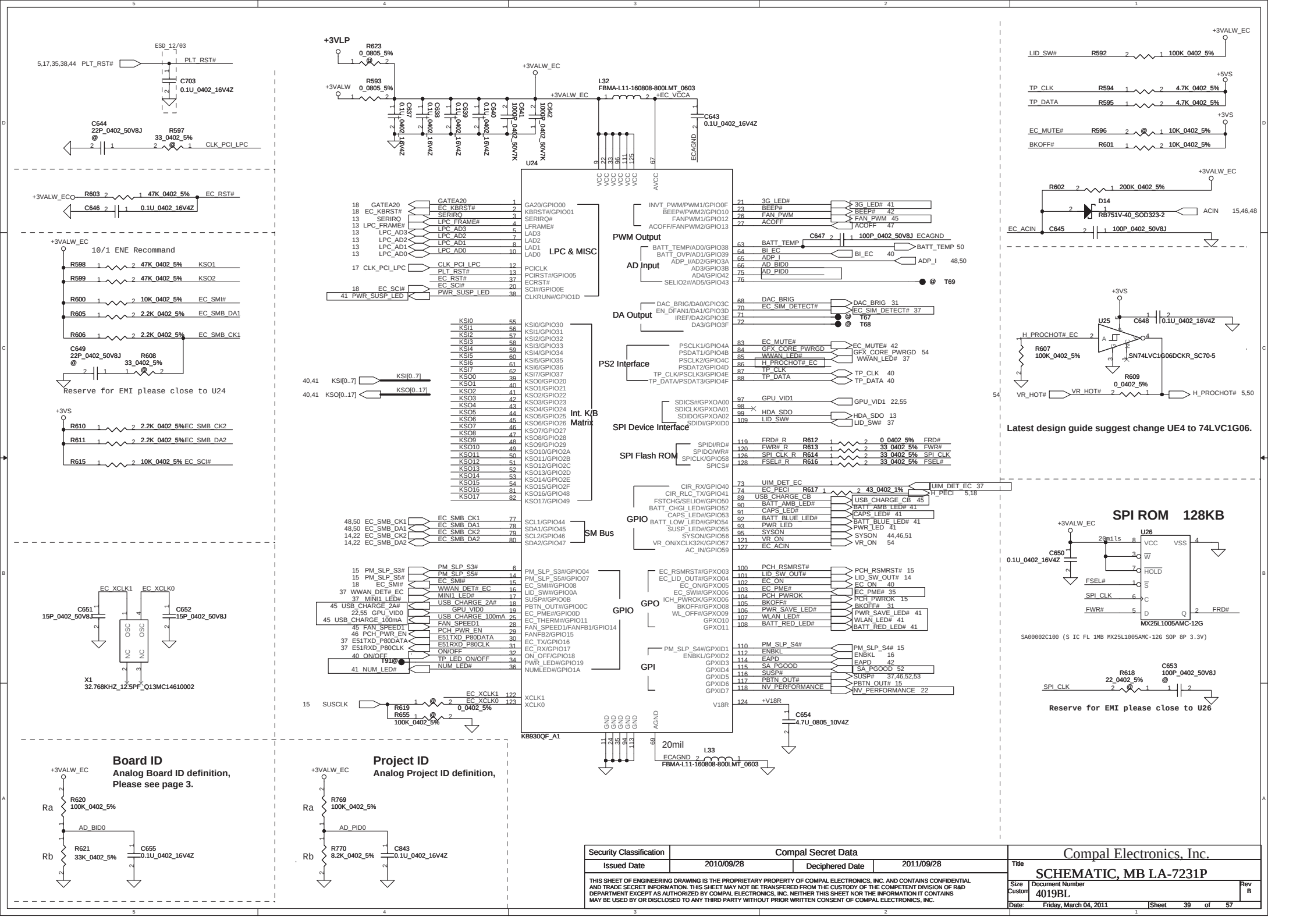
+3VLP
+3VALW_EC
+3VALW
+EC_VCCA
U24
KB930QF_A1
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
10/1 ENE Recommand
Reserve for EMI please close to U24
Board ID
Analog Board ID definition,
Please see page 3.
Project ID
Analog Project ID definition,
Latest design guide suggest change UE4 to 74LVC1G06.
SPI ROM 128KB
SA00002C100 (S IC FL 1MB MX25L1005AMC-12G SOP 8P 3.3V)
Reserve for EMI please close to U26
Security Classification
Compal Secret Data
Issued Date
2010/09/28
Deciphered Date
2011/09/28
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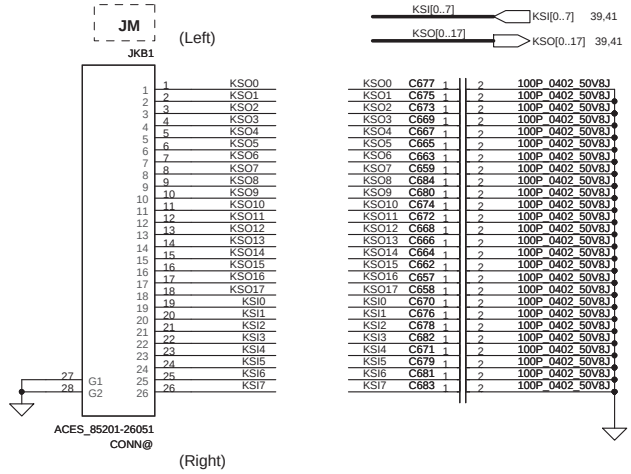
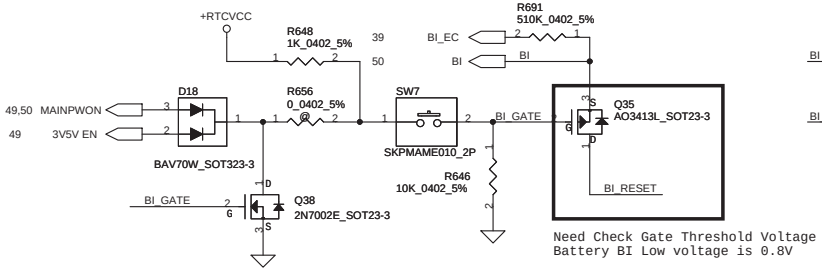
57

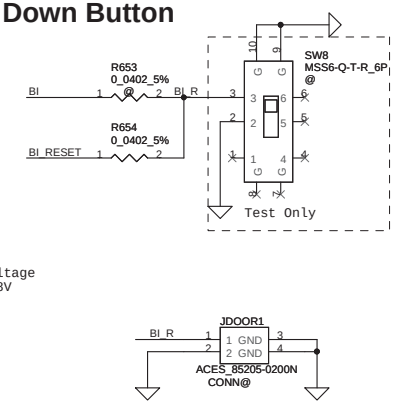
INT_KBD Conn.



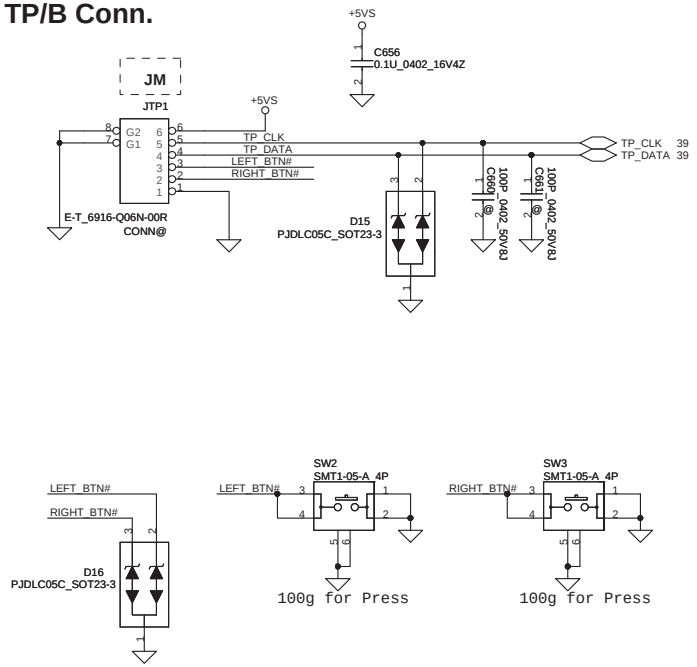
Reset Button



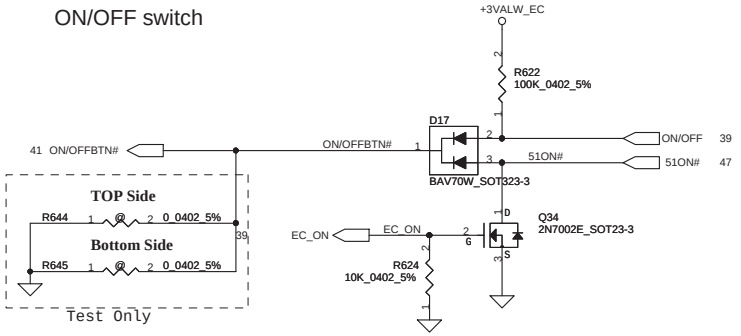
D-Door Battery Power Down Button



To TP/B Conn.



Power Button



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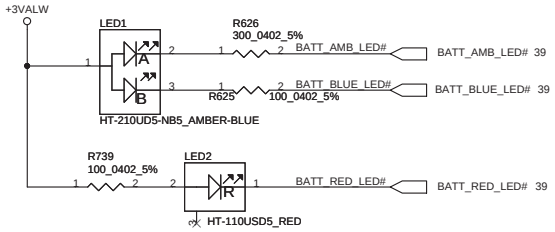
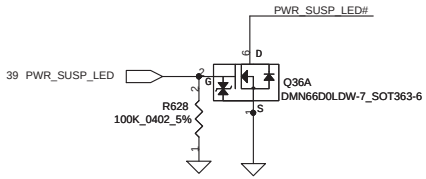
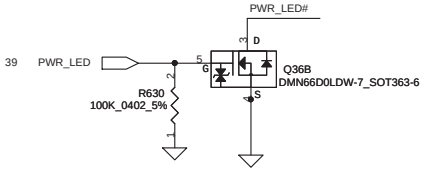
Battery LED

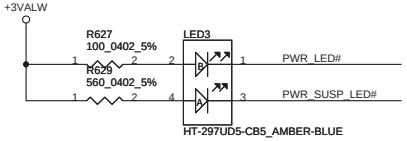
Side View LED with Blue/Amber/Red Color



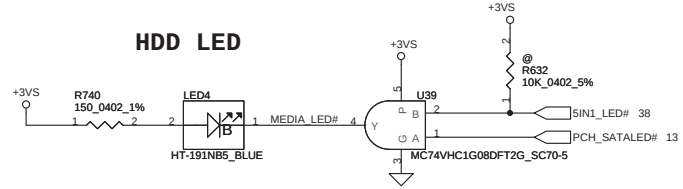




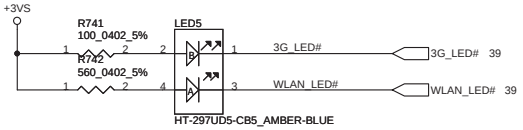
Power LED



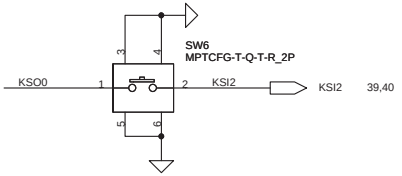
HDD LED



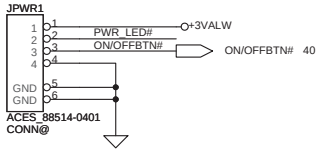
3G/Wireless LED



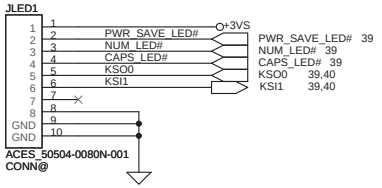
Battery Indicator BTN



PWR/B



FUN Board



	KSO0
KSI1	PWR SAVE BTN#
KSI2	Battery ID BTN#

LED Status	Power/SUS		Battery		3G/WLAN		BlueTooth	ACIN
	ON	SUS	Full	Charge	3G	WLAN		
	Blue	Amber	Blue	Amber	Blue	Amber		

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SM010014520 3000ma 220ohm@100mhz DCR 0.04

+5VS — L34 FBMA-L11-201209-221LMA30T_0805 — L35 FBMA-L11-201209-221LMA30T_0805 @ — +5VAMP — C685 0.1U_0402_16V4Z — C686 0.1U_0402_16V4Z — 60mil — U28 G9191-475T1U_SOT23-5 @ (IN, GND, SHDN, OUT, BYP) — 40mil — +VDDA 4.75V — C687 0.01U_0402_16V7K @ — R633 0_0805_5%

(output = 300 mA)

Modify R02
Add R834 between +3VS and +3VS_Codec.
change power from +3VS to +3VS_CODEC.

+3VS — R834 0_0805_5% — +3VS_CODEC

40mils — 40mils

+3VS_CODEC — C688 10U_0805_10V4Z — C689 0.1U_0402_16V4Z — C690 0.1U_0402_16V4Z

+3VS_CODEC — C693 1U_0603_10V6K — C694 0.1U_0402_16V4Z

+3VS_CODEC — C700 10U_0805_10V4Z — C701 0.1U_0402_16V4Z

+5VAMP — R790 100K_0402_5% — Q67 AO3413L_SOT23-3 — +5VSPDIF — SPDIF_PLUG# — R789 100K_0402_5% — Q66A DMN66D0LDW-7_SOT363-6 — Q66B DMN66D0LDW-7_SOT363-6 — HP_PLUG# — SPDIF_PLUG# 37

+VDDA — R635 0_1206_5% — C692 10U_0805_10V4Z — C691 0.1U_0402_16V4Z

Layout Note:Path from +5VS to LPWR_5.0
RPWR_5.0 must be very low
resistance (<0.01 ohms)

+VDDA_R — C695 0.1U_0402_16V4Z — C696 0.1U_0402_16V4Z — C697 0.1U_0402_16V4Z — C698 10U_0805_10V4Z — C699 10U_0805_10V4Z

Please bypass caps very close to device.

U29 — CX20584-21Z_QFN48_7X7

VAUX_3.3 — VDD_IO — DVDD_3.3 — AVDD_HP — AVDD_5V — LPWR5.0 — RPWR5.0 — CLASSDREF

37 HP_LEFT — HP_LEFT — PORTA_L
37 HP_RIGHT — HP_RIGHT — PORTA_R
PORTD_L
PORTD_R
PORTE_L
PORTE_R
PORTF_L
PORTF_R
FLY_P — C702 1U_0603_10V6K — FLY_N
37 MIC1_L — MIC1_L — C704 4.7U_0603_6.3V6K — PORTC_L
37 MIC1_R — MIC1_R — C705 4.7U_0603_6.3V6K — PORTC_R
MIC1_VREFO — C_BIAS
MONO_IN — PCBEEP
39 EC_MUTE# — EC_MUTE# — R732 0_0402_5% — EXT_MUTE#
+3VS — R472 5.1K_0402_1% — HP_PLUG# — R650 39.2K_0402_1% — 37 MIC_PLUG# — R649 10K_0402_1% — SENSE_A — R488 5.1K_0402_1% — SENSE_B — +3VS — SENSE A / SENSE B
39 EAPD — 0_0402_5% — R651 — GPIO0/EAPD#
37 SPDIF_OUT — SPDIFO
AVEE — C713 10U_0805_10V4Z — C714 0.1U_0402_16V4Z — AVEE
EP_GND

EAPD active low
0=power down ex AMP
1=power up ex AMP

SPK_OUT_L+ — SPKL+ L41 FBMA-L11-201209-221LMA30T_0805 — C796 1000P_0402_50V7K — SPKL+_L 43
SPK_OUT_L- — SPKL- L42 FBMA-L11-201209-221LMA30T_0805 — C797 1000P_0402_50V7K — SPKL-_L 43
SPK_OUT_R+ — SPKR+ L43 FBMA-L11-201209-221LMA30T_0805 — C798 1000P_0402_50V7K — SPKR+_L 43
SPK_OUT_R- — SPKR- L44 FBMA-L11-201209-221LMA30T_0805 — C799 1000P_0402_50V7K — SPKR-_L 43

40mils — Internal SPEAKER

PORTB_L
PORTB_R
B_BIAS
SDATA_IN — HDA_SDIN0_AUDIO — R730 33_0402_5% — HDA_SDIN0 13
SDATA_OUT — HDA_SDOUT_AUDIO — @C800 22P_0402_50V8J — HDA_SDOUT_AUDIO 13
SYNC — HDA_SYNC_AUDIO — HDA_SYNC_AUDIO 13
RESET# — HDA_RST_AUDIO# — @C802 22P_0402_50V8J — HDA_RST_AUDIO# 13
BIT_CLK — HDA_BITCLK_AUDIO_R — @C803 22P_0402_50V8J — R642 0_0402_5% For EMI — HDA_BITCLK_AUDIO 13

DMIC_3/4
DMIC_CLK0 — 90.9_0402_1% — R647 — DMIC_CLK 43
DMIC_1/2 — DMIC_DATA — DMIC_DATA 43

GPIO1/SPK_MUTE# / GPIO2/SPDIF2 — R733 @ 0_0402_5% — EC_MUTE#

FILT_1.8 — FILT_1.8V
FILT_1.65 — FILT_1.65V
AVDD_3.3 — LDO_OUT_3.3V

FILT_1.8V — R652 @ 10K_0402_5% — C709 10U_0805_10V4Z — C710 0.1U_0402_16V4Z
FILT_1.65V — C711 0.1U_0402_16V4Z — C712 1U_0402_6.3V6K

LDO_OUT_3.3V — C715 10U_0805_10V4Z — C716 0.1U_0402_16V4Z

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

39 BEEP# — D34 RB751V-40_SOD323-2 — C801 0.1U_0402_16V4Z — MONO_IN
13 HDA_SPKR — D35 RB751V-40_SOD323-2 — R731 10K_0402_5%

C804 0.1U_0402_16V4Z @
C806 0.1U_0402_16V4Z @
C808 0.1U_0402_16V4Z @

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Issued Date	2010/09/28	Deciphered Date	2011/09/28

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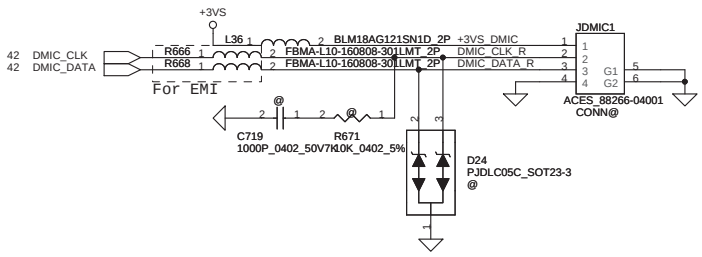
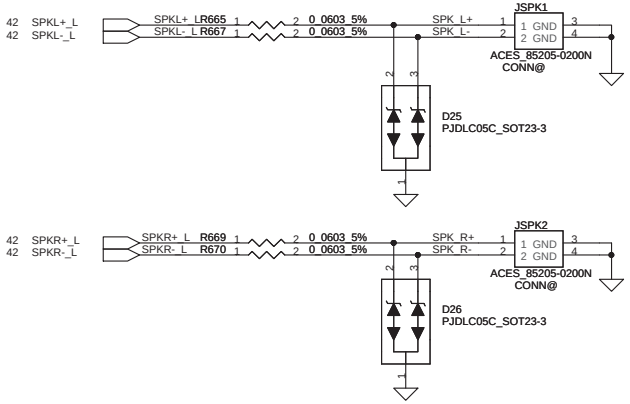
Digital MIC CONN



Int. Speaker Conn.



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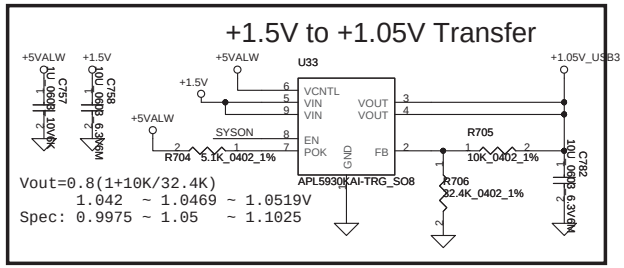

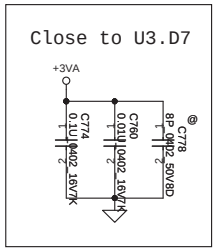

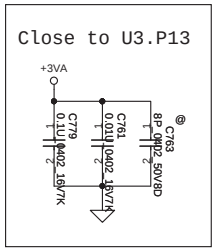

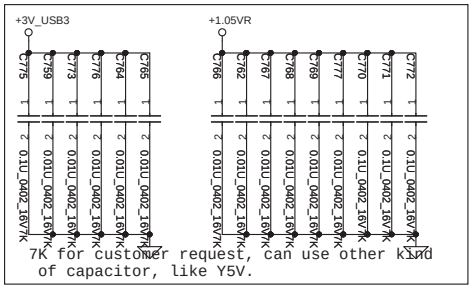

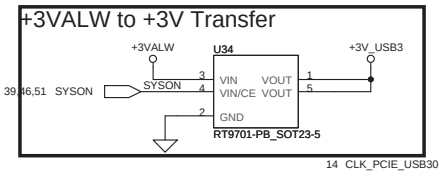

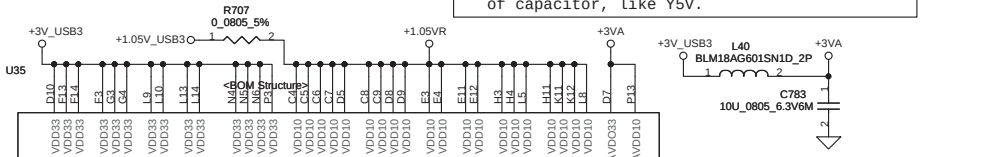

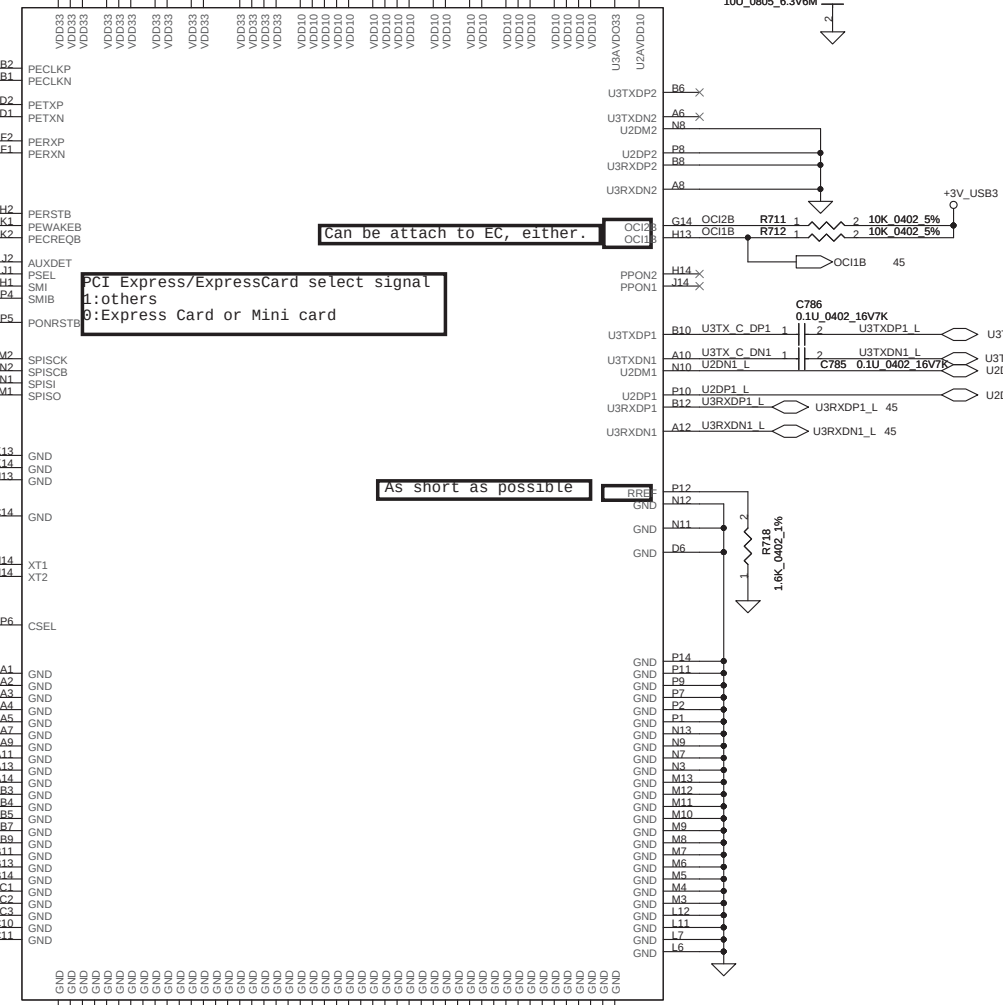

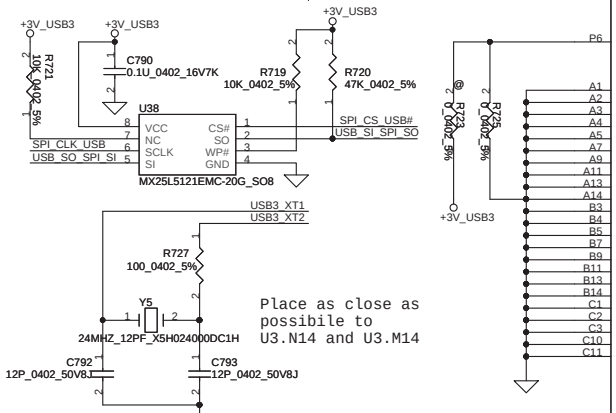

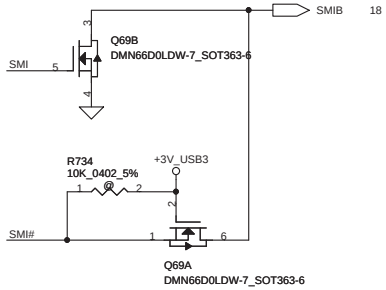

Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

P/N: SA000048H10
(S IC UPD720200AF1-DAP-A FBGA 176P USB3.0)

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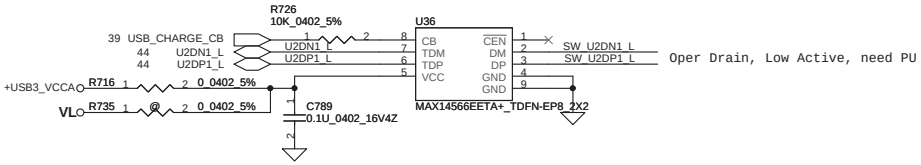
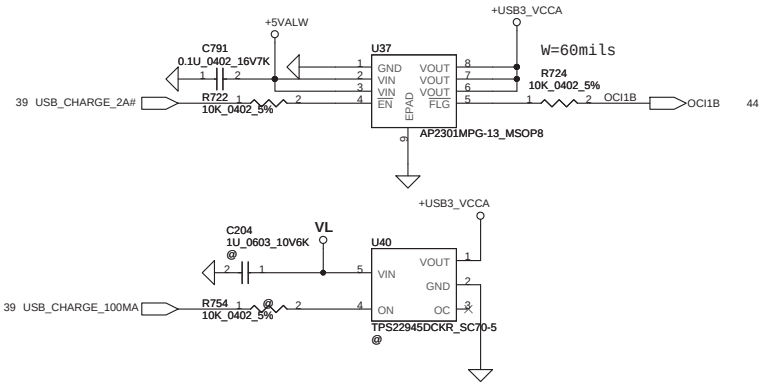
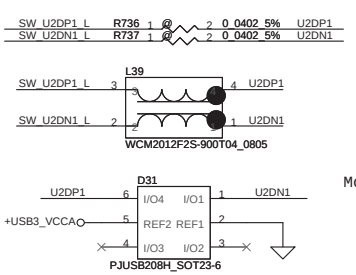
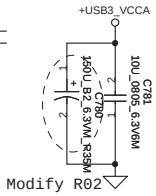
USB Host Charger



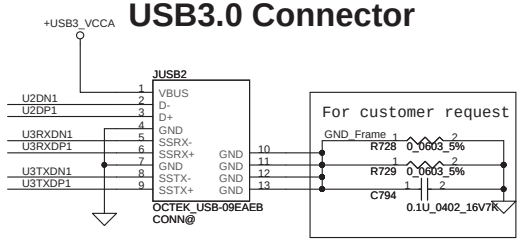
CB=0	Auto detection charger identification active
CB=1	Connect DP/DM to TDP/TDM

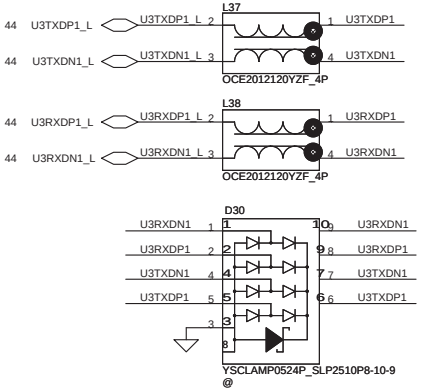




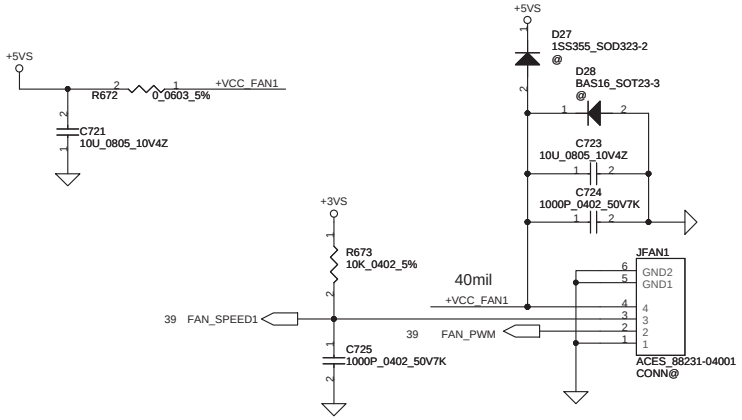


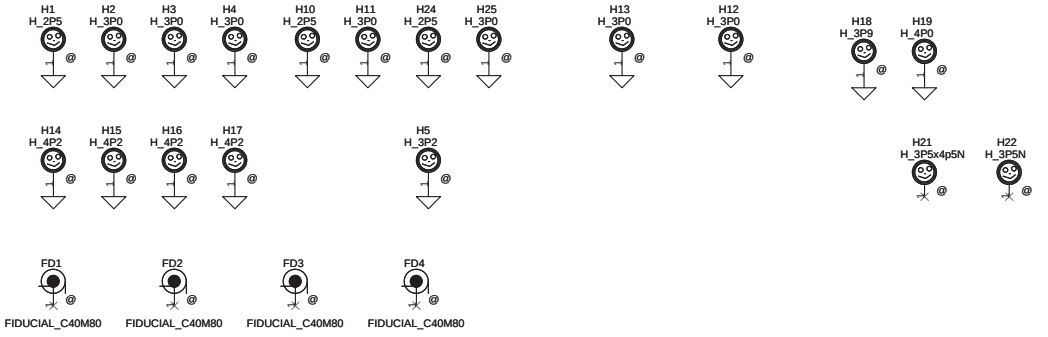
USB3.0 Connector





FAN1 Conn





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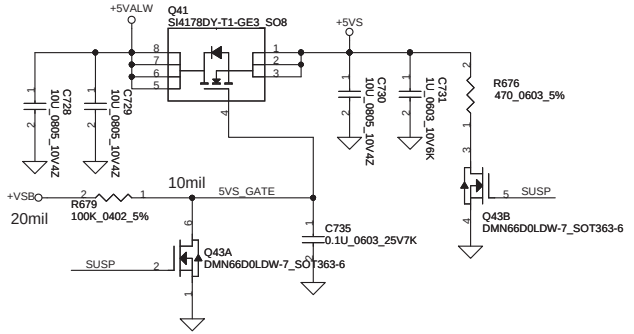
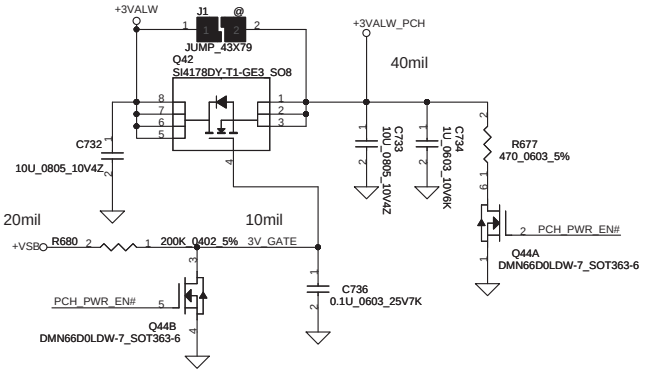
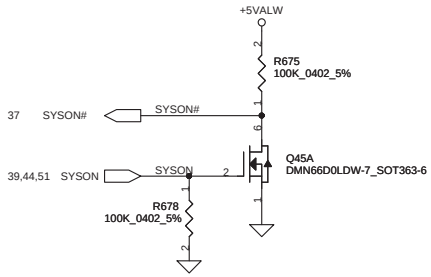
+5VALW TO +5VS

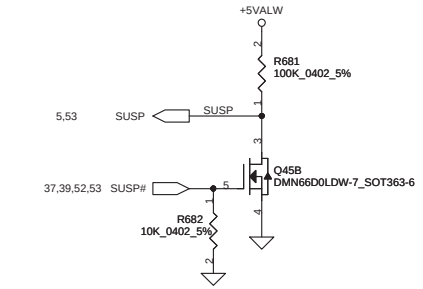


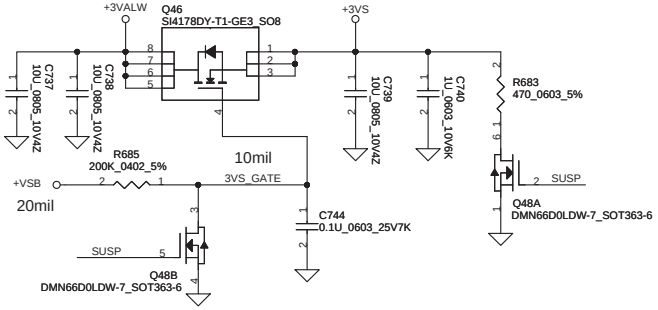
+3VALW TO +3VALW(PCH AUX Power)

Short J5 for PCH VCCSUS3.3

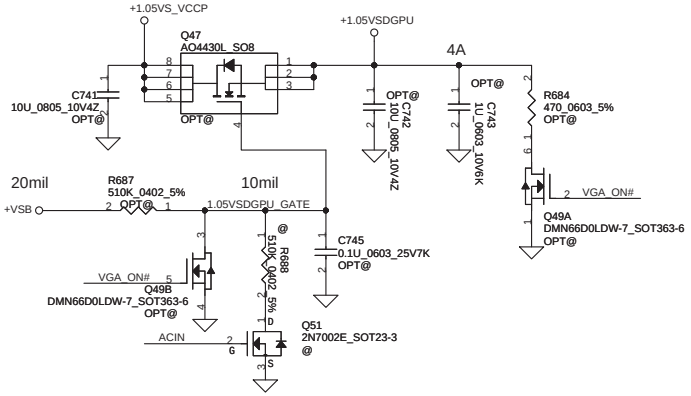


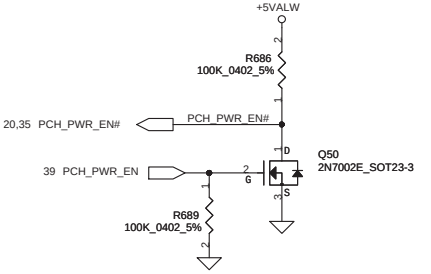




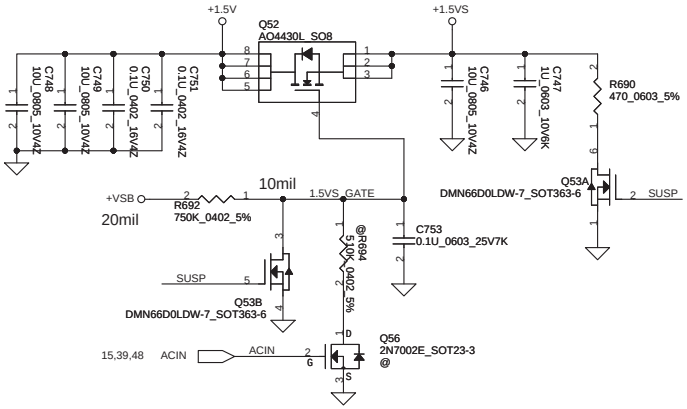


+1.05VS_VCCP to +1.05VSDGPU for GPU

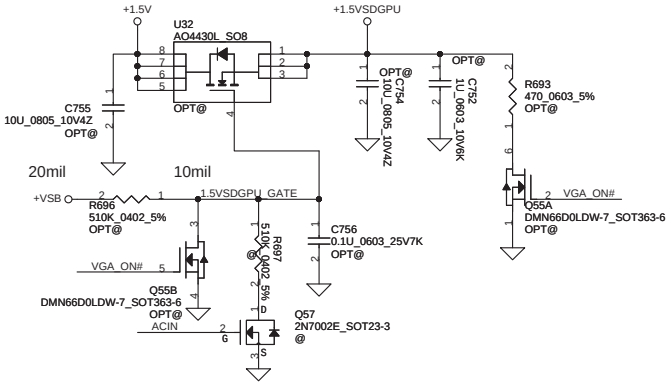


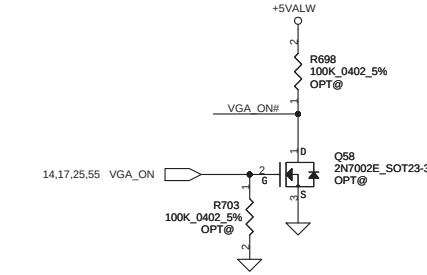


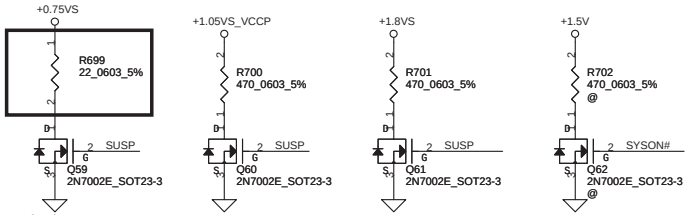
+1.5V to +1.5VS



+1.5V to +1.5VSDGPU for GPU







2009/08/14
CP_S3PowerReduction
WhitePaper_Rev0.9
0.75VS speed up discharge

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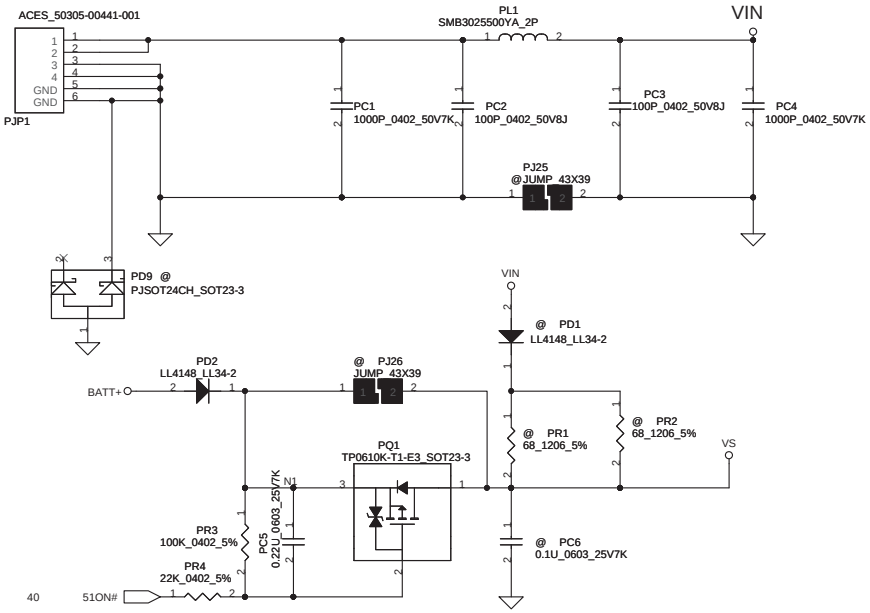

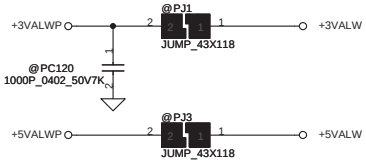

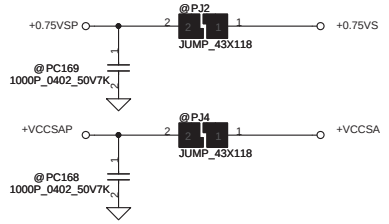

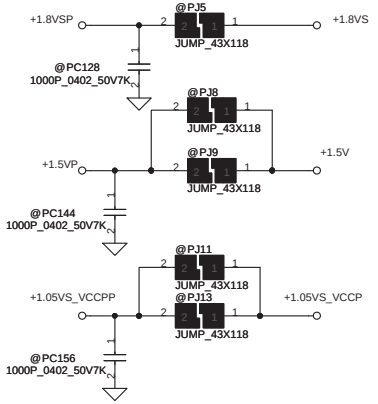

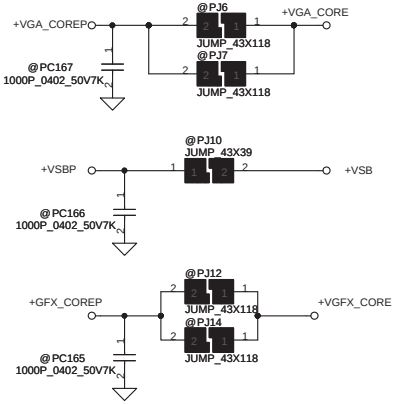

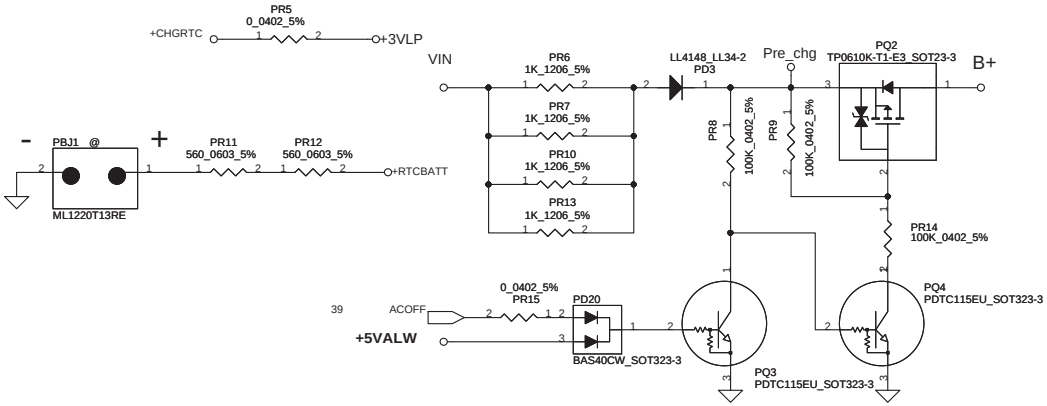

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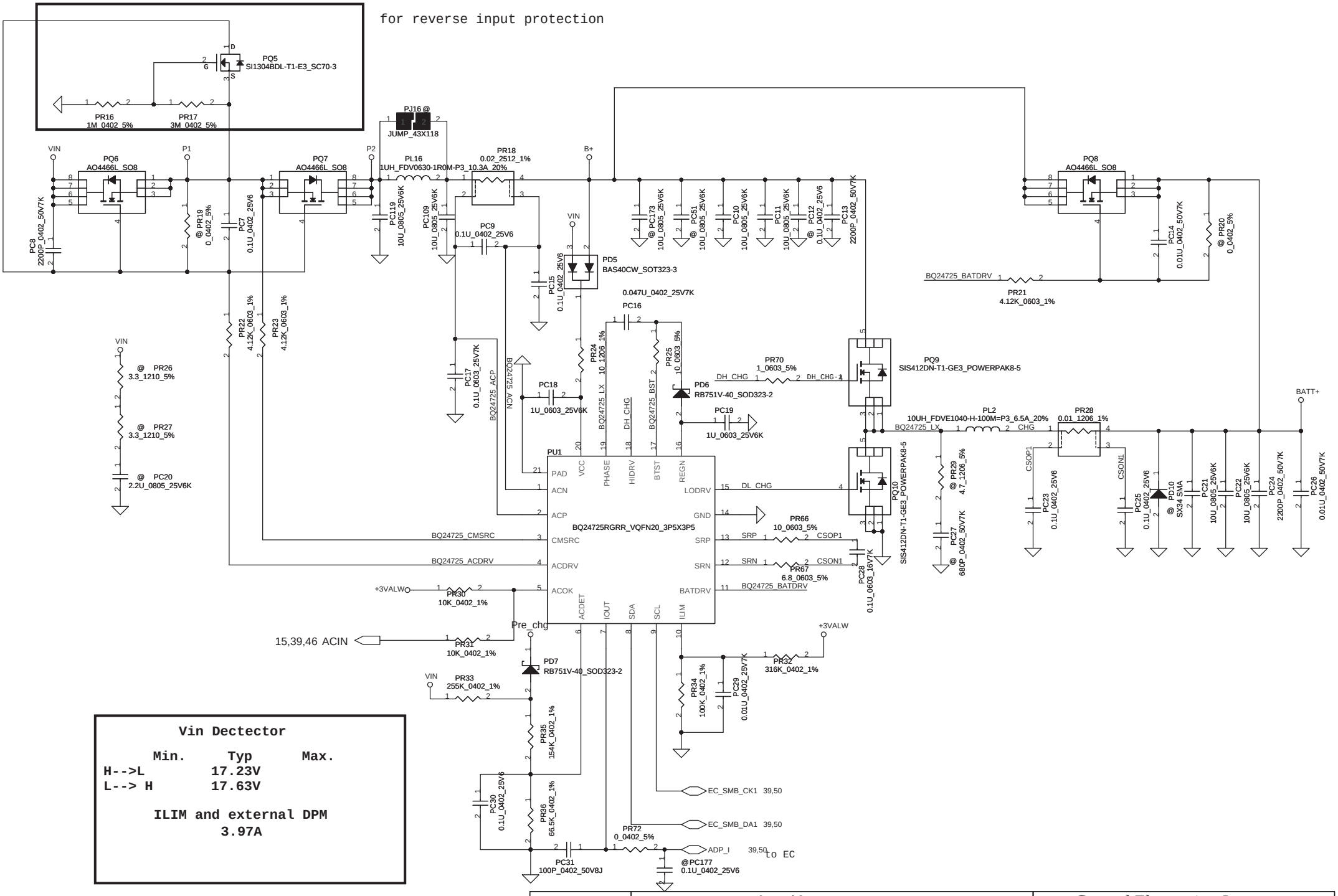

Vin Dectector

	Min.	Typ	Max.
H-->L		17.23V	
L--> H		17.63V	

ILIM and external DPM
3.97A

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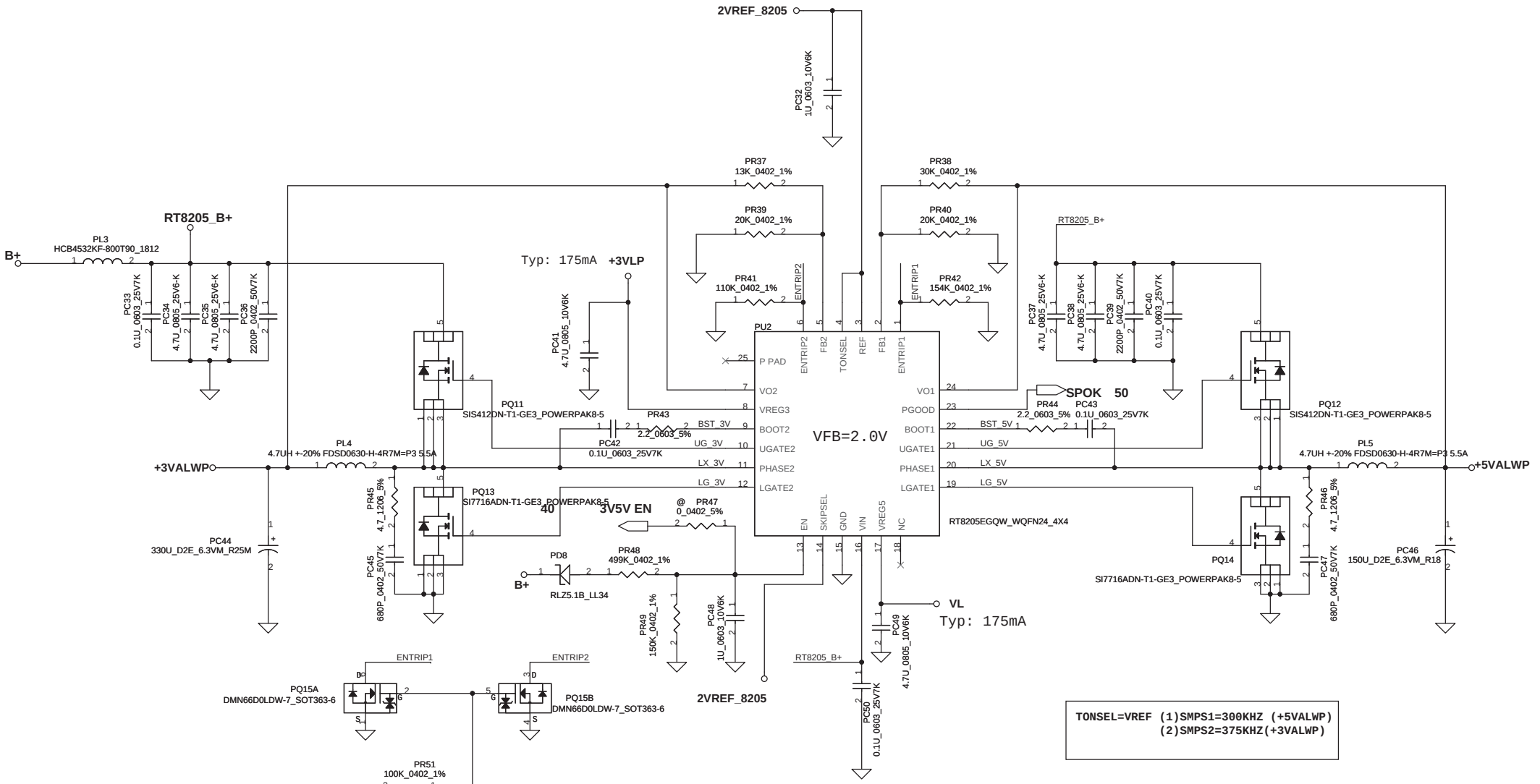

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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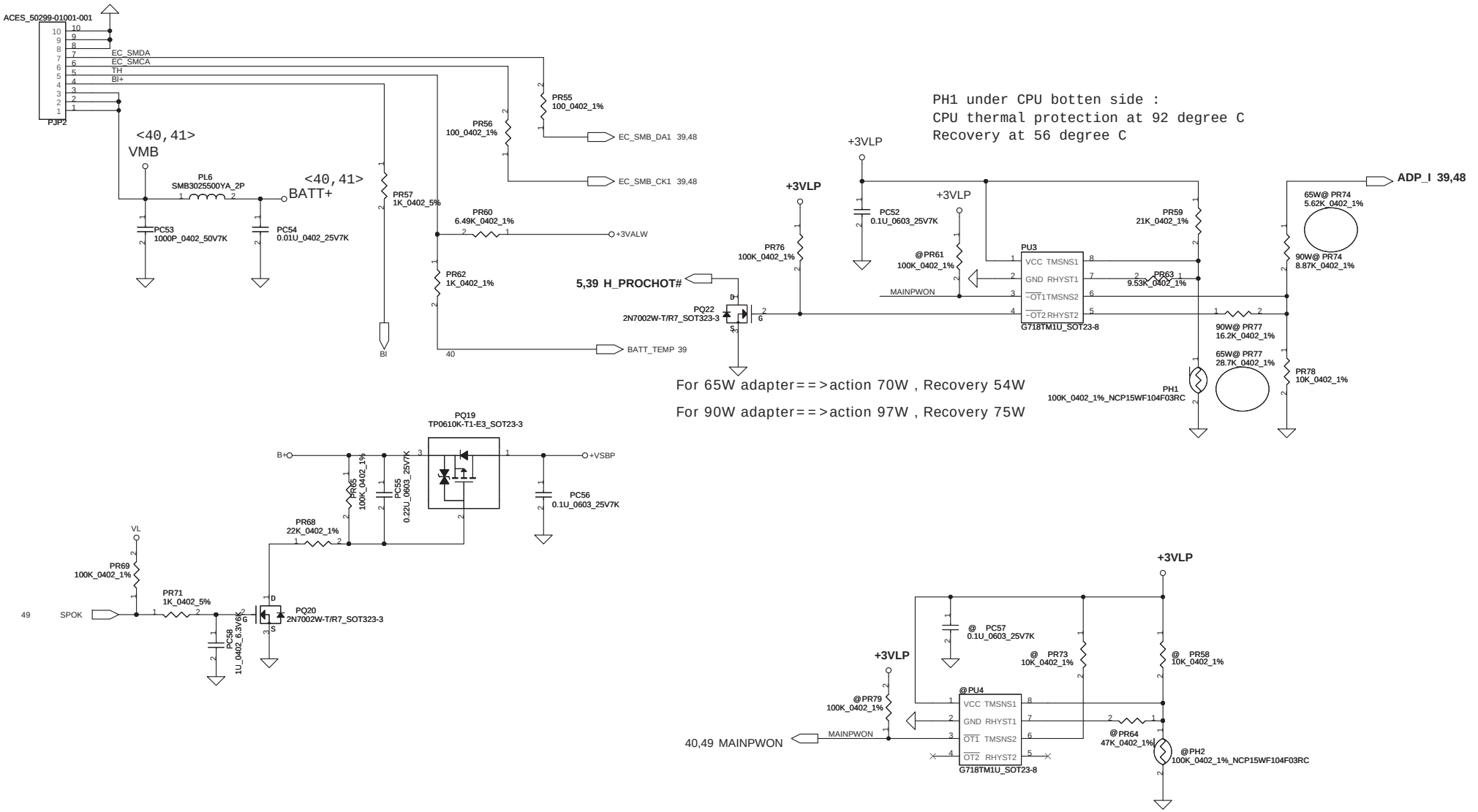

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Issued Date	2010/01/25	Deciphered Date	2010/12/31

Compal Electronics, Inc.

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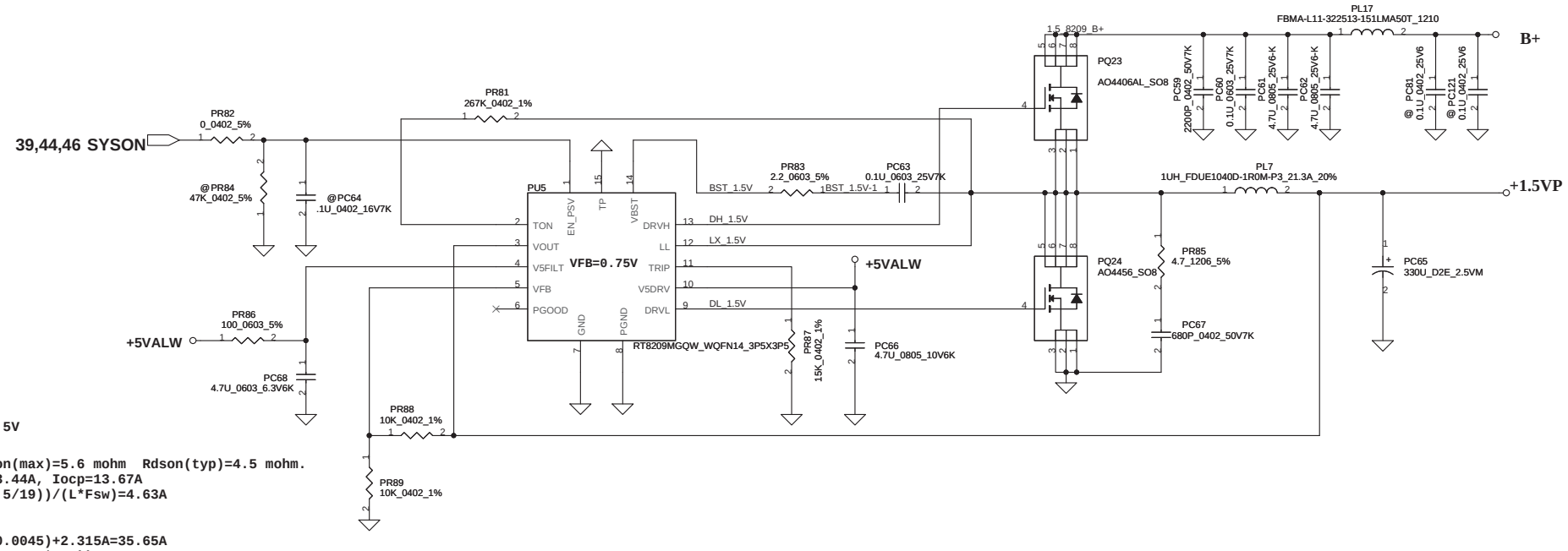

<Vo=1.5V> VFB=0.75V
V=0.75*(1+10K/10K)=1.5V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=19.53A, Imax=23.44A, Iocp=13.67A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.63A
=>1/2Delta I=2.315A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+2.315A=35.65A
Iocpmin=((15K*9uA)/(0.0056*1.3))+2.315A=23.06A
Iocp=23.06A~35.65A

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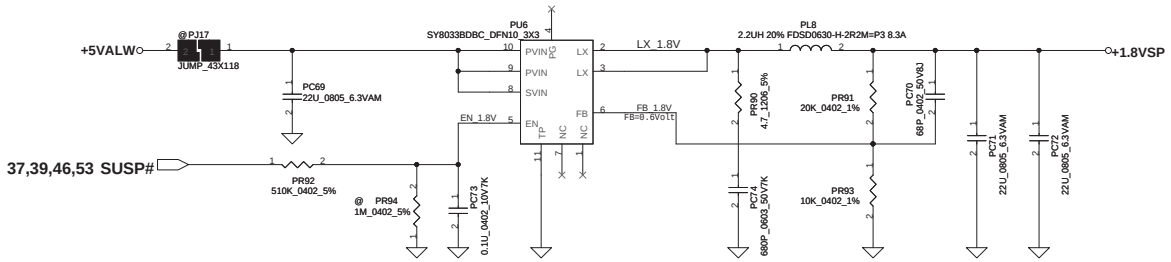
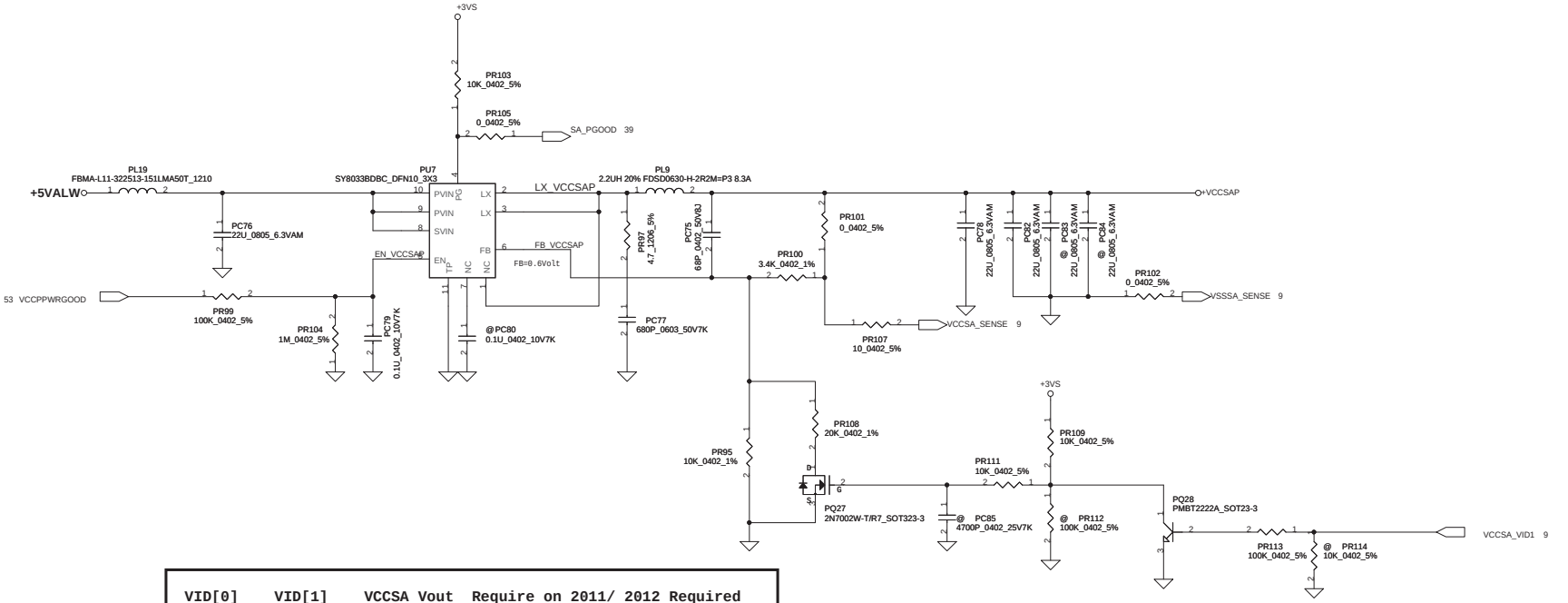
1.8VSP
Ipeak=3.35A ; 1.2Ipeak=4.02 ;Imax=2.345A
Vout=0.6*(1+(20K/10K))=1.8V





VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note:Use VCCSA_SEL to switch High & Low Level for VID[1]
(ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.

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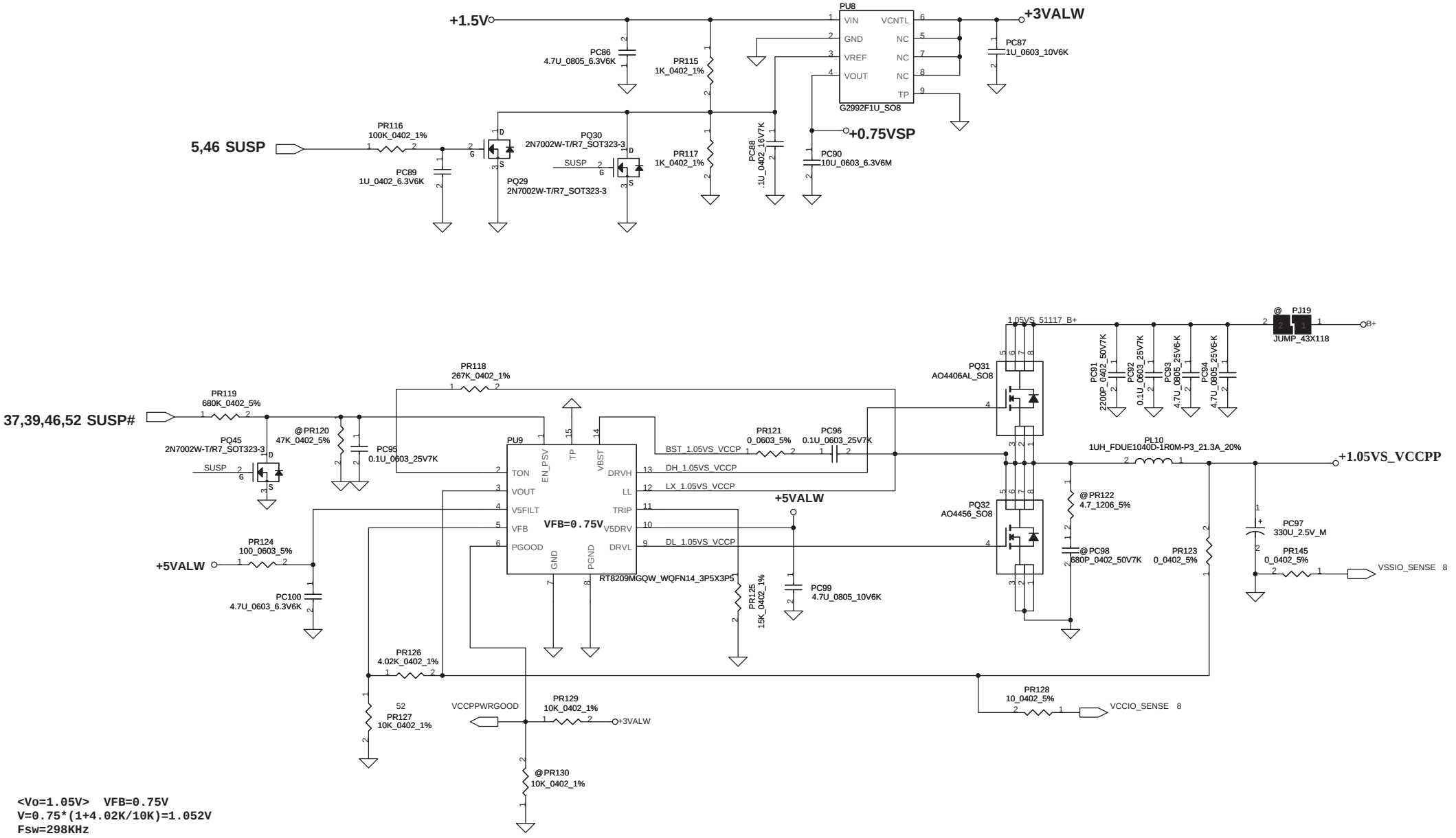

<Vo=1.05V> VFB=0.75V
V=0.75*(1+4.02K/10K)=1.052V
Fsw=298KHz

Cout ESR=15m ohm Rdson(max)=5.6 mohm Rdson(typ)=4.5 mohm.
Ipeak=12.866A, Imax=9A, Iocp=15.439A
Delta I=((19-1.05)*(1.05/19))/(L*Fsw)=3.33A
=>1/2Delta I=1.665A
choose Rcs=15K
Iocpmax=((15K*11uA)/0.0045)+1.665A=37.62A
Iocpmin=((15K*9uA)/(0.0056*1.3))+1.665A=23.02A
Iocp=23.02A~37.62A

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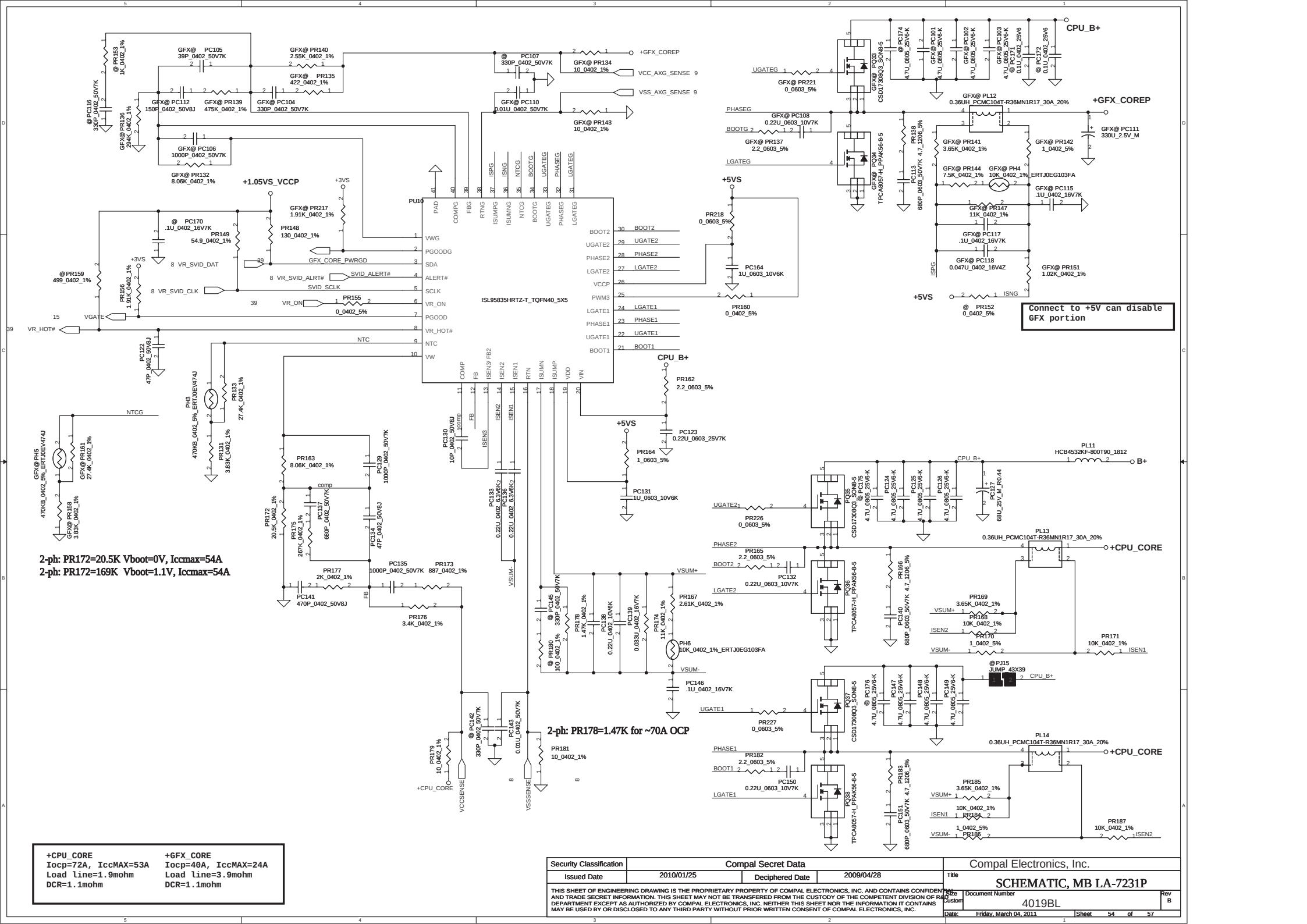
ISL95835HRTZ-T_TQFN40_5X5
+1.05VS_VCCP
+3VS
+5VS
CPU_B+
+GFX_COREP
+CPU_CORE
B+
VCC_AXG_SENSE 9
VSS_AXG_SENSE 9
+GFX_COREP
VR_HOT#
VR_ON
VGATE
NTCG
SVID_ALERT#
SVID_SCLK
GFX_CORE_PWRGD
Connect to +5V can disable GFX portion
2-ph: PR172=20.5K Vboot=0V, Iccmax=54A
2-ph: PR172=169K Vboot=1.1V, Iccmax=54A
2-ph: PR178=1.47K for ~70A OCP
+CPU_CORE
Iocp=72A, IccMAX=53A
Load line=1.9mohm
DCR=1.1mohm
+GFX_CORE
Iocp=40A, IccMAX=24A
Load line=3.9mohm
DCR=1.1mohm
Security Classification
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2010/01/25
Deciphered Date
2009/04/28
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SCHEMATIC, MB LA-7231P
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Custom
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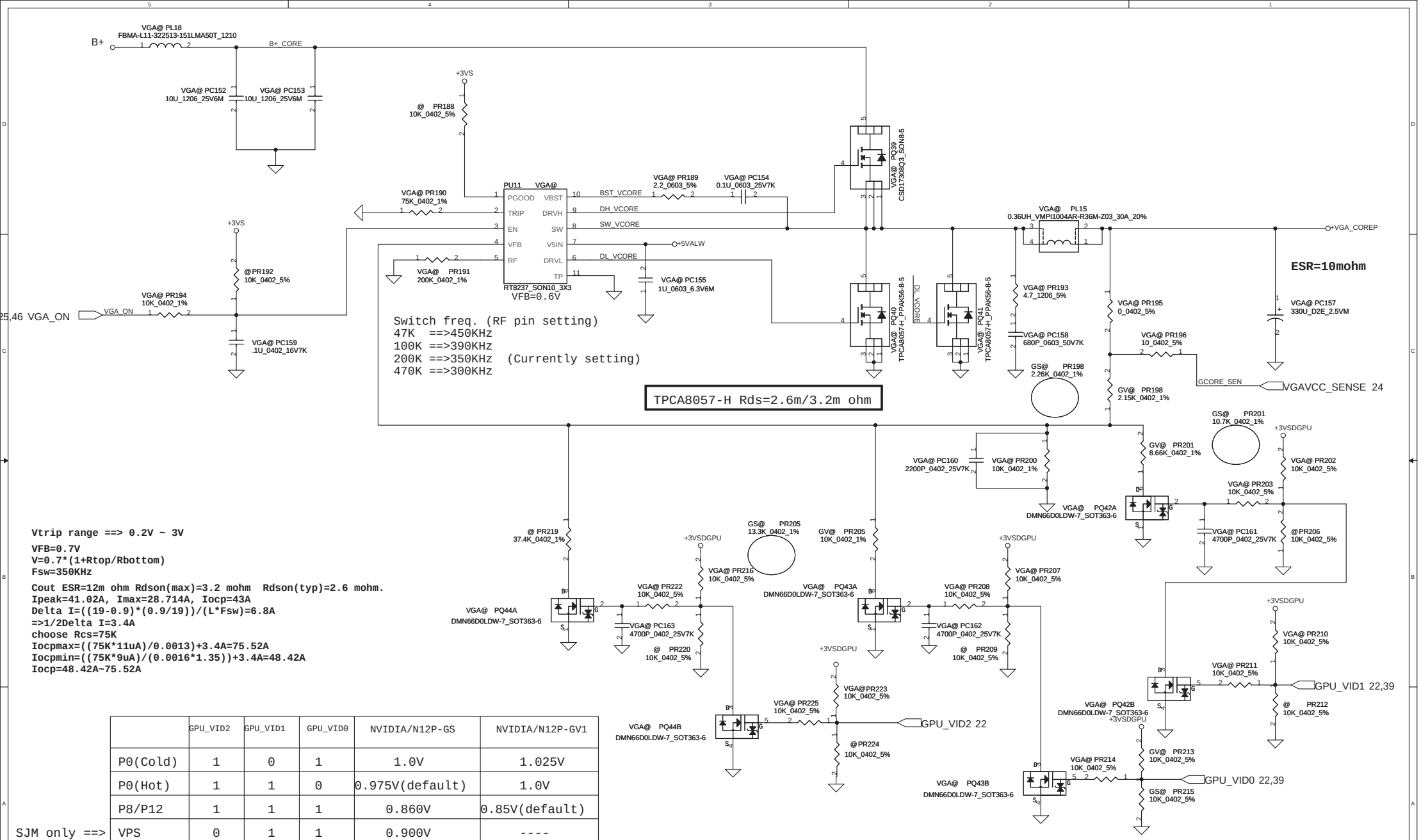

Vtrip range ==> 0.2V ~ 3V

VFB=0.7V
V=0.7*(1+Rtop/Rbottom)
Fsw=350KHz

Cout ESR=12m ohm Rdson(max)=3.2 mohm Rdson(typ)=2.6 mohm.
Ipeak=41.02A, Imax=28.714A, Iocp=43A
Delta I=((19-0.9)*(0.9/19))/(L*Fsw)=6.8A
=>1/2Delta I=3.4A
choose Rcs=75K
Iocpmax=((75K*11uA)/0.0013)+3.4A=75.52A
Iocpmin=((75K*9uA)/(0.0016*1.35))+3.4A=48.42A
Iocp=48.42A~75.52A

	GPU_VID2	GPU_VID1	GPU_VID0	NVIDIA/N12P-GS	NVIDIA/N12P-GV1
P0(Cold)	1	0	1	1.0V	1.025V
P0(Hot)	1	1	0	0.975V(default)	1.0V
P8/P12	1	1	1	0.860V	0.85V(default)
SJM only ==> VPS	0	1	1	0.900V	----

Security Classification	Compal Secret Data		
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	HW/Edward request	Meet Turn off sequence		53	Add PQ45	2010 11/24	DVT
2	HW/Edward request	Meet Turn on sequence		53	Change PR119 to 680KΩ, PC95 to 0.1uF	2010 11/27	DVT
3	HW/Edward request	Meet new VGA table		55	Change PR201, PR205, PR219	2010 12/03	DVT
4	Battery Turn on time too long	Change enable 3/5V path				2010 12/04	DVT
5	HW/Edward request	For USB 3.0 charger function		47	Add PJ26	2010 12/04	DVT
6	HW/Edward request	Don't need VGA_PW_OK net		55	Delete net	2010 12/04	DVT
7	HW/Edward request	Tune Power sequence		52	Change PR92 from 100K to 510K Delete PR94	2010 12/08	DVT
8	HW/Edward request	Tune Power sequence		53	Change PR116 from 24.9K to 100K	2010 12/09	DVT
9	Costdown			54	Change PC97, PC111 to OS-CON cap.	2011 01/06	PVT
10	ISN test fail	ISN solution		49	Change PL16 to 1uH Add PC109, PC119	2011 01/07	PVT
11	Trigger ACOC	Prevent to trigger phase to gnd threshold Reserve RC for ADP_I		48	Change PC28 from 2.2u to 0.1u Add PR72	2011 01/24	PVT2
12							
13							
14							
15							
16							
17							

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

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A --> B Change List

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1209-----------------------------------
1. Page 24, Change R383 to GS@
            Change R380 to @
            Add Option Component for R383 and R386 4.99K_0402_1% with BOM structure GV@
2. Page 46, Change R679 to 100K_0402_5%
            Change R685 to 200K_0402_5%
            Change R692 to 750K_0402_5%
3. Page 40, Change SW8 to SN200002800
1206-----------------------------------------
1. Page 17, U16 BOM Structure change to OPT@
2. Page 37, C613 BOM structure change to BT@
3. Page 32, Add T70, T71 for JCRT1.
4. Page 45, Change H10 to H2P5.
5. Page 14, Change C183, C184 to 27P
6. Page 22, Change C297, C298 to 22P
7. Page 35, Change C582, C583 to 33P
8. Page 43, Change R666, R668 to SM010017710 (For EMI)
9. Page 38, Pop R590, R591 with 33 ohm, C635, C636 with 6P for EMI
1203-----------------------------------------
1. Page 39, Add C703 for ESD.
1202-----------------------------------------
1. Update power schematics
2. Change H24 to H2P5
3. Page 35, Add R557 for power source +3VALW_PCH reserved
1201-----------------------------------------
1. Page 40, Update Reset Button circuit
   Add R656, Q38
2. Page 17, delete VGA_ON for PD only.
   Change PR3.2 to PCH_GPIO2, PR3.1 to PCH_GPIO53
   Delete R257
3. Update Power Schematics 1201
1130b----------------------------------------
1. Page 38, U23.11 change to +3VS_CARD
2. Q2, Q13, Q19, Q21~Q29, Q31, Q33, Q34, Q50, Q51, Q54, Q56~Q63, Q68, Q74 change to SB00000J200
1130-----------------------------------------
1. Page 18, Add Q75,Q74,R841 (The new circuit for DGPU_PWROK after 1.5V).
   Delete R271
2. Page40, Change R646 to 10K
   Change R648 to 1K
   Pop R646, R648, D18, Q35, R645 for Reset mainpower and BI
   Change R653 BOM structure to @
   Change SW8 to SN200002700
1129-----------------------------------------
1. Page 07, Correct R70 bom structure to EDP@
2. Page 15,Change R244.1 net name from PCH_RSMRST# to  PCH_RSMRST#_R
   Unpop R231
3. Page 17, U6, U7 change to SA00000OH00 (Same as U5/U39)
4. Page 24, Delete R390, R391, R392 for space issue.
5. Page 35, Add Q37 and Unpop R555
6. Page 38, Add R833 between +3VS and +3VS_CARD
   Change U23.47 to +3VS_CARD
7. Page 39,Change R621 from 0ohm to 8.2k(Board ID)
8. Page 42, Unpop R733
   Pop R732, R299
   Delete R637, R638, Q38, Q39, R299, R634, R636, R639, R640
   Change netname of PD# to EC_MUTE#
   Connect U29.4.9.21.29 to +3VS_CODEC
9. Page 45, Change C780 from SGA19151410(D size) to SGA00002N80(B2 size)
   Unpop U40, C204, R754
10.Page 46, Change Q47, Q52 to AO4430L_SO8
11.Update Power Schematics (11/25)
12.C226, C540, C549, C566, C573, C576, C580, C590, C712 change material to SE000000K80
13.D8, D9 change material to SCS00003600 (Need check again)
14.D32 change to SC100001K00 (Need apply CIS Symbol)
1123-----------------------------------------
1. Page 22, Change R342 PU location from R762.2 to Q68.3
2. Page 24, Fix N12P-GV device ID
   R489 change BOM Structure to GS@
   R382, R380, R760, R756, R758, R757 change BOM Structure to GV@
   R380 change to 45.3K_0402_1% (SD034453280)
   R760 change to 4.99K_0402_1% (SD034499180)
   Delete Option compoent of R386
3. Page35, Modify auto boot-up issue
   Unpop R552
   POP R553, R541
   Change R541 PU location from R552.1 to R552.2
4. Page36, L31 update CIS Symbol and PCB footprint
5. Page 40, Change R622 PU to +3VALW_EC
   JTP1 pin definition upside down.
   Update D-Door Circuit
   Delete SW1, R631
   Add JDOOR1, SW
6. Page 41, SW6 change to SN100001D10
7. Page 42, Modify PD# circuit for 3V tolerance.
   Add R299
   Change R637, R638 PU to +3VS
   Fix Headphone/MIC detect issue
   Change R649 to 10K_0402_1%
   Change R650 to 39.2K_0402_1%
8. Page 44, Modify SMI circuit for leakage issue.
   Delete R830
   Add Q69, R734
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B --> C Change List

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0121A----------------------------------
1. Page 19, Change L1 to SHI00003Y00
2. Page 41, Change R626 to SD034499080 (499_1%)
            Change R739 to SD034150080 (100_5%)
3. Page 17, Add R185
4. Page 46, Change R703 to 100K
0110A----------------------------------
1. Change SE107475M80 to SE107475K80
2. Change SE052105Z80 to SE080105K80
3. Change SE068221J80 to SE074221K80
4. Change SE070473Z80 to SE076473K80
5. Page 15, UnPOP U5 and POP R223
6. Page 35, Unpop Q37 and POP R557
7. Change U8 to SA000047U10(N12P-GS) and SA00004JO10(N12P-GV)
8. Page41,
   R625 form 390 to 100
   R626 from 820 to 200
   R739 from 820 to 100
   R627 from 390 to 2.49K
   R629 from 820 to 3K
   R740 from 390 to 3.3K
   R741 from 390 to 2.2K
   R740 from 820 to 3.3K
0107A----------------------------------
1. Page 40, Unpop SW8
2. Page 05, Add C215.
1. Page 11, Add C207, C212, C214 (0.1U_0402) for EMI reuqire
2. Page 12, Delete C159 for Layout space
3. Page 36, Delete R968, C994
4. Page 45, Reserved R736, R739
5. Page 18, Delete Q75
            Change Q74 to Q74A, A74B (DMN66D0LDW-7_SOT363-6)
            Change R842 PU to +3VSDGPU
0103-----------------------------------------
1. Page 40, Add R691 for EC_BI
2. Page 39, Connect EC_BI to U24.64
            Change R621 to 18K_0402_5%
            Delete net 65W/90W#
3. Page 25, Unpop C345, C346, C347, C348 L13, L14, C356, C357, C358
            Change C349, C359 to 10K_5%_0402
            Unpop R415, R416
4. Page 18, Change Q75 to AP2302GN-HF_SOT23-3
            Add R842, C185 with BOM structure OPT@
            Change Q74, Q75, R841 with BOM structure OPT@
5. Page 37, Delete R572
6. Page 08, change C81, C82 to SGA20331E10
7. Page 26, Change C381,C857 to SGA20471D20
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C --> Pre-MP Change List

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0222A----------------------------------
1. Page 41, Change R627, R741 to 100_0402_5%
            Change R740 to 150_0402_1%
            Change R627, R742 to 560_0402_5%
2. Page 45, Unpop D30 (Remove USB3.0 ESD Diode)
0218A----------------------------------
1.Page 31, Add L45 for USB20_P10/N10
           Change R478/R479 to @
           Move C492, C493 to USB20_P10/N10
           Delete D5 for layout space
0215A----------------------------------
1. Page 44, Mount R720 for EEPROM (EON)
2. Change U3 to B3 version(SA00004EEY0)
3. Page 41, change R626 to 300_0402_5%
            change R739 to 100_0402_5%
0125A----------------------------------
1. Page39 Change R621 to 33K_0402_5% (Board ID)
2. Update Power Schematics
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