

JE40 HR

DIS/UMA/Muxless Schematics Document

Sandy Bridge

Intel PCH

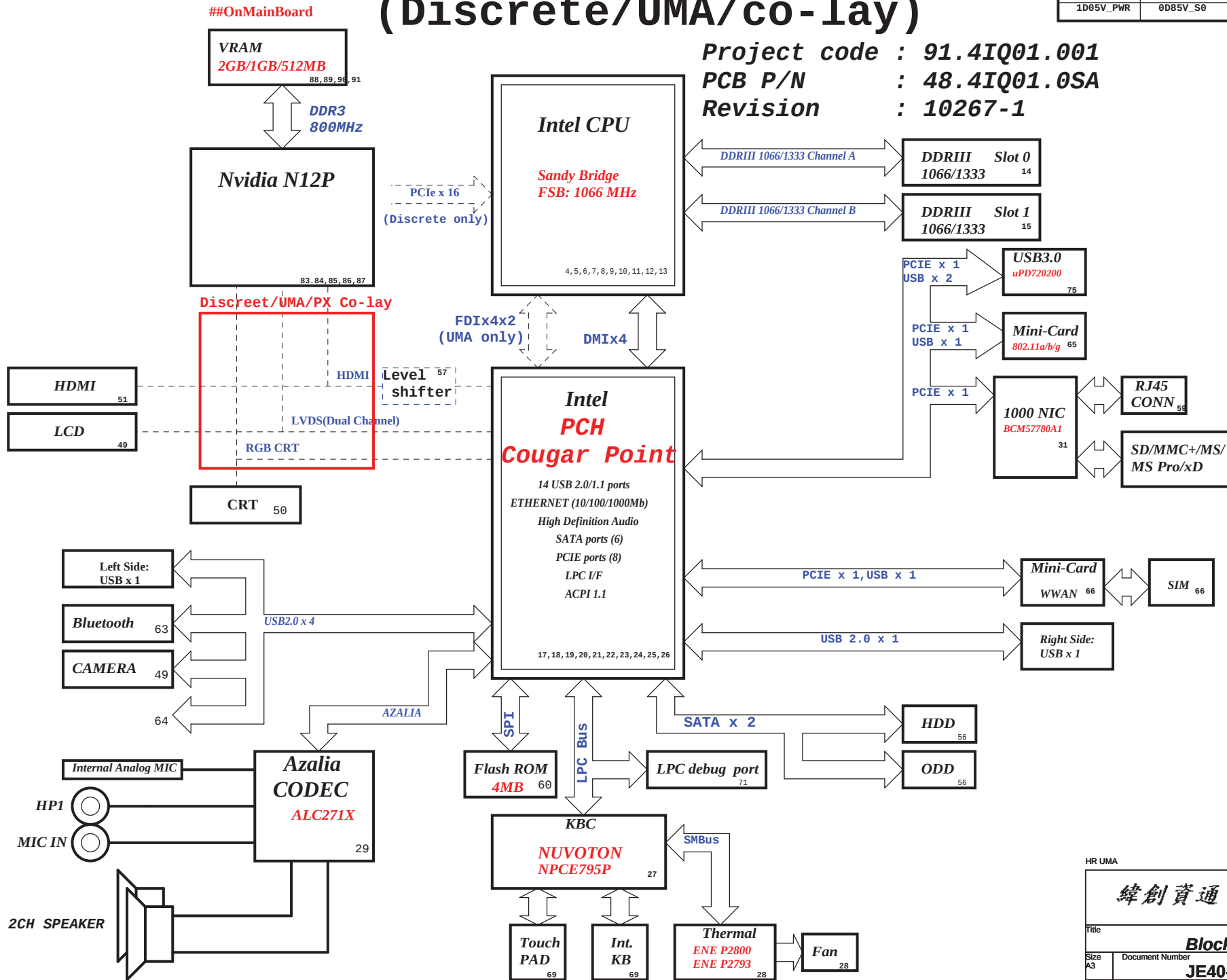
DY :None Installed
DIS:DIS installed
DIS_Muxless :BOTH DIS or Muxless installed
DIS_PX:BOTH DIS or PX installed
DIS_PX_Muxless:DIS or PX or Muxless installed.
Muxless: Muxless installed.(PX4.0)
PX:MUX installed.(PX3.0)
PX_Muxless:BOTH PX or Muxless installed.
UMA:UMA installed
UMA_Muxless:BOTH UMA or Muxless installed
UMA_PX_Muxless:UMA or PX or Muxless installed

ANNIE: ONLY FOR ANNIE solution.
PSL: KBC795 PSL circuit for 10mW solution installed.
10mW: External circuit for 10mW solution installed.
65W: for 65W adaptor installed.
90W: for 90W adaptor installed.

HR UMA

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Title			
Cover Page			
Size A3	Document Number JE40-HR	Rev -1	
Date: Thursday, December 02, 2010	Sheet 1	of	102

JE40 HR Block Diagram (Discrete/UMA/co-lay)



SYSTEM DC/DC APL5916KAI 48		CPU DC/DC NCP6131S52MNR 42~43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S5	1V_VGA_S0 1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3 3D3V_S0	1D5V_VGA_S0 3D3V_VGA_S0

PCB LAYER	
L1:Top L2:VCC L3:Signal	L4:Signal L5:GND L6:Bottom

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Title Block Diagram		
Size A3	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 2 of 102	

A

B

C

D

E

PCH Strapping

Huron River Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

A

B

C

D

E

USB Table

A

B

C

D

E

PCIE Routing

LANE1	Mini Card2(WWAN)
LANE2	Mini Card1(WLAN)
LANE3	Card Reader
LANE4	Onboard LAN
LANE5	USB3.0
LANE6	Intel GBE LAN
LANE7	Dock
LANE8	New Card

A

B

C

D

E

SATA Table

SATA	
Pair	Device
0	HDD1
1	HDD2
2	N/A
3	N/A
4	ODD
5	ESATA

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

A

B

C

D

E

Processor Strapping

Huron River Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. Enabled - An external Display Port device is connect to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	
		ACTIVE IN	DESCRIPTION
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D85V_VTT 0D85V_S0 0D75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 0.95 - 0.85V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
3D3V_LAN_S5	3.3V	WOL_EN	Legacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and +V3ALW in Sx

A

B

C

D

E

SMBus ADDRESSES

I ² C / SMBus Addresses		Ref	Des	HURON RIVER ORB	
Device				Address	Hex Bus
EC SMBus 1 Battery CHARGER					BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP					SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA SML1_CLK/SML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI					PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

A

B

C

D

E

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Table of Content

JE40-HR

Size A3

Document Number

Date: Thursday, December 02, 2010

Rev -1

Sheet 3 of 102

Note:
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

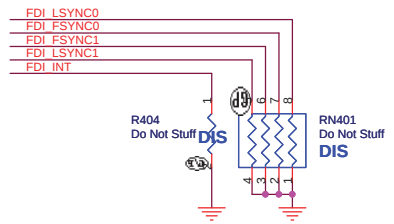
Note:
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:
Lane reversal does not apply to FDI sideband signals.

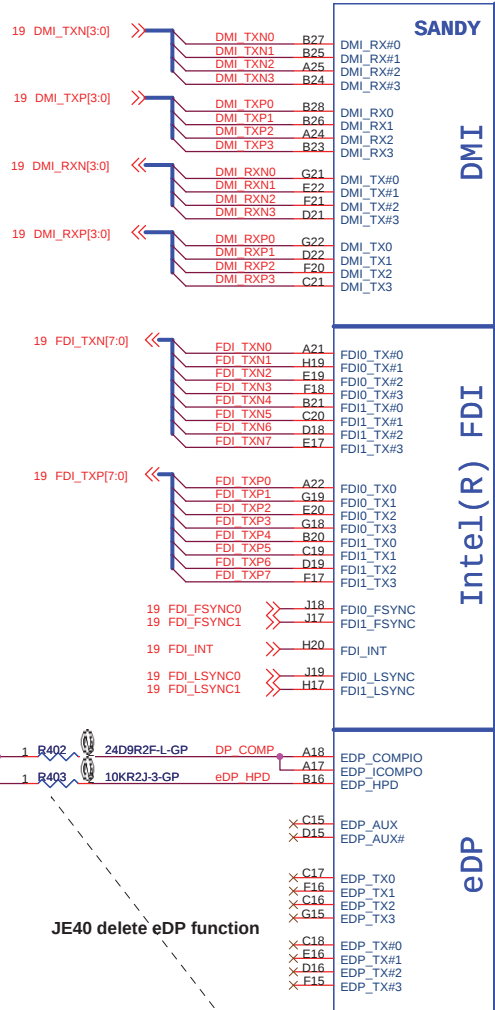
Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

NOTE.
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

Stuff to disable internal graphics function for power saving.

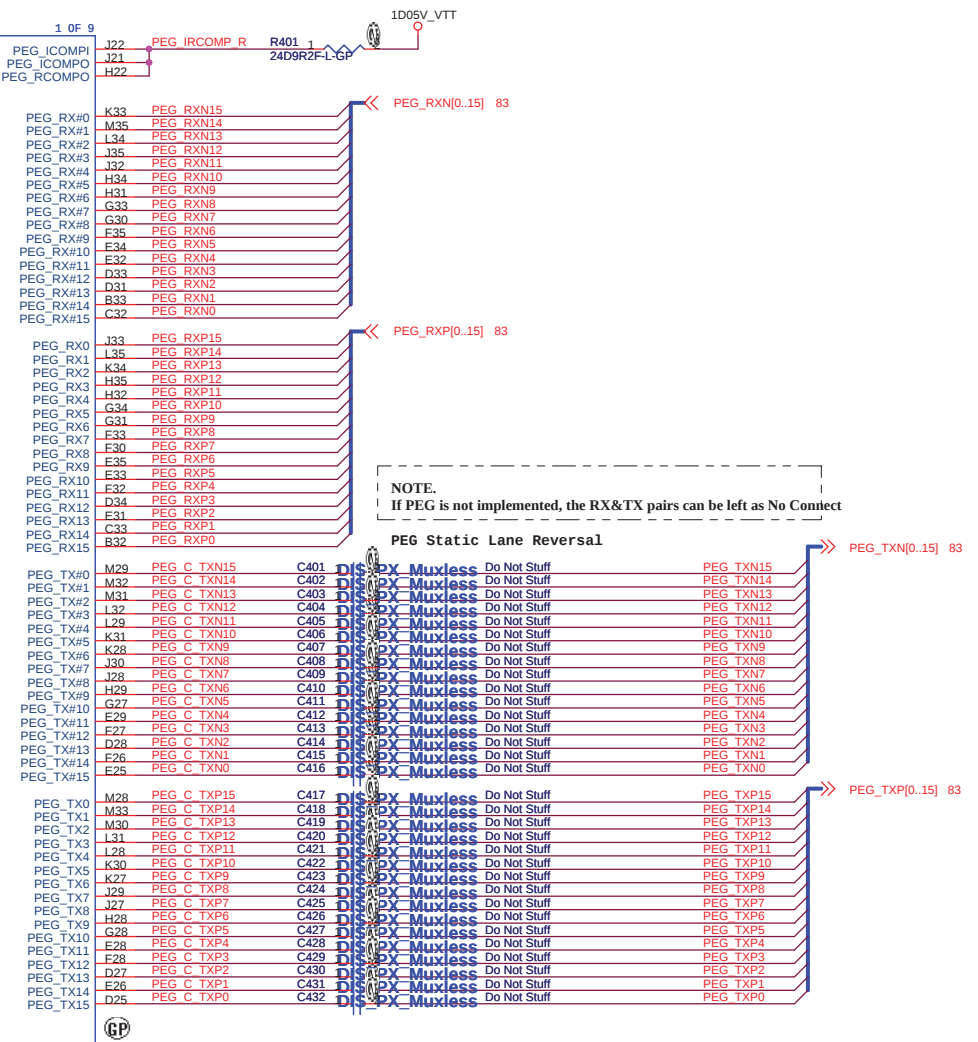


CPU1A
SANDY
62.10055.421
Change:62.10053.611
2nd = 62.10055.321
3rd = 62.10040.821



Intel(R) FDI
PCI EXPRESS* - GRAPHICS

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.



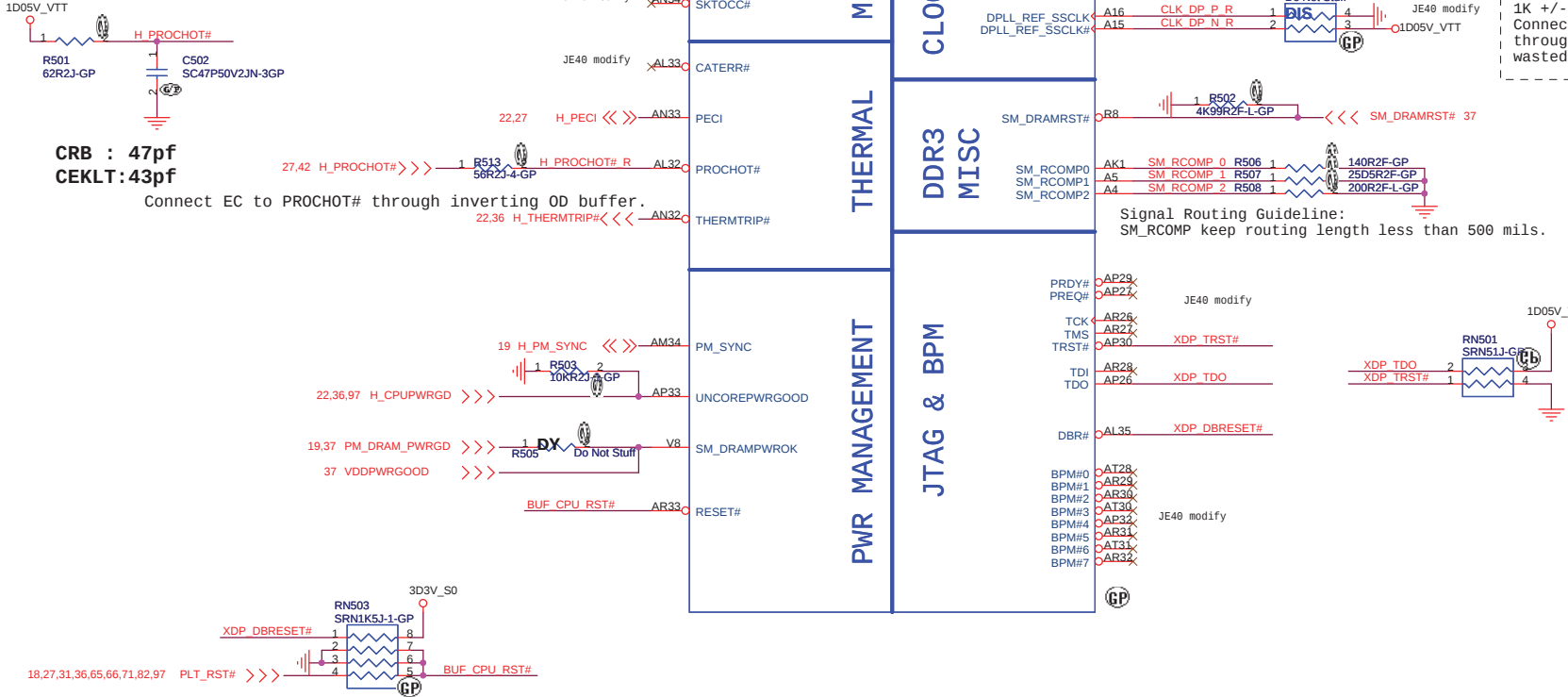
NOTE.
If PEG is not implemented, the RX&TX pairs can be left as No Connect

PEG Static Lane Reversal

20100614 V1.1

NOTE:
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

SSID = CPU



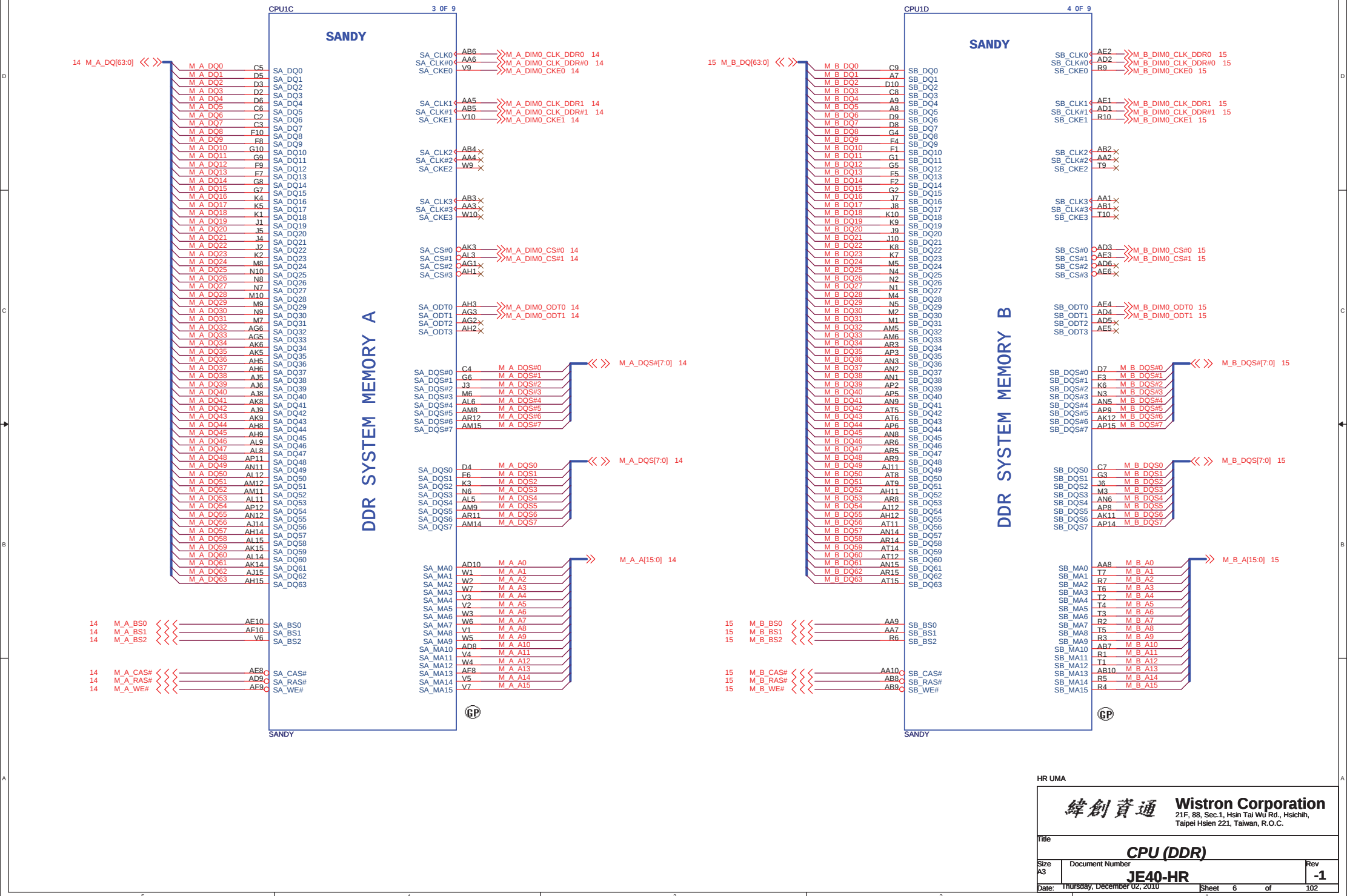
Disabling Guidelines:
If motherboard only supports external graphics:
Connect DPLL_REF_SSCLK on Processor to GND through
1K +/- 5% resistor.
Connect DPLL_REF_SSCLK# on Processor to VCCP
through 1K +/- 5% resistorpower (~15 mW) may be
wasted.

Signal Routing Guideline:
SM_RCOMP keep routing length less than 500 mils.

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Title CPU (THERMAL/CLOCK/PM)		
Size Custom	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 5 of 102	

SSID = CPU



SSID = CPU

PEG Static Lane Reversal	
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	0: Lane Reversed

DIS_PX_Muxless

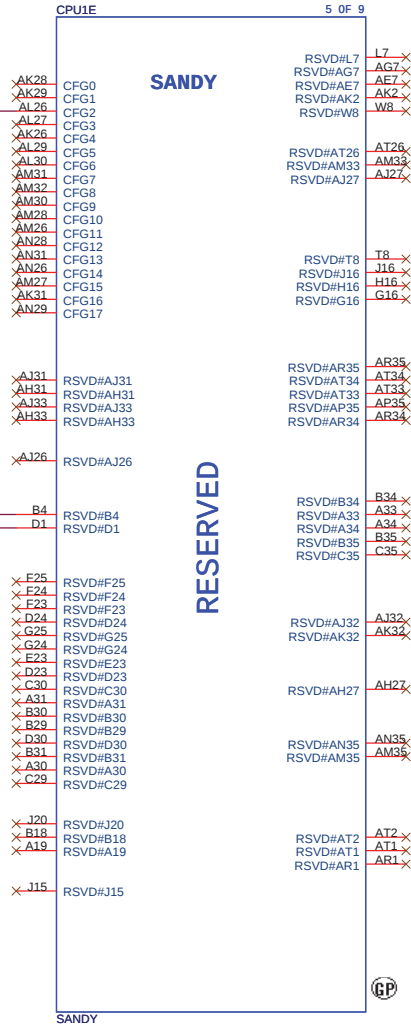
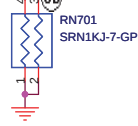


B4: VREF_DQ CHA

M: VREF_DQ DIMM0 C

M: VREF_DQ DIMM1 C

D1: VREF_DQ CHB



HR UMA

POWER

PEG AND DDR

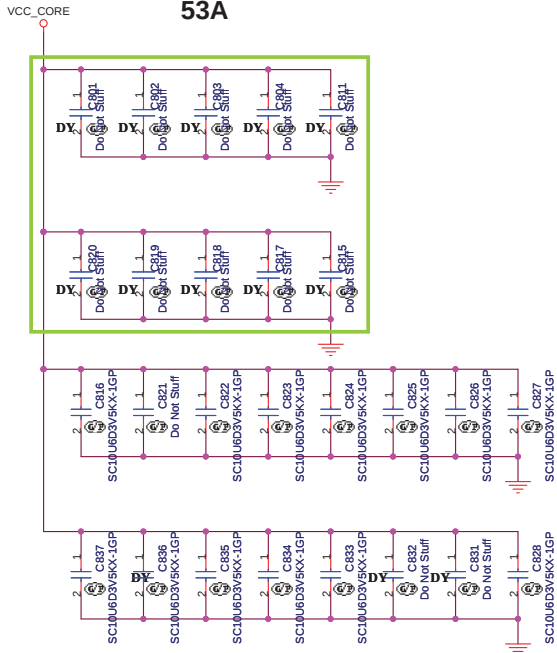
CORE SUPPLY

SVID

SENSE LINES

PROCESSOR CORE POWER

53A



VCC Output Decoupling Recommendation:
4 x 470 uF at Bottom Socket Edge
8 x 22 uF at Top Socket Cavity
8 x 22 uF at Top Socket Edge
8 x 22 uF at Bottom Socket Cavity

VCC_CORE

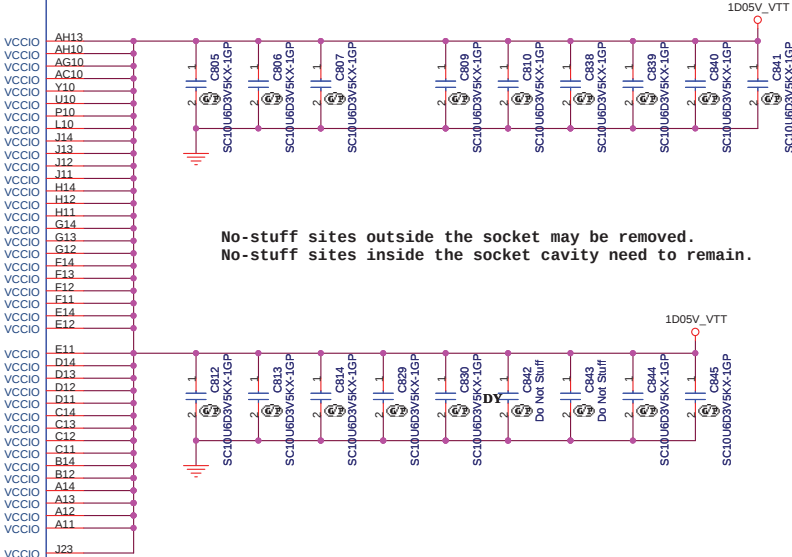
- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V35 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- R35 VCC
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- R32 VCC
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- R30 VCC
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- R27 VCC
- R26 VCC
- P34 VCC
- P33 VCC
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- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

CPU1F

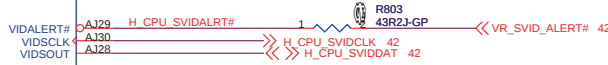
SANDY

6 OF 9

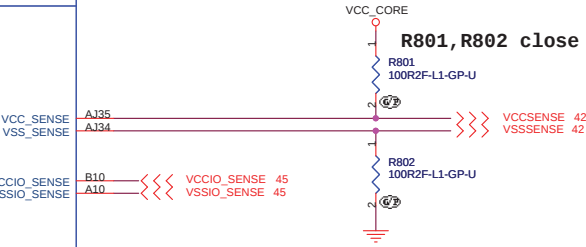
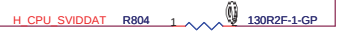
VCCIO Output Decoupling Recommendation:
2 x 330 uF (3 x 330 uF for 2012 capable designs)
5 x 22 uF & 5 x 0805 no-stuff at Bottom
7 x 22 uF & 2 x 0805 no-stuff at Top



No-stuff sites outside the socket may be removed.
No-stuff sites inside the socket cavity need to remain.



For CRB VIDSOUT need to pull high 130 ohm closr to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

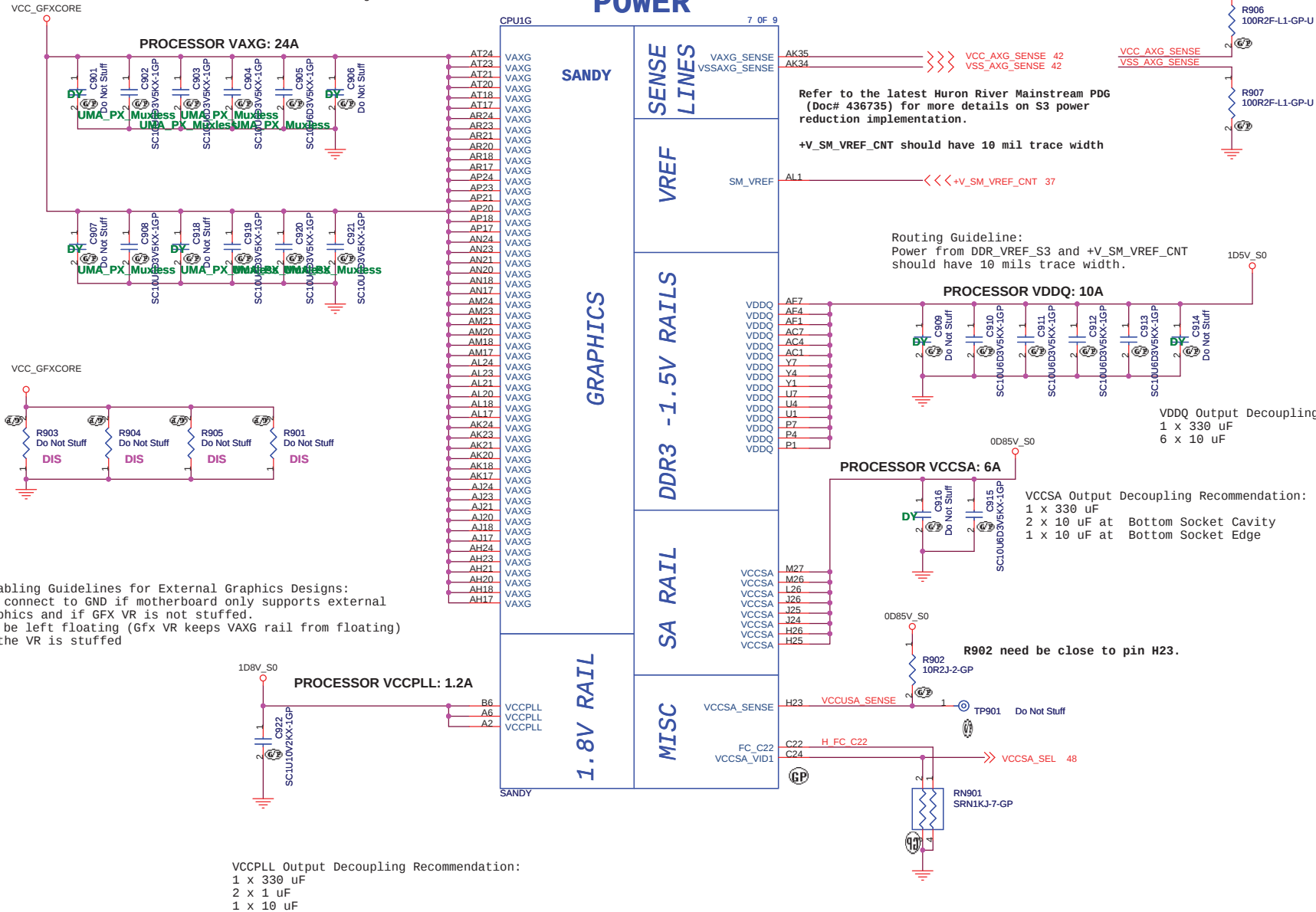


R801, R802 close to CPU

SSID = CPU

VAXG Output Decoupling Recommendation:
 2 x 470 uF at Bottom Socket Edge
 2 x 22 uF at Top Socket Cavity
 4 x 22 uF at Top Socket Edge
 2 x 22 uF at Bottom Socket Cavity
 4 x 22 uF at Bottom Socket Edge

R906,R907 close to CPU



Disabling Guidelines for External Graphics Designs:
Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.
Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed

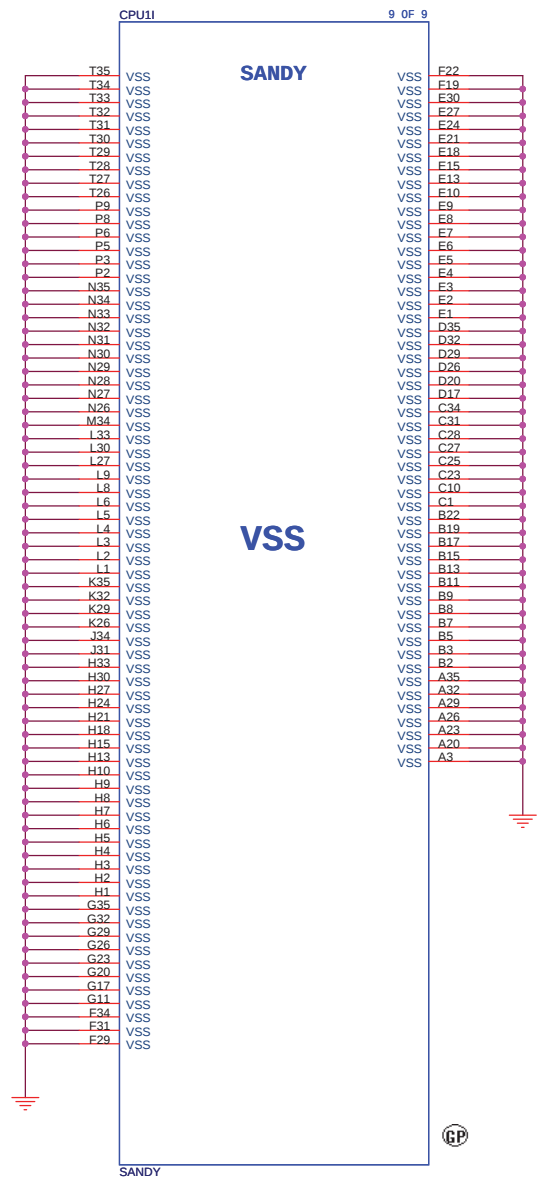
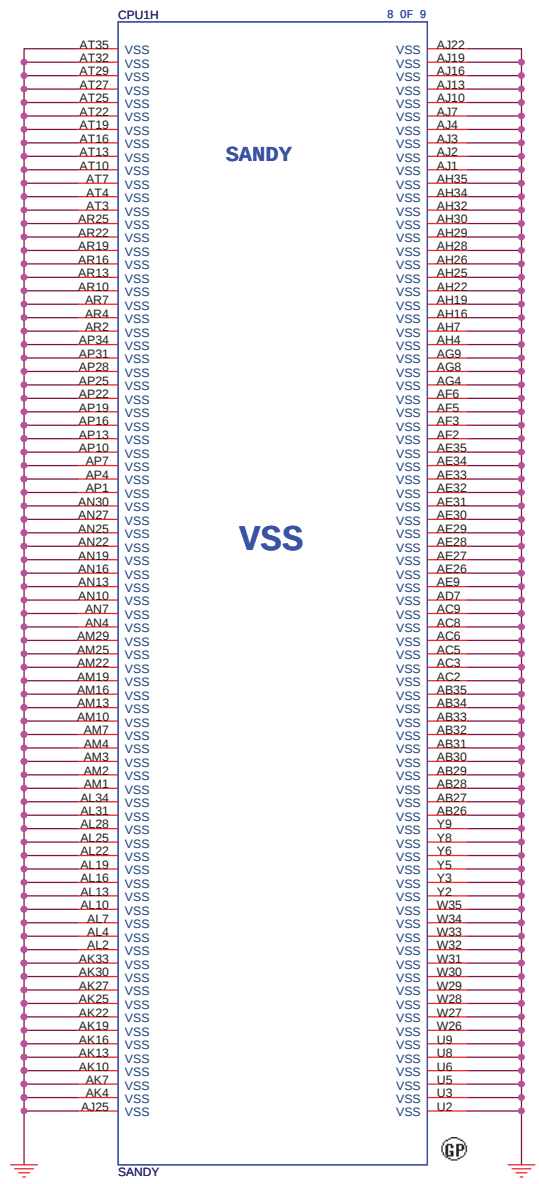
VCCPLL Output Decoupling Recommendation:
1 x 330 uF
2 x 1 uF
1 x 10 uF

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Title			
CPU (VCC GFXCORE)			
Size A3	Document Number		Rev
	JE40-HR		-1
Date:	Thursday, December 02, 2010	Sheet 9 of	102

SSID = CPU



5	4	3	2	1
D				
C				
B				
A				

JE40 delete XDP function

HR UMA

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Title

Size
A3

Document Number
JE40-HR

Date: **Thursday, December 02, 2010**

SDP

-1

Sheet 11 of 102

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HR UMA

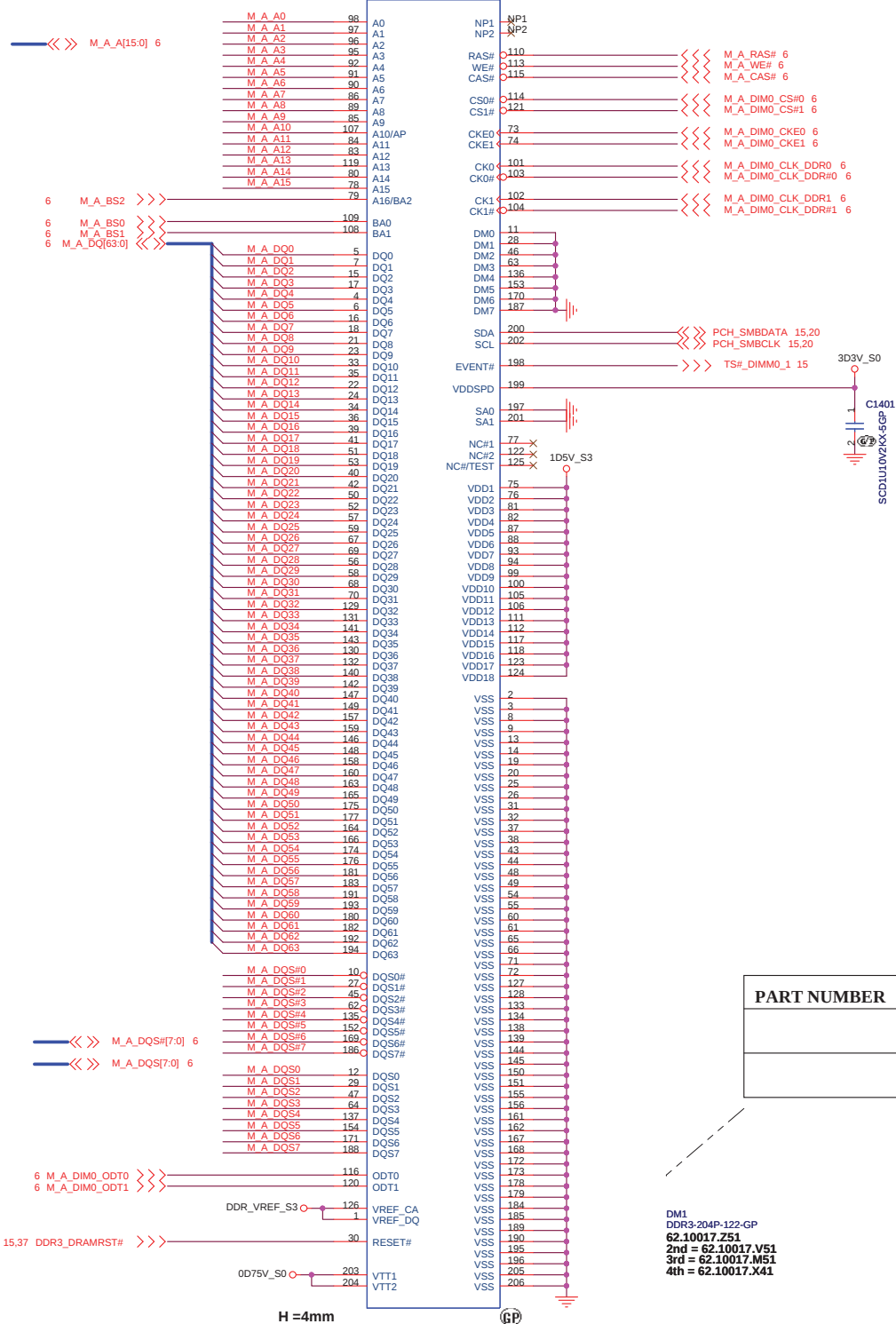
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Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 12 of 102

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HR UMA

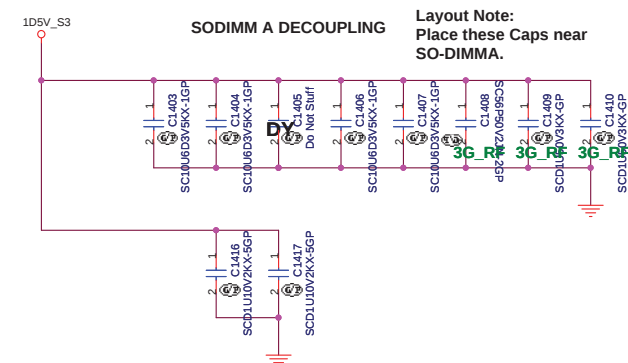
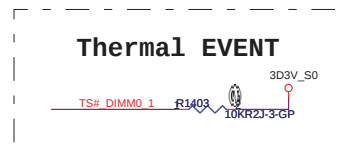
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Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 13 of 102

SSID = MEMORY



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



PART NUMBER	Height	TYPE

DM1
DDR3-204P-122-GP
62.10017.Z51
2nd = 62.10017.V51
3rd = 62.10017.M51
4th = 62.10017.X41

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Title			
DDR3-SODIMM1			
Size Custom	Document Number		Rev
	JE40-HR		-1
Date:	Thursday, December 02, 2010	Sheet 14 of	102

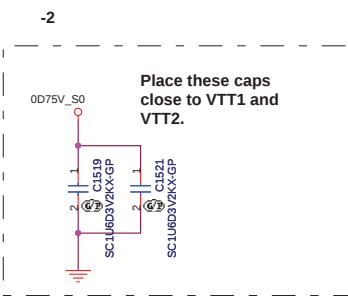
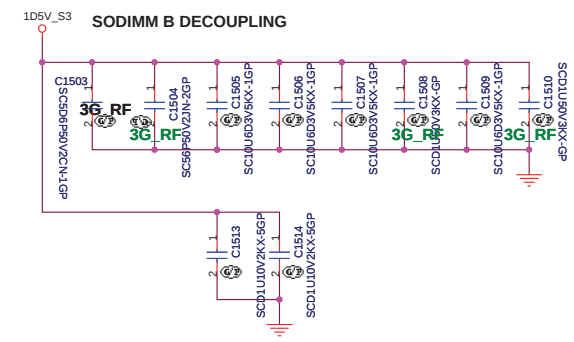
SSID = MEMORY



Note:
SO-DIMMB SPD Address is 0x44
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

Layout Note:
Place these Caps near SO-DIMMB.



DM2
DDR3-204P-126-GP
62.10024.D41

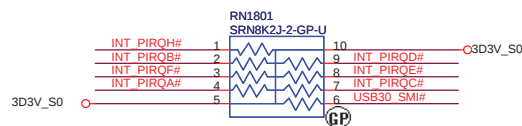
2nd = 62.10017.R91
3rd = 62.10017.V61
4th = 62.10017.X51

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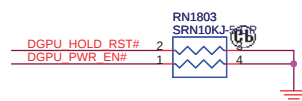
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Title DDR3-SODIMM2		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 16 of 102

SSID = PCH

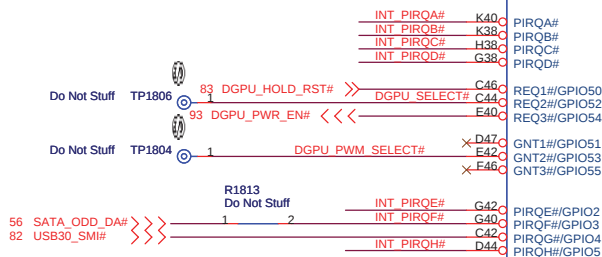


A16 swap override Strap/Top-Block
Swap Override jumper

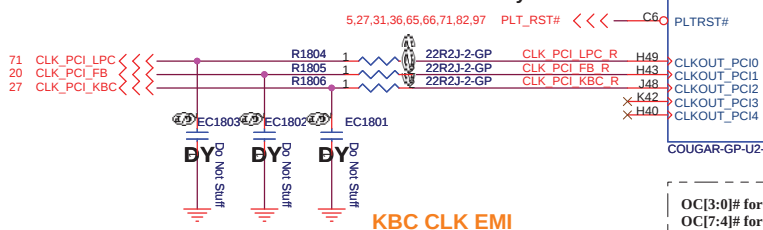
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default
-----------	---



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)



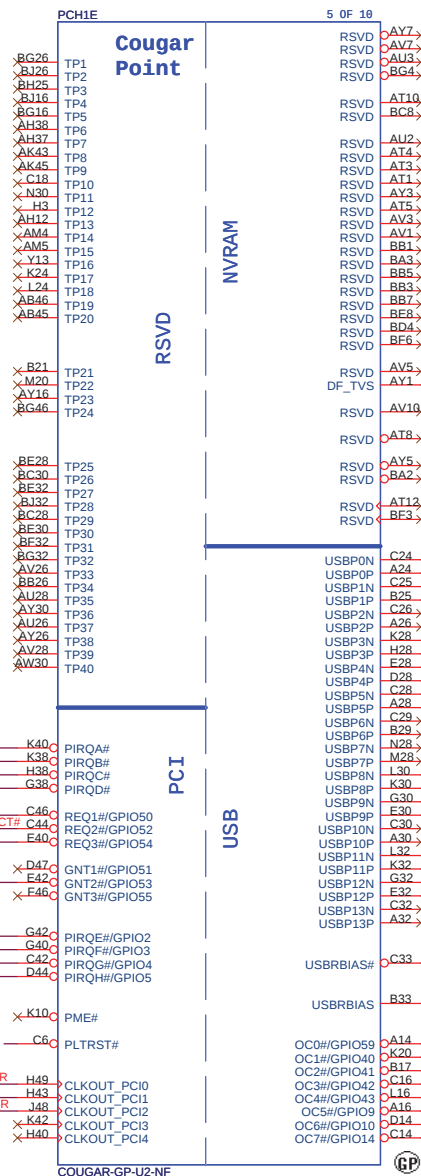
JE40 modify 07/16



KBC CLK EMI

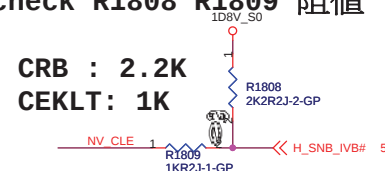
OC[3:0]# for Device 29 (Ports 0-7)

OC[7:4]# for Device 26 (Ports 8-13)



DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

check R1808 R1809 阻值



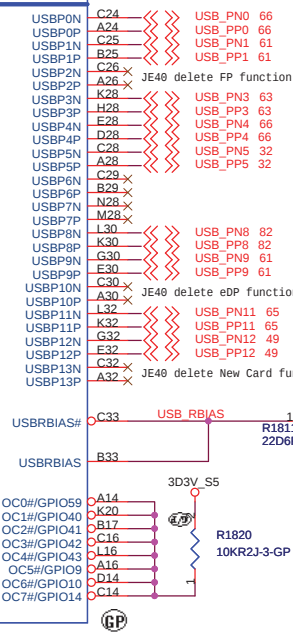
CRB : 2.2K
CEKLT: 1K

- ✗ USB Ext. port 1 (HS)
- ✗ External debug port use on Huron river platform

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA /USB CHARGE
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card

SB add USB port 5

JE40 co-lay USB2.0



USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

PCH (PCI/USB/NVRAM)

Size

Document Number

JE40-HR

Date: Thursday, December 02, 2010

Sheet 18 of 102

Rev

REV
-1

SSID = PCH

4 DMI_RXN[3:0] <<<>>>=
4 DMI_RXP[3:0] <<<>>>=
4 DMI_TXN[3:0] <<<>>>=
4 DMI_TXP[3:0] <<<>>>=

=<<<>>> FDI_TXN[7:0] 4
FDI_TXP[7:0] 4

Signal Routing Guideline:
DMI_ZCOMP keep W=4 mils and
routing length less than 500
mils.
DMI_IRCOMP keep W=4 mils and
routing length less than 500
mils.

Deep S4/S5 Supported

Deep S4/S5 Not Supported

VccDSW3_3

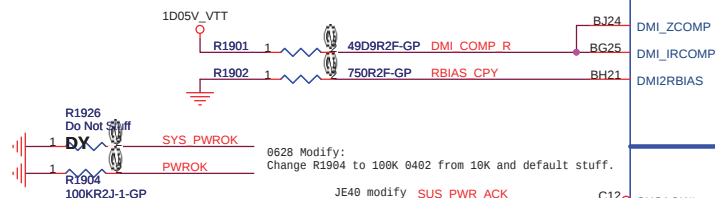
DPWROK

VccSUS3_3

RSMRST#

For platforms not supporting Deep S4/S5

- 1.VccSUS3_3 and VccDSW3_3 will rise at the same time (connected on board)
- 2.DPWROK and RSMRST# will rise at the same time (connected on board)
- 3.SLP_SUS# and SUSACK# are left as 'no connect'
- 4.SUSWARN# used as SUSPWRDNACK/GPIO30



FDI_INT >>> FDI_INT 4
FDI_FSYNC0 >>> FDI_FSYNC0 4
FDI_FSYNC1 >>> FDI_FSYNC1 4
FDI_LSYNC0 >>> FDI_LSYNC0 4
FDI_LSYNC1 >>> FDI_LSYNC1 4

DSWVRMEN >>> DSWODVREN 4
DPWROK >>> PCH_DPWROK 4
WAKE# >>> PCIE_WAKE# 31,65,66,82
CLKRUN#/GPIO32 >>> PM_CLKRUN# 27
SUS_STAT#/GPIO61 >>> PCH_SUSCLK_KBC 27
SUSCLK#/GPIO62 >>> PCH_SUSCLK_KBC 27
SLP_S5#/GPIO63 >>> PCH_SLP_S5# 27,36,37,47,92
SLP_S4# >>> PM_SLP_S4# 27,46
SLP_S3# >>> PM_SLP_S3# 27,36,37,47,92
SLP_A# >>> G10
SLP_SUS# >>> G16
PMSYNCH >>> H_PM_SYNC 5
SLP_LAN#/GPIO29 >>> K14

JE40 modify 07/16

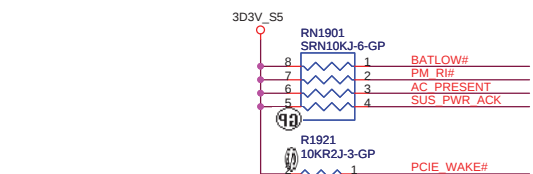
SB modify

DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled



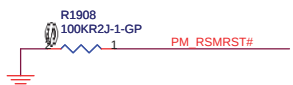
S0_PWR_GOOD after PM_SLP_S3# delay 200 ms

27,42 S0_PWR_GOOD >>> 2
1924 Do Not Stuff
JE40 modify
L22
L10
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRDNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
PM_RI#

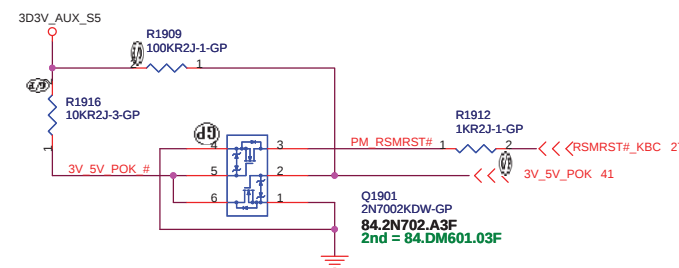


PCIE_WAKE#
CRB : 1K
CEKLT: 10K

PWRBTN#
This signal has an internal pull-up resistor



PM_RSMRST#
CRB : PL 10K
ANNIE : PL 100K

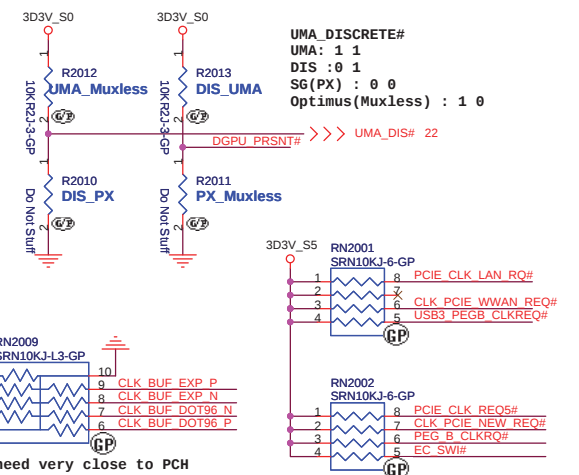
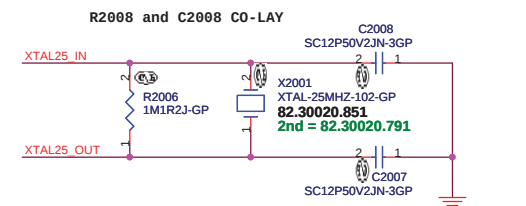
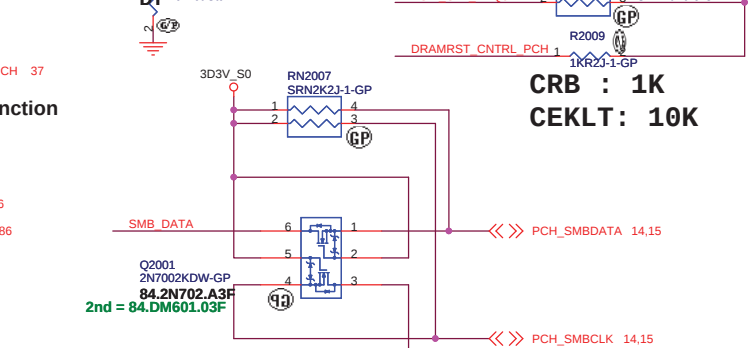
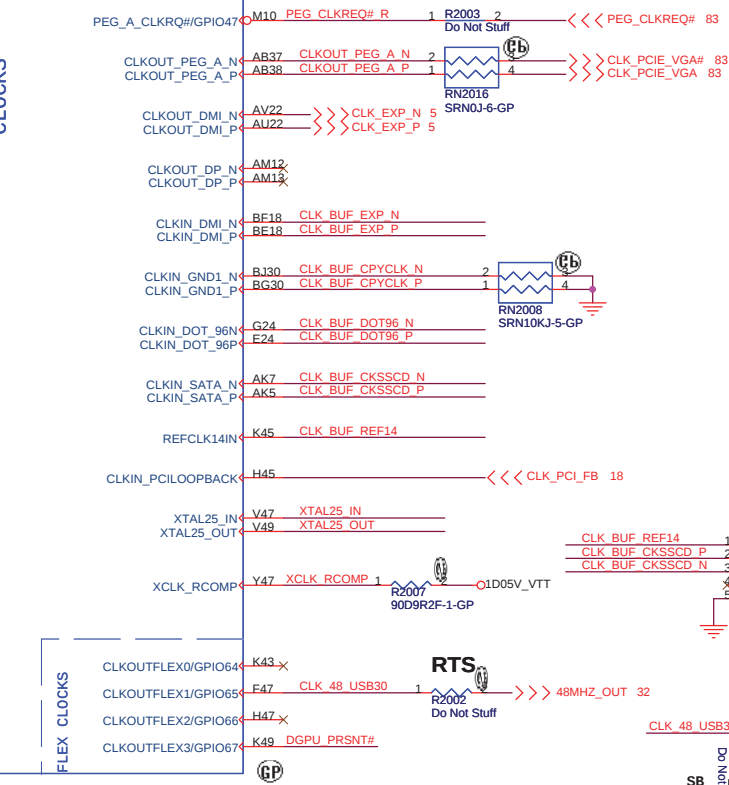
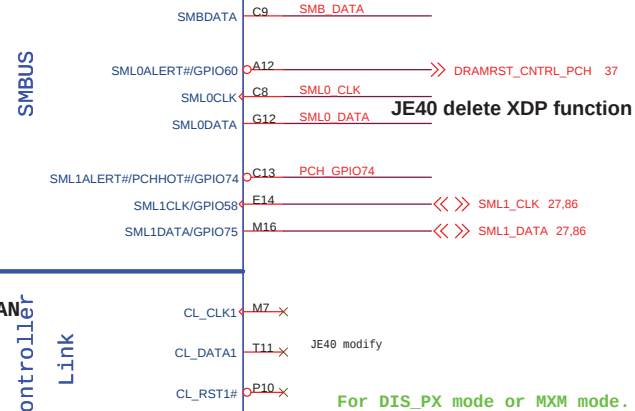
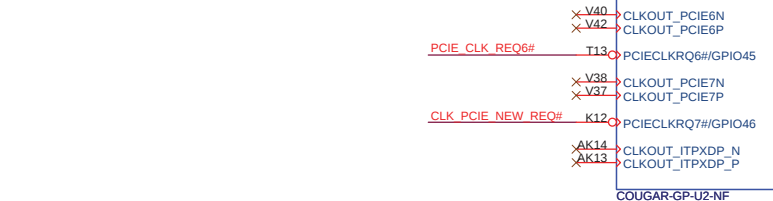
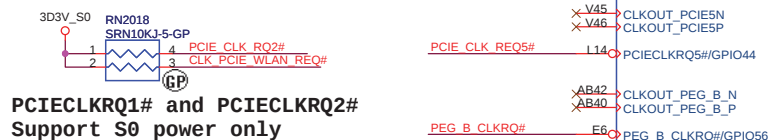
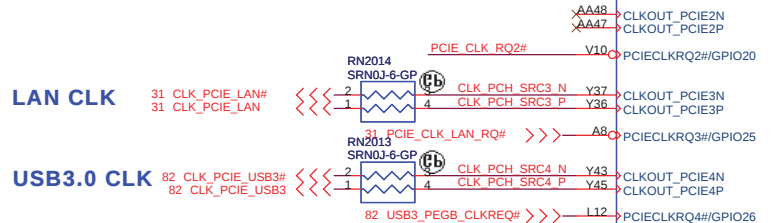
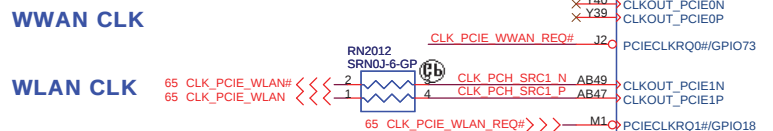
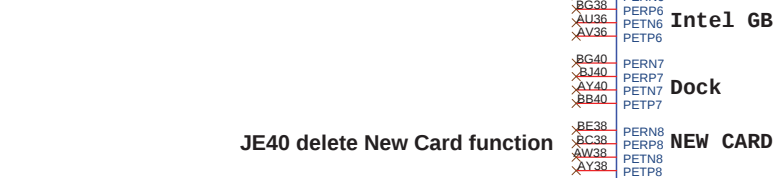
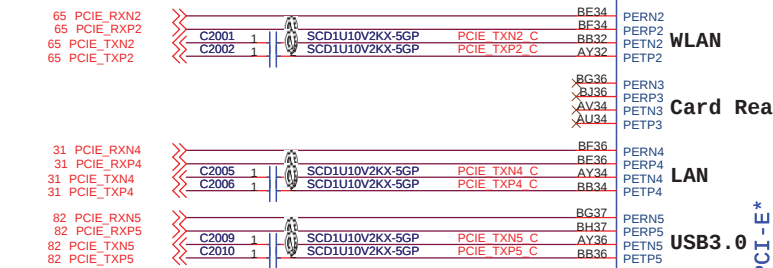


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Taipei Hsien 221, Taiwan, R.O.C.

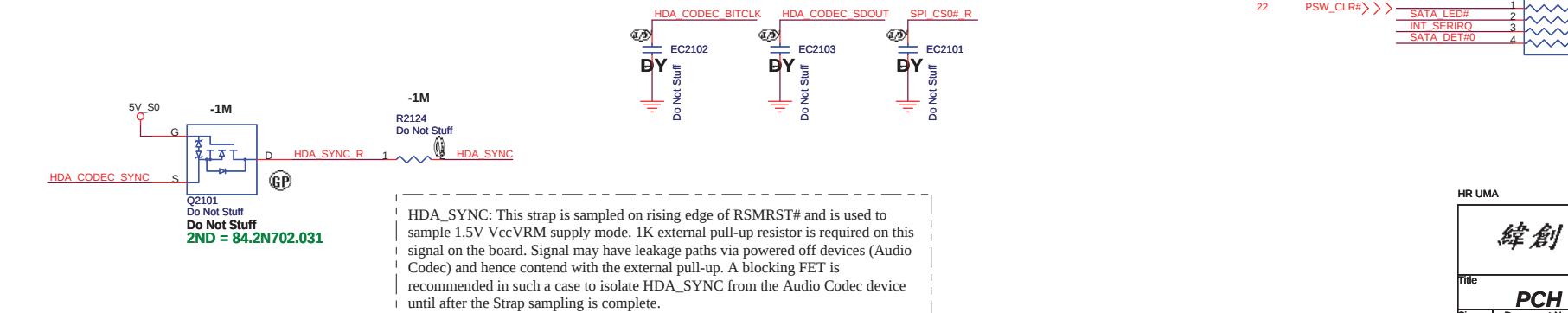
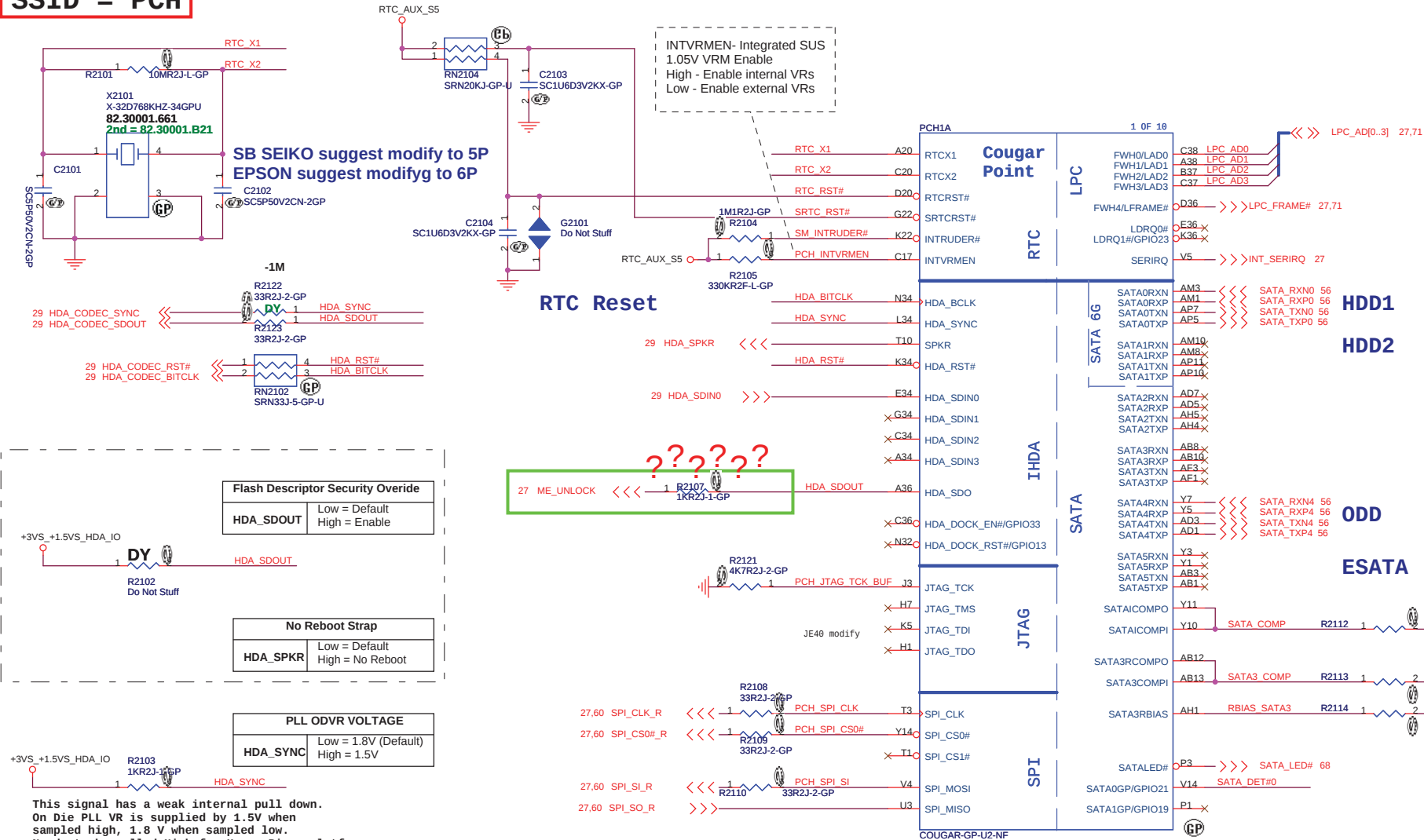
Title PCH (DM I/FDI/PM)
Size A3 Document Number JE40-HR
Date: Thursday, December 02, 2010 Sheet 19 of 102
Rev -1

SSID = PCH



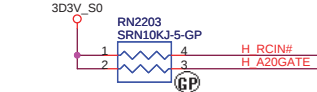
- Prioritize 27/14/24/48/25-MHz FLEX on FLEX1 and FLEX3
- Do not configure 27/14/24/48/25-MHz FLEX clock on FLEX0 and FLEX2 if more than 2 PCI clocks + PCI loopback are routed.

SSID = PCH

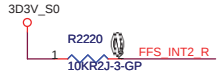


SSID = PCH

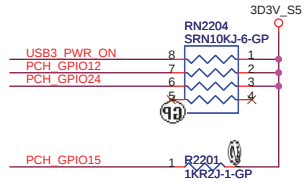
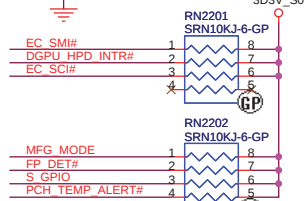
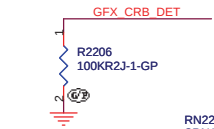
Note:
For PCH debug with XDP, need to NO STUFF R2218



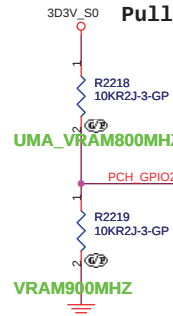
GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



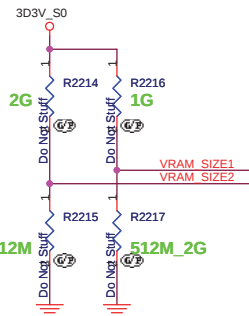
	INTERNAL GFX	EXTERNAL GFX
R2205	DY	10K
R2206	100K	DY



SB VRAM Frequency
Pull high: 800MHZ
Pull low :900MHZ

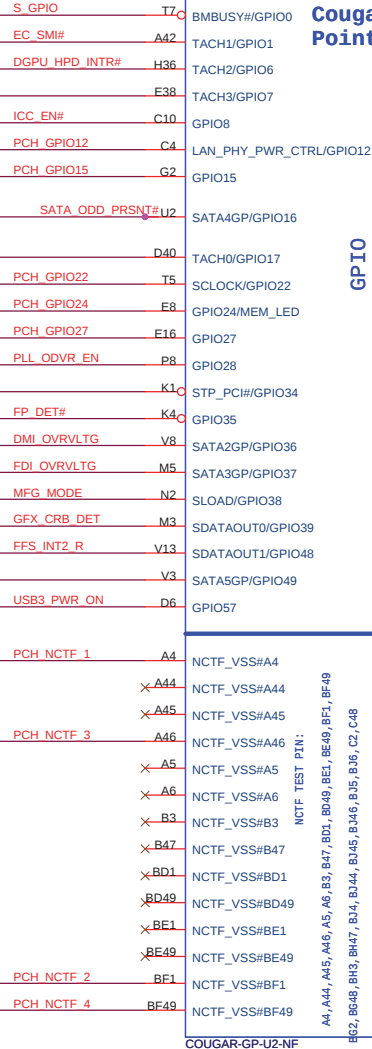
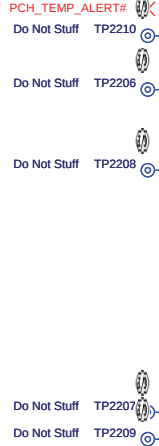


VRAM Size



Pass Word Clear

JE40 delete G Sensor

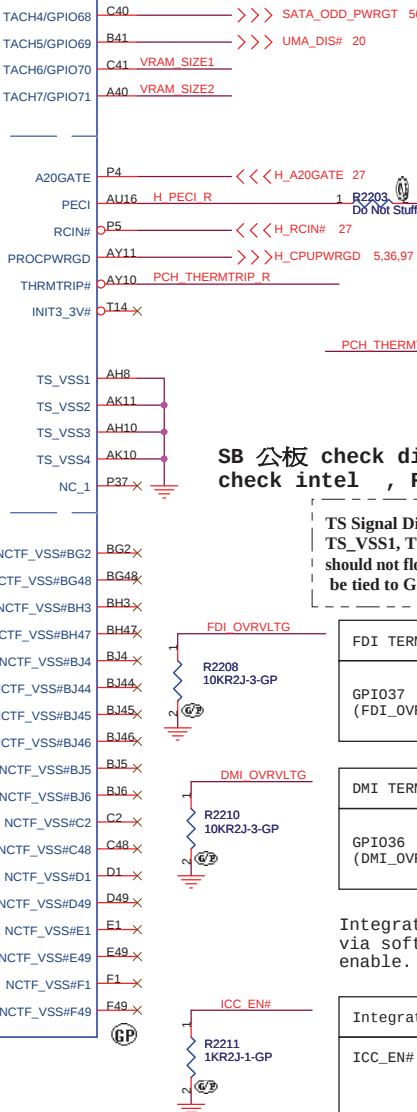


Cougar Point

GPIO

NCTF

SB add Zero ODD function



TS Signal Disable Guideline:
TS_VSS1, TS_VSS2, TS_VSS3 and TS_VSS4
should not float on the motherboard. They should
be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT] LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up.
Integrated Clock Enable functionality is achieved
via soft-strap. The default is integrated clock
enable.

PLL ON DIE VR ENABLE
NOTE: This signal has a weak internal pull-up 20K
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT
DISABLED -- LOW (R2212 STUFFED)

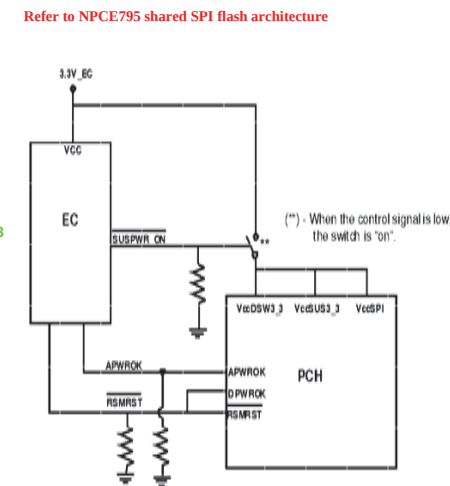
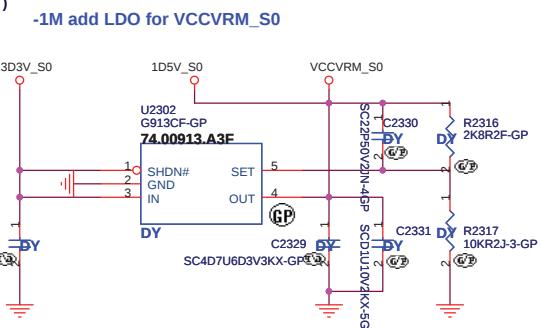
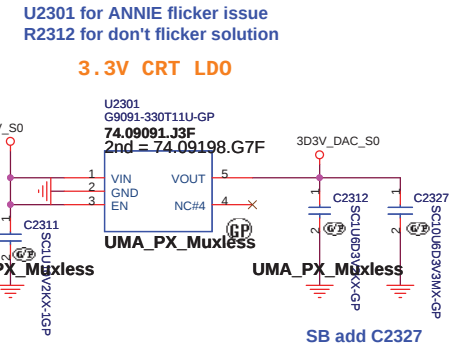
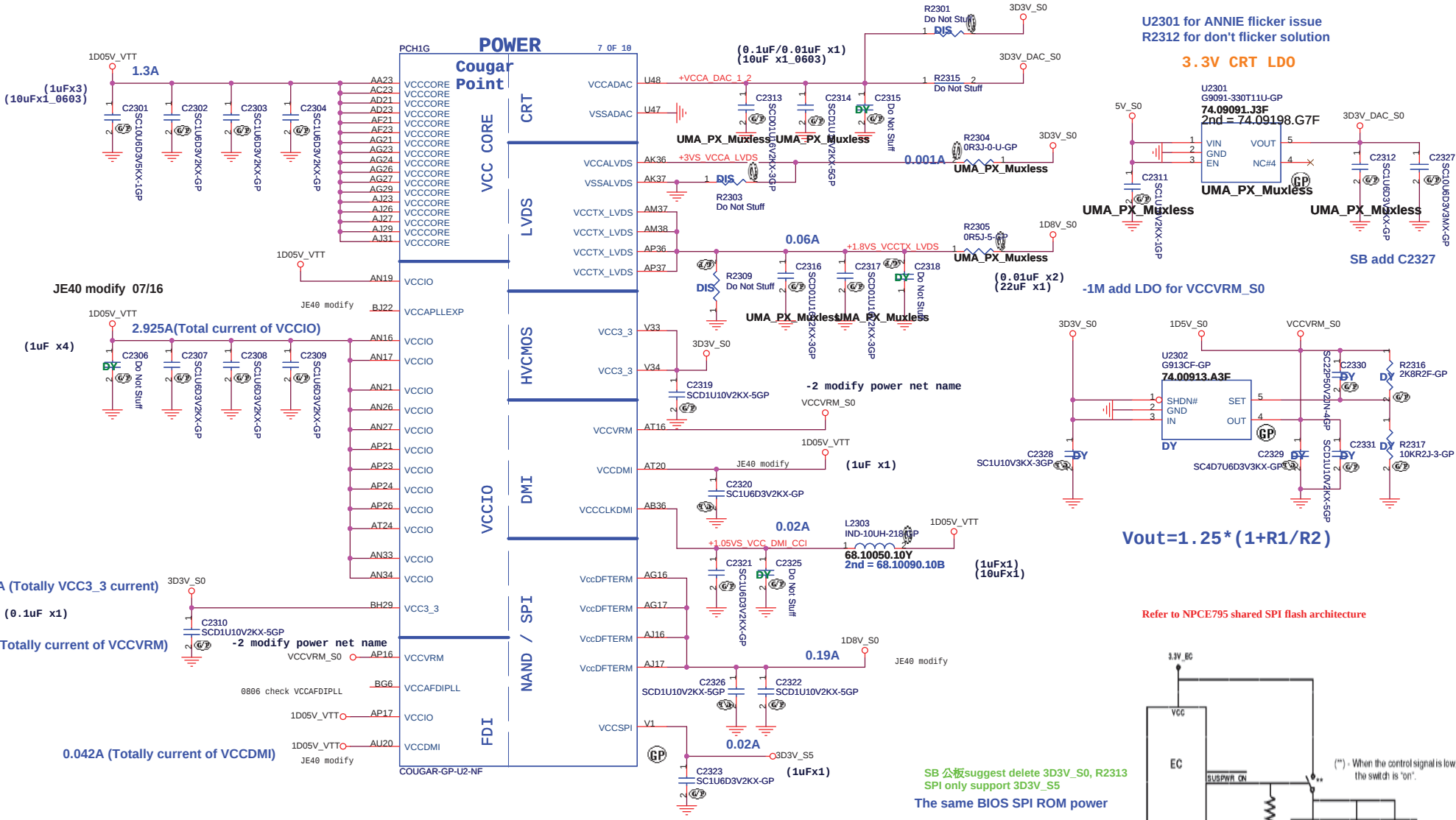
HR UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (GPIO/CPU)

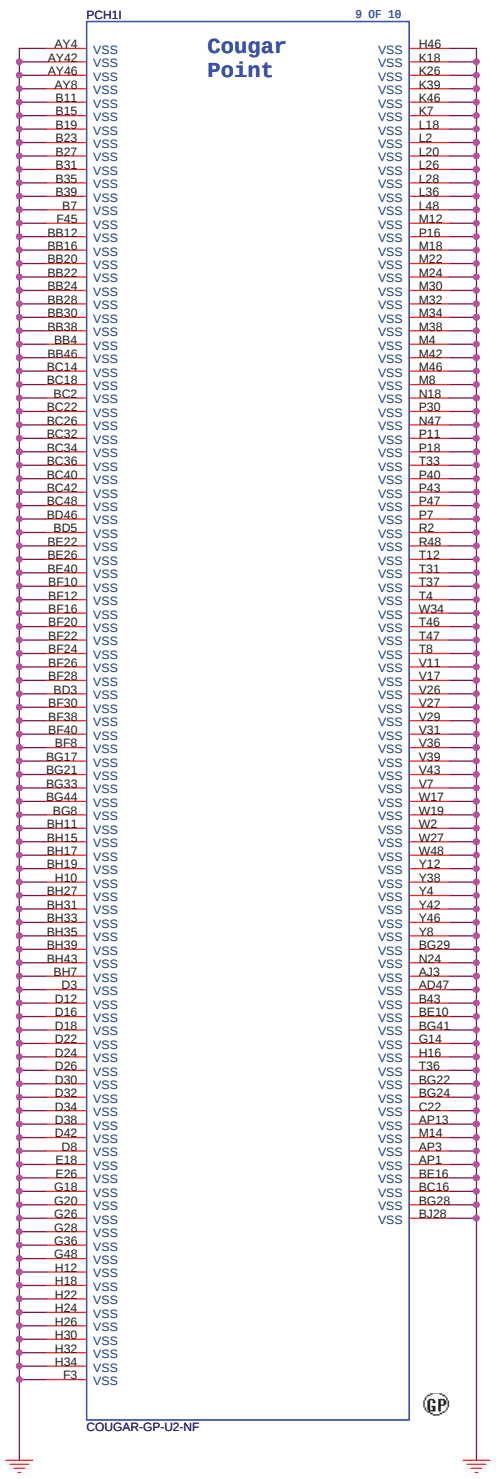
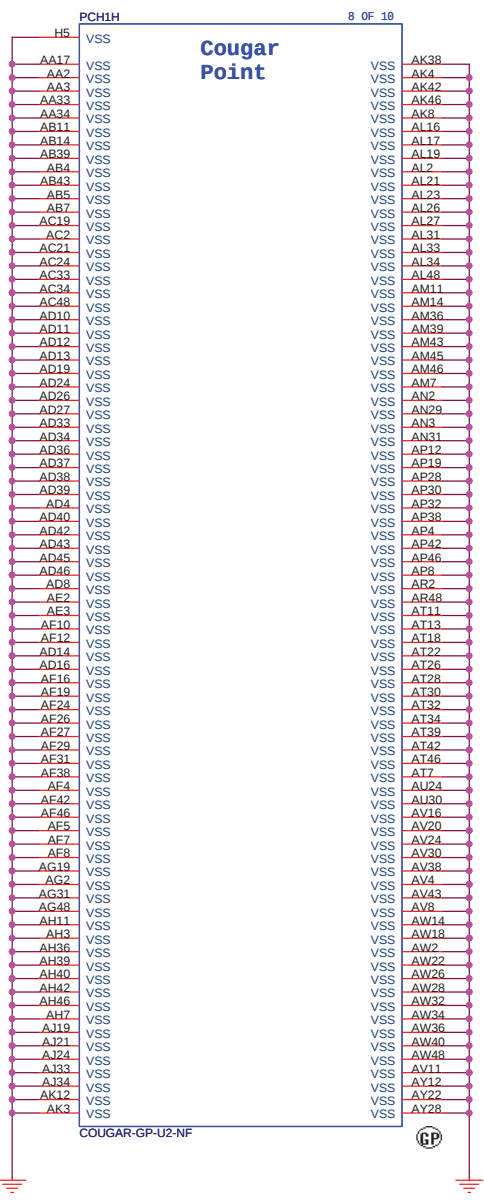
Size: A3 Document Number: JE40-HR Rev: -1

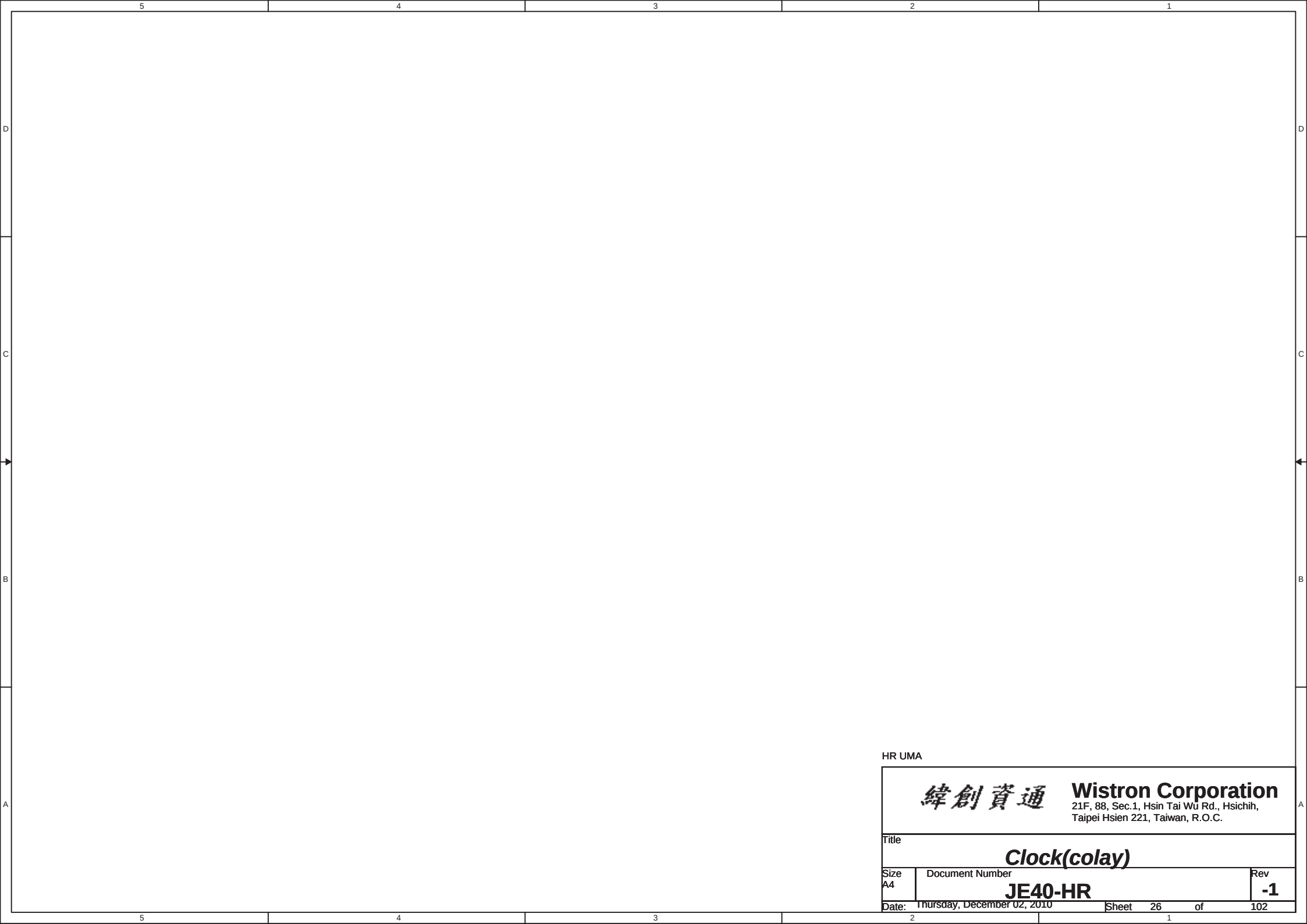
Date: Thursday, December 02, 2010 Sheet: 22 of 102



SB 公板 suggest delete 3D3V_S0, R2313
SPI only support 3D3V_S5
The same BIOS SPI ROM power

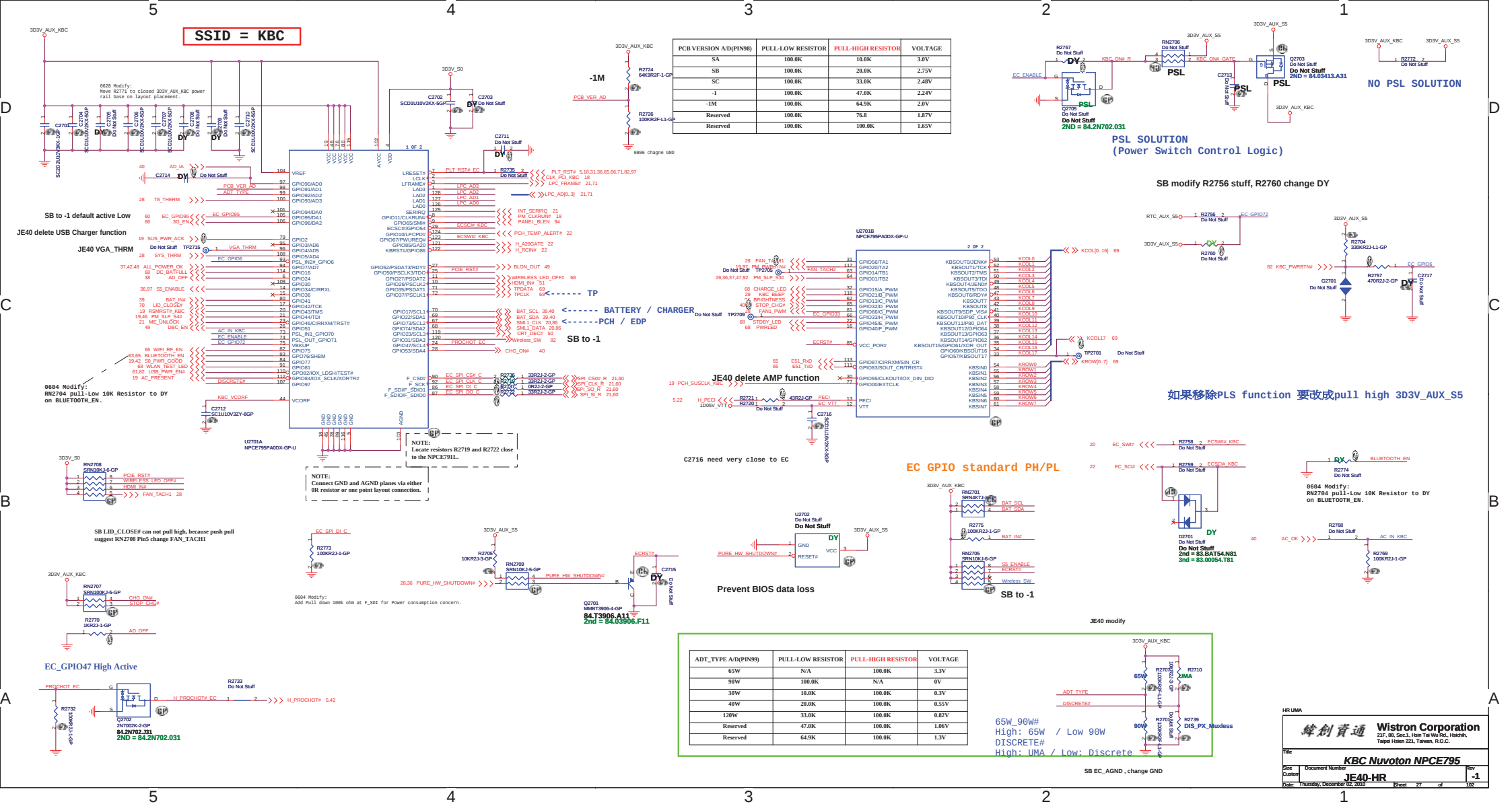
SSID = PCH





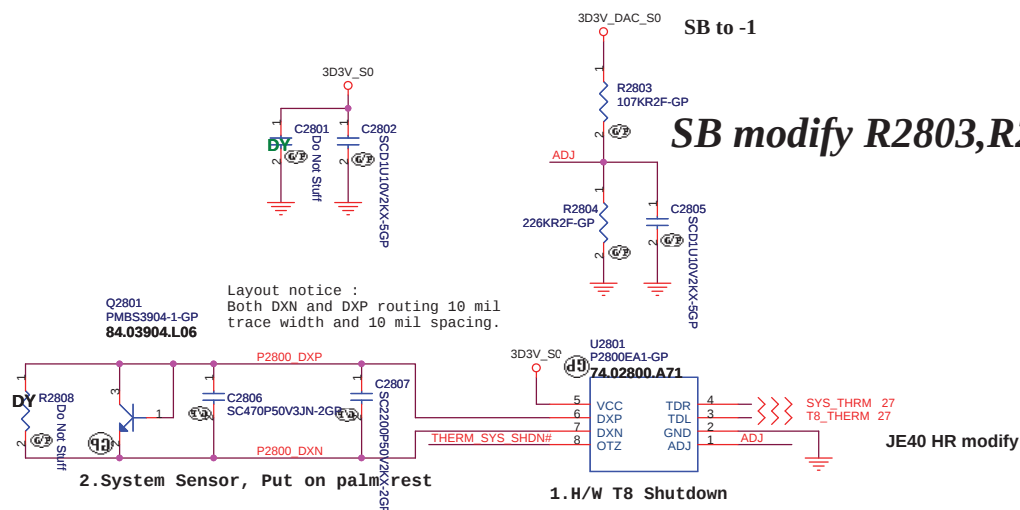
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Clock(colay)		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 26 of 102



SSID = Thermal

Thermal sensor P2800



ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 $\pm 1\%$ Series)

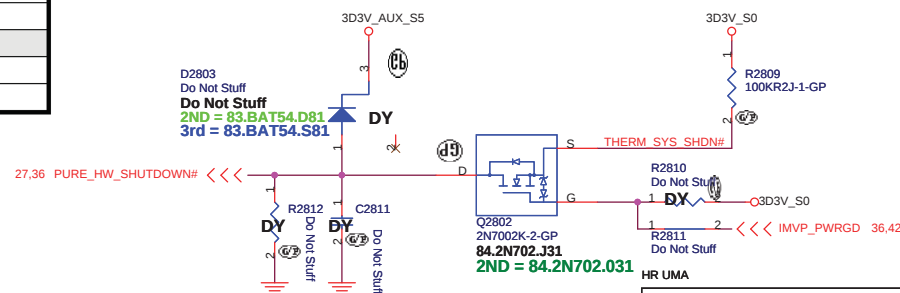
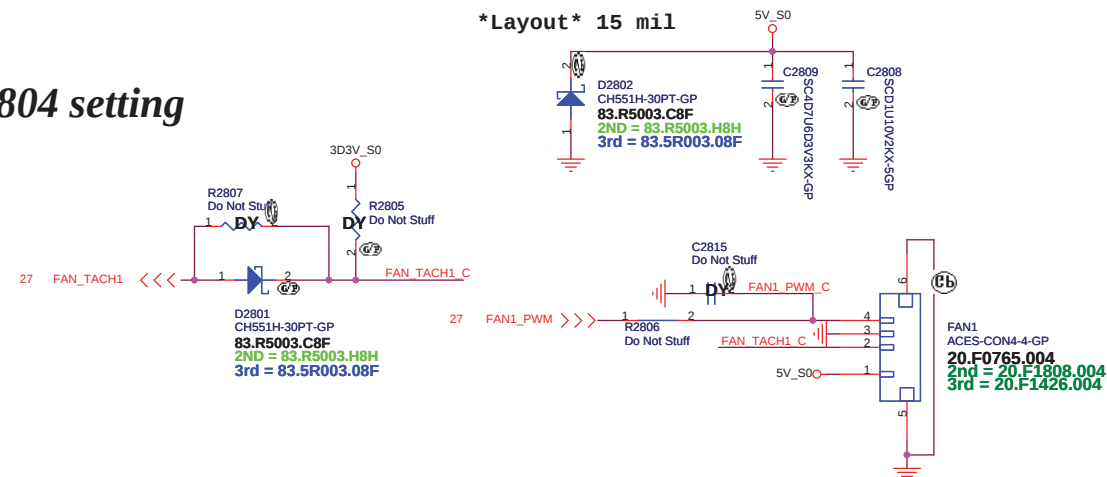
RADJ1 (K Ω)	RADJ2 (K Ω)	VADJ (V)	OTZ Threshold Temperature ($^{\circ}$ C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

VGA Thermal sensor P2800

SMBUS modify to Page 84

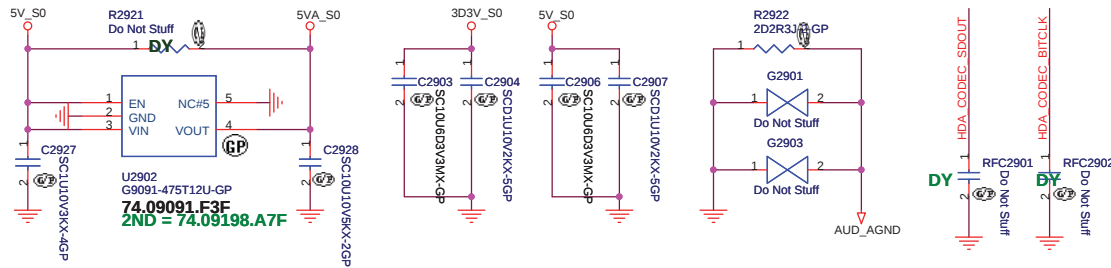
Fan controller P2793

Layout 15 mil



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Taipei Hsien 221, Taiwan, R.O.C.

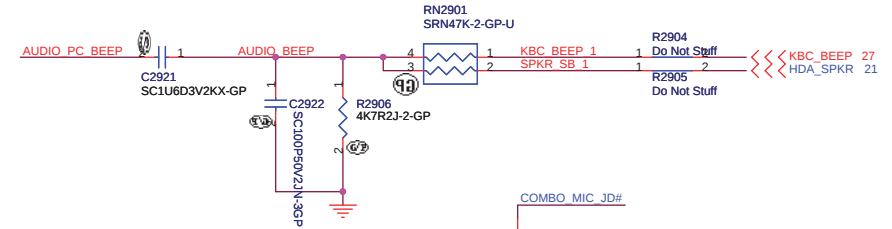
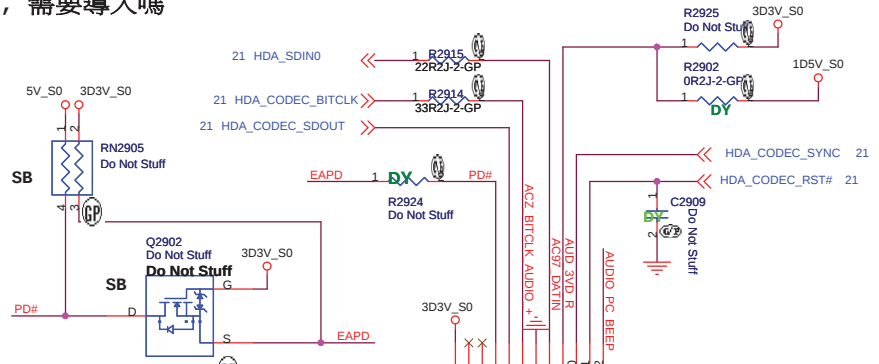
Title		
Thermal P2800/Fan Controller P2793		
Size	Document Number	Rev
Custom	JE40-HR	-1
Date:	Thursday, December 02, 2010	Sheet 28 of 102



CLOSE TO PIN39 and 46

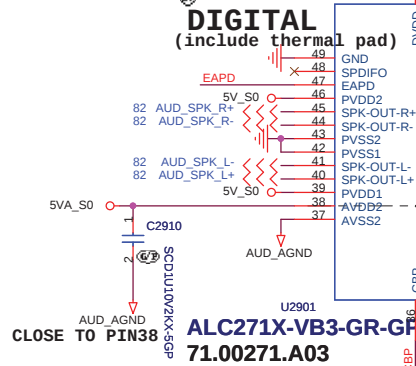
-1 PVDD timing 需要比 AVDD晚, 使用PW 74.00545.079 去開
vensor suggest , 需要導入嗎

CLOSE TO PIN1 and 9

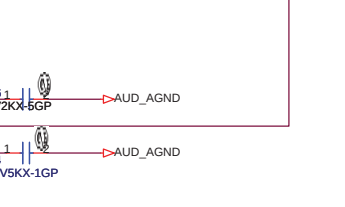
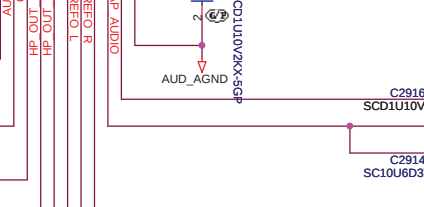
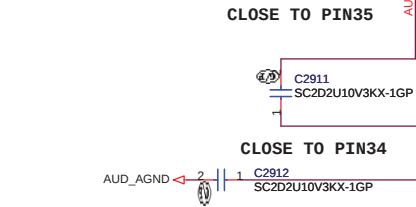
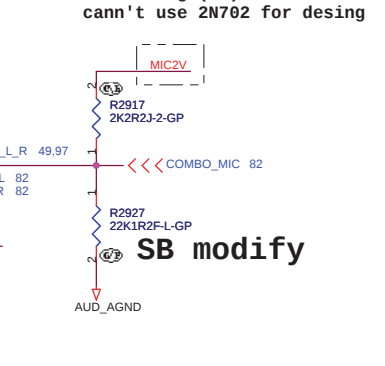
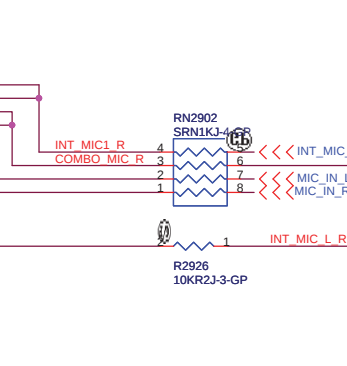
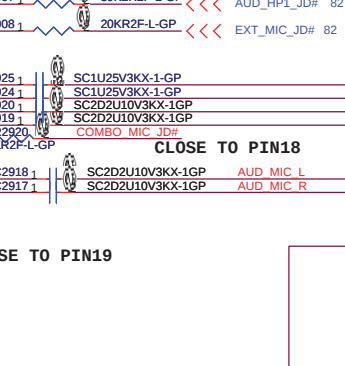
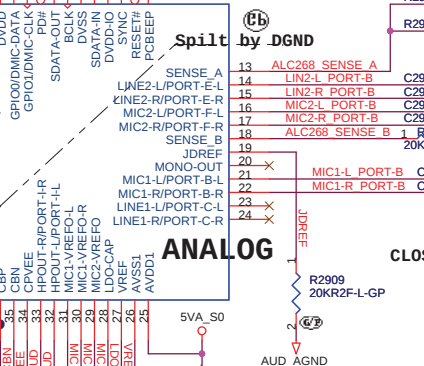


Q2901
BSS138-7F-GP
84.00138.F31
2ND = 84.00138.H31
Max Vgs(th) 1.8V

MIC2V Ref voltage is 2.5V
because Vgs(th) concern
cann't use 2N702 for desing



ALC271X-VB3-GR-GP
71.00271.A03



HR UMA

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Audio Codec			
Size A3	Document Number	Rev -1	
JE40-HR			
Date: Thursday, December 02, 2010	Sheet 29	of	102

AUDIO OP AMPLIFIER

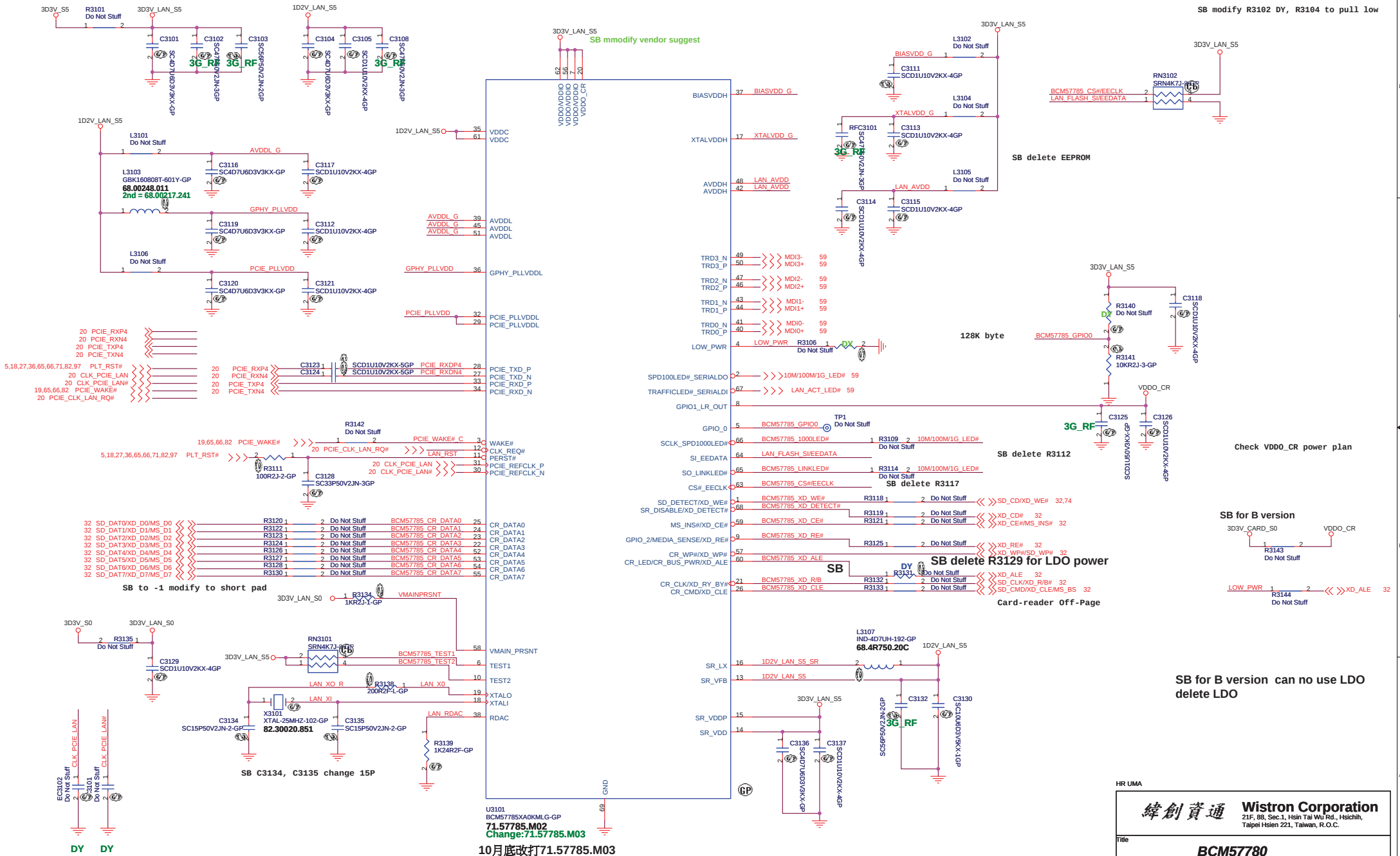
JE40 delete AMP function

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Audio AMP		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 30 of 102

SB modify L3101,2,4,5,6 to 0 ohm

SB modify R3102 DY, R3104 to pull low

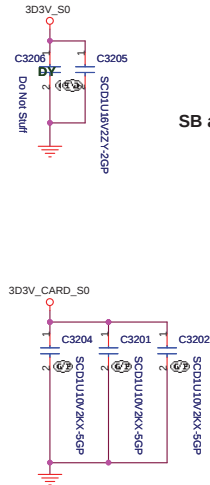


SB for B version can no use LDO
delete LDO

HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

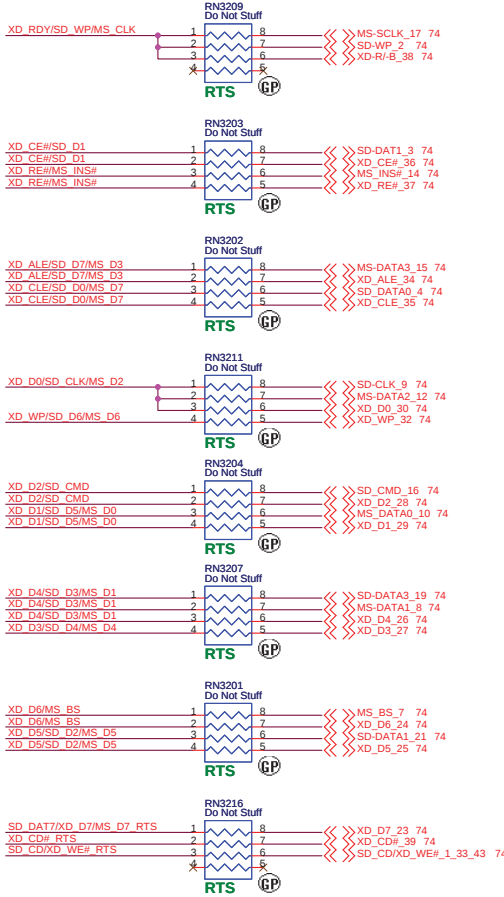
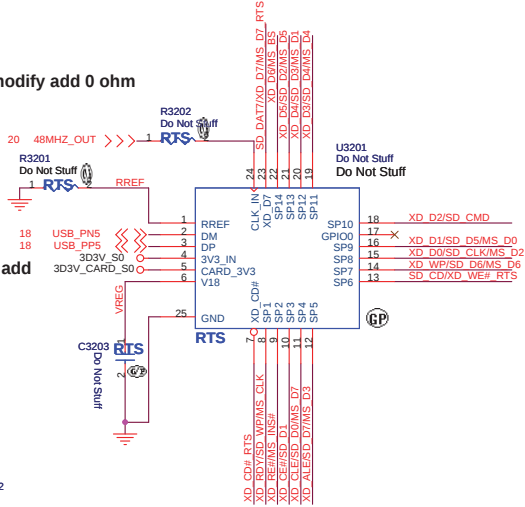
Title			
BCM57780			
Size Custom	Document Number		Rev
	JE40-HR		-1
Date:	Thursday, December 02, 2010	Sheet 31 of	102



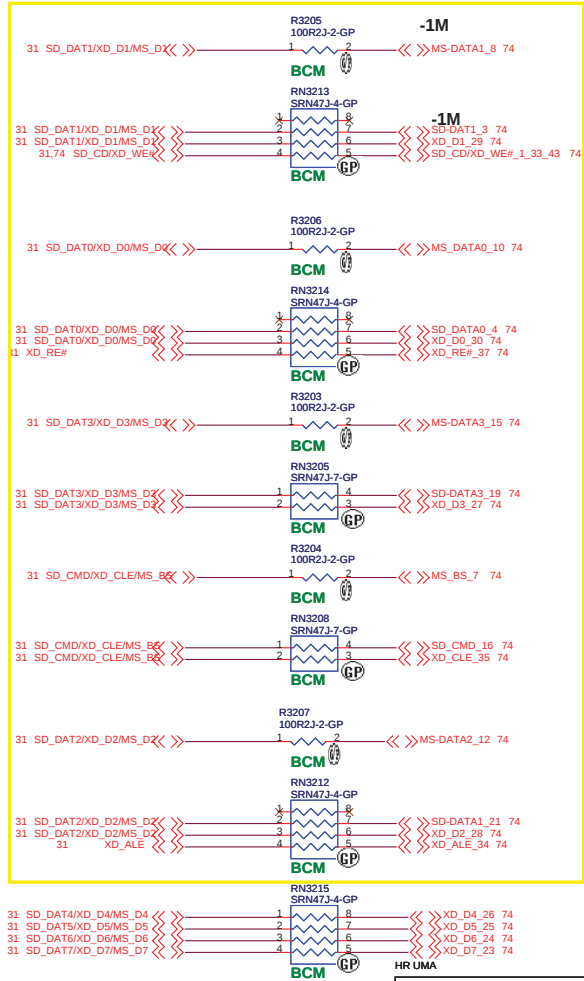
SB modify add 0 ohm

SB add

Near CARD1 Pin11, Pin18, Pin22



SB to -1



(Blanking)

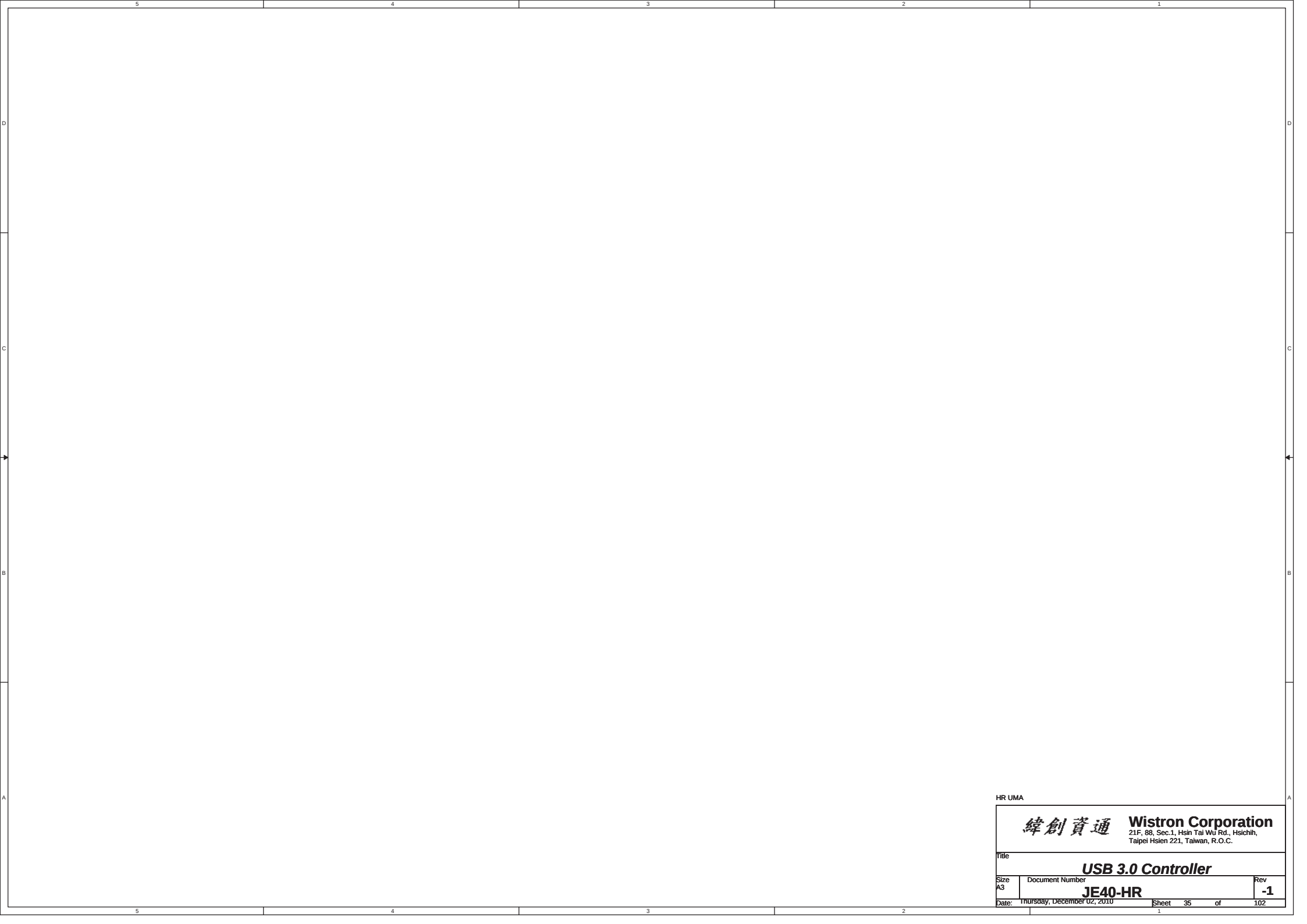
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 33 of 102

(Blanking)

HR UMA

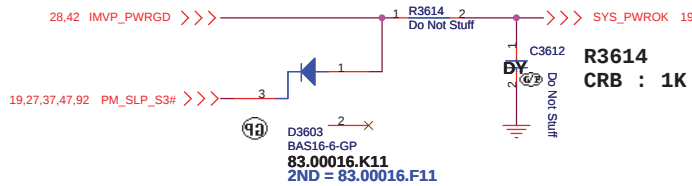
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 34 of 102



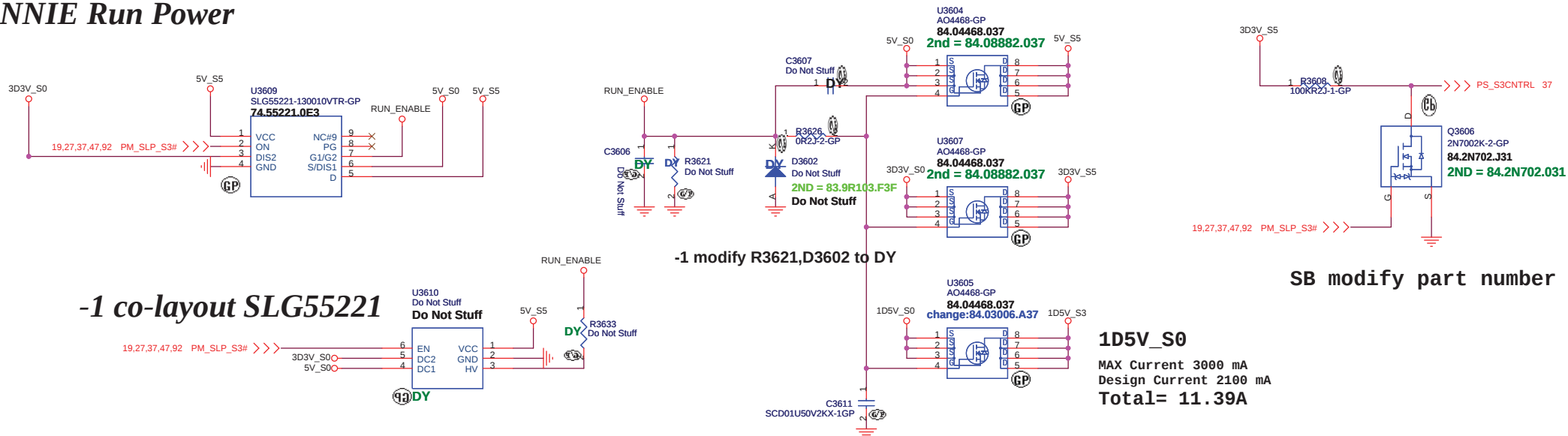
HR UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 3.0 Controller			
Size A3	Document Number		Rev
JE40-HR		-1	
Date:	Thursday, December 02, 2010		Sheet 35 of 102

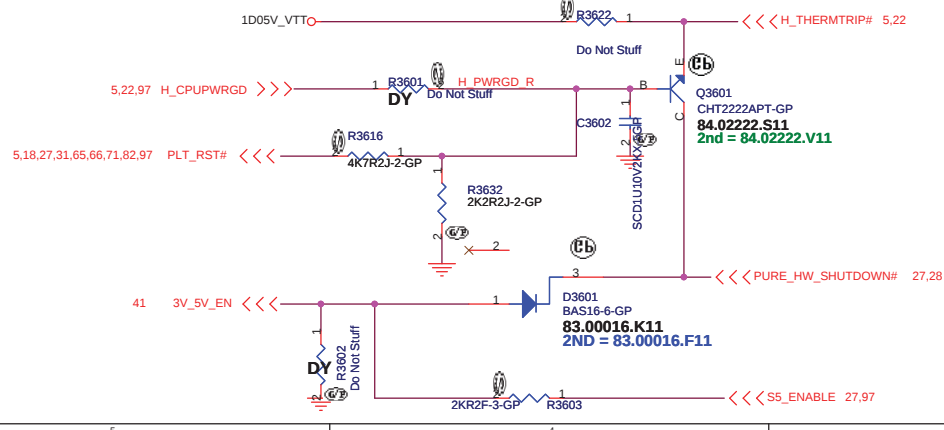
Power Sequence



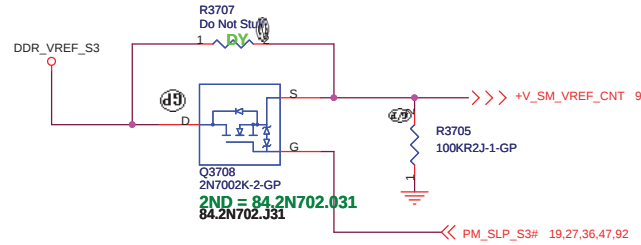
ANNIE Run Power



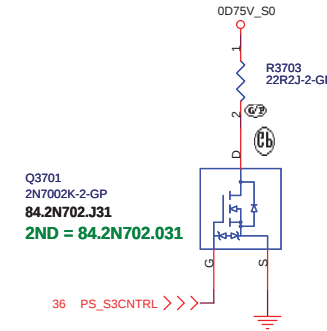
SB



Close to CPU
S3 Power Reduction Circuit Processor VREF_DQ Implementation

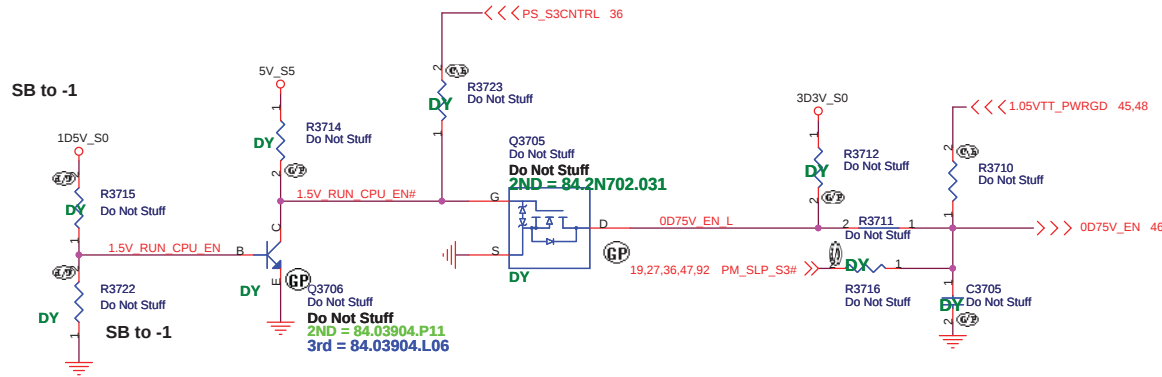


Close to DIMM
S3 Power Reduction Circuit SM_DRAMPWROK

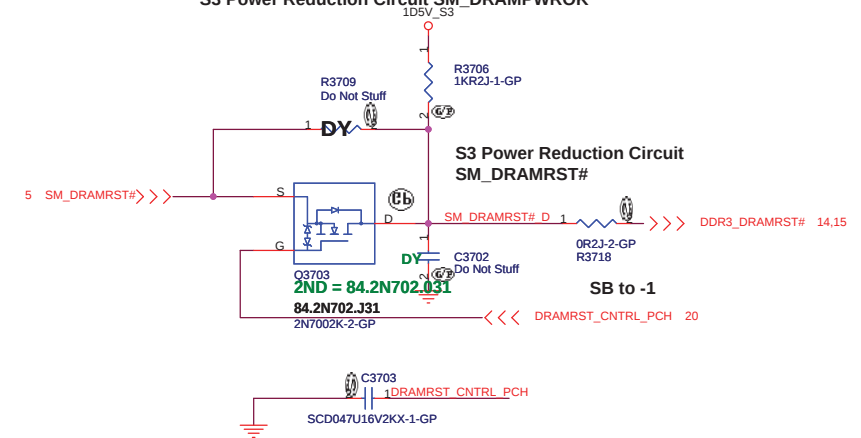


5 S3 Power Reduction X01 20091111 JE40 HR modify 驗證R3710上件

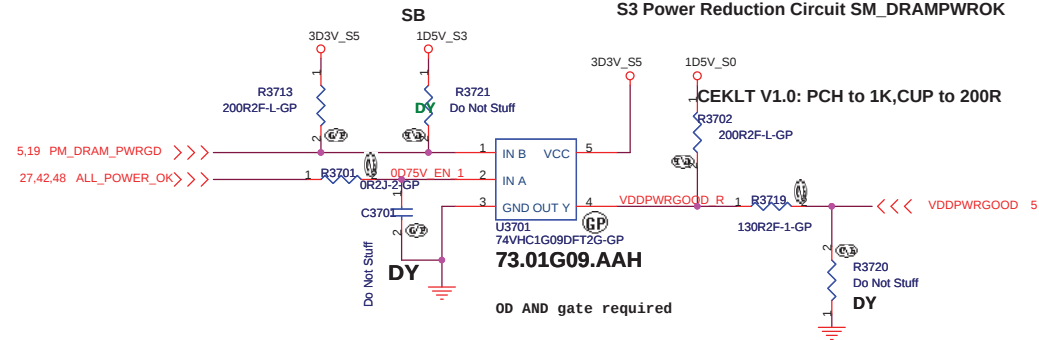
SB to -1 reserve R3723



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



Close to CPU
S3 Power Reduction Circuit SM_DRAMPWROK



For U3701 not OD AND gate
R3719 to 64.15015.6DL
R3720 to 64.75005.6DL
R3702 to DY

SM_DRAMPWROK must have a maximum of 15ns rise or fall time over VDDQ * 0.55± 200mV and the edge must be monotonic

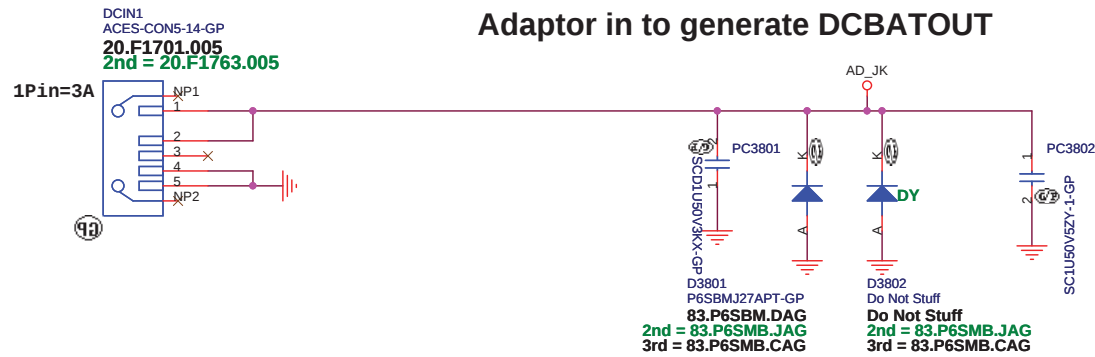
HR UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

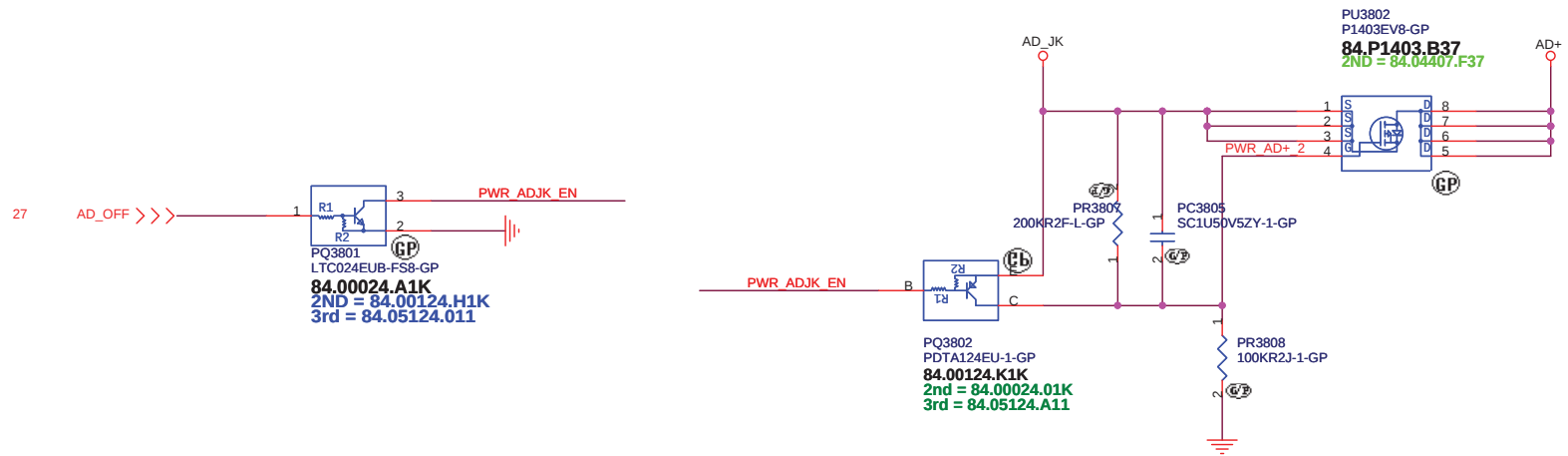
Title			ADAPTER	
Size	Document Number	Rev		
A3	JE40-HR	-1		
Date:	Thursday, December 02, 2010	Sheet	37	of 102

ANNIE solution

Adaptor in to generate DCBATOUT



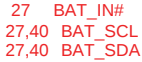
JE40 change DCIN1 part number



HR UMA

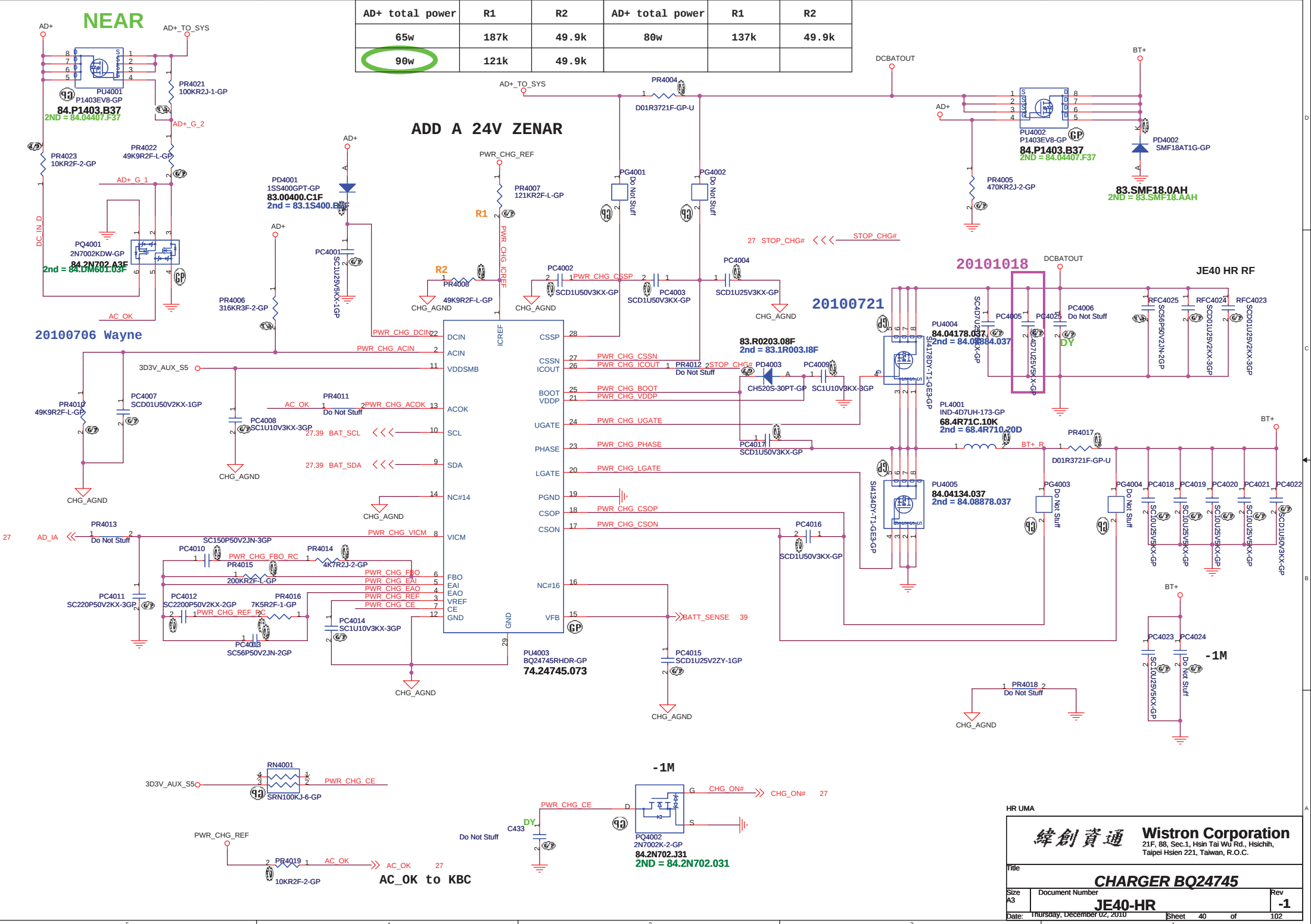
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title DCIN JACK			
Size	Document Number		Rev
Custom	JE40-HR		-1
Date:	Thursday, December 02, 2010	Sheet	38 of 102

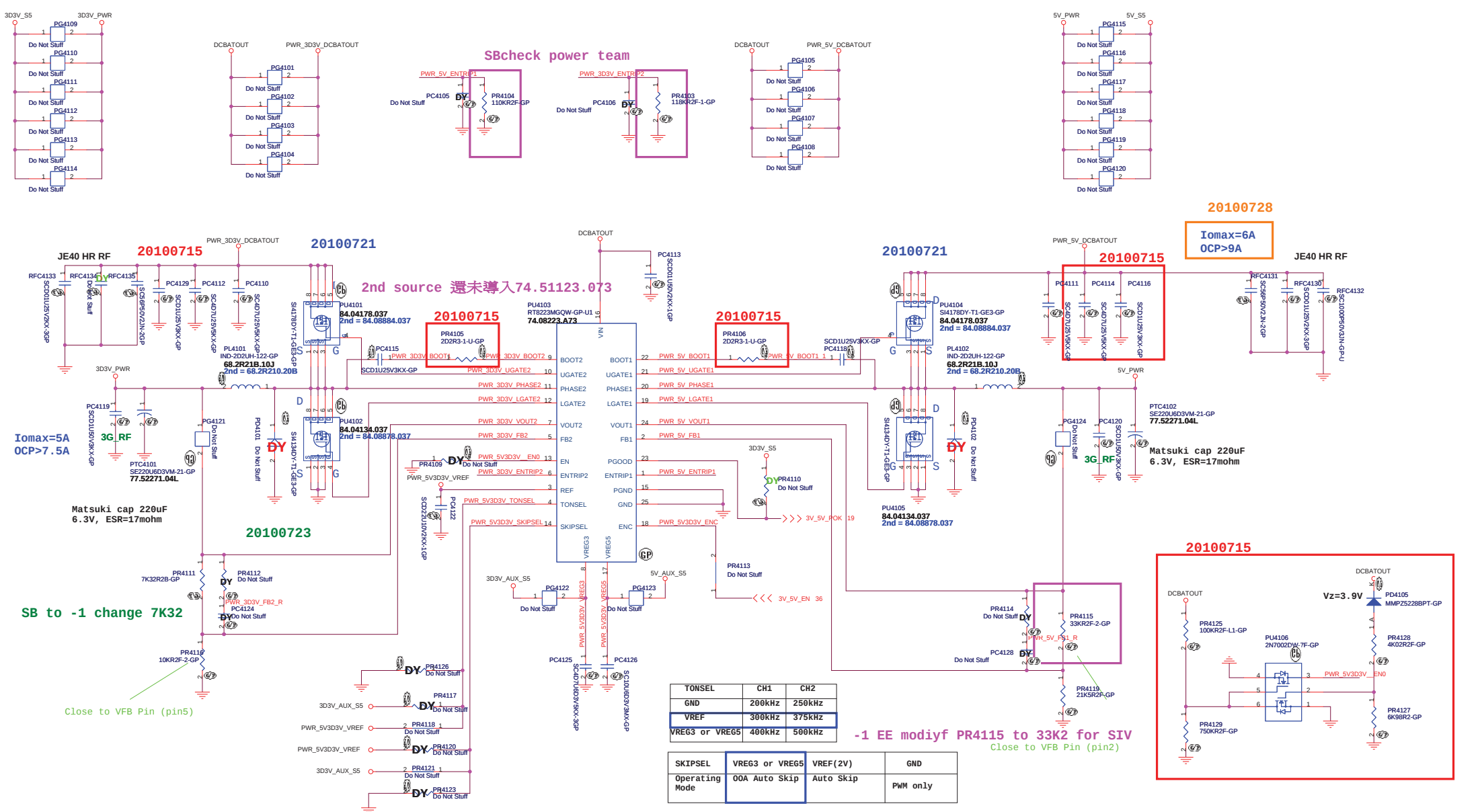
BATTERY CONNECTOR

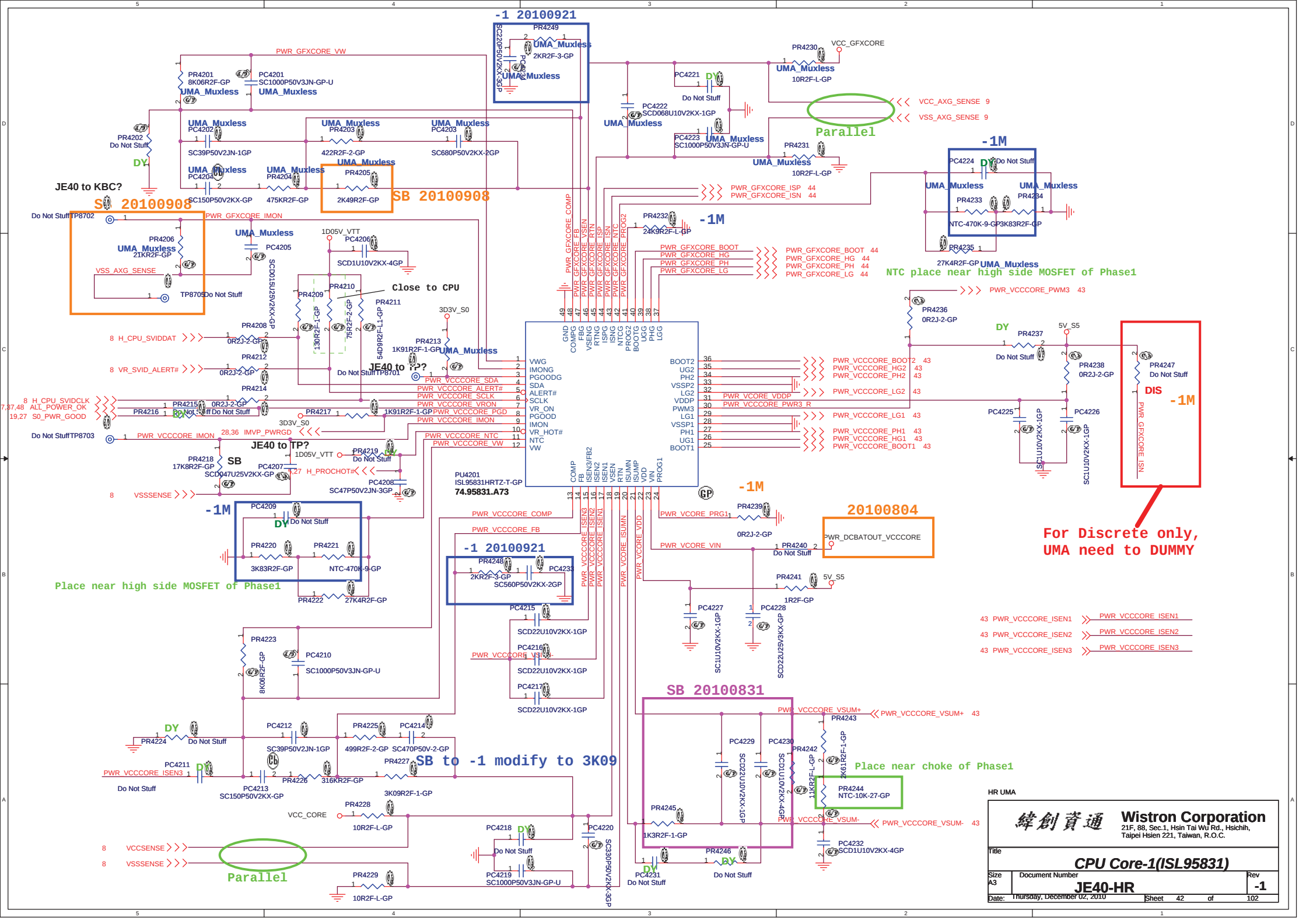


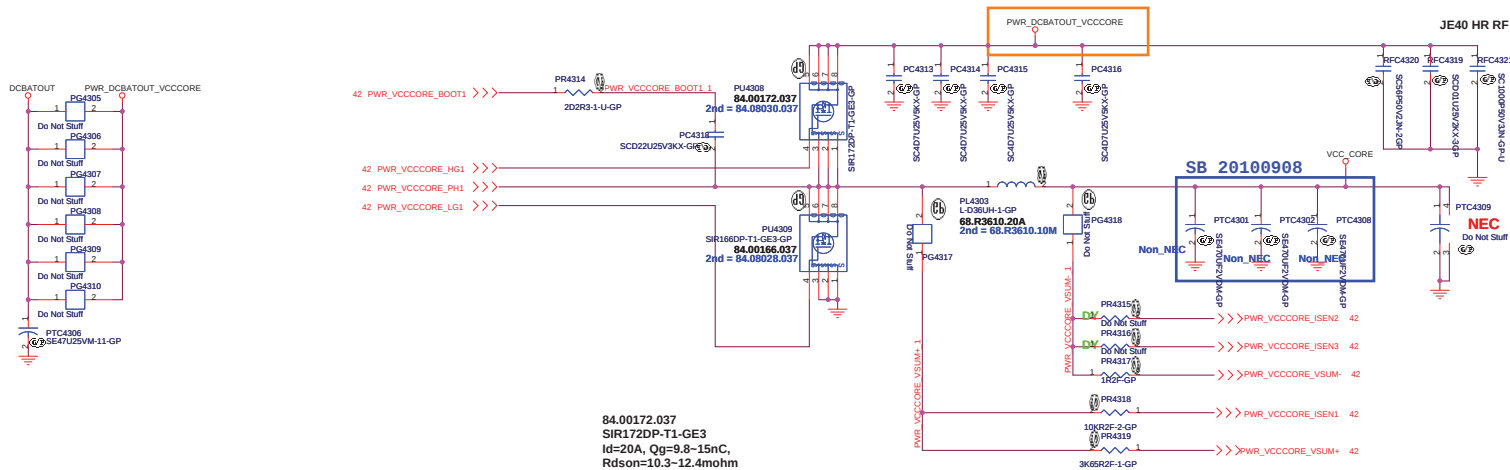
EC Protect

AD+ total power	R1	R2	AD+ total power	R1	R2
65w	187k	49.9k	80w	137k	49.9k
90w	121k	49.9k			

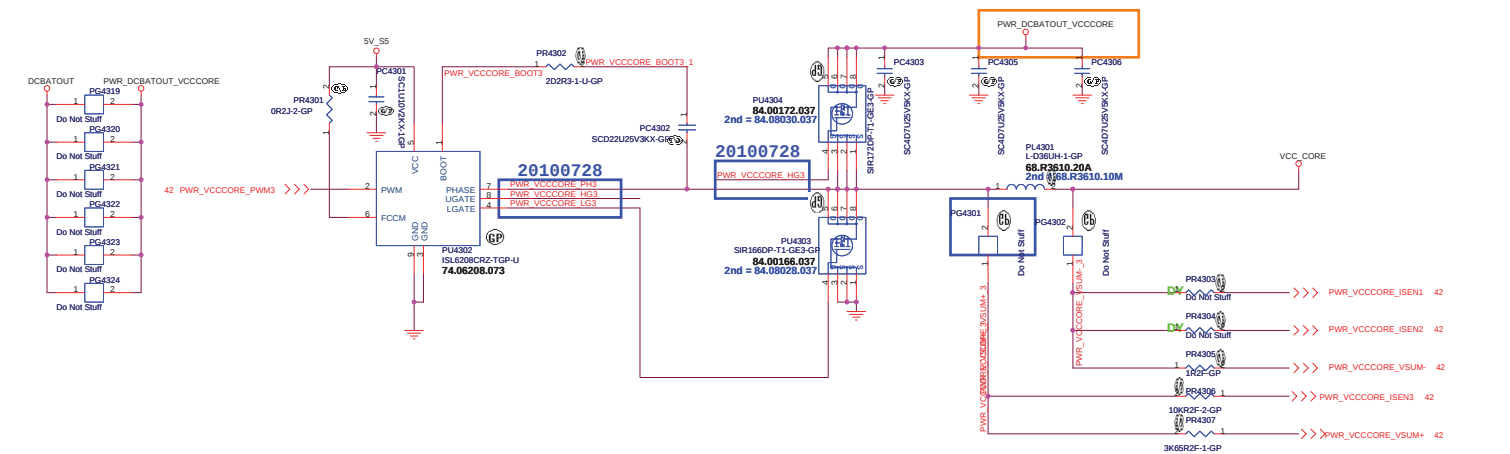
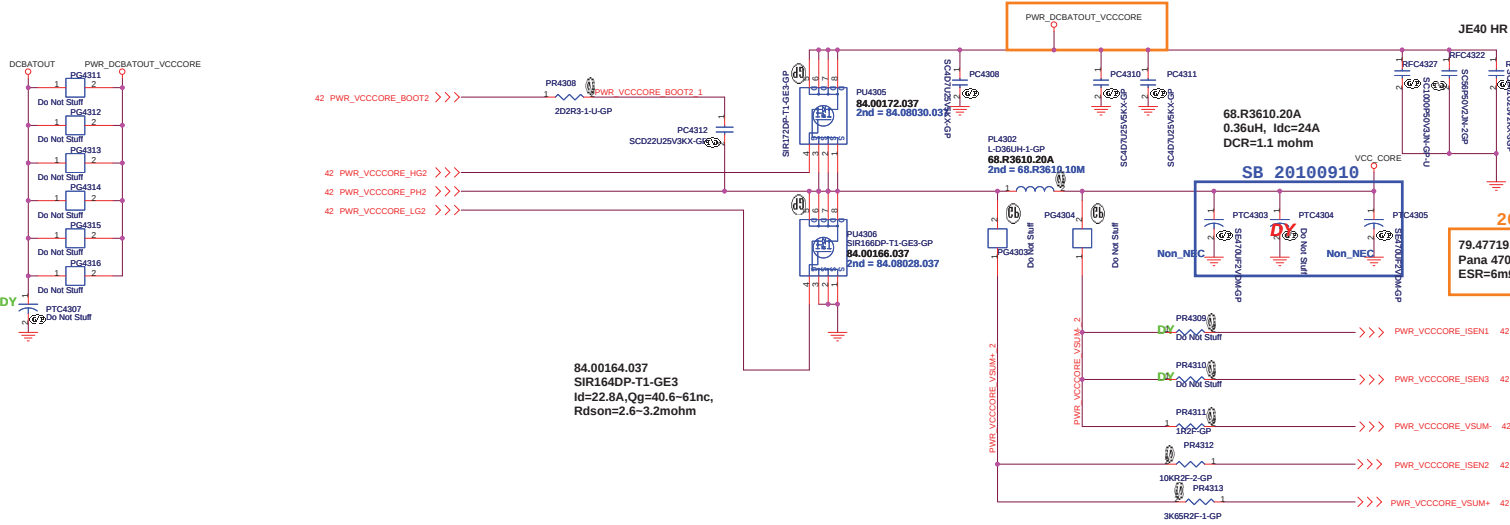


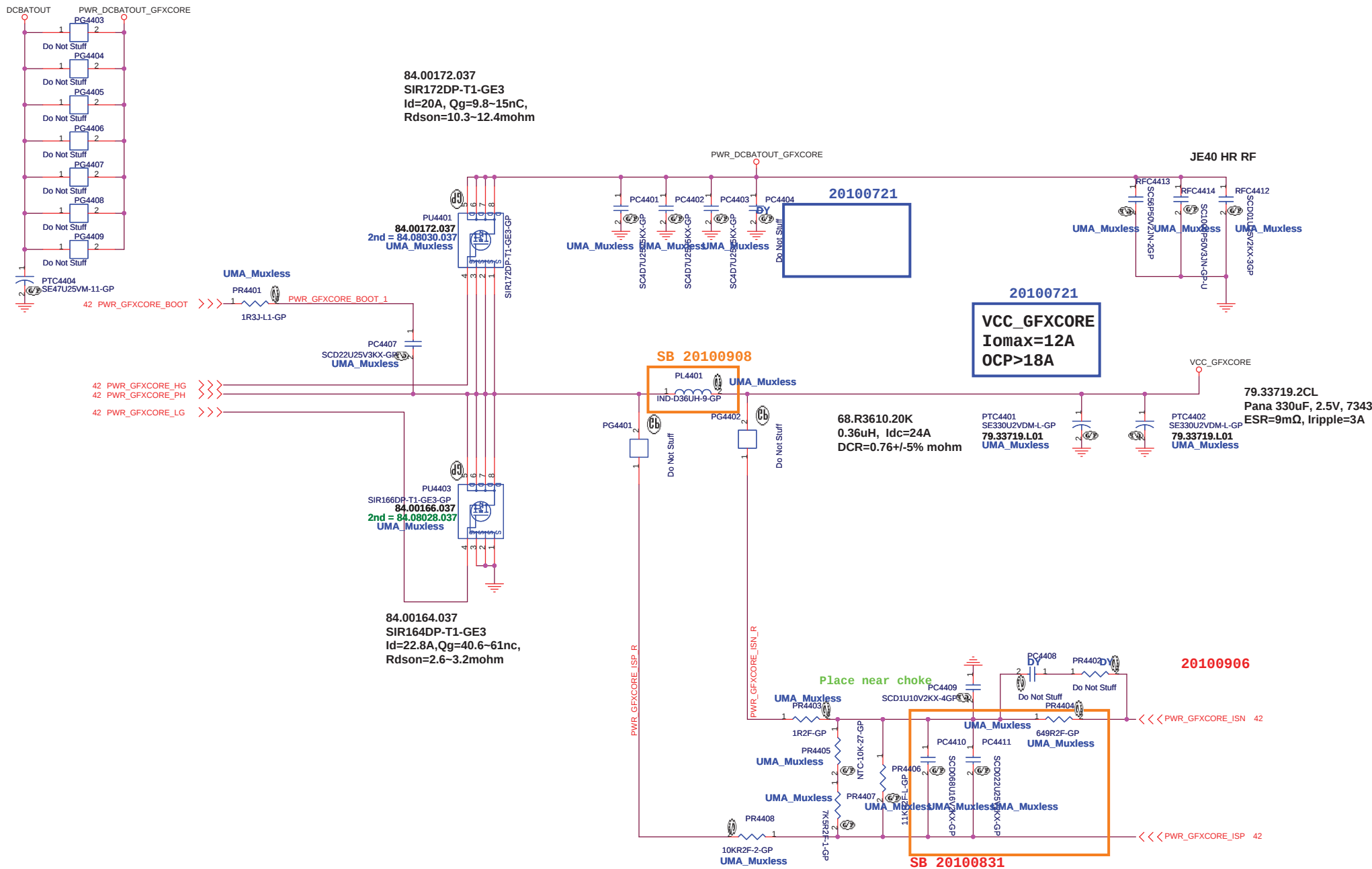




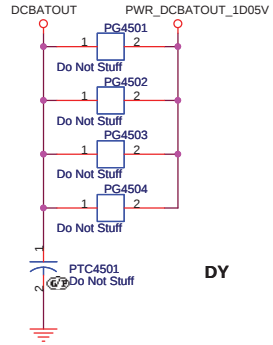


Vcc_core
Iomax=53A
OCP>97.5A

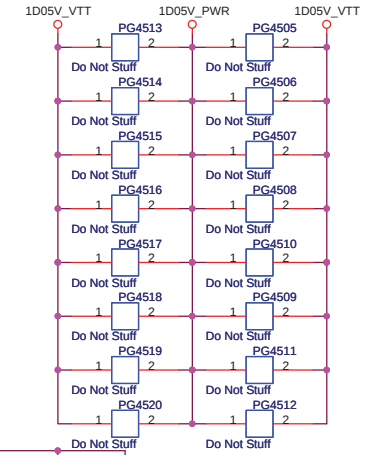
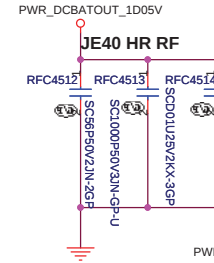




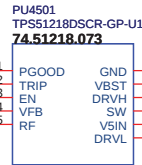
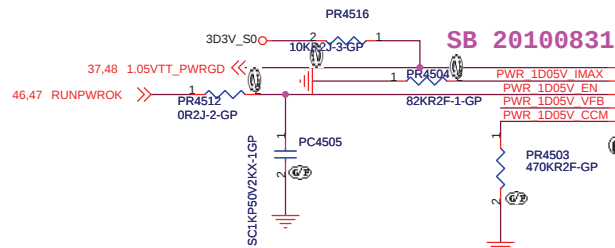
TPS51218D for 1D05V



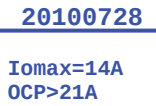
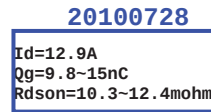
DY



2nd source 還未導入 74.08237.073

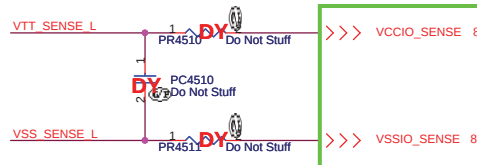
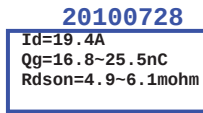
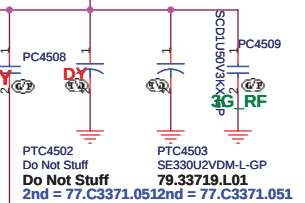


Freq=360KHz



Mag. 0.56uH 10*10*4
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

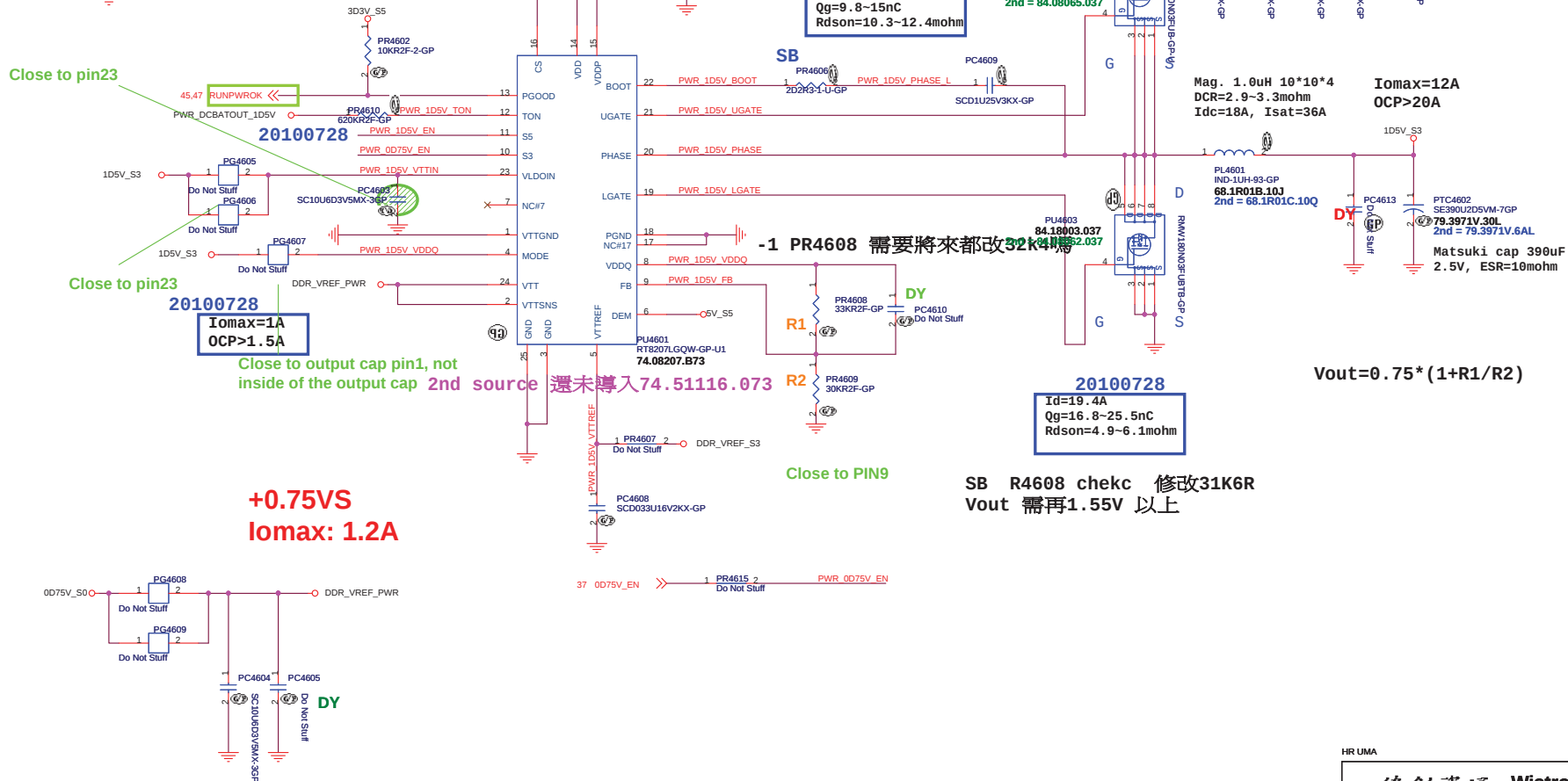
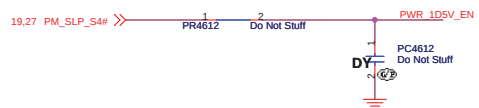
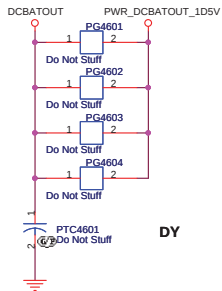
20100906



$$V_{out} = 0.704 * (1 + R1/R2)$$

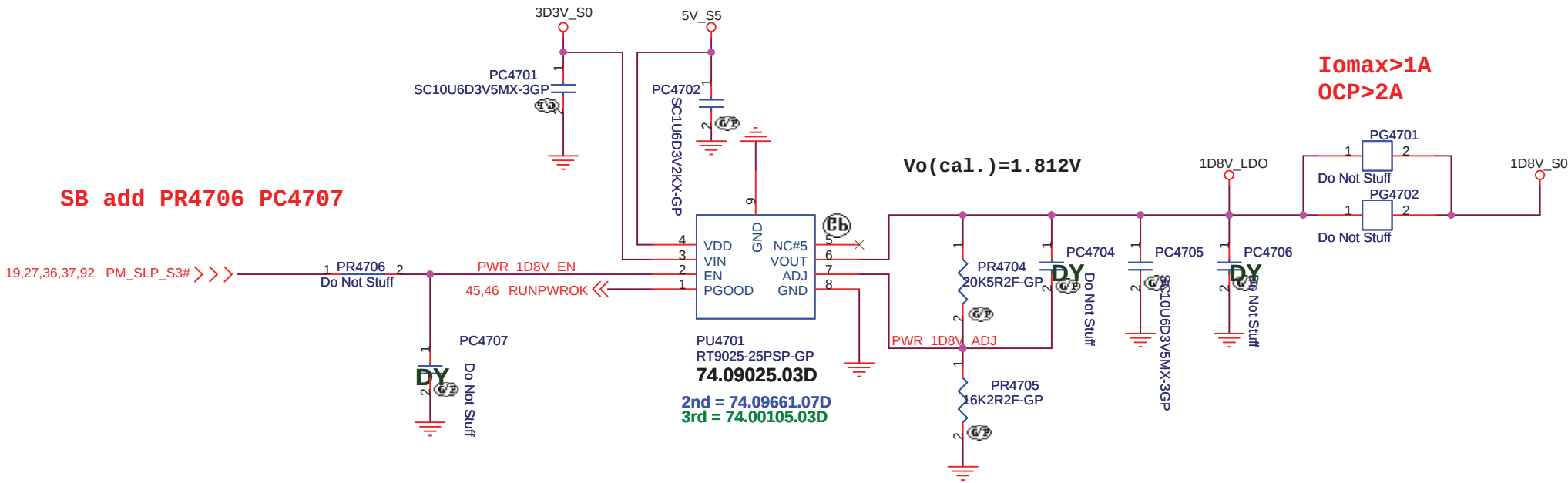
HR UMA

```
SSID = PWR.Plane.Regulator_1p5v0p75v
```



SSID = PWR.Plane.Regulator_1p8v

RT9025 for 1D8V_S0



HR UMA

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Title

LDO 1D8V(RT9025)

Size

Document Number

Rev

JE40-HR

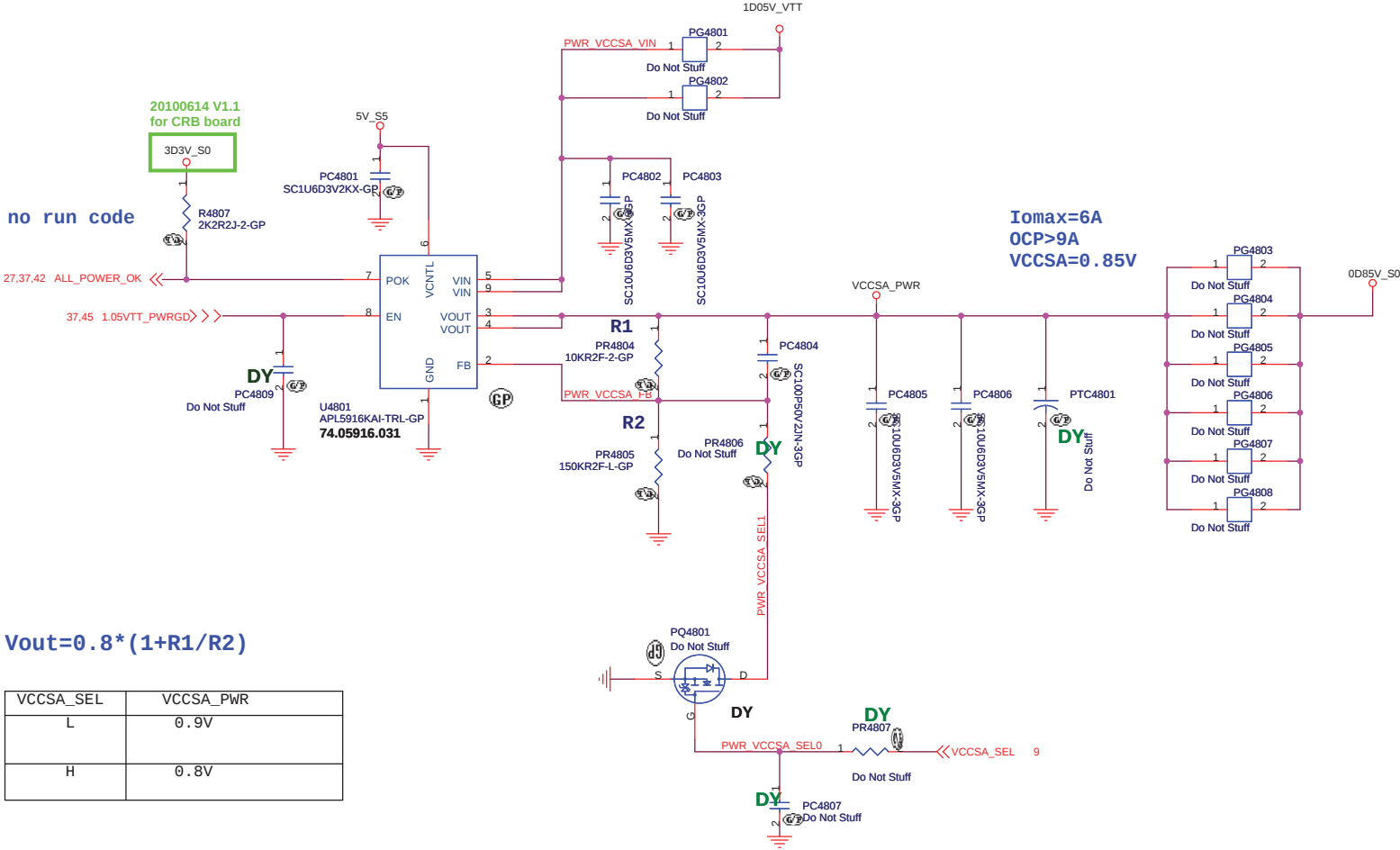
-1

Date: Thursday, December 02, 2010

Sheet 47 of 102

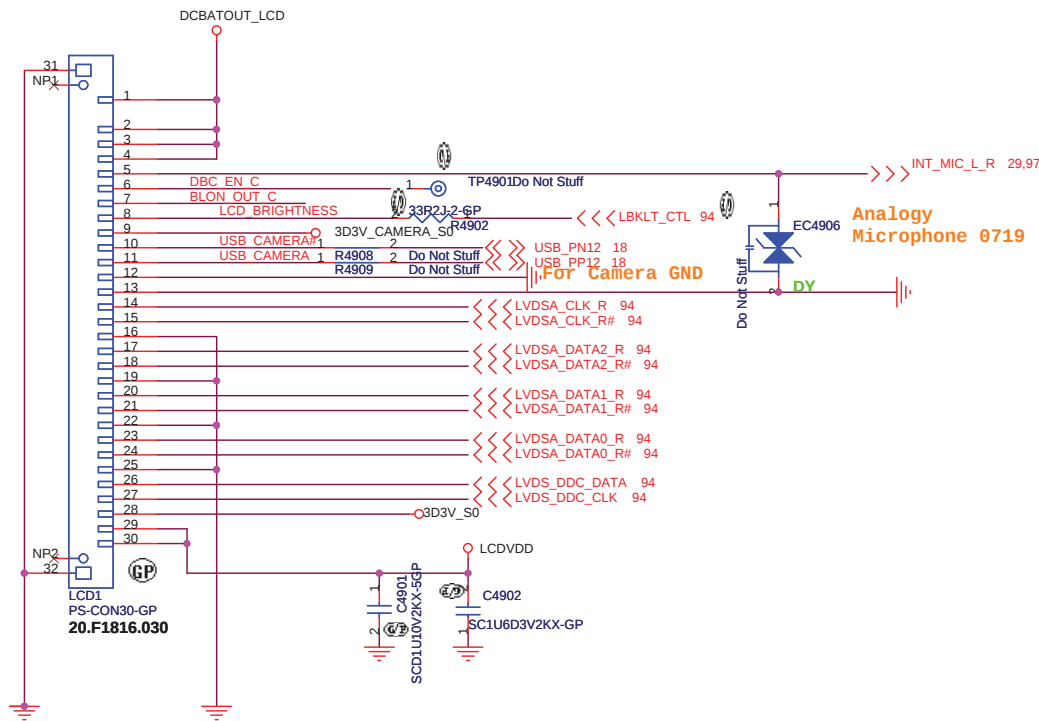
APL5916 for VCCSA

SB modify 2K2 for no run code

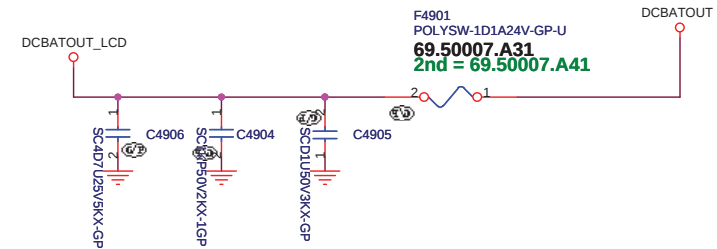


SSID = VIDEO

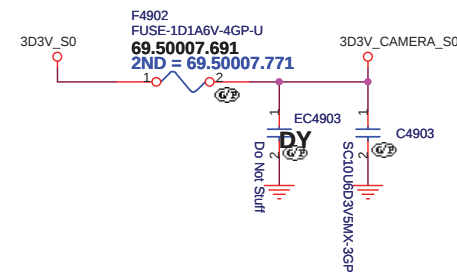
LVDS CONNECTOR



INVERTER POWER

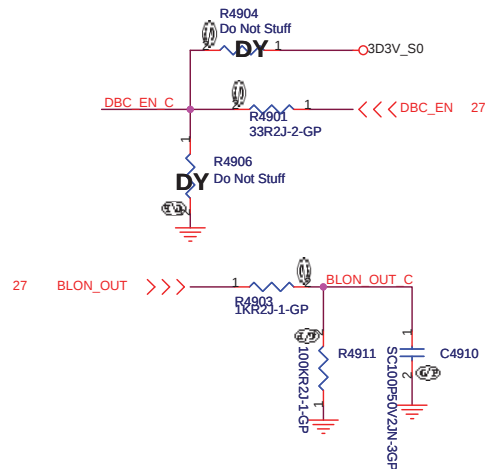
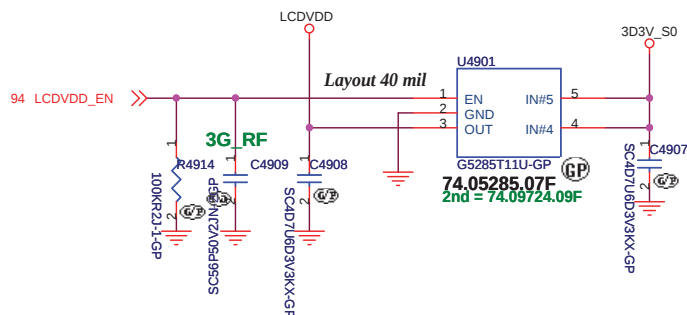


Camera Power

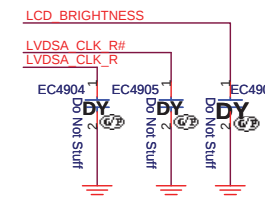


SSID = VIDEO

LCD POWER for ANNIE



For EMI request
Close to LVDS connector



HR UMA

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Title

LCD Connector

Size
Custom

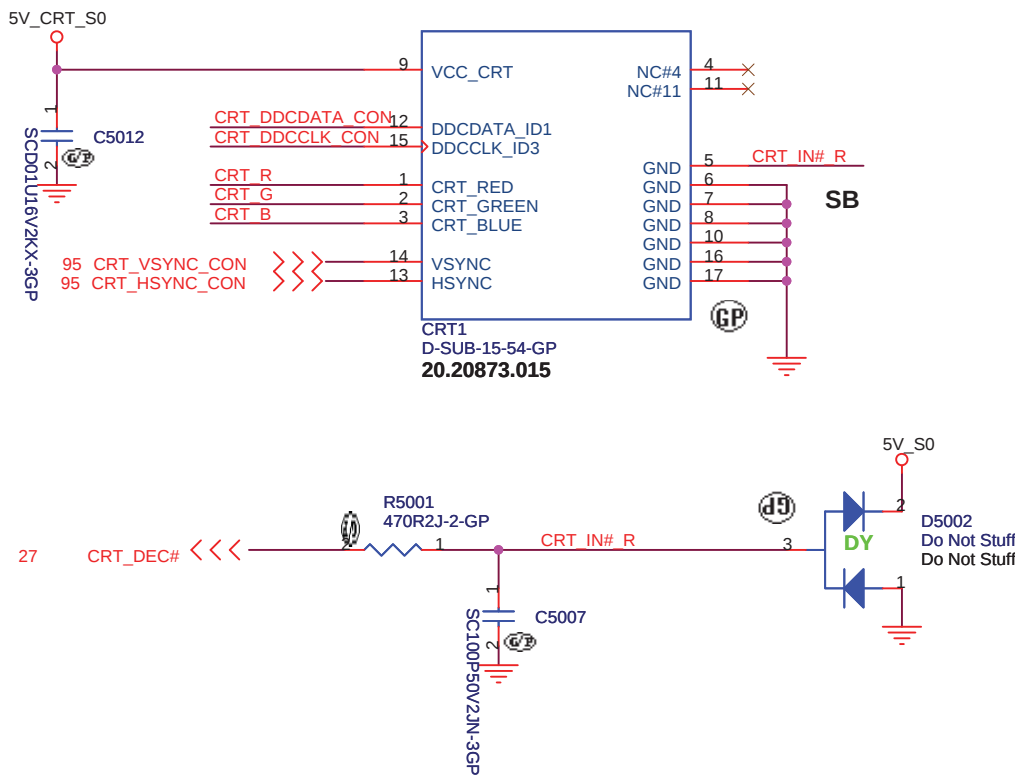
Document Number

JE40-HR

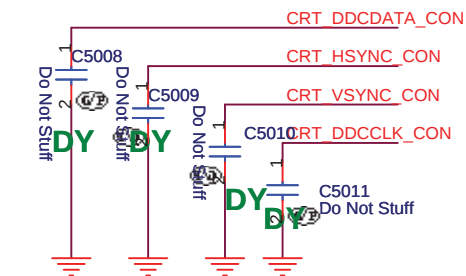
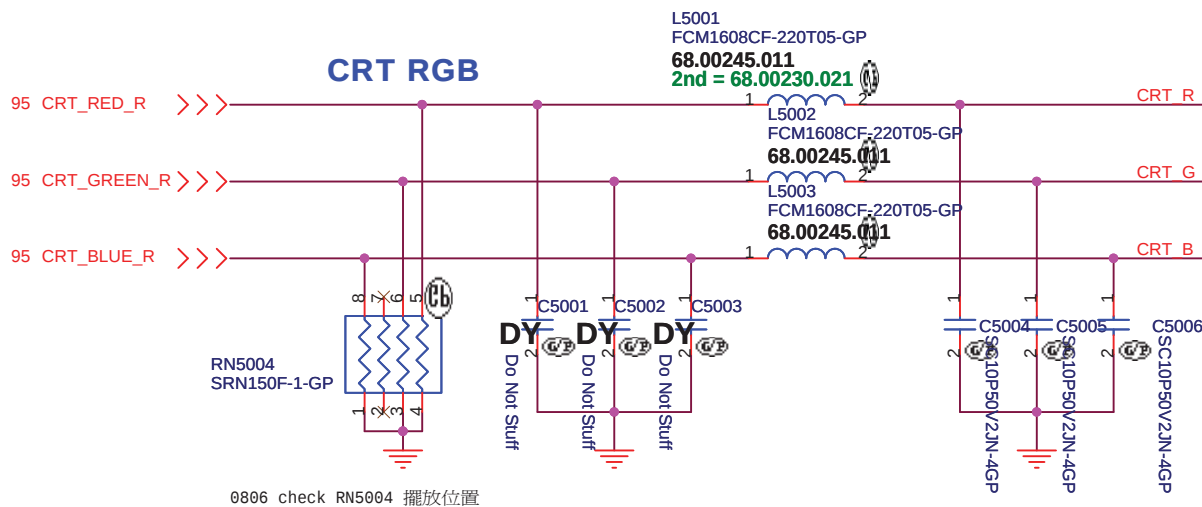
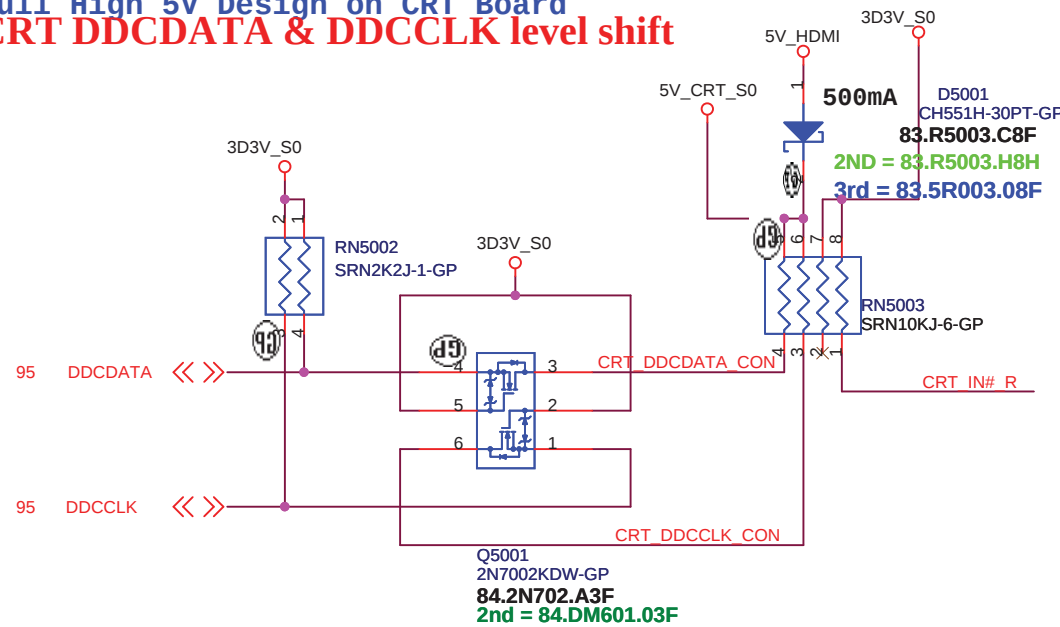
Rev
-1

Date: Thursday, December 02, 2010

Sheet 49 of 102



Pull High 5V Design on CRT Board CRT DDCDATA & DDCCLK level shift



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

CRT Connector

Size
A4

Document Number

JE40-HR

Rev

-1

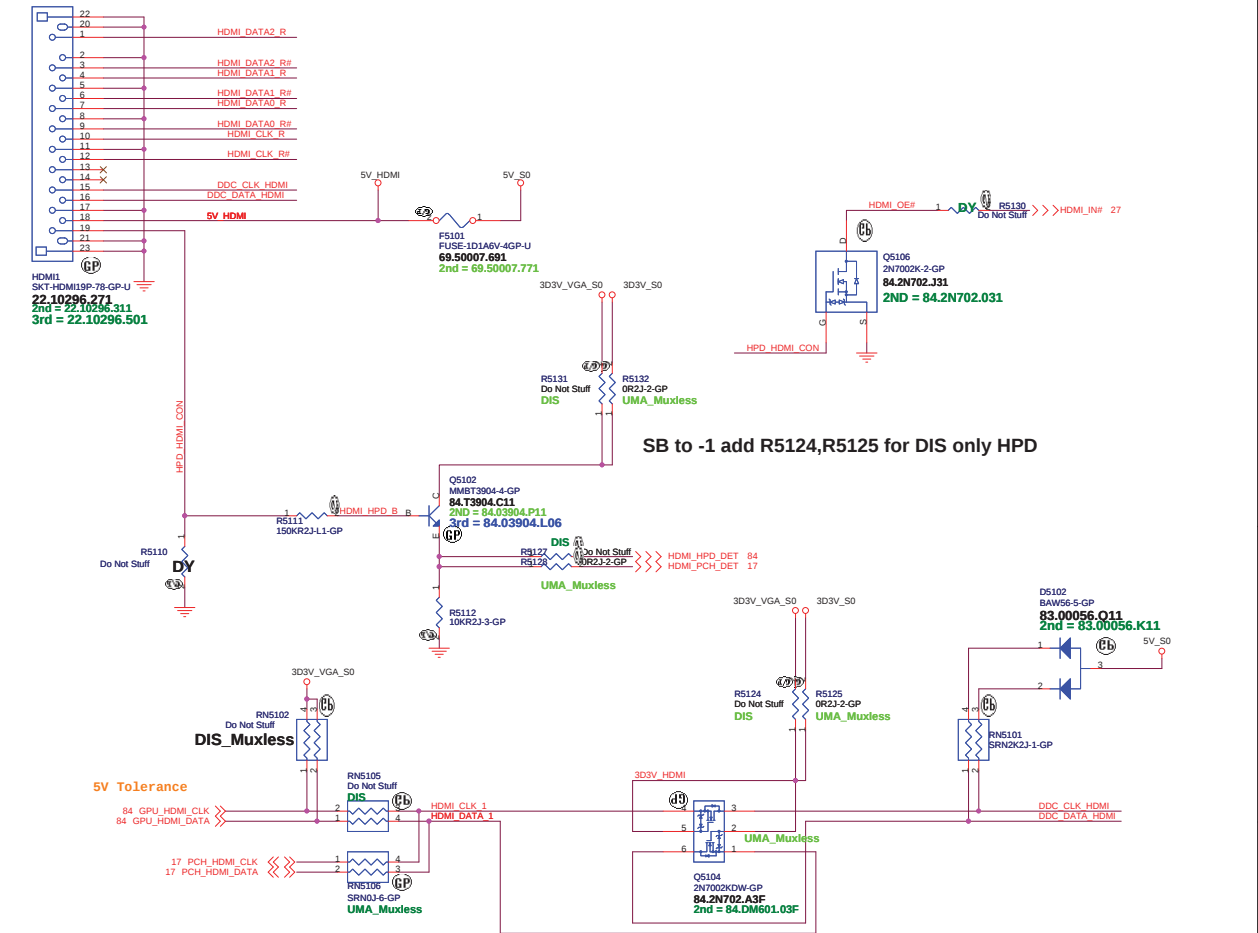
Date: Thursday, December 02, 2010

Sheet 50 of 102

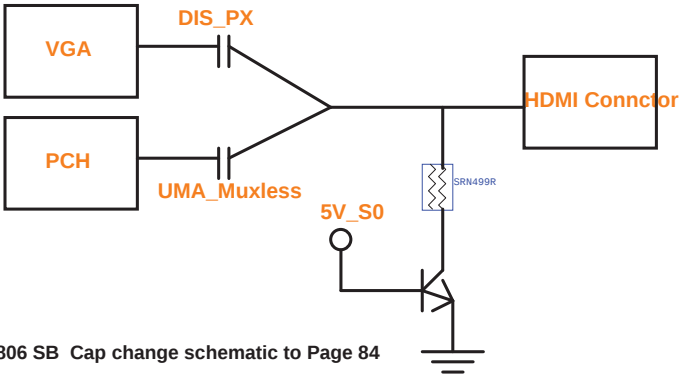
SSID = VIDEO HDMI Level Shifter & CONNECTOR

UMA_Muxless : default setting used PS8101. if don't used PS8101
please change C5103-C5110 to 0 ohm resistor

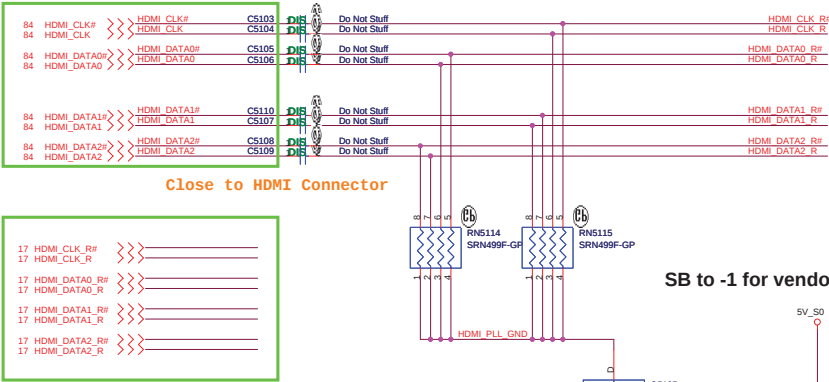
HDMI CONN



HDMI DISCRETE/ UMA Co-lay



0806 SB Cap change schematic to Page 84



LED BACKLIGHT CONVERTER POWER

HR UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
eDP			
Size	Document Number		Rev
A3	JE40-HR		-1
Date:	Thursday, December 02, 2010		Sheet 52 of 102

(Blanking)

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
S-VIDEO		
Size	Document Number	Rev
A4	JE40-HR	-1
Date: Thursday, December 02, 2010		Sheet 53 of 102

(Blanking)

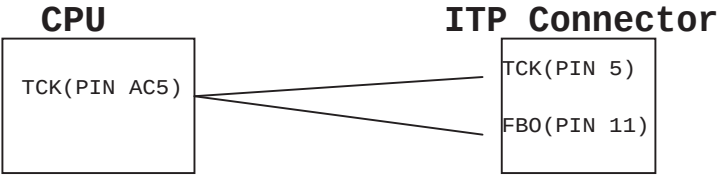
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 54 of 102

SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

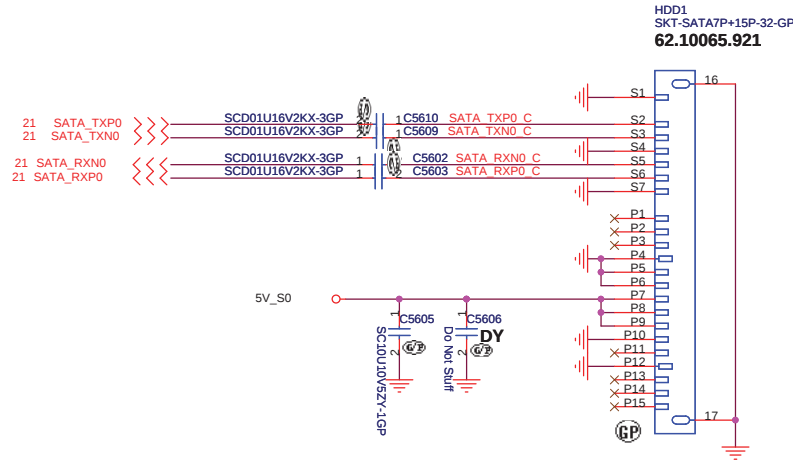


HR UMA

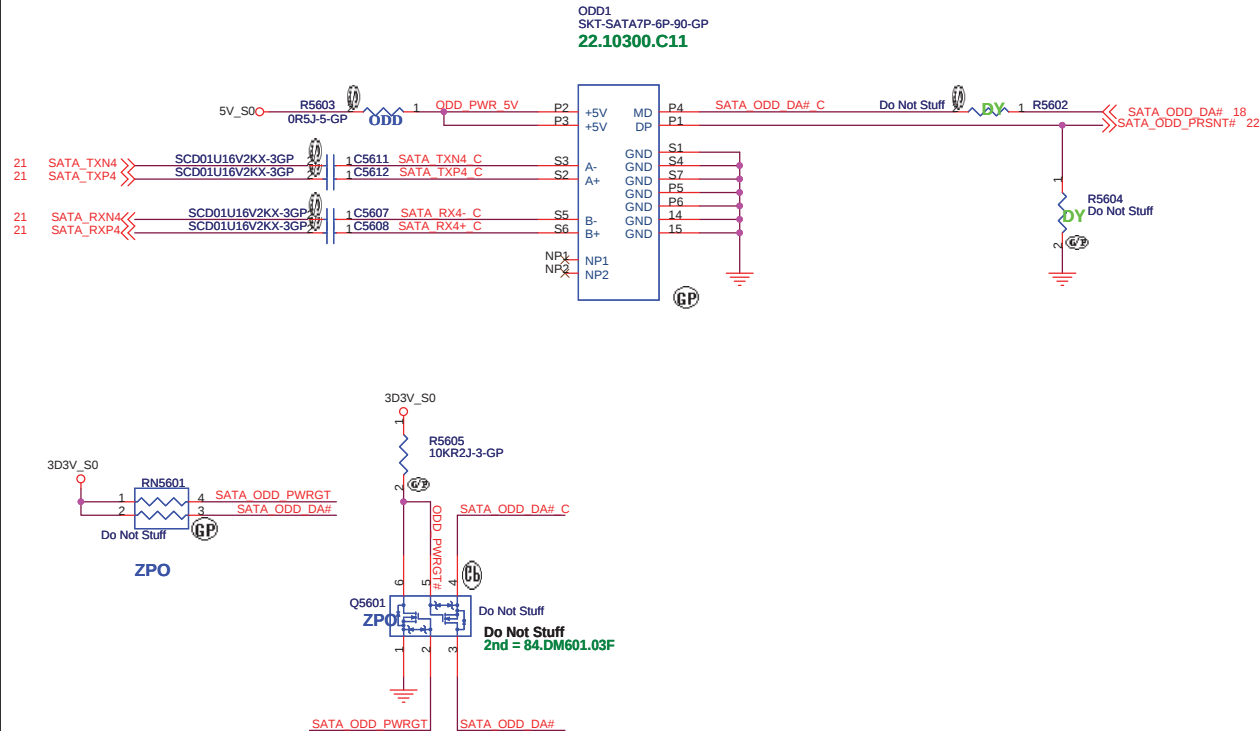
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Title ITP			
Size A4	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010		Sheet 55 of	102

SSID = SATA

SATA HDD Connector



ODD Connector

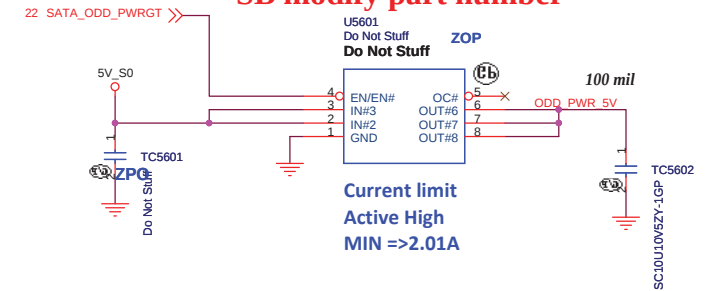


0707 Modify:
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

SB

SATA Zero Power ODD

SB modify part number



Current limit
Active High
MIN =>2.01A

HR UMA

ESATA Power

USB CHARGER

SSID = AUDIO

Speaker Connector

LINE1 OUT
SPDIF

JE40 Modify LINE OUT

Audio at small board

MIC IN

Internal
Microphone

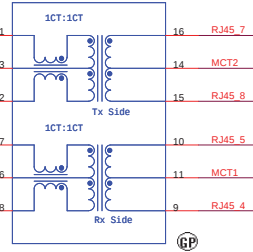
JE40 delete Line in function

SSID = LOM

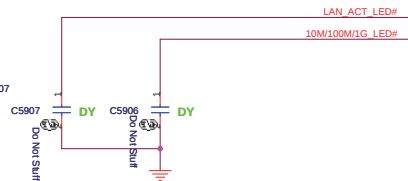
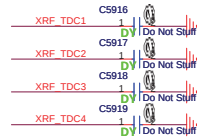
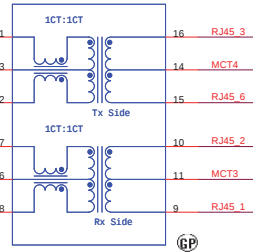
GIGA Lan Transformer

LAN MDI Off-Page

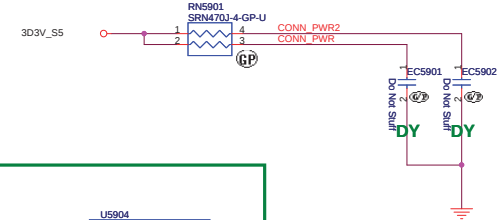
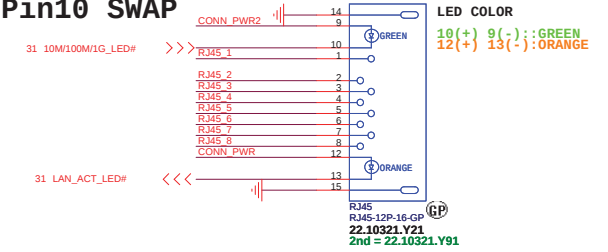
XF5901
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B



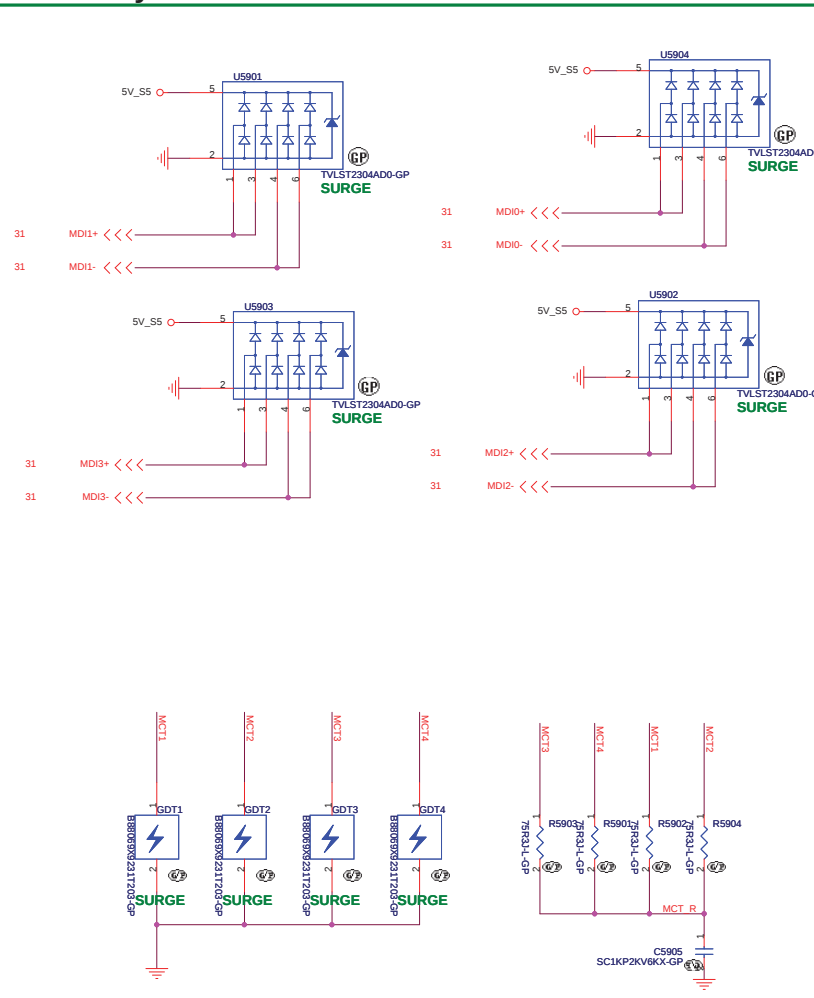
XF5902
XFORM-12P-36-GP
68.HD081.30B
Change:68.68160.30B
2nd = 68.HD081.30B



SB modify Pin9 Pin10 SWAP



SB modify For EMI



HR UMA

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LAN CONNECTOR		
Title	JE40-HR	Rev -1
Size	Document Number	
Custom		
Date:	Thursday, December 02, 2010	Sheet 59 of 102

SSID = Flash.ROM



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Taipei Hsien 221, Taiwan, R.O.C.

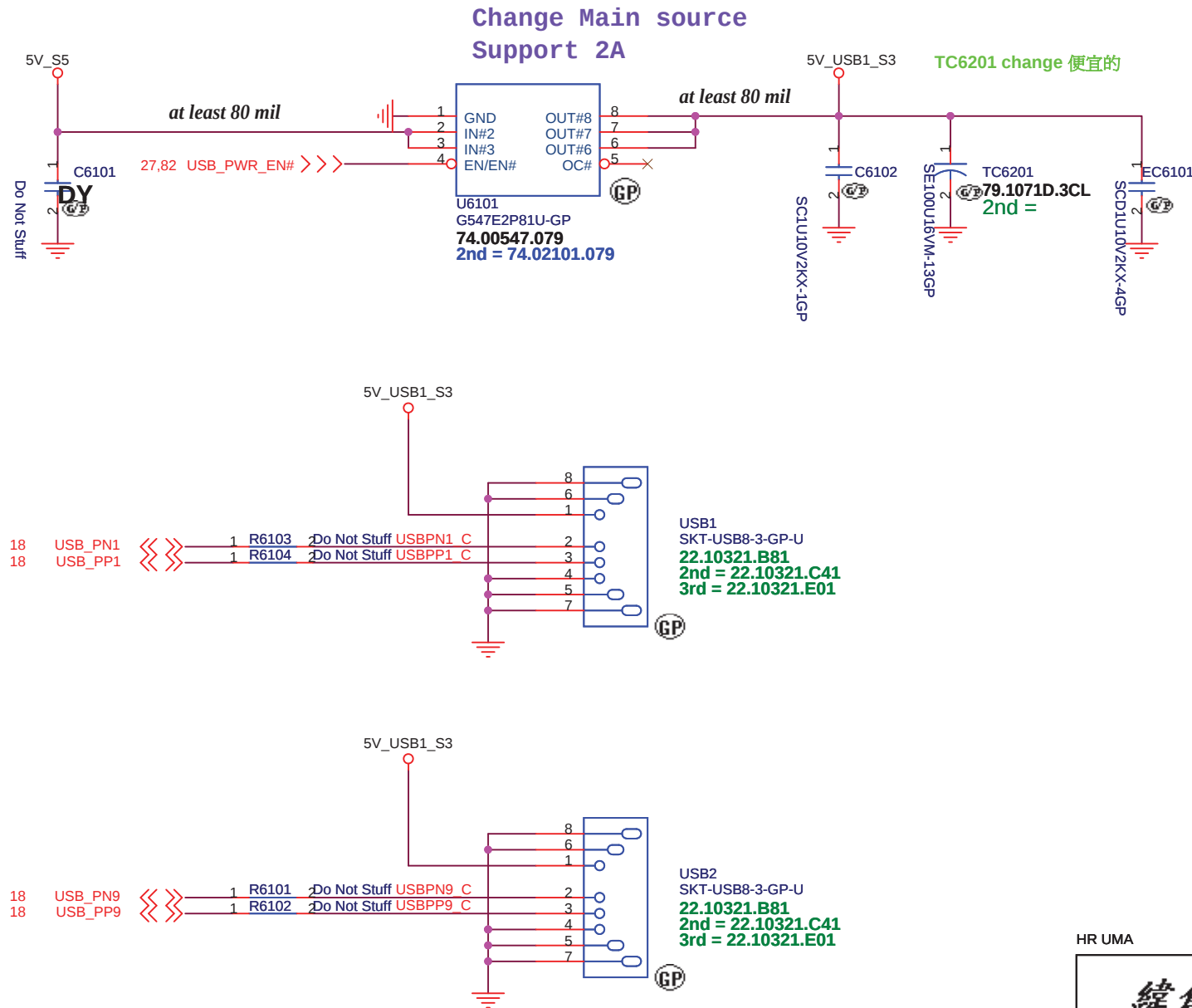
Title

Flash/RTC

Size	Document Number	Rev
Custom	JE40-HR	-1
Date:	Thursday, December 02, 2010	Sheet 60 of 102

SSID = USB

IO Board USB Power



HR UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Power SW

Size
A4

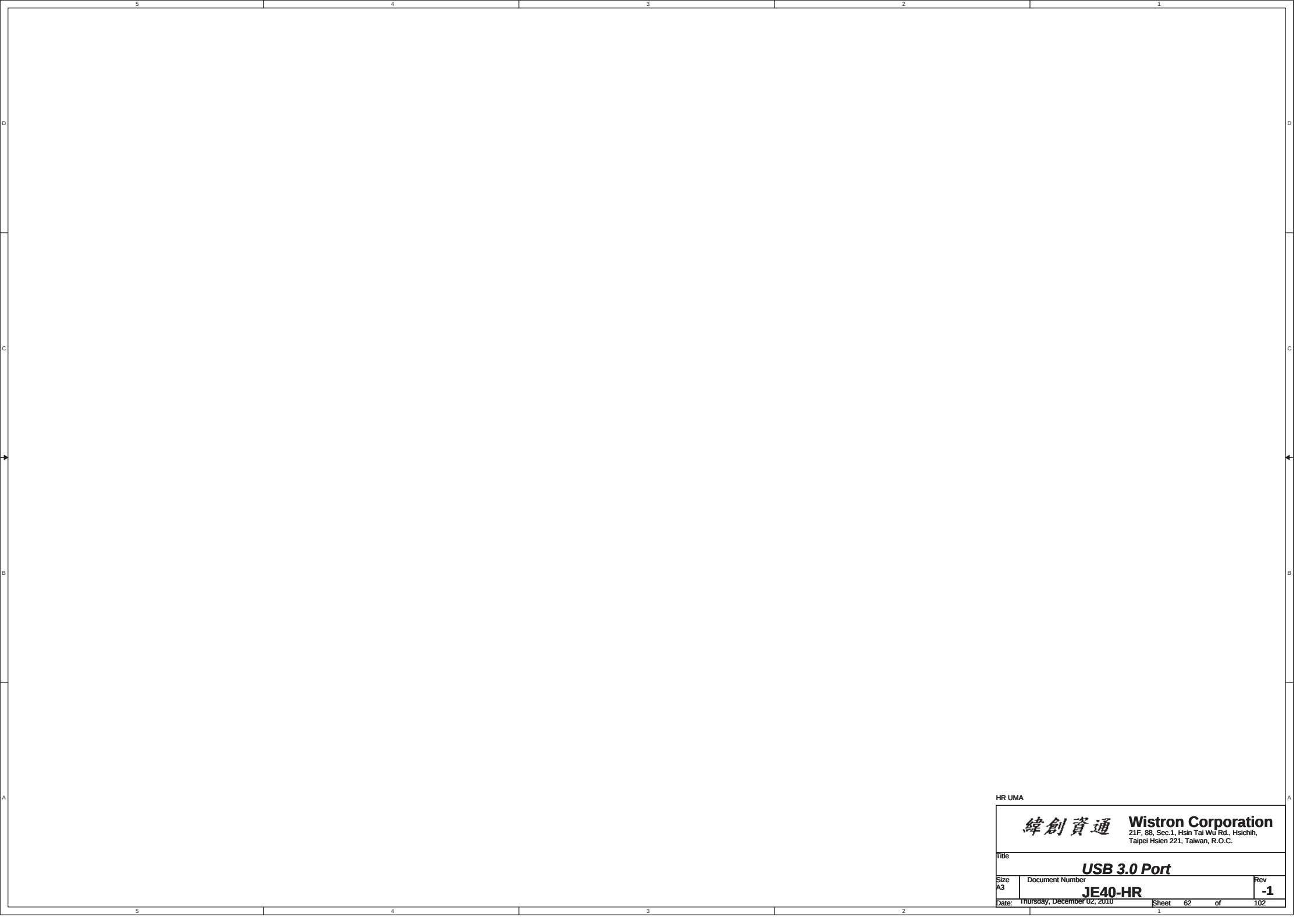
Document Number

JE40-HR

Rev
-1

Date: Thursday, December 02, 2010

Sheet 61 of 102



D

D

C

C

B

B

A

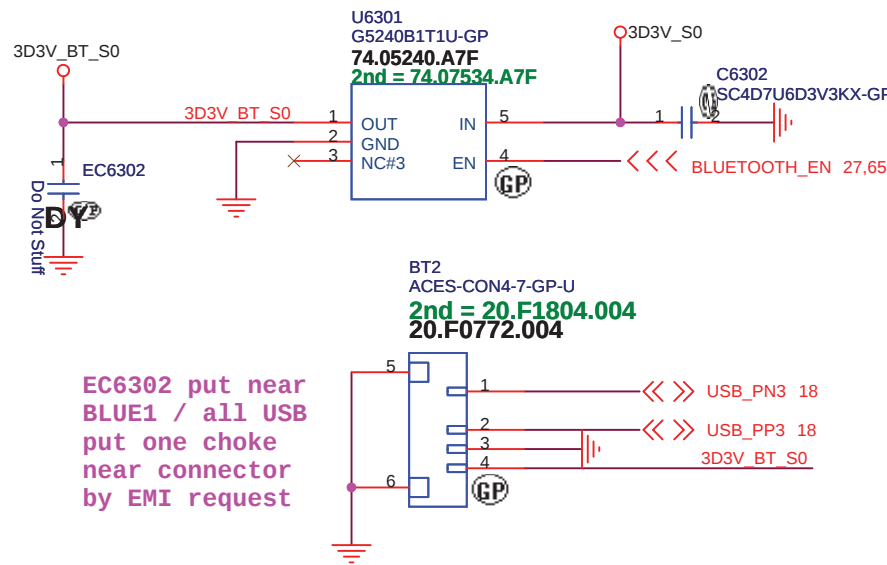
A

HR UMA

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB 3.0 Port			
Size A3	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010	Sheet 62	of 102	

SSID = User.Interface
Bluetooth Module conn.

ANNIE Bluetooth Module



HR UMA

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Bluetooth			
Size	Document Number	Rev	
A4	JE40-HR	-1	
Date:	Thursday, December 02, 2010	Sheet	63 of 102

Finger printer

JE40 delete FP function

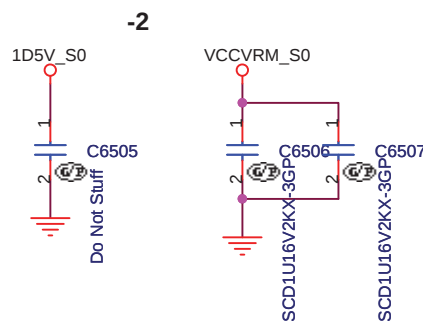
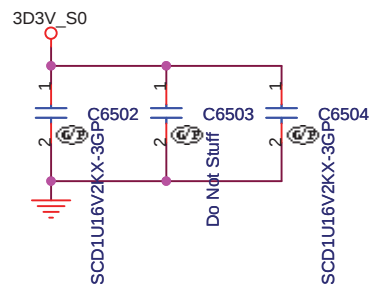
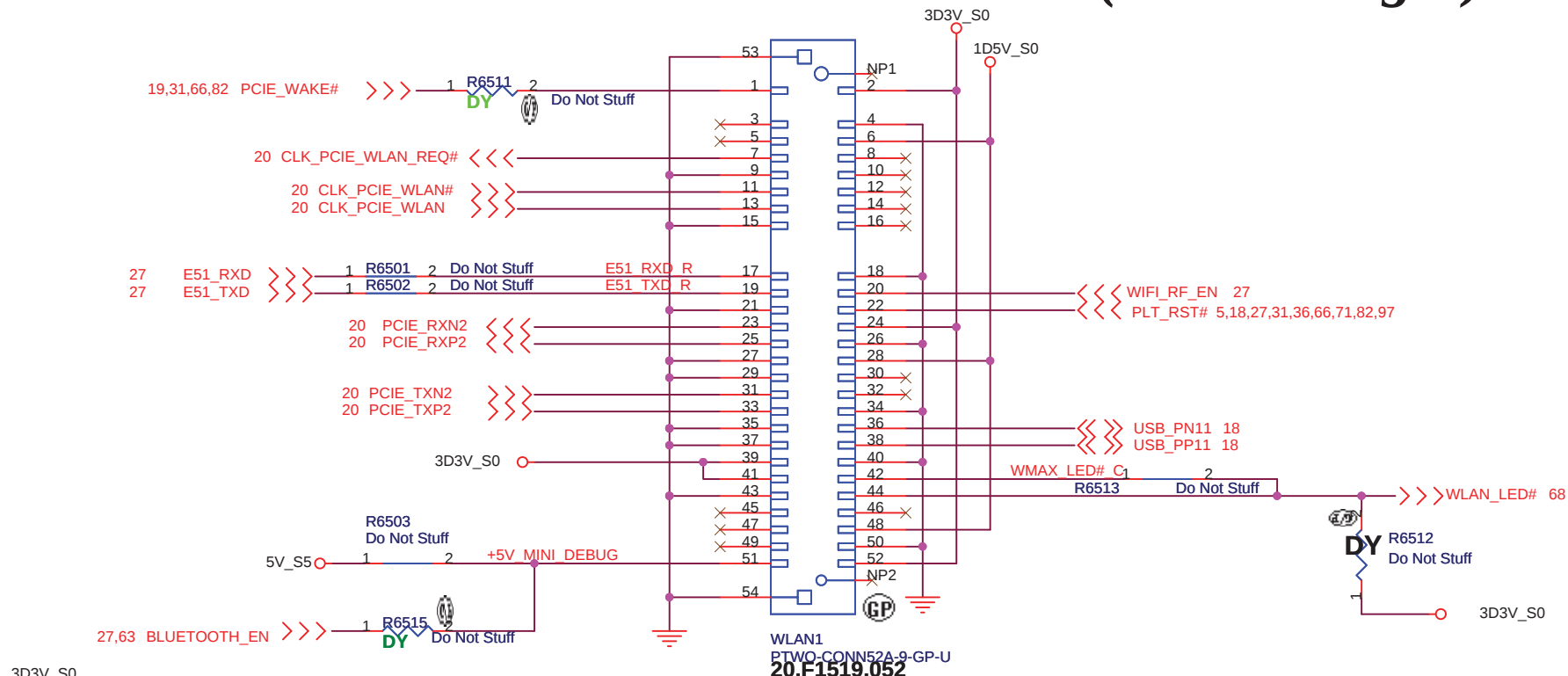


HR UMA

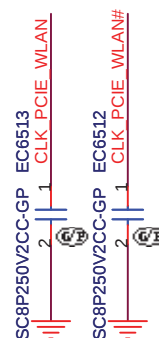
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
RESERVED		
Size	Document Number	Rev
A4	JE40-HR	-1
Date: Thursday, December 02, 2010		Sheet 64 of 102

SSID = Wireless

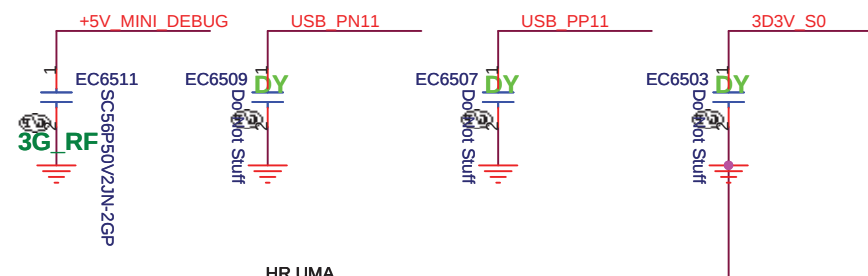
Mini Card Connector(802.11a/b/g/n)



SB modify for SIV



RF suggestion



HR UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
MINICARD(WLAN)/ITP CONN

Size A4 Document Number JE40-HR Rev -1

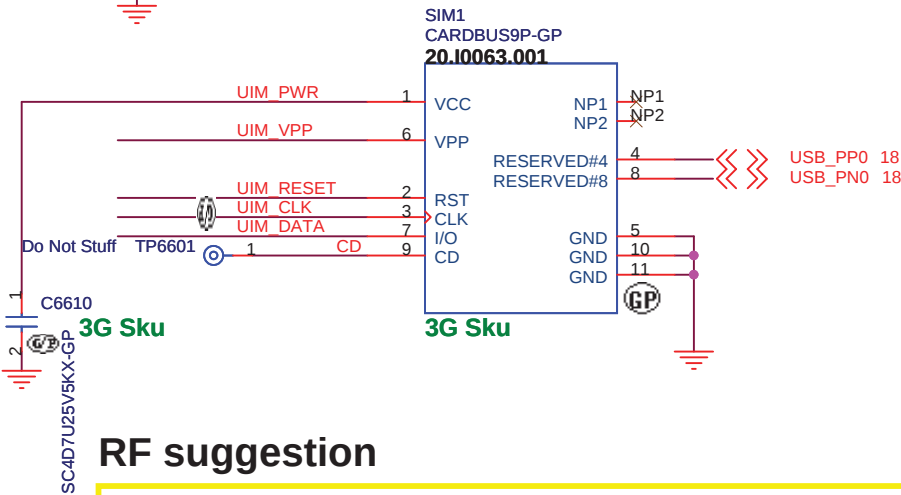
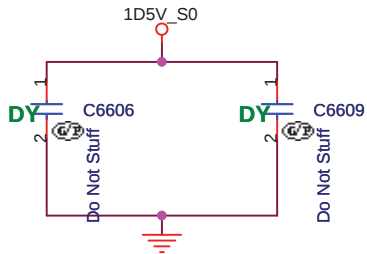
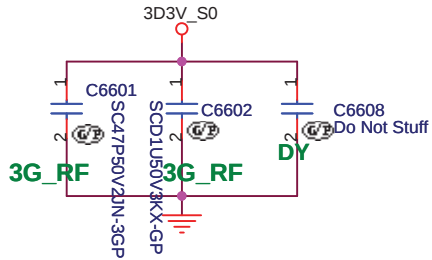
Date: Thursday, December 02, 2010 Sheet 65 of 102

SSID = Wireless

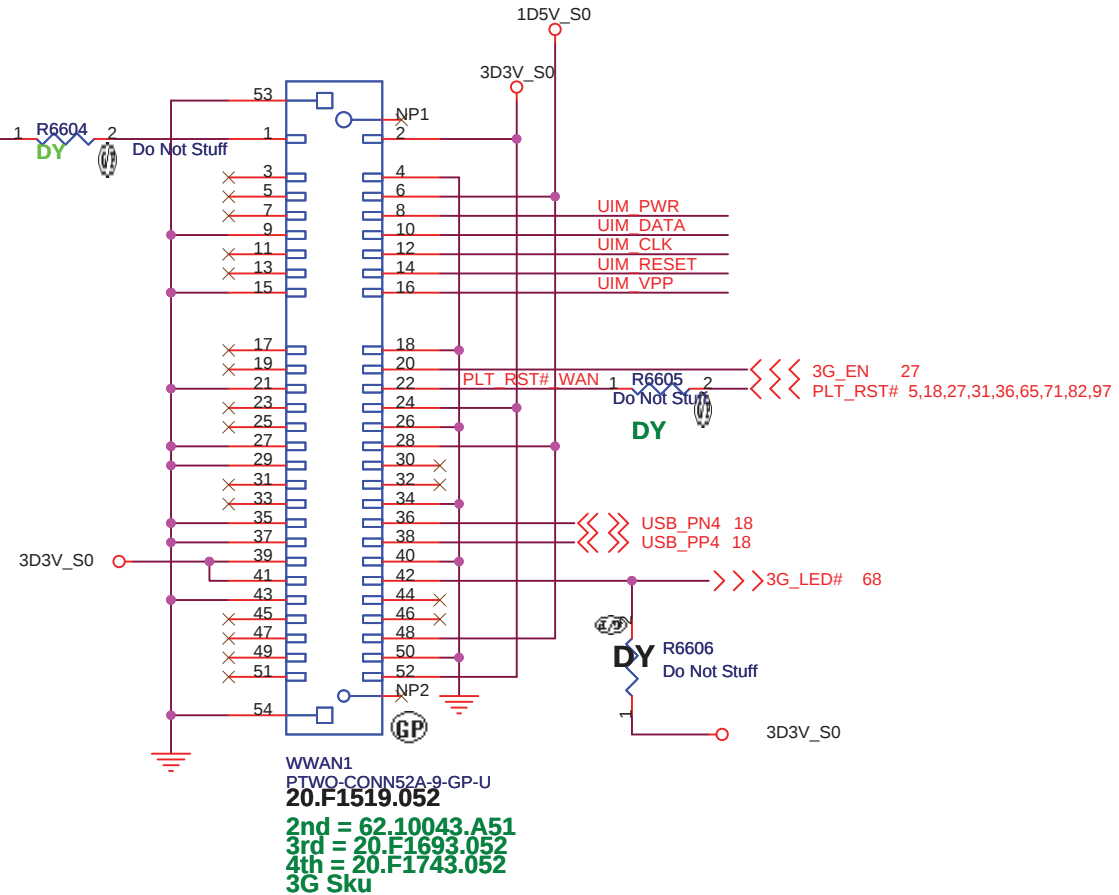
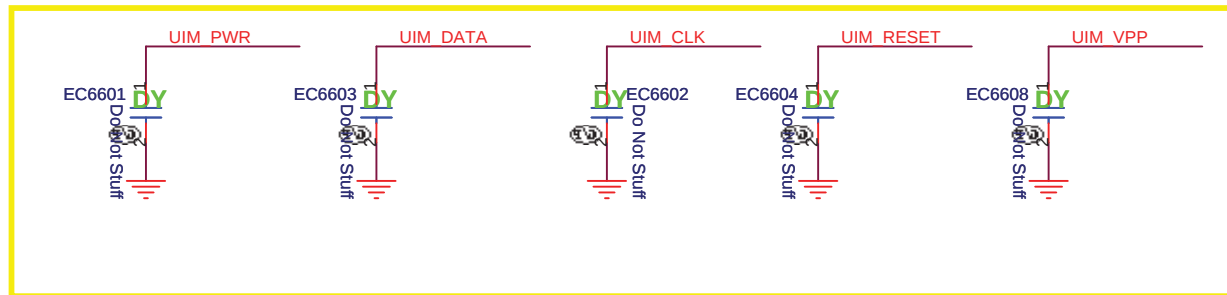
Mini Card Connector(WWAN)

20100712 V1.5

Place near MINI Card CONN



RF suggestion



HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size

Document Number

JE40-HR

Rev

-1

Date: Thursday, December 02, 2010

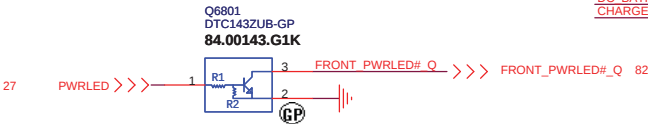
Sheet 66 of 102

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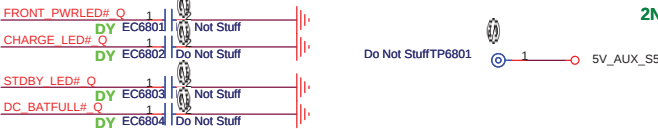
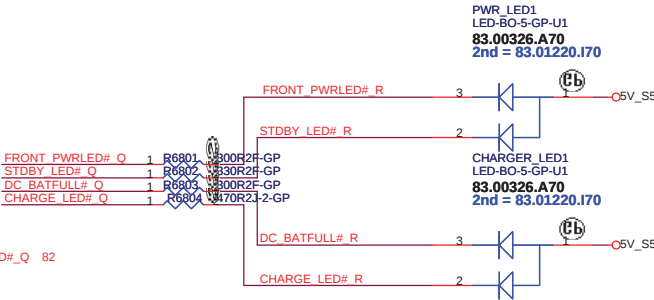
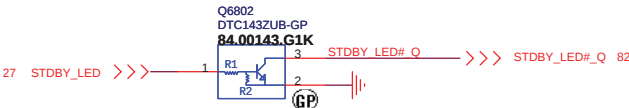
HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 67 of 102

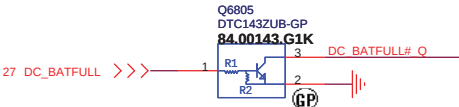
Power button LED



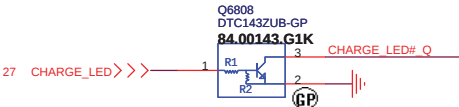
Power STDBY_LED



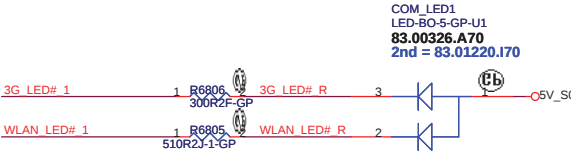
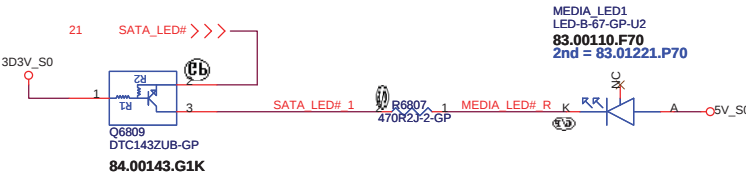
Battery LED2(DC_BATFULL)



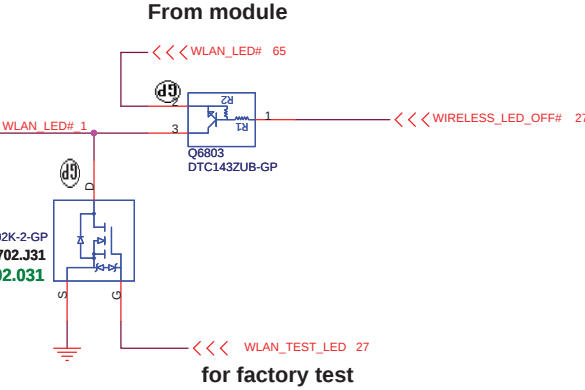
Battery LED1(CHARGE)



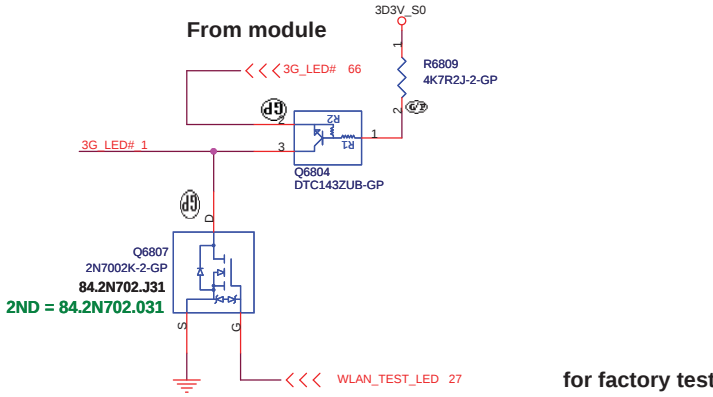
SATA HDD LED



WLAN_LED

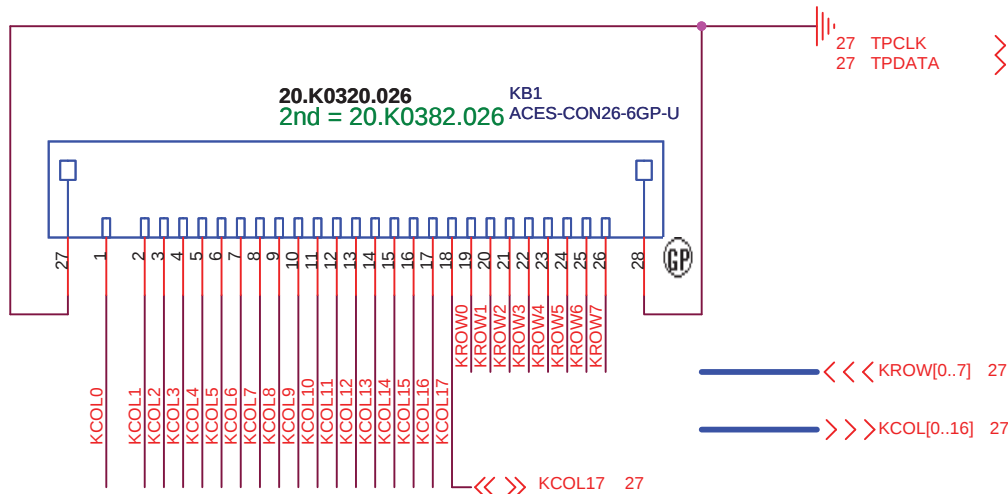


3G LED



SSID = KBC

Internal KeyBoard Connector



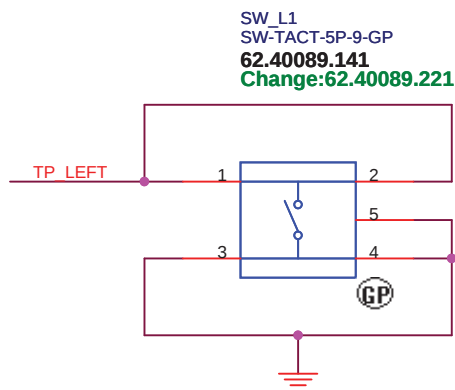
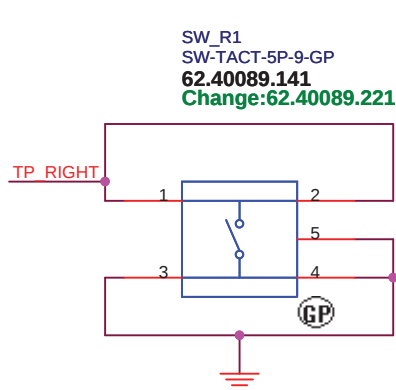
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26

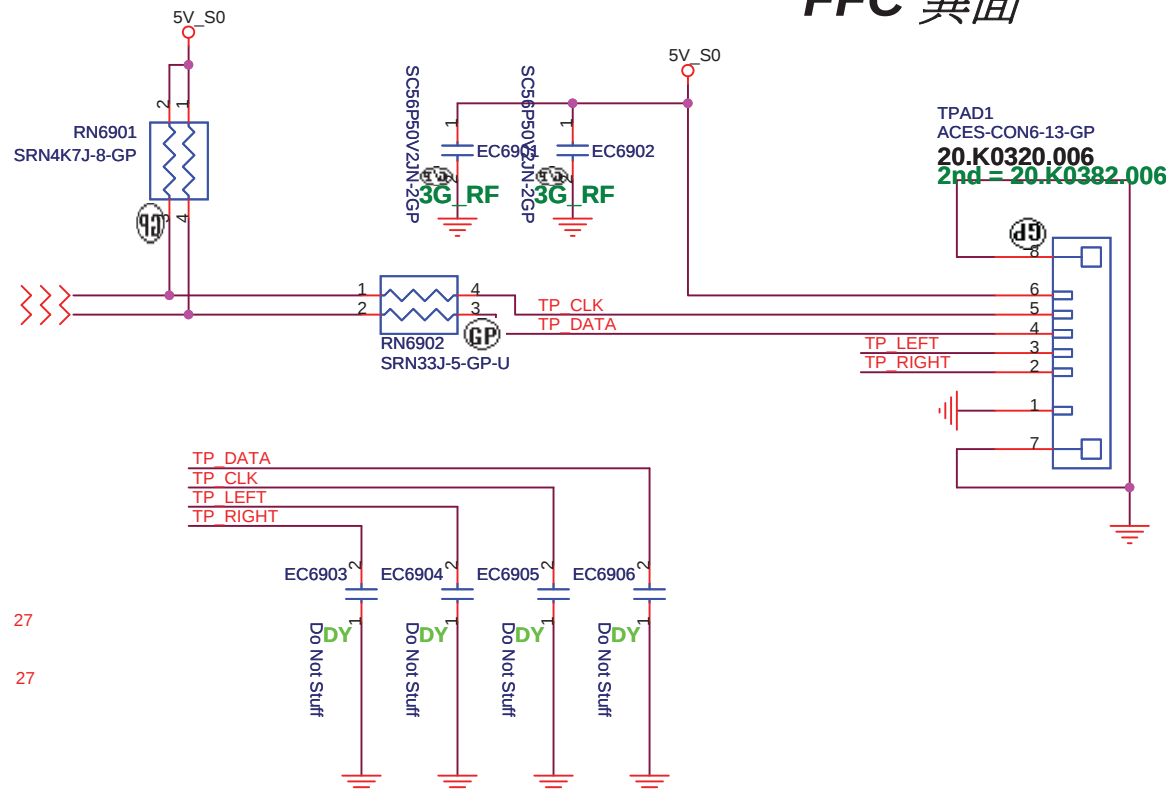
K/B

1

SB to -1 modify Part number



TOUCH PAD



FFC 異面

HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

Key Board/Touch Pad

Size

Document Number

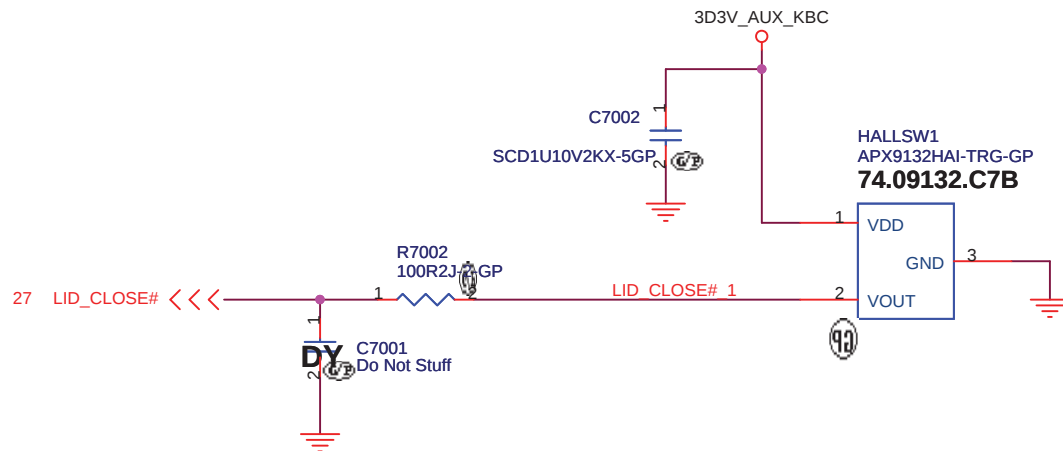
JE40-HR

Rev

-1

Date: Thursday, December 02, 2010

Sheet 69 of 102



HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size
A4

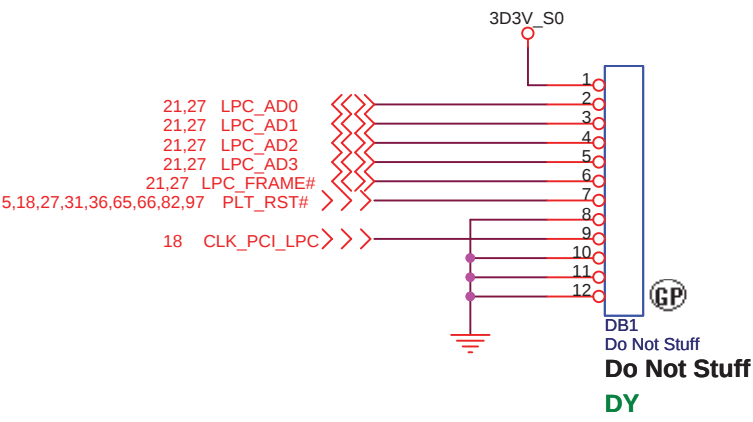
Document Number

JE40-HR

Rev
-1

Date: Thursday, December 02, 2010

Sheet 70 of 102



HR UMA

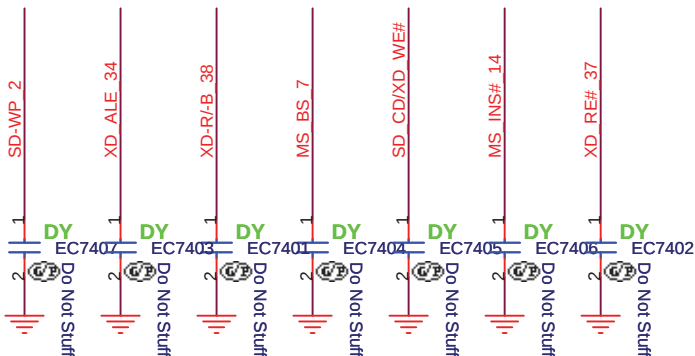
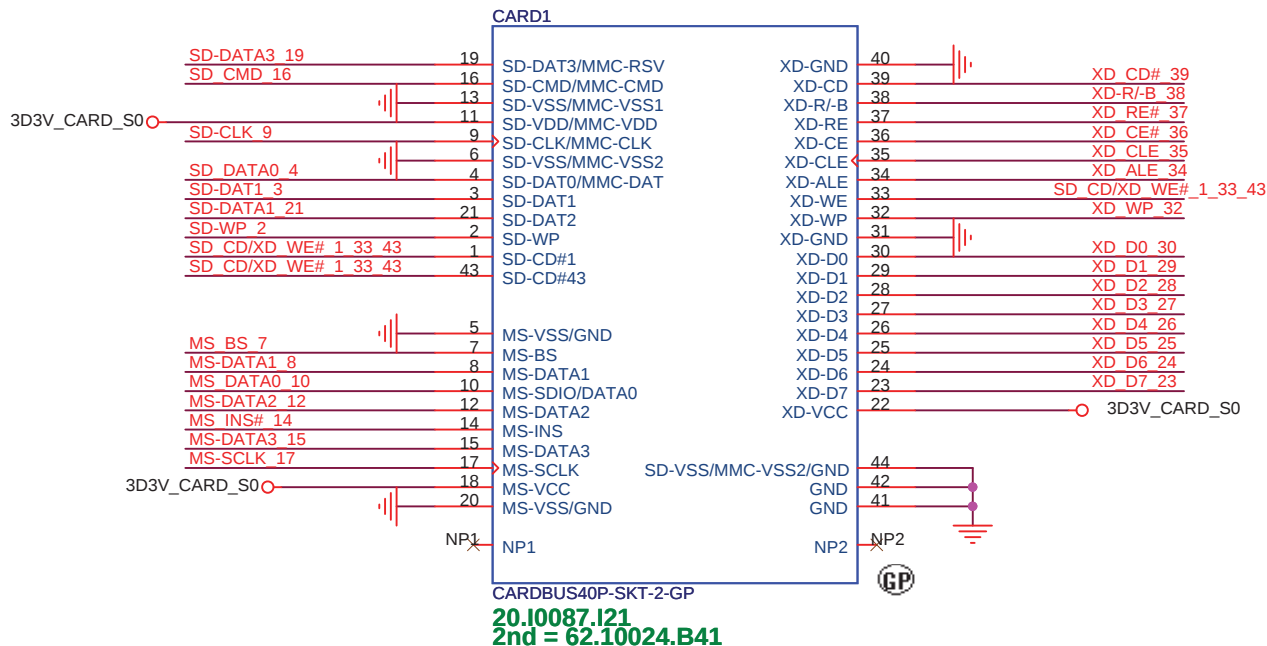
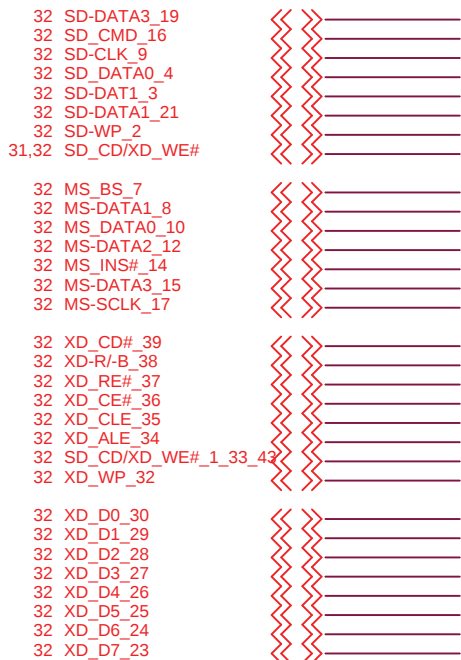
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Dubug connector		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010	Sheet 71 of 102	

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SSID = SDIO

SD/XD/MS Card Reader



HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CARD Reader CONN

Size

Document Number

Rev

JE40-HR

-1

Date: Thursday, December 02, 2010

Sheet 74 of 102

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
+3.3V_CARD Max. 1300mA, Average 1000mA
+3.3V_CARDAUX Max. 275mA

HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
New Card		
Size	Document Number	Rev
A3	JE40-HR	-1
Date:	Thursday, December 02, 2010	Sheet 75 of 102

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Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 76 of 102

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HR UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 77 of 102

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HR UMA

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Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 78 of 102

SSID = User.Interface

Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can

JE40 delete G Sensor Function

Note

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Free Fall Sensor

Size
A4

Document Number

JE40-HR

Rev

-1

Date: Thursday, December 02, 2010

Sheet 79 of 102

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HR UMA

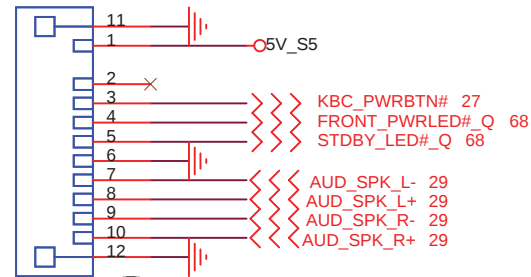
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 80 of 102

(Blanking)

HR UMA

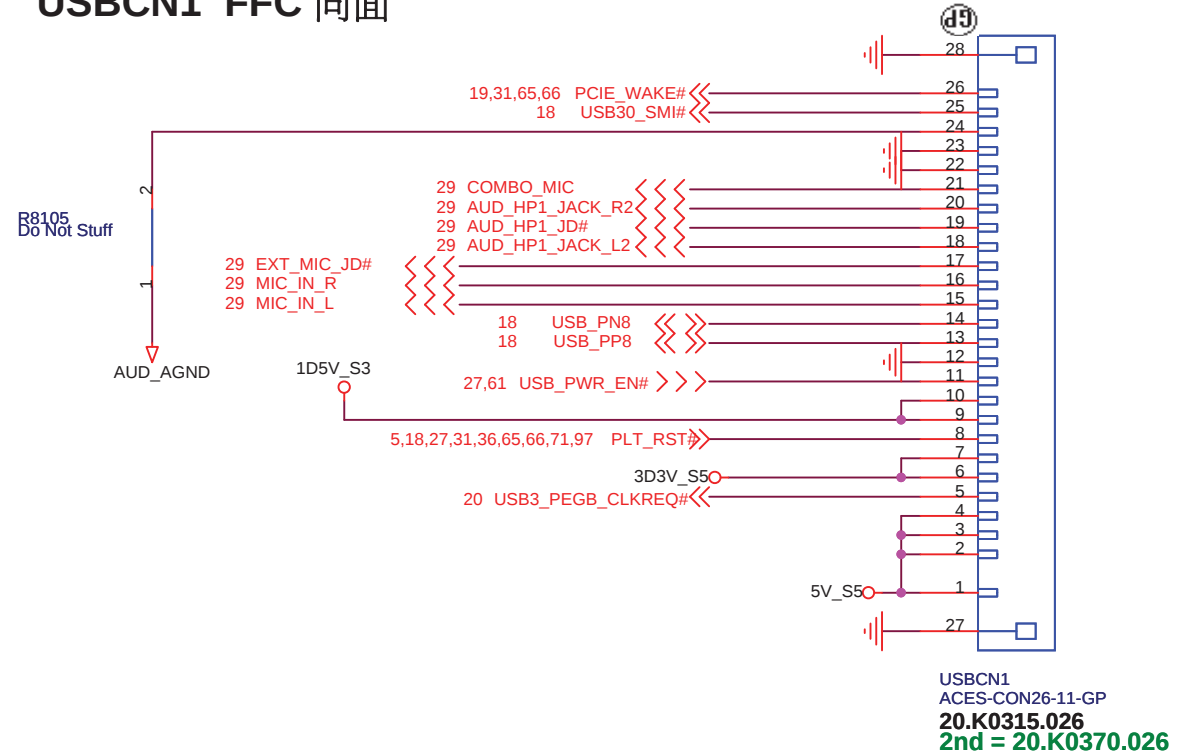
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A4	Document Number JE40-HR	Rev -1
Date: Thursday, December 02, 2010		Sheet 81 of 102

PWRCN1 FFC 異面



PWRCN1
ACES-CON10-20-GP
20.K0422.010
2nd = 20.K0382.010

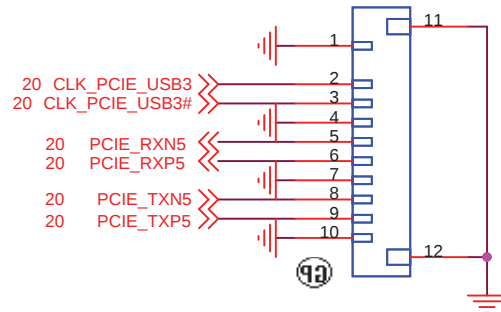
USBCN1 FFC 同面



USBCN1
ACES-CON26-11-GP
20.K0315.026
2nd = 20.K0370.026

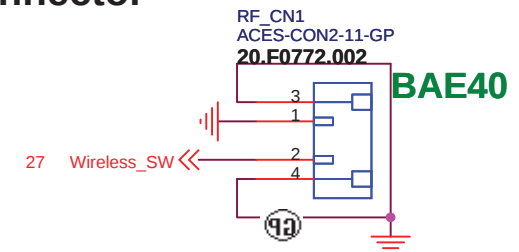
0806 change 10Pin

USBCN2
ACES-CON10-18-GP
20.K0315.010
2nd = 20.K0392.010



USBCN2 FFC 同面

-1 add RF connector
BAE40 Only

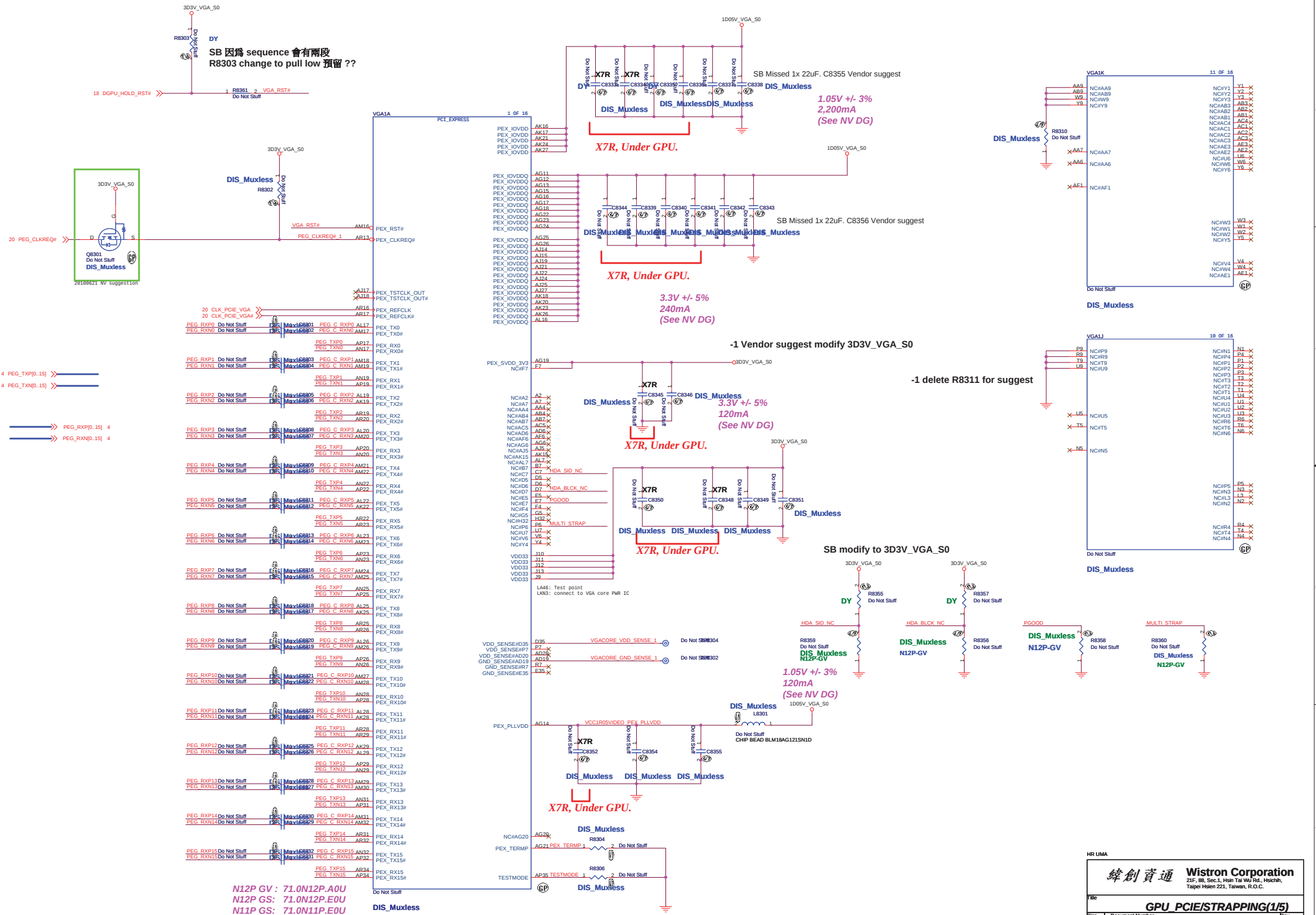


RF_CN1
ACES-CON2-11-GP
20.F0772.002
BAE40

Cabele Wire to BD

HR UMA

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Title IO Board Connector			
Size A4	Document Number JE40-HR		Rev -1
Date: Thursday, December 02, 2010		Sheet 82 of 102	



[illegible]

SB modify connector to IFPC_IOVDD_PWR

SA R8412, R8413 change DY
SB R8412, R8413 change delete



EDP 10A

DC tolerance +/- 75mV
AC tolerance +/- 50mV < 100MHz

DIS_Muxless DIS_Muxless DIS_Muxless DIS_Muxless DIS_Muxless DIS_Muxless DIS_Muxless DIS_Muxless

X7R, Under GPU.

X7R, Near GPU.

1.05V +/- 3%
200mA
(See NV DG)

Group A

CKE0 FBA_CKE0
CKE1 FBA_CKE1
Reset FBA_RST
ODT0 FBA_ODT0
ODT1 FBA_ODT1

Group B

FBB_CKE0
FBB_CKE1
FBB_RST
FBB_ODT0
FBB_ODT1

FBCLK Termination place on VRAM side

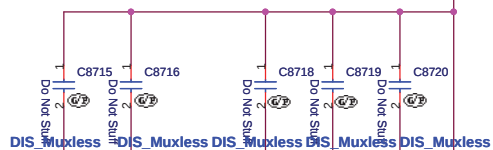
FBCLK Termination place on VRAM side

Wistron Corporation
23F, 8F, Sec.1, Hsin Tai Wu Rd, Hsueh,
Taippei Hsien 221, Taiwan, R.O.C.

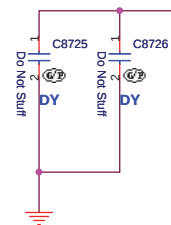
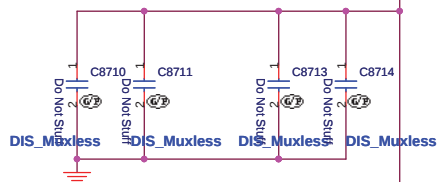
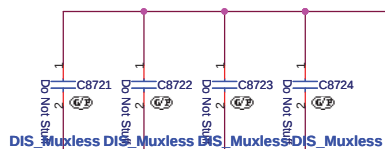
GPU DP/LVDS/CRT/GPIO(3/5)
JE40-HR

Rev -1
Date: Thursday, December 02, 2010

Under GPU



NEAR GPU



VGA1P 16 OF 16

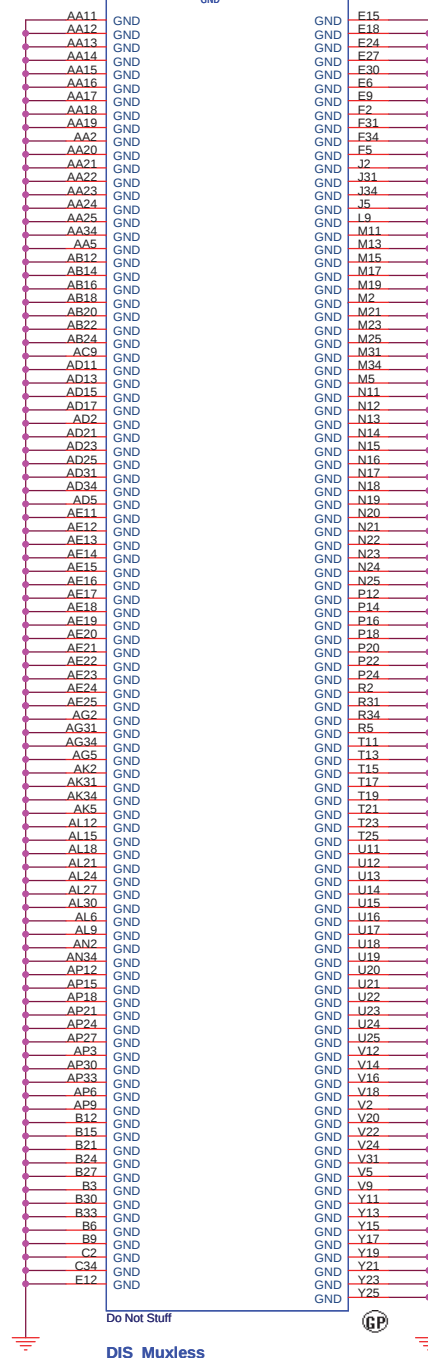
VGA CORE

DIS_Muxless

DIS_Muxless

VGA10

15 OF 16



DIS_Muxless

DIS_Muxless

HR UMA

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU_DPPWR/GND(5/5)

Size

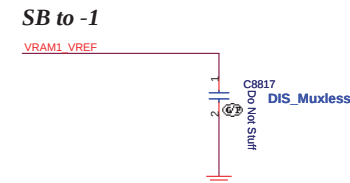
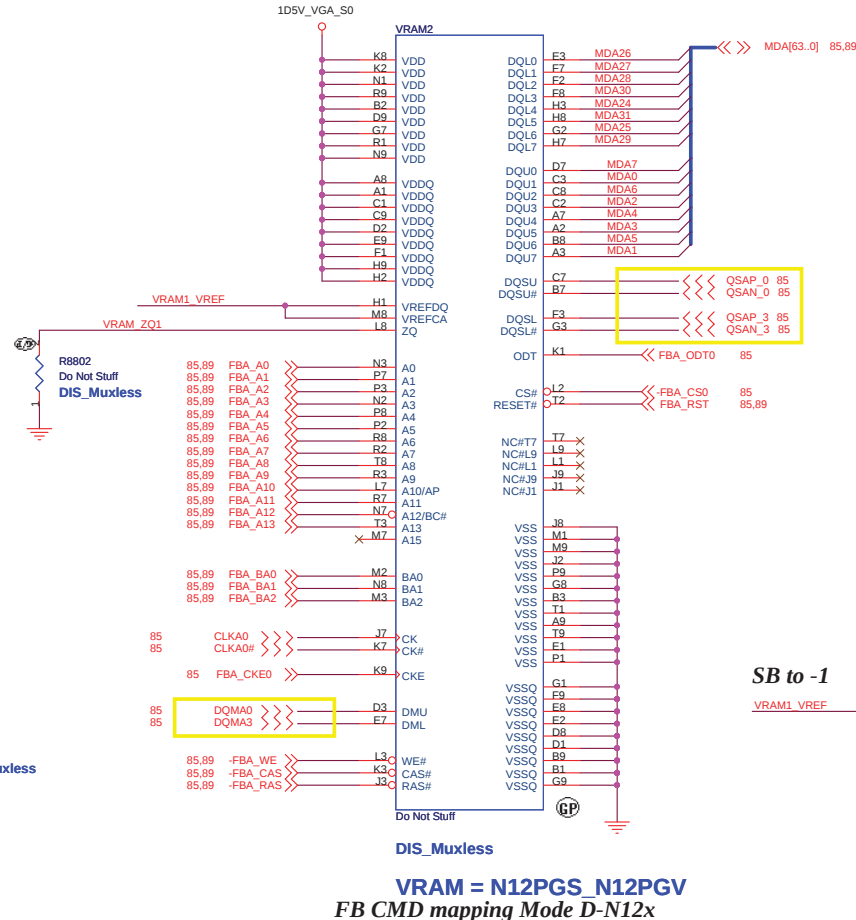
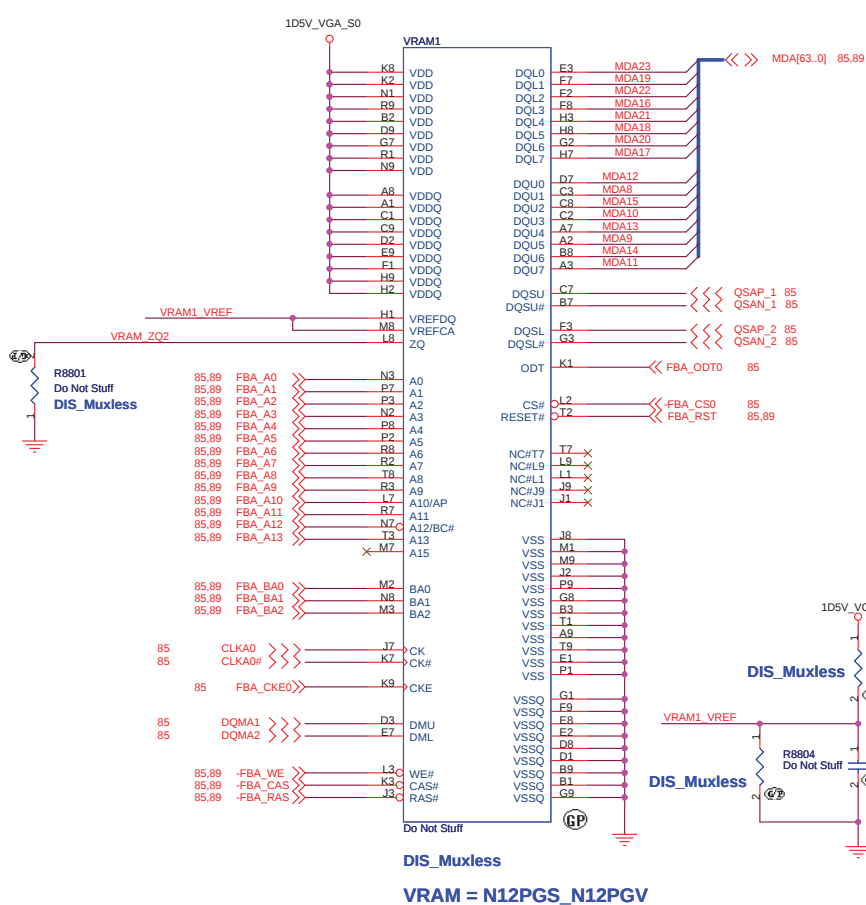
Document Number

Rev

Date: Thursday, December 02, 2010

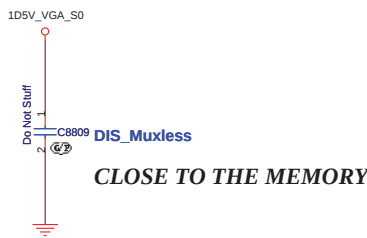
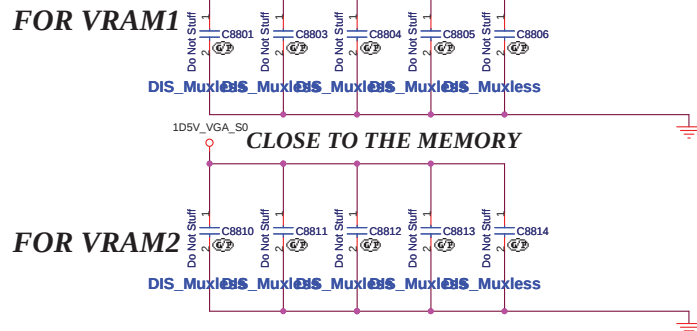
Sheet 87

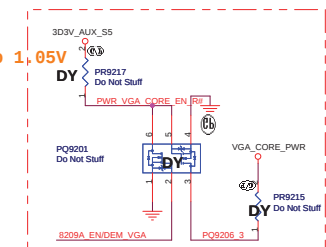
of 102



VRAM SAMSUNG 1Gb VR.1GB0B.006
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005
 VRAM HYNIX 2Gb VR.2GB0G.001

DG requires 4x0.1uF and 8x1.0uF per VRAM chip

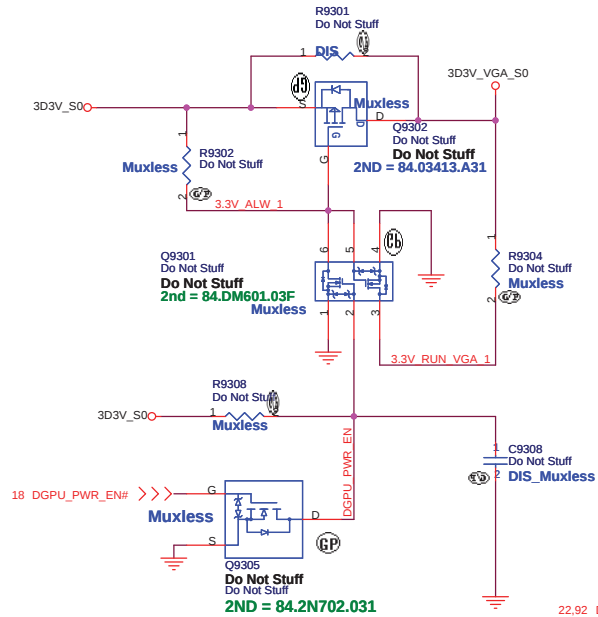




$$V_{out} = 0.75V * (R1 + R2) / R2$$

N12P GV			
P-State	PWR_VGA_CORE_D1	PWR_VGA_CORE_D0	VGA_CORE_PWR
P8 , P12	L	L	0.85V
P0 - HOT	L	H	1.00V
P0 - COLD	H	L	1.025V
	H	H	

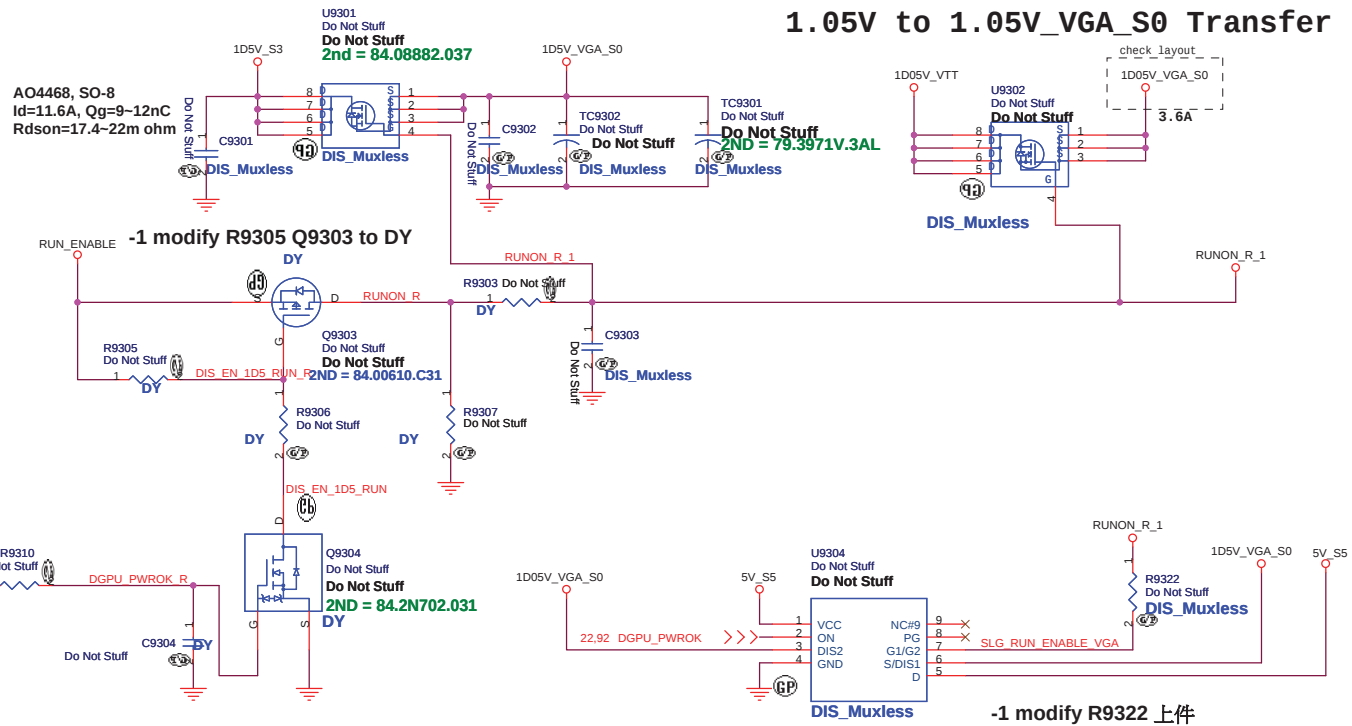
+3VS to 3.3V_DELAY Transfer



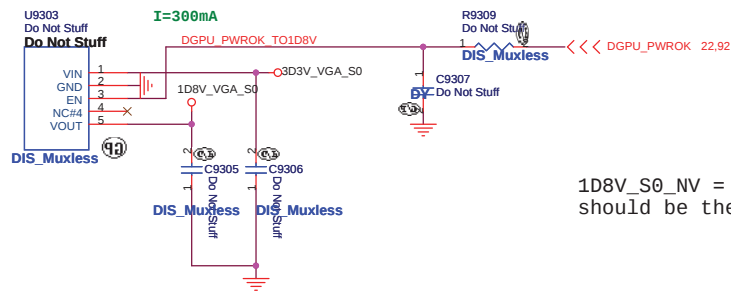
1D5V_VGA_S0

SB modify to 84.03006.A37

1.05V to 1.05V_VGA_S0 Transfer

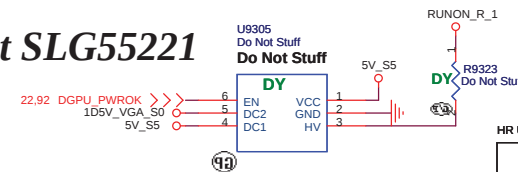


RT9025 for 1D8V_VGA +3VS to 1.8V Transfer



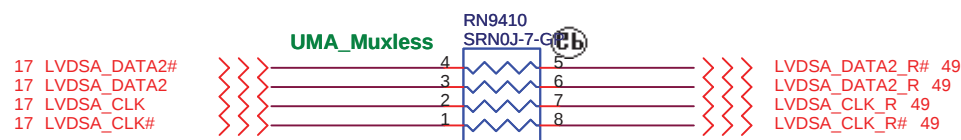
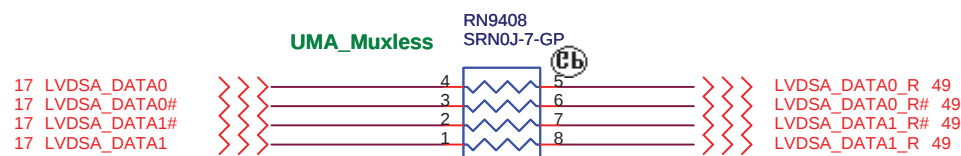
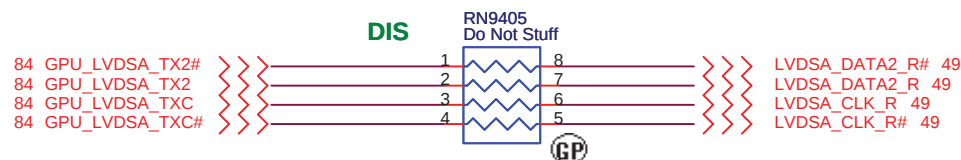
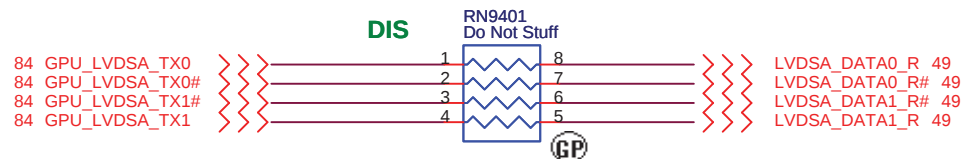
1D8V_S0_NV = IFPA_IOVDD & IFPB_IOVDD, it should be the latest ramp up rail.

-1 co-layout SLG55221

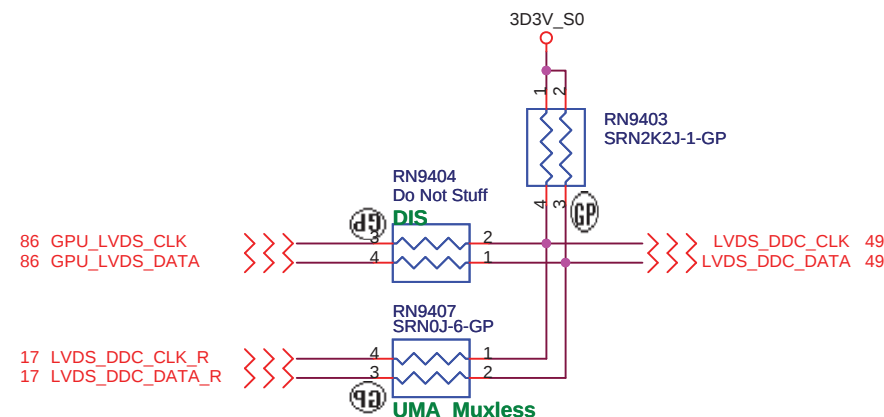
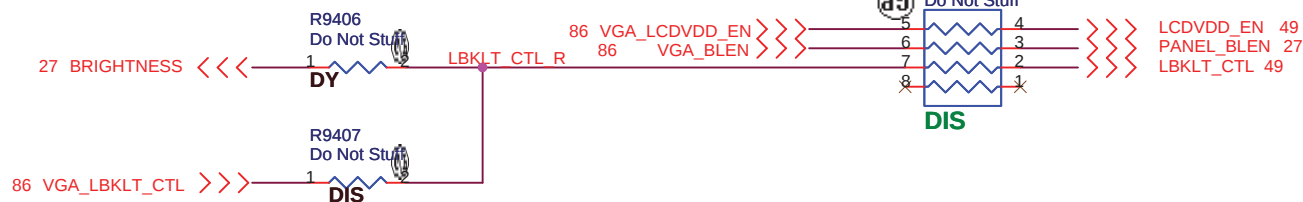
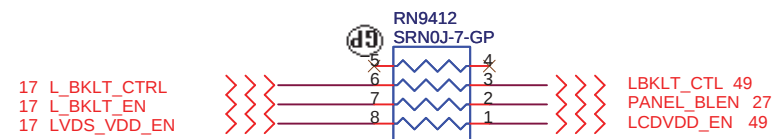


HR UMA		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		DISCRETE VGA POWER	
Size	Document Number	Rev	
Custom	JE40-HR	-1	
Date:	Thursday, December 02, 2010	Sheet	93 of 102

LVDS Channel A



Panel BL brightness/Power En/BL En



HR UMA

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

LVDS Switch

Size

Document Number

JE40-HR

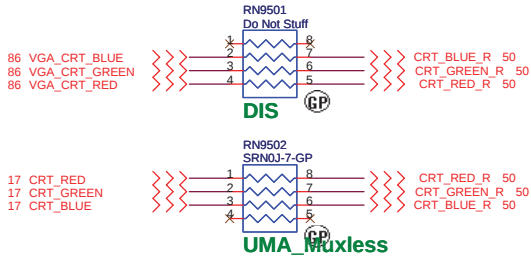
Rev

-1

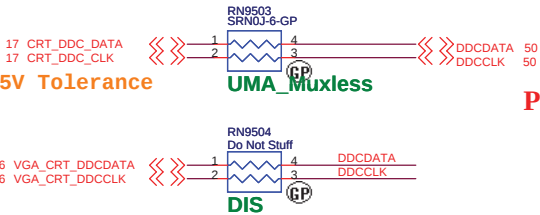
Date: Thursday, December 02, 2010

Sheet 94 of 102

Close to CRT Board CONN

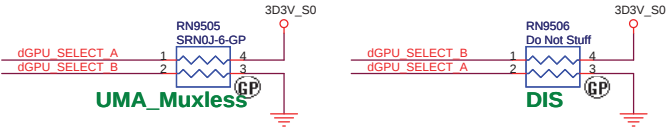


CRT DDCDATA & DDCCLK



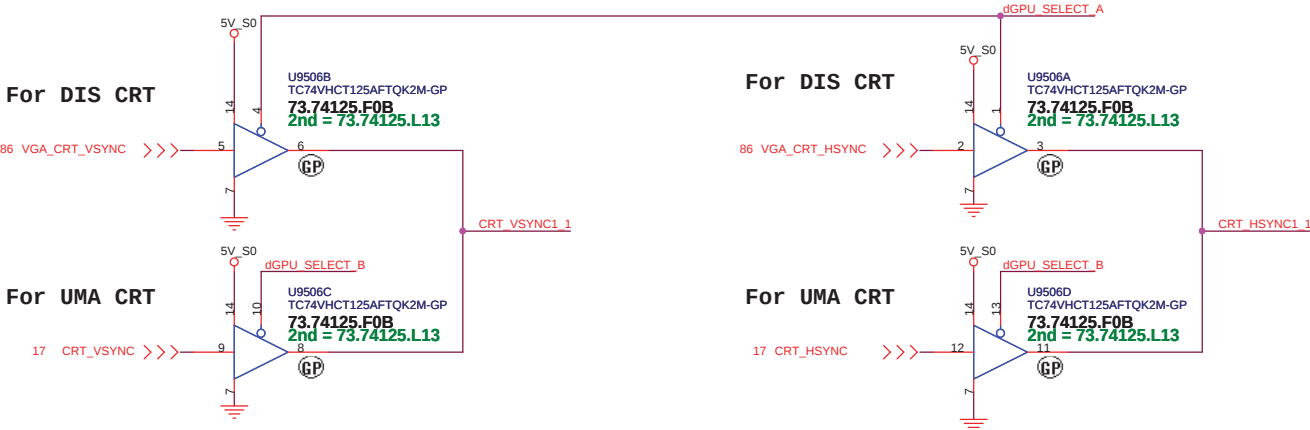
Pull high 在CRT

SB to -1 modify 4 port Logic



CRT Hsync & Vsync level shift

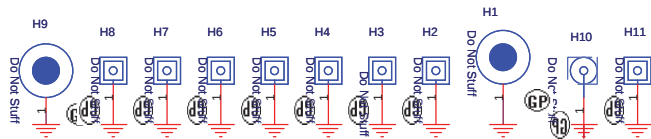
L=>B0 -DIS
H=>B1 -UMA



SB to -1 modify R9503,R9504 to 10 ohm

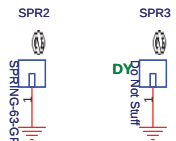


SSID = SDIO

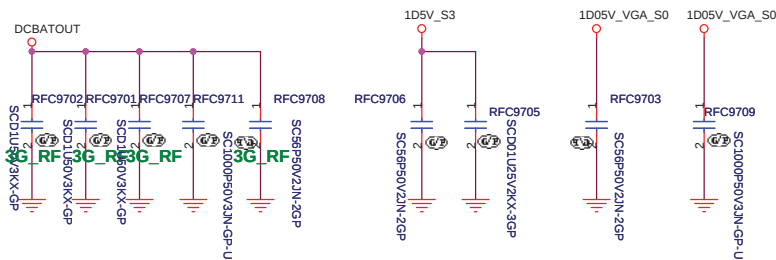
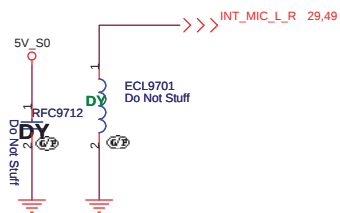
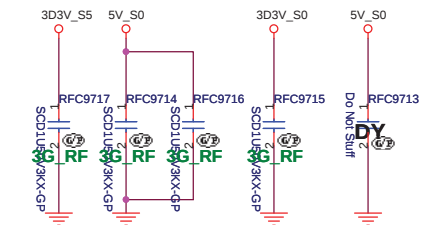


SB to -1 BOM add SPR2

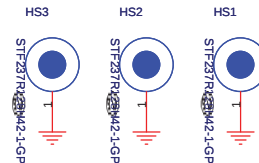
-2 delete SPR5



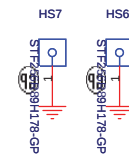
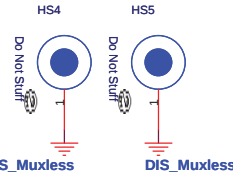
Change:34.40V16.001



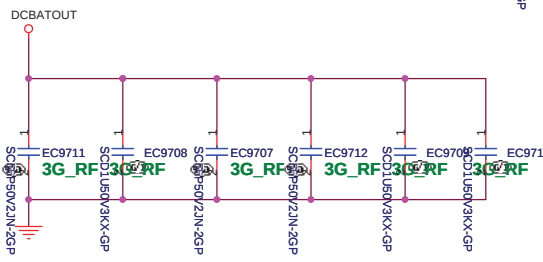
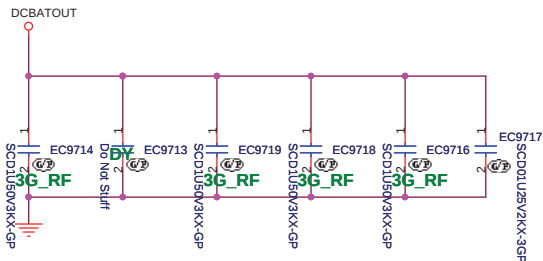
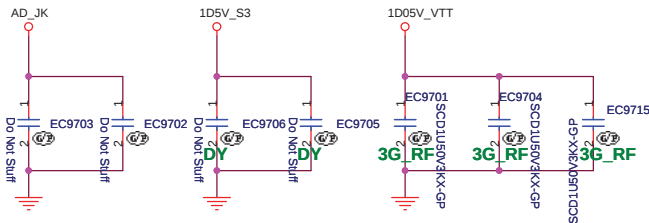
CPU



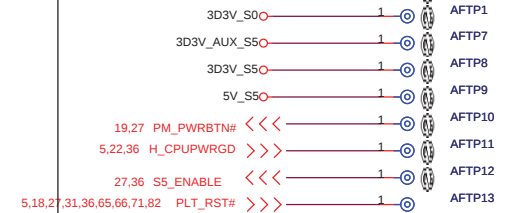
VGA



3G Sku



Check test point

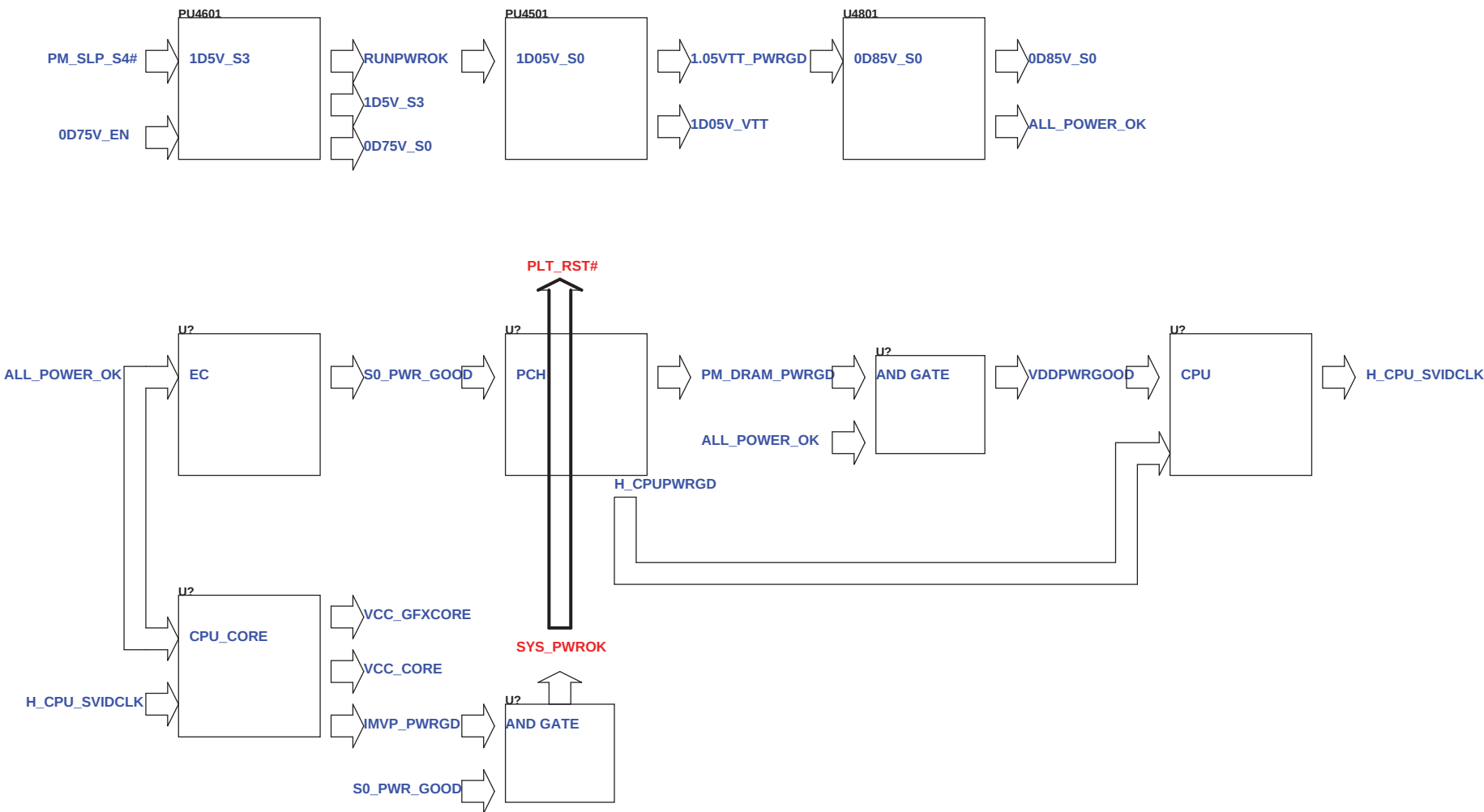


Test Point放在Dimm Door打開可量測處

HR UMA

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Title	UNUSED PARTS/EMI Capacitors	
Size A3	Document Number	Rev
	JE40-HR	-1
Date: Thursday, December 02, 2010	Sheet 97 of 102	

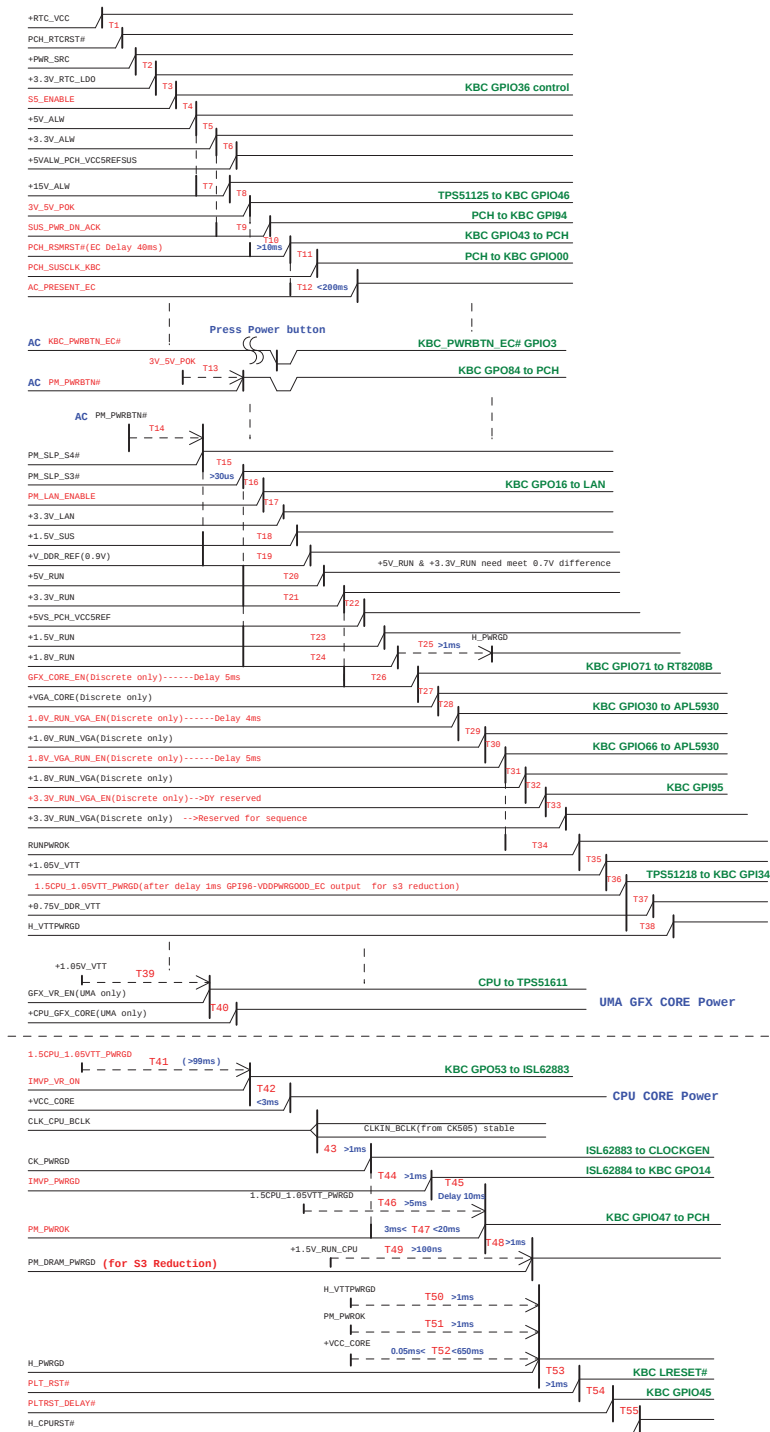
Power Sequence



Intel-Power Up Sequence

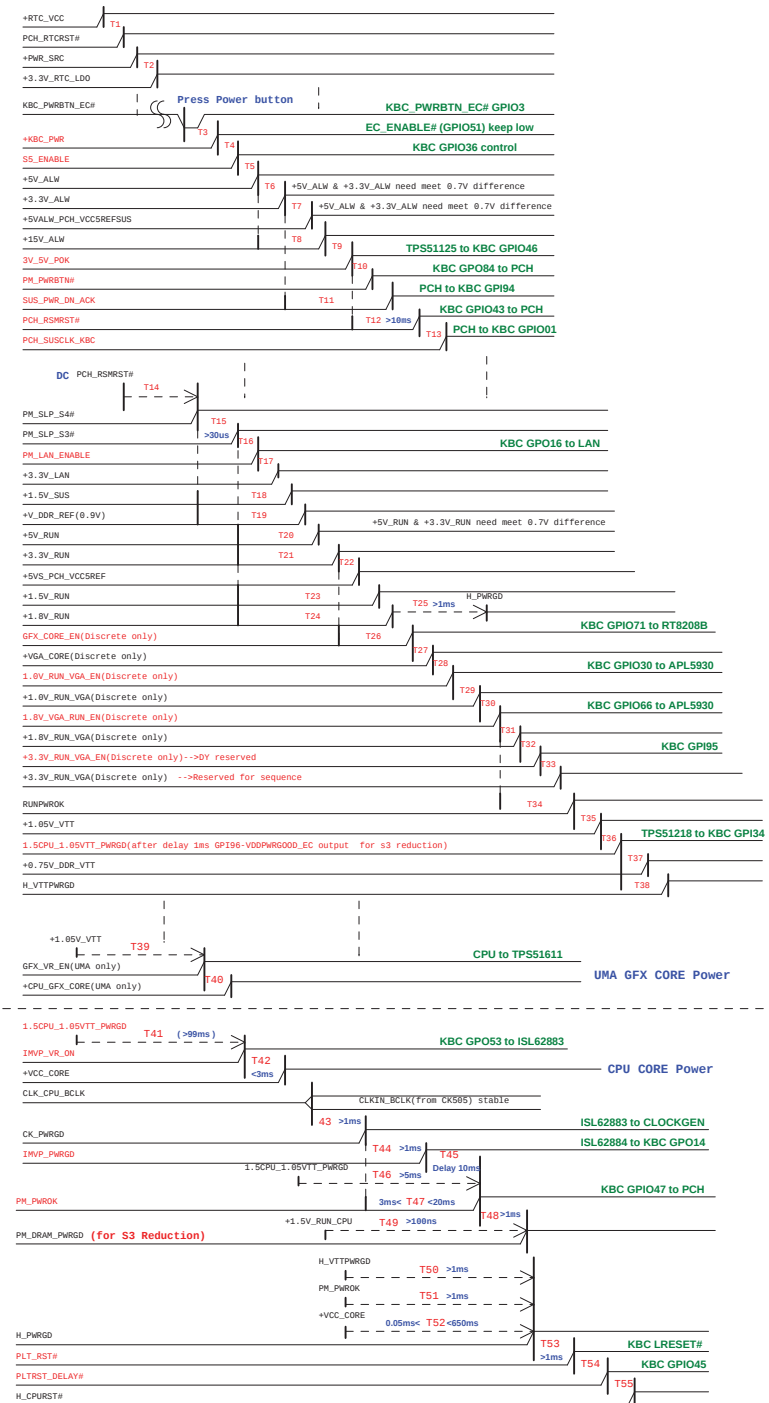
(AC mode)

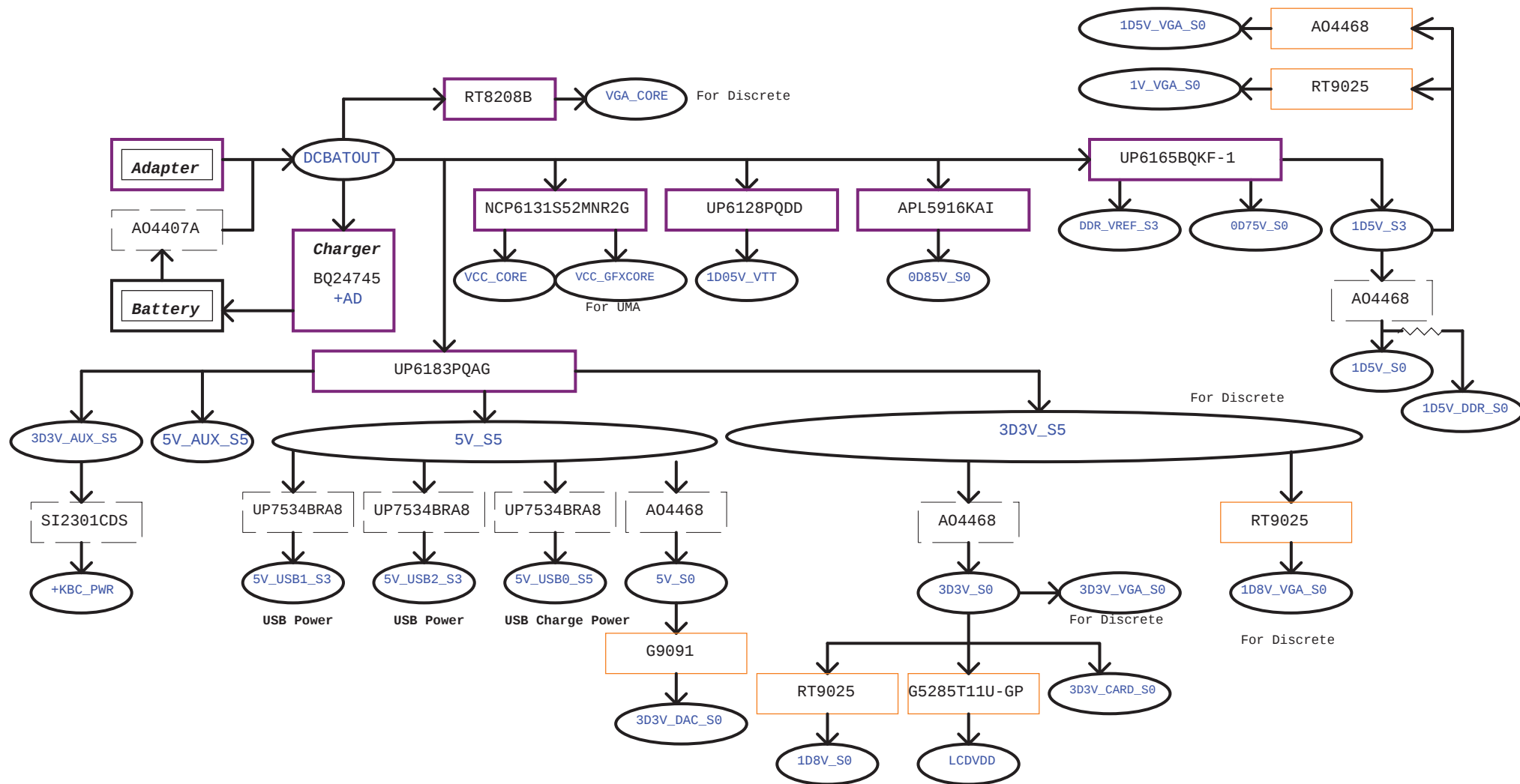
red word: KBC GPIO



(DC mode)

red word: KBC GPIO





Power Shape

Regulator

LDO

Switch

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power Block Diagram

Size

A3

Date:

Thursday, December 02, 2010

Sheet

100

of

102

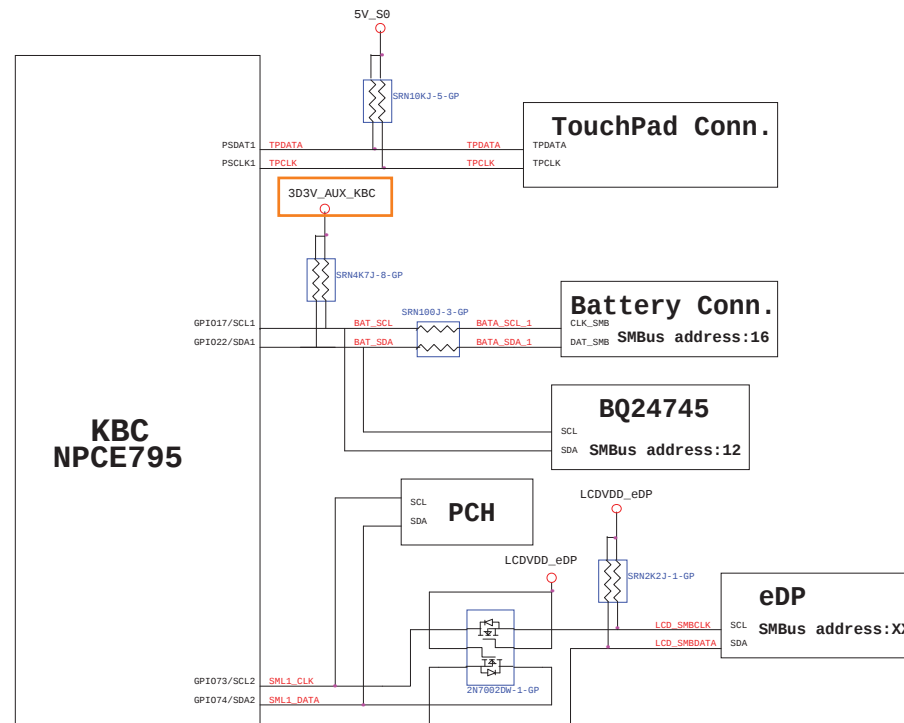
Rev

-1

Document Number

JE40-HR

KBC SMBus Block Diagram



Thermal Block Diagram

The diagram illustrates the thermal management system architecture. Key components and their connections are as follows:

- KBC NPCE795P (PAGE27):**
 - GPIO5 and GPIO92 connect to **SYS_THRM** and **CPU_THRM** nodes of the UMA Thermal P2800.
 - GPIO94 and GPIO56 connect to **VGA_THRM** of the VGA Thermal P2800.
 - GPIO4 connects to the **FAN** block via **FAN_TACH1**.
 - It also interfaces with the **FAN CONTROL P2793** via **FAN1_DAC**, **VSET**, and **VOUT**.
- UMA Thermal P2800 (PAGE28):**
 - Contains thermal nodes: **SYS_THRM**, **CPU_THRM**, **VGA_THRM**, **TDR**, **TDL**, **OTZ**, **DXP**, and **DXN**.
 - Hardware shutdown signals: **THERM_SYS_SHDN#** (connected to 2N7002) and **PURE_HW_SHUTDOWN#** (connected to VR).
 - Temperature measurement points: **T8** (near CPU) and **PH** (near GPU).
- VGA Thermal P2800 (PAGE28):**
 - Contains thermal nodes: **VGA_THRM**, **TDR**, **TDL**, **OTZ**, **DXP**, and **DXN**.
 - Temperature measurement points: **THRMDA** and **THRMDC** (near GPU).
- FAN and FAN CONTROL P2793 (PAGE28):**
 - The **FAN** block provides **TACH** feedback to the KBC.
 - The **FAN CONTROL P2793** manages fan speed via **VIN**, **VSET**, and **VOUT** signals.
- Power and Protection:**
 - A **3V/5V** supply is connected to the **EN** pin of the **VR** (Voltage Regulator).
 - The **VR** is also connected to **PG0B** and **IMVP_PMRGD** signals.

Additional notes from the diagram:

- Place near CPU PWM CORE** (near MMBT3904-3-GP).
- Put under CPU(T8 HW shutdown)** (referring to the T8 node).
- Place near GPU(DISCRETE only).** (referring to the THRMDA/THRMDC nodes).

Audio Block Diagram

The diagram illustrates the audio block architecture. On the left, a large box represents the **Codec 92HD79B1**. It contains several pins and their connections to external components on the right:

- SPEAKER**: Connected to `SPKR_PORT_D_L-` and `SPKR_PORT_D_R+`.
- HP OUT**: Connected to `HP1_PORT_B_L` and `HP1_PORT_B_R`.
- MIC IN**: Connected to `HP0_PORT_A_L`, `HP0_PORT_A_R`, and `VREFOUT_A_OR_F`.
- Digital MIC**: Connected to `DMIC_CLK/GPIO1` and `DMIC0/GPIO2`.
- Analog MIC**: Connected to `PORTC_L`, `PORTC_R`, and `VREFOUT_C`.

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Title Thermal/Audio Block Diagram			
Size	Document Number		Rev
Custom	JE40-HR		-1
Date:	Thursday, December 02, 2010		Sheet 102 of 102