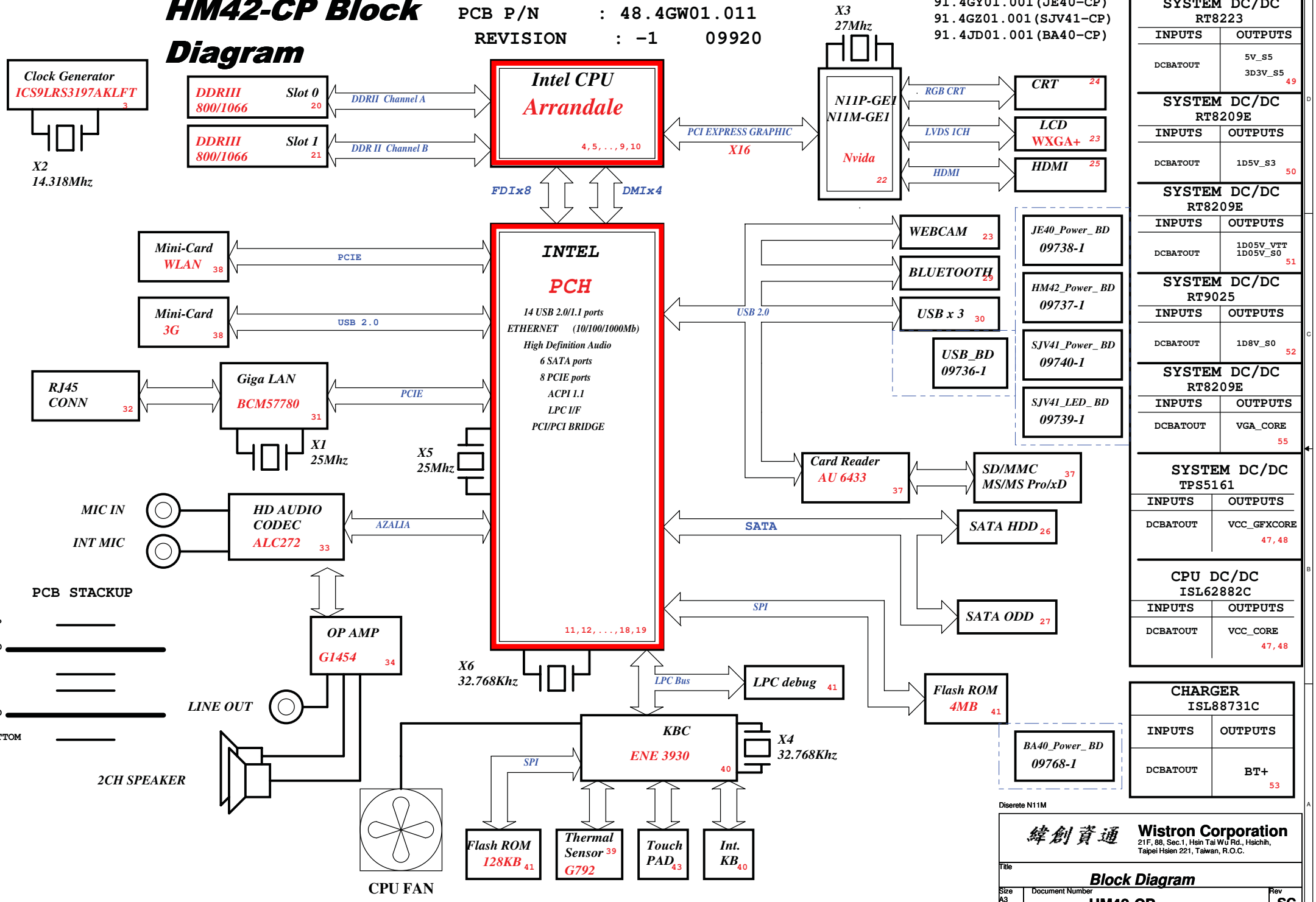
HM42-CP Block Diagram

PCB P/N : 48.4GW01.011
REVISION : -1 09920

Project code: 91.4GW01.001(HM42-CP)
91.4GY01.001(JE40-CP)
91.4GZ01.001(SJV41-CP)
91.4JD01.001(BA40-CP)



SYSTEM DC/DC RT8223	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 49

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 50

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT 1D05V_S0 51

SYSTEM DC/DC RT9025	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S0 52

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE 55

SYSTEM DC/DC TPS5161	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 47,48

CPU DC/DC ISL62882C	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 47,48

CHARGER ISL88731C	
INPUTS	OUTPUTS
DCBATOUT	BT+ 53

Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ – 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default – Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled – No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled – An external Display Port device is connected to the Embedded Display Port.	**1**
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	**1**
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	**1**
CFG[7]	**Reserved – Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** – Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	**0**

PCIE Routing

LANE1	**LAN**
LANE2	**MiniCard1**
LANE3	**MiniCard2**

USB Table

Pair	*Device*
0	*USB3*
1	*USB2*
2	*USB4*
3	*MINICARD1*
4	*WECAM*
5	*Touch Panel*
6	*NC*
7	*NC*
8	*NC*
9	*USB1(HS)*
10	*Finger Print*
11	*Blue Tooth*
12	*MINIC2*
13	*Cardreader*

<Variant Name>

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Title: ***Table of Content***

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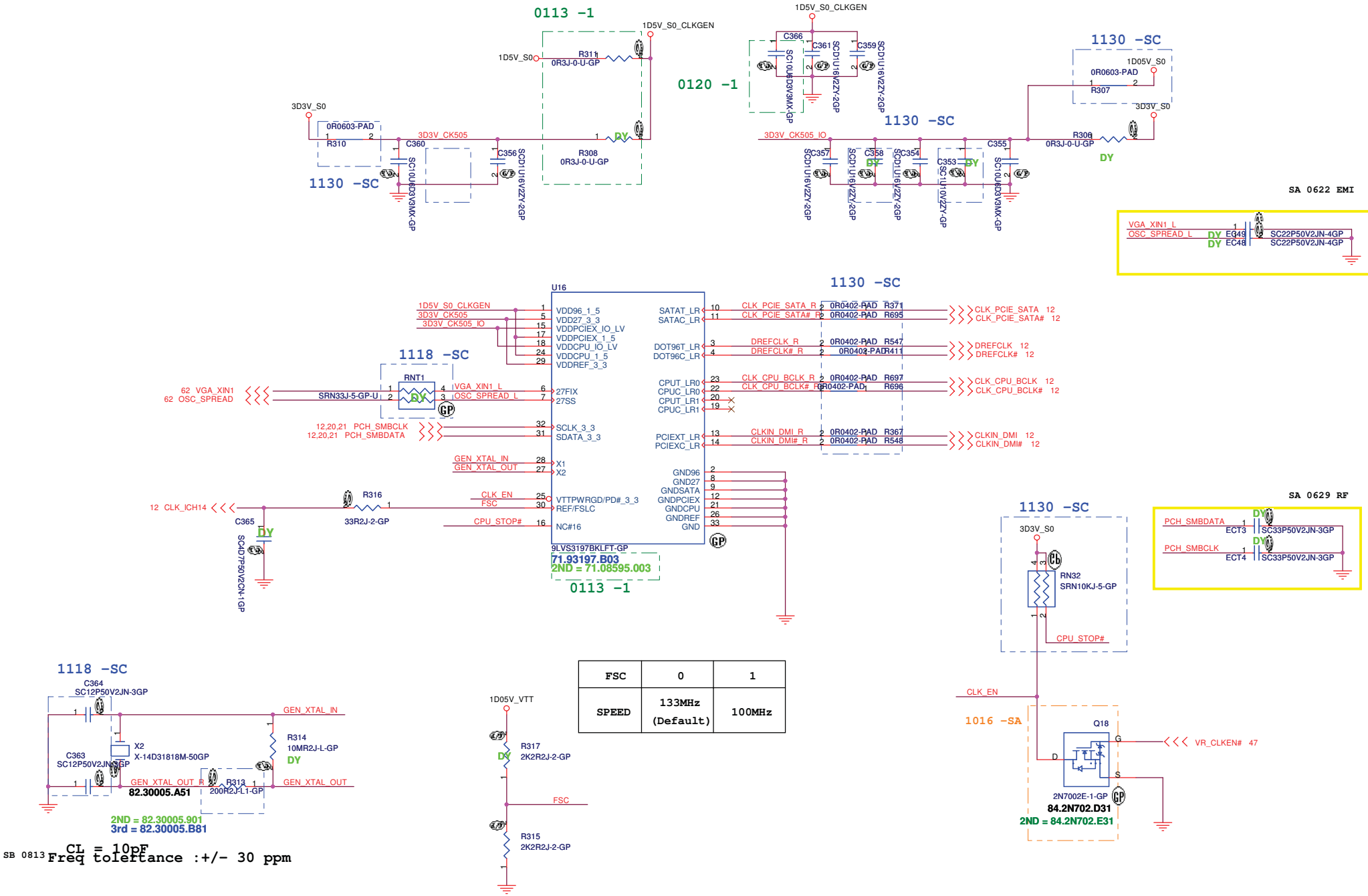

FSC	0	1
SPEED	133MHz (Default)	100MHz

UMA

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Title: Clock Generator

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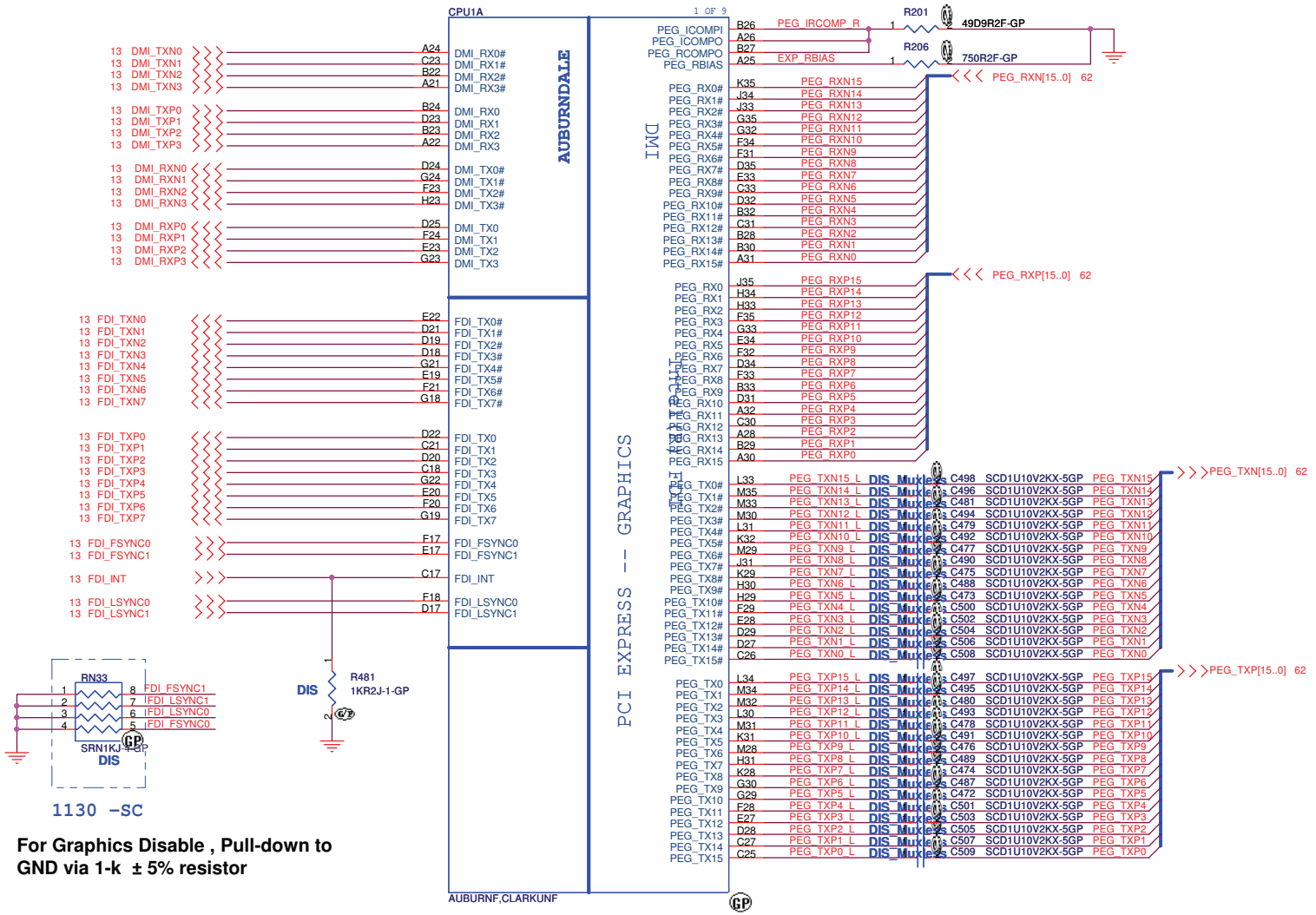

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Title: CPU (1/7)	
Size: A3	Document Number: HM42-CP
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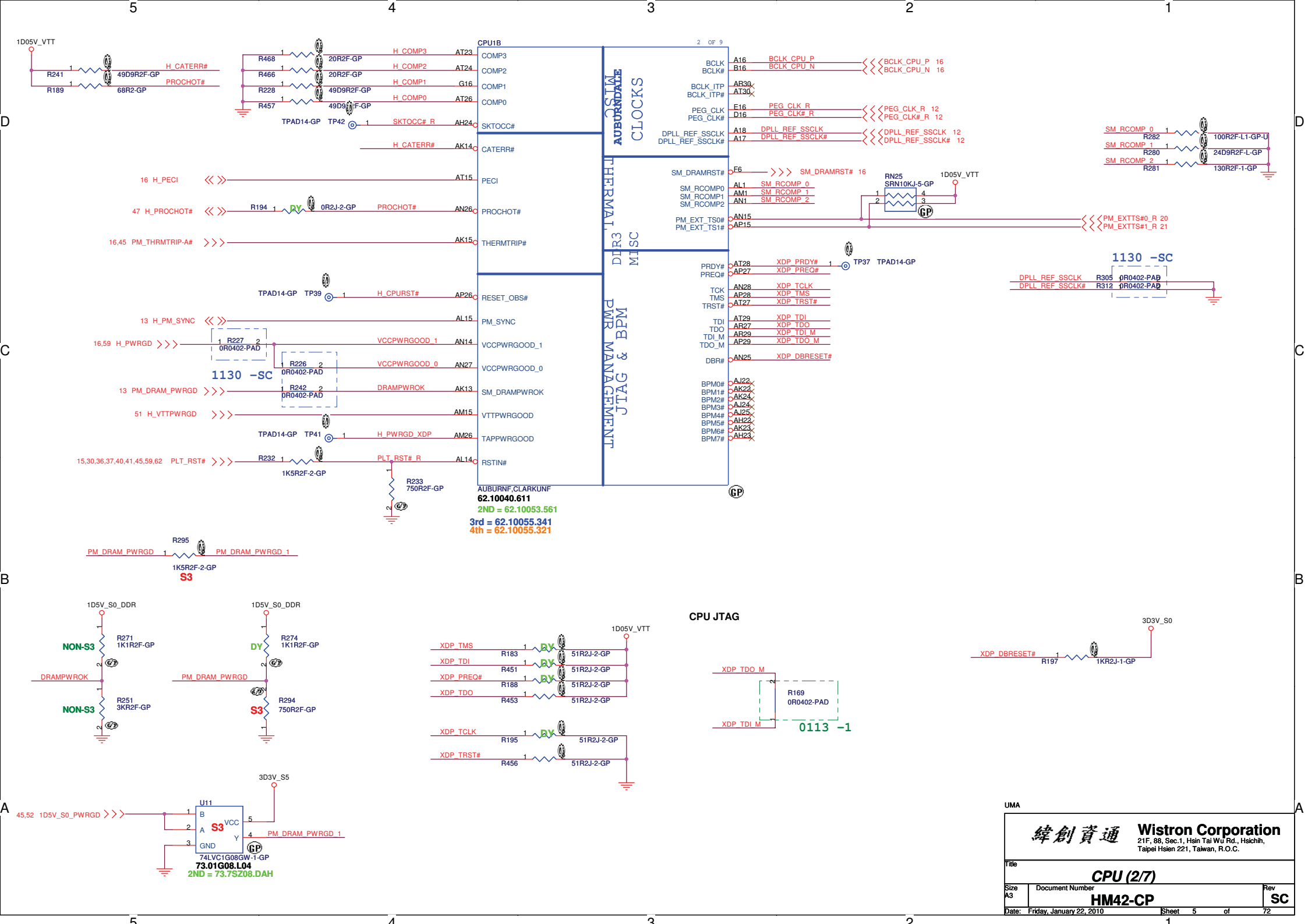
CPU1B
2 OF 9
CLOCKS
THERMAL, DIR3 MISC
JTAG & BPM
PWR MANAGEMENT
AUBURNDALE
1D05V_VTT
H_CATERR#
PROCHOT#
H_COMP3
H_COMP2
H_COMP1
H_COMP0
SKTOCC# R
H_PECI
H_PROCHOT#
PM_THRMTRIP-A#
H_CPURST#
H_PM_SYNC
H_PWRGD
PM_DRAM_PWRGD
H_VTTPWRGD
H_PWRGD_XDP
PLT_RST#
PM_DRAM_PWRGD_1
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321
1130 -SC
S3
NON-S3
DY
1D5V_S0_DDR
DRAMPWROK
XDP_TMS
XDP_TDI
XDP_PREQ#
XDP_TDO
XDP_TCLK
XDP_TRST#
CPU JTAG
XDP_TDO_M
XDP_TDI_M
0113 -1
3D3V_S0
XDP_DBRESET#
3D3V_S5
U11
74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.DAH
UMA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU (2/7)
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CPU1C

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AUBURNDALE

DDR SYSTEM MEMORY A

20 M_A_DQ[63..0]

M_A_DQ0	A10	SA_DQ0
M_A_DQ1	C10	SA_DQ1
M_A_DQ2	C7	SA_DQ2
M_A_DQ3	A7	SA_DQ3
M_A_DQ4	B10	SA_DQ4
M_A_DQ5	D10	SA_DQ5
M_A_DQ6	E10	SA_DQ6
M_A_DQ7	A8	SA_DQ7
M_A_DQ8	D8	SA_DQ8
M_A_DQ9	F10	SA_DQ9
M_A_DQ10	E6	SA_DQ10
M_A_DQ11	F7	SA_DQ11
M_A_DQ12	E9	SA_DQ12
M_A_DQ13	B7	SA_DQ13
M_A_DQ14	E7	SA_DQ14
M_A_DQ15	C6	SA_DQ15
M_A_DQ16	H10	SA_DQ16
M_A_DQ17	G8	SA_DQ17
M_A_DQ18	K7	SA_DQ18
M_A_DQ19	J8	SA_DQ19
M_A_DQ20	G7	SA_DQ20
M_A_DQ21	G10	SA_DQ21
M_A_DQ22	J7	SA_DQ22
M_A_DQ23	J10	SA_DQ23
M_A_DQ24	L7	SA_DQ24
M_A_DQ25	M6	SA_DQ25
M_A_DQ26	M8	SA_DQ26
M_A_DQ27	L9	SA_DQ27
M_A_DQ28	L6	SA_DQ28
M_A_DQ29	K8	SA_DQ29
M_A_DQ30	N8	SA_DQ30
M_A_DQ31	P9	SA_DQ31
M_A_DQ32	AH5	SA_DQ32
M_A_DQ33	AF5	SA_DQ33
M_A_DQ34	AK6	SA_DQ34
M_A_DQ35	AK7	SA_DQ35
M_A_DQ36	AF6	SA_DQ36
M_A_DQ37	AG5	SA_DQ37
M_A_DQ38	AJ7	SA_DQ38
M_A_DQ39	AJ6	SA_DQ39
M_A_DQ40	AJ10	SA_DQ40
M_A_DQ41	AJ9	SA_DQ41
M_A_DQ42	AL10	SA_DQ42
M_A_DQ43	AK12	SA_DQ43
M_A_DQ44	AK8	SA_DQ44
M_A_DQ45	AL7	SA_DQ45
M_A_DQ46	AK11	SA_DQ46
M_A_DQ47	AL8	SA_DQ47
M_A_DQ48	AN8	SA_DQ48
M_A_DQ49	AM10	SA_DQ49
M_A_DQ50	AR11	SA_DQ50
M_A_DQ51	AL11	SA_DQ51
M_A_DQ52	AM9	SA_DQ52
M_A_DQ53	AN9	SA_DQ53
M_A_DQ54	AT11	SA_DQ54
M_A_DQ55	AP12	SA_DQ55
M_A_DQ56	AM12	SA_DQ56
M_A_DQ57	AN12	SA_DQ57
M_A_DQ58	AM13	SA_DQ58
M_A_DQ59	AT14	SA_DQ59
M_A_DQ60	AT12	SA_DQ60
M_A_DQ61	AL13	SA_DQ61
M_A_DQ62	AR14	SA_DQ62
M_A_DQ63	AP14	SA_DQ63

20 M_A_BS0
20 M_A_BS1
20 M_A_BS2

AC3	SA_BS0
AB2	SA_BS1
U7	SA_BS2

20 M_A_CAS#
20 M_A_RAS#
20 M_A_WE#

AE1	SA_CAS#
AB3	SA_RAS#
AE9	SA_WE#

SA_CK0	AA6	M_CLK_DDR0 20
SA_CK0#	AA7	M_CLK_DDR#0 20
SA_CKE0	P7	M_CKE0 20
SA_CK1	Y6	M_CLK_DDR1 20
SA_CK1#	Y5	M_CLK_DDR#1 20
SA_CKE1	P6	M_CKE1 20
SA_CS0#	AE2	M_CS#0 20
SA_CS1#	AE8	M_CS#1 20
SA_ODT0	AD8	M_ODT0 20
SA_ODT1	AF9	M_ODT1 20

M_A_DM[7..0] 20

SA_DM0	B9	M_A_DM0
SA_DM1	D7	M_A_DM1
SA_DM2	H7	M_A_DM2
SA_DM3	M7	M_A_DM3
SA_DM4	AG6	M_A_DM4
SA_DM5	AM7	M_A_DM5
SA_DM6	AN10	M_A_DM6
SA_DM7	AN13	M_A_DM7

M_A_DQS#[7..0] 20

SA_DQS0#	C9	M_A_DQS#0
SA_DQS1#	F8	M_A_DQS#1
SA_DQS2#	J9	M_A_DQS#2
SA_DQS3#	N9	M_A_DQS#3
SA_DQS4#	AH7	M_A_DQS#4
SA_DQS5#	AK9	M_A_DQS#5
SA_DQS6#	AP11	M_A_DQS#6
SA_DQS7#	AT13	M_A_DQS#7

M_A_DQS[7..0] 20

SA_DQS0	C8	M_A_DQS0
SA_DQS1	F9	M_A_DQS1
SA_DQS2	H9	M_A_DQS2
SA_DQS3	M9	M_A_DQS3
SA_DQS4	AH8	M_A_DQS4
SA_DQS5	AK10	M_A_DQS5
SA_DQS6	AN11	M_A_DQS6
SA_DQS7	AR13	M_A_DQS7

M_A_A[15..0] 20

SA_MA0	Y3	M_A_A0
SA_MA1	W1	M_A_A1
SA_MA2	AA8	M_A_A2
SA_MA3	AA3	M_A_A3
SA_MA4	V1	M_A_A4
SA_MA5	AA9	M_A_A5
SA_MA6	V8	M_A_A6
SA_MA7	T1	M_A_A7
SA_MA8	Y9	M_A_A8
SA_MA9	U6	M_A_A9
SA_MA10	AD4	M_A_A10
SA_MA11	T2	M_A_A11
SA_MA12	U3	M_A_A12
SA_MA13	AG8	M_A_A13
SA_MA14	T3	M_A_A14
SA_MA15	V9	M_A_A15

AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321

CPU1D

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AUBURNDALE

DDR SYSTEM MEMORY - B

21 M_B_DQ[63..0]

M_B_DQ0	B5	SB_DQ0
M_B_DQ1	A5	SB_DQ1
M_B_DQ2	C3	SB_DQ2
M_B_DQ3	B3	SB_DQ3
M_B_DQ4	E4	SB_DQ4
M_B_DQ5	A6	SB_DQ5
M_B_DQ6	A4	SB_DQ6
M_B_DQ7	C4	SB_DQ7
M_B_DQ8	D1	SB_DQ8
M_B_DQ9	D2	SB_DQ9
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M_B_DQ12	C2	SB_DQ12
M_B_DQ13	F5	SB_DQ13
M_B_DQ14	F3	SB_DQ14
M_B_DQ15	G4	SB_DQ15
M_B_DQ16	H6	SB_DQ16
M_B_DQ17	G2	SB_DQ17
M_B_DQ18	J6	SB_DQ18
M_B_DQ19	J3	SB_DQ19
M_B_DQ20	G1	SB_DQ20
M_B_DQ21	G5	SB_DQ21
M_B_DQ22	J2	SB_DQ22
M_B_DQ23	J1	SB_DQ23
M_B_DQ24	J5	SB_DQ24
M_B_DQ25	K2	SB_DQ25
M_B_DQ26	L3	SB_DQ26
M_B_DQ27	M1	SB_DQ27
M_B_DQ28	K5	SB_DQ28
M_B_DQ29	K4	SB_DQ29
M_B_DQ30	M4	SB_DQ30
M_B_DQ31	N5	SB_DQ31
M_B_DQ32	AF3	SB_DQ32
M_B_DQ33	AG1	SB_DQ33
M_B_DQ34	AJ3	SB_DQ34
M_B_DQ35	AK1	SB_DQ35
M_B_DQ36	AG4	SB_DQ36
M_B_DQ37	AG3	SB_DQ37
M_B_DQ38	AJ4	SB_DQ38
M_B_DQ39	AH4	SB_DQ39
M_B_DQ40	AK3	SB_DQ40
M_B_DQ41	AK4	SB_DQ41
M_B_DQ42	AM6	SB_DQ42
M_B_DQ43	AN2	SB_DQ43
M_B_DQ44	AK5	SB_DQ44
M_B_DQ45	AK2	SB_DQ45
M_B_DQ46	AM4	SB_DQ46
M_B_DQ47	AM3	SB_DQ47
M_B_DQ48	AP3	SB_DQ48
M_B_DQ49	AN5	SB_DQ49
M_B_DQ50	AT4	SB_DQ50
M_B_DQ51	AN6	SB_DQ51
M_B_DQ52	AN4	SB_DQ52
M_B_DQ53	AN3	SB_DQ53
M_B_DQ54	AT5	SB_DQ54
M_B_DQ55	AT6	SB_DQ55
M_B_DQ56	AN7	SB_DQ56
M_B_DQ57	AP6	SB_DQ57
M_B_DQ58	AP8	SB_DQ58
M_B_DQ59	AT9	SB_DQ59
M_B_DQ60	AT7	SB_DQ60
M_B_DQ61	AP9	SB_DQ61
M_B_DQ62	AR10	SB_DQ62
M_B_DQ63	AT10	SB_DQ63

21 M_B_BS0
21 M_B_BS1
21 M_B_BS2

AB1	SB_BS0
W5	SB_BS1
R7	SB_BS2

21 M_B_CAS#
21 M_B_RAS#
21 M_B_WE#

AC5	SB_CAS#
Y7	SB_RAS#
AC6	SB_WE#

SB_CK0	W8	M_CLK_DDR2 21
SB_CK0#	W9	M_CLK_DDR#2 21
SB_CKE0	M3	M_CKE2 21
SB_CK1	V7	M_CLK_DDR3 21
SB_CK1#	V6	M_CLK_DDR#3 21
SB_CKE1	M2	M_CKE3 21
SB_CS0#	AB8	M_CS#2 21
SB_CS1#	AD6	M_CS#3 21
SB_ODT0	AC7	M_ODT2 21
SB_ODT1	AD1	M_ODT3 21

M_B_DM[7..0] 21

SB_DM0	D4	M_B_DM0
SB_DM1	E1	M_B_DM1
SB_DM2	H3	M_B_DM2
SB_DM3	K1	M_B_DM3
SB_DM4	AH1	M_B_DM4
SB_DM5	AL2	M_B_DM5
SB_DM6	AR4	M_B_DM6
SB_DM7	AT8	M_B_DM7

M_B_DQS#[7..0] 21

SB_DQS0#	D5	M_B_DQS#0
SB_DQS1#	F4	M_B_DQS#1
SB_DQS2#	J4	M_B_DQS#2
SB_DQS3#	L4	M_B_DQS#3
SB_DQS4#	AH2	M_B_DQS#4
SB_DQS5#	AL4	M_B_DQS#5
SB_DQS6#	AR5	M_B_DQS#6
SB_DQS7#	AR8	M_B_DQS#7

M_B_DQS[7..0] 21

SB_DQS0	C5	M_B_DQS0
SB_DQS1	E3	M_B_DQS1
SB_DQS2	H4	M_B_DQS2
SB_DQS3	M5	M_B_DQS3
SB_DQS4	AG2	M_B_DQS4
SB_DQS5	AL5	M_B_DQS5
SB_DQS6	AP5	M_B_DQS6
SB_DQS7	AR7	M_B_DQS7

M_B_A[15..0] 21

SB_MA0	U5	M_B_A0
SB_MA1	V2	M_B_A1
SB_MA2	T5	M_B_A2
SB_MA3	V3	M_B_A3
SB_MA4	R1	M_B_A4
SB_MA5	T8	M_B_A5
SB_MA6	R2	M_B_A6
SB_MA7	R6	M_B_A7
SB_MA8	R4	M_B_A8
SB_MA9	R5	M_B_A9
SB_MA10	AB5	M_B_A10
SB_MA11	P3	M_B_A11
SB_MA12	R3	M_B_A12
SB_MA13	AF7	M_B_A13
SB_MA14	P5	M_B_A14
SB_MA15	N1	M_B_A15

AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561
3rd = 62.10055.341
4th = 62.10055.321

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (3/7)

Size	Document Number	Rev
A3	HM42-CP	SC

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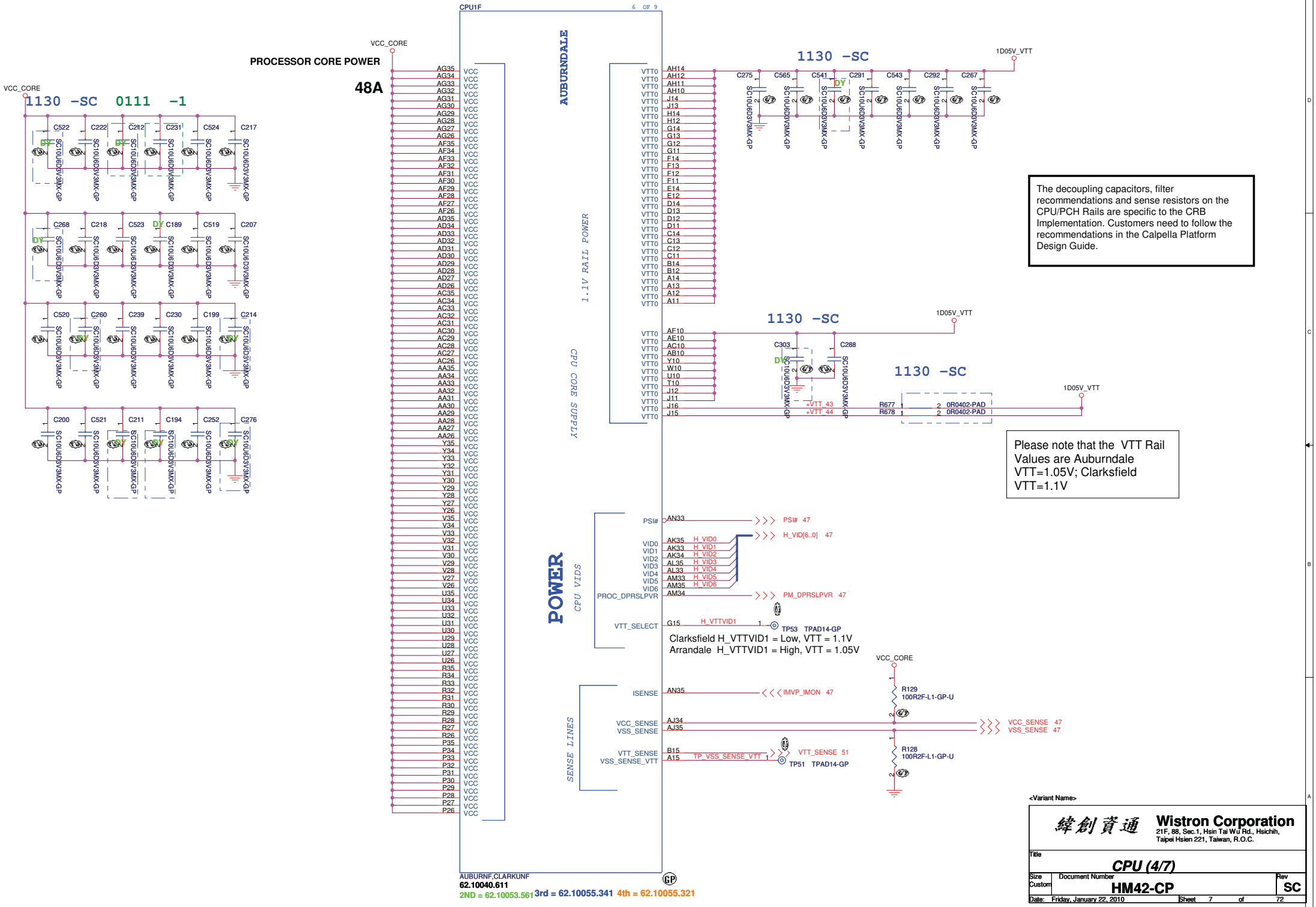
VCC_CORE
1130 -SC 0111 -1
C522 C222 C212 C231 C524 C217
C268 C218 C523 C189 C519 C207
C520 C260 C239 C230 C199 C214
C200 C521 C211 C194 C252 C276
SC10U6D3V3MX-GP
DY
PROCESSOR CORE POWER
48A
CPU1F
6 OF 9
AUBURNDALE
1.1V RAIL POWER
CPU CORE SUPPLY
VCC_CORE
AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC
1130 -SC
1D05V_VTT
C275 C565 C541 C291 C543 C292 C267
SC10U6D3V3MX-GP
VTT0
AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11
1130 -SC
1D05V_VTT
AF10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15
C303 C288
+VTT_43 +VTT_44
R677 R678
0R0402-PAD
1130 -SC
1D05V_VTT
The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
POWER
CPU VIDS
PSI# AN33 PSI# 47
VID0 AK35 H_VID0
VID1 AK33 H_VID1
VID2 AK34 H_VID2
VID3 AL35 H_VID3
VID4 AL33 H_VID4
VID5 AM33 H_VID5
VID6 AM35 H_VID6
H_VID[6..0] 47
PROC_DPRSLPVR AM34 PM_DPRSLPVR 47
VTT_SELECT G15 H_VTTVID1
TP53 TPAD14-GP
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
SENSE LINES
ISENSE AN35 IMVP_IMON 47
VCC_SENSE AJ34 VCC_SENSE 47
VSS_SENSE AJ35 VSS_SENSE 47
VTT_SENSE B15 VTT_SENSE 51
VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT
TP51 TPAD14-GP
VCC_CORE
R129 100R2F-L1-GP-U
R128 100R2F-L1-GP-U
AUBURNF,CLARKUNF
62.10040.611
2ND = 62.10053.561 3rd = 62.10055.341 4th = 62.10055.321
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CPU (4/7)
Size Custom
Document Number HM42-CP
Rev SC
Date: Friday, January 22, 2010
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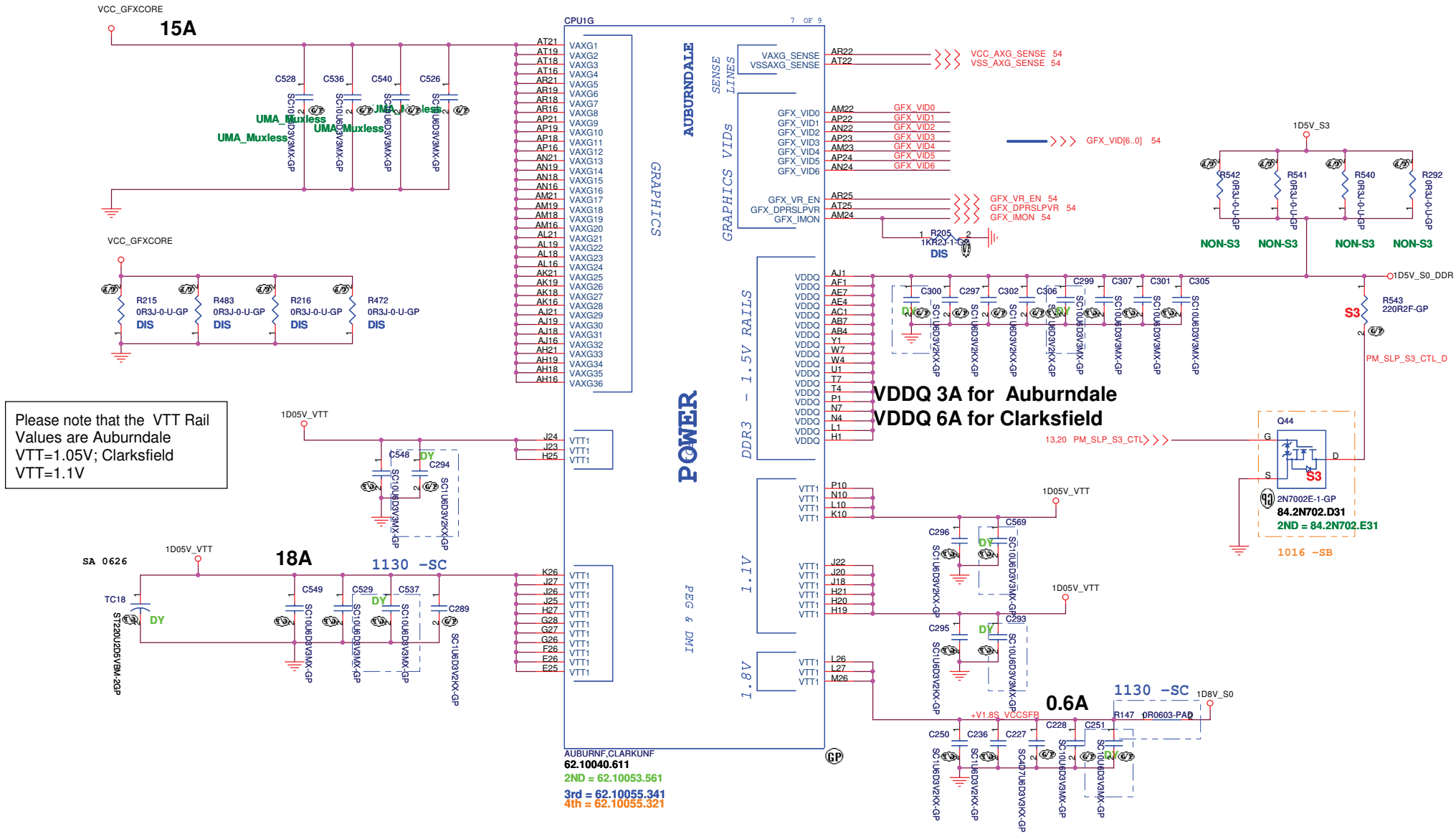
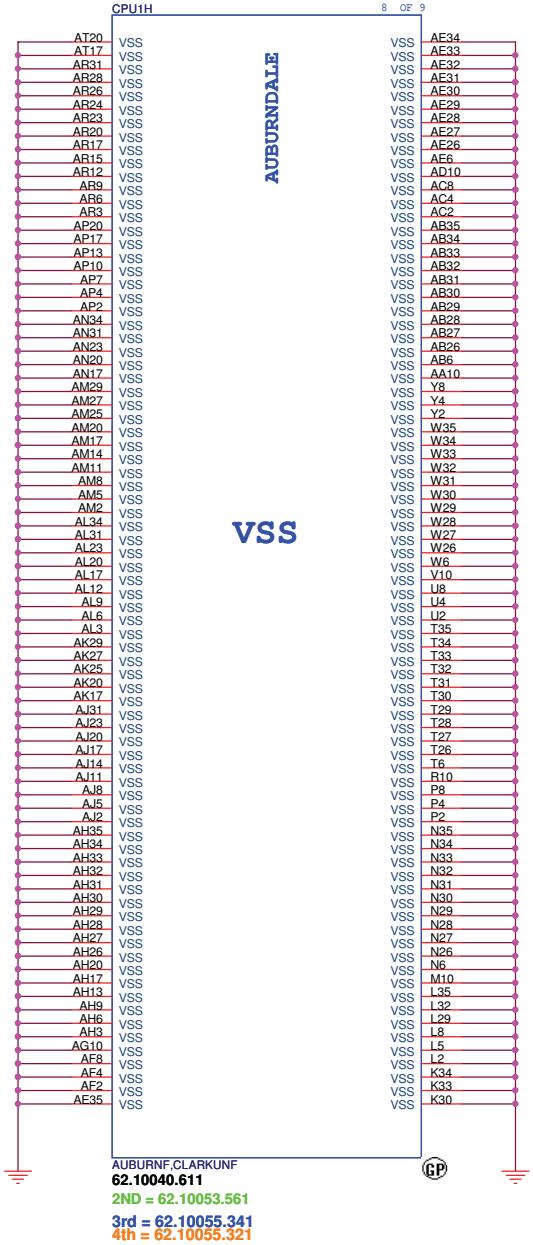
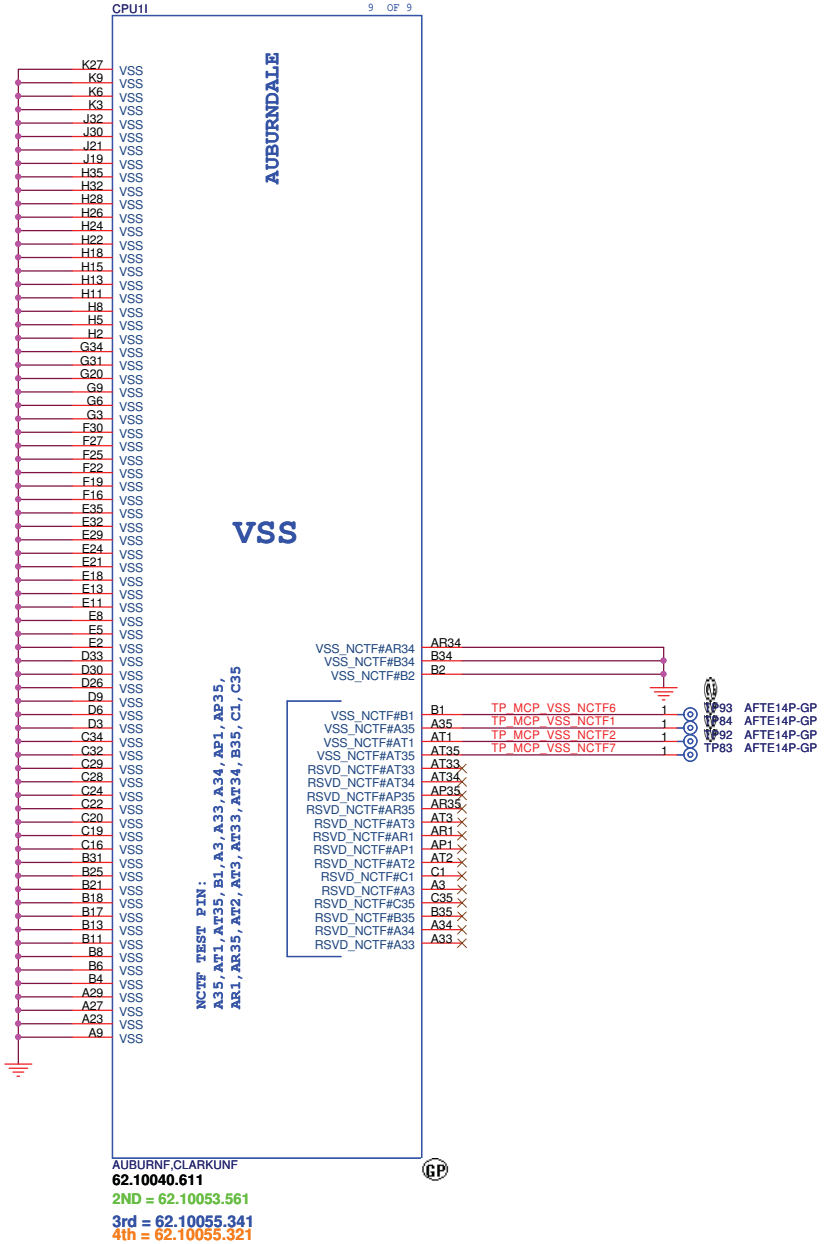


UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (5/7)***	
Size A3	Document Number **HM42-CP**	Rev **SC**
Date: Friday, January 22, 2010	Sheet 8 of 72	





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *CPU (6/7)*

Size	Document Number	Rev
A3	HM42-CP	SC

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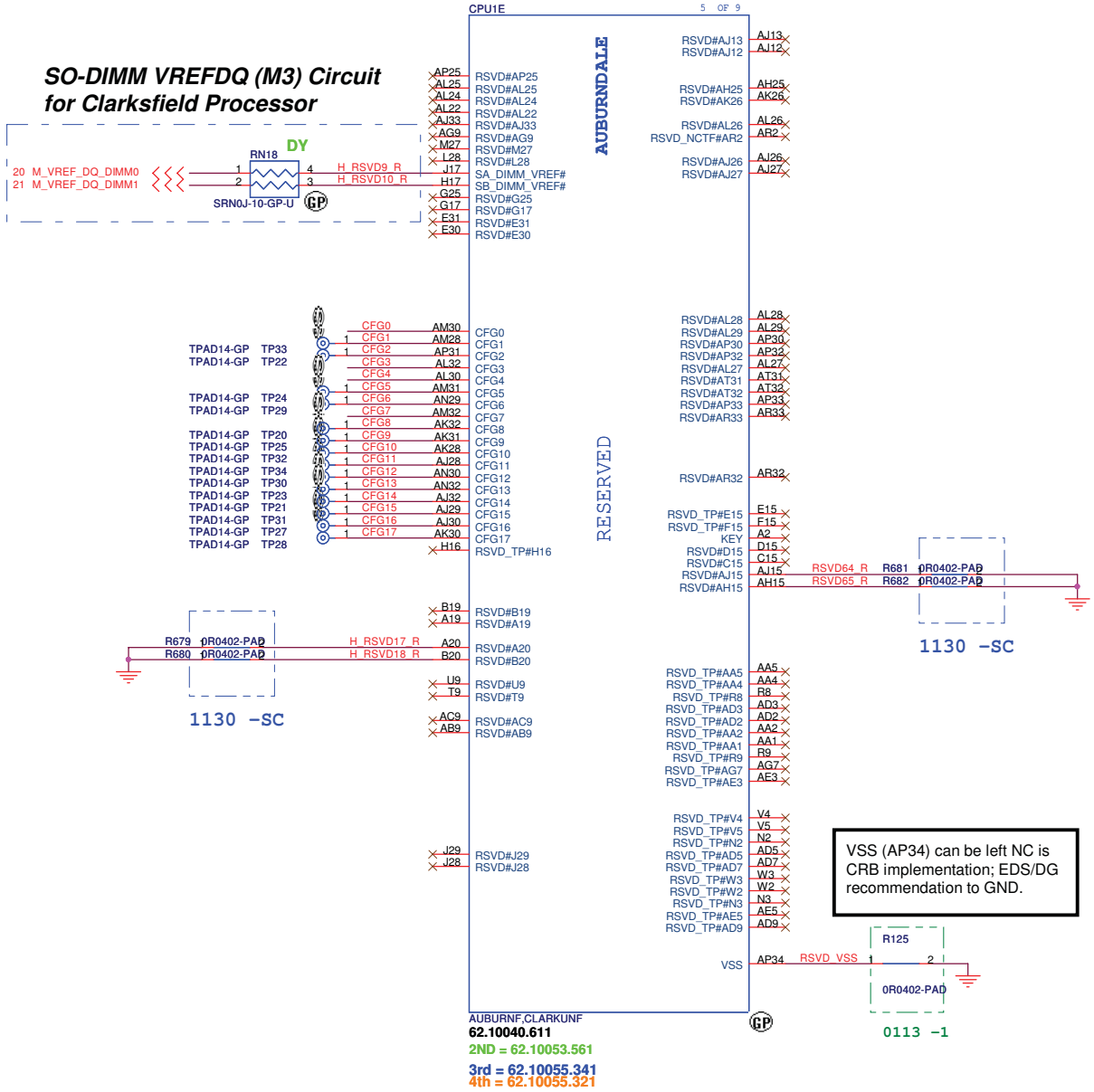

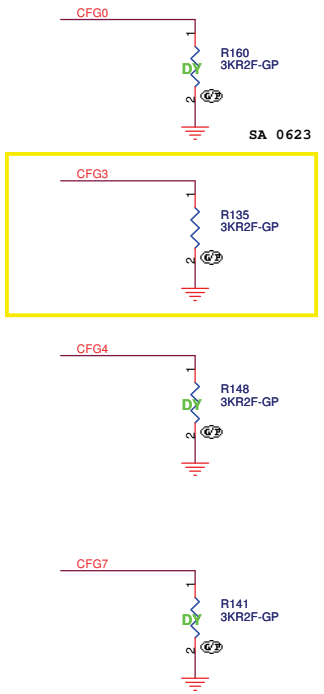

Processor Strapping

PCI-Express Configuration Select	
CFG0	1:Single PEG(Default) 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation(Default) 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port (Default) 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (7/7)

Size: A3 | Document Number: HM42-CP | Rev: SC

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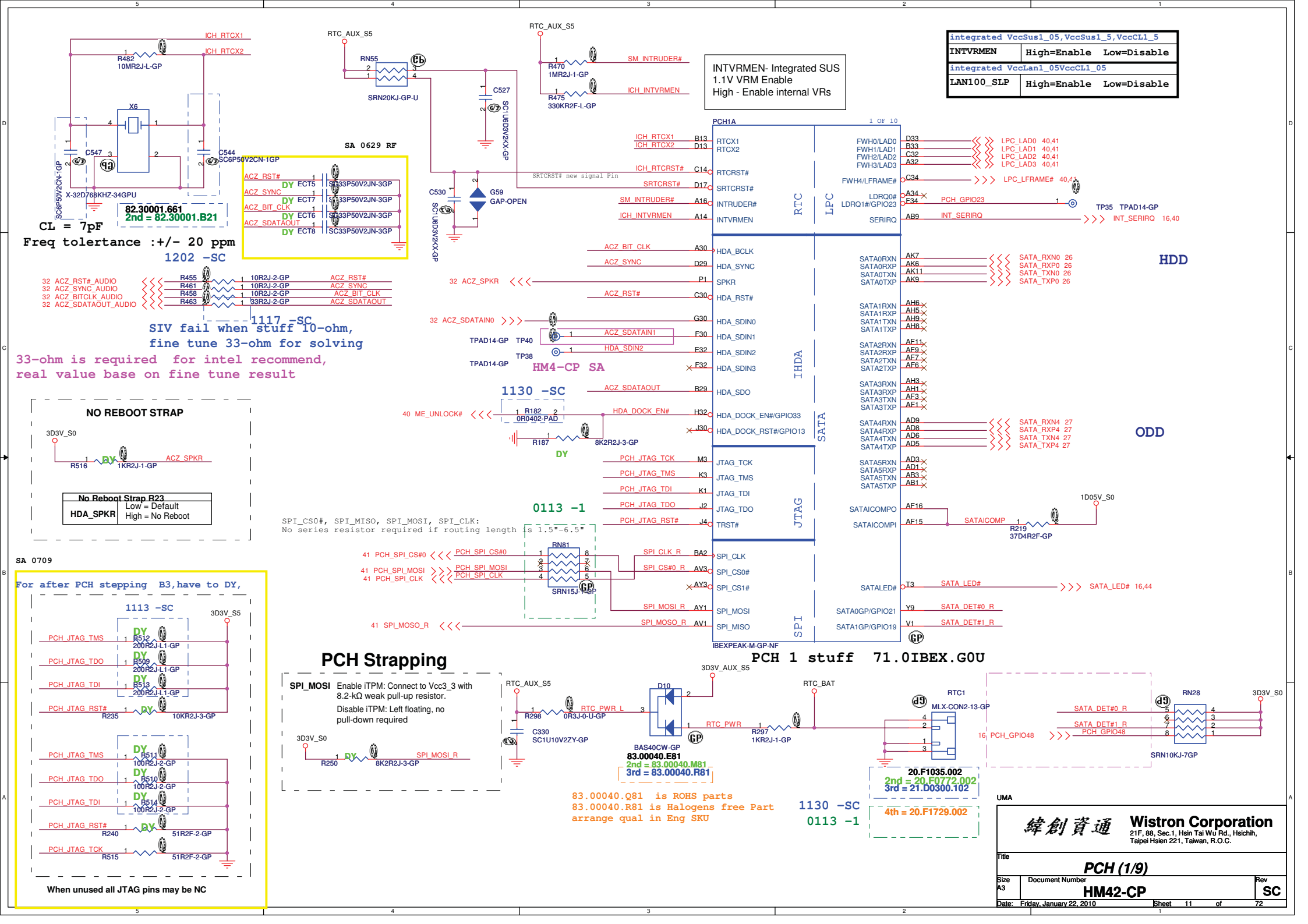
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs
PCH1A
1 OF 10
RTC
LPC
IHDA
SATA
JTAG
SPI
IBEXPEAK-M-GP-NF
ICH_RTCX1
ICH_RTCX2
R482 10MR2J-L-GP
X6
X-32D768KHZ-34GPU
C547
C544
SC6P50V2CN-1GP
82.30001.661
2nd = 82.30001.B21
CL = 7pF
Freq tolertance :+/- 20 ppm
1202 -SC
RTC_AUX_S5
RN55
SRN20KJ-GP-U
C527
SC1U6D3V2KX-GP
C530
G59
GAP-OPEN
SA 0629 RF
ACZ_RST#
ACZ_SYNC
ACZ_BIT_CLK
ACZ_SDATAOUT
SC33P50V2JN-3GP
R470 1MR2J-1-GP
R475 330KR2F-L-GP
SM_INTRUDER#
ICH_INTVRMEN
SRTCRST# new signal Pin
ICH_RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LPC_LAD0 40,41
LPC_LAD1 40,41
LPC_LAD2 40,41
LPC_LAD3 40,41
LPC_LFRAME# 40,41
PCH_GPIO23
TP35 TPAD14-GP
INT_SERIRQ
INT_SERIRQ 16,40
HDD
SATA_RXN0 26
SATA_RXP0 26
SATA_TXN0 26
SATA_TXP0 26
ODD
SATA_RXN4 27
SATA_RXP4 27
SATA_TXN4 27
SATA_TXP4 27
SATA_LED# 16,44
SATA_DET#0_R
SATA_DET#1_R
R455 10R2J-2-GP
R461 10R2J-2-GP
R458 10R2J-2-GP
R463 33R2J-2-GP
32 ACZ_RST#_AUDIO
32 ACZ_SYNC_AUDIO
32 ACZ_BITCLK_AUDIO
32 ACZ_SDATAOUT_AUDIO
1117 -SC
SIV fail when stuff 10-ohm,
fine tune 33-ohm for solving
33-ohm is required for intel recommend,
real value base on fine tune result
32 ACZ_SPKR
32 ACZ_SDATAIN0
TPAD14-GP TP40
TPAD14-GP TP38
HM4-CP SA
1130 -SC
40 ME_UNLOCK#
R182 0R0402-PAD
R187 8K2R2J-3-GP
DY
0113 -1
SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"
RN81
SRN15J-GP
41 PCH_SPI_CS#0
41 PCH_SPI_MOSI
41 PCH_SPI_CLK
41 SPI_MOSO_R
1D05V_S0
R219 37D4R2F-GP
SATAICOMP
NO REBOOT STRAP
3D3V_S0
R516 1KR2J-1-GP
ACZ_SPKR
No Reboot Strap R23
HDA_SPKR
Low = Default
High = No Reboot
SA 0709
For after PCH stepping B3,have to DY,
1113 -SC
3D3V_S5
PCH_JTAG_TMS
PCH_JTAG_TDO
PCH_JTAG_TDI
PCH_JTAG_RST#
PCH_JTAG_TCK
R512 200R2J-L1-GP
R509 200R2J-L1-GP
R513 200R2J-L1-GP
R235 10KR2J-3-GP
R511 100R2J-2-GP
R510 100R2J-2-GP
R514 100R2J-2-GP
R240 51R2F-2-GP
R515 51R2F-2-GP
When unused all JTAG pins may be NC
PCH Strapping
SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required
R250 8K2R2J-3-GP
RTC_PWR_L
R298 0R3J-0-U-GP
C330 SC1U10V2ZY-GP
D10
BAS40CW-GP
83.00040.E81
2nd = 83.00040.M81
3rd = 83.00040.R81
RTC_PWR
R297 1KR2J-1-GP
RTC_BAT
RTC1
MLX-CON2-13-GP
20.F1035.002
2nd = 20.F0772.002
3rd = 21.D0300.102
4th = 20.F1729.002
RN28
SRN10KJ-7GP
16 PCH_GPIO48
83.00040.Q81 is ROHS parts
83.00040.R81 is Halogens free Part
arrange qual in Eng SKU
1130 -SC
0113 -1
PCH 1 stuff 71.0IBEX.G0U
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (1/9)
Size A3
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LAN

MINICARD1

MINICARD2

PCH1B

2 OF 10

PCI-E*

SMBus

Controller Link

PEG

From CLK BUFFER

Clock Flex

IBEXPEAK-M-GP-NF

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

if use ENE KBC stuff 2.2K-ohm thermal IC will be abnormal

1130 -SC

1105 -SC

CL = 12pF
Freq tolertance :+/- 30 ppm

SB 0812

1117 -SC

84.2N702.A3F
2nd = 84.DM601.03F

82.30020.971

82.30020.851
2nd = 82.30020.791
3rd = 82.30020.A31

UMA

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Title	PCH (2/9)
Size A3	Document Number HM42-CP
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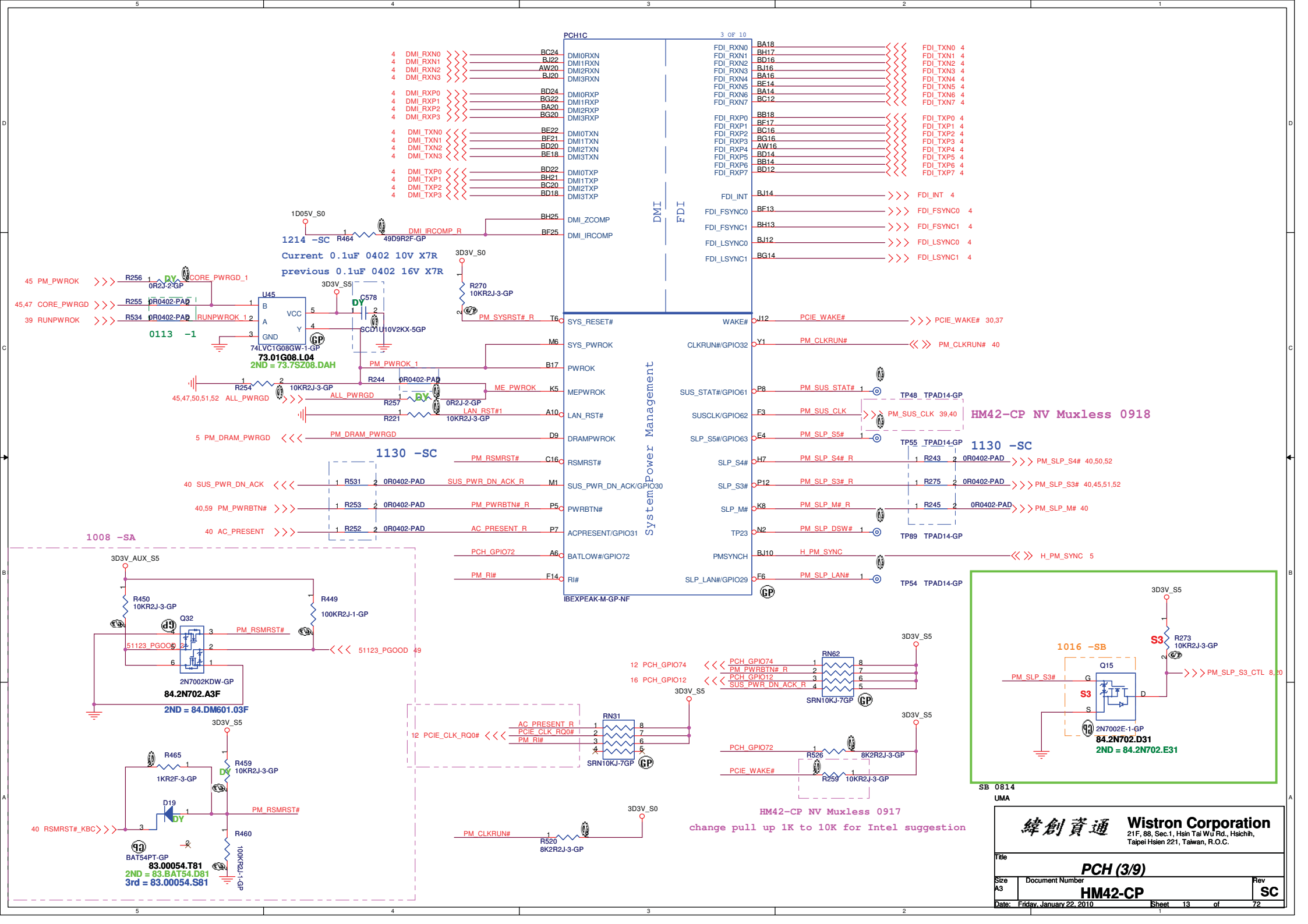
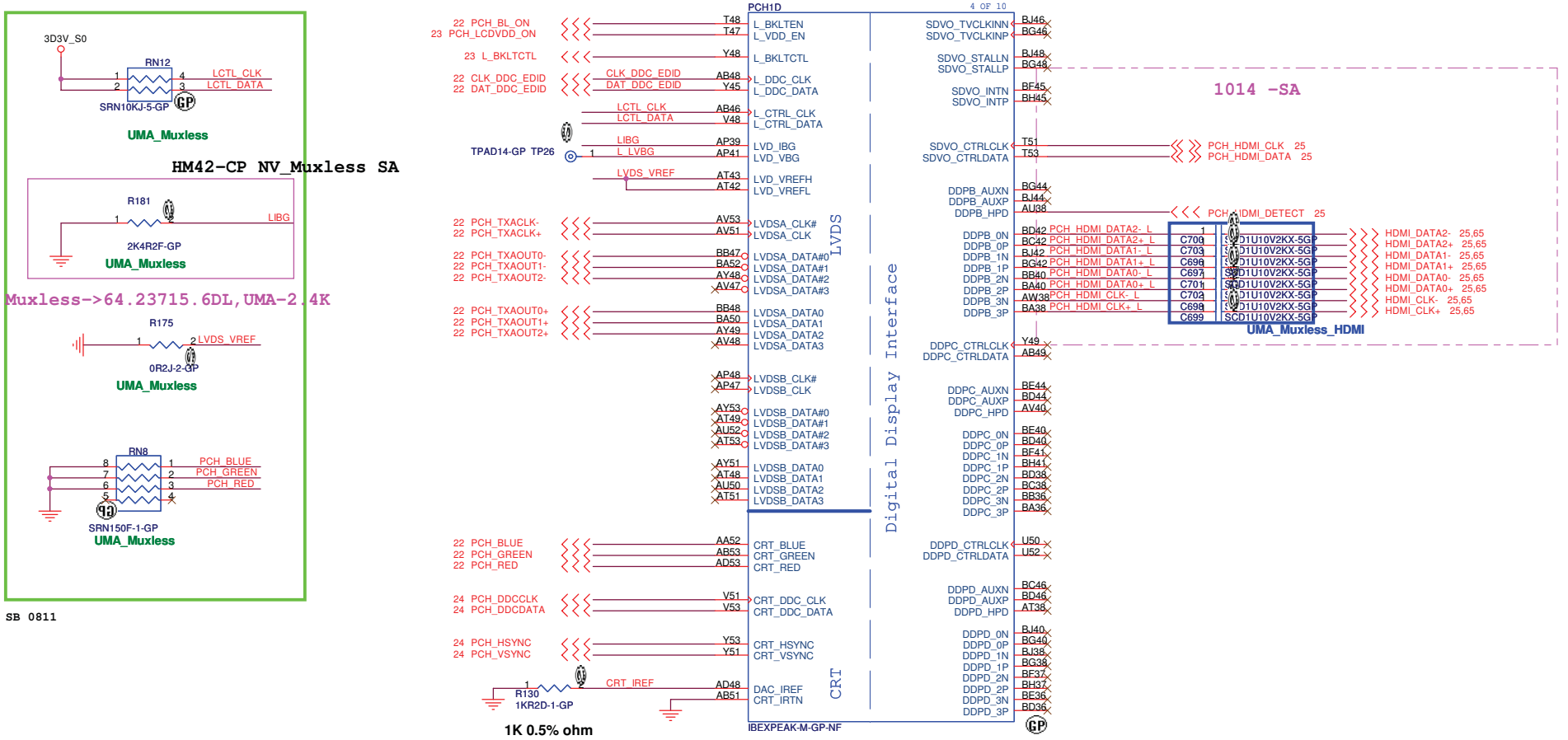

PCH1C
3 OF 10
DMI
FDI
System Power Management
IBEXPEAK-M-GP-NF
1214 -SC
Current 0.1uF 0402 10V X7R
previous 0.1uF 0402 16V X7R
0113 -1
73.01G08.L04
2ND = 73.7SZ08.DAH
1130 -SC
HM42-CP NV Muxless 0918
1008 -SA
84.2N702.A3F
2ND = 84.DM601.03F
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.00054.S81
1016 -SB
84.2N702.D31
2ND = 84.2N702.E31
SB 0814
UMA
HM42-CP NV Muxless 0917
change pull up 1K to 10K for Intel suggestion
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
PCH (3/9)
HM42-CP
SC
Friday, January 22, 2010
13
72



<Core Design>

Wistron Corporation
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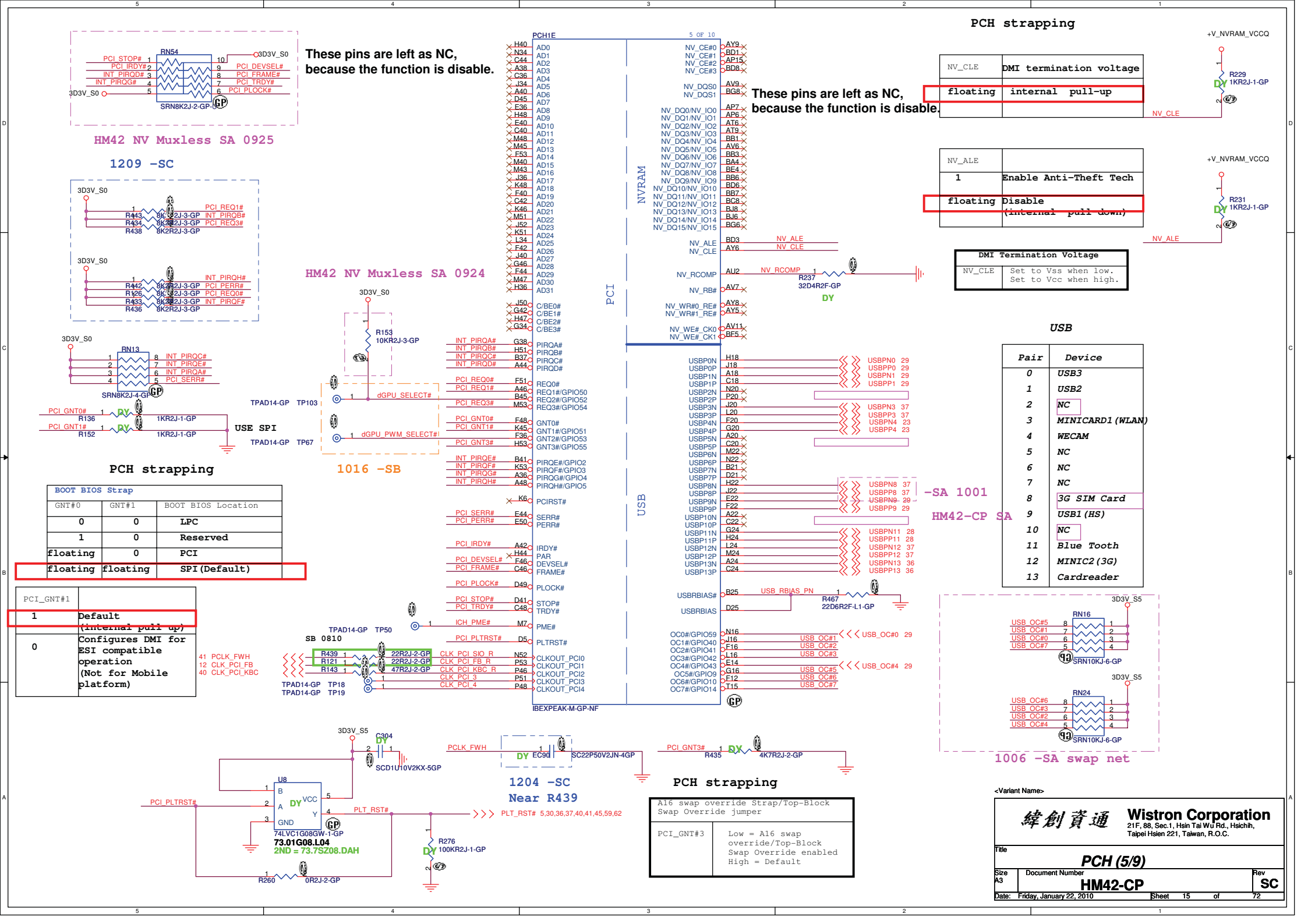
Title: PCH (4/9)

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 14 of 72


These pins are left as NC, because the function is disable.
HM42 NV Muxless SA 0925
1209 -SC
HM42 NV Muxless SA 0924
1016 -SB
USE SPI
PCH strapping
BOOT BIOS Strap
GNT#0 GNT#1 BOOT BIOS Location
0 0 LPC
1 0 Reserved
floating 0 PCI
floating floating SPI(Default)
PCI_GNT#1
1 Default (internal pull up)
0 Configures DMI for ESI compatible operation (Not for Mobile platform)
These pins are left as NC, because the function is disable.
PCH strapping
NV_CLE DMI termination voltage
floating internal pull-up
NV_ALE
1 Enable Anti-Theft Tech
floating Disable (internal pull down)
DMI Termination Voltage
NV_CLE Set to Vss when low. Set to Vcc when high.
USB
Pair Device
0 USB3
1 USB2
2 NC
3 MINICARD1(WLAN)
4 WECAM
5 NC
6 NC
7 NC
8 3G SIM Card
9 USB1(HS)
10 NC
11 Blue Tooth
12 MINIC2(3G)
13 Cardreader
-SA 1001
HM42-CP SA
1006 -SA swap net
1204 -SC
Near R439
PCH strapping
A16 swap override Strap/Top-Block Swap Override jumper
PCI_GNT#3 Low = A16 swap override/Top-Block Swap Override enabled
High = Default
PCH1E
IBEXPEAK-M-GP-NF
NVRAM
PCI
USB
SB 0810
73.01G08.L04
2ND = 73.7SZ08.DAH
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (5/9)
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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

HM42-CP_NV _Muxless SA

HM42-CP_NV _Muxless SA

HM42-CP_NV _Muxless SA

H: No SG function
L: SG Support

SB 0819
SB 0814
SB 0722
SB 0812

1016 -SB

Placed Within 2" from PCH

0121 -1

UMA_Muxless

DIS_UMA

Muxless

DIS

UMA_DISCRETE#
Optimus: HIGH
UMA: HIGH
DIS ONLY: LOW

NCTF TEST PIN:
A4,A49,A5,A50,A52,A53,B2,B53,BE1,
BE53,BF1,BF53,BH1,BH53,BJ1,BJ2,BJ4,
BJ49,BJ5,BJ50,BJ52,BJ53,D1,D53,E1,E53

IBEXPEAK-M-GP-NF

UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: PCH (6/9)

Size	Document Number	Rev
A3	HM42-CP	SC

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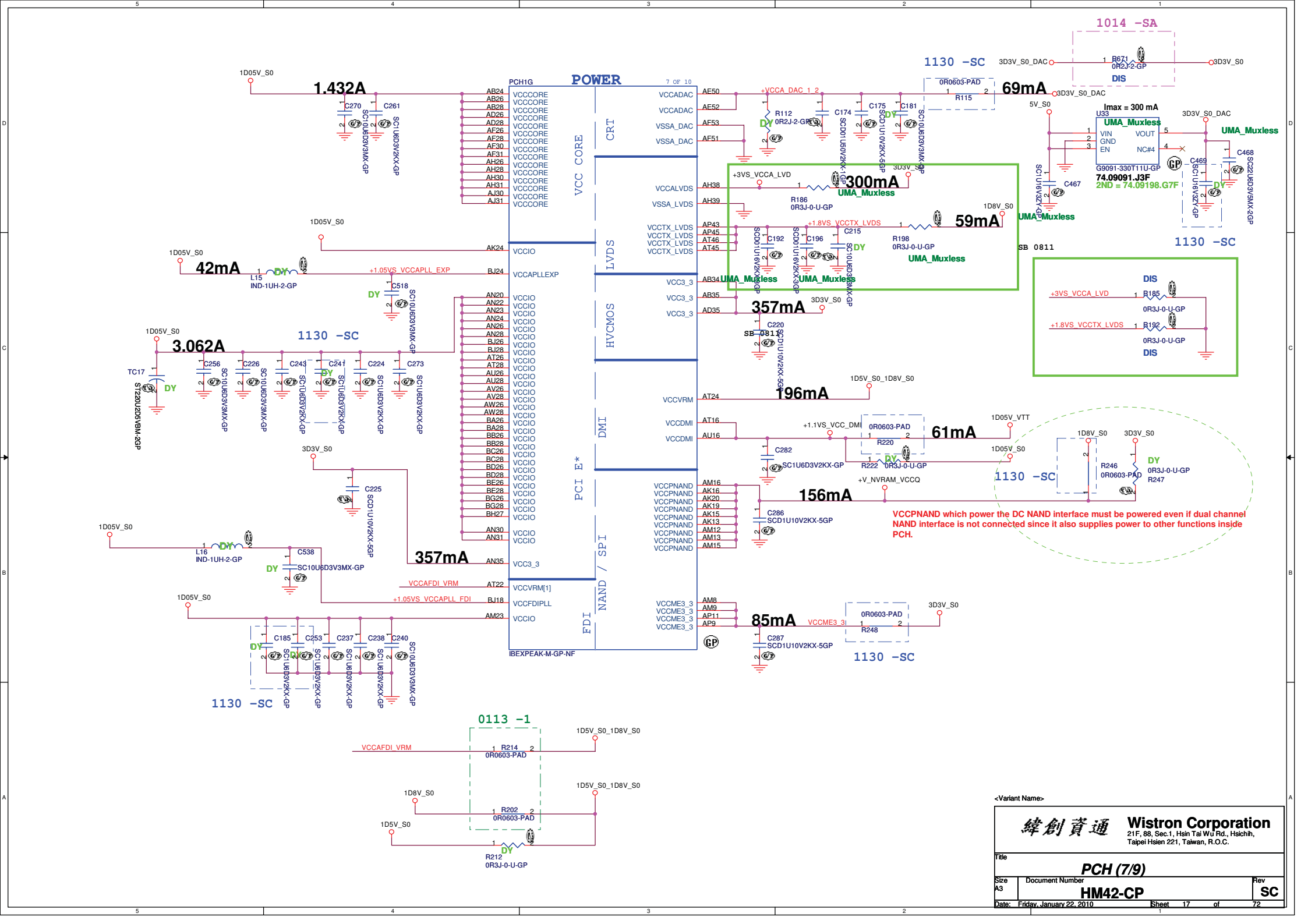
1014 -SA
1130 -SC
POWER
PCH1G
7 OF 10
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
1.432A
3.062A
42mA
357mA
196mA
61mA
156mA
85mA
69mA
300mA
59mA
357mA
UMA_Muxless
DIS
DY
0113 -1
SB 0811
Imax = 300 mA
G9091-330T11U-GP
74.09091.J3F
2ND = 74.09198.G7F
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
IBEXPEAK-M-GP-NF
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (7/9)
Size A3
Document Number HM42-CP
Rev SC
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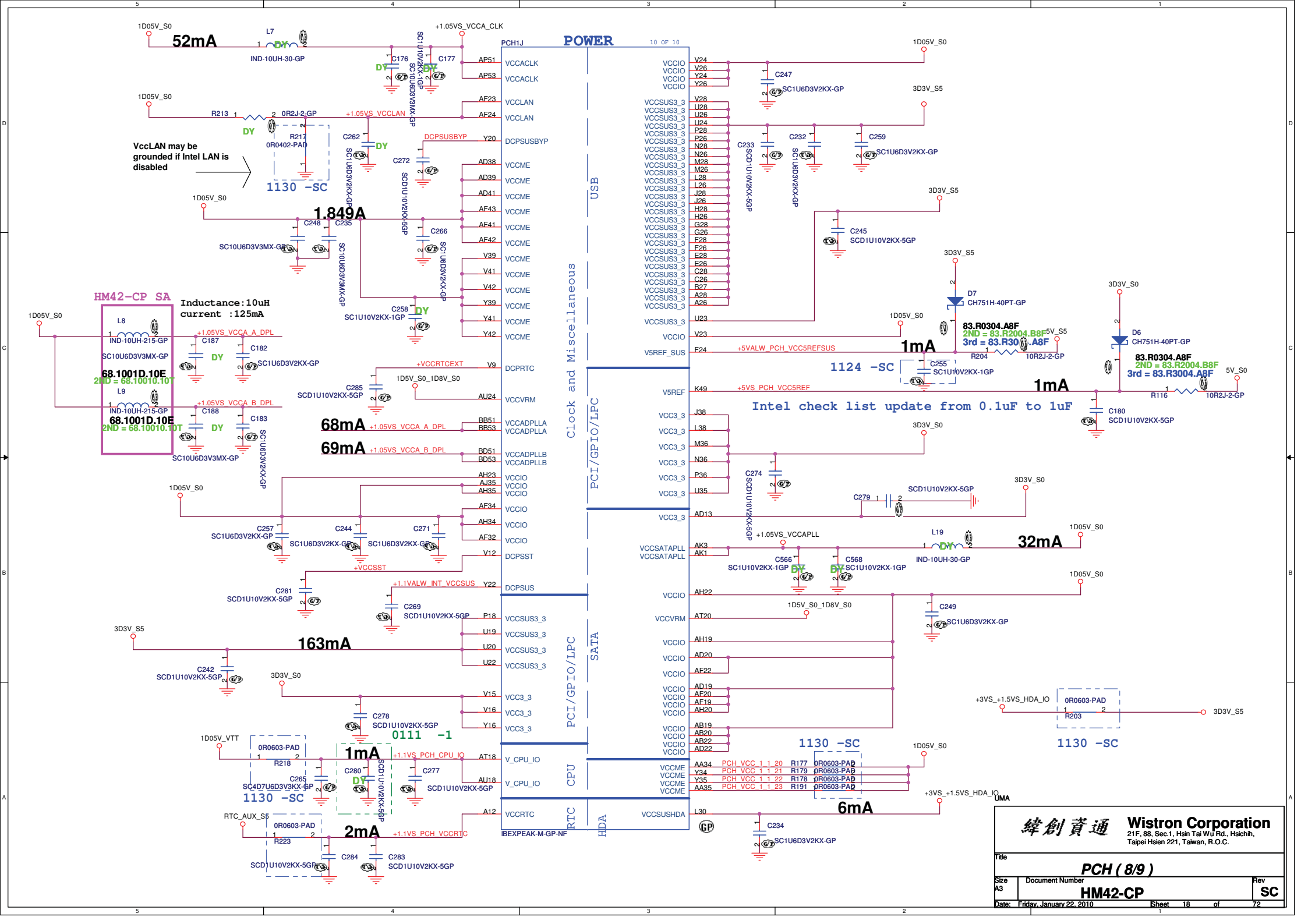
POWER
PCH1J
10 OF 10
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
52mA
1.849A
68mA
69mA
163mA
1mA
2mA
6mA
32mA
HM42-CP SA
Inductance:10uH
current :125mA
68.1001D.10E
2ND = 68.10010.10T
VccLAN may be grounded if Intel LAN is disabled
1130 -SC
1124 -SC
0111 -1
Intel check list update from 0.1uF to 1uF
83.R0304.A8F
2ND = 83.R2004.B8F
3rd = 83.R3004.A8F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
PCH (8/9)
Size A3
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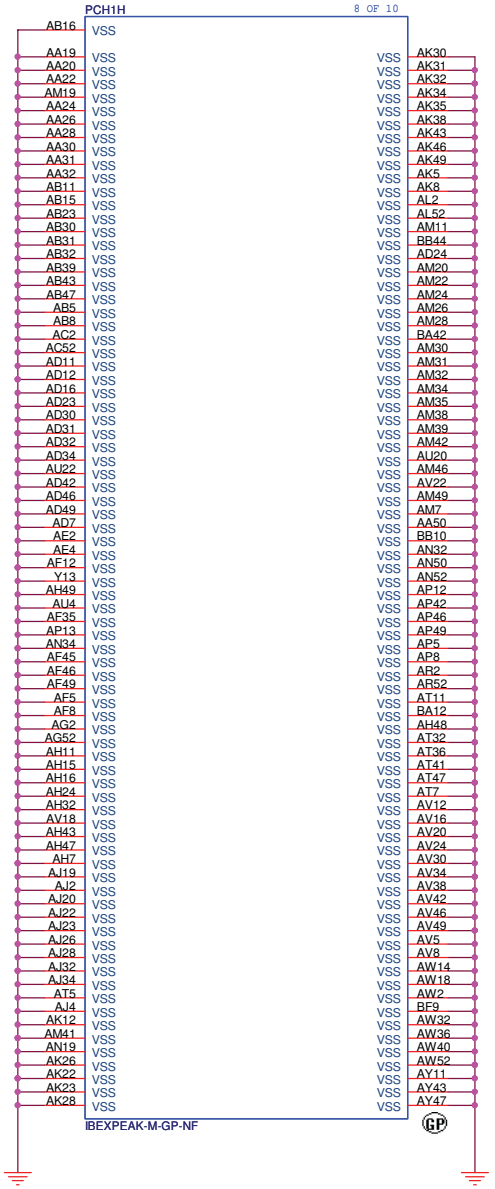

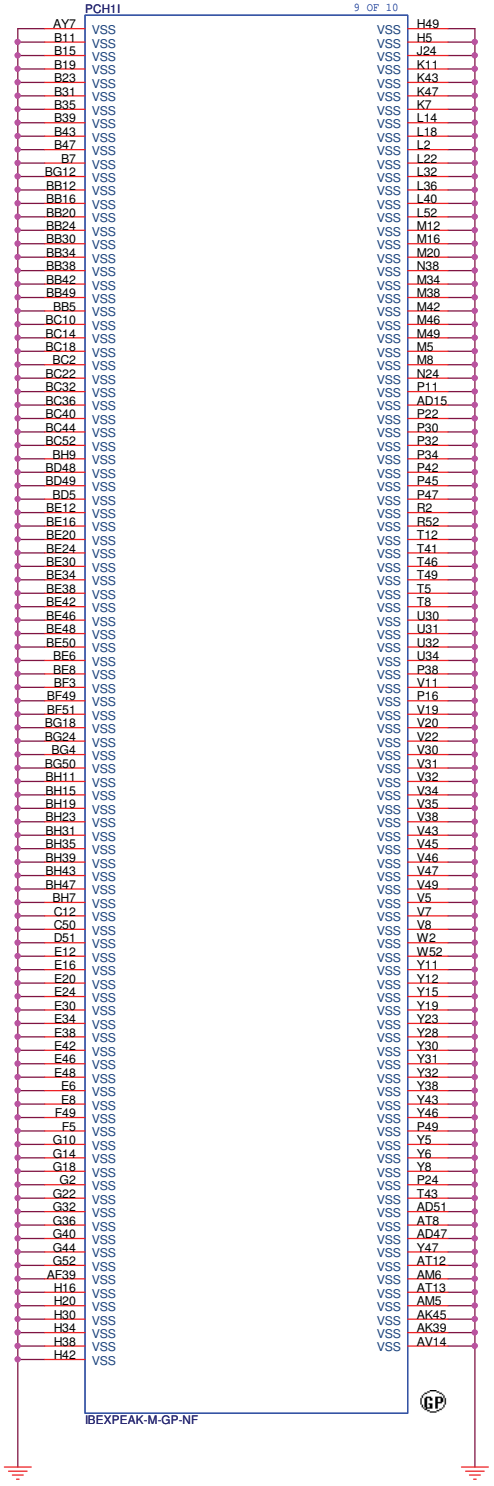

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (9/9)**

Size	Document Number	Rev
A3	HM42-CP	SC

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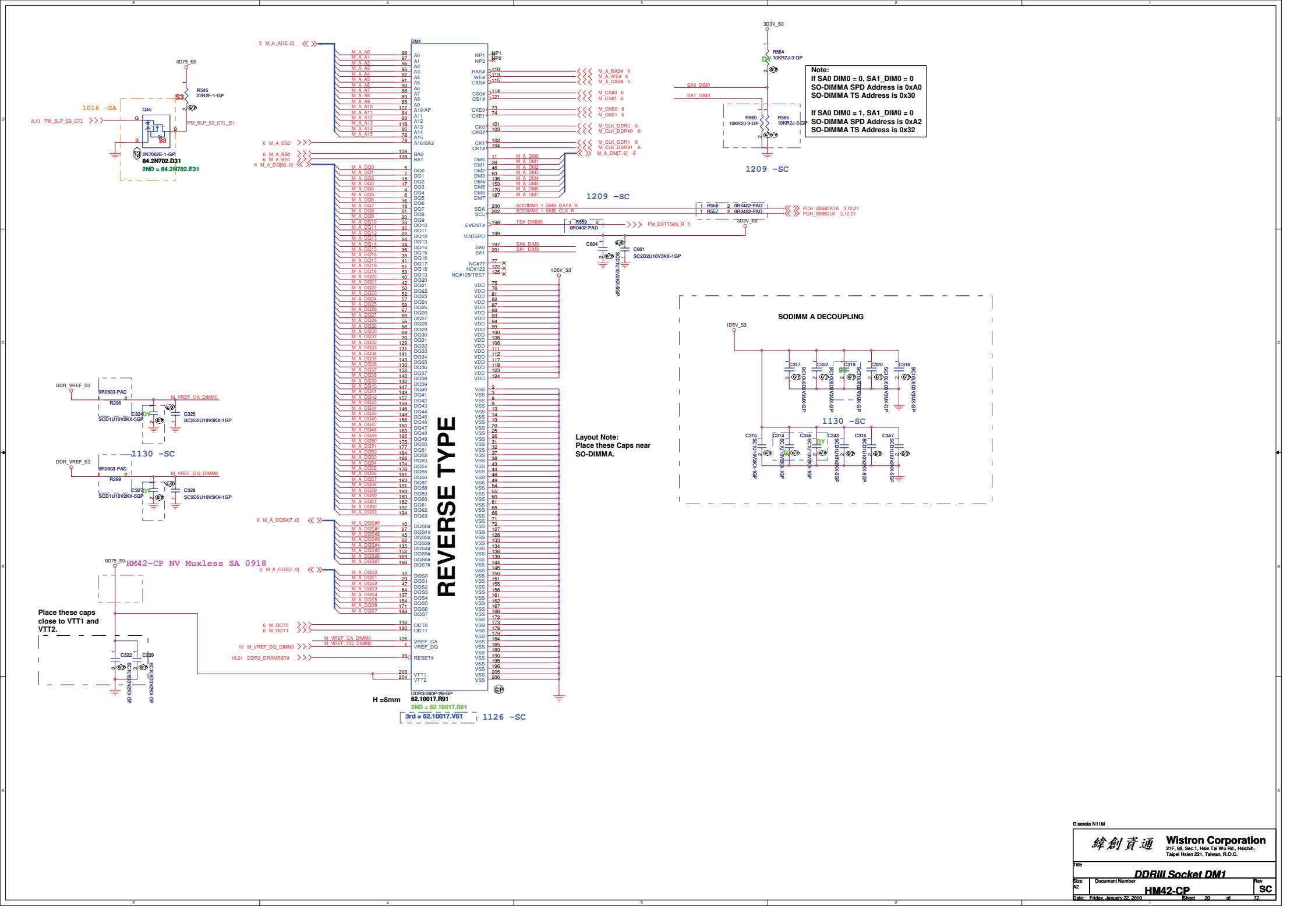
DM1
REVERSE TYPE
DDR3-240P-28-GP
62.10017.R91
2ND = 62.10017.S01
3rd = 62.10017.V61
1126 -SC
H =8mm
1016 -SA
84.2N702.D31
2ND = 84.2N702.E31
1209 -SC
1130 -SC
HM42-CP NV Muxless SA 0918
Place these caps close to VTT1 and VTT2.
Layout Note:
Place these Caps near SO-DIMMA.
SODIMM A DECOUPLING
Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30
If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32
Diserete N11M
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
DDRIII Socket DM1
Size A2
Document Number HM42-CP
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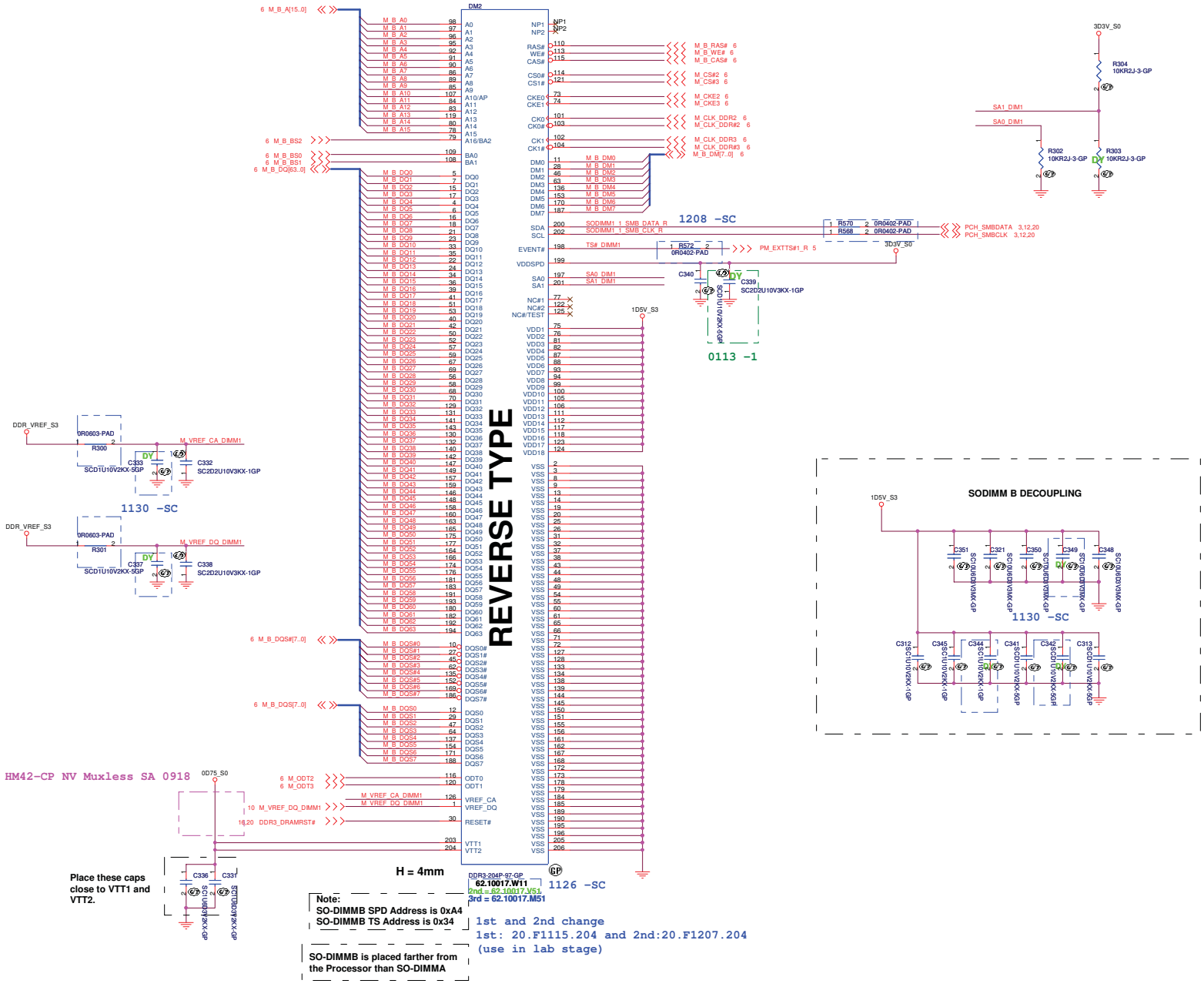

Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDRIII Socket DM2

Size	Document Number	Rev
A2	HM42-CP	SC

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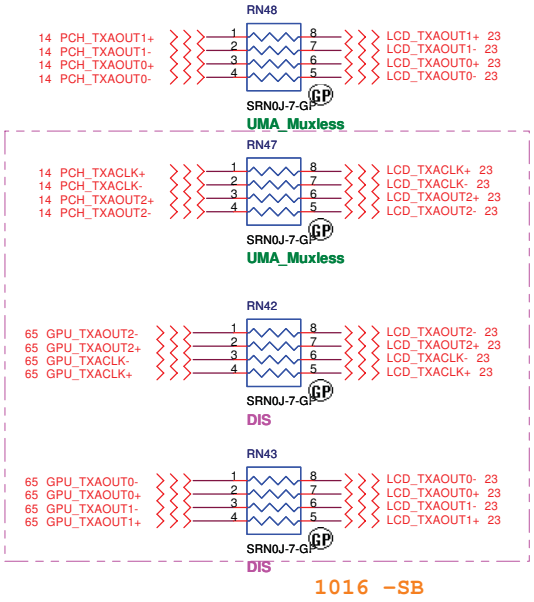
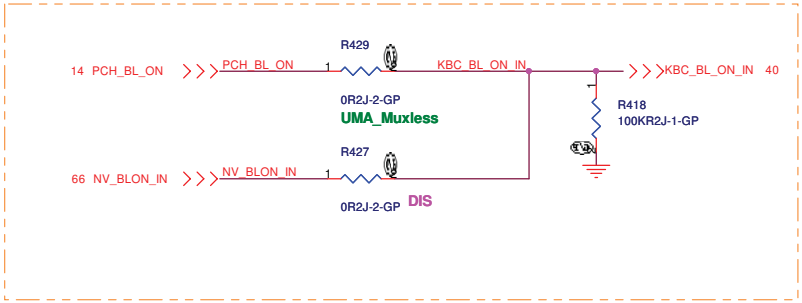
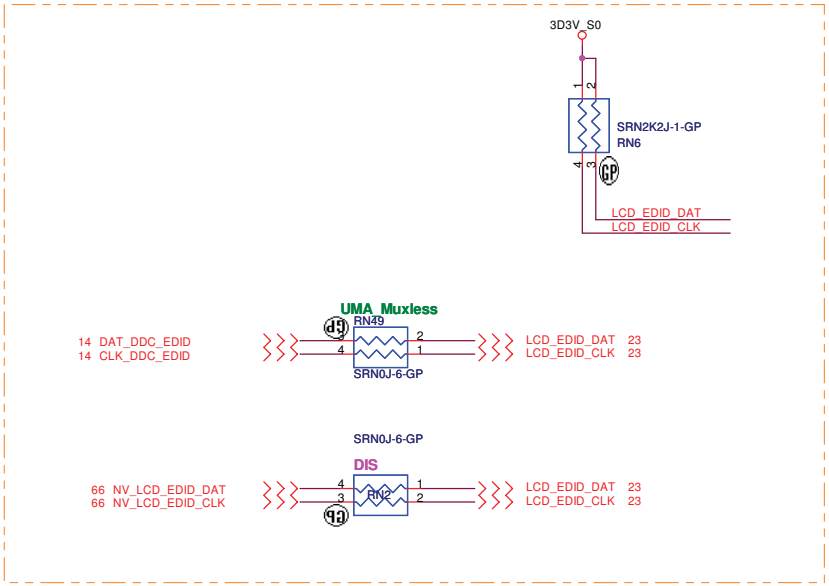
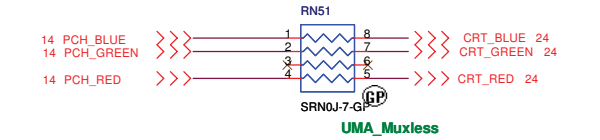


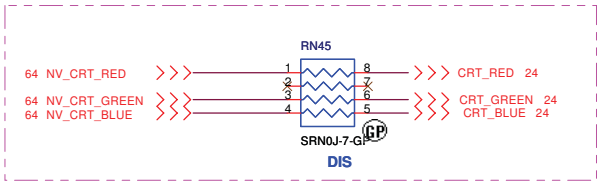
1016 -SB





1016 -SB





UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Function

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A3	HM42-CP	SC

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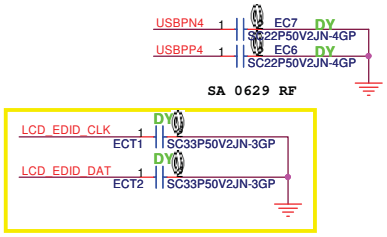
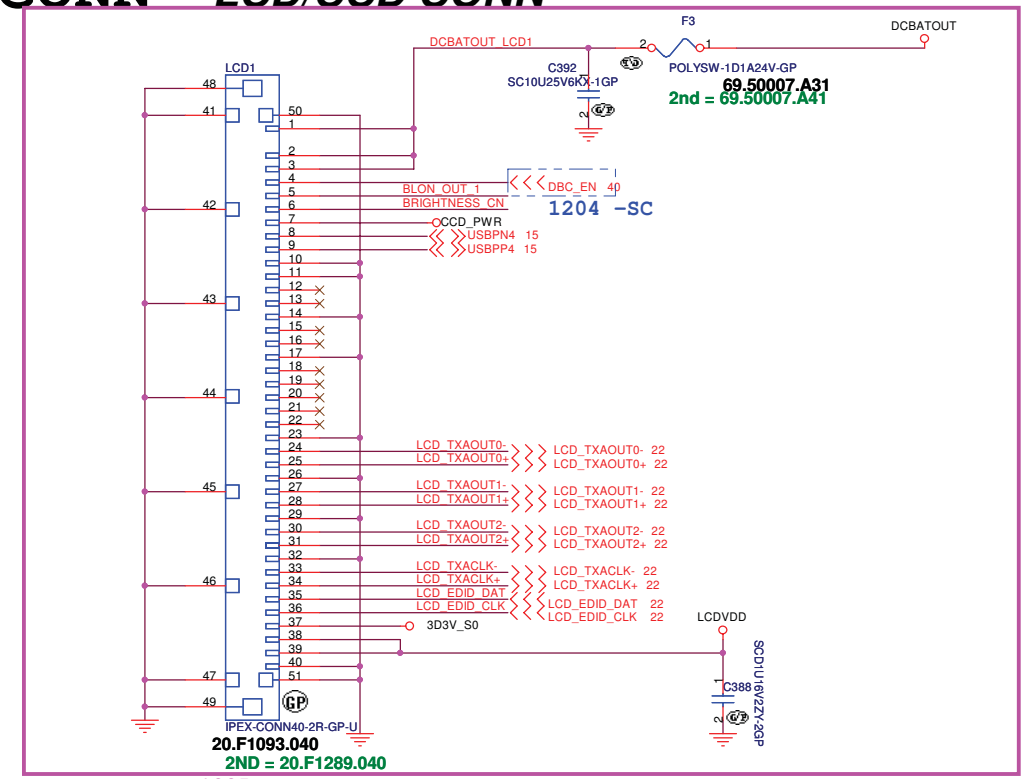
LCD/INVERTER/CCD CONN

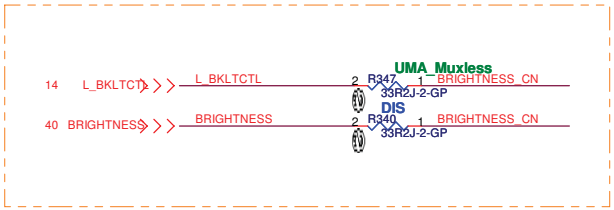
LCD/CCD CONN



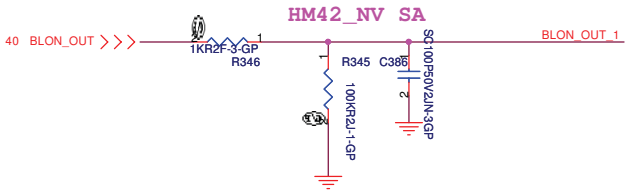


1005 -SA
define same as SJM50-PU,can use SJM50 Cable

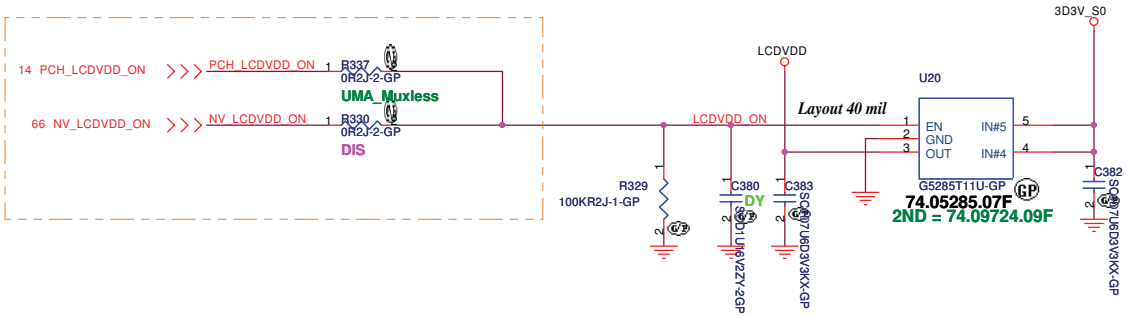
1016 -SB



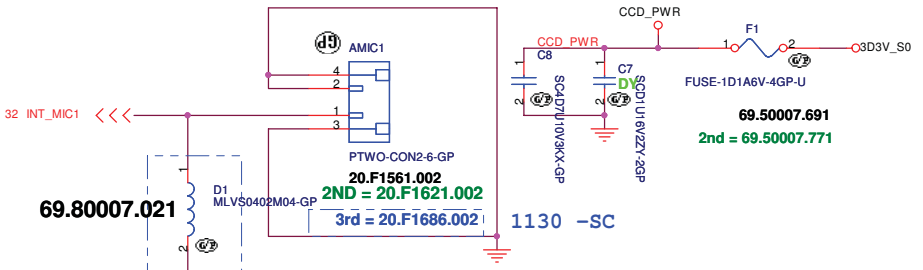
HM42_NV SA



1016 -SB



Internal Mic



1209 -SC
request by EMI Aaron

Pin 1- >right side
20.F1240.002 Pin1->left side
same as JV70-CP

Diserete N11M

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Title	LCD CONN	
Size	Document Number HM42-CP	Rev SC
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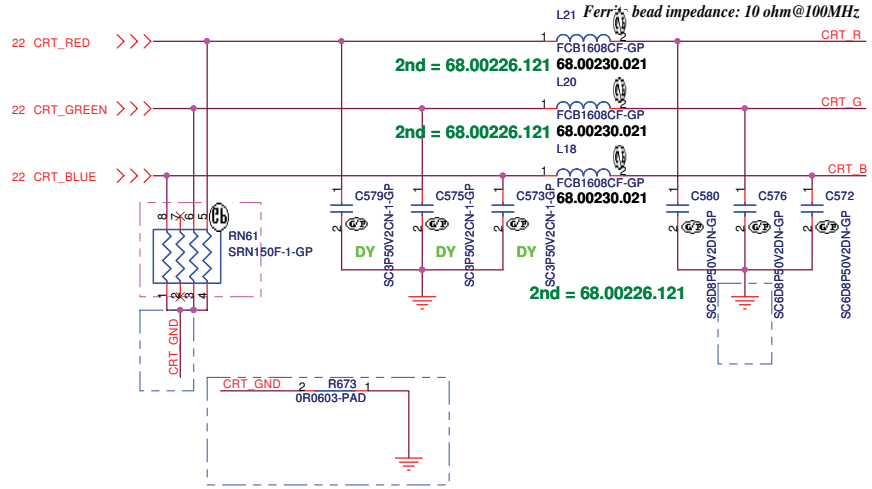
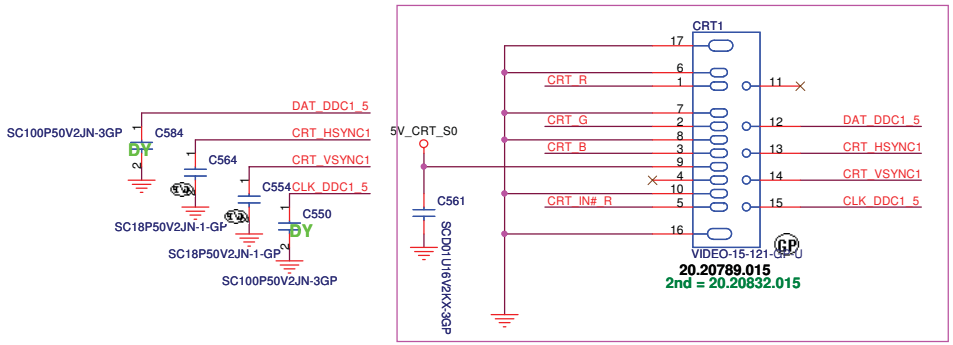
Layout Note:
Place these resistors close to the CRT-out connector

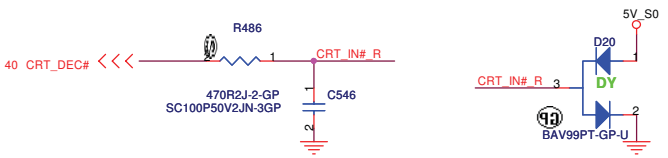


Layout Note:
** Must be a ground return path between this ground and the ground on the VGA connector.*
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR

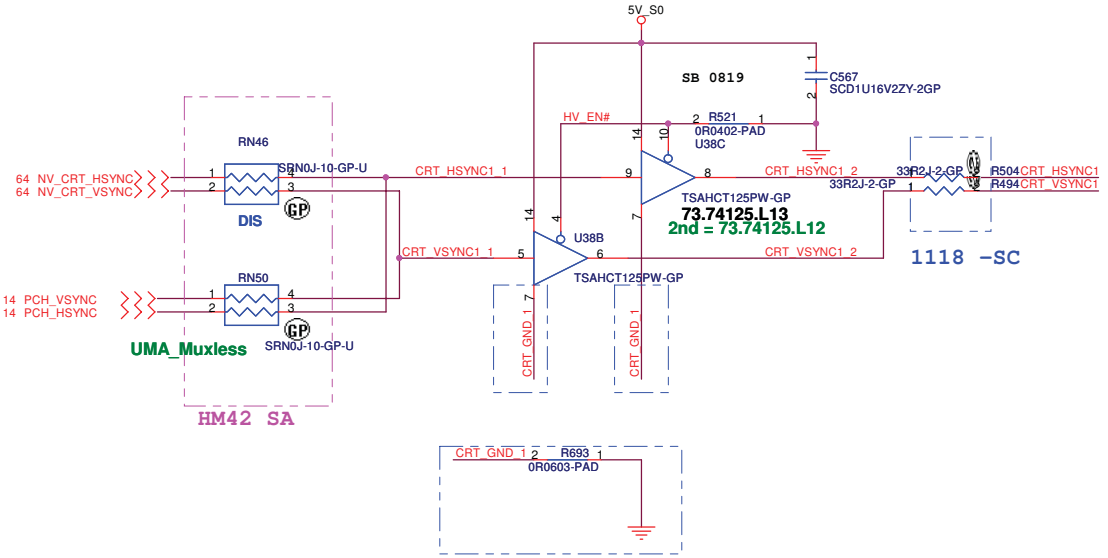


HM42 CP NV Muxless

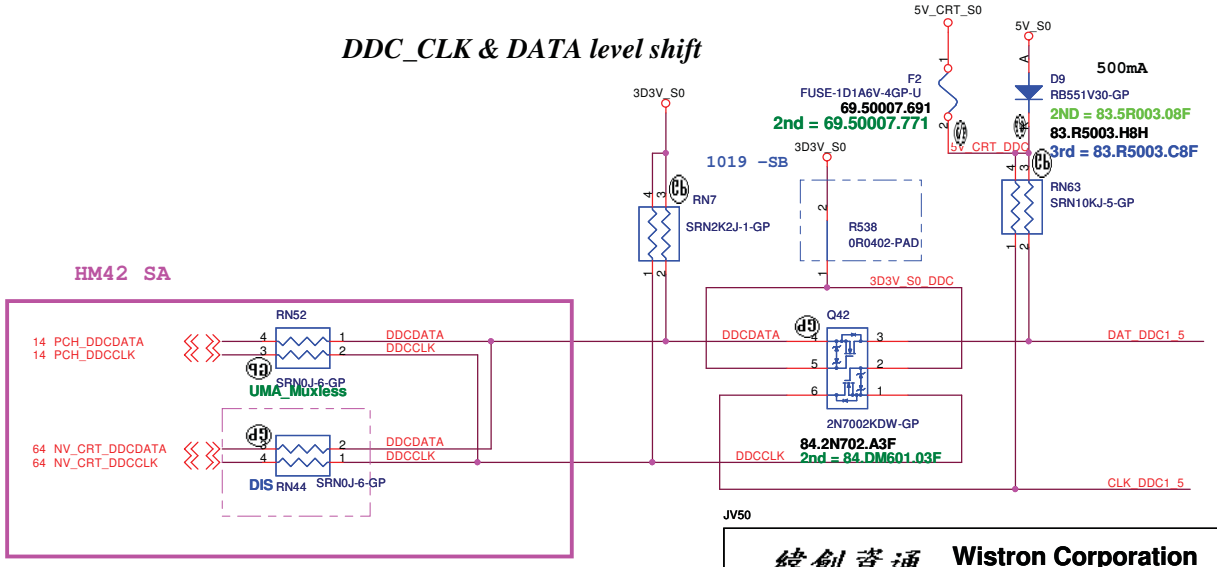


6 1 7 2 8 3 9 4 10 5

Hsync & Vsync level shift



DDC_CLK & DATA level shift



JV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **CRT CONN**		
Size	Document Number: **HM42-CP**	Rev: SC
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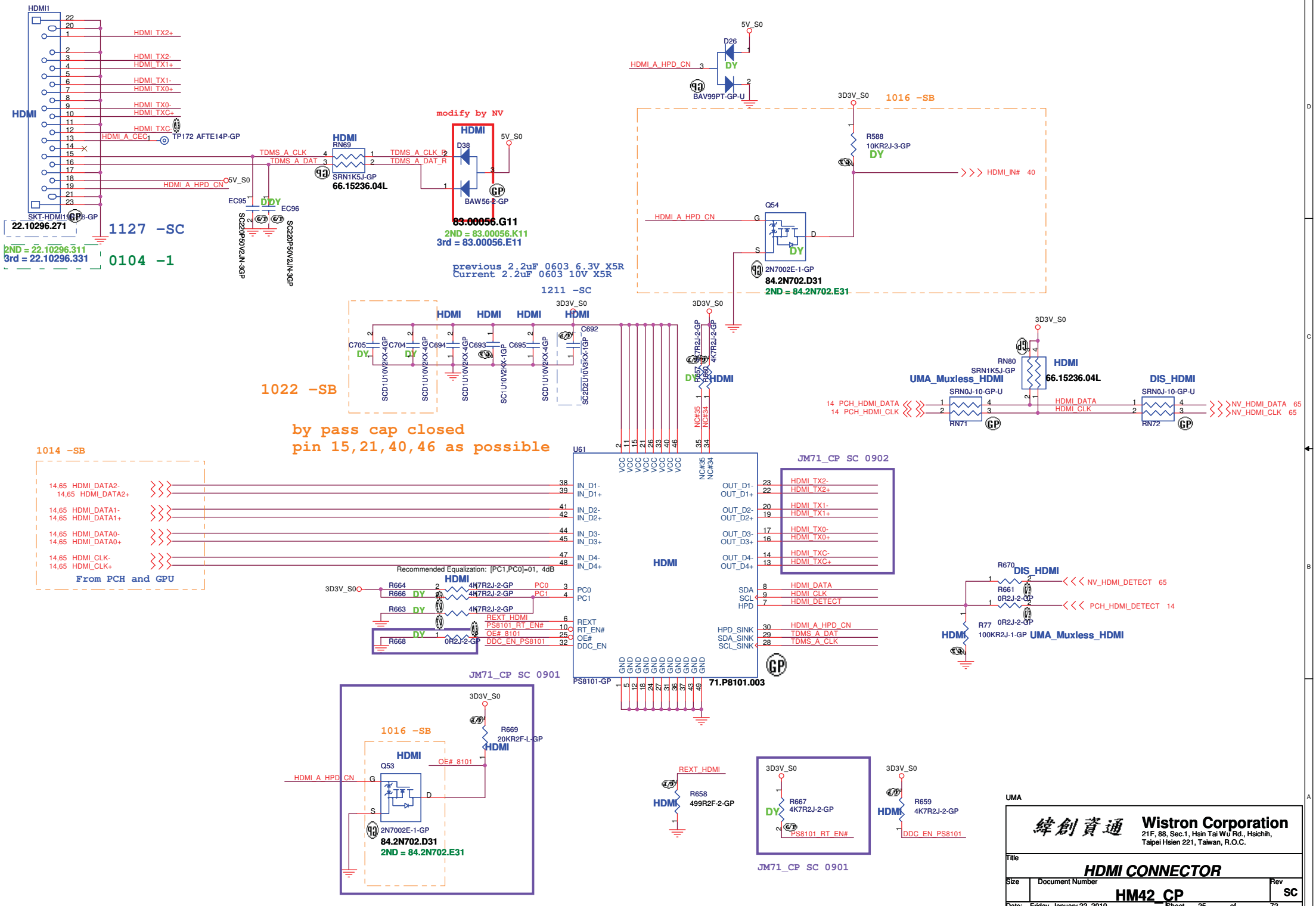
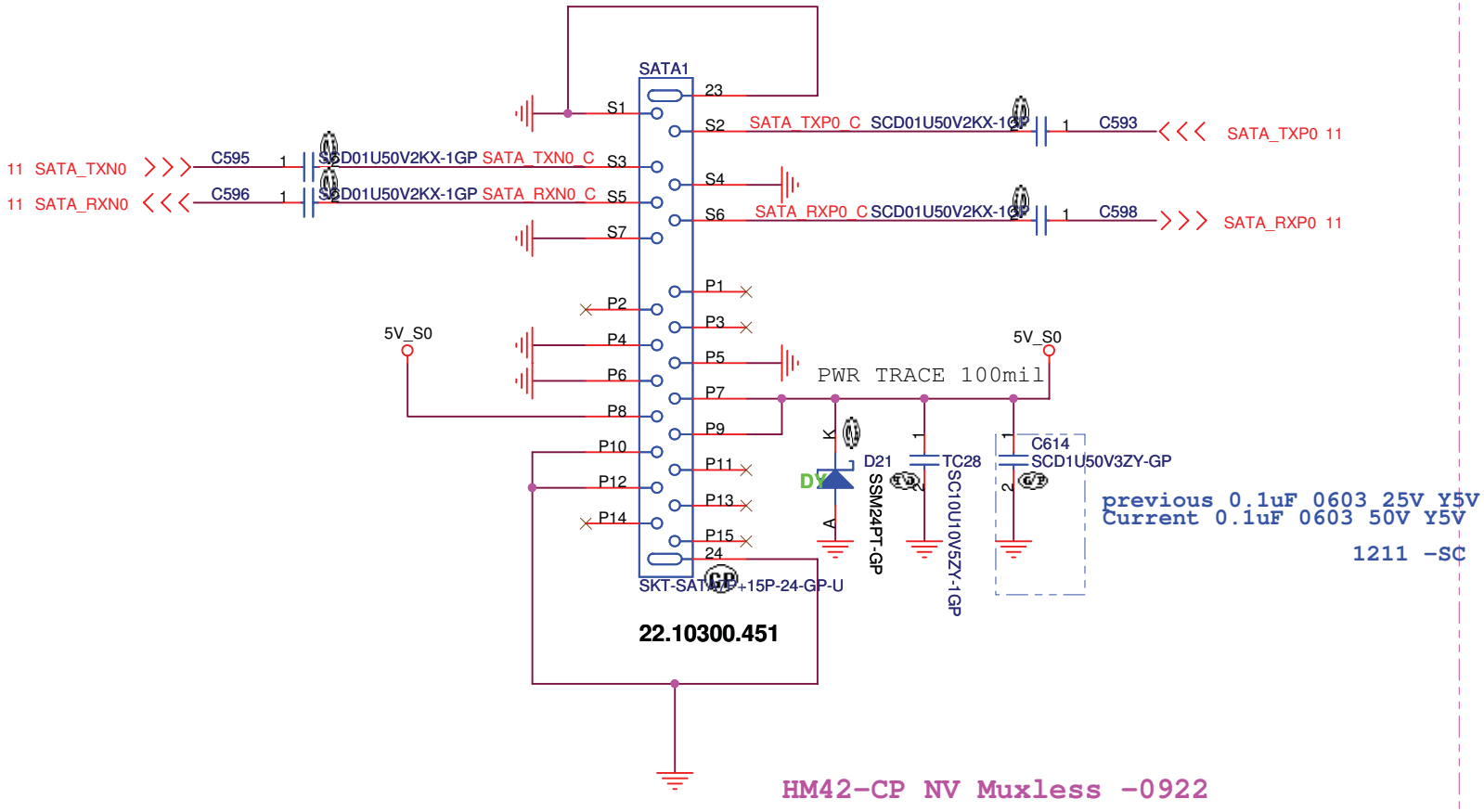


緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***HDMI CONNECTOR***
Size	Document Number: **HM42_CP** Rev: **SC**
Date: Friday, January 22, 2010	Sheet 25 of 72

SATA Connector



UMA

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HDD CONN***	
Size	Document Number **HM42-CP**	Rev SC
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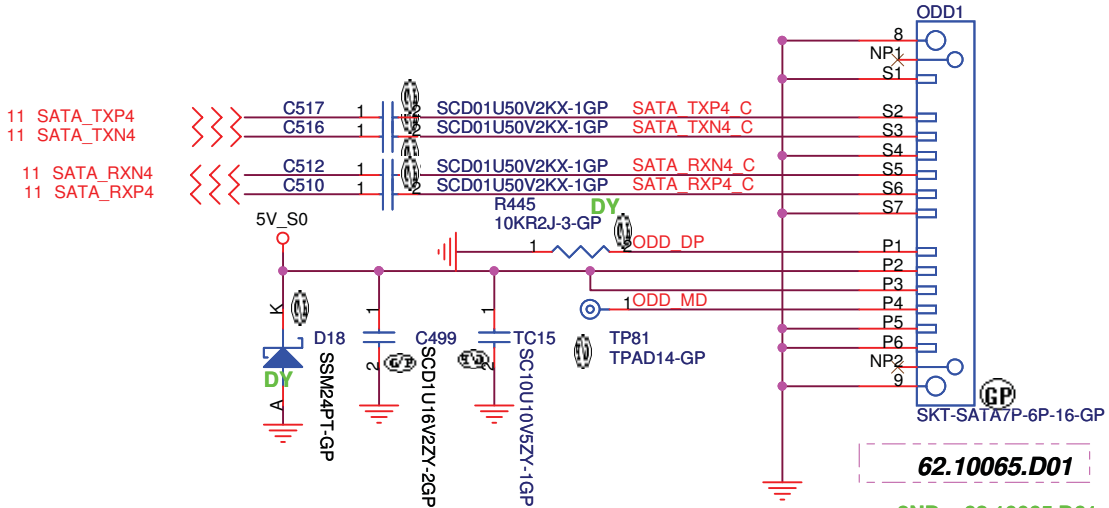
ODD Connector



62.10065.D01 1006 -SA

2ND = 62.10065.D61

1230 -1 3rd = 62.10065.E01

S1~S7,P1~P6 same as 62.10065.631

UMA

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Title: ODD		
Size	Document Number: HM42-CP	Rev: SC
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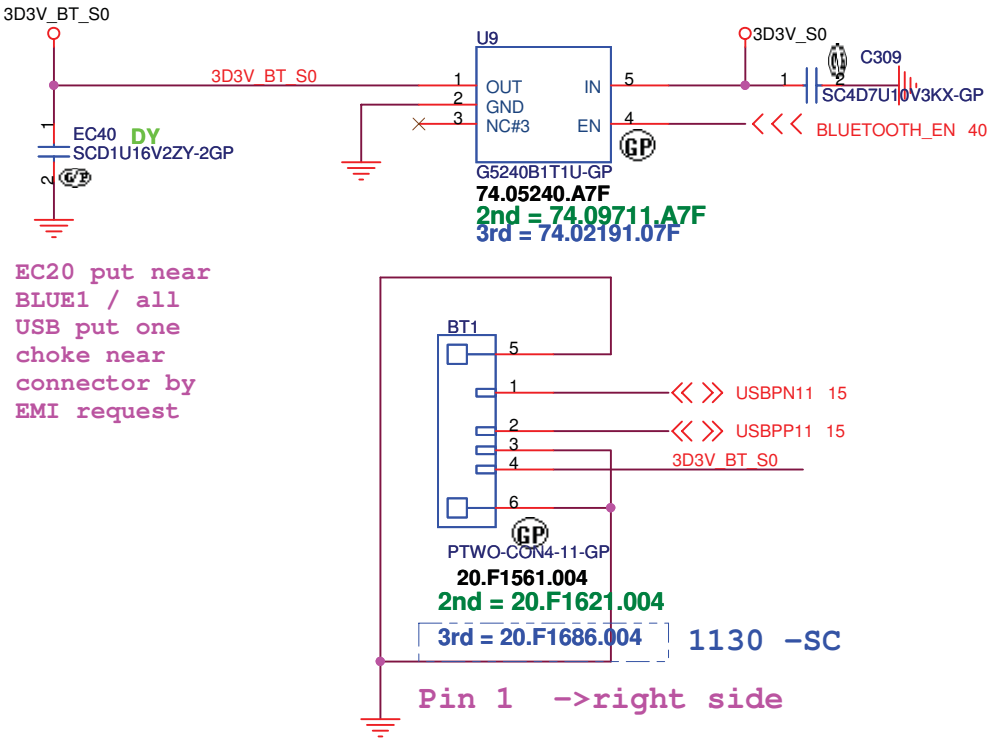
BLUETOOTH MODULE



JV50

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Title: BLUETOOTH		
Size	Document Number: HM42-CP	Rev: SC
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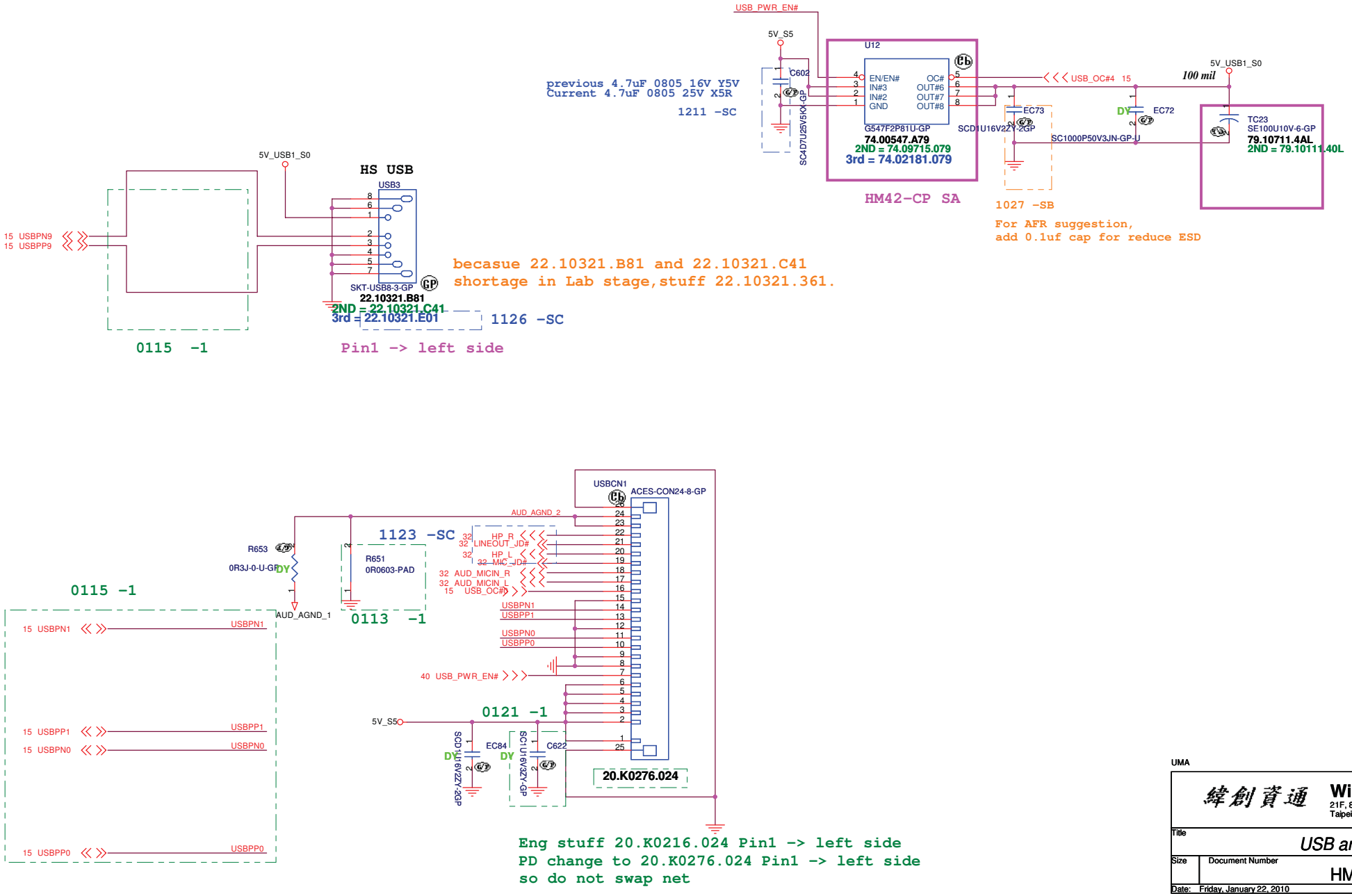
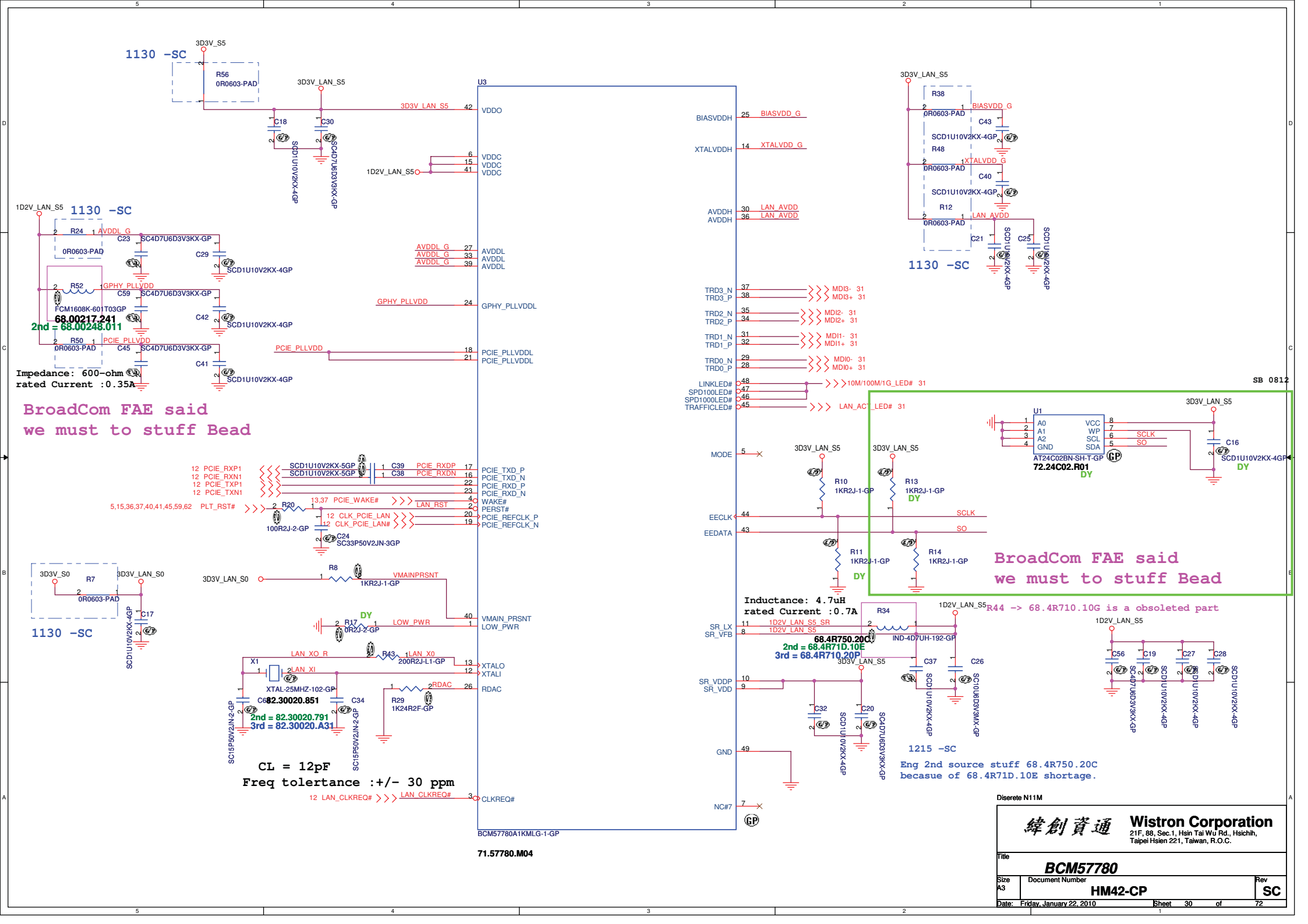


UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *USB and Audio CONN*		
Size	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 29 of 72	



Diserete N11M

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	***BCM57780***	
Size A3	Document Number **HM42-CP**	Rev **SC**
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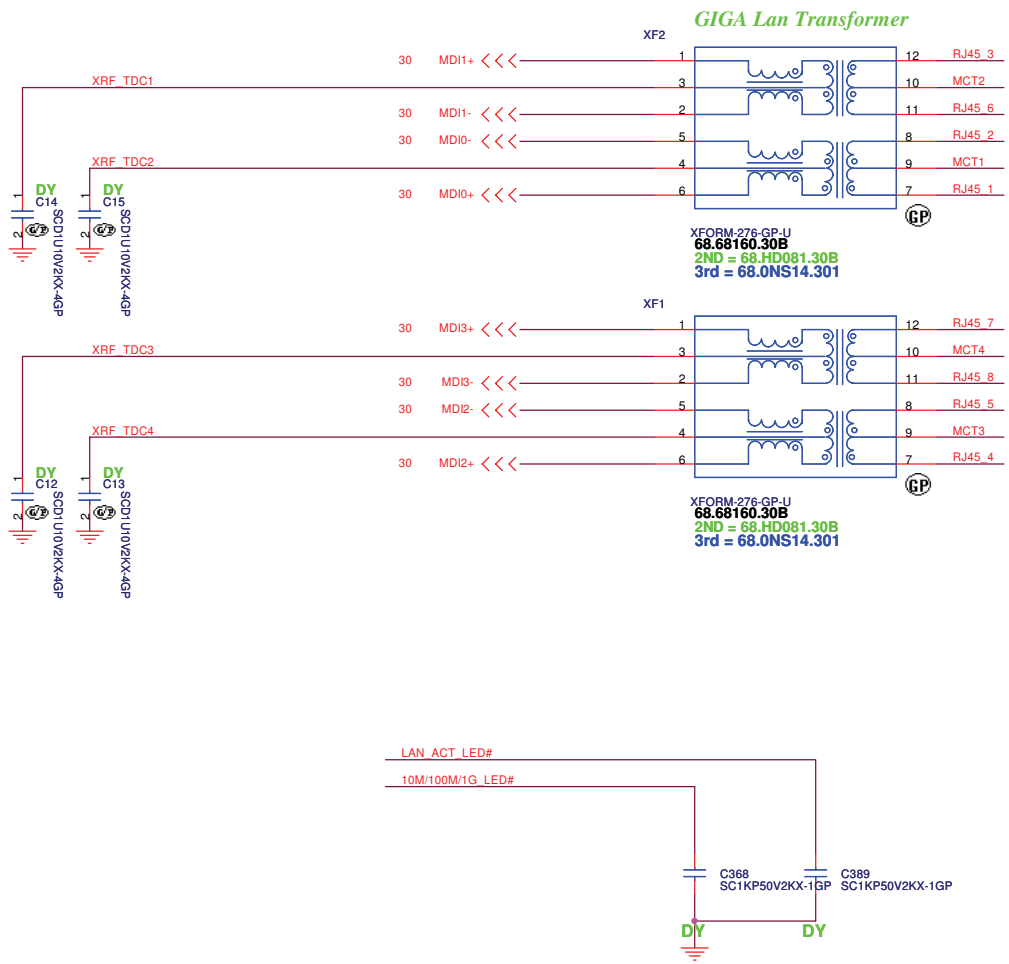
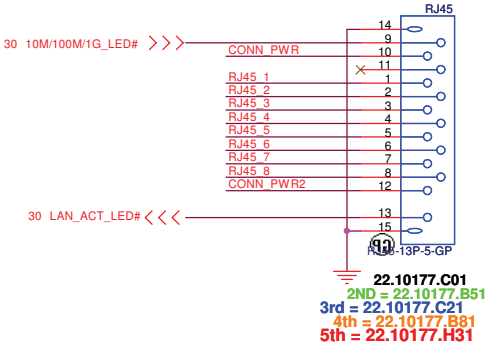
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

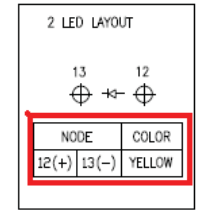
LAN Connector

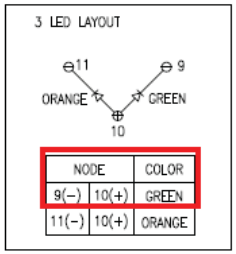
LAN Connector

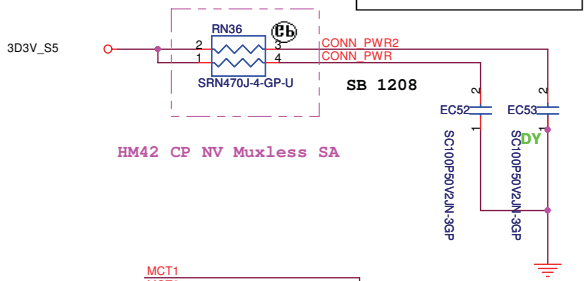
GIGA Lan Transformer

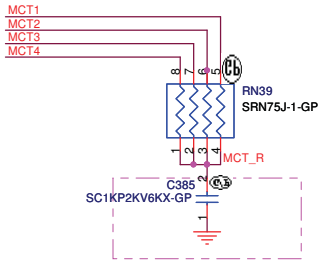








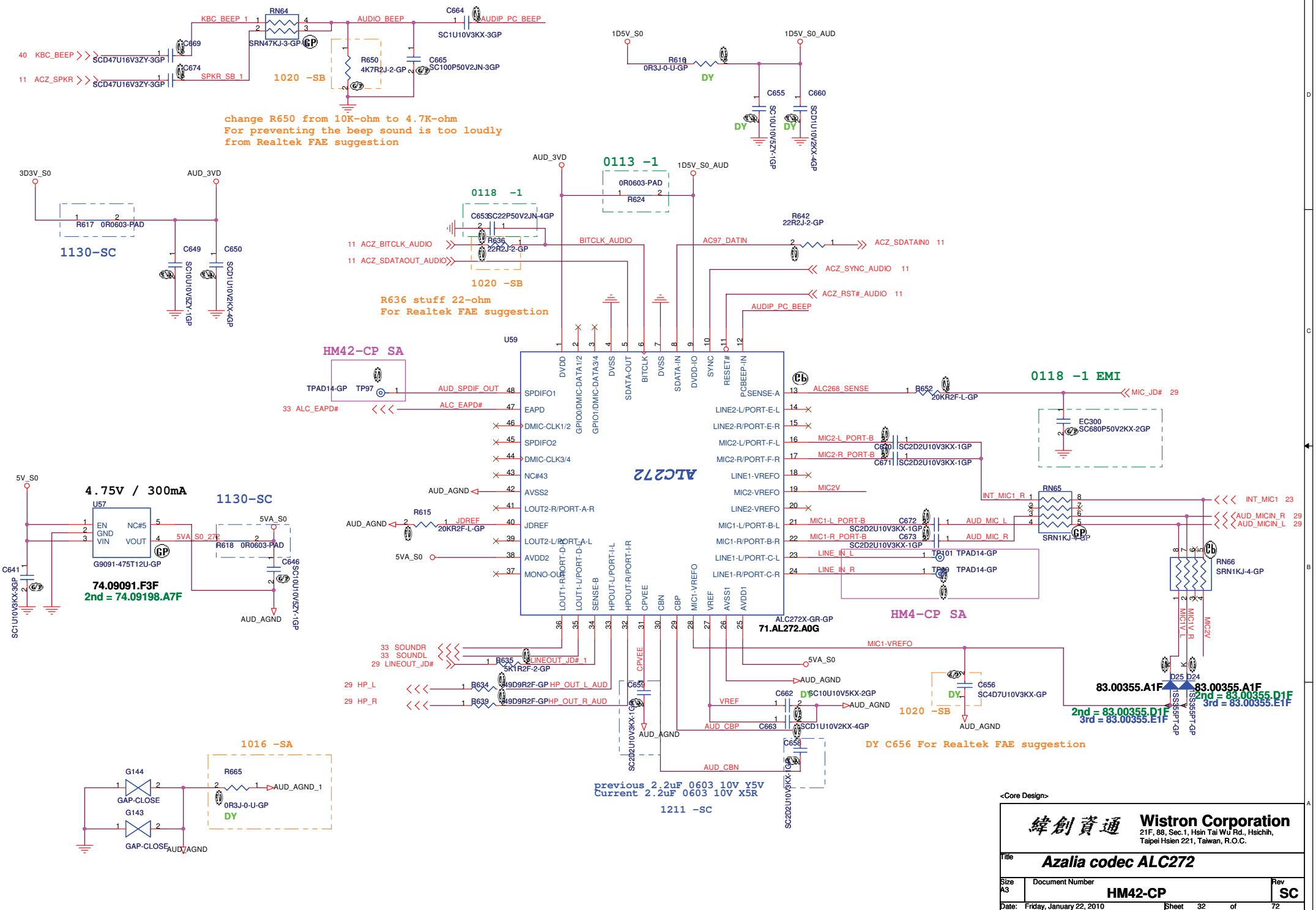




UMA

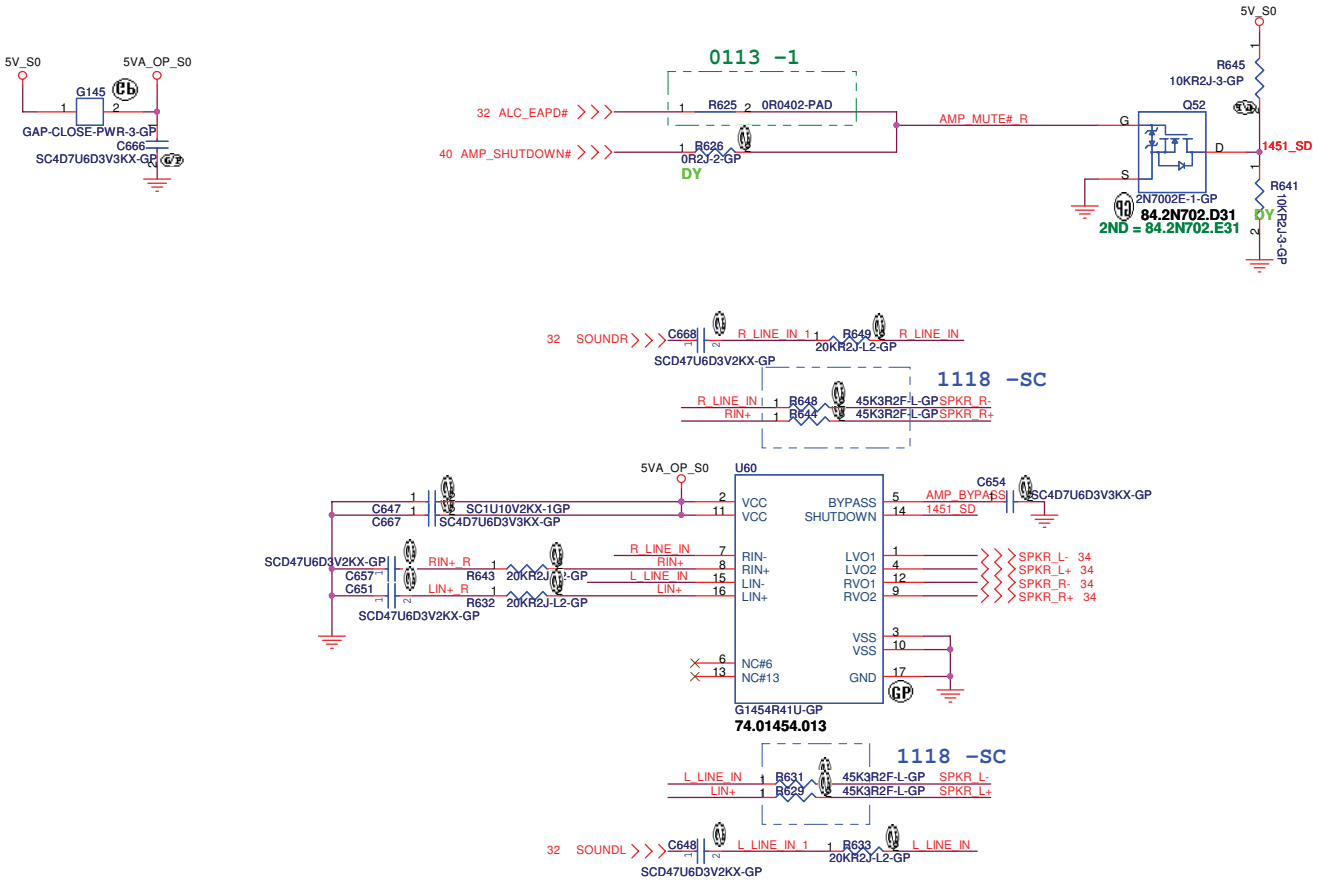
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN		
Size: A3	Document Number: HM42-CP	Rev: SC
Date: Friday, January 22, 2010	Sheet 31 of 72	



<Core Design>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **Azalia codec ALC272**		
Size: A3	Document Number: **HM42-CP**	Rev: **SC**
Date: Friday, January 22, 2010	Sheet 32 of 72	



Gain= Rf/Ri=52K/20K=2.6V/V
f(HP)=1/(2 Pi*20K*0.47uf)=16.9Hz
If VIN= 1.54V Gain=2.6V/V RL=4Ω VO(peak) = 4V V(rms)=2.828V
Power= 2.446^2/4=1.5W

UMA

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Title: *AUDIO AMP*

Size	Document Number	Rev
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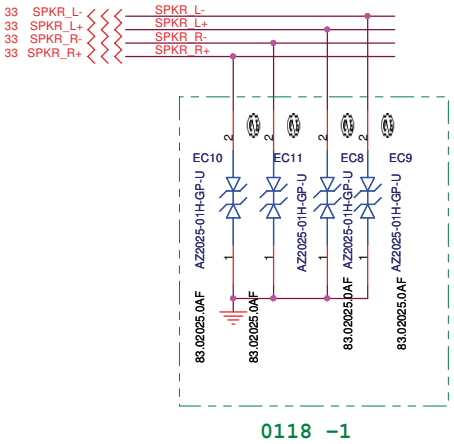
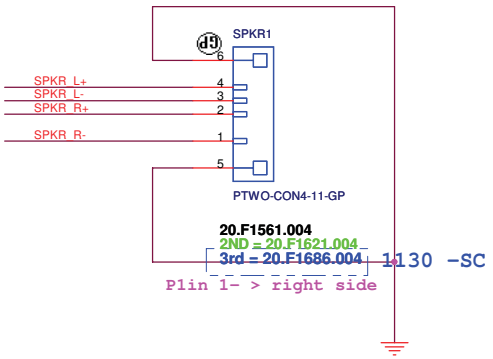
Internal Speaker





Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *AUDIO SPEARK*		
Size	Document Number: HM42-CP	Rev: SC
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JV50

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
Resrve_MDC

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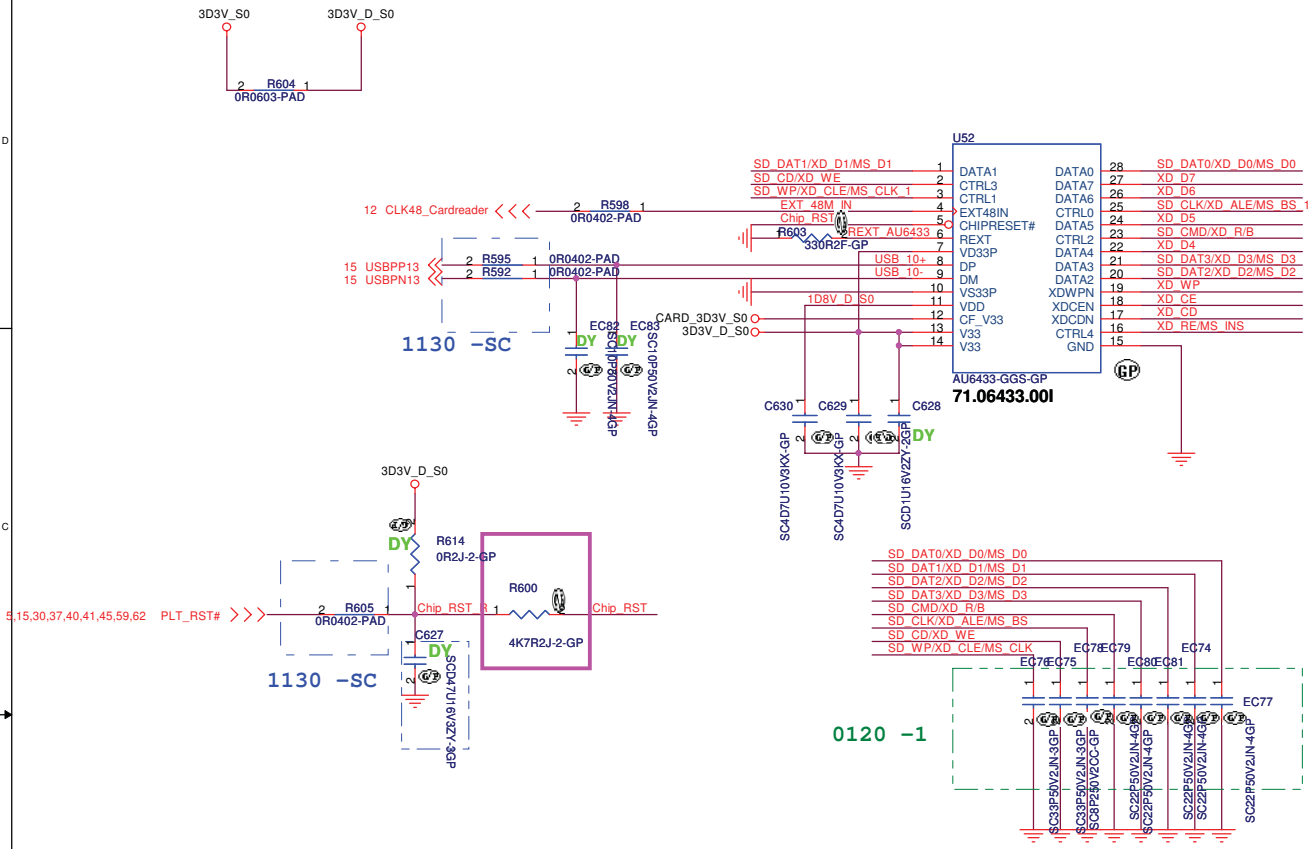
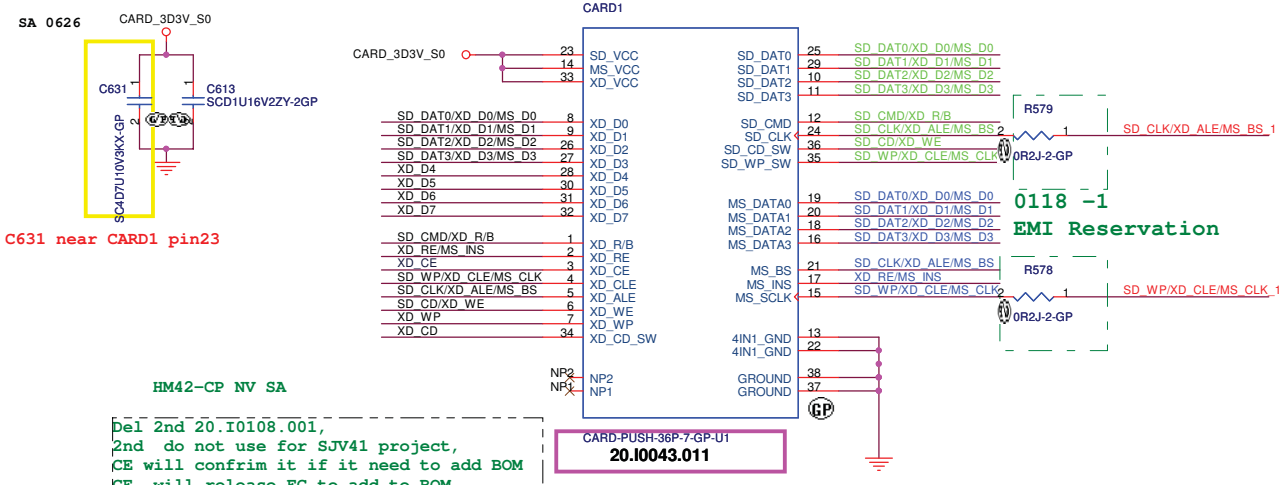


Pin	SD Mode	
	Name	Description
1	CD/DAT3	Card detect/Data line[Bit 3]
2	CMD	Command/Response
3	VSS1	Supply voltage ground
4	VDD	Supply voltage
5	CLK	Clock
6	VSS2	Supply voltage ground
7	DAT0	Data line[Bit 0]
8	DAT1	Data line[Bit 1]
9	DAT2	Data line[Bit 2]

Pin No.	SD/MMC	MS/MS PRO	xD
P1 xD-R/B			2P
P2 xD-RE			3P
P3 xD-CE			4P
P4 xD-CLE			5P
P5 xD-ALE			6P
P6 xD-WE			7P
P7 xD-WP			8P
P8 xD-D0			10P
P9 xD-D1			11P
P10 SD-DAT2	9P		
P11 SD-DAT3	1P		
P12 SD-CMD	2P		
P13 4in1-GND	3P/6P	1P/10P	1P/9P
P14 MS-VCC		9P	
P15 MS-SCLK		8P	
P16 MS-DATA3		7P	
P17 MS-INS		6P	
P18 MS-DATA2		5P	
P19 MS-DATA0		4P	

Pin No.	SD/MMC	MS/MS PRO	xD
P20 MS-DATA1		3P	
P21 MS-BS		2P	
P22 4in1-GND	3P/6P	1P/10P	1P/9P
P23 SD-VCC	4P		
P24 SD-CLK	5P		
P25 SD-DAT0	7P		
P26 xD-D2			12P
P27 xD-D3			13P
P28 xD-D4			14P
P29 SD-DAT1	8P		
P30 xD-D5			15P
P31 xD-D6			16P
P32 xD-D7			17P
P33 xD-VCC			18P
P34 XD-CD-SW			19P
P35 SD-WP-SW	SD-WP-SW		
P36 SD-CD-SW	SD-CD-SW		
P37 P38	4 IN 1-GND	SD-WP/CD-SW-GND	

5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



Pin	Name	Dir	description
1	XD_CD#	-	presence detect
2	R/B#	OUT	Ready / Busy (open-drain)
3	RE#	IN	Read Enable
4	CE#	IN	Card Enable
5	CLE	IN	Command Latch Enable
6	ALE#	IN	Address Latch Enable
7	WE#	IN	Write Enable
8	WP#	IN	Write Protect
9	GND	-	Ground
10	SD0	IN/OUT	data bit 0
11	SD1	IN/OUT	data bit 1
12	SD2	IN/OUT	data bit 2
13	SD3	IN/OUT	data bit 3
14	SD4	IN/OUT	data bit 4
15	SD5	IN/OUT	data bit 5
16	SD6	IN/OUT	data bit 6
17	SD7	IN/OUT	data bit 7
18	VCC	-	3.3V power

Pin	Pin Name	Description
1	VSS	Vss
2	BS	Bus state signal
3	DATA1	Data1 Parallel / NC Serial
4	SDIO/DATA0	Data0 Parallel / Data Serial
5	DATA2	Data2 Parallel / NC Serial
6	INS	Stick detect (connected to VSS)
7	DATA3	Data3 Parallel / NC Serial
8	SCLK	Clock signal
9	VCC	Vcc (2,7V - 3,6V)
10	VSS	Vss

UMA

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Title: Cardreader
Size | Document Number: HM42-CP | Rev: SC
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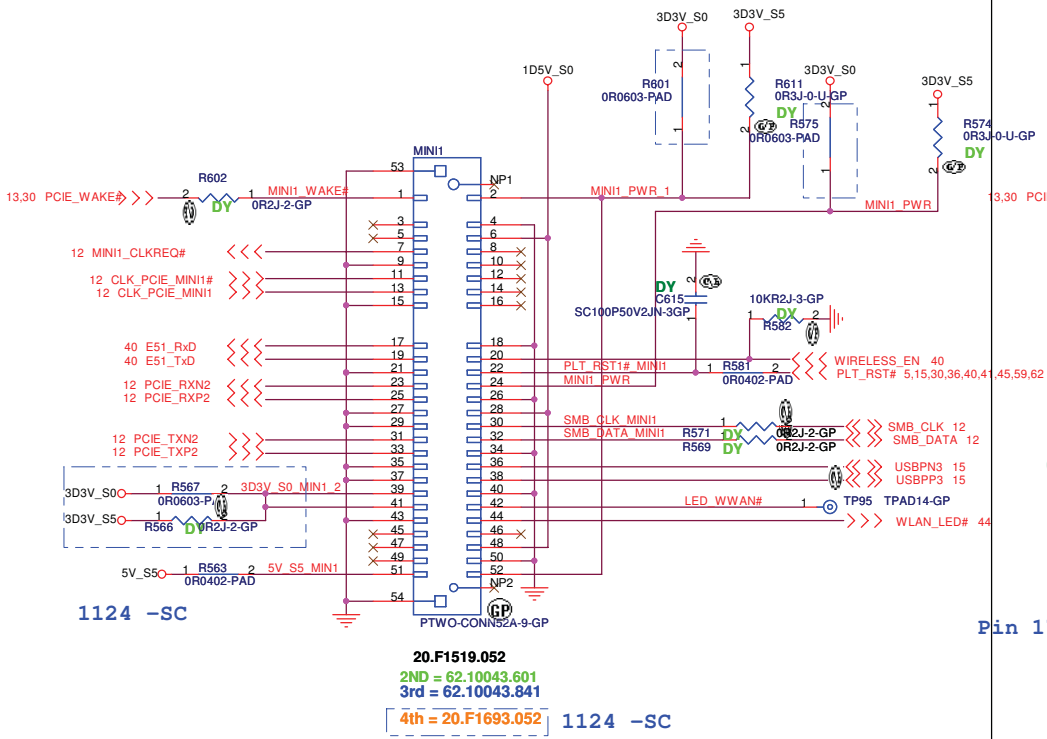
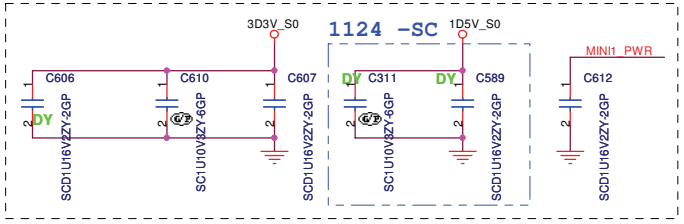
Mini Card Connector(WLAN)
Support debug-card

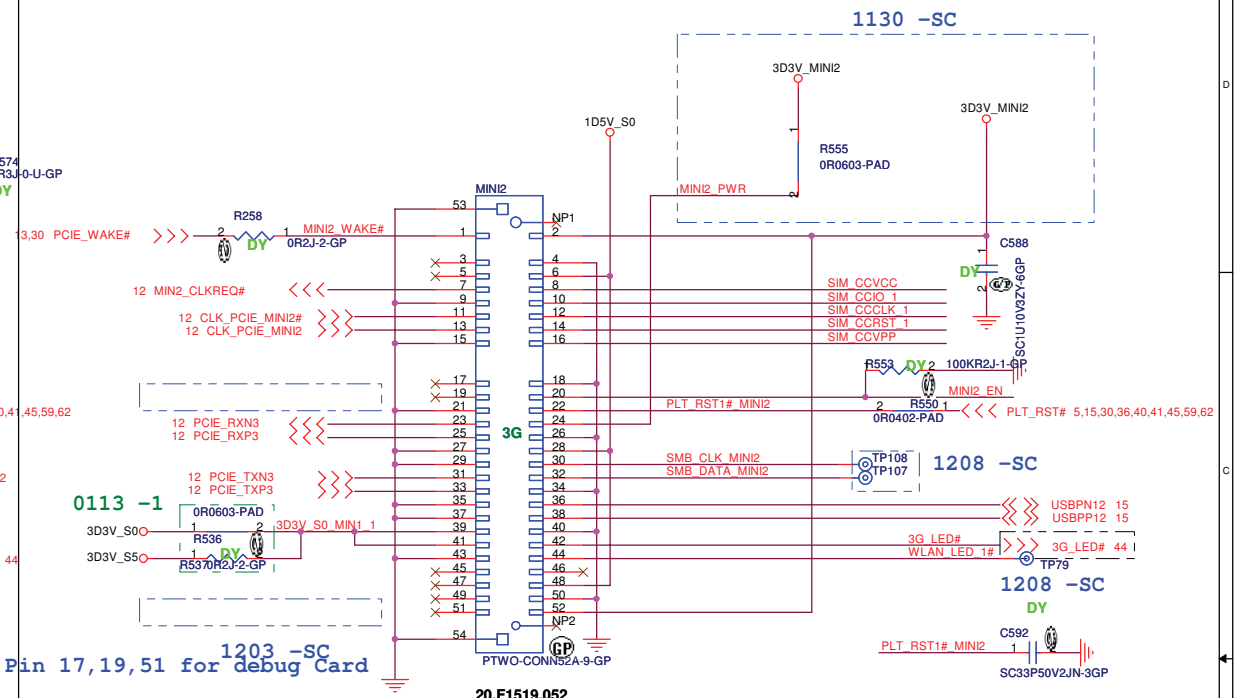


20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC

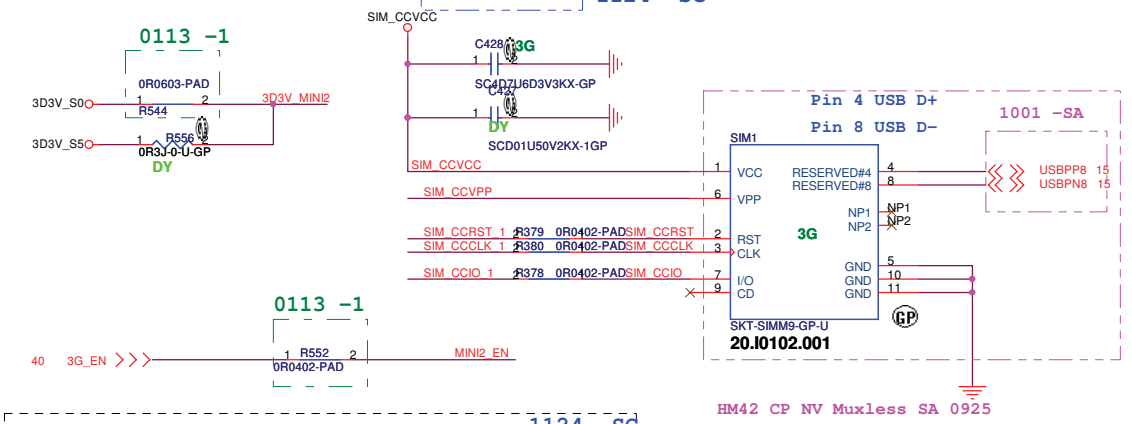
Place near MINI1



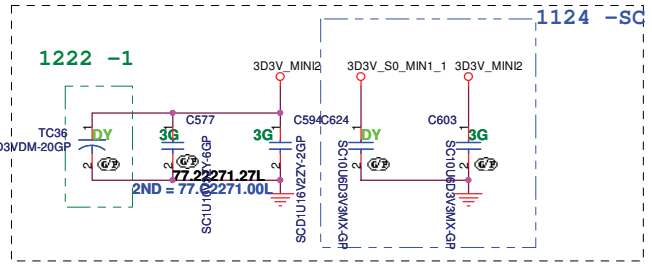
Mini Card Connector(Robson2 and 3G)



20.F1519.052
2ND = 62.10043.601
3rd = 62.10043.841
4th = 20.F1693.052 1124 -SC



HM42 CP NV Muxless SA 0925



Diserete N11M

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD**

Size	Document Number	Rev
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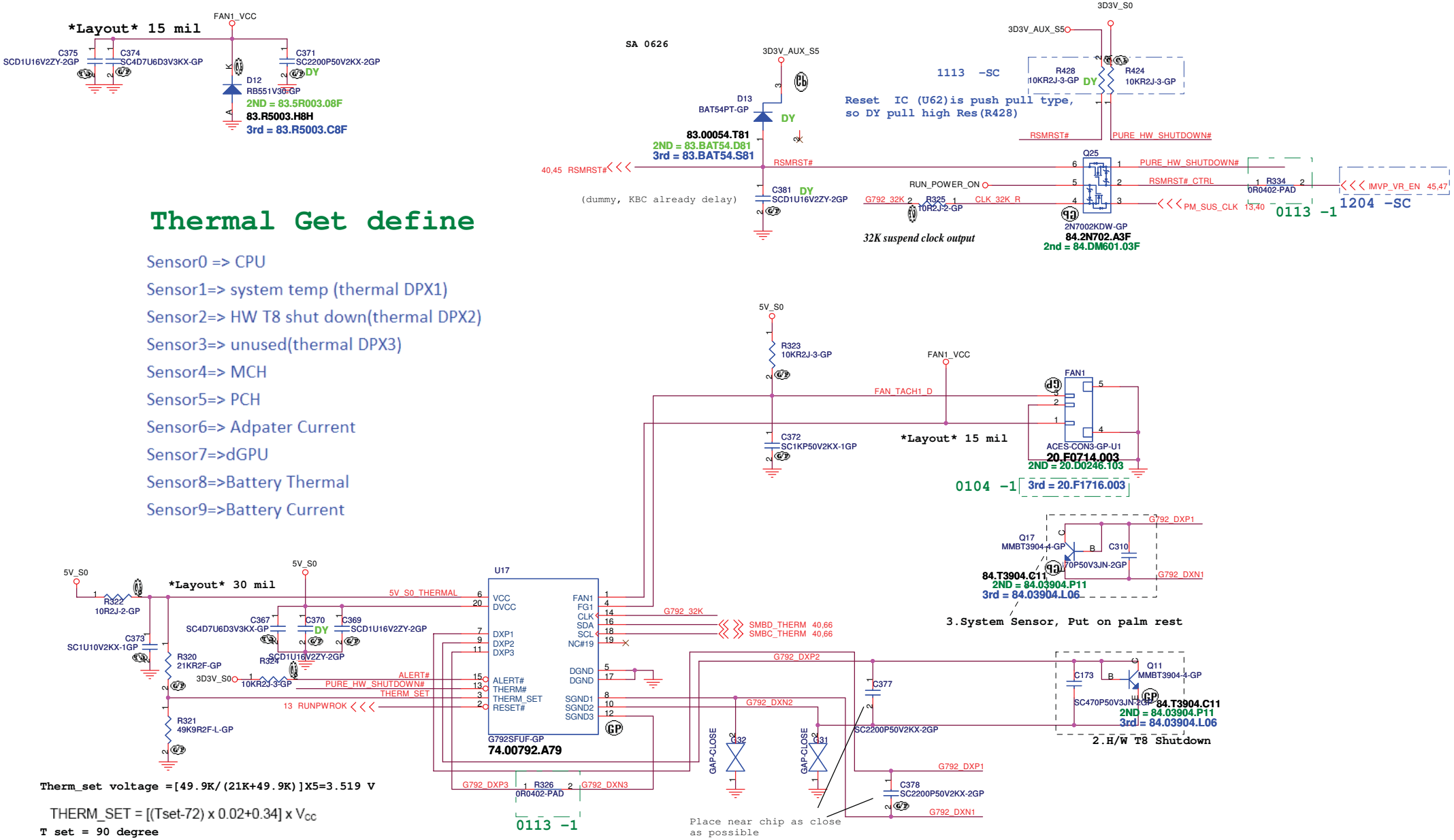


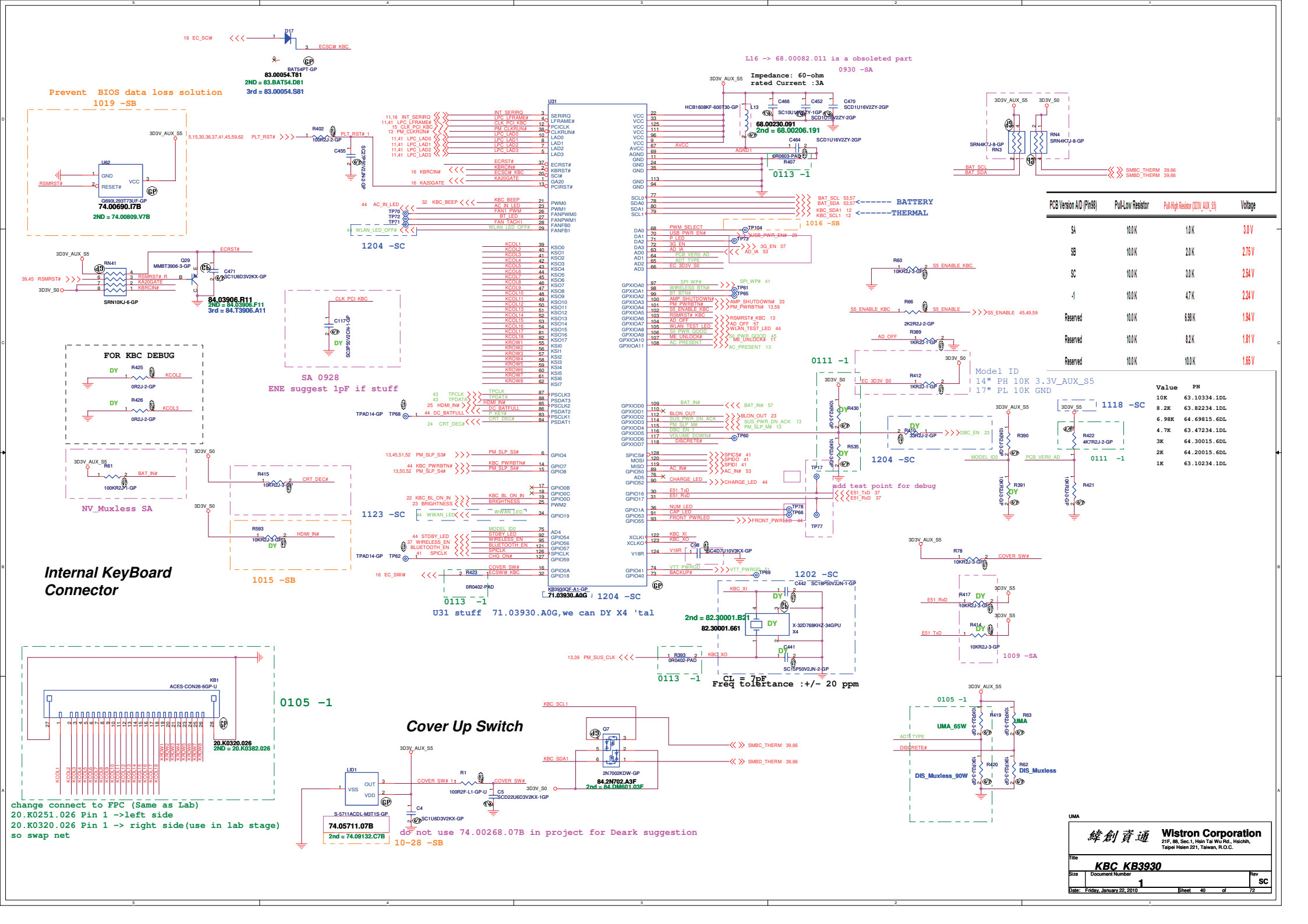
UMA

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan Connector***

Size	Document Number	Rev
	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 39 of 72


Prevent BIOS data loss solution
1019 -SB
83.00054.T81
2ND = 83.BAT54.D81
3rd = 83.00054.S81
L16 -> 68.00082.011 is a obsoleted part
0930 -SA
Impedance: 60-ohm
rated Current :3A
68.00230.091
2nd = 68.00206.191
0113 -1
BATTERY
THERMAL
1016 -SB
1204 -SC
74.00690.I7B
2ND = 74.00809.V7B
84.03906.R11
2ND = 84.03906.F11
3rd = 84.T3906.A11
SA 0928
ENE suggest 1pF if stuff
FOR KBC DEBUG
NV_Muxless SA
1015 -SB
1123 -SC
0111 -1
1118 -SC
1009 -SA
1202 -SC
add test point for debug
Model ID
14" PH 10K 3.3V_AUX_S5
17" PL 10K GND
Internal KeyBoard Connector
U31 stuff 71.03930.A0G,we can DY X4 'tal
71.03930.A0G
2nd = 82.30001.B21
82.30001.661
CL = 7pF
Freq tolerance :+/- 20 ppm
0105 -1
Cover Up Switch
20.K0320.026
2ND = 20.K0382.026
change connect to FPC (Same as Lab)
20.K0251.026 Pin 1 ->left side
20.K0320.026 Pin 1 -> right side(use in lab stage)
so swap net
74.05711.07B
2nd = 74.09132.C7B
do not use 74.00268.07B in project for Deark suggestion
10-28 -SB
UMA
UMA_65W
DIS_Muxless_90W
PCB Version A/D (Pin98)
Pull-Low Resistor
Pull-High Resistor (3D3V_AUX_S5)
Voltage
SA 10.0 K 1.0 K 3.0 V
SB 10.0 K 2.0 K 2.75 V
SC 10.0 K 3.0 K 2.54 V
-1 10.0 K 4.7 K 2.24 V
Reserved 10.0 K 6.98 K 1.94 V
Reserved 10.0 K 8.2 K 1.81 V
Reserved 10.0 K 10.0 K 1.65 V
Value PN
10K 63.10334.1DL
8.2K 63.82234.1DL
6.98K 64.69815.6DL
4.7K 63.47234.1DL
3K 64.30015.6DL
2K 64.20015.6DL
1K 63.10234.1DL
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_KB3930
Size
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Rev
SC
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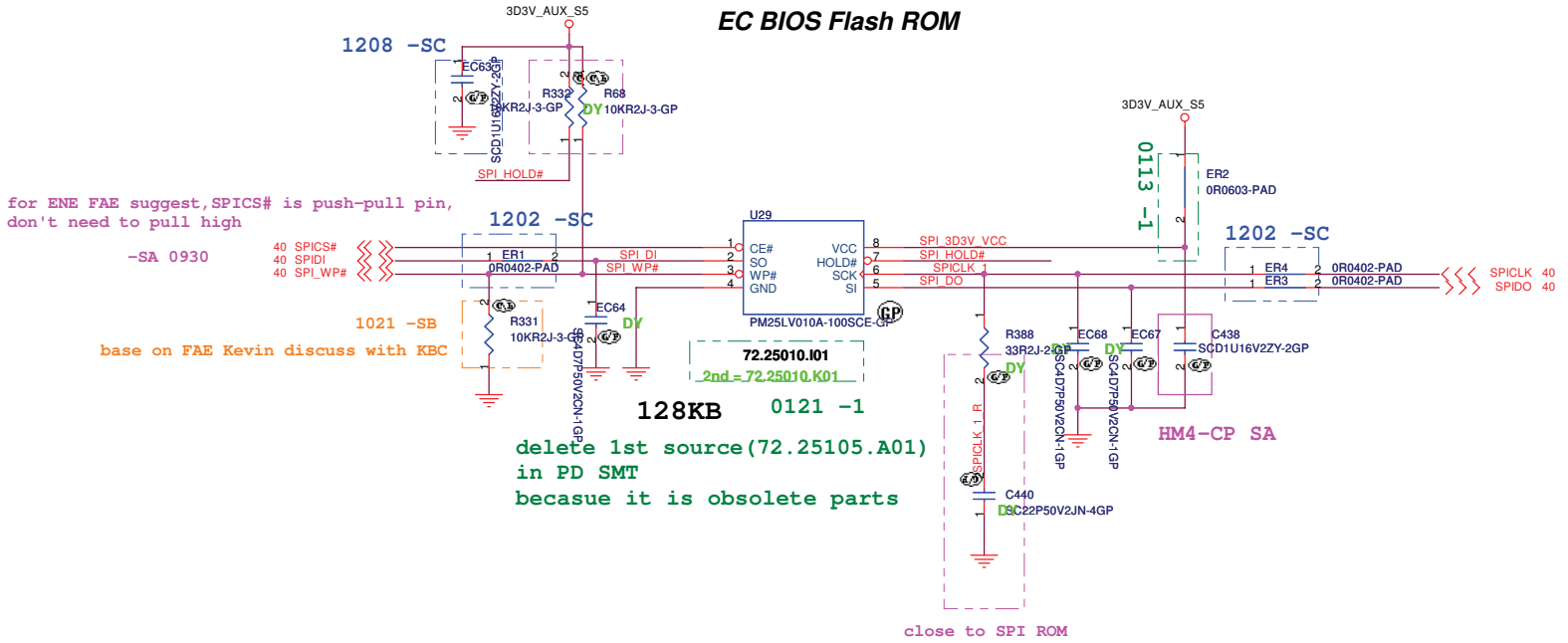
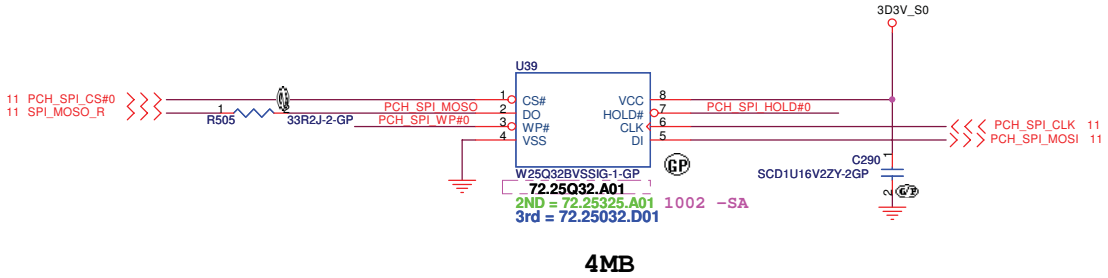
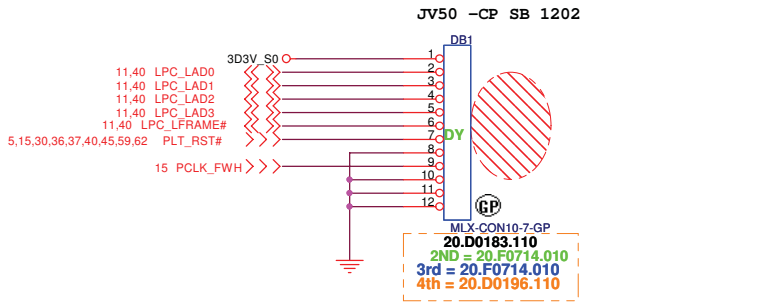
EC BIOS Flash ROM

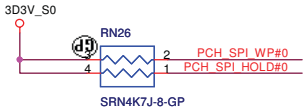


System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD





Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
BIOS		
Size	Document Number	Rev
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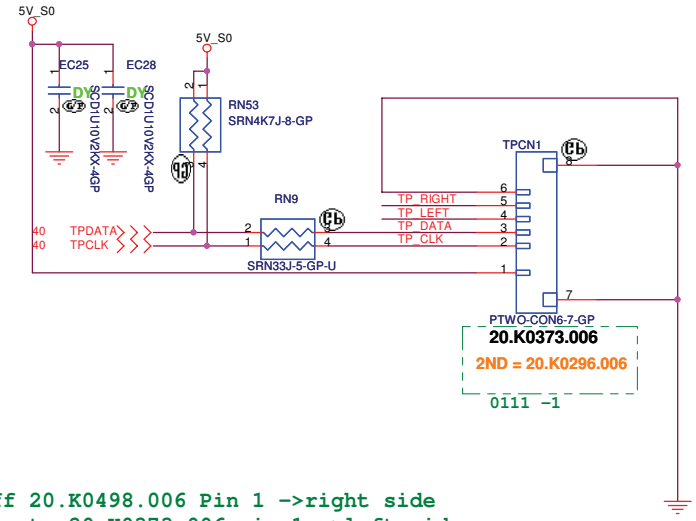
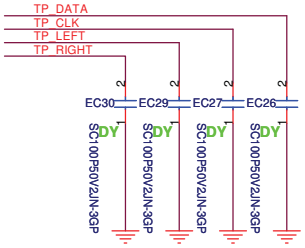
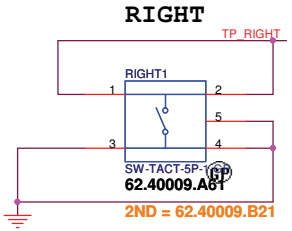
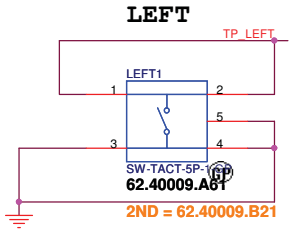




Eng stuff 20.K0498.006 Pin 1 ->right side
PD change to 20.K0373.006 pin 1 ->left side
so net mirror Vertically





Diserete N11M

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Touch PAD		
Size	Document Number: HM42-CP	Rev: SC
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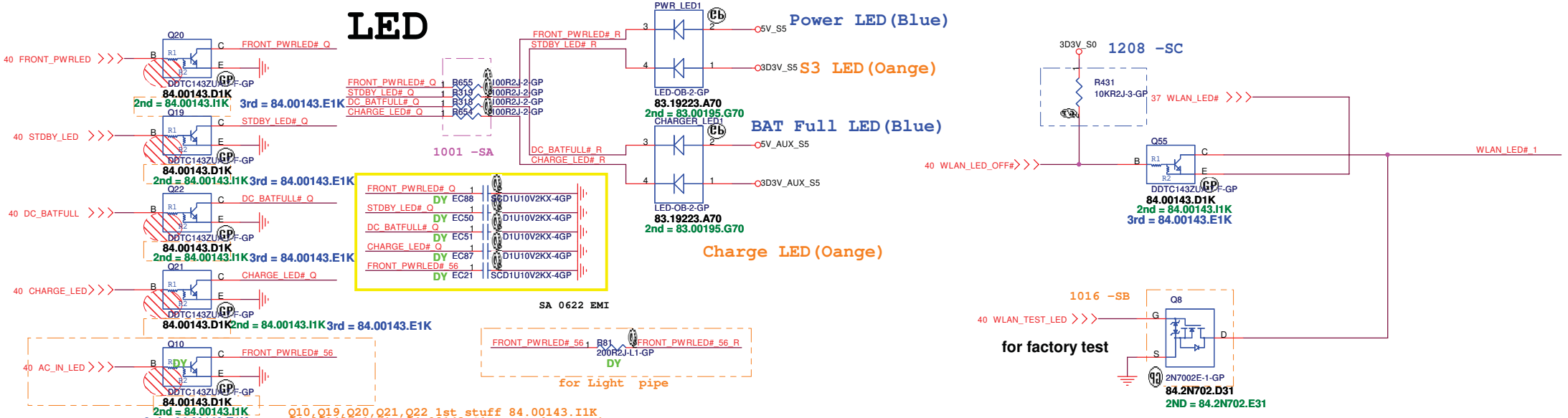
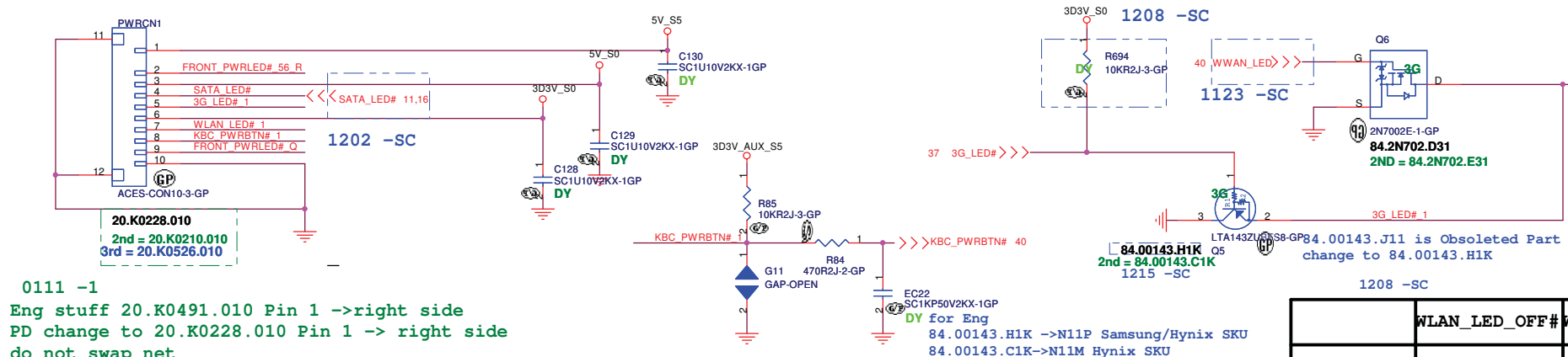
LED



For 2010 Acer Project, WLAN and 3G LED control by KBC



0111 -1
Eng stuff 20.K0491.010 Pin 1 ->right side
PD change to 20.K0228.010 Pin 1 -> right side
do not swap net

Pin 1	5V_S5	
Pin 2	FRONT_PWRLED#_56_R	AC IN
Pin 3	5V_S0	
Pin 4	MEDIA_LED#_R	HDD
Pin 5	3G_LED#_R	3G
Pin 6	3D3V_S0	
Pin 7	WLAN_LED#_R	WLAN
Pin 8	KBC_PWRBTN#_1	Power button
Pin 9	FRONT_PWRLED#_Q	Power LED
Pin 10	GND	

1208 -SC

	WLAN_LED_OFF#	WLAN_TEST_LED	WWAN_LED
WLAN ON Always on	L	H	L
WLAN ON (flash)	H	L	L
WWAN_ON	L	L	H
WLAN ON WWAN_ON	L	L	H

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LED&POWERBD CONN

Size | Document Number: HM42-CP | Rev: SC

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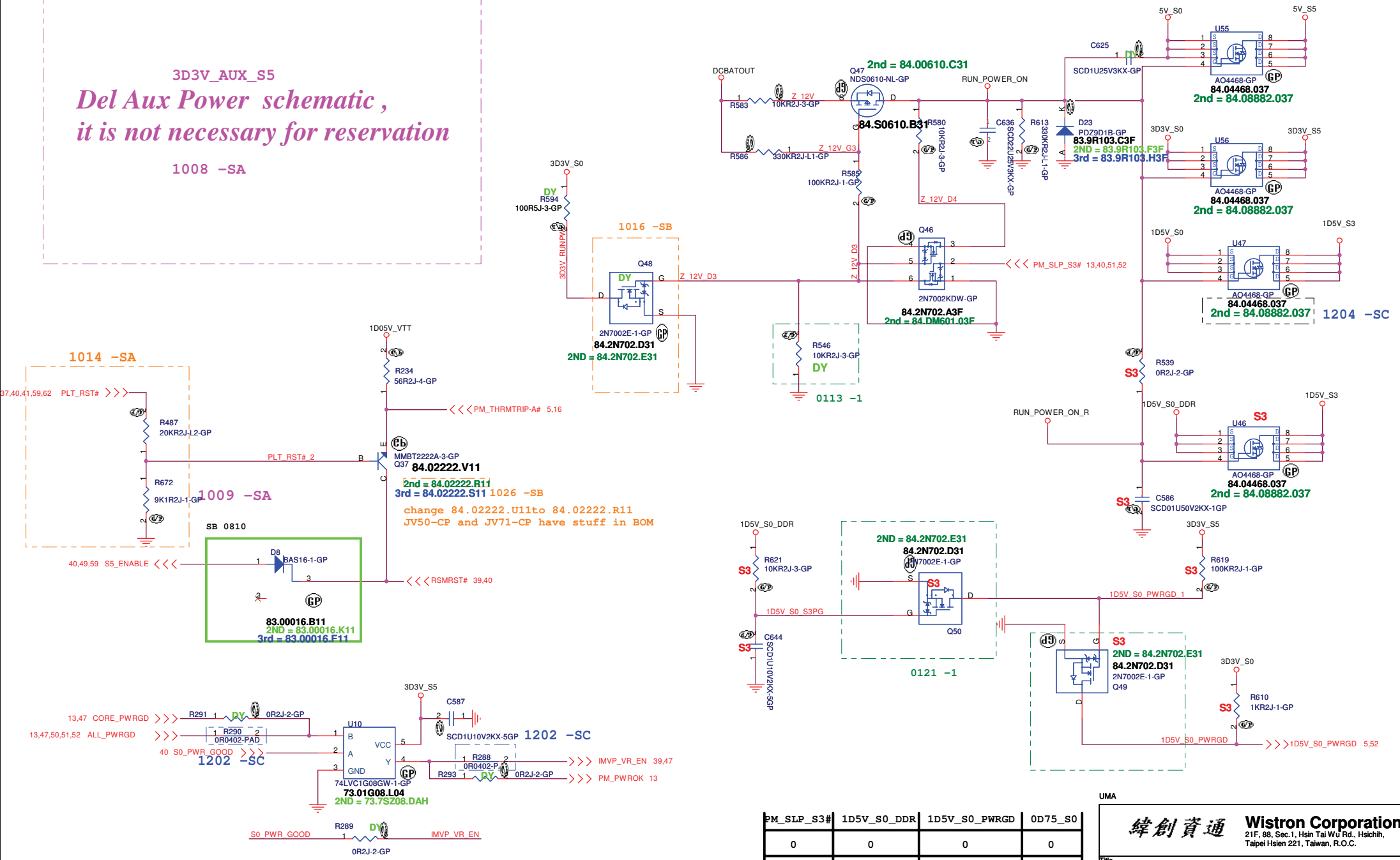
Run Power

3D3V_AUX_S5

Del Aux Power schematic ,
it is not necessary for reservation

1008 -SA



PM_SLP_S3#	1D5V_S0_DDR	1D5V_S0_PWRGD	0D75_S0
0	0	0	0
1	1	1	1

UMA

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RUN POWER and 3D3V_AUX_S5

Size	Document Number	Rev
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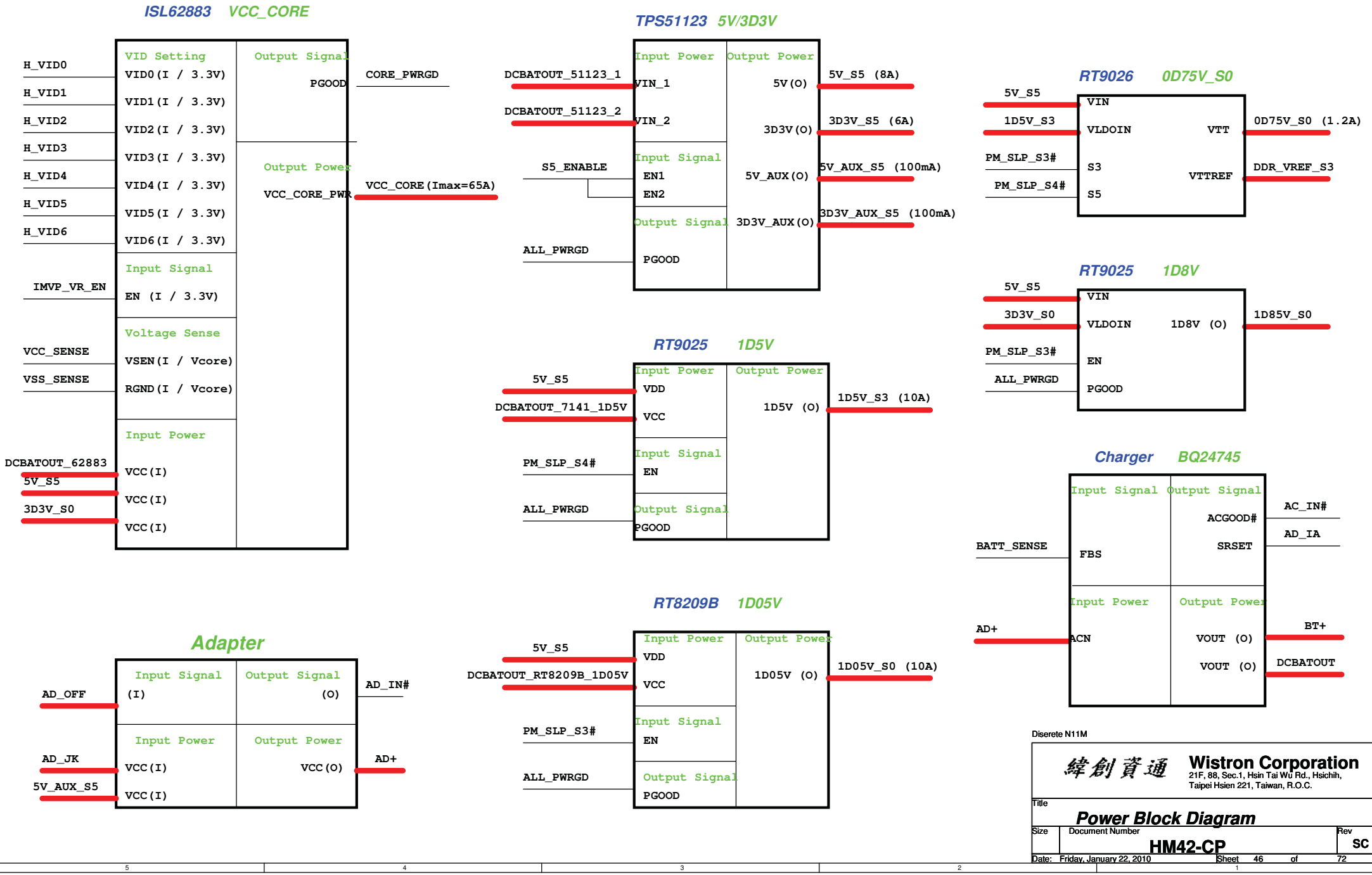

Diserete N11M

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

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	HM42-CP	SC

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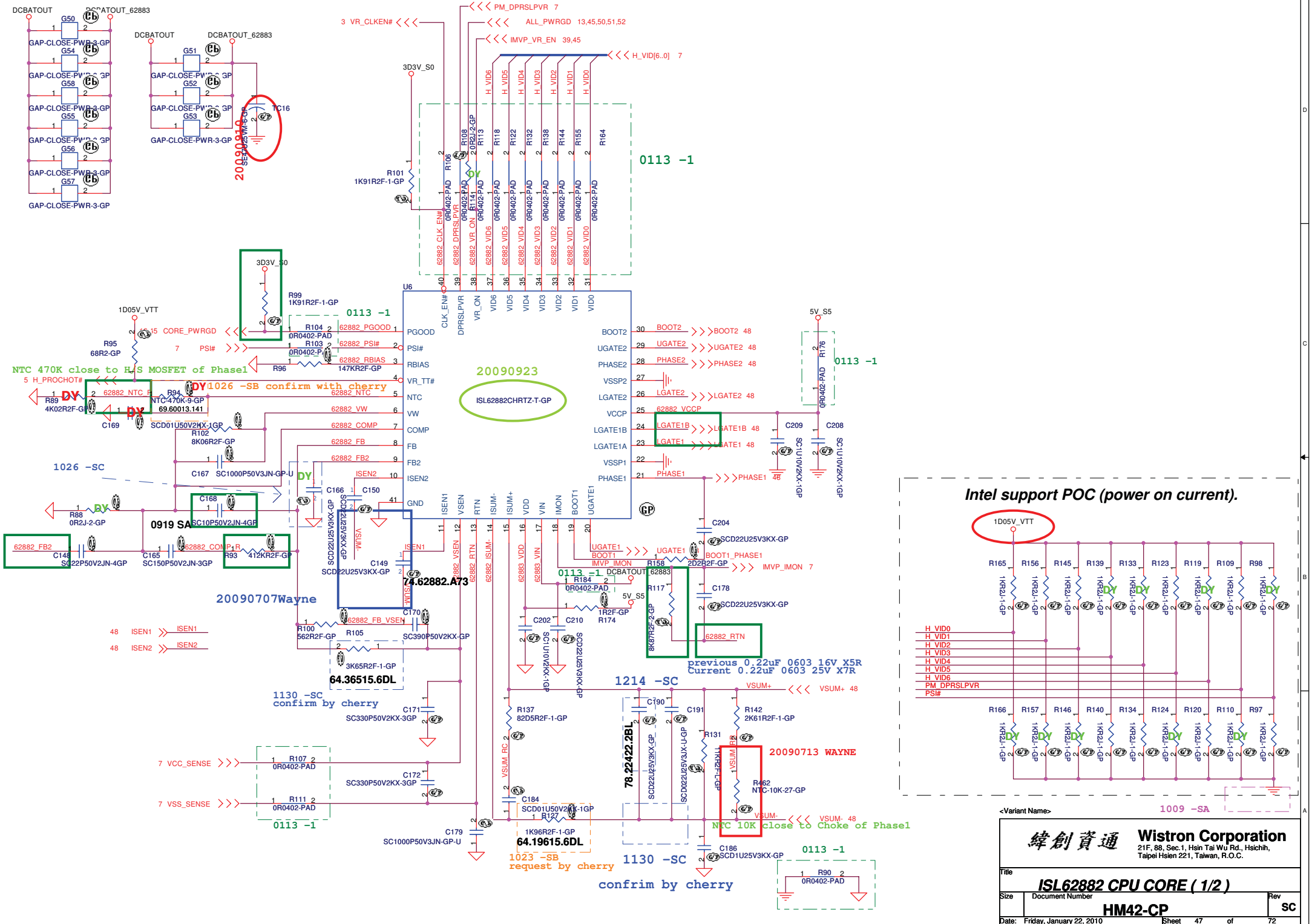
DCBATOUT
DCBATOUT_62883
GAP-CLOSE-PWR-3-GP
TC16
SE025VM-6-GP
20090910
3 VR_CLKEN#
PM_DPRSLPVR 7
ALL_PWRGD 13,45,50,51,52
IMVP_VR_EN 39,45
H_VID[6..0] 7
3D3V_S0
R101 1K91R2F-1-GP
R106 0R2J-2-GP
0R0402-PAD
0113 -1
U6
ISL62882CHRTZ-T-GP
20090923
PGOOD
PSI#
RBIAS
VR_TT#
NTC
VW
COMP
FB
FB2
ISEN2
GND
ISEN1
VSEN
RTN
ISUM-
ISUM+
VDD
VIN
IMON
BOOT1
UGATE1
BOOT2
UGATE2
PHASE2
VSSP2
LGATE2
VCCP
LGATE1B
LGATE1A
VSSP1
PHASE1
1D05V_VTT
5V_S5
CORE_PWRGD
PSI#
R95 68R2-GP
R96 147KR2F-GP
R99 1K91R2F-1-GP
R104 0R0402-PAD
R103 0R0402-PAD
NTC 470K close to H_LS MOSFET of Phase1
H_PROCHOT#
R89 4K02R2F-GP
R94 NTC-470K-9-GP
69.60013.141
1026 -SB confirm with cherry
C169 SCD01U50V2KX-1GP
R102 8K06R2F-GP
C167 SC1000P50V3JN-GP-U
1026 -SC
R88 0R2J-2-GP
C168 SC10P50V2JN-4GP
0919 SA
C166 SCD22U25V3KX-GP
C150 SC1U10V2KX-1GP
C148 SC22P50V2JN-4GP
C165 SC150P50V2JN-3GP
R93 412KR2F-GP
C149 SCD22U25V3KX-GP
74.62882.A73
20090707Wayne
C170 SC390P50V2KX-GP
R100 562R2F-GP
R105 3K65R2F-1-GP
64.36515.6DL
1130 -SC confirm by cherry
C171 SC330P50V2KX-3GP
C172 SC330P50V2KX-3GP
7 VCC_SENSE
7 VSS_SENSE
R107 0R0402-PAD
R111 0R0402-PAD
0113 -1
C179 SC1000P50V3JN-GP-U
R137 82D5R2F-1-GP
C190 78.22422.2BL
C191 SCD22U25V3JX-U-GP
R131 1KR2F-1-GP
R142 2K61R2F-1-GP
20090713 WAYNE
R462 NTC-10K-27-GP
NTC 10K close to Choke of Phase1
C184 SCD01U50V2KX-1GP
R127 1K96R2F-1-GP
64.19615.6DL
1023 -SB request by cherry
1214 -SC
1130 -SC confrim by cherry
C186 SCD1U25V3KX-GP
R90 0R0402-PAD
0113 -1
C204 SCD22U25V3KX-GP
R158 2D2R2F-GP
C178 SCD22U25V3KX-GP
R117 8K87R2F-2-GP
C202 SCD22U25V3KX-GP
C210 SC1U10V2KX-1GP
R174 1R2F-GP
previous 0.22uF 0603 16V X5R
Current 0.22uF 0603 25V X7R
R176 0R0402-PAD
C209 SC1U10V2KX-1GP
C208 SC1U10V2KX-1GP
Intel support POC (power on current).
1009 -SA
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
PM_DPRSLPVR
PSI#
R165 R156 R145 R139 R133 R123 R119 R109 R98
R166 R157 R146 R140 R134 R124 R120 R110 R97
1KR2J-1-GP
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62882 CPU CORE (1/2)
Size
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
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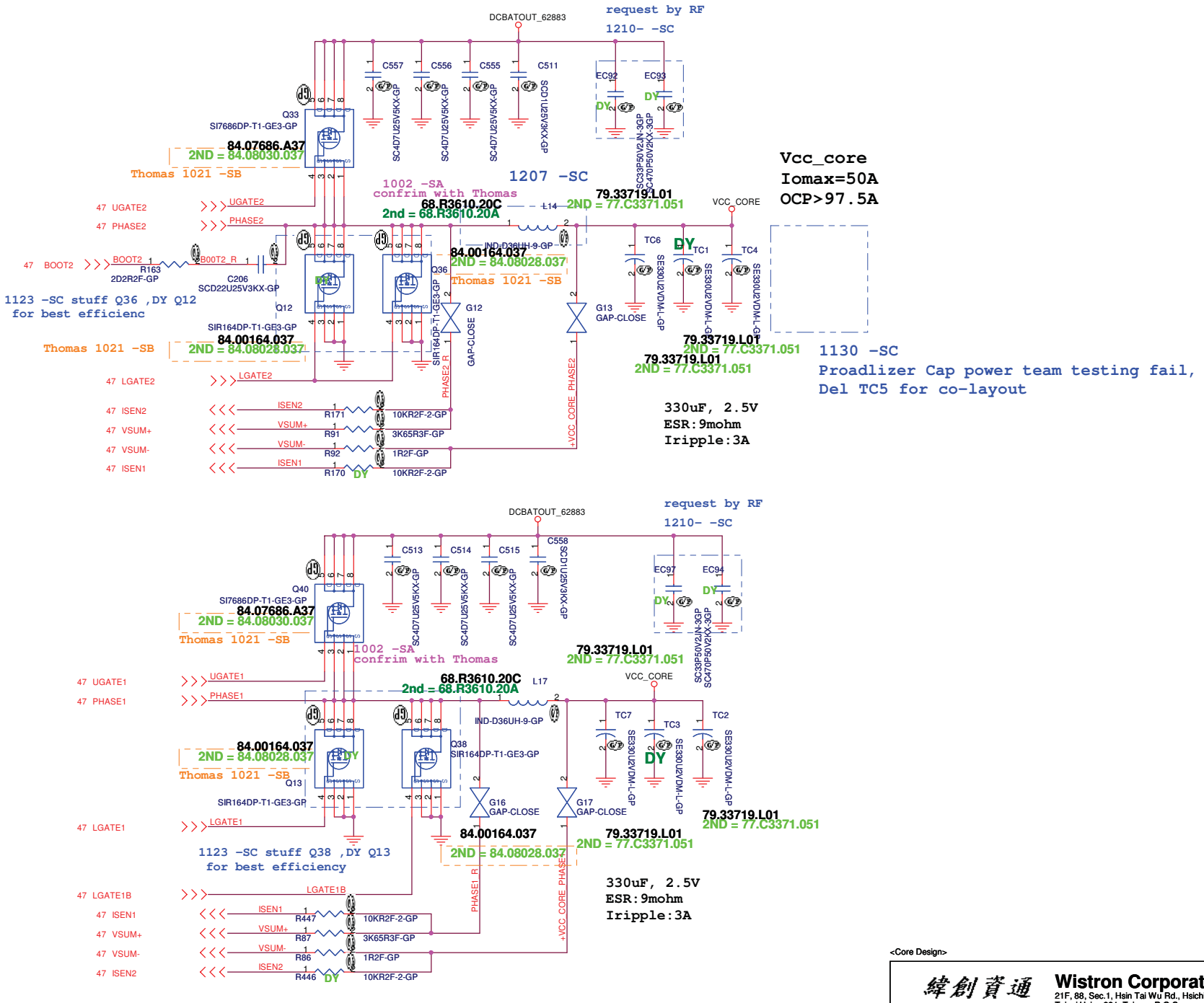

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL62882 CPU CORE (1/2)

Size	Document Number	Rev
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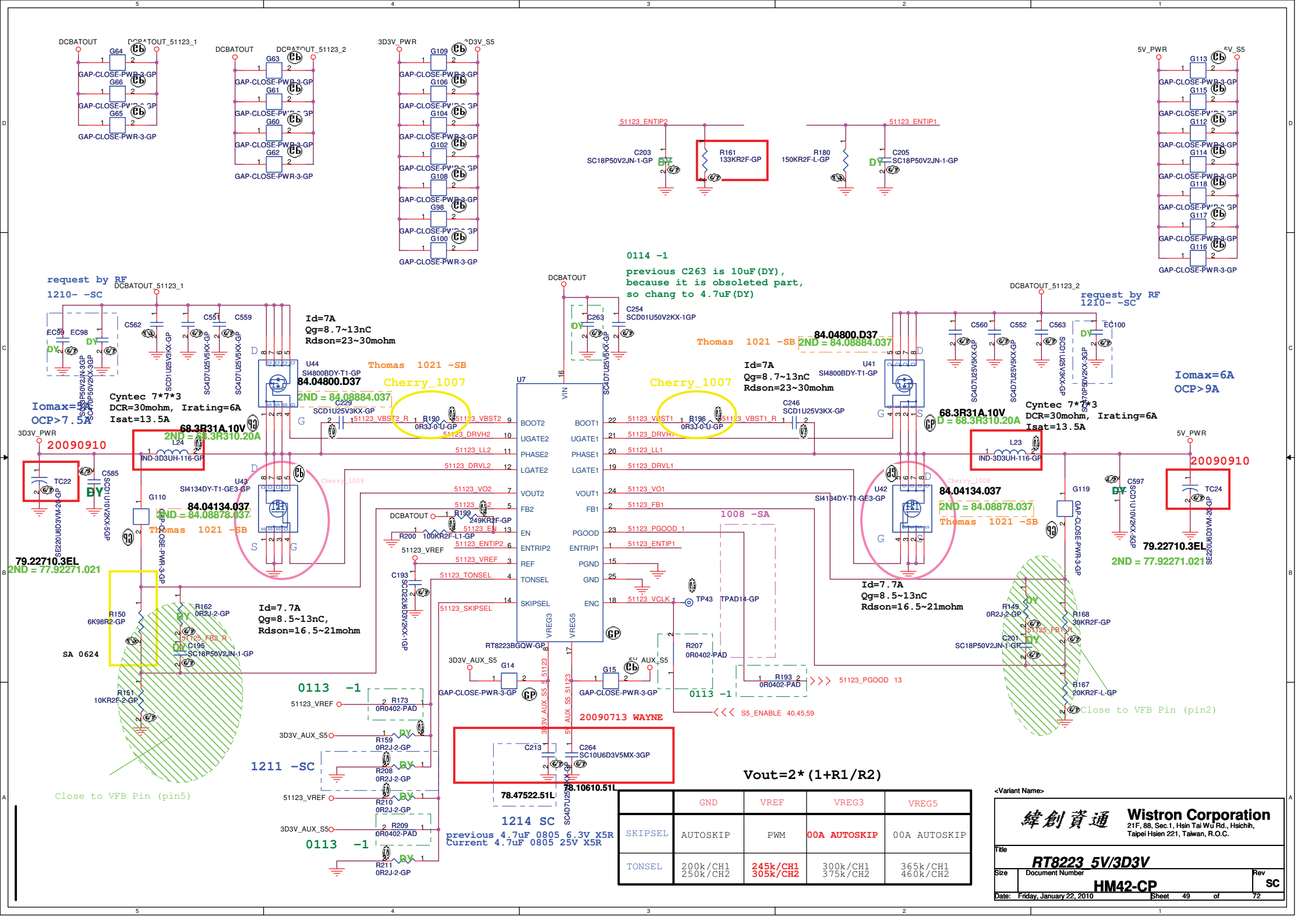

	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8223_5V/3D3V

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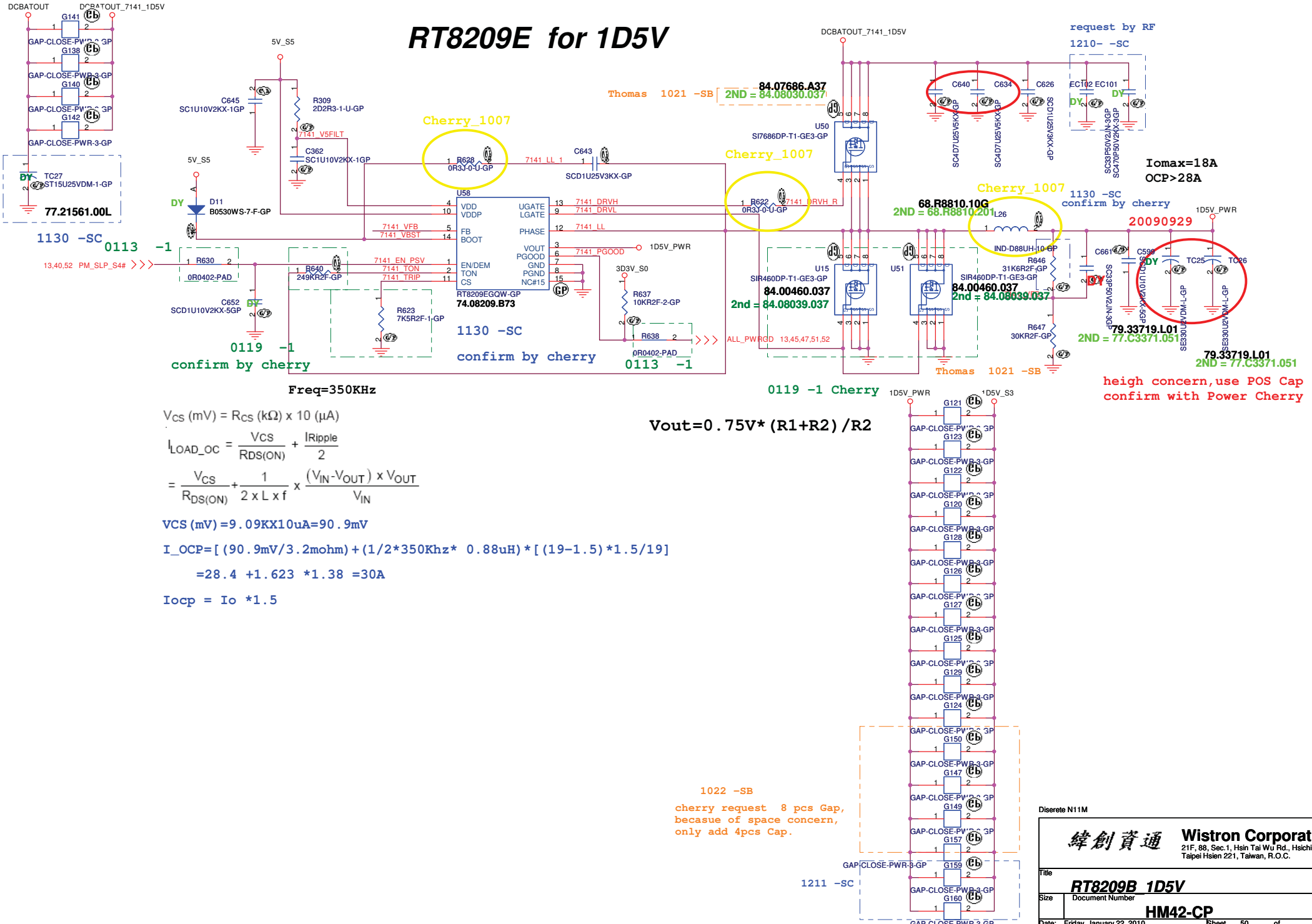
RT8209E for 1D5V



$$V_{CS}\,(mV) = R_{CS}\,(k\Omega) \times 10\,(\mu A)$$

$$I_{LOAD\_OC} = \frac{V_{CS}}{R_{DS(ON)}} + \frac{I_{Ripple}}{2}$$

$$= \frac{V_{CS}}{R_{DS(ON)}} + \frac{1}{2 \times L \times f} \times \frac{(V_{IN}-V_{OUT}) \times V_{OUT}}{V_{IN}}$$

VCS(mV)=9.09KX10uA=90.9mV

I_OCP=[(90.9mV/3.2mohm)+(1/2*350Khz* 0.88uH)*[(19-1.5)*1.5/19]

=28.4 +1.623 *1.38 =30A

Iocp = Io *1.5

Diserete N11M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT8209B 1D5V		
Size	Document Number	Rev
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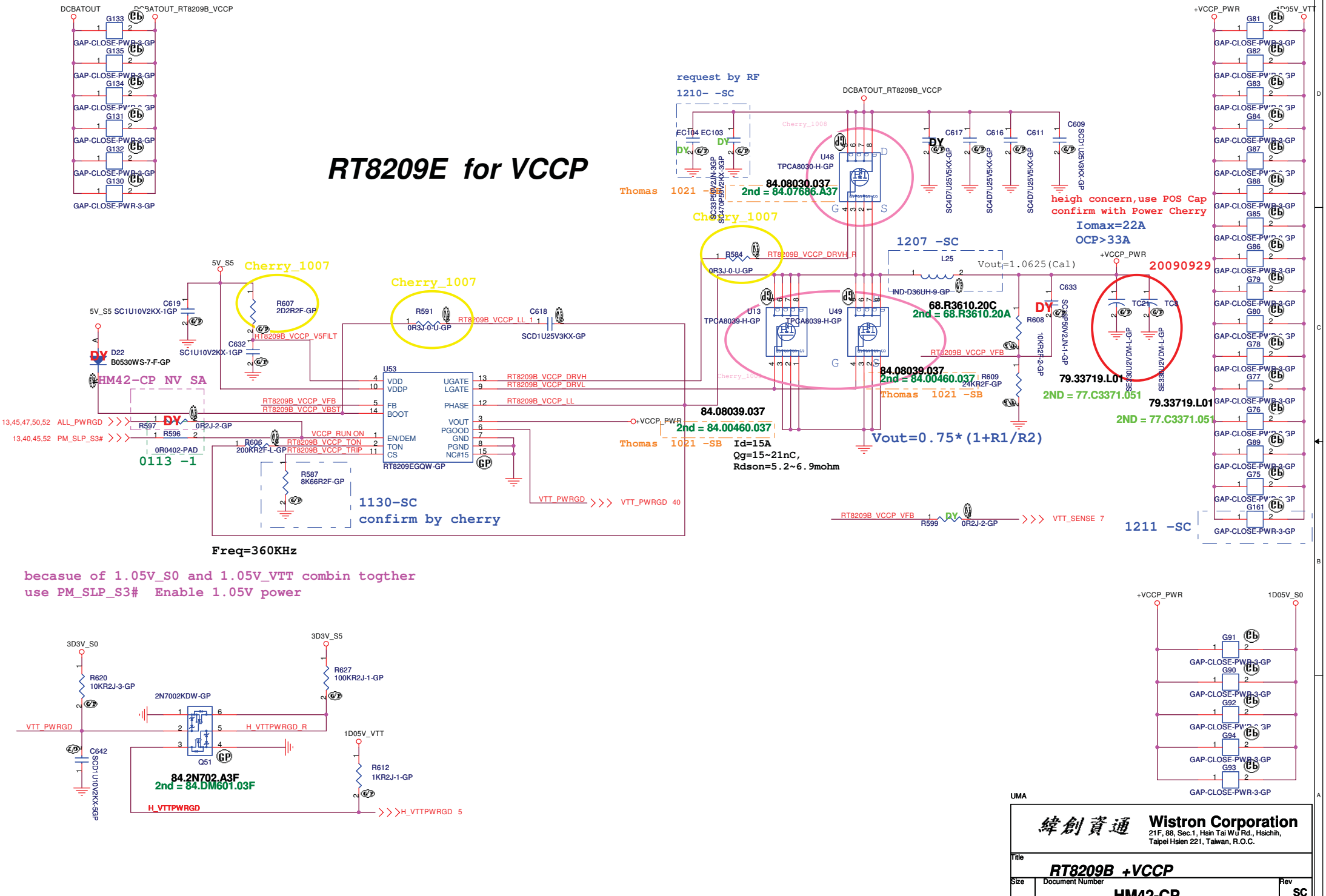
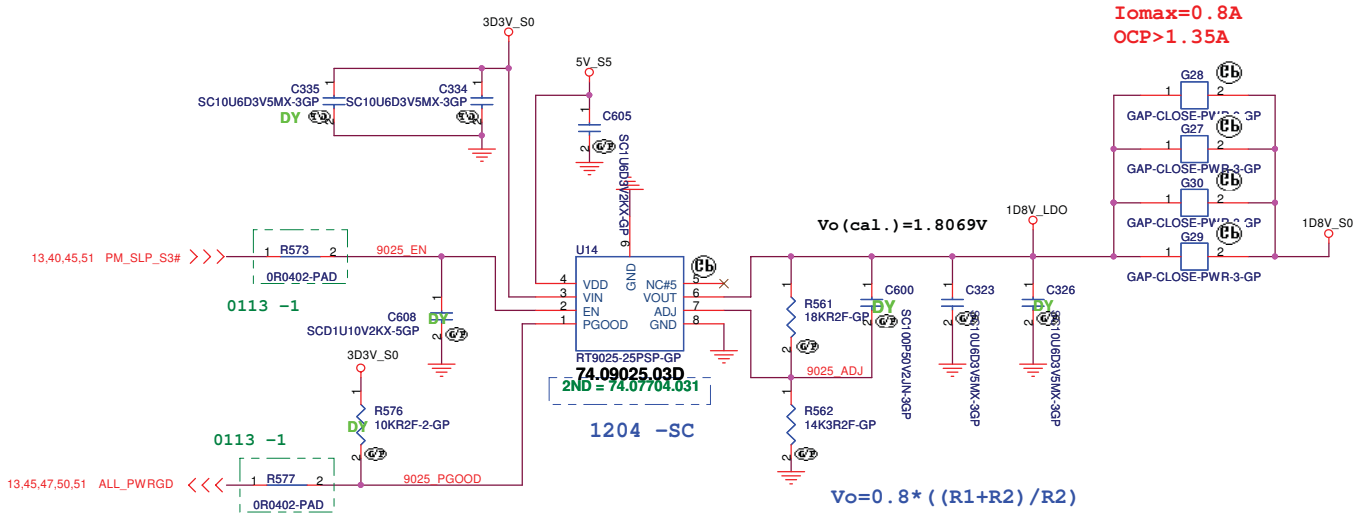
RT8209E for VCCP

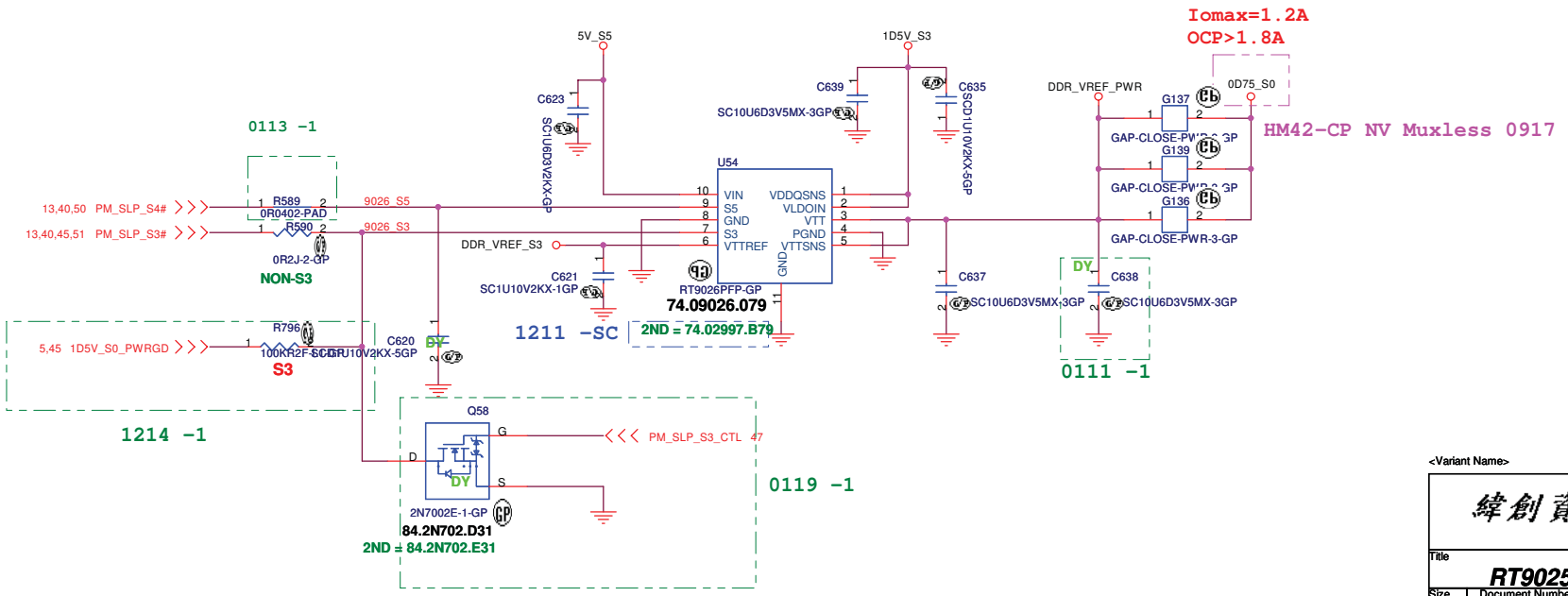


RT9025 for 1D8V_S0

20090915



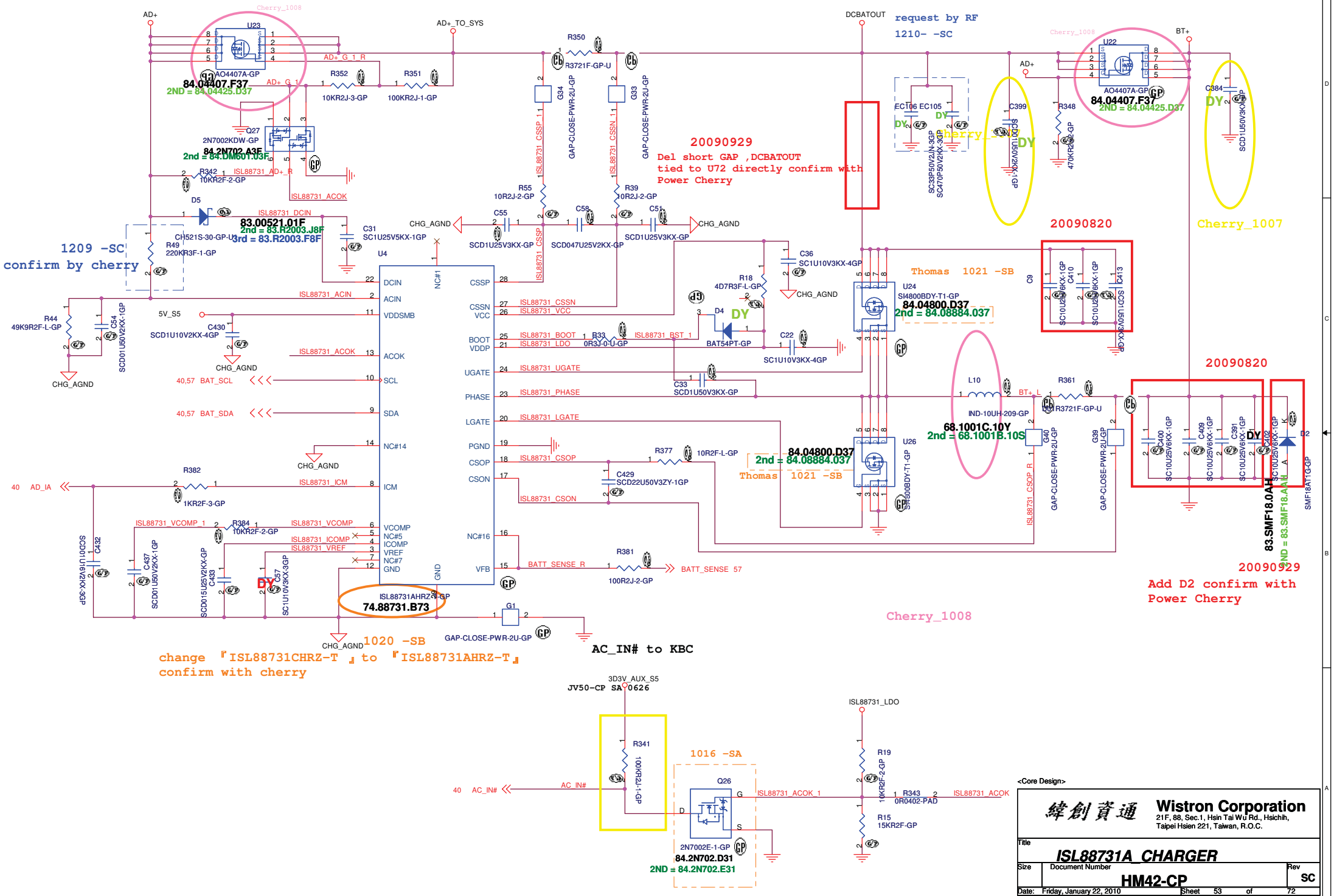
RT9026 for 0D75V_S0



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RT9025_1D8V/RT9026_0D75		
Size	Document Number	Rev
	HM42-CP	SC
Date: Friday, January 22, 2010	Sheet 52 of 72	



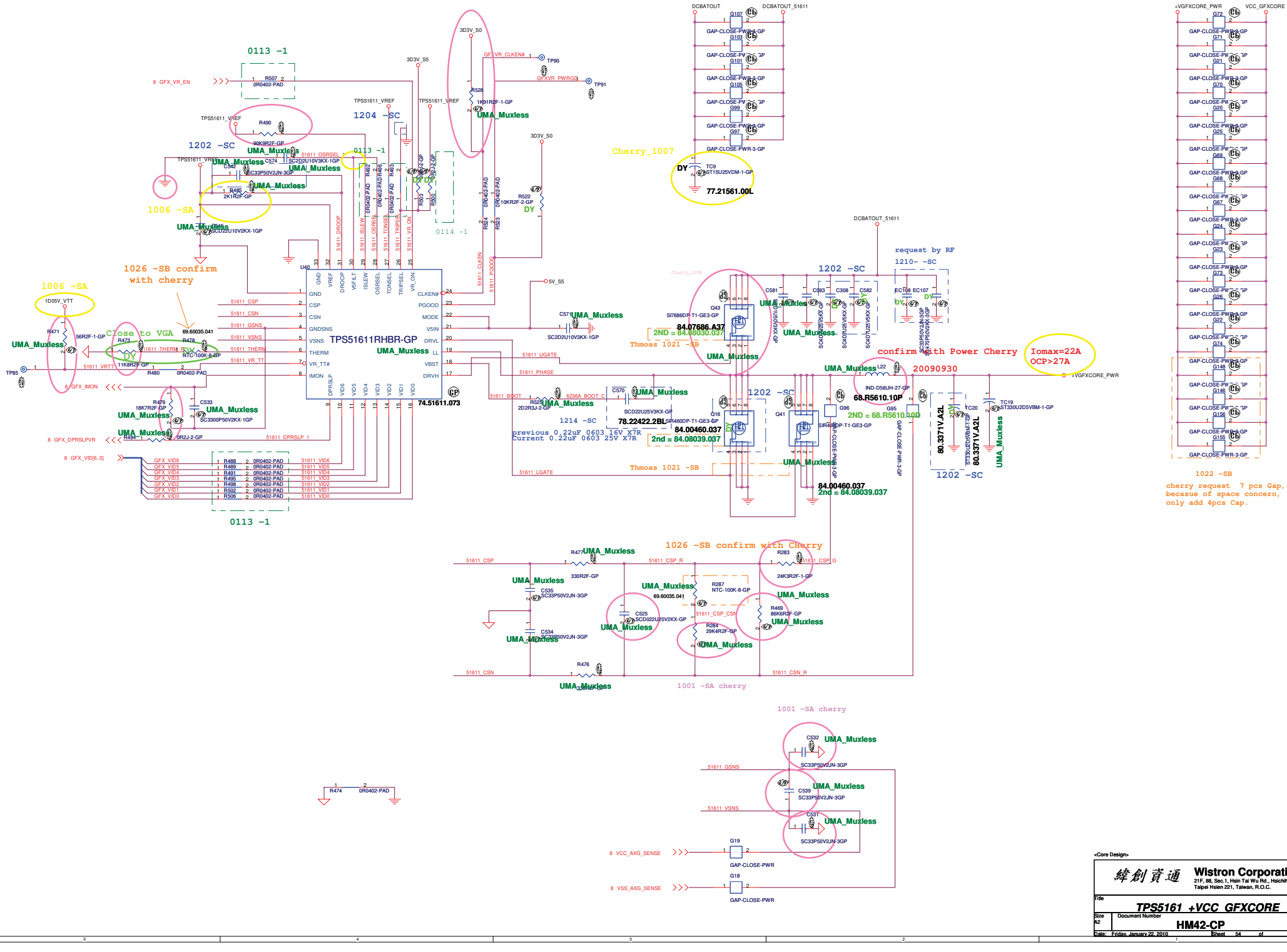
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

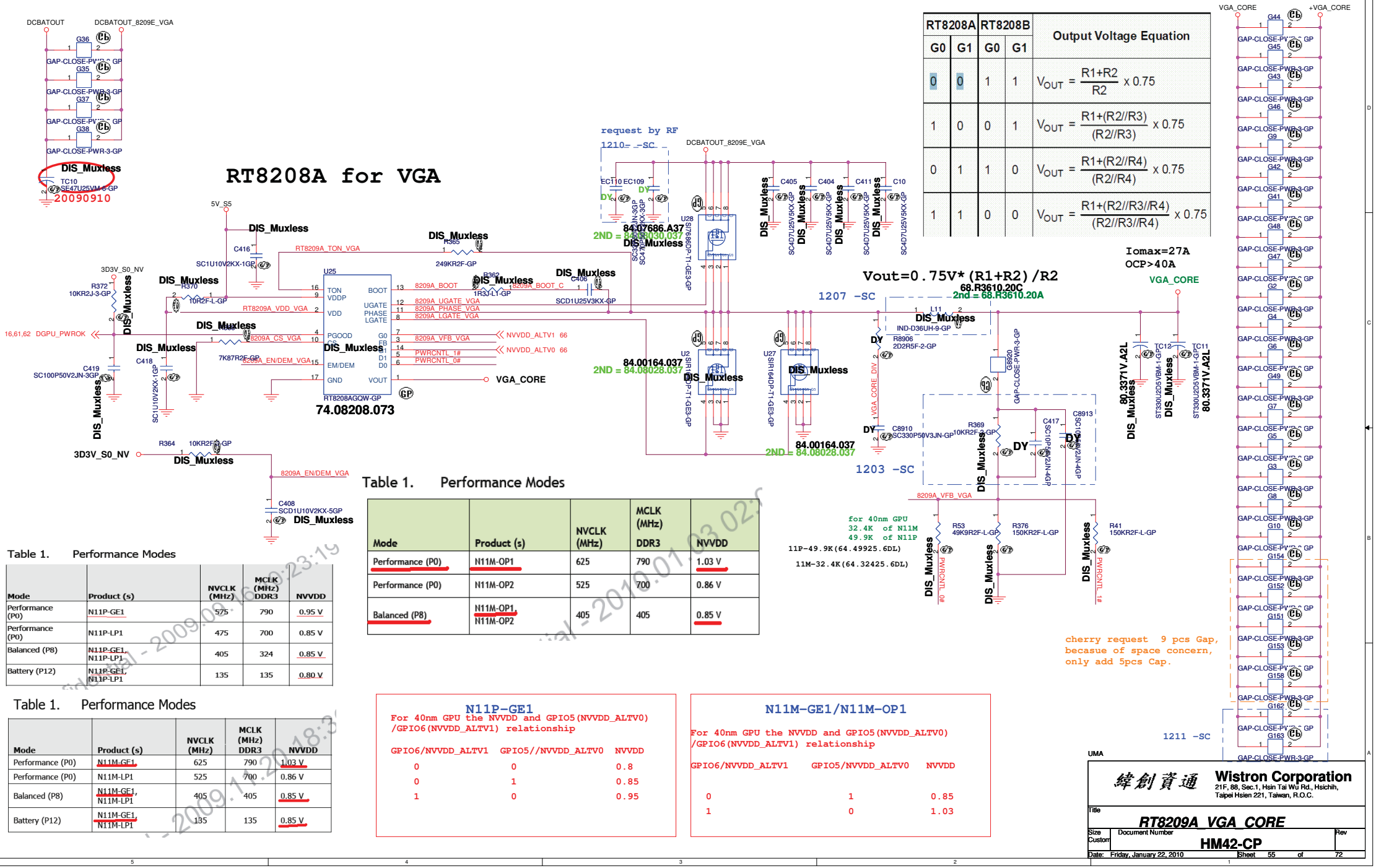
Title: ISL88731A_CHARGER

Size: | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 53 of 72


TPS51611RHBR-GP
74.51611.073
0113 -1
1204 -SC
1202 -SC
1006 -SA
1026 -SB confirm with cherry
Close to VGA
Cherry_1007
77.21561.00L
confirm with Power Cherry
Iomax=22A
OCP>27A
20090930
request by RF
1210- -SC
1022 -SB
cherry request 7 pcs Gap, becasue of space concern, only add 4pcs Cap.
1001 -SA cherry
Thmoas 1021 -SB
previous 0.22uF 0603 16V X7R
Current 0.22uF 0603 25V X7R
Wistron Corporation
TPS5161 +VCC_GFXCORE
HM42-CP
SC

RT8208A for VGA



RT8208A		RT8208B		Output Voltage Equation
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-OP1	625	790	1.03 V
Performance (P0)	N11M-OP2	525	700	0.86 V
Balanced (P8)	N11M-OP1, N11M-OP2	405	405	0.85 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11P-GE1	575	790	0.95 V
Performance (P0)	N11P-LP1	475	700	0.85 V
Balanced (P8)	N11P-GE1, N11P-LP1	405	324	0.85 V
Battery (P12)	N11P-GE1, N11P-LP1	135	135	0.80 V

Table 1. Performance Modes

Mode	Product (s)	NVCLK (MHz)	MCLK (MHz) DDR3	NVVDD
Performance (P0)	N11M-GE1	625	790	1.03 V
Performance (P0)	N11M-LP1	525	700	0.86 V
Balanced (P8)	N11M-GE1, N11M-LP1	405	405	0.85 V
Battery (P12)	N11M-GE1, N11M-LP1	135	135	0.85 V

N11P-GE1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5//NVVDD_ALTV0	NVVDD
0	0	0.8
0	1	0.85
1	0	0.95

N11M-GE1/N11M-OP1

For 40nm GPU the NVVDD and GPIO5(NVVDD_ALTV0) /GPIO6(NVVDD_ALTV1) relationship

GPIO6/NVVDD_ALTV1	GPIO5/NVVDD_ALTV0	NVVDD
0	1	0.85
1	0	1.03

UMA

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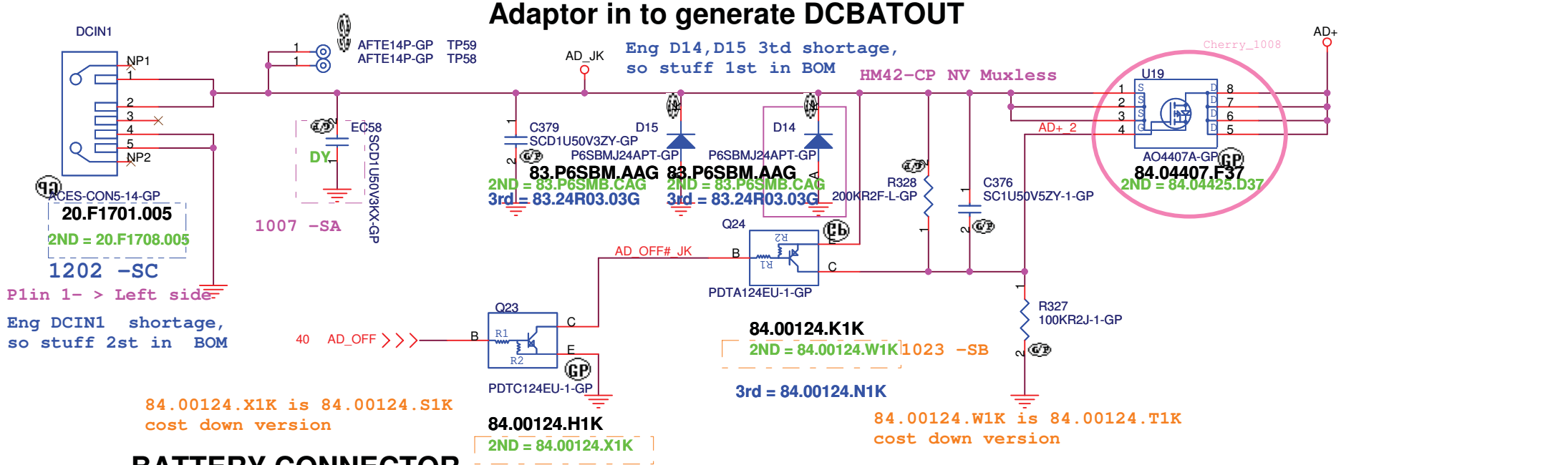
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8209A_VGA_CORE

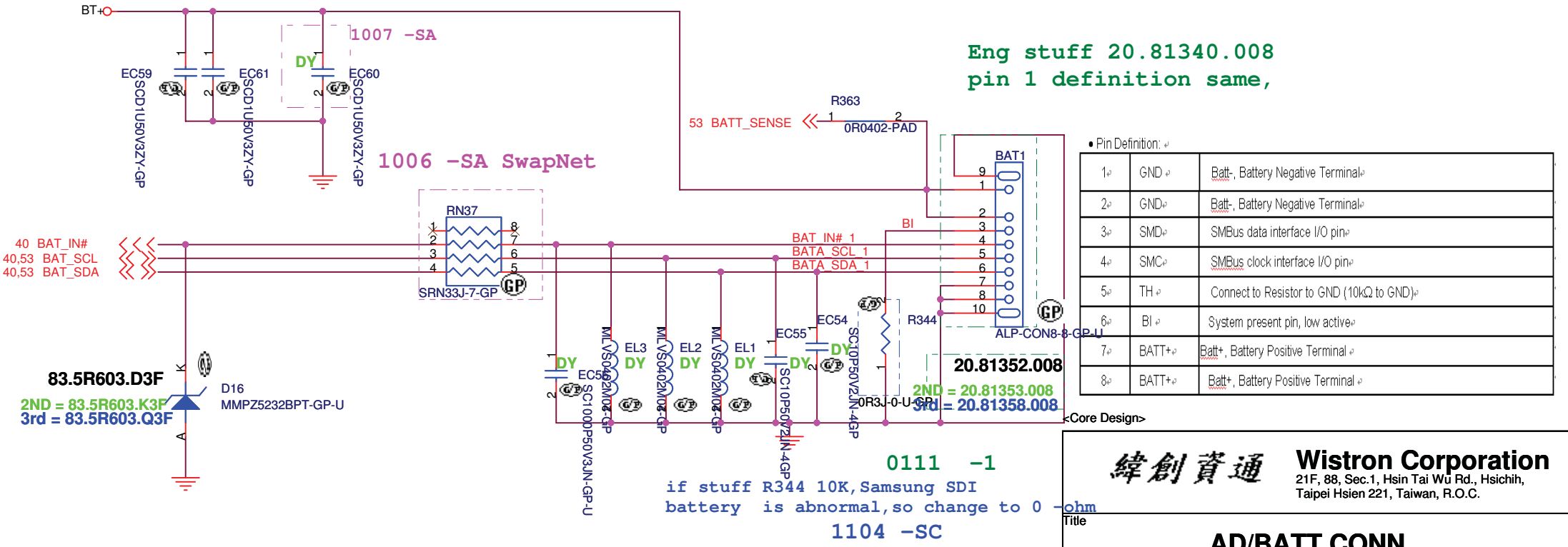
Size: Custom | Document Number: HM42-CP | Rev:

Date: Friday, January 22, 2010 | Sheet 55 of 72

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



• Pin Definition:

1	GND	Batt-, Battery Negative Terminal
2	GND	Batt-, Battery Negative Terminal
3	SMD	SMBus data interface I/O pin
4	SMC	SMBus clock interface I/O pin
5	TH	Connect to Resistor to GND (10kΩ to GND)
6	BI	System present pin, low active
7	BATT+	Batt+, Battery Positive Terminal
8	BATT+	Batt+, Battery Positive Terminal

<Core Design>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

Size	Document Number	Rev
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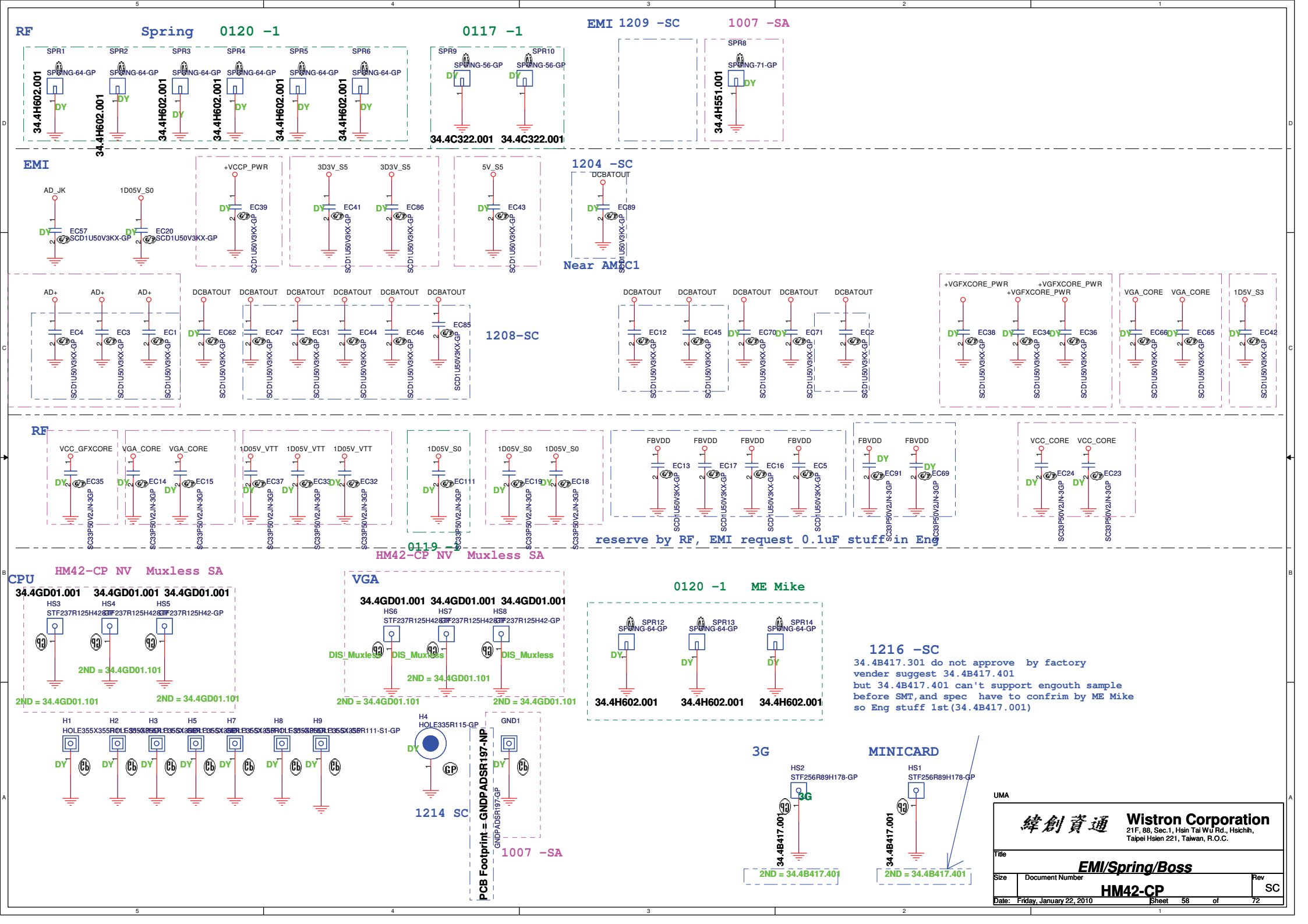
Date: Friday, January 22, 2010 Sheet 57 of 72


RF
Spring
0120 -1
0117 -1
EMI 1209 -SC
1007 -SA
SPR1
SPR2
SPR3
SPR4
SPR5
SPR6
SPRING-64-GP
34.4H602.001
DY
SPR9
SPR10
SPRING-56-GP
34.4C322.001
SPR8
SPRING-71-GP
34.4H551.001
EMI
AD_JK
1D05V_S0
EC57
SCD1U50V3KX-GP
EC20
+VCCP_PWR
EC39
3D3V_S5
EC41
EC86
5V_S5
EC43
1204 -SC
DCBATOUT
EC89
Near AMEC1
AD+
EC4
EC3
EC1
EC62
EC47
EC31
EC44
EC46
EC85
1208-SC
EC12
EC45
EC70
EC71
EC2
+VGFXCORE_PWR
EC38
EC34
EC36
VGA_CORE
EC66
EC65
1D5V_S3
EC42
RF
VCC_GFXCORE
EC35
EC14
EC15
1D05V_VTT
EC37
EC33
EC32
EC111
EC19
EC18
FBVDD
EC13
EC17
EC16
EC5
EC91
EC69
VCC_CORE
EC24
EC23
SC33P50V2JN-3GP
0119 -1
HM42-CP NV Muxless SA
reserve by RF, EMI request 0.1uF stuff in Eng
CPU
HM42-CP NV Muxless SA
34.4GD01.001
HS3
HS4
HS5
STF237R125H42-GP
2ND = 34.4GD01.101
VGA
HS6
HS7
HS8
DIS_Muxless
0120 -1 ME Mike
SPR12
SPR13
SPR14
34.4H602.001
1216 -SC
34.4B417.301 do not approve by factory
vender suggest 34.4B417.401
but 34.4B417.401 can't support engouth sample
before SMT,and spec have to confrim by ME Mike
so Eng stuff 1st(34.4B417.001)
H1
H2
H3
H5
H7
H8
H9
HOLE355X355R111-S1-GP
CB
H4
HOLE335R115-GP
GP
GND1
GNDPADSR197-GP
PCB Footprint = GNDPADSR197-NP
1214 SC
1007 -SA
3G
MINICARD
HS2
HS1
STF256R89H178-GP
34.4B417.001
2ND = 34.4B417.401
UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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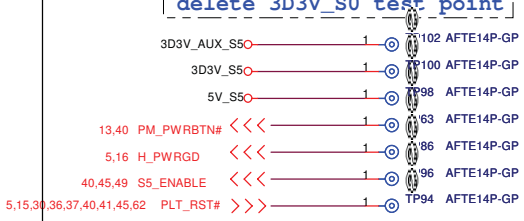
Title
EMI/Spring/Boss
Size
Document Number
HM42-CP
Rev
SC
Date: Friday, January 22, 2010
Sheet 58 of 72

Check test point

delete 3D3V_S0 test point



Test Point放在Dimm Door打開可量測處

<Variant Name>

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Title		
AFTE_TP		
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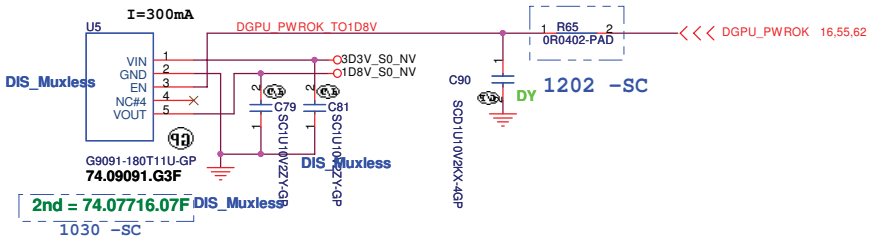
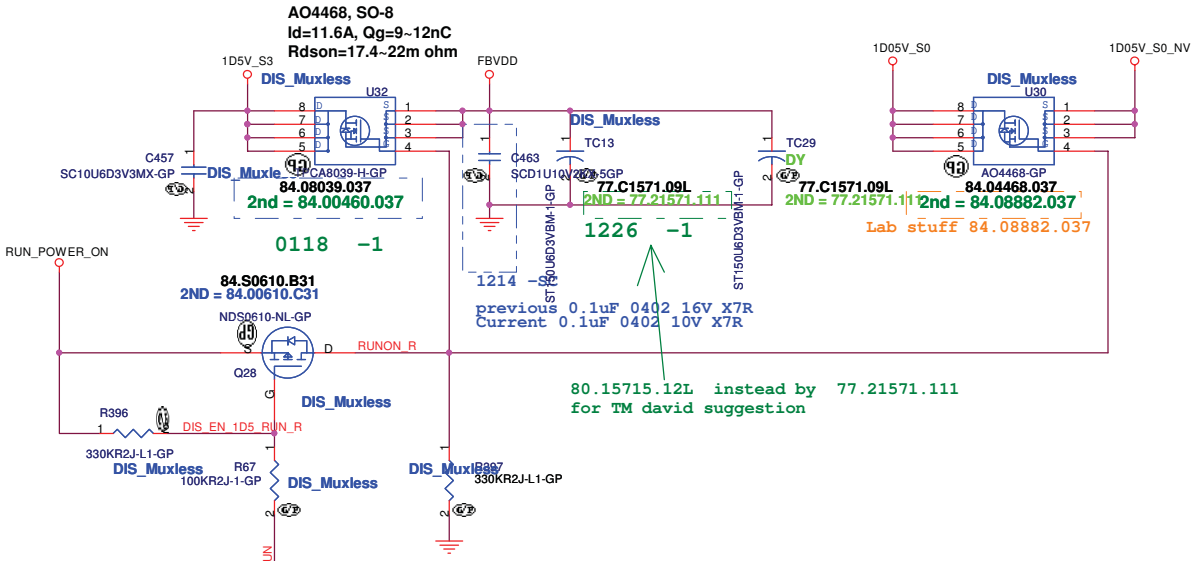
Date: Friday, January 22, 2010	Sheet 59 of 72	

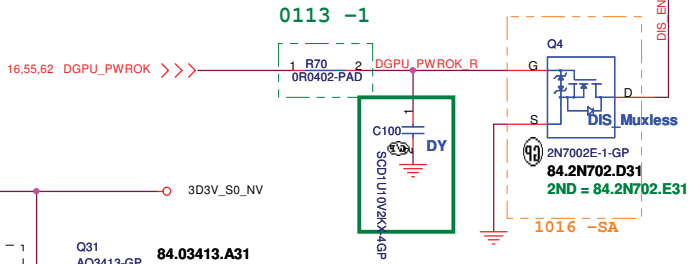
+3VS to 1.8V Transfer

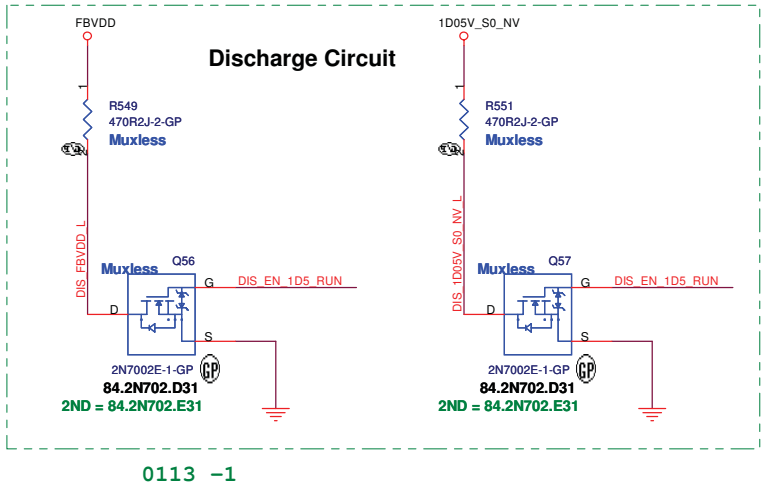


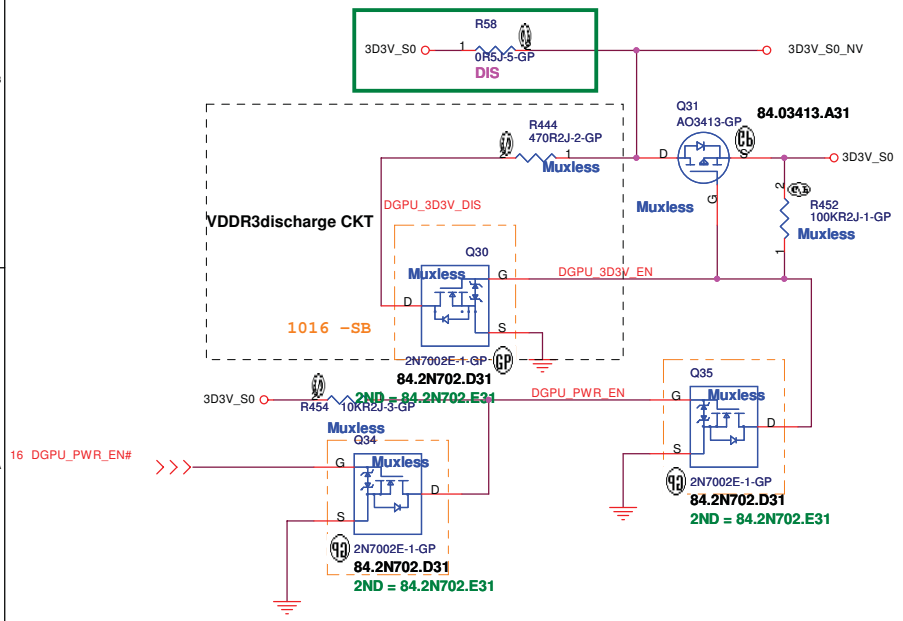
+1.5V to FBVDD Transfer

+1.05V to +1.05V_NV Transfer









UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *NV power*		
Size: A3	Document Number: HM42-CP	Rev: SC
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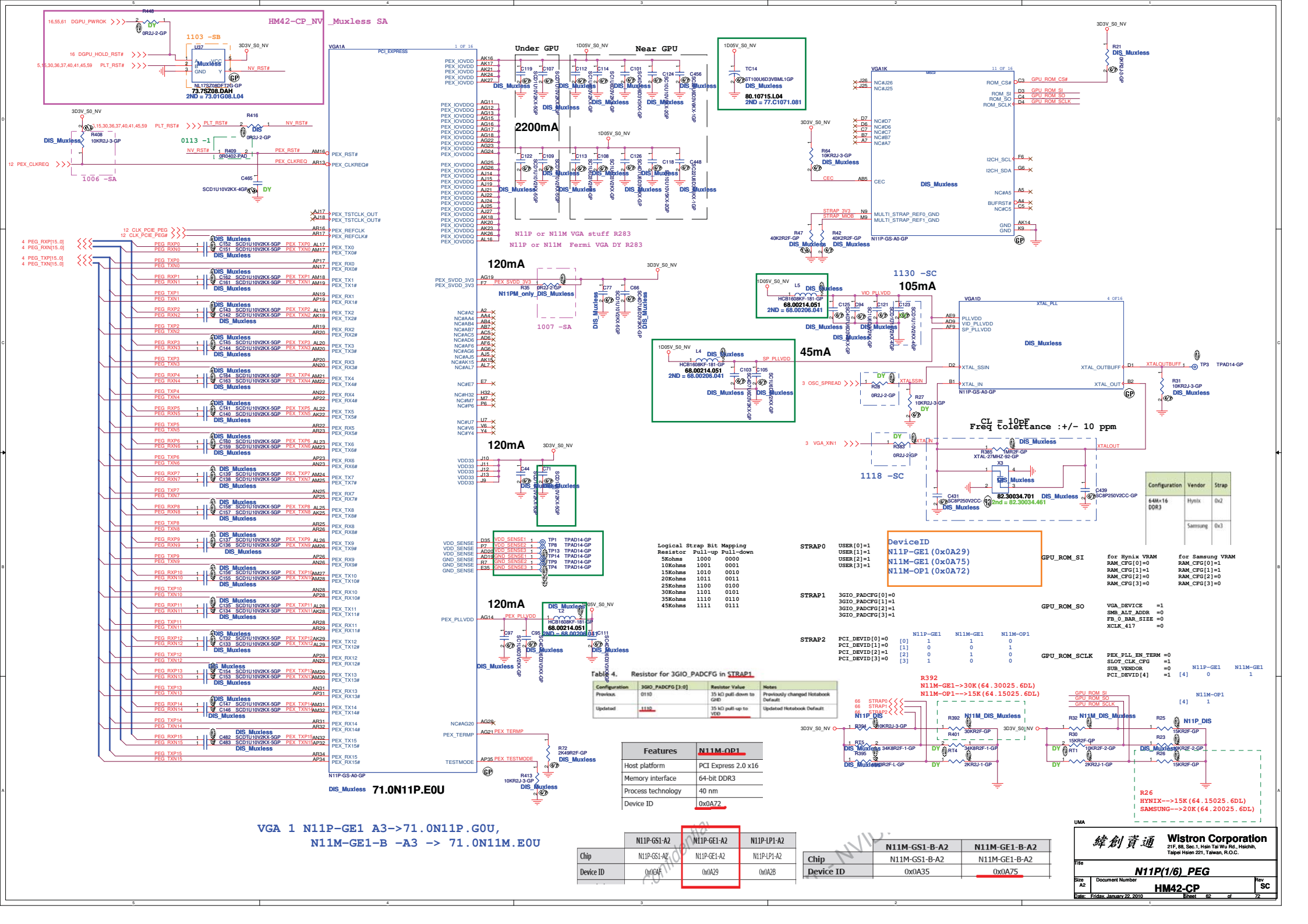
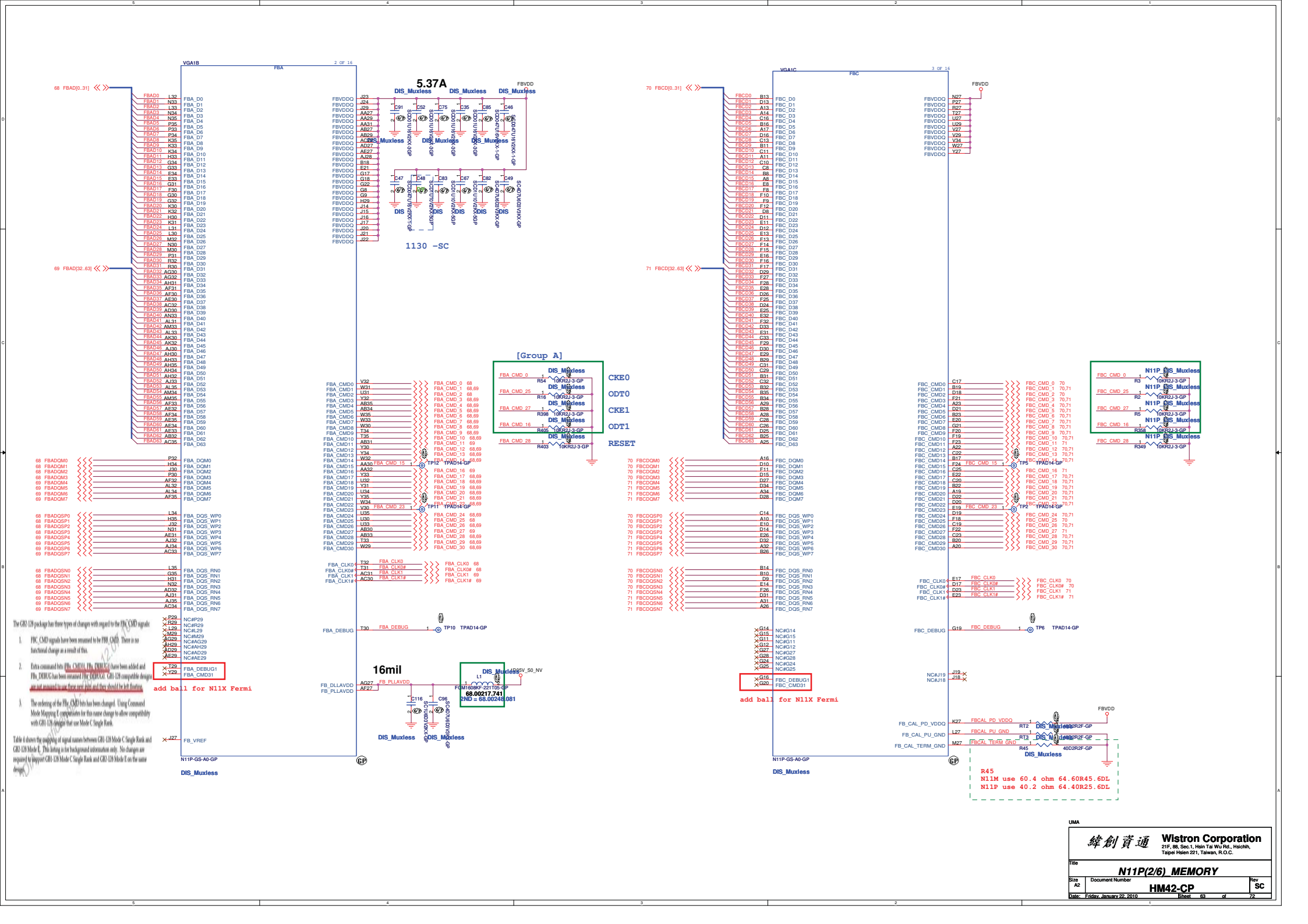

HM42-CP_NV _Muxless SA
1103 -SB
73.7SZ08.DAH
2ND = 73.01G08.L04
1006 -SA
0113 -1
VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
71.0N11P.E0U
Under GPU
Near GPU
2200mA
N11P or N11M VGA stuff R283
N11P or N11M Fermi VGA DY R283
120mA
1007 -SA
45mA
1130 -SC
105mA
1118 -SC
CL = 10pF
Freq tolerance :+/- 10 ppm
DeviceID
N11P-GE1(0x0A29)
N11M-GE1(0x0A75)
N11M-OP1(0x0A72)
R392
N11M-GE1->30K(64.30025.6DL)
N11M-OP1-->15K(64.15025.6DL)
R26
HYNIX-->15K(64.15025.6DL)
SAMSUNG-->20K(64.20025.6DL)
Logical Strap Bit Mapping
Table 4. Resistor for 3GIO_PADCFG in STRAP1
Features
Host platform
Memory interface
Process technology
Device ID
N11M-OP1
PCI Express 2.0 x16
64-bit DDR3
40 nm
0x0A72
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
N11P(1/6)_PEG
HM42-CP
Friday, January 22, 2010



UMA

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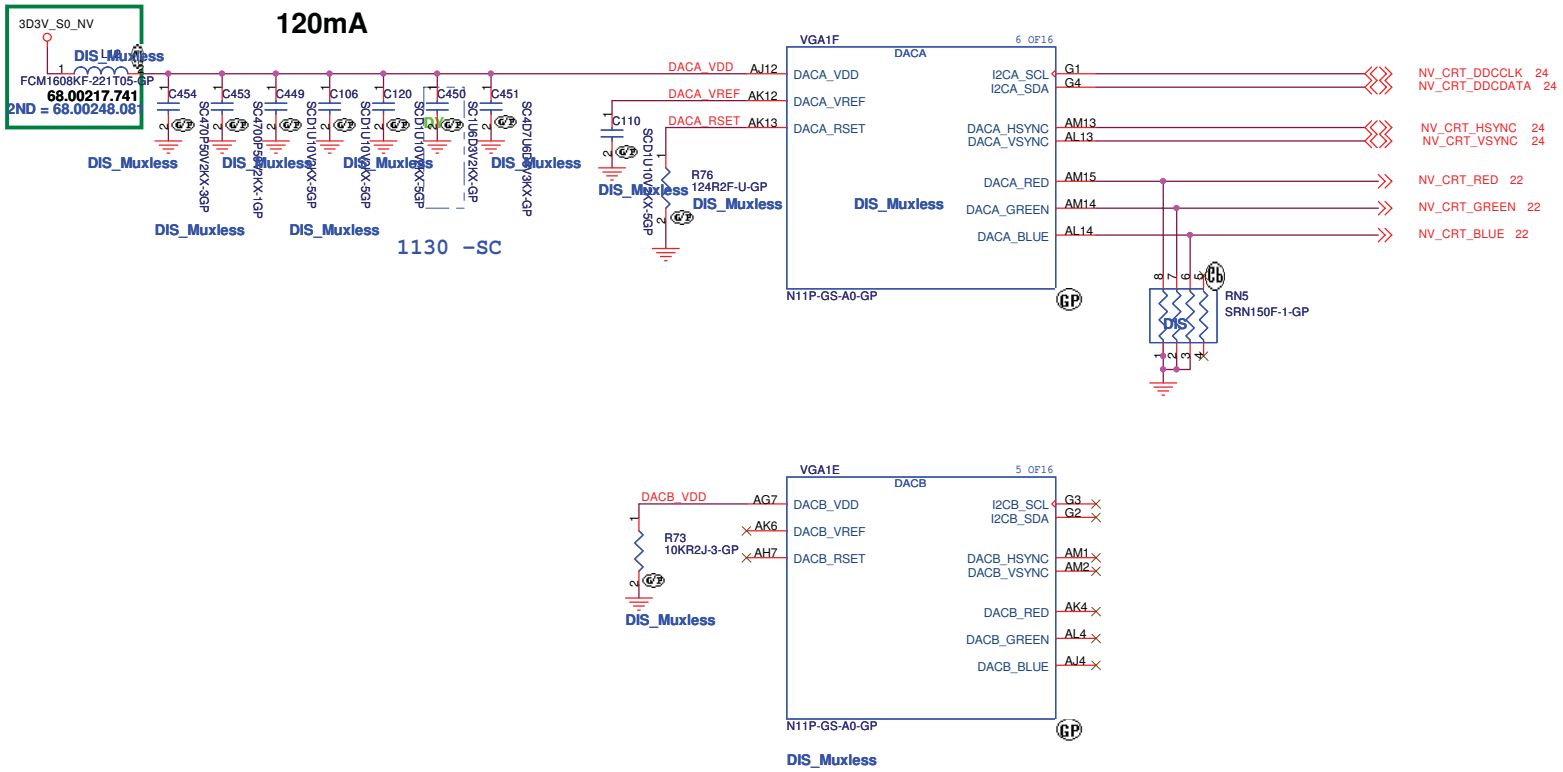
Title: N11P(2/6)_MEMORY

Size: A2 | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 63 of 72



Diserete N11M

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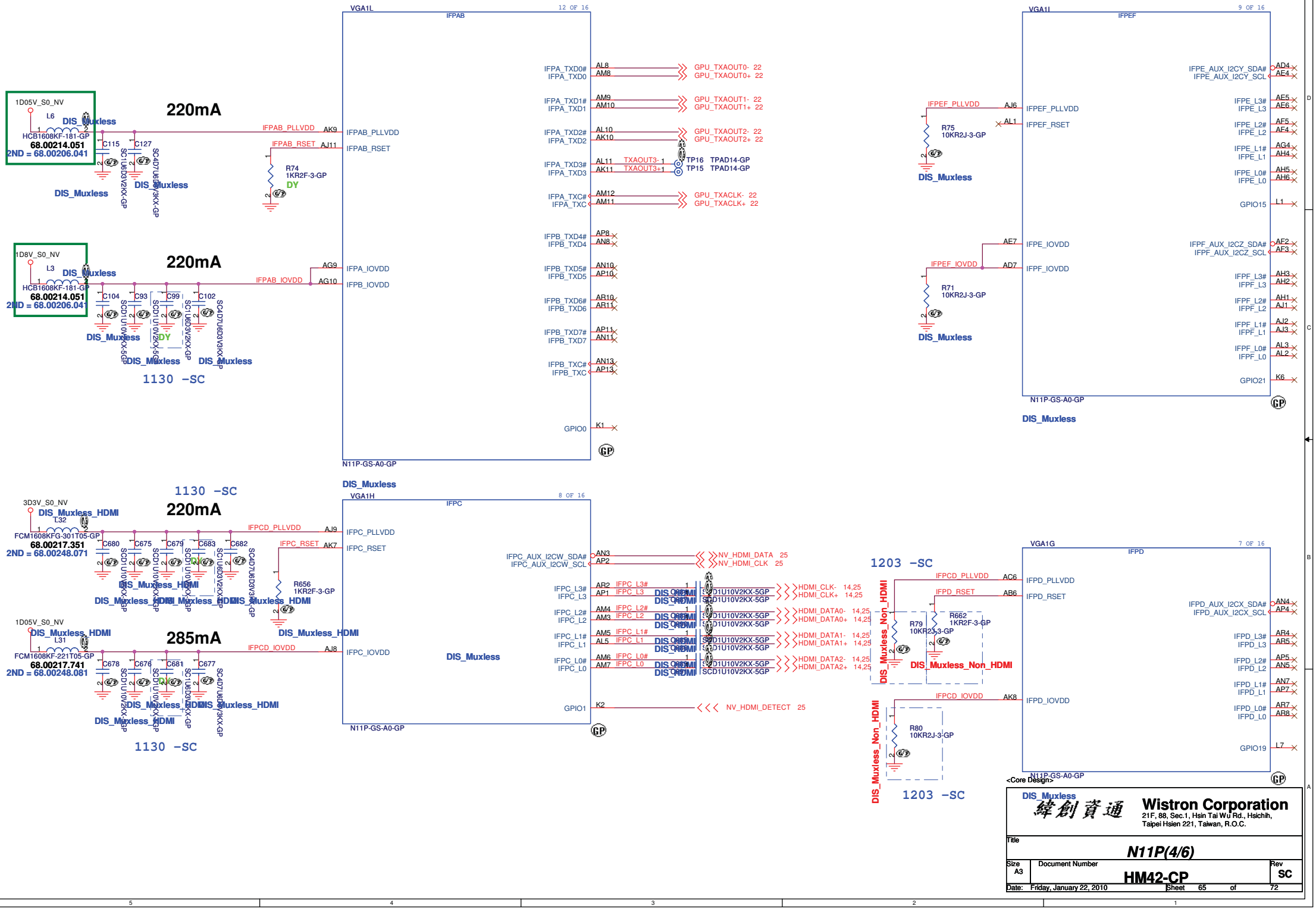
Title: N11P(3/6)_DAC

Size	Document Number	Rev
A3	HM42-CP	SC

Date: Friday, January 22, 2010 Sheet 64 of 72


VGA1L
12 OF 16
IFPAB
N11P-GS-A0-GP
1D05V_S0_NV
L6
HCB1608KF-181-GP
68.00214.051
2ND = 68.00206.041
220mA
DIS_Muxless
IFPAB_PLLVDD
IFPAB_RSET
R74
1KR2F-3-GP
DY
1D8V_S0_NV
L3
IFPAB_IOVDD
IFPA_IOVDD
IFPB_IOVDD
1130 -SC
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPA_TXC#
IFPA_TXC
GPU_TXAOUT0- 22
GPU_TXAOUT0+ 22
GPU_TXAOUT1- 22
GPU_TXAOUT1+ 22
GPU_TXAOUT2- 22
GPU_TXAOUT2+ 22
TXAOUT3-
TXAOUT3+
TP16 TPAD14-GP
TP15 TPAD14-GP
GPU_TXACLK- 22
GPU_TXACLK+ 22
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPB_TXC#
IFPB_TXC
GPIO0
VGA1I
9 OF 16
IFPEF
N11P-GS-A0-GP
IFPEF_PLLVDD
IFPEF_RSET
R75
10KR2J-3-GP
IFPEF_IOVDD
R71
10KR2J-3-GP
IFPE_IOVDD
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
GPIO15
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
GPIO21
VGA1H
8 OF 16
IFPC
N11P-GS-A0-GP
3D3V_S0_NV
DIS_Muxless_HDMI
L32
FCM1608KFG-301T05-GP
68.00217.351
2ND = 68.00248.071
220mA
IFPCD_PLLVDD
IFPC_PLLVDD
IFPC_RSET
R656
1KR2F-3-GP
1D05V_S0_NV
L31
FCM1608KF-221T05-GP
68.00217.741
2ND = 68.00248.081
285mA
IFPCD_IOVDD
IFPC_IOVDD
1130 -SC
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
NV_HDMI_DATA 25
NV_HDMI_CLK 25
IFPC_L3#
IFPC_L3
IFPC_L2#
IFPC_L2
IFPC_L1#
IFPC_L1
IFPC_L0#
IFPC_L0
HDMI_CLK- 14,25
HDMI_CLK+ 14,25
HDMI_DATA0- 14,25
HDMI_DATA0+ 14,25
HDMI_DATA1- 14,25
HDMI_DATA1+ 14,25
HDMI_DATA2- 14,25
HDMI_DATA2+ 14,25
GPIO1
NV_HDMI_DETECT 25
1203 -SC
DIS_Muxless_Non_HDMI
R79
10KR2J-3-GP
R662
1KR2F-3-GP
R80
10KR2J-3-GP
VGA1G
7 OF 16
IFPD
N11P-GS-A0-GP
IFPCD_PLLVDD
IFPD_PLLVDD
IFPD_RSET
IFPCD_IOVDD
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
IFPD_L3#
IFPD_L3
IFPD_L2#
IFPD_L2
IFPD_L1#
IFPD_L1
IFPD_L0#
IFPD_L0
GPIO19
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
N11P(4/6)
Size A3
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120mA

3D3V_S0_NV

N11PM_only_DIS_Muxless

R57 0R3J-0-U-GP

R59 0R3J-0-U-GP N11PM_Fermi_DIS_Muxless

1006 -SA

N11P or N11M VGA stuff R277

N11P or N11M Fermi VGA stuff R282

C84 SCD1U10V2KX-4GP N11PM_only_DIS_Muxless

VGA1O MIOA 15 OF 16

MIOA_B_VDDQ

P9 MIOA_VDDQ
R9 MIOA_VDDQ
T9 MIOA_VDDQ
U9 MIOA_VDDQ

U5 MIOA_CAL_PD_VDDQ
T5 MIOA_CAL_PU_GND
N5 MIOA_VREF

MIOA_D0 N1
MIOA_D1 P4
MIOA_D2 P1
MIOA_D3 P2
MIOA_D4 P3
MIOA_D5 T3
MIOA_D6 T2
MIOA_D7 T1
MIOA_D8 U4
MIOA_D9 U1
MIOA_D10 U2
MIOA_D11 U3
MIOA_D12 R6
MIOA_D13 T6
MIOA_D14 N6

MIOA_CTL3 P5
MIOA_HSYNC N3
MIOA_VSYNC L3
MIOA_DE N2

MIOA_CLKOUT R4
MIOA_CLKOUT# T4
MIOA_CLKIN N4

N11P-GS-A0-GP

DIS_Muxless

MIOA_CLKIN

R46 10KR2J-3-GP N11PM_only_DIS_Muxless

120mA

VGA1P MIOB 16 OF 16

AA9 MIOB_VDDQ
AB9 MIOB_VDDQ
W9 MIOB_VDDQ
Y9 MIOB_VDDQ

AA7 MIOB_CAL_PD_VDDQ
AA6 MIOB_CAL_PU_GND
AF1 MIOB_VREF

MIOB_D0 Y1
MIOB_D1 Y2
MIOB_D2 Y3
MIOB_D3 AB3
MIOB_D4 AB2
MIOB_D5 AB1
MIOB_D6 AC4
MIOB_D7 AC1
MIOB_D8 AC2
MIOB_D9 AC3
MIOB_D10 AE3
MIOB_D11 AE2
MIOB_D12 U6
MIOB_D13 W6
MIOB_D14 Y6

STRAP0 W5
STRAP1 W7
STRAP2 V7

STRAP0 62
STRAP1 62
STRAP2 62

MIOB_CTL3 W3
MIOB_HSYNC W1
MIOB_VSYNC W2
MIOB_DE Y5

MIOB_CLKOUT V4
MIOB_CLKOUT# W4
MIOB_CLKIN AE1

N11P-GS-A0-GP

DIS_Muxless

MIOB_CLKIN

R69 10KR2J-3-GP N11PM_only_DIS_Muxless

VGA1J MISC1 10 OF 16

B4 THERMDN
B5 THERMDP

I2CS_SCL E2 SMBC_N11PM
I2CS_SDA E1 SMBD_N11PM
I2CC_SCL E3 NV_LCD_EDID_CLK 22
I2CC_SDA E4 NV_LCD_EDID_DAT 22
NC#F4
NC#G5
NC#D5
NC#E5

GPIO2 K3
GPIO3 H3 NV_LCDVDD_ON 23
GPIO4 H2 NV_BLON_IN 22
GPIO5 H1 NVVDD_ALTV0 NVVDD_ALTV0 55
GPIO6 H4 NVVDD_ALTV1 NVVDD_ALTV1 55
GPIO7 H5
GPIO8 H6 NV_GPIO8
GPIO9 J7 NV_GPIO9
GPIO10 K4 MEM_VREF_CTRL
GPIO11 K5
GPIO12 H7
GPIO13 J4
GPIO14 J6

GPIO16 L2
GPIO17 L4
GPIO18 M4
GPIO20 L5
GPIO22 L6
GPIO23 M6

TP7 TPAD14-GP

JTAG_TCK AP14
JTAG_TMS AR14
JTAG_TDI AN14
JTAG_TDO AN16
JTAG_TRST# AP16

DIS_Muxless

N11P-GS-A0-GP

TPAD14-GP TP74 JTAG_TCK
TPAD14-GP TP75 JTAG_TRST#

RN68 SRN10KJ-5-GP DIS_Muxless

1202 -SC

HM42-CP NV Muxless SA 0916

3D3V_S0_NV

RN1 SRN4K7J-8-GP Muxless

SMBC_N11PM
SMBD_N11PM

1105 -SC

Q1 Muxless

SMBC_N11PM SMBC_THERM SMBC_THERM 39,40
39,40 SMBD_THERM SMBD_THERM SMBD_N11PM

2N7002KDW-GP

84.2N702.A3F 2ND = 84.DM601.03F

DIS R9 0R2J-2-GP SMBC_THERM SMBC_N11PM

DIS R22 0R2J-2-GP SMBD_THERM SMBD_N11PM

HM42-CP NV Muxless SA 0923

RN70 SRN10KJ-5-GP DIS_Muxless

NV_GPIO8
NV_GPIO9
3D3V_S0_NV

1202 -SC

UMA

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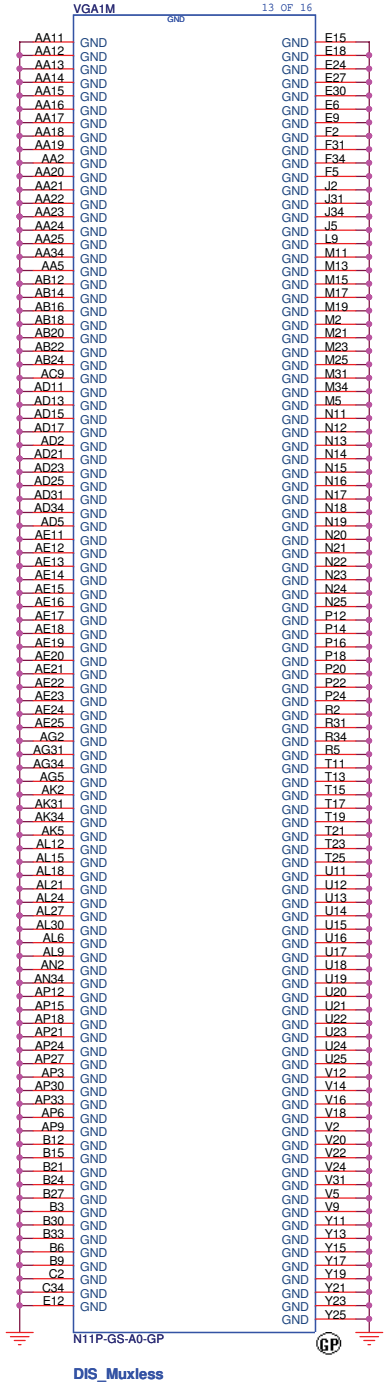
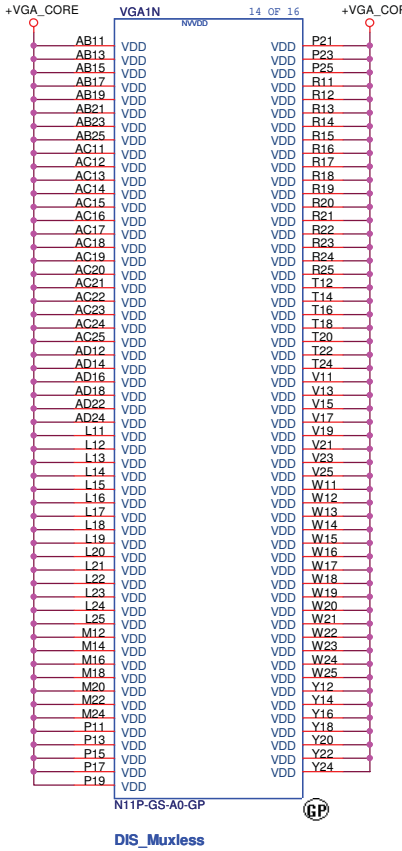
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

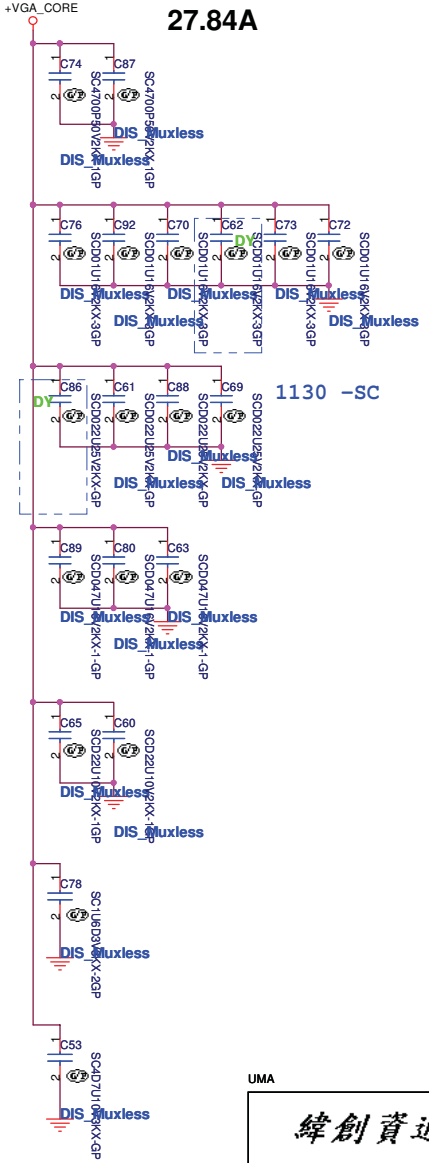
Title: N11P(5/6)_MIO/ GPIO

Size: A3 | Document Number: HM42-CP | Rev: SC

Date: Friday, January 22, 2010 | Sheet 66 of 72







UMA

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: *N11P(6/6)_POWER*

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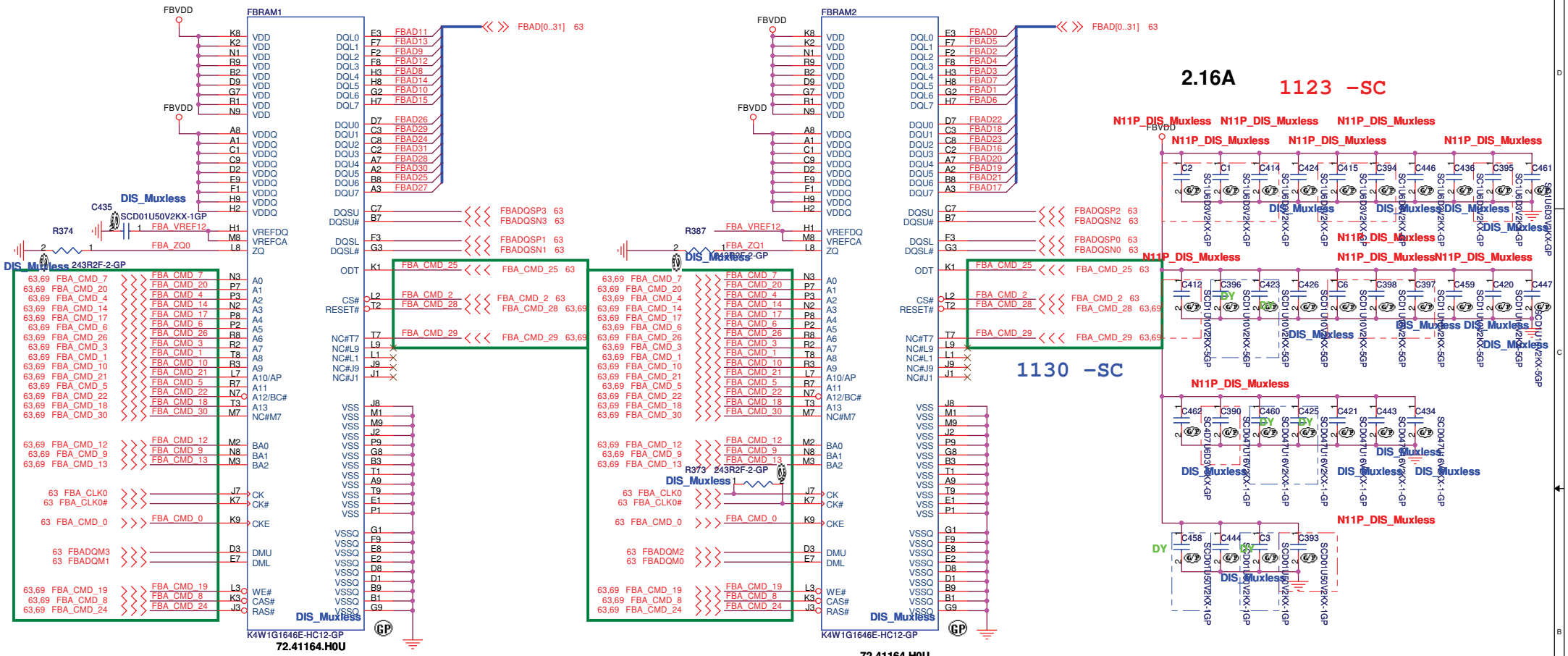
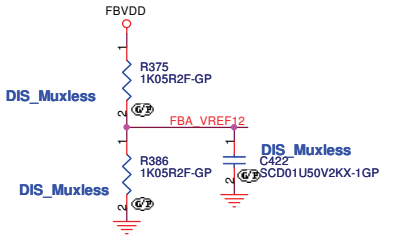
DDR3



SAMSUNG: 72.41164.H0U(Use OEM PN:VR.1GB0B.006)
HYNIX: 72.51G63.C0U(Use OEM PN: VR.1GB0G.004)



UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: VRAM(1/4)		
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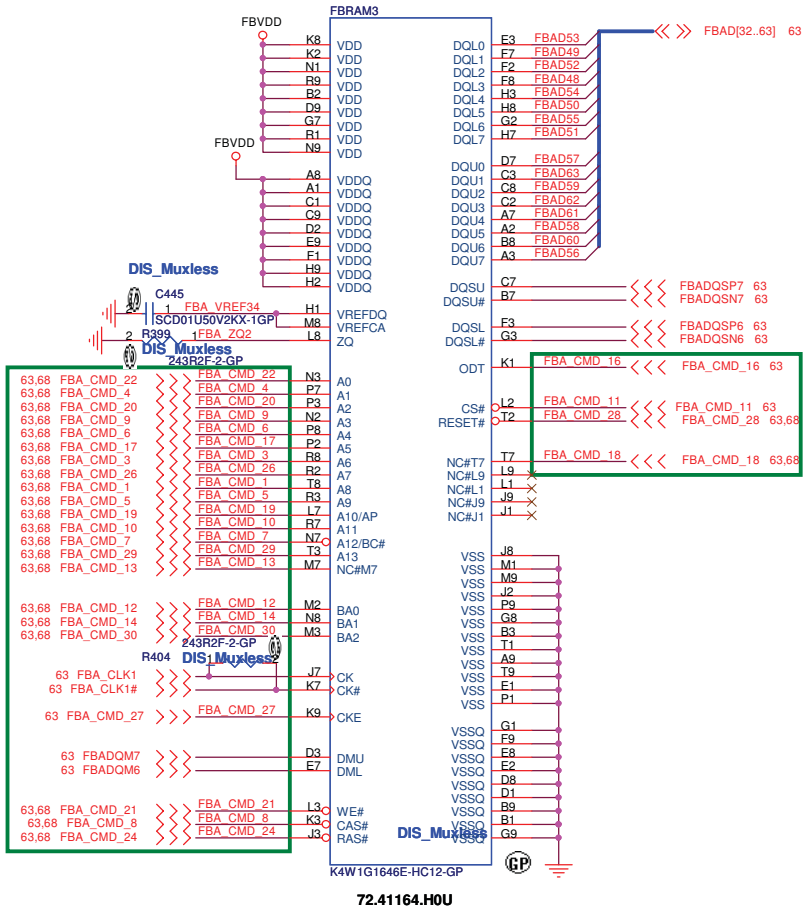
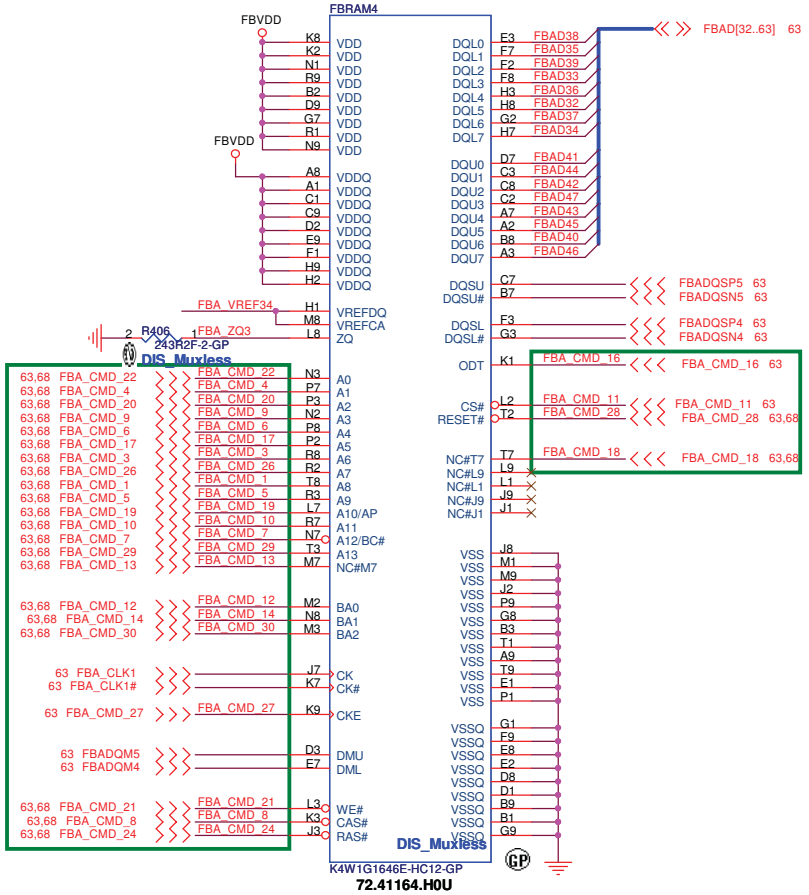
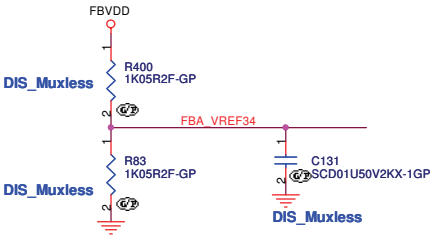
DDR3







SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U

HM42-CP

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *VRAM(2/4)*		
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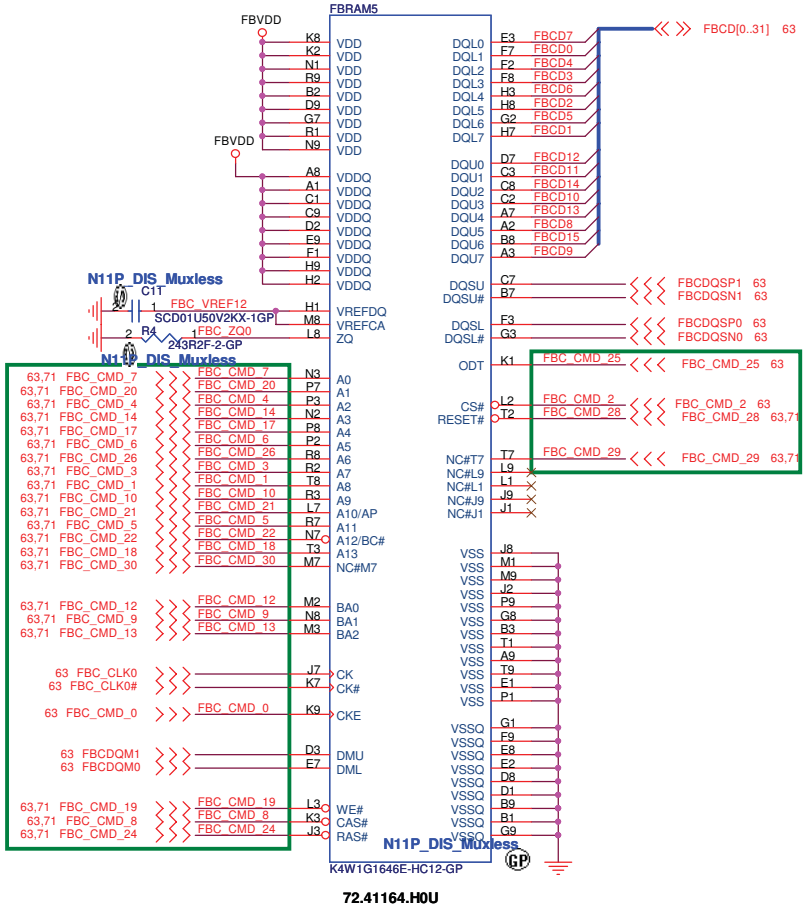
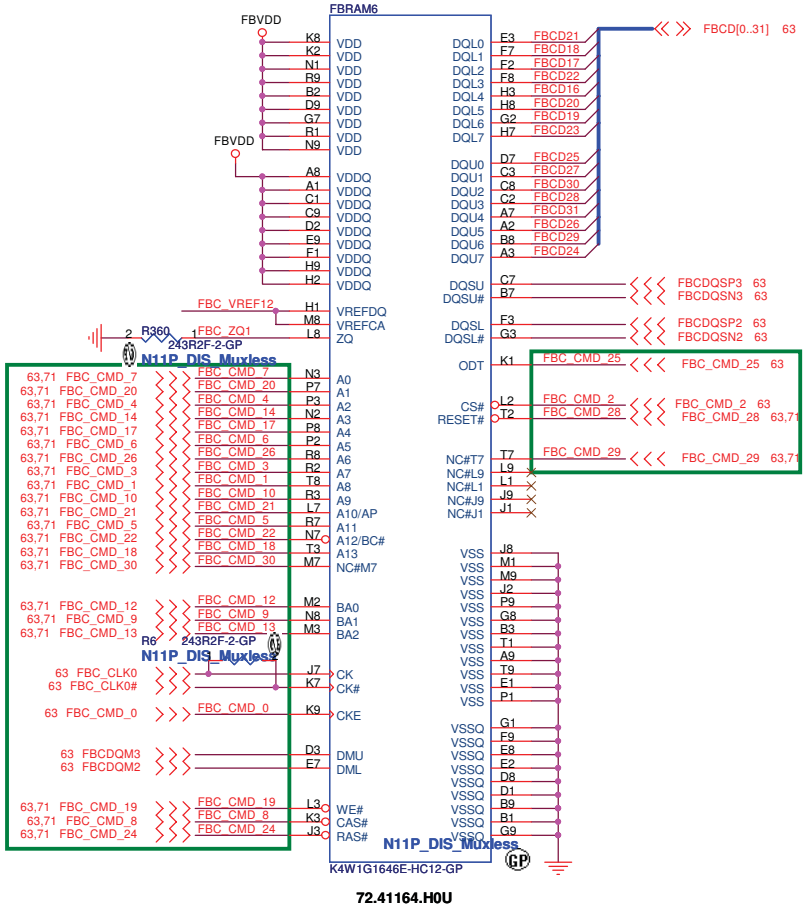
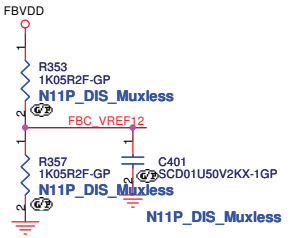
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



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Title	VRAM(3/4)	
Size A3	Document Number HM42-CP	Rev SC
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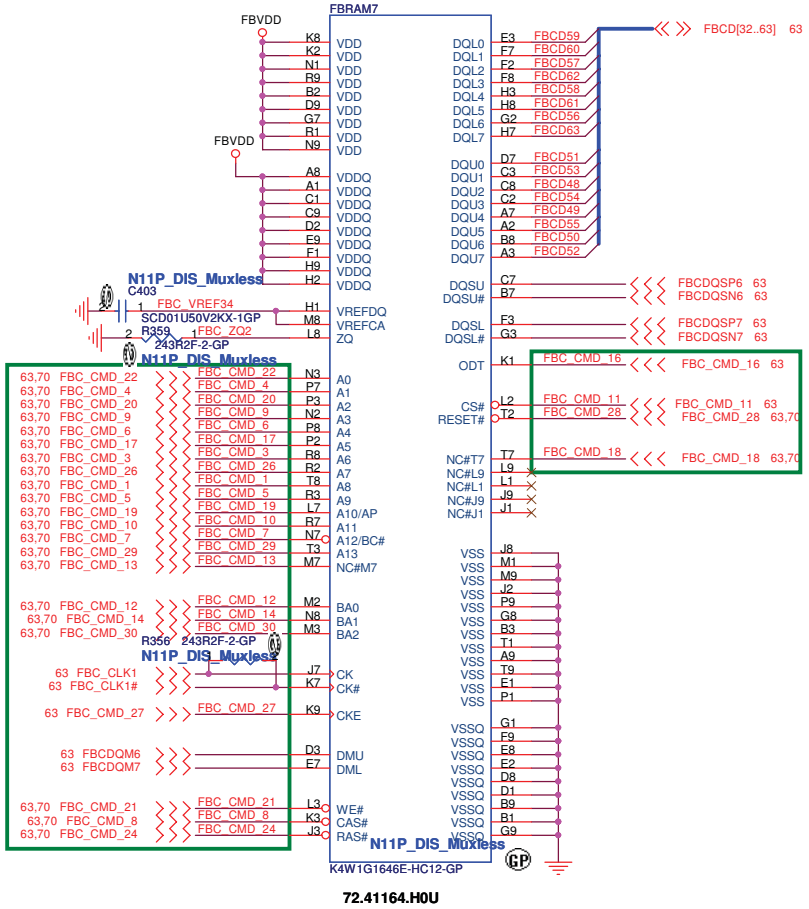
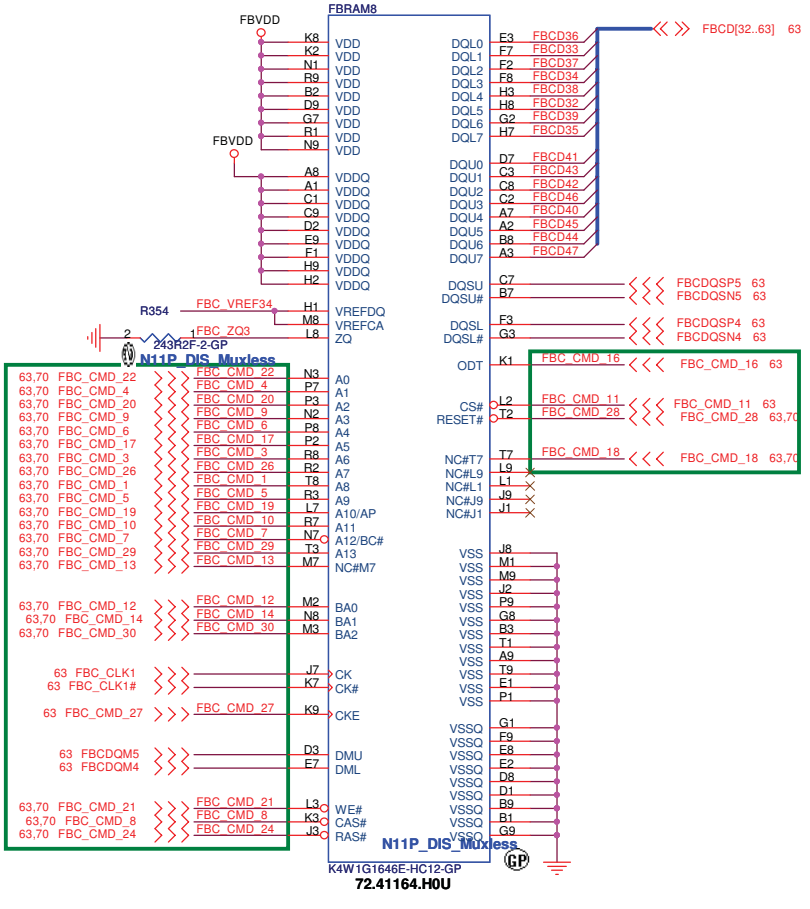
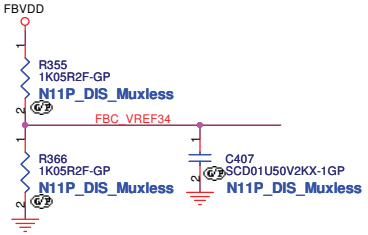
DDR3





SAMSUNG: 72.41164.H0U
HYNIX: 72.51G63.C0U



UMA

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM(4/4)***

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3) Samsung VRAM FBRAM1~8 PN:VR.1GB0B.006
Hynix VRAM FBRAM1~8 PN:VR.1GB0G.004

4) VGA 1 N11P-GE1 A3->71.0N11P.G0U,
N11M-GE1-B -A3 -> 71.0N11M.E0U
N11M-OP1 ->

6) VGA 1 N11P-GE1-> R53 49.9K(64.49925.6DL)
N11M-GE1 -> R53 32.4K(64.32425.6DL)

7) R26 stuff Hynix VRAM : 15K(64.15025.6DL)
Samsung VRAM : 20K(64.20025.6DL)

8) R45 stuff N11M use 60.4 ohm (64.32425.6DL)
N11P use 40.2 ohm (64.40R25.6DL)

9) Muxless SKU stuff R181 2.37K (64.23715.6DL)
UMA SKU Stuff R181 2.4K (64.24015.6DL)

10) N11M OP1 ->R392 15K(64.15025.6DL)
N11M GE1 ->R392 30K(64.30025.6DL)

Mini Card 2nd and 3rd source PN confirm

Card Reader 2nd source confrim

[ECR]

Date	released by	ECR Number
11/22	Anita	R1001240

[lab -SB]

2nd -> UMA (S01G)

1st -> Diserete N11P Hynix(S02G)
1st +3rd -> Diserete N11M Hynix(S03G)
2nd +4th -> Diserete N11M Samsung(S04G)
1st -> Diserete N11P Samsung (S05G)

2nd -> N11M Hynix_support Optimus (S06G)

[Eng -SC]

2nd -> UMA Non 3G (55.4GY01.S07G)

1st -> Diserete N11P Hynix_3G(55.4GZ01.S03G)
1st +3rd -> Diserete N11M Hynix_3G(55.4GY01.S09G)
2nd +4th -> Diserete N11M Samsung_Non 3G(55.4GZ01.S02G)
1st + 5th -> Diserete N11P Samsung _3G(55.4GY01.S10G)

1st +3 rd -> UMA Non 3G Non HDMI (55.4GW01.S01G)

[PD -1]

UMA 3G (55.4GY01.M01G)
Diserete N11P Hynix_3G(55.4GY01.M02G) => 1st
Diserete N11P Hynix_Non 3G(55.4GY01.M03G) => 2nd
UMA Non 3G (55.4GY01.M04G)
Diserete N11M Hynix_3G(55.4GY01.M05G)
Diserete N11P Samsung _3G(55.4GY01.M06G) =>1 st
Diserete N11M Samsung_Non 3G(55.4GY01.M07G)

[PD action]

qual TPCN1 2nd source(20.K0296.006)
qual KB1 2nd source(20.K0382.026)

qual HDMI 2nd and 3rd

qual ODD1 3rd source(62.10065.E01)

qual PWRCN1 2nd and 3rd
qual RTC1 4th source
qual BT1 2nd and 3 source

[Old]
PCH1 PN : 71.0IBEX.A0U
[New]
PCH1 PN : 71.0HM55.00U(KI.G5501.002)

qual U51 and U15 2nd source
qual TC13 2nd source(77.21571.111)
qual U32 2nd source
Qual HS1,HS2 2nd: 34.4B417.401

UMA

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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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