Compal Confidential

NAL90/NALG0 M/B Schematics Document

Intel Auburndale/Clarksfield Processor with DDRIII + Ibex Peak-M

2009-10-20

REV:1.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date 2010/04/15	Title: Cover Page
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			Date: Friday, October 23, 2009; Sheet 1 of 60

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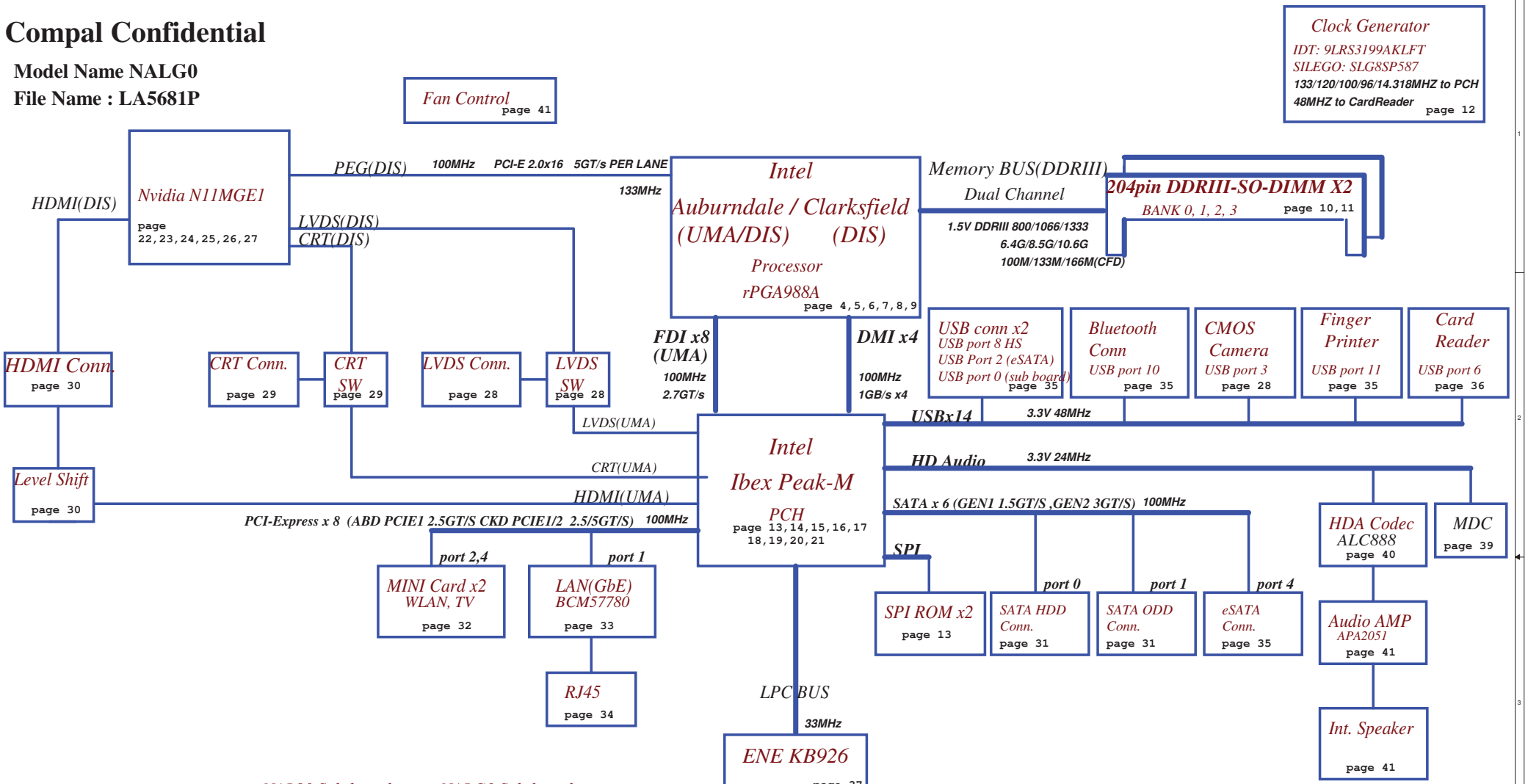
Model Name NALG0
File Name : LA5681P



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Compal Electronics, Inc.			
Title: Block Diagrams			
Size: B	Document Number: NALG0 M/B LA-5681P Schematic		Rev: 1.0
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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	ON	OFF
+GFX_core	Core voltage for CPU	ON	OFF	OFF
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF
+VGA_CORE	Core voltage for N11M VGA	ON	OFF	OFF
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF
+1.5VS	1.5V power rail for DDRIII	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
PCH	
VGA	

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
Mini card	

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA only	UMA only@
DIS	DIS@
DIS Only	DIS only@
Switchable	SG@
	XDP@
	NonSG@
	MINI2@
	FP@
	eDriver@
	Dmic@
	Caps@
	X76@
	HDCP@
	AMIC@
S3 power	S3@
	non S3@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	Ext4 HS USB
		1	sub Board
	UHCI1	2	
		3	Camera
	UHCI2	4	1st Min-Card
		5	2st Min-Card
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Ext4 HS USB
		9	Card Reader
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	
		13	

BOM Config
UMA only
UMA@/UMA only@/FP@/Dmic@/XDP@/S3@

DIS ONLY
DIS@/DIS only@/FP@/Dmic@/XDP@/S3@

Switchable Graphics
SG@/UMA@/DIS@/FP@/Dmic@/XDP@/S3@

Note:do cost BOM add X76@

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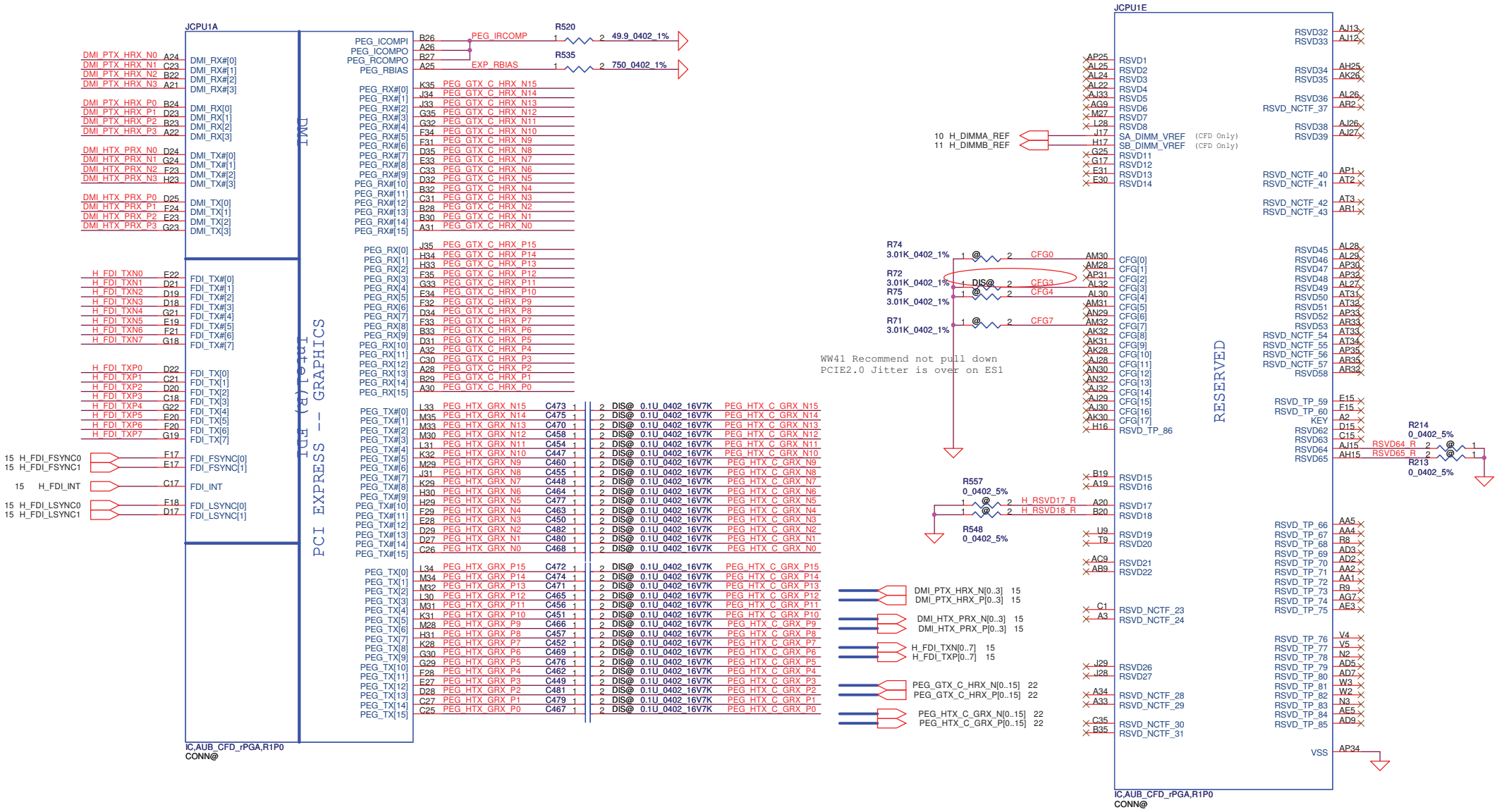
Title	Notes List		
Size B	Document Number NALG0 M/B LA-5681P Schematic		Rev 1.0
Date: Friday, October 23, 2009	Sheet 3 of 60		



eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 – PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 – PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 – Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

CheckList0.8 1.22
Auburndale Graphics Disable

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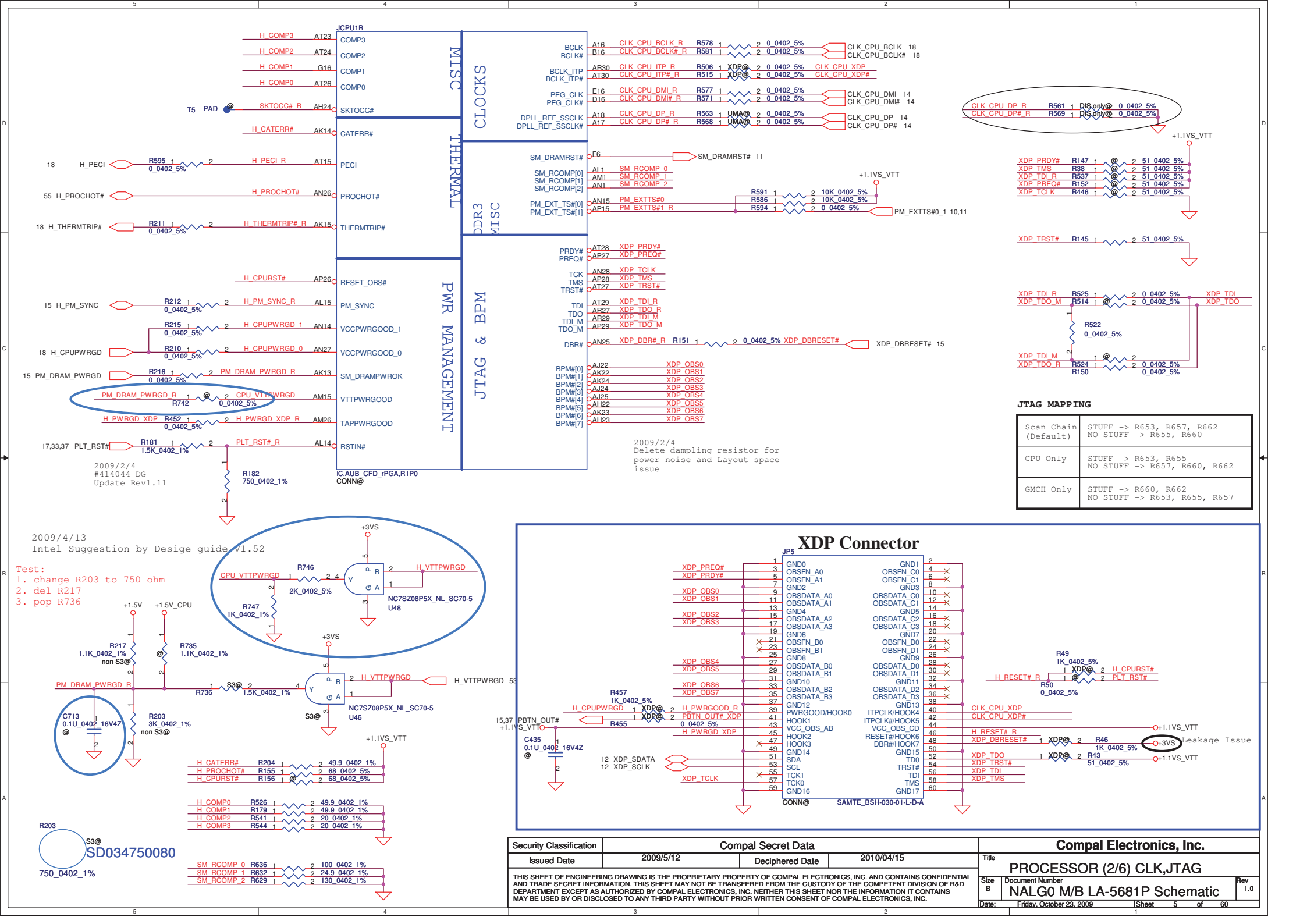
Title: PROCESSOR (1/6) DMI,FDI,PEG

Size	Document Number	Rev
B	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 Sheet 4 of 60



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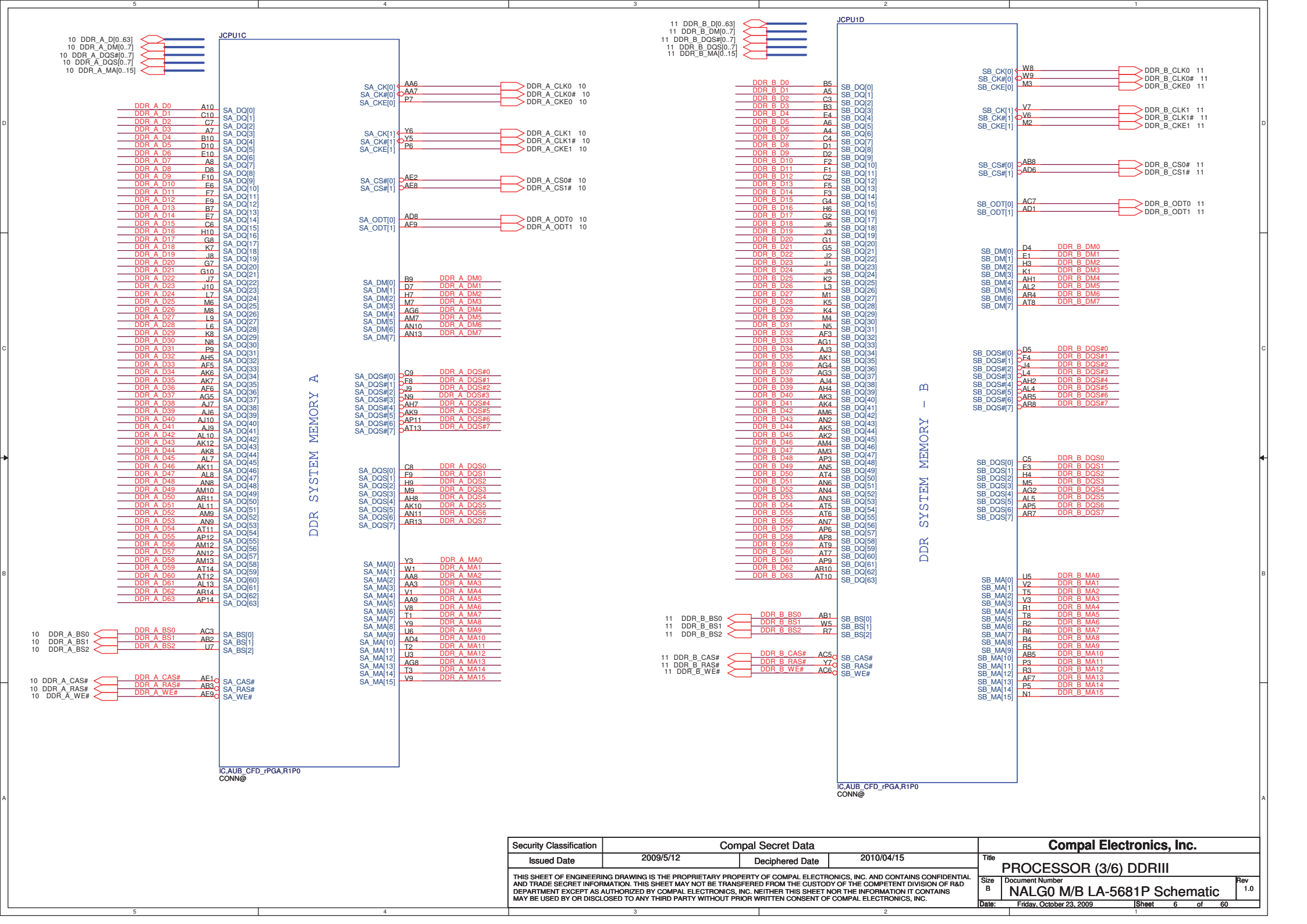
Compal Electronics, Inc.

Title: PROCESSOR (2/6) CLK,JTAG

Size	Document Number	Rev
B	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 Sheet 5 of 60



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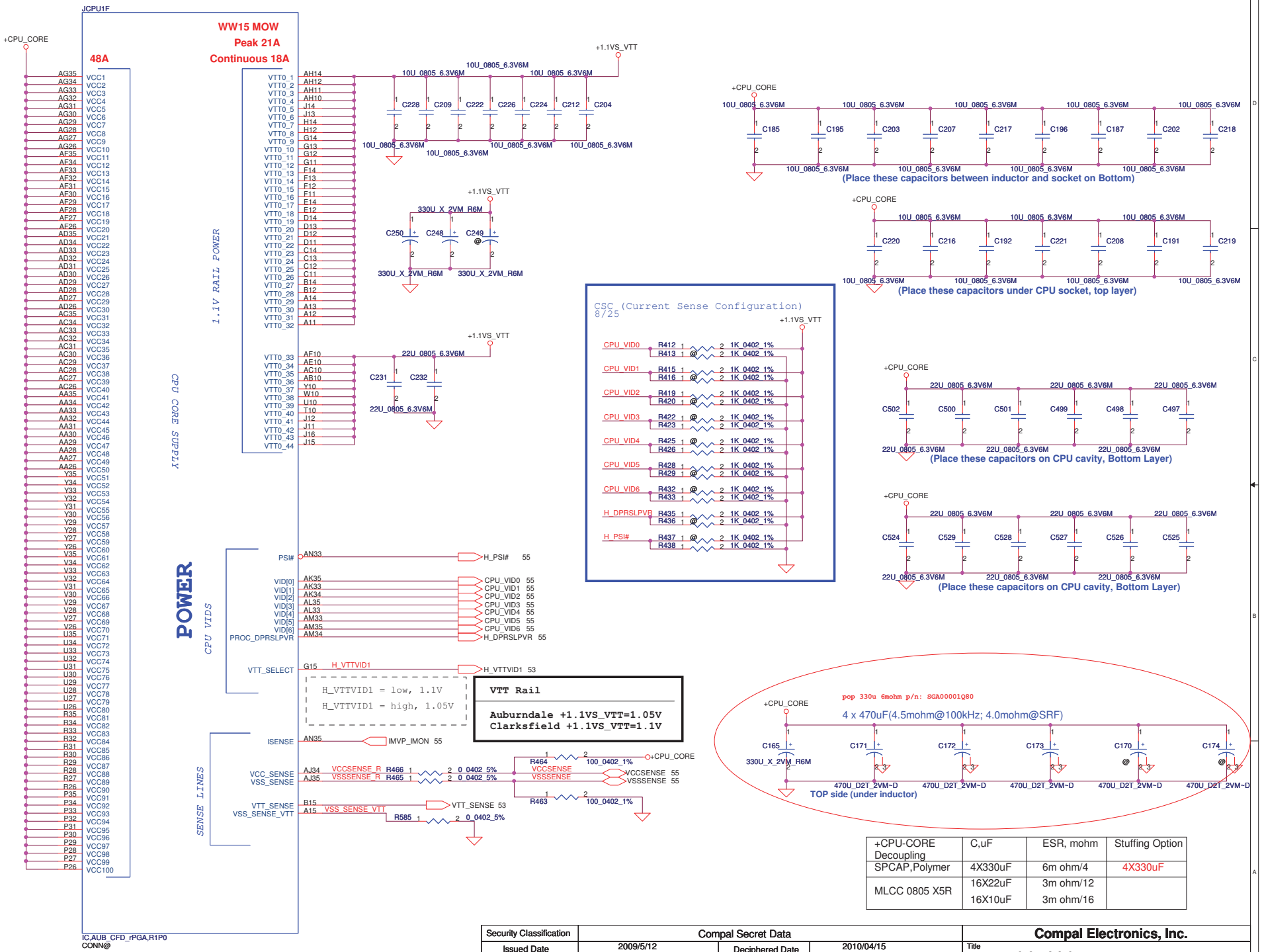
Title: PROCESSOR (3/6) DDRIII

Size	Document Number	Rev
B	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 Sheet 6 of 60



+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	4X330uF
MLCC 0805 X5R	16X22uF	3m ohm/12	
	16X10uF	3m ohm/16	

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Title: PROCESSOR (4/6) PWR,Bypass

Size: B(28 Custom) | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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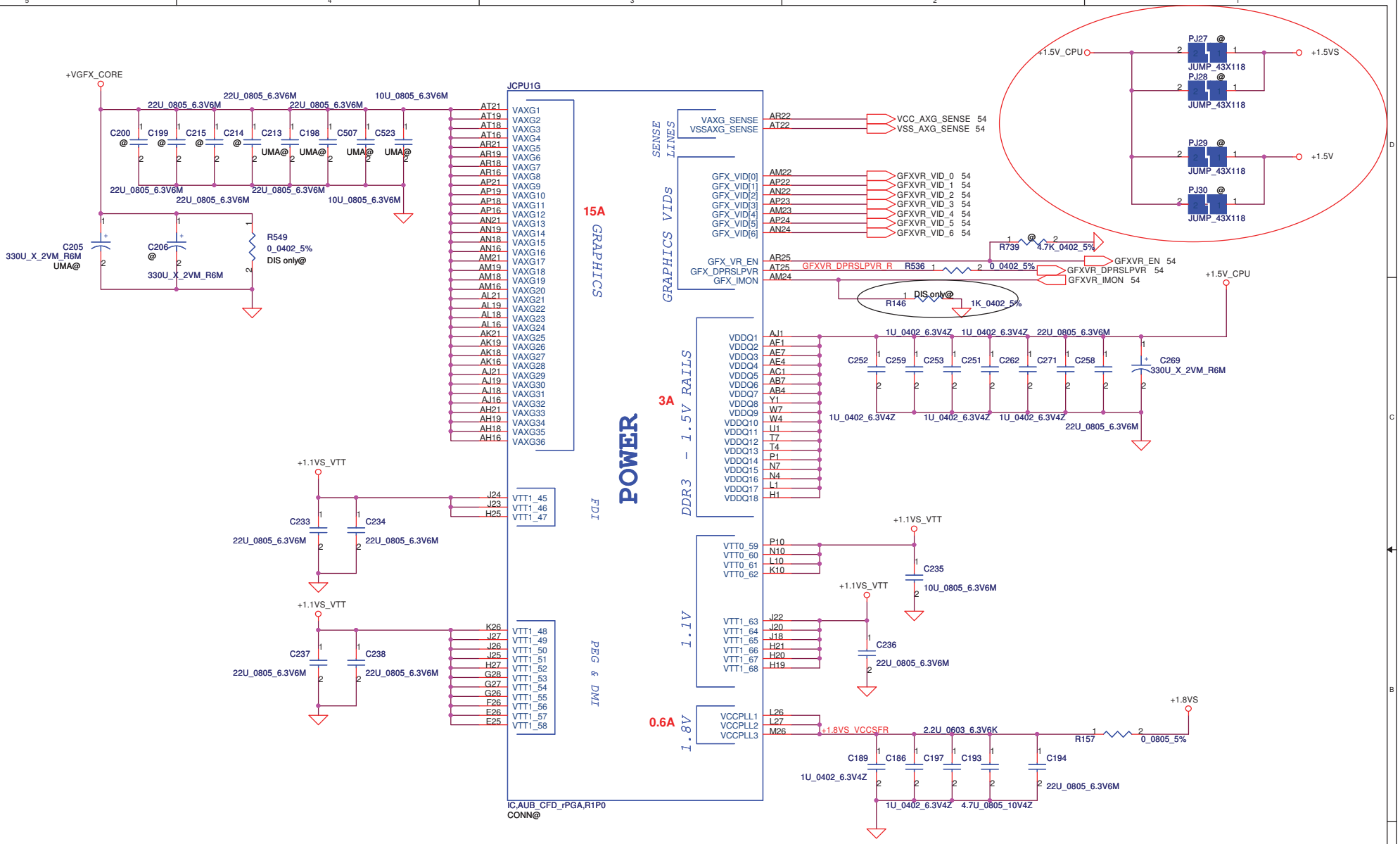

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Title: PROCESSOR (5/6) PWR

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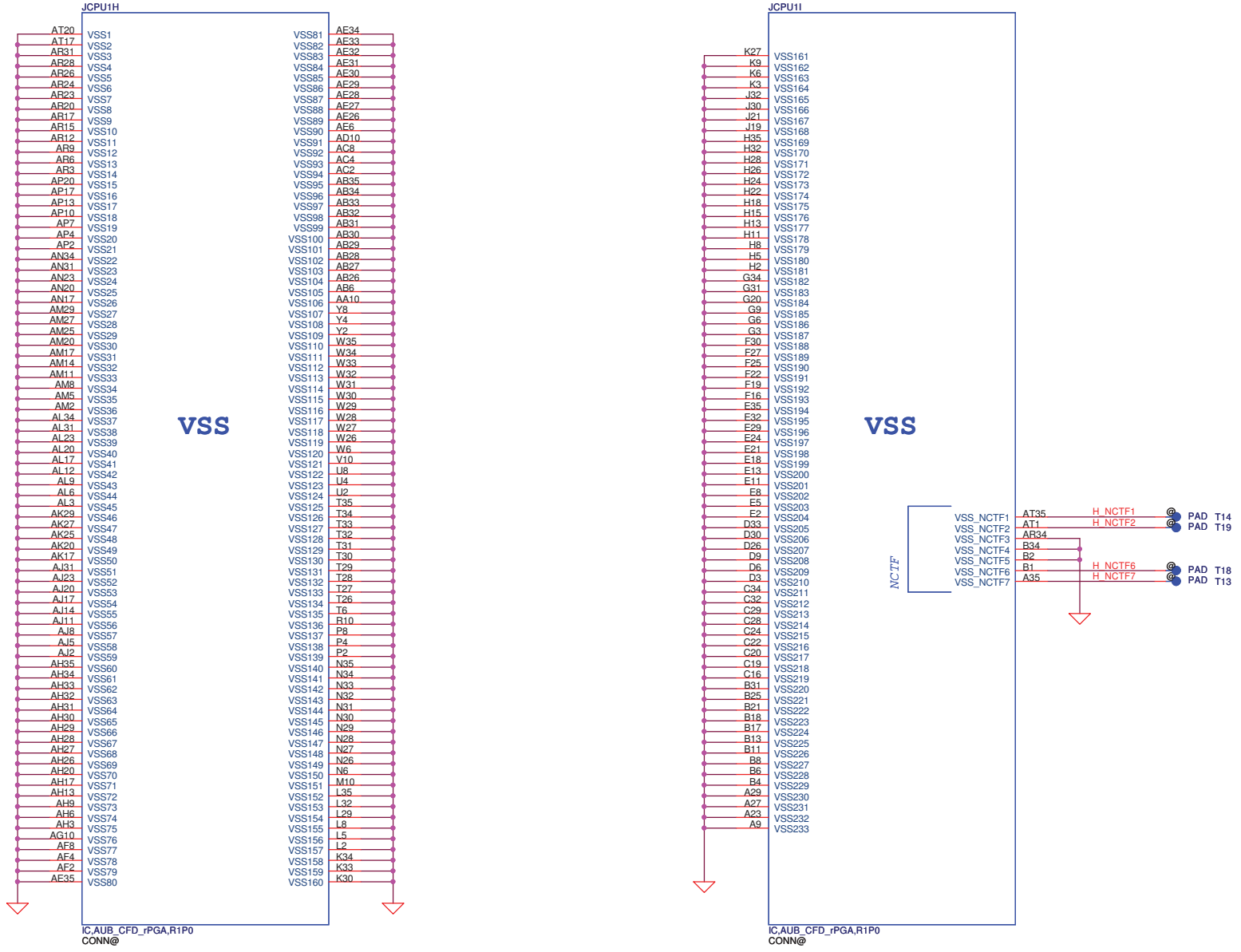

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Compal Electronics, Inc.

Title: PROCESSOR (6/6) VSS

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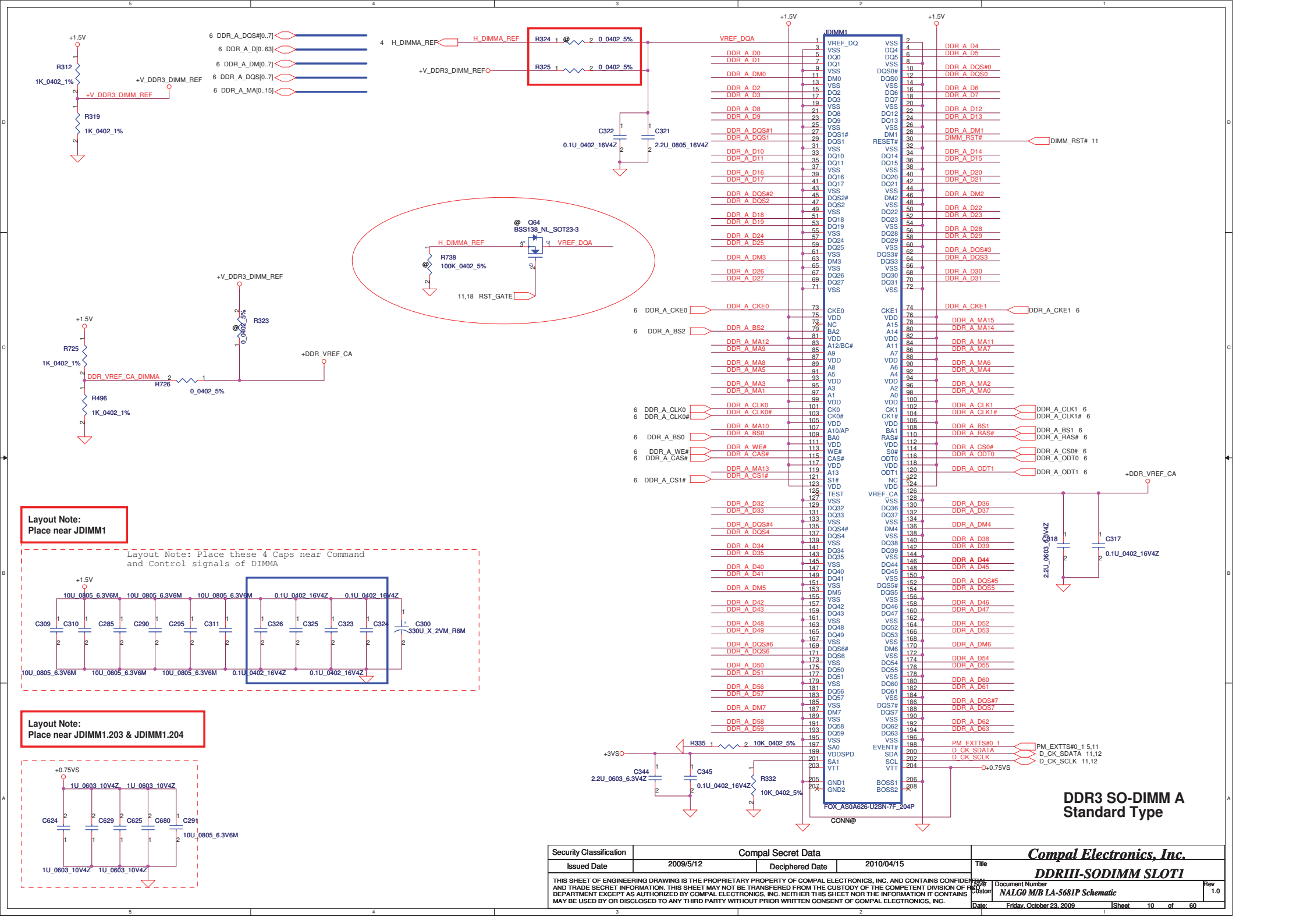

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Title	*Compal Electronics, Inc.*		
	DDRIII-SODIMM SLOT1		
Size: Custom	Document Number: *NALG0 M/B LA-5681P Schematic*		Rev: 1.0
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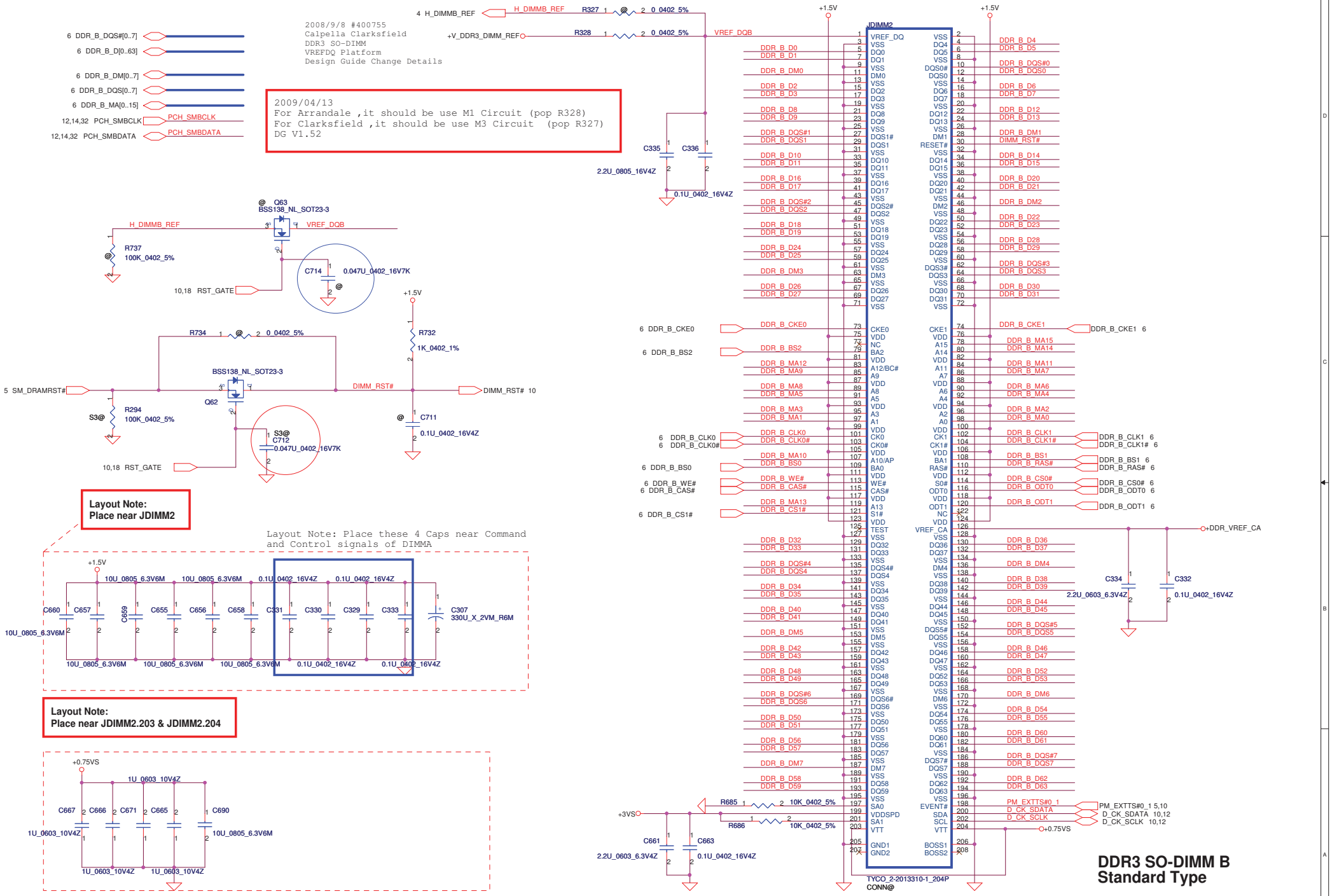

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Title: DDRIII-SODIMM SLOT2

Size: B28 | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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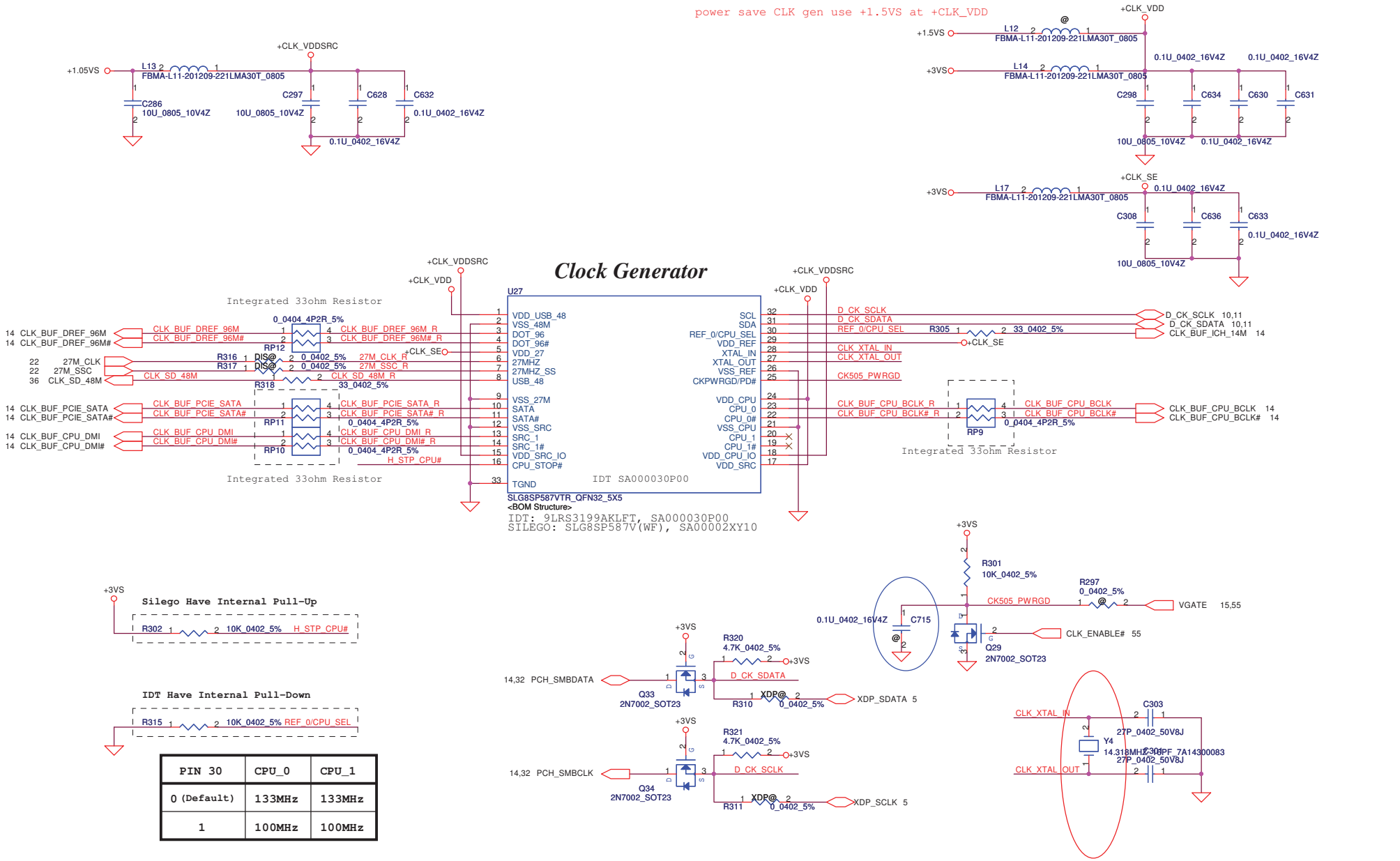
power save CLK gen use +1.5VS at +CLK_VDD
Clock Generator
U27
IDT SA000030P00
SLG8SP587VTR_QFN32_5X5
<BOM Structure>
IDT: 9LRS3199AKLFT, SA000030P00
SILEGO: SLG8SP587V(WF), SA00002XY10
Integrated 33ohm Resistor
Silego Have Internal Pull-Up
IDT Have Internal Pull-Down
R302 10K_0402_5% H_STP_CPU#
R315 10K_0402_5% REF_0/CPU_SEL
PIN 30 | CPU_0 | CPU_1
0 (Default) | 133MHz | 133MHz
1 | 100MHz | 100MHz
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Clock Generator (CK505)
NALG0 M/B LA-5681P Schematic
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+RTCVCC — R565 20K_0402_1% — PCH_RTCRST# — RC Delay 18~25mS

close to RAM door — J4 10K_0603_5% @ — C505 1U_0603_10V6K

+RTCVCC — R566 20K_0402_1% — PCH_SRTCRST# — RC Delay 18~25mS

close to RAM door — J5 10K_0603_5% @ — C518 1U_0603_10V6K

C210 18P_0402_50V8J — PCH_RTCX1

X1 32.768KHZ_12.5PF_Q13MC14610002 (NC OSC / NC OSC)

C211 18P_0402_50V8J — PCH_RTCX2

R176 10M_0402_5%

+RTCVCC

R567 1M_0402_5% — SM_INTRUDER#

R564 332K_0402_1% — PCH_INTVRMEN

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

U18A — REV1.0

RTC: RTCX1 B13, RTCX2 D13, RTCRST# C14, SRTCRST# D17, INTRUDER# A16, INTVRMEN A14

LPC: FWH0 / LAD0 D33 — LPC_AD0 — LPC_AD0 37
FWH1 / LAD1 B33 — LPC_AD1 — LPC_AD1 37
FWH2 / LAD2 C32 — LPC_AD2 — LPC_AD2 37
FWH3 / LAD3 A32 — LPC_AD3 — LPC_AD3 37
FWH4 / LFRAME# C34 — LPC_FRAME# — LPC_FRAME# 37
LDRQ0# A34
LDRQ1# / GPIO23 F34
SERIRQ AB9 — SERIRQ — SERIRQ 37

IHDA: HDA_BITCLK_PCH A30, HDA_SYNC_PCH D29, PCH_SPKR P1, HDA_RST#_PCH C30, HDA_SDIN0 G30, HDA_SDIN1 F30, HDA_SDIN2 E32, HDA_SDIN3 F32, HDA_SDO B29

SATA: ME_EN# H32, HDA_DOCK_RST# / GPIO13 J30

JTAG: PCH_JTAG_TCK M3, PCH_JTAG_TMS K3, PCH_JTAG_TDI K1, PCH_JTAG_TDO J2, PCH_JTAG_RST# J4

SPI: SPI_CLK BA2, SPI_CS0# AV3, SPI_CS1# AY3, SPI_MOSI AY1, SPI_MISO AV1

IBEXPEAK-M_FCBGA107

HDA for AUDIO
40 HDA_BITCLK_AUDIO — R185 33_0402_5% — HDA_BITCLK_PCH
40 HDA_SYNC_AUDIO — R183 33_0402_5% — HDA_SYNC_PCH
40 HDA_RST_AUDIO# — R186 33_0402_5% — HDA_RST#_PCH
40 HDA_SDOUT_AUDIO — R180 33_0402_5% — HDA_SDOUT_PCH

HDA for MDC
39 HDA_BITCLK_MDC — R593 33_0402_5% — HDA_BITCLK_PCH
39 HDA_SYNC_MDC — R590 33_0402_5% — HDA_SYNC_PCH
39 HDA_RST_MDC# — R596 33_0402_5% — HDA_RST#_PCH
39 HDA_SDOUT_MDC — R583 33_0402_5% — HDA_SDOUT_PCH

37,40 PCH_SPKR

GPIO33 can not pull down
(manufacturing environments)

SATA for HDD1
SATA0RXN AK7 — SATA_DTX_C_PRX_N0 — SATA_DTX_C_PRX_N0 31
SATA0RXP AK6 — SATA_DTX_C_PRX_P0 — SATA_DTX_C_PRX_P0 31
SATA0TXN AK11 — SATA_PTX_DRX_N0 — SATA_PTX_DRX_N0 31
SATA0TXP AK9 — SATA_PTX_DRX_P0 — SATA_PTX_DRX_P0 31

SATA for ODD
SATA1RXN AH6 — SATA_DTX_C_PRX_N1 — SATA_DTX_C_PRX_N1 31
SATA1RXP AH5 — SATA_DTX_C_PRX_P1 — SATA_DTX_C_PRX_P1 31
SATA1TXN AH9 — SATA_PTX_DRX_N1 — SATA_PTX_DRX_N1 31
SATA1TXP AH8 — SATA_PTX_DRX_P1 — SATA_PTX_DRX_P1 31

2/10 SATA2, SATA3 not support on HM55
SATA2RXN AE11, SATA2RXP AE9, SATA2TXN AE7, SATA2TXP AE6
SATA3RXN AH3, SATA3RXP AH1, SATA3TXN AF3, SATA3TXP AF1

SATA for eSATA
SATA4RXN AD9 — SATA_DTX_C_PRX_N4 — SATA_DTX_C_PRX_N4 35
SATA4RXP AD8 — SATA_DTX_C_PRX_P4 — SATA_DTX_C_PRX_P4 35
SATA4TXN AD6 — SATA_PTX_DRX_N4 — SATA_PTX_DRX_N4 35
SATA4TXP AD5 — SATA_PTX_DRX_P4 — SATA_PTX_DRX_P4 35
SATA5RXN AD3, SATA5RXP AD1, SATA5TXN AB3, SATA5TXP AB1

SATAICOMPO AE16
SATAICOMPI AE15 — SATA_COMP — R576 37.4_0402_1% — +1.05VS

SATALED# T3 — R136 10K_0402_5% — +3VS — SATA_LED# 44

SATA0GP / GPIO21 Y9 — R517 10K_0402_5% — +3VS
SATA1GP / GPIO19 V1 — R135 10K_0402_5% — +3VS

R111 10K_0402_5%
R518 10K_0402_5%

If GPIO33 pull down, ME will not working.
For factory update ME, pull down resistor pull under door.

+3VS — R130 1K_0402_5% — PCH_SPKR — Have internal PD
R512 10K_0402_5% — SERIRQ

PCH_SPI_CLK_1 R122 0_0402_5% — PCH_SPI_CLK
PCH_SPI_CS0# R124 15_0402_5% — PCH_SPI_CS0#_R
PCH_SPI_MOSI_1 R123 15_0402_5% — PCH_SPI_MOSI
PCH_SPI_MISO_1 R125 33_0402_5% — PCH_SPI_MISO

+3VALW +1.05VS

PCH_JTAG_TMS: R115 51_0402_5% @, R114 200_0402_5%, R138 100_0402_5%
PCH_JTAG_TDO: R141 51_0402_5% @, R118 200_0402_5%, R140 100_0402_5%
PCH_JTAG_TDI: R116 51_0402_5% @, R117 200_0402_5%, R139 100_0402_5%
PCH_JTAG_RST#: R142 51_0402_5% @, R119 20K_0402_5%, R143 10K_0402_5%

2008 Intel MOW36/MOW50
TDO:
Reserved on ES1 Sample
Mount R516, R517 on ES2 Sample

MP mount R689, R690, R691, R692 and remove others

+3VS — R97 3.3K_0402_5% — PCH_SPI_CS0# — SPI_WP1# — R96 3.3K_0402_5% — SPI_HOLD1#

U14: CS# 1, WP# 3, HOLD# 7, GND 4, VCC 8, SCLK 6, SI 5, SO 2
PCH_SPI_CLK_1, PCH_SPI_MOSI_1, PCH_SPI_MISO_1

MX25L1605DM2I-12G SOP 8P
SA000021A00
SPI ROM (4M)

+3VS — PCH_SPI_MOSI R134 1K_0402_5% — enable iTPM: SPI_MOSI High

PCH_JTAG_TCK R137 4.7K_0402_5% — CRB 1.0 Change to 4.7K

+3VS — R729 100K_0402_5% — ME_EN#
37 ME_EN — R730 100K_0402_5% — Q61 2N7002_SOT23

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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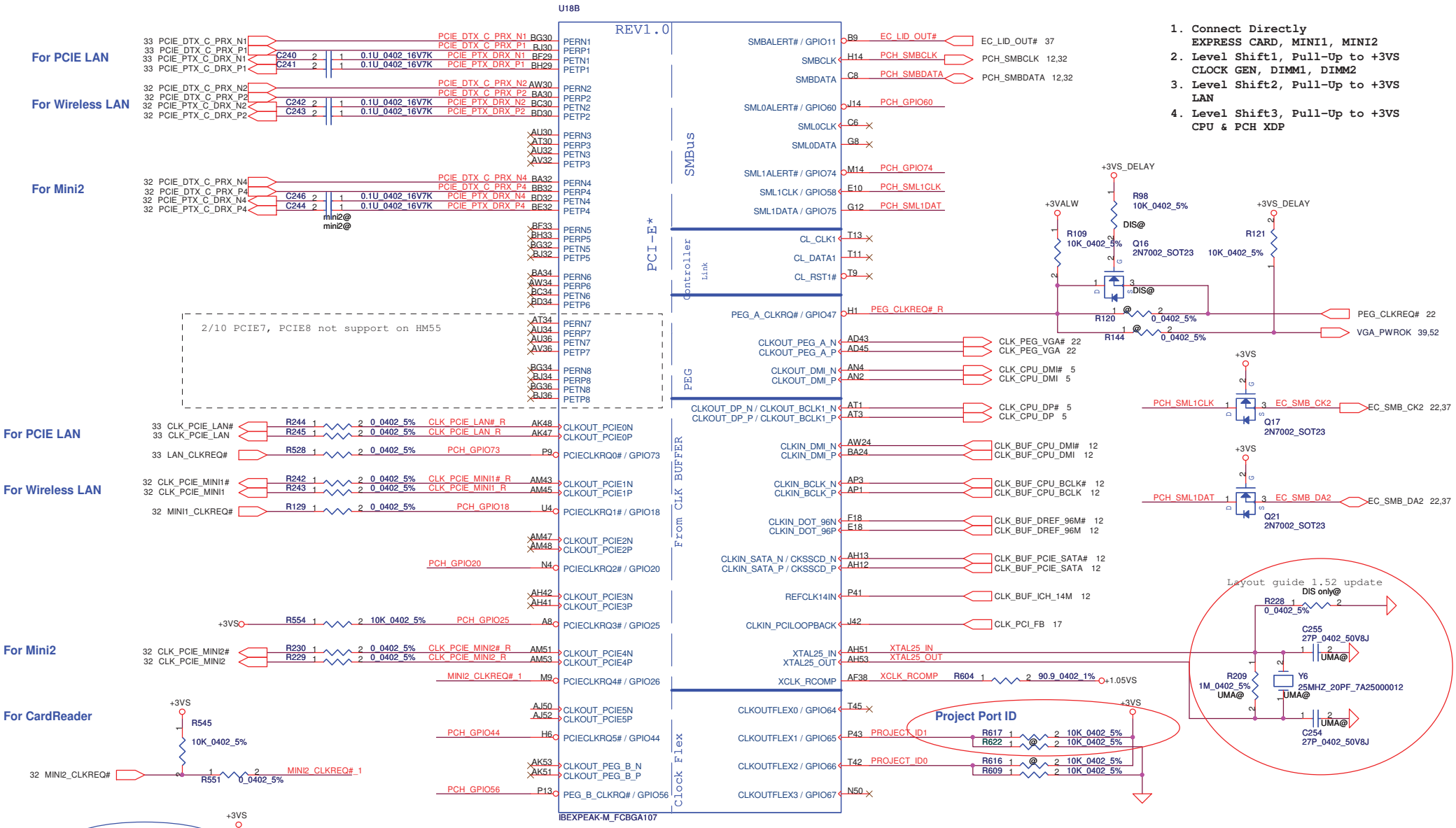
Compal Electronics, Inc.

Title: PCH (1/9) SATA,HDA,SPI, LPC

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 13 of 60



Project ID		
ID1	ID0	Project
* 1	0	JV 40
1	1	JM 40

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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Compal Electronics, Inc.

Title: PCH (2/9) PCIE, SMBUS, CLK

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 14 of 60

4 DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
4 DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
4 DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
4 DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

4 H_FDI_TXN[0..7] H_FDI_TXN[0..7]
4 H_FDI_TXP[0..7] H_FDI_TXP[0..7]

U18C

REV1.0

DMI0RXN DMI_HTX_PRX_N0 BC24
DMI1RXN DMI_HTX_PRX_N1 BJ22
DMI2RXN DMI_HTX_PRX_N2 AW20
DMI3RXN DMI_HTX_PRX_N3 BJ20
DMI0RXP DMI_HTX_PRX_P0 BD24
DMI1RXP DMI_HTX_PRX_P1 BG22
DMI2RXP DMI_HTX_PRX_P2 BA20
DMI3RXP DMI_HTX_PRX_P3 BG20
DMI0TXN DMI_PTX_HRX_N0 BE22
DMI1TXN DMI_PTX_HRX_N1 BF21
DMI2TXN DMI_PTX_HRX_N2 BD20
DMI3TXN DMI_PTX_HRX_N3 BE18
DMI0TXP DMI_PTX_HRX_P0 BD22
DMI1TXP DMI_PTX_HRX_P1 BH21
DMI2TXP DMI_PTX_HRX_P2 BC20
DMI3TXP DMI_PTX_HRX_P3 BD18
DMI_ZCOMP BH25
DMI_IRCOMP BF25

DMI

FDI

FDI_RXN0 BA18 H_FDI_TXN0
FDI_RXN1 BH17 H_FDI_TXN1
FDI_RXN2 BD16 H_FDI_TXN2
FDI_RXN3 BJ16 H_FDI_TXN3
FDI_RXN4 BA16 H_FDI_TXN4
FDI_RXN5 BE14 H_FDI_TXN5
FDI_RXN6 BA14 H_FDI_TXN6
FDI_RXN7 BC12 H_FDI_TXN7
FDI_RXP0 BB18 H_FDI_TXP0
FDI_RXP1 BF17 H_FDI_TXP1
FDI_RXP2 BC16 H_FDI_TXP2
FDI_RXP3 BG16 H_FDI_TXP3
FDI_RXP4 AW16 H_FDI_TXP4
FDI_RXP5 BD14 H_FDI_TXP5
FDI_RXP6 BB14 H_FDI_TXP6
FDI_RXP7 BD12 H_FDI_TXP7
FDI_INT BJ14 H_FDI_INT 4
FDI_FSYNC0 BF13 H_FDI_FSYNC0 4
FDI_FSYNC1 BH13 H_FDI_FSYNC1 4
FDI_LSYNC0 BJ12 H_FDI_LSYNC0 4
FDI_LSYNC1 BG14 H_FDI_LSYNC1 4

+3VS
R127 1 2 8.2K_0402_5% PM_CLKRUN#
R509 1 @ 2 10K_0402_5% XDP_DBRESET#

+3VALW
R108 1 2 10K_0402_5% SUS_PWR_ACK
R165 1 2 8.2K_0402_5% PCH_GPIO72
R580 1 2 10K_0402_5% EC_SWI#
R552 1 2 1K_0402_5% PCH_PCIE_WAKE#
R540 1 @ 2 10K_0402_5% PM_SLP_LAN#

+1.05VS
R184 1 2 49.9_0402_1% DMI_COMP

5 XDP_DBRESET# XDP_DBRESET# T6
SYS_PWROK R100 2 1 0_0402_5% SYS_PWROK_R M6
VGATE R95 2 @ 1 0_0402_5%
SYS_PWROK B17
R101 2 1 0_0402_5% ME_PWROK K5
LAN_RST# A10
5 PM_DRAM_PWRGD D9
PCH_RSMRST# C16
37 SUS_PWR_ACK SUS_PWR_ACK M1
10/2 Intel suggestion change to 10K
+3VALW R530 1 2 100K_0402_5% 5,37 PBTN_OUT# PBTN_OUT# P5
37,43,44,45 ACIN D10 CH751H-40PT_SOD323-2 PCH_ACIN P7
PCH_GPIO72 A6
37 EC_SWI# EC_SWI# F14

SYS_RESET#
SYS_PWROK
PWROK
MEPWROK
LAN_RST#
DRAMPWROK
RSMRST#
SUS_PWR_DN_ACK / GPIO30
PWRBTN#
ACPRESENT / GPIO31
BATLOW# / GPIO72
RI#

System Power Management

WAKE# J12 PCH_PCIE_WAKE# PCH_PCIE_WAKE# 32,33
CLKRUN# / GPIO32 Y1 PM_CLKRUN# PM_CLKRUN# 37
SUS_STAT# / GPIO61 P8 PCH_GPIO61 @ PAD T17
SUSCLK / GPIO62 F3 PCH_GPIO62 @ PAD T15
SLP_S5# / GPIO63 E4 PM_SLP_S5# 37
SLP_S4# H7 PM_SLP_S4# 37
SLP_S3# P12 PM_SLP_S3# 37
SLP_M# K8 PM_SLP_M# @ PAD T16
TP23 N2 PM_SLP_DSW# @ PAD T4
PMSYNCH BJ10 H_PM_SYNC 5
SLP_LAN# / GPIO29 F6 PM_SLP_LAN#

IBEXPEAK-M_FCBGA107
@

+3VS
U13
SYS_PWROK 4 Y
B 2 EC_PWROK EC_PWROK 37
A 1 VGATE VGATE 12,55
NC7SZ08P5X_NL_SC70-5

SYS_PWROK R103 1 2 10K_0402_5%
EC_PWROK R94 1 2 10K_0402_5%
LAN_RST# R174 1 2 10K_0402_5%
No used Integrated LAN,
connecting LAN_RST# to GND

R198 2 1 @ 0_0402_5%
Q25 MMBT3906_SOT23-3
PCH_RSMRST# 1 3 EC_RSMRST# 37
R197 10K_0402_5% 2
R207 1 2 4.7K_0402_5% +3VALW
D14A BAV99DW-7_SOT363
D14B BAV99DW-7_SOT363
R206 2.2K_0402_5%

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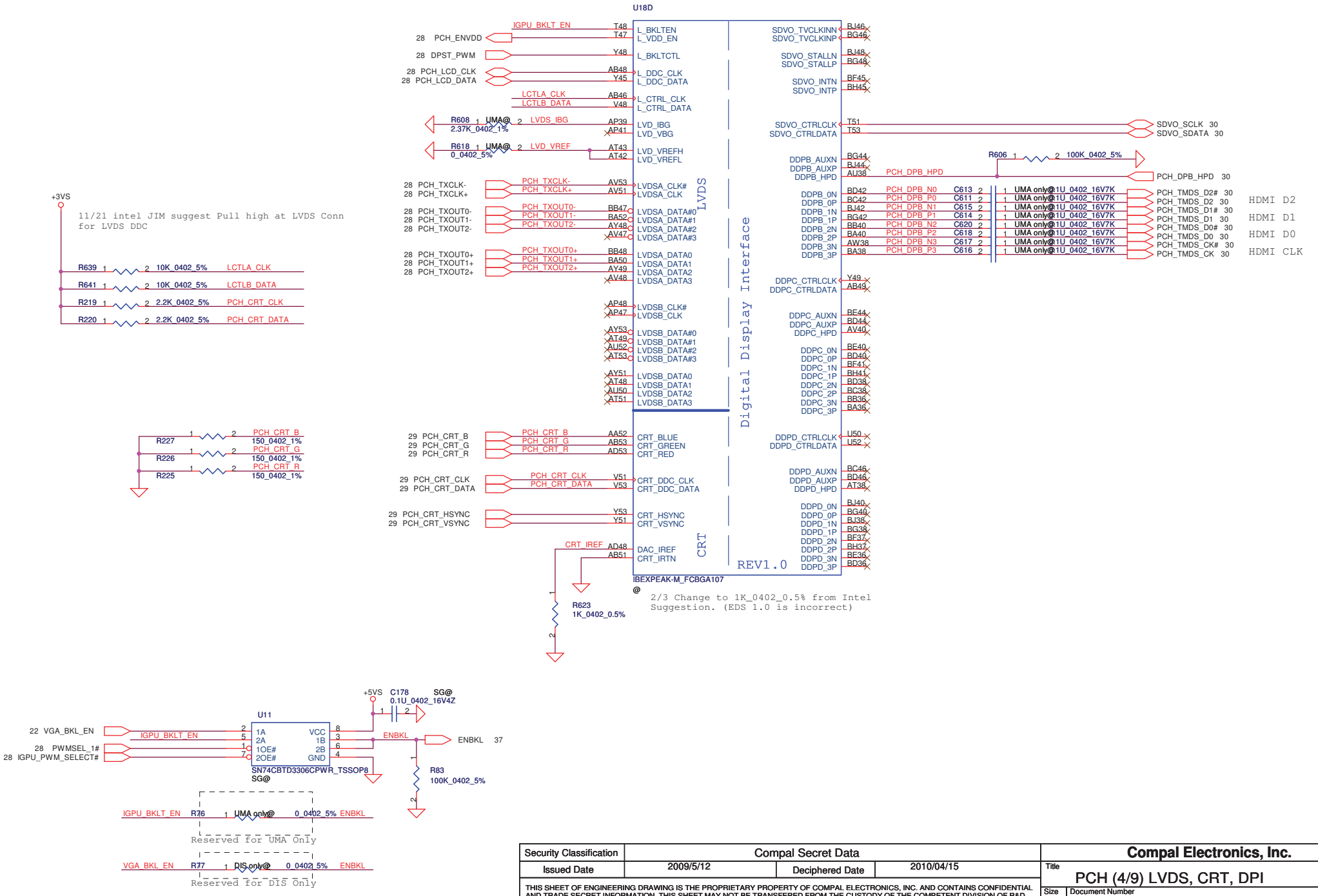
Compal Electronics, Inc.

Title: PCH (3/9) DMI, FDI, PM

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 15 of 60



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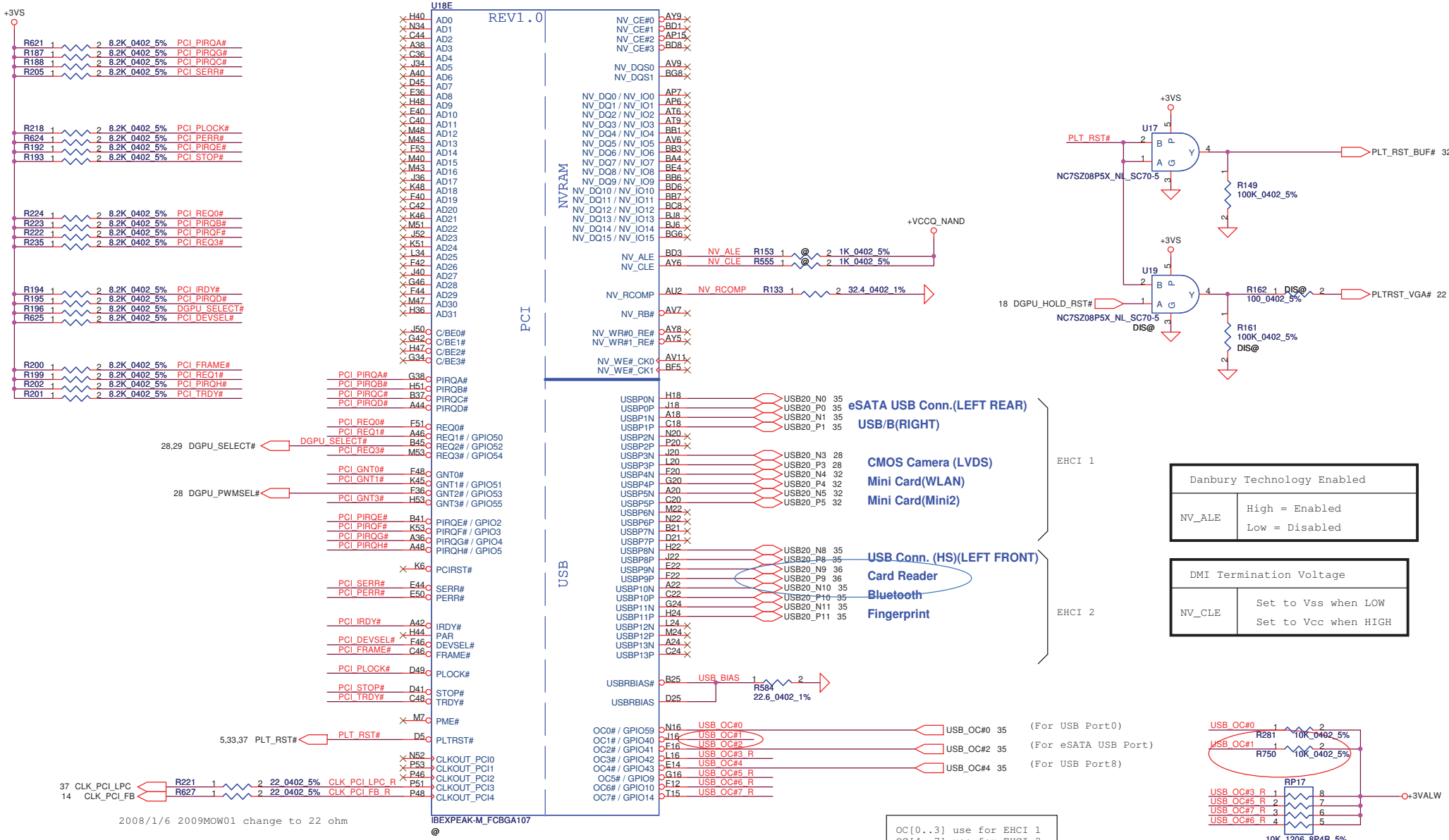
Compal Electronics, Inc.

Title: PCH (4/9) LVDS, CRT, DPI

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 16 of 60



Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

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Issued Date	2009/5/12	Deciphered Date	2010/04/15

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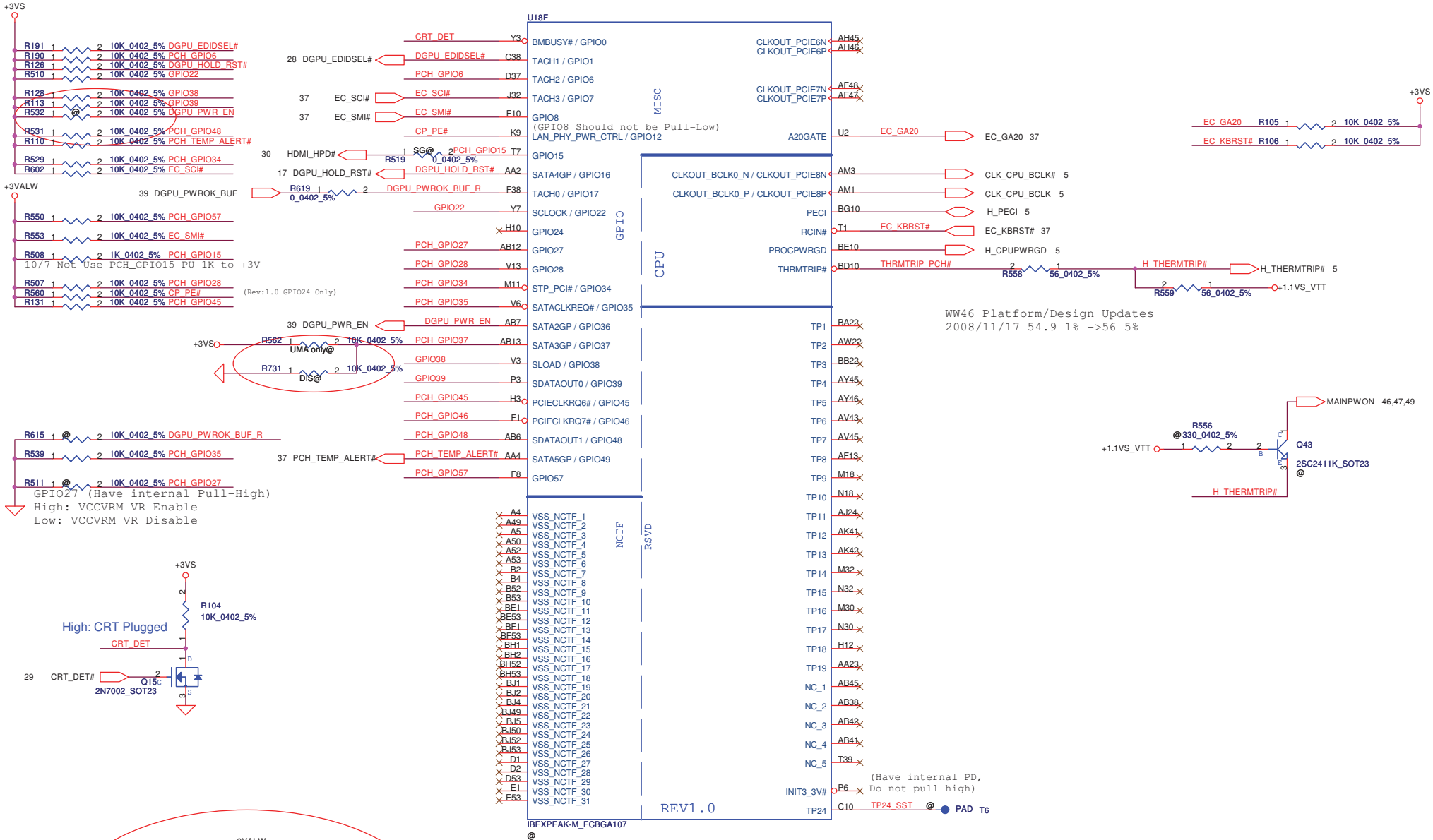
Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB, VRAM

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 17 of 60



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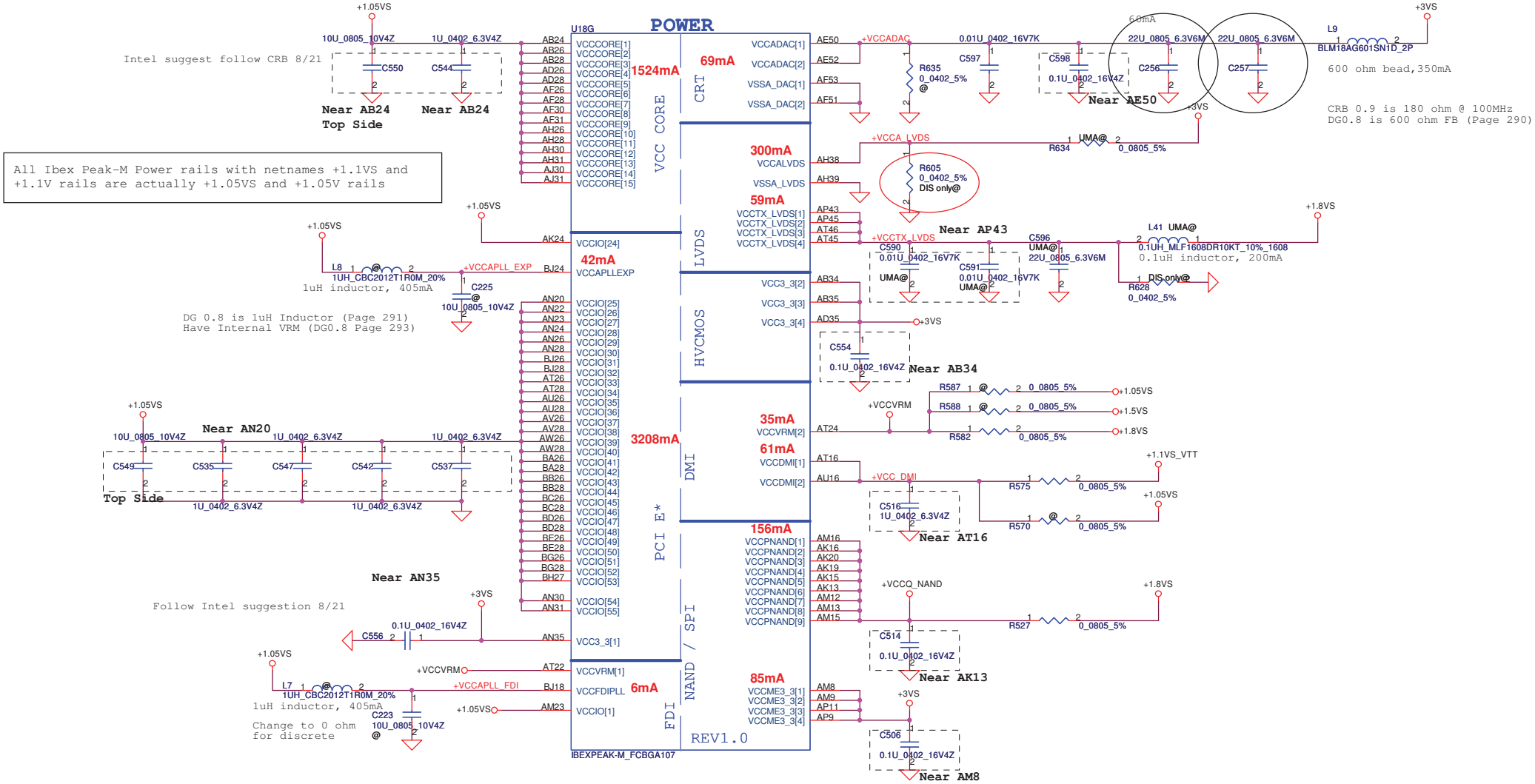
Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 18 of 60



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Compal Electronics, Inc.

Title: PCH (7/9) PWR

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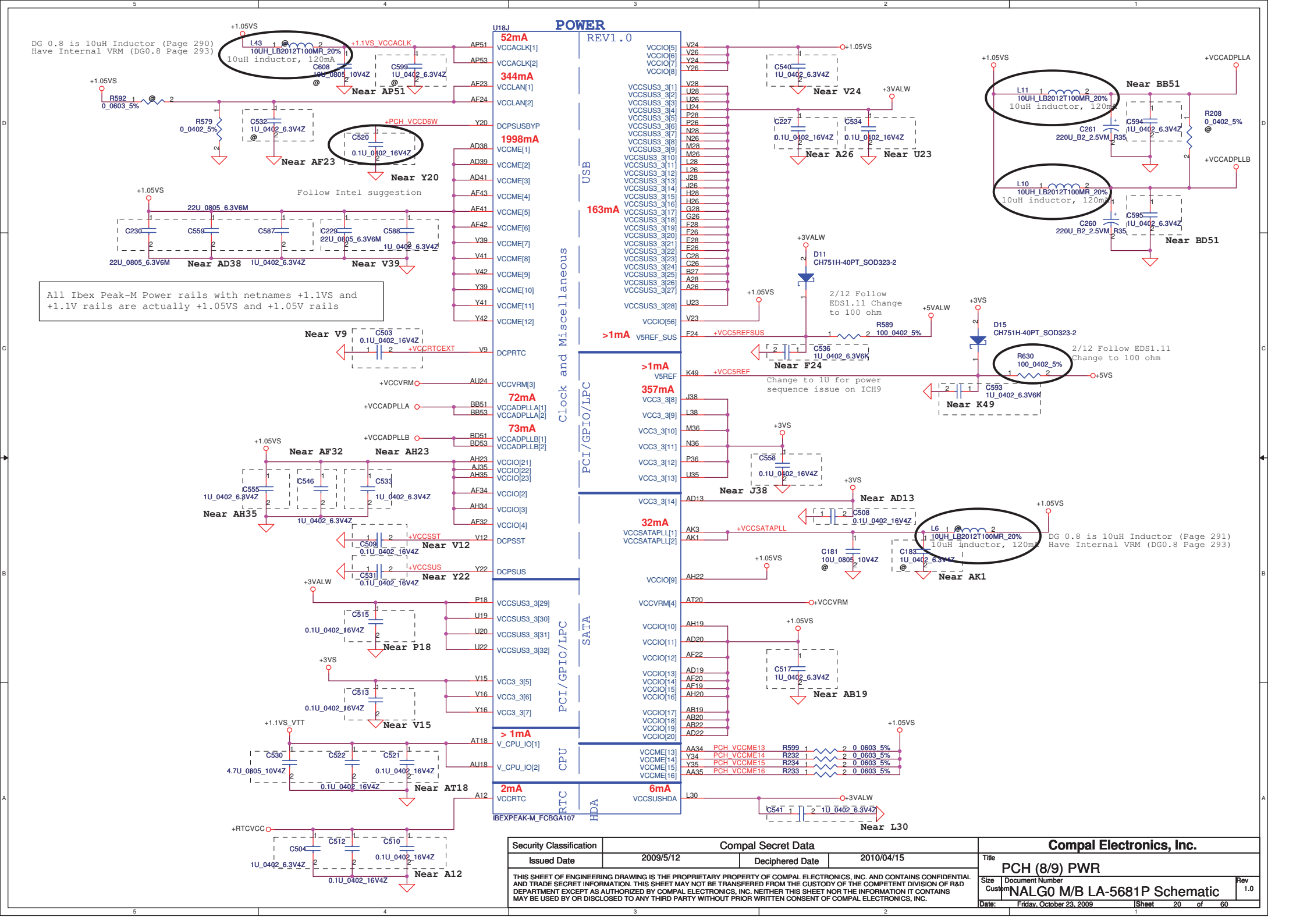
POWER
REV1.0
U18J
IBEXPEAK-M_FCBGA107
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
DG 0.8 is 10uH Inductor (Page 290)
Have Internal VRM (DG0.8 Page 293)
10uH inductor, 120mA
Follow Intel suggestion
All Ibex Peak-M Power rails with netnames +1.1VS and +1.1V rails are actually +1.05VS and +1.05V rails
2/12 Follow EDS1.11 Change to 100 ohm
Change to 1U for power sequence issue on ICH9
DG 0.8 is 10uH Inductor (Page 291)
Have Internal VRM (DG0.8 Page 293)
Near AP51
Near AF23
Near Y20
Near AD38
Near V39
Near V9
Near F24
Near K49
Near BB51
Near BD51
Near V24
Near A26
Near U23
Near AF32
Near AH23
Near AH35
Near V12
Near Y22
Near J38
Near AD13
Near AK1
Near P18
Near V15
Near AB19
Near AT18
Near A12
Near L30
52mA
344mA
1998mA
163mA
72mA
73mA
>1mA
357mA
32mA
> 1mA
2mA
6mA
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Title
PCH (8/9) PWR
Size
Custom
Document Number
NALG0 M/B LA-5681P Schematic
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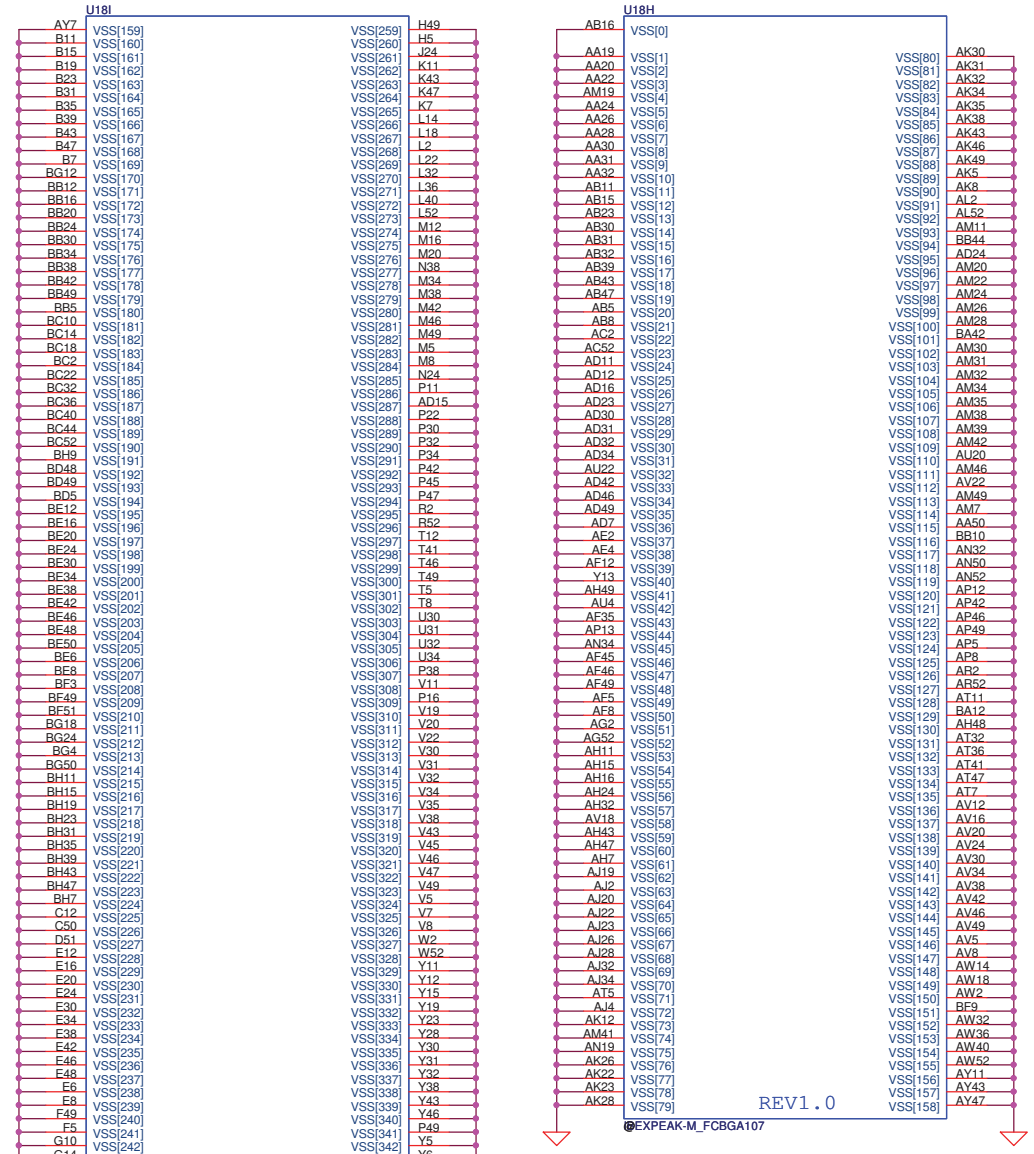

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Compal Electronics, Inc.

Title: PCH (9/9) VSS & PCH XDP Port

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

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GPIO	I/O	ACTIVE	USAGE
GPIO0	IN	N/A	N/A
GPIO1	IN	H	HDMI Hot-plug
GPIO2	OUT	H	VGA_PNL_PWM
GPIO3	OUT	H	ENVDD
GPIO4	OUT	H	VGA_BKL_EN
GPIO5	OUT	N/A	NVVDD VID0
GPIO6	OUT	N/A	NVVDD VID1
GPIO7	OUT	N/A	N/A
GPIO8	IN	L	N/A
GPIO9	OUT	L	N/A
GPIO10	OUT	N/A	N/A
GPIO11	OUT	N/A	N/A
GPIO12	IN	N/A	N/A
GPIO13	OUT	N/A	N/A
GPIO14	OUT	N/A	N/A

External Spread Spectrum

If External Spread Spectrum not stuff then stuff resistor

CRT

LVDS

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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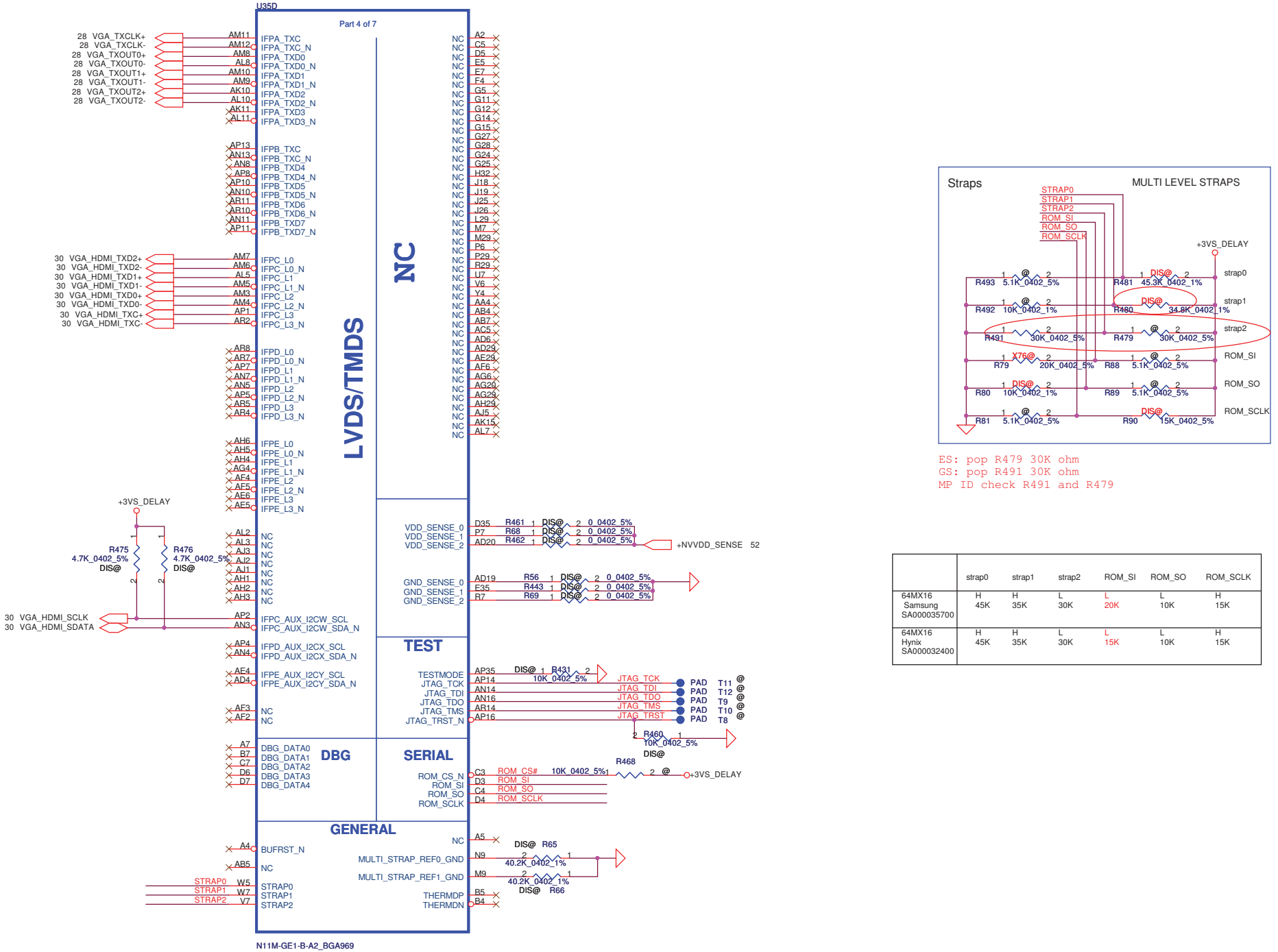
Compal Electronics, Inc.

Title: N11M PEG 1/6

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 22 of 60



ES: pop R479 30K ohm
GS: pop R491 30K ohm
MP ID check R491 and R479

	strap0	strap1	strap2	ROM_SI	ROM_SO	ROM_SCLK
64MX16 Samsung SA000035700	H 45K	H 35K	L 30K	L 20K	L 10K	H 15K
64MX16 Hynix SA000032400	H 45K	H 35K	L 30K	L 15K	L 10K	H 15K

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date 2010/04/15	Title: N11M LVDS 2/6
			Size: Custom; Document Number: NALG0 M/B LA-5681P Schematic; Rev:
			Date: Friday, October 23, 2009; Sheet 23 of 60

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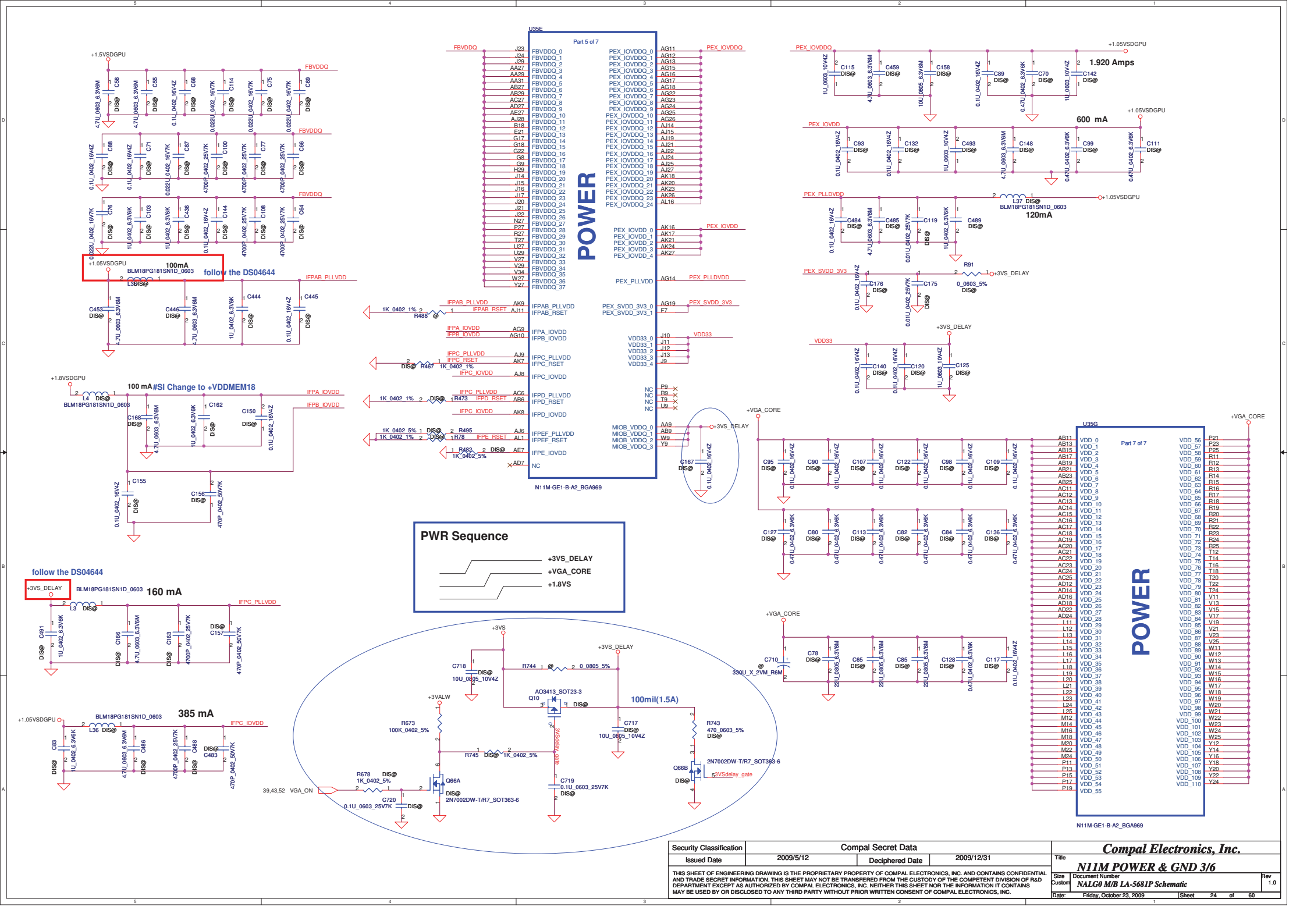

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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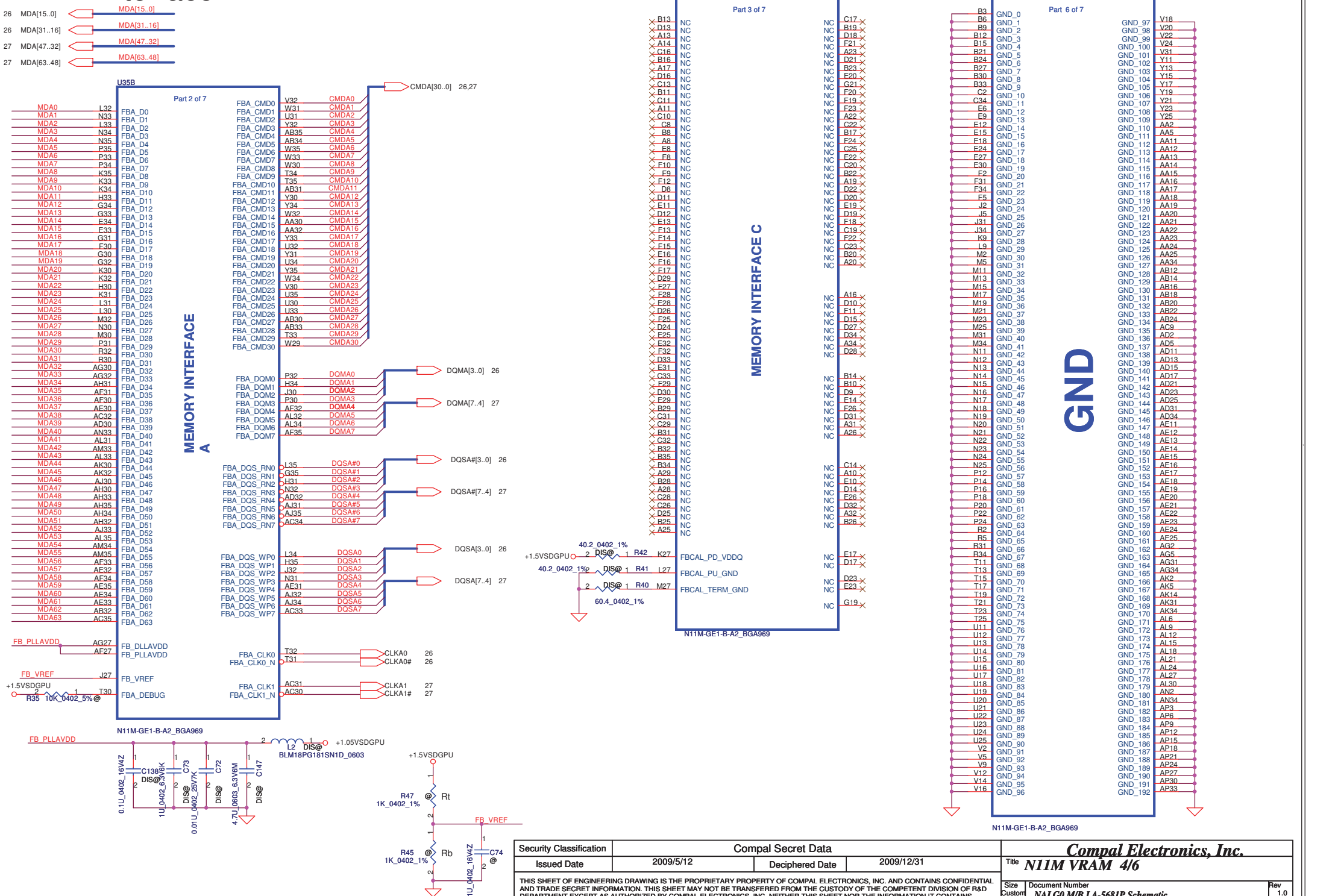
Compal Electronics, Inc.

Title: **N11M POWER & GND 3/6**

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 | Sheet 24 of 60

VRAM Interface



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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Compal Electronics, Inc.

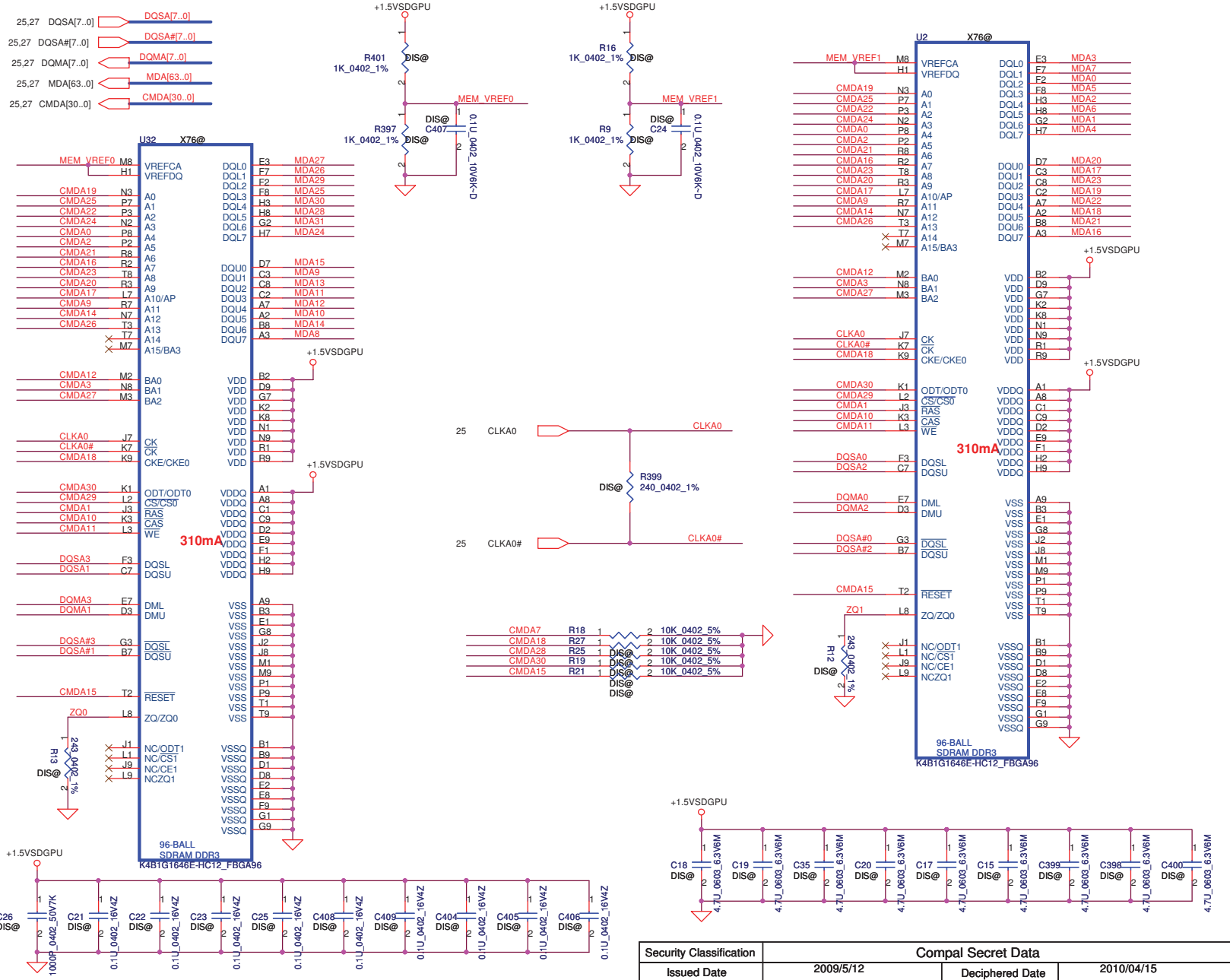
Title: **N11M VRAM 4/6**

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

Date: Friday, October 23, 2009 Sheet 25 of 60

VRAM gDDR3 chips (256MB & 512MB)

32Mx16 gDDR2 *4==>256MB
64Mx16 gDDR3 *4==>512MB



Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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Compal Electronics, Inc.

Title: N11M gDDR3 5/6

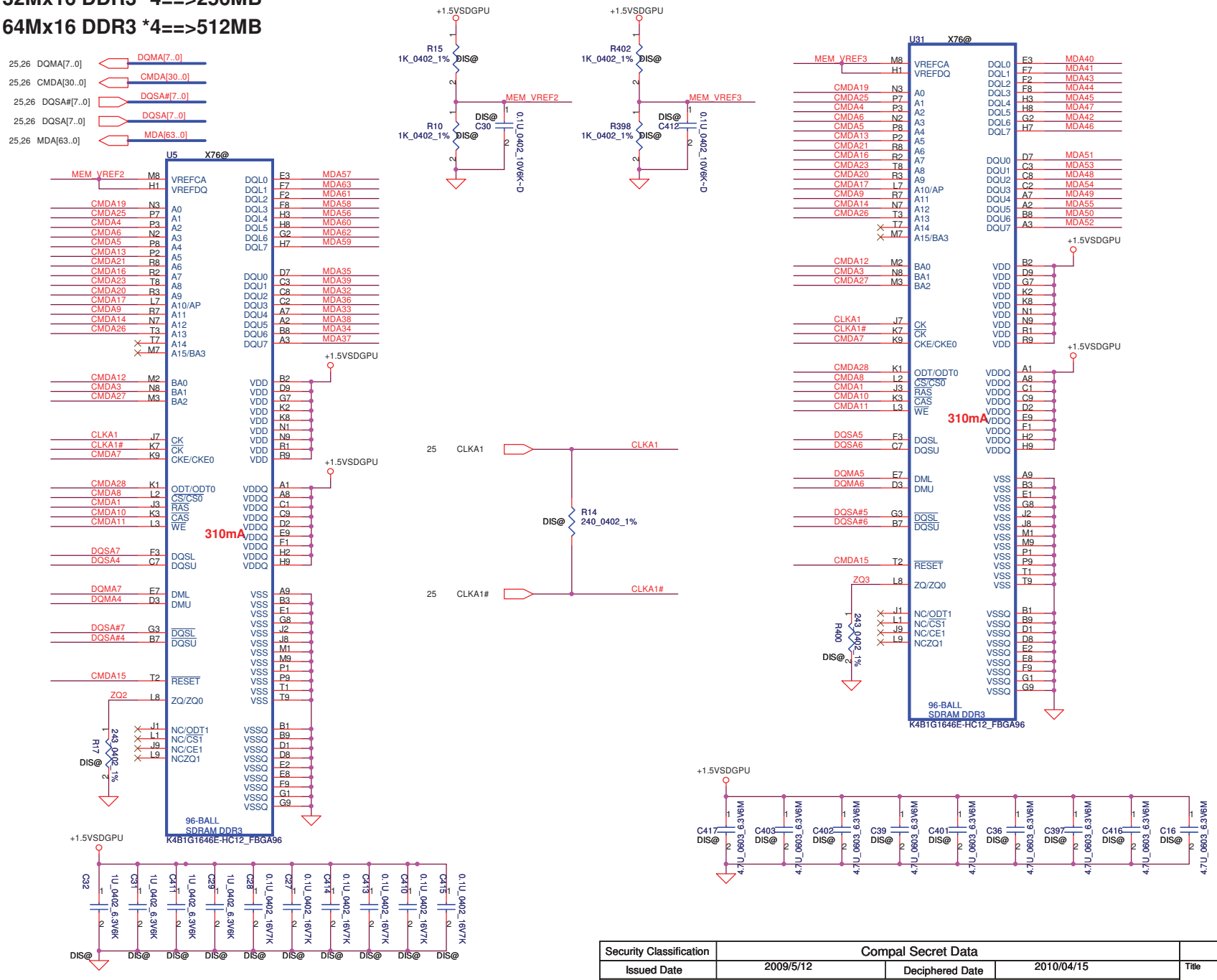
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev:

Date: Friday, October 23, 2009 | Sheet 26 of 60

VRAM DDR3 chips (256MB & 512MB)

32Mx16 DDR3 *4==>256MB

64Mx16 DDR3 *4==>512MB



Address	0..31	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7		CKE
CMD8		CS#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST	RST
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28		ODT
CMD29	CS#	
CMD30	ODT	
	LOW	HIGH

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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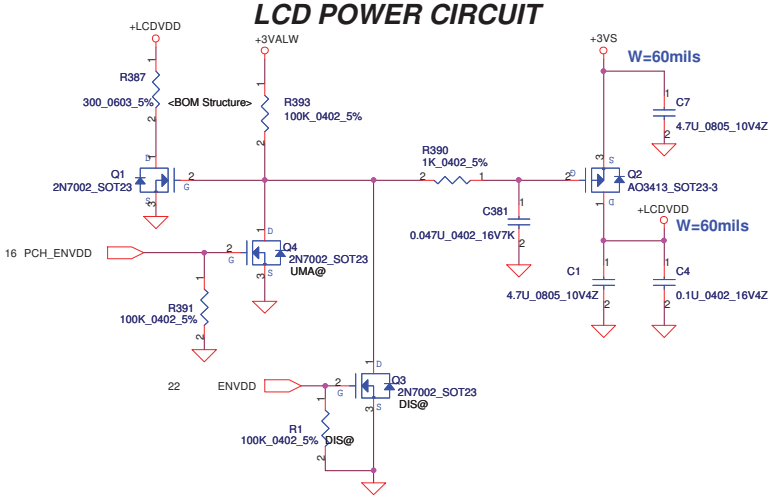
Compal Electronics, Inc.

Title: N11M gDDR3 6/6

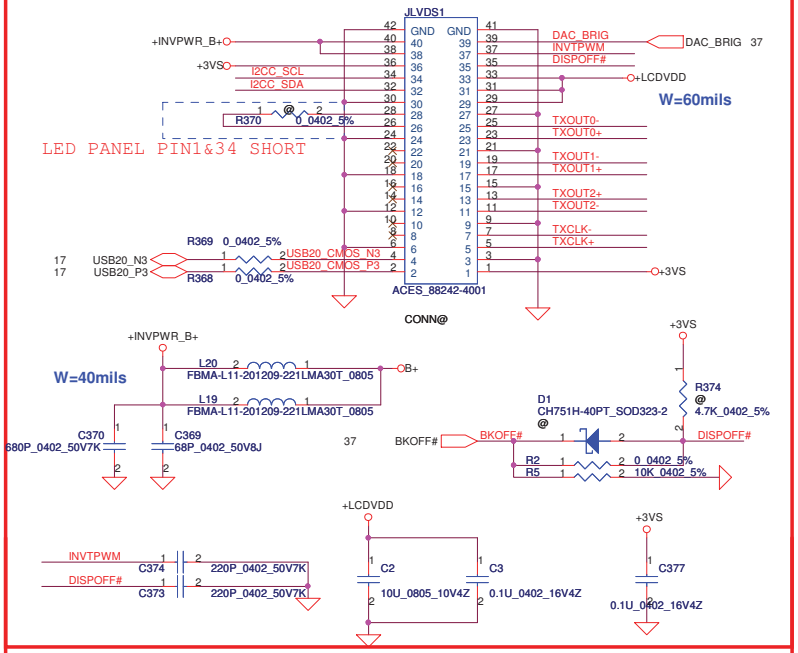
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 27 of 60

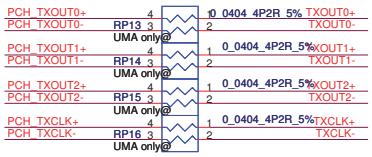
LCD POWER CIRCUIT



LED PANEL Conn.

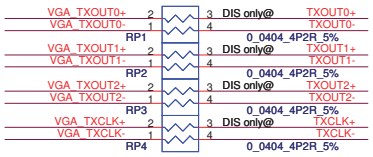


UMA ONLY

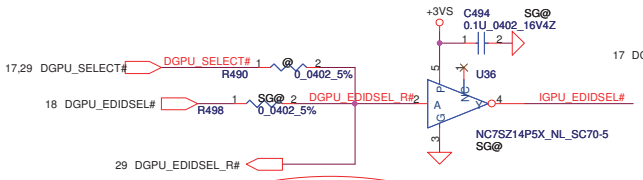


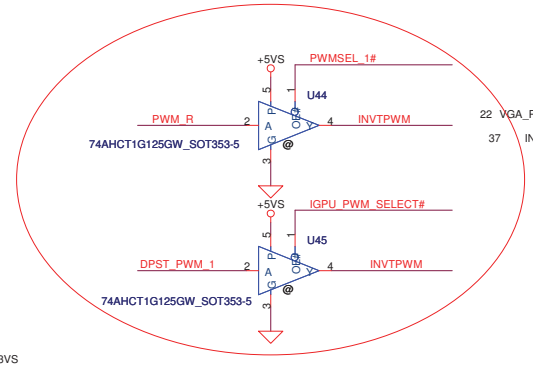
PCH_LCD_CLK R501 1 UMA only@ 0_0402_5% I2CC_SCL
PCH_LCD_DATA R483 1 UMA only@ 0_0402_5% I2CC_SDA

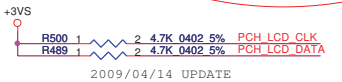
DIS ONLY

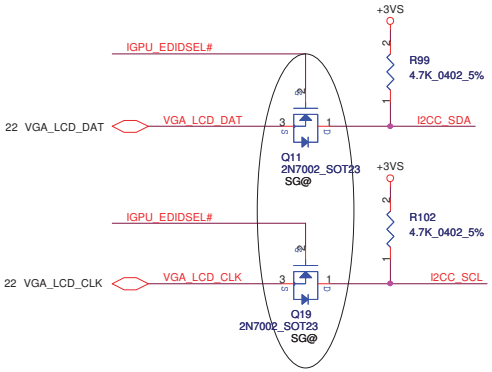


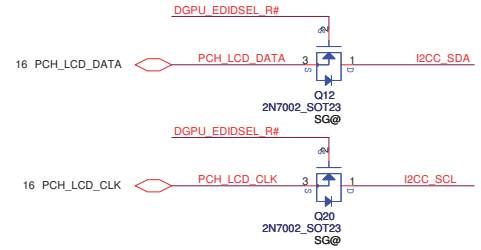
VGA_LCD_CLK R502 1 DIS only@ 0_0402_5% I2CC_SCL
VGA_LCD_DAT R484 1 DIS only@ 0_0402_5% I2CC_SDA

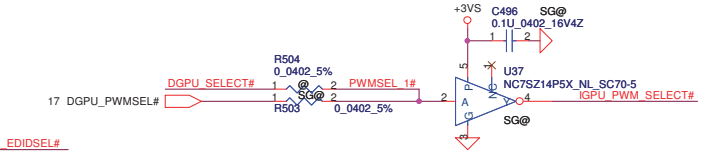


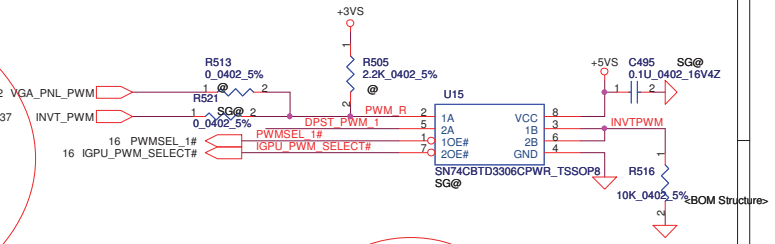


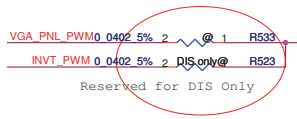


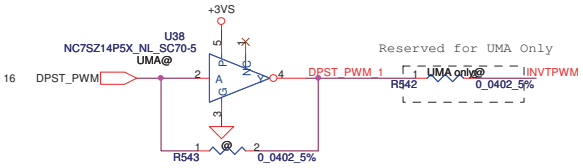






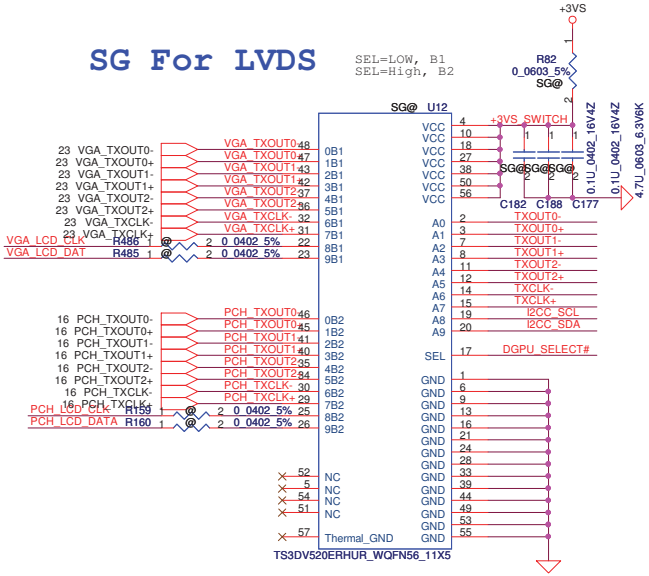






SG For LVDS

SEL=LOW, B1
SEL=High, B2



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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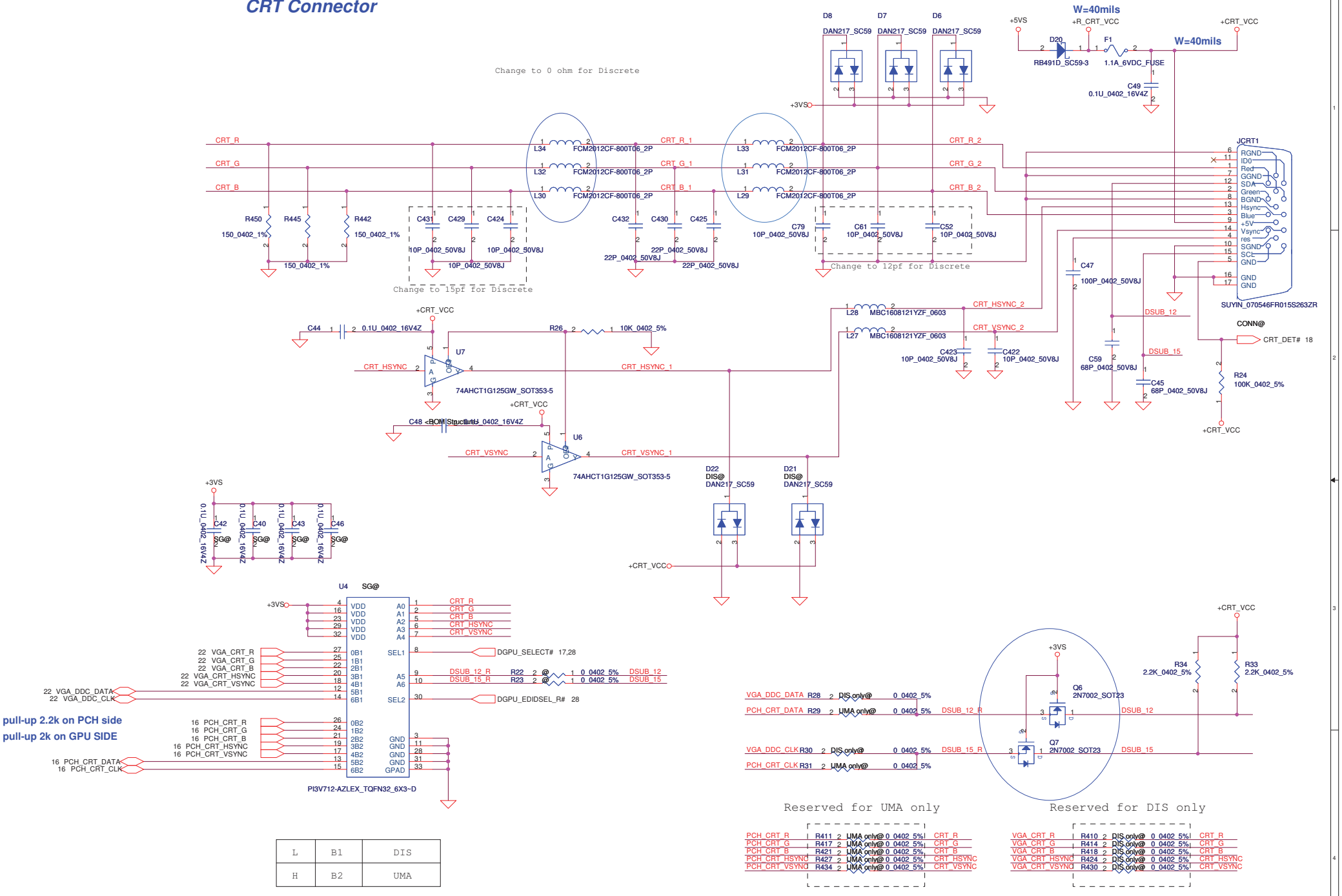
Compal Electronics, Inc.

Title: LVDS Connector

Size: B (Custom) | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 28 of 60

CRT Connector



L	B1	DIS
H	B2	UMA

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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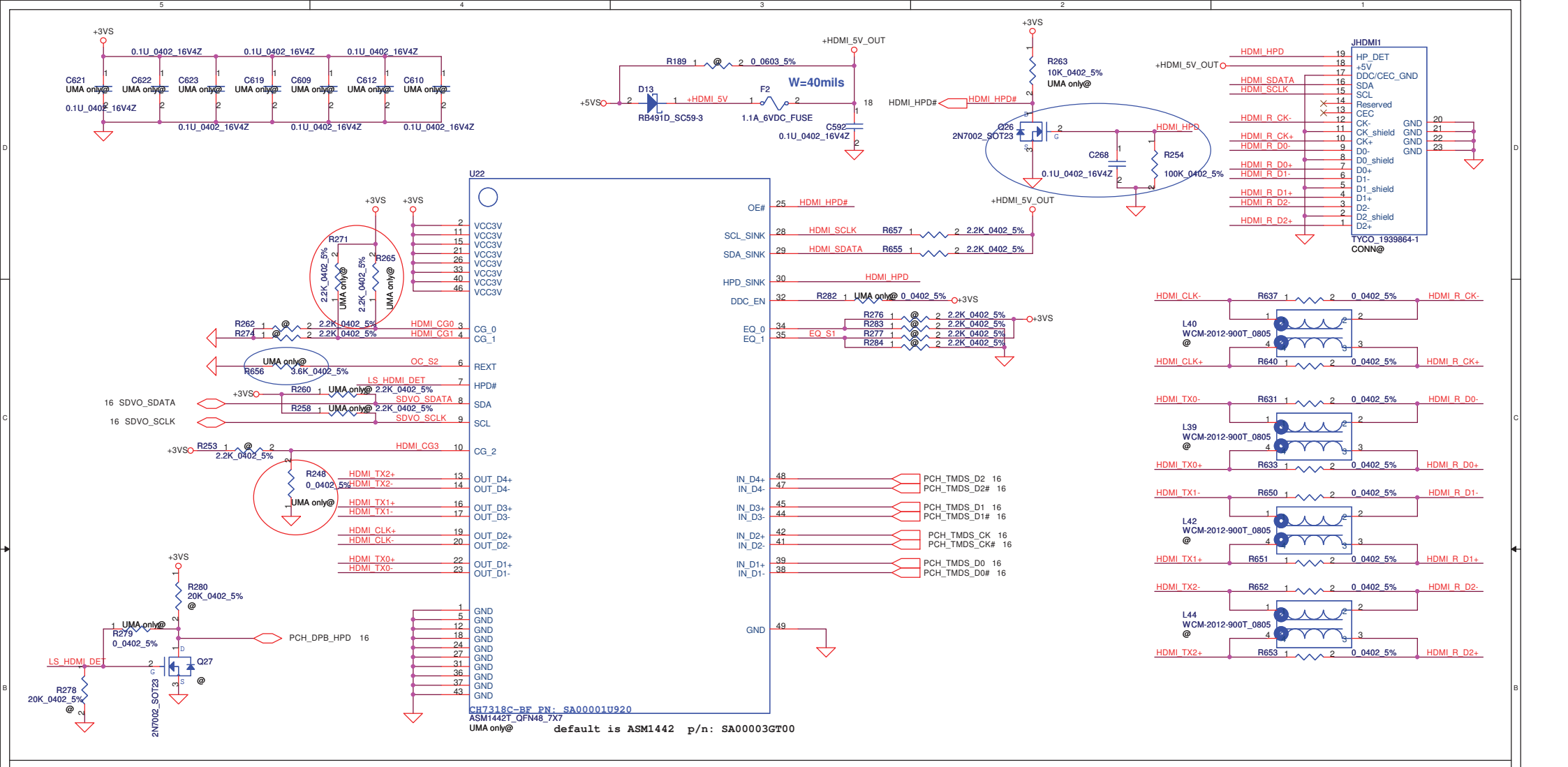
Compal Electronics, Inc.

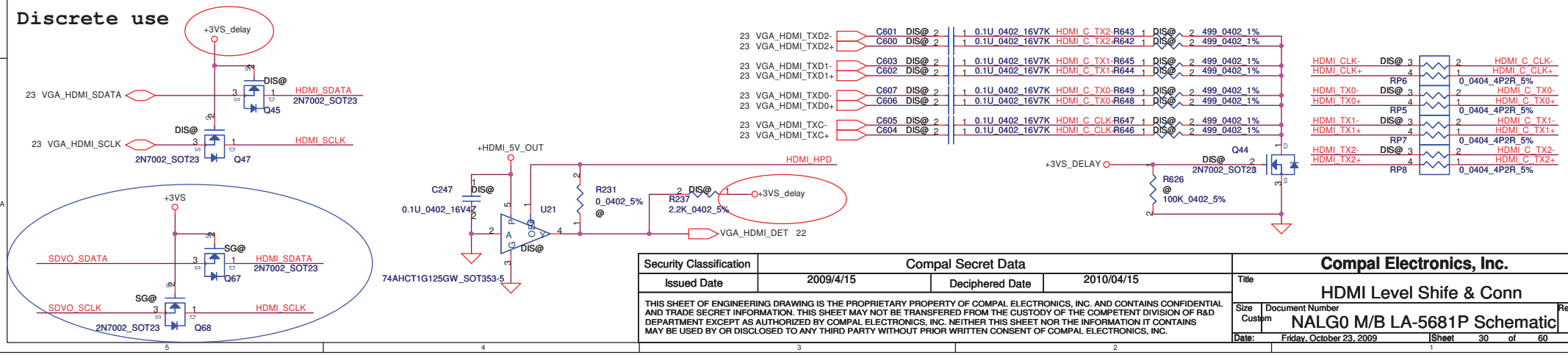
Title: CRT Connector

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 29 of 60



Discrete use



Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

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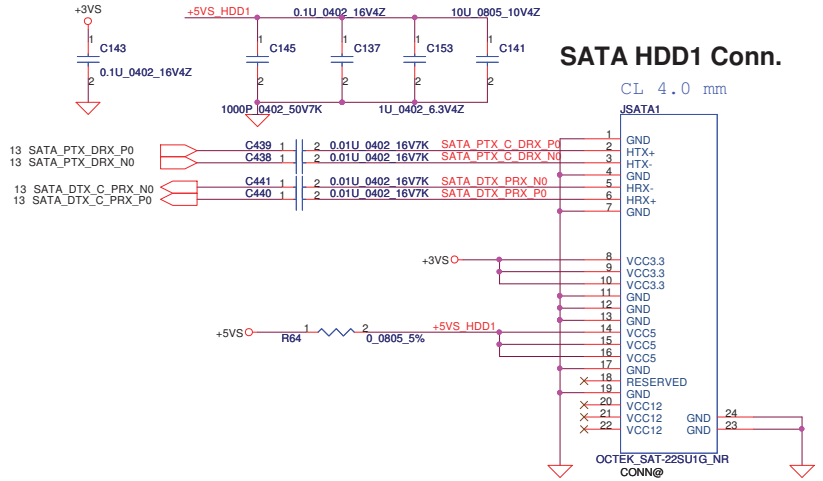
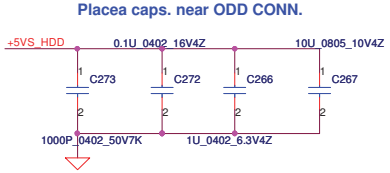
Compal Electronics, Inc.

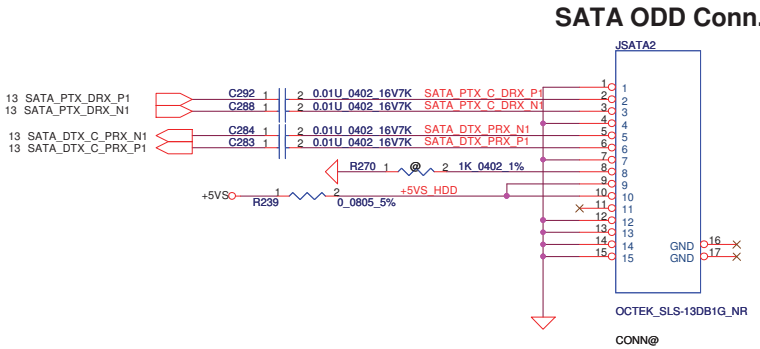
Title: HDMI Level Shife & Conn

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 30 of 60







Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2009/5/12	Deciphered Date 2010/04/15	Title: HDD & ODD & MINI CARD &CARDREADER Connector
			Size: B; Document Number: NALG0 M/B LA-5681P Schematic; Rev: 1.0
			Date: Friday, October 23, 2009; Sheet 31 of 60

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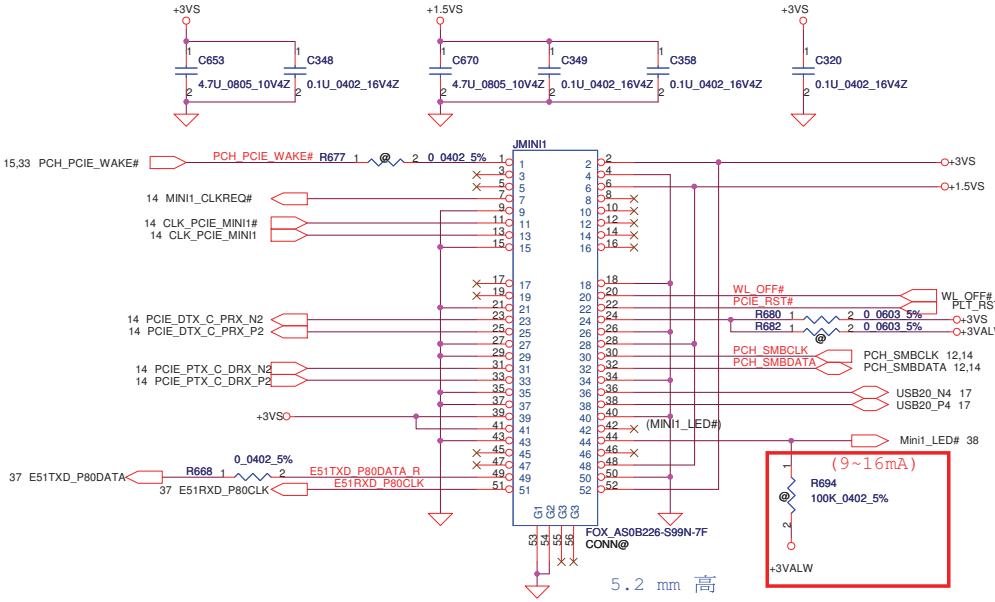
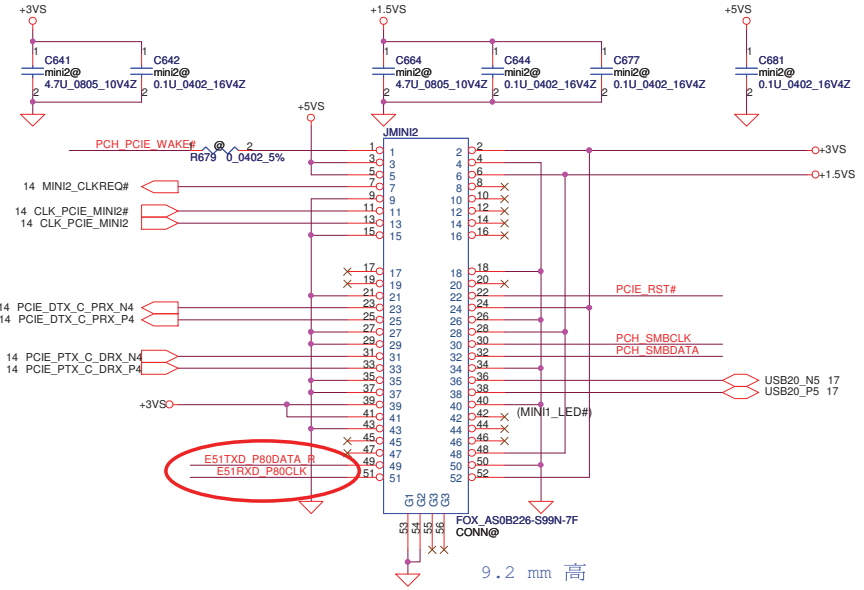
For Wireless LAN



For TV-Tuner/HW MPEG



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2007/12/25

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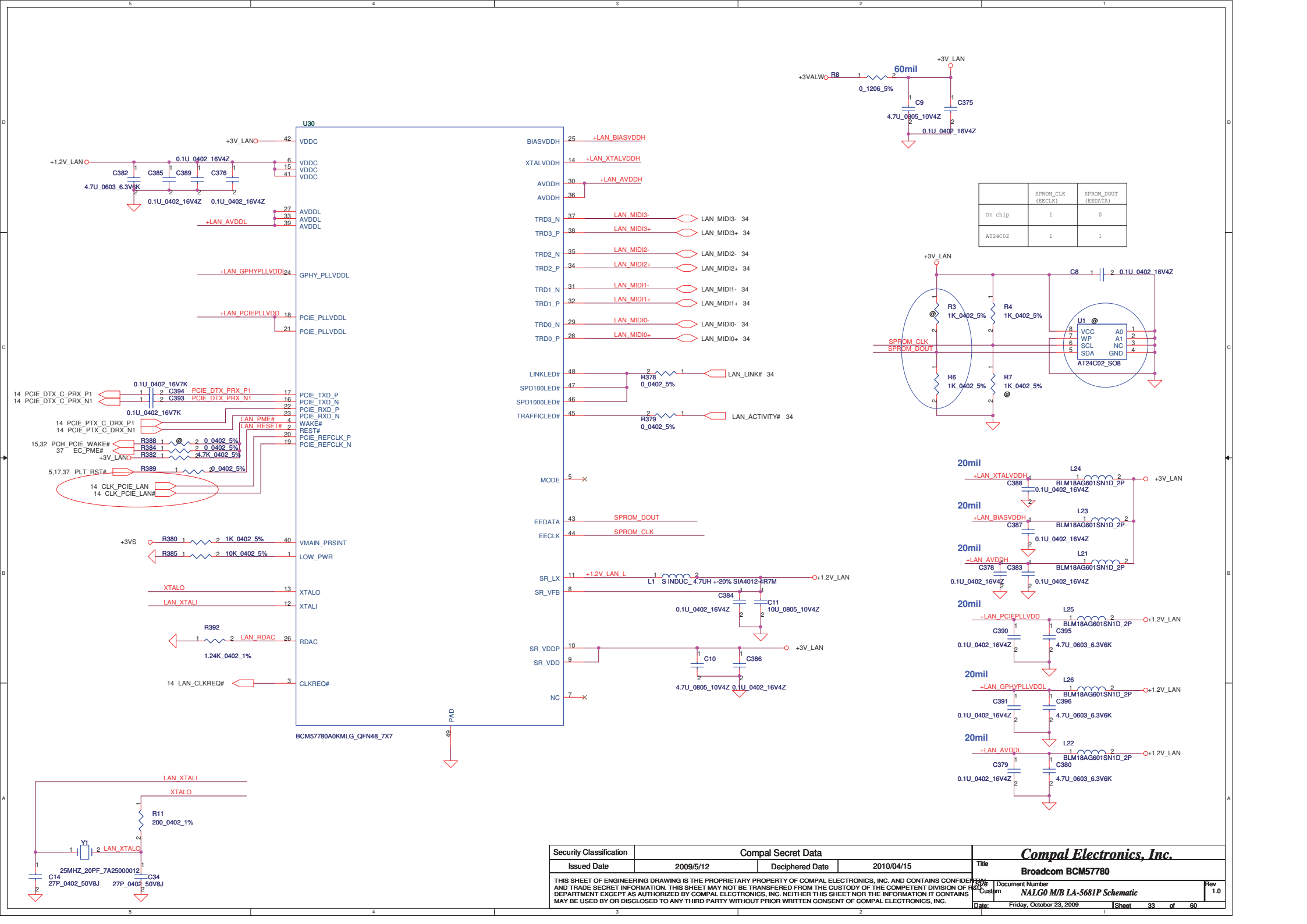
Compal Electronics, Inc.

Title: MINI CARD (WLAN & TV-Tuner)

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 32 of 60



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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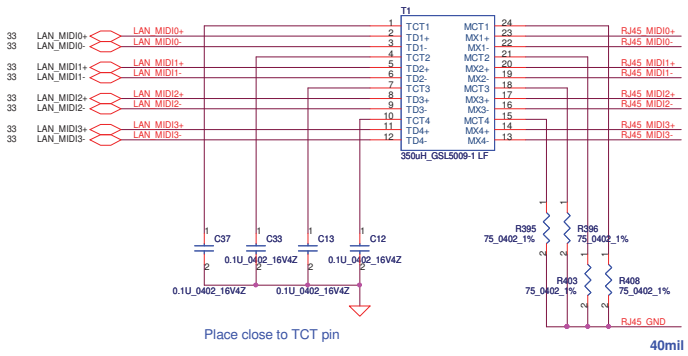
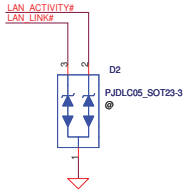
Compal Electronics, Inc.

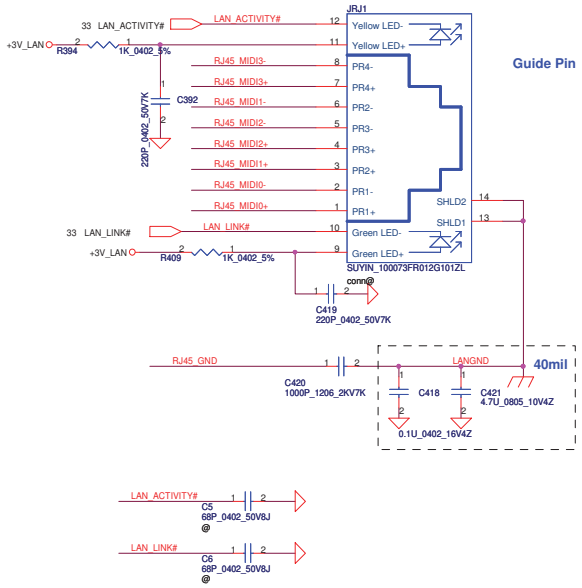
Title: Broadcom BCM57780

Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 33 of 60







Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2010/04/15

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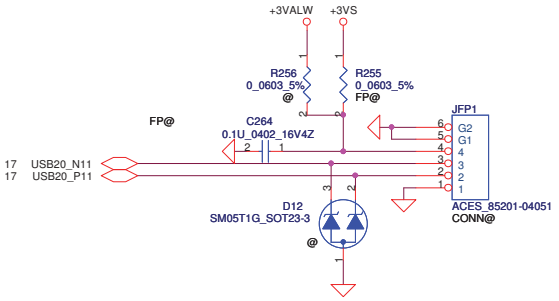
Compal Electronics, Inc.

Title: **LAN Magnetic & RJ45**

Size	Document Number	Rev
	NALG0 M/B LA-5681P Schematic	1.0

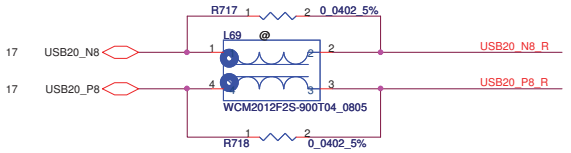
Date: Friday, October 23, 2009 | Sheet 34 of 60

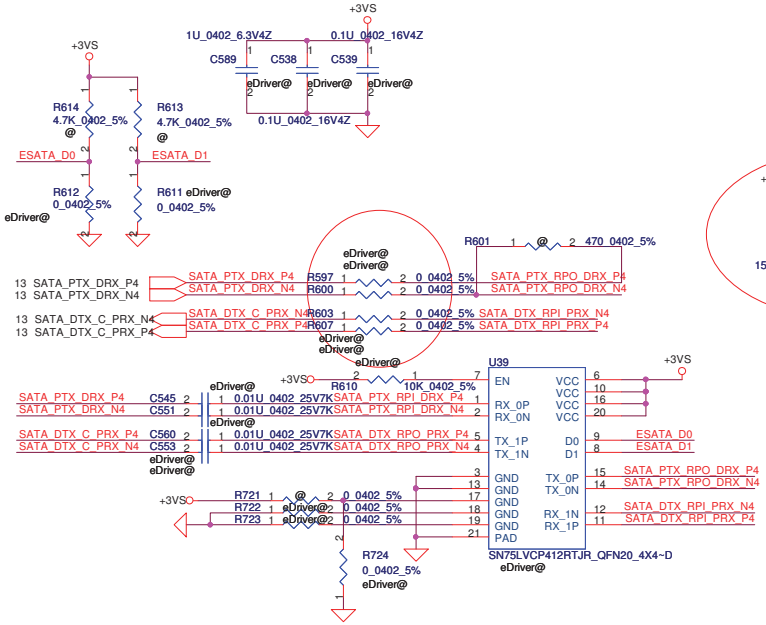
Finger Print Conn.

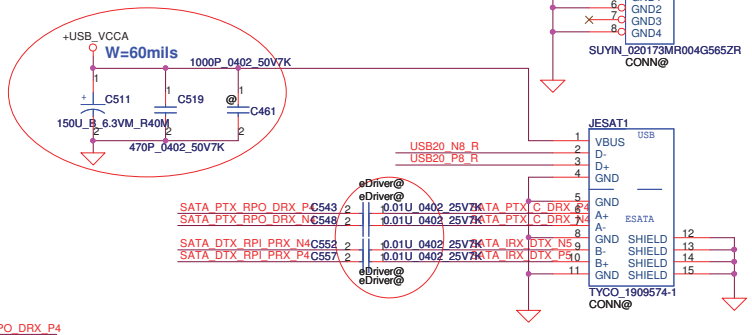


ESATA CONN

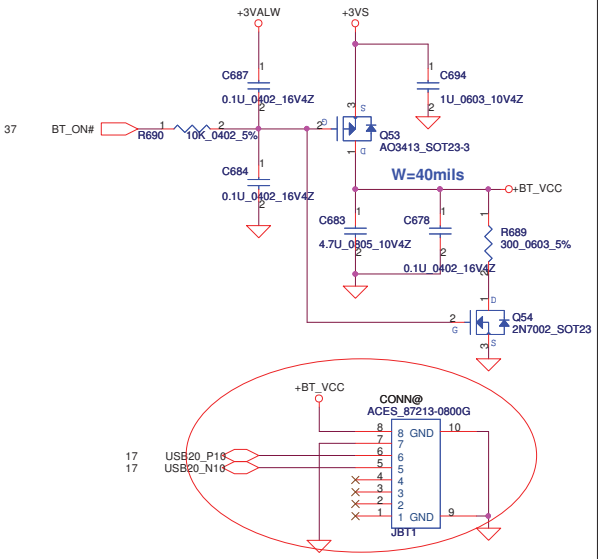
D0	D1	Function
0	0	defalut; CH0/CH1 ->0dB
0	1	CH0->2.5dB pre-emphasis;CH1->0dB
1	0	CH1->2.5dB pre-emphasis;CH0->0dB
1	1	CH0/CH1->2.5dB pre-emphasis



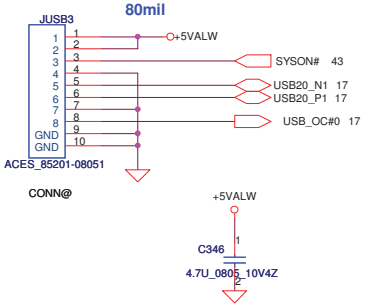




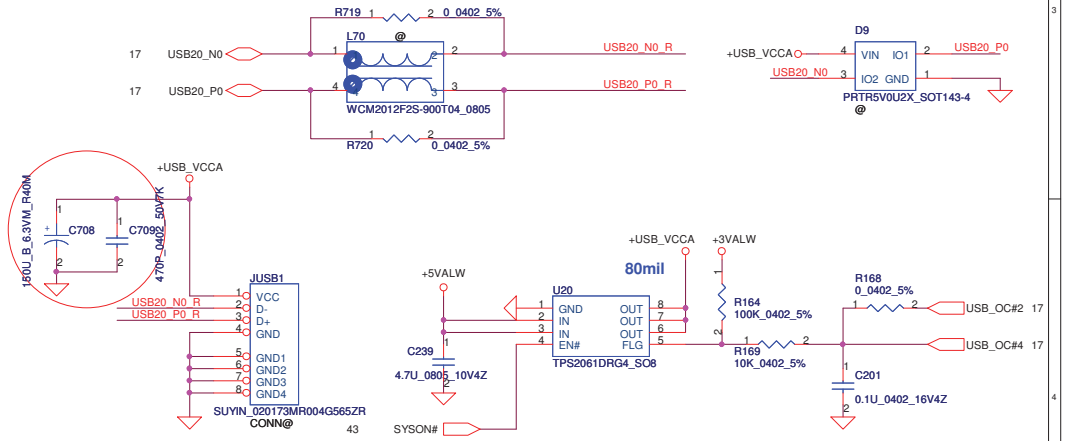
Bluetooth Conn.



To USB/B Connector



USB CONN.



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/12/31

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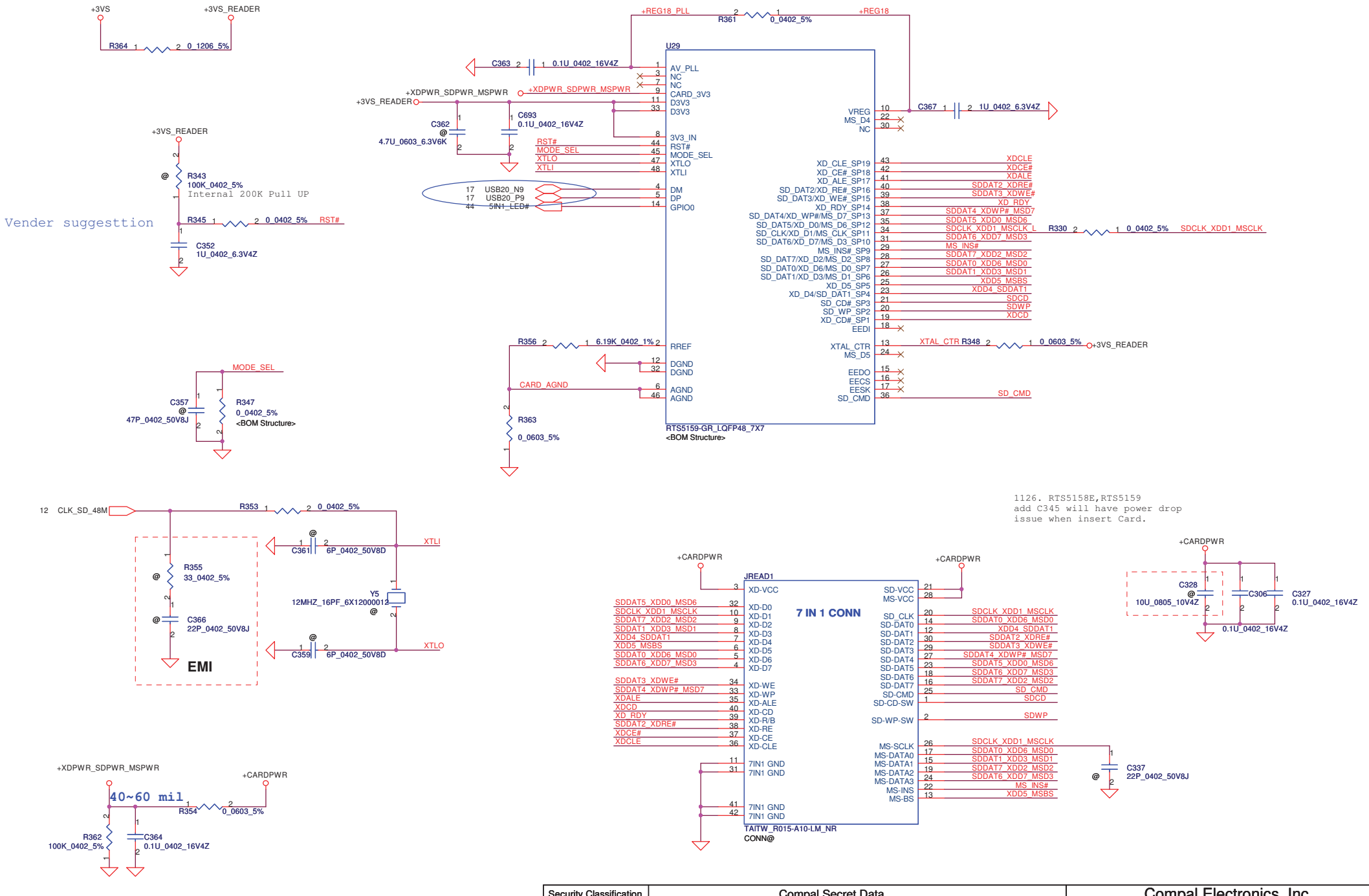
Compal Electronics, Inc.

Title: NEW CARD & eSATA Connector

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 35 of 60



Security Classification	Compal Secret Data		
Issued Date	2009/5/12	Deciphered Date	2009/08/10

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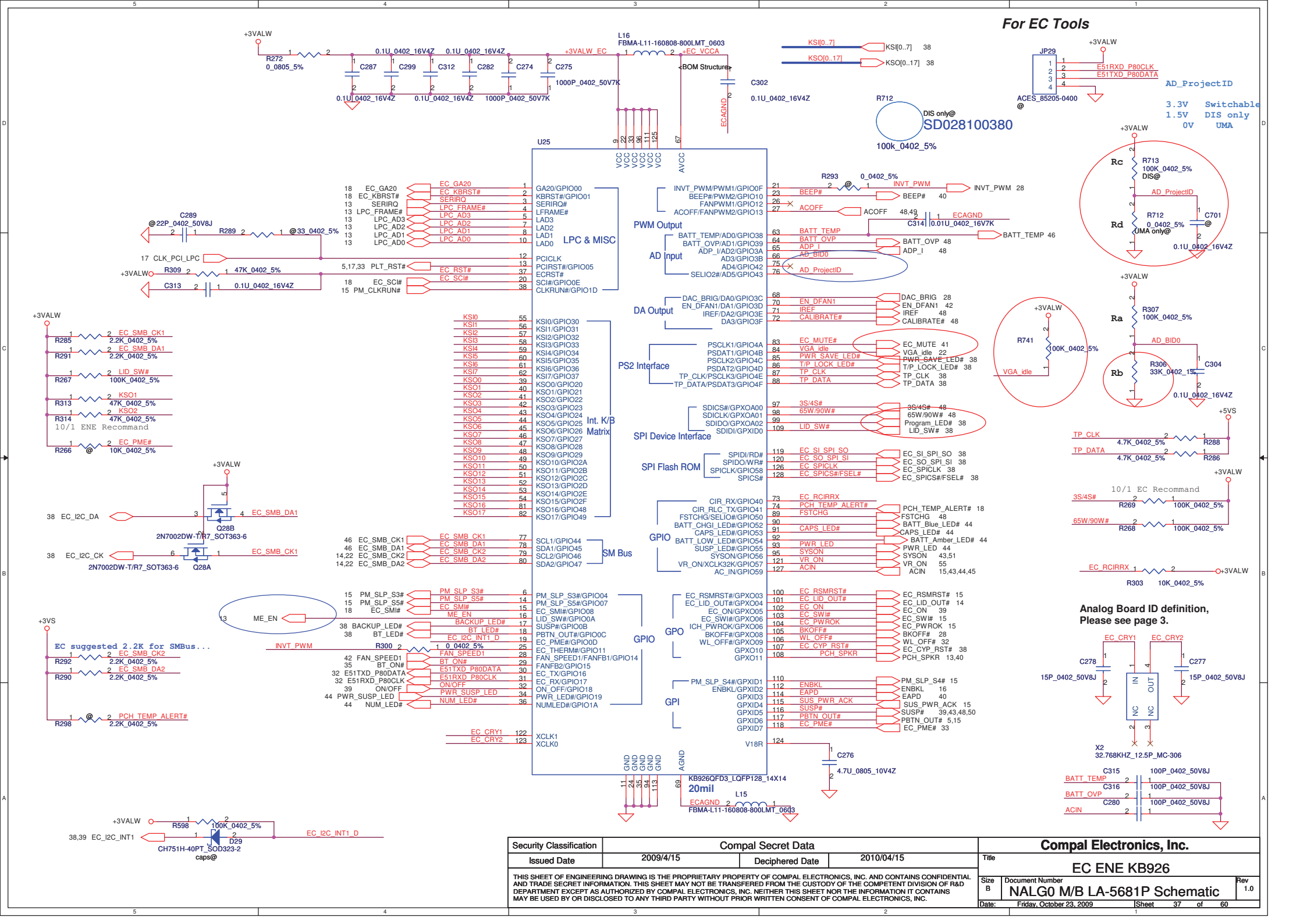
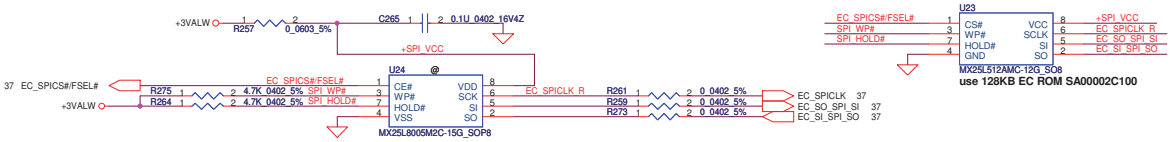
Compal Electronics, Inc.

Title: Card Reader RTS5159

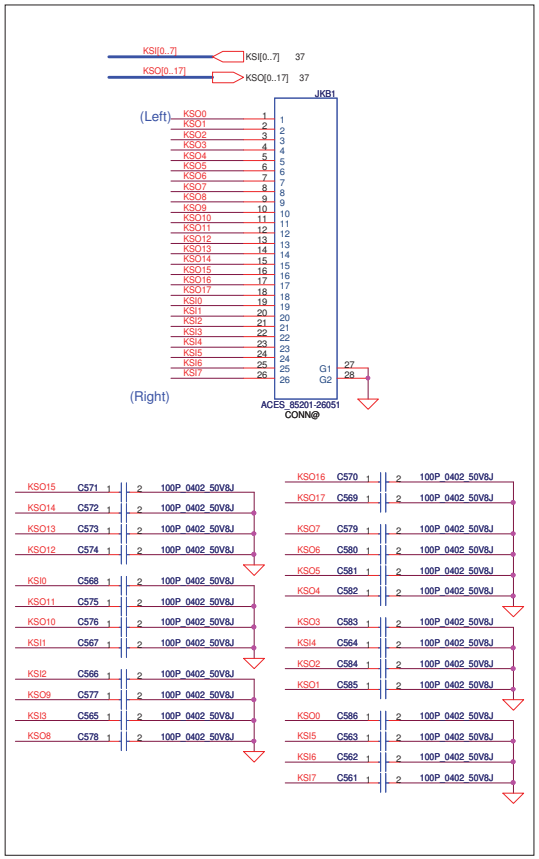
Size: Custom | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 36 of 60

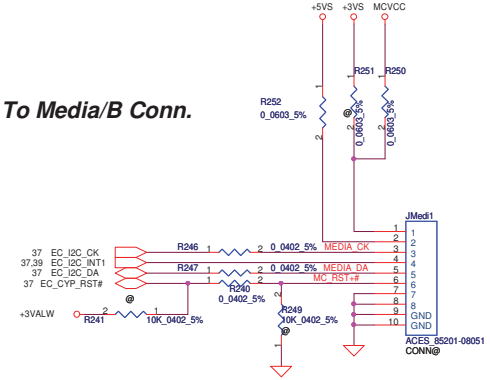

For EC Tools
U25
KB926QFD3_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
AD_ProjectID
3.3V Switchable
1.5V DIS only
0V UMA
SD028100380
100k_0402_5%
Analog Board ID definition, Please see page 3.
EC suggested 2.2K for SMBus...
10/1 ENE Recommand
10/1 EC Recommand
caps@
Security Classification
Compal Secret Data
Issued Date
2009/4/15
Deciphered Date
2010/04/15
Compal Electronics, Inc.
EC ENE KB926
NALG0 M/B LA-5681P Schematic
Rev 1.0
Friday, October 23, 2009
Sheet 37 of 60

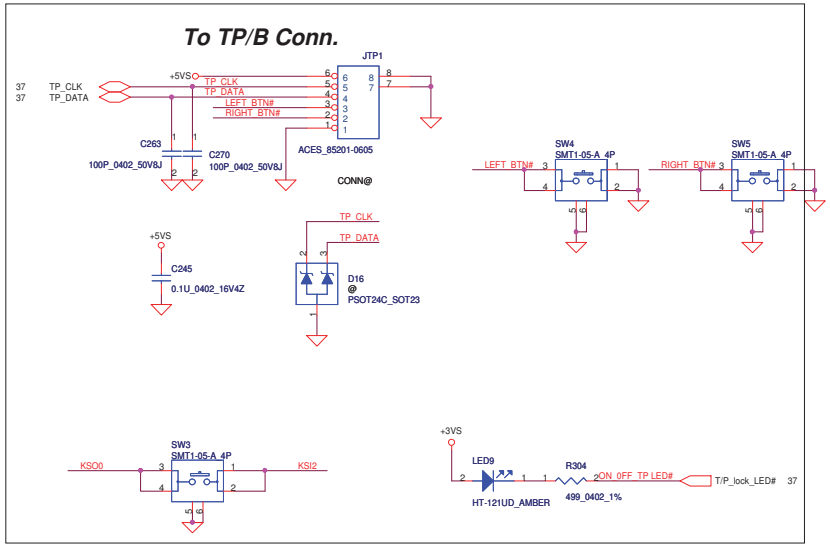


ENE suggestion SPI Frequency over 66MHz
SST: 50MHz
MXIC: 70MHz
ST: 40MHz



To Media/B Conn.



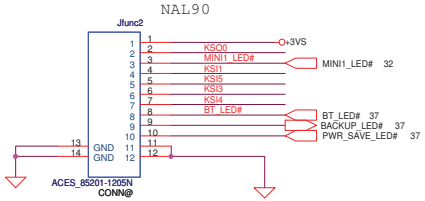


To BTN/B Conn.

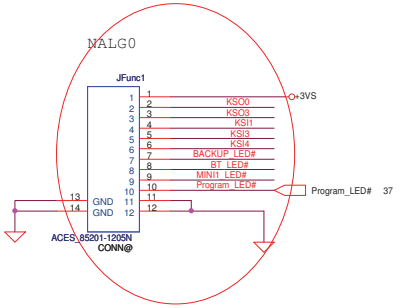
	KSO0	KSO3
KSI1	WL_BTN#	Program_BTN#
KSI2	T/P lock_BTN#	
KSI3	Back up_BTN#	Volum up_BTN#
KSI4	BT_BTN#	Volum down_BTN#
KSI5	Power save_BTN#	

FN/B

NAL90

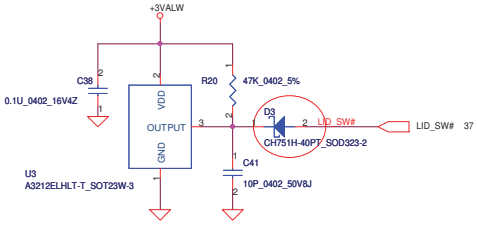


NALG0



Lid Switch

(Hall Effect Switch)



Anpec p/n:SA00003B900

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Compal Electronics, Inc.

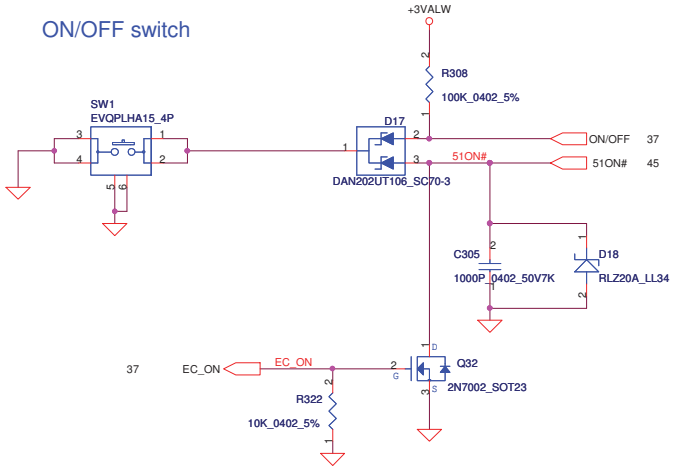
Title: BIOS, I/O Port & K/B Connector

Size: C | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 0.3

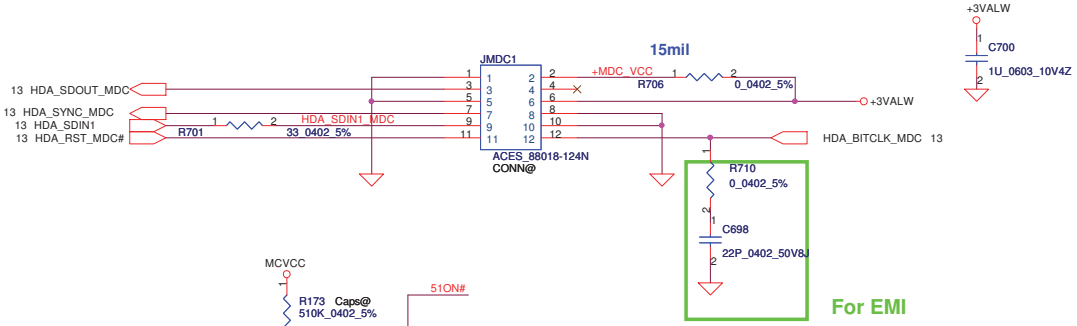
Date: Friday, October 23, 2009 | Sheet 38 of 60

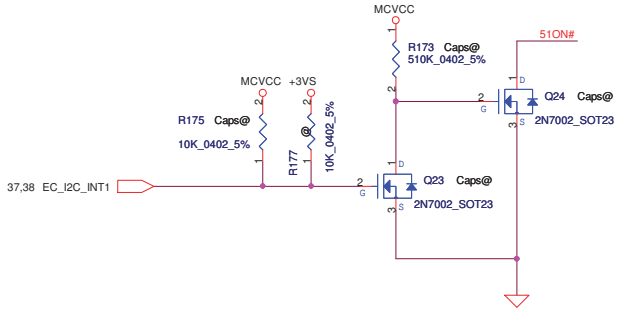
Power Button

ON/OFF switch

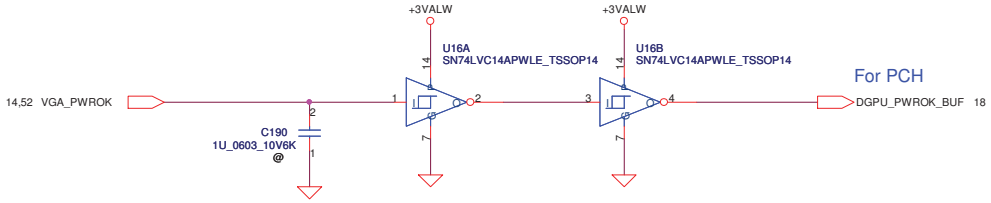


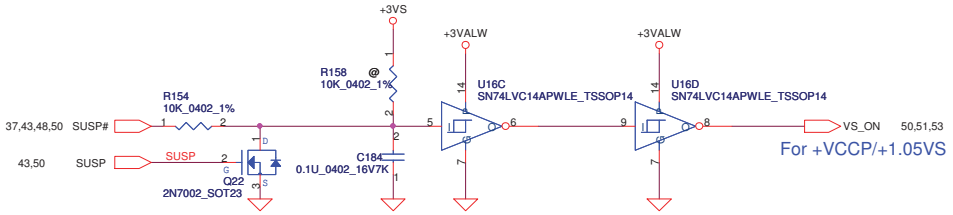
HDA MDC Conn.

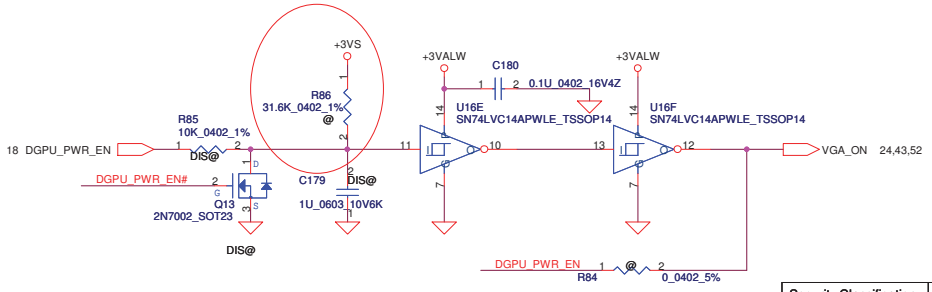


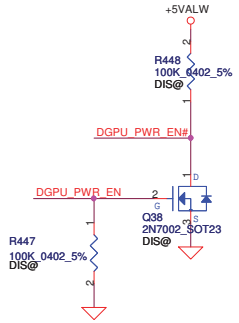


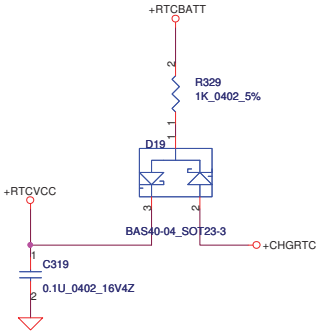
Power ON Circuit











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Compal Electronics, Inc.

Title: Power OK, Reset,RTC, CIR, MDC

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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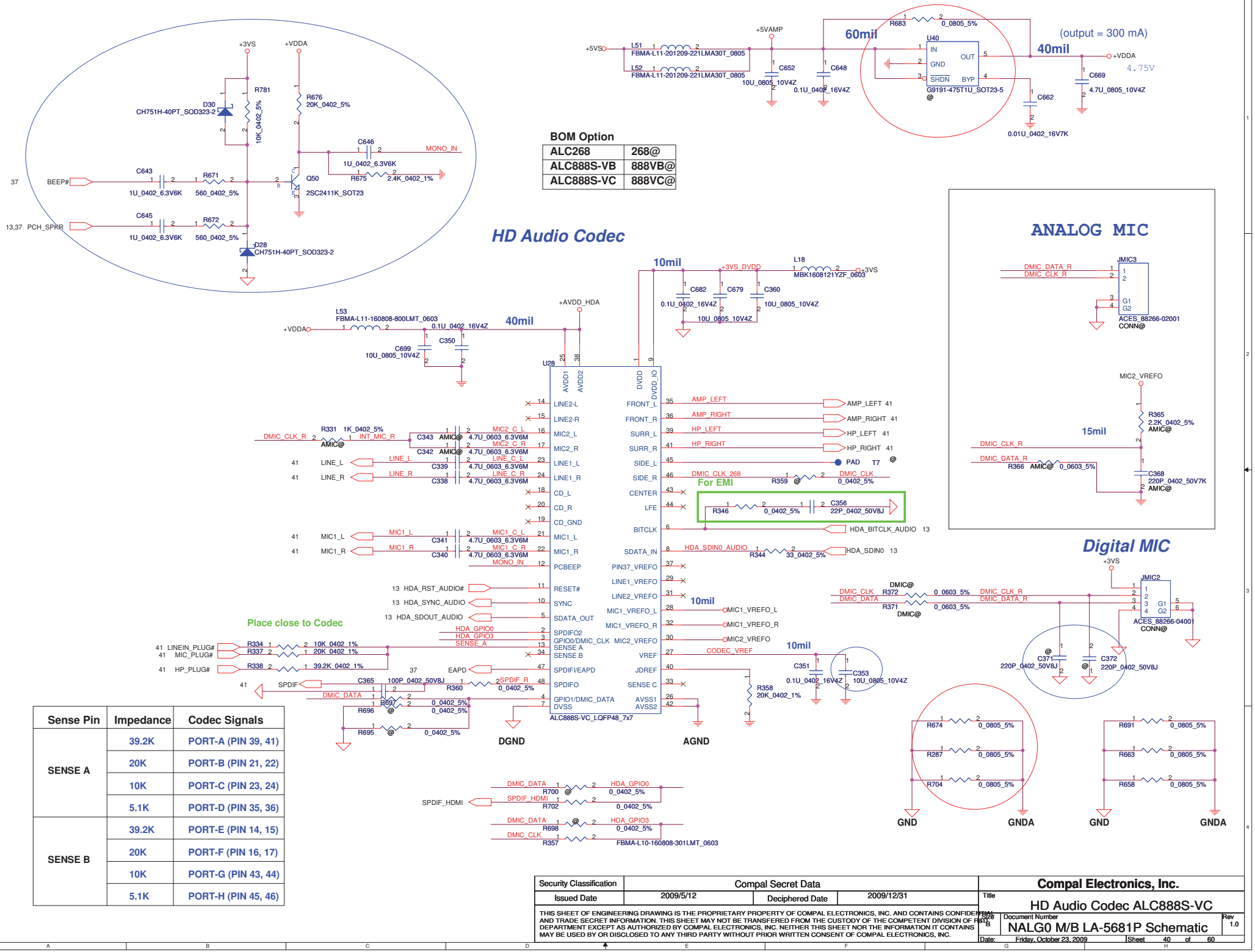

Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)

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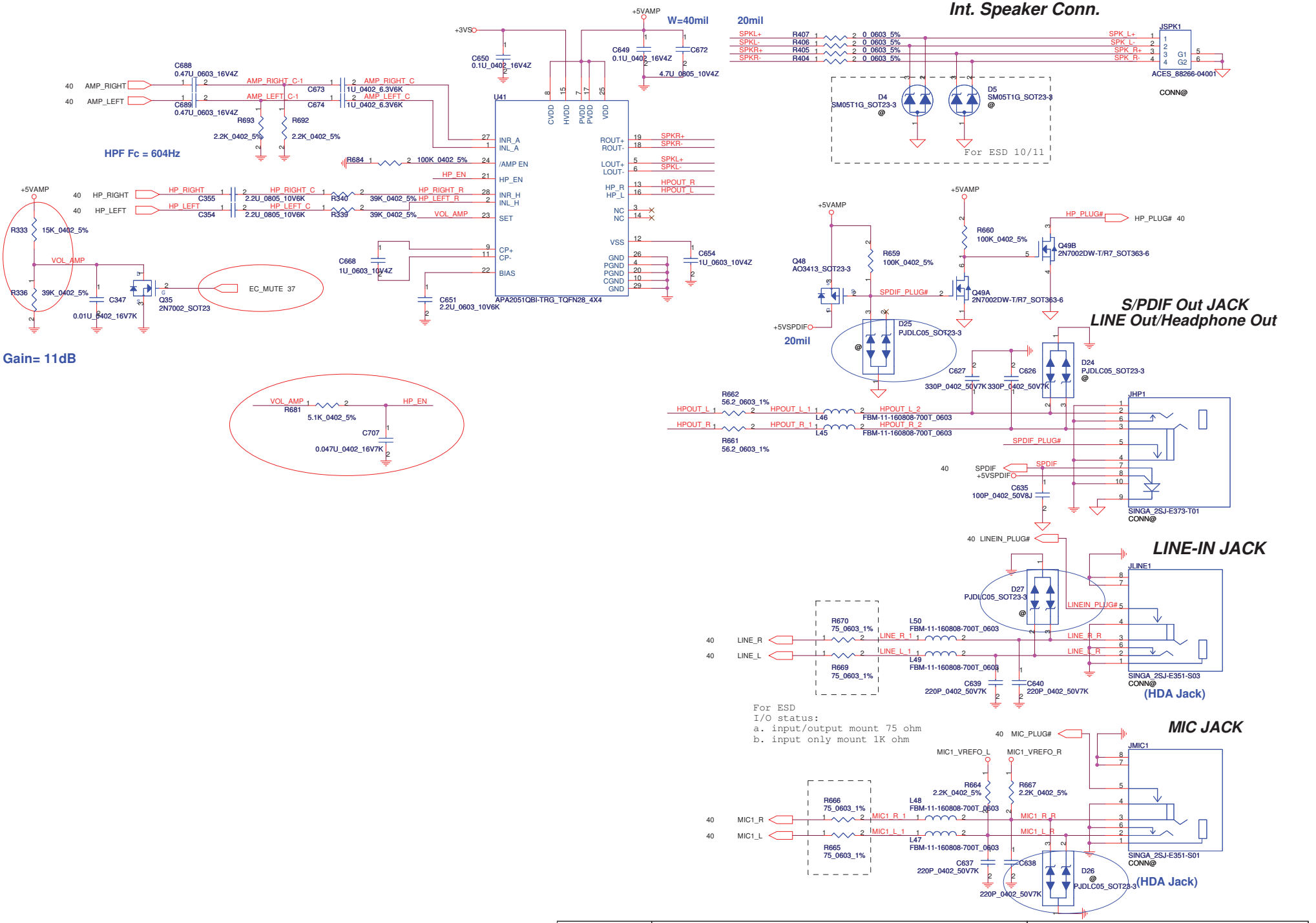
Compal Electronics, Inc.

Title: HD Audio Codec ALC888S-VC

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 40 of 60



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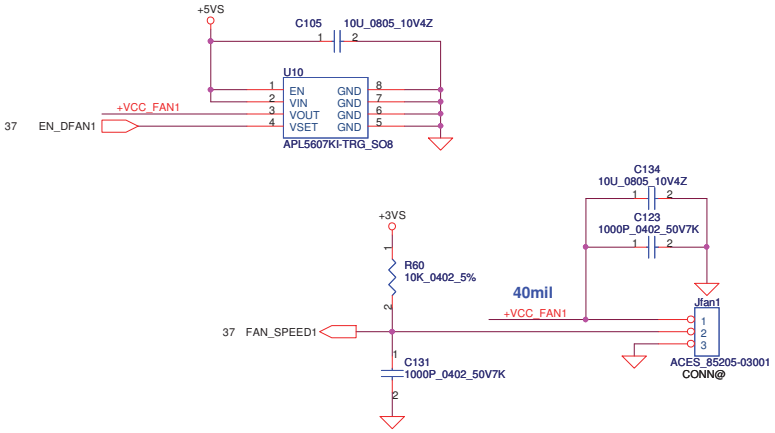
Compal Electronics, Inc.

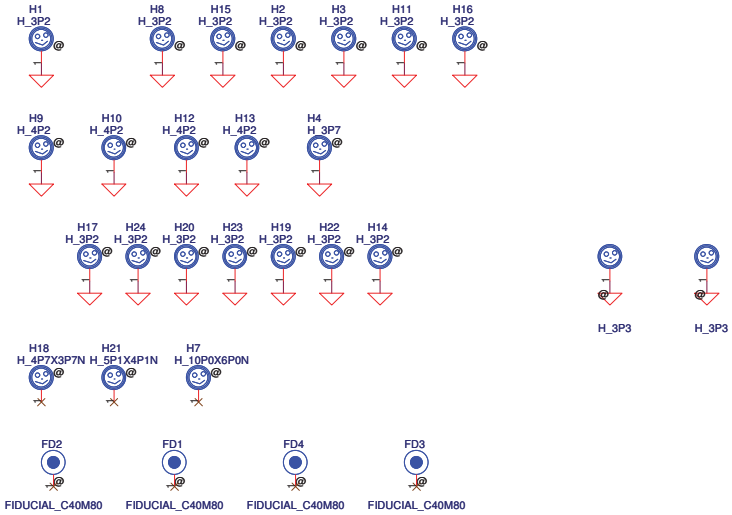
Title: Amplifier & Audio Jack

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

Date: Friday, October 23, 2009 | Sheet 41 of 60

FAN1 Conn





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Compal Electronics, Inc.

Title: FAN & COVER LIGHT& Screw Hole

Size	Document Number	Rev
B	NALG0 M/B LA-5681P Schematic	1.0

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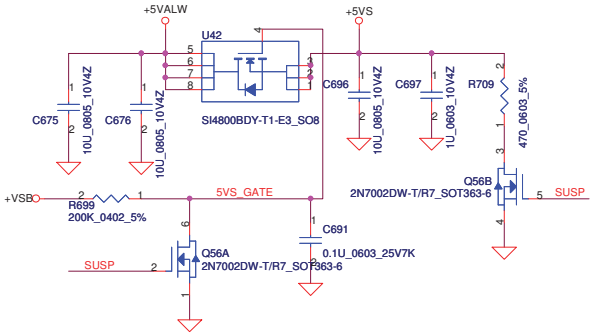
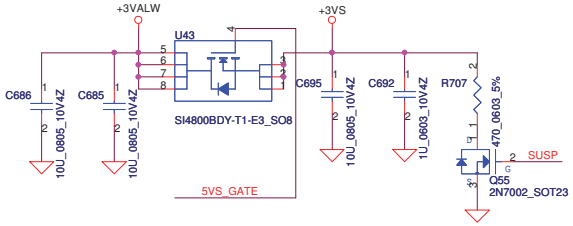
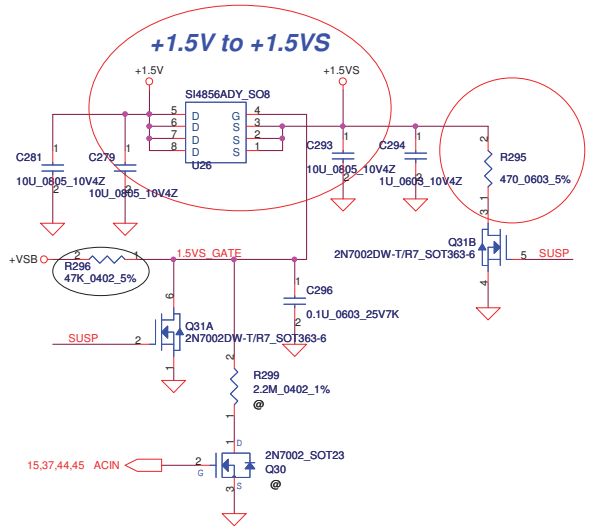
+5VALW TO +5VS



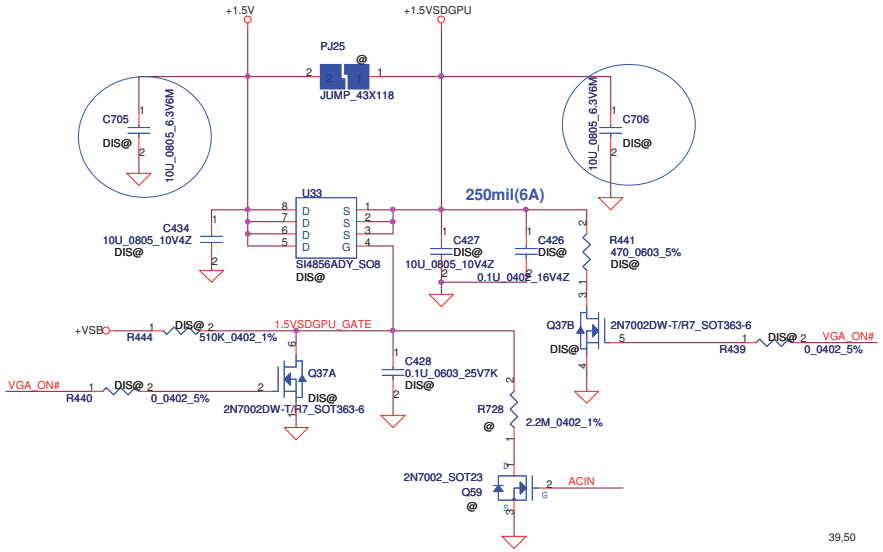
+3VALW TO +3VS



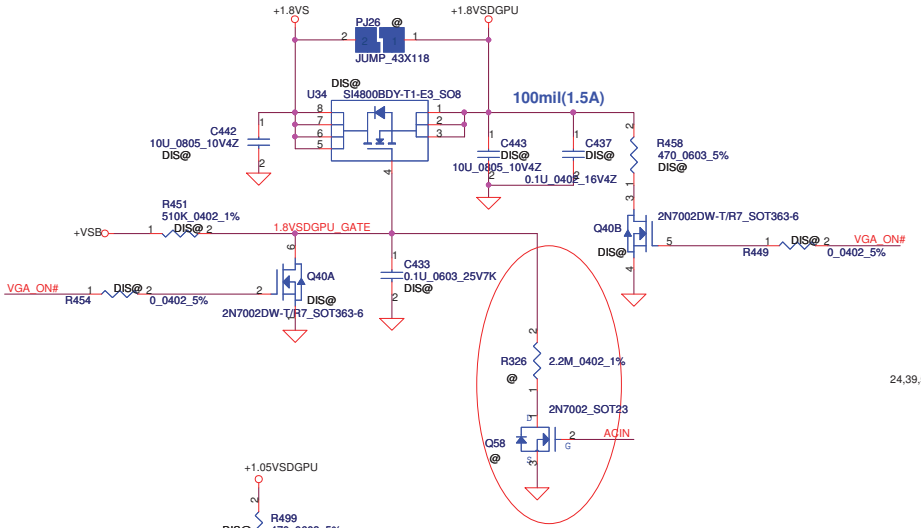
+1.5V to +1.5VS

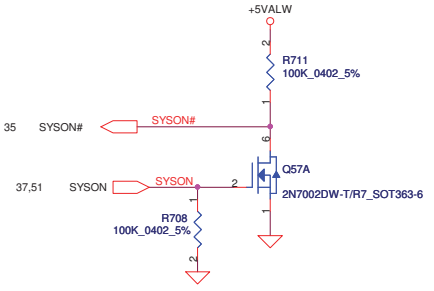


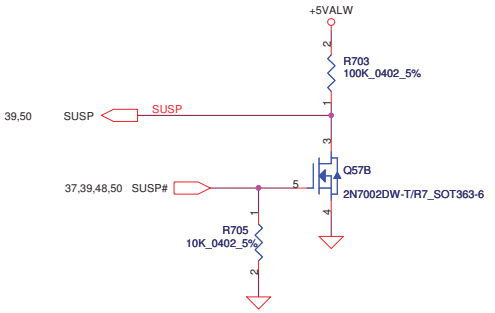
+1.5V to +1.5VSDGPU Transfer

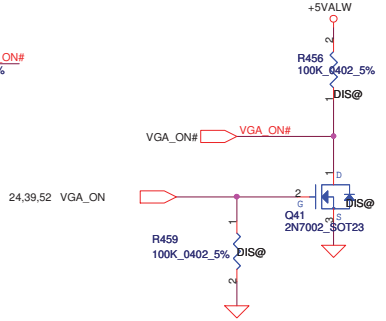


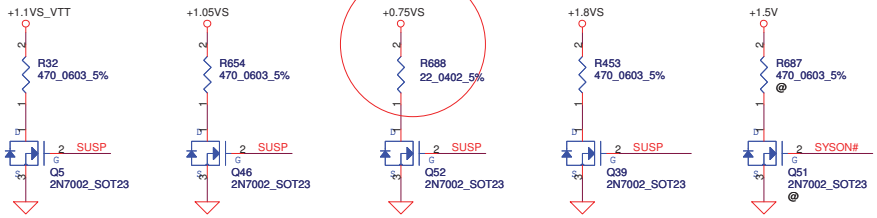
+1.8VS to +1.8VSDGPU Transfer

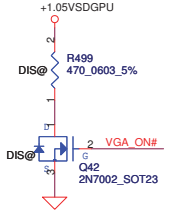












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Compal Electronics, Inc.

Title: DC Interface

Size: B | Document Number: NALG0 M/B LA-5681P Schematic | Rev: 1.0

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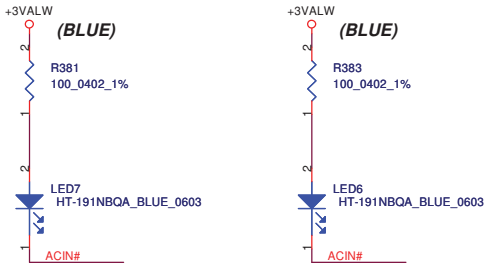
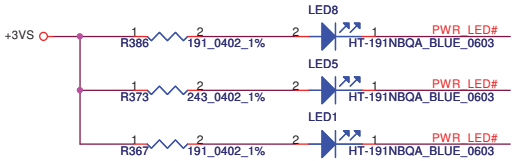
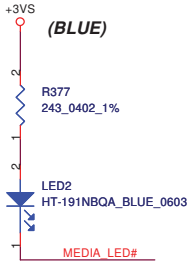
Enlightener LED



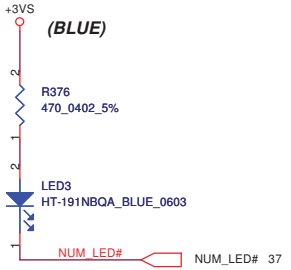
ON/OFF LED LEFT



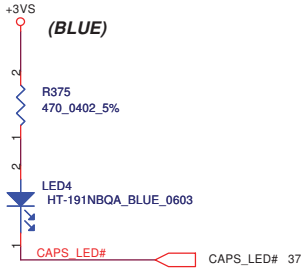
MEDIA_LED

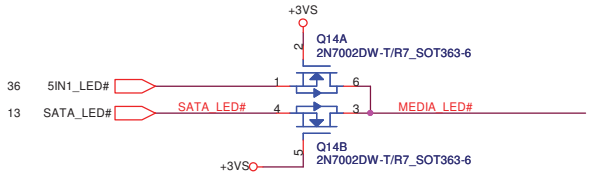


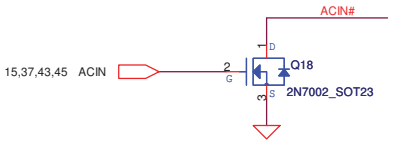
NUM_LED

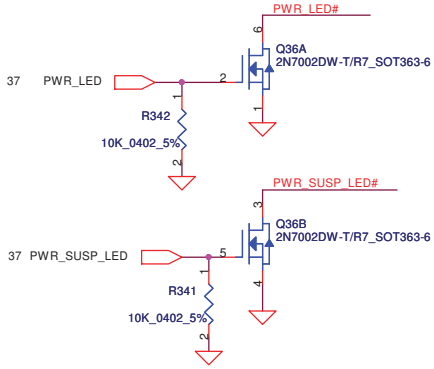


CAPS_LED

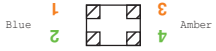


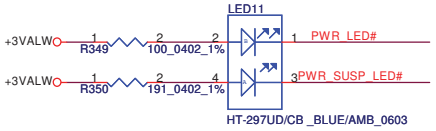


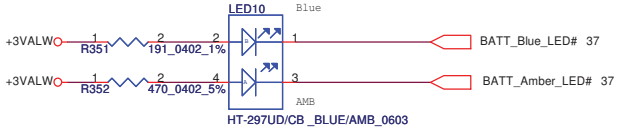




Compal Footprint







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Compal Electronics, Inc.

Title: PWR/B

Size	Document Number	Rev
Custom	NALG0 M/B LA-5681P Schematic	1.0

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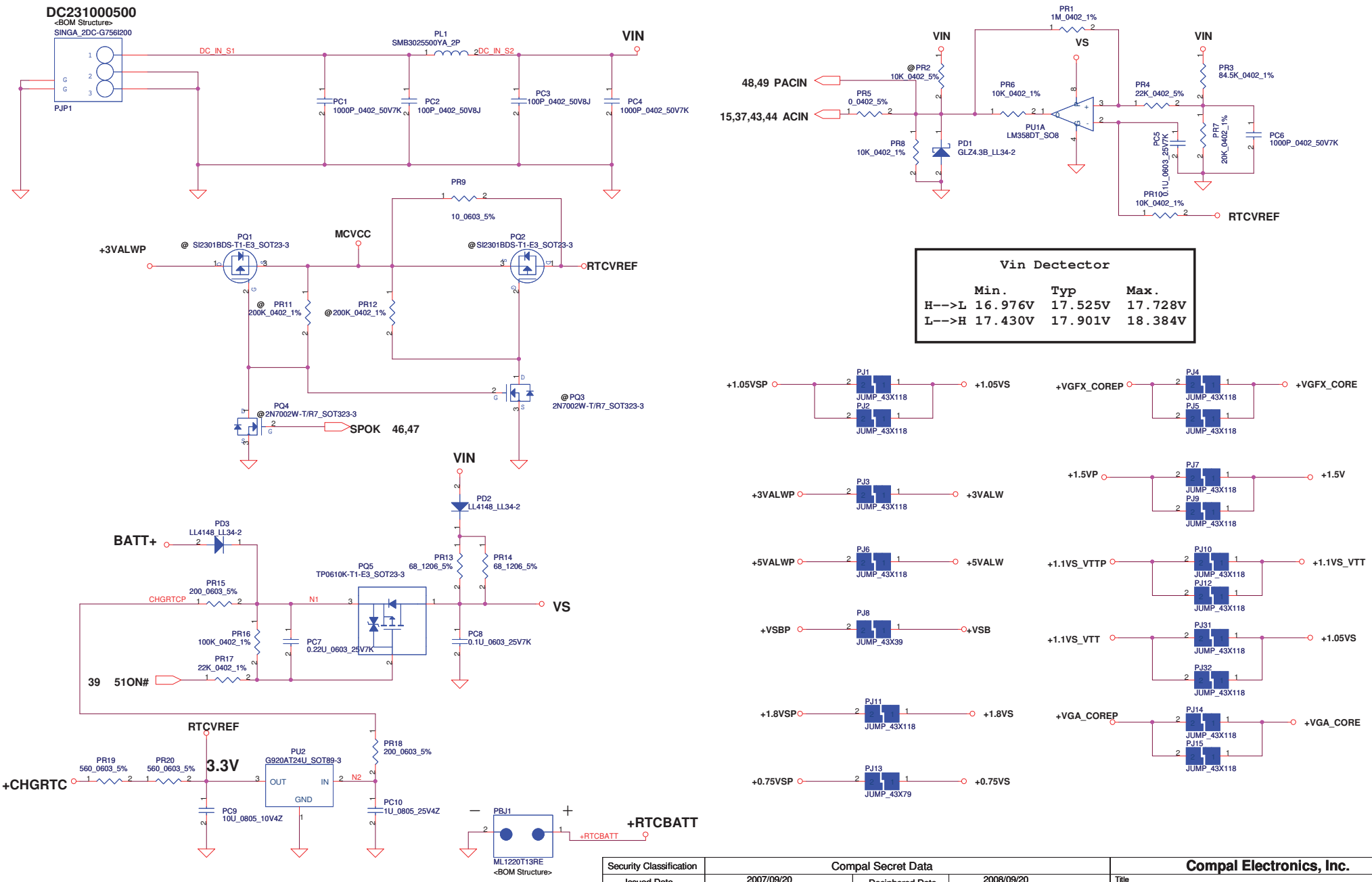

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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: **DCIN & DETECTOR**

Size	Document Number	Rev
Custom	NALG0	0.1

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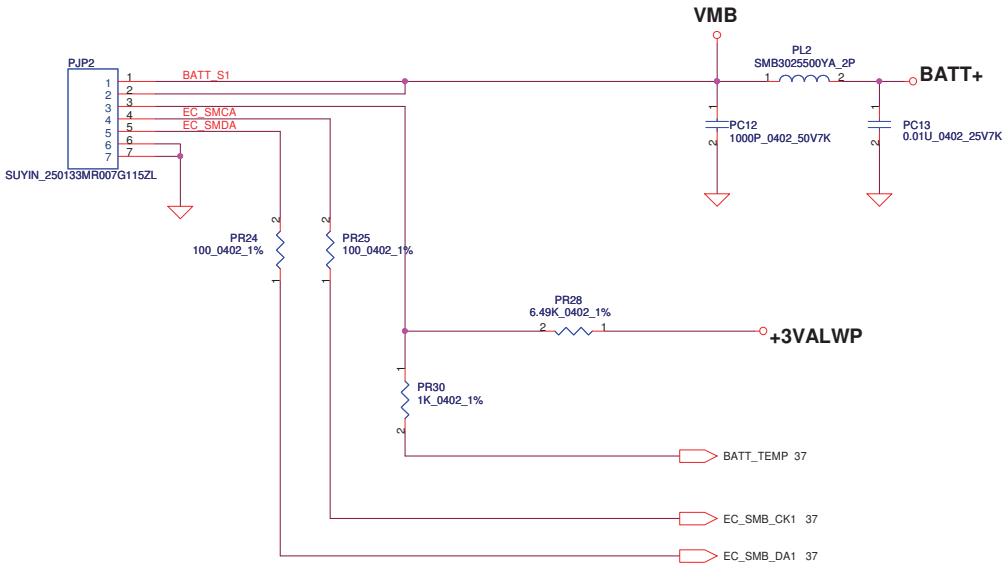
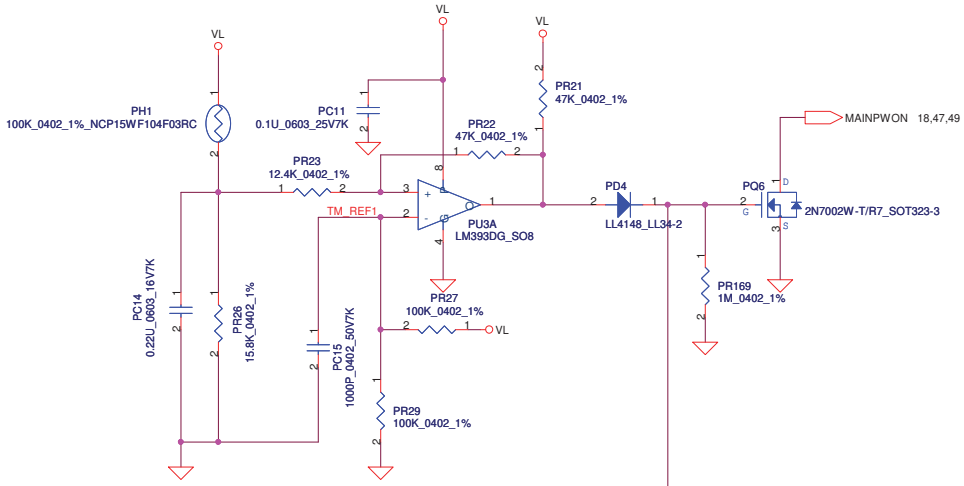
PH1 under CPU botten side :

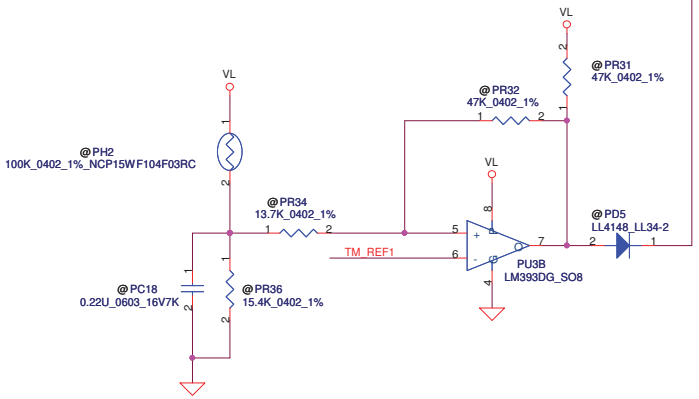
CPU thermal protection at 92 degree C

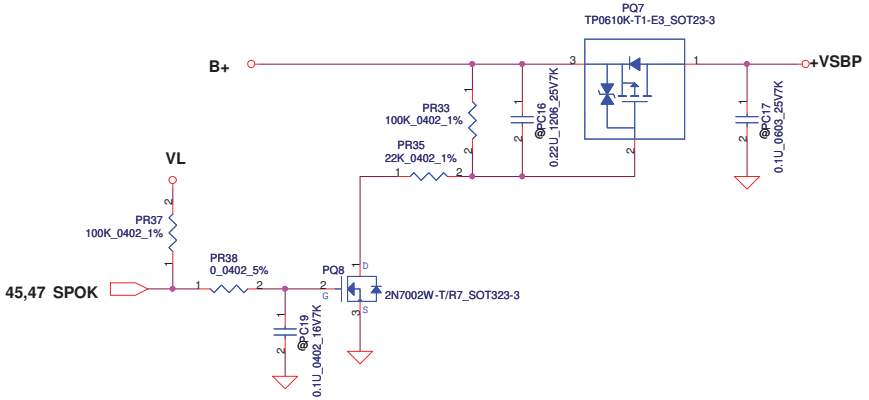




PH2 near main Battery CONN :

BAT. thermal protection at 79 degree C





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Compal Electronics, Inc.

Title: **BATTERY CONN / OTP**

Size	Document Number	Rev
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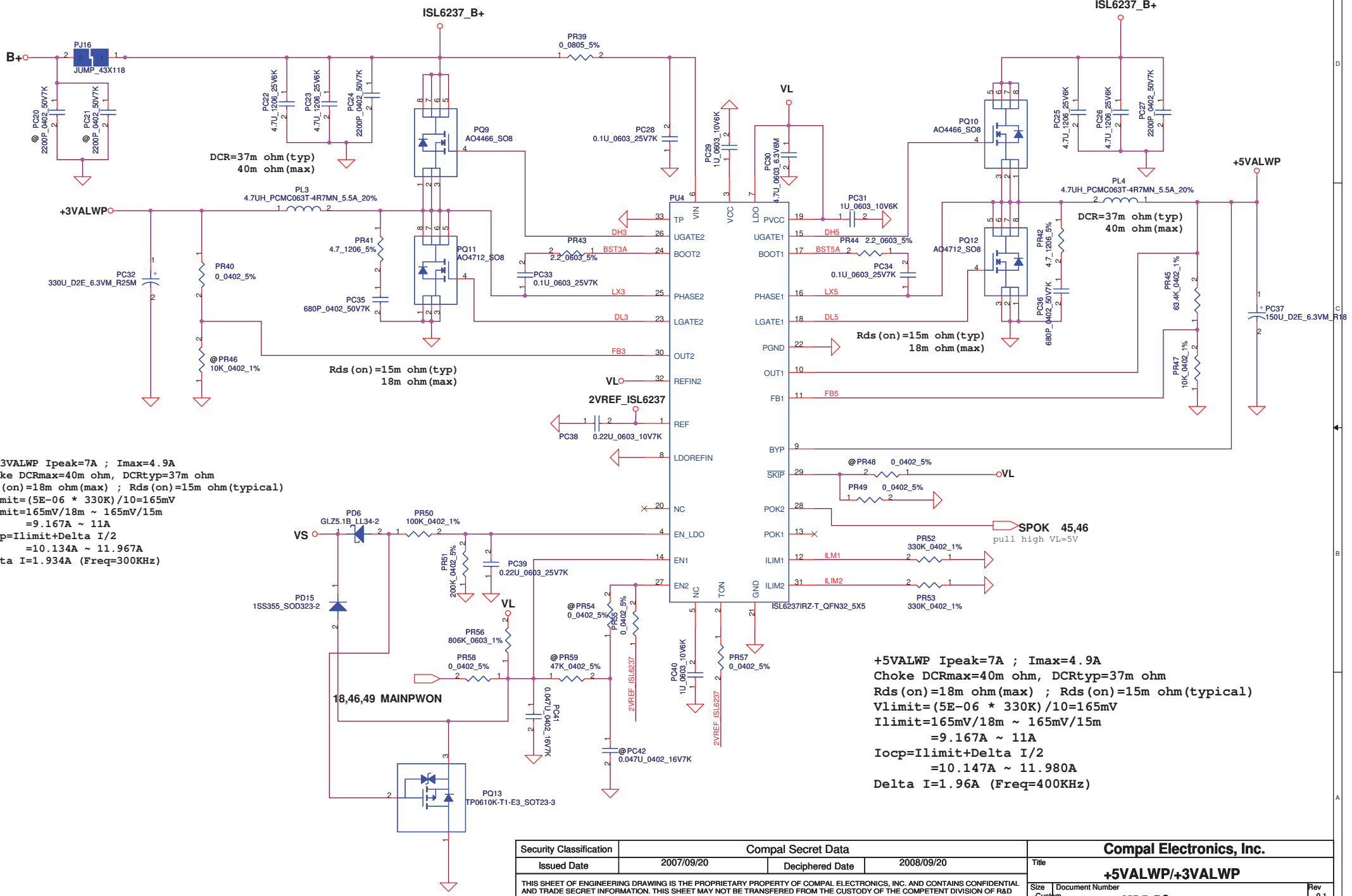

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Compal Electronics, Inc.

Title: +5VALWP/+3VALWP

Size: Custom | Document Number: NALG0 | Rev: 0.1

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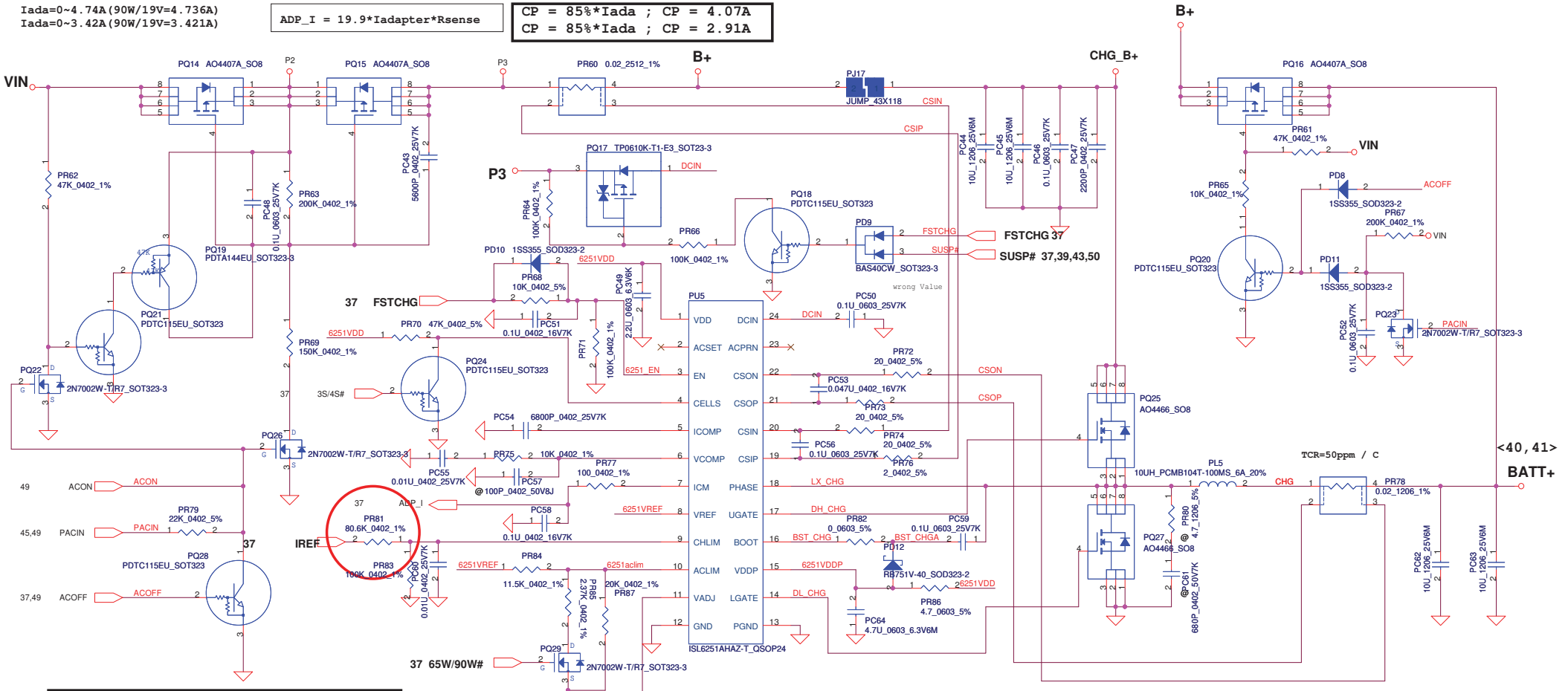
Iada=0~4.74A(90W/19V=4.736A)
Iada=0~3.42A(90W/19V=3.421A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A
CP = 85%*Iada ; CP = 2.91A



CP mode
Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)
where Vaclm=1.502V, Iinput=4.07A

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

LI-3S :13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
Per cell=3.5V

Vcell = (0.175 * Vadj) + 3.99

CALIBRATE#	Pre Cell
3.3V	4.35V
1.899V	4.20V

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

-

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Compal Electronics, Inc.

Title: CHARGER

Size: Custom | Document Number: NALG0 | Rev: 0.1

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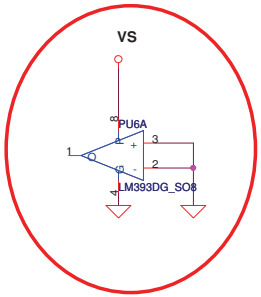

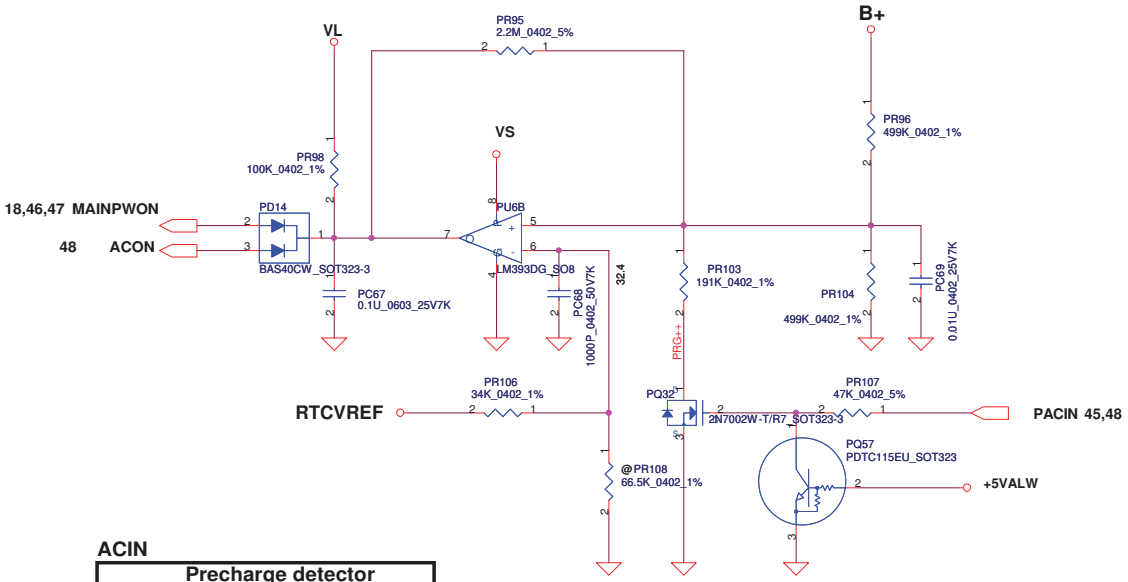

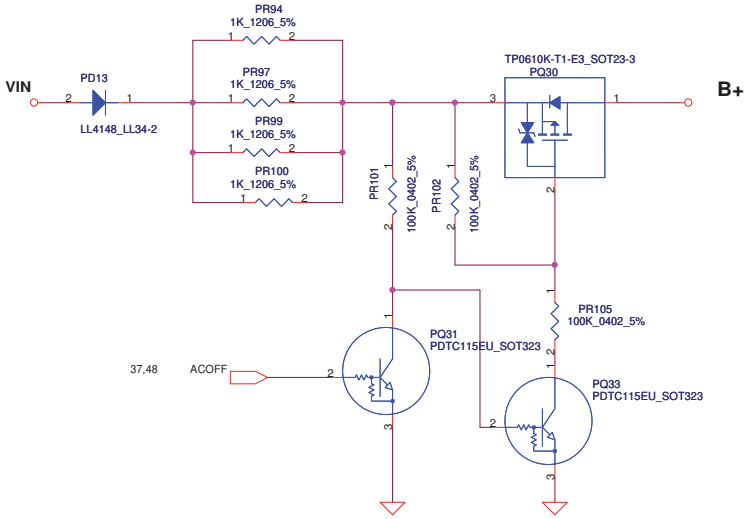

ACIN

Precharge detector	Min.	typ.	Max
H-->L	14.589V	14.84V	15.243V
L-->H	15.562V	15.97V	16.388V

BATT ONLY

Precharge detector	Min.	typ.	Max
H-->L	6.138V	6.214V	6.359V
L-->H	7.196V	7.349V	7.505V

Security Classification	Compal Secret Data		
Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.

Title: **PRECHARGE**

Size	Document Number	Rev
Custom	NALG0	0.1

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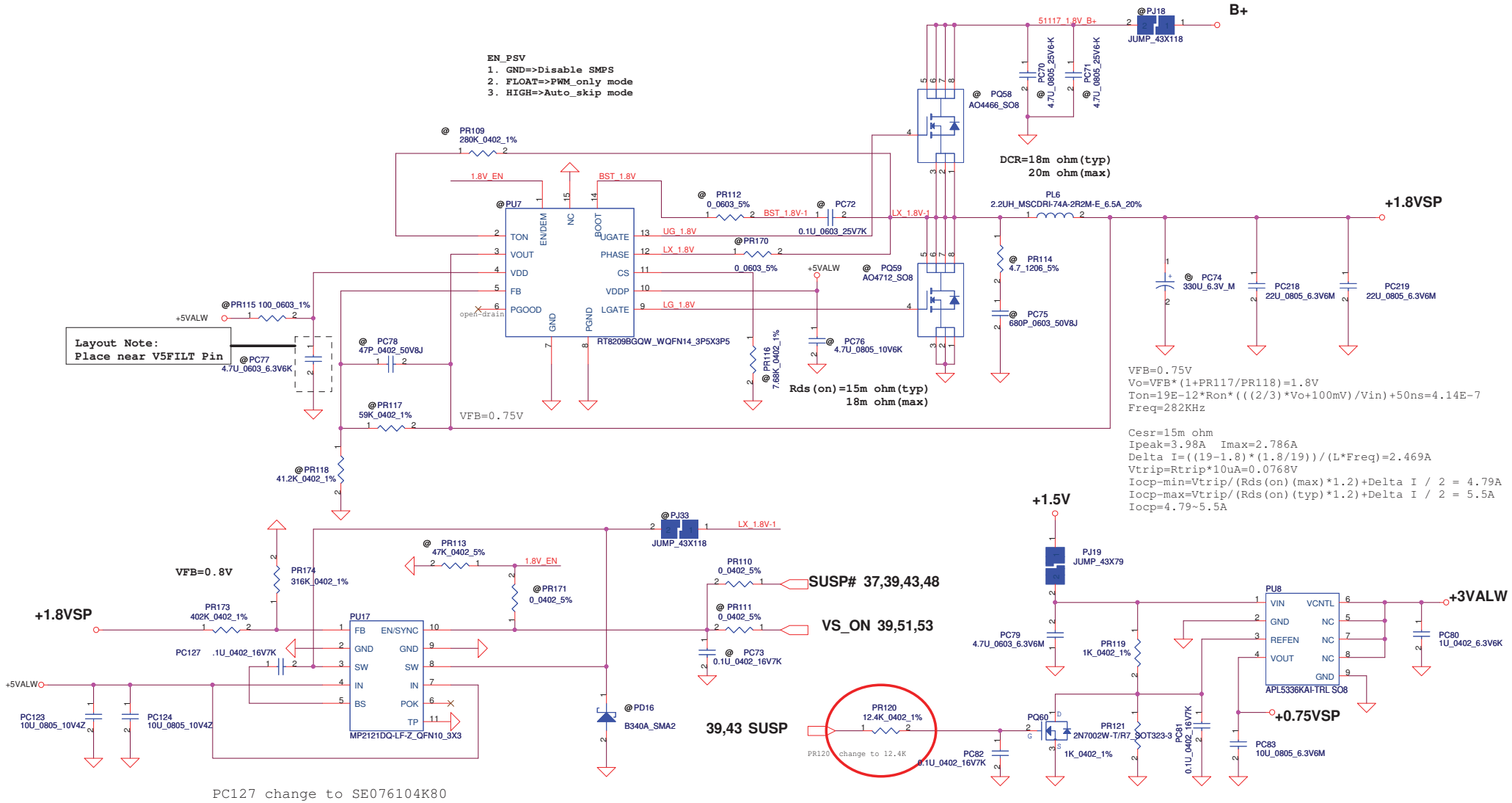

Security Classification	Compal Secret Data		
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Compal Electronics, Inc.

Title: **+1.8VSP/+0.75VSP**

Size	Document Number	Rev
Custom	NALG0	0.1

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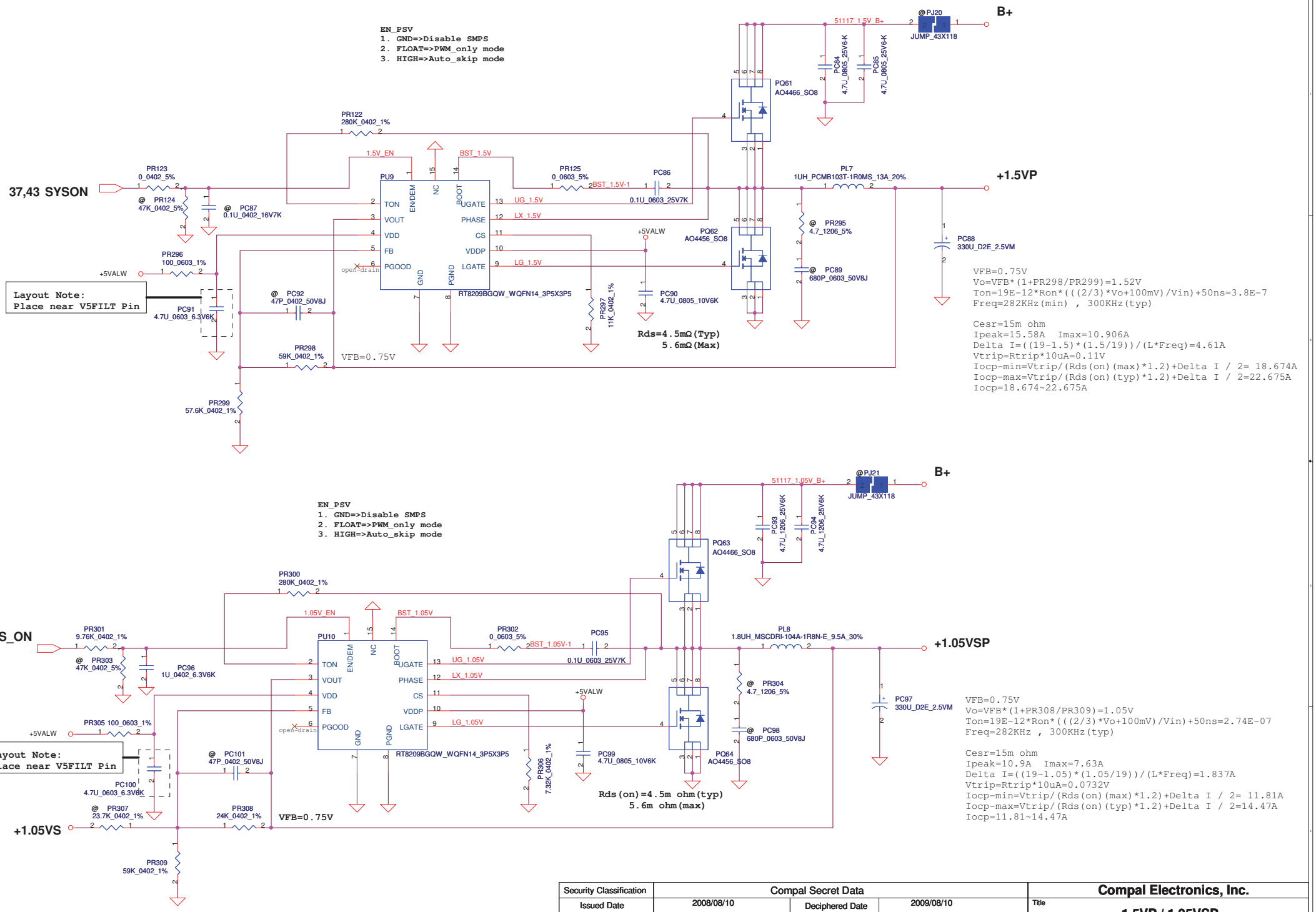

Security Classification	Compal Secret Data		
Issued Date	2008/08/10	Deciphered Date	2009/08/10

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Compal Electronics, Inc.

Title: **1.5VP / 1.05VSP**

Size	Document Number	Rev
Custom	NALG0	0.1

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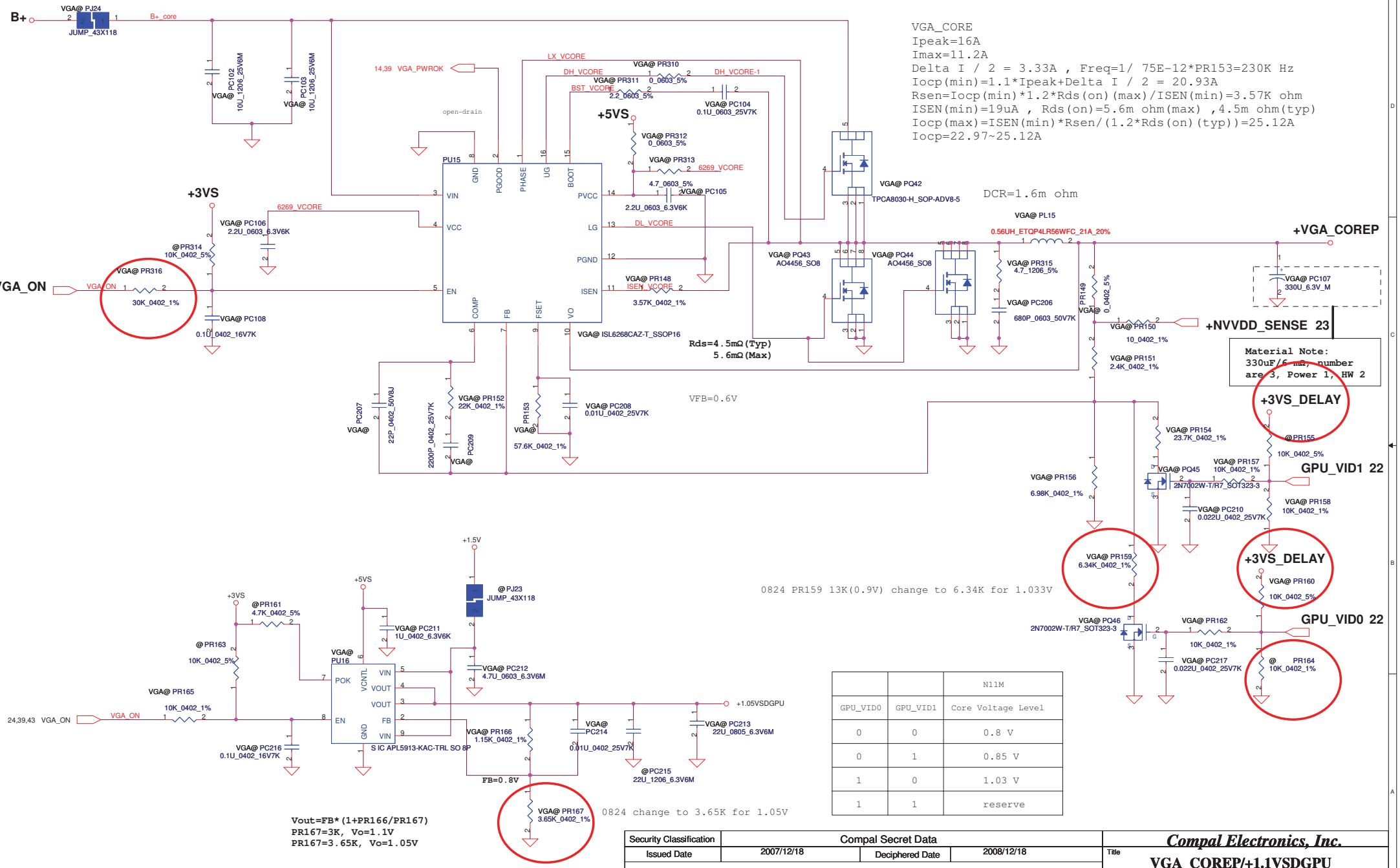

VGA_CORE
Ipeak=16A
Imax=11.2A
Delta I / 2 = 3.33A , Freq=1/ 75E-12*PR153=230K Hz
Iocp(min)=1.1*Ipeak+Delta I / 2 = 20.93A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=3.57K ohm
ISEN(min)=19uA , Rds(on)=5.6m ohm(max) ,4.5m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=25.12A
Iocp=22.97~25.12A

DCR=1.6m ohm

Rds=4.5mΩ(Typ)
5.6mΩ(Max)

VFB=0.6V

Material Note:
330uF/6 m2, number are 3, Power 1, HW 2

0824 PR159 13K(0.9V) change to 6.34K for 1.033V

0824 change to 3.65K for 1.05V

Vout=FB*(1+PR166/PR167)
PR167=3K, Vo=1.1V
PR167=3.65K, Vo=1.05V

		N11M
GPU_VID0	GPU_VID1	Core Voltage Level
0	0	0.8 V
0	1	0.85 V
1	0	1.03 V
1	1	reserve

Security Classification	Compal Secret Data		
Issued Date	2007/12/18	Deciphered Date	2008/12/18

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Compal Electronics, Inc.

Title: VGA_COREP/+1.1VSDGPU

Size: Custom	Document Number: NALG0	Rev: 0.1
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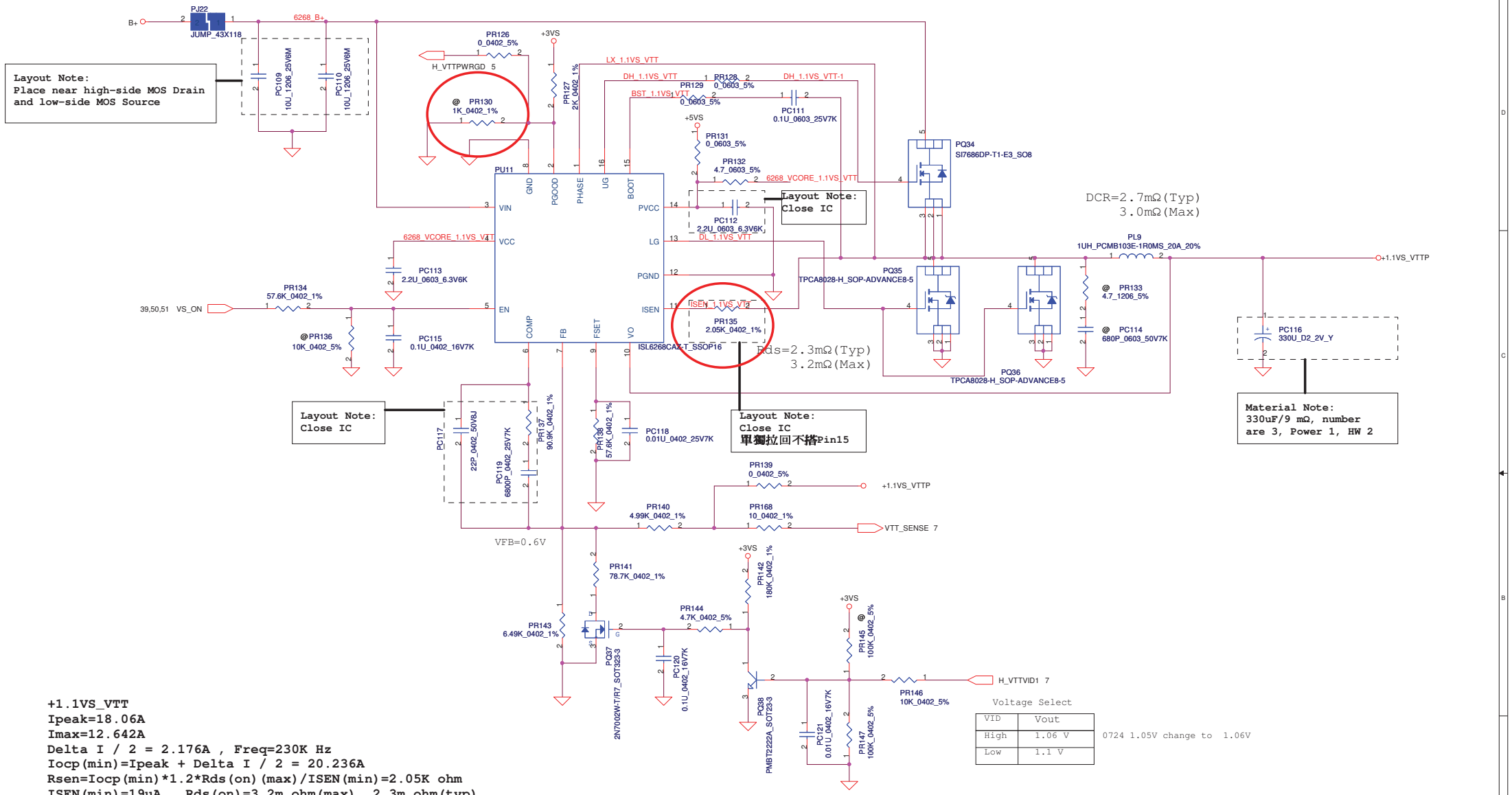

+1.1VS_VTT
Ipeak=18.06A
Imax=12.642A
Delta I / 2 = 2.176A , Freq=230K Hz
Iocp(min)=Ipeak + Delta I / 2 = 20.236A
Rsen=Iocp(min)*1.2*Rds(on)(max)/ISEN(min)=2.05K ohm
ISEN(min)=19uA , Rds(on)=3.2m ohm(max) ,2.3m ohm(typ)
Iocp(max)=ISEN(min)*Rsen/(1.2*Rds(on)(typ))=28.225A
Iocp=20.236~28.225A

Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

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Compal Electronics, Inc.

Title: +1.1VS_VTTP

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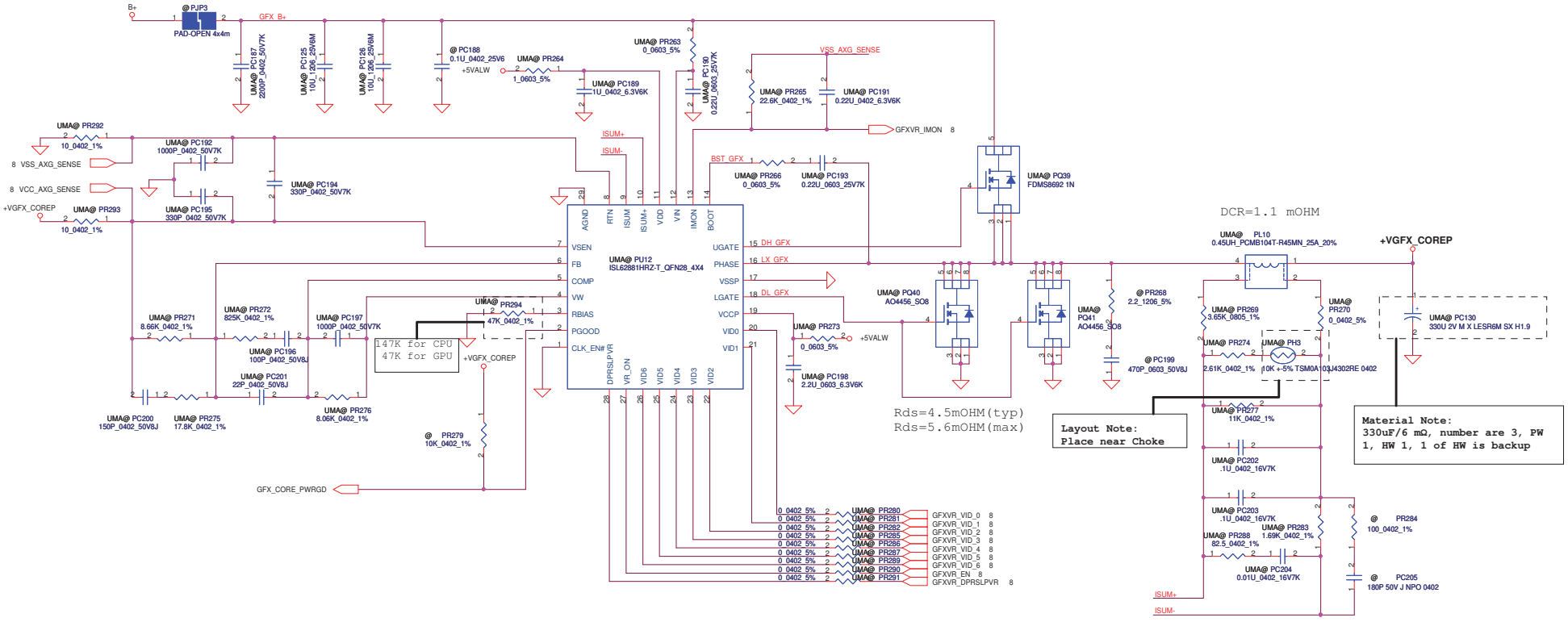
Intel Auburndale CPU(Integrate Graphics) Imax=15A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum)=0.617
where Rn=PR277 // (PR274+PH3)=5.875k ohm
Rsum=PR269=3.65k ohm
LL=2*Rdroop*G1*DCR/Ri= 6.96m V/A
where Rdroop=PR271=8.66k ohm, Ri=PR283=1.69k ohm
Iocp=OCP Threshold*Rdroop/LL=24.89A



Security Classification	Compal Secret Data		
Issued Date	2009/4/15	Deciphered Date	2010/04/15

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Compal Electronics, Inc.

Title: GFX_COREP

Size	Document Number	Rev
C	NALG0	0.1

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Intel Auburndale CPU(Integrate Graphics) , Ipeak = 48A
OCP calculation : Assume DCR=1.1m ohm
G1=Rn/(Rn+Rsum/2)=0.763
where Rn=PR258 // (PR251+PH6)=5.875k ohm
Rsum=PR221, PR253 =3.65k ohm
LL = 2*Rdroop*G1*(DCR/2)/Ri = 1.81mV/A
where Rdroop=PR239=2.61k ohm , Ri=PR256=1.21k ohm
Iocp= OCP Threshold*Rdroop/LL=40E-06*2.61E03/1.81E-03=57.68A

Layout Note:
PH5 place near Phase1 L-MOS

Layout Note:
Place near Phase1 Choke

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Issued Date	2009/4/15	Deciphered Date	2010/04/15

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Compal Electronics, Inc.

Title: +CPU_CORE

Size	Document Number	Rev
C	NALG0	0.1

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Modify chager circuit	design change	0.1	48	Change PR60 to SD000001F00(0.02_2512_1%) Cahnge PR115 to SD014100080 (S RES 1/10W 100 +-1% 0603)	09/06/23	EVT
2	Modify 1.8V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	50	Cahnge PC77 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
3	Modify 1.5V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Cahnge PR296 to SD014100080 (S RES 1/10W 100 +-1% 0603) Cahnge PC91 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
4	Modify 1.05V V5FILT PIN	Avoid 2'nd source RT8209B can no power on	0.1	51	Cahnge PR305 to SD014100080 (S RES 1/10W 100 +-1% 0603) Cahnge PC100 to SE107475K80 (S CER CAP 4.7U 6.3V K X5R 0603)	09/07/21	DVT
5	Modify VGA_COREP circuit	design change	0.1	52	Cahnge PR149 to SD028000080 (S RES 1/16W 0 +-5% 0402) Cahnge PR150 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
6	Modify +1.1VS_VTTP circuit	design change	0.1	53	Cahnge PR139 to SD028000080 (S RES 1/16W 0 +-5% 0402) Cahnge PR168 to SD034100A80 (S RES 1/16W 10 +-1% 0402)	09/06/23	EVT
7	Modify OTP circuit	Link right component	0.1	46	Add PH1 to SL210031F00 (S THERM_ 100K +-1% TH11-4H104FT 0603)	09/06/25	EVT
8	Modify 5V/3V circuit	Delete component	0.1	47	Delete PC42 to SE076473K80 (S CER CAP .047U 16V K X7R 0402)	09/06/25	EVT
9	Modify 1.1VSDGPU circuit	design change	0.1	52	Change PU16, PR165, PR166, PR167, PC211, PC212, PC213, PC214, PC215, PC216 BOM structure to VGA@	09/06/26	EVT
10	Modify chager circuit	design change	0.1	48	Change PR78 to SD012200D80(S RES 1/2W 0.02 +-1% 1206)	09/06/26	EVT
11	Modify VGA_COREP circuit	design change(Voltage Level)	0.1	52	Cahnge PR151 to SD034240180 (S RES 1/16W 2.4K +-1% 0402) Cahnge PR156 to SD000002680 (S RES 1/16W 6.98K +-1% 0402)	09/06/30	EVT
12	Modify VGA_COREP circuit	design change(Voltage Level)	0.1	52	Cahnge PR154 to SD034237280 (S RES 1/16W 23.7K +-1% 0402) Cahnge PR159 to SD034130280 (S RES 1/16W 13K +-1% 0402)	09/06/30	EVT
13	Modify OTP circuit	design change	0.2	46	Cahnge PQ6 to SB000006800 (S TR 2N7002W T/R7 1N SOT-323) Add PR169 to SD034100480 (S RES 1/16W 1M +-1% 0402)	09/07/13	DVT
14	Modify 1.5VP circuit	design change	0.2	51	Change PL7 to SH000009U00(S COIL 1UH +-20% FDUE1040D-1R0M=P3 21.3A)	09/07/20	DVT
15	Modify VGA_COREP circuit	design change	0.2	52	Cahnge PR153 to SD034576280 (S RES 1/16W 57.6K +-1% 0402)	09/07/20	DVT
16	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PQ35 to SB00000GL00 (S TR TPCA8028-H 1N SOP ADVANCE) Cahnge PQ36 to SB00000GL00 (S TR TPCA8028-H 1N SOP ADVANCE)	09/07/20	DVT
17	Modify VGA_COREP circuit	design change	0.2	52	Cahnge PC107 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU)	09/07/20	DVT
18	Modify 1.8V circuit	design change	0.2	50	Cahnge PC74 to SF000002000 (S ELE CAP 330U 6.3V M 6.3X5.9 LESR15M VU) and BOM structure to @	09/07/20	DVT
19	Modify CPU circuit	design change	0.2	55	Cahnge PR226 to SD000009O80 (S RES 1/16W 1.91K +-1% 0402)	09/07/20	DVT
20	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PC116 to SGA20331E10 (S POLY C 330U 2V Y D2 LESR9M EEFSX H1.9)	09/07/21	DVT
21	Modify CPU circuit	design change	0.2	55	Cahnge PC179 to SE026683K80 (S CER CAP .068U 16V K X7R 0603)	09/07/22	DVT
22	Modify chager circuit	design change	0.2	48	Cahnge PC53 to SE076473K80 (S CER CAP .047U 16V K X7R 0402) Cahnge PC64 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT
23	Modify 1.1VSDGPU circuit	design change	0.2	52	Cahnge PC212 to SE107475M80 (S CER CAP 4.7U 6.3V M X5R 0603 H0.8)	09/07/22	DVT

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Issued Date	2007/09/20	Deciphered Date	2008/09/20

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Compal Electronics, Inc.			
Title: PIR (PWR)			
Size: Custom	Document Number		Rev: 0.1
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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	Modify GFX_COREP circuit	design change	0.2	54	Cahnge PC189 to SE000000K80 (S CER CAP 1U 6.3V K X5R 0402)	09/07/22	DVT
25	Modify 1.8V circuit	design change	0.2	50	Add PR170 to SD013000080 (S RES 1/10W 0 +-5% 0603)and BOM structure to @ Change PR109, PR117, PC72, PQ58, PQ59 BOM structure to @	09/07/28	DVT
26	Modify 1.8V circuit	design change	0.2	50	Add PU17 to SA00003KL00(S IC MP2121DQ-LF-Z QFN 10P PWM) Add PD16 to SCS00001I80(S SCH DIO B340A SMA VISHAY) BOM structure to @ Add PR173 to SD034402380(S RES 1/16W 402K +-1% 0402)	09/07/28	DVT
27	Modify 1.8V circuit	design change	0.2	50	Add PR174 to SD034316380(S RES 1/16W 316K +-1% 0402) Add PR171 to SD028000080(S RES 1/16W 0 +-5% 0402)BOM structure to @	09/07/28	DVT
28	Modify 1.8V circuit	design change	0.2	50	Add PR113 to SD028470280(S RES 1/16W 47K +-5% 0402) Add PC123,PC124 to SE053106Z80(S CER CAP 10U 10V Z Y5V 0805) Add PC127 to SE076103K80(S CER CAP .01U 16V K X7R 0402)	09/07/28	DVT
29	Modify 1.8V circuit	design change	0.2	50	Add PC218, PC219 to SE000000I10(S CER CAP 22UF 6.3V M X5R 0805 H1.25) Add PR41, PR42 to SD001470B80(S RES 1/4W 4.7 +-5% 1206)	09/07/28	DVT
30	Modify 5V/3V circuit	add snubber(PR42 PC36),(PR41 PC35) add boost PR43, PR44	0.2	47	Add PC35, PC36 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR43, PR44 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
31	Modify VGA_COREP circuit	add snubber(PR315 PC206) add boost PR311	0.2	52	Add PR311 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)and BOM structure to VGA@ Change PR315 PC206 BOM structure to VGA@	09/07/28	DVT
32	Modify CPU circuit	add snubber(PR220 PC158),(PR252 PC184) add boost PR217, PR249	0.2	55	Add PR220, PR252 to SD011220B80(S RES 1/4W 2.2 +-5% 1206) Add PC158, PC184 to SE074681K80(S CER CAP 680P 50V K X7R 0402) Add PR217, PR249 to SD013220B80(S RES 1/10W 2.2 +-5% 0603)	09/07/28	DVT
33	Modify +1.1VS_VTTP circuit	design change	0.2	53	Cahnge PR141 to SD034787280(S RES 1/16W 78.7K +-1% 0402) Cahnge PR143 to SD034649180(S RES 1/16W 6.49K +-1% 0402)	09/07/28	DVT
34	Modify OTP circuit	design change	0.2	46	Cahnge PH1 to SL200000U00(S THERM_ 100K +-1% TSM0B104F4251RZ 0402) Cahnge PH2 to SL200000U00(S THERM_ 100K +-1% TSM0B104F4251RZ 0402)	09/07/28	DVT
35	Modify +1.1VS_VTTP circuit	design change(OCP)	0.2	53	Cahnge PR135 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/07/29	DVT
36	Modify GFX_COREP circuit	design change	0.2	54	Cahnge PH3 to SL200000Y00(10K +-5% TSM0A103J4302RE 0402)	09/07/29	DVT
37	Modify CPU circuit	design change	0.2	55	Cahnge PH6 to SL200000W00(10K +-1% TSM0A103F34D1RZ 0402)	09/07/29	DVT
38	Modify 1.5V circuit	Change to 3mm height choke for thermal issue	0.2	51	Cahnge PL7 to SH00000AB00(S COIL 1UH +-20% PCMB103T-1R0MS 13A)	09/08/06	DVT
39	Modify VGA_COREP circuit	design change (GS sample define 1.03V,+1.05VSDGPU Vo=1.05V)	0.3	52	Cahnge PR159 to SD034634180(S RES 1/16W 6.34K +-1% 0402) Cahnge PR167 to SD034365180(S RES 1/16W 3.65K +-1% 0402)	09/08/24	PVT
40	Modify 1.8V circuit	design change	0.3	50	Cahnge PC127 to SE076104K80(S CER CAP .1U 16V K X7R 0402)	09/08/24	PVT
41	Modify chager circuit	design change	0.3	48	Cahnge PR88 to SD034154280(S RES 1/16W 15.4K +-1% 0402) Change PR81 to SD034154380(S RES 1/16W 154K +-1% 0402)	09/08/26	PVT
42	Modify VGA_COREP circuit	design change	0.3	52	Change PR160 BOM structure to VGA@ VID pull high voltage change to +3VS_DELAY	09/09/03	PVT
43	Modify +1.1VS_VTTP circuit	design change	0.3	53	Change PR130 BOM structure to @	09/09/03	PVT
44	Modify 0.75V circuit	design change	0.3	50	Cahnge PR120 to SD034280180(S RES 1/16W 2.8K +-1% 0402)	09/09/11	PVT
45	Modify VGA_COREP circuit	design change	0.3	52	Cahnge PR316 to SD034300280(S RES 1/16W 30K +-1% 0402) Change PR164 BOM structure to @	09/09/11	PVT
46	Modify +1.1VS_VTTP circuit	design change	0.3	53	Cahnge PR135 to SD034205180(S RES 1/16W 2.05K +-1% 0402)		

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
47	Modify OTP circuit	design change	0.3	46	Change PR23 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402) Change PR26 to SD034158280(S RES 1/16W 15.8K +-1% 0402)	09/09/14	PVT
48	Modify 1.8V circuit	design change	0.3	50	Change PL6 to SH000009Q00(S COIL 2.2UH 20% MSCDRI-74A-2R2M-E 6.5A)	09/09/16	PVT
49	Modify 5V/3V circuit	design change	0.3	47	Change PU4 to SA00001TN00(S IC ISL6237IRZ-T QFN 32P)	09/09/16	PVT
50	Modify 0.75V circuit	design change	0.3	50	Change PR120 to SD00000AJ80(S RES 1/16W 12.4K +-1% 0402)	09/10/08	PVT
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Title: PIR (PWR)

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				4	R72 bom structure	7/23	0.2
2				5	reserve R735	7/23	0.2
3				8	rename CPU VDDQ from +1.5V to +1.5V_CPU	7/23	0.2
4				8	R146 BOM structure	7/23	0.2
5				11	reserve S3 power consumptiosn circuit	7/23	0.2
6				12	change Y1 Y4 Y6 footprint	7/23	0.2
7				13	add ME_EN# from EC to PCH	7/23	0.2
8				14	pop Y6,C254,C255 , and project ID pin	7/23	0.2
9				17	change USB port 8 to port 1 , port 2 to port 8	7/23	0.2
10				18	GPIO35 pin(VGa presetnt) modfiy	7/23	0.2
11				19	R605 and R628 BOM structure modify	7/23	0.2
12				22	add VGA thermal sensor from EC to VGA	7/23	0.2
13				23	pop R479,del R491	7/23	0.2
14				29	L29~L34 change from 0805 to 0603	7/23	0.2
15				30	Q45,Q47 gate voltage change from +3VS to +3VS_delay	7/23	0.2
16				37	change R306 to 8.2K, add D29, rename EC_MUTE	7/23	0.2
17				38	Jfun1 pin3 change form KSO1 to KSO3	7/23	0.2
18				39	del SW2	7/23	0.2
19				41	change R333, R336 to 39k,15k, add R681,C707	7/23	0.2
20				43	reserve Q58,Q59,R728,R326, change U26,R688	7/23	0.2
21				24	reserve C710	7/23	0.2
22				28	reserve U44,U45	7/23	0.2
23				19	update L7,L8,L10,L11 footprint	7/23	0.2

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				30	pop R248, R271,R265	7/23	0.2
2				7	pop C165, del C170	7/23	0.2
3				18	unpop R532, R86	7/23	0.2
4				5	add R472 and C713	8/31	0.3
5				11	add C714	8/31	0.3
6				12	add C715	8/31	0.3
7				17	USB20 port 6 change to USB20 port 9	8/31	0.3
8				24	3VS_delay related circuit	8/31	0.3
9				30	del R236,C257 , pop R254,C268 in all sku	8/31	0.3
10				33	unpop R3 , U1, pop R6 , change R306 to 18K	8/31	0.3
11				37	ME_EN change from U25,75 to U25.16	8/31	0.3
12				29	pop Q6,Q7 in all sku	8/31	0.3
13				29	change L29~L34 footprint	8/31	0.3
14				41	del D25,D26,D27	8/31	0.3
15				43	update C705,C706 BOM structure	8/31	0.3
16				14	unpop R112	8/31	0.3
17				7	change C165 p/n	8/31	0.3
18				40	pop C353	9/10	0.3
19					change R157,R527,R570,R575,R582,R634,R239,R64 to 0 ohm		0.3
20				5	add R746,R747	9/10	0.3
21				12	U27 clk gen change to siligo	9/10	0.3
22				40	del C371,C372	9/10	0.3
23				3	Modify BOM Config add S3@ on all SKU	10/20	1.0

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1				14	Change R209,C254,C255,Y6 BOM config to UMA@	10/20	1.0
2				19	Added C257	10/20	1.0
3				22	Change N11 to A2 (P/N SA00003HZ10)	10/20	1.0
4				22	Added R748 and R749 as I2C pull high resistor.	10/20	1.0
5				22	Pop R36,R37 as DIS@	10/20	1.0
6				28	Change Q11,Q19 BOM config to SG@	10/20	1.0
7				28	Change R502,R484 BOM config to DIS only@	10/20	1.0
8				37	Change R306 to 33k(Board ID)	10/20	1.0
9				38	Change LED9 PN to SC5191UD00	10/20	1.0
10				43	Change R296 to 47K,R295 to 470	10/20	1.0
11				44	Change LED Resistors:	10/20	1.0
12					R373 to 243,R381 and R383 to 100,R377 to 243,		
13					R375 and R376 to 470,R349 to 100,R350 to 191		
14					R304 to 499		1.0
15				17	Change C256 to 22u	10/22	
16				18	ADD R750 10K pull hig resistor	10/22	1.0
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Title: PIR (HW)
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