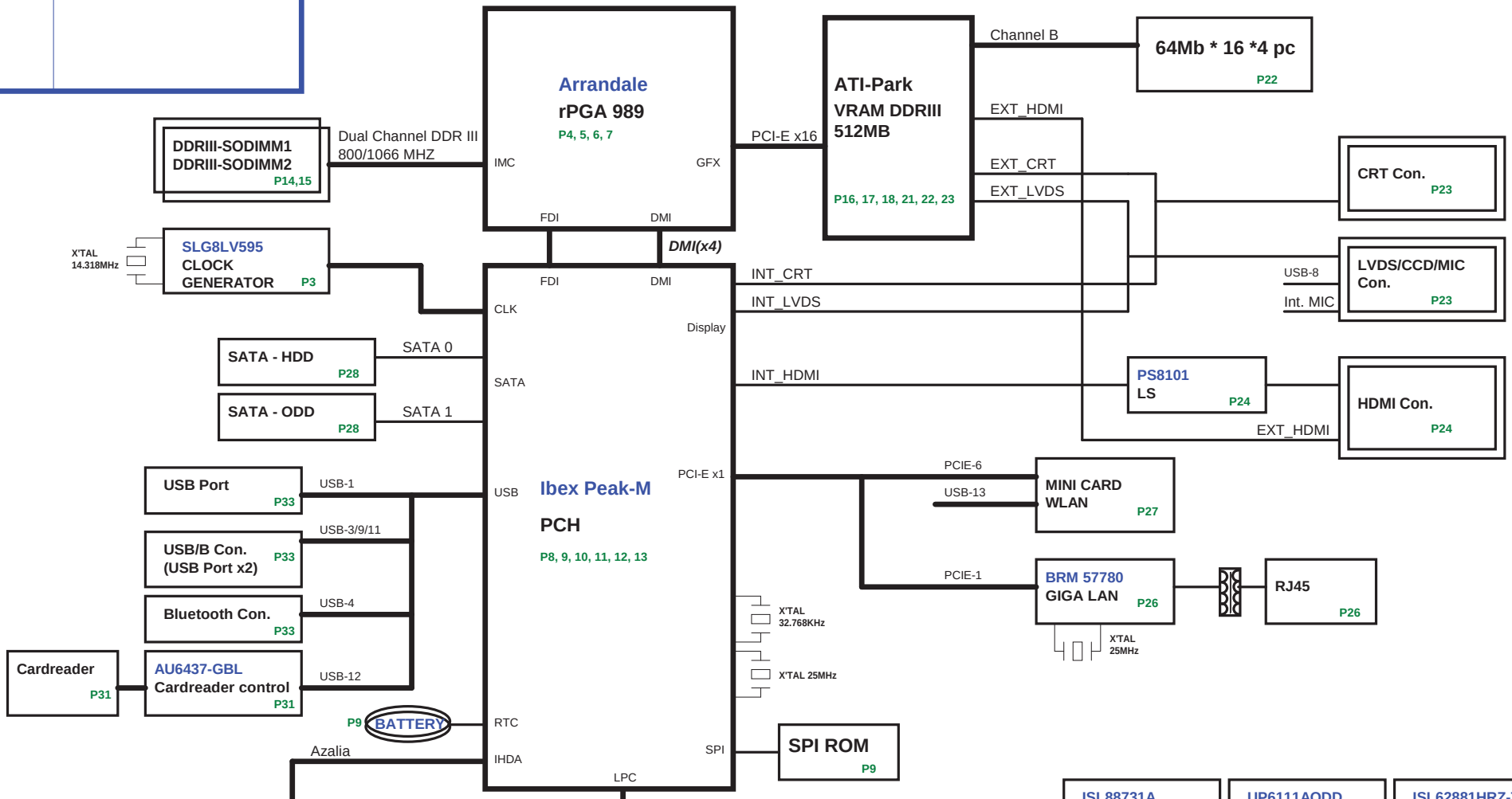
VER : 1A

BOM P/N	Description

ZQ9 SYSTEM BLOCK DIAGRAM



BOM Option Table

Reference	Description
IV@	for UMA only SKU
EV@	for Discrete Graphic only SKU
VRAM@	for different VRAM parts
*	do not stuff

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Size	Document Number	Rev
	Block Diagram	1A

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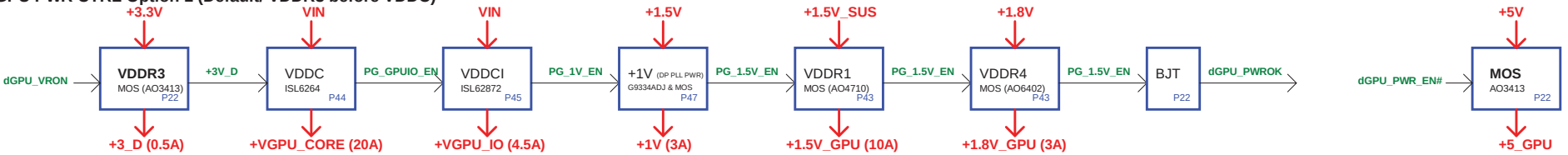
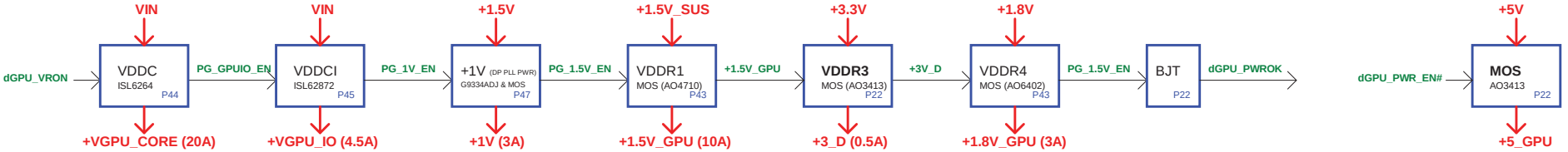
GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



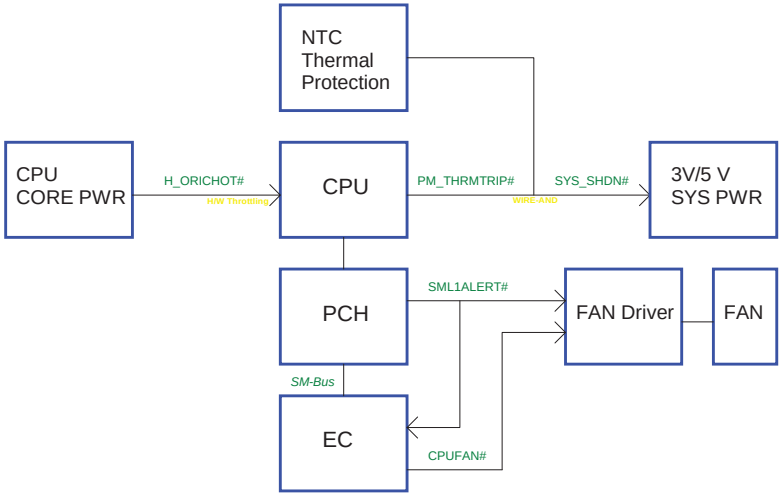
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart



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Size	Document Number	Rev
	PWR Status & GPU PWR CRL & THRM	1A

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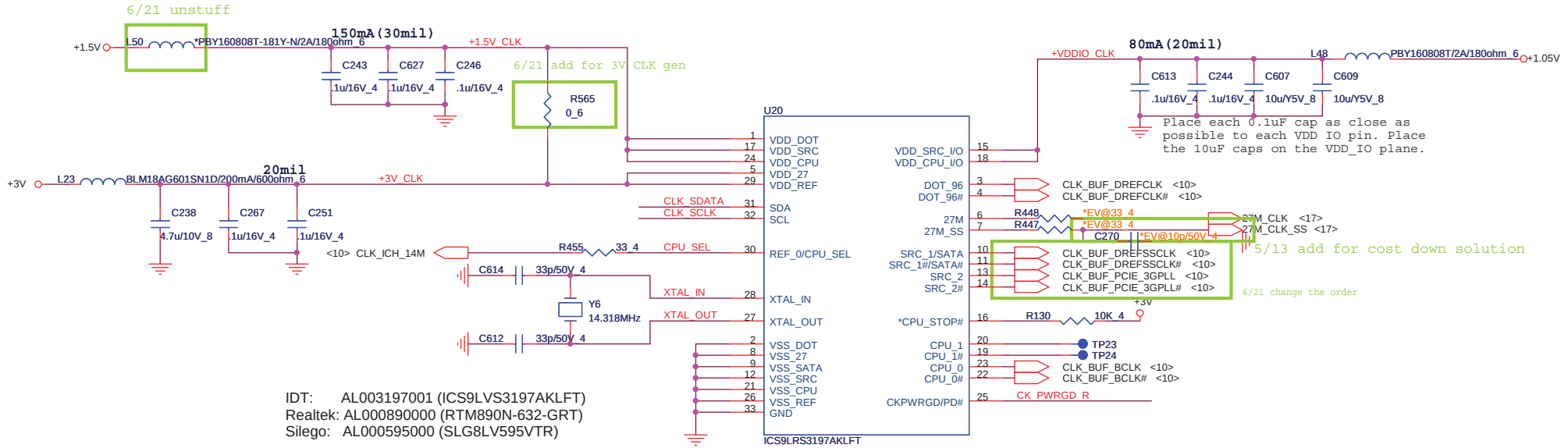
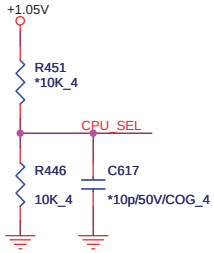


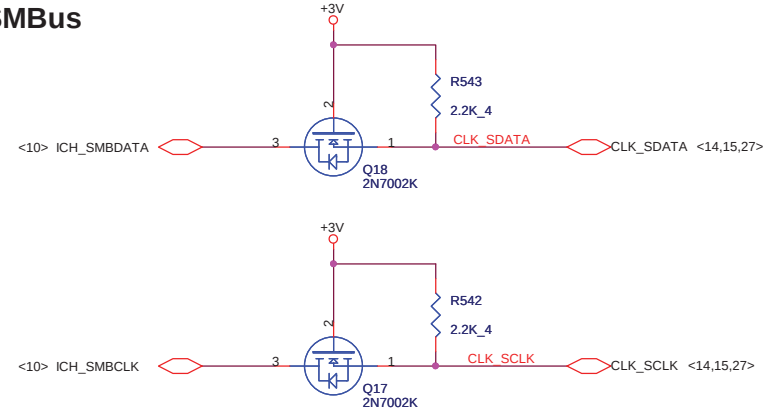
IDT: AL003197001 (ICS9LVS3197AKLFT)
Realtek: AL000890000 (RTM890N-632-GRT)
Silego: AL000595000 (SLG8LV595VTR)

CPU_CLK select

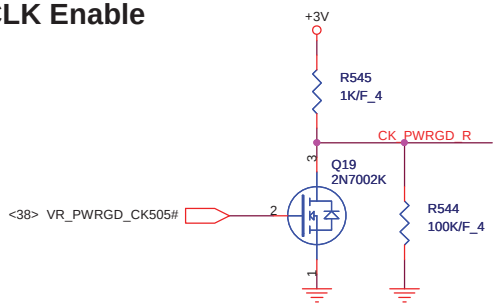


	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

SMBus



CLK Enable



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Size	Document Number	Rev
	Clock Generator	1A
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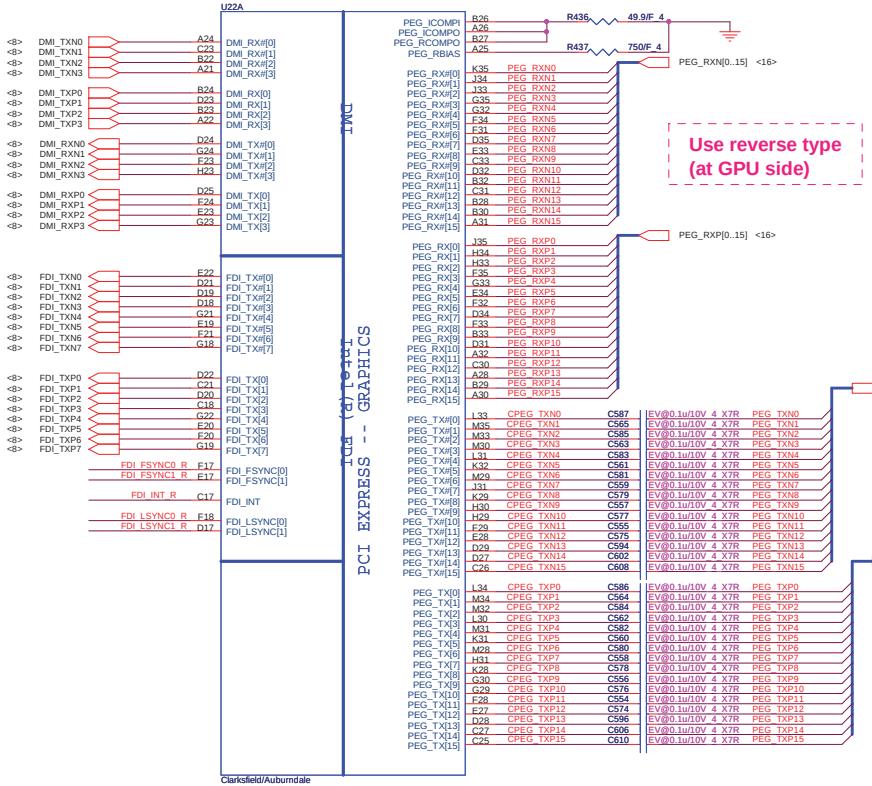
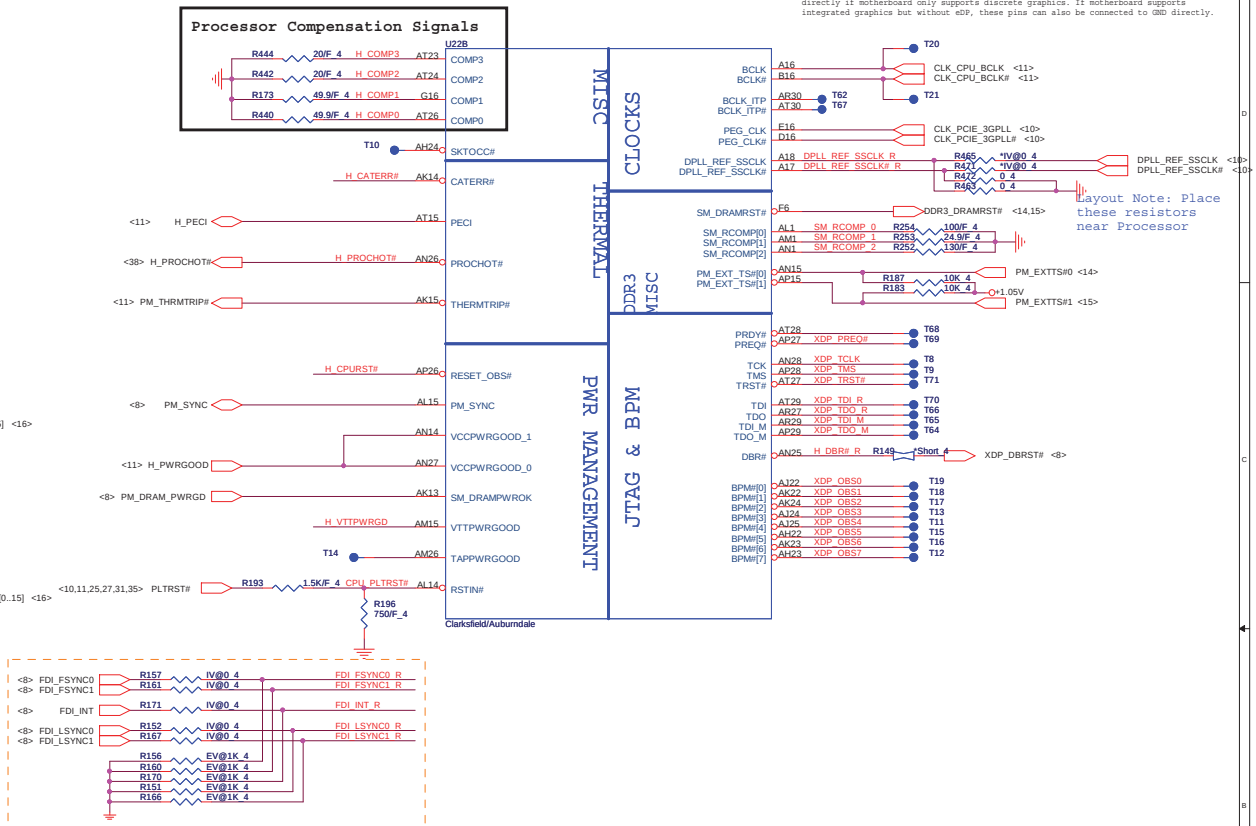
AUBURNDALE/CLARKSFIELD PROCESSOR (DMI,PEG,FDI)

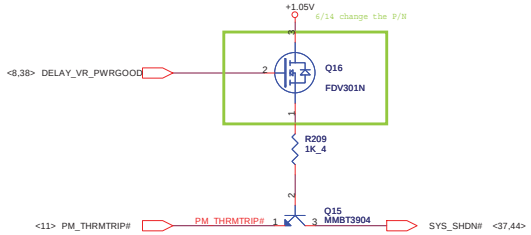


AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)

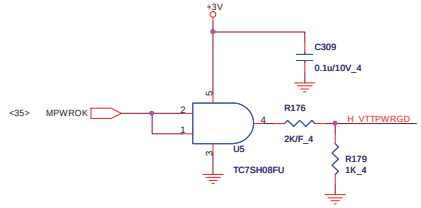


<The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT>Note that if these signals are left as no connect, there are no functional impacts, but a small amount of power (~15 mW) maybe wasted.

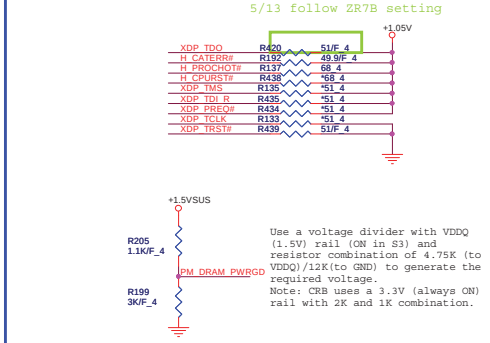
Thermaltrip protect



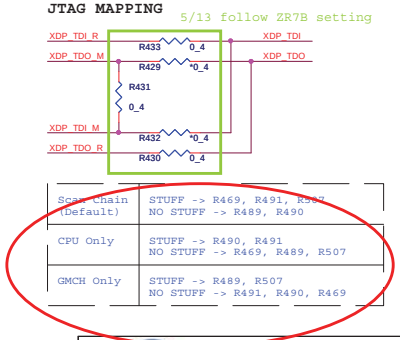
VTT PWR_Good



Processor pull-up



JTAG MAPPING



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Size	Document Number	Rev
	AUBURNDA 1/4	1A

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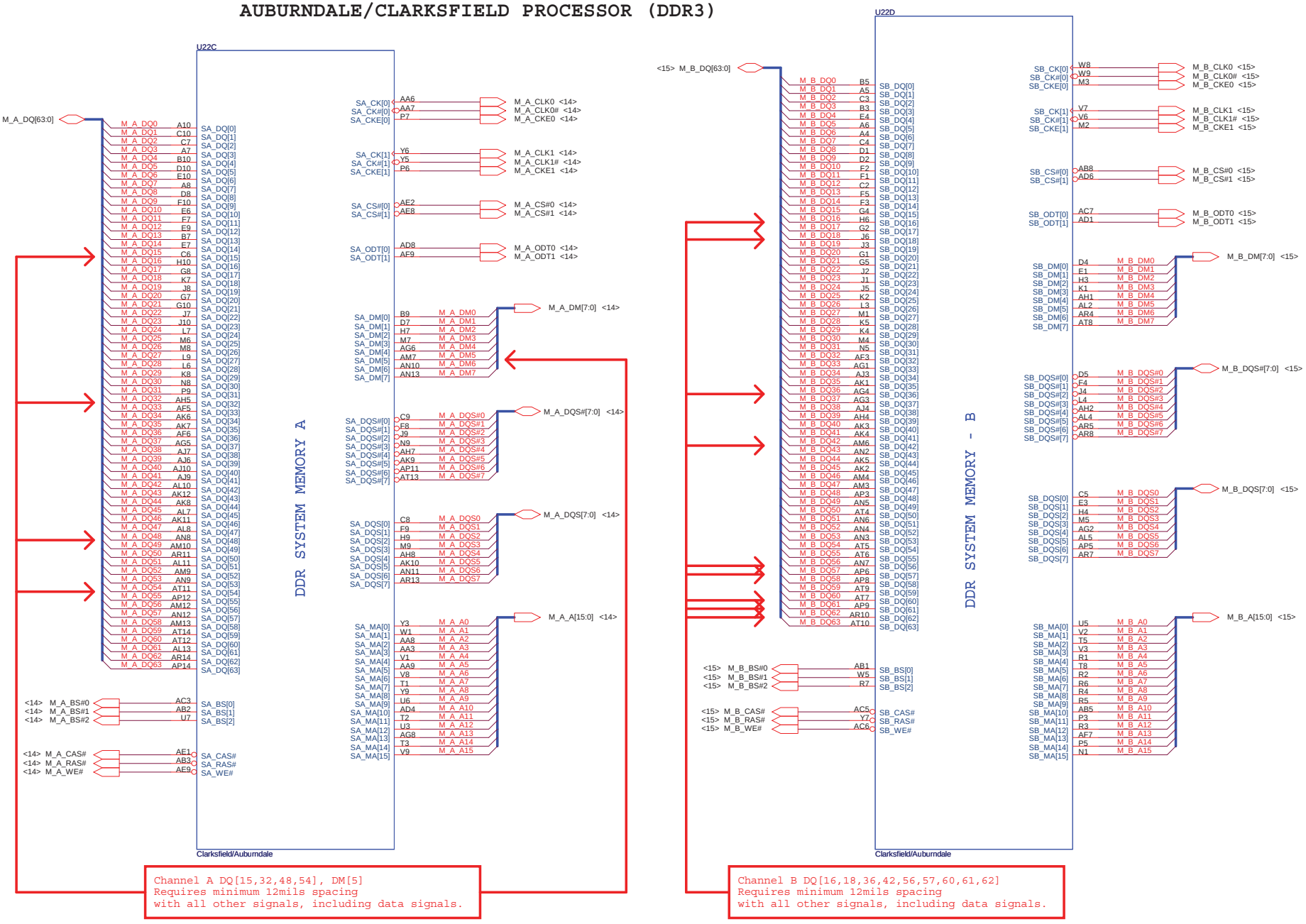
AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



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Size	Document Number: AUBURNDA 2/4	Rev: 1A
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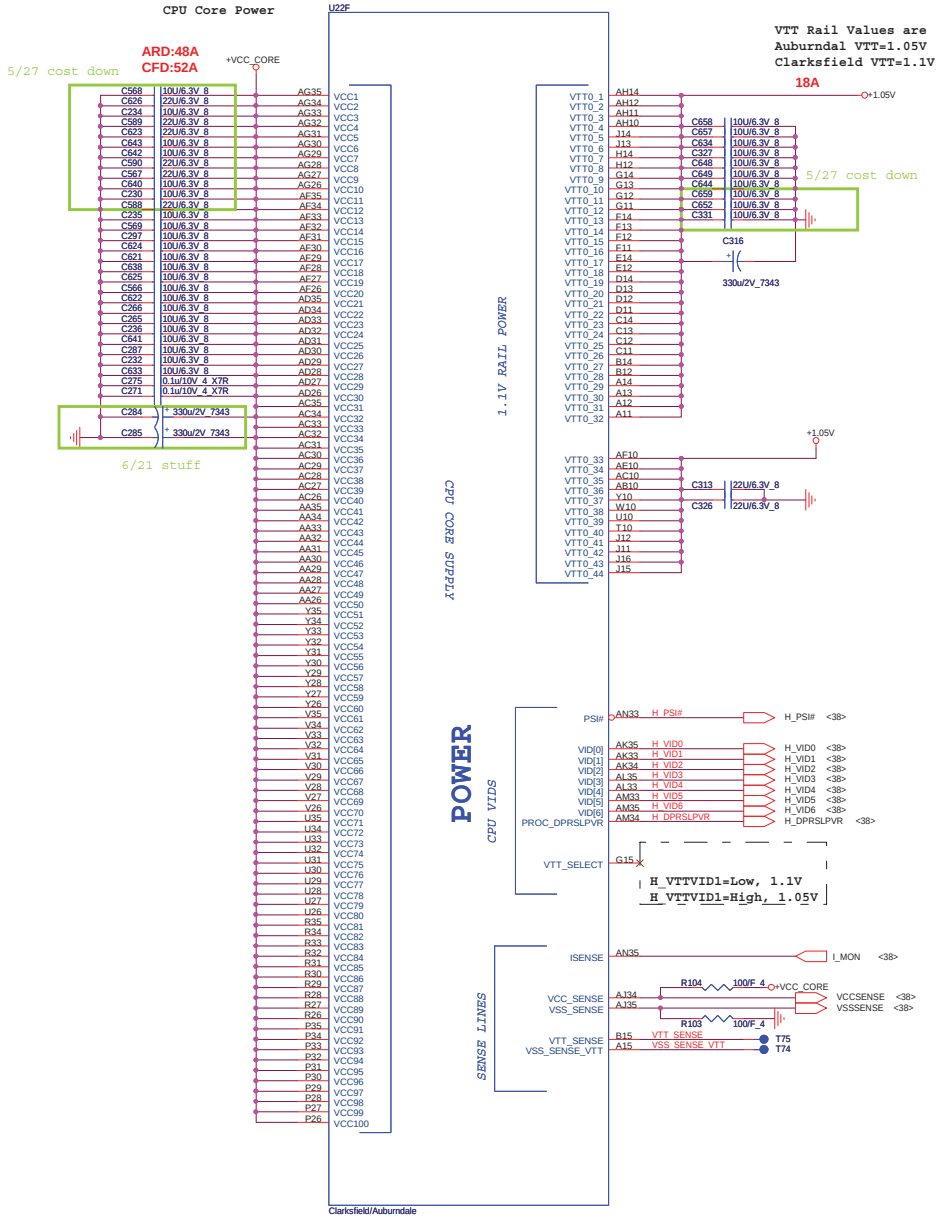
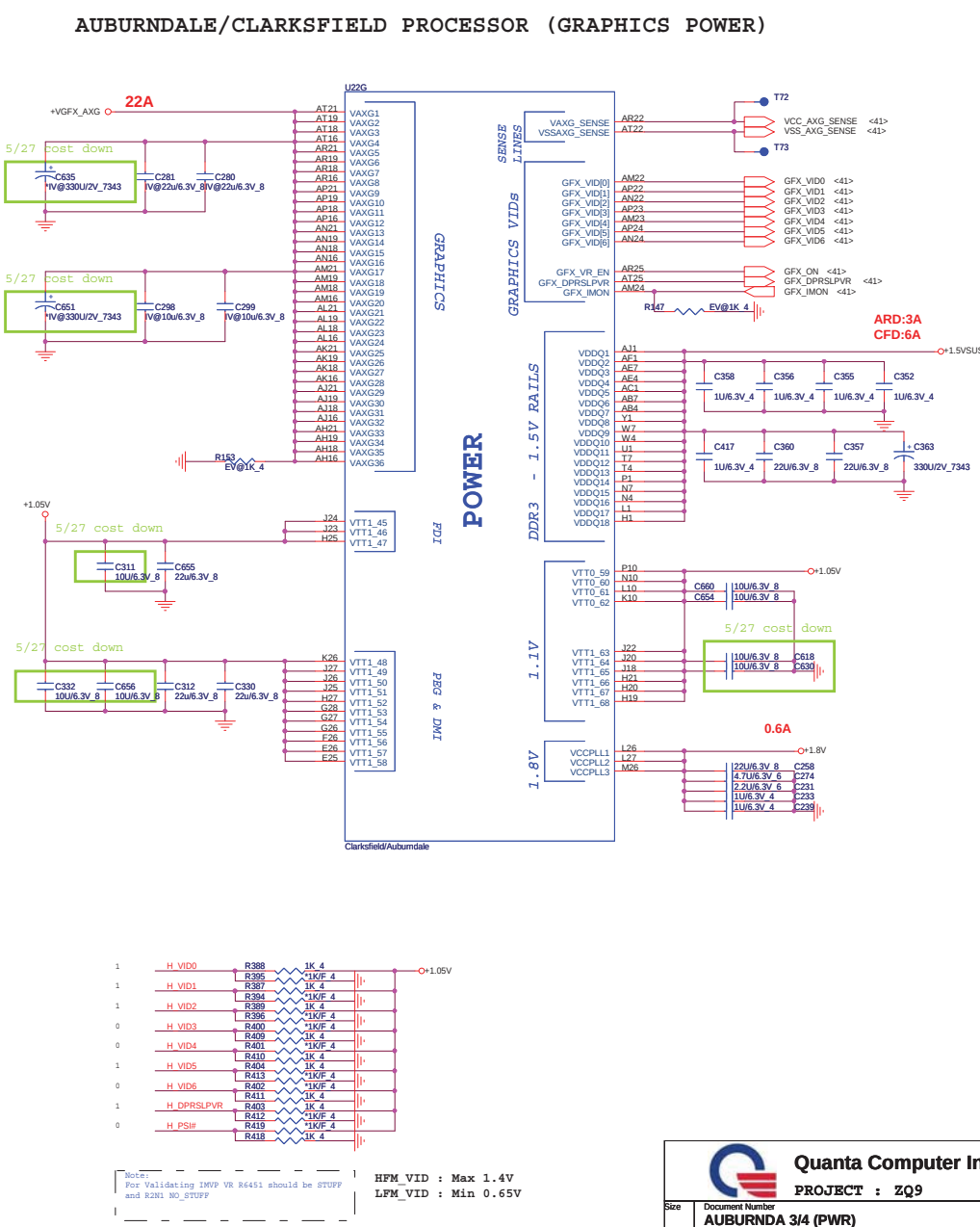


AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



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	AUBURNDA 3/4 (PWR)	1A
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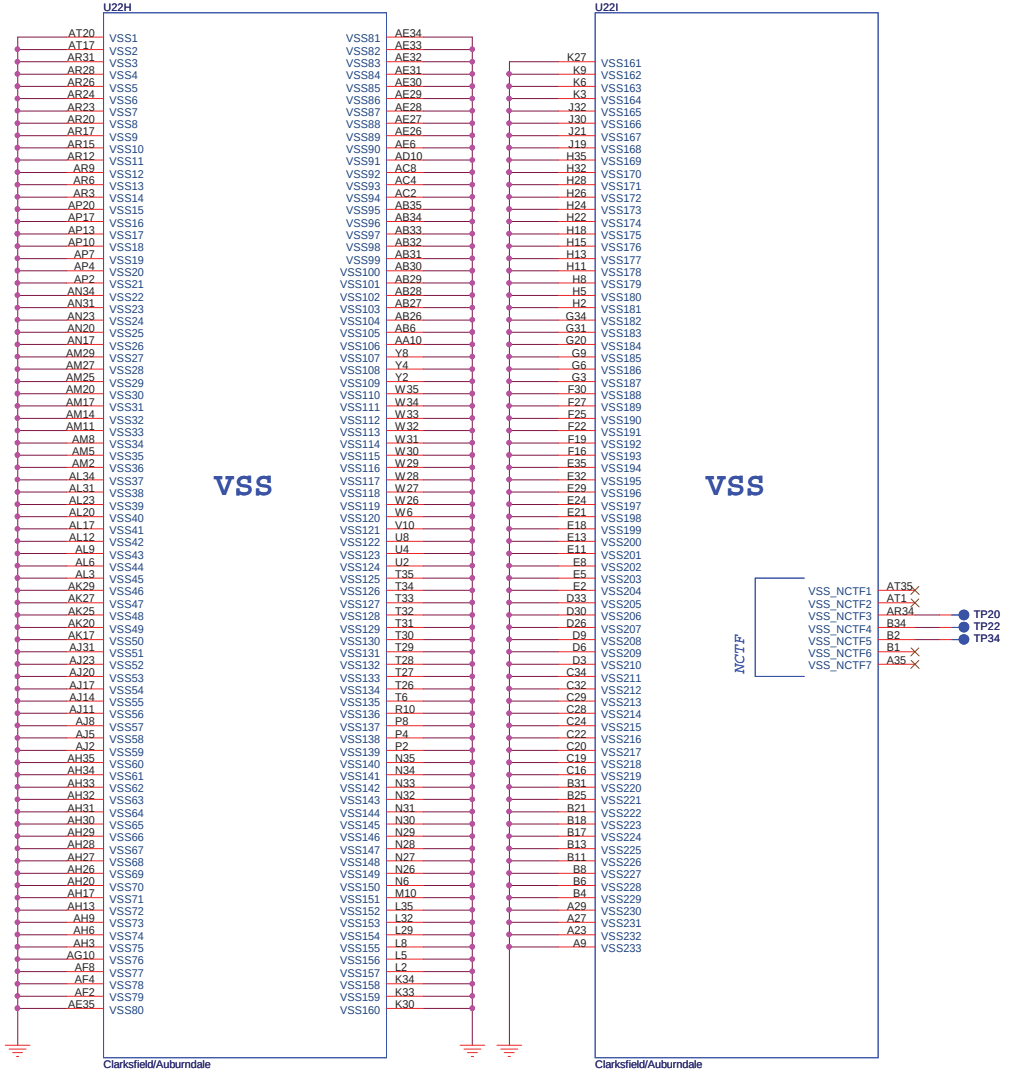
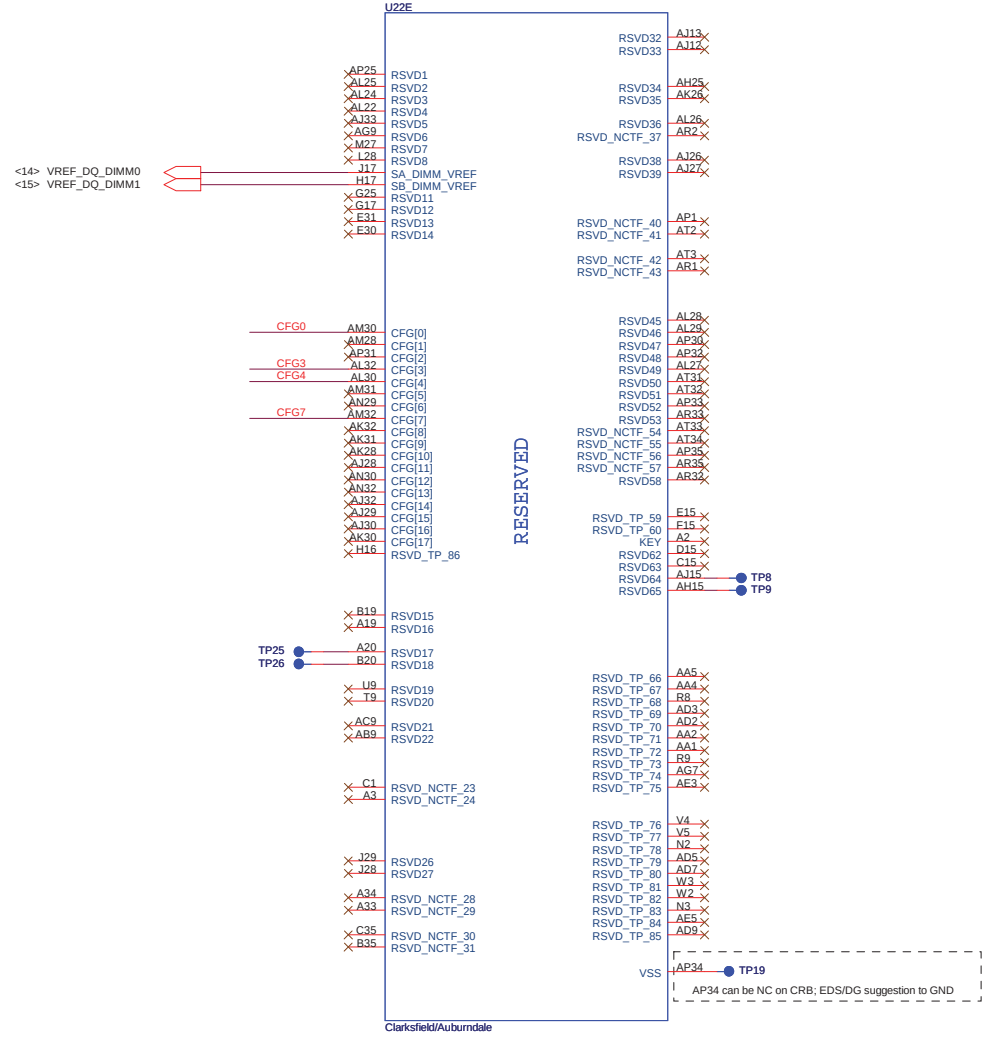
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



Processor Strapping

	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 *3.01K_NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 3.01K/F_4
CFG4 (Embended Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 *3.01K
T				CFG7 R126 *3.01K/F_4

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	AUBURNDA 4/4	1A

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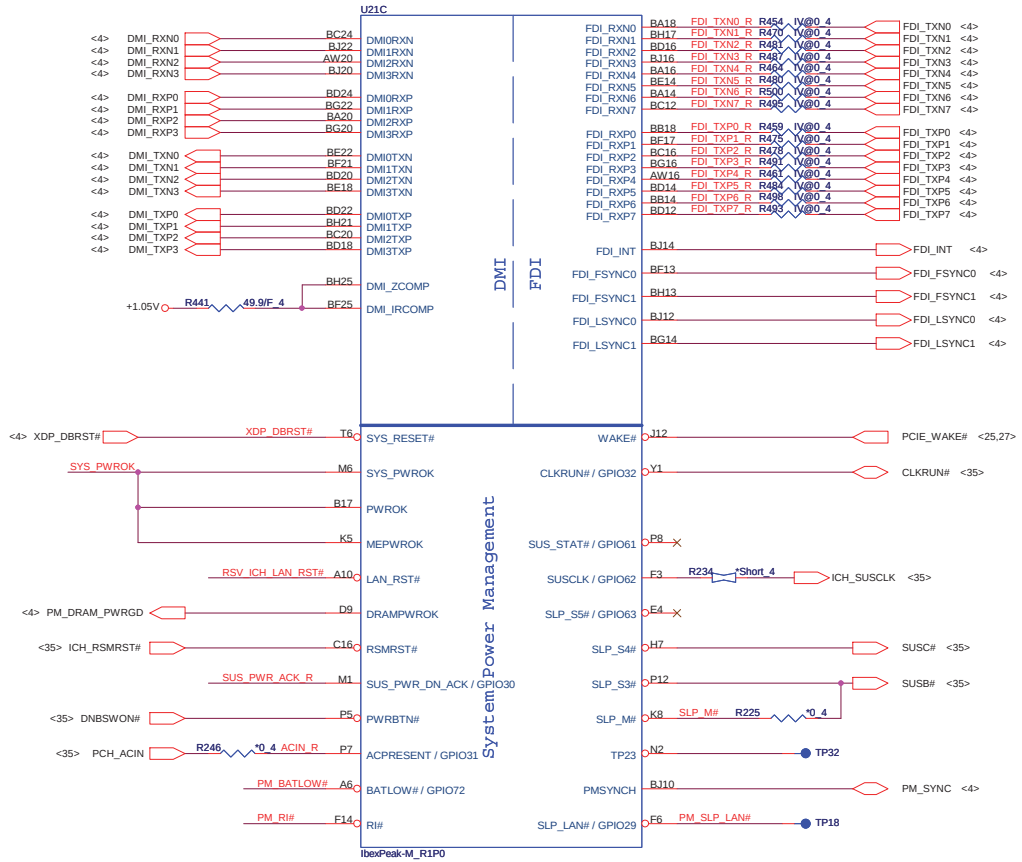
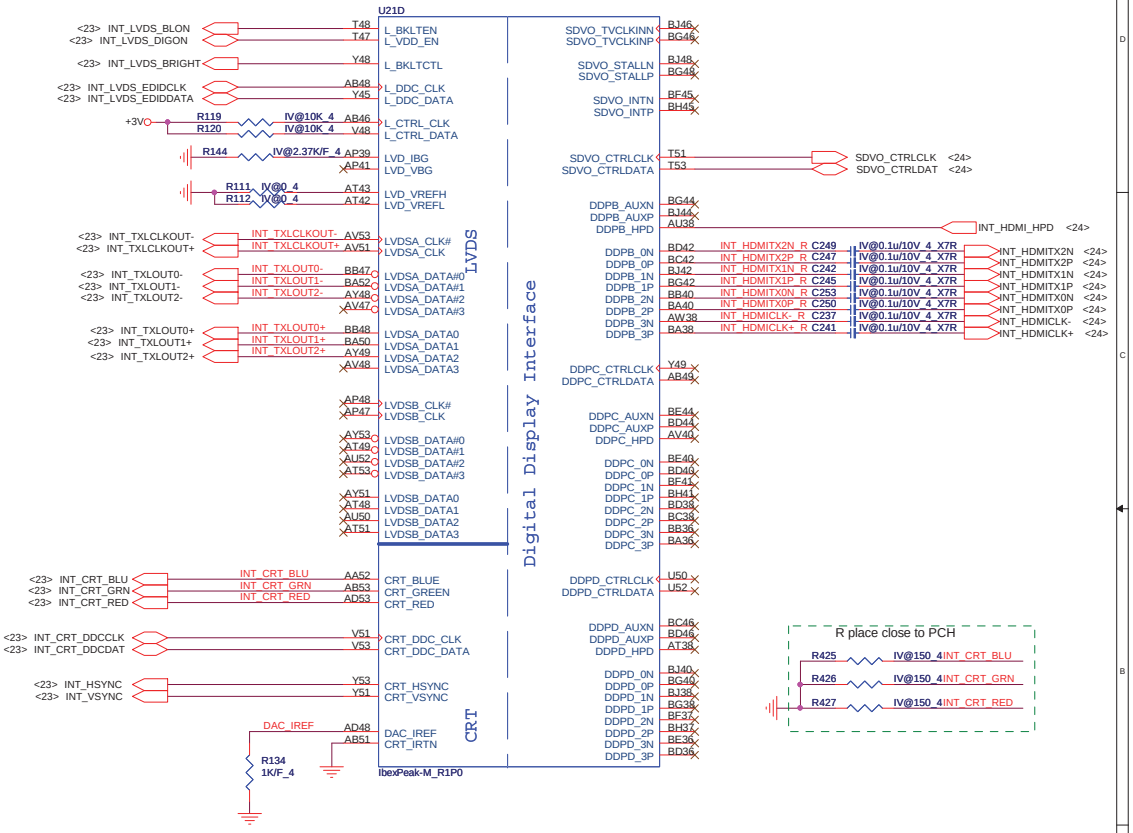
IBEX PEAK-M (DMI,FDI,GPIO)

0-ohm resistor place close to PCH

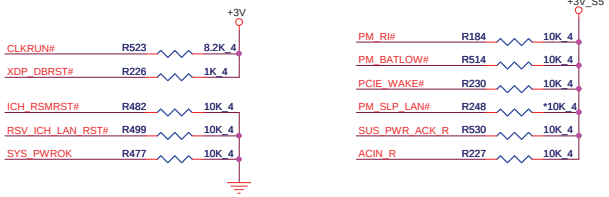


AC-coupling CAP place close to PCH

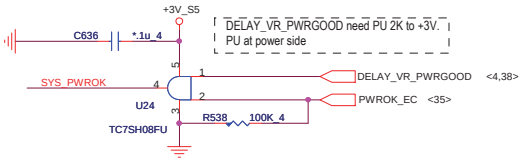
IBEX PEAK-M (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



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	IBEX PEAK-M 1/6	1A
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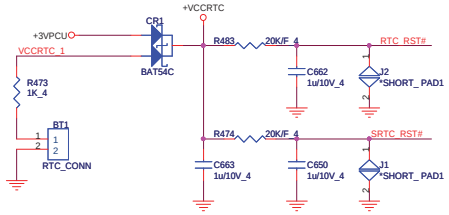
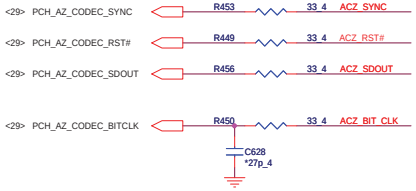
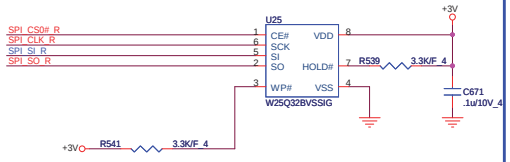
RTC Circuitry

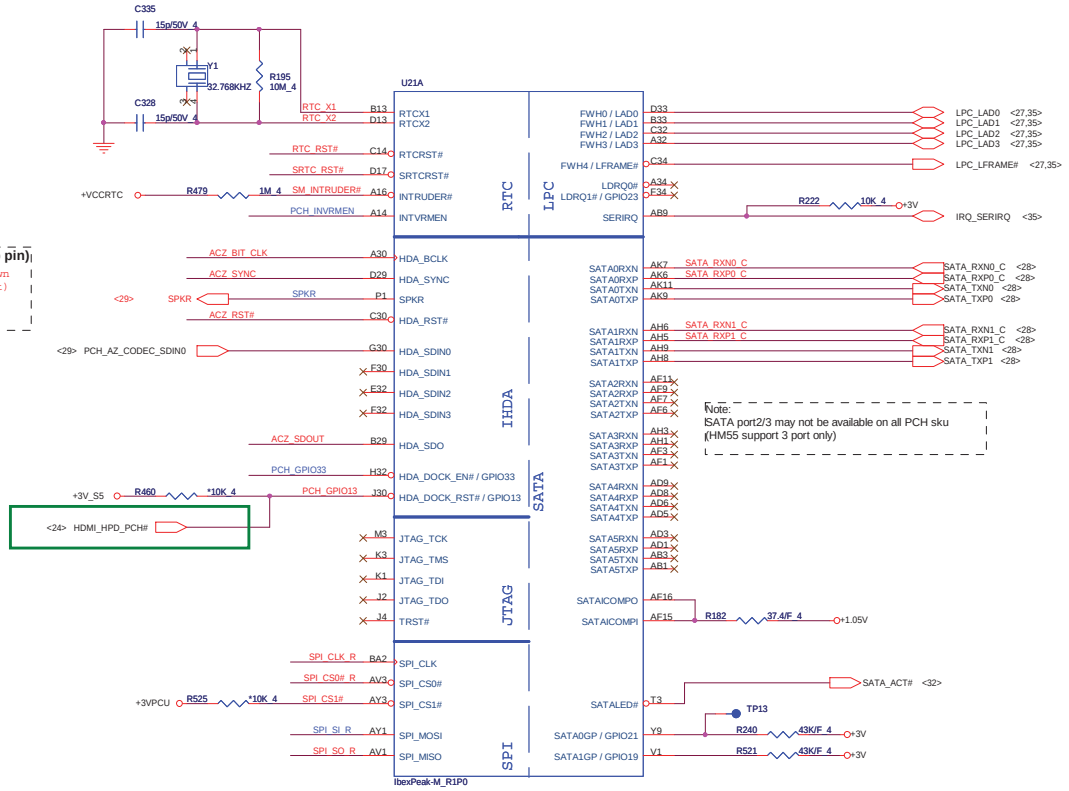


HDA Bus



PCH SPI





PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K_6 PCH_INVRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 *1K_4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 *1K/F_4 SPKR
HDA_DOCK_EN #/GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 *1K/F_4 R145 *10K_4 +3V
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K_4 R122 1K_4 R123 *1K_4 R131 *1K_4 +3V <10> PCI_GNT0# <10> PCI_GNT1#
GNT2#/ GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	<10> PWM_SELECT# R158 *1K/F_4
GNT3#/ GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	<10> PCI_GNT3# R421 *10K/F_4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	<10> NV_ALE R202 *1K/F_4 +1.8V
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	<10> NV_CLE R206 *1K/F_4 +1.8V

GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	<11> RSV_GPIO8 R204 10K_4 +3V_S5 R203 *1K_4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	<11> CR_WAKE# R244 1K_4 +3V_S5
GPIO27	On-Die PLL Voltage Regulator <internal weak pull-up>	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	<11> PCH_GPIO27 R221 *10K_4

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	IBEX PEAK-M 2/6	1A

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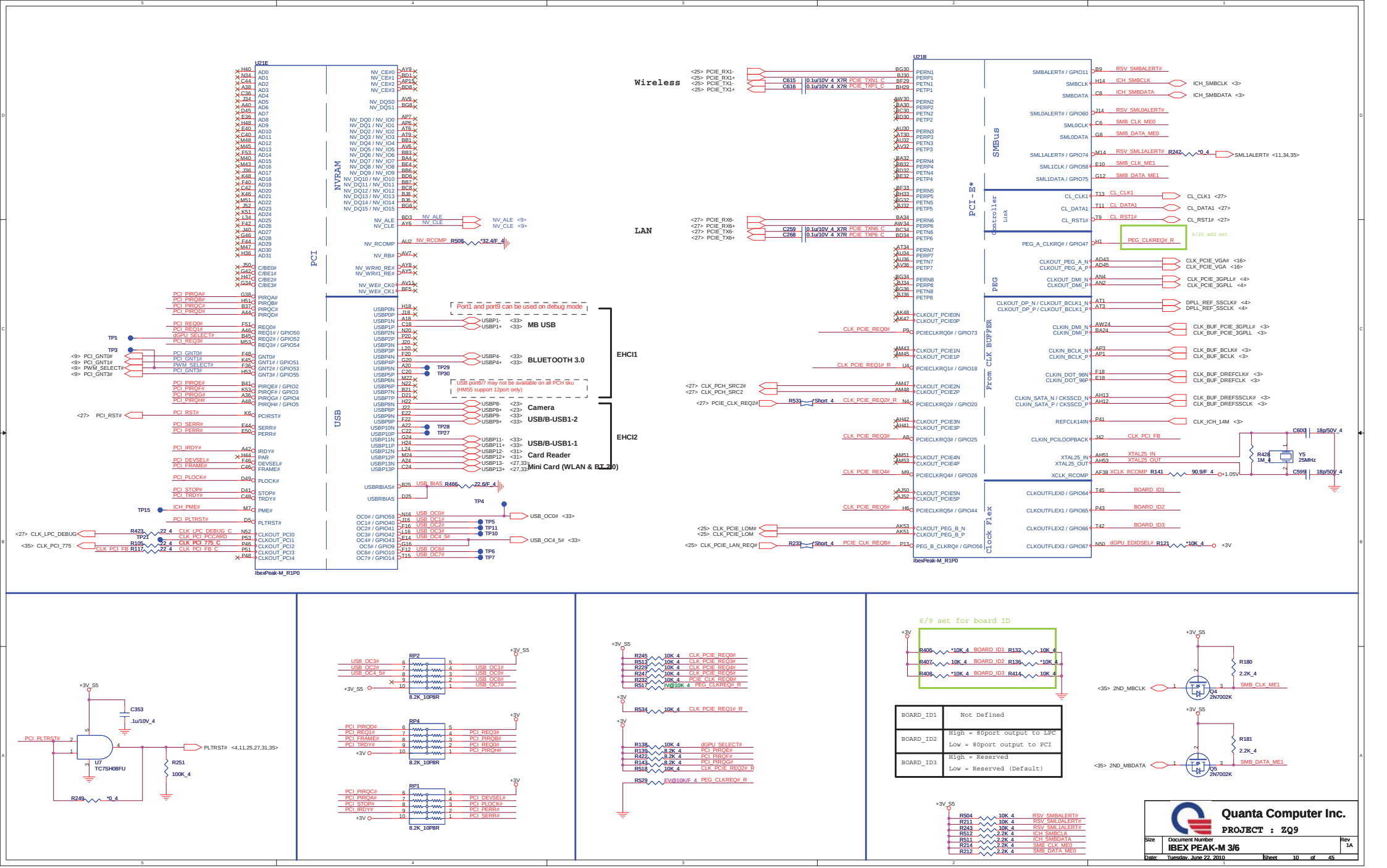
U21E
PCI
NVRAM
USB
IbexPeak-M_R1P0
Port1 and port9 can be used on debug mode
USB port6/7 may not be available on all PCH sku
(HM55 support 12port only)
MB USB
BLUETOOTH 3.0
Camera
USB/B-USB1-2
USB/B-USB1-1
Card Reader
Mini Card (WLAN & BT 2.0)
EHCI1
EHCI2
Wireless
LAN
U21B
PCI-E*
SMBus
PEG
Prom CLK BUFFER
Clock Flex
Controller
Link
IbexPeak-M_R1P0
6/9 set for board ID
BOARD_ID1 Not Defined
BOARD_ID2 High = 80port output to LPC
Low = 80port output to PCI
BOARD_ID3 High = Reserved
Low = Reserved (Default)
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IBEX PEAK-M 3/6
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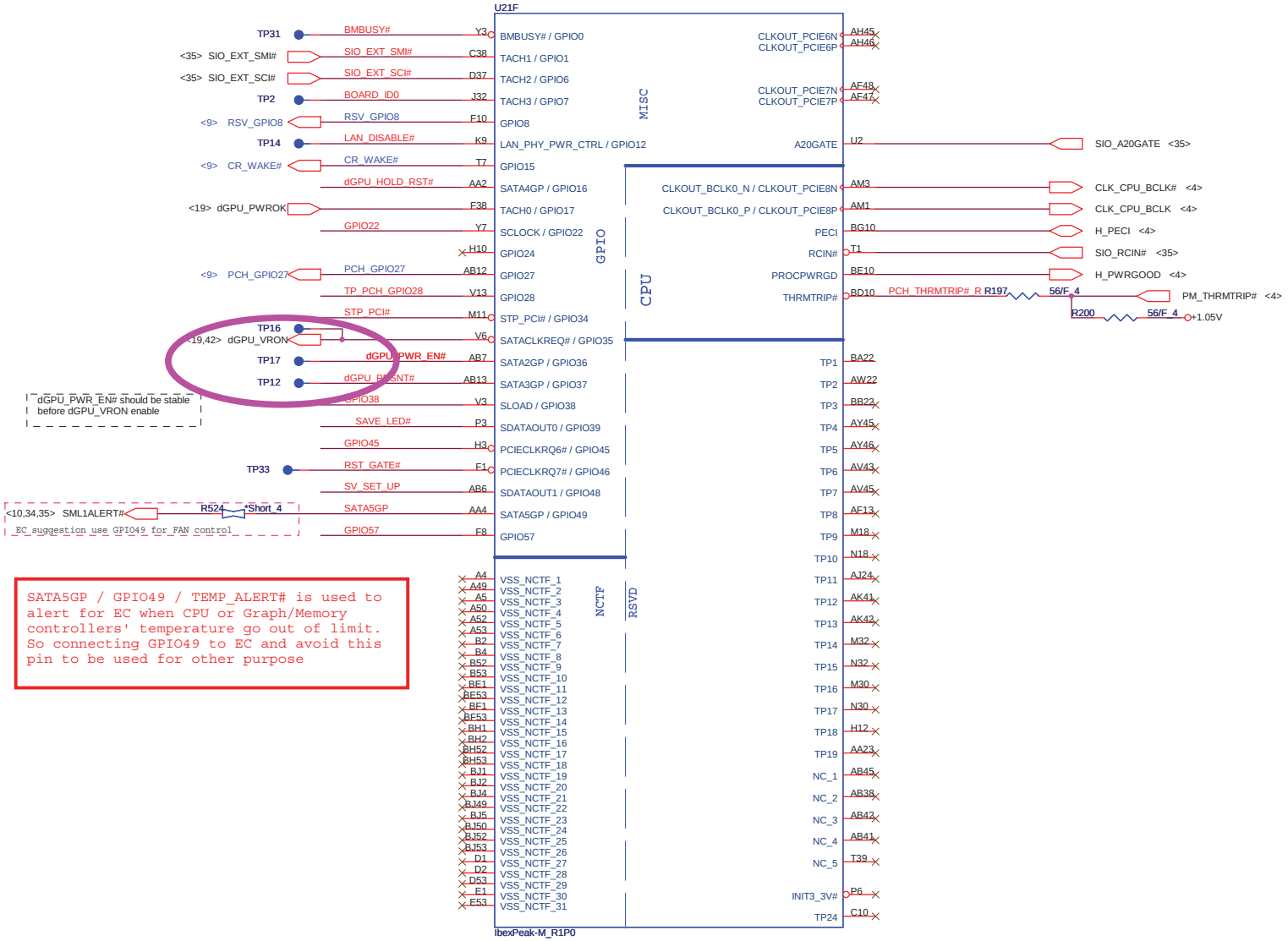
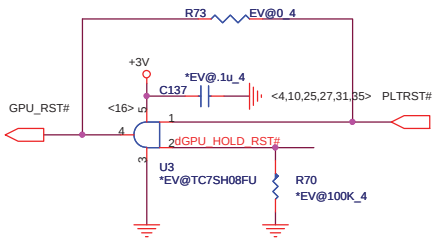
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



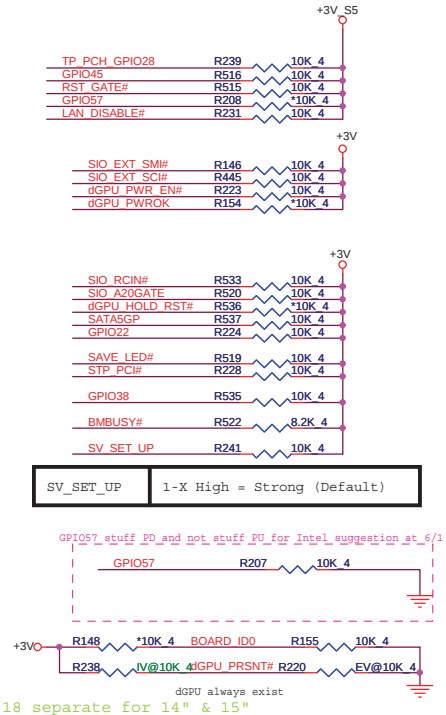
SATA5GP / GPIO49 / TEMP_ALERT# is used to alert for EC when CPU or Graph/Memory controllers' temperature go out of limit. So connecting GPIO49 to EC and avoid this pin to be used for other purpose

GPU RST#

5/18 change for discrete only



GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)

5/18 separate for 14" & 15"

BOARD_ID0	High = 15" Low = 14"
RSV_GPIO8	High = Disable Low = Enable

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	IBEX PEAK-M 4/6	1A

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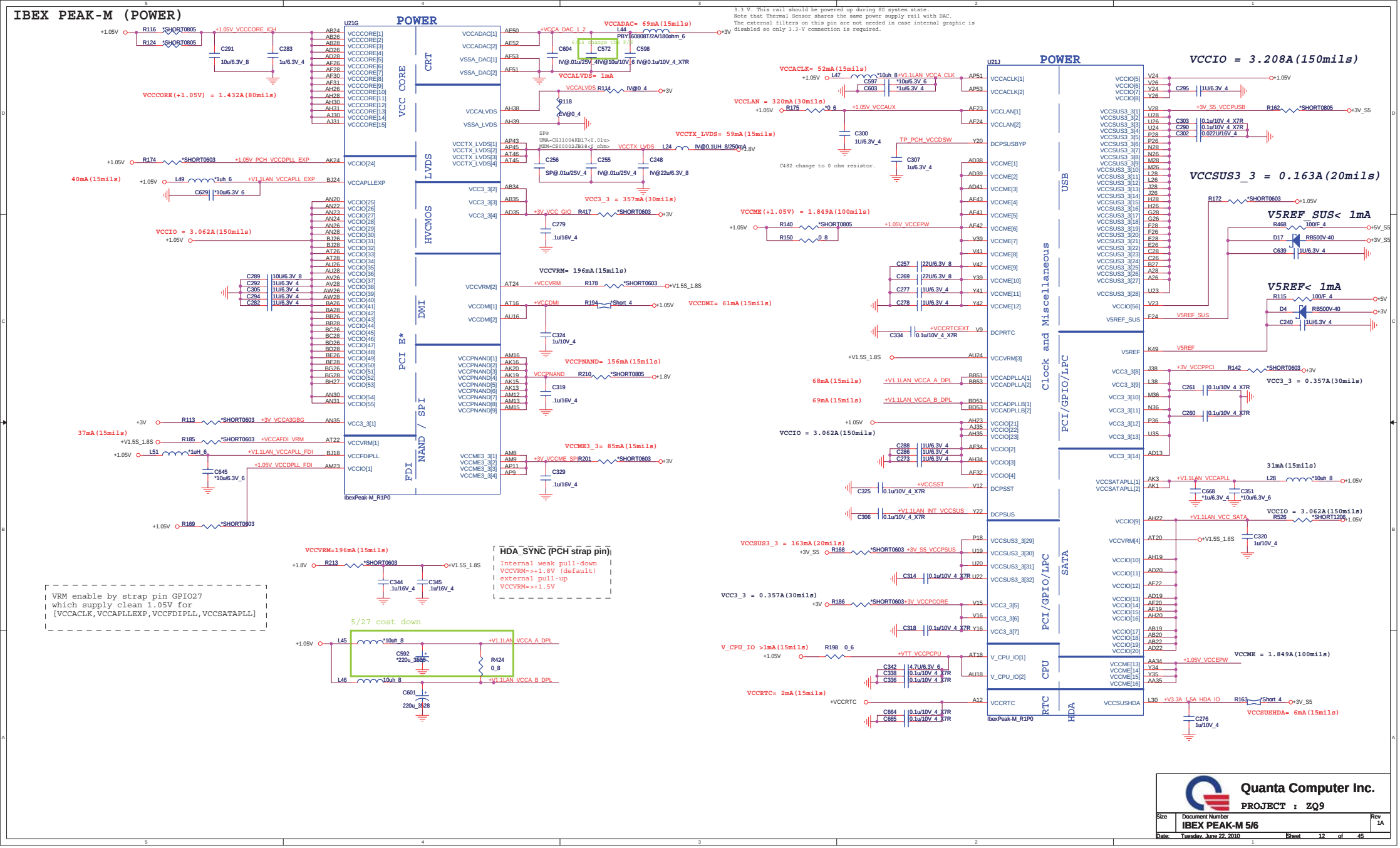
IBEX PEAK-M (POWER)

3.3 V. This rail should be powered up during S0 system state.
Note that Thermal Sensor shares the same power supply rail with DAC.
The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.



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	IBEX PEAK-M 5/6		1A
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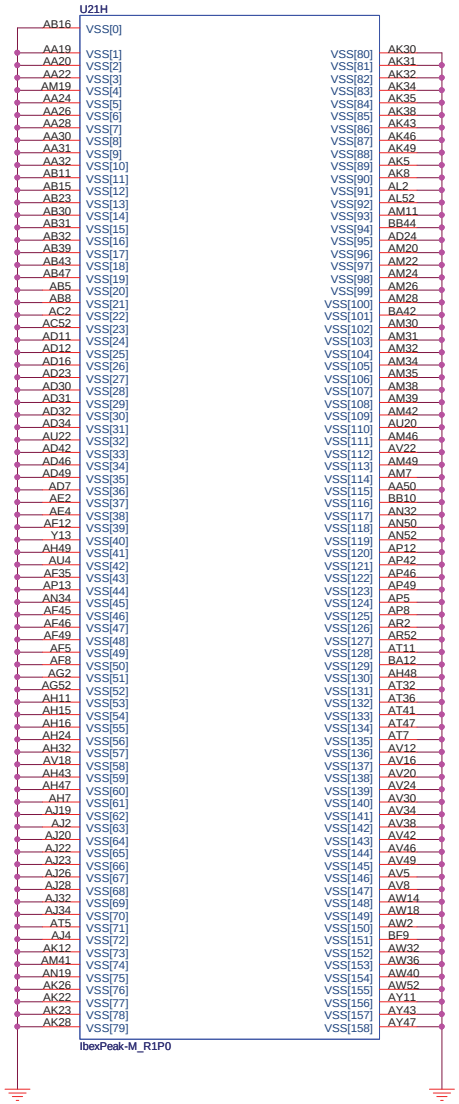
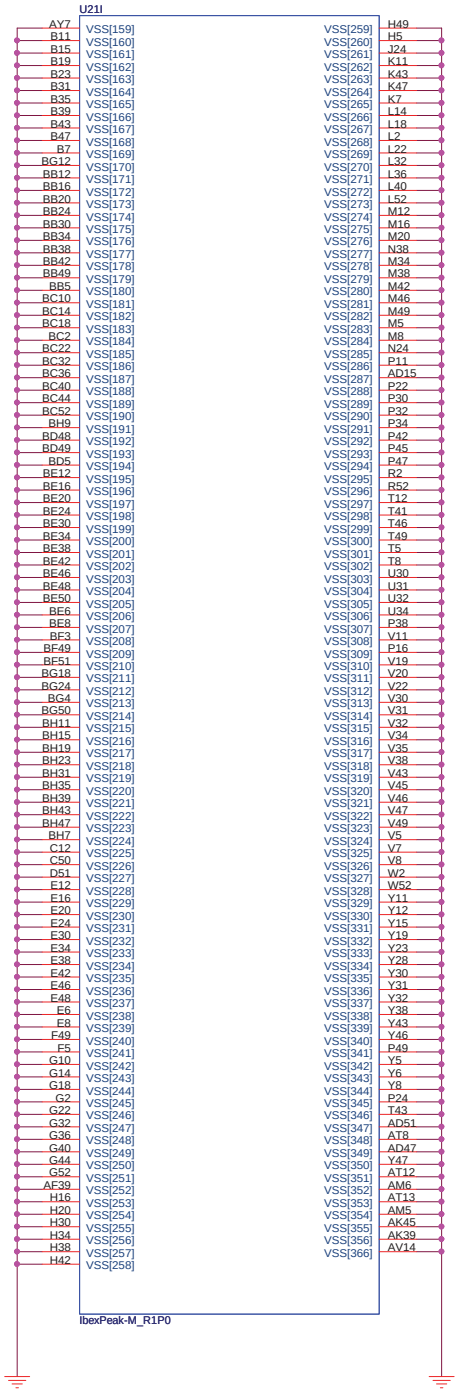
IBEX PEAK-M (GND)





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Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

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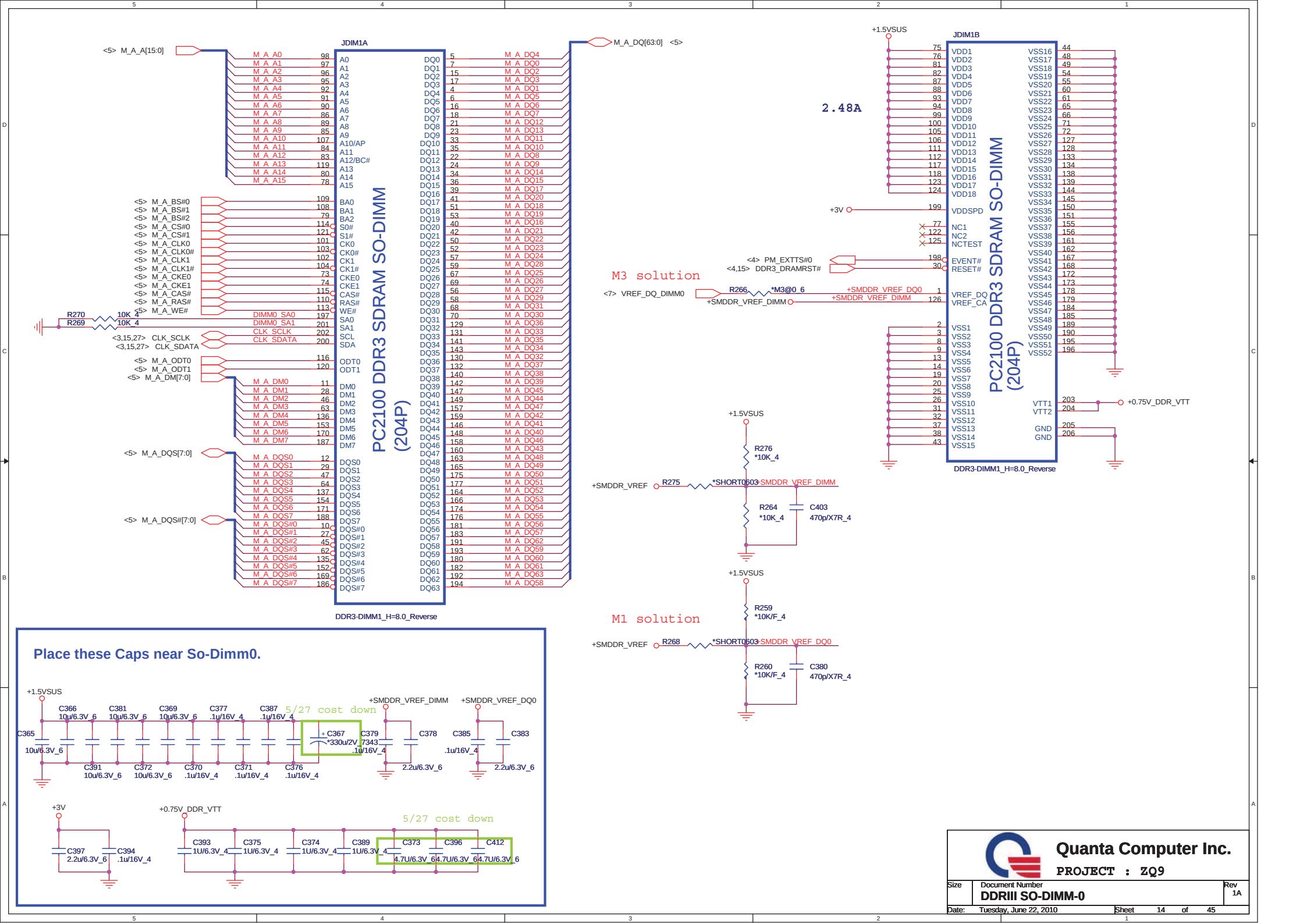

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Size	Document Number	Rev
	DDRIII SO-DIMM-0	1A
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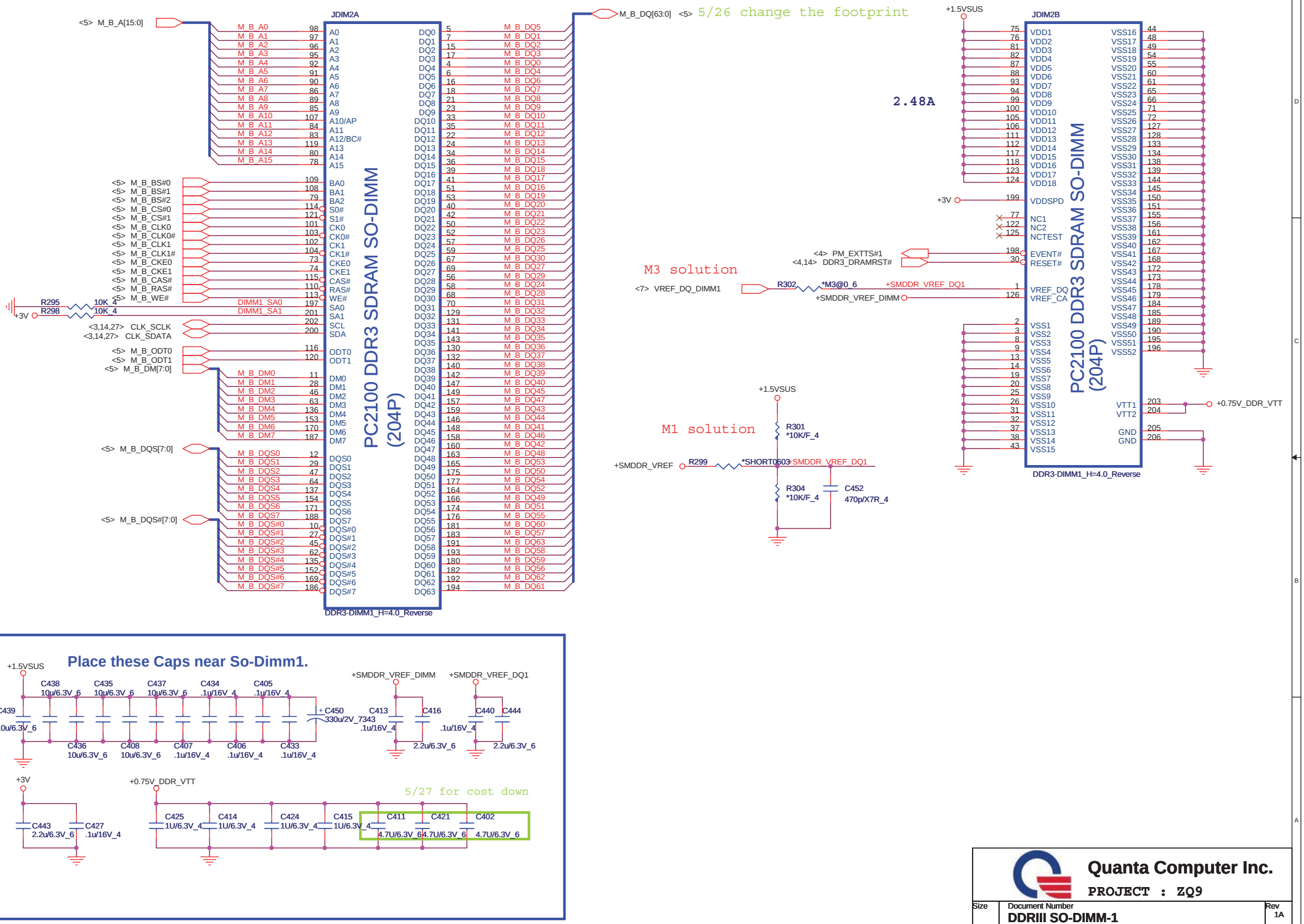

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	DDRIII SO-DIMM-1	1A
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GPU_1(VGA)

For M97, Broadway, Madison and Park PCIE_VDDC is 1.0V

Madison	AJ007720T02
Park	AJ077400T08

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	Madison/Park M2-PCIE I/F	1A
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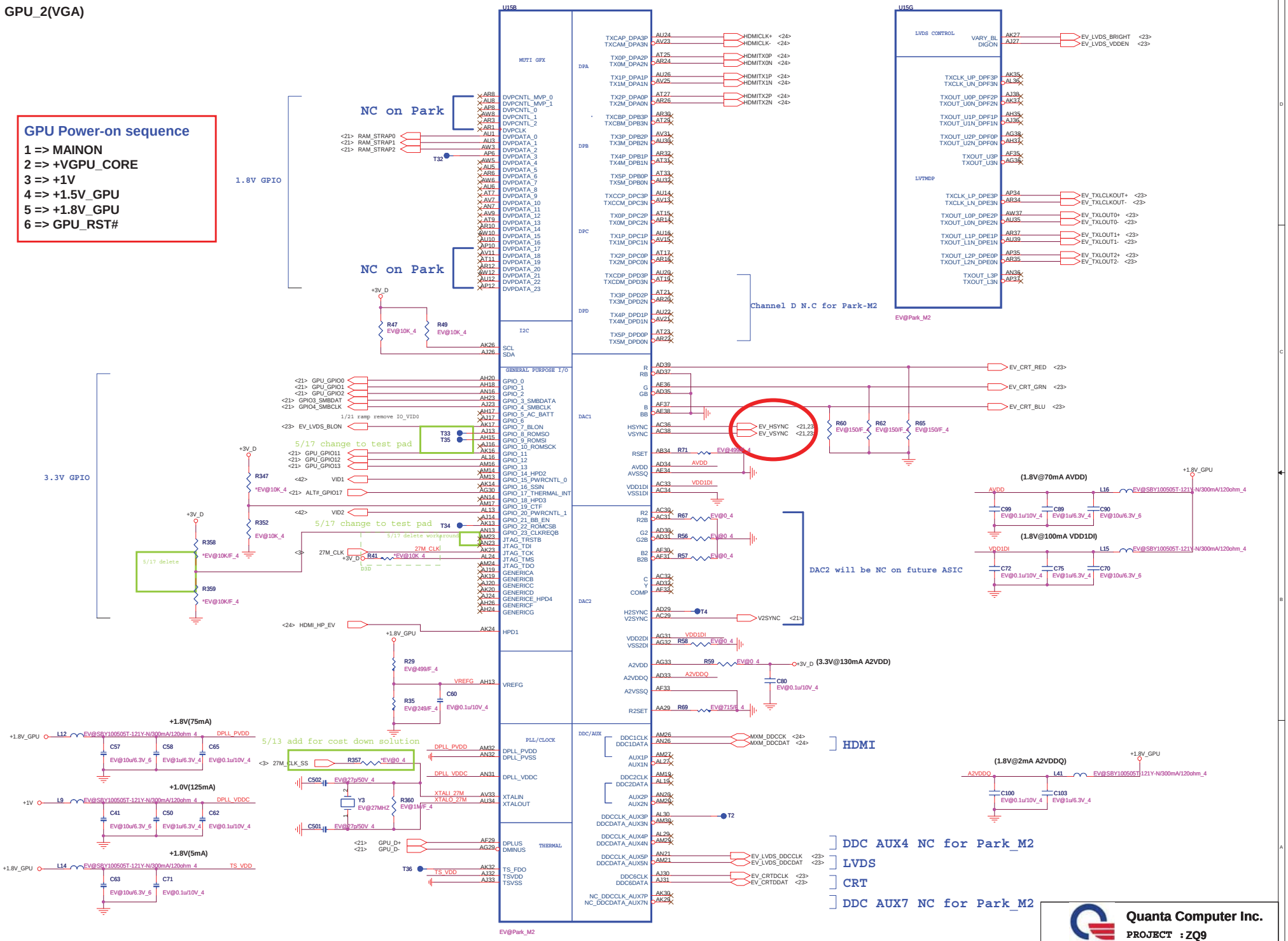
GPU_2(VGA)

GPU Power-on sequence

1 => MAINON
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => GPU_RST#



Quanta Computer Inc.			
PROJECT : ZQ9			
Size	Document Number		Rev
	Madison/Park M2-HOST I/F		1A
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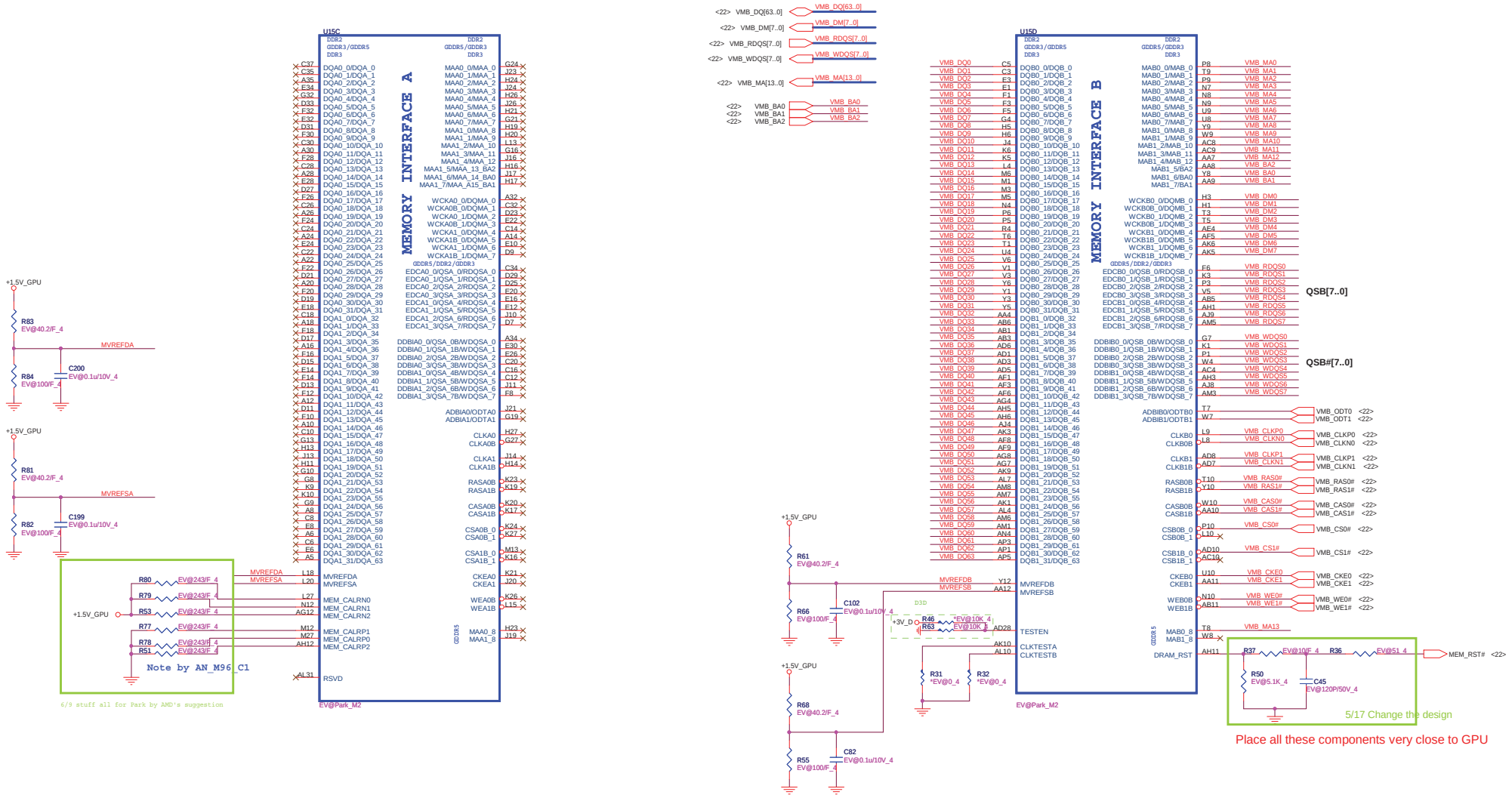
GPU_3(VGA)

Park M2-channel B used(S3 package use Channel A)



Quanta Computer Inc.			
PROJECT : ZQ9			
Size	Document Number		Rev
	Madison/Park M2-MEM I/F		1A
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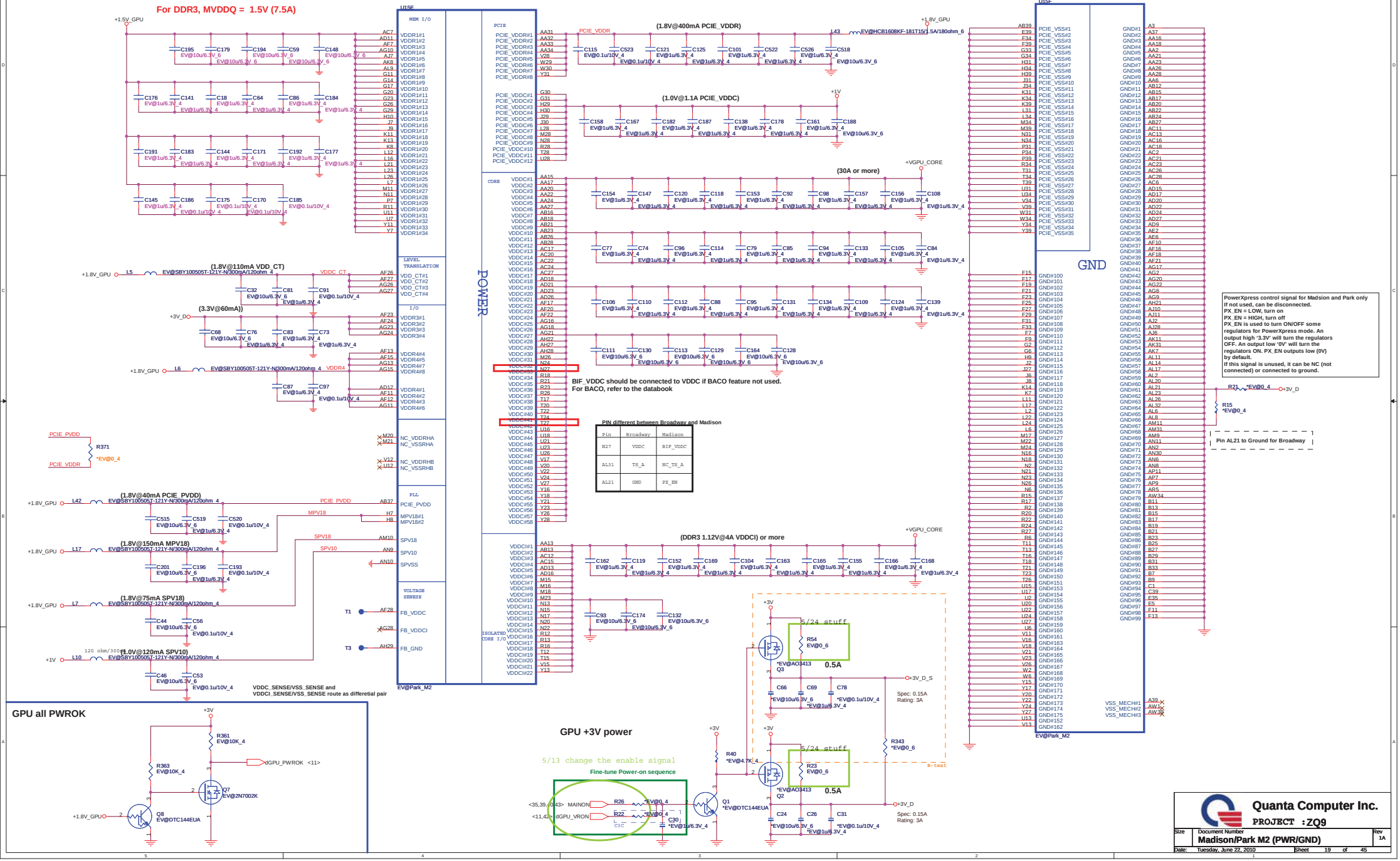
GPU_4(VGA)


For DDR3, MVDDQ = 1.5V (7.5A)
U15E
MEM I/O
POWER
PCIE
CORE
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(DDR3 1.12V@4A VDDCI) or more
BIF_VDDC should be connected to VDDC if BACO feature not used.
For BACO, refer to the databook
PIN different between Broadway and Madison
PowerXpress control signal for Madsion and Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.
Pin AL21 to Ground for Broadway
VDDC_SENSE/VSS_SENSE and VDDCI_SENSE/VSS_SENSE route as differetial pair
EV@Park_M2
U15F
GND
GPU all PWROK
GPU +3V power
5/13 change the enable signal
Fine-tune Power-on sequence
0.5A
Spec: 0.15A
Rating: 3A
Quanta Computer Inc.
PROJECT : ZQ9
Madison/Park M2 (PWR/GND)
Tuesday, June 22, 2010
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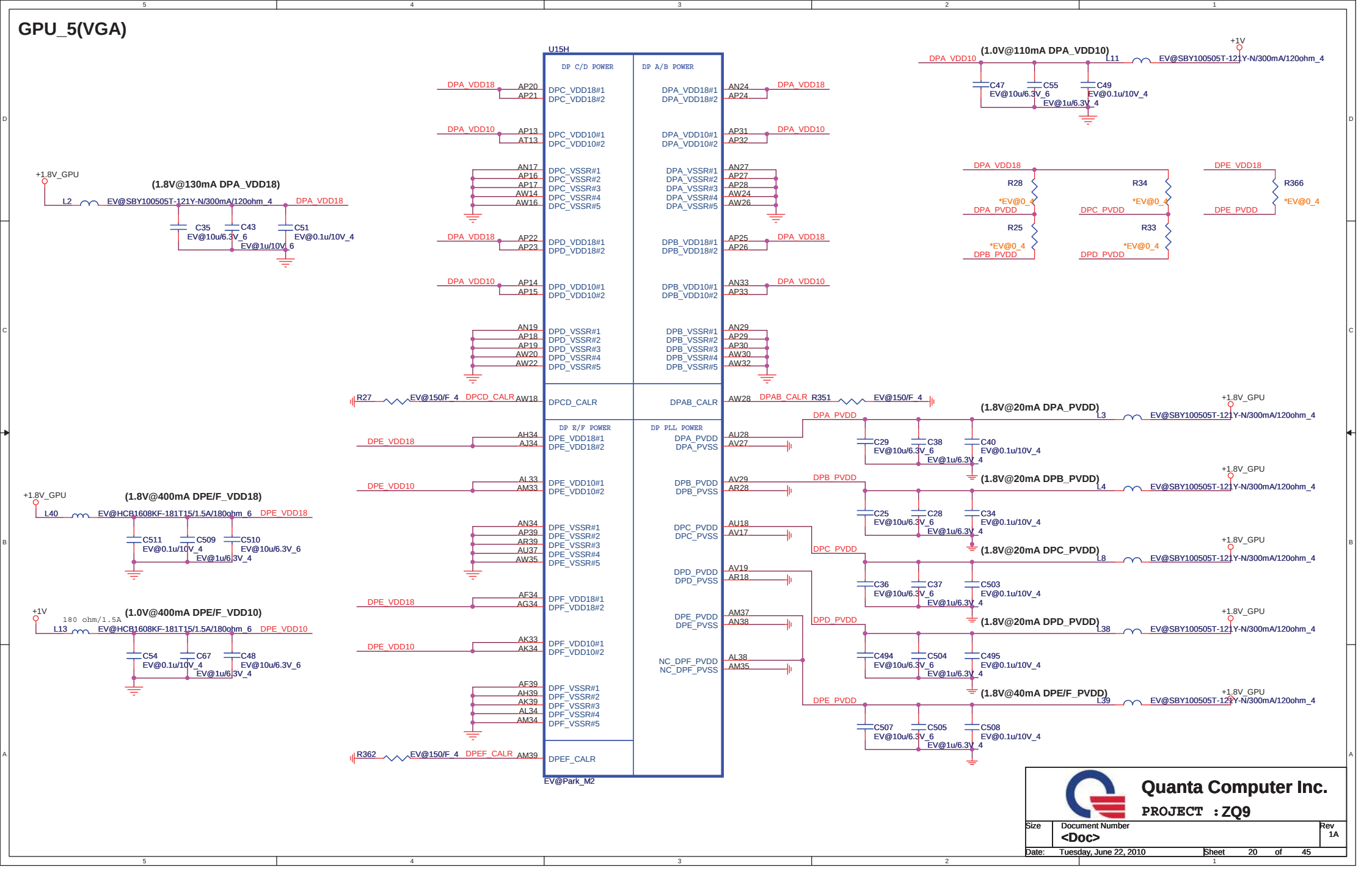
GPU_5(VGA)


U15H
DP C/D POWER
DP A/B POWER
DP E/F POWER
DP PLL POWER
DPC_VDD18#1
DPC_VDD18#2
DPA_VDD18#1
DPA_VDD18#2
DPC_VDD10#1
DPC_VDD10#2
DPA_VDD10#1
DPA_VDD10#2
DPC_VSSR#1
DPC_VSSR#2
DPC_VSSR#3
DPC_VSSR#4
DPC_VSSR#5
DPA_VSSR#1
DPA_VSSR#2
DPA_VSSR#3
DPA_VSSR#4
DPA_VSSR#5
DPD_VDD18#1
DPD_VDD18#2
DPB_VDD18#1
DPB_VDD18#2
DPD_VDD10#1
DPD_VDD10#2
DPB_VDD10#1
DPB_VDD10#2
DPD_VSSR#1
DPD_VSSR#2
DPD_VSSR#3
DPD_VSSR#4
DPD_VSSR#5
DPB_VSSR#1
DPB_VSSR#2
DPB_VSSR#3
DPB_VSSR#4
DPB_VSSR#5
DPCD_CALR
DPAB_CALR
DPE_VDD18#1
DPE_VDD18#2
DPA_PVDD
DPA_PVSS
DPE_VDD10#1
DPE_VDD10#2
DPB_PVDD
DPB_PVSS
DPE_VSSR#1
DPE_VSSR#2
DPE_VSSR#3
DPE_VSSR#4
DPE_VSSR#5
DPC_PVDD
DPC_PVSS
DPF_VDD18#1
DPF_VDD18#2
DPD_PVDD
DPD_PVSS
DPF_VDD10#1
DPF_VDD10#2
DPE_PVDD
DPE_PVSS
DPF_VSSR#1
DPF_VSSR#2
DPF_VSSR#3
DPF_VSSR#4
DPF_VSSR#5
NC_DPF_PVDD
NC_DPF_PVSS
DPEF_CALR
EV@Park_M2
(1.0V@110mA DPA_VDD10)
(1.8V@130mA DPA_VDD18)
(1.8V@400mA DPE/F_VDD18)
(1.0V@400mA DPE/F_VDD10)
(1.8V@20mA DPA_PVDD)
(1.8V@20mA DPB_PVDD)
(1.8V@20mA DPC_PVDD)
(1.8V@20mA DPD_PVDD)
(1.8V@40mA DPE/F_PVDD)
EV@SBY100505T-121Y-N/300mA/120ohm_4
EV@HCB1608KF-181T15/1.5A/180ohm_6
EV@150/F_4
EV@10u/6.3V_6
EV@0.1u/10V_4
EV@1u/6.3V_4
EV@1u/10V_6
*EV@0_4
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<Doc>
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1A
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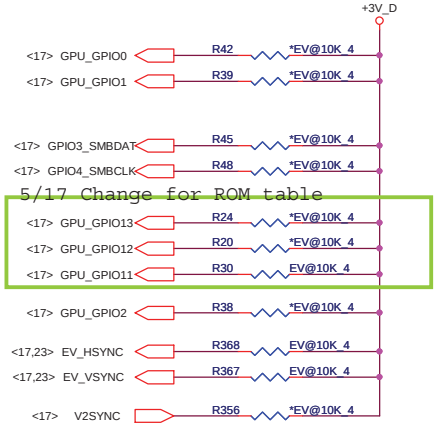
PIN STRAPS(VGA)



Size of the primary memory apertures	GPIO[13:11]
128 MB	000
256MB	001
64 MB	010
32 MB	011
More than 512 MB	Not Supported

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

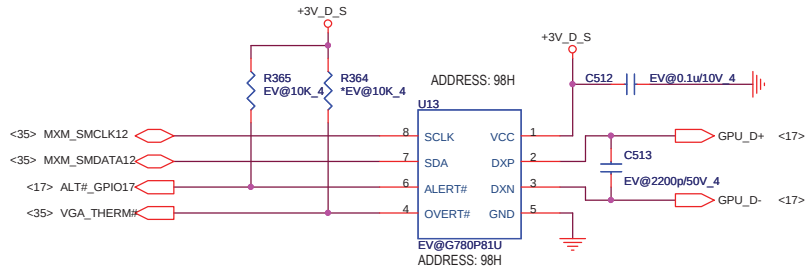
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	Enable external BIOS ROM device 0 - Disable external BIOS ROM device 1 - Enable external BIOS ROM device	0	
ROMIDCFG[2:0]	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	001	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

EEPROM(VGA) 5/17 delete EEPROM

Thermal Sensor(VGA)

Vendor	P/N
WINDBOND	AL83L771K01
GMT	AL000780000

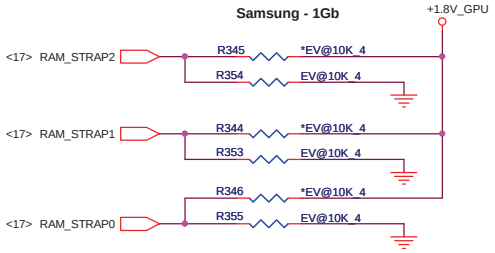
USD0.16



DDR3 Memory Aperture size(GPU)

DDR3 Memory size

Vendor	Vendor P/N	STN B/S P/N	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1	0	0
	H5TQ2G63BFR-12C	AKD5MGGTW03 (128M*16)	1	0	1
Samsung					
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500 (128m*16)	0	0	1
AMD	23EY2387MA12-SZ	AKD5LGGT700	0	1	0



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

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	Strip/Thermal	1A

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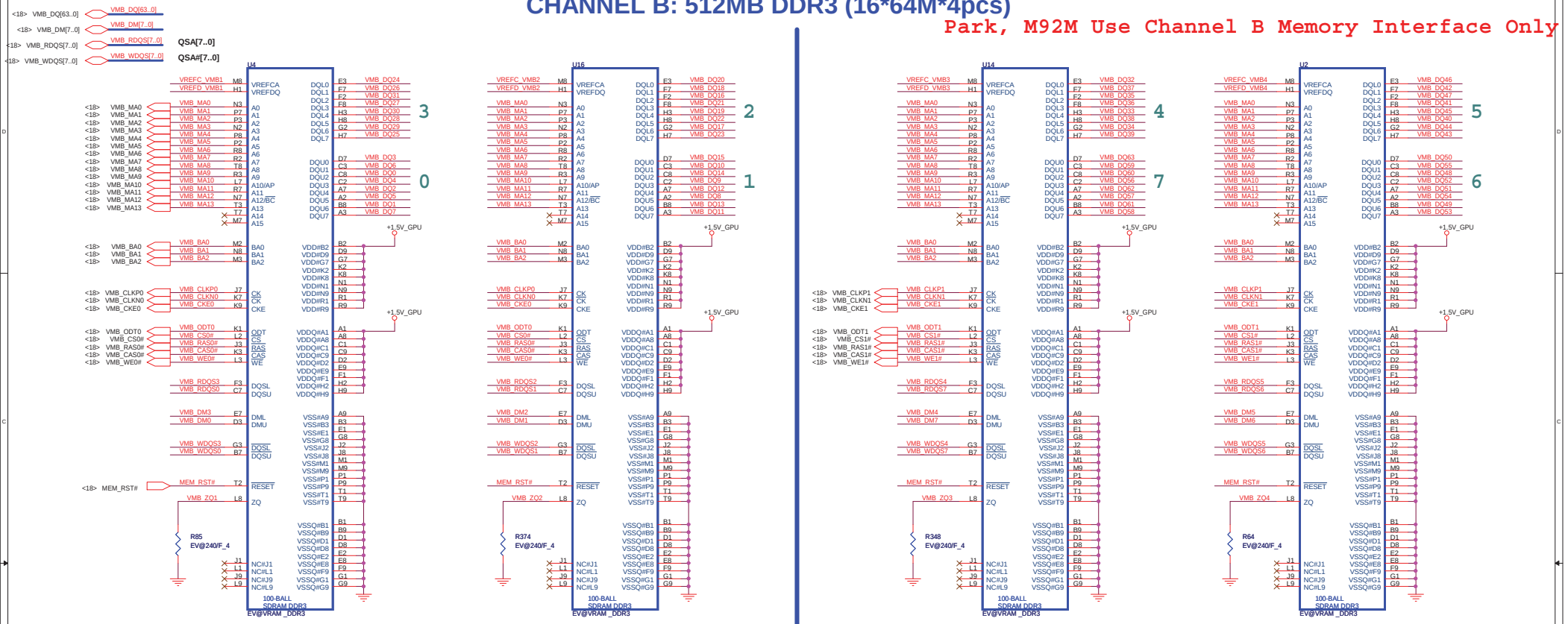
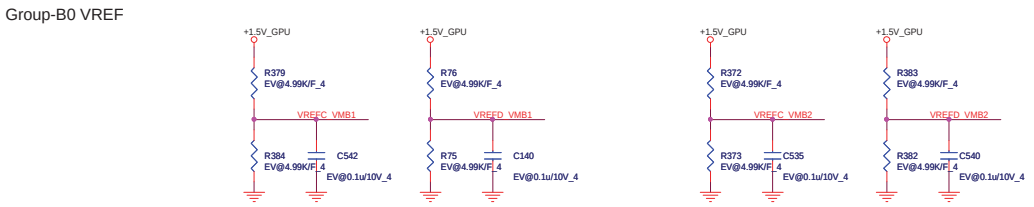
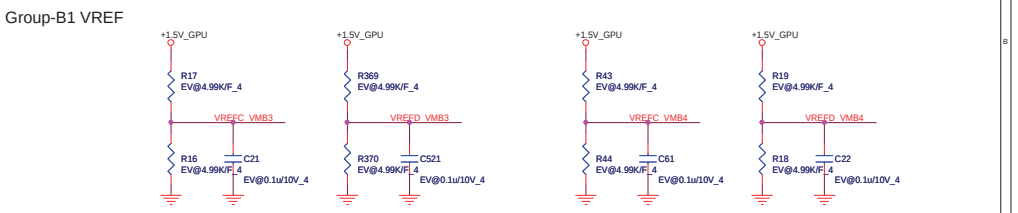
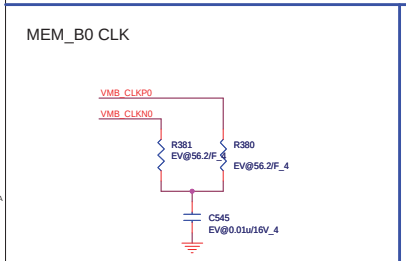
CHANNEL B: 512MB DDR3 (16*64M*4pcs)

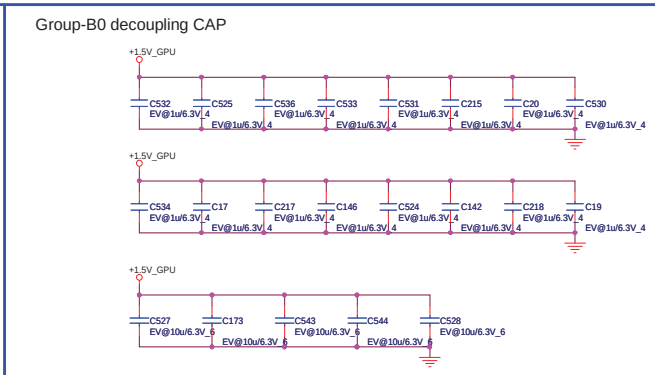
Park, M92M Use Channel B Memory Interface Only

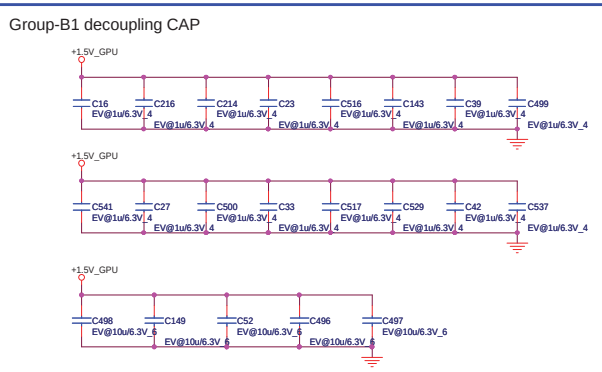


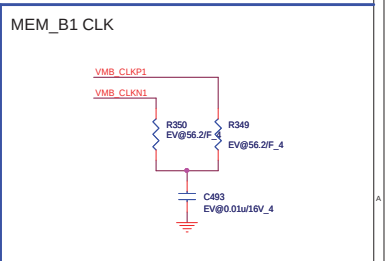












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Size	Document Number	Rev
	MEMORY 2 channel B	1A

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CRT Switch

IV@ 0_ohm Resistor place close to Joint-Point
EV@

<8> INT_CRT_RED — INT_CRT_RED — R95 — IV@0_4 — VGA_RED
<8> INT_CRT_GRN — INT_CRT_GRN — R94 — IV@0_4 — VGA_GRN
<8> INT_CRT_BLU — INT_CRT_BLU — R93 — IV@0_4 — VGA_BLU

RN7 IV@0_4P2R
<8> INT_VSYNC — INT_VSYNC — 1 — 2 — VSYNC
<8> INT_HSYNC — INT_HSYNC — 3 — 4 — HSYNC

RN8 IV@0_4P2R
<8> INT_CRT_DDCDAT — INT_CRT_DDCDAT — 1 — 2 — CRTDDATA
<8> INT_CRT_DDCCLK — INT_CRT_DDCCLK — 3 — 4 — CRTDCLK

<17> EV_CRT_BLU — EV_CRT_BLU — R391 — EV@0_4 — VGA_BLU
<17> EV_CRT_GRN — EV_CRT_GRN — R397 — EV@0_4 — VGA_GRN
<17> EV_CRT_RED — EV_CRT_RED — R399 — EV@0_4 — VGA_RED

RN15 EV@0_4P2R
<17,21> EV_HSYNC — EV_HSYNC — 1 — 2 — HSYNC
<17,21> EV_VSYNC — EV_VSYNC — 3 — 4 — VSYNC

RN16 EV@0_4P2R
<17> EV_CRTDCLK — EV_CRTDCLK — 1 — 2 — CRTDCLK
<17> EV_CRTDDAT — EV_CRTDDAT — 3 — 4 — CRTDDATA

CRT

+5V — F2 SMD1206P110TFT — D16 SSM22LLPT — CRTVDD5
C272 0.1u/10V_4_X7R

VGA_RED — L27 BLM18BA750SN1D/0.3A/75ohm_6 — CRT_R1
VGA_GRN — L26 BLM18BA750SN1D/0.3A/75ohm_6 — CRT_G1
VGA_BLU — L25 BLM18BA750SN1D/0.3A/75ohm_6 — CRT_B1

R189 150/F_4 | R177 150/F_4 | R165 150/F_4 | C322 10p/50V_4 | C308 10p/50V_4 | C293 10p/50V_4 | C637 10p/50V_4 | C647 10p/50V_4 | C653 10p/50V_4

CN8 CRT-CONN
CRT_R1 — 5
CRT_G1 — 10
CRT_B1 — 15
CRT_11 — T22
DDCDAT_1 — 12
CRTHSYNC — 13
CRTVSYNC — 14
DDCCLK_1 — 15

+3V — C301 0.1u/10V_4_X7R
+3V — C315 0.1u/10V_4_X7R
C632 22u/25V_6 — CRT_BYP

U23 CM2009-02QR
CRTVDD5 — 1 VCC_SYNC
2 VCC_VIDEO
7 VCC_DDC BYP
8 CRT_BYP
3 CRT_R1 VIDEO_1
4 CRT_G1 VIDEO_2
5 CRT_B1 VIDEO_3
6 GND
16 SYNC_OUT2 — CRT_VSYNC2
14 SYNC_OUT1 — CRT_HSYNC2
15 SYNC_IN2 — VSYNC
13 SYNC_IN1 — HSYNC
10 DDC_IN1 — CRTDCLK
11 DDC_IN2 — CRTDDATA
9 DDC_OUT1 — DDCCLK_1
12 DDC_OUT2 — DDCDAT_1

6/21 change to 0 ohm
R458 0_4 — CRTVSYNC
R457 0_4 — CRTHSYNC

+3V — R462 2.7K_4 — R469 2.7K_4
CRTVDD5 — R452 2.7K_4 — R476 2.7K_4

C661 *.1u/10V_4 — CRTVDD5
C620 *10p/50V_4 — CRTVSYNC
C619 *10p/50V_4 — CRTHSYNC
C631 10p/50V_4 — DDCCLK_1
C646 10p/50V_4 — DDCDAT_1

LVDS

0_ohm Resistor place close to Joint-Point

RN1 EV@0_4P2R
<17> EV_LVDS_DDCCLK — EV_LVDS_DDCCLK — 1 — 2 — LCD_EDIDCLK
<17> EV_LVDS_DDCDAT — EV_LVDS_DDCDAT — 3 — 4 — LCD_EDIDDATA

RN14 EV@0_4P2R
<17> EV_LVDS_VDDEN — EV_LVDS_VDDEN — 1 — 2 — LVDS_VDDEN
<17> EV_LVDS_BLON — EV_LVDS_BLON — 3 — 4 — LVDS_BLON

RN9 IV@0_4P2R
<8> INT_LVDS_EDIDCLK — INT_LVDS_EDIDCLK — 1 — 2 — LCD_EDIDCLK
<8> INT_LVDS_EDIDDATA — INT_LVDS_EDIDDATA — 3 — 4 — LCD_EDIDDATA

RN6 IV@0_4P2R
<8> INT_LVDS_DIGON — INT_LVDS_DIGON — 1 — 2 — LVDS_VDDEN
<8> INT_LVDS_BLON — INT_LVDS_BLON — 3 — 4 — LVDS_BLON

RN5 EV@0_4P2R
<17> EV_TXLCLKOUT- — EV_TXLCLKOUT- — 1 — 2 — TXLCLKOUT-
<17> EV_TXLCLKOUT+ — EV_TXLCLKOUT+ — 3 — 4 — TXLCLKOUT+
RN2 EV@0_4P2R
<17> EV_TXLOUT0- — EV_TXLOUT0- — 1 — 2 — TXLOUT0-
<17> EV_TXLOUT0+ — EV_TXLOUT0+ — 3 — 4 — TXLOUT0+
RN3 EV@0_4P2R
<17> EV_TXLOUT1- — EV_TXLOUT1- — 1 — 2 — TXLOUT1-
<17> EV_TXLOUT1+ — EV_TXLOUT1+ — 3 — 4 — TXLOUT1+
RN4 EV@0_4P2R
<17> EV_TXLOUT2- — EV_TXLOUT2- — 1 — 2 — TXLOUT2-
<17> EV_TXLOUT2+ — EV_TXLOUT2+ — 3 — 4 — TXLOUT2+

RN10 IV@0_4P2R
<8> INT_TXLCLKOUT+ — INT_TXLCLKOUT+ — 1 — 2 — TXLCLKOUT+
<8> INT_TXLCLKOUT- — INT_TXLCLKOUT- — 3 — 4 — TXLCLKOUT-
RN13 IV@0_4P2R
<8> INT_TXLOUT0+ — INT_TXLOUT0+ — 1 — 2 — TXLOUT0+
<8> INT_TXLOUT0- — INT_TXLOUT0- — 3 — 4 — TXLOUT0-
RN12 IV@0_4P2R
<8> INT_TXLOUT1+ — INT_TXLOUT1+ — 1 — 2 — TXLOUT1+
<8> INT_TXLOUT1- — INT_TXLOUT1- — 3 — 4 — TXLOUT1-
RN11 IV@0_4P2R
<8> INT_TXLOUT2+ — INT_TXLOUT2+ — 1 — 2 — TXLOUT2+
<8> INT_TXLOUT2- — INT_TXLOUT2- — 3 — 4 — TXLOUT2-

<35> CONTRAST — R7 EV@0_4
<17> EV_LVDS_BRIGHT — R12 *0_4 — LVDS_BRIGHT
<8> INT_LVDS_BRIGHT — R13 IV@0_4

LVDS

+3V — C8 0.1u/10V_4_X7R — C7 1000p/50V_4
VIN — C2 4.7u/25V_8 — C3 1000p/50V_4

5/7 add
C11 *1u/6.3V_4 — C14 *1u/6.3V_4
LCDVCC — R11 0_6

VIN — R8 *SHORT0805 — R14 *SHORT0805 — 0.8A — INVCC0
+3V — R9 2.2K_4 — LCD_EDIDCLK
R10 2.2K_4 — LCD_EDIDDATA

CN5
TXLOUT0- / TXLOUT0+
TXLOUT1- / TXLOUT1+
TXLOUT2- / TXLOUT2+
TXLCLKOUT- / TXLCLKOUT+
USBP8- R / USBP8+ R
CCD_PWR
LVDS_BRIGHT — R6 BLM15AG121SS1/0.5A/120ohm_4 — BL_ON
LVDS

5/7 add
C12 *1u/6.3V_4 — C13 *1u/6.3V_4
+3V — R5 0_6
CCD-USB

CCD +3V-current budget 0.2A

5/21 Change the LVDS connector and swap

<10> USBP8+ — R2 *0_4 — L1 RFCMF1632100M3T/200mA/90ohm — R3 *0_4 — USBP8+ R
<10> USBP8- — USBP8- R

+3VPCU — C491 0.1u/10V_4_X7R
HE1 PT3661-BB — LID591#
D13 *VPORT_6
PT3661-BB : AL003661003
EM-6781-T3 : AL006781000

Lid Switch (Hall sensor)

LCD Power

+3V — C1 1U/6.3V_4
U1 AAT4280-4
IN — IN — ON/OFF — OUT — GND — GND
LVDS_VDDEN
R4 100K_4
C6 *.1u/10V_4 — C5 *2.2u/10V_8 — C9 0.1u/10V_4_X7R — C10 R01u/25V_4 — C4 22u/6.3V_8
LCDVCC

Backlight Control

+3VPCU — R375 *100K_4 — LID591# <35>
LID591#,EC intrnal PU

+3V — D14 BAS316
R376 10K_4 — BL_ON
R377 10K_4 — BL#
Q10 2N7002K
Q9 DTC144EUA — EC_FPBACK# <35>
LVDS_BLON
Q11 2N7002K
R378 100K_4

Quanta Computer Inc.
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Size	Document Number	Rev
	CRT/LVDS/CAMERA/LID	1A

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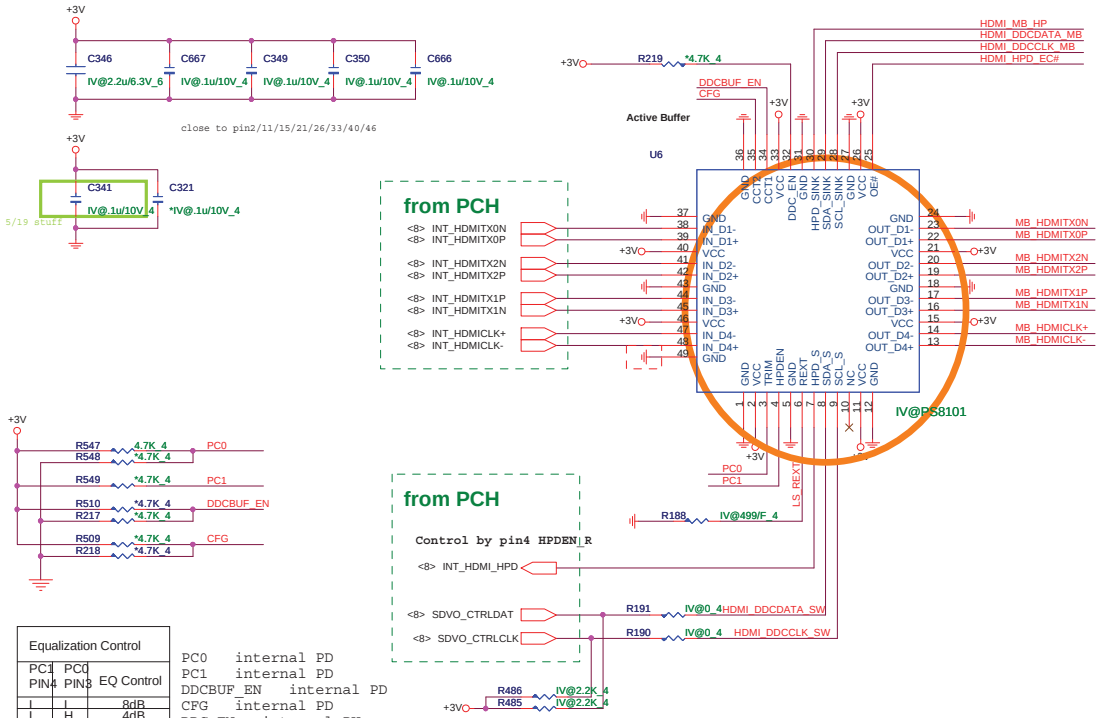
I@ HDMI LEVEL SHIFTER

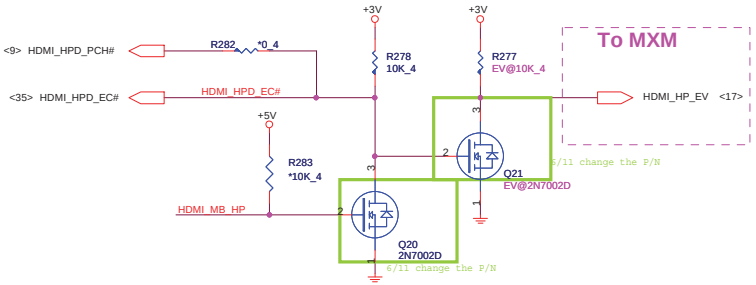
IV@
EV@



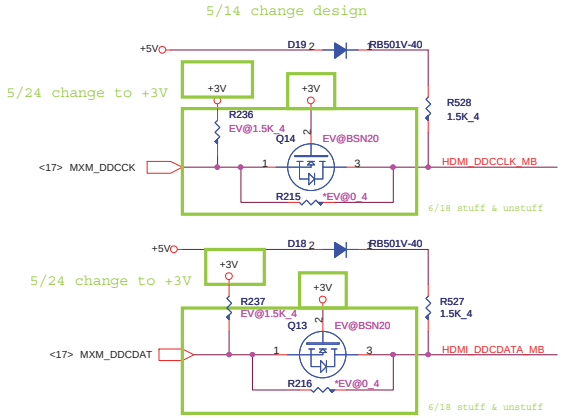
Equalization Control		
PC1 PIN4	PC0 PIN3	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

PC0 internal PD
PC1 internal PD
DDCBUF_EN internal PD
CFG internal PD
DDC_EN internal PU

SW@HDMI-detect



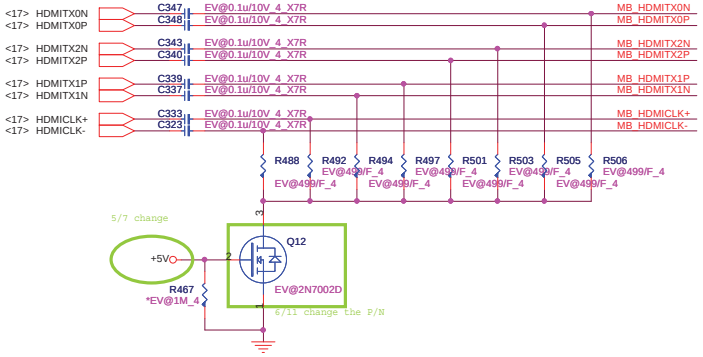
I2C



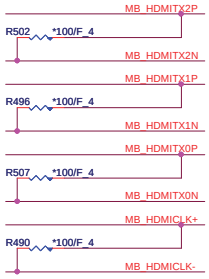
AC-coupling CAP place close to HDMI-connector

Switchable Graphic HDMI source

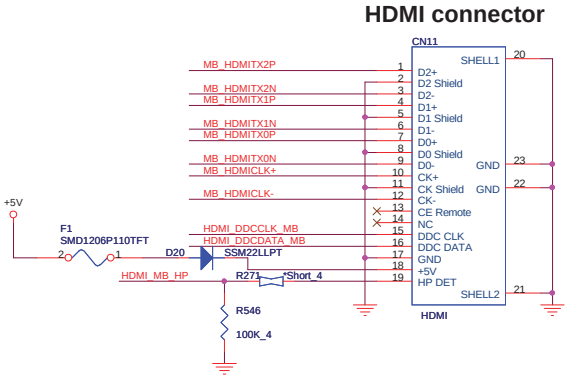
From GPU



EMI

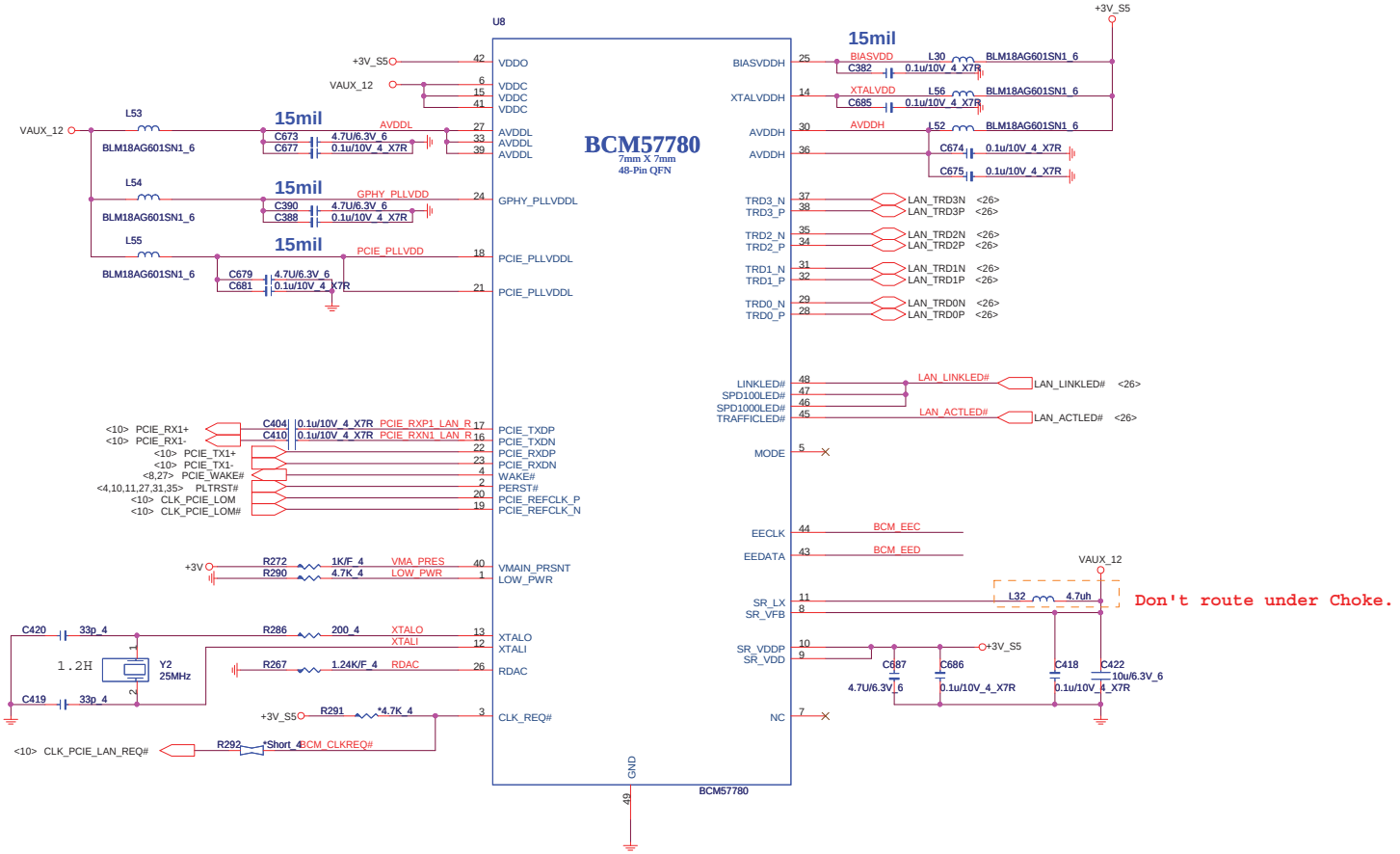


HDMI connector

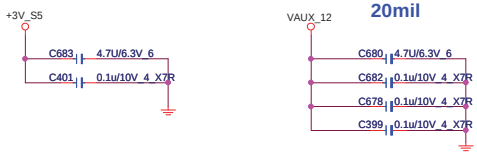


Quanta Computer Inc.
PROJECT : ZQ9
Size | Document Number | Rev
HDMI (PS8101) | 1A
Date: Tuesday, June 22, 2010 | Sheet 24 of 45

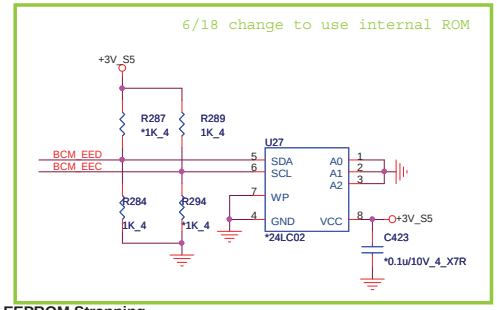
Giga-LAN BCM57780



LAN POWER



EEPROM



EEPROM Strapping

EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

A version Still mount the EEPROM

Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	GLAN BCM57780	1A

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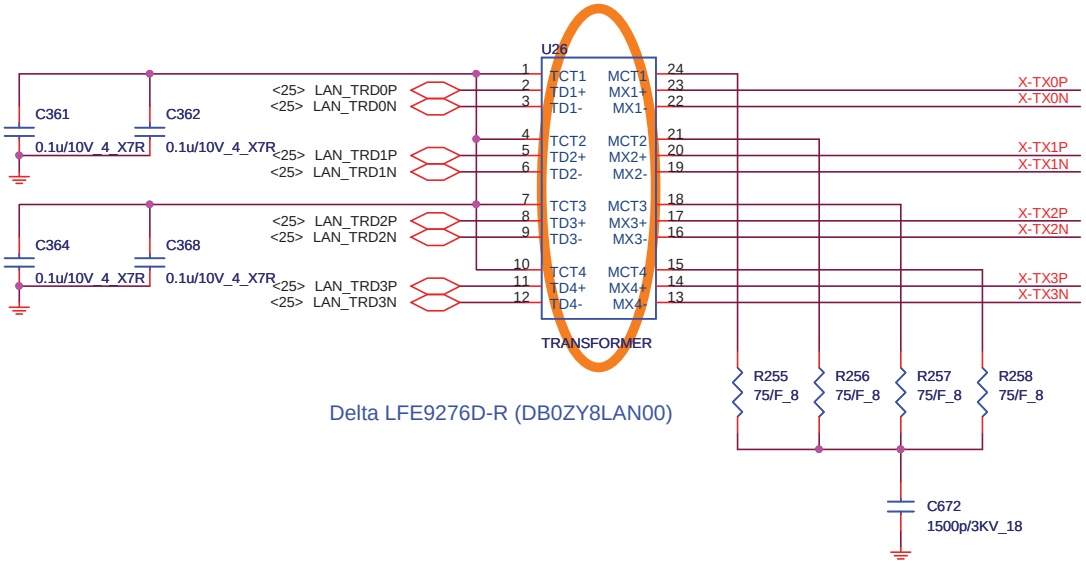
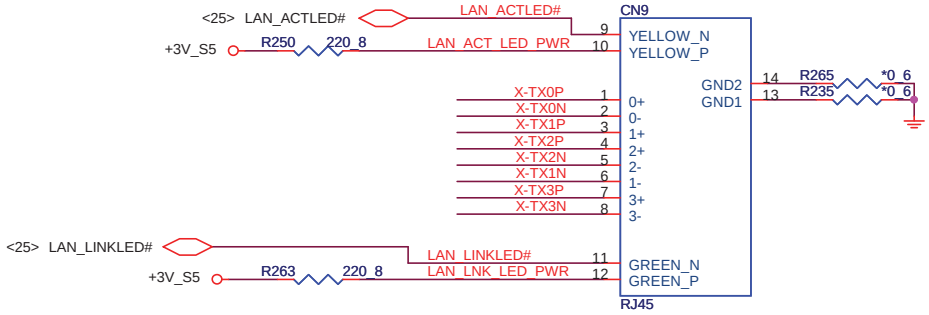
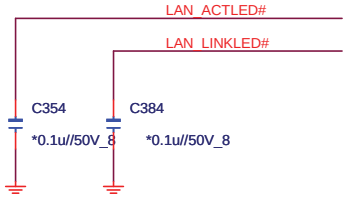
TRANSFORMER



Delta LFE9276D-R (DB0ZY8LAN00)





Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number: LAN Transformer and RJ45	Rev: 1A
Date: Tuesday, June 22, 2010	Sheet 26 of 45	

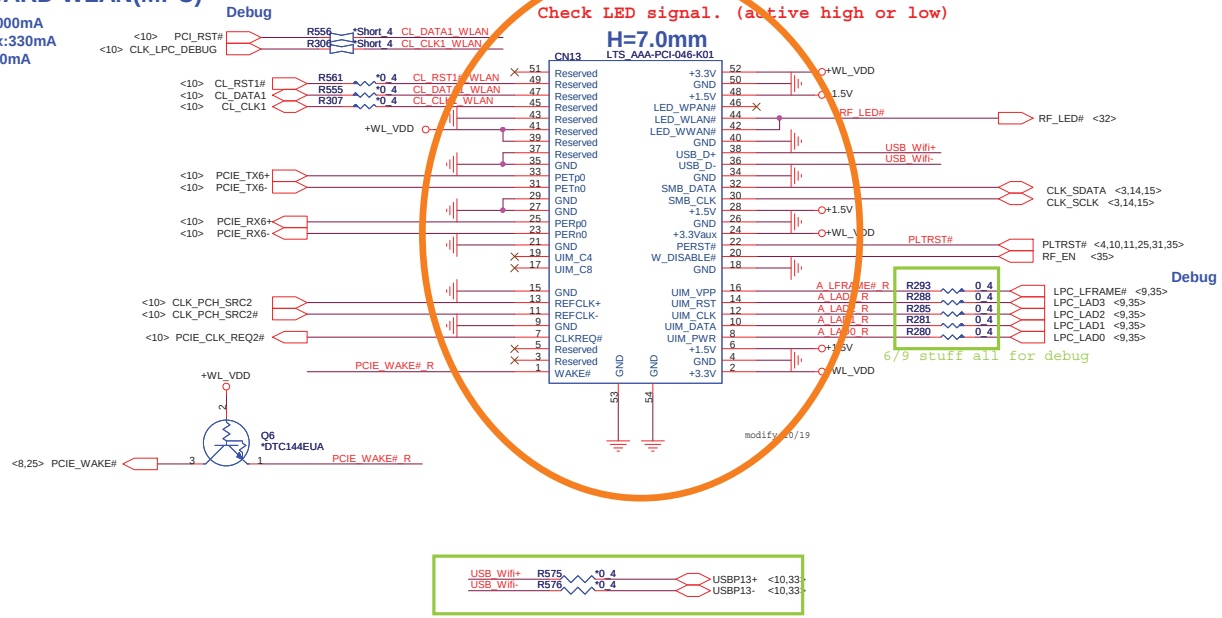
MINI-CARD WLAN(MPC)

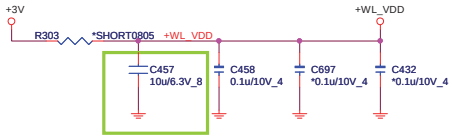
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Debug

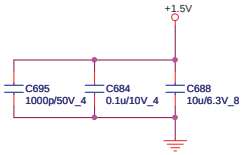
Check LED signal. (active high or low)

H=7.0mm



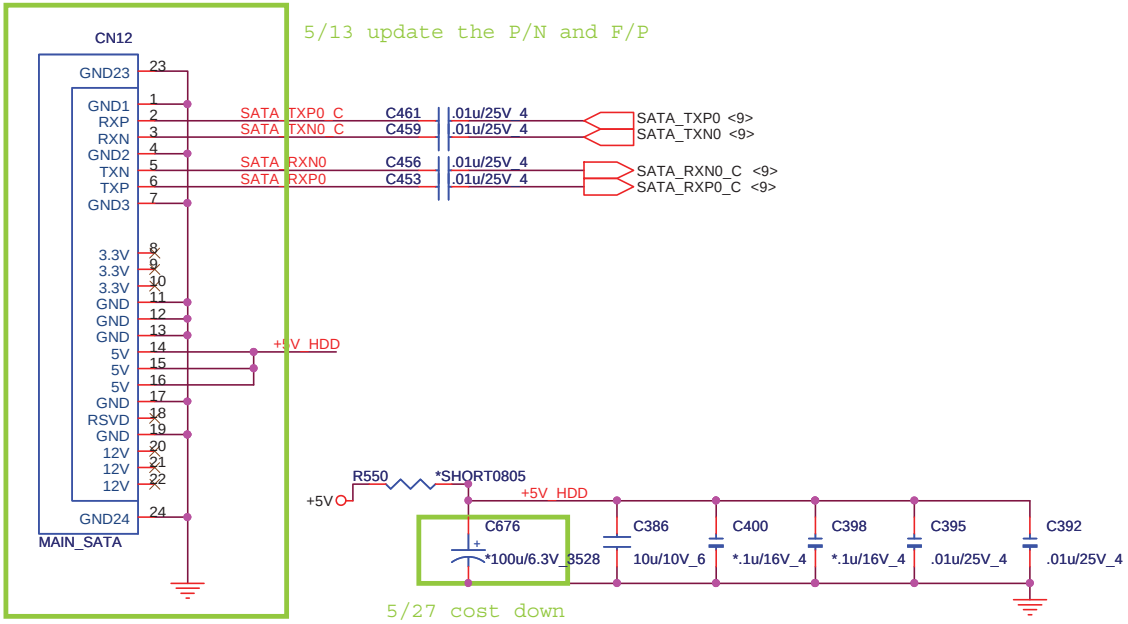


5/13 change to 6.3V

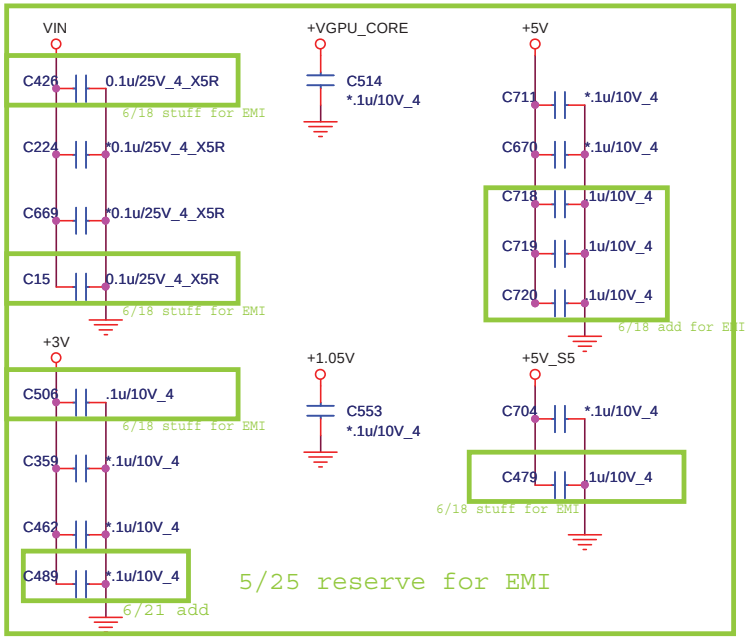


Quanta Computer Inc.			
PROJECT : ZQ9			
Size	Document Number		Rev
	MINI PCI-E card/TV		1A
Date: Tuesday, June 22, 2010		Sheet 27 of 45	

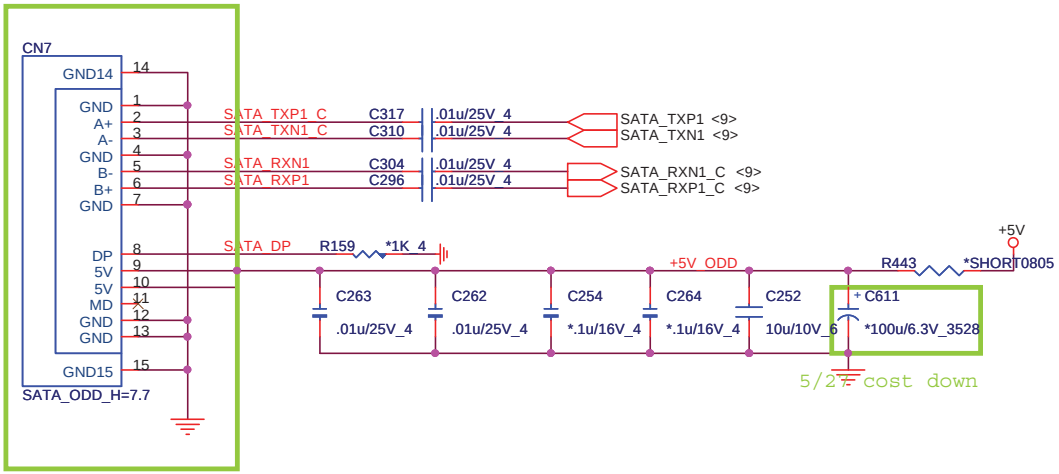
MAIN SATA HDD



EE RETURN-PATH CAPACITORS

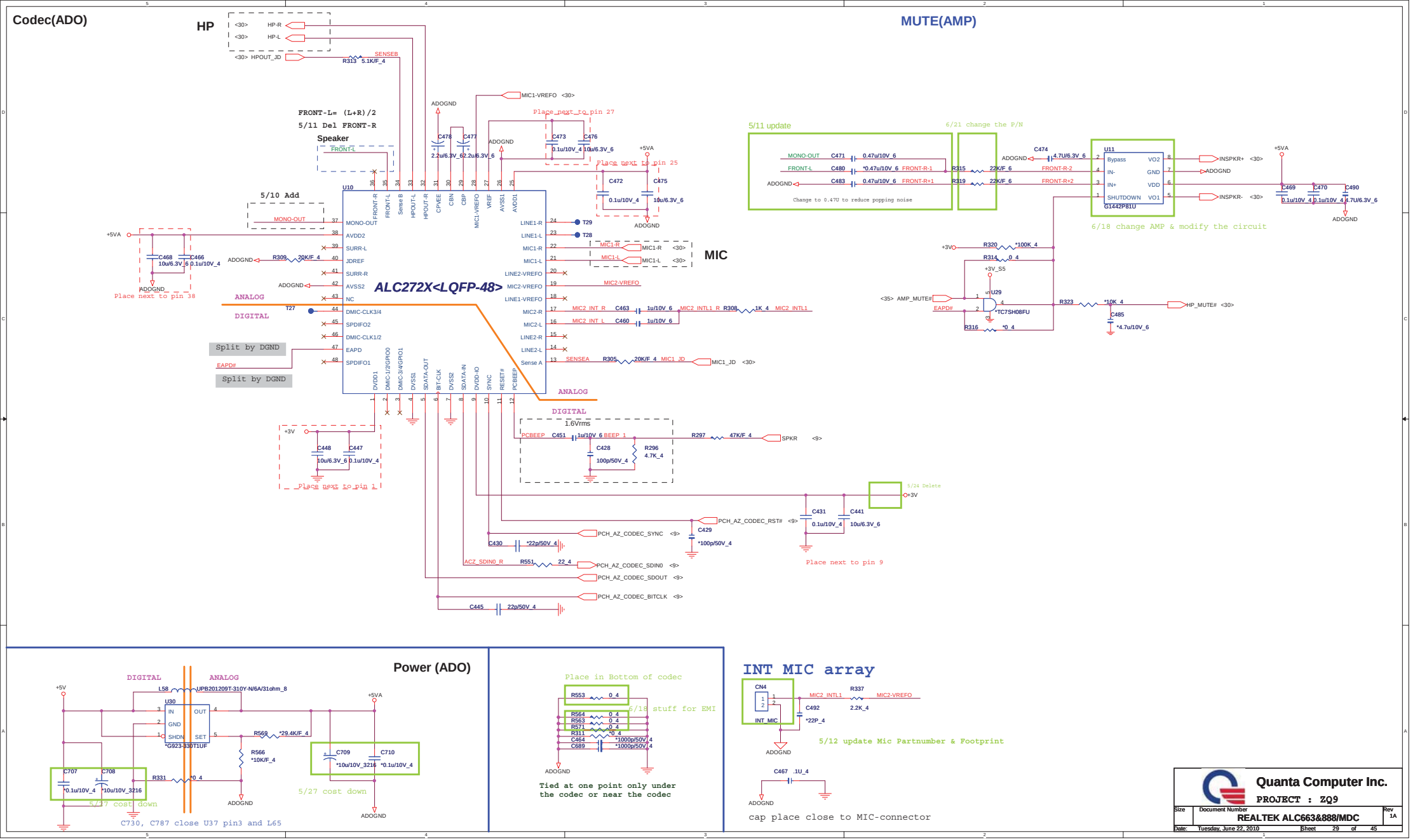


ODD (SATA)

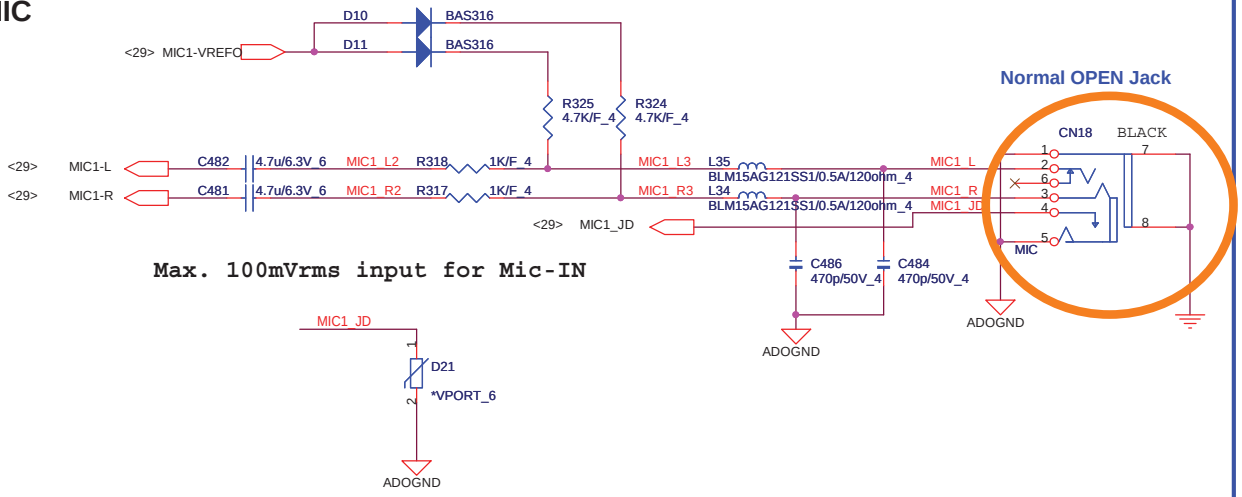


5/26 change the footprint

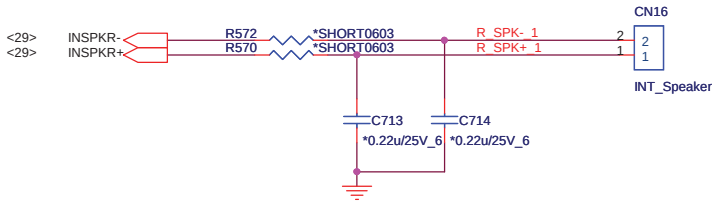
Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number: SATA-HDD/ODD/USB-ESATA	Rev: 1A
Date: Tuesday, June 22, 2010	Sheet 28 of 45	


Codec(ADO)
HP
MUTE(AMP)
MIC
ALC272X<LQFP-48>
Power (DEGO)
INT MIC array
Quanta Computer Inc.
PROJECT : ZQ9
REALTEK ALC663&888/MDC
Tuesday, June 22, 2010

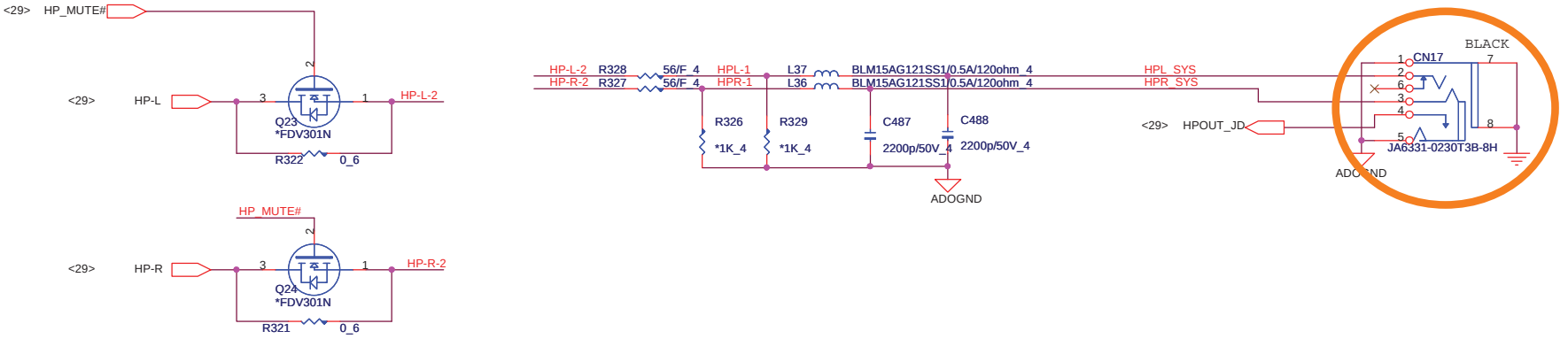
MIC

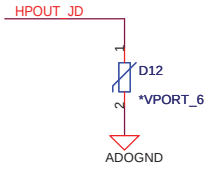


Internal Speaker



HP/SPDIF





Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
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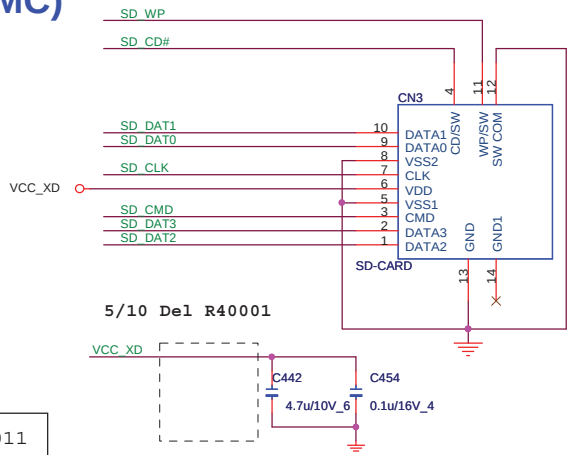
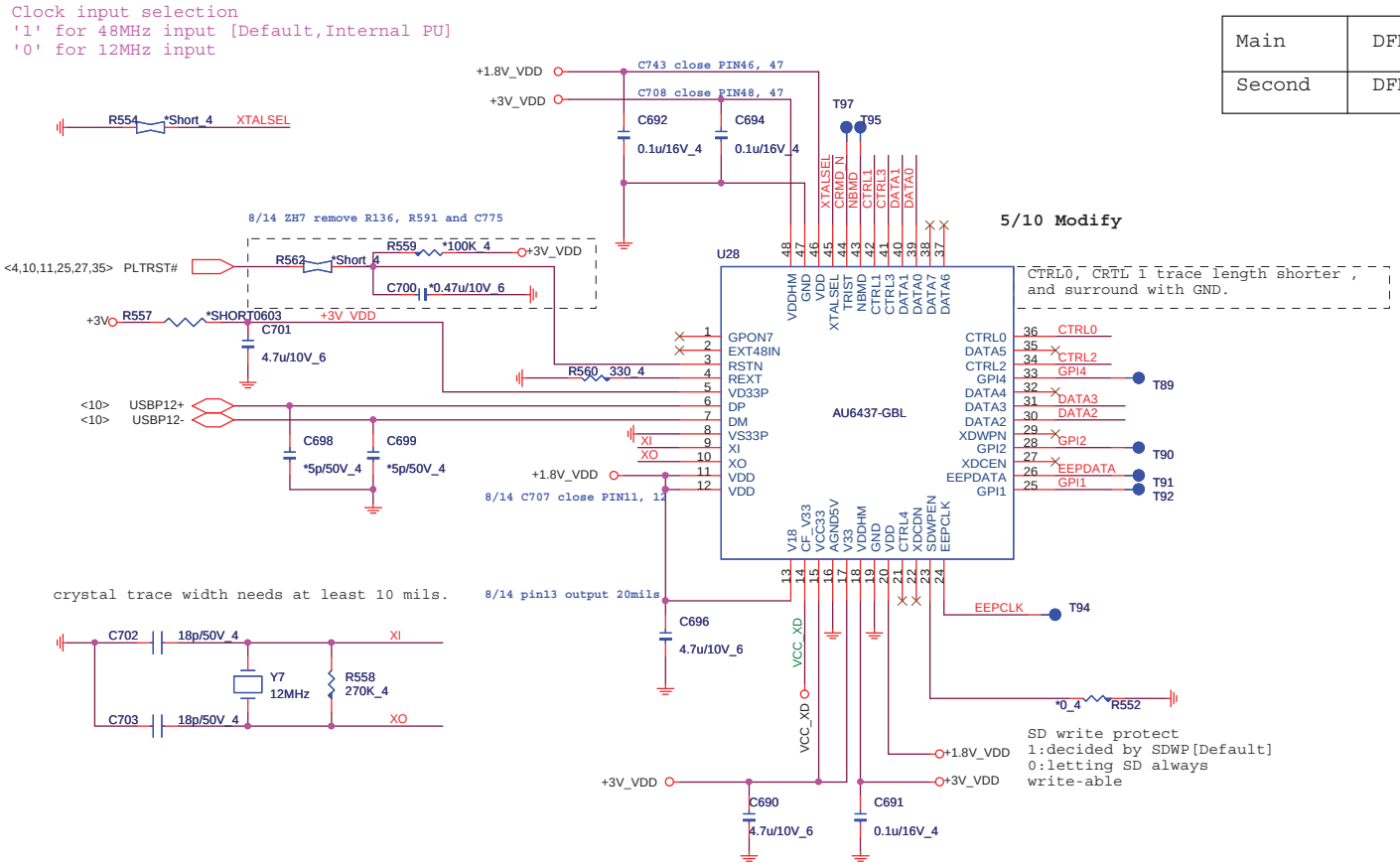
CARD READER Controller

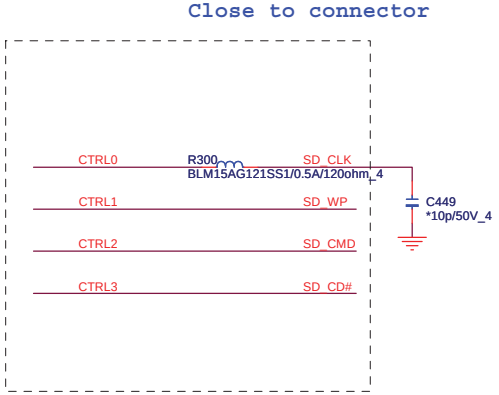
2 IN 1 CARD READER (SD/MMC)



Main	DFHS11FR011
Second	DFHS11FR033

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt





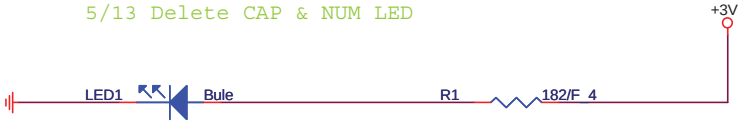
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
Date: Tuesday, June 22, 2010	Sheet 31 of 43	

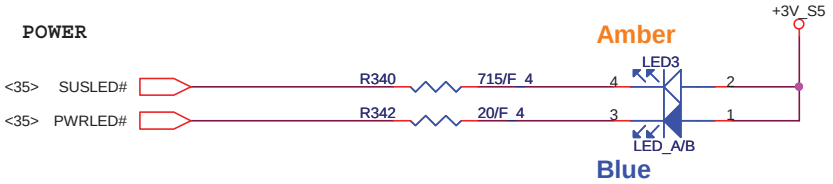
LED

5/13 Delete CAP & NUM LED

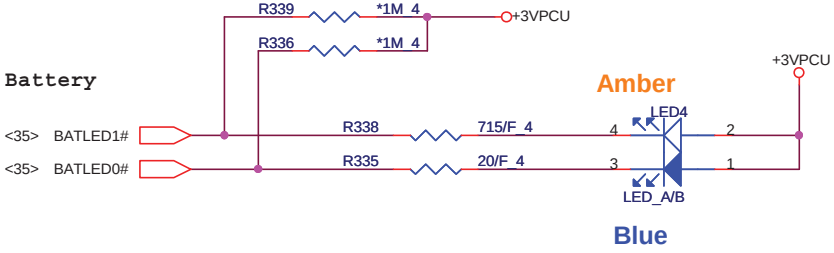
Power LED



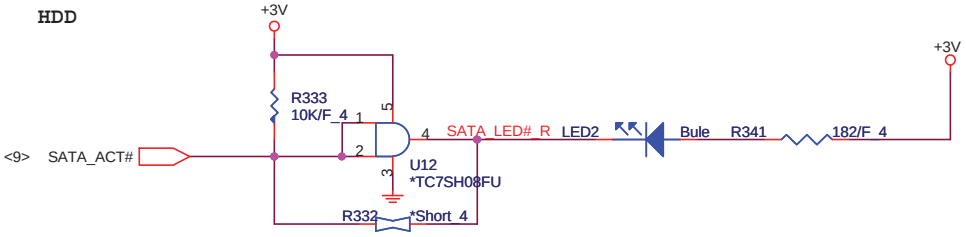
POWER



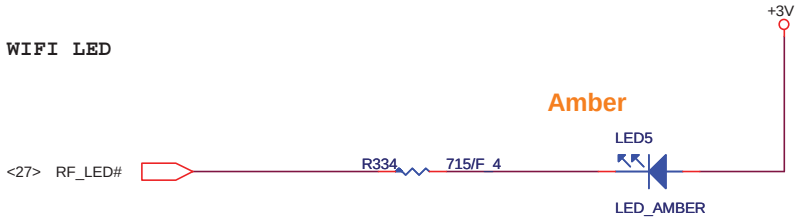
Battery



HDD



WIFI LED

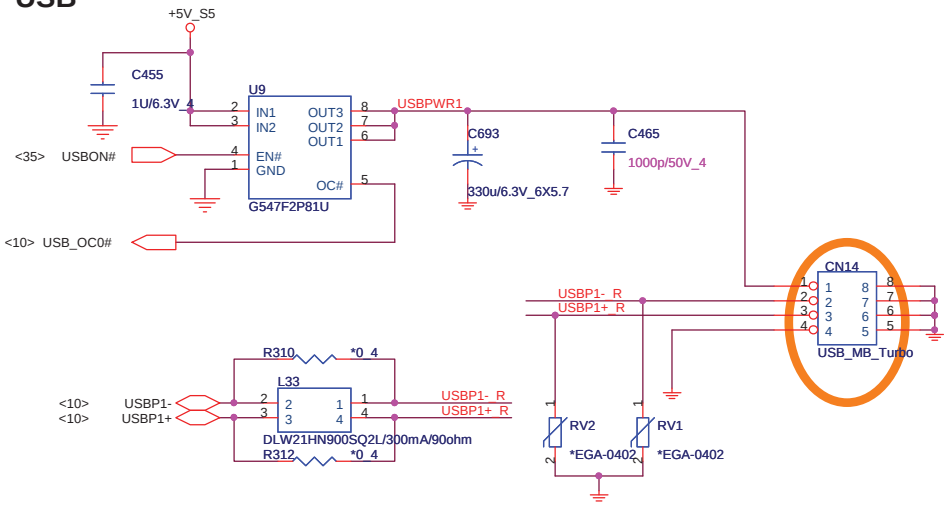


Quanta Computer Inc.

PROJECT : ZQ9

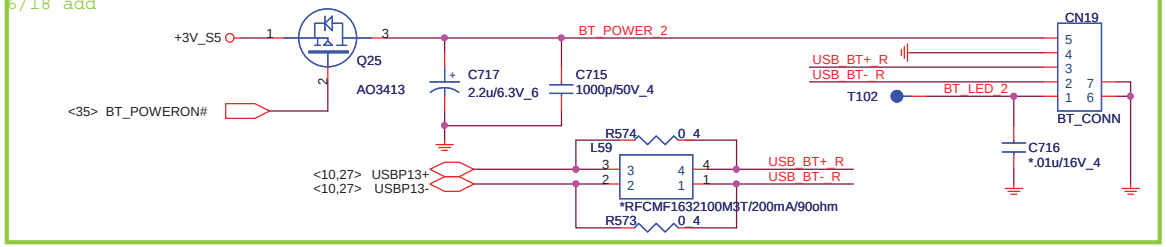
Size	Document Number	Rev
	POWER/MMB/LAUNCH/LED	1A
Date: Tuesday, June 22, 2010	Sheet 32 of 45	

USB

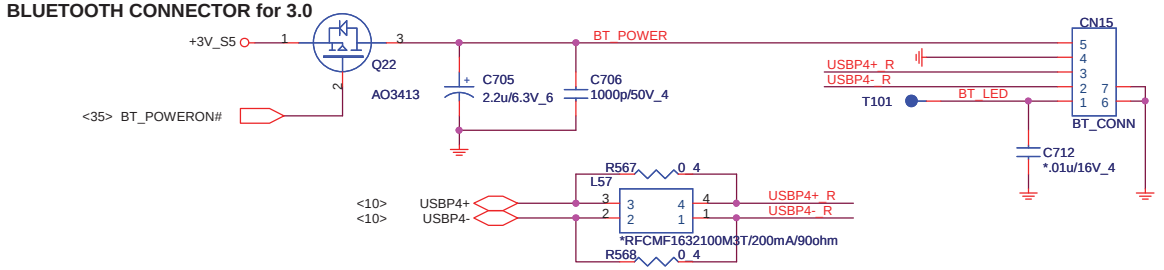


BLUETOOTH CONNECTOR for 2.0

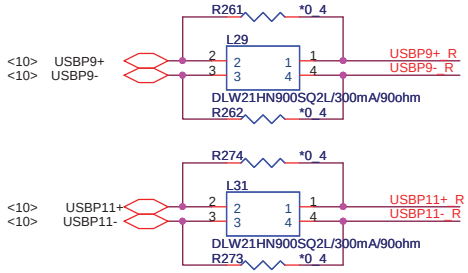
6/18 add

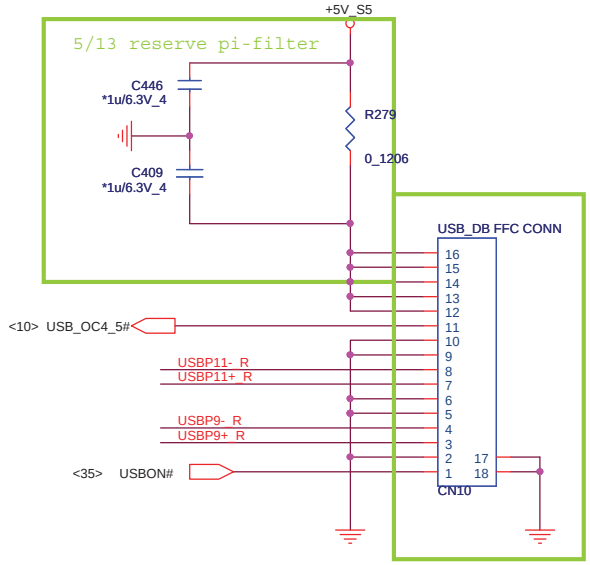


BLUETOOTH CONNECTOR for 3.0



USB/B





5/11 update the footprint

Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	USB/ BT	1A
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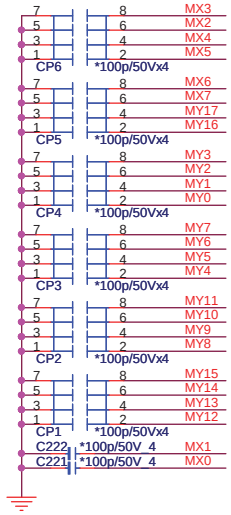
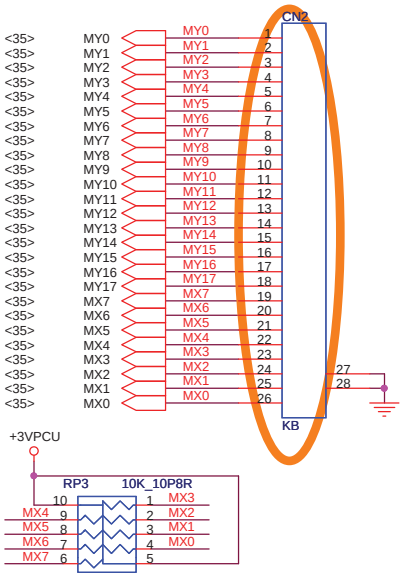
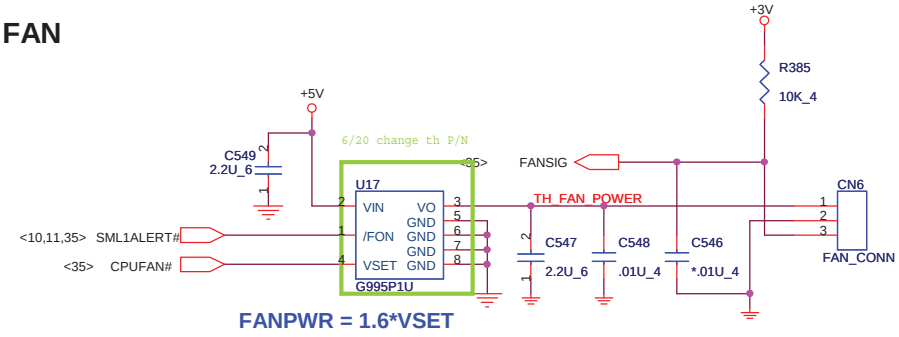
K/B



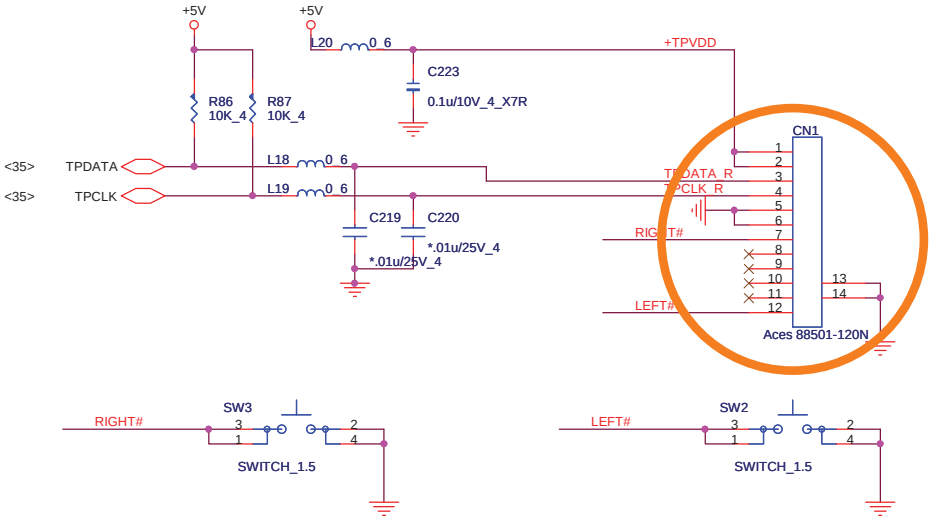


CPU FAN

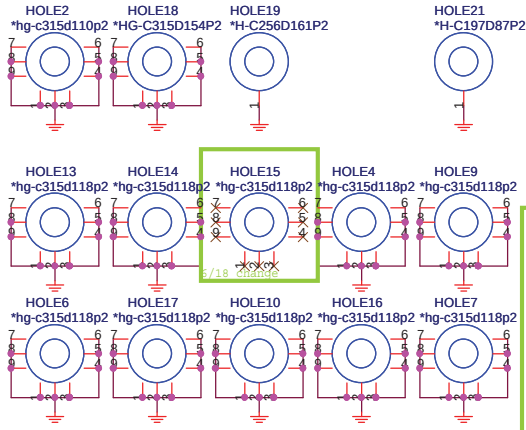


FANPWR = 1.6*VSET

TOUCHPAD & Switch CONN.



HOLE



5/12 add

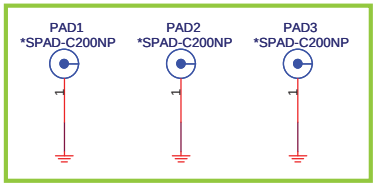
HOLE8 *H-TC256BC165D165P2
HOLE11 *H-TC256BC165D165P2
HOLE12 *H-TC256BC165D165P2
HOLE20 *H-C256D161P2

5/21 add

5/24 add

HOLE1 *HG-C315D118P2

5/27 Delete HOLE4, HOLE22



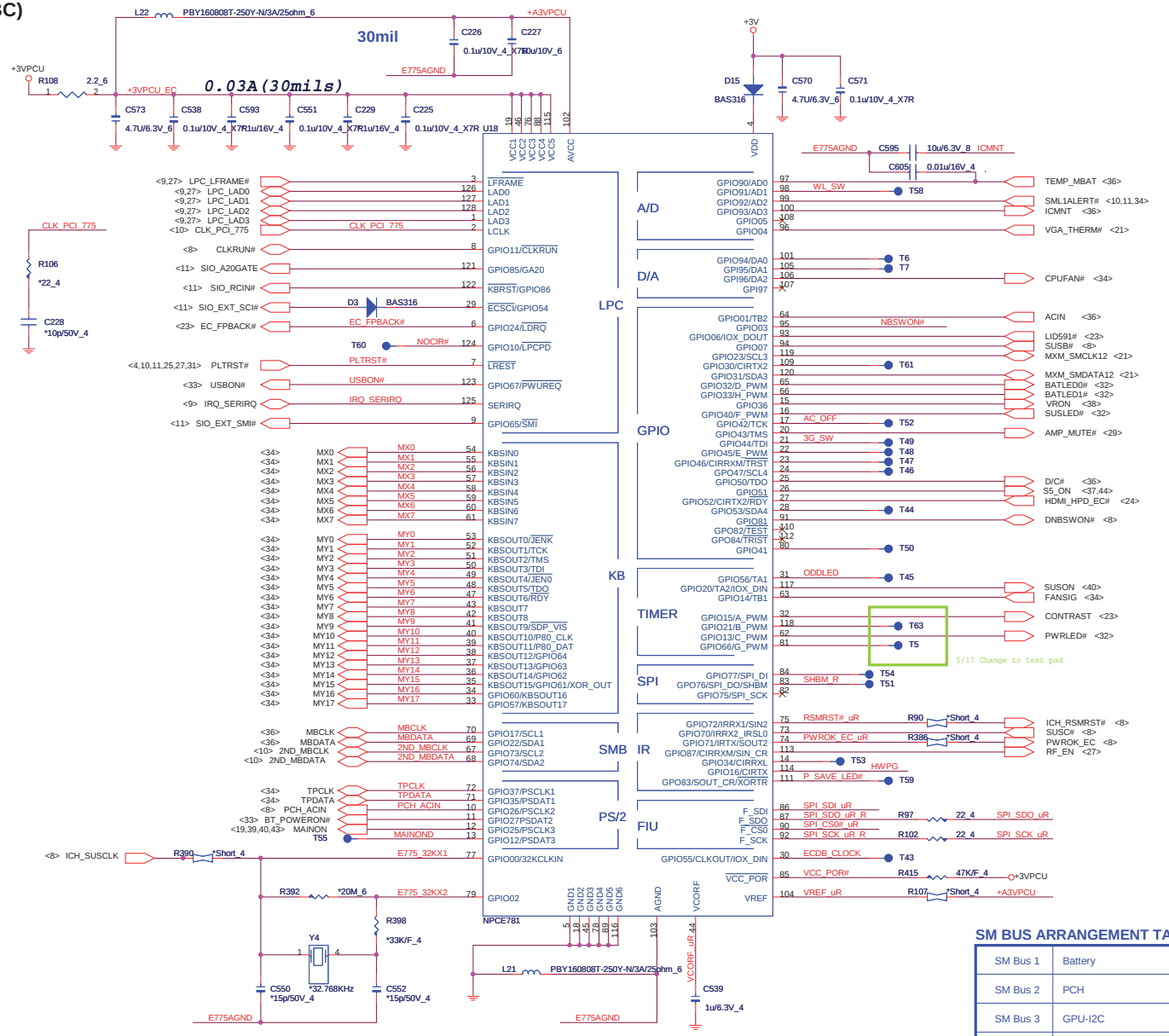
6/21 add

Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date: Tuesday, June 22, 2010	Sheet 34 of 45	

EC(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

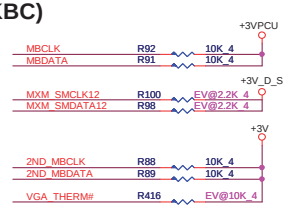
I/O ADDRESS SETTING(KBC)

SHBM=0: Enable shared memory with host BIOS

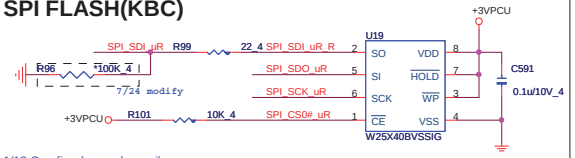
SHBM R405 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

SM BUS PU(KBC)

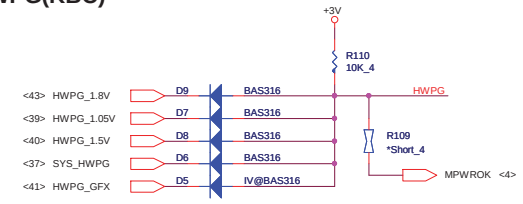


SPI FLASH(KBC)

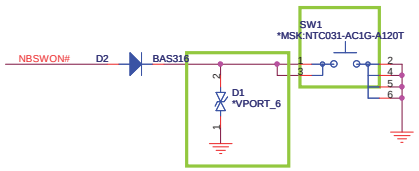


1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by
default, the flash device should be 50MHz (or faster)

HWPG(KBC)



POWER-ON Switch(KBC)



INTERNAL KEYBOARD STRIP SET(KBC)

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	WPCE781 & FLASH	1A

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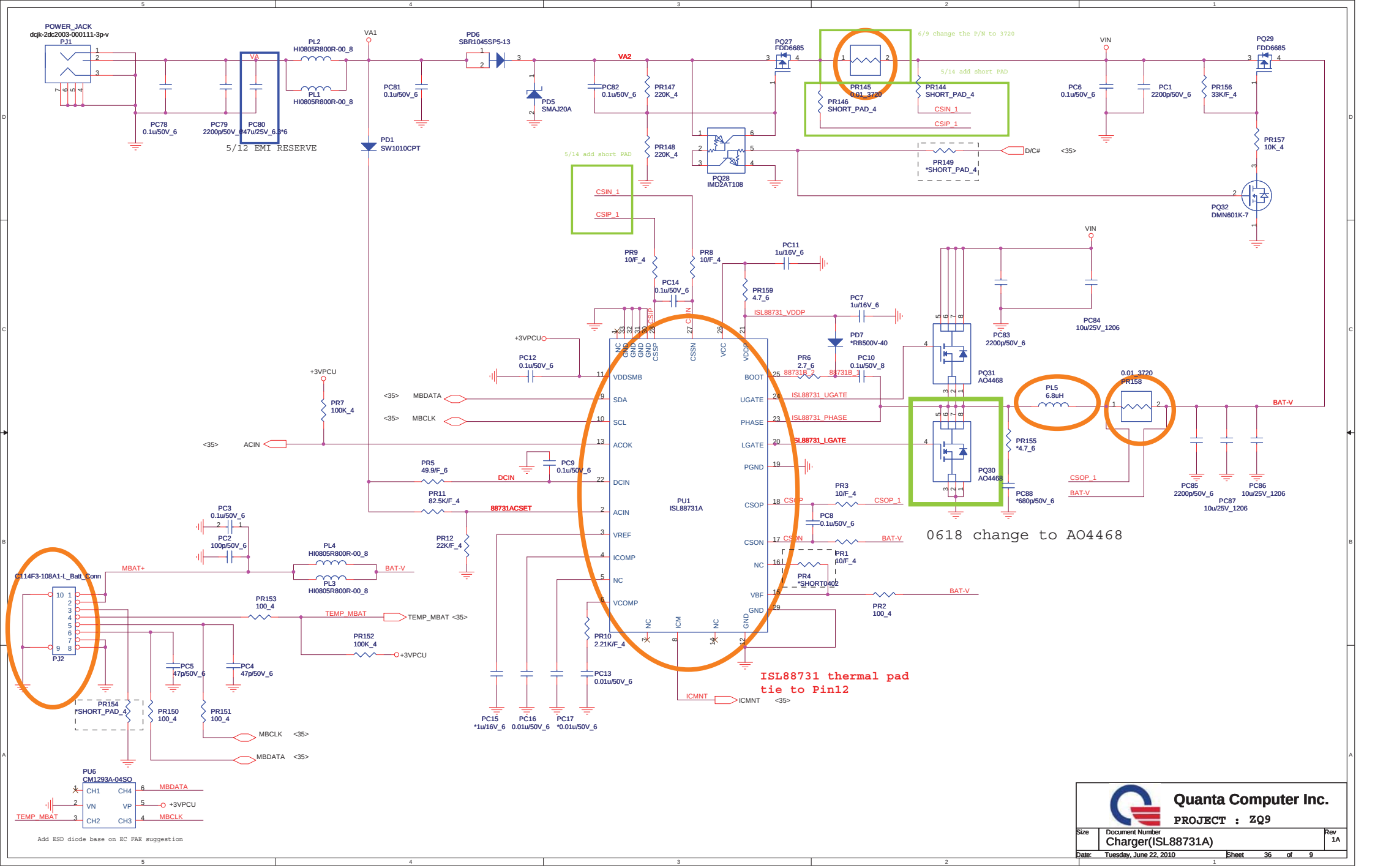
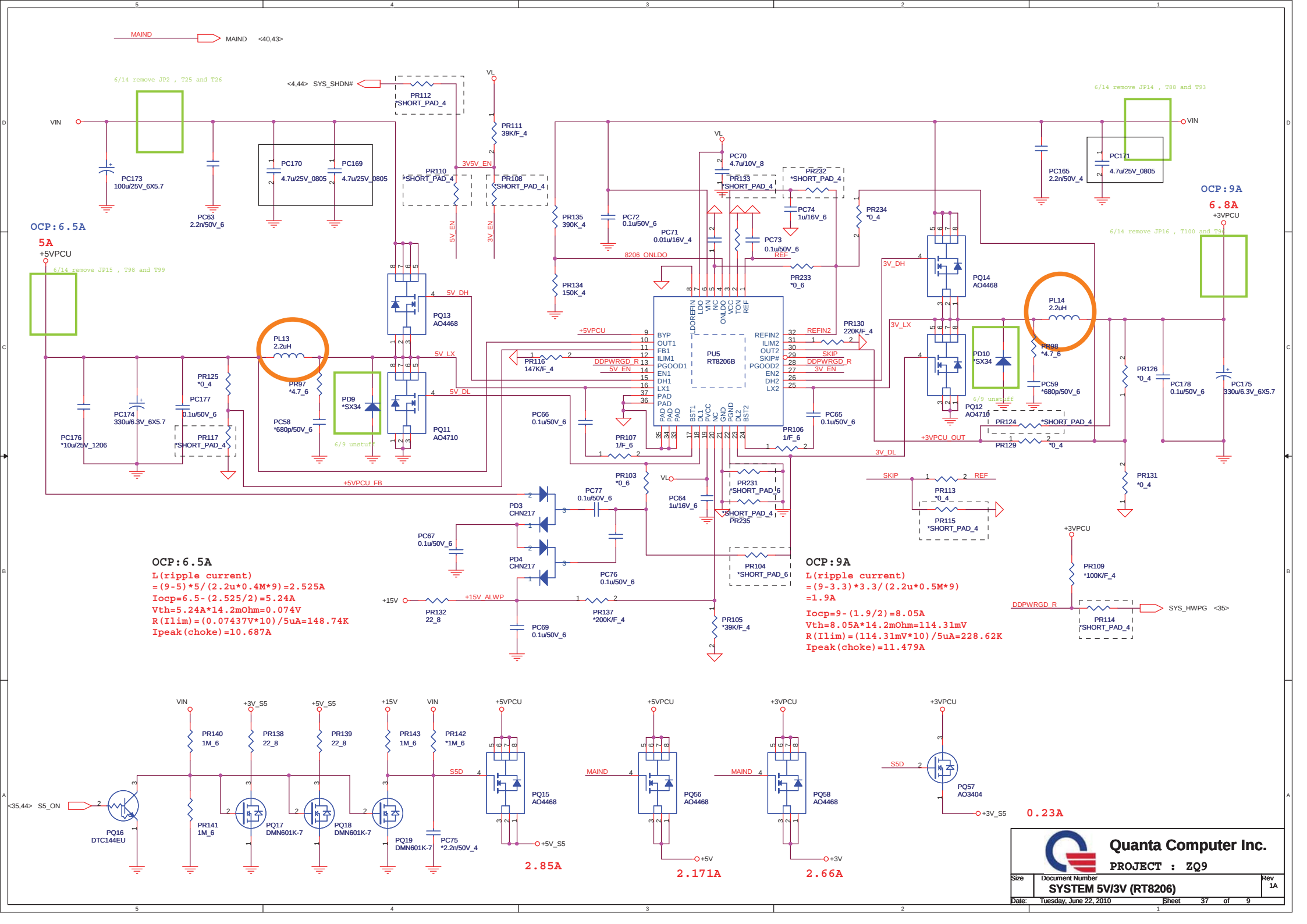
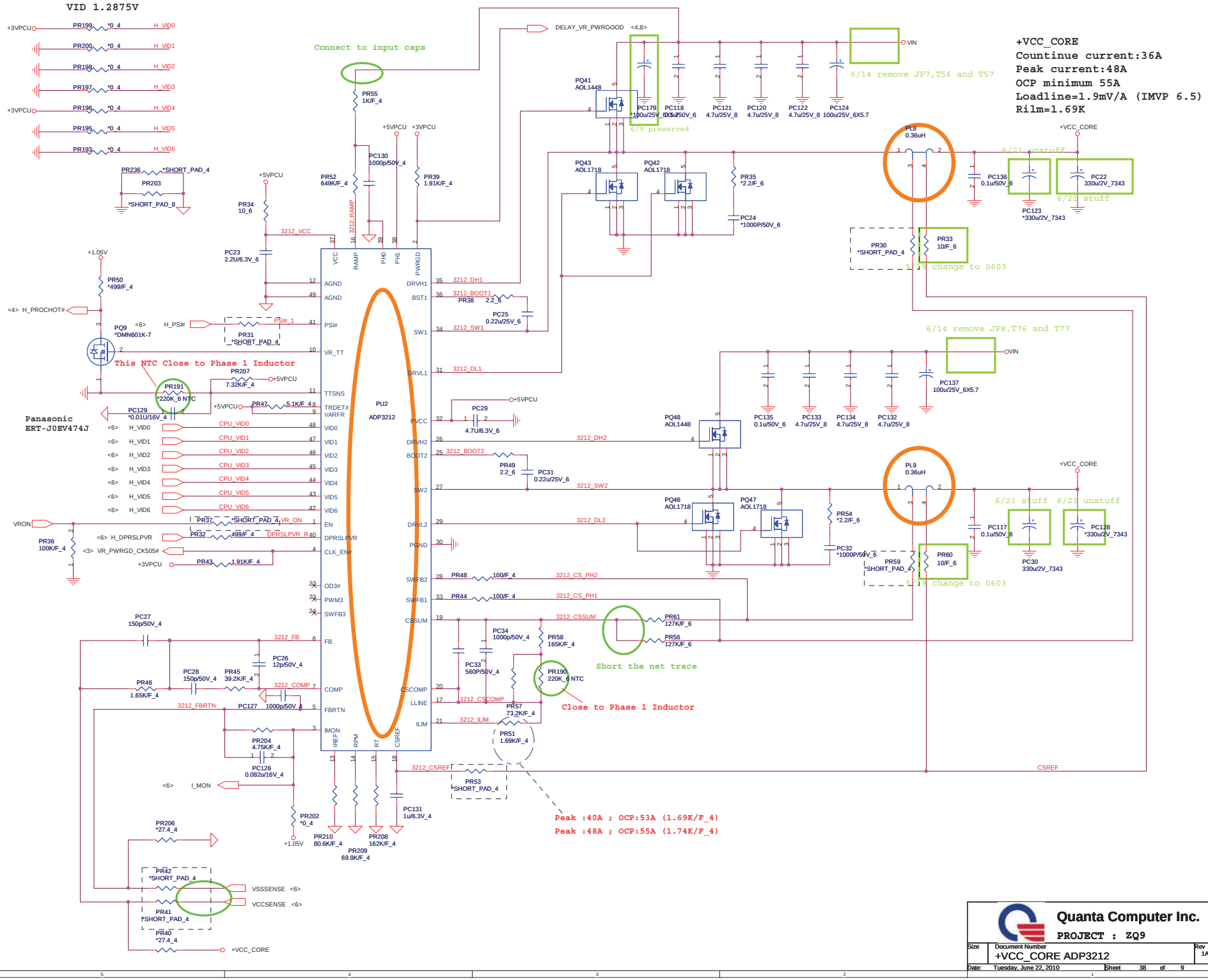
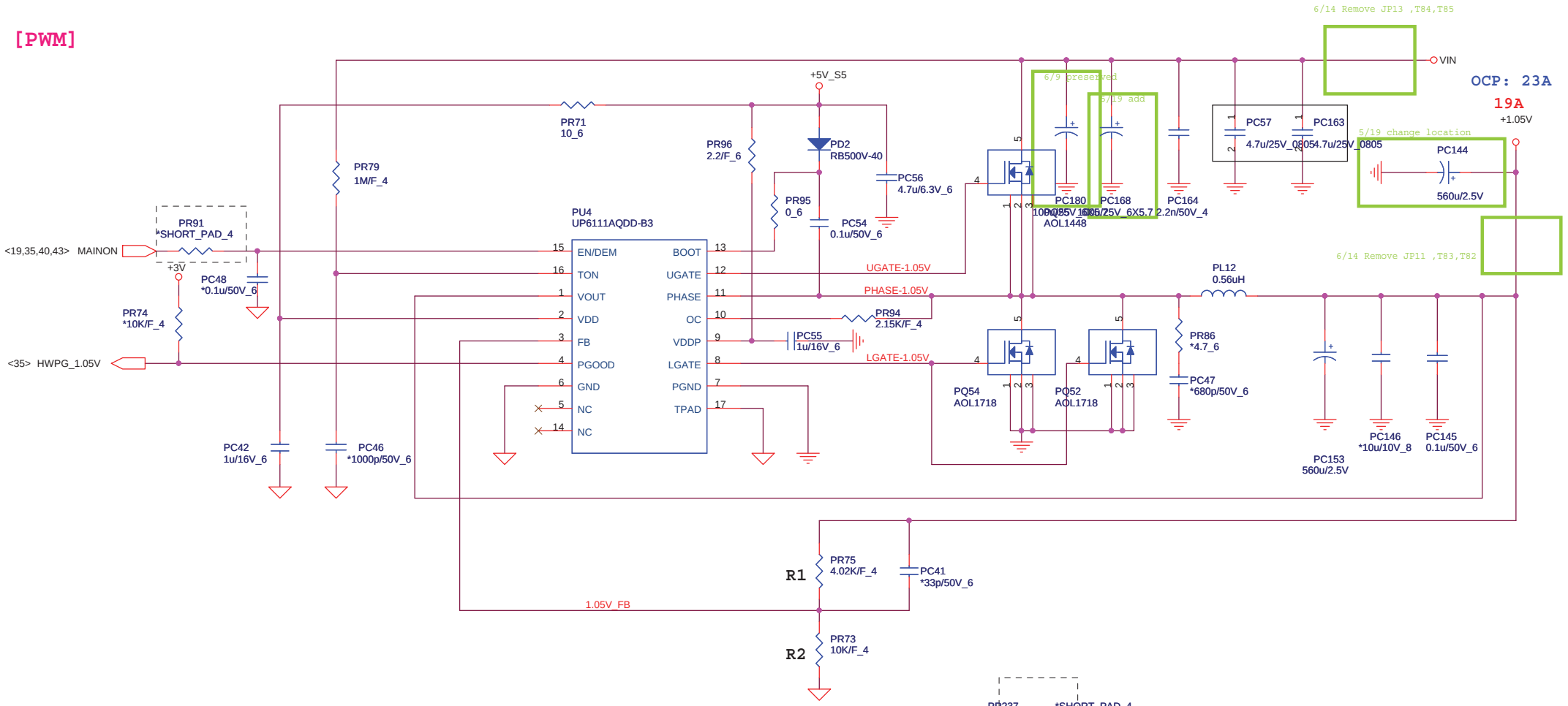


Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number: Charger(ISL88731A)	Rev: 1A
Date: Tuesday, June 22, 2010	Sheet 36 of 9	


MAIND
MAIND <40,43>
6/14 remove JP2 , T25 and T26
<4,44> SYS_SHDN#
PR112 *SHORT_PAD_4
VL
PR111 39K/F_4
VIN
PC173 100u/25V_6X5.7
PC63 2.2n/50V_6
PC170 4.7u/25V_0805
PC169 4.7u/25V_0805
PR110 *SHORT_PAD_4
PR108 *SHORT_PAD_4
3V5V_EN
5V_EN
3V_EN
OCP:6.5A
5A
+5VPCU
6/14 remove JP15 , T98 and T99
PR135 390K_4
PR134 150K_4
PC72 0.1u/50V_6
PC71 0.01u/16V_4
8206_ONLDO
PC70 4.7u/10V_8
PR133 *SHORT_PAD_4
PC73 0.1u/50V_6
PC74 1u/16V_6
PR232 *SHORT_PAD_4
REF
PR233 *0_6
PR234 *0_4
PU5 RT8206B
LDOREFIN LDO VIN NC ONLDO VCC TON REF
BYP OUT1 FB1 ILIM1 PGOOD1 EN1 DH1 LX1 PAD PAD PAD PAD
REFIN2 ILIM2 OUT2 SKIP# PGOOD2 EN2 DH2 LX2
BST1 DL1 PVCC NC GND PGND DL2 BST2
PR130 220K/F_4
REFIN2
SKIP
DDPWRGD_R
3V_EN
PR116 147K/F_4
5V_DH
5V_LX
5V_DL
PQ13 AO4468
PL13 2.2uH
PR97 *4.7_6
PD9 *SX34
PQ11 AO4710
PR125 *0_4
PC174 330u/6.3V_6X5.7
PC177 0.1u/50V_6
PC176 *10u/25V_1206
PR117 *SHORT_PAD_4
PC58 *680p/50V_6
6/9 unstuff
PC66 0.1u/50V_6
PC65 0.1u/50V_6
PR107 1/F_6
PR106 1/F_6
+5VPCU_FB
PR103 *0_6
PC77 0.1u/50V_6
PC64 1u/16V_6
PR231 *SHORT_PAD_6
*SHORT_PAD_4
PR235
PR104 *SHORT_PAD_6
PD3 CHN217
PD4 CHN217
PC67 0.1u/50V_6
PC76 0.1u/50V_6
+15V
+15V_ALWP
PR132 22_8
PR137 *200K/F_4
PC69 0.1u/50V_6
PR105 *39K/F_4
OCP:6.5A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)=2.525A
Iocp=6.5-(2.525/2)=5.24A
Vth=5.24A*14.2mOhm=0.074V
R(Ilim)=(0.07437V*10)/5uA=148.74K
Ipeak(choke)=10.687A
6/14 remove JP14 , T88 and T93
VIN
PC165 2.2n/50V_4
PC171 4.7u/25V_0805
OCP:9A
6.8A
+3VPCU
6/14 remove JP16 , T100 and T94
3V_DH
3V_LX
PQ14 AO4468
PL14 2.2uH
PD10 *SX34
PR98 *4.7_6
PC59 *680p/50V_6
PQ12 AO4710
6/9 unstuff
PR124 *SHORT_PAD_4
PR129 *0_4
+3VPCU_OUT
3V_DL
PR126 *0_4
PC178 0.1u/50V_6
PC175 330u/6.3V_6X5.7
PR131 *0_4
SKIP
REF
PR113 *0_4
PR115 *SHORT_PAD_4
OCP:9A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
=1.9A
Iocp=9-(1.9/2)=8.05A
Vth=8.05A*14.2mOhm=114.31mV
R(Ilim)=(114.31mV*10)/5uA=228.62K
Ipeak(choke)=11.479A
+3VPCU
PR109 *100K/F_4
DDPWRGD_R
PR114 *SHORT_PAD_4
SYS_HWPG <35>
VIN
+3V_S5
+5V_S5
+15V
VIN
+5VPCU
PR140 1M_6
PR138 22_8
PR139 22_8
PR143 1M_6
PR142 *1M_6
S5D
<35,44> S5_ON
PQ16 DTC144EU
PR141 1M_6
PQ17 DMN601K-7
PQ18 DMN601K-7
PQ19 DMN601K-7
PC75 *2.2n/50V_4
PQ15 AO4468
+5V_S5
2.85A
+5VPCU
MAIND
PQ56 AO4468
+5V
2.171A
+3VPCU
MAIND
PQ58 AO4468
+3V
2.66A
+3VPCU
S5D
PQ57 AO3404
+3V_S5
0.23A
Quanta Computer Inc.
PROJECT : ZQ9
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Tuesday, June 22, 2010
Sheet 37 of 9


VID 1.2875V
+VCC_CORE
Countinue current:36A
Peak current:48A
OCP minimum 55A
Loadline=1.9mV/A (IMVP 6.5)
Rilm=1.69K
Connect to input caps
6/14 remove JP7,T56 and T57
6/9 preserved
6/14 remove JP8,T76 and T77
6/21 unstuff
6/21 stuff
5/19 change to 0603
This NTC Close to Phase 1 Inductor
Panasonic
ERT-J0EV474J
Short the net trace
Close to Phase 1 Inductor
Peak :40A ; OCP:53A (1.69K/F_4)
Peak :48A ; OCP:55A (1.74K/F_4)
PU2
ADP3212
Quanta Computer Inc.
PROJECT : ZQ9
+VCC_CORE ADP3212
Tuesday, June 22, 2010
Sheet 38 of 9



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AO1718 Rdson=3~4.3mOhm

L(ripple current)
=(19-1.05)*1.05/(0.56u*272k*19)
~6.512A

RILIM=2.15mohm*23-3.256/20uA=2.122Kohm

I(choke)peak=29.512A

Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	+VTT (UP6111A)	1A

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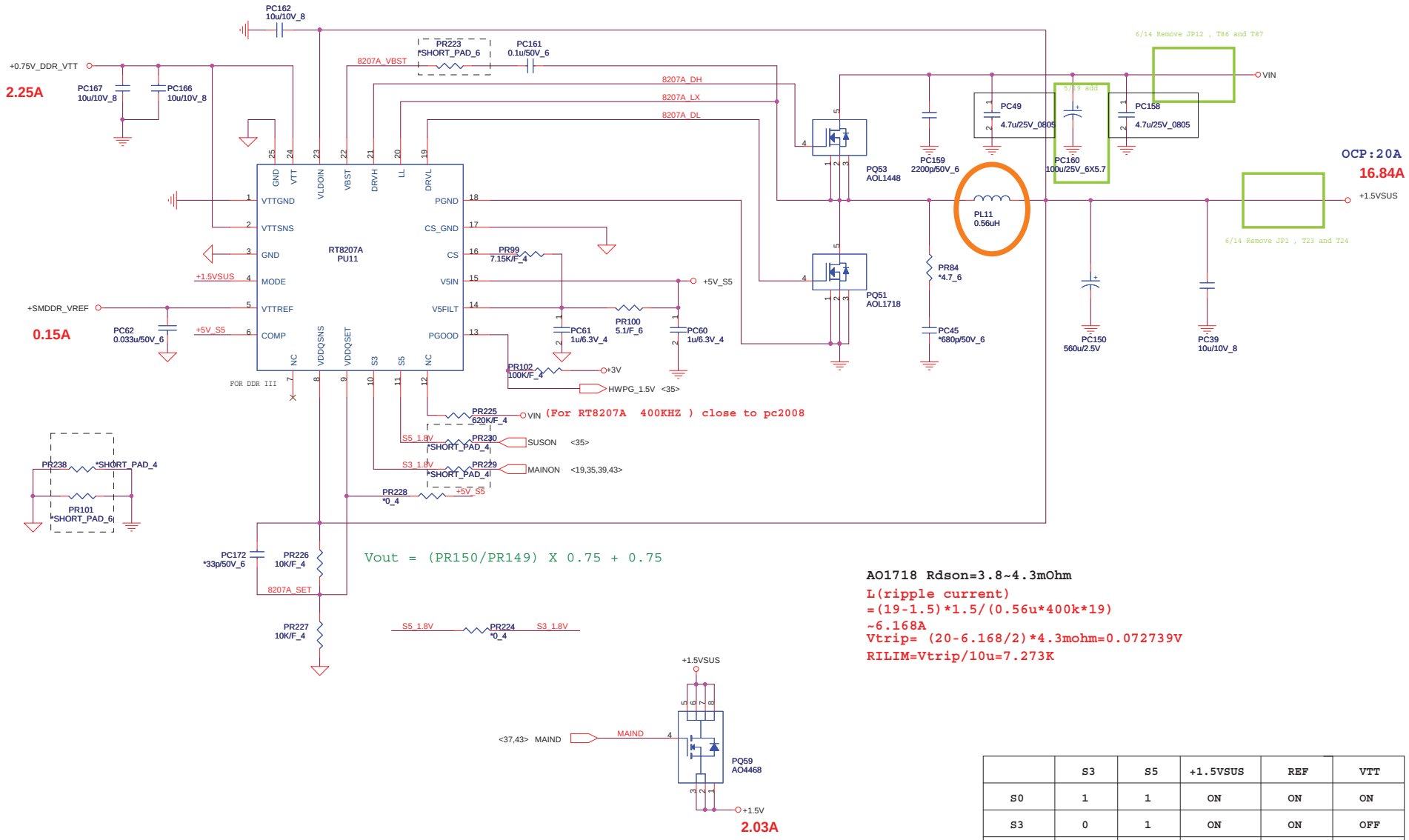
[PWM]



AO1718 Rdson=3.8~4.3mOhm

L(ripple current)
=(19-1.5)*1.5/(0.56u*400k*19)
~6.168A
Vtrip= (20-6.168/2)*4.3mohm=0.072739V
RILIM=Vtrip/10u=7.273K

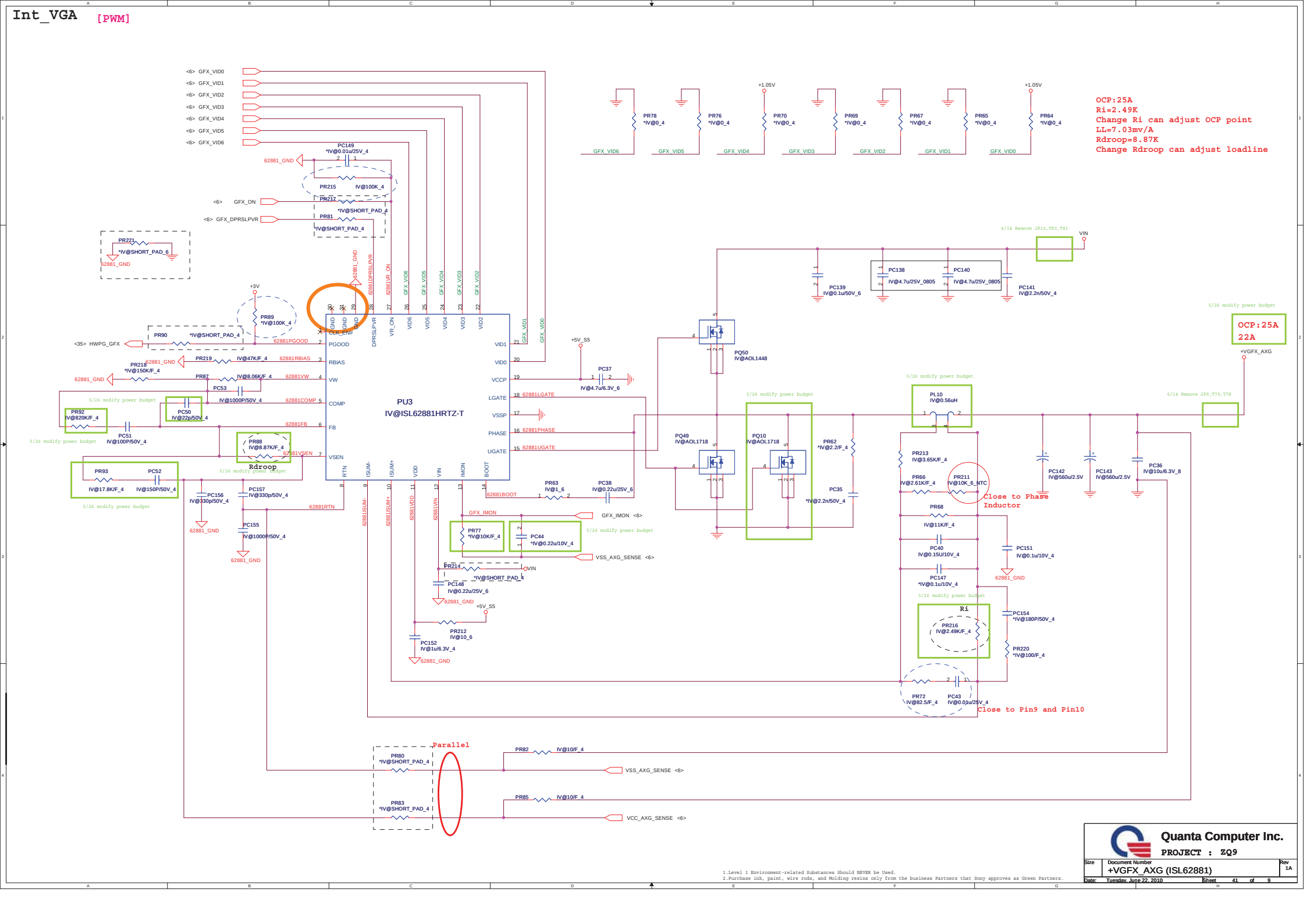
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	DDR 1.5V(RT8207A)	1A

Date: Tuesday, June 22, 2010 Sheet 40 of 9

Int_VGA [PWM]

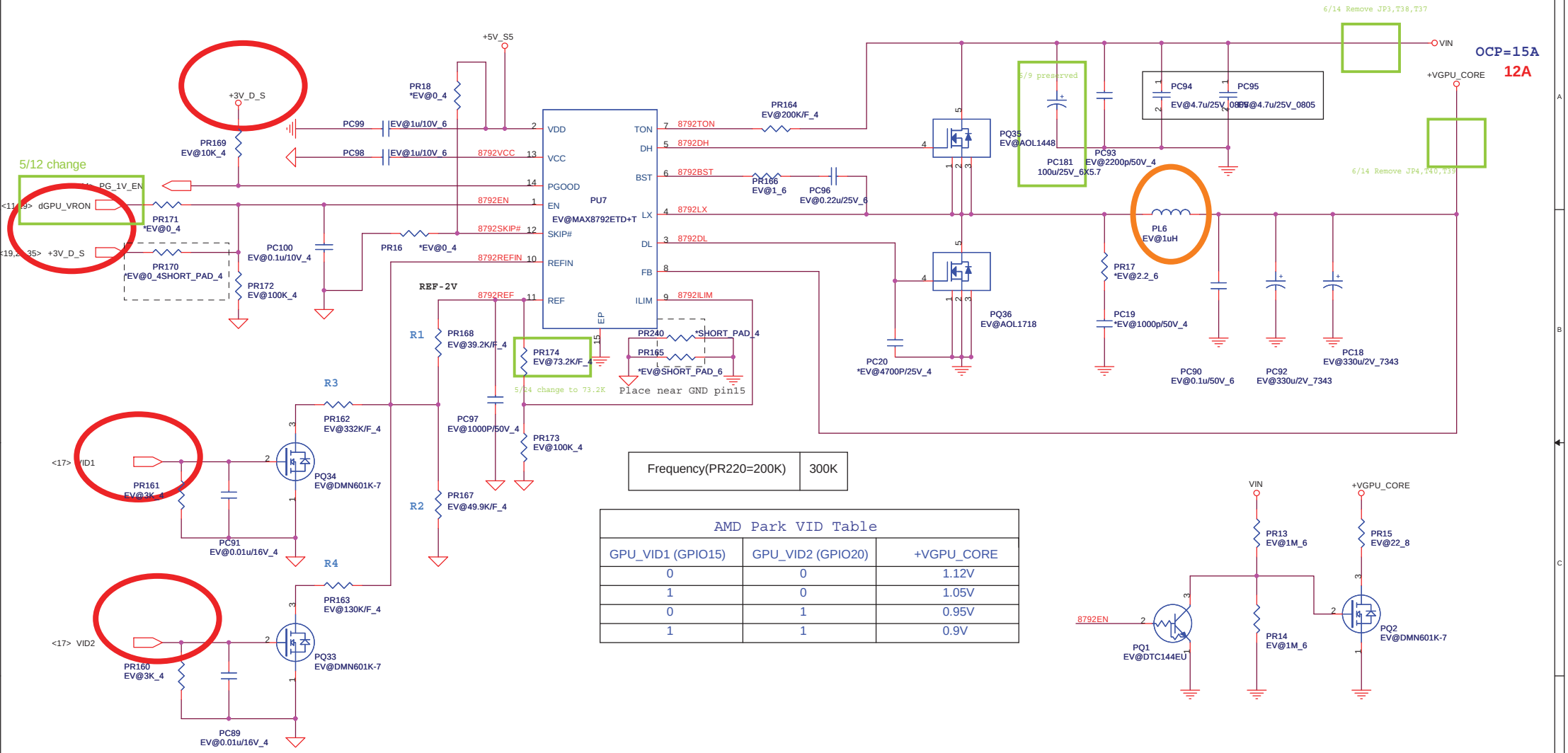


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Quanta Computer Inc.
PROJECT : ZQ9

Size	Document Number	Rev
	+VGFX_AXG (ISL62881)	1A

Date: Tuesday, June 22, 2010 Sheet 41 of 9



Frequency(PR220=200K)	300K

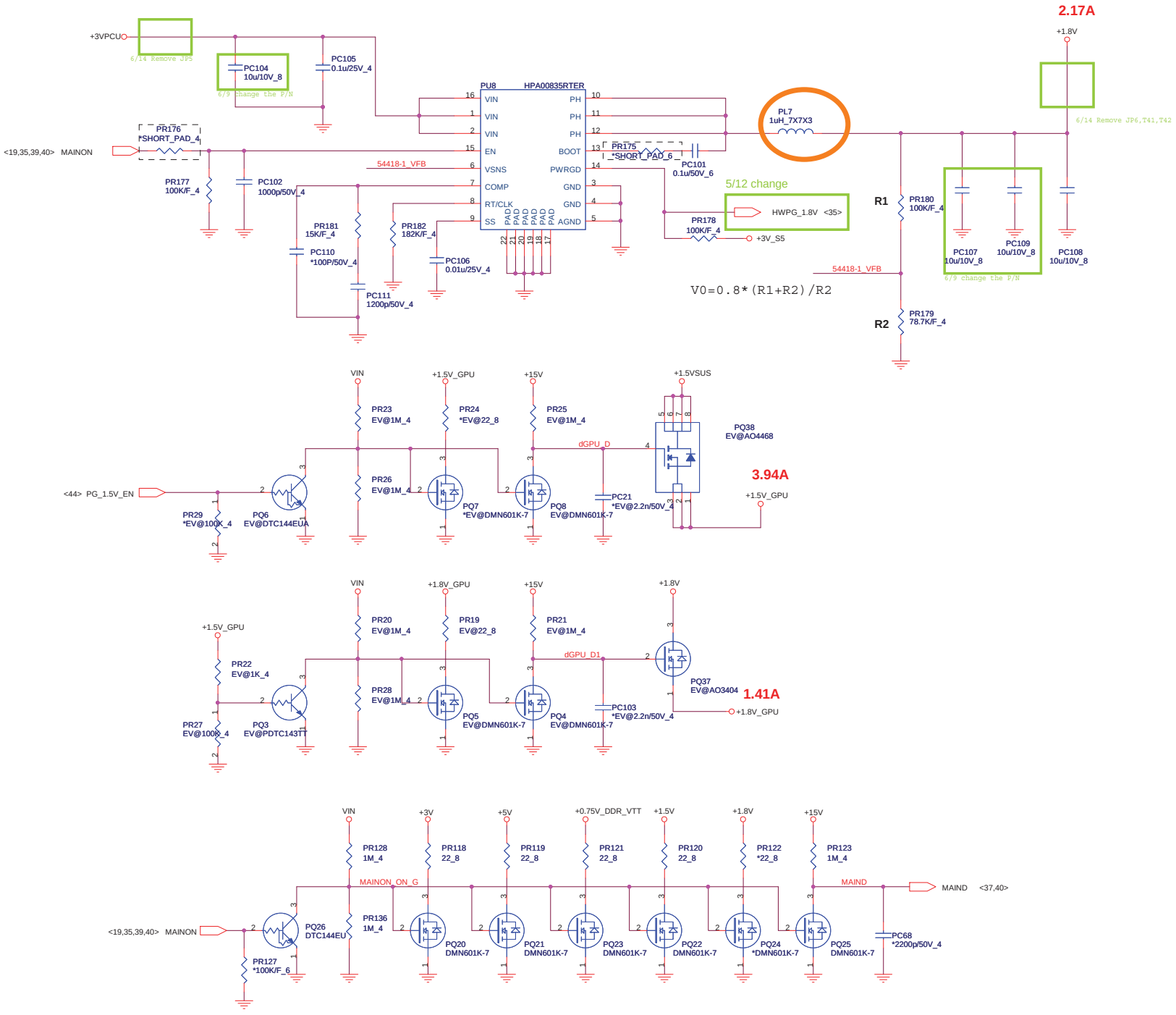
AMD Park VID Table

GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	1.05V
0	1	0.95V
1	1	0.9V

Quanta Computer Inc.

PROJECT : ZQ9

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
Date: Tuesday, June 22, 2010	Sheet 42 of 9	



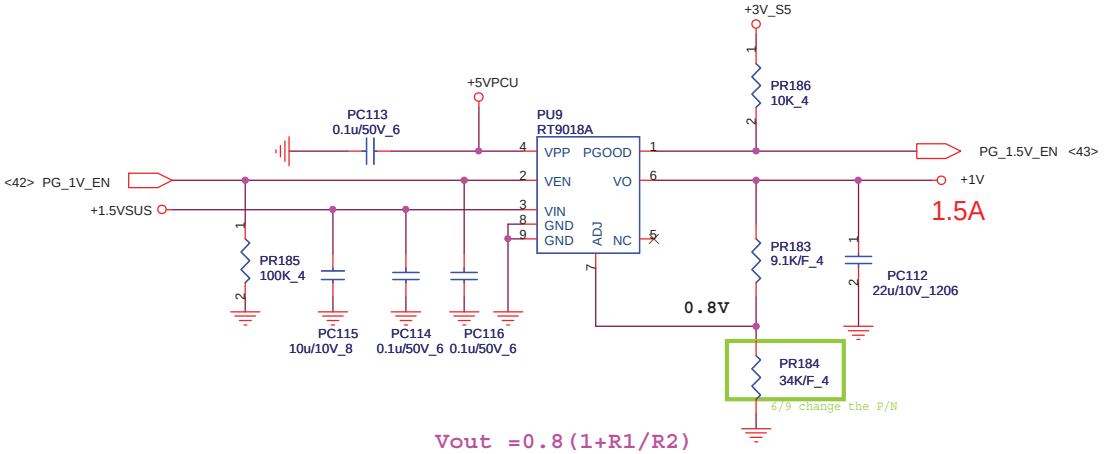
7/7 modify

Quanta Computer Inc.

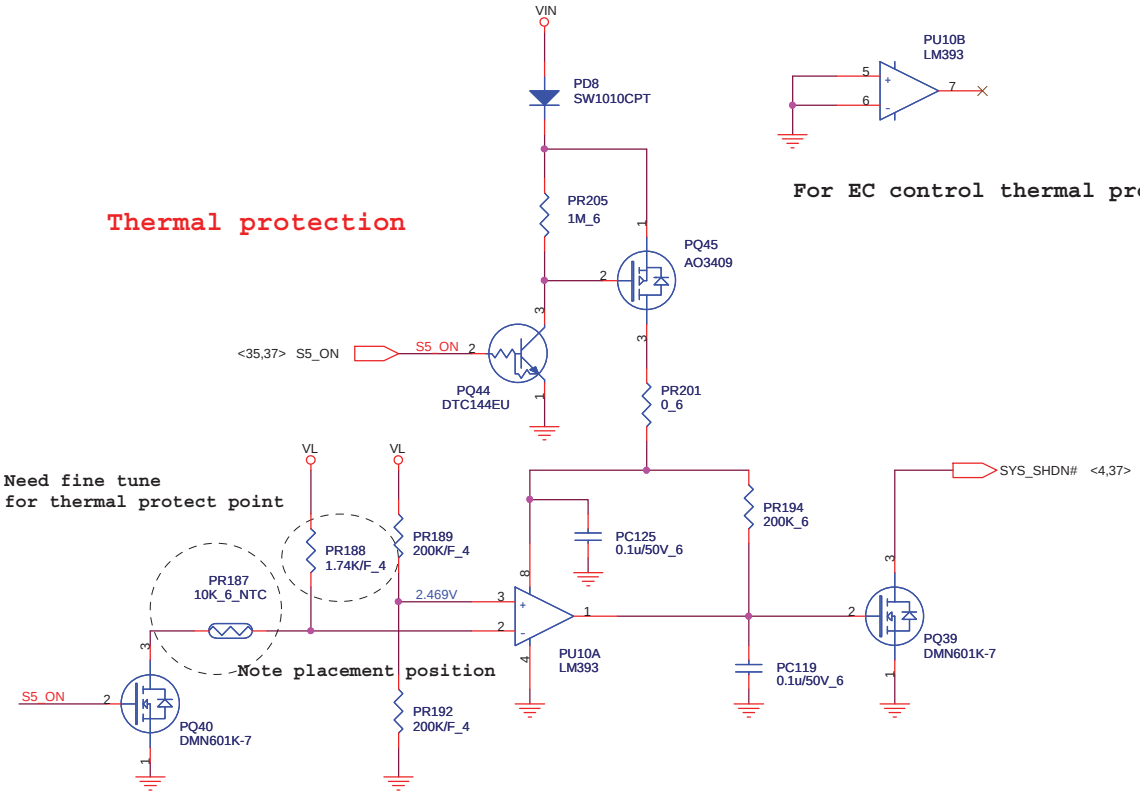
PROJECT : ZQ9

Size	Document Number	Rev
	Discharge/1.8V)	1A

Date: Tuesday, June 22, 2010 Sheet 43 of 9



Vout =0.8(1+R1/R2)
=1V



Thermal protection

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.		
PROJECT : ZQ9		
Size	Document Number	Rev 1A
Date: Tuesday, June 22, 2010	Sheet 44 of 9	

CHANGE LIST

Model	REV	CHANGE LIST
ZQ9	1A	
	2A	
Power parts		
	4A	

MODEL: ZQ9

FROM	To	

Quanta Computer Inc.

PROJECT: ZQ9

Change list

BBE NO.	PROJECT MODEL:	ZQ9	APPROVED BY:	DATE:	2009/12/24
	PART NUMBER:		DRAWING BY:	REVISON:	C1A