ZQ2B SOLE UMA SYSTEM DIAGRAM

VER : 1A

BOM P/N	Description	Model	SidePort	ODD
31ZQ2MB00A0	ZQ2B 6L JM MB (W/GRN,SAM,W/O CPU)ASSY	JM	Sansung	Slim
31ZQ2MB00E0	ZQ2B 6L JM MB (W/GRN,HYU,W/O CPU)ASSY	JM	Hynix	Slim
31ZQ2MB00H0	ZQ2B 6L JV MB (W/GRN,W/O CPU,VRAM)ASSY	JV	No Support	Standard

AMD Smarter Choice
Danube Platform
(Main Stream)

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

IV@ -----> iGPU
SP@ -----> Option Notice
SIDE@ -----> SidePort VRAM
GA@ ----> Green Adapter (Default stuff)

Sideport-L75,L76,R583,R392,C832,R455,R550,R502
NB A11-R105,R108
SB A12-R267,R271
JV/JM-CN16,R450,R456
EC-D8,D27
UMA-R461
VRAM-R358,R359,R360,R363,R365,R72

CPU
- CHARGER (ISL88731A) PAGE 26
- AMD CPU CORE (ISL6265) PAGE 28

NB
- NB_CORE (UP6111AQDD) PAGE 30
- 0.9V/DDR 1.5V(RT8207) PAGE 31
- SYSTEM 5V/3V (RT8206) PAGE 27
- 1.1V(UP6111AQDD) PAGE 29
- Discharge /Thermal protec PAGE 32

DDR3- SODIMM1 PAGE 5 — DDR3 channel A
DDR3- SODIMM2 PAGE 5 — DDR3 channel B

AMD Champlain
S1G4 Processor
35mm X 35mm
638P (PGA) 35W
PAGE 2,3,4

CPU THERMAL SENSOR (Reserve Only) PAGE 4
PWM FAN SCH. PAGE 24 — CPU (PROCHOT), E.C. (CPUFAN#)

CPU SideBand TemperatureSense I2C

HT3
1.8GHz

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

From SB CLK GEN
SB820M
PAGE 10
CLK_PCI_775
PCLK_DEBUG
25MHz
32.768KHz

PCI-Expresss
P0
P2

NORTH BRIDGE
RS880M GFX Engine: 500MHz
A11
21mm X 21mm, 528pin BGA
TDP: 13W
0.95 ~ 1.1V
PAGE 6,7,8,9

Side Port — gDDR3 VRAM DDR III-800MHz PAGE 6
HDMI — HDMI PAGE 16
CRT — CRT PAGE 15
LVDS — LVDS PAGE 23

LAN
Atheros
PCIE-LAN
AR8151
(10/100/1000)
PAGE 17
25MHz
RJ45 PAGE 17

Mini PCI-E Card
(Wireless LAN)
PAGE 18

A-LINK

SOUTH BRIDGE
SB820M
A12
23mm X 23mm, 605pin BGA
TDP: 4.9W
PAGE 10,11,12,13, 14
No PCI I/F

SATA - HDD PAGE 19 — SATA0 150MB 3 Gb/s
SATA - ODD PAGE 19 — SATA1 150MB 3 Gb/s

P0 — USB2.0 Port on board x1 PAGE 30
P9 — Blue Tooth PAGE 22
P13 — Web-Camera PAGE 15
P4 — Mini Card WLAN & Debug PAGE 18
P10 — CardReader AU6347 PAGE 21
12MHz
PCLK_DEBUG

P8, 11, 12
- USB BOARD — USB2.0 Ports x3 PAGE 22
- Power BOARD PAGE 22
- Switch BOARD PAGE 22

There are three Daughter boards.

LPC
Azalia

CLK_PCI_775
Winbond KBC
NPCE781L &
Green Adapter
PAGE 25
CPU SideBand TemperatureSense I2C

Audio CODEC
RTL ALC271X
PAGE 20

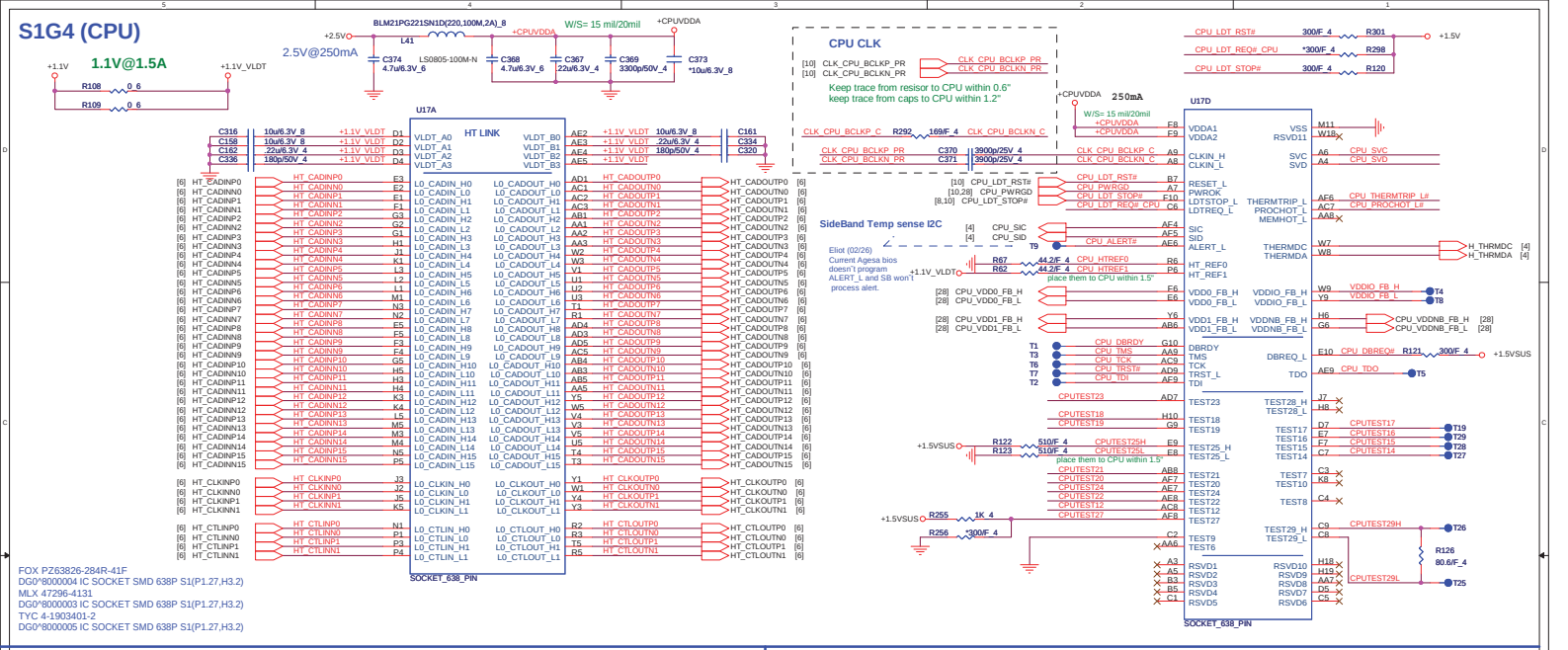
- Green ADP. PAGE 25
- Keyboard TouchPad PAGE 24
- SPI ROM PAGE 25
- Digital MIC PAGE 15 & 20
- AUDIO CONN (H.P./ MIC) PAGE 20
- Speaker CN PAGE 20

SSID: 035E
SVID: 1025

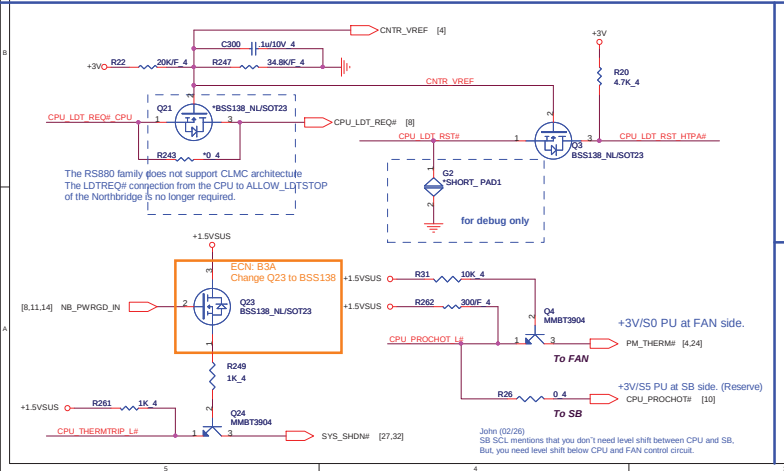
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Thursday, March 04, 2010	Sheet 1 of 36	

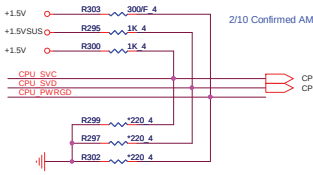
S1G4 (CPU)



FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)



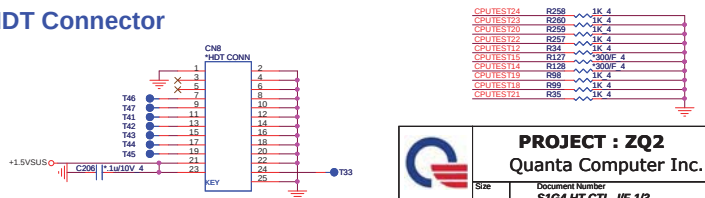
Serial VID



VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

HDT Connector



PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A
Date: Thursday, March 04, 2010	Sheet 2 of 36	

35W CPU support 0.9V
45W CPU support 1.05V

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

VDDR=>1.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

Processor Memory Interface

U17B

MEM:CMD/CTRL/CLK

U17C

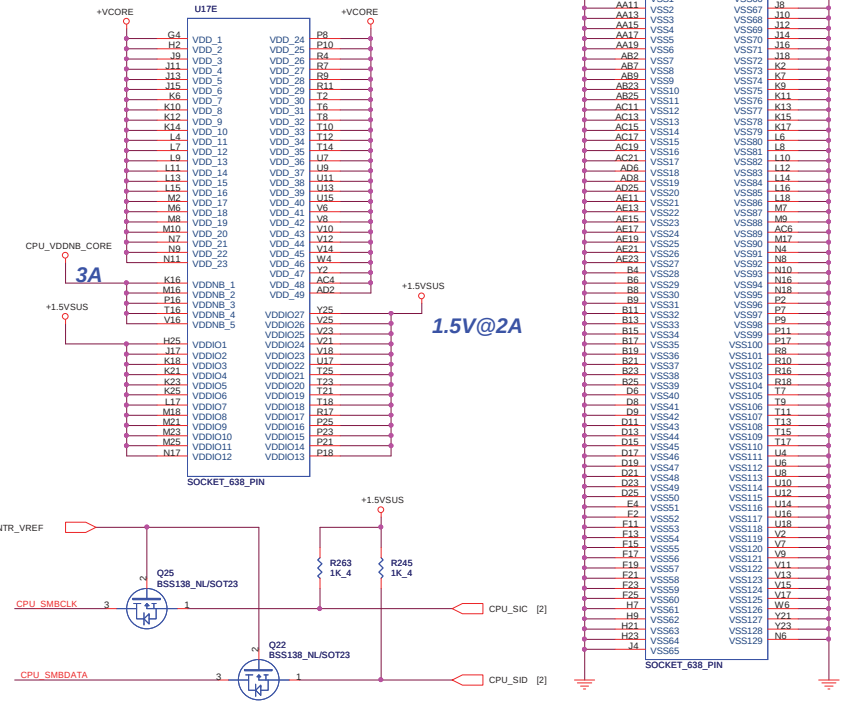
MEM:DATA

SOCKET_638_PIN

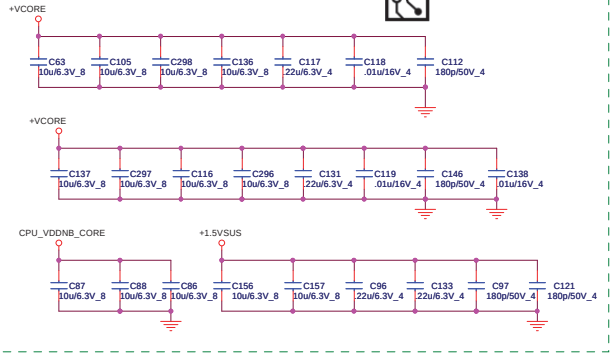
Place close to socket

Reserved for AMD suggest

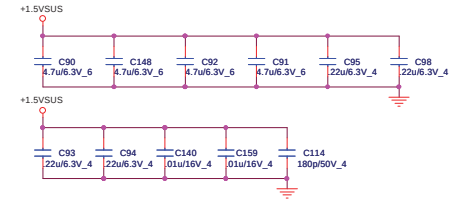
PROJECT :	ZQ2
Quanta Computer Inc.	
Size	Document Number: S1G4 DDRIII MEMORY I/F 2/3 — Rev: 1A
Date: Thursday, March 04, 2010	Sheet 3 of 36



BOTTOM SIDE DECOUPLING

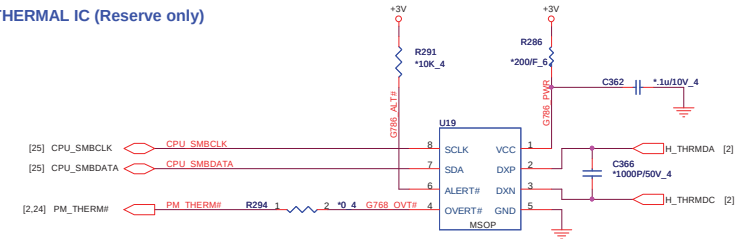


DECOUPLING BETWEEN PROCESSOR AND DIMMs
PLACE CLOSE TO PROCESSOR AS POSSIBLE



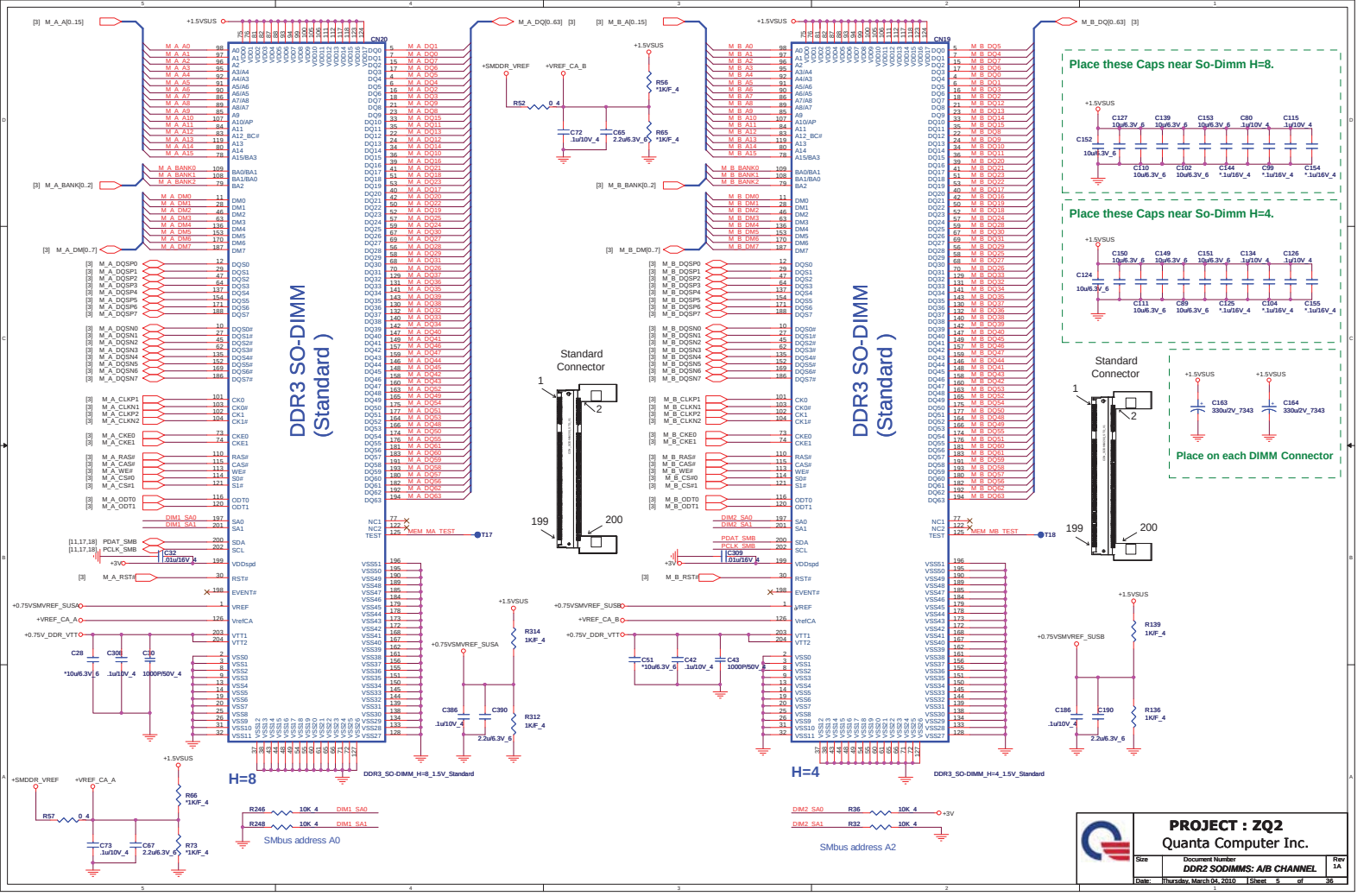
PROCESSOR POWER AND GROUND

THERMAL IC (Reserve only)



Adress ID: 9A

PROJECT : ZQ2			
Quanta Computer Inc.			
Size	Document Number		Rev
	S1G4 PWR & GND 3/3		1A
Date:	Thursday, March 04, 2010	Sheet 4 of	36


DDR3 SO-DIMM (Standard)
CN20
CN19
M_A_A0
M_A_A1
M_A_A2
M_A_A3
M_A_A4
M_A_A5
M_A_A6
M_A_A7
M_A_A8
M_A_A9
M_A_A10
M_A_A11
M_A_A12
M_A_A13
M_A_A14
M_A_A15
M_A_BANK0
M_A_BANK1
M_A_BANK2
M_A_DM0
M_A_DM1
M_A_DM2
M_A_DM3
M_A_DM4
M_A_DM5
M_A_DM6
M_A_DM7
M_A_DQSP0
M_A_DQSP1
M_A_DQSP2
M_A_DQSP3
M_A_DQSP4
M_A_DQSP5
M_A_DQSP6
M_A_DQSP7
M_A_DQSN0
M_A_DQSN1
M_A_DQSN2
M_A_DQSN3
M_A_DQSN4
M_A_DQSN5
M_A_DQSN6
M_A_DQSN7
M_A_CLKP1
M_A_CLKN1
M_A_CLKP2
M_A_CLKN2
M_A_CKE0
M_A_CKE1
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_CS#0
M_A_CS#1
M_A_ODT0
M_A_ODT1
M_A_RST#
M_A_DQ[0..63]
M_A_A[0..15]
M_A_BANK[0..2]
M_A_DM[0..7]
M_A_DQ0
M_A_DQ1
M_A_DQ2
M_A_DQ3
M_A_DQ4
M_A_DQ5
M_A_DQ6
M_A_DQ7
M_A_DQ8
M_A_DQ9
M_A_DQ10
M_A_DQ11
M_A_DQ12
M_A_DQ13
M_A_DQ14
M_A_DQ15
M_A_DQ16
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M_A_DQ30
M_A_DQ31
M_A_DQ32
M_A_DQ33
M_A_DQ34
M_A_DQ35
M_A_DQ36
M_A_DQ37
M_A_DQ38
M_A_DQ39
M_A_DQ40
M_A_DQ41
M_A_DQ42
M_A_DQ43
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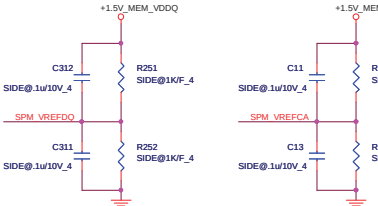
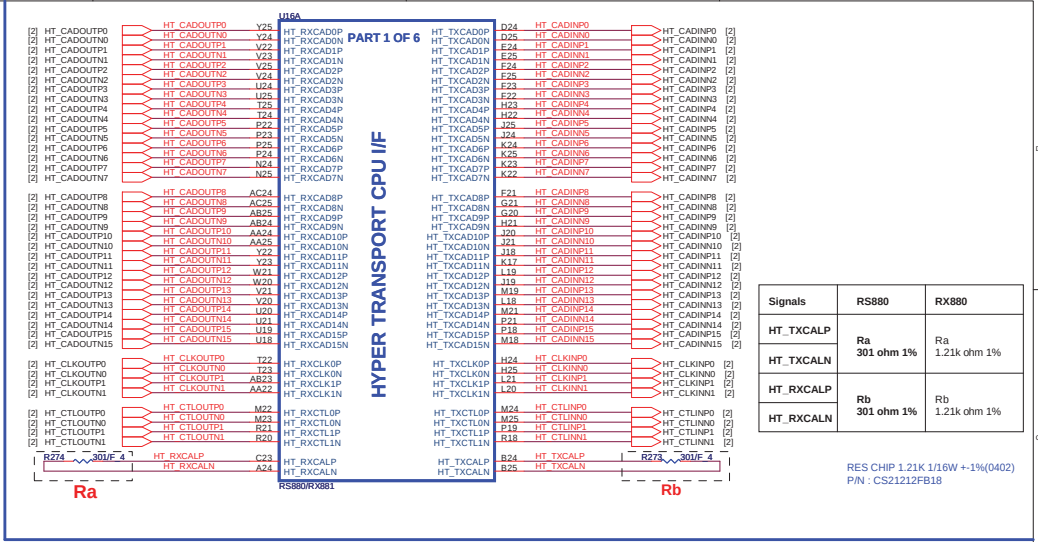
M_A_DQ45
M_A_DQ46
M_A_DQ47
M_A_DQ48
M_A_DQ49
M_A_DQ50
M_A_DQ51
M_A_DQ52
M_A_DQ53
M_A_DQ54
M_A_DQ55
M_A_DQ56
M_A_DQ57
M_A_DQ58
M_A_DQ59
M_A_DQ60
M_A_DQ61
M_A_DQ62
M_A_DQ63
+1.5VSUS
+3V
+SMDDR_VREF
+VREF_CA_B
+0.75VSMVREF_SUS
+VREF_CA_A
+0.75V_DDR_VTT
+0.75VSMVREF_SUSA
R52 0_4
R56 *1K/F_4
R65 *1K/F_4
C72 .1u/10V_4
C65 2.2u/6.3V_6
C32 .01u/16V_4
C28 *10u/6.3V_6
C30 .1u/10V_4
C31 1000P/50V_4
C386 .1u/10V_4
C390 2.2u/6.3V_6
R314 1K/F_4
R312 1K/F_4
C51 *10u/6.3V_6
C42 .1u/10V_4
C43 1000P/50V_4
C309 .01u/16V_4
R57 0_4
R66 *1K/F_4
R73 *1K/F_4
C73 .1u/10V_4
C67 2.2u/6.3V_6
R246 10K_4
R248 10K_4
DIM1_SA0
DIM1_SA1
SMbus address A0
DIM2_SA0
DIM2_SA1
R36 10K_4
R32 10K_4
SMbus address A2
Standard Connector
MEM_MA_TEST
MEM_MB_TEST
T17
T18
H=8
H=4
DDR3_SO-DIMM_H=8_1.5V_Standard
DDR3_SO-DIMM_H=4_1.5V_Standard
Place these Caps near So-Dimm H=8.
C127 10u/6.3V_6
C139 10u/6.3V_6
C153 10u/6.3V_6
C80 .1u/10V_4
C115 .1u/10V_4
C152 10u/6.3V_6
C110 10u/6.3V_6
C102 10u/6.3V_6
C144 *.1u/16V_4
C99 *.1u/16V_4
C154 *.1u/16V_4
Place these Caps near So-Dimm H=4.
C150 10u/6.3V_6
C149 10u/6.3V_6
C151 10u/6.3V_6
C134 .1u/10V_4
C126 .1u/10V_4
C124 10u/6.3V_6
C111 10u/6.3V_6
C89 10u/6.3V_6
C125 *.1u/16V_4
C104 *.1u/16V_4
C155 *.1u/16V_4
Place on each DIMM Connector
C163 330u/2V_7343
C164 330u/2V_7343
R139 1K/F_4
R136 1K/F_4
C186 .1u/10V_4
C190 2.2u/6.3V_6
PROJECT : ZQ2
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Size
Document Number
Rev 1A
Date: Thursday, March 04, 2010
Sheet 5 of 36

SIDE PORT

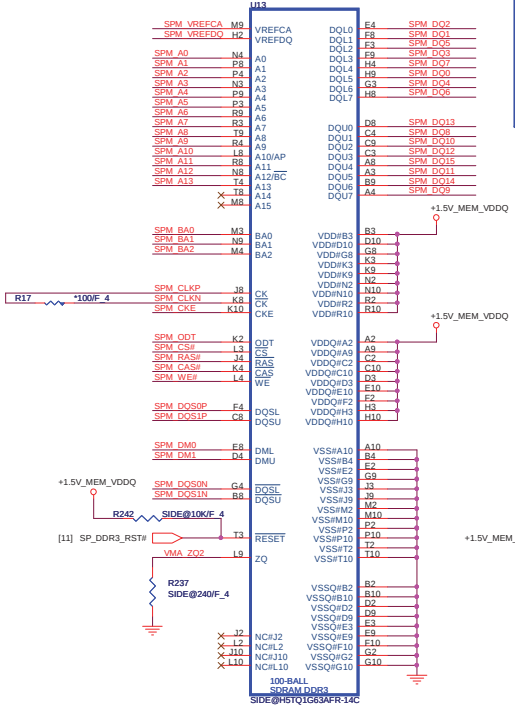


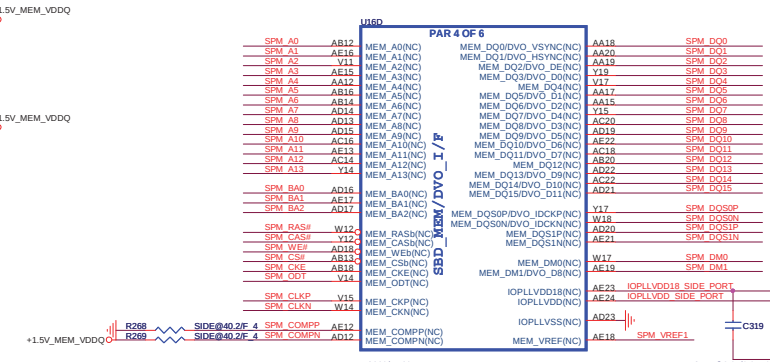


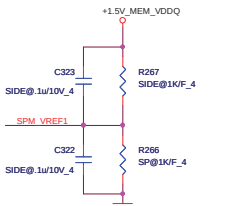
Signals	RS880	RX880
HT_TXCALP	Ra **301 ohm 1%**	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb **301 ohm 1%**	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

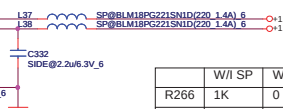
This block is for Side-Port only







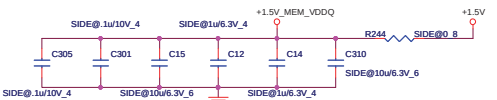
IOPLLVDD18 - memory PLL
not applicable to RX881



0ohm size 0603 CS00003J951
size 0402 CS00002JB38
1K ohm CS21002FB24
Bead CX8PG221003

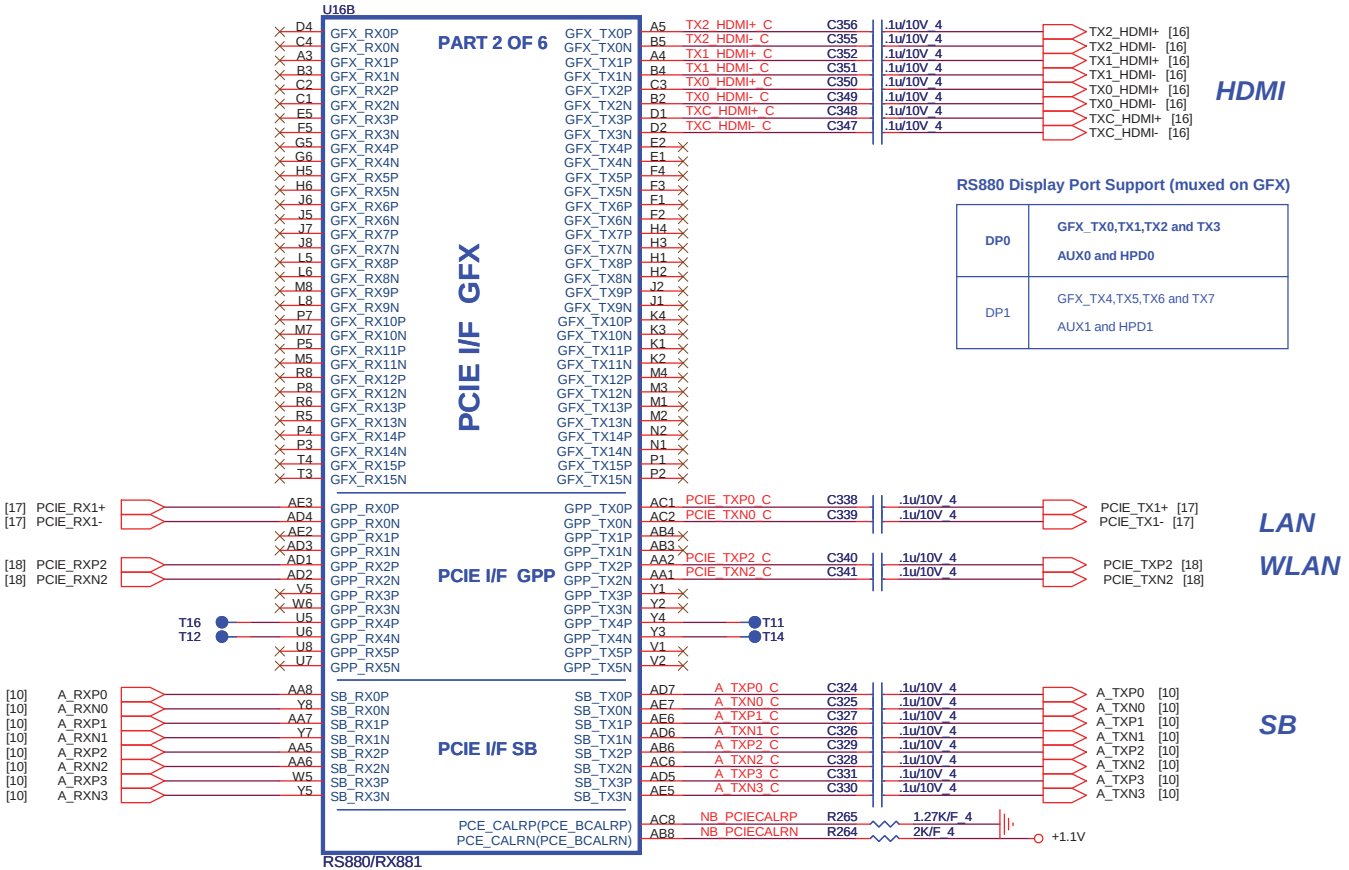
	W/I SP	W/O SP
R266	1K	0
L37	Bead	0
L38	Bead	0

40 mil~50 mil

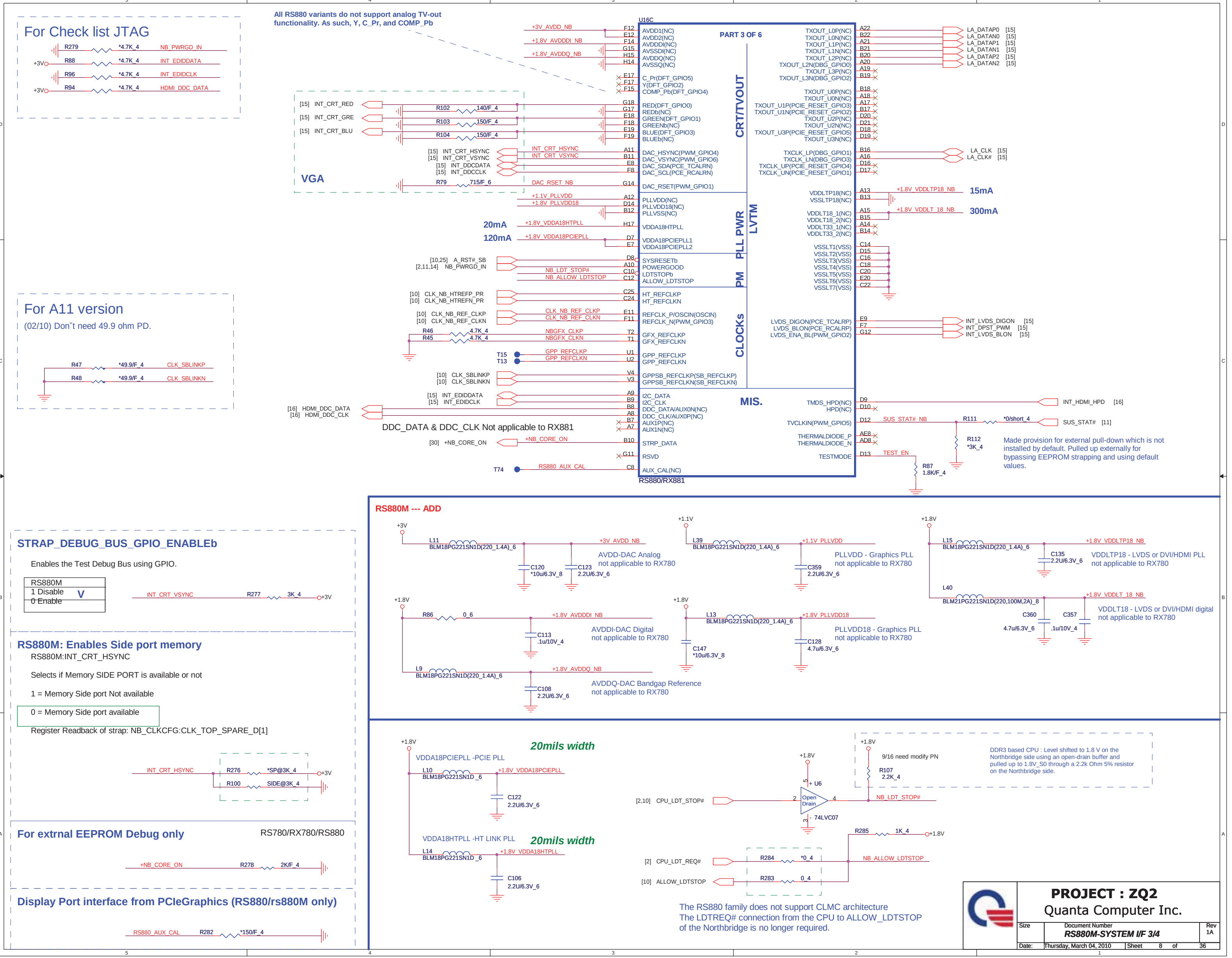


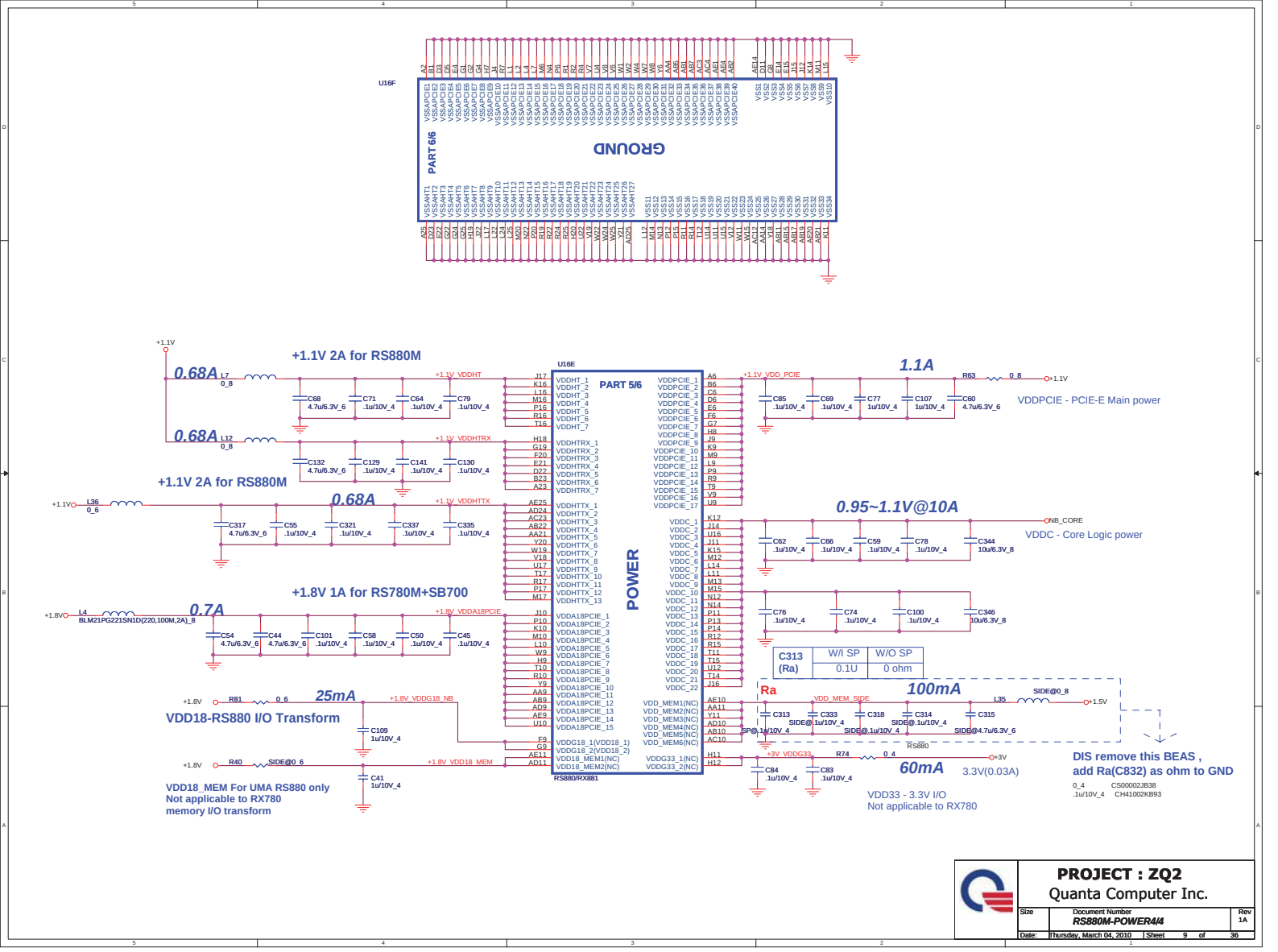
PROJECT : ZQ2
Quanta Computer Inc.

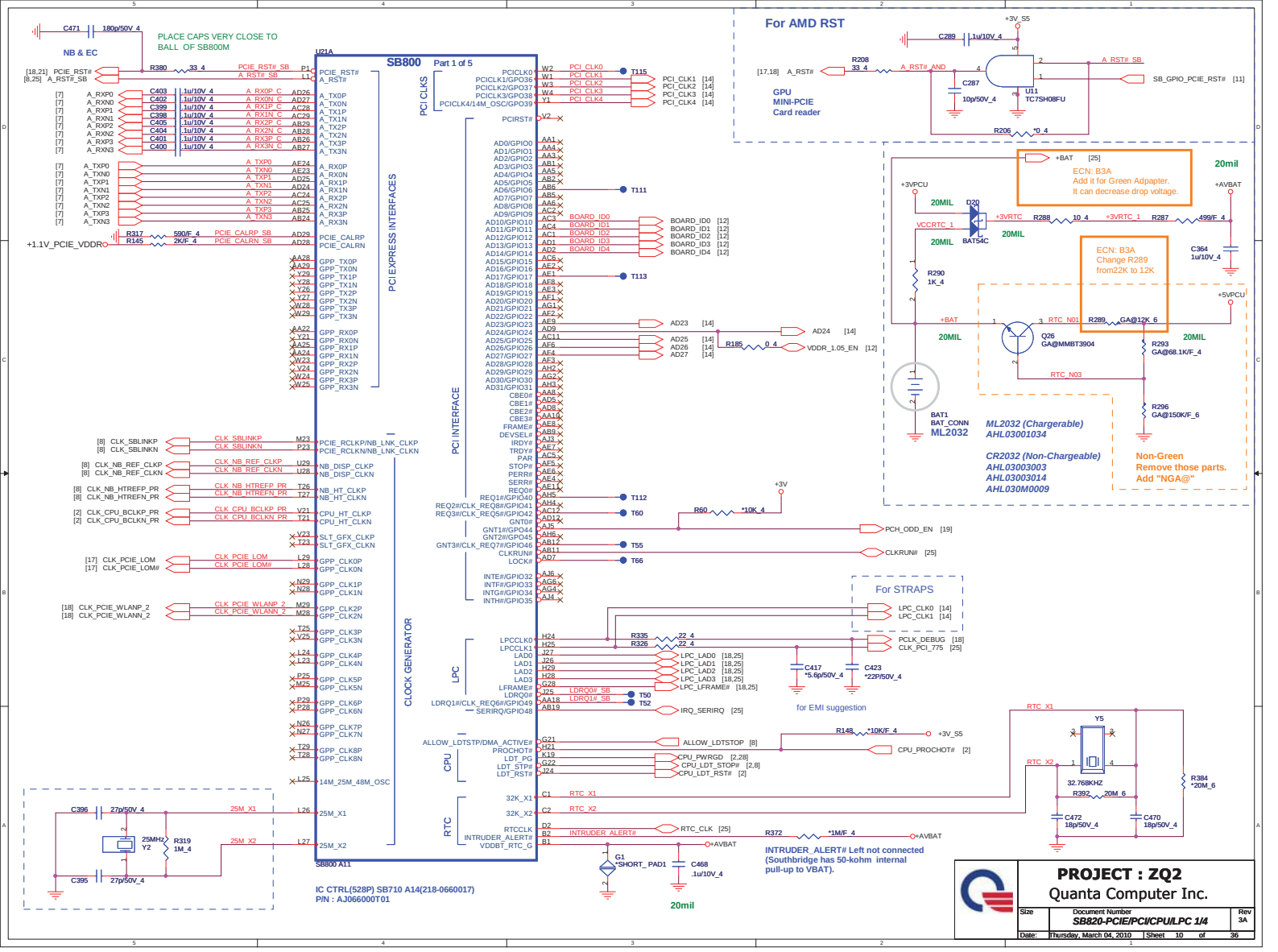
Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A
Date: Thursday, March 04, 2010	Sheet 6 of 36	



PROJECT : ZQ2		
Quanta Computer Inc.		
Size	Document Number: RS880M-PCIE I/F 2/4	Rev 1A
Date: Thursday, March 04, 2010	Sheet 7 of 36	


For Check list JTAG
All RS880 variants do not support analog TV-out functionality. As such, Y, C_Pr, and COMP_Pb
U16C
PART 3 OF 6
CRT/TVOUT
VGA
PLL PWR
LVTM
PM
CLOCKS
MIS.
15mA
300mA
20mA
120mA
For A11 version
(02/10) Don˜t need 49.9 ohm PD.
DDC_DATA & DDC_CLK Not applicable to RX881
RS880/RX881
Made provision for external pull-down which is not installed by default. Pulled up externally for bypassing EEPROM strapping and using default values.
RS880M --- ADD
AVDD-DAC Analog not applicable to RX780
PLLVDD - Graphics PLL not applicable to RX780
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
AVDDI-DAC Digital not applicable to RX780
PLLVDD18 - Graphics PLL not applicable to RX780
AVDDQ-DAC Bandgap Reference not applicable to RX780
STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.
RS880M
1 Disable
0 Enable
RS880M: Enables Side port memory
RS880M:INT_CRT_HSYNC
Selects if Memory SIDE PORT is available or not
1 = Memory Side port Not available
0 = Memory Side port available
Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]
For extrnal EEPROM Debug only
RS780/RX780/RS880
Display Port interface from PCIeGraphics (RS880/rs880M only)
VDDA18PCIEPLL -PCIE PLL
VDDA18HTPLL -HT LINK PLL
20mils width
9/16 need modify PN
DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.
The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.
PROJECT : ZQ2
Quanta Computer Inc.
Document Number
RS880M-SYSTEM I/F 3/4
Rev 1A
Date: Thursday, March 04, 2010
Sheet 8 of 36


U16F
PART 6/6
GROUND
U16E
PART 5/6
POWER
RS880/RX881
+1.1V 2A for RS880M
0.68A
+1.1V 2A for RS880M
0.68A
+1.8V 1A for RS780M+SB700
0.7A
25mA
VDD18-RS880 I/O Transform
VDD18_MEM For UMA RS880 only
Not applicable to RX780
memory I/O transform
1.1A
VDDPCIE - PCIE-E Main power
0.95~1.1V@10A
VDDC - Core Logic power
100mA
60mA
3.3V(0.03A)
VDD33 - 3.3V I/O
Not applicable to RX780
C313 | W/I SP | W/O SP
(Ra) | 0.1U | 0 ohm
DIS remove this BEAS , add Ra(C832) as ohm to GND
PROJECT : ZQ2
Quanta Computer Inc.
RS880M-POWER4/4
Thursday, March 04, 2010
Sheet 9 of 36


For AMD RST
GPU
MINI-PCIE
Card reader
U11
TC7SH08FU
SB800
Part 1 of 5
U21A
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
NB & EC
PLACE CAPS VERY CLOSE TO
BALL OF SB800M
ECN: B3A
Add it for Green Adpapter.
It can decrease drop voltage.
20mil
ECN: B3A
Change R289
from22K to 12K
ML2032 (Chargerable)
AHL03001034
CR2032 (Non-Chargeable)
AHL03003003
AHL03003014
AHL030M0009
Non-Green
Remove those parts.
Add "NGA@"
BAT1
BAT_CONN
ML2032
Q26
GA@MMBT3904
BAT54C
For STRAPS
for EMI suggestion
INTRUDER_ALERT# Left not connected
(Southbridge has 50-kohm internal
pull-up to VBAT).
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
SB800 A11
PROJECT : ZQ2
Quanta Computer Inc.
Document Number
SB820-PCIE/PCI/CPU/LPC 1/4
Rev 3A
Date: Thursday, March 04, 2010
Sheet 10 of 36

NC only ,Can't be install

+3V_S5
R368 *2.2K_4 SB_TEST0
R217 *2.2K_4 SB_TEST1
R210 *2.2K_4 SB_TEST2

SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer

+3V
R150 2.2K_4 PCLK_SMB
R147 2.2K_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

+3V_S5
R188 10K_4 SB_SMBCLK1
R215 10K_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it

+3V_S5
R153 10K_4 SB_SCLK2
R149 10K_4 SB_SDATA2

+3V
R195 4.7K_4 SUS_STAT#

+3V
R316 8.2K_4 CLK_PCIE_LAN_REQ#
R178 8.2K_4 CLK_PCIE_2_REQ#

JTAG DEBUG

+3V_S5
CN13
C279 10P/50V_4
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

To Azalia

ACZ_SDOUT R200 33_4 ACZ_SDOUT_AUDIO [20]
C283 *10P/50V_4
ACZ_SYNC R202 33_4 ACZ_SYNC_AUDIO [20]
C284 *10P/50V_4
ACZ_BCLK R203 33_4 ACZ_BITCLK_AUDIO [20]
C285 *10P/50V_4
ACZ_RST# R201 33_4 ACZ_RST#_AUDIO [20]
ACZ_SDIN0 ACZ_SDIN0 [20]

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U21D
SB800
Part 4 of 5
SB800 A11

T71 SB_PCI_PME# J2 PCI_PME#/GEVENT4#
K1 RI#/GEVENT22#
K3 SPI_CS3#/GBE_STAT1/GEVENT21#
[25] SUSB# F1 SLP_S3#
[25] SUSC# SUSC# H1 SLP_S5#
[25] DNBSWON# F2 PWR_BTN#
[14] SB_PWRGD_IN H5 PWR_GOOD
[8] SUS_STAT# G6 SUS_STAT#
SB_TEST0 B3 TEST0
SB_TEST1 C4 TEST1/TMS
SB_TEST2 F6 TEST2
[25] SIO_A20GATE AD21 GA20IN/GEVENT0#
[25] SIO_RCIN# SIO_RCIN# AE21 KBRST#/GEVENT1#
LANLINK_STATE#
T114 K2 LPC_PME#/GEVENT3#
[25] SIO_EXT_SMI# J29 LPC_SMI#/GEVENT23#
[25] SIO_EXT_SCI# H2 GEVENTS#
T116 SYS_RST# J1 SYS_RESET#/GEVENT19#
[17,18] PCIE_WAKE# H6 WAKE#/GEVENT8#
T117 IR_RX1 F3 IR_RX1/GEVENT20#
T69 SB_THERMTRIP# J6 THRMTRIP#/SMBALERT#/GEVENT2#
[2,8,14] NB_PWRGD_IN AC19 NB_PWRGD
[25] ICH_RSMRST# G1 RSMRST#

ACPI / WAKE UP EVENTS
USB 1.1 USB MISC

USBCLK/14M_25M_48M_OSC A10 USB_14_48M T110
USB_RCOMP G19 USB_RCOMP_SB R169 11.8K/F_6
USB_FSD1P/GPIO186 J10 USB_FSD1P
USB_FSD1N H11 USB_FSD1N
USB_FSD0P/GPIO185 H9 USB_FSD12P T63
USB_FSD0N J8 USB_FSD12N T58

USB_HSD13P B12 USBP13+ [15]
USB_HSD13N A12 USBP13- [15] CAMERA
USB_HSD12P F11 USBP12+ [22]
USB_HSD12N E11 USBP12- [22] USBX3 board
USB_HSD11P E14 USBP11+ [22]
USB_HSD11N E12 USBP11- [22] USBX3 board
USB_HSD10P J12 USBP10+ [21]
USB_HSD10N J14 USBP10- [21] Card reader
USB_HSD9P A13 USBP9+ [22] BLUETOOTH
USB_HSD9N B13 USBP9- [22]
USB_HSD8P D13 USBP8+ [22]
USB_HSD8N C13 USBP8- [22] USBX3 board
USB_HSD7P G12
USB_HSD7N G14
USB_HSD6P G16
USB_HSD6N G18
USB_HSD5P D16
USB_HSD5N C16
USB_HSD4P B14 USBP4+ [18]
USB_HSD4N A14 USBP4- [18] WLAN Min-Card
USB_HSD3P F18
USB_HSD3N E16
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17 USBP1+ T54
USB_HSD1N A17 USBP1- T53
USB_HSD0P A16 USBP0+ [22]
USB_HSD0N B16 USBP0- [22]

EHCI3/ OHCI3
EHCI2/ OHCI2
EHCI1/ OHCI1

GPIO
USB 2.0

[10] SB_GPIO_PCIE_RST# SB_GPIO_PCIE_RST#
[17] CLK_PCIE_LAN_REQ# CLK_PCIE_LAN_REQ# AB19 CLK_REQ4#/SATA_IS0#/GPIO64
AA16 CLK_REQ3#/SATA_IS1#/GPIO63
AB21 SMARTVOLT1/SATA_IS2#/GPIO50
AC18 CLK_REQ0#/SATA_IS3#/GPIO60
AF20 SATA_IS4#/FANOUT3/GPIO55
T51 SB_GPIO59 AE19 SATA_IS5#/FANIN3/GPIO59
[20] SPKR AF19 SPKR/GPIO66
[5,17,18] PCLK_SMB PCLK_SMB AD22 SCL0/GPIO43
[5,17,18] PDAT_SMB PDAT_SMB AE22 SDA0/GPIO47
SB_SMBCLK1 F5 SCL1/GPIO227
SB_SMBDATA1 F4 SDA1/GPIO228
[18] CLK_PCIE_2_REQ# AH21 CLK_REQ2#/FANIN4/GPIO62
AB18 CLK_REQ1#/FANOUT4/GPIO61
E1 IR_LED#/ILB#/GPIO184
AJ21 SMARTVOLT2/SHUTDOWN#/GPIO51
[6] SP_DDR3_RST# H4 DDR3_RST#/GEVENT7#
D5 GBE_LED0/GIO183
D7 GBE_LED1/GEVENT9#
G5 GBE_LED2/GEVENT10#
K5 GBE_STAT0/GEVENT11#
T109 E_SB_OSC AA20 CLK_REQG#/GPIO65/OSCIN

USB OC

[22] OC_7# H3 BLINK/USB_OC7#/GEVENT18#
[22] OC_6# D1 USB_OC6#/IR_TX1/GEVENT6#
T59 SB_PM_THERM# E4 USB_OC5#/IR_TX0/GEVENT17#
[22] OC_4# D4 USB_OC4#/IR_RX0/GEVENT16#
SB_JTAG_TDO E8 USB_OC3#/AC_PRES/TDO/GEVENT15#
SB_JTAG_TCK F7 USB_OC2#/TCK/GEVENT14#
SB_JTAG_TDI E7 USB_OC1#/TDI/GEVENT13#
SB_JTAG_RST# F8 USB_OC0#/TRST#/GEVENT12#

Eliot (02/26)
Current Agesa bios doesn't program ALERT_L and SB won't process alert.

HD audio interface is +3VS5 voltage

ACZ_BCLK M3 AZ_BITCLK
ACZ_SDOUT N1 AZ_SDOUT
[14] ACZ_SDOUT ACZ_SDIN0 L2 AZ_SDIN0/GPIO167
M2 AZ_SDIN1/GPIO168
M1 AZ_SDIN2/GPIO169
M4 AZ_SDIN3/GPIO170
ACZ_SYNC N2 AZ_SYNC
ACZ_RST# P2 AZ_RST#

HD AUDIO

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_GPIO195
SDA3_LV/GPIO196 E26 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197 F25 T48
EC_PWM1/EC_TIMER1/GPIO198 F22
EC_PWM2/EC_TIMER2/GPIO199 F22 GPIO199 [14]
EC_PWM3/EC_TIMER3/GPIO200 E21 GPIO200 [14]

On Board USB Connector
Only USB Port0 can be configured as debug port.

+3V_S5
R197 10K_4 GBE_COL
R191 10K_4 GBE_CRS
R182 10K_4 GBE_MDIO
R196 10K_4 GBE_RXERR
R190 10K_4 GBE_PHY_INTR
T49 ADP_PRES0

GBE_COL T1
GBE_CRS T4
GBE_MDCK L6
GBE_MDIO L5
GBE_RXCLK T9
GBE_RXD3 U1
GBE_RXD2 U3
GBE_RXD1 T2
GBE_RXD0 U2
GBE_RXCTL/RXDV T5
GBE_RXERR V5
GBE_TXCLK P5
GBE_TXD3 M5
GBE_TXD2 P9
GBE_TXD1 T7
GBE_TXD0 P7
GBE_TXCTL/TXEN M7
GBE_PHY_PD P4
GBE_PHY_RST# M9
GBE_PHY_INTR V7

GBE LAN

PS2_DAT/SDA4/GPIO187 E23
PS2_CLK/SCL4/GPIO188 E24
SPI_CS2#/GBE_STAT2/GPIO166 F21
FC_RST#/GPIO160 G29
PS2KB_DAT/GPIO189 D27
PS2KB_CLK/GPIO190 F28
PS2M_DAT/GPIO191 F29
PS2M_CLK/GPIO192 E27

EMBEDDED CTRL

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

EMBEDDED CTRL

[02/22] AMD FAE and checklist request PL.

Check list

SB_GPIO195 R146 10K_4
SB_GPIO196 R144 10K_4

PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number SB820-ACPI/GPIO/USB 2/4
Rev 1A
Date: Thursday, March 04, 2010 Sheet 11 of 36

Max trace length: 6"

SATA HDD

SATA ODD

SATA PORT 0,1,2,3 can support AHCI mode

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

U21B

SB800

Part 2 of 5

SB800 A11

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Check list

TEMPIN0	R346	10K_4
TEMPIN1	R345	10K_4
MB_THRMDA_SB	R350	10K_4
SB_GPIO174	R353	10K_4
SB_GPIO175	R364	10K_4
SB_GPIO176	R366	10K_4

BOM check

	1	0
ID0	15"	14"
ID1	DIS	UMA
ID2	W/I	W/O
ID3	JM	JV
ID4	6L	8L

Sideport

DDR3 Sideport Memory Device

	1	0
ID0	SAM	HYU
ID1	RSV	RSV

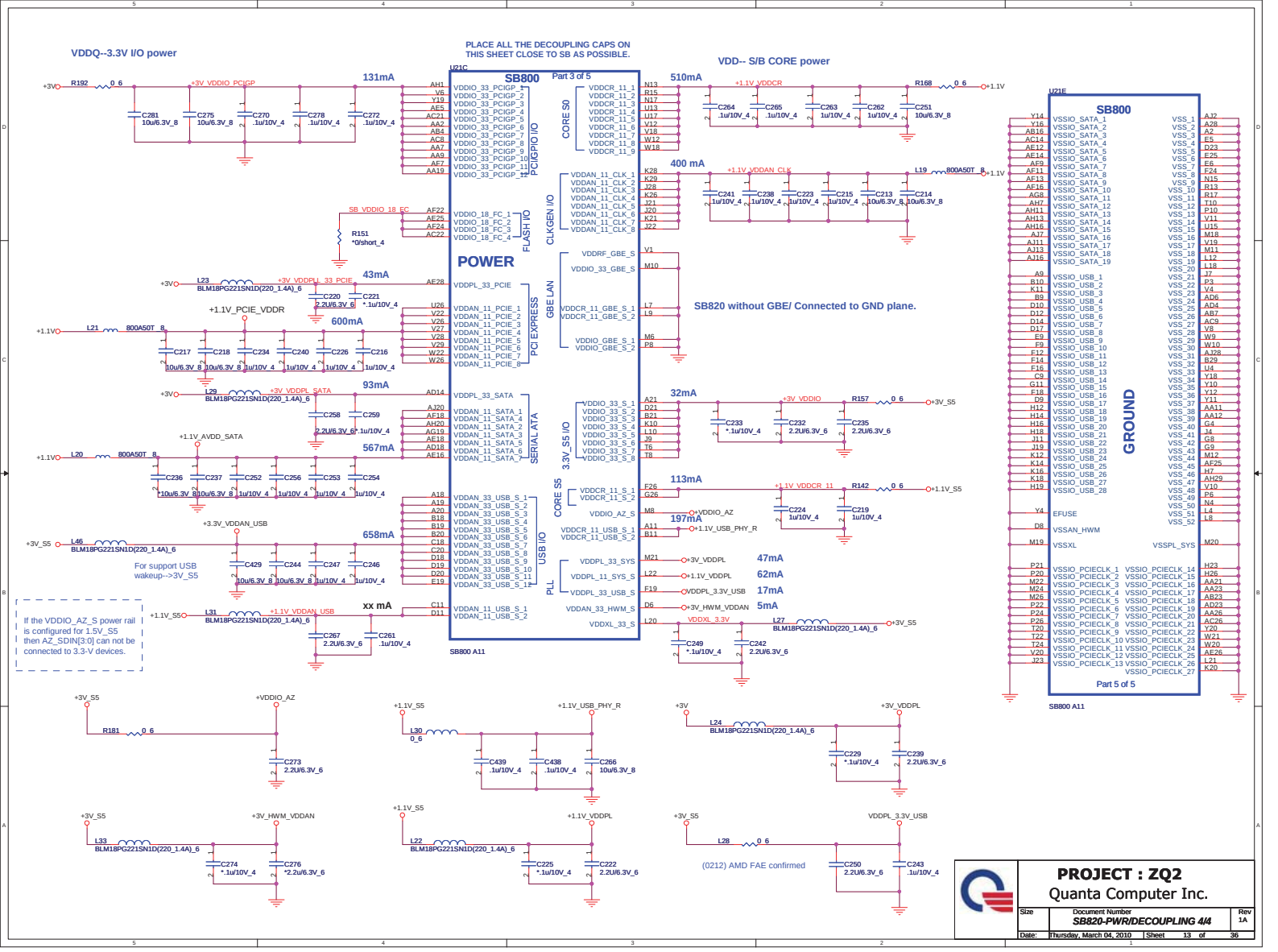
Vendor	Vendor P/N	STN B/S P/N	Size	BOARD_ID2 GPIO12	SIDE_PORT_ID1 GPIO178	SIDE_PORT_ID0 GPIO177
Hynix	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	0 (WO/Sideport)	0	0
Samsung	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	1 (W/Sideport)	0	1

VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A

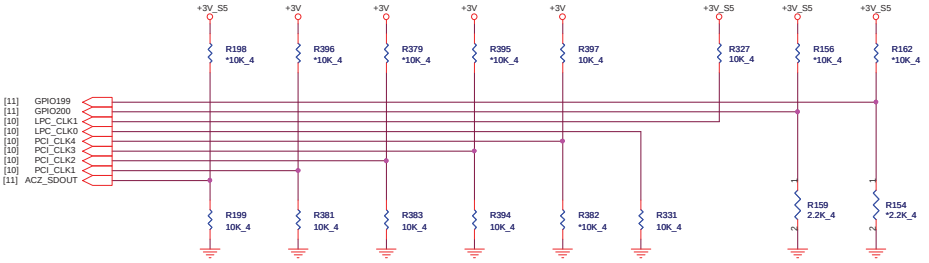
Date: Thursday, March 04, 2010 Sheet 12 of 36


VDDQ--3.3V I/O power
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.
VDD-- S/B CORE power
SB800
Part 3 of 5
POWER
SB820 without GBE/ Connected to GND plane.
GROUND
Part 5 of 5
131mA
510mA
43mA
400 mA
+1.1V_PCIE_VDDR
600mA
93mA
32mA
+1.1V_AVDD_SATA
567mA
113mA
+3.3V_VDDAN_USB
658mA
197mA
For support USB wakeup-->3V_S5
xx mA
If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.
47mA
62mA
17mA
5mA
(0212) AMD FAE confirmed
SB800 A11
PROJECT : ZQ2
Quanta Computer Inc.
Document Number
SB820-PWR/DECOUPLING 4/4
Rev 1A
Date: Thursday, March 04, 2010
Sheet 13 of 36

REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

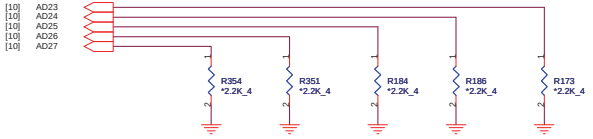


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

DEBUG STRAPS

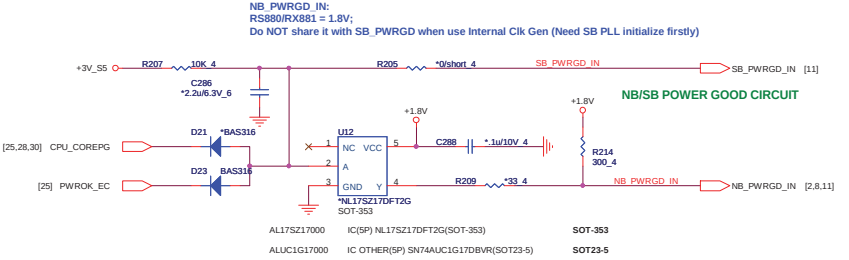
SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)

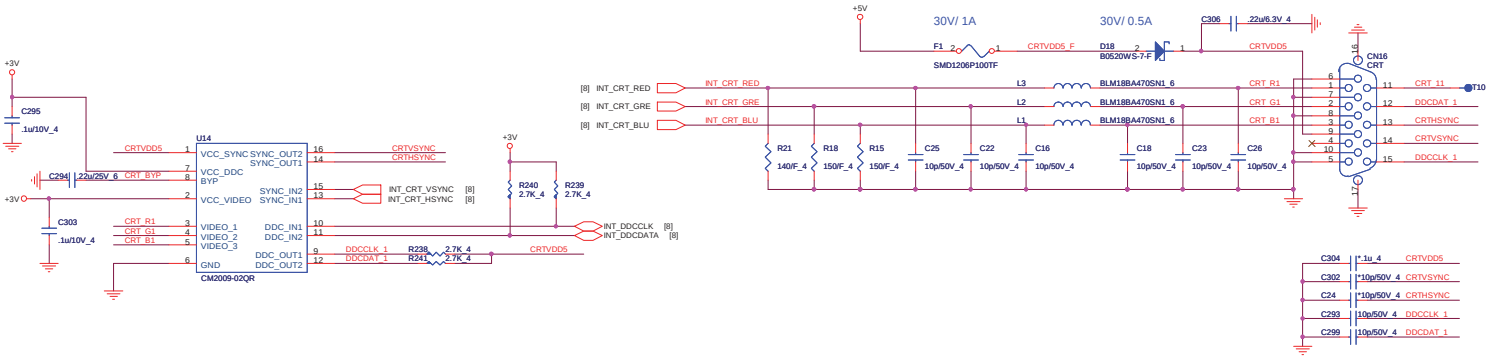


PROJECT : ZQ2
Quanta Computer Inc.

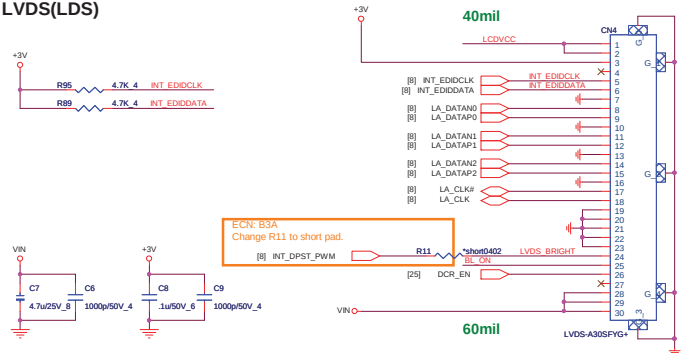
Size	Document Number	Rev
	SB820-STRAPS	1A

Date: Thursday, March 04, 2010 | Sheet 14 of 36

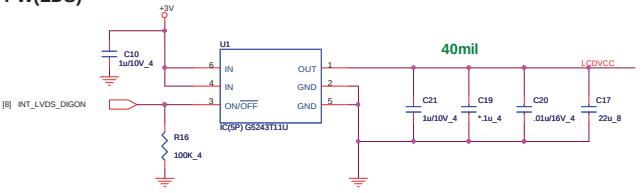
CRT



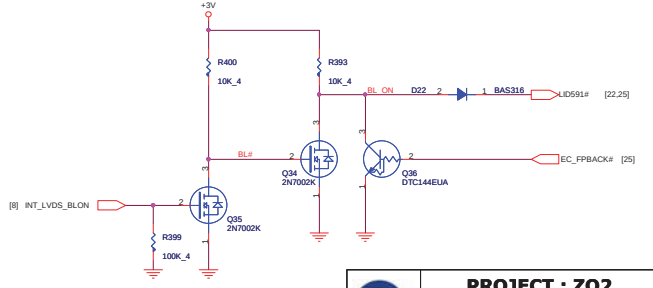
LVDS(LDS)



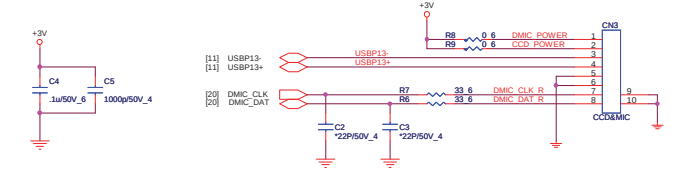
LCD PW(LDS)



Backlight Control(LDS)



CAMERA Module(CCD)

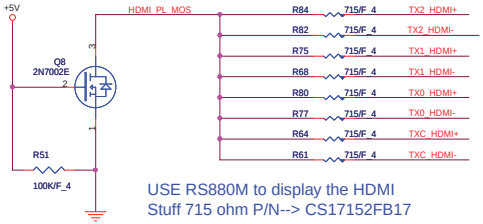


PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	CRT/LVDS/LID	3A
Date: Thursday, March 04, 2010	Sheet 15 of 36	

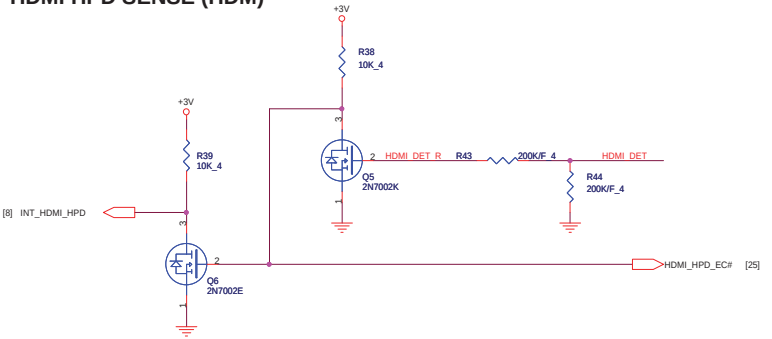
HDMI (HDM)

Close to HDMI Connector

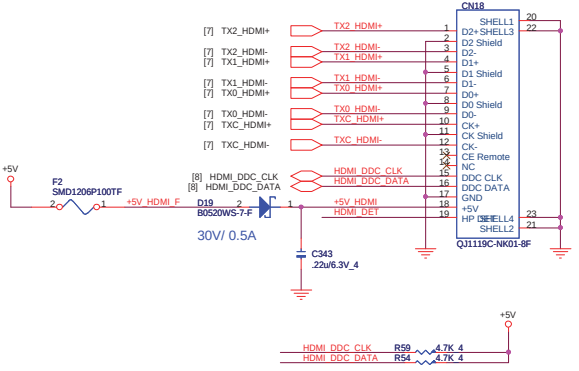


USE RS880M to display the HDMI
Stuff 715 ohm P/N--> CS17152FB17

HDMI HPD SENSE (HDM)

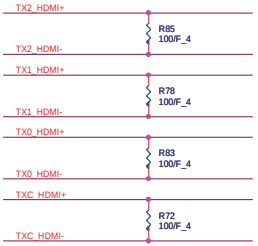


HDMI PORT (HDM)



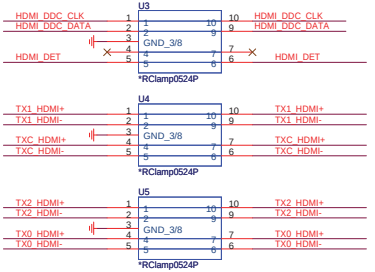
EMI reserve for HDMI(EMC)

Close connector



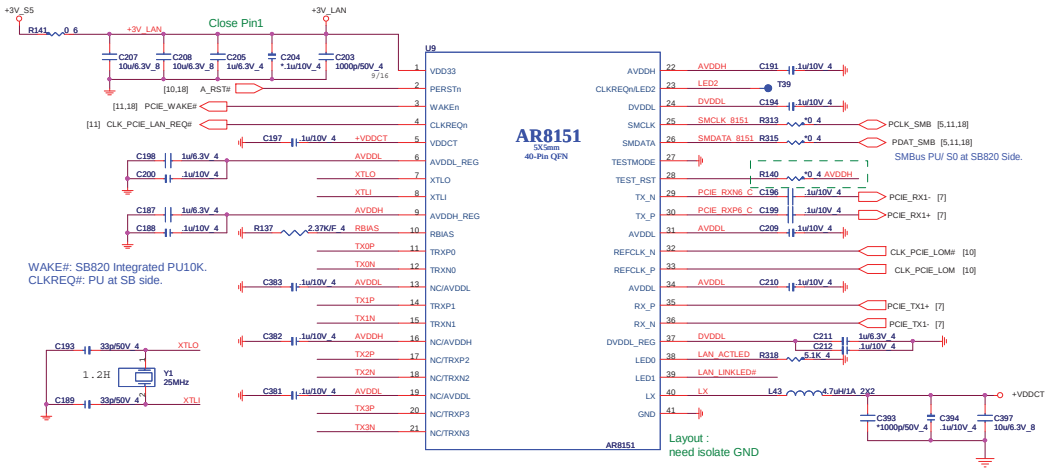
ESD Protect (EMC)

close to HDMI connector

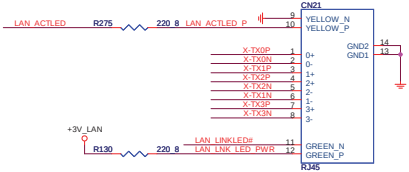


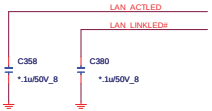
	PROJECT : ZQ2		
	Quanta Computer Inc.		
Size	Document Number **HDMI**		Rev 1A
Date: Thursday, March 04, 2010	Sheet 16 of 36		

Giga-LAN AR8151



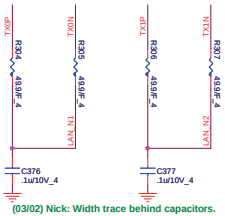
RJ45(LAN)



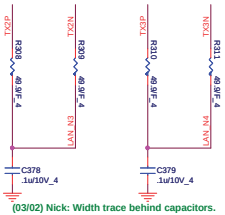


Sertek (03/01):
EMI capacitors, 470pF is enough.
Don't over 490 pF.

TRANSFORMER(LAN)

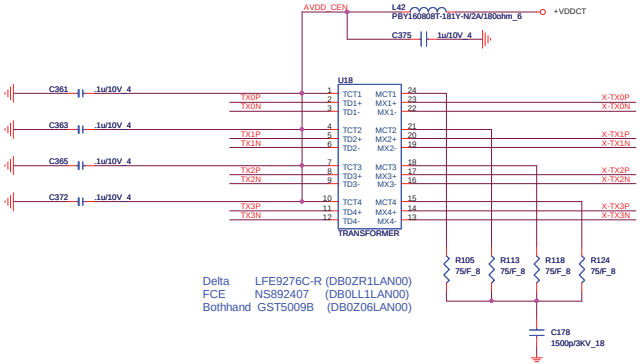


(03/02) Nick: Width trace behind capacitors.



(03/02) Nick: Width trace behind capacitors.

Close Transformer U28

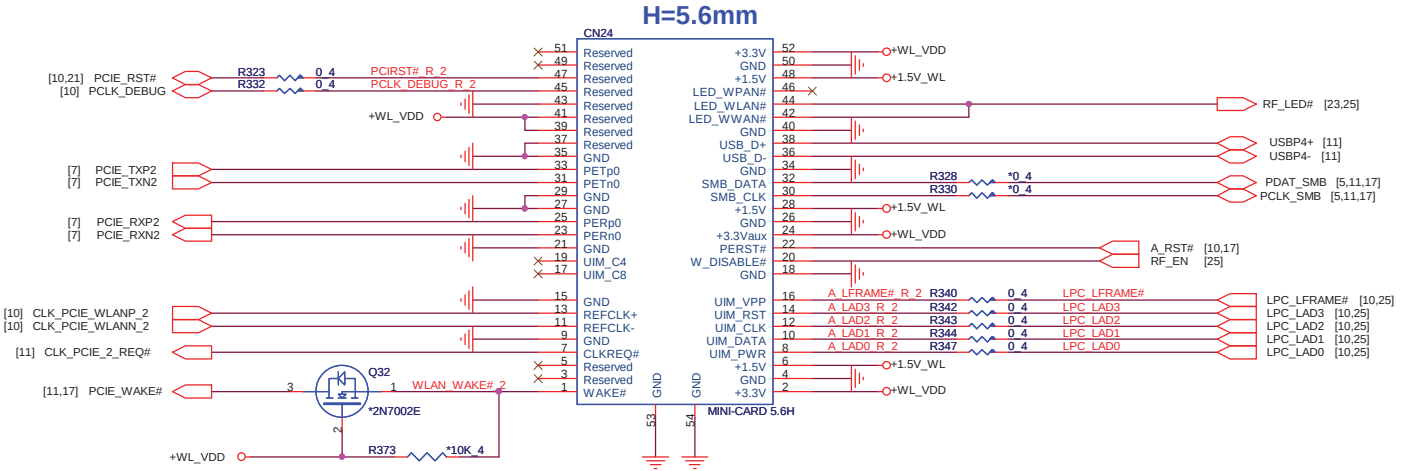


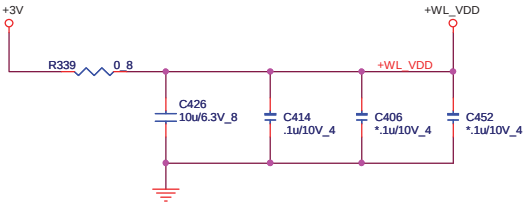
Delta LFE9276C-R (DB0ZR1LAN00)
FCE NS892407 (DB0LL1LAN00)
Bothhand GST5009B (DB0Z06LAN00)

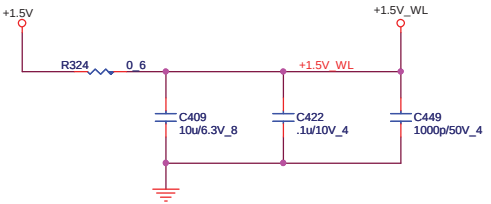
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	LAN (AR8151)	1A
Date: Thursday, March 04, 2010	Sheet 17 of 36	

MINI-CARD WLAN(MNC)





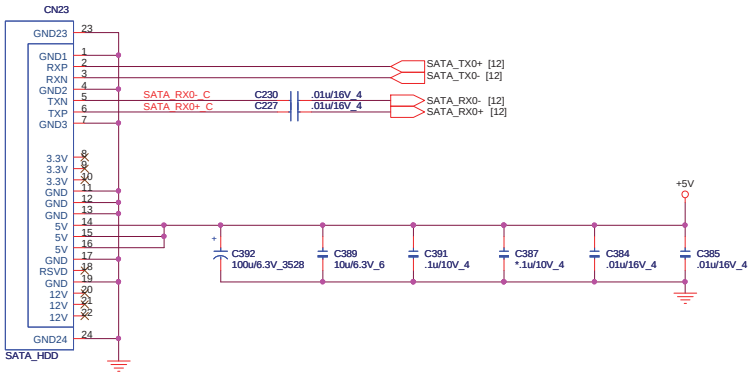


PROJECT : ZQ2

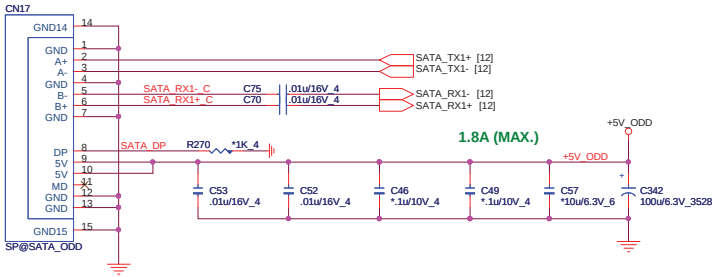
Quanta Computer Inc.

Size	Document Number	Rev
	Mini-Card/WL	1A
Date: Thursday, March 04, 2010	Sheet 18 of 36	

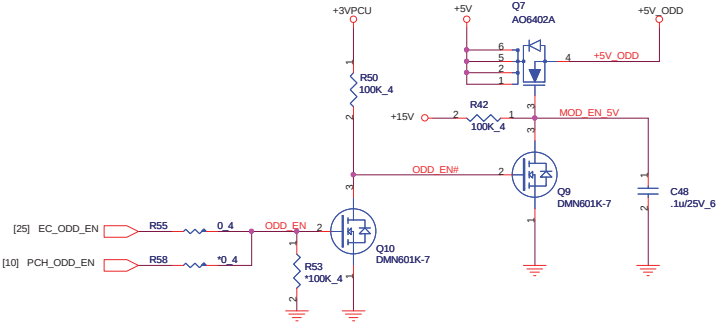
SATA HDD(HDD)



SATA ODD (ODD)



ODD POWER(ODD)



JM-9.5mm (H=2.4mm)/ Slim

Main	DFHS13FR078, DFHS13FR077
Second	DFHS13FR075

JV-12.7mm(H=5.5mm)/ Standard

Main	DFHS13FR017
Second	DFHS13FR006, DFHS13FR005

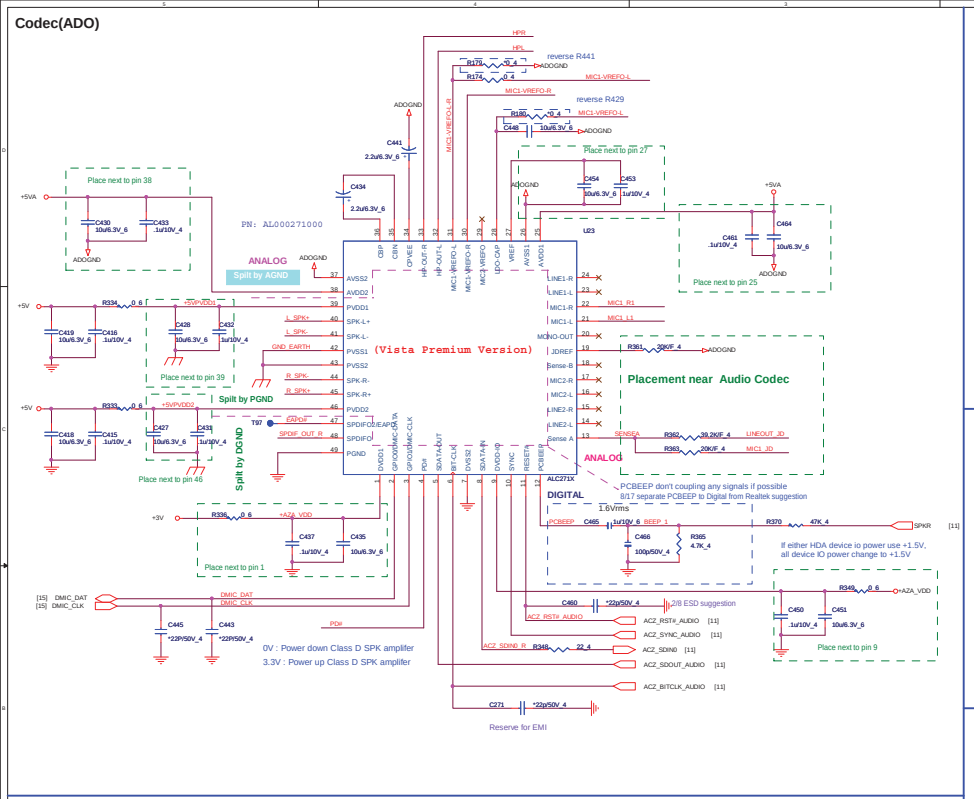
PROJECT : ZQ2

Quanta Computer Inc.

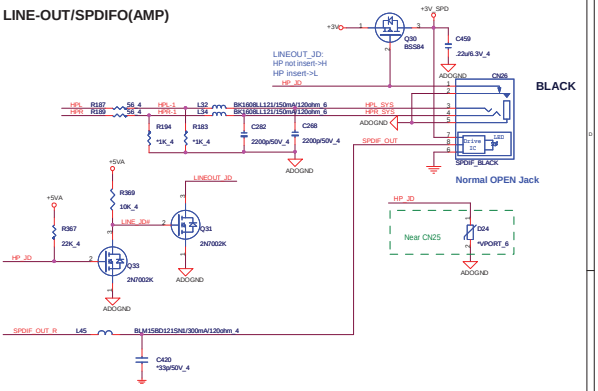
Size	Document Number	Rev
	SATA-HDD/ODD/HOLE	1A

Date: Thursday, March 04, 2010 Sheet 19 of 36

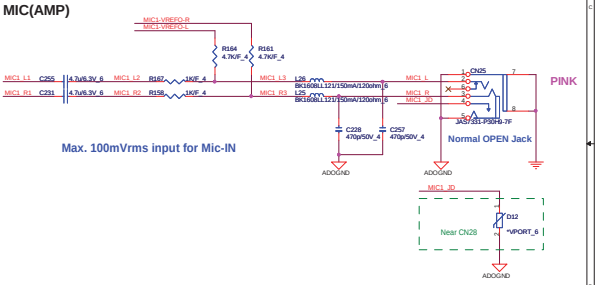
Codec(ADO)



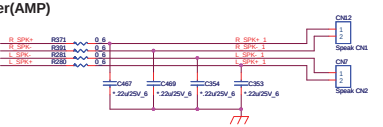
LINE-OUT/SPDIFO(AMP)



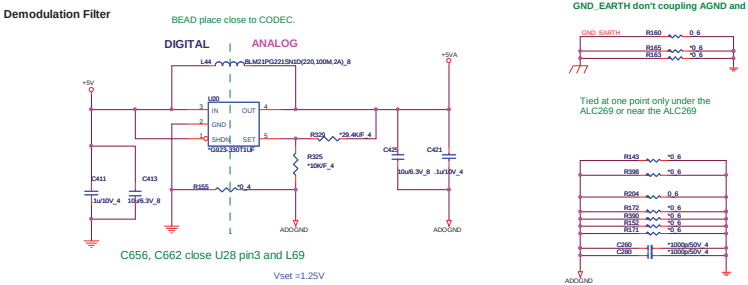
MIC(AMP)



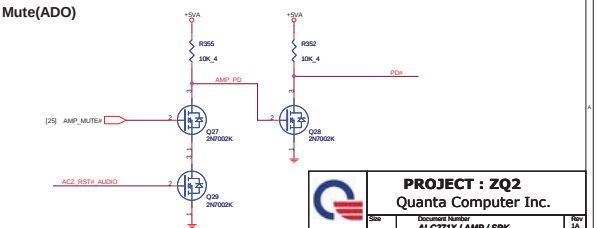
Internal Speaker(AMP)



Power (ADO)

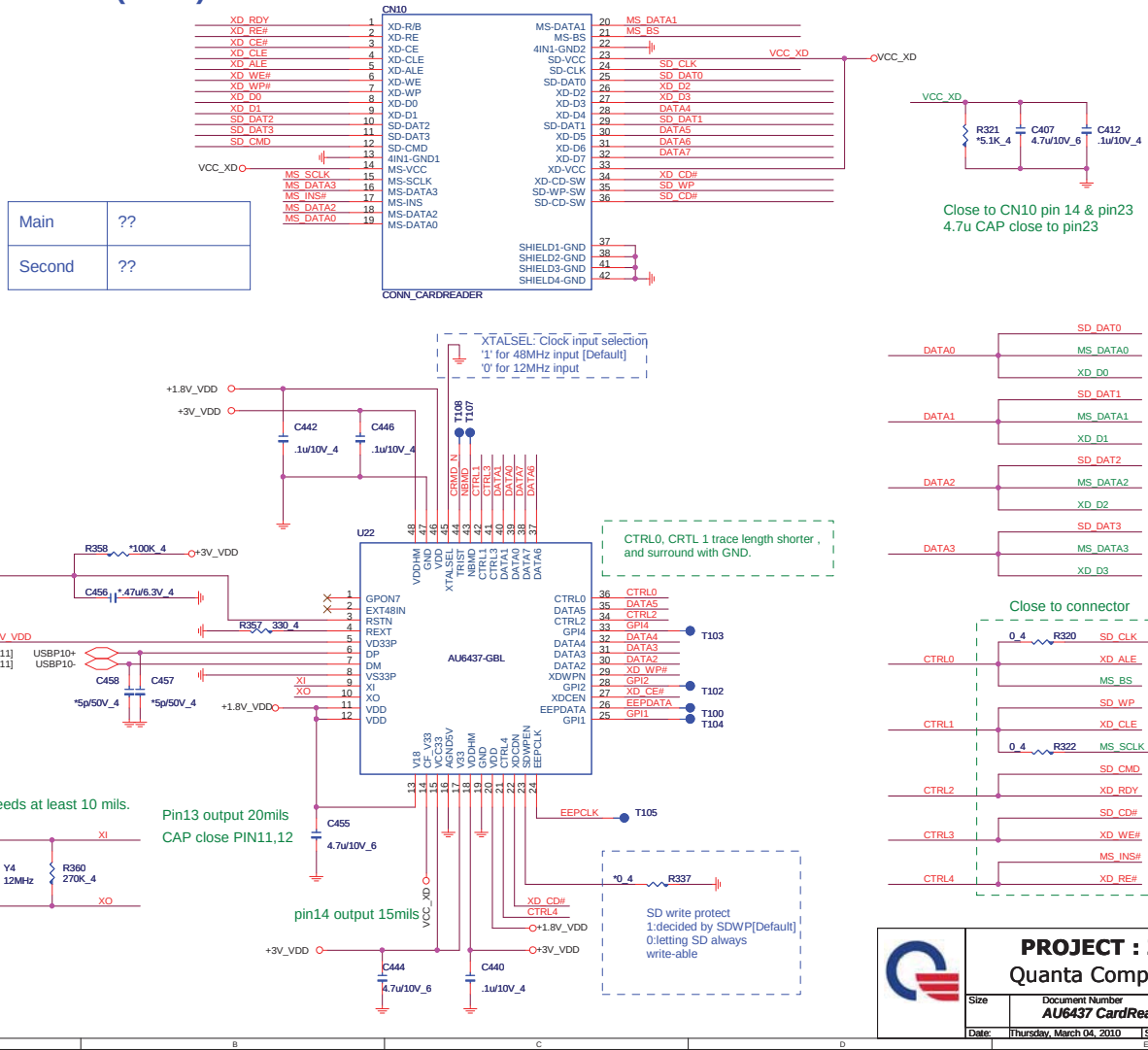


Mute(ADO)



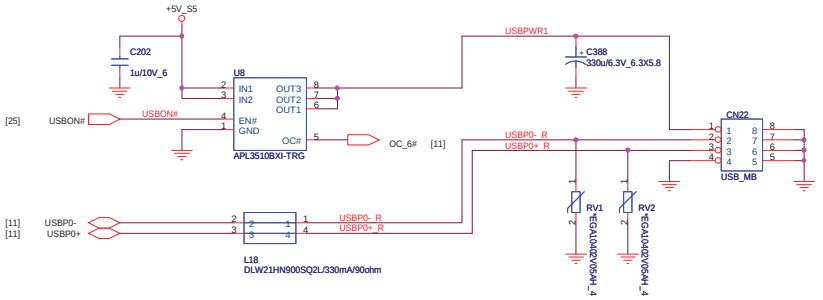
PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: *ALC271X / AMP / SPK* | Rev: 1A
Date: Thursday, March 04, 2010 | Sheet 20 of 36

4 IN 1 CARD READER (MMC)

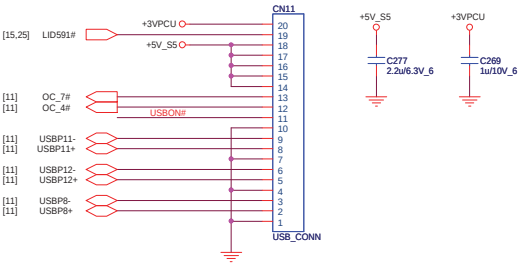


PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: AU6437 CardReader — Rev 1A
Date: Thursday, March 04, 2010	Sheet 21 of 36

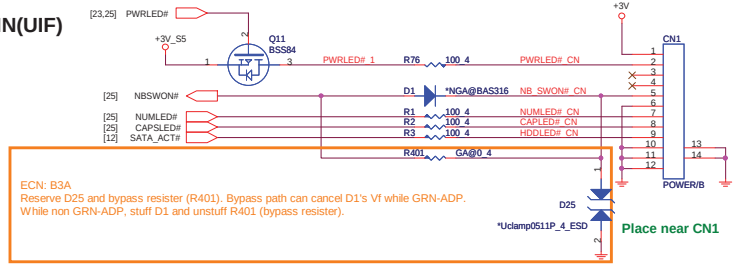
USB PORT(USB/MB)



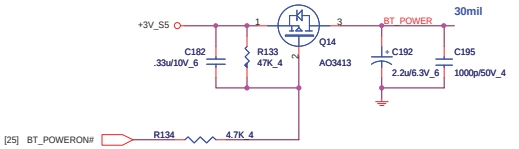
USB BOARD CONN(USB/SB)

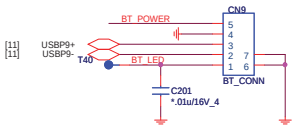


POWER BOARD CONN(UIF)

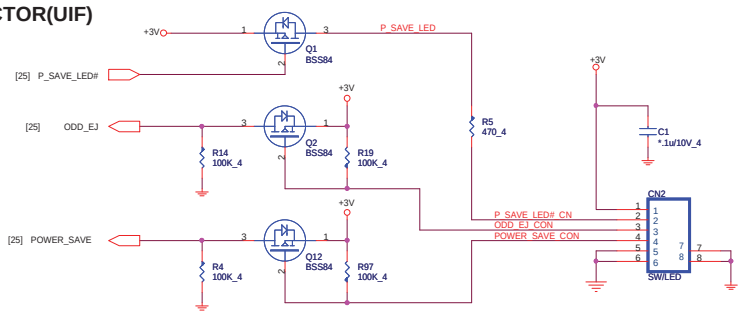


BLUETOOTH CONN(BTM)





LED BOARD CONNECTOR(UIF)

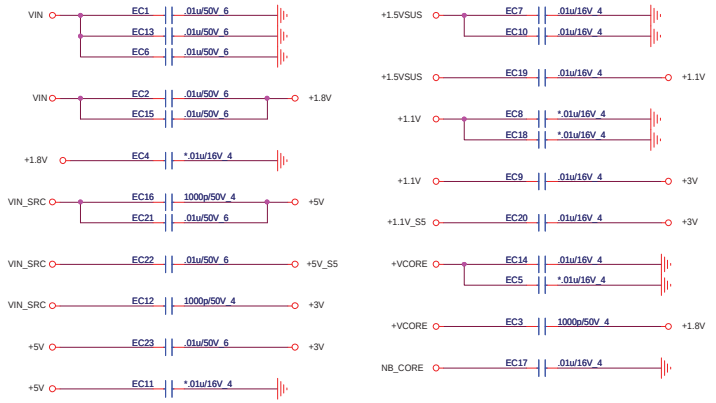


PROJECT : ZQ2

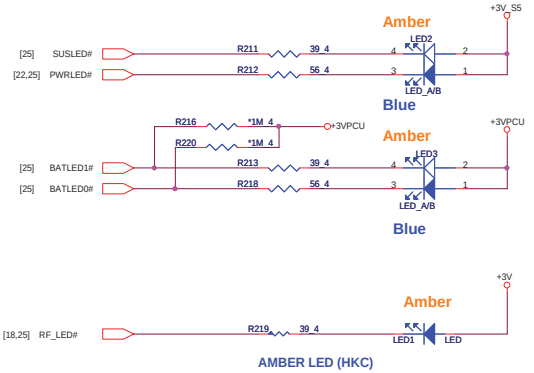
Quanta Computer Inc.

Size	Document Number	Rev
	USB/BT/TP	3A
Date: Thursday, March 04, 2010	Sheet 22 of 36	

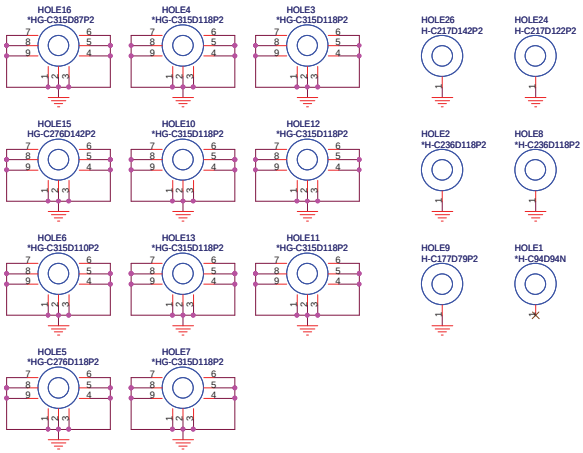
EE RETURN-PATH CAPACITORS(EMC)

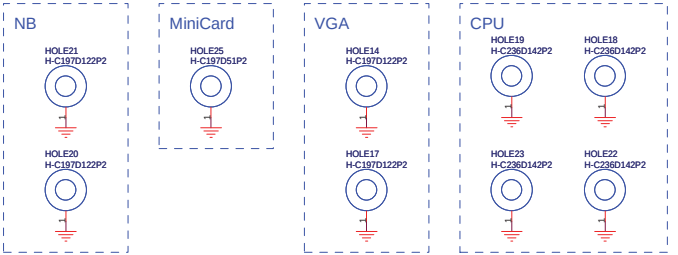


LED(UIF)



HOLE(OTH)



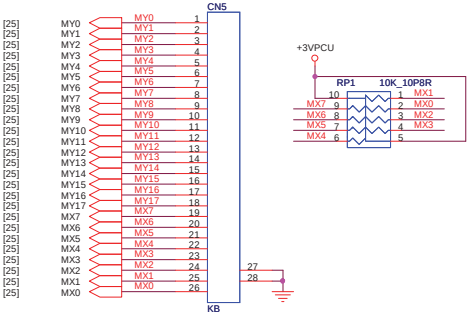


PROJECT : ZQ2

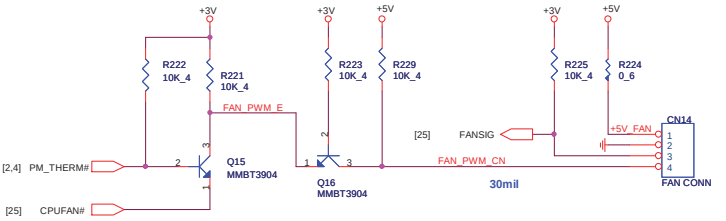
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
Date: Thursday, March 04, 2010	Sheet 23 of 36	

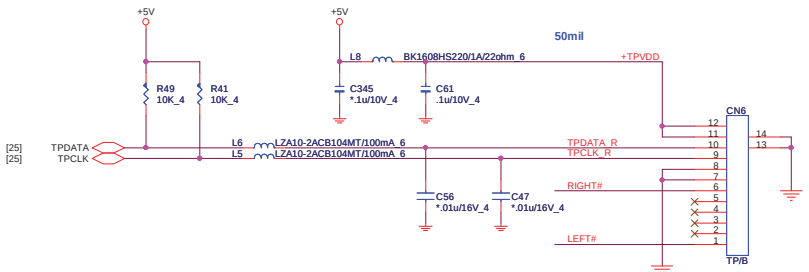
K/B(KBC)

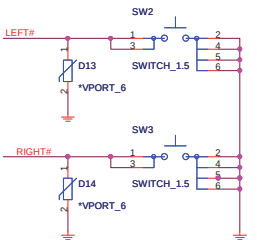


CPU FAN(THM)



TOUCHPAD BOARD CONN(TPD)



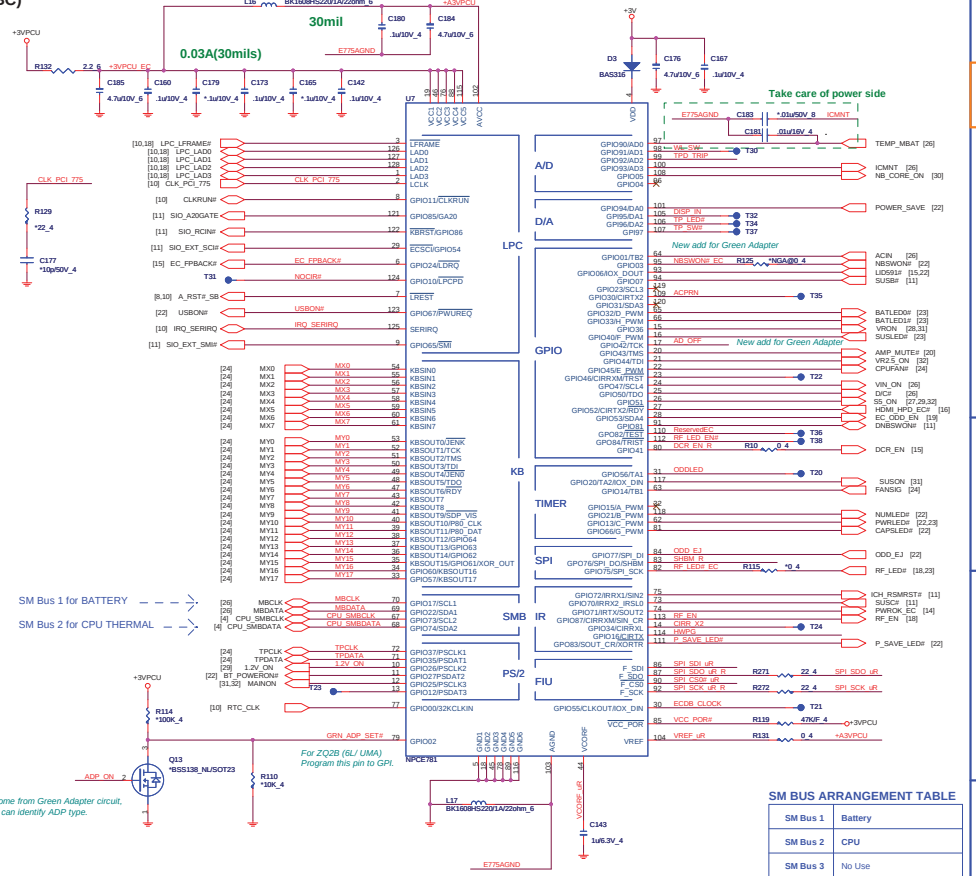


PROJECT : ZQ2

Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
Date: Thursday, March 04, 2010	Sheet 24 of 36	

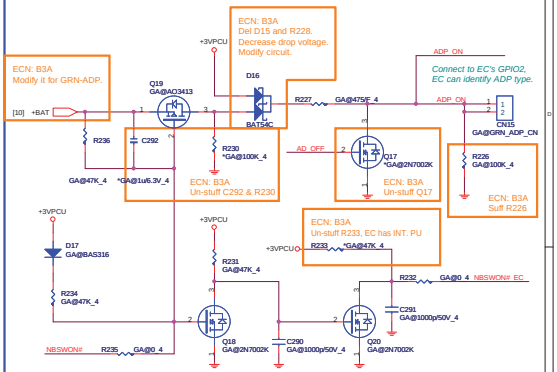
EC(KBC)



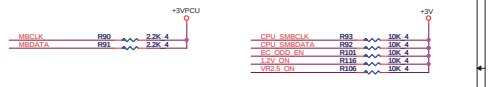
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU
SM Bus 3	No Use

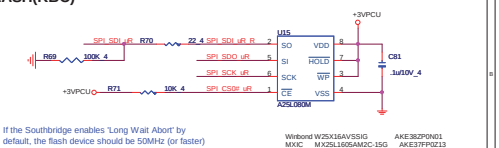
GREEN ADAPTER CIRCUIT



SM BUS PU(KBC)



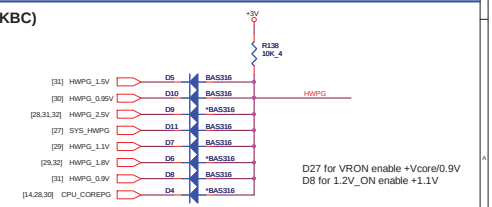
SPI FLASH(KBC)



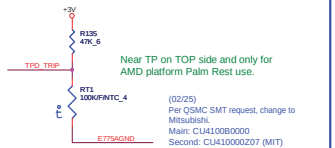
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

Winbond W25X16AVSSIG — AKE382P0N01
MXIC MX25L1605AM2C-15G — AKE37P0Z13
EON EN25F16-100HIP — AKE38ZA0Q00
AMIC A25L016 — AKE38ZN0800

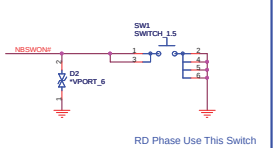
HWPG(KBC)



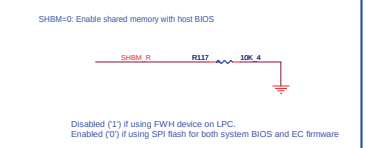
PALM REST THERMAL SENSOR (THM)



POWER-ON SWITCH (KBC)

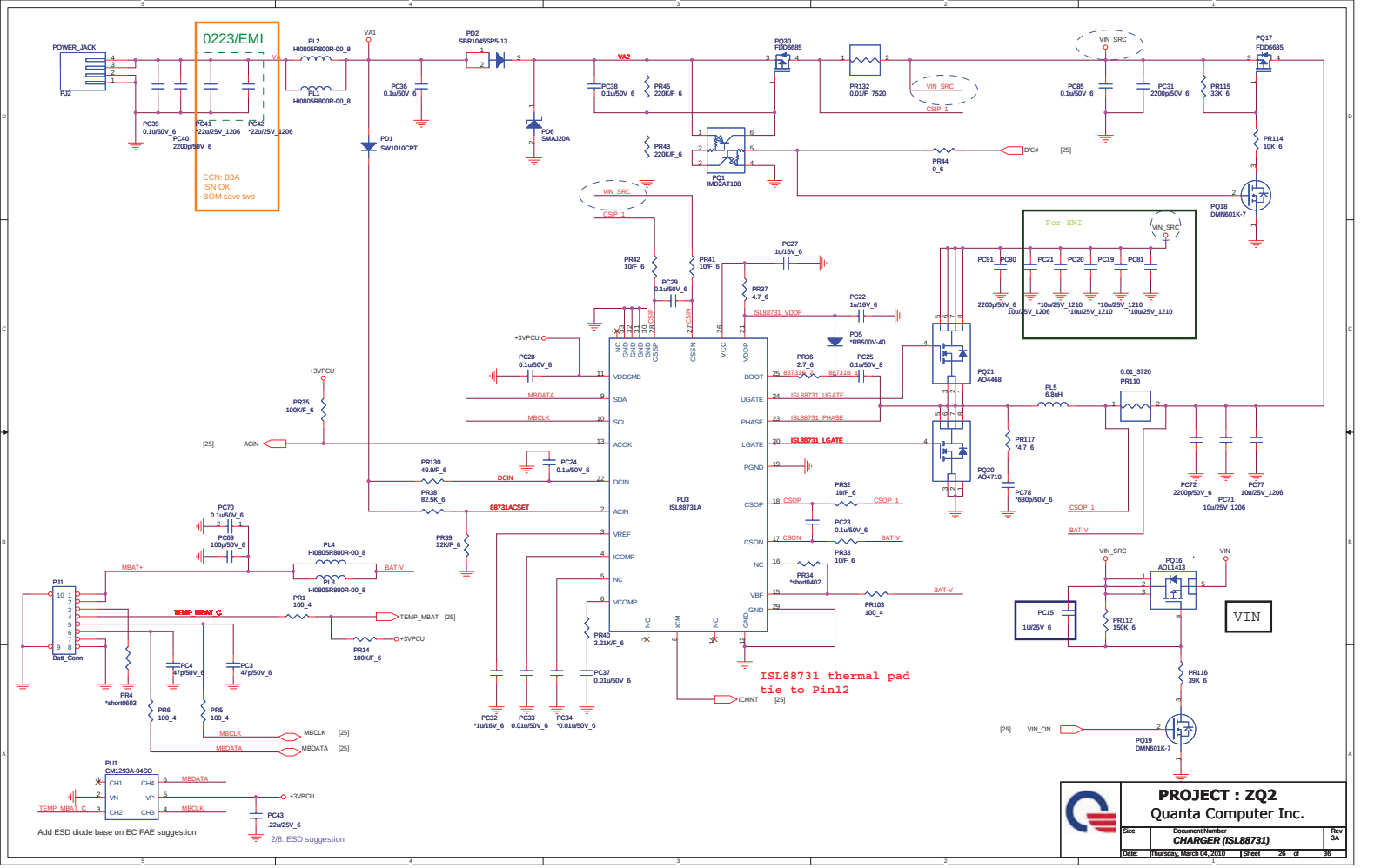


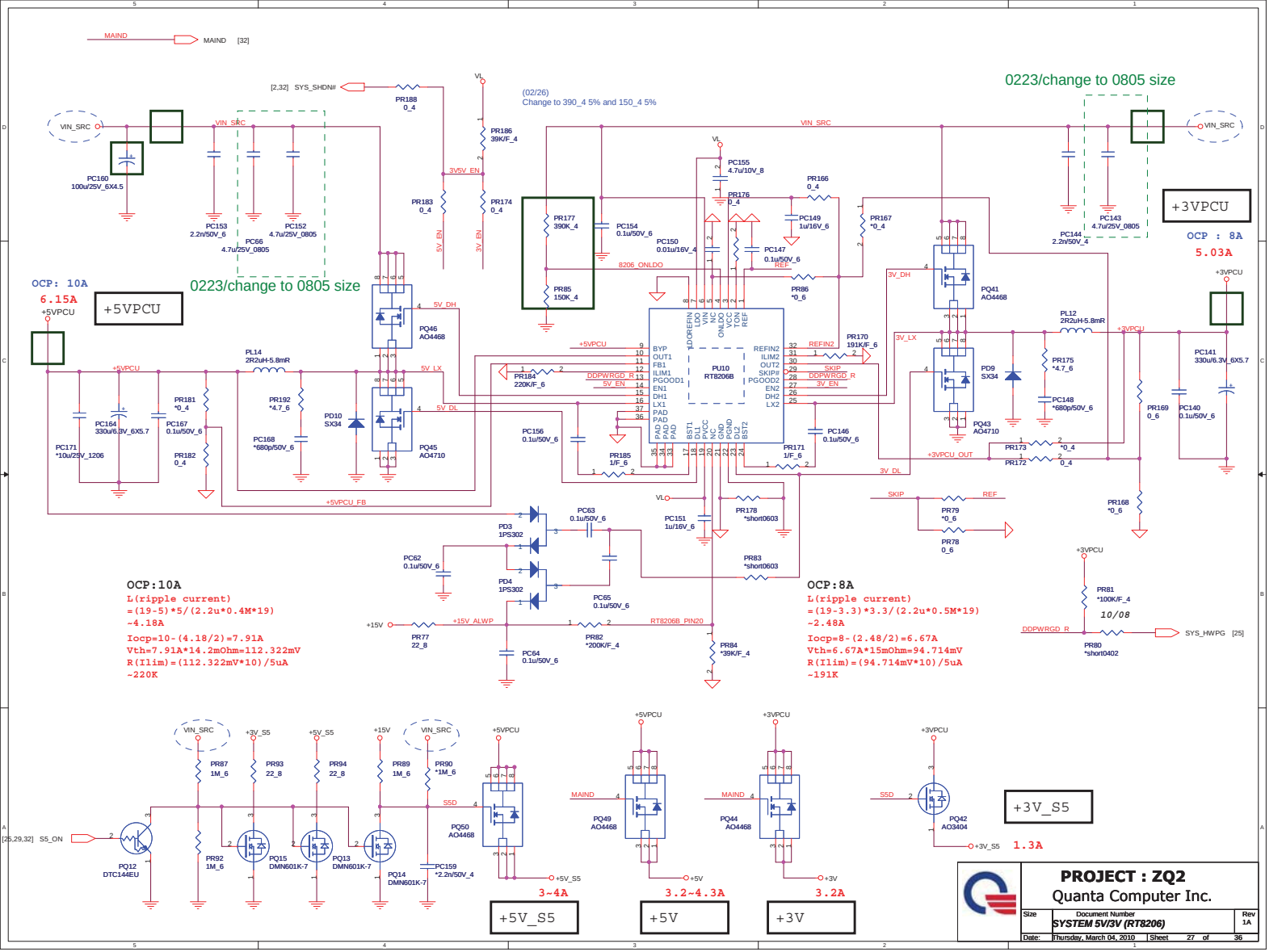
POWER-ON SWITCH (KBC)

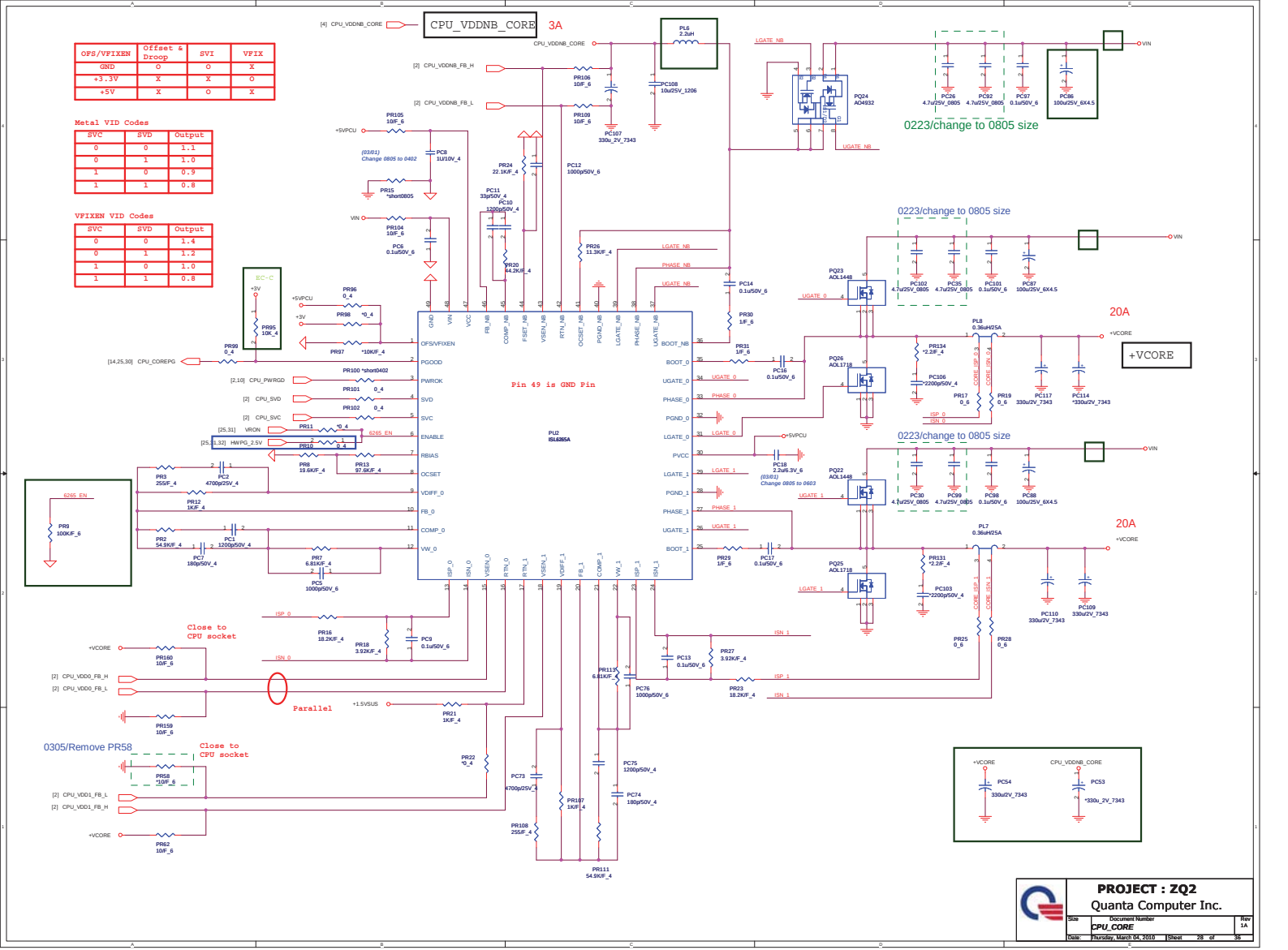


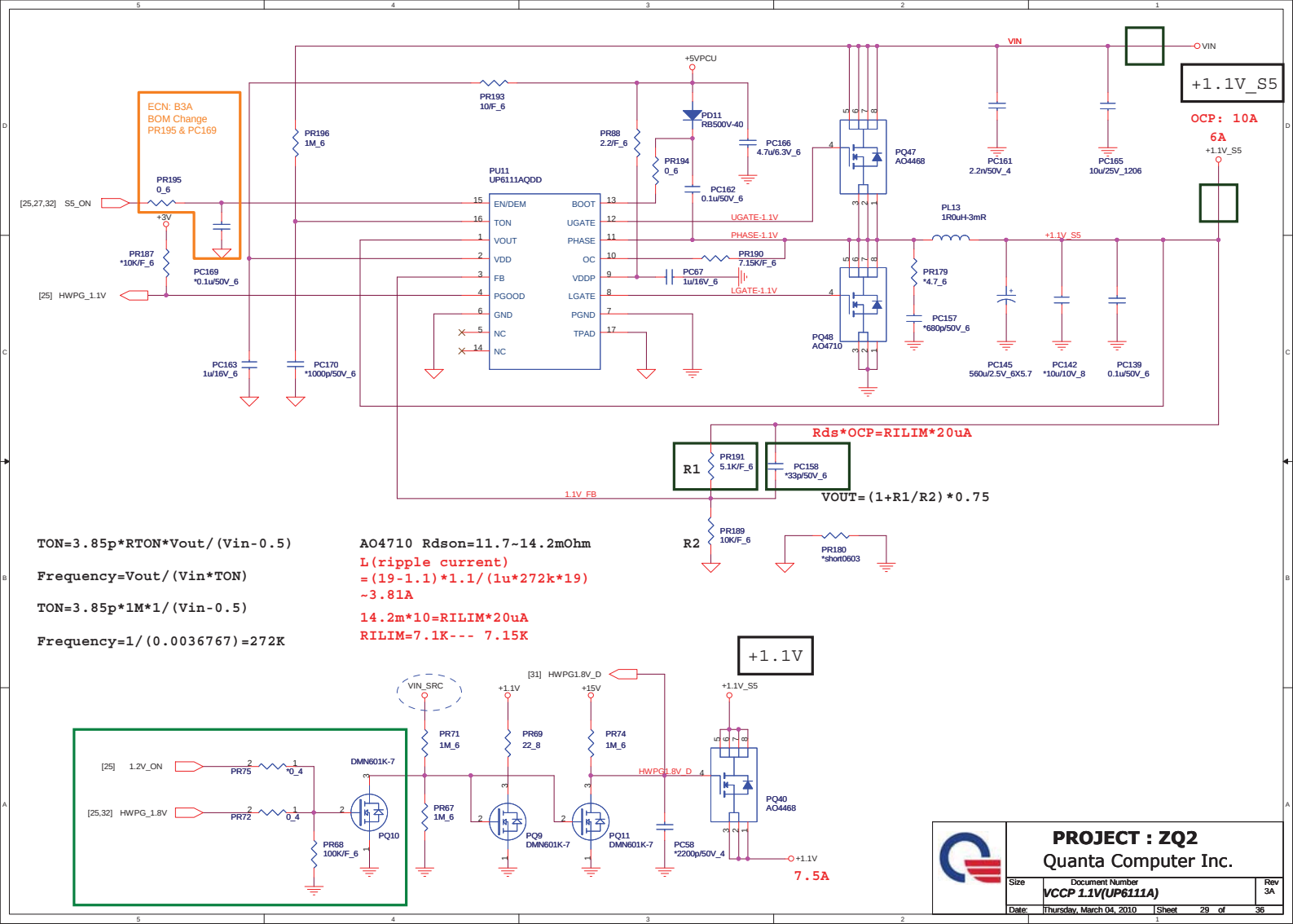
PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	3A
Date: Thursday, March 04, 2010	Sheet 25 of 36	

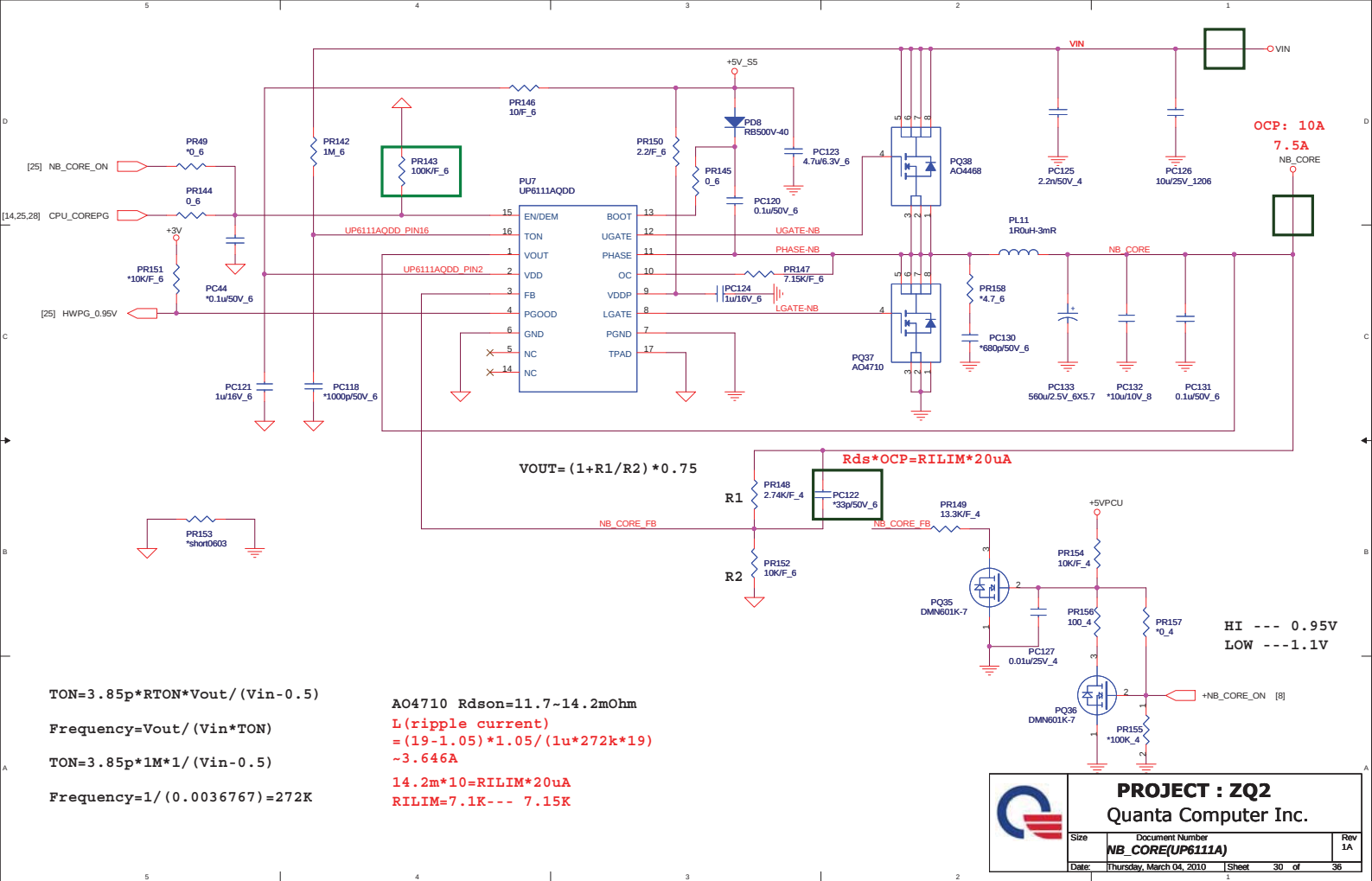

0223/EMI
ECN: B3A
ISN OK
BOM save two
POWER_JACK
PJ2
PL2
HI0805R800R-00_8
PL1
HI0805R800R-00_8
VA1
PD2
SBR1045SP5-13
PD1
SW1010CPT
PD6
SMAJ20A
VA2
PQ30
FDD6685
PR132
0.01/F_7520
VIN_SRC
CSIP_1
PQ17
FDD6685
PR115
33K_6
PR114
10K_6
PQ18
DMN601K-7
PR44
0_6
D/C#
[25]
PQ1
IMD2AT108
For EMI
PC91
2200p/50V_6
PC80
10u/25V_1206
PC21
*10u/25V_1210
PC20
*10u/25V_1210
PC19
*10u/25V_1210
PC81
*10u/25V_1210
PC27
1u/16V_6
PR42
10/F_6
PR41
10/F_6
PC29
0.1u/50V_6
PR37
4.7_6
PC22
1u/16V_6
ISL88731_VDDP
PD5
*RB500V-40
PC25
0.1u/50V_8
PR36
2.7_6
88731X
88731B_1
+3VPCU
PC28
0.1u/50V_6
PR35
100K/F_6
[25]
ACIN
MBDATA
MBCLK
PR130
49.9/F_6
DCIN
PC24
0.1u/50V_6
PR38
82.5K_6
88731ACSET
PC70
0.1u/50V_6
PC69
100p/50V_6
PL4
HI0805R800R-00_8
PL3
HI0805R800R-00_8
MBAT+
BAT-V
PJ1
Batt_Conn
TEMP_MBAT_C
PR1
100_4
TEMP_MBAT
[25]
PR14
100K/F_6
+3VPCU
PR4
*short0603
PC4
47p/50V_6
PC3
47p/50V_6
PR6
100_4
PR5
100_4
MBCLK
MBDATA
[25]
PU1
CM1293A-04SO
CH1
CH2
CH3
CH4
VN
VP
TEMP_MBAT_C
PC43
.22u/25V_6
2/8: ESD suggestion
Add ESD diode base on EC FAE suggestion
PU3
ISL88731A
NC
GND
GND
GND
GND
CSIP
CSSN
VCC
VDDP
VDDSMB
SDA
SCL
ACOK
DCIN
ACIN
VREF
ICOMP
NC
VCOMP
BOOT
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC
VBF
GND
ICM
NC
GND
PR40
2.21K/F_6
PC37
0.01u/50V_6
PC32
*1u/16V_6
PC33
0.01u/50V_6
PC34
*0.01u/50V_6
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
CSOP
CSON
PR32
10/F_6
PC23
0.1u/50V_6
PR33
10/F_6
PR34
*short0402
PR103
100_4
BAT-V
ICMNT
[25]
ISL88731 thermal pad
tie to Pin12
PQ21
AO4468
PQ20
AO4710
PL5
6.8uH
0.01_3720
PR110
PR117
*4.7_6
PC78
*680p/50V_6
PC72
2200p/50V_6
PC71
10u/25V_1206
PC77
10u/25V_1206
CSOP_1
BAT-V
VIN_SRC
PQ16
AOL1413
PC15
1U/25V_6
PR112
150K_6
VIN
PR116
39K_6
[25]
VIN_ON
PQ19
DMN601K-7
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
CHARGER (ISL88731)
Rev
3A
Date:
Thursday, March 04, 2010
Sheet
26
of
36


MAIND
MAIND [32]
[2,32] SYS_SHDN#
VL
PR188 0_4
(02/26)
Change to 390_4 5% and 150_4 5%
0223/change to 0805 size
VIN_SRC
PC160 100u/25V_6X4.5
PC153 2.2n/50V_6
PC66 4.7u/25V_0805
PC152 4.7u/25V_0805
PR186 39K/F_4
PR183 0_4
PR174 0_4
3V5V_EN
5V_EN
3V_EN
PR177 390K_4
PR85 150K_4
PC154 0.1u/50V_6
PC150 0.01u/16V_4
8206_ONLDO
PC155 4.7u/10V_8
PR176 0_4
PR166 0_4
PC149 1u/16V_6
PC147 0.1u/50V_6
REF
PR86 *0_6
PR167 *0_4
PC144 2.2n/50V_4
PC143 4.7u/25V_0805
+3VPCU
OCP : 8A
5.03A
OCP: 10A
6.15A
+5VPCU
+5VPCU
0223/change to 0805 size
5V_DH
PQ46 AO4468
5V_LX
5V_DL
PQ45 AO4710
PL14 2R2uH+-5.8mR
PR181 *0_4
PR182 0_4
PC164 330u/6.3V_6X5.7
PC167 0.1u/50V_6
PC171 *10u/25V_1206
PR192 *4.7_6
PR168 *680p/50V_6
PD10 SX34
PC156 0.1u/50V_6
PR184 220K/F_6
DDPWRGD_R
5V_EN
PR185 1/F_6
+5VPCU_FB
PU10 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
BST1
DL1
PVCC
GND
PGND
DL2
SST2
DORFIN
LDO
VIN
VCC
ONLDO
VCC
FDN
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR170 191K/F_6
REFIN2
SKIP
DDPWRGD_R
3V_EN
PC146 0.1u/50V_6
PR171 1/F_6
3V_DH
3V_LX
3V_DL
PQ41 AO4468
PQ43 AO4710
PD9 SX34
PL12 2R2uH+-5.8mR
PR175 *4.7_6
PC148 *680p/50V_6
PC141 330u/6.3V_6X5.7
PR169 0_6
PC140 0.1u/50V_6
+3VPCU_OUT
PR173 *0_4
PR172 0_4
PR168 *0_6
SKIP
REF
PR79 *0_6
PR78 0_6
PC63 0.1u/50V_6
PD3 1PS302
PD4 1PS302
PC62 0.1u/50V_6
PC65 0.1u/50V_6
PC64 0.1u/50V_6
PC151 1u/16V_6
PR178 *short0603
PR83 *short0603
+15V
+15V_ALWP
PR77 22_8
PR82 *200K/F_4
RT8206B_PIN20
PR84 *39K/F_4
PR81 *100K/F_4
10/08
DDPWRGD_R
PR80 *short0402
SYS_HWPG [25]
OCP:10A
L(ripple current)
=(19-5)*5/(2.2u*0.4M*19)
~4.18A
Iocp=10-(4.18/2)=7.91A
Vth=7.91A*14.2mOhm=112.322mV
R(Ilim)=(112.322mV*10)/5uA
~220K
OCP:8A
L(ripple current)
=(19-3.3)*3.3/(2.2u*0.5M*19)
~2.48A
Iocp=8-(2.48/2)=6.67A
Vth=6.67A*15mOhm=94.714mV
R(Ilim)=(94.714mV*10)/5uA
~191K
VIN_SRC
+3V_S5
+5V_S5
+15V
PR87 1M_6
PR93 22_8
PR94 22_8
PR89 1M_6
PR90 *1M_6
S5D
[25,29,32] S5_ON
PQ12 DTC144EU
PR92 1M_6
PQ15 DMN601K-7
PQ13 DMN601K-7
PQ14 DMN601K-7
PC159 *2.2n/50V_4
PQ50 AO4468
+5V_S5
3~4A
+5V_S5
MAIND
PQ49 AO4468
+5V
3.2~4.3A
+5V
PQ44 AO4468
+3V
3.2A
+3V
S5D
PQ42 AO3404
+3V_S5
1.3A
+3V_S5
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Thursday, March 04, 2010
Sheet 27 of 36

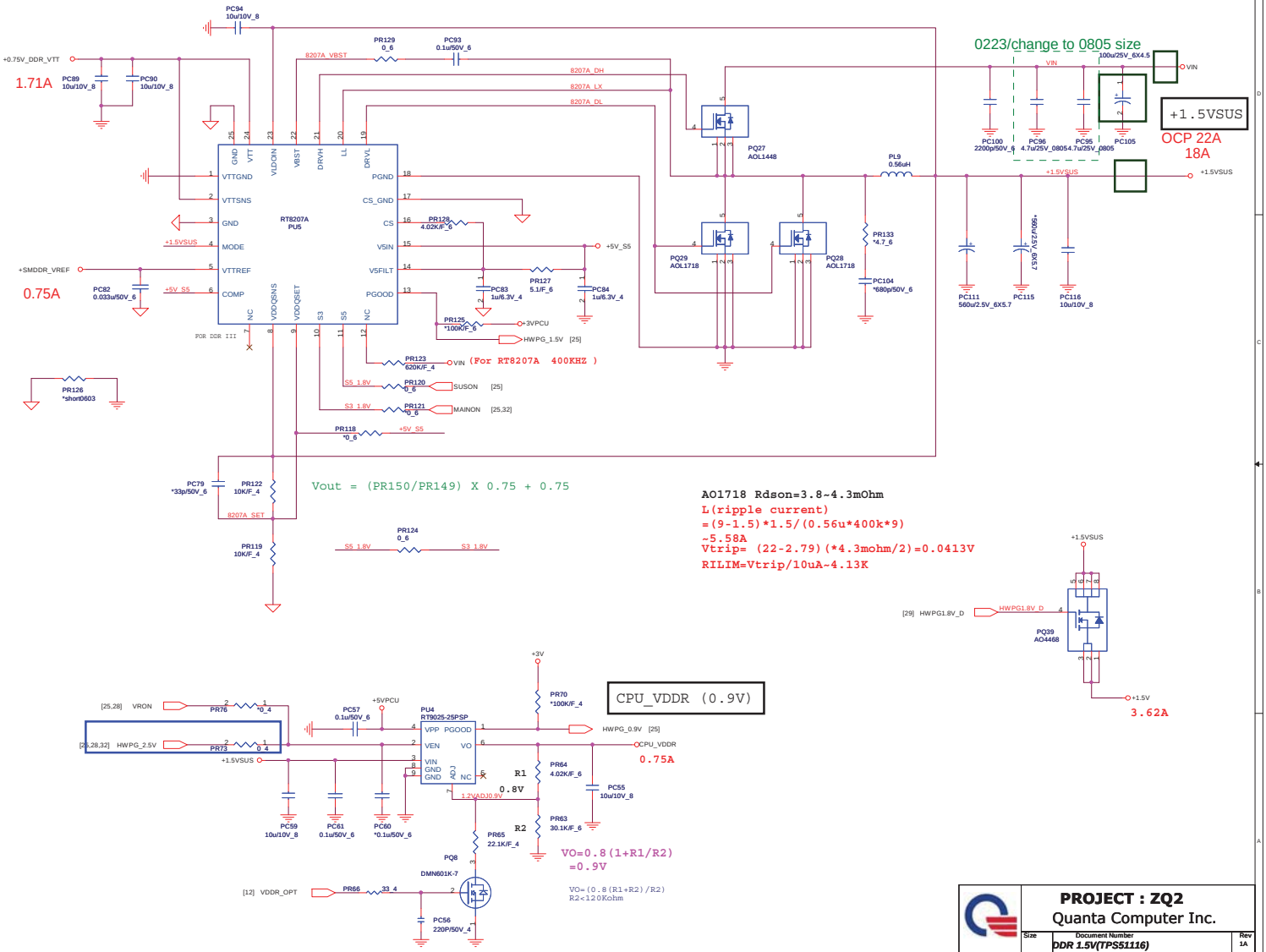

CPU_VDDNB_CORE
3A
OFS/VFIXEN | Offset & Droop | SVI | VFIX
GND | O | O | X
+3.3V | X | X | O
+5V | X | O | X
Metal VID Codes
SVC | SVD | Output
0 | 0 | 1.1
0 | 1 | 1.0
1 | 0 | 0.9
1 | 1 | 0.8
VFIXEN VID Codes
SVC | SVD | Output
0 | 0 | 1.4
0 | 1 | 1.2
1 | 0 | 1.0
1 | 1 | 0.8
0223/change to 0805 size
20A
+VCORE
Pin 49 is GND Pin
Close to CPU socket
Parallel
0305/Remove PR58
PROJECT : ZQ2
Quanta Computer Inc.
CPU_CORE
Thursday, March 04, 2010



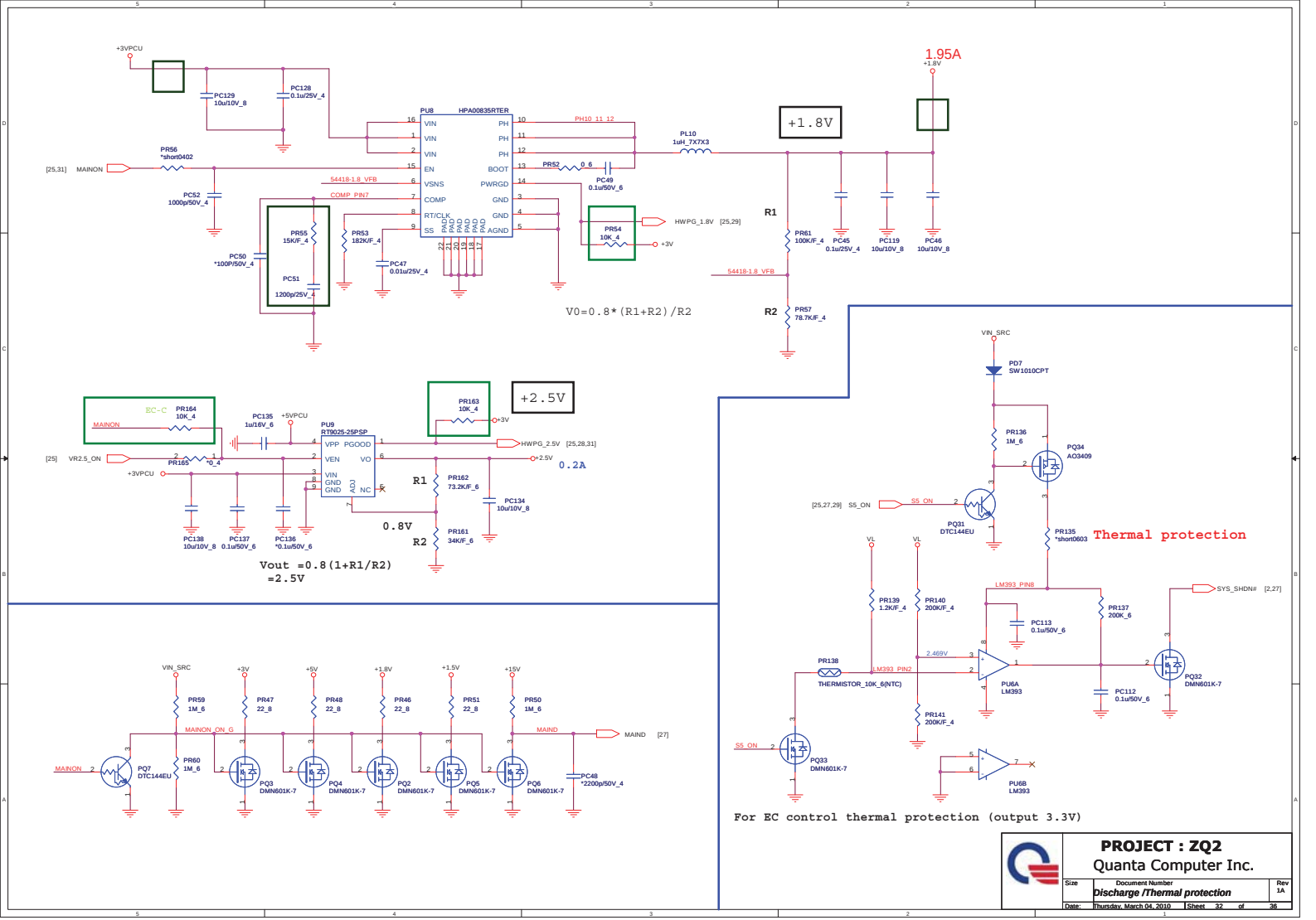
	PROJECT : ZQ2 Quanta Computer Inc.		
Size	Document Number *VCCP 1.1V(UP6111A)*		Rev 3A
Date: Thursday, March 04, 2010	Sheet 29 of 36		


VIN
+5V_S5
PR146 10/F_6
PD8 RB500V-40
PC123 4.7u/6.3V_6
PR150 2.2/F_6
PR145 0_6
PC120 0.1u/50V_6
PU7 UP6111AQDD
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-NB
PHASE-NB
LGATE-NB
PQ38 AO4468
PQ37 AO4710
PL11 1R0uH-3mR
NB_CORE
PR158 *4.7_6
PC130 *680p/50V_6
PC125 2.2n/50V_4
PC126 10u/25V_1206
PC133 560u/2.5V_6X5.7
PC132 *10u/10V_8
PC131 0.1u/50V_6
OCP: 10A
7.5A
[25] NB_CORE_ON
[14,25,28] CPU_COREPG
[25] HWPG_0.95V
+3V
PR49 *0_6
PR144 0_6
PR151 *10K/F_6
PC44 *0.1u/50V_6
PR142 1M_6
PR143 100K/F_6
PR147 7.15K/F_6
PC124 1u/16V_6
PC121 1u/16V_6
PC118 *1000p/50V_6
PR153 *short0603
VOUT=(1+R1/R2)*0.75
Rds*OCP=RILIM*20uA
R1
R2
PR148 2.74K/F_4
PC122 *33p/50V_6
PR152 10K/F_6
NB_CORE_FB
PR149 13.3K/F_4
+5VPCU
PR154 10K/F_4
PQ35 DMN601K-7
PC127 0.01u/25V_4
PR156 100_4
PR157 *0_4
PQ36 DMN601K-7
PR155 *100K_4
+NB_CORE_ON [8]
HI --- 0.95V
LOW ---1.1V
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
AO4710 Rdson=11.7~14.2mOhm
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A
14.2m*10=RILIM*20uA
RILIM=7.1K--- 7.15K
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
NB_CORE(UP6111A)
Rev 1A
Date: Thursday, March 04, 2010
Sheet 30 of 36

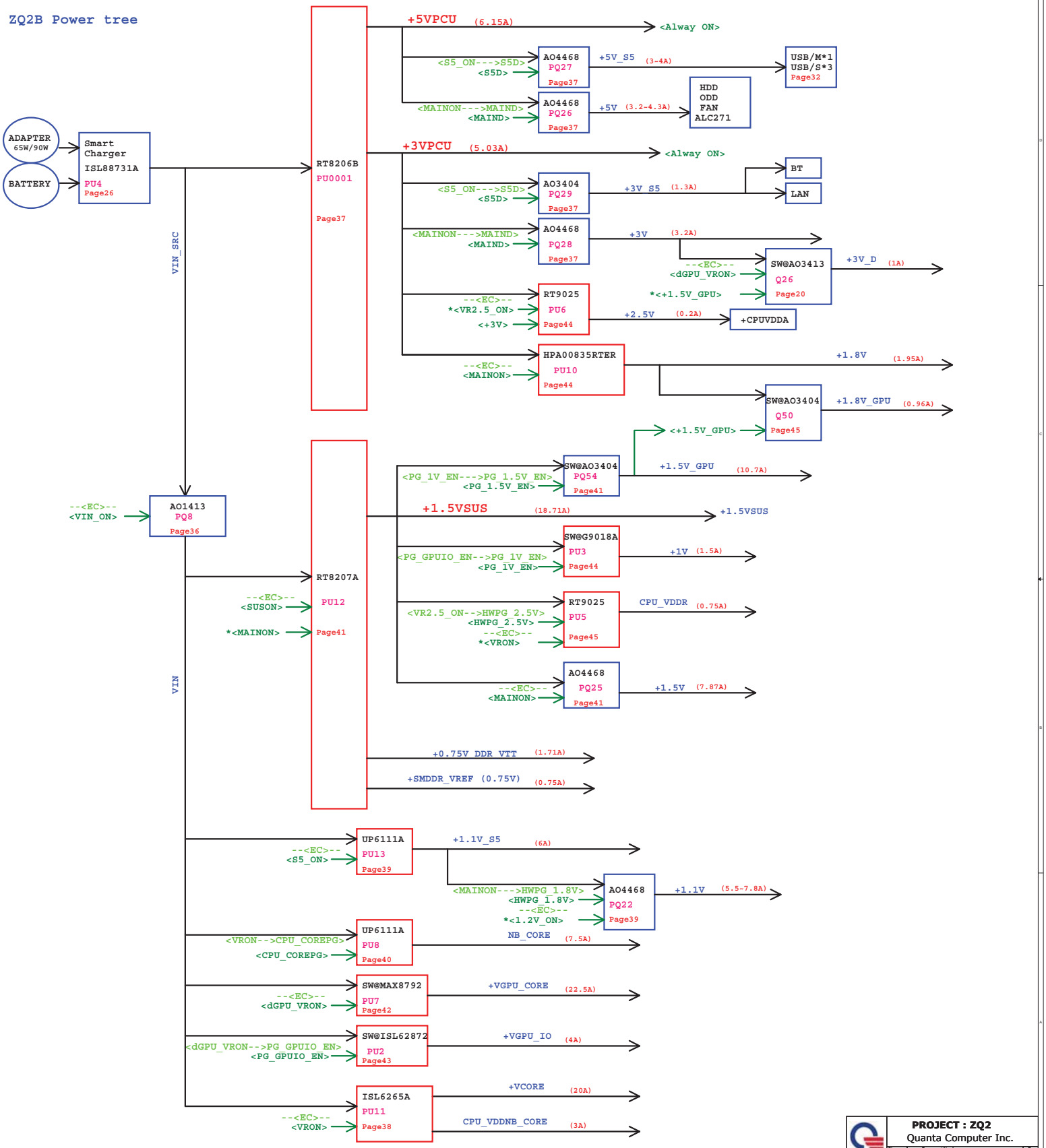
[PWM]



PROJECT : ZQ2	
Quanta Computer Inc.	
Size	Document Number: DDR 1.5V(TPS51116) — Rev 1A
Date: Thursday, March 04, 2010	Sheet 31 of 36


+3VPCU
PC129 10u/10V_8
PC128 0.1u/25V_4
PU8 HPA00835RTER
VIN
VIN
VIN
EN
VSNS
COMP
RT/CLK
SS
PH
PH
PH
BOOT
PWRGD
GND
GND
AGND
PAD
PH10_11_12
PL10 1uH_7X7X3
1.95A
+1.8V
+1.8V
PR56 *short0402
[25,31] MAINON
PR52 0_6
PC49 0.1u/50V_6
PC52 1000p/50V_4
54418-1.8_VFB
COMP_PIN7
PR55 15K/F_4
PR53 182K/F_4
PC47 0.01u/25V_4
PC50 *100P/50V_4
PC51 1200p/25V_4
PR54 10K_4
HWPG_1.8V [25,29]
+3V
R1
PR61 100K/F_4
PC45 0.1u/25V_4
PC119 10u/10V_8
PC46 10u/10V_8
54418-1.8_VFB
R2
PR57 78.7K/F_4
V0=0.8*(R1+R2)/R2
+2.5V
PR163 10K_4
+3V
EC-C
PR164 10K_4
MAINON
PC135 1u/16V_6
+5VPCU
PU9 RT9025-25PSP
VPP
VEN
VIN
GND
GND
PGOOD
VO
NC
ADJ
HWPG_2.5V [25,28,31]
+2.5V
0.2A
[25] VR2.5_ON
PR165 *0_4
+3VPCU
R1
PR162 73.2K/F_6
PC134 10u/10V_8
0.8V
R2
PR161 34K/F_6
PC138 10u/10V_8
PC137 0.1u/50V_6
PC136 *0.1u/50V_6
Vout =0.8(1+R1/R2)
=2.5V
VIN_SRC
PD7 SW1010CPT
PR136 1M_6
PQ34 AO3409
[25,27,29] S5_ON
S5_ON
PQ31 DTC144EU
PR135 *short0603
Thermal protection
VL
VL
PR139 1.2K/F_4
PR140 200K/F_4
LM393_PIN8
SYS_SHDN# [2,27]
PC113 0.1u/50V_6
PR137 200K_6
PR138
THERMISTOR_10K_6(NTC)
LM393_PIN2
2.469V
PU6A LM393
PQ32 DMN601K-7
PC112 0.1u/50V_6
PR141 200K/F_4
S5_ON
PQ33 DMN601K-7
PU6B LM393
For EC control thermal protection (output 3.3V)
VIN_SRC
+3V
+5V
+1.8V
+1.5V
+15V
PR59 1M_6
PR47 22_8
PR48 22_8
PR46 22_8
PR51 22_8
PR50 1M_6
MAINON_ON_G
MAIND
MAIND [27]
MAINON
PQ7 DTC144EU
PR60 1M_6
PQ3 DMN601K-7
PQ4 DMN601K-7
PQ2 DMN601K-7
PQ5 DMN601K-7
PQ6 DMN601K-7
PC48 *2200p/50V_4
PROJECT : ZQ2
Quanta Computer Inc.
Size
Document Number
Discharge /Thermal protection
Rev 1A
Date: Thursday, March 04, 2010
Sheet 32 of 36

ZQ2B Power tree

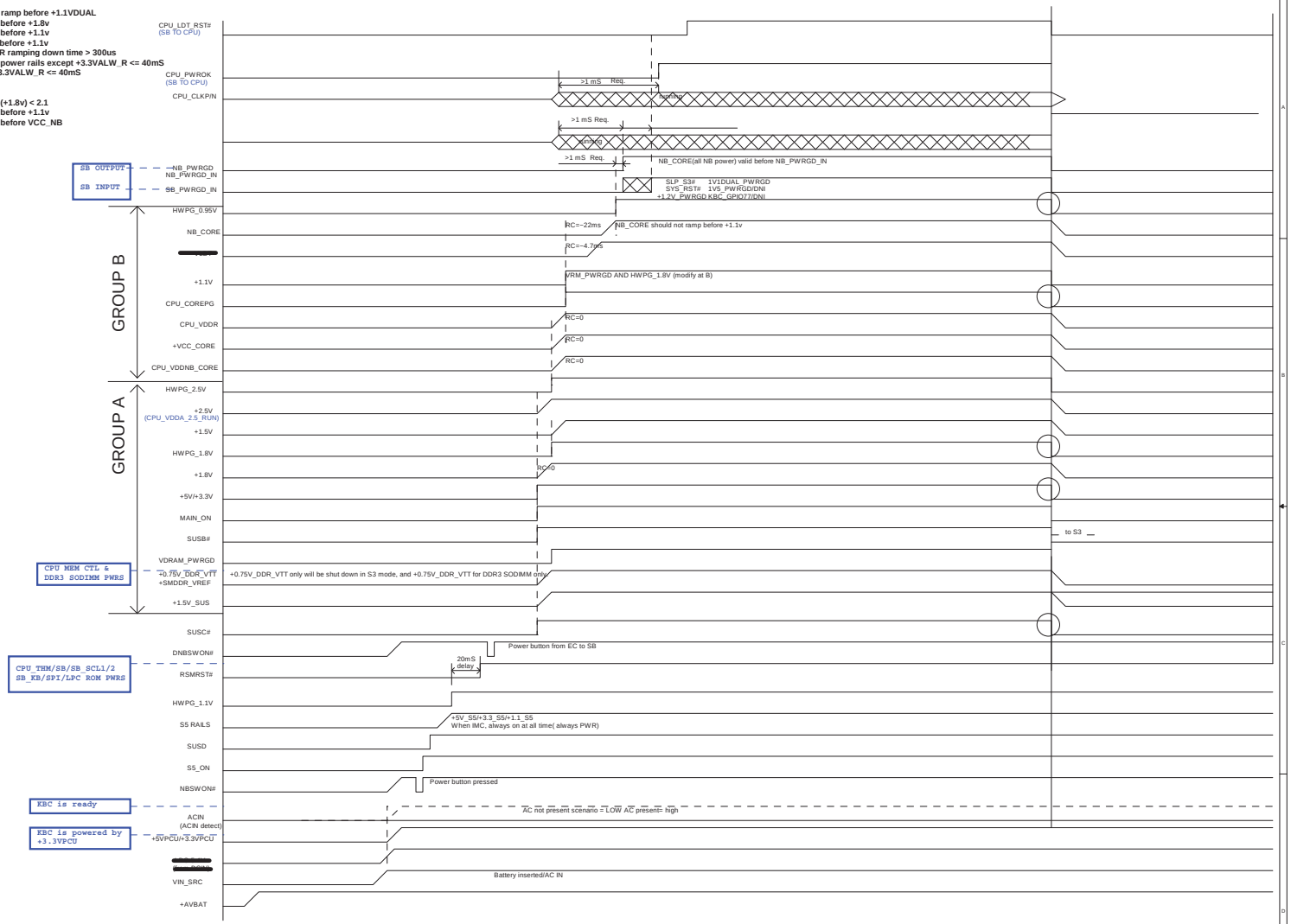


PROJECT : ZQ2
Quanta Computer Inc.
Size | Document Number: Power Tree | Rev 1A
Date: Thursday, March 04, 2010 | Sheet 33 of 38

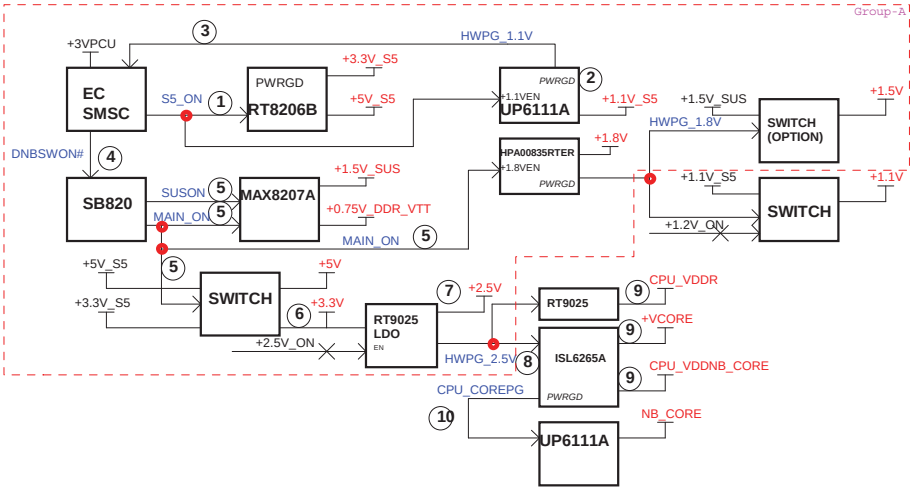
Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



	PROJECT : ZQ2 Quanta Computer Inc.		
Size	Document Number: *Power Squence Chart*		Rev 1A
Date: Thursday, March 04, 2010	Sheet 34 of 36		

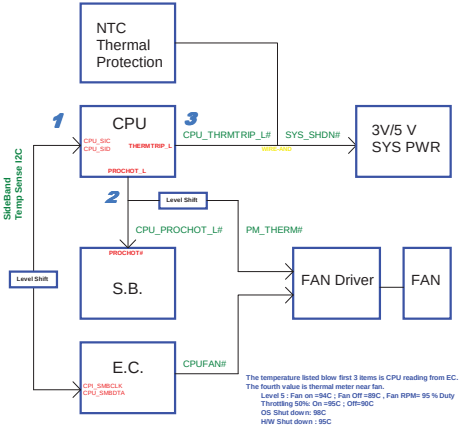


Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

H/W Thermal Follow Chart



POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	PWR ON SEQ and THERM POLICY	1A
Date: Thursday, March 04, 2010	Sheet 35 of 36	

CHANGE LIST

Model	REV	
ZQ2B MB	1A	A1A The First Release.
	3A	B3A Page 02 Q23 cahnge from FDV301V to BSS138. Becasue FDV301V EOL. B3A Page 10 Add off-page net of +BAT for Green Adpapter. It can decrease drop voltage. R289 change value to 12K beucase charge current. B3A Page 15 Change R11's footprint to short pad. BOM cancel R11. B3A Page 22 Reserve D25 and add R401. It can cancel D1's Vf while GRN-ADP. B3A Page 25 Del D15 and R228. And change PWR source of ADP_ON. All for decrease drop voltage. And un-stuff Q17 in oreder to EC suggestion. B3A Page 25 BOM change for fine-tune. Stuff R226 and BOM unstuff C292, R230 and R233. B3A Page 26 BOM save PC41 and PC42. B3A Page 29 BOM change for Pr195 and PC169 in order to AMD power up timing requirement.

MODEL	ZQ2B	
	FROM	To
	X	1A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	3A
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	
	1A	

DOC NO.						
	PROJECT MODEL :	ZQ2B	APPROVED BY:		DATE:	2010/03/05
	PART NUMBER:		DRAWING BY:		REVISON:	1A

PROJECT : ZQ2
Quanta Computer Inc.

Size	Document Number	Rev
	Change list	1A
Date: Thursday, March 04, 2010	Sheet 36 of 36	