

Compal Confidential

KBLG0/NBLG0 Schematics Document

AMD Puma (JV40-PU) : Griffin Processor with RS780MN/SB700/M92-M2 XT
Tigris (JV40-TR) : Caspian Processor with RS880M/SB710/M92-M2 XT

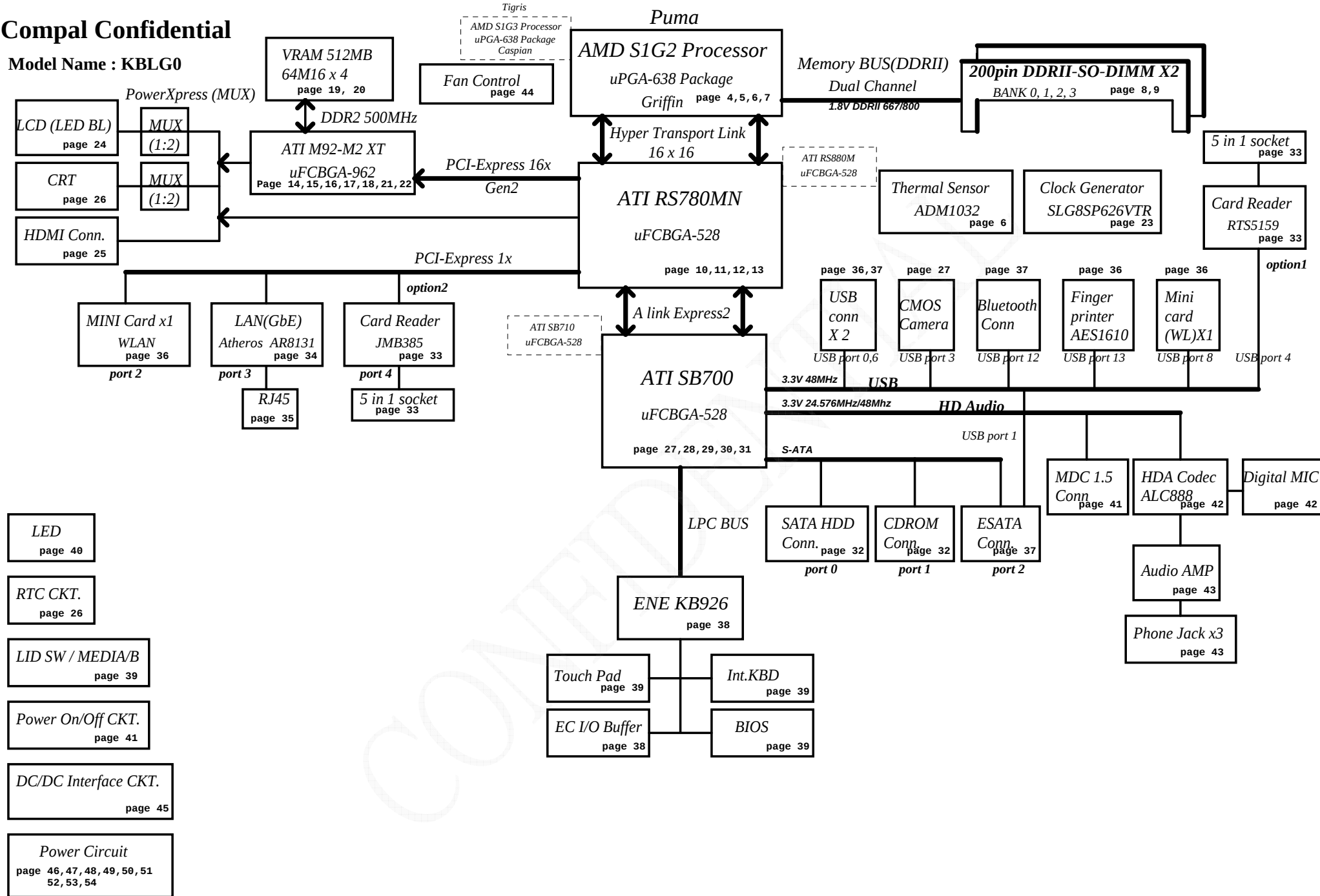
2009-03-11

REV:1.0

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Model Name : KBLG0



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE_0	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_1	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+CPU_CORE_NB	Voltage for On-die Northbridge of CPU(0.8-1.1V)	DN	OFF	OFF
+0.9V	0.9V switched power rail for DDR terminator	ON	ON	OFF
+1.1VS	1.1V switched power rail for NB VDDC & VGA	ON	OFF	OFF
+1.2V_HT	1.2V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VS	1.5V power rail for PCIE Card	ON	OFF	OFF
+1.8V	1.8V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
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EC SM Bus1 address

Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (CPU)	1001 100X b	98H
			GMT G781-1 (GPU)	1001 101X b	9AH
			SB-Temp Sensor		9CH

SB700

SM Bus 0 address

Device	Address	HEX	Device	Address
Clock Generator (SILEGO SLG8SP626)	1101 001Xb	D2	New card	
DDR DIMM1	1001 000Xb	90		
DDR DIMM2	1001 010Xb	94		
Mini card				

EC SM Bus2 address

SB700

SM Bus 1 address

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Discrete	VGA@
UMA	UMA@
M92-M2 XT	M92@
VRAM STRAP	VRAM@
LAN 8121	8121@
LAN 8131	8131@
HDT debug	HDT@
JMB385 CR	JMB385@
RTS5159 CR	RTS5159@
FOR PUMA	PUMA@
FOR TIGRIS	TIGRIS@
FOR TEST	UB@

	SB700	SB700	RS780MN	DISPLAY OUTPUT
	PX_GPIO0	PX_GPIO1	PX_GPIO2	
Function Description	dGPU_Reset	dGPU_PWR_Enable	PX Mode Switch	
IGP only mode	X	X	X	
PowerXpress mode	H : Enable	H : Enable	L : IGPU(DC) / H : dGPU(AC)	LVDS / CRT

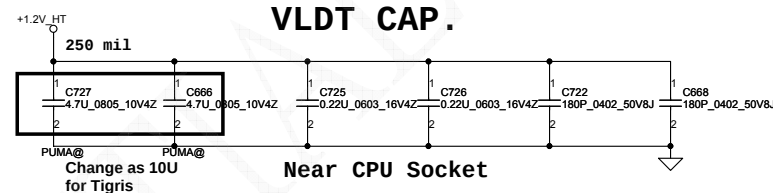
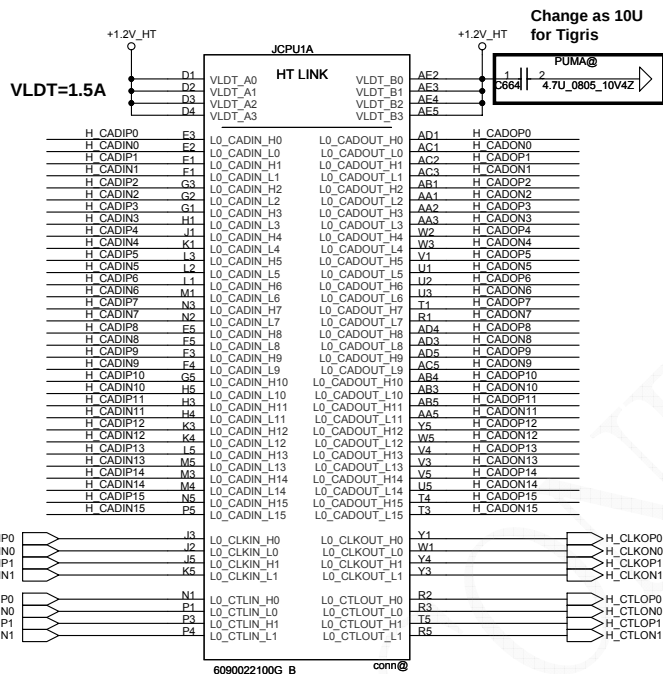
	KB926					
	PX_GPIO1	PX_GPIO2	PX_+3VS	PX_+1.8VS	PX_+VGA_CORE	PX_GPIO2_NB
Function Description	Enable +1.1VS_PX	PX MODE SWITCH	Enable +3VS_DELAY	Enable +1.8VS_PX	Enable +VGA_CORE	Trigger from SB
IGP only mode	X	X	X	X	X	X
PowerXpress mode	H : Enable	Reserved	H : Enable	H : Enable	H : Enable	Reserved

	KB926	
	PX_GPIO1_SB	
Function Description	Trigger from SB to Enable (PX_GPIO1/PX_+3VS/PX_+1.8VS/PX_+VGA_CORE)	
IGP only mode	X	
PowerXpress mode	H : Enable	

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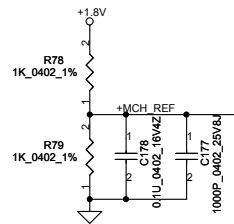
10 H_CADIP[0..15] H_CADIP[0..15]
10 H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] 10
H_CADON[0..15] H_CADON[0..15] 10

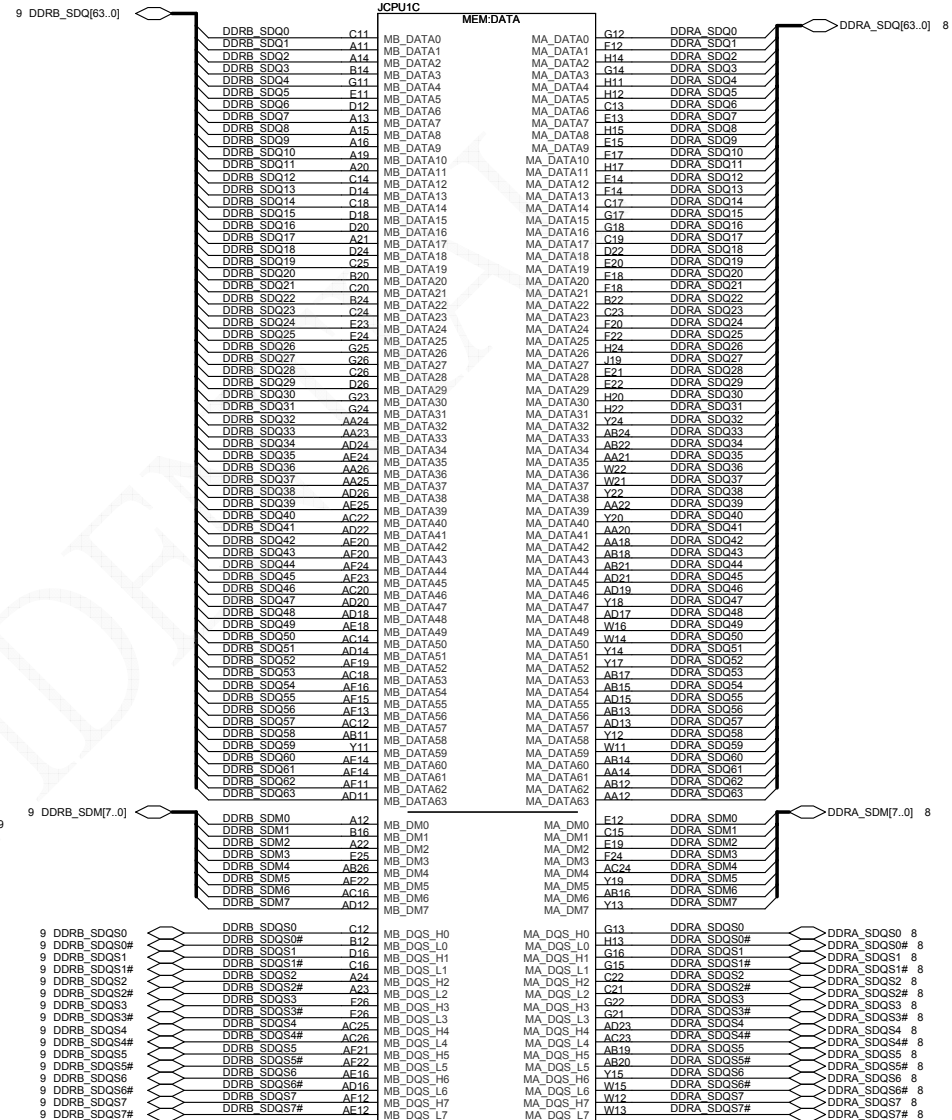
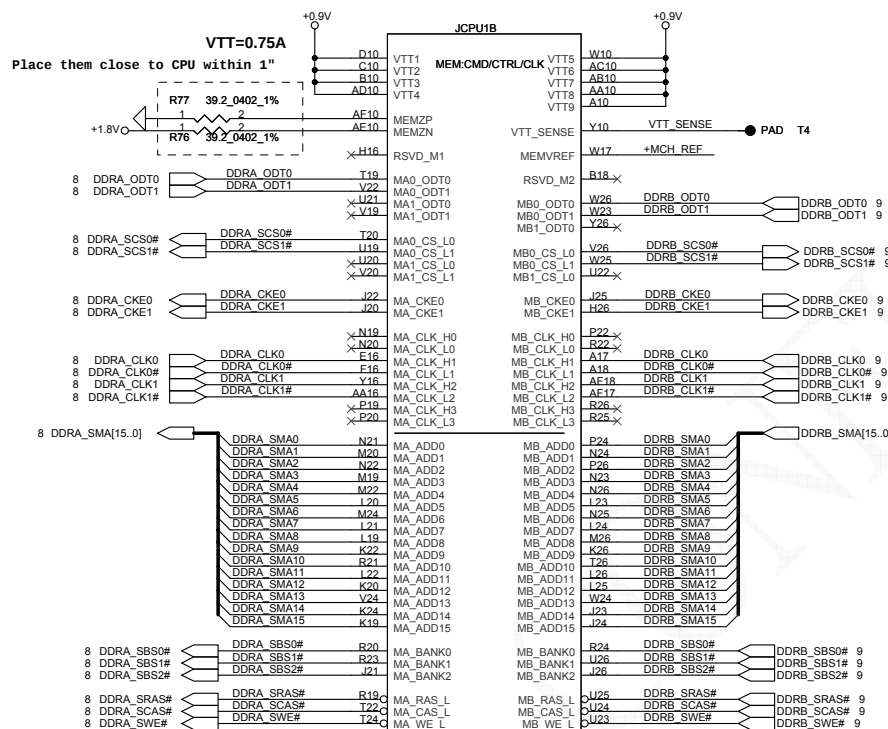
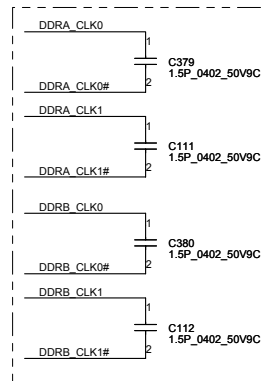


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Processor DDR2 Memory Interface

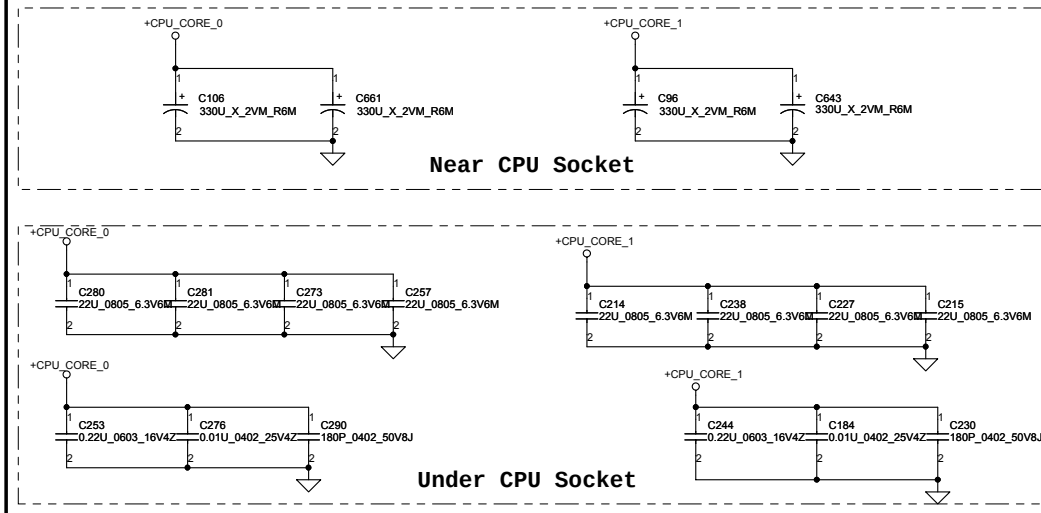


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

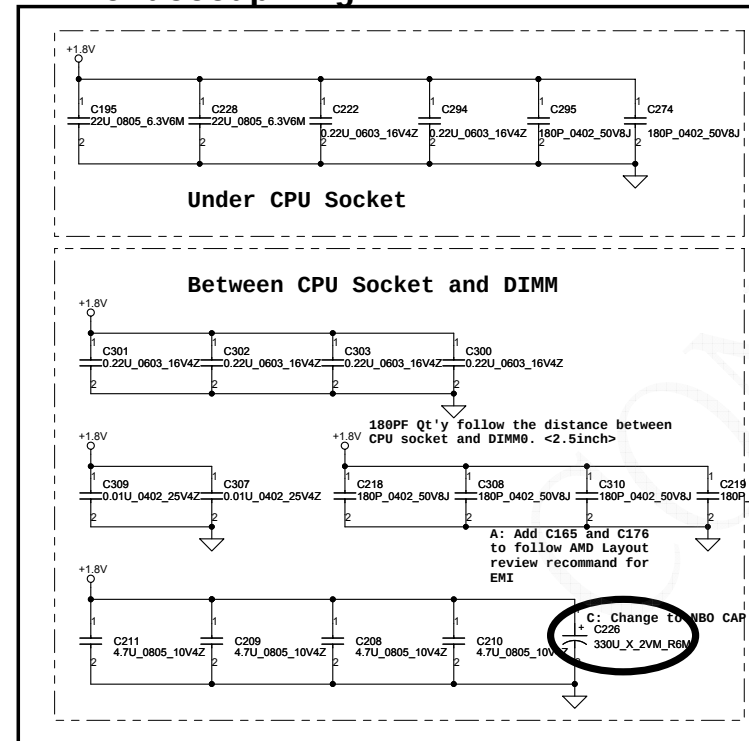


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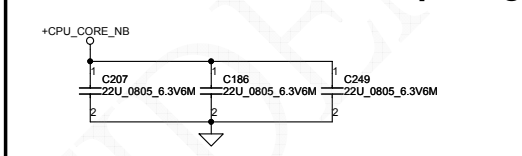
VDD(+CPU_CORE) decoupling.



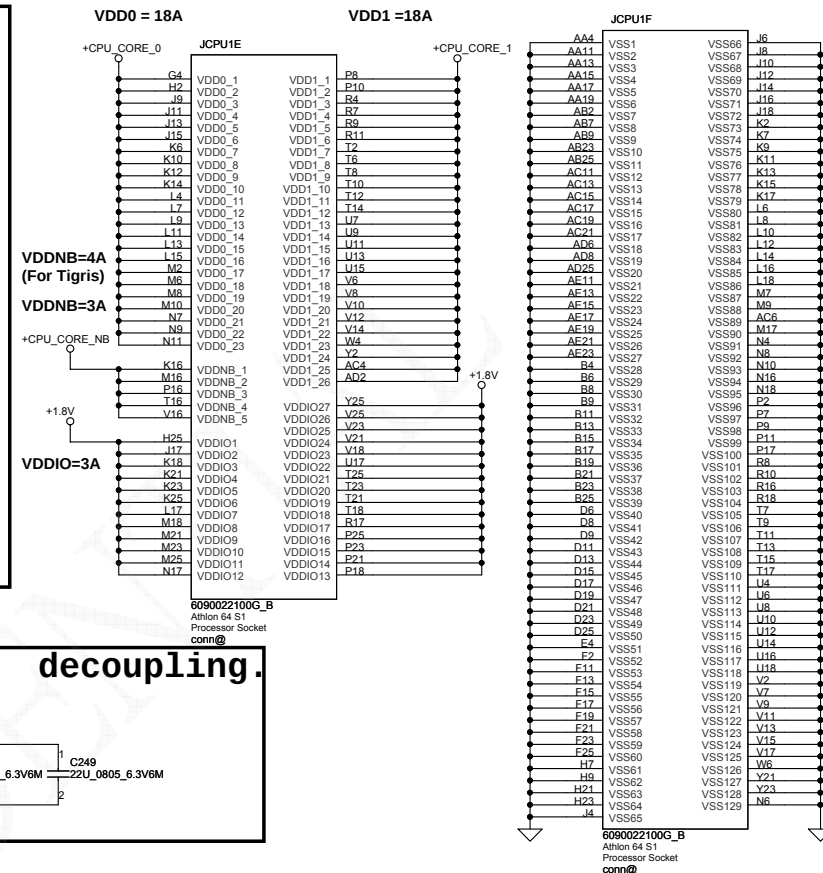
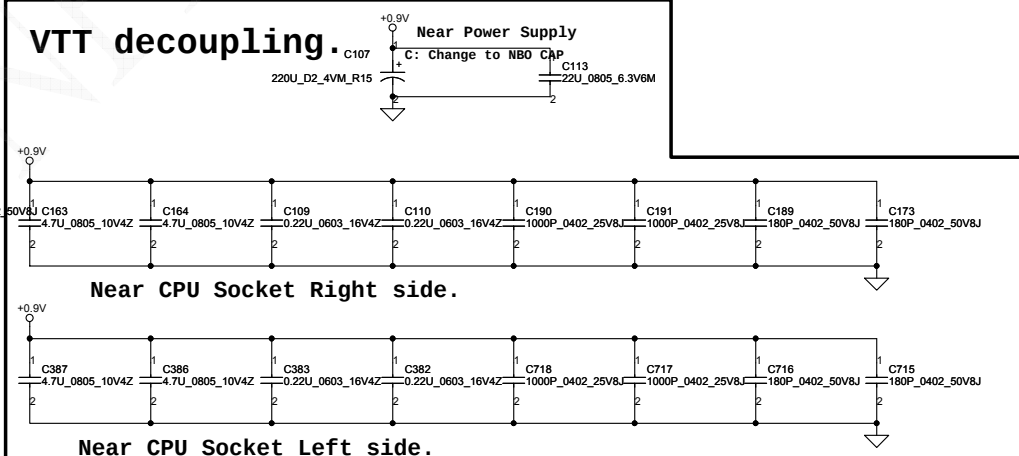
VDDIO decoupling.



+CPU_CORE_NB decoupling.



VTT decoupling.



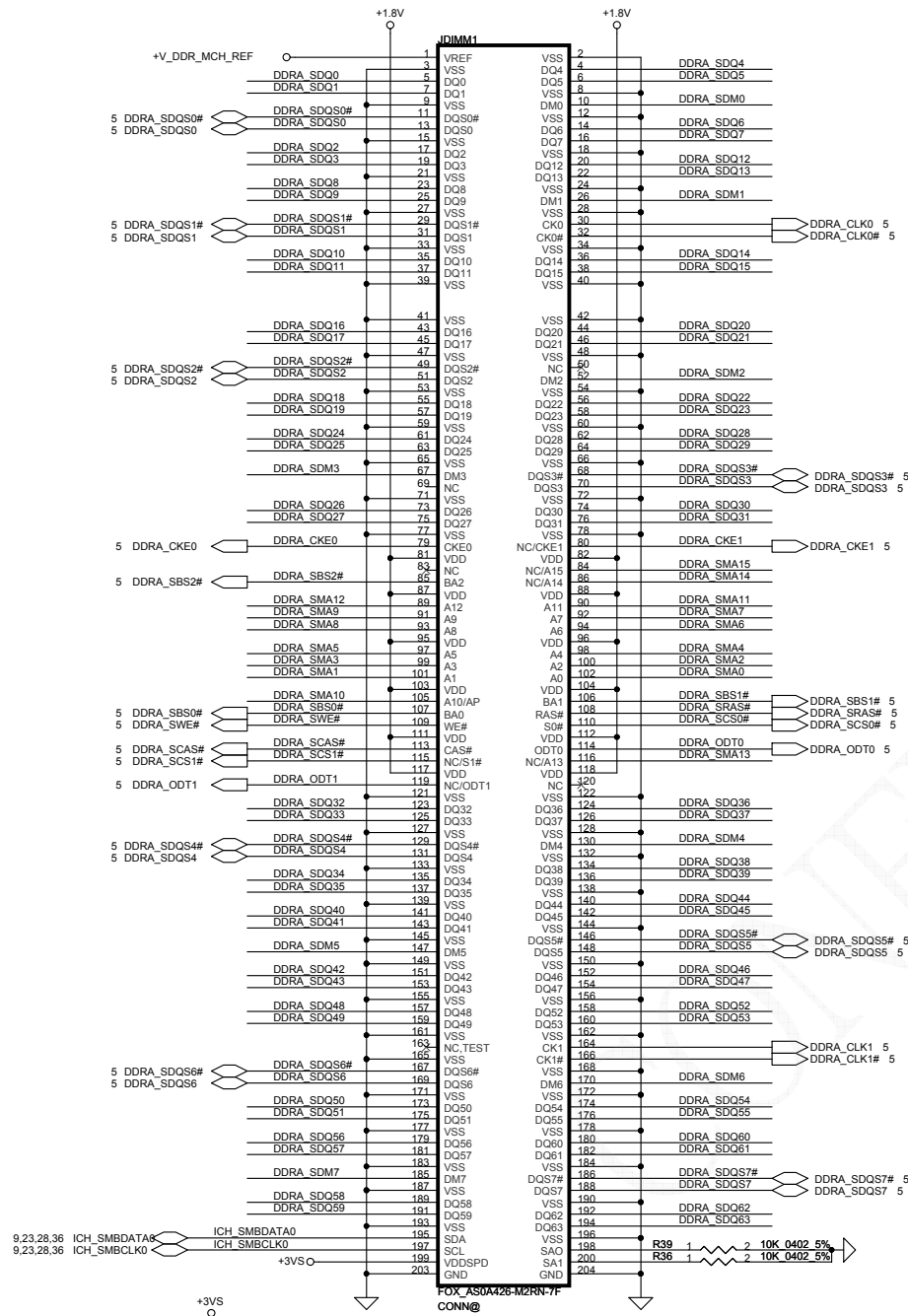
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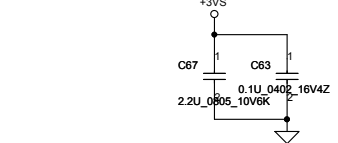
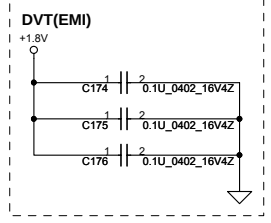
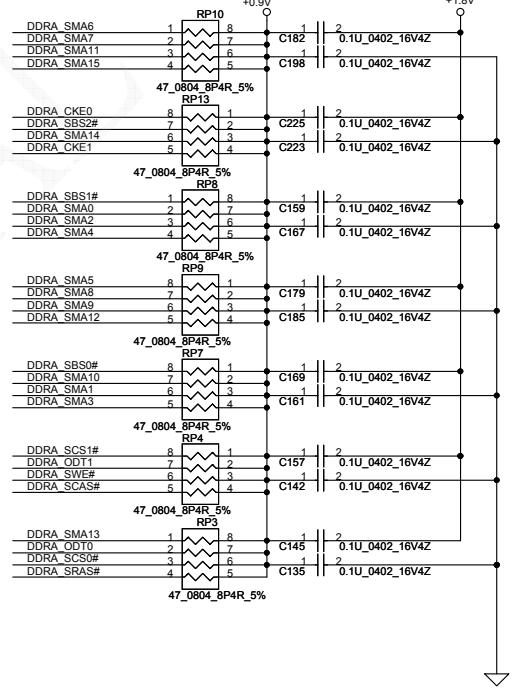
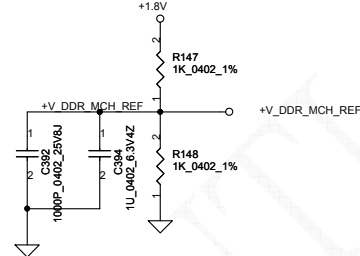
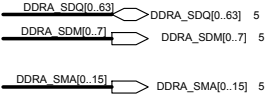
SCHEMATIC A4921P

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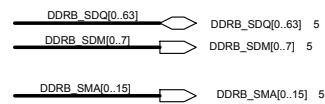
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DIMM1 REV H:5.2mm (BOT)



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DIMM2 REV H:9.2mm (BOT)

14 PCIE_GTX_C_MRX_P[0..15] PCIE GTX C MRX P[0..15]
14 PCIE_GTX_C_MRX_N[0..15] PCIE GTX C MRX N[0..15]

PCIE_MTX_C_GRX_P[0..15] PCIE_MTX_C_GRX_P[0..15] 14
PCIE_MTX_C_GRX_N[0..15] PCIE_MTX_C_GRX_N[0..15] 14

PCIE_MTX_GRX_N[0..3] PCIE_MTX_GRX_N[0..3] 25
PCIE_MTX_GRX_P[0..3] PCIE_MTX_GRX_P[0..3] 25

PCIE GTX C MRX P0 D4
PCIE GTX C MRX N0 C4
PCIE GTX C MRX N1 A3
PCIE GTX C MRX P1 B3
PCIE GTX C MRX P2 C2
PCIE GTX C MRX N2 C1
PCIE GTX C MRX P3 F3
PCIE GTX C MRX N3 F6
PCIE GTX C MRX P4 G5
PCIE GTX C MRX N4 G6
PCIE GTX C MRX P5 H6
PCIE GTX C MRX N5 H6
PCIE GTX C MRX N6 I J6
PCIE GTX C MRX P6 I J5
PCIE GTX C MRX P7 J7
PCIE GTX C MRX N7 J8
PCIE GTX C MRX P8 I J5
PCIE GTX C MRX N8 I J6
PCIE GTX C MRX P9 M8
PCIE GTX C MRX N9 L8
PCIE GTX C MRX P10 P7
PCIE GTX C MRX N10 M7
PCIE GTX C MRX P11 P5
PCIE GTX C MRX N11 M6
PCIE GTX C MRX P12 R8
PCIE GTX C MRX N12 P8
PCIE GTX C MRX P13 R6
PCIE GTX C MRX N13 R6
PCIE GTX C MRX P14 P4
PCIE GTX C MRX N14 P3
PCIE GTX C MRX P15 T4
PCIE GTX C MRX N15 T3

U38
PART 2 OF 6
PCIE I/F GFX
GFX_RX0P
GFX_RX0N
GFX_RX1P
GFX_RX1N
GFX_RX2P
GFX_RX2N
GFX_RX3P
GFX_RX3N
GFX_RX4P
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GFX_RX12N
GFX_RX13P
GFX_RX13N
GFX_RX14P
GFX_RX14N
GFX_RX15P
GFX_RX15N

A5 PCIE_MTX_GRX_P0
B5 PCIE_MTX_GRX_P1
C46 PCIE_MTX_GRX_P2
B4 PCIE_MTX_GRX_N1
C3 PCIE_MTX_GRX_P2
B2 PCIE_MTX_GRX_N2
D1 PCIE_MTX_GRX_P3
D2 PCIE_MTX_GRX_N3
E2 PCIE_MTX_GRX_P4
E1 PCIE_MTX_GRX_N4
F4 PCIE_MTX_GRX_P5
F3 PCIE_MTX_GRX_N5
F1 PCIE_MTX_GRX_P6
F2 PCIE_MTX_GRX_N6
H4 PCIE_MTX_GRX_P7
H3 PCIE_MTX_GRX_N7
H1 PCIE_MTX_GRX_P8
H2 PCIE_MTX_GRX_N8
J2 PCIE_MTX_GRX_P9
J1 PCIE_MTX_GRX_N9
K4 PCIE_MTX_GRX_P10
K3 PCIE_MTX_GRX_N10
K1 PCIE_MTX_GRX_P11
K2 PCIE_MTX_GRX_N11
M4 PCIE_MTX_GRX_P12
M3 PCIE_MTX_GRX_N12
M1 PCIE_MTX_GRX_P13
M2 PCIE_MTX_GRX_N13
N2 PCIE_MTX_GRX_P14
N1 PCIE_MTX_GRX_N14
P1 PCIE_MTX_GRX_P15
P2 PCIE_MTX_GRX_N15

C647 1 2 VGA@0.1U_0402_16V7K
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C620 1 2 VGA@0.1U_0402_16V7K
C624 1 2 VGA@0.1U_0402_16V7K
C621 1 2 VGA@0.1U_0402_16V7K
C619 1 2 VGA@0.1U_0402_16V7K

PCIE_MTX_C_GRX_P0
PCIE_MTX_C_GRX_N0
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DVT
New Card
WLAN
GLAN
Card Reader

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4 H_CADON[0..15] H_CADON[0..15]
4 H_CADIP[0..15] H_CADIP[0..15]
4 H_CADIN[0..15] H_CADIN[0..15]

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AE2 GPP_RX1P
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U6 GPP_RX3N
U7 GPP_RX4P
U8 GPP_RX4N
U9 GPP_RX5P
U10 GPP_RX5N

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AB4 GPP_RX1P
AB3 GPP_RX1N
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AA1 PCIE_ITX_PRX_N2
Y1 PCIE_ITX_PRX_P3
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Y4 PCIE_ITX_PRX_P4
Y3 PCIE_ITX_PRX_N4

C617 1 2 0.1U_0402_16V7K
C618 1 2 0.1U_0402_16V7K
C614 1 2 0.1U_0402_16V7K
C613 1 2 0.1U_0402_16V7K
C46 1 2 0.1U_0402_16V7K
C42 1 2 0.1U_0402_16V7K

PCIE_ITX_C_PRX_P2
PCIE_ITX_C_PRX_N2
PCIE_ITX_C_PRX_P3
PCIE_ITX_C_PRX_N3
PCIE_ITX_C_PRX_P4
PCIE_ITX_C_PRX_N4

4 H_CADOP[0..15] H_CADOP[0..15]
4 H_CADON[0..15] H_CADON[0..15]
4 H_CADIP[0..15] H_CADIP[0..15]
4 H_CADIN[0..15] H_CADIN[0..15]

4 H_CADOP[0..15] H_CADOP[0..15]
4 H_CADON[0..15] H_CADON[0..15]
4 H_CADIP[0..15] H_CADIP[0..15]
4 H_CADIN[0..15] H_CADIN[0..15]

AA8 SB_RX0P
Y8 SB_RX0N
AA7 SB_RX1P
Y7 SB_RX1N
AA5 SB_RX2P
AA6 SB_RX2N
W5 SB_RX3P
Y6 SB_RX3N

PCIE I/F SB
SB_RX0P
SB_RX0N
SB_RX1P
SB_RX1N
SB_RX2P
SB_RX2N
SB_RX3P
SB_RX3N

AD7 SB_TX0P_C
AE7 SB_TX0N_C
AE6 SB_TX1P_C
AD6 SB_TX1N_C
AB6 SB_TX2P_C
AC6 SB_TX2N_C
AD5 SB_TX3P_C
AE5 SB_TX3N_C

C615 1 2 0.1U_0402_16V7K
C609 1 2 0.1U_0402_16V7K
C38 1 2 0.1U_0402_16V7K
C33 1 2 0.1U_0402_16V7K
C37 1 2 0.1U_0402_16V7K
C32 1 2 0.1U_0402_16V7K
C610 1 2 0.1U_0402_16V7K
C616 1 2 0.1U_0402_16V7K

SB_TX0P
SB_TX0N
SB_TX1P
SB_TX1N
SB_TX2P
SB_TX2N
SB_TX3P
SB_TX3N

AC8 R32 1 2 1.27K_0402_1%
AB8 R267 1 2 2K_0402_1%

PCIE_CALR(PCE_BCALR)
PCIE_CALRN(PCE_BCALRN)

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

DP0
DP1

RS780M_FCBGA528

RS780M Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

DP0
DP1

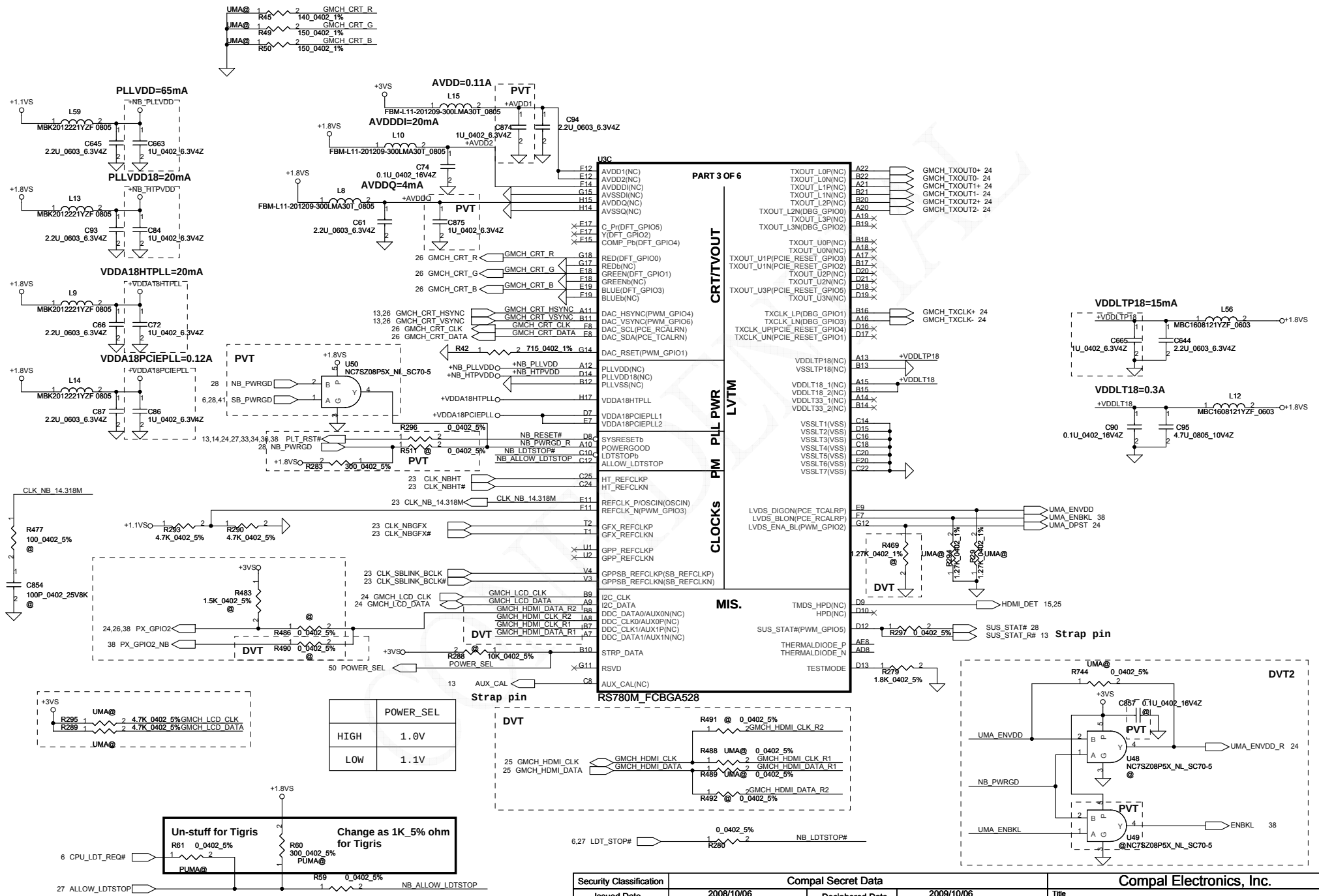
DP0
DP1

DP0
DP1

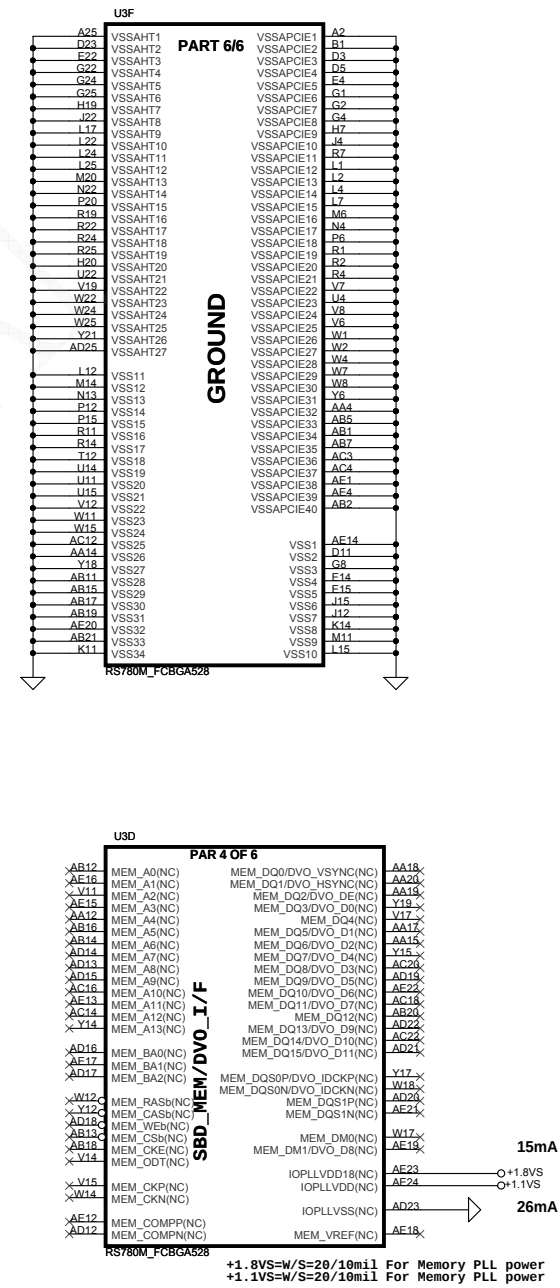
DP0
DP1

DP0
DP1

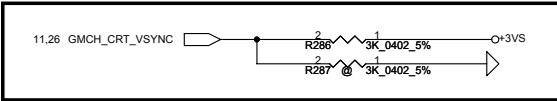
For RS780M A13
RED: Connected to GND through two separate 140ohm 1% resistor



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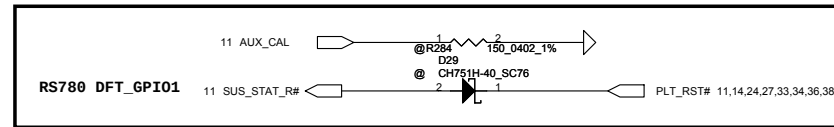


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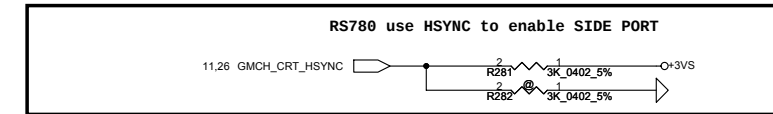
DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



RS780 use HSYNC to enable SIDE PORT

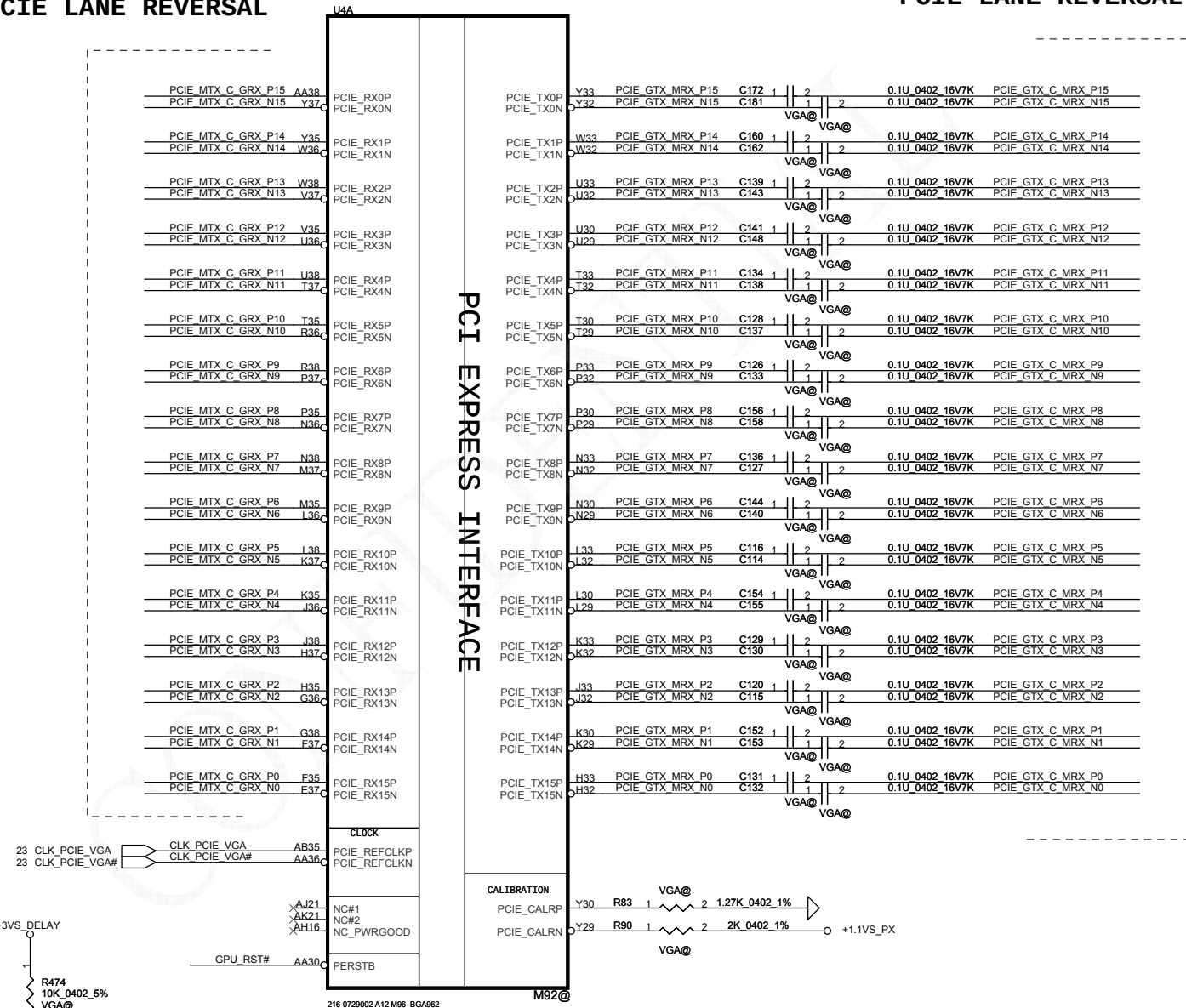
RS740/RS780: Enables Side port memory (RS780 use HSYNC#)
0. Enable (RS780)
1 : Disable(RS780)

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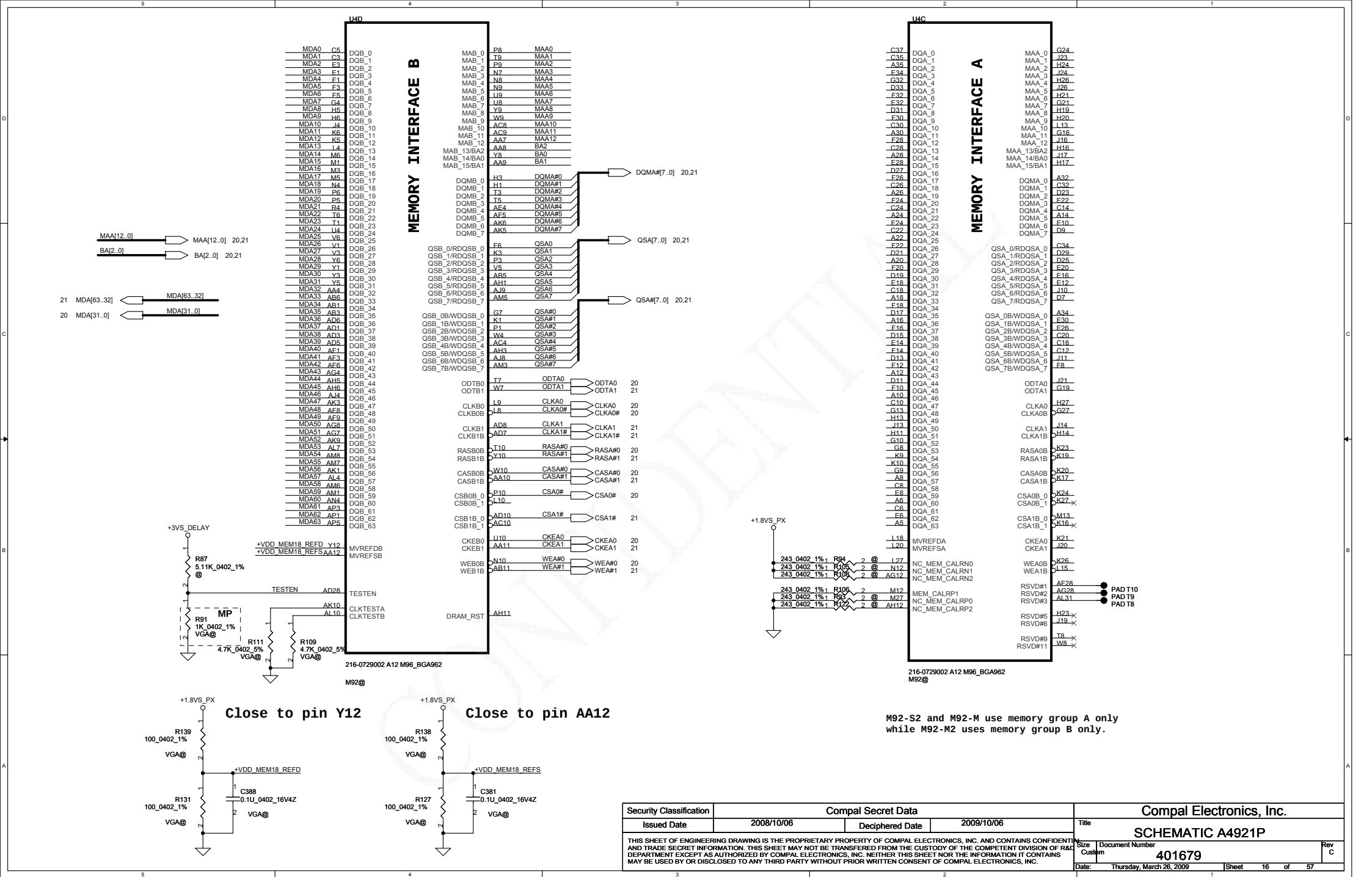
10 PCIE_GTX_C_MRX_P[0..15] < PCIE GTX C MRX P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] < PCIE GTX C MRX N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] < PCIE MTX C GRX P[0..15]
10 PCIE_MTX_C_GRX_N[0..15] < PCIE MTX C GRX N[0..15]

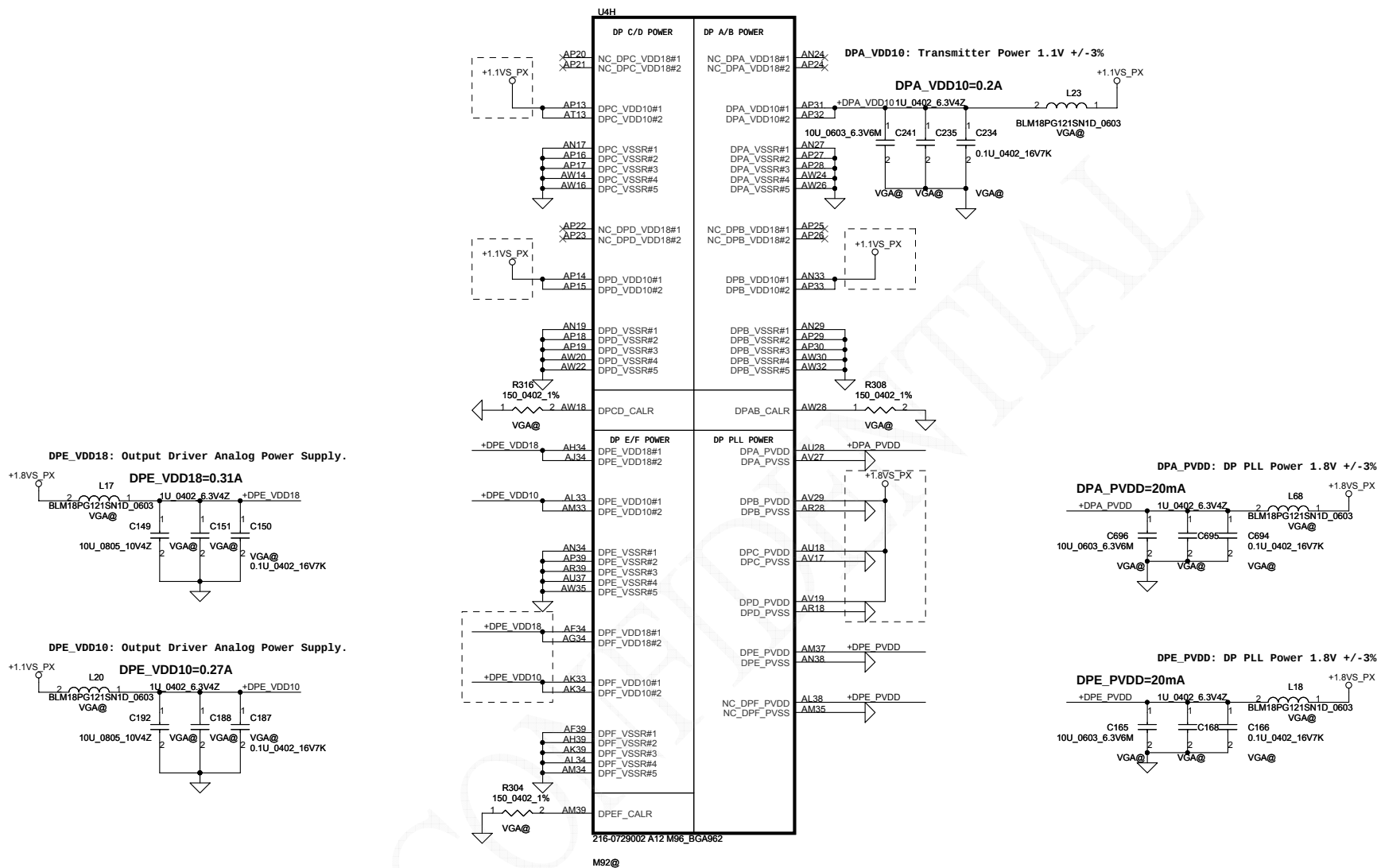
PCIE LANE REVERSAL

PCIE LANE REVERSAL

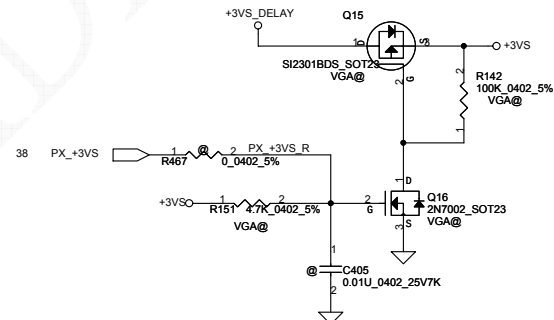
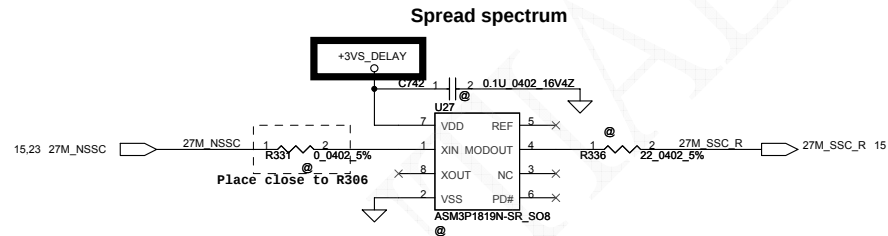
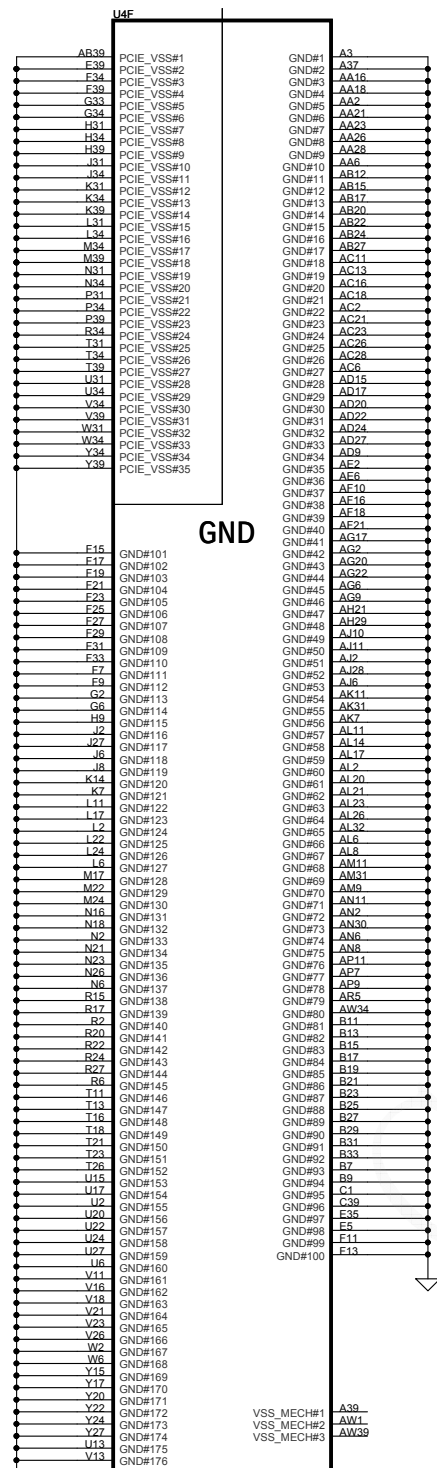


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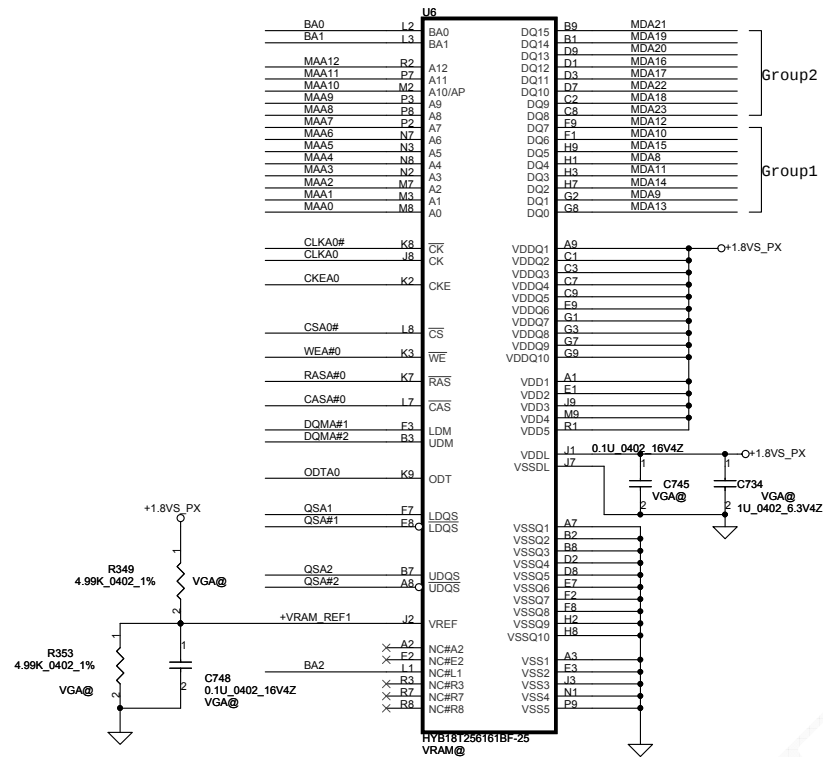


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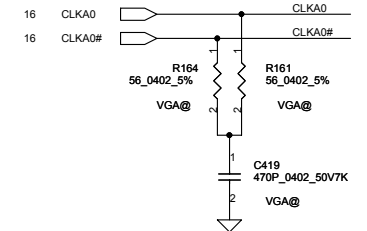
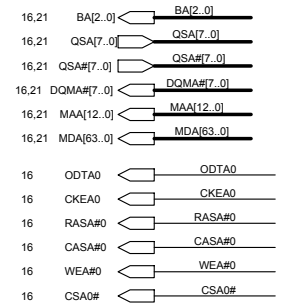
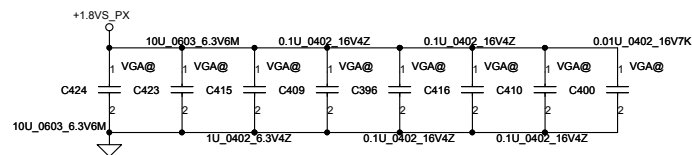
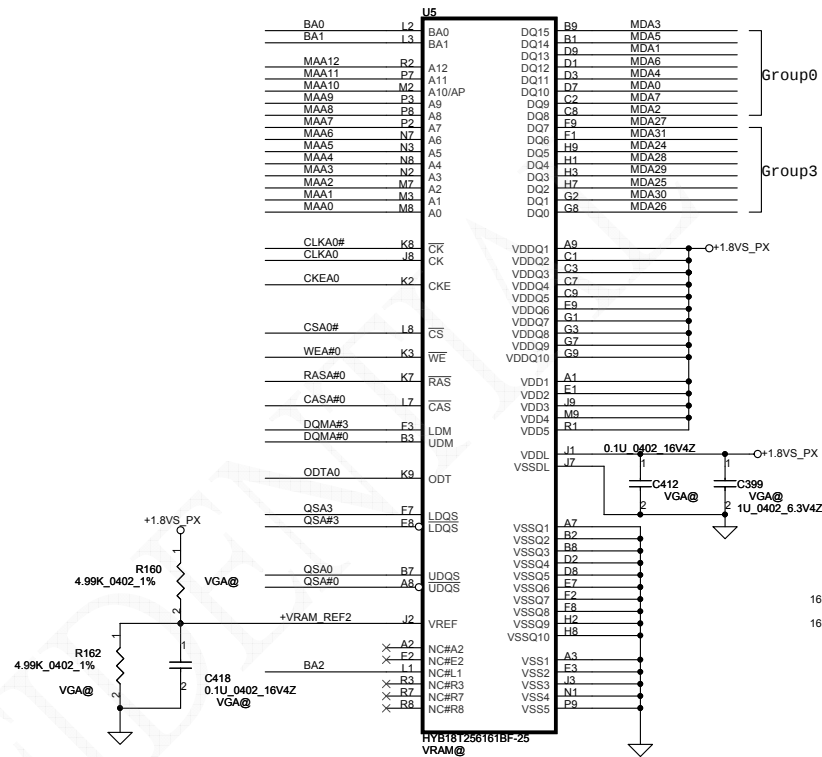
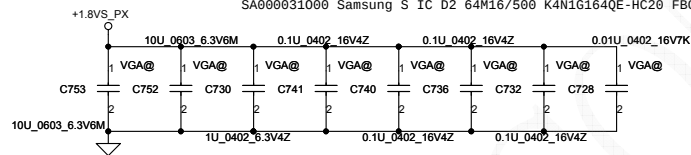


Use Delay 3.3V BUS (VDDR3) for GPIO/DDC Pull up to reduce Leakage to VDDR3 Bus.

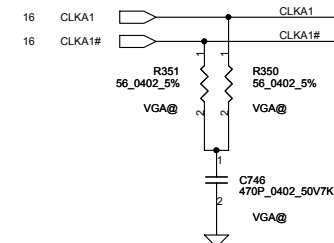
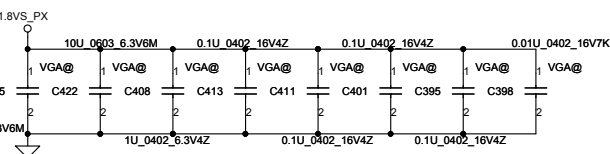
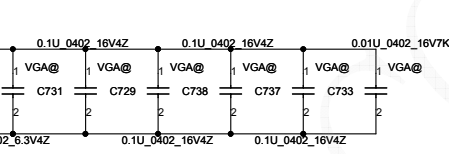
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SA00002UH00 HYNIX S IC D2 64M16/500 H5PS1G63EFR-20L FBGA84
 SA00002MF00 Qimonda S IC D2 64M16/500 HYB18T1G161C2F-20
 SA00002MD00 Samsung S IC D2 64M16/500 K4N1G164Q0-HC20 FBGA84
 SA00003I000 Samsung S IC D2 64M16/500 K4N1G164Q0-HC20 FBGA 84P

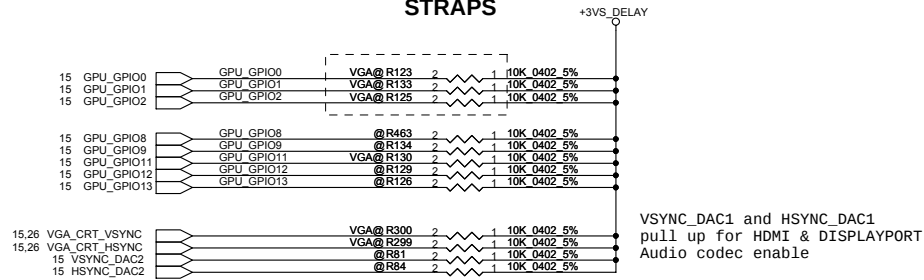


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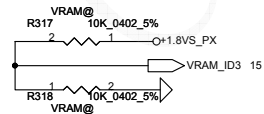
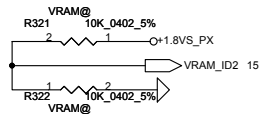
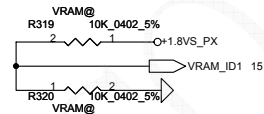
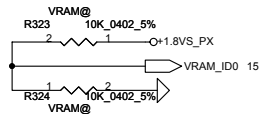
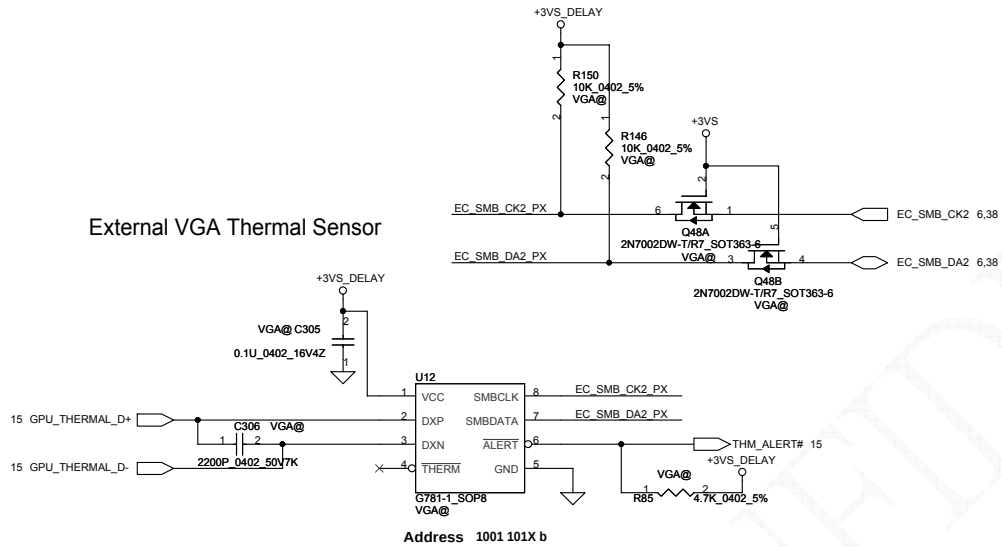


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STRAPS



External VGA Thermal Sensor



CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable	1 : PCIe bus Full Tx output swing 0 : PCIe bus 50% Tx output swing
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable	1 : Tx de-emphasis enabled 0 : Tx de-emphasis disabled
BIF_GEN2_EN_A	GPIO2	PCIe GNE2 ENABLED 0 = Advertises the PCIe device as 2.5 GT/s capable at power-on. 1 = Advertises the PCIe device as 5.0 GT/s capable at power-on.	0 (5.0 GT/s capability will be controlled by software)
VGA_DIS	GPIO9	VGA Disable determines whether or not the card will be recognized as the system's VGA controller	0 : VGA Controller capacity enabled 1 : The device will not be recognized as the system's VGA controller
CONFIG(2:0)	GPIO[13:11]	Size of the primary memory apertures	0 0 1
VIP_DEVICE_STRAP_EN	V2SYNC		0
RESERVED	H2SYNC		0
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1] AUD[0] 0 0 No audio function 0 1 Audio for DisplayPort and HDMI if dongle is detected 1 0 Audio for DisplayPort only 1 1 Audio for both DisplayPort and HDMI	11
RESERVED	GPIO21		0
BIOS_ROM_EN	GPIO_22_ROMCSB		0: Disable external BIOS ROM device 1: Enable external BIOS ROM device
CCBPASS	GENERICC	IGNORE VIP DEVICE STRAPS	0
BIF_CLK_PM_EN	GPIO8	BIF_CLK_PM_EN	0

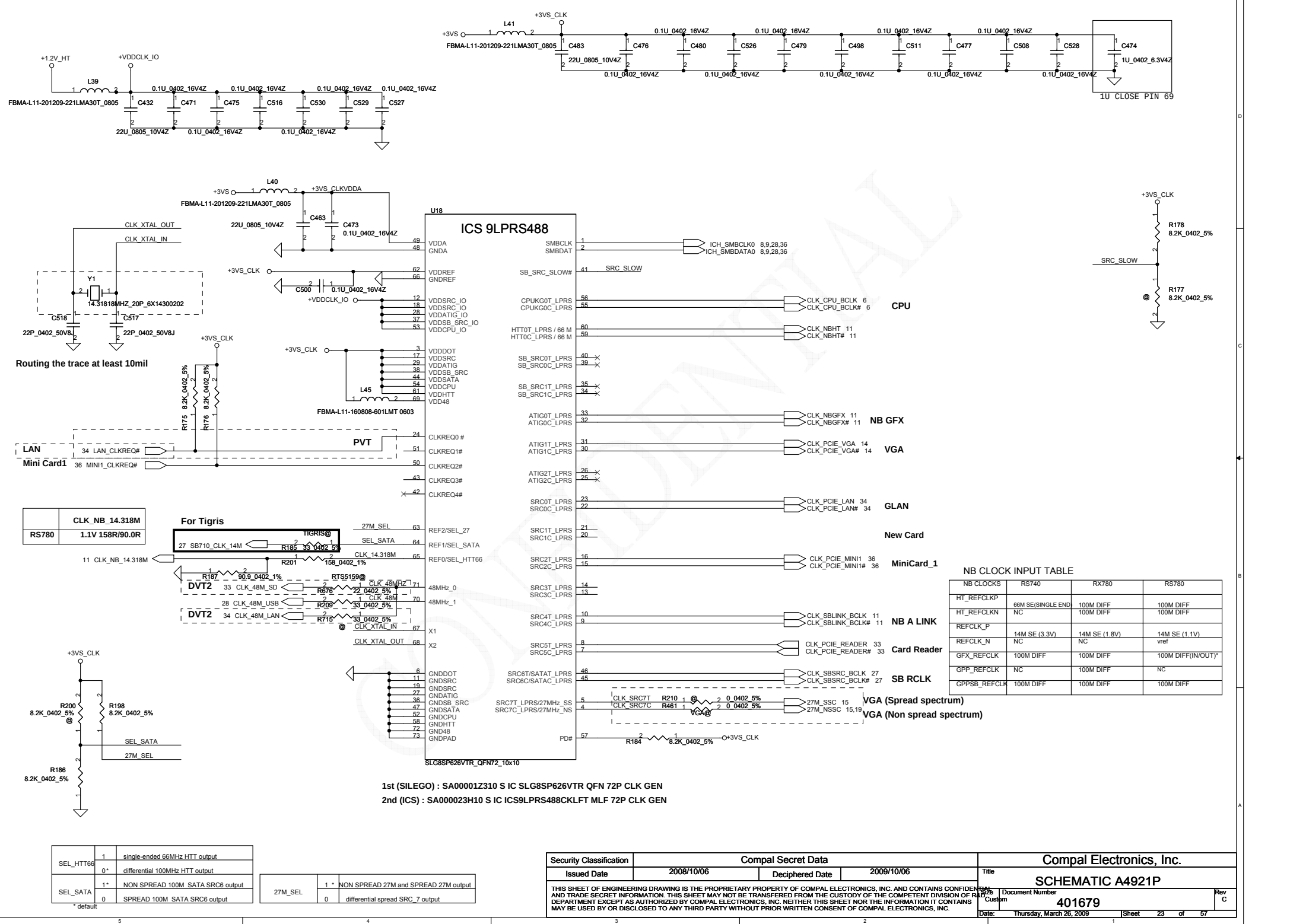
AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC	GENERICC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET	
GPI0_28_TDO	GPI021_BB_EN

STRAPS	PIN	GPU	Project	VRAM size	Vendor Part Number#	Compal Part Number#	VRAM_ID 3,2,1,0
VRAM_ID[3:0]	DVPDATA (23,22,21,20)	M92-M2 XT	JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (Q-die)	SA00002MD00	0 0 0 0
			JV40-PU_KBLG0	512M(x4)	Hynix 64Mx16 1.8V	SA00002UH20	0 0 0 1
			JV40-PU_KBLG0	512M(x4)	Qimonda 64Mx16 1.8V	SA00002MF0PVT	0 0 1 0
			JV40-PU_KBLG0	512M(x4)	Samsung 64Mx16 1.8V (E-die)	SA000031O10	0 1 0 0

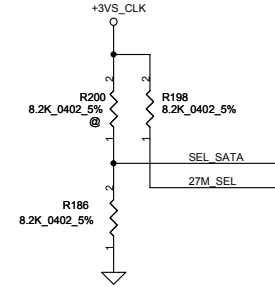
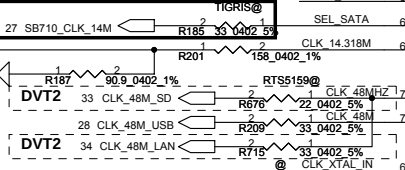
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Routing the trace at least 10mil

	CLK_NB_14.318M
RS780	1.1V 158R/90.0R

For Tigris



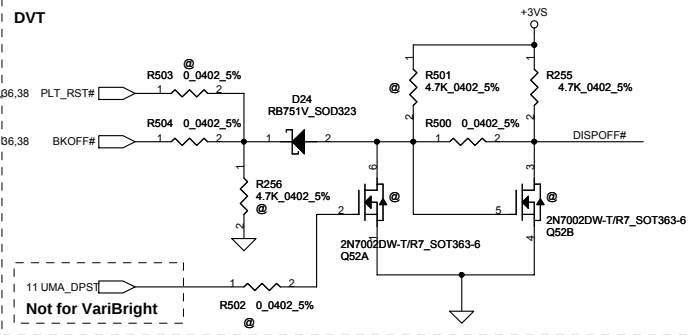
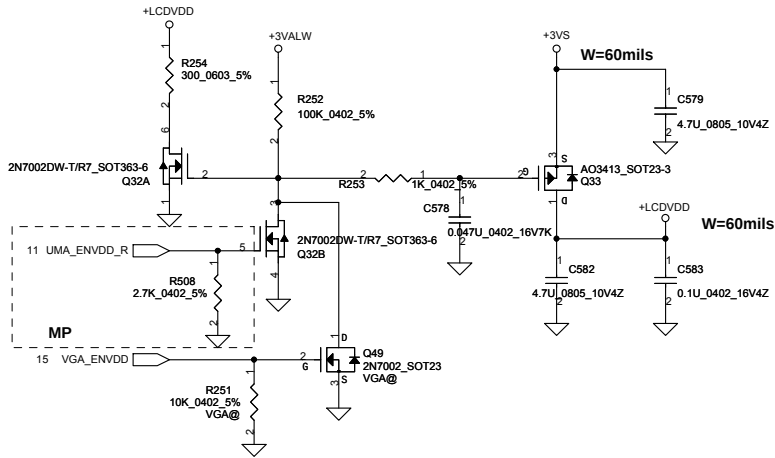
SEL_HTT66	1	single-ended 66MHz HTT output
	0*	differential 100MHz HTT output
SEL_SATA	1*	NON SPREAD 100M SATA SRC6 output
	0	SPREAD 100M SATA SRC6 output

27M_SEL	1 *	NON SPREAD 27M and SPREAD 27M output
	0	differential spread SRC_7 output

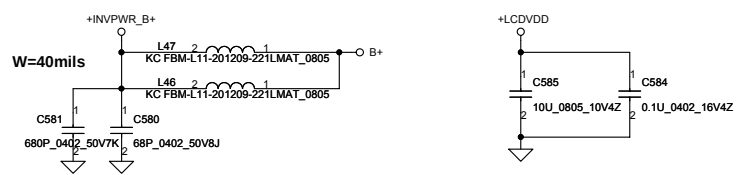
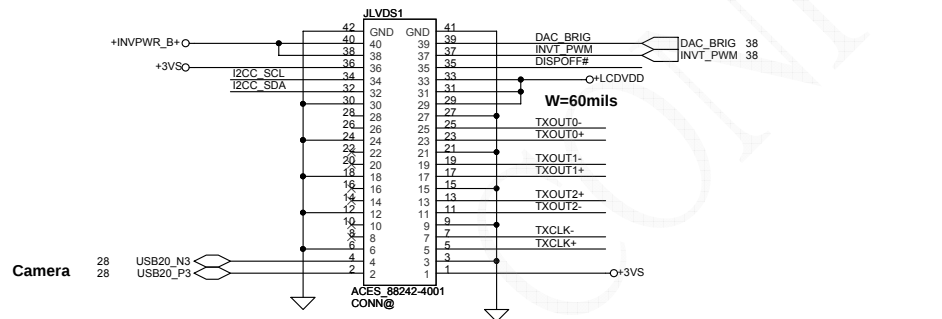
1st (SILEGO) : SA00001Z310 S IC SLG8SP626VTR QFN 72P CLK GEN
2nd (ICS) : SA000023H10 S IC ICS9LPRS488CLKLFT MLF 72P CLK GEN

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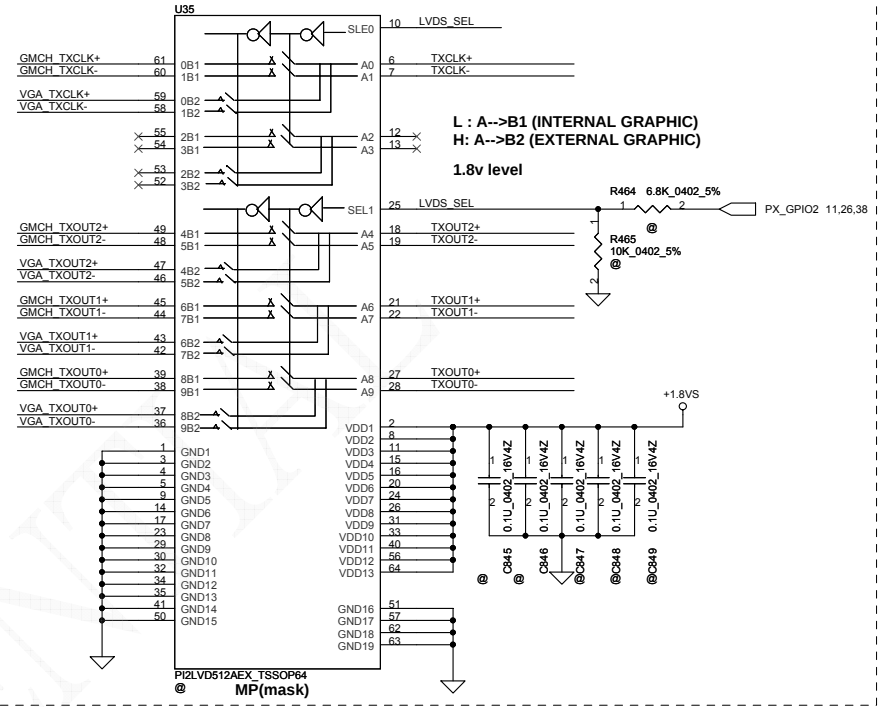
LCD POWER CIRCUIT



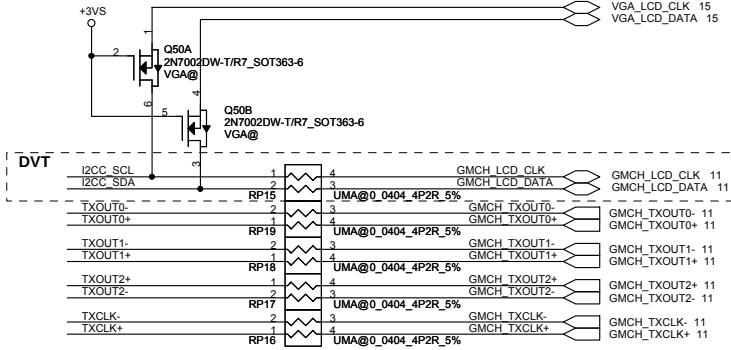
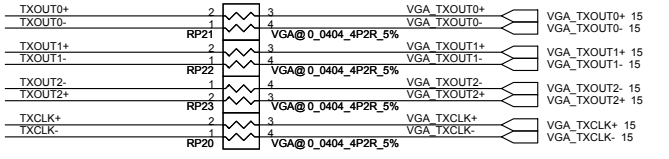
LCD/PANEL BD. Conn.



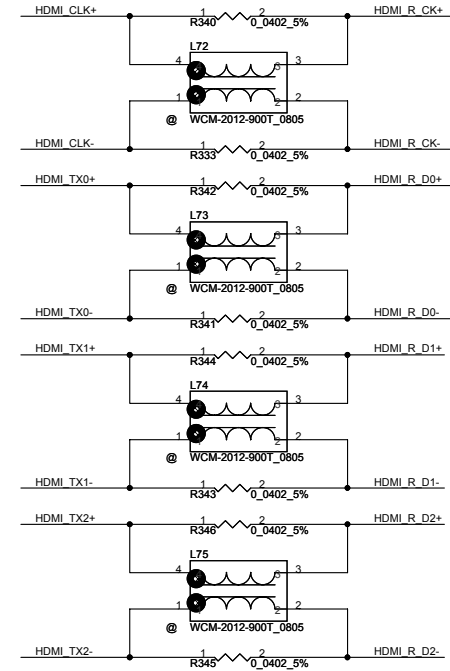
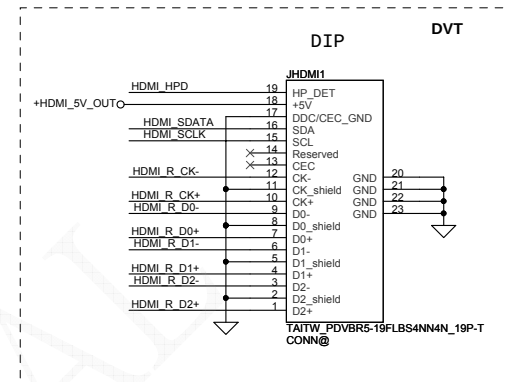
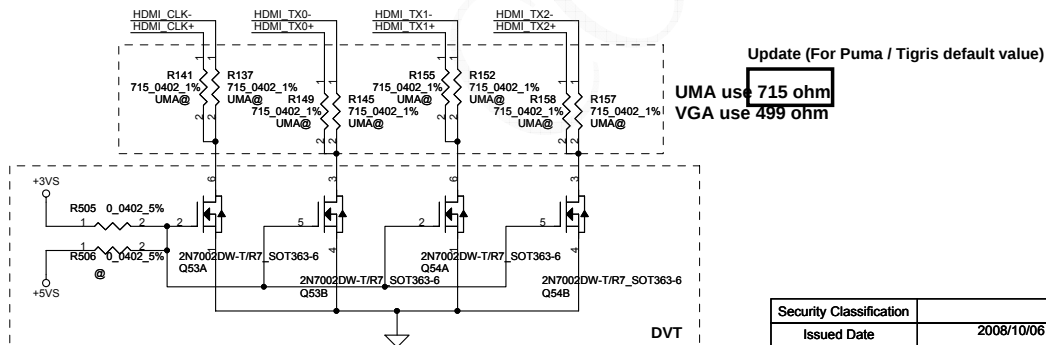
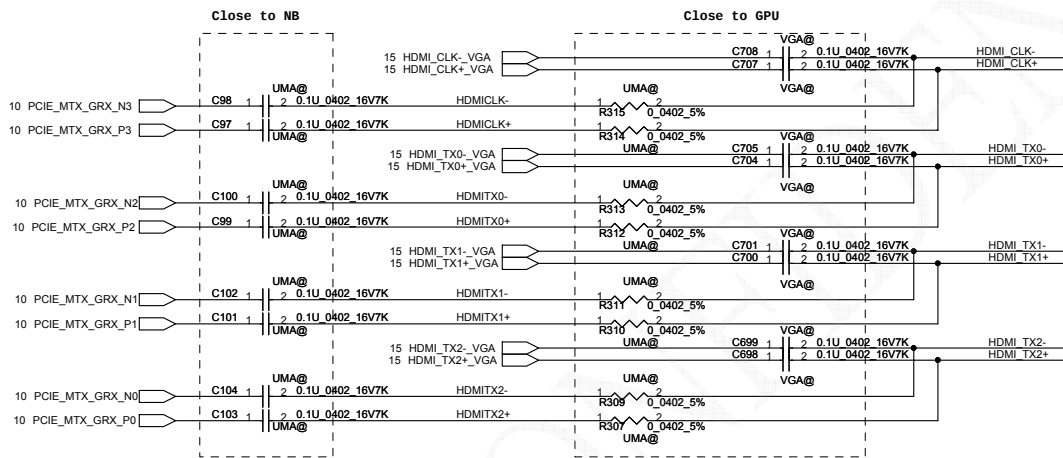
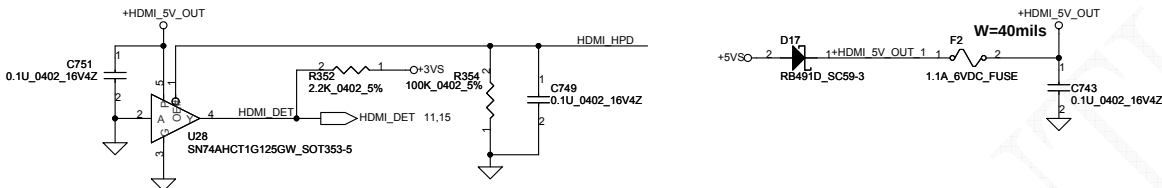
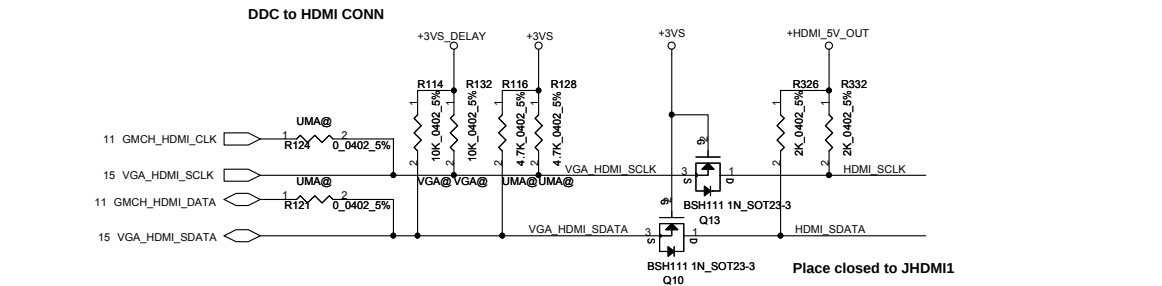
DVT



DVT

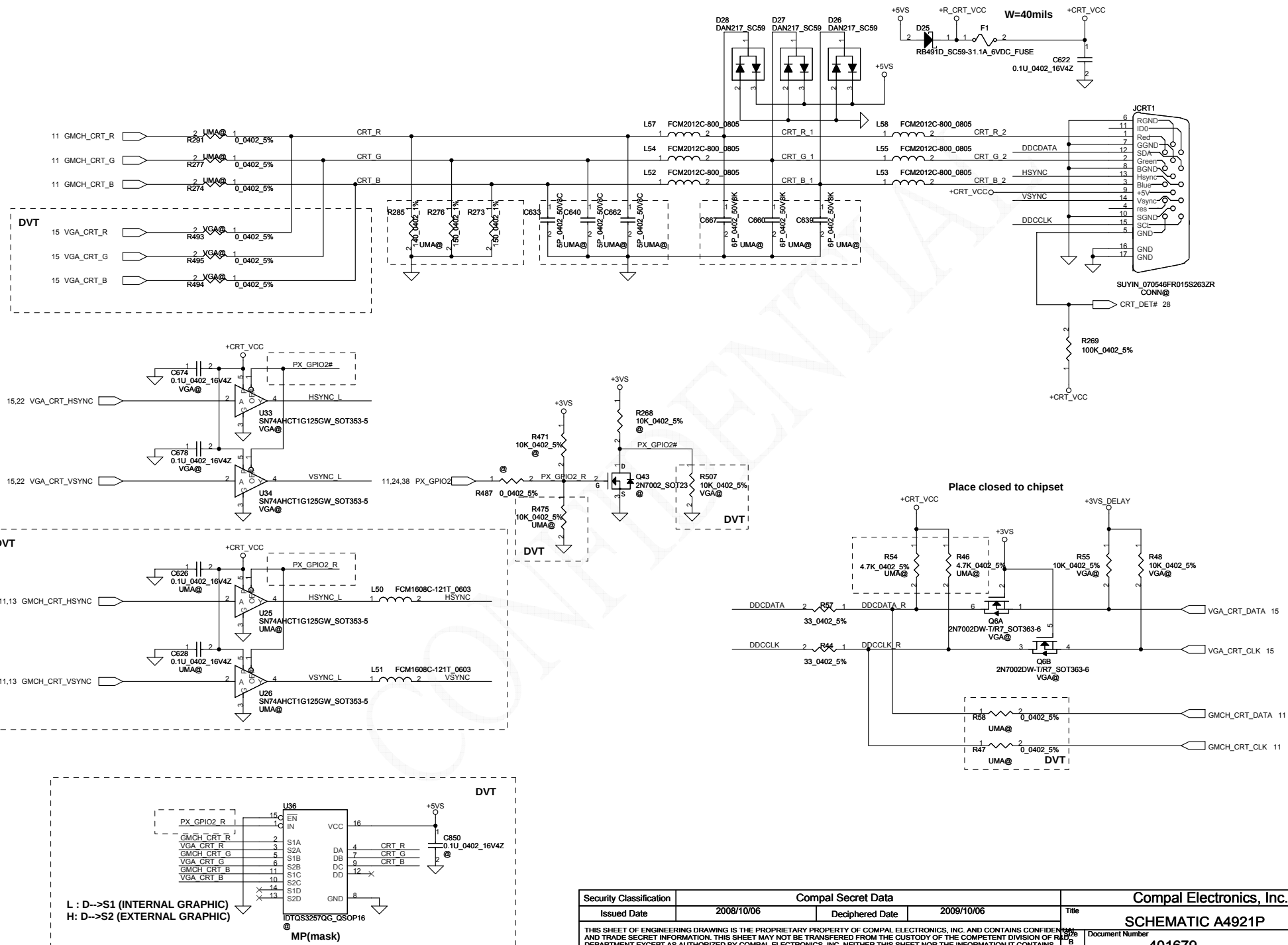


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								401679		C					
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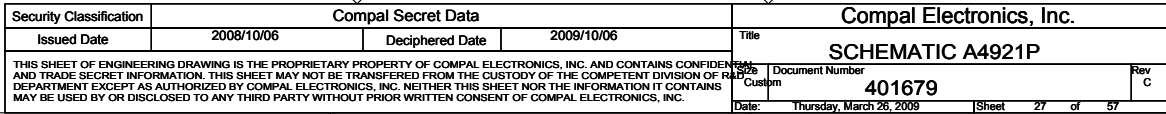


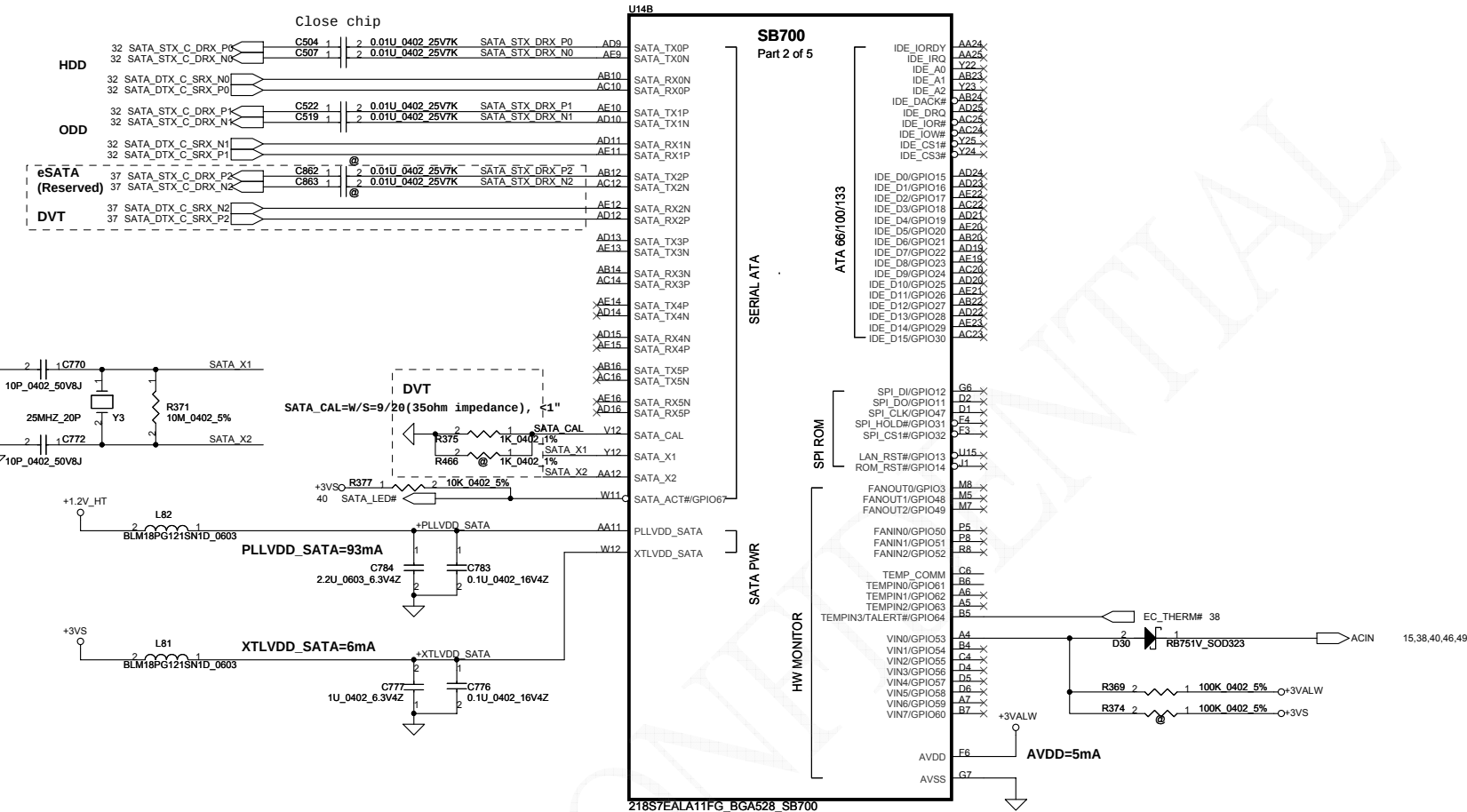
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Issued Date	2008/10/06	Deciphered Date	2009/10/06	Title	Document Number	SCHEMATIC A4921P	
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CRT CONNECTOR



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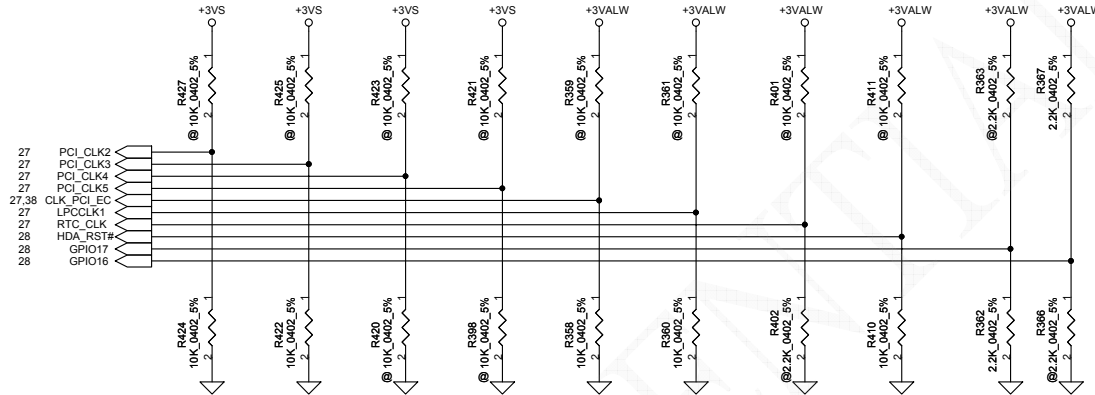


Port Number	Pri/SEC,Mas/Slave assignment	SATA drive controlled by
Port 0	Primary master	SATA controler
Port 1	Secondary master	SATA controler
Port 2	Primary slave	SATA controler
Port 3	Secondary slave	SATA controler
Port 4	Primary (Secondary) master	PATA controler
Port 5	Primary (Secondary) slave	PATA controler

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

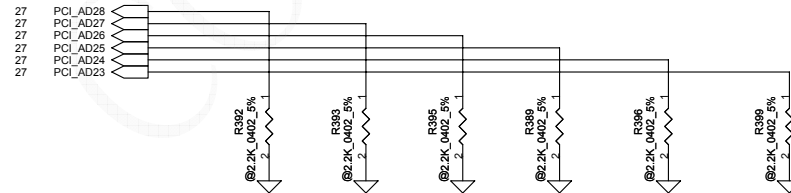
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0 CLK_PCI_EC	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	L,H = LPC ROM (Default L,NC) L,L = FWH ROM
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

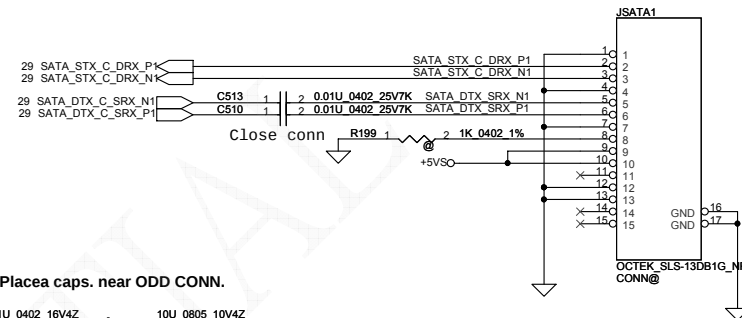
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

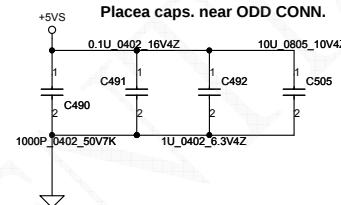


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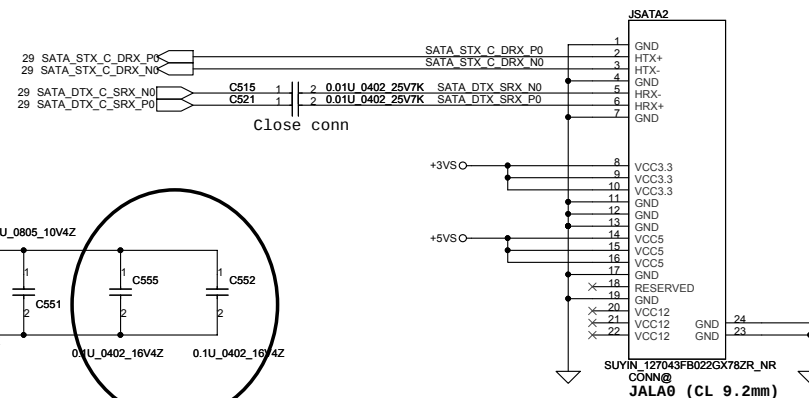
SATA ODD Conn.



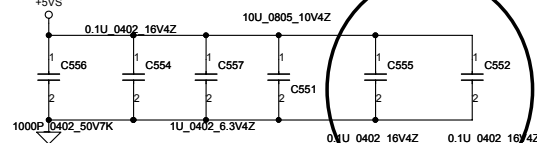
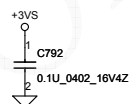
Placea caps. near ODD CONN.



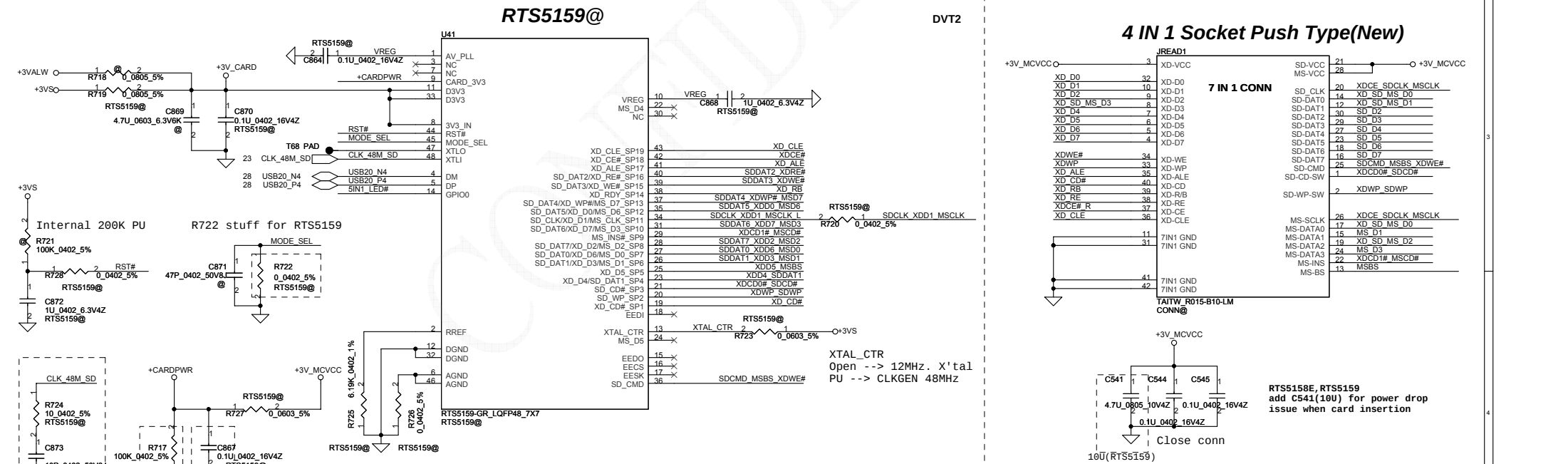
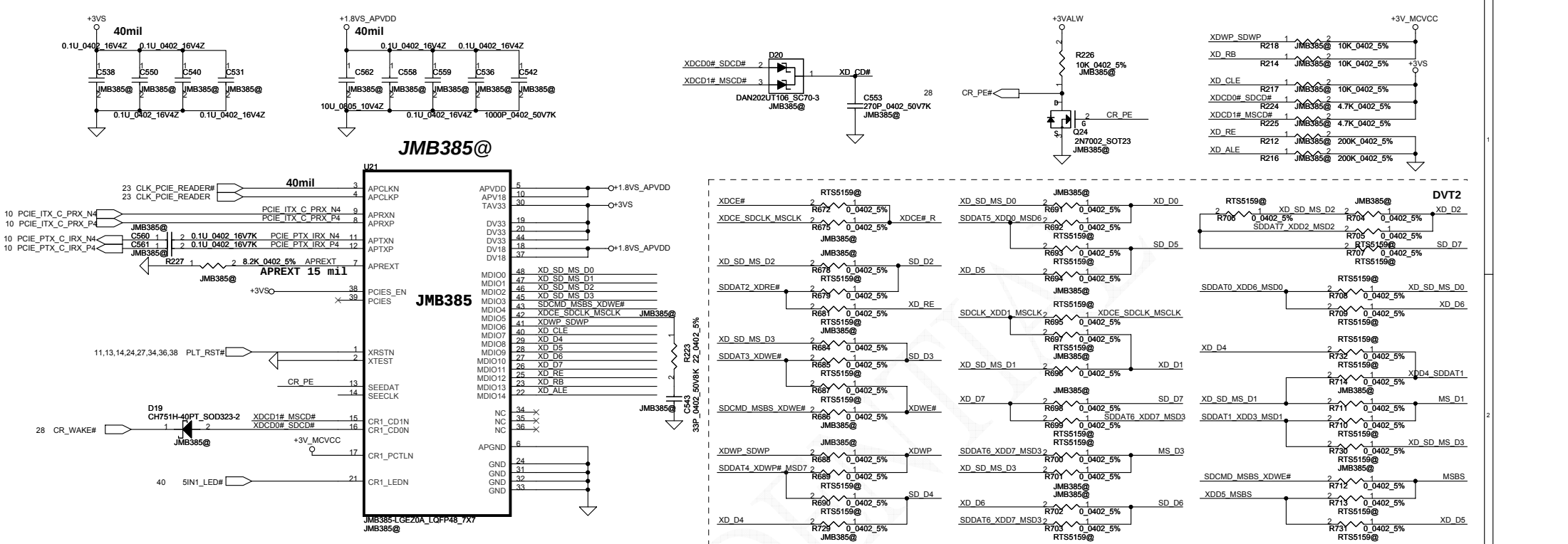
SATA HDD Conn.



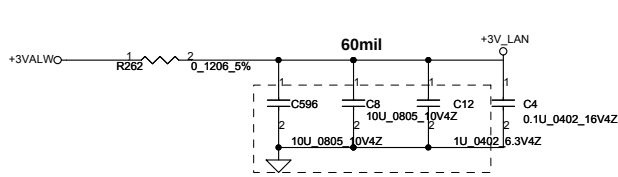
for ESD issue



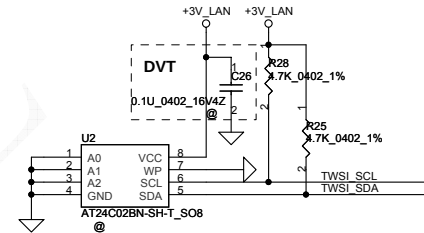
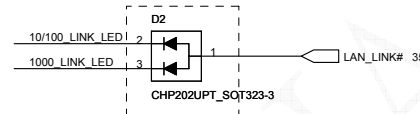
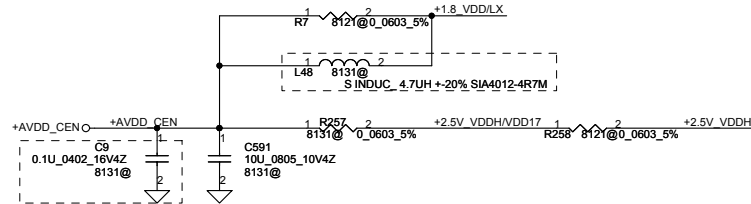
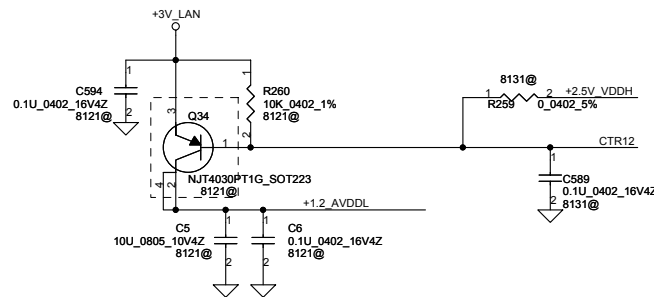
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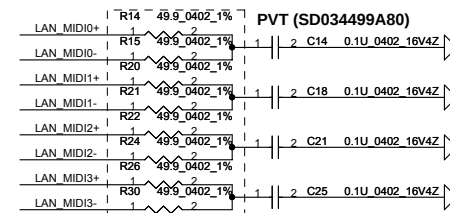
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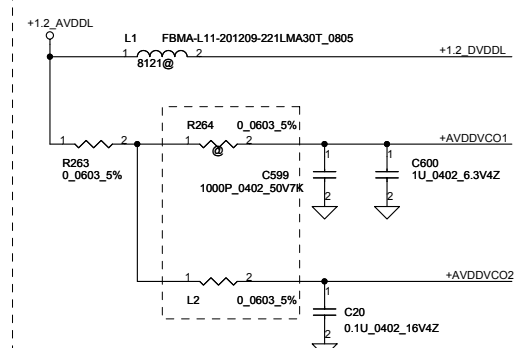
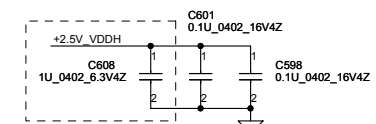
Place Close to Pin 2



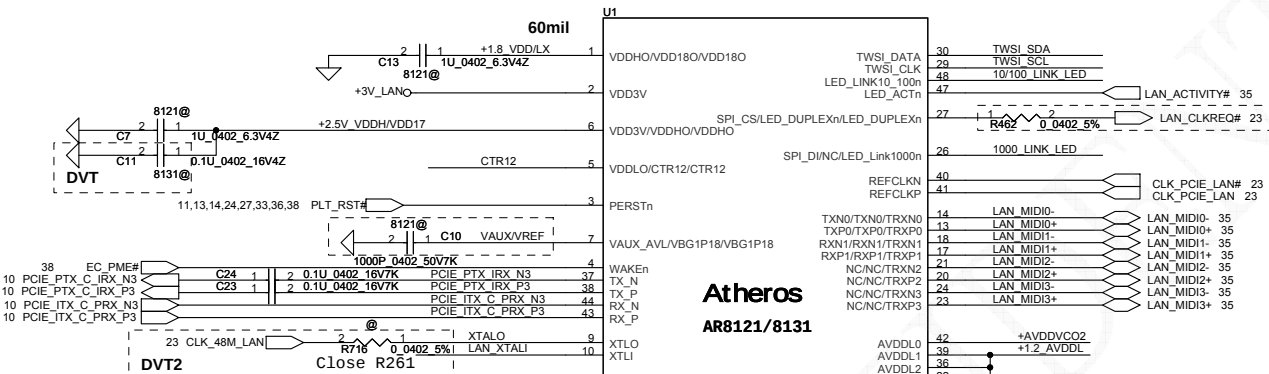
Place Close to LAN chip



Place Close to Pin15, 19, 25
C608 close to Pin15

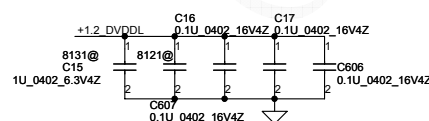


If overclocking, R264, L2 stuffed and R263 removed.
If not overclocking, R263, L2 stuffed and R264 removed.
AR8131:L2=0ohm (more power saving mode)

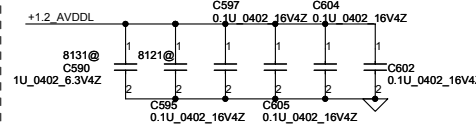


Atheros
AR8121/8131

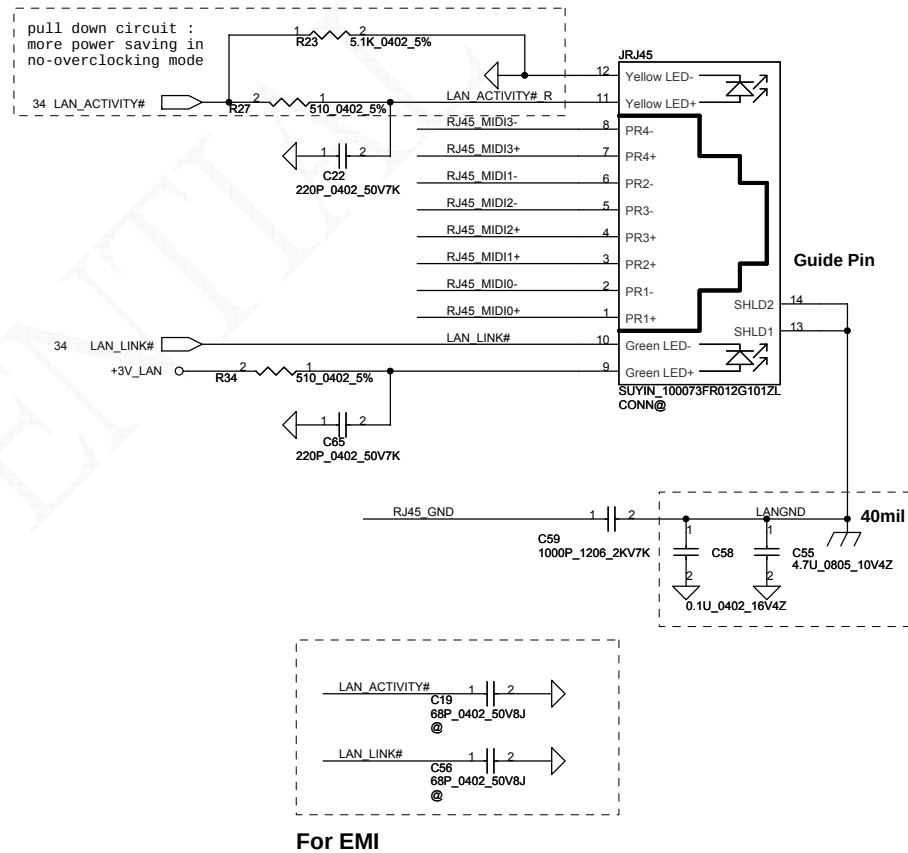
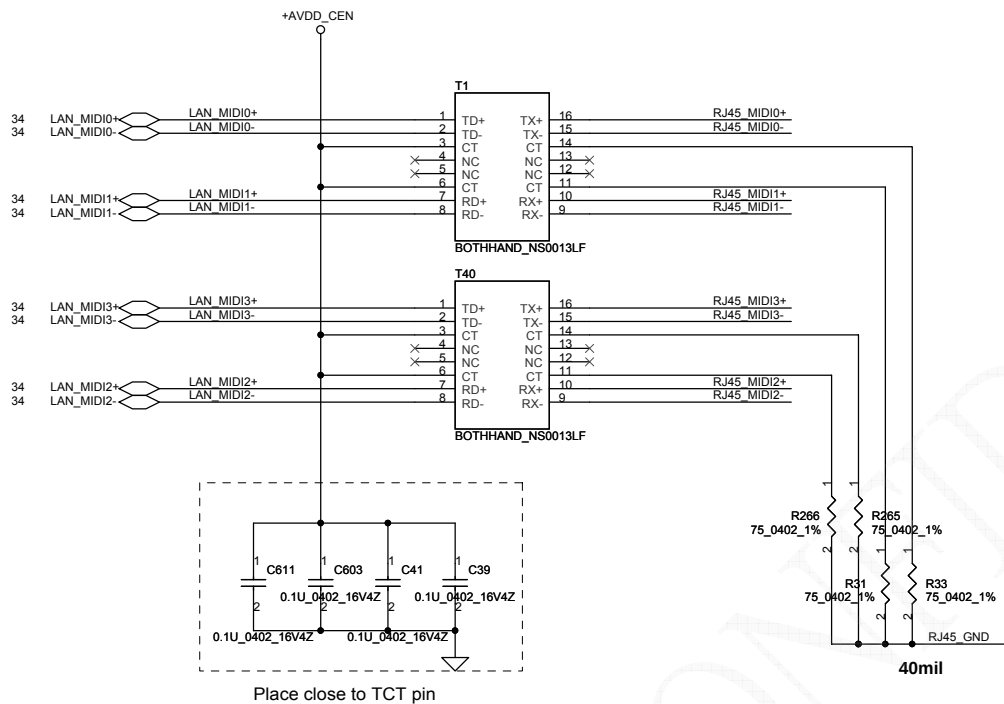
Place Close to Pin 28, 32, 45, 46
C15 and C607 close to Pin46
C16 close to Pin45



Place Close to Pin8, 16, 22, 36, 39
C590 and C595 close to Pin8

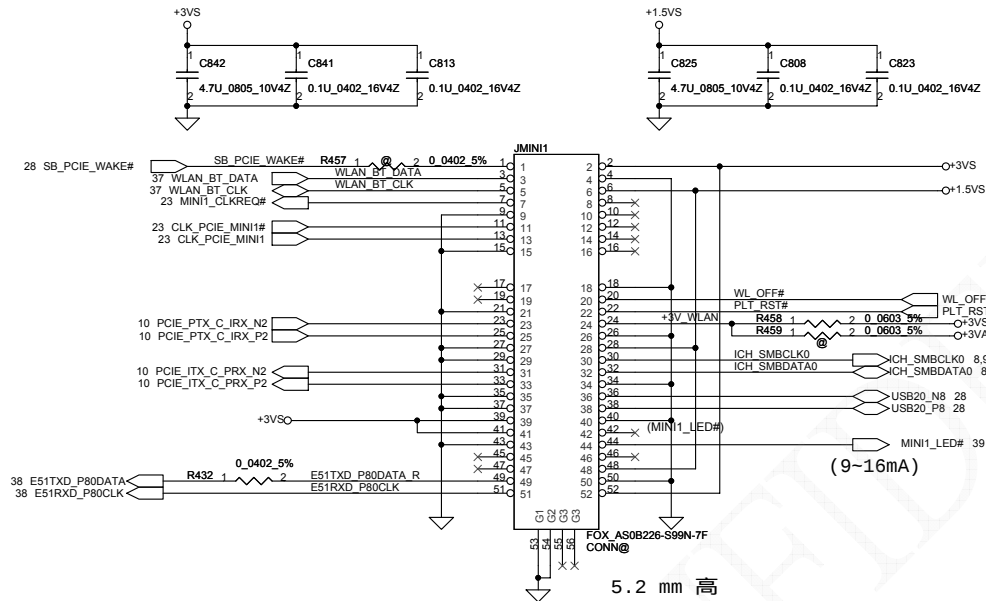


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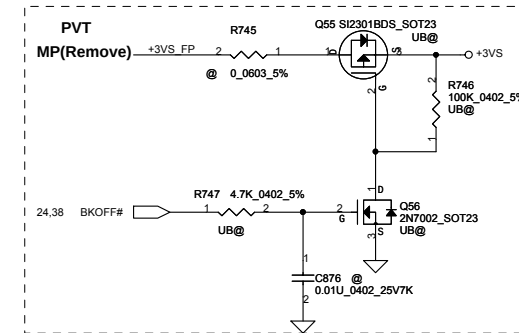
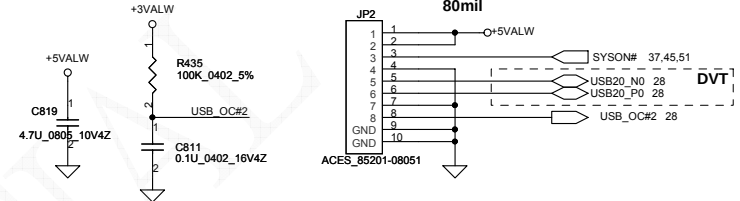
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For Wireless LAN

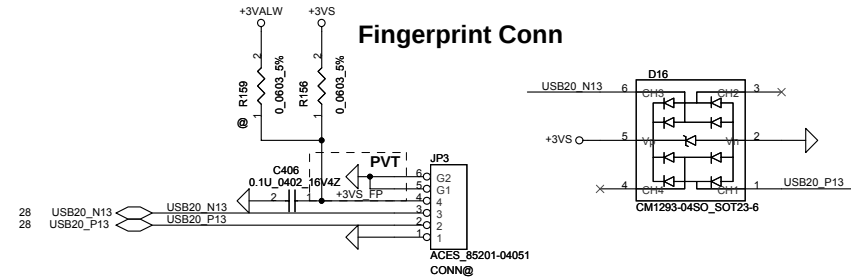


Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	
+3VS	1000	750	Normal
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

To USB/B Connector

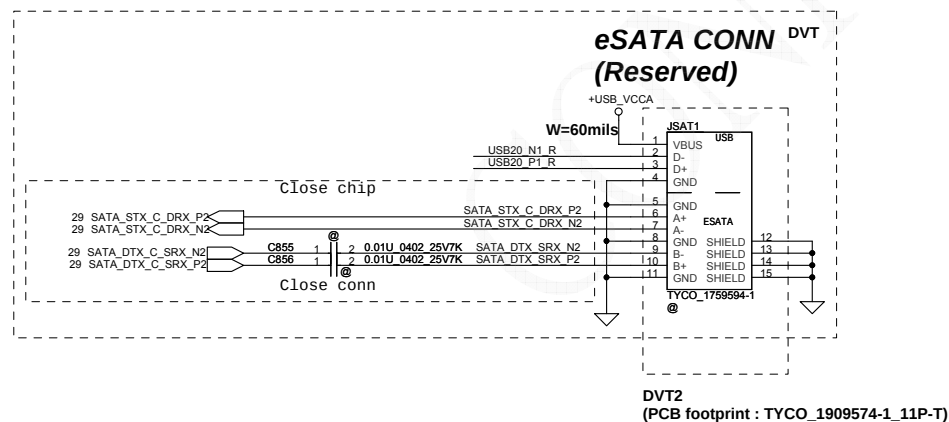
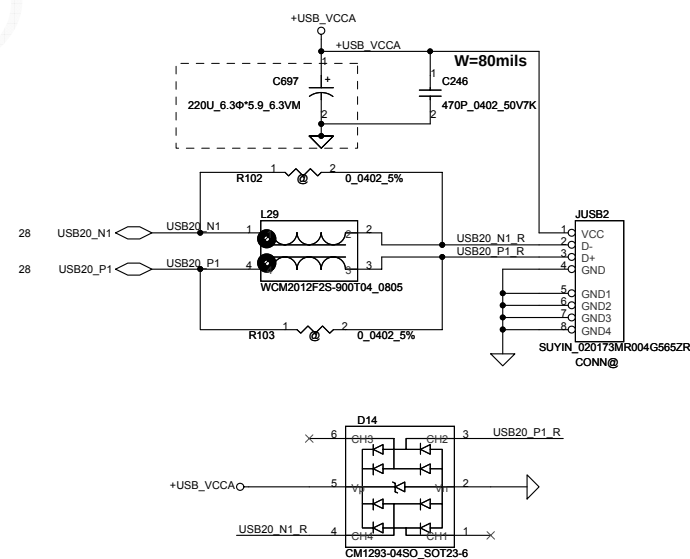
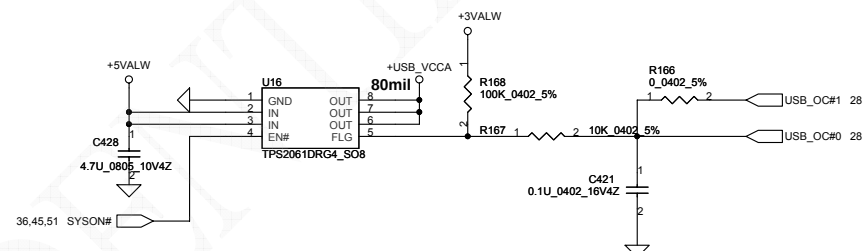
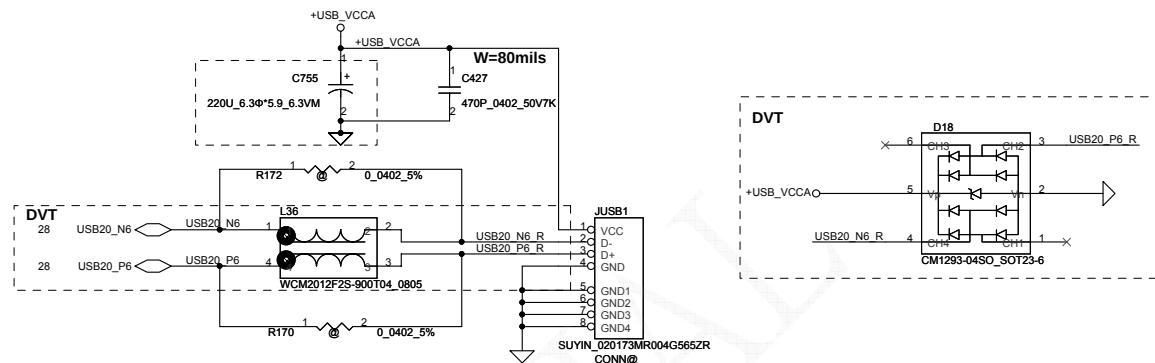
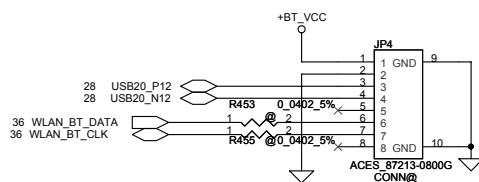
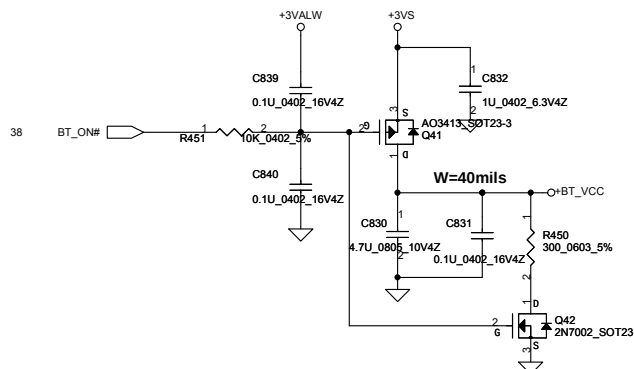


Fingerprint Conn

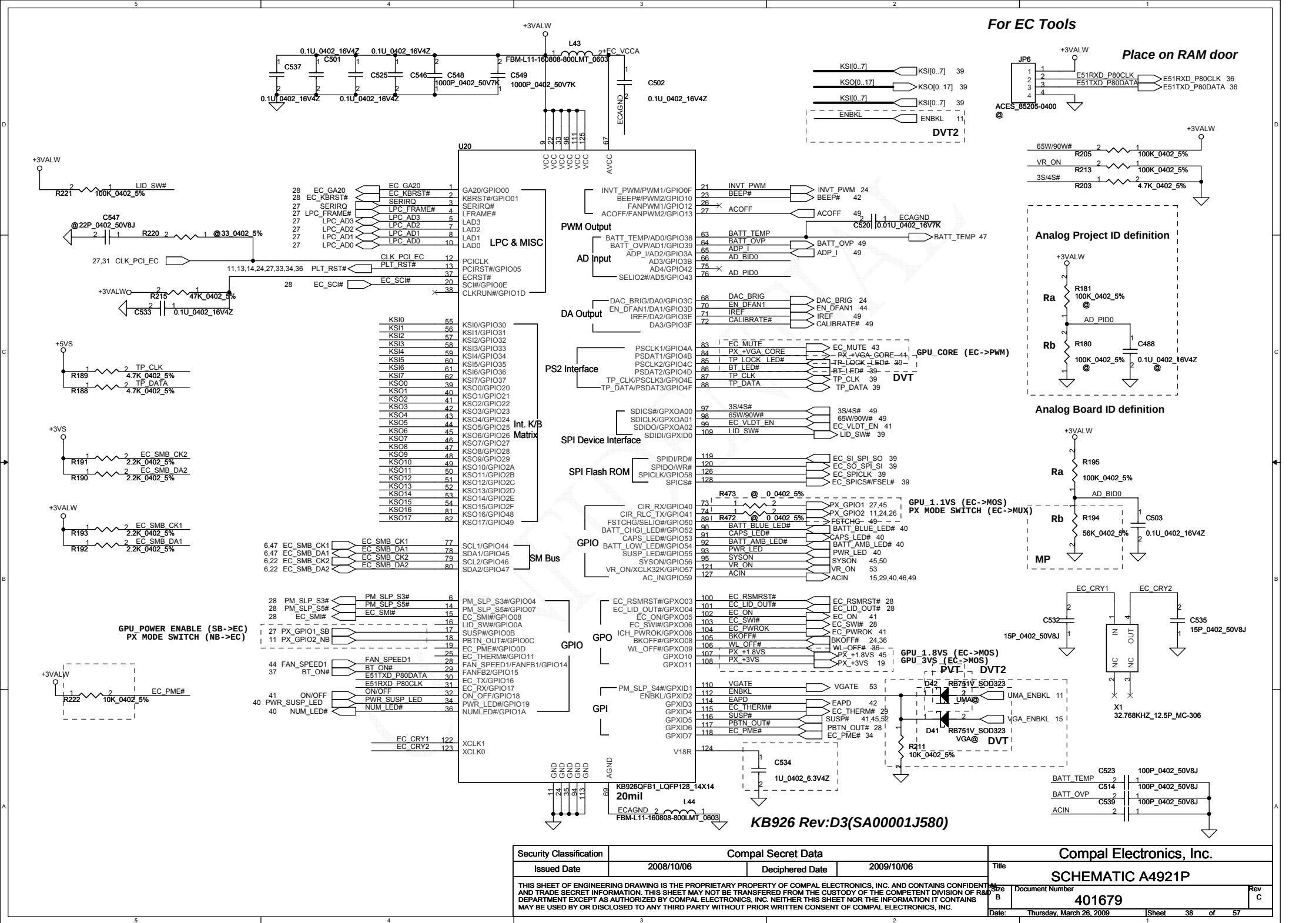


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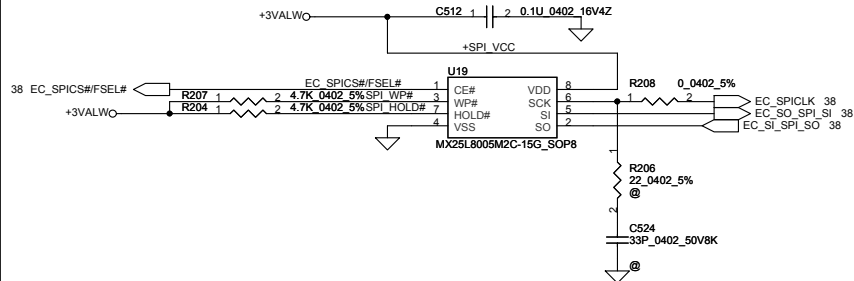
Bluetooth Conn.



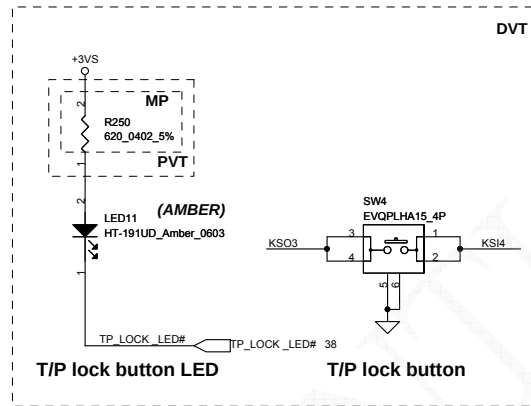
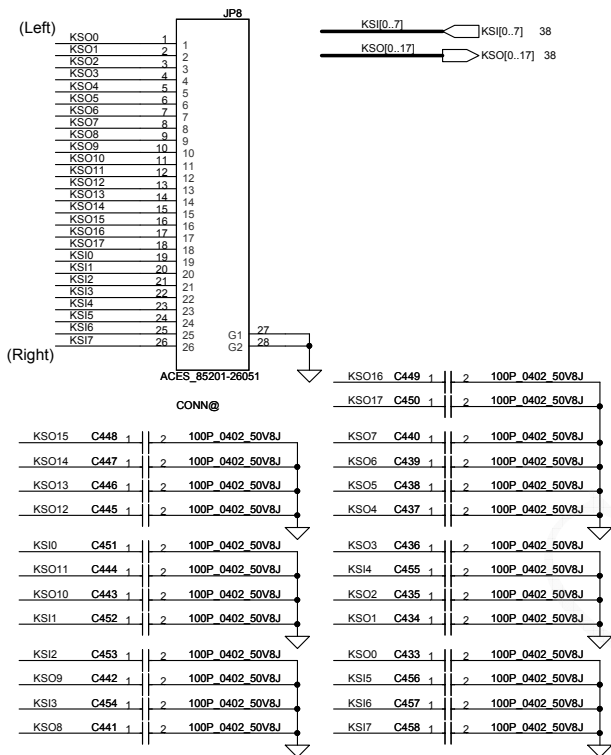
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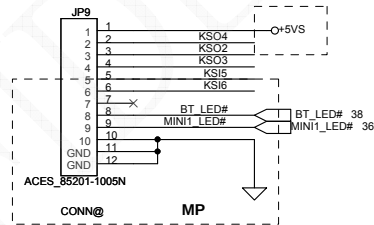
BIOS(SYS / EC / VGA)



INT_KBD Conn.

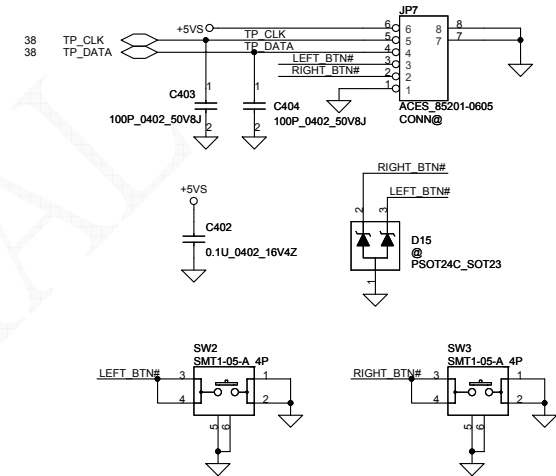


To FUN/B Conn (10PIN)

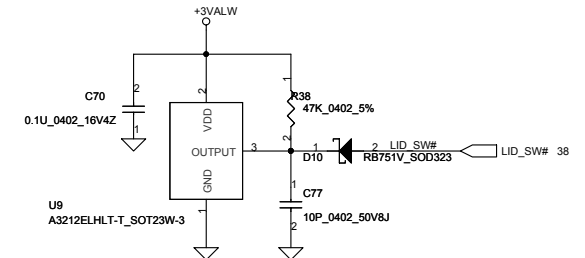


	KSO4	KSO2	KSO3
KSI5	WL_BTN#	Volume Down	Back Up
KSI6	BT_BTN#	Volume Up	Program (KBLG0) Battery (KALG0)
KSI4			T/P lock

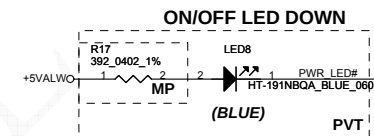
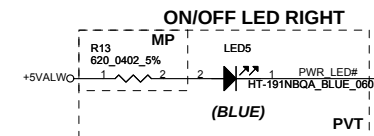
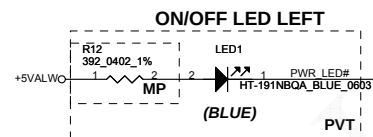
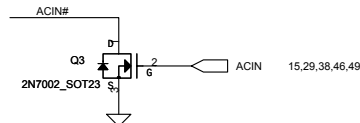
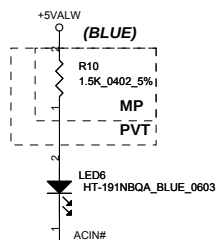
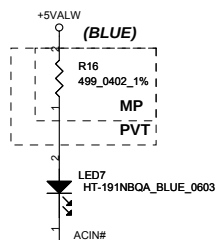
To TP/B Conn.



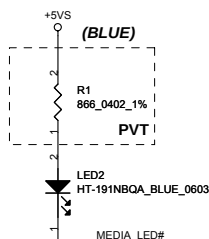
Lid Switch (Hall Effect Switch)



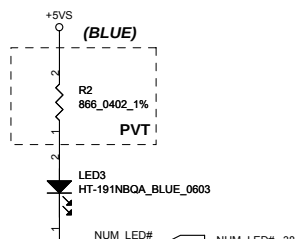
Enlightener LED



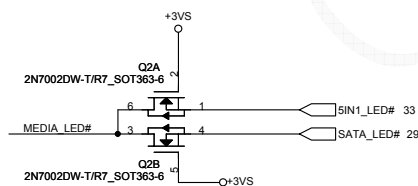
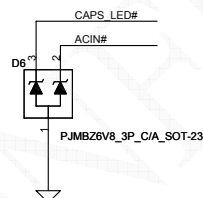
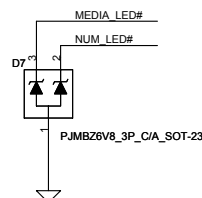
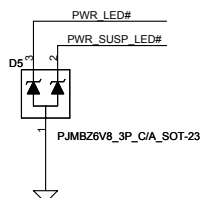
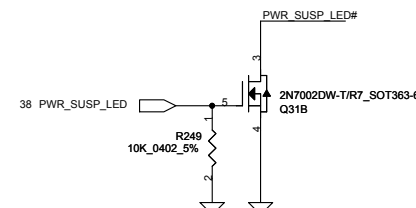
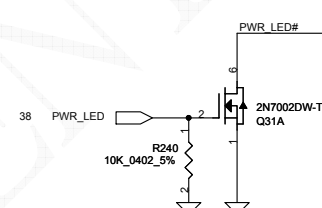
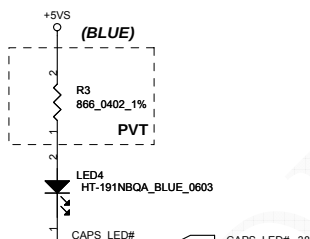
MEDIA_LED



NUM_LED

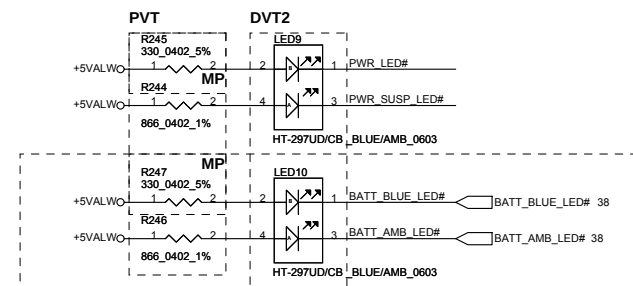


CAPS_LED



Compal Footprint

Footprint : LED_HT-297DQ-GQ_4P

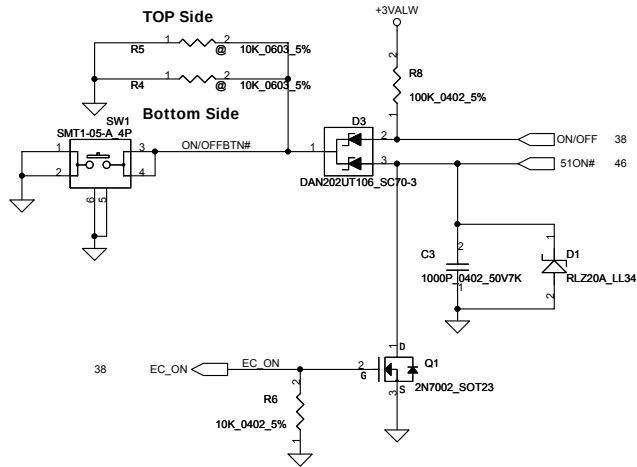


BLUE/AMBER

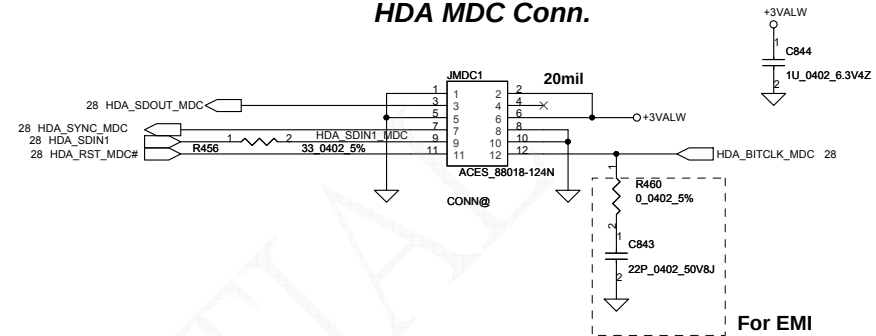
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Power Button

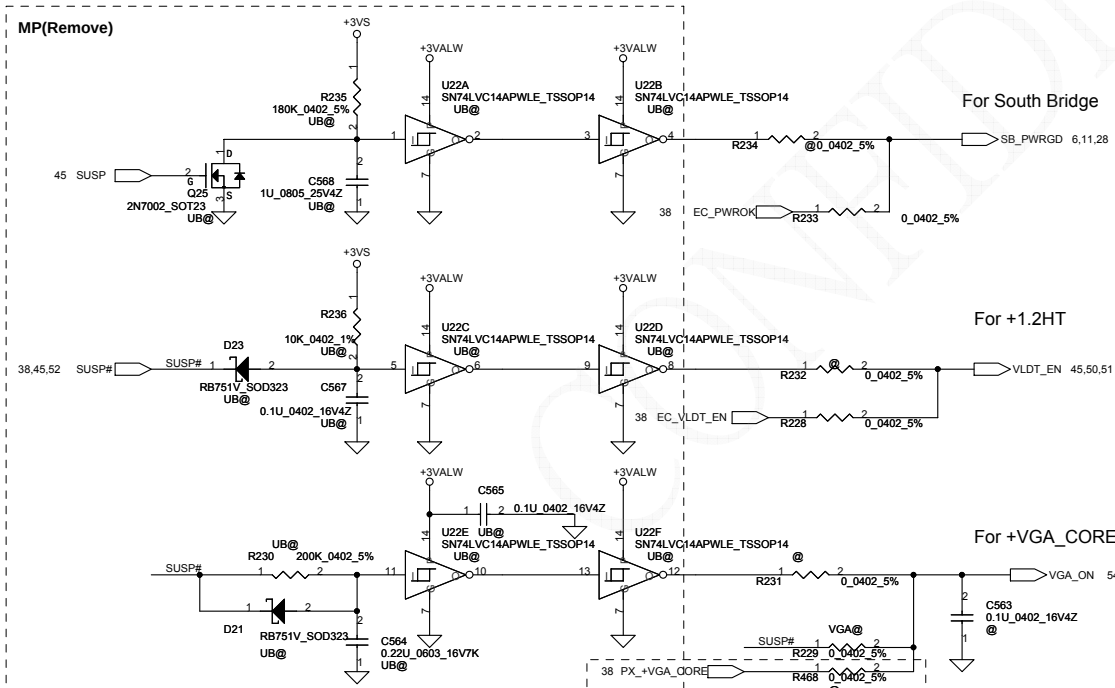
ON/OFF switch



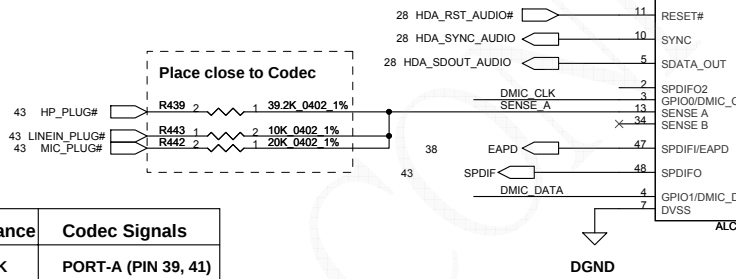
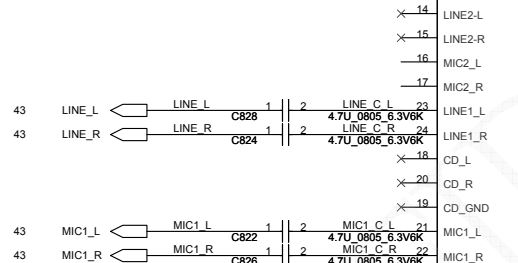
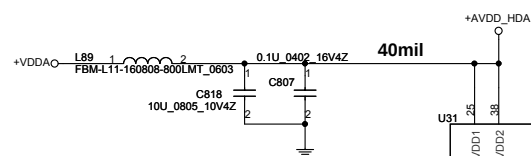
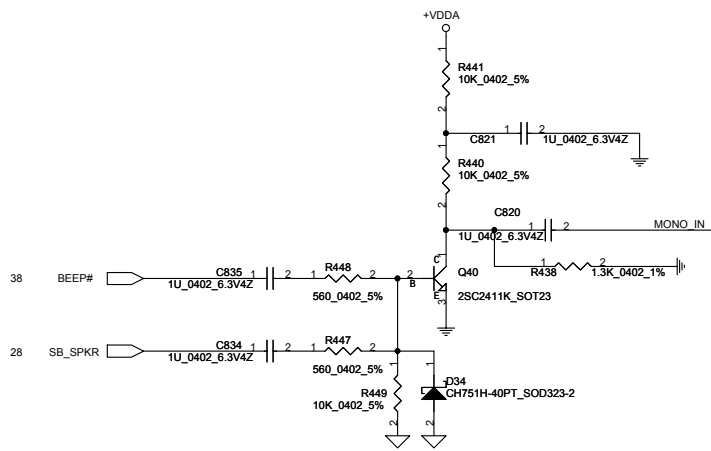
HDA MDC Conn.



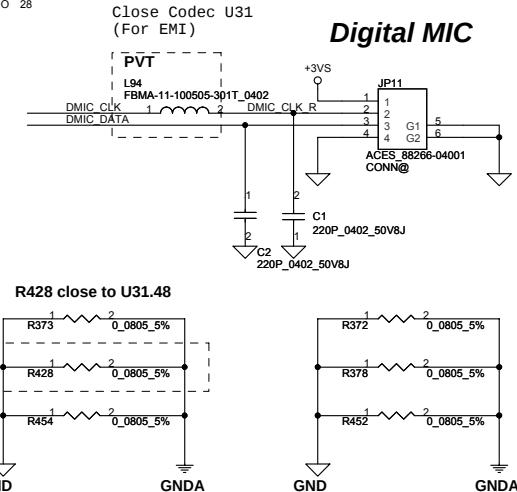
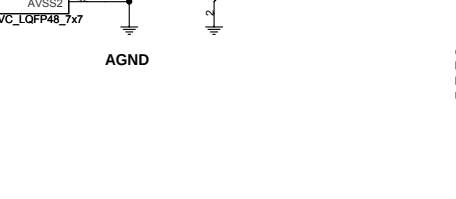
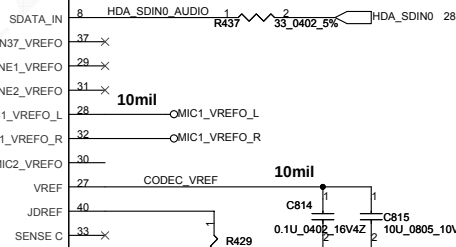
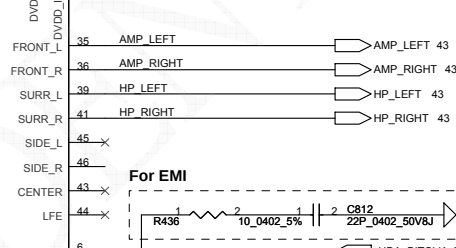
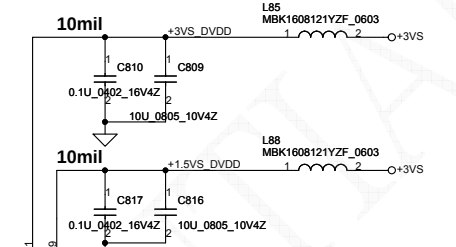
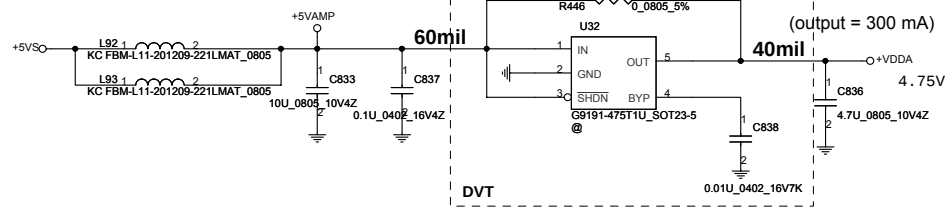
Power ON Circuit



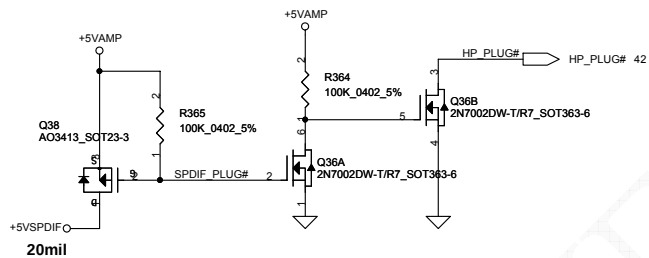
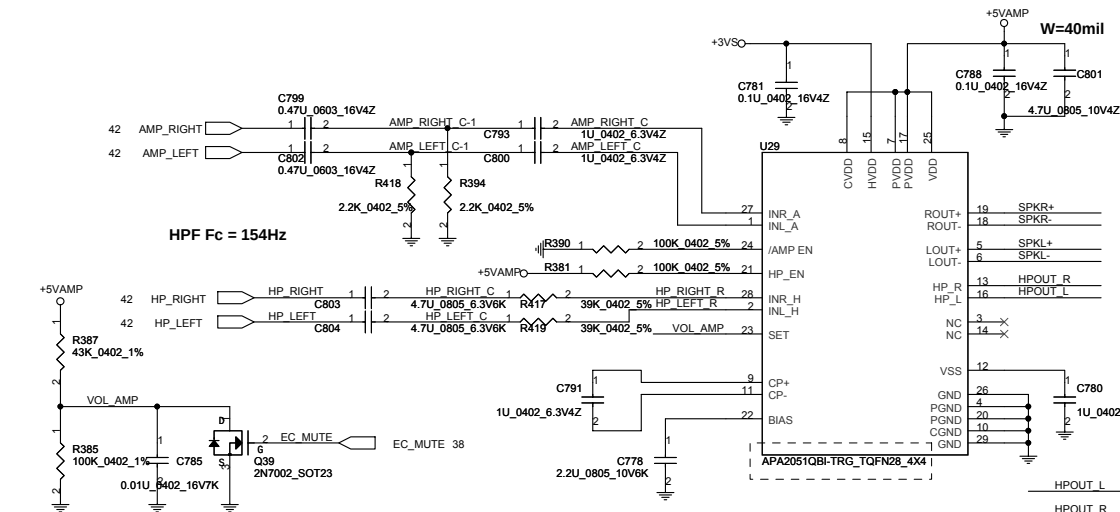
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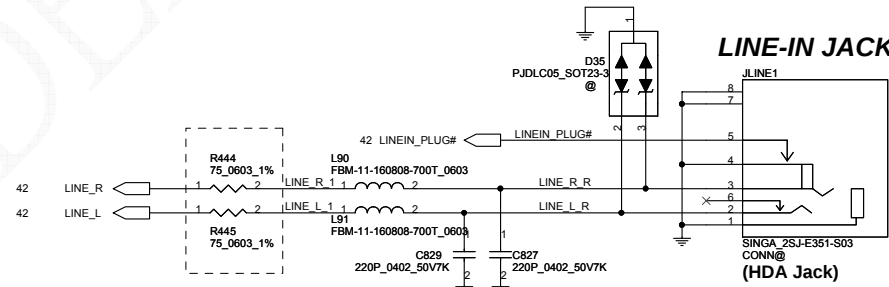
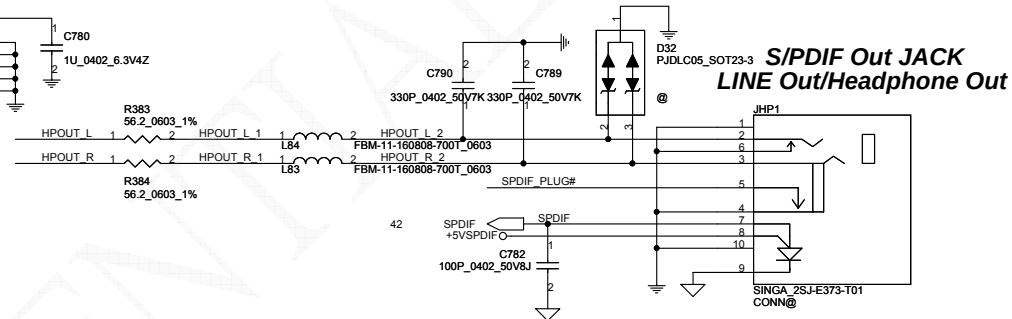
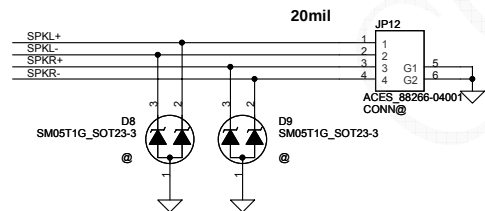
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
	5.1K	PORT-D (PIN 35, 36)
SENSE B	39.2K	PORT-E (PIN 14, 15)
	20K	PORT-F (PIN 16, 17)
	10K	PORT-G (PIN 43, 44)
	5.1K	PORT-H (PIN 45, 46)



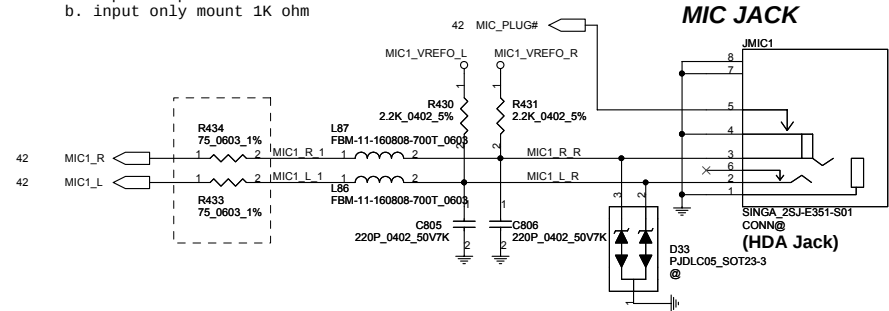
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Int. Speaker Conn.

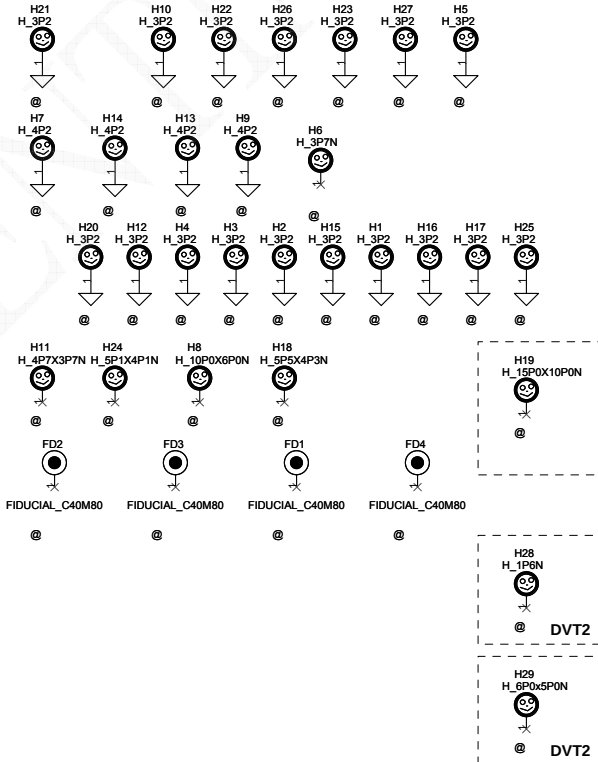
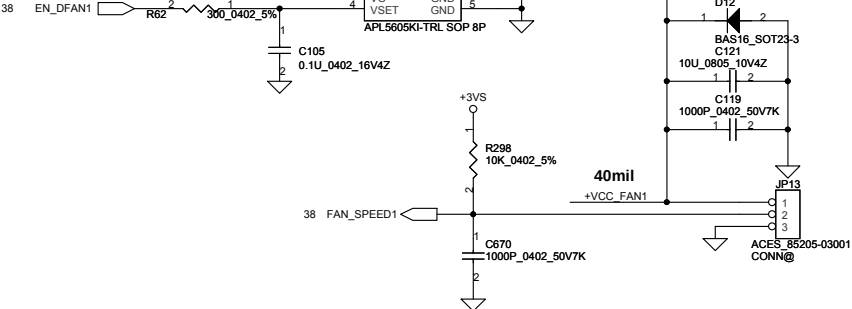


For ESD
I/O status:
a. input/output mount 75 ohm
b. input only mount 1K ohm



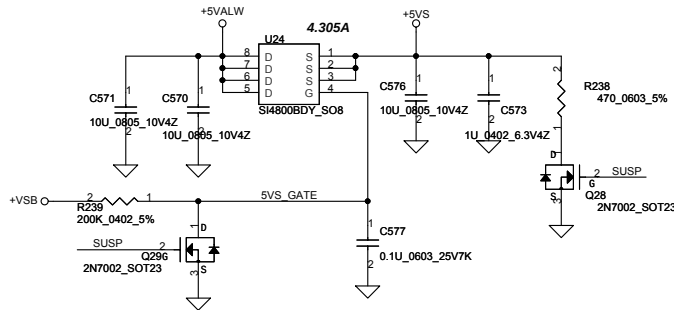
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FAN1 Conn

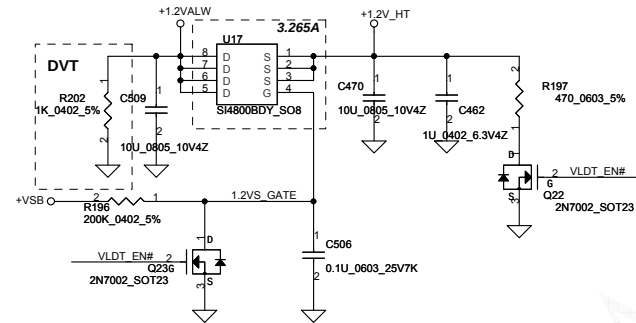


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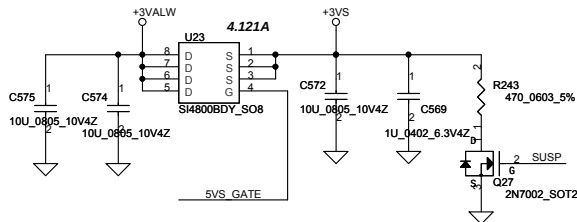
+5VALW TO +5VS



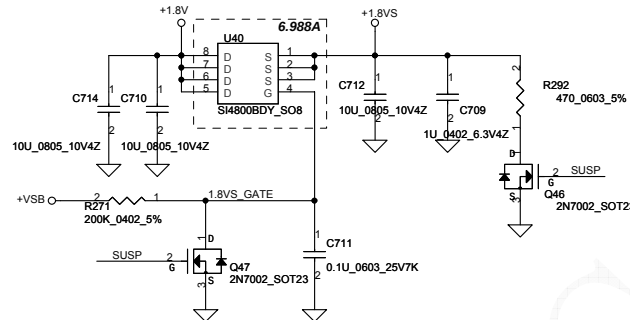
+1.2VALW TO +1.2V_HT



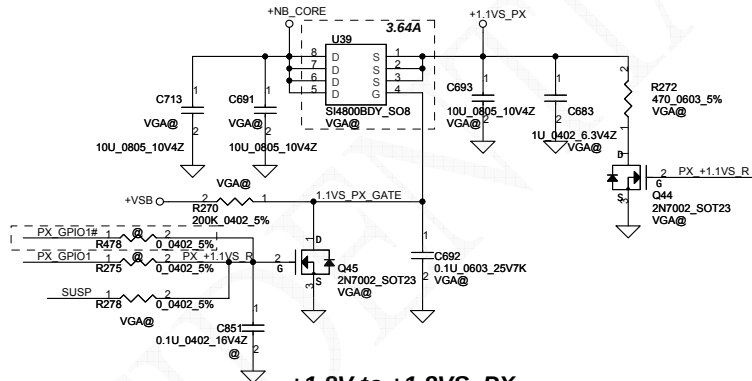
+3VALW TO +3VS



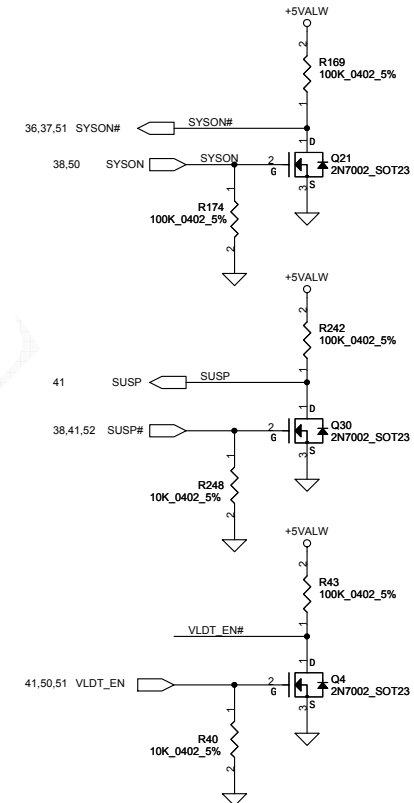
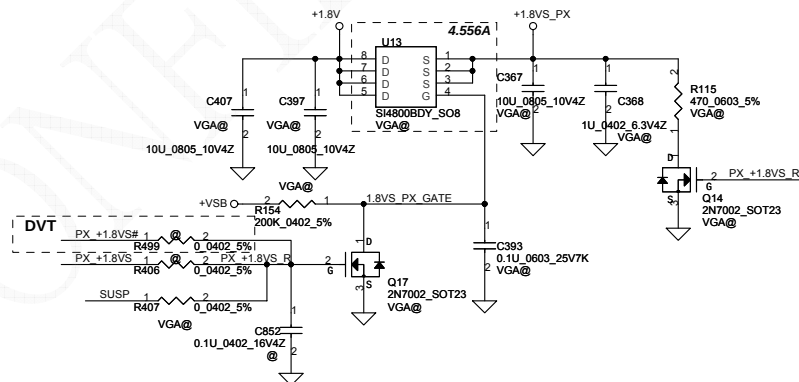
+1.8V to +1.8VS



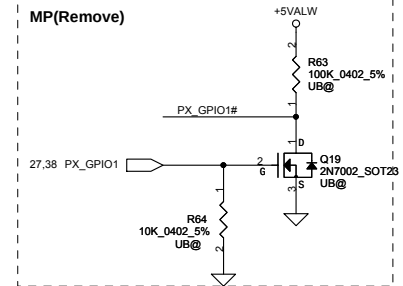
+NB_CORE TO +1.1VS_PX



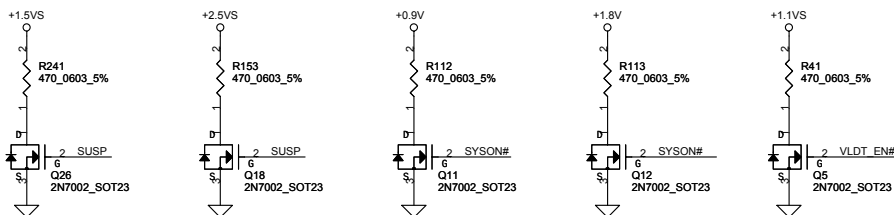
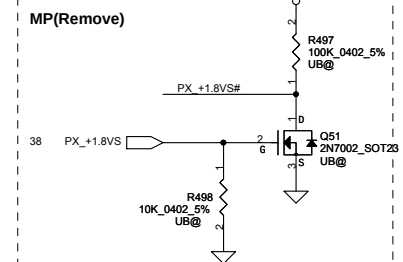
+1.8V to +1.8VS_PX



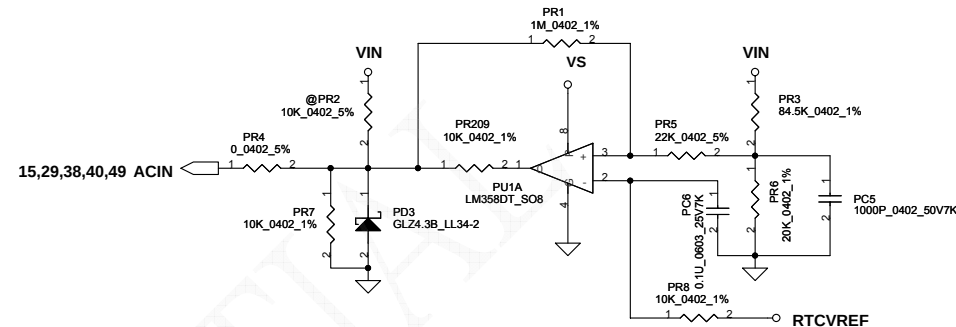
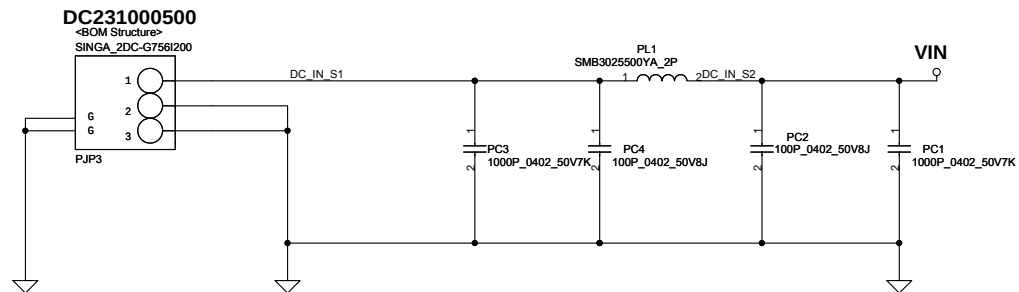
MP(Remove)



DVT MP(Remove)

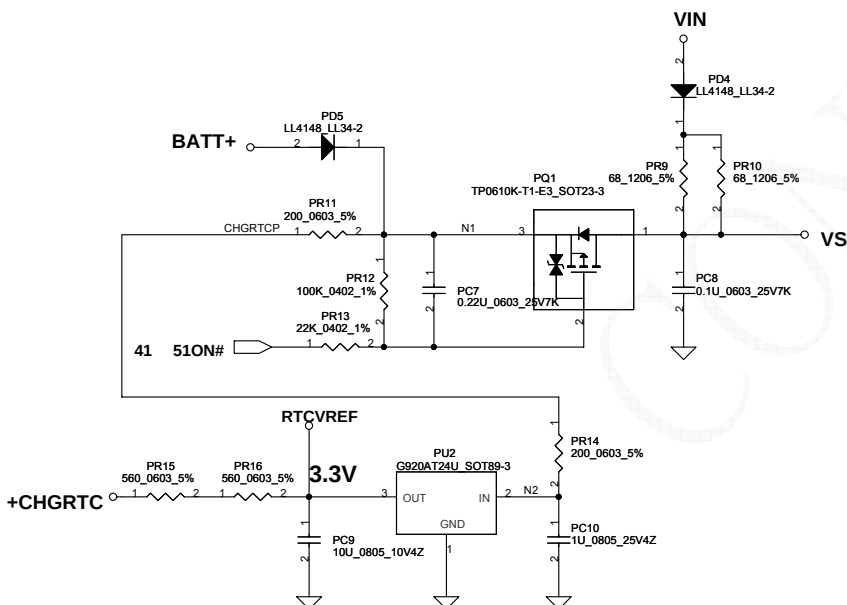
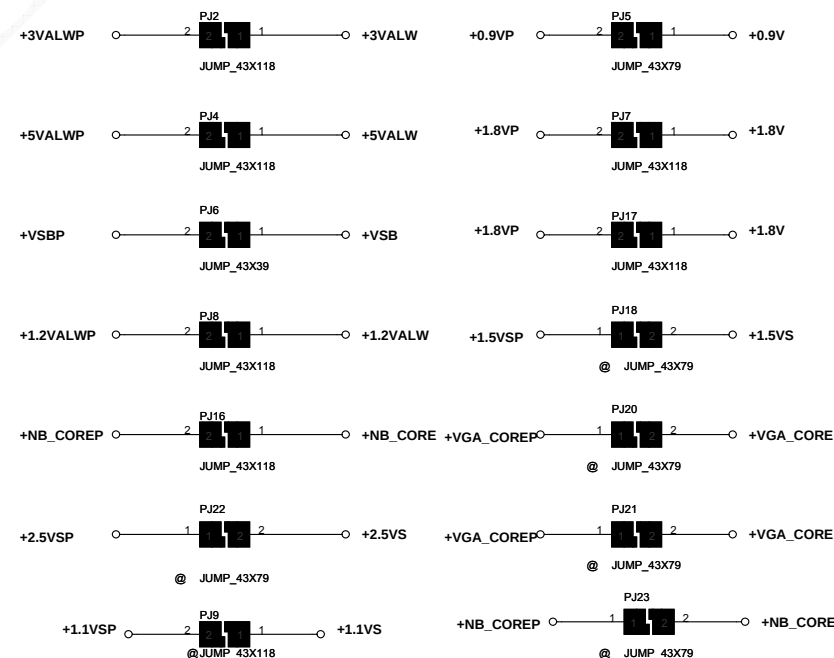
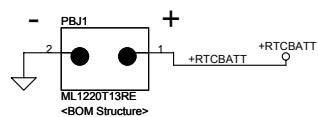


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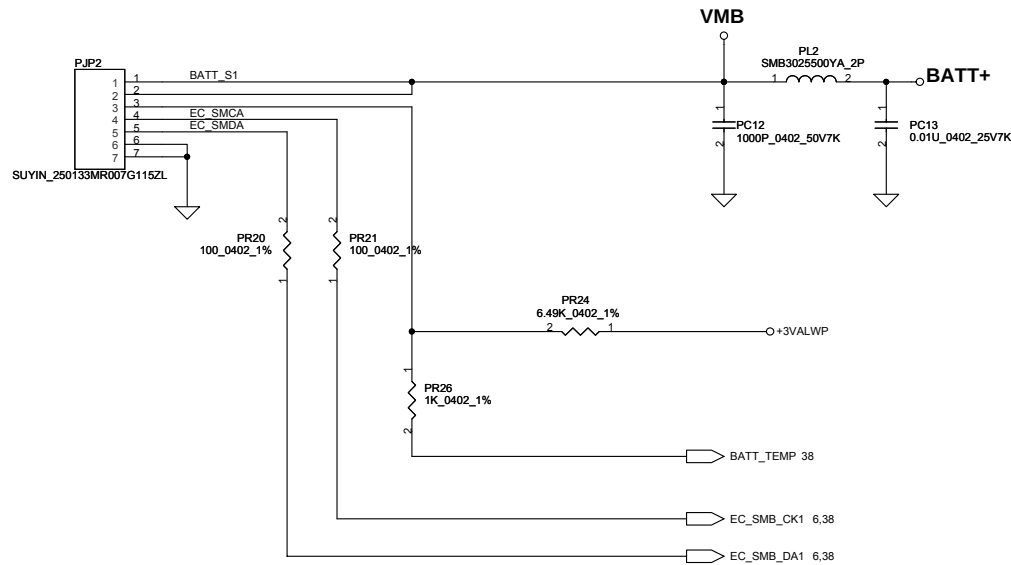


Vin Dectector

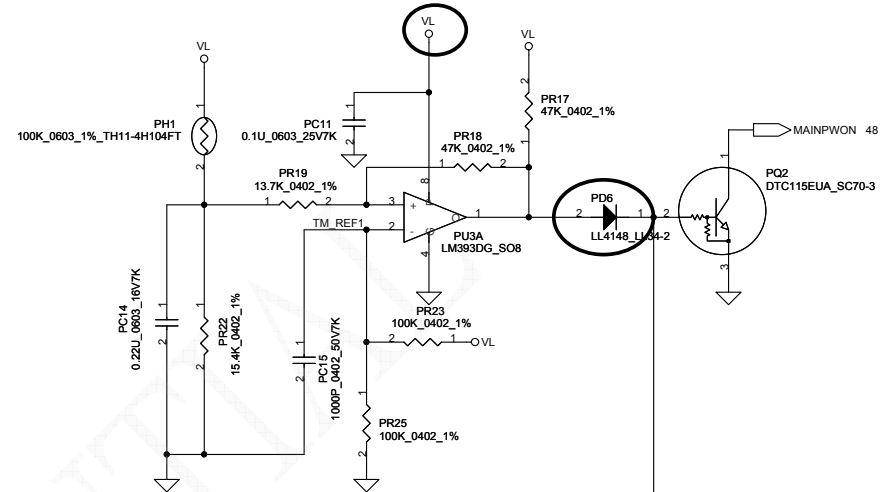
	Min.	Typ	Max.
H-->L	16.976V	17.525V	17.728V
L-->H	17.430V	17.901V	18.384V



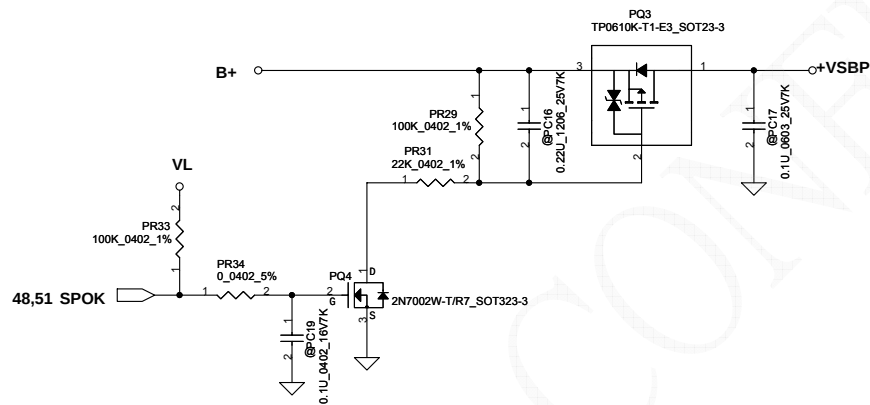
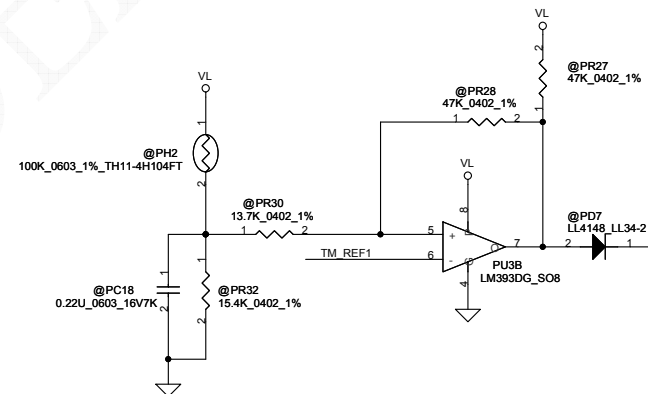
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PH1 under CPU botten side :
CPU thermal protection at 93 degree C
Recovery at 57 degree C



PH2 near main Battery CONN :
BAT. thermal protection at 79 degree C
Recovery at 47 degree C



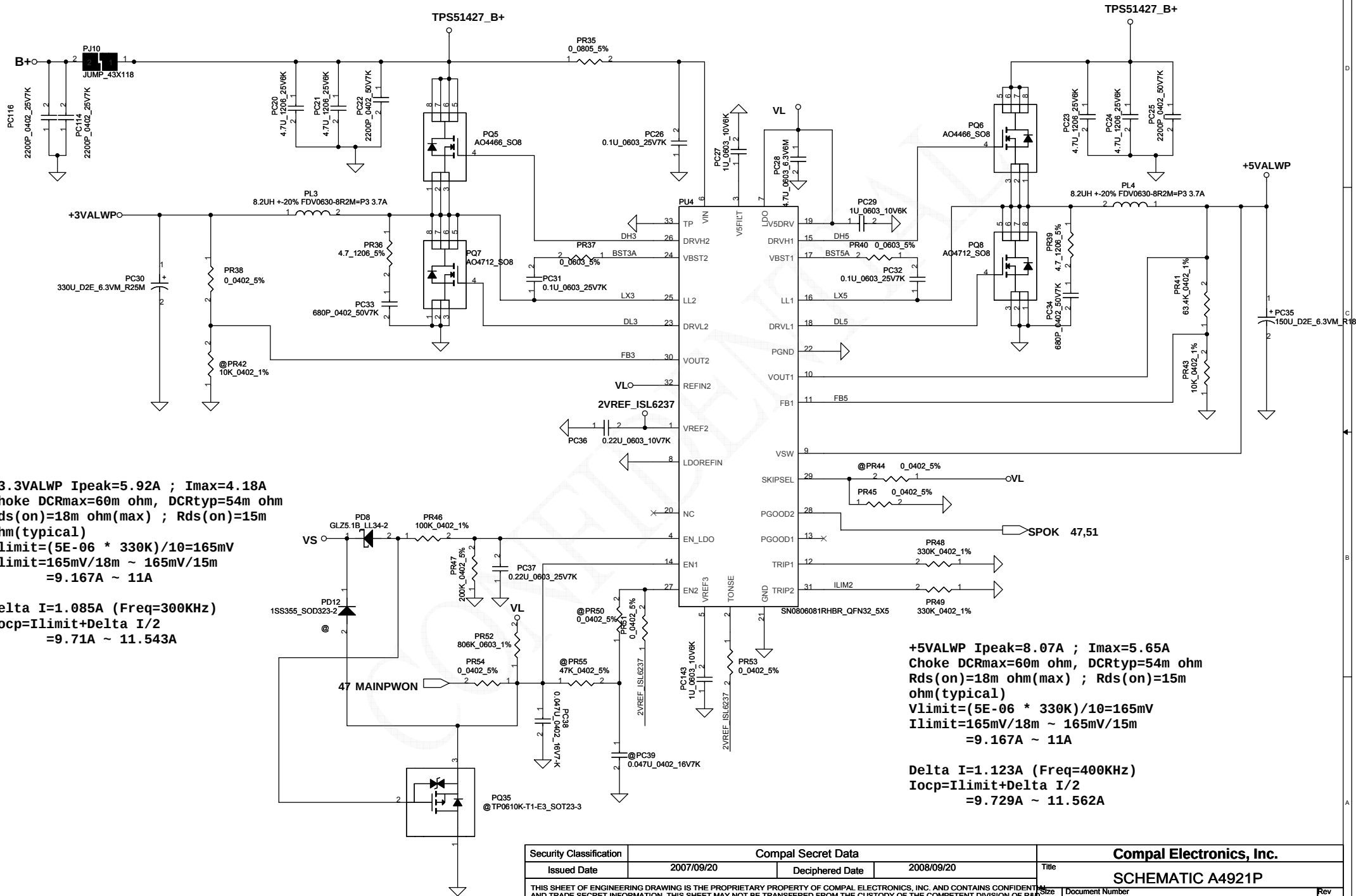
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+3.3VALWP Ipeak=5.92A ; I_{max}=4.18A
 Choke DCR_{max}=60m ohm, DCR_{typ}=54m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$

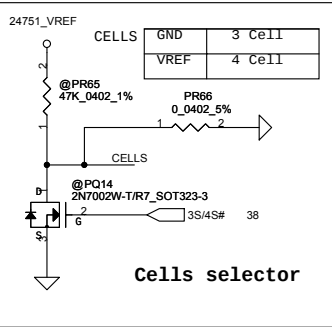
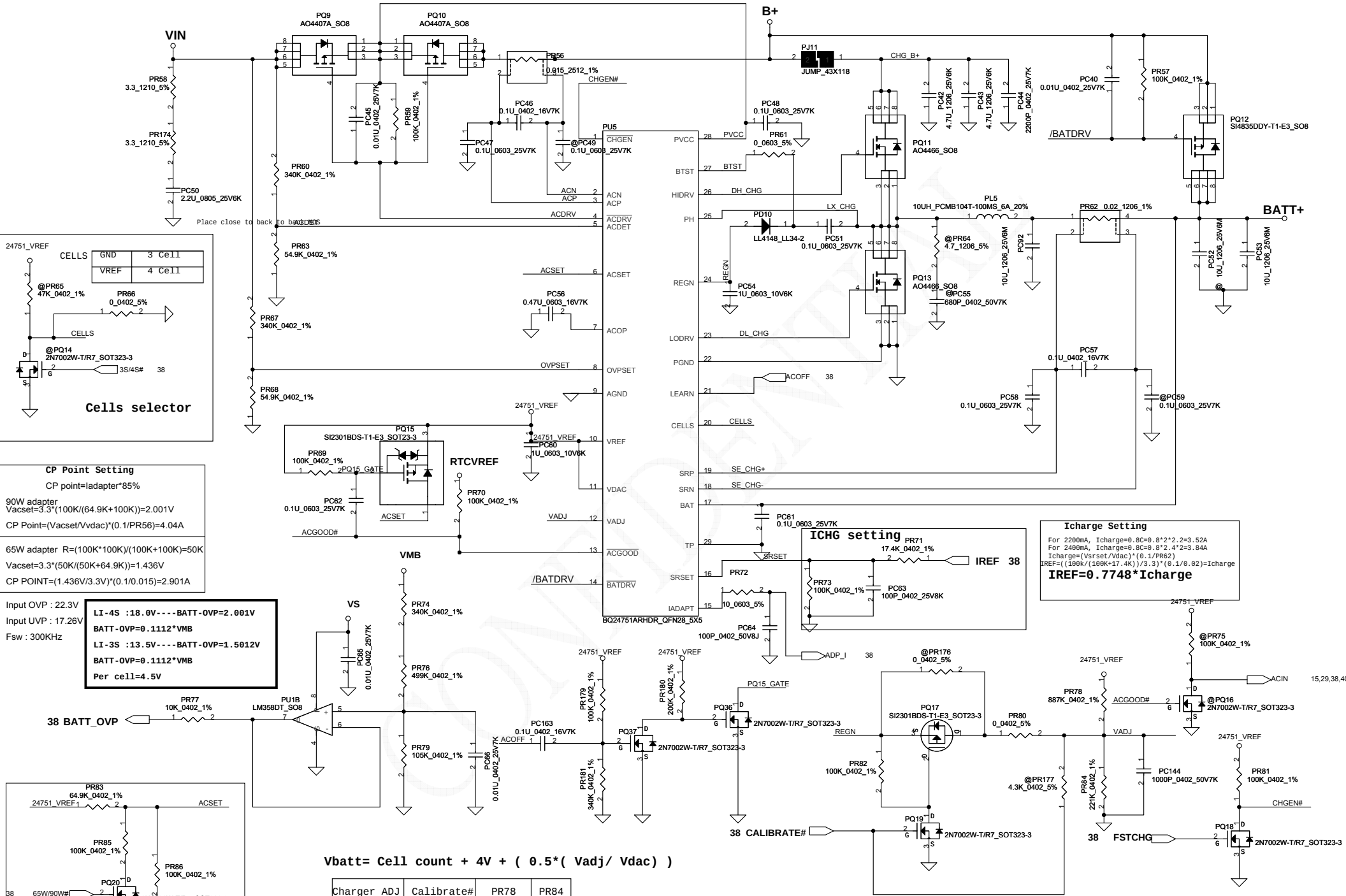
Delta I=1.085A (Freq=300KHz)
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 9.71A \sim 11.543A$

+5VALWP Ipeak=8.07A ; I_{max}=5.65A
 Choke DCR_{max}=60m ohm, DCR_{typ}=54m ohm
 R_{ds(on)}=18m ohm(max) ; R_{ds(on)}=15m ohm(typical)
 $V_{limit} = (5E-06 * 330K) / 10 = 165mV$
 $I_{limit} = 165mV / 18m \sim 165mV / 15m$
 $= 9.167A \sim 11A$

Delta I=1.123A (Freq=400KHz)
 $I_{ocp} = I_{limit} + \Delta I / 2$
 $= 9.729A \sim 11.562A$



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CP Point Setting
 CP point=ladapter*85%

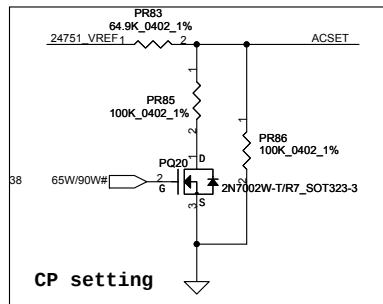
90W adapter
 $V_{acset}=3.3 \cdot (100K/(64.9K+100K))=2.001V$
 $CP\ Point=(V_{acset}/V_{vdac}) \cdot (0.1/PR56)=4.04A$

65W adapter $R=(100K \cdot 100K)/(100K+100K)=50K$
 $V_{acset}=3.3 \cdot (50K/(50K+64.9K))=1.436V$
 $CP\ POINT=(1.436V/3.3V) \cdot (0.1/0.015)=2.901A$

Input OVP : 22.3V
 Input UVP : 17.26V
 Fsw : 300KHz

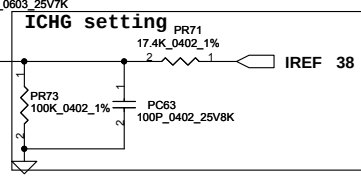
LI-4S : 18.0V----BATT-OVP=2.001V
BATT-OVP=0.1112*VMB

LI-3S : 13.5V----BATT-OVP=1.5012V
BATT-OVP=0.1112*VMB
 Per cell=4.5V



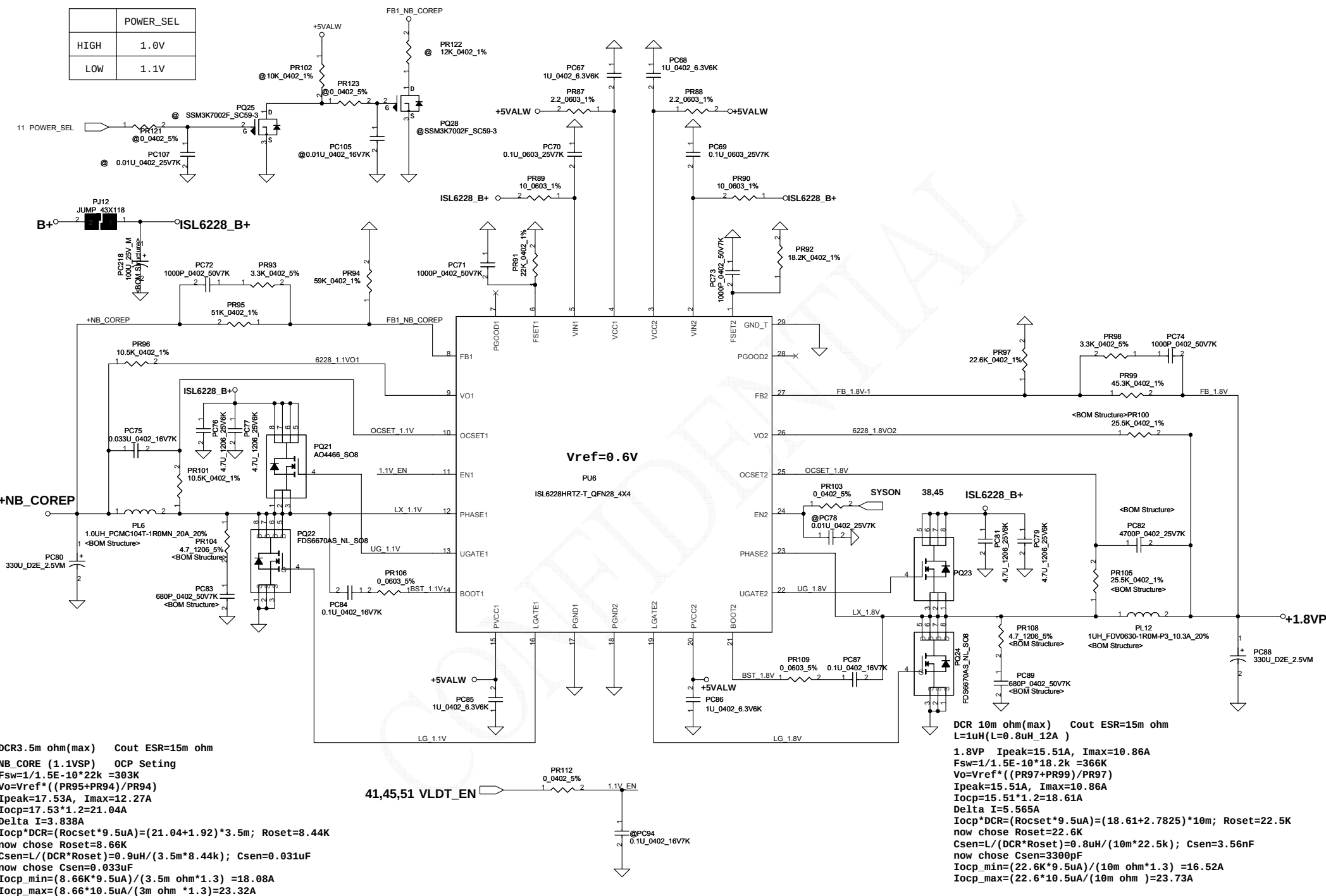
$$V_{batt} = \text{Cell count} + 4V + (0.5 \cdot (V_{adj} / V_{dac}))$$

Charger ADJ	Calibrate#	PR78	PR84
4.0V	L	@	@
4.1V	L	887K	221K
4.2V(1.32)	H	@	@

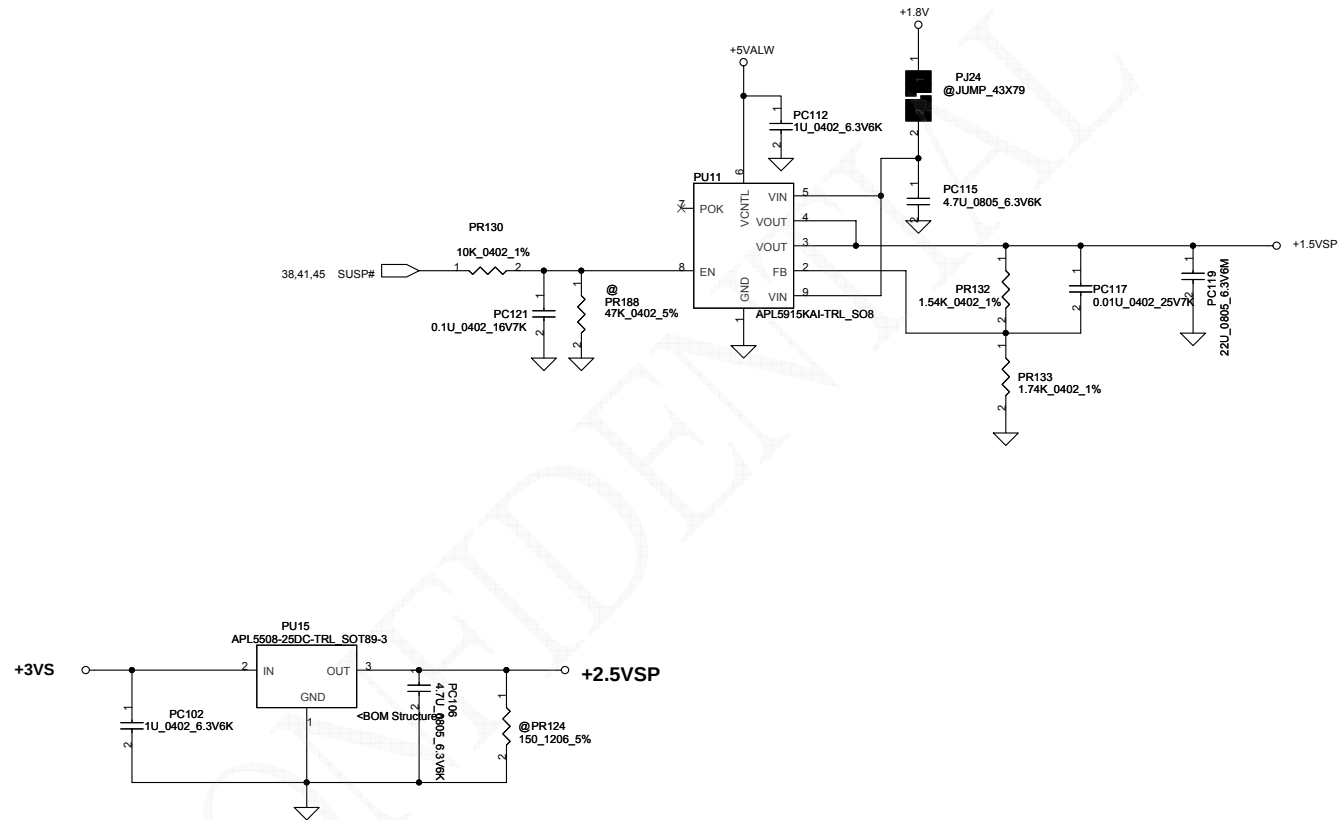


Icharge Setting
 For 2200mA, Icharge=0.8C=0.8*2.2=3.52A
 For 2400mA, Icharge=0.8C=0.8*2.4=3.84A
 $I_{charge}=(V_{srset}/V_{dac}) \cdot (0.1/PR62)$
 $IREF=(100K/(100K+17.4K))/3.3 \cdot (0.1/0.02)=I_{charge}$
IREF=0.7748*Icharge

	POWER_SEL
HIGH	1.0V
LOW	1.1V



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Item	Fixed Issue	Reason for change	Rev.	PG #	Modify List	Date	Phase
1	ADD circuit	Switch NB_core voltage	0.1	50	ADD PC107, PC105, PR121, PR123, PR122, PR102, PQ25, PQ28 at UMA Sku	2009/01/04	DVT
2	ADD circuit	Switch NB_core voltage	0.1	51	ADD PC110, PC111, PC108, PC109, PC1113, PR1128, PR194, PR129, PR127 at UMA Sku	2009/01/04	DVT
3	ADD snubber	EMI requestmrnt	0.1	50	Add PR104 4.7 ohm and PC83 680p	2009/01/04	DVT
4	ADD snubber	EMI requestmrnt	0.1	50	Add PR108 4.7 ohm and PC89 680p	2009/01/04	DVT
5	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR229 2.2 ohm	2009/01/04	DVT
6	ADD CPU boot	EMI requestmrnt	0.1	53	Add PR243 2.2 ohm	2009/01/04	DVT
7	Change resistance value	Switch NB_core voltage	0.1	50	Change PR95 from 51 Kohm to 39.2 Kohm	2009/01/04	DVT
8	Change resistance value	Switch NB_core voltage	0.1	50	Change PR122 from 12 Kohm to 226 Kohm	2009/01/04	DVT
9	Change resistance value	soft start of Switch NB_core voltage	0.1	50	Change PR123 from 0 ohm to 10 Kohm	2009/01/04	DVT
10	Change capacitor value	soft start of Switch NB_core voltage	0.1	50	Change PC105 from 0.01 uF to 0.1 uF	2009/01/04	DVT
11	Change IC part number	Change IC part number	0.1	48	Change PU4 part number to SA00002V400	2009/01/04	DVT

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PHASE	PAGE	MODIFICATION LIST			PURPOSE																						
D	DVT	P.6	Reserve R484/R485(0ohm_0402) for CPU SB temp sensor		Reserved EC SMBUS1 due to +3VS leakage when S3 entry with SMBUS2																						
		P.8	Add C174/C175/C176 (0.1u_0402)		EMI request																						
		P.10	C646/C647/C648/C649/C650/C651/C652/C653 with VGA@		BOM error																						
		P.11	Add R488/R489 (0ohm_0402) & reserve R491/R492 (0ohm_0402)		UMA HDMI I2C bus mainly to RS780MN DDC port1 & reserve to port0																						
		P.11	Reserve R490(0ohm_0402)		NA																						
C		P.12	Change L6/L7 from 0ohm_0805 as 0ohm_1206 & with VGA@		For DIS +1.1VS power source from fixed +NB_CORE																						
		P.22	Remove VRAM Samsung(Q-die) & Qimonda type		Customer request																						
		P.24	U35/R464/R465/C845/C846/C847/C848/C849 with @ & RP15 with UMA@		Separately as DIS sku only & UMA sku only																						
		P.24	Add RP20/RP21/RP22/RP23(0ohm_0404_4P2R) with VGA@		For DIS sku only																						
		P.24	Reserve Q52/R501/R502/R503		Reserve for UMA sku white screen flash when boot issue check																						
B		P.25	Change JHDMI1 from SMD type as DIP type(DC232000800)		DFX request																						
		P.25	Change single MOS as 2 dual N-ch MOS(Q53/Q54) & reserve R506		NA (Just no need to modify)																						
		P.26	R47/R58/U25/U26/C626/C628/R475 with UMA@ & R507 with VGA@ , U36/C850 with @ & delete R466 , add R493/R494/R495 with VGA@		Separately as DIS sku only & UMA sku only																						
		P.27	Add R496 with @ & R476/R482 with @		NA																						
		P.28	Add R509 with VGA@ & R510 with UMA@		Reserve SKU ID for SW even SW check device ID instead currently																						
A		P.29	Reserve C862/C863/C855/C856		Reserve eSATA function for future request																						
		P.37	Change JUSB1 as SB700 USB port6		Dedicated HS port on lower-left position																						
		P.38	Change U20 as KB926 D3 version (SA00001J580)		NA																						
		P.38	D41 with VGA@ & D42 with UMA@		Separately as DIS sku only & UMA sku only																						
		P.38	U20.85 defined as TP_LOCK_LED# feature		LED control simultaneously with Tutch-Pad locked function																						
	P.38	Change R194 as 8.2kohm_0402		Change board ID as 1 (PCB revision : 0.2)																							
		<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td></tr><tr><td>Issued Date</td><td>2008/10/06</td><td>Deciphered Date</td><td>2009/10/06</td></tr><tr><td colspan="4">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td></tr></table>				Security Classification	Compal Secret Data			Issued Date	2008/10/06	Deciphered Date	2009/10/06	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				<table><tr><td colspan="2">Compal Electronics, Inc.</td></tr><tr><td>Title</td><td>SCHEMATIC A4921P</td></tr><tr><td>Document Number</td><td>401679</td></tr><tr><td>Date:</td><td>Thursday, March 26, 2009</td></tr></table>		Compal Electronics, Inc.		Title	SCHEMATIC A4921P	Document Number	401679	Date:	Thursday, March 26, 2009
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PHASE	PAGE	MODIFICATION LIST	PURPOSE	
	P.39	Add R250/LED11/SW4	Add T/P lock button & T/P lock button LED	
	P.45	Reserve R499 , R497/R498/Q51	NA	
	P.45	Stuff R202	+1.2VALW leakage 640mv pulse when AC insertion & then might cause OVP	
	P.34	C26 with @ & C11 as SE070104Z80	NA	
	P.42	Stuff R446(0ohm_0805) & un-stuff U32(Audio LD0)	NA	
	DVT2	P.6	Remove CPU side-band(internal) temp sensor function	NA
	P.11/38	Add U49/C857/R744 (Reserve U48) & D42 with @, remove D42	NA	
	P.23/34	Add R676 for CLK_48M_SD , reserve R715 / R716 for CLK_48M_LAN	NA	
	P.24	Add R508(2.7K_0402) for ENVDD of UMA sku	NA	
	P.28	SB700 USB port 4 for Realtek RTS5159 card reader	NA	
	P.33	Add(co-layout) Realtek RTS5159 card reader	NA	
	P.37	Change JSAT1 PCB footprint as TYCO_1909574-1_11P-T	NA	
	P.38	R194 change as 18K_0402	Change board ID as 2 (PCB revision : 0.3)	
	P.40	LED1 / 5 / 8 / 9 /10 PCB footprint change as LED_HT-297DQ-GQ_4P	For DFX	
	P.44	Add H28 & H29	For thermal	
	PVT	P.11	Add R511 with @ & U50	For LCD white screen flash when coldboot issue
	P.11	Add C874 / C875 (1u_0402)	For CRT(acer lab) flicker	
	P.11/38	C857 / U49 with @ , R744 / D42 with UMA@	NA	
	P.42	Add L94(SM010027780) close to audio codec	For EMI	
	P.40	Modify LED 1 / 5 / 8 from dual Blue/Amber LED as single Blue LED	Follow acer spec	
	P.39/40	Modify R12/R13/R17/R16 (300->220ohm) , modify R1/R2/R3 (1.2K->866ohm) , modify R10 (300->715ohm) , modify R245/R247 (4.99K->750ohm) , modify R244/R246 (4.99K->866ohm) , modify R250 (1.2K->5.1K)	For LED brightness test	
	P.23	Change LAN_CLKREQ# from U18.51 to U18.24 output	NA	
	NA	Change test pad (execpt T8/T13/T15/T17/T18/T24/T28 /T29/T33/T45/T46/T48/T50/T56/T57/T12) from TPC12 to TPC24		
	P.36	Reserve Q55 / Q56 / R745 / R746 / R747 / C876 to turn off power of finger printer		
	P.38	R194 change as 18K_0402 for change board ID as 3 (PCB revision : 0.4)		
	MP	Search for MP font		

PCB

PCB 047 LA-4921P REV1 M/B

LA4921MB Rev0: DA80000DP00

LA4921MB Rev1: DA80000DP10

LA4921MB with Sub/B Rev1: DAZ07R00100

For TIGRIS

For Discrete(CRT)

For Discrete(HDMI)

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