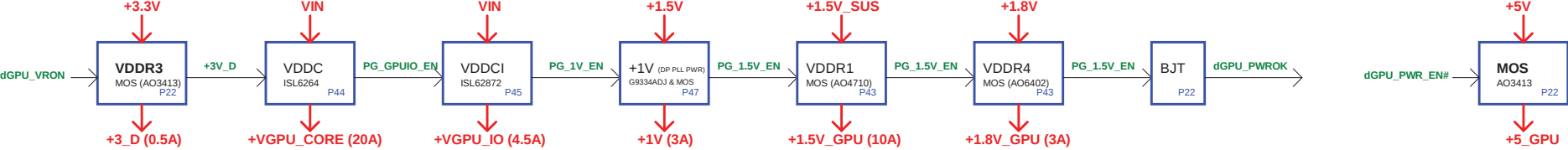
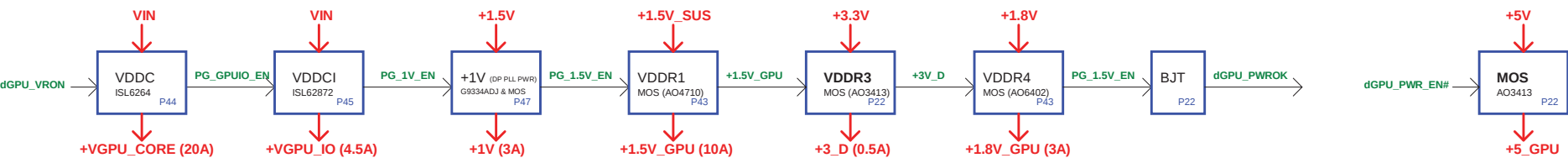


GPU PWR CTRL Option 1 (Default/ VDDR3 before VDDC)



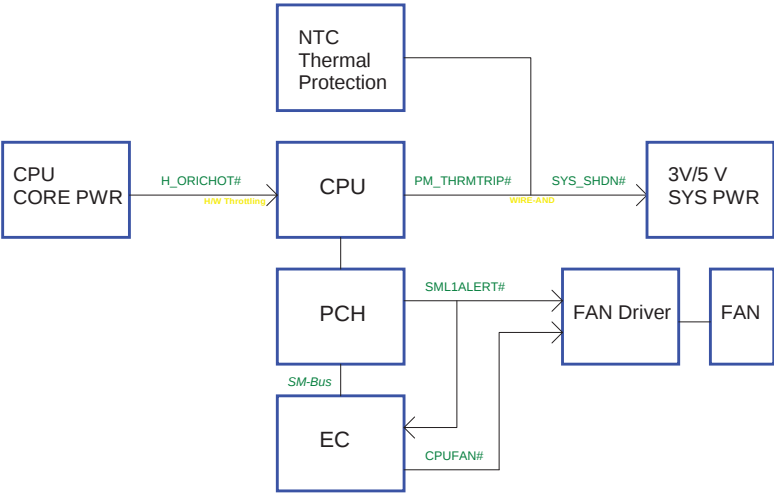
GPU PWR CTRL Option 2 (VDDR3 after VDDR1)



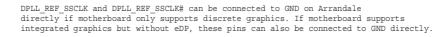
Power States

POWER PLANE	VOLTAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	+10V~+19V	MAIN POWER	ALWAYS	ALWAYS
+VCCRTC	+3V~+3.3V	RTC POWER	ALWAYS	ALWAYS
+3VPCU	+3.3V	EC POWER	ALWAYS	ALWAYS
+5VPCU	+5V	CHARGE POWER	ALWAYS	ALWAYS
+15V	+15V	CHARGE PUMP POWER	ALWAYS	ALWAYS
+3V_S5	+3.3V	LAN/BT/CIR POWER	S5_ON	S0-S5
+5V_S5	+5V	USB POWER	S5_ON	S0-S5
+5V	+5V	HDD/ODD/Codec/TP/CRT/HDMI POWER	MAINON	S0
+3V	+3.3V	PCH/GPU/Peripheral component POWER	MAINON	S0
+1.5VSUS	+1.5V	CPU/SODIMM CORE POWER	SUSON	S0-S3
+0.75V_DDR_VTT	+0.75V	SODIMM Termination POWER	MAINON	S0
+VGFX_AXG	variation	Internal GPU POWER	GFX_ON	S0
+1.8V	+1.8V	CPU/PCH/Braidwood POWER	MAINON	S0
+1.5V	+1.5V	MINI CARD/NEW CARD POWER	MAINON	S0
+1.1V_VTT	+1.05V or +1.1V	CPU VTT POWER	MAINON	S0
+1.05V	+1.05V	PCH CORE POWER	MAINON	S0
+VCC_CORE	variation	CPU CORE POWER	VRON	S0
LCDVCC	+3.3V	LCD POWER	LVDS_VDDEN	S0
+5V_GPU	+5V	SWITCHABLE PWM IC POWER	dGPU_PWR_EN#	Discrete enable
+GPU_CORE	+0.9V~+1.1V	GPU CORE POWER	+3V_D	Discrete enable
+GPU_IO	+0.9V~+1.1V	GPU I/O POWER	PG_GPUIO_EN	Discrete enable
+1.5V_GPU	+1.5V	VRAM CORE POWER	PG_1.5V_EN	Discrete enable
+1.8V_GPU	+1.8V	GPU_CRE/LVDS/PLL POWER	+1.5V_GPU	Discrete enable
+1V	+1V	DP/PEG POWER	PG_1V_EN	Discrete enable

Thermal Follow Chart

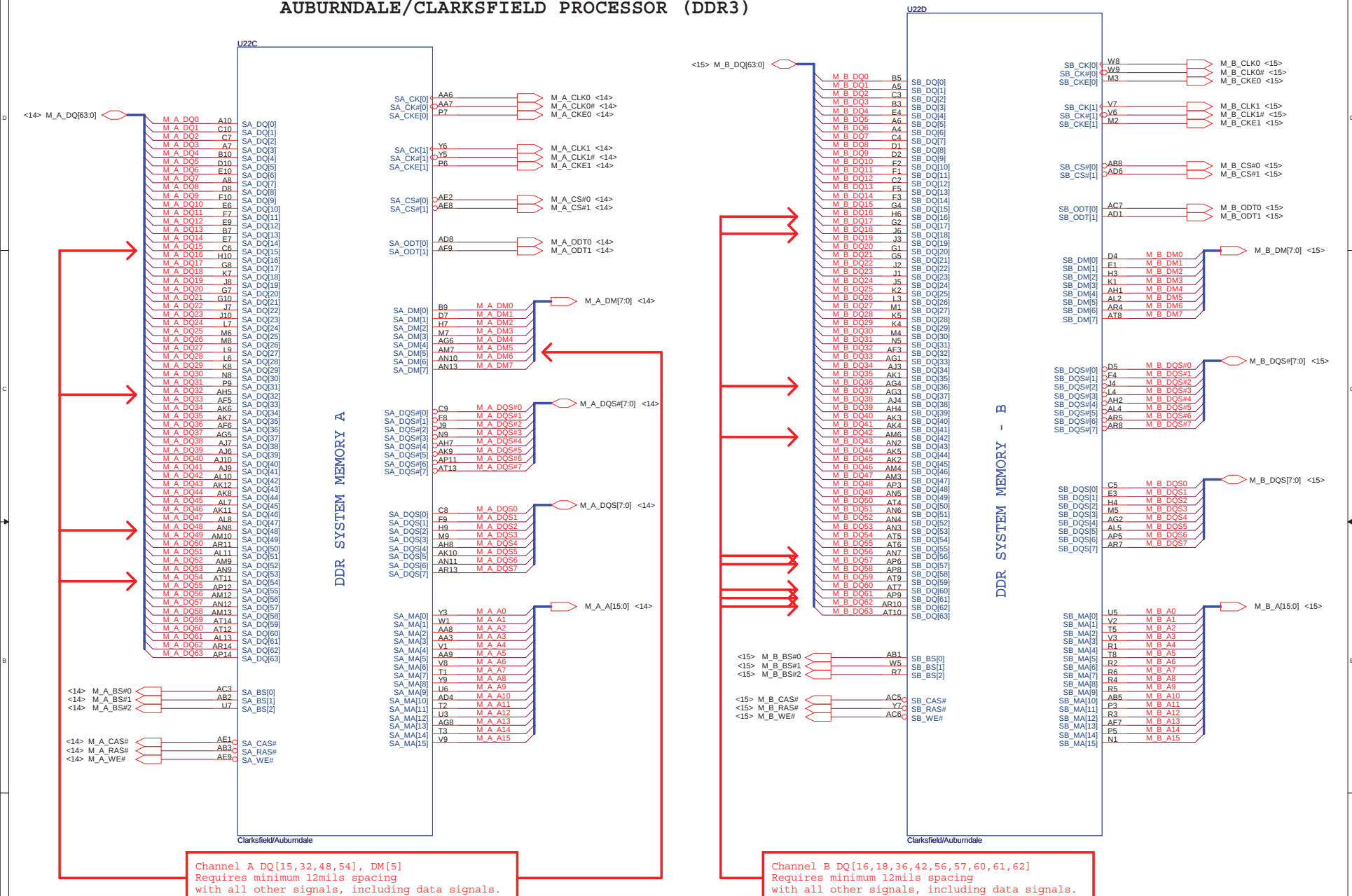


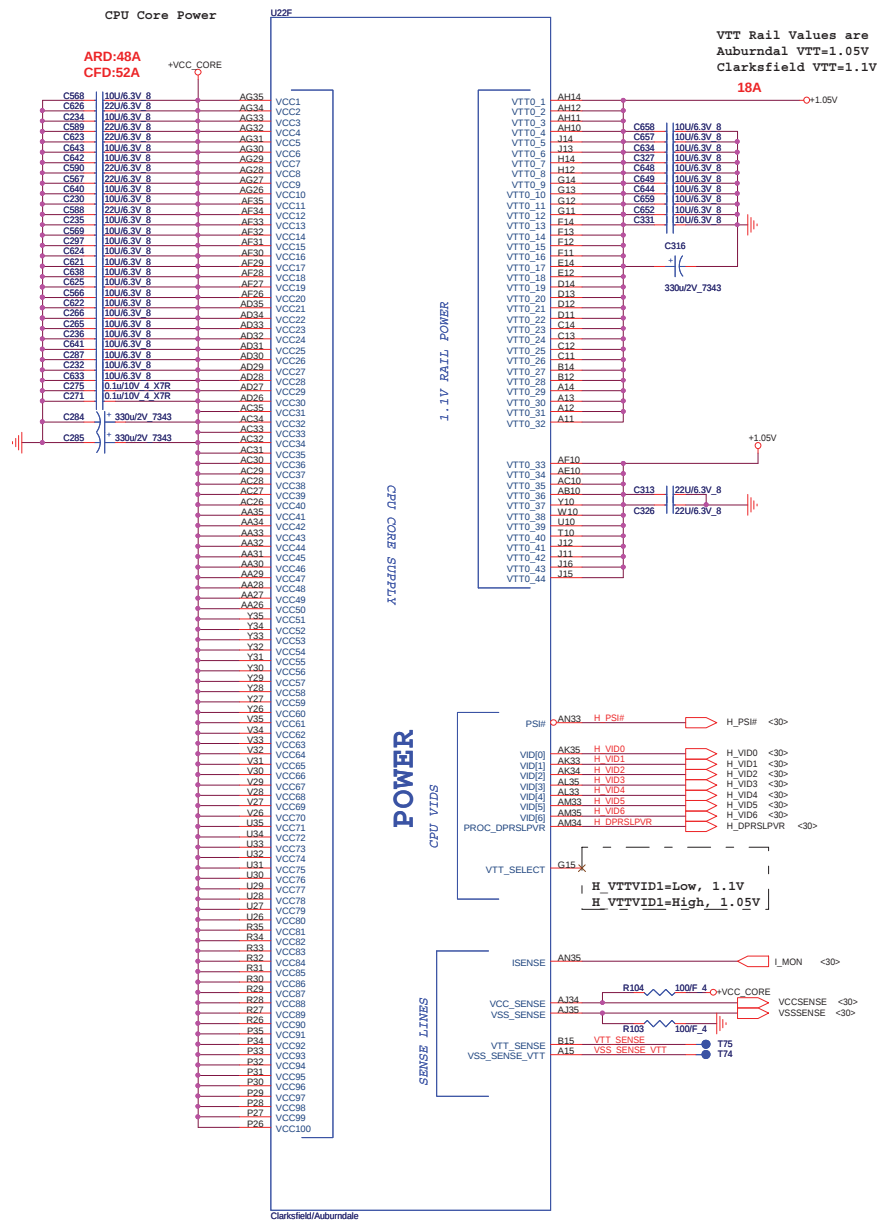
AUBURNDALE/CLARKSFIELD PROCESSOR (CLK,MISC,JTAG)



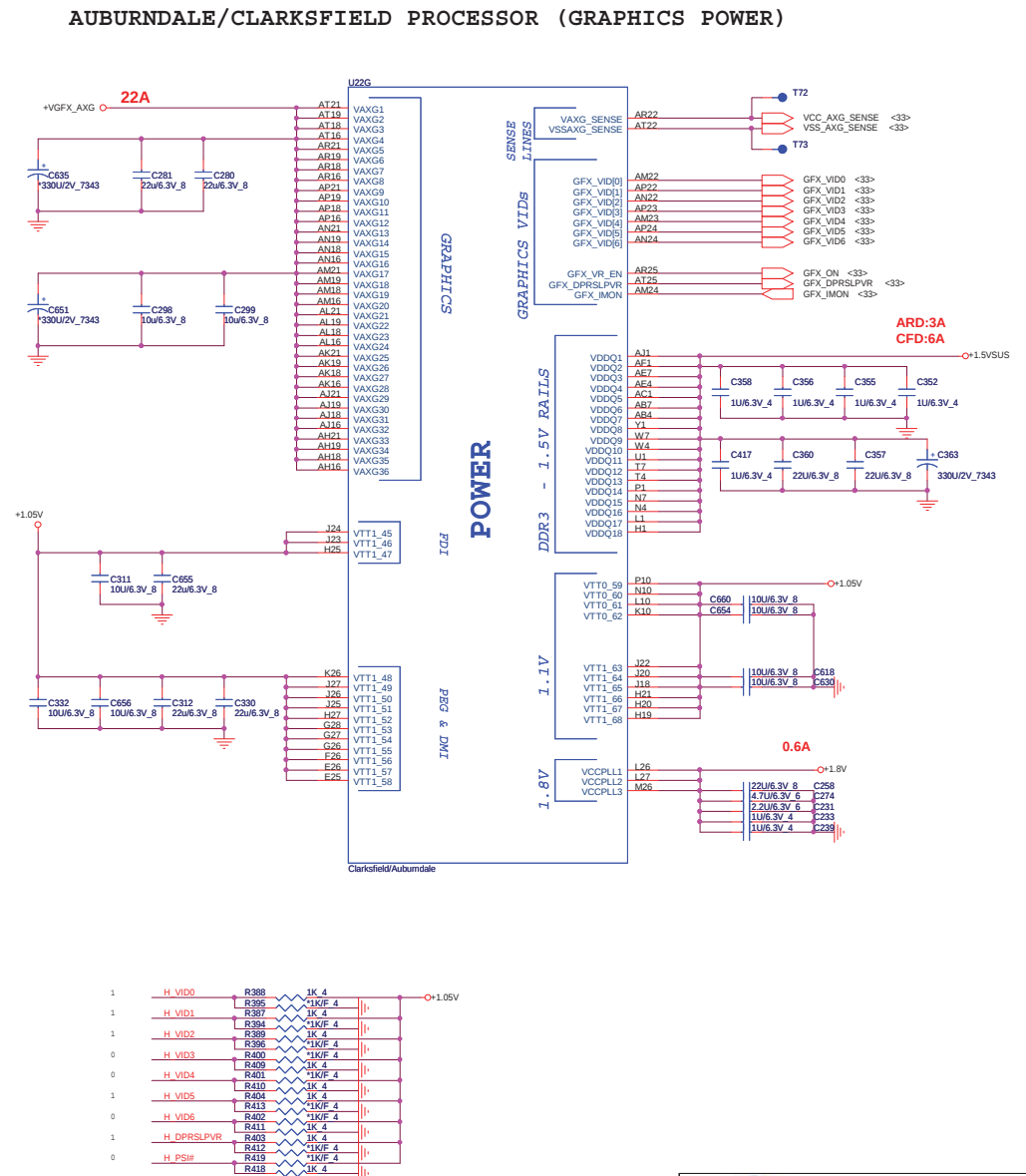
 Quanta Computer Inc. PROJECT : ZQH			Rev 1
Size	Document Number AUBURNA 1/4		

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)



Note:
For Validating IMVP VR R6451 should be STUFF
and R2N1 NO_STUFF

```
HFM_VID : Max 1.4V
LFM_VID : Min 0.65V
```



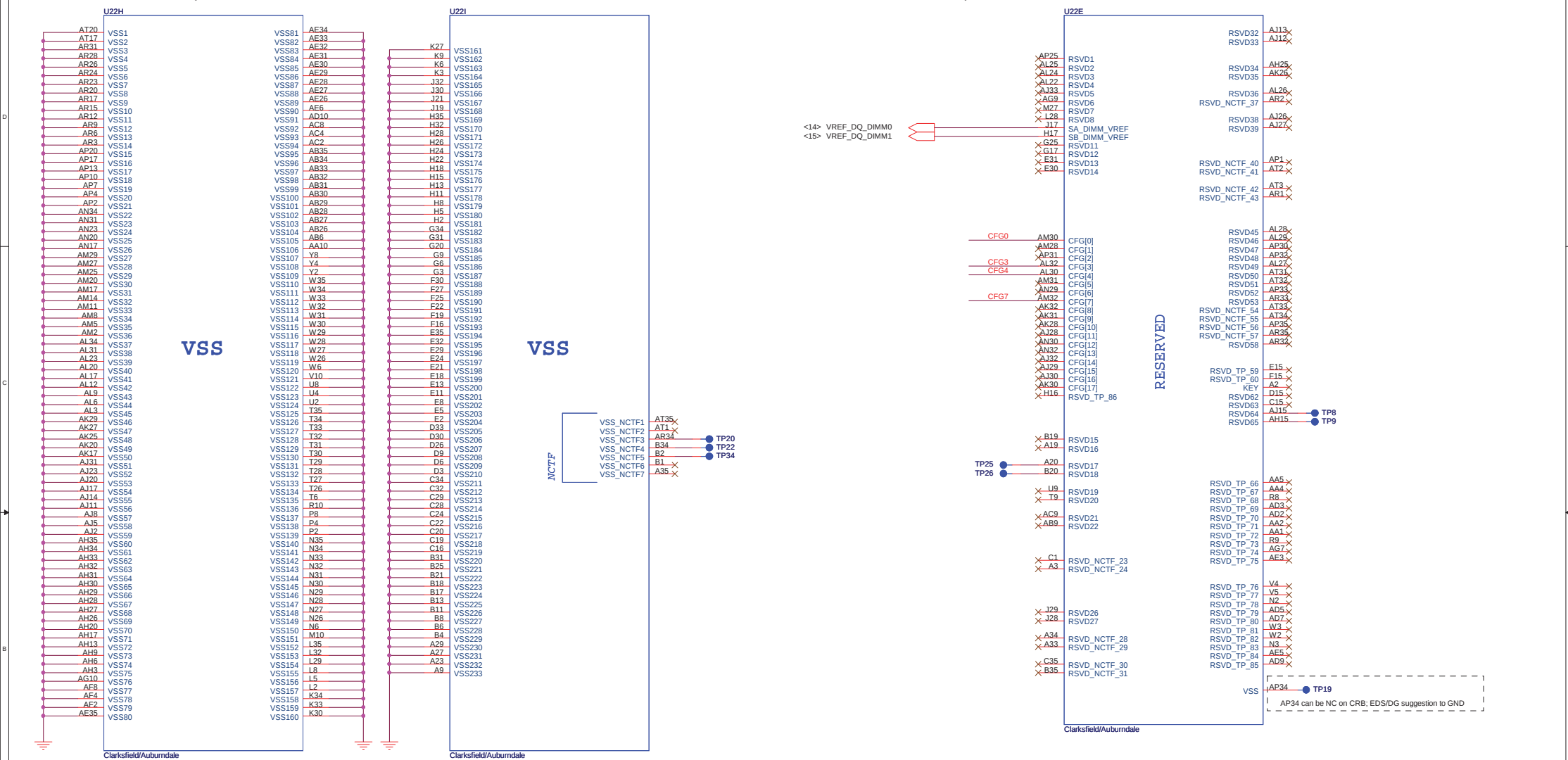
Quanta Computer Inc.

PROJECT : ZQH

Size	Document Number	Rev
	AUBURND 3/4 (PWR)	1A
Date:	Monday, March 14, 2011	Sheet 6 of 45

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)

AUBURNDALE/CLARKSFIELD PROCESSOR (RESERVED, CFG)

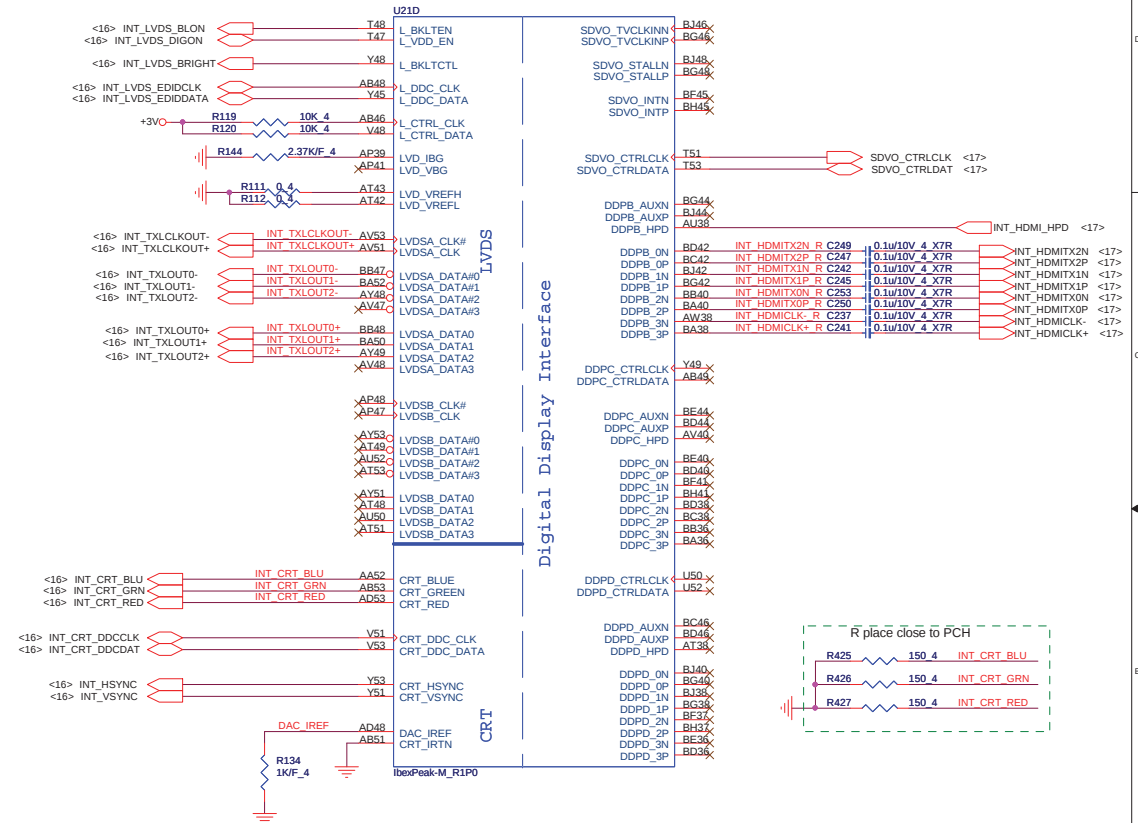


Processor Strapping

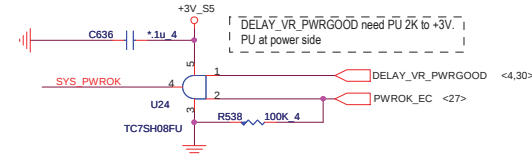
	1	0	DEFAULT	
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled	1	CFG0 R128 $\sim$ 3.01K NC
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed	1	CFG3 R125 $\sim$ 3.01K/F 4
CFG4 (Embedded Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port	1	CFG4 R127 $\sim$ 3.01K
T h b e t t e r				CFG7 R126 $\sim$ 3.01K/F 4

AC-coupling CAP place close to PCH

IBEX PEAK-M (LVDS, DDI)



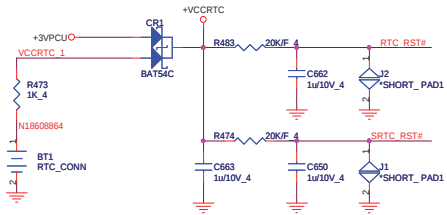
System PWR_OK



PROJECT : ZQH

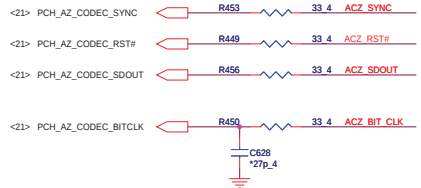
Size	Document Number IBEX PEAK-M 1/6	Rev 1A
Date:	Monday, March 14, 2011	Sheet 8 of 45

RTC Circuitry

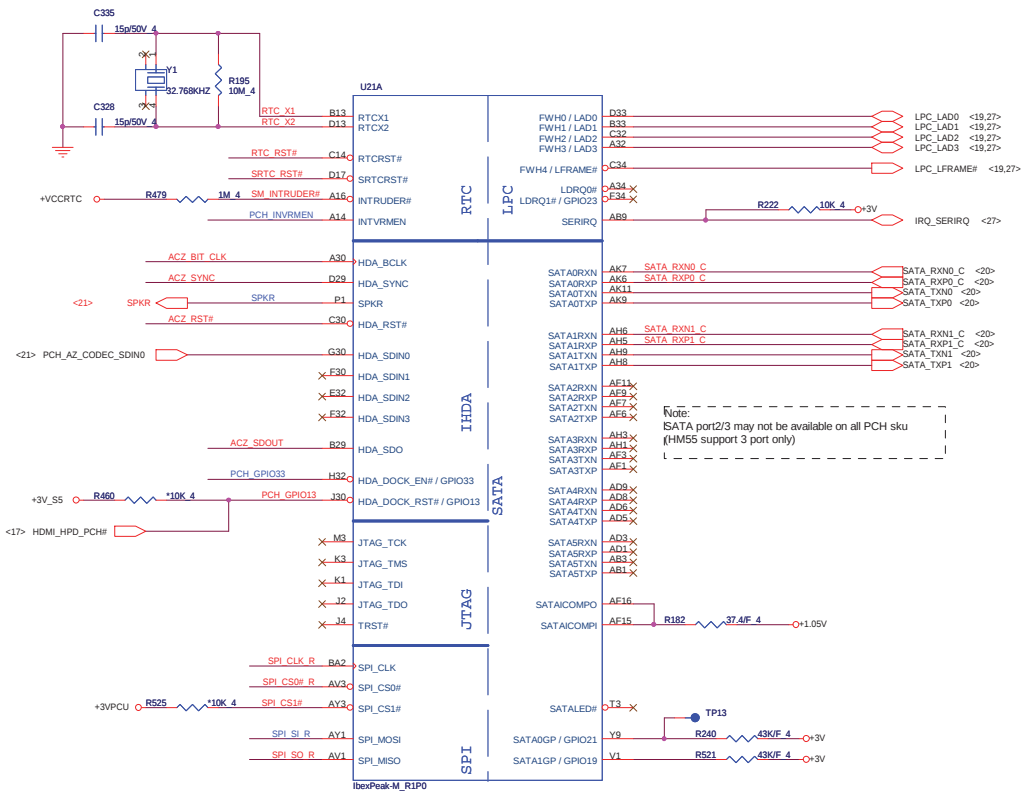
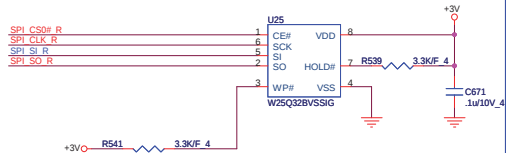


HDA_SYNC (PCH strap pin)
 Internal weak pull-down
 VCCVRM=>+1.8V (default)
 external pull-up
 VCCVRM=>+1.5V

HDA Bus

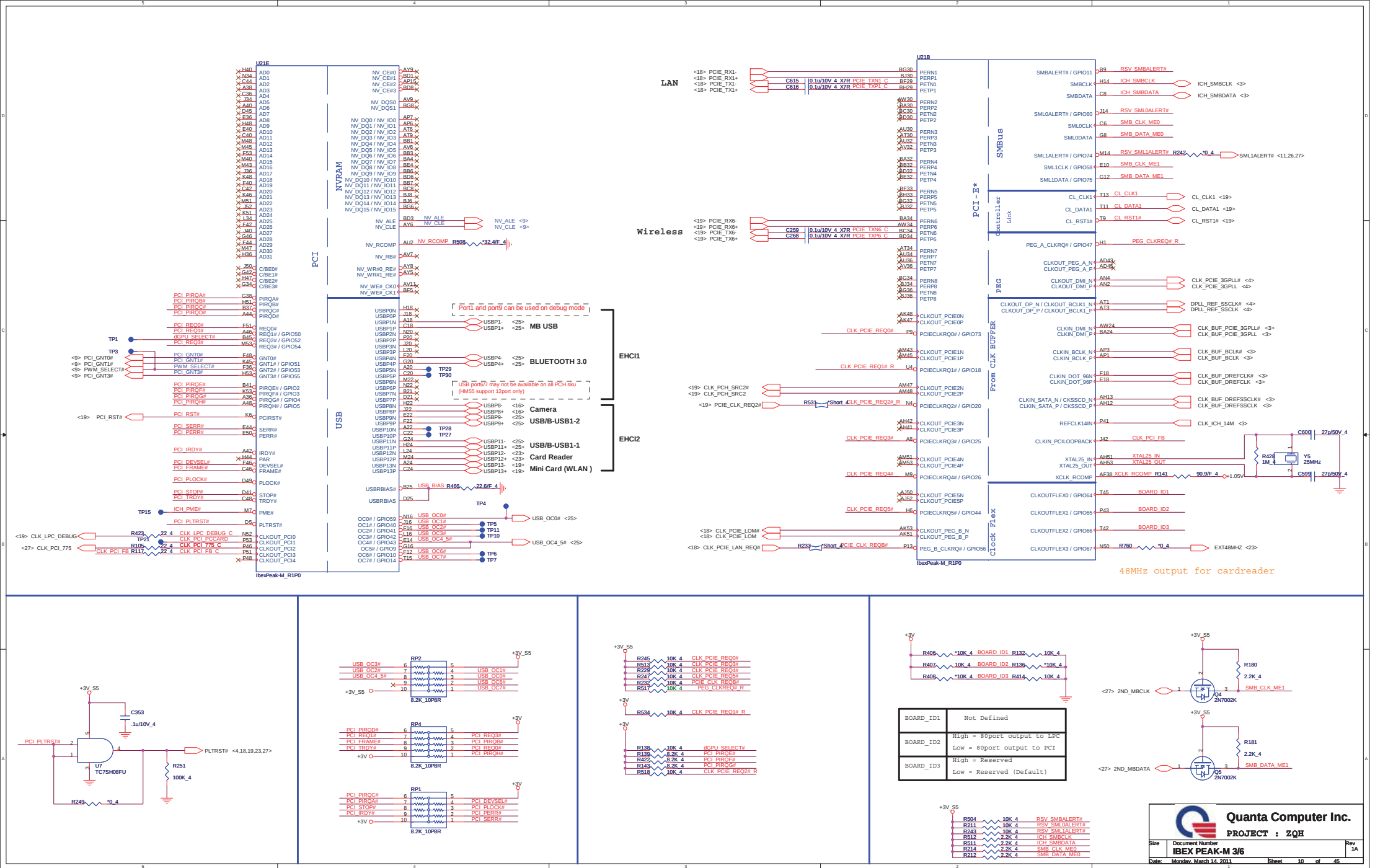


PCH SPI

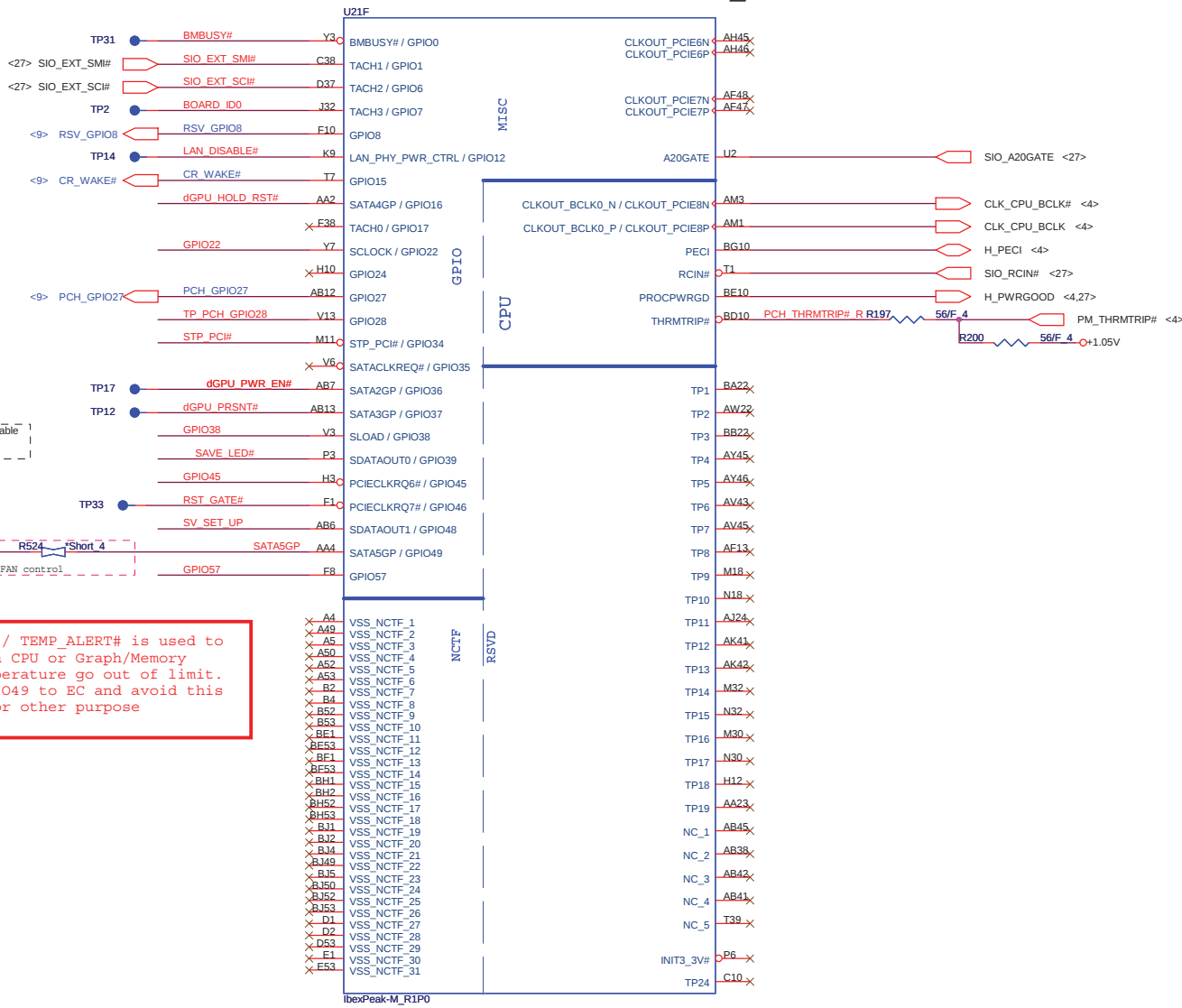


PCH Strap Pin Configuration Table-1

INTVRMEN	Integrated 1.05V VRM Enable / Disable	1 = Integrated VRM is enabled 0 = Integrated VRM is disabled	+VCCRTC R489 330K 6 PCH_INVNRMEN
SPI_MOSI	TPM Functionality Disable	1 = Enabled 0 = Disable	+3V R540 1K 4 SPI_SI_R
SPKR	Reboot option at power-up	0 = Default Mode (Internal weak Pull-down) 1 = No Reboot Mode with TCO Disabled	+3V R532 1K 4 SPKR
HDA_DOCK_EN# / GPIO33	Flash Descriptor Security Override	0 = Flash Descriptor Security will be overridden 1 = Security measure defined in the Flash Descriptor will be enabled.	PCH_GPIO33 R164 1K 4 R146 10K 4
GNT0#, GNT1#	Boot BIOS Strap	(0,0) = LPC (0,1) = Reserved NAND (1,0) = PCI (1,1) = SPI	R129 1K 4 R122 1K 4 R123 1K 4 R131 1K 4
GNT2# / GPIO53	ESI Strap (Server Only)	ESI compatible mode is for server platforms only	PWM_SELECT# R158 1K 4
GNT3# / GPIO55	Top-Block Swap Override	0 = Top Block Swap Mode 1 = Default Mode (Internal pull-up)	PCI_GNT3# R421 10K 4
NV_ALE	IntelR Anti-Theft Technology HDD Data Protection (Intel AT-d) Enable	1 = Enabled 0 = Disabled (Default)	NV_ALE R202 1K 4
NV_CLE	DMI Termination Voltage	DMI termination voltage. Weak internal pull-up. Do not pull low.	NV_CLE R206 1K 4
GPIO8	Reserved	This signal has a weak internal pull up. NOTE: This signal should not be pulled low	SV_GPIO8 R204 10K 4 R203 1K 4
GPIO15	Reserved	0 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality 1 = Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality	CR_WAKE# R244 1K 4
GPIO27	On-Die PLL Voltage Regulator	0 = Disables the VccVRM. 1 = Enables the internal VccVRM to have a clean supply for analog rails.	PCH_GPIO27 R221 10K 4

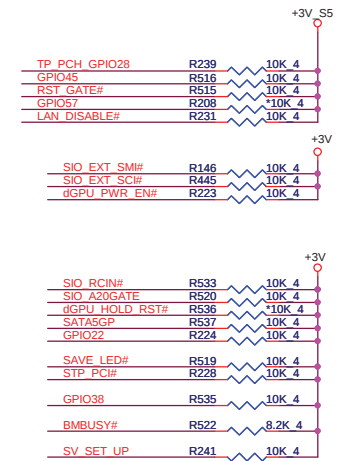


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)

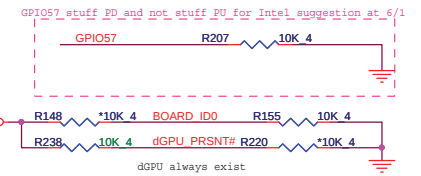


GPU RST#

GPIO Pull-up/Pull-down



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

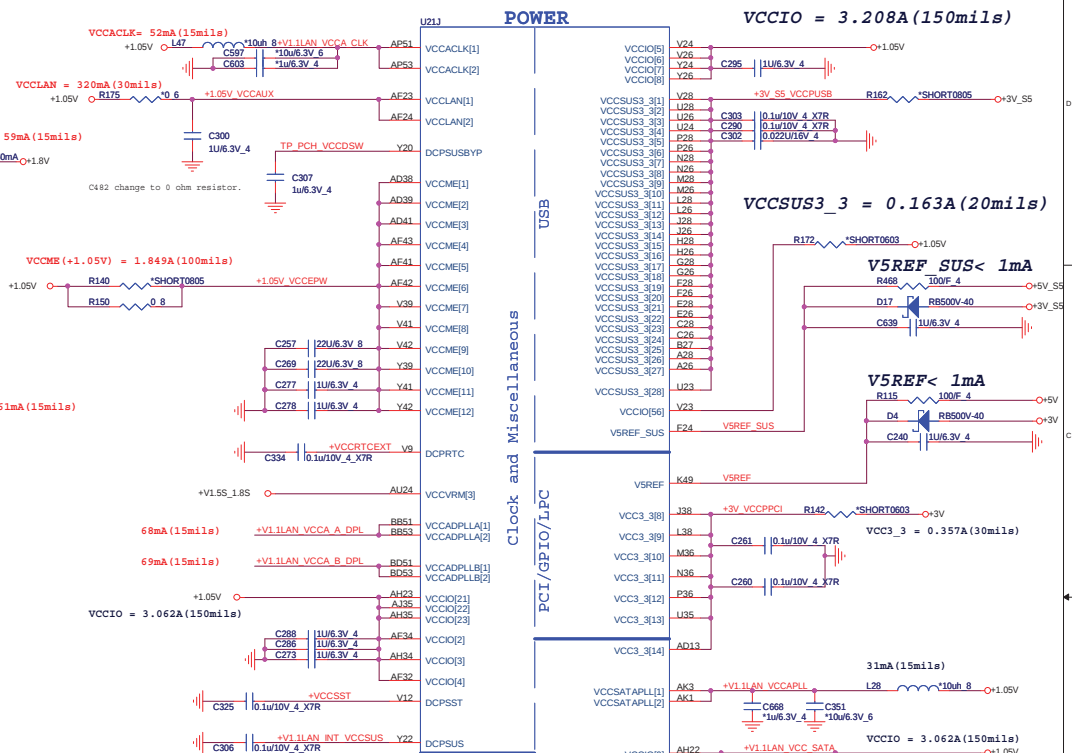
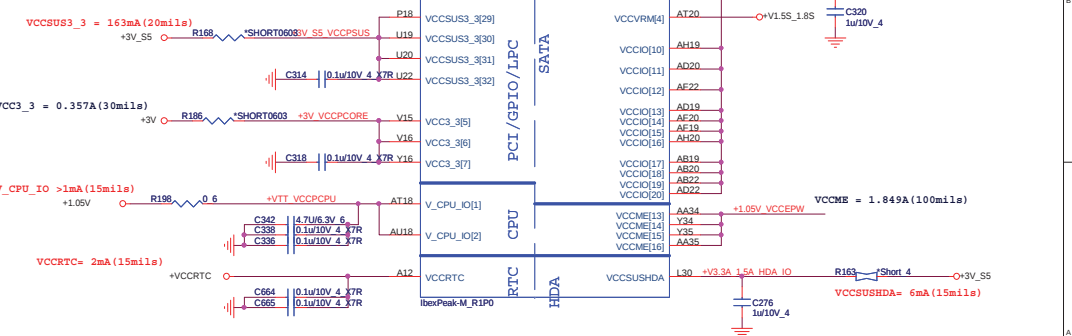


BOARD_ID#	High = 15"
	Low = 14"
RSV_GPIO8	High = Disable
	Low = Enable

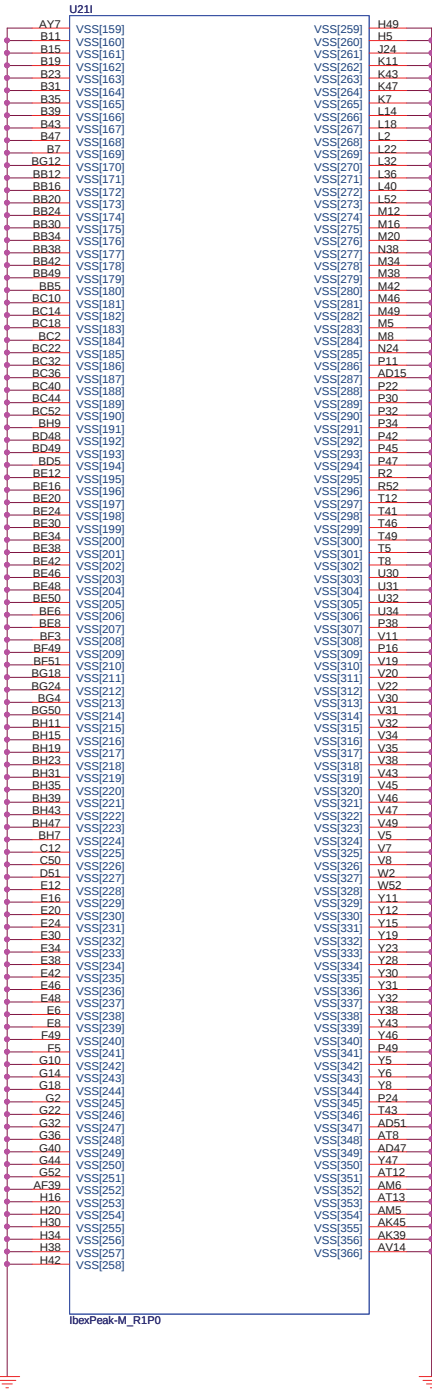
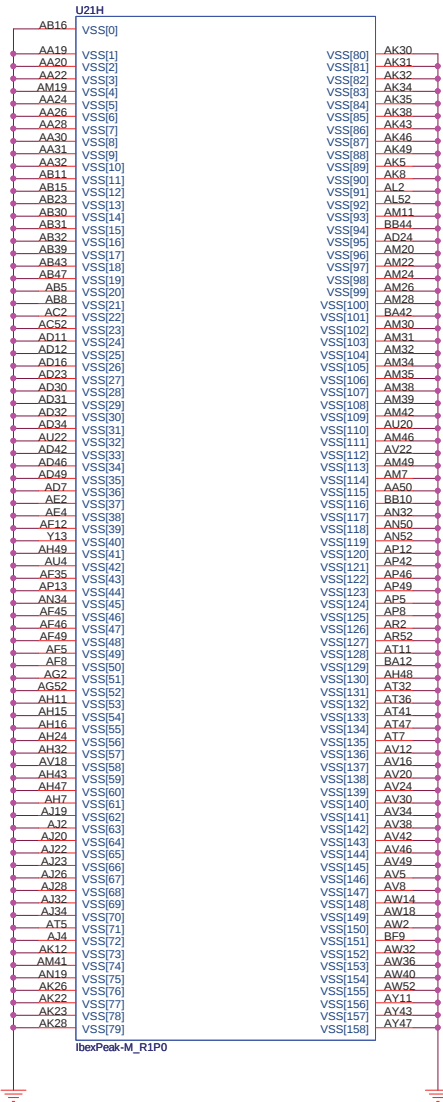


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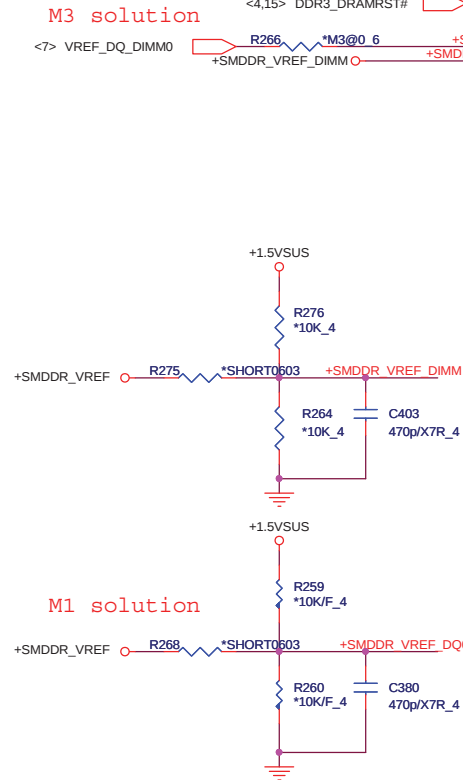
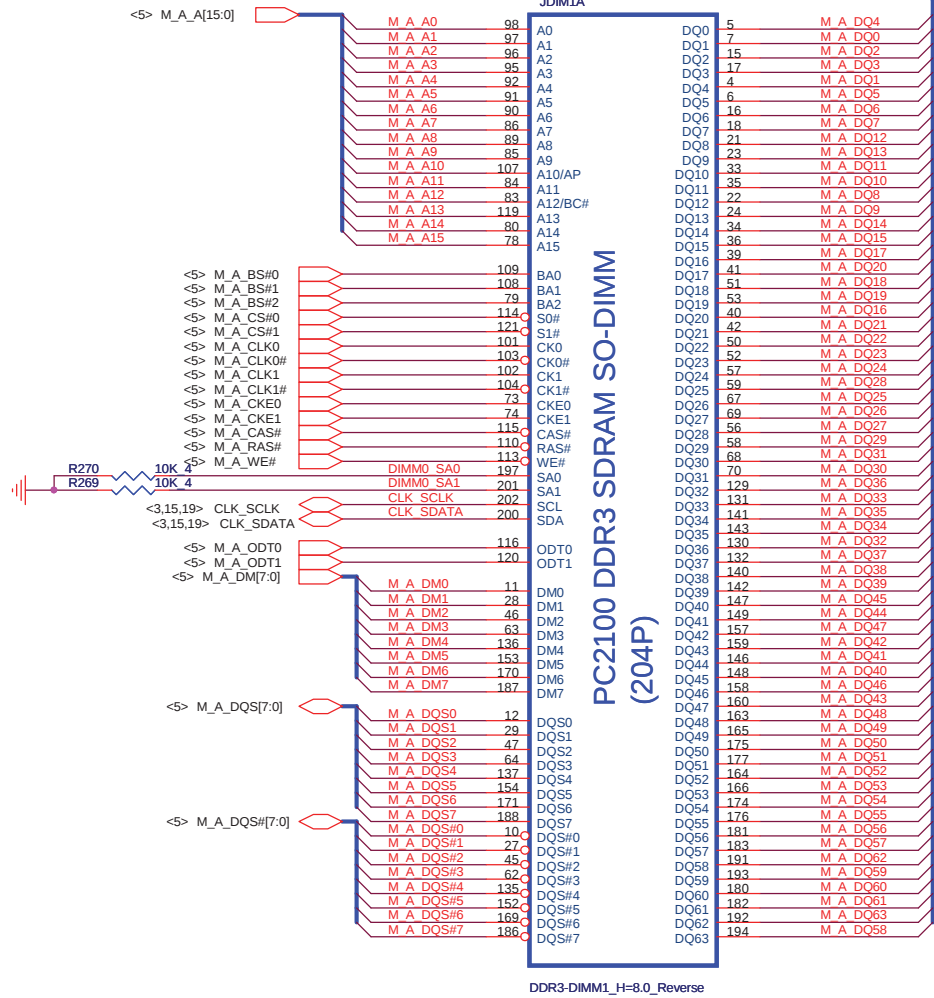
3.3 V. This rail should be powered up during S0 system state. Note that Thermal Sensor shares the same power supply rail with DAC. The external filters on this pin are not needed in case internal graphic is disabled so only 3.3-V connection is required.

[illegible]

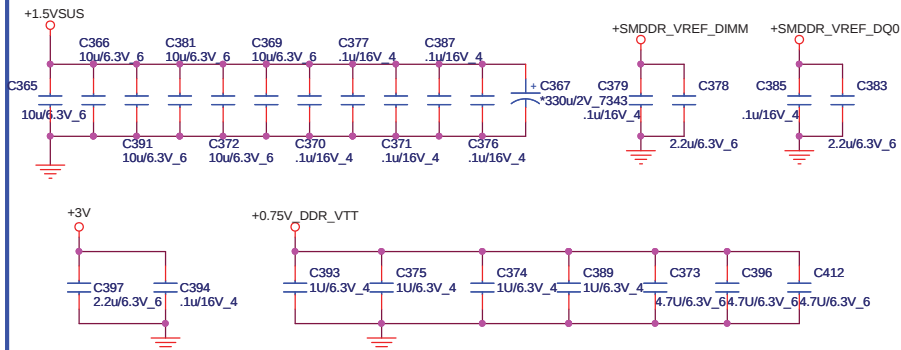
IBEX PEAK-M (GND)

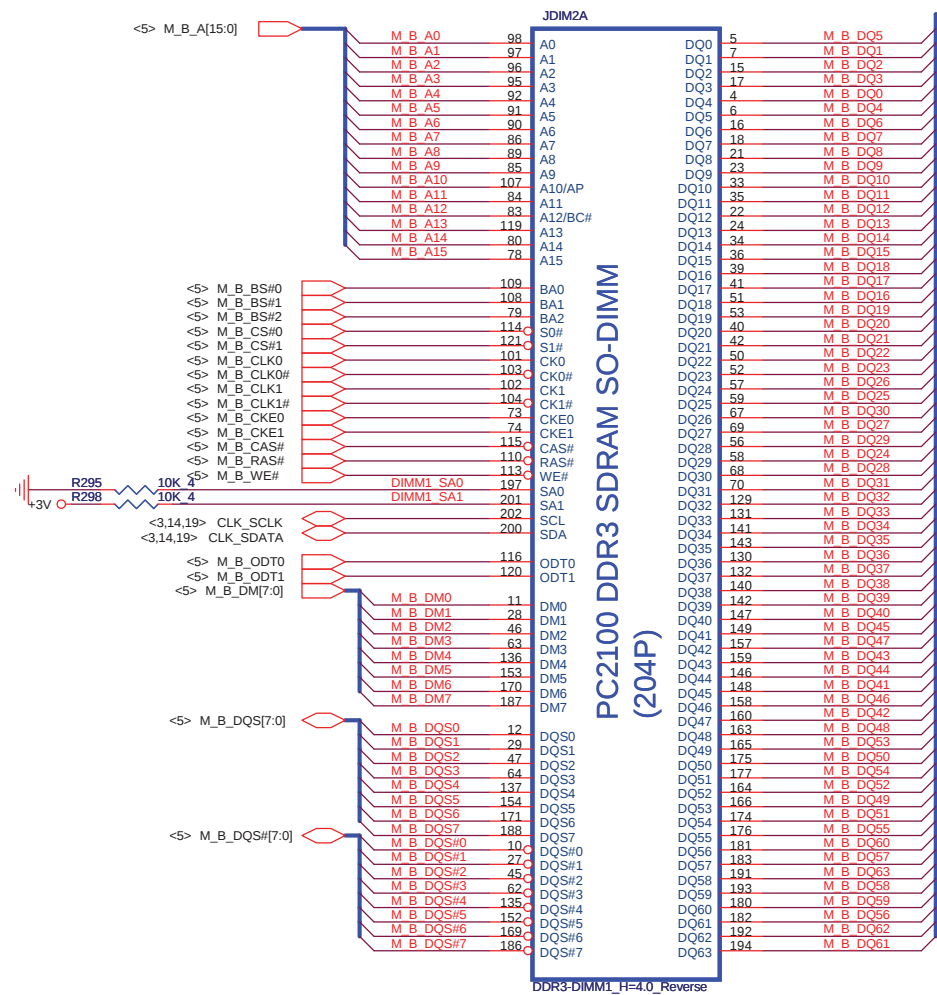


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Place these Caps near So-Dimm0.

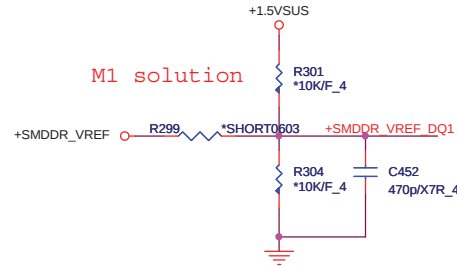




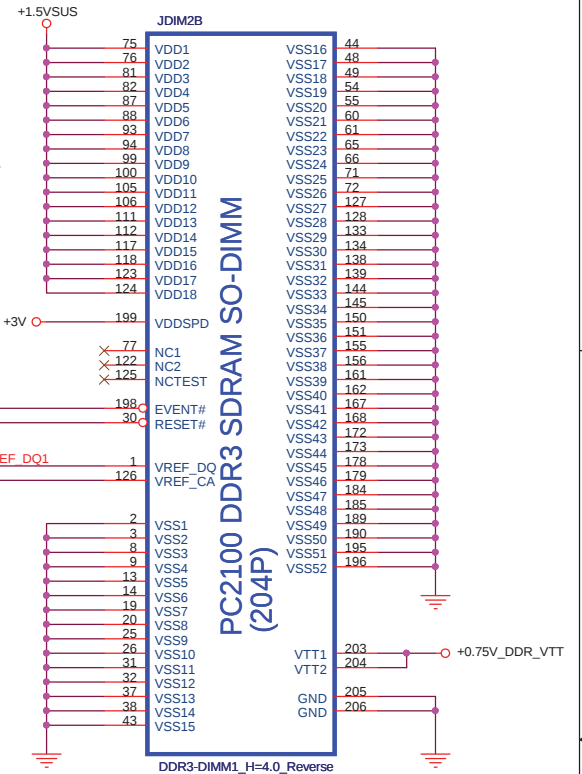
M3 solution



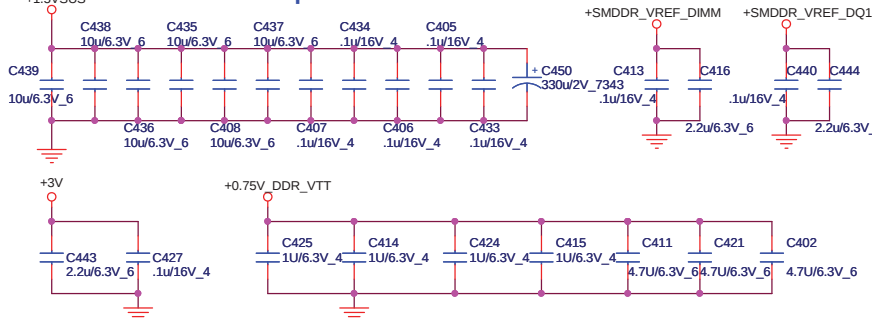
M1 solution



2.48A



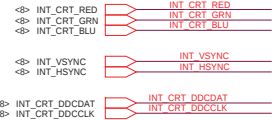
Place these Caps near So-Dimm1.



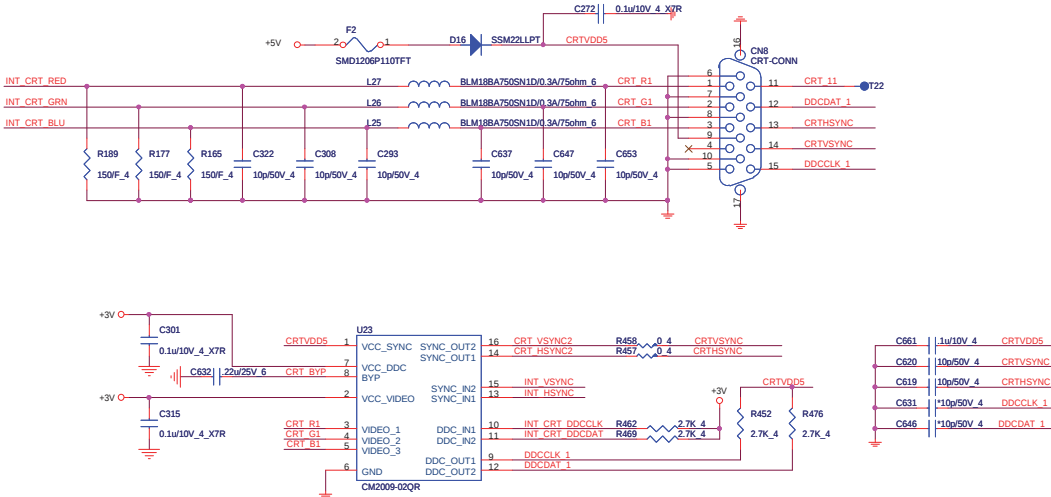
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CRT Switch

0_ohm Resistor place close to Joint-Point

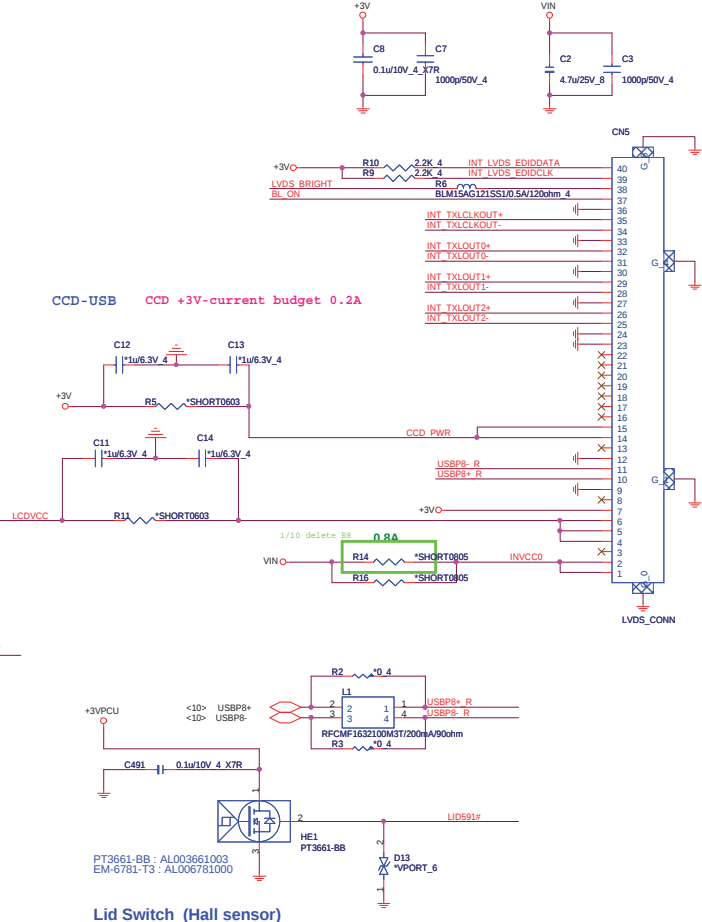
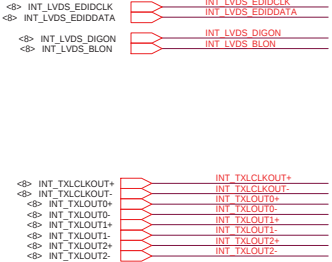


CRT

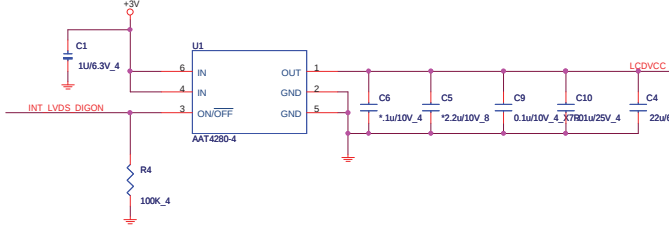


LVDS

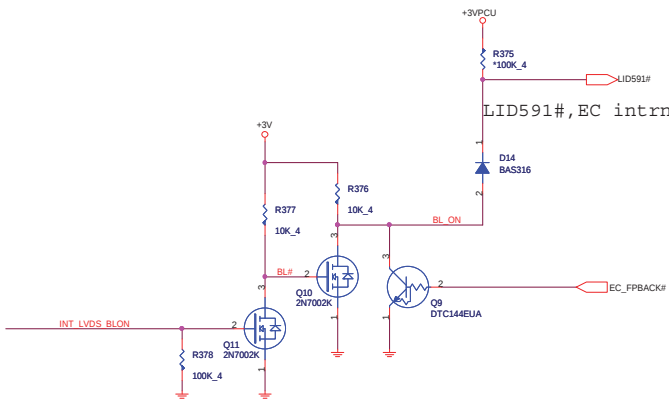
0_ohm Resistor place close to Joint-Point



LCD Power

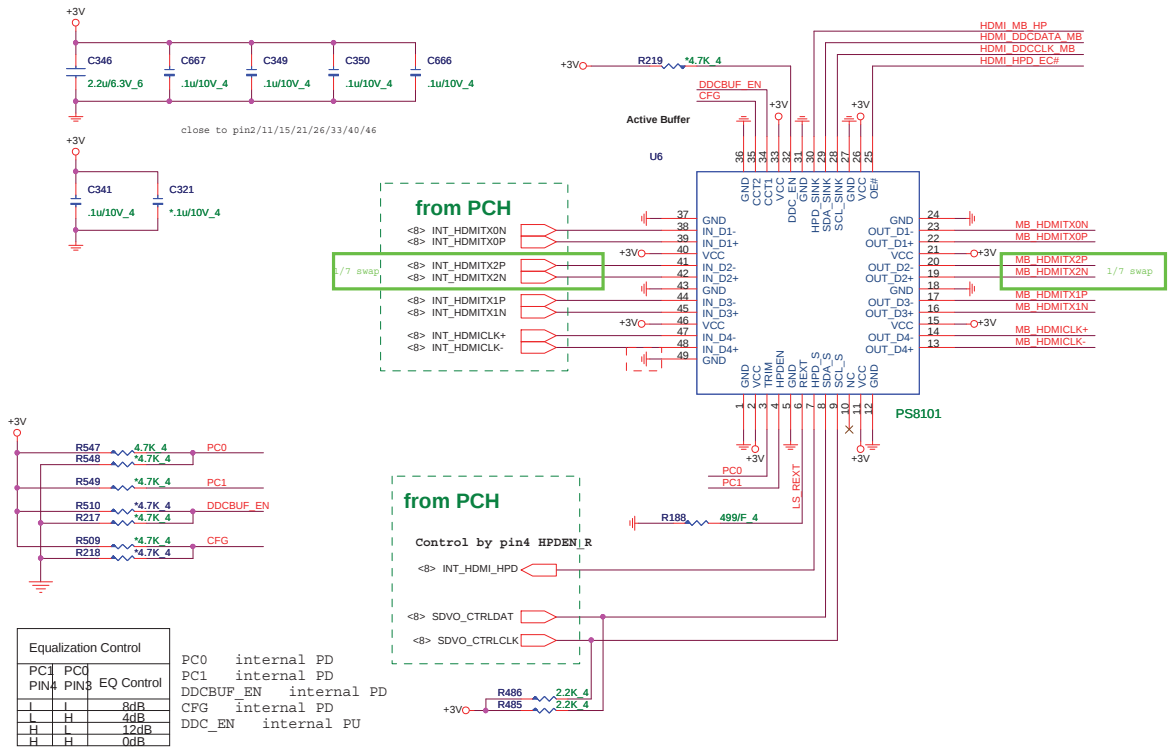


Backlight Control

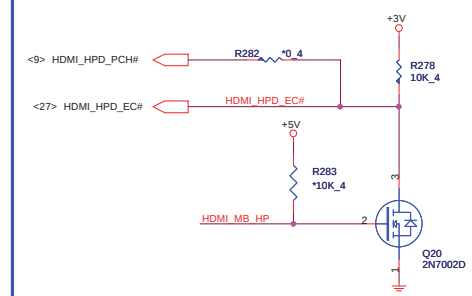


Lid Switch (Hall sensor)

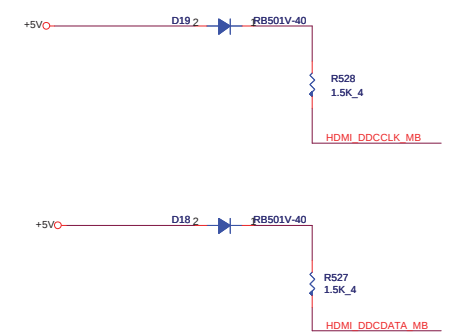
HDMI LEVEL SHIFTER



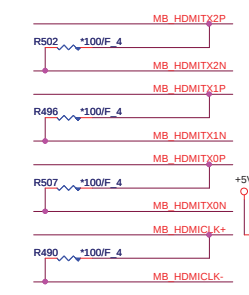
HDMI-detect



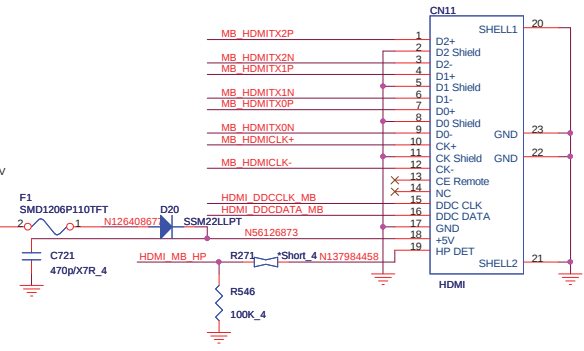
I2C



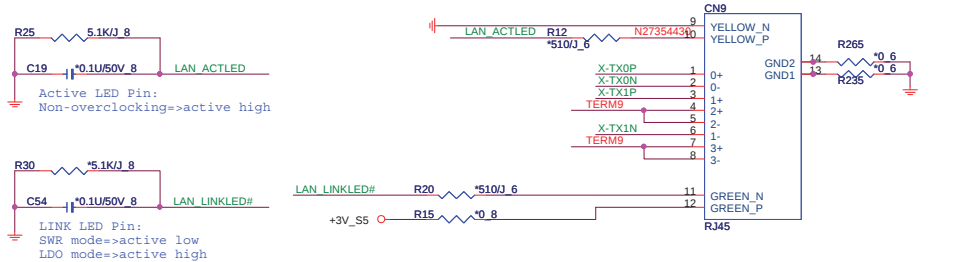
EMI



HDMI connector



```
<BOM note>
If center tap power come from internal switch
regulator
=>Stuff 52SWR@ (Default)
If center tap power come from internal LDO
=>Stuff 52LDO@
```



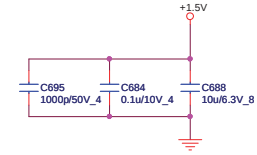
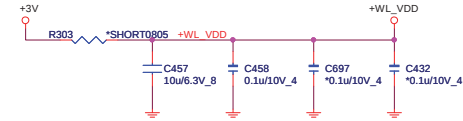
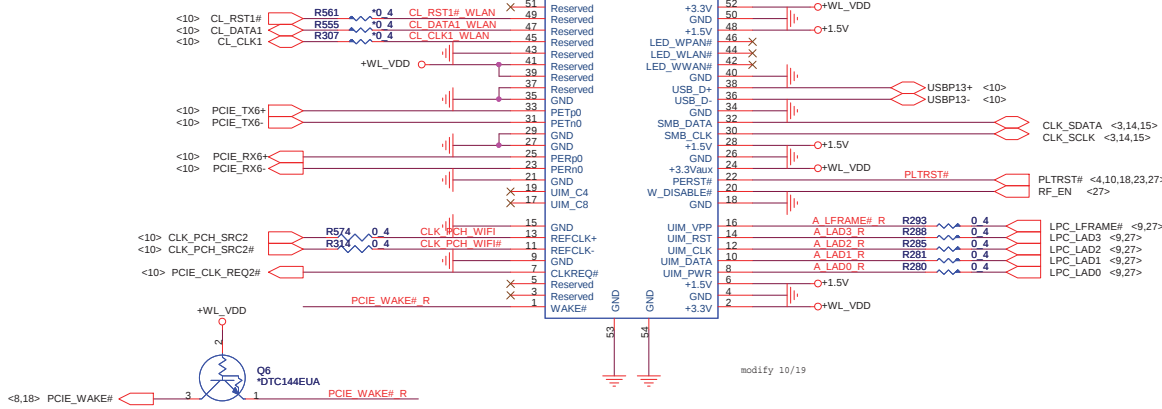
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Debug

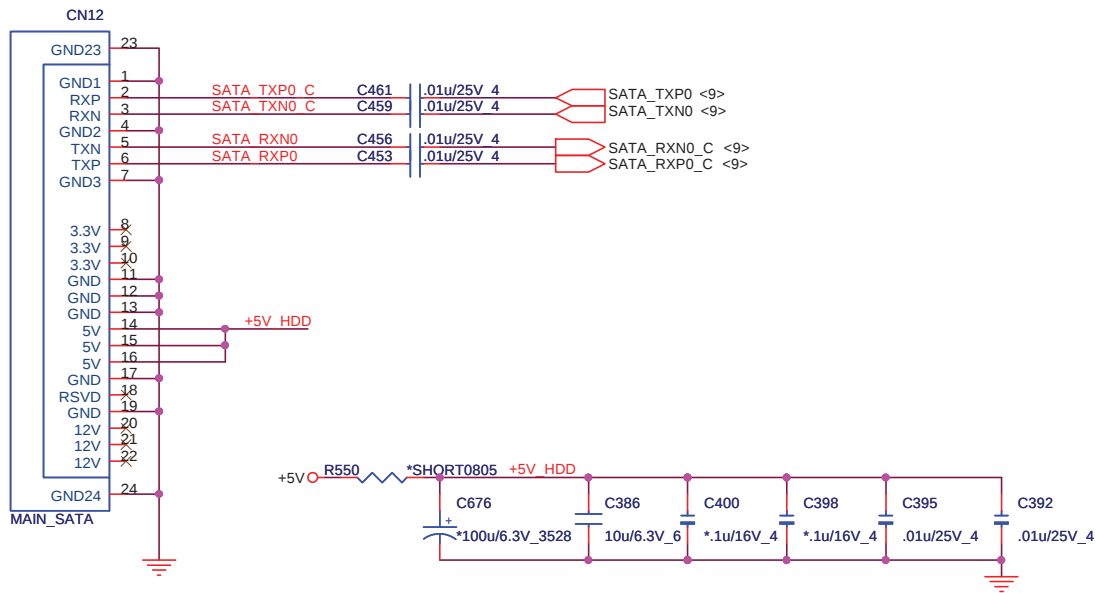
Check LED signal. (active high or low)

H=7.0mm
LTS AAA-PCI-046-K01

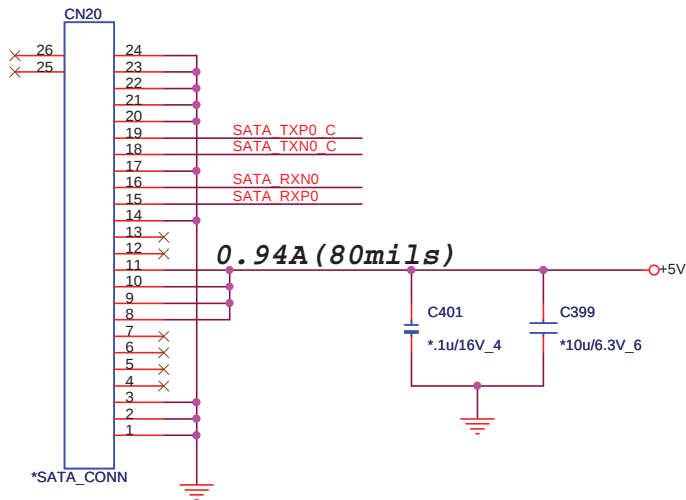


Debug

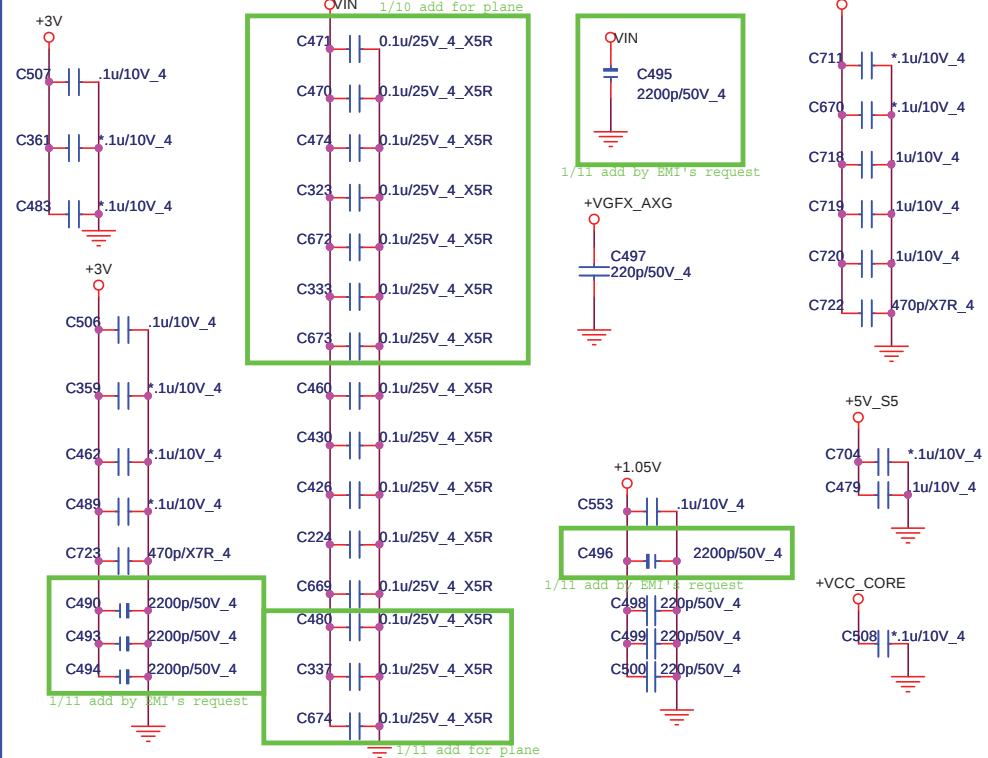
MAIN SATA HDD



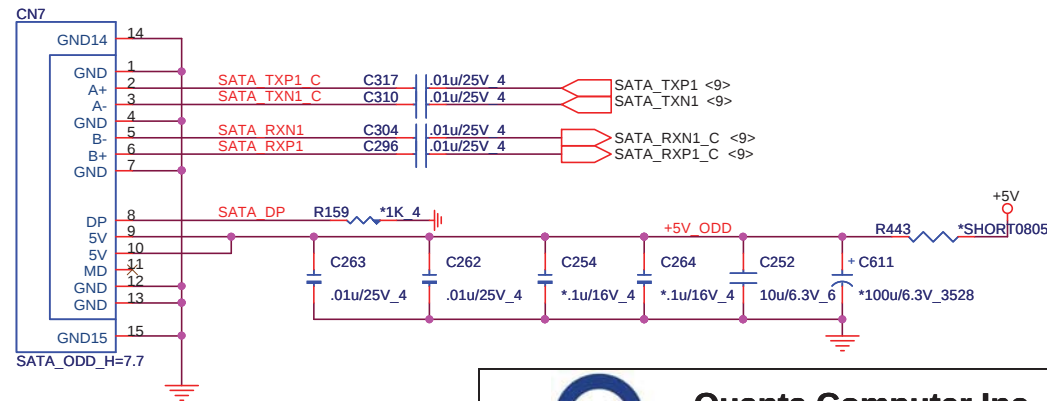
2.5" SATA HDD



EE RETURN-PATH CAPACITORS



ODD (SATA)



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PROJECT : ZQH

Size	Document Number	Rev
	SATA-HDD/ODD/USB-ESATA	1A
Date:	Monday, March 14, 2011	Sheet 20 of 35

Codec(ADO)

HP



ANALOG

(Vista Premium Version)

Split by DGND

0V : Power down Class D SPK amplifier
3.3V : Power up Class D SPK amplifier

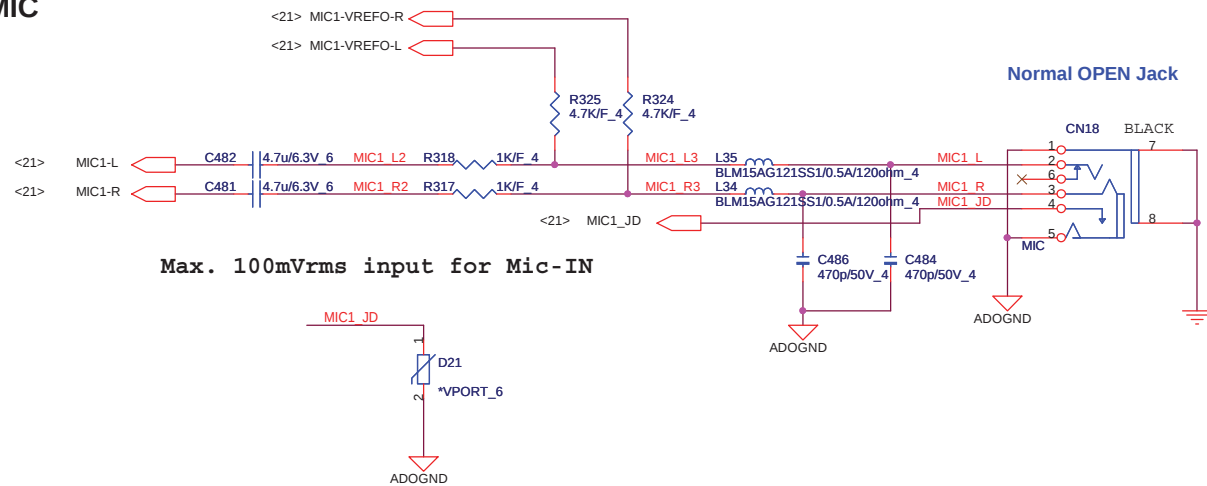
Power (ADO)

Mute(ADO)

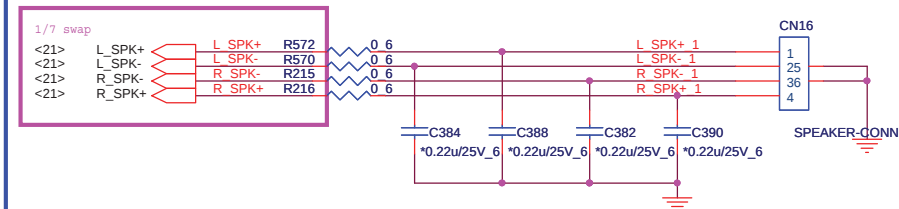
MIC

INT MIC array

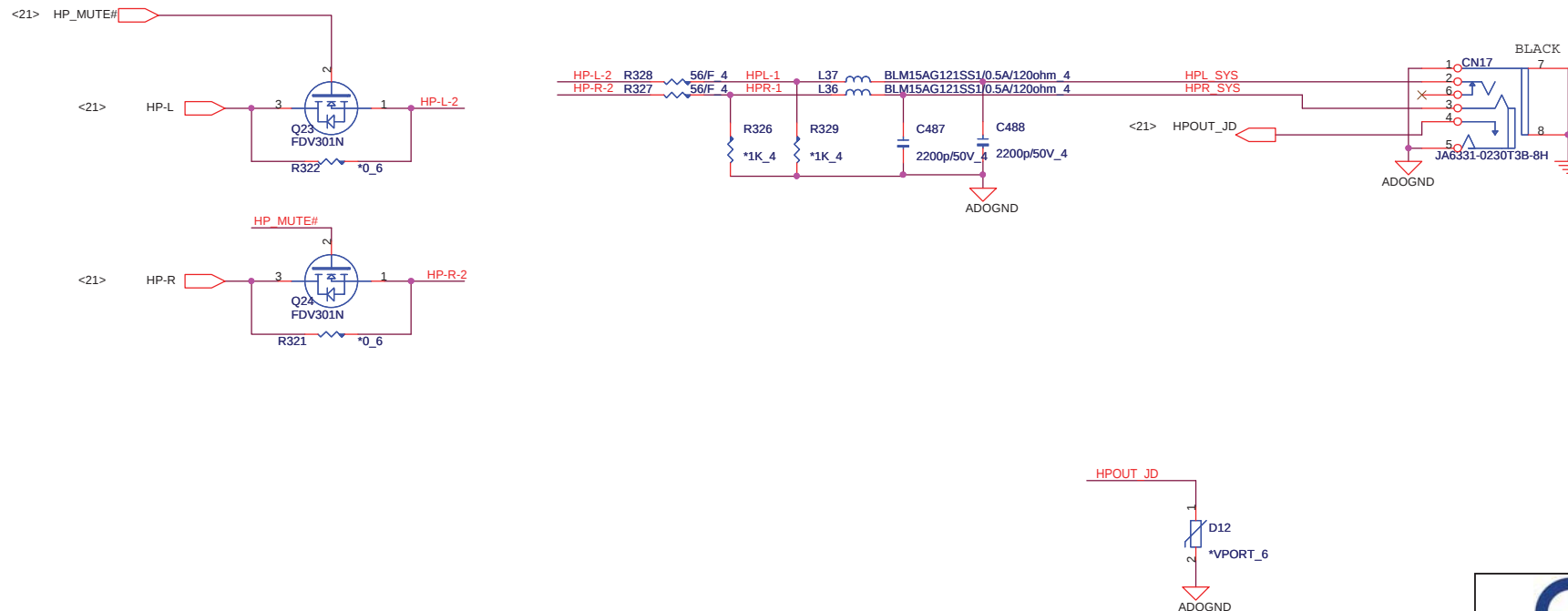
MIC



Internal Speaker



HP/SPDIF



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PROJECT : ZQH

Size	Document Number	Rev
		1A

AMP /AUDIO JACK CONN

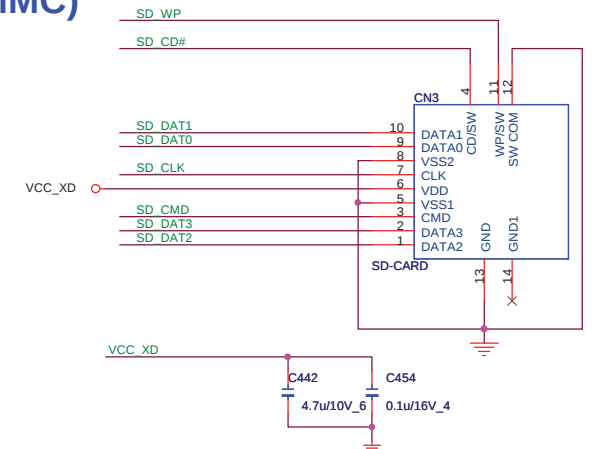
Date: Monday, March 14, 2011 Sheet 22 of 35

CARD READER Controller

AU6435-GDL

2 IN 1 CARD READER (SD/MMC)

Main	DFHS11FR011
Second	DFHS11FR033



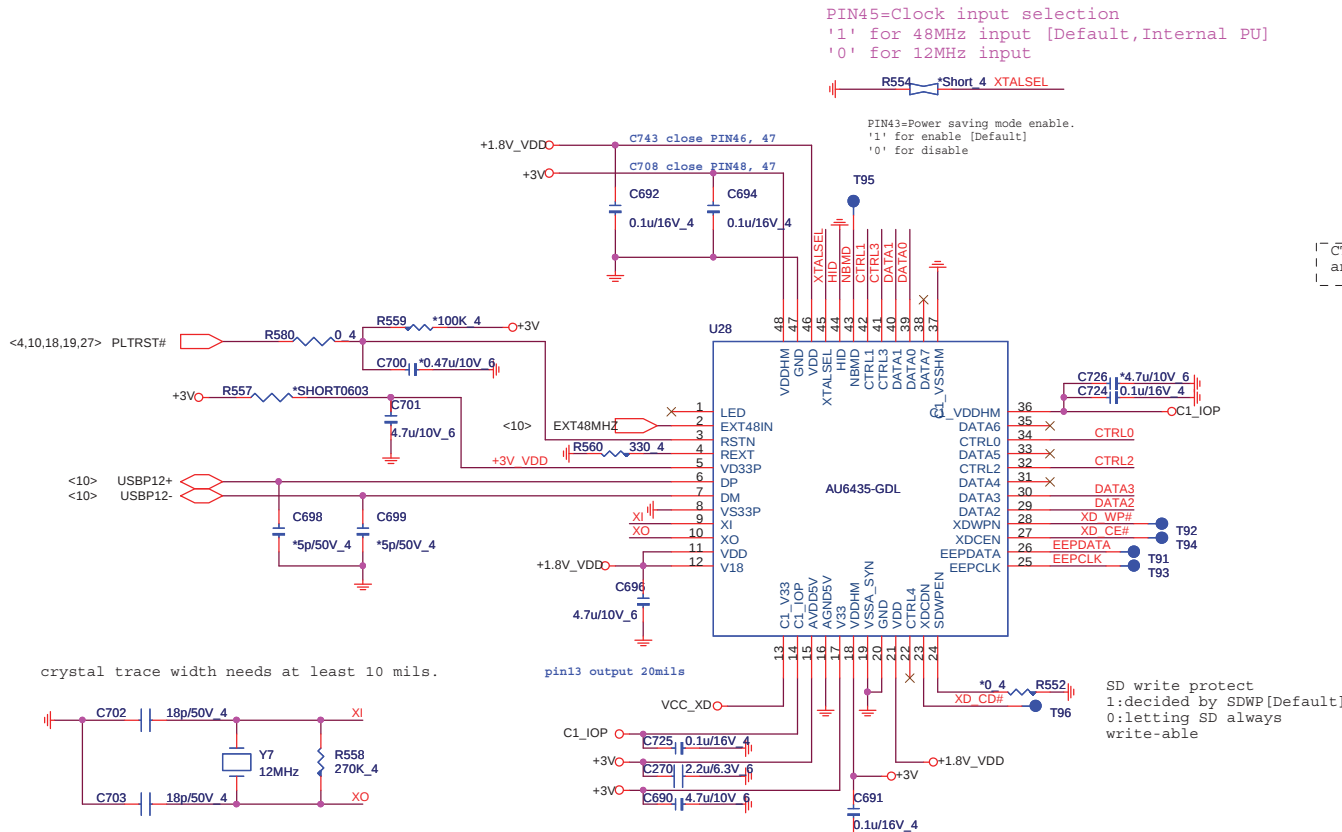
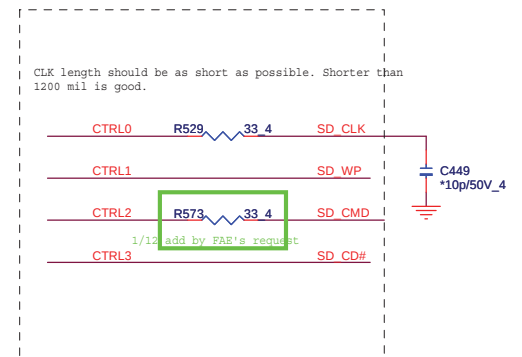
Close to CN14 pin 14 & pin23
4.7u CAP close to pin23

CTRL0, CTRL1 trace length shorter,
and surround with GND.

The trace length difference for each card interfaces should be
smaller than 500 mil



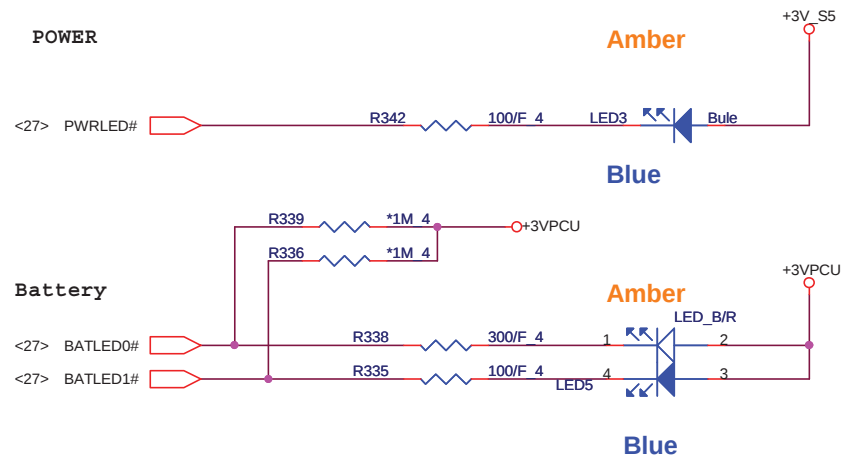
Close to connector



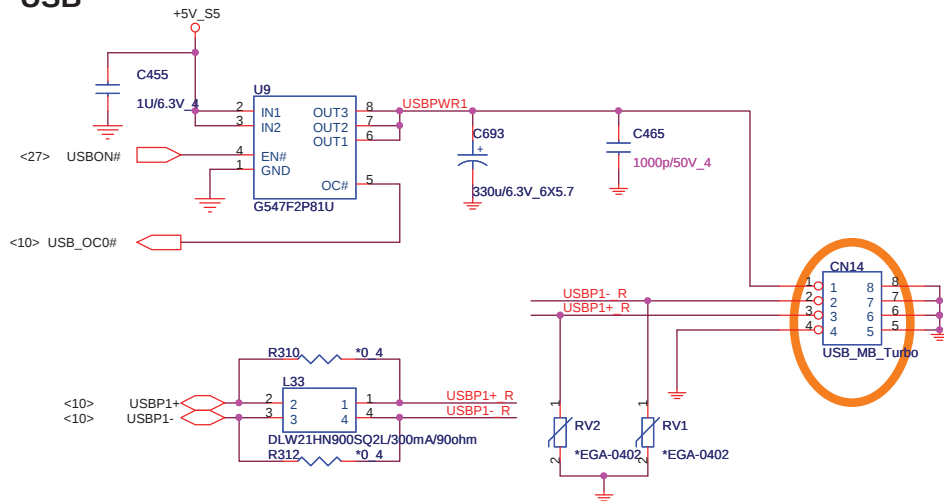
PROJECT : ZQ5
Quanta Computer Inc.

Size	Document Number AU6433 CardReader	Rev 1A
Date:	Monday, March 14, 2011	Sheet 23 of 43

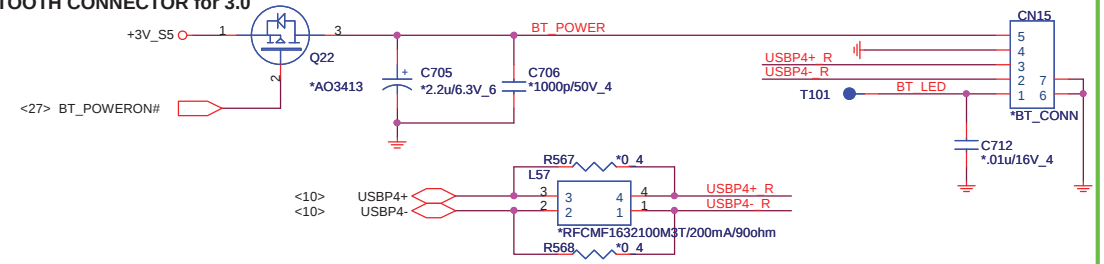
LED



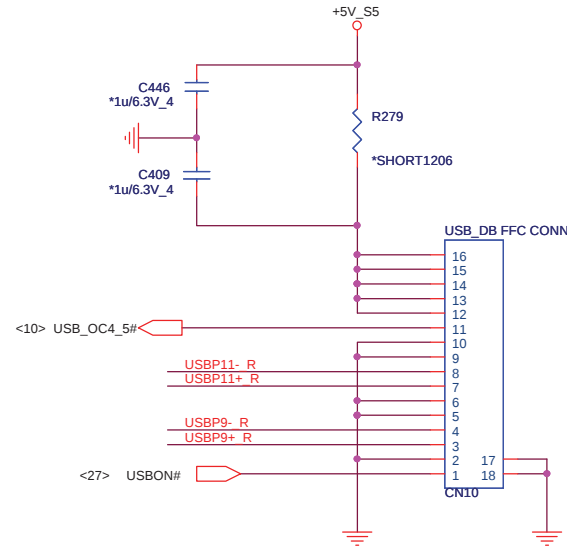
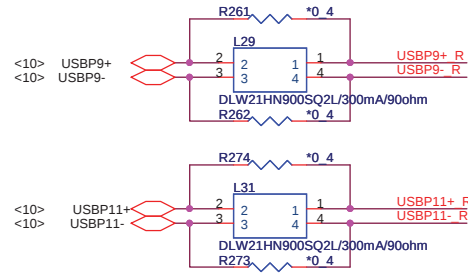
USB



BLUETOOTH CONNECTOR for 3.0



USB/B



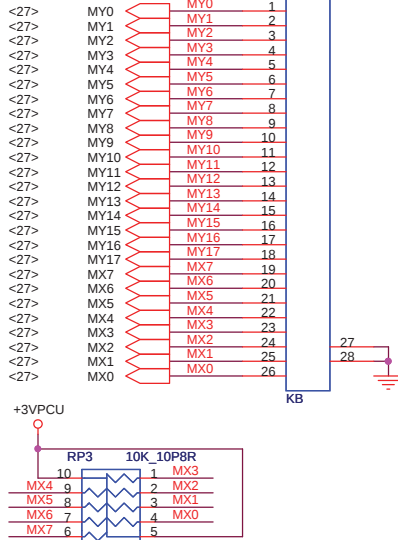
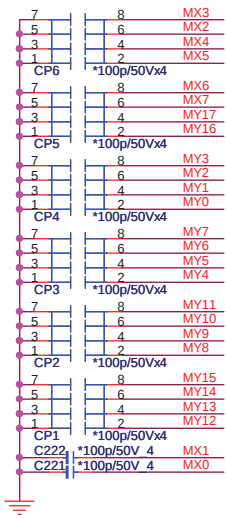
Quanta Computer Inc.

PROJECT : ZQH

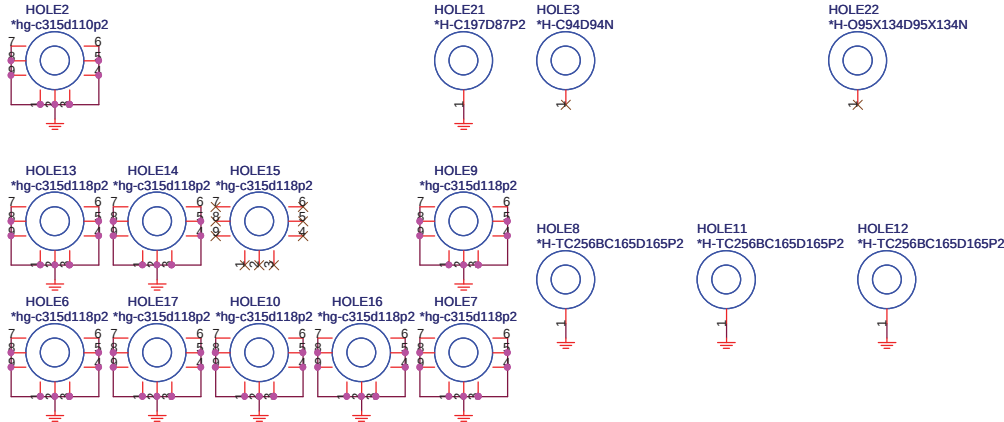
Size	Document Number	Rev
	USB/ BT	1A

Date: Monday, March 14, 2011 Sheet 25 of 35

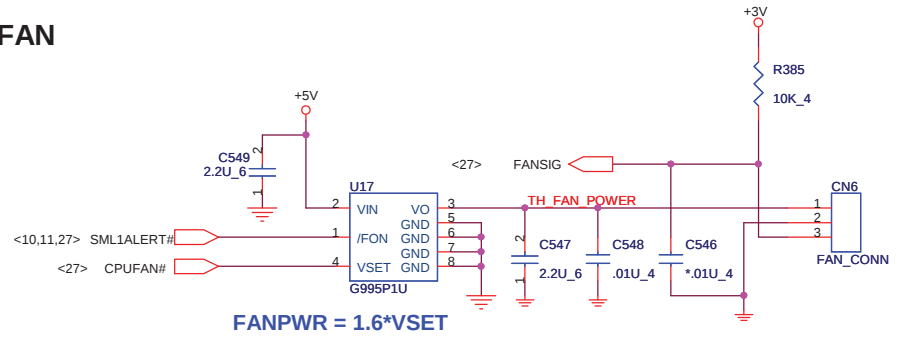
K/B



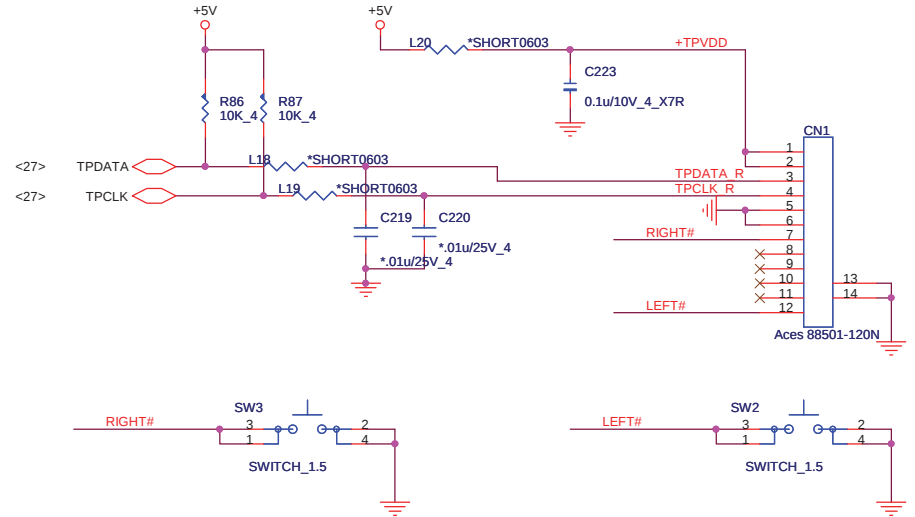
HOLE



CPU FAN



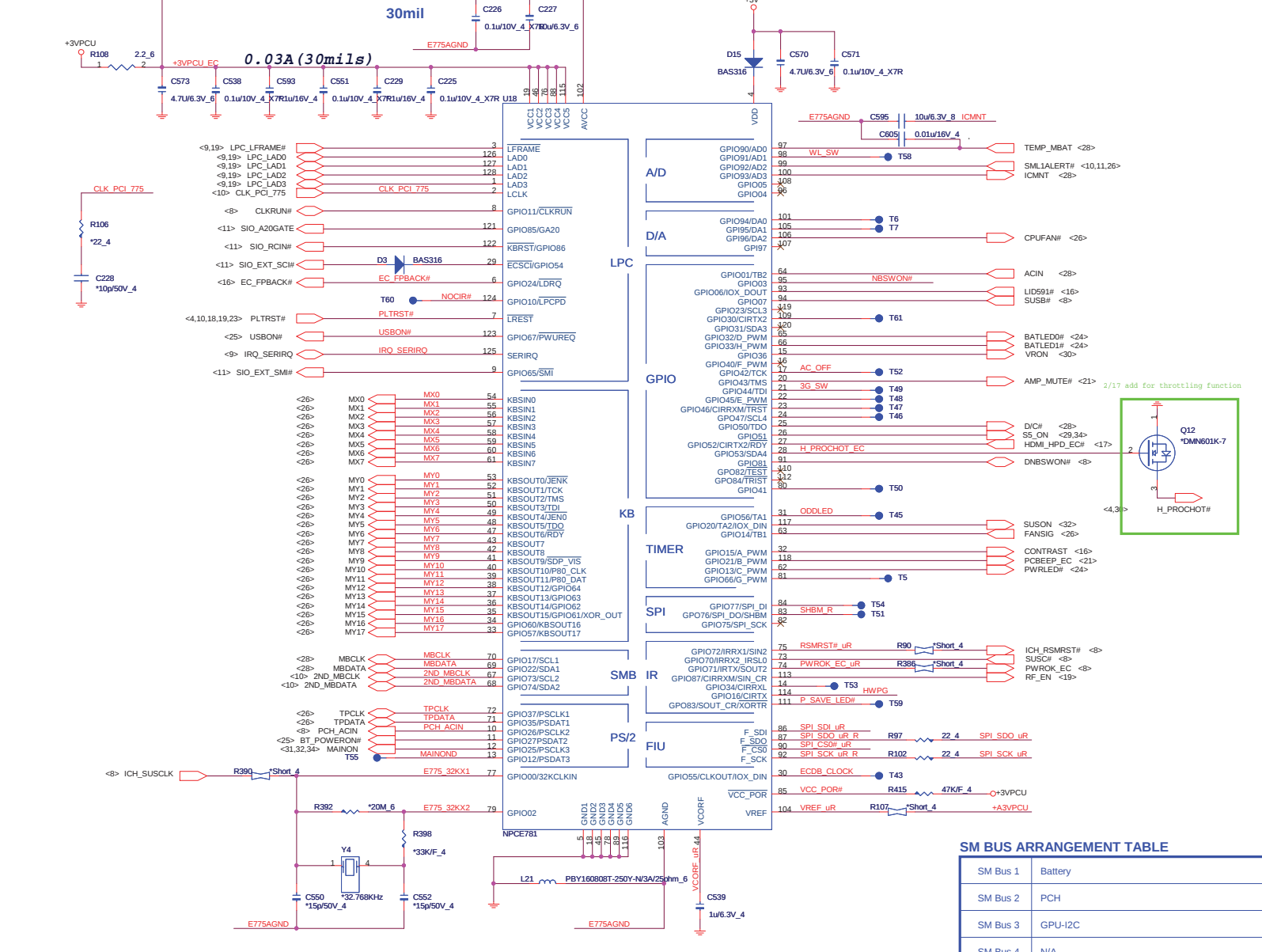
TOUCHPAD & Switch CONN.



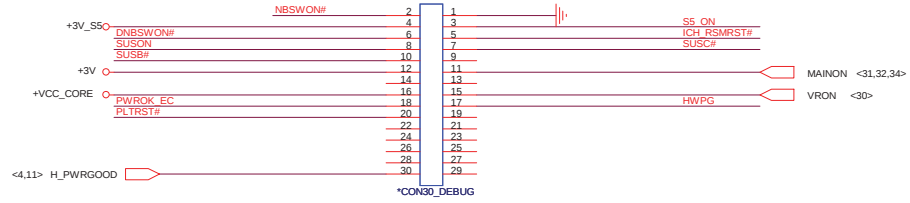
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PROJECT : ZQH

Size	Document Number	Rev
	KB/FAN/TP+FP	1A
Date:	Monday, March 14, 2011	Sheet 26 of 35

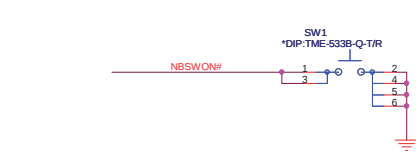
EC(KBC)



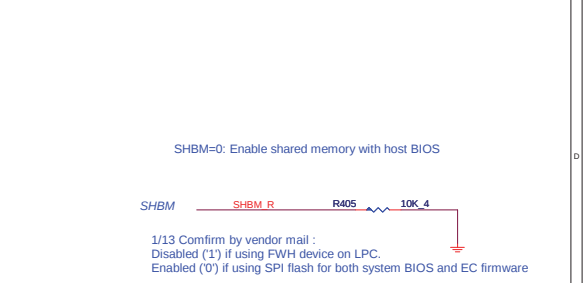
Power sequence



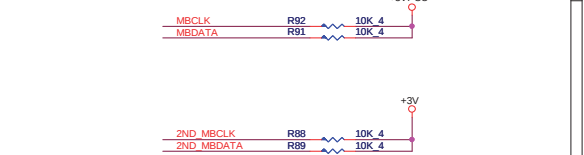
POWER-ON Switch(KBC)



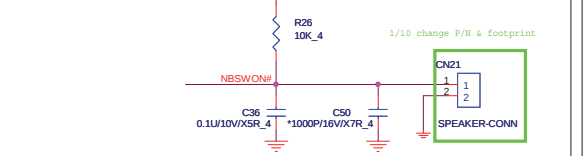
I/O ADDRESS SETTING(KBC)



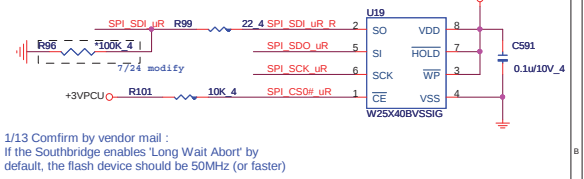
SM BUS PU(KBC)



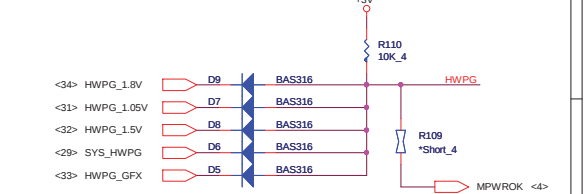
PWR/B



SPI FLASH(KBC)



HWPG(KBC)



SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU-I2C
SM Bus 4	N/A

INTERNAL KEYBOARD STRIP SET(KBC)



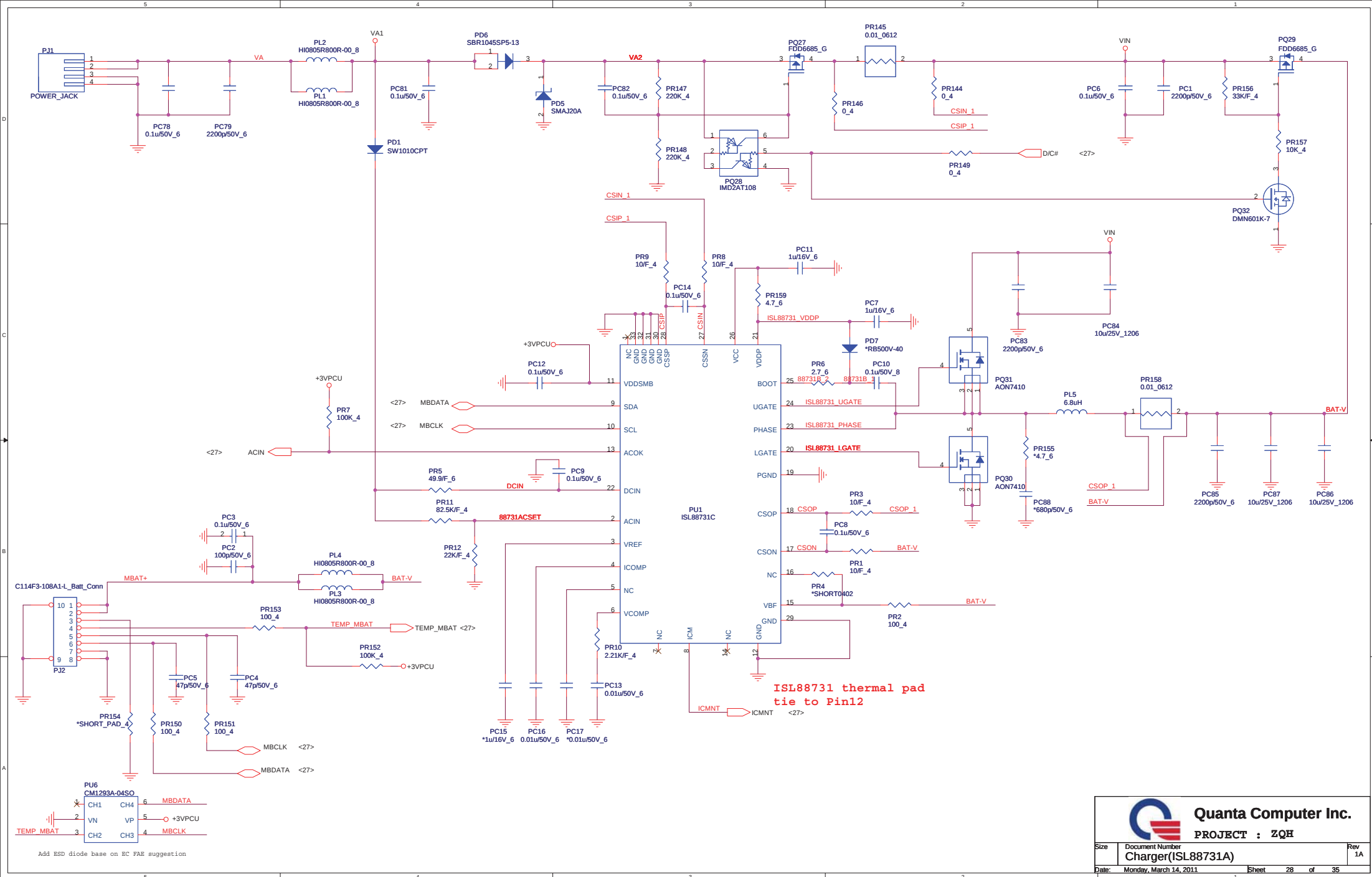
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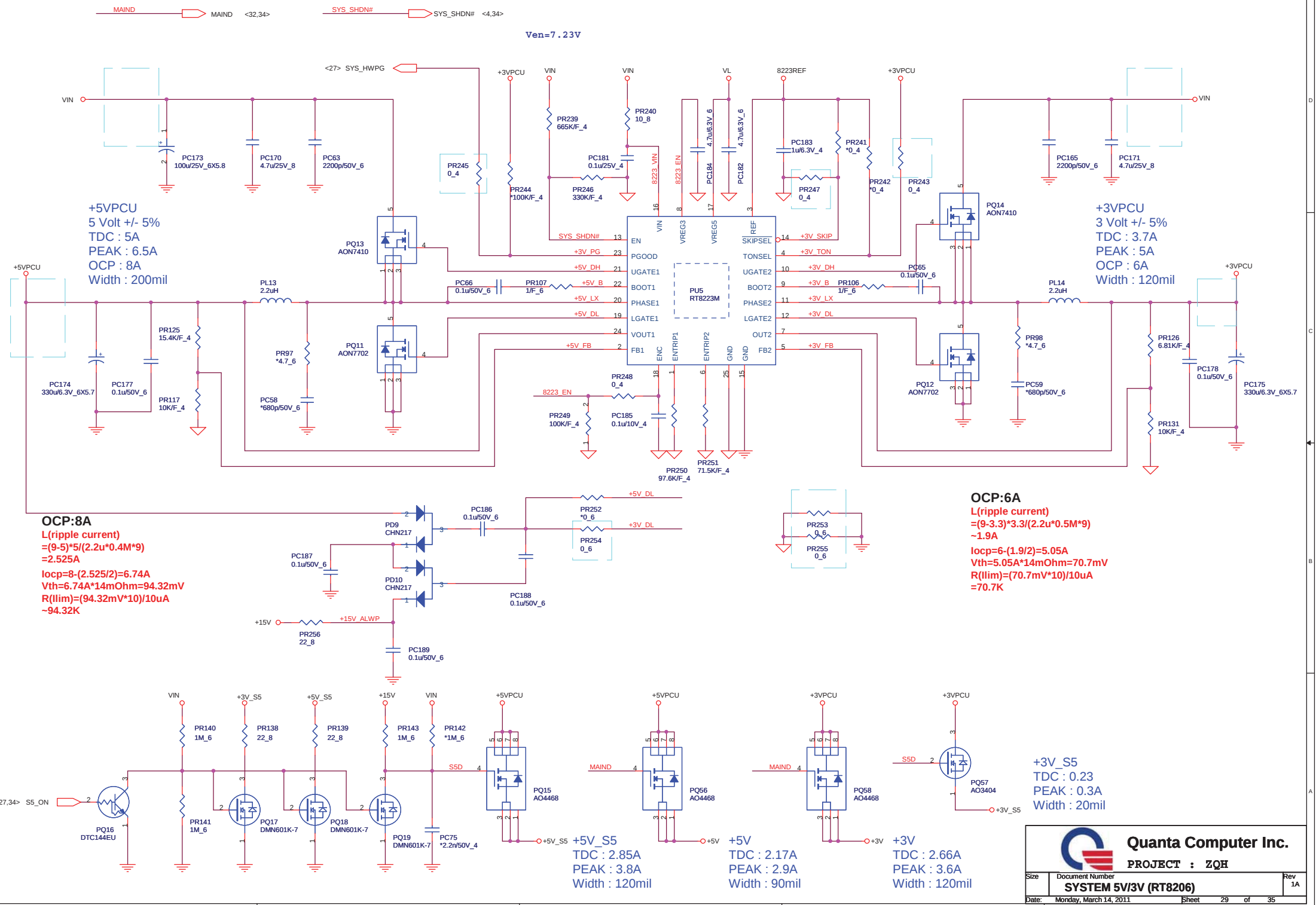
PROJECT : ZQH

WPCE781 & FLASH

Size	Document Number	Rev
		1A

Date: Monday, March 14, 2011 Sheet 27 of 35





OCP:8A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=8-(2.525/2)=6.74A
Vth=6.74A*14mOhm=94.32mV
R(Ilim)=(94.32mV*10)/10uA
~94.32K

OCP:6A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
~1.9A
Iocp=6-(1.9/2)=5.05A
Vth=5.05A*14mOhm=70.7mV
R(Ilim)=(70.7mV*10)/10uA
~70.7K

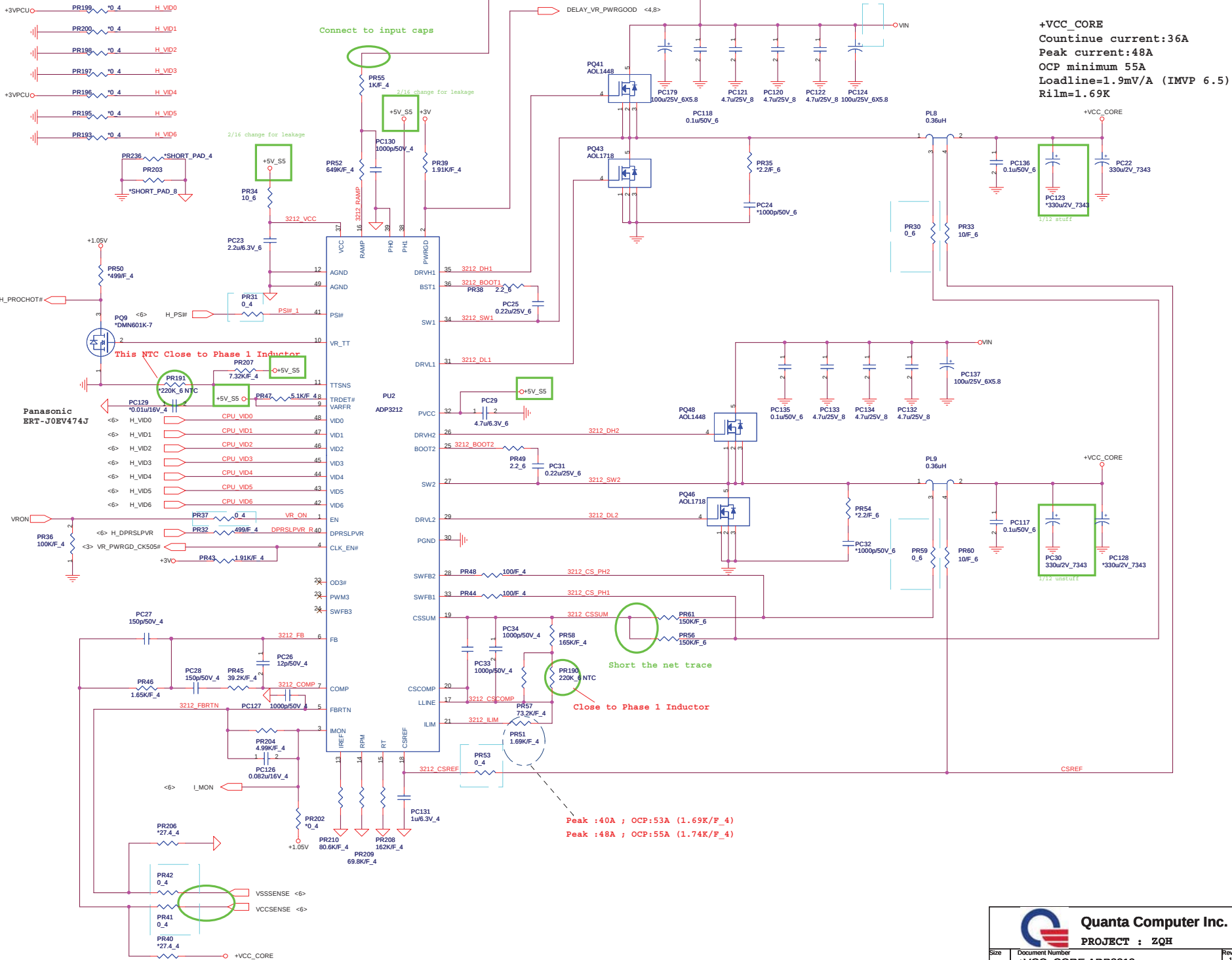
+3V_S5
TDC : 0.23
PEAK : 0.3A
Width : 20mil

+5V_S5
TDC : 2.85A
PEAK : 3.8A
Width : 120mil

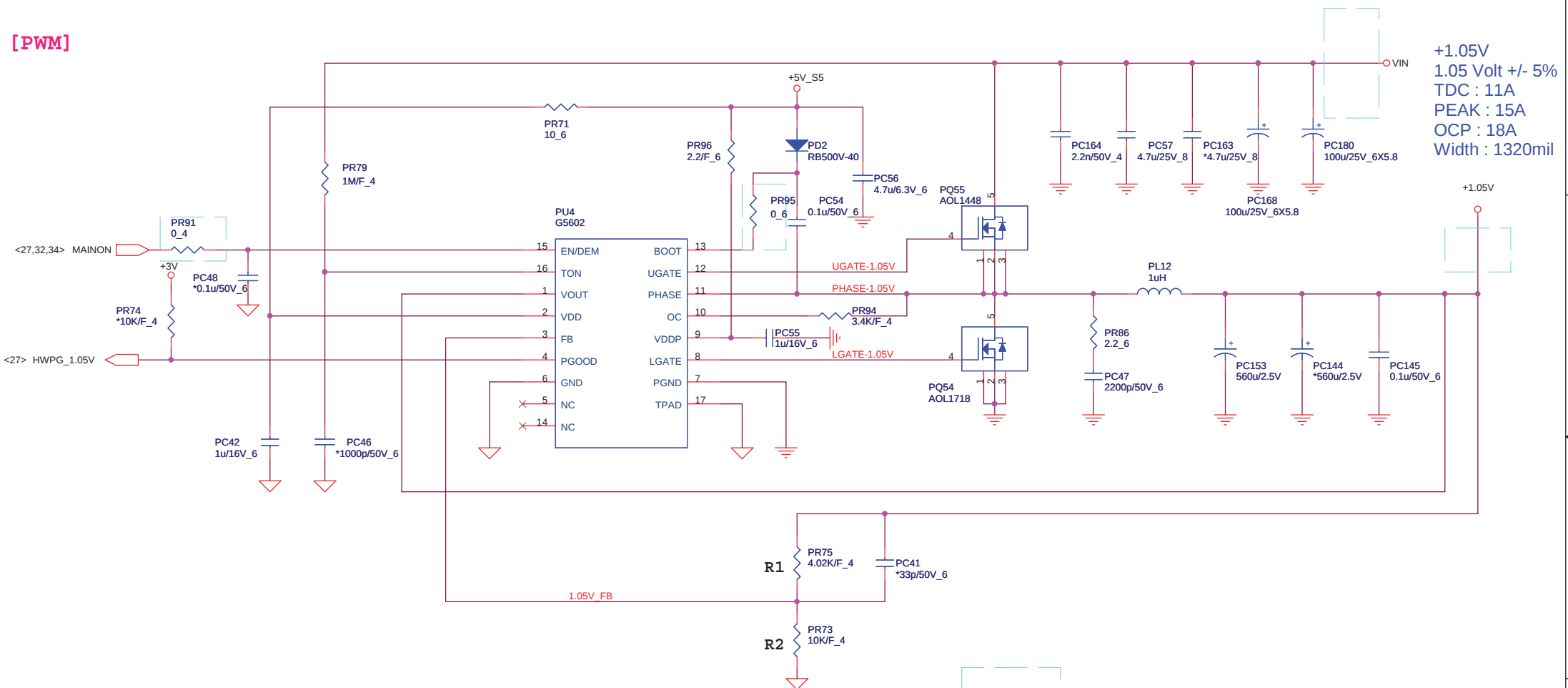
+5V
TDC : 2.17A
PEAK : 2.9A
Width : 90mil

+3V
TDC : 2.66A
PEAK : 3.6A
Width : 120mil

VID 1.2875V



[PWM]



+1.05V
1.05 Volt +/- 5%
TDC : 11A
PEAK : 15A
OCP : 18A
Width : 1320mil

$$TON = 3.85p \cdot RTON \cdot Vout / (Vin - 0.5)$$

$$Frequency = Vout / (Vin \cdot TON)$$

$$TON = 3.85p \cdot 1M \cdot 1 / (Vin - 0.5)$$

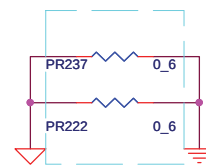
$$Frequency = 1 / (0.0036767) = 272K$$

A01718 $R_{dson} = 3 \sim 4.3m\Omega$

$$I(\text{ripple current}) = (19 - 1.05) \cdot 1.05 / (1u \cdot 272k \cdot 19) \sim 3.647A$$

$$RILIM = 4.3m\Omega \cdot 18 - 1.823 / 20uA = 3.477K\Omega$$

$$I(\text{choke})_{peak} = 21.647A$$



Quanta Computer Inc.
PROJECT : ZQH

Size	Document Number	Rev
	+VTT (G5602R41U)	1A
Date:	Monday, March 14, 2011	Sheet 31 of 35

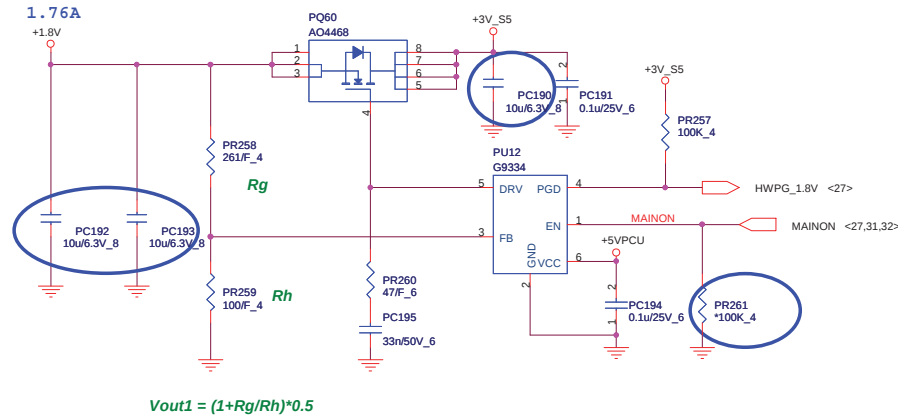
```
AO1718 Rdson=3.8~4.3mOhm
L(ripple current)
=(19-1.5)*1.5/(1u*400k*19)
~3.454A
Vtrip= (18-3.454/2)*4.3mohm=0.0699V
RILIM=Vtrip/10u=6.997K
```

	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

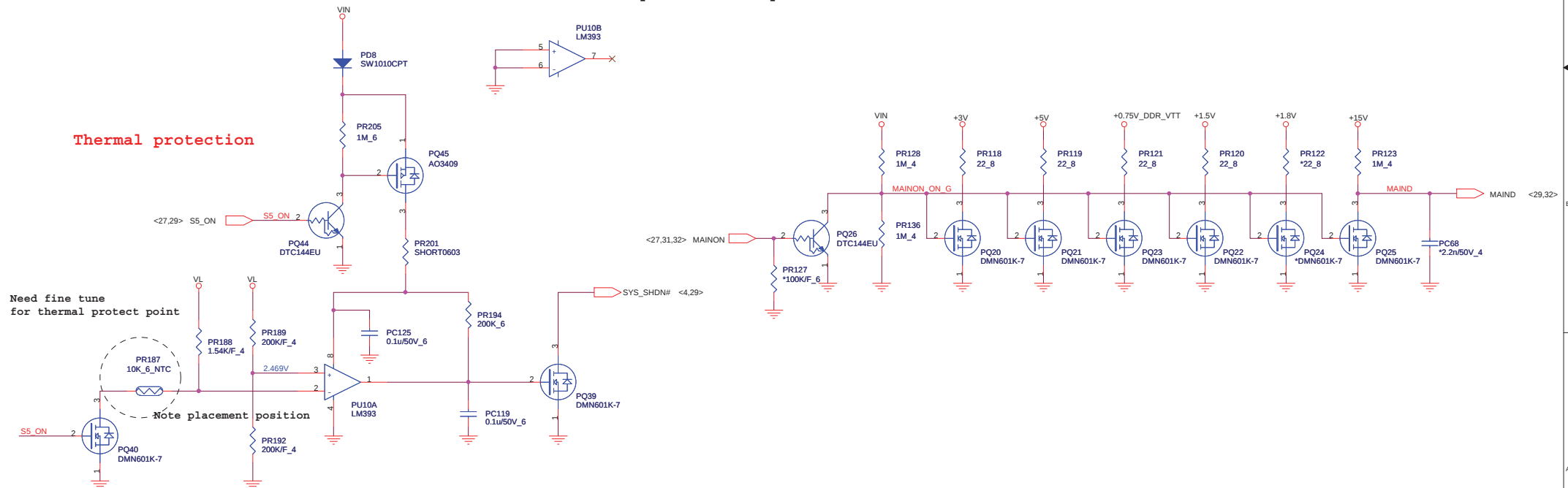


+VGFX_AXI

+1.8V
1.8 Volt +/- 5%
TDC : 0.76A
PEAK : 1.01A
Width : 40mil



For EC control thermal protection (output 3.3V)



[illegible]