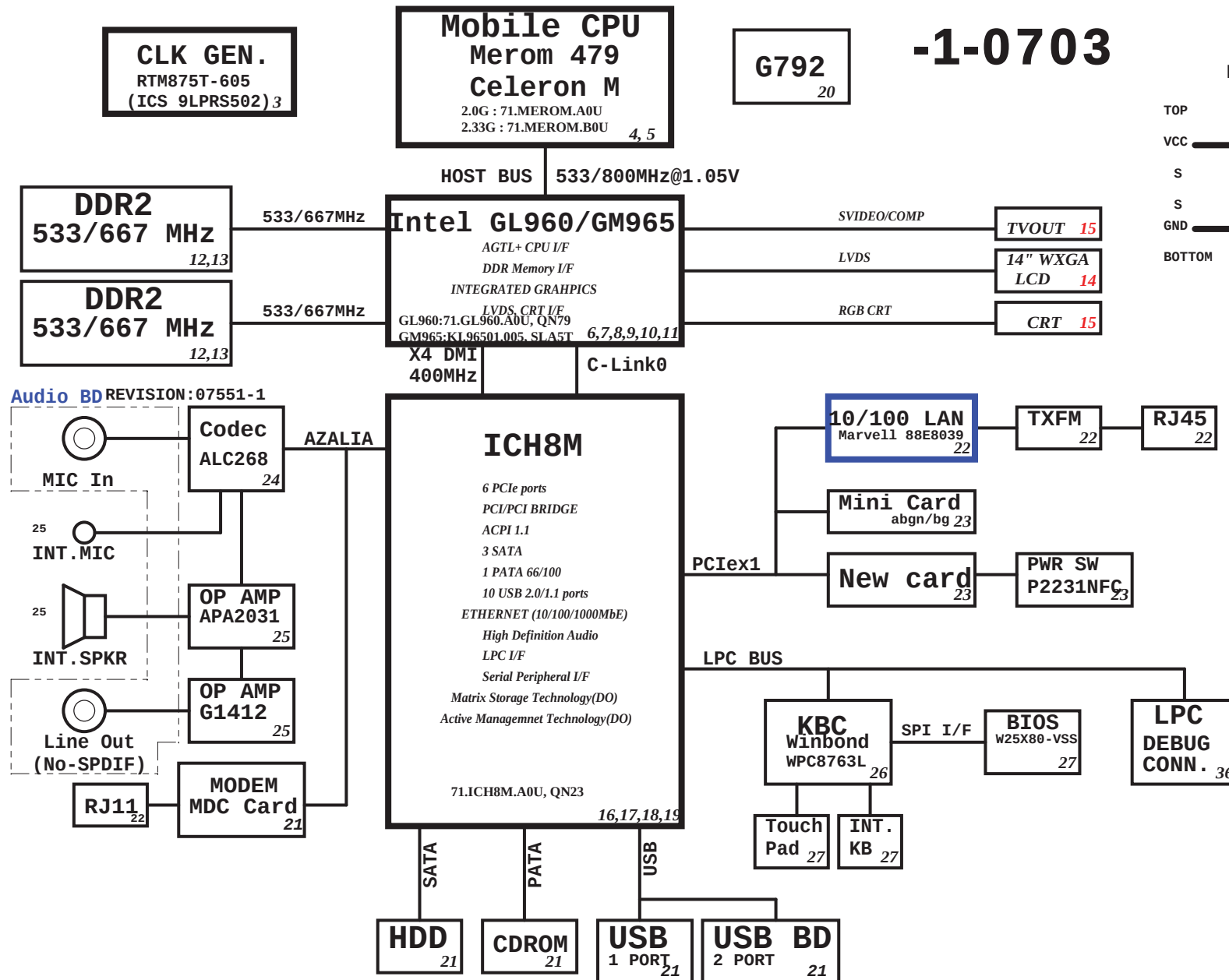


Volvi2 Block Diagram

Project code: 91.4X101.001
PCB P/N : 48.4X101.011
REVISION : 07220-1

-1-0703



PCB STACKUP
TOP
VCC
S
S
GND
BOTTOM

SYSTEM DC/DC MAX8744 31	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 (6A) 3D3V_S5 (6A)
SYSTEM DC/DC TPS51124 32	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 (8A) 1D8V_S3 (12A)
TPS51100 (G2997) 33	
1D8V_S3	DDR_VREF_S0 (1.5A) DDR_VREF_S3
APL5913 33	
1D8V_S3	1D25V_S0 (1.5A)
G909 28	
5V_AUX_S5	3D3V_AUX_S5 (100mA)
APL5915 33	
1D8V_S3	1D5V_S0 (1.5A)
CHARGER MAX8731 34	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA
CPU DC/DC MAX8770 30	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

RTM

ICH8M Functional Strap Definitions

ICH8-M EDS 21762 2.0V1 page 16

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIe Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIe config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIe config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPI020	Reserved	This signal should not be pulled high.
GNT1#/ GPI051	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSusi_05, VccSusi_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSusi_05, VccSusi_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPI033/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOw#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

PCIe Routing

LANE1	LAN Marvell
LANE2	MiniCard WLAN
LANE3	NewCard WLAN

ICH8M Integrated Pull-up and Pull-down Resistors

ICH8-M EDS 21762 2.0V1

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPI0[20]	PULL-DOWN 20K ?
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPI023	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K ?
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP 13K

History

2007/05/02
1 Based on Tahoe to modify schematics.
=====

2007/05/14
1. Page 34: Replace "D25" with "BAS16-1-GP".
2. Page 27: Replace "R485" with "2K7R2j".
3. Page 27: DY: C379"
4. Page 27: Add "C682" D1u capacitor on "LID1.PIN1"
5. Page 27: Replace "R238" with "0R2".
6. Page 25: Replace "INTMIC1" & "SPKR1" with main source follow connector list.
7. Page 5: Add C115, C116, C141, C149, C169, C171 for Colay with TC25.
8. Page 10: Replace "L20" with "68.00217.141".
9. Page 10: Replace "L10" & "L23" with "68.00217.101"
=====

Crestline Strapping Signals and Configuration

Crestline EDS 20954 1.0 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[8:6]	Reserved	
	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Crestline GMCH PWORK in signal.

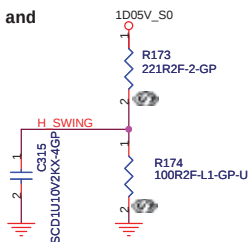
RTM

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size A3	Document Number	Rev	-1
Date: Thursday, July 05, 2007		Sheet 2	of 36

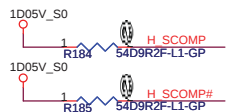


H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



H_SCOMP and H_SCOMP# Resistors and
Capacitors close MCH 500 mil (MAX)

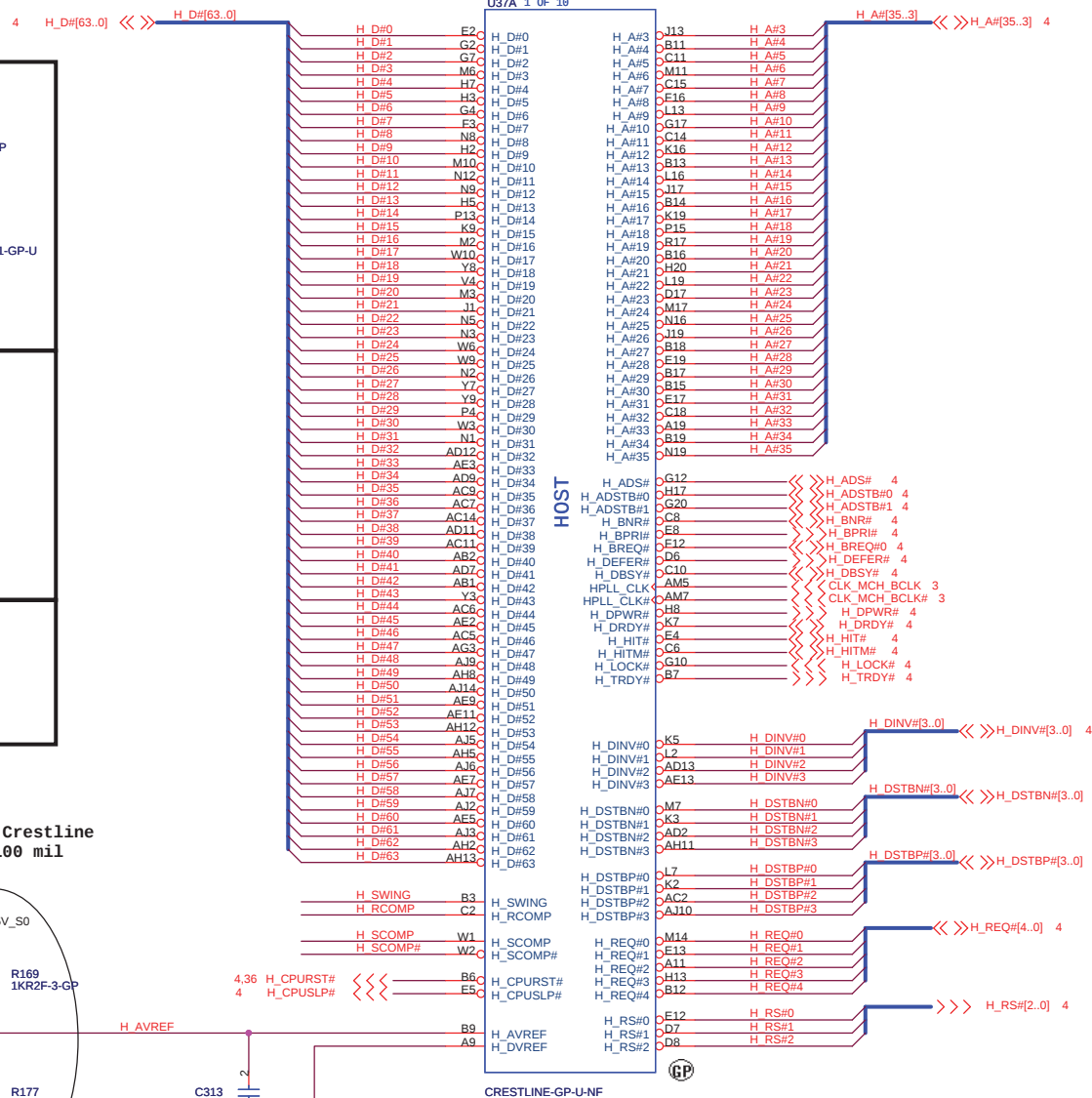
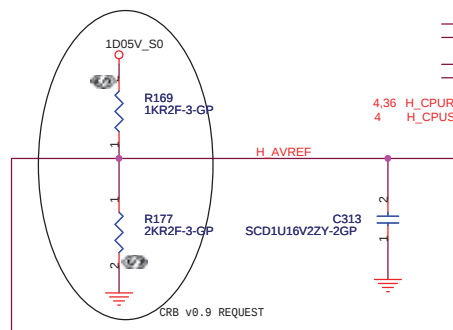


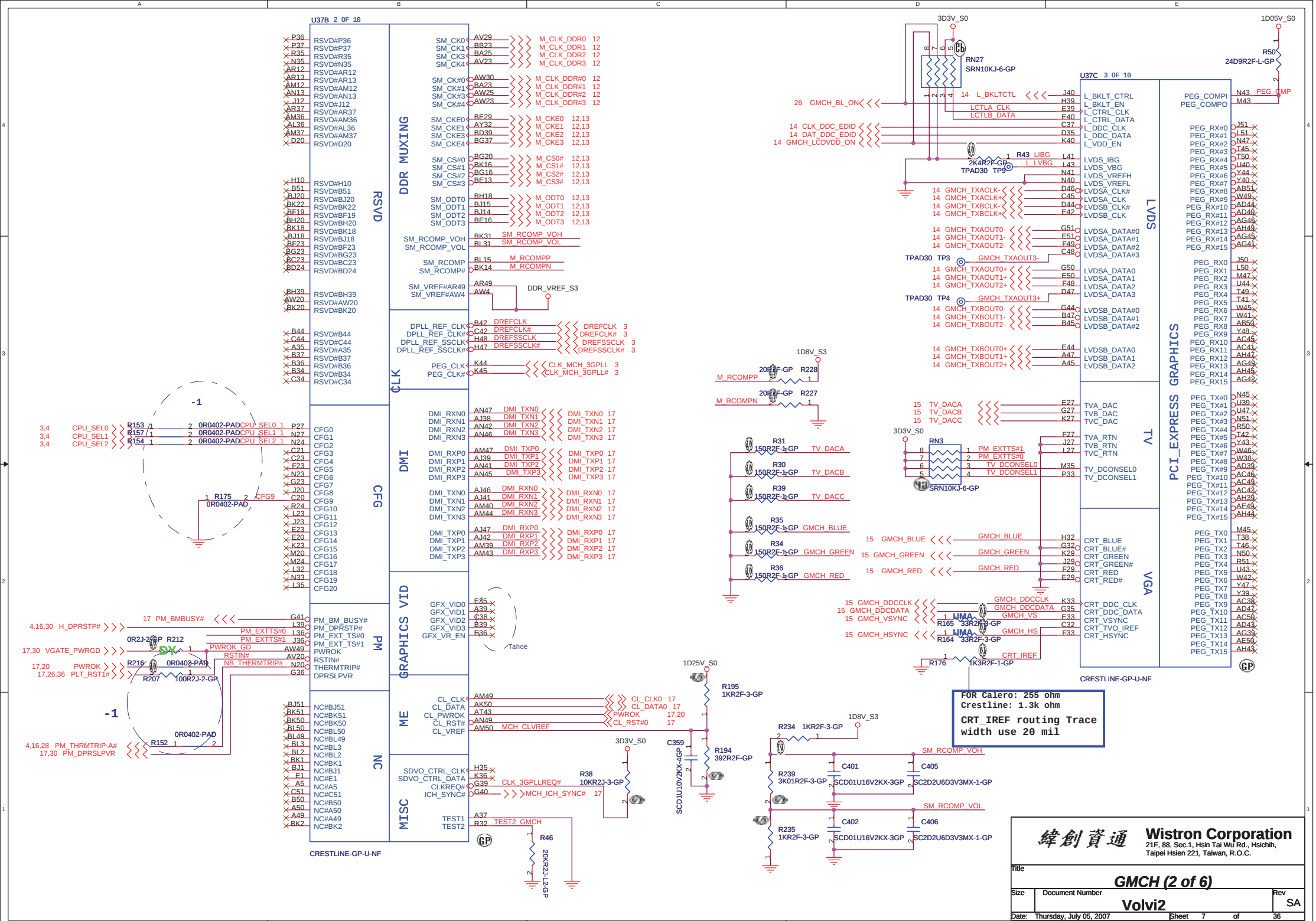
H_RCOMP routing Trace width and Spacing use 10 / 20 mil

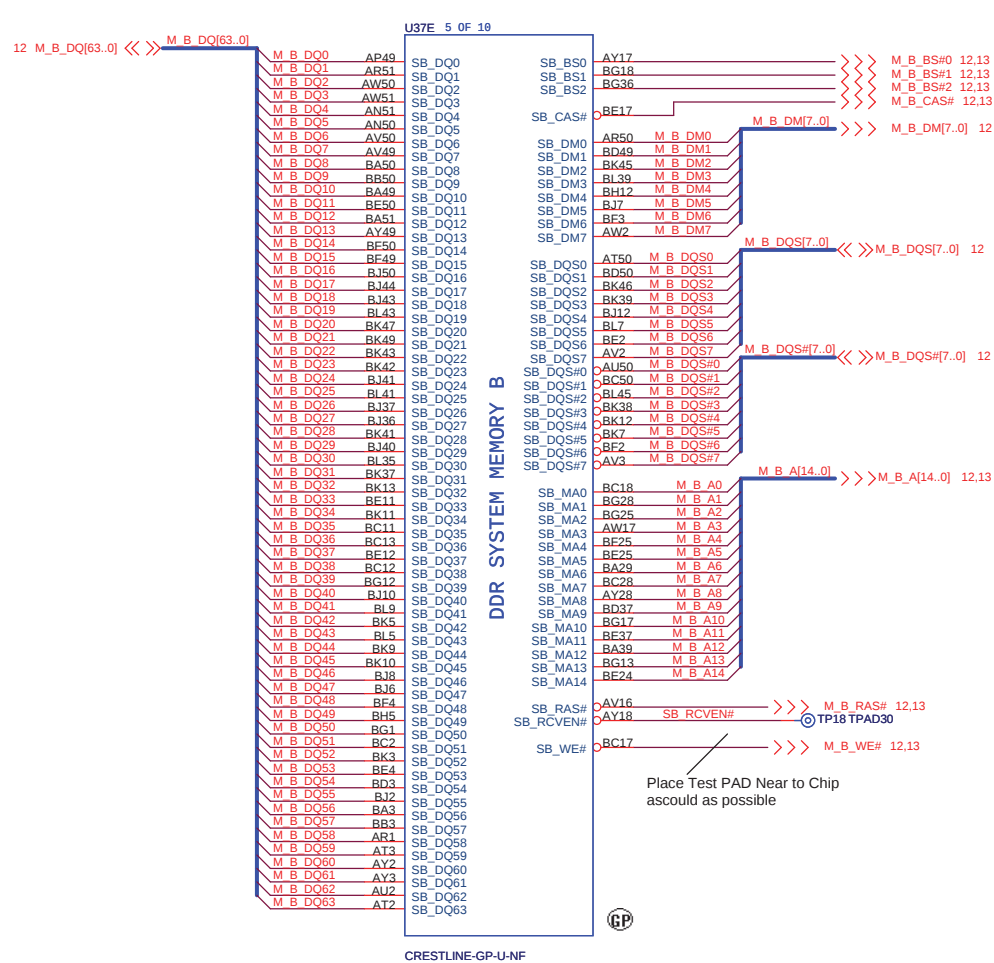
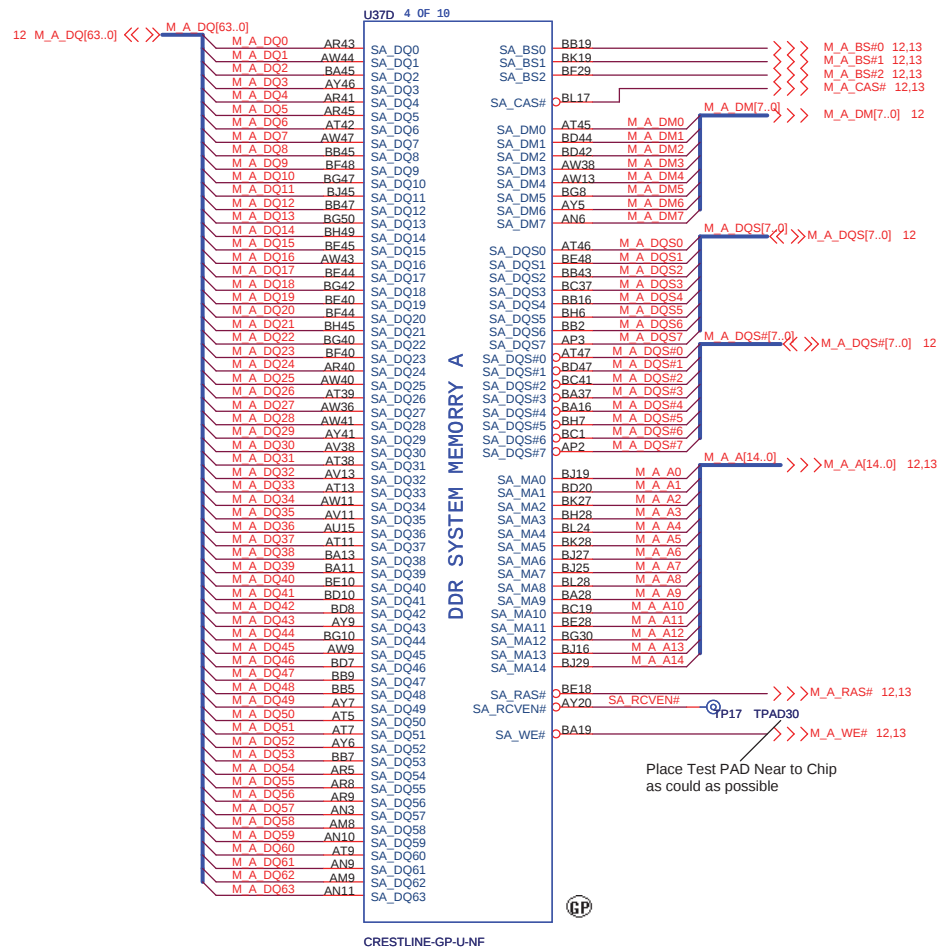


Place them near to the chip ($< 0.5''$)

H_REF Decoupling Crestline
close Crestline 100 mil



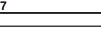
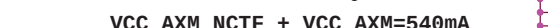


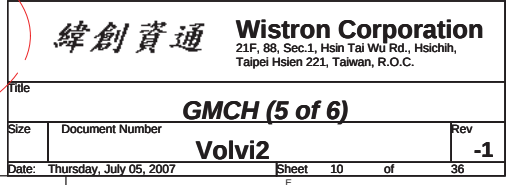


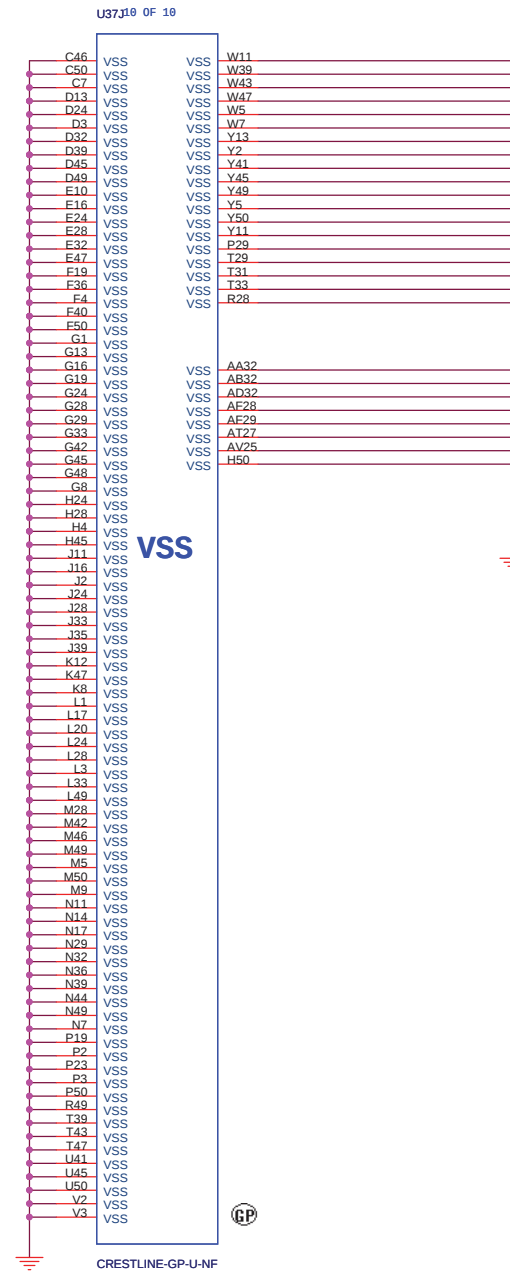
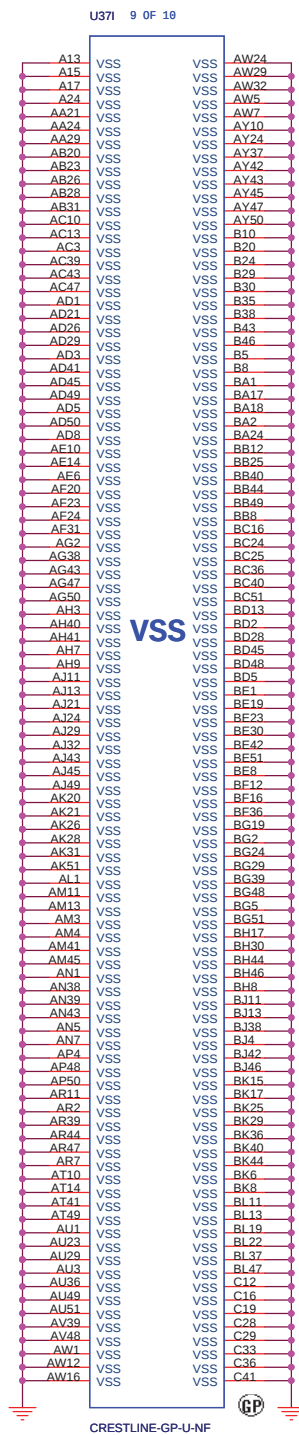
14375 6 05 18

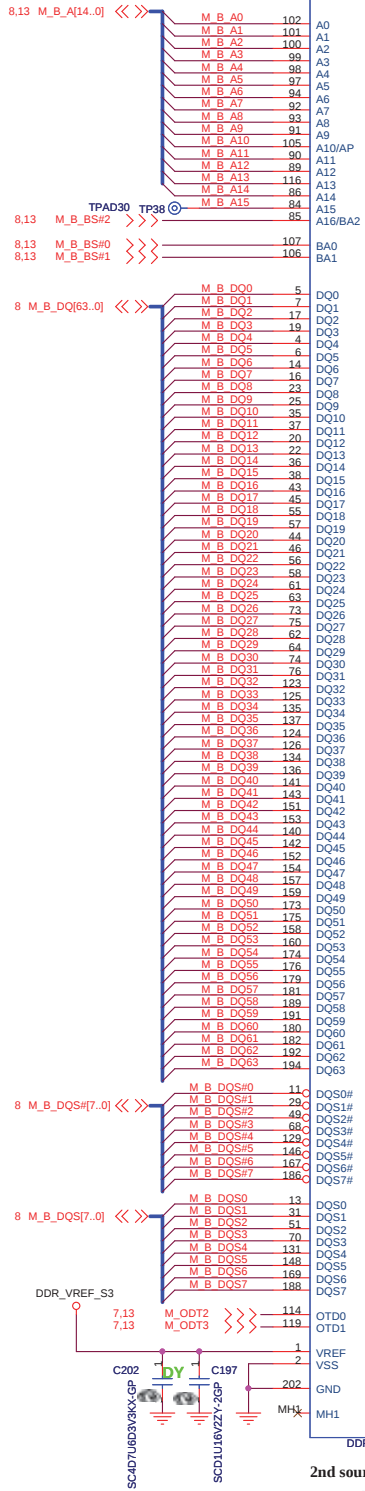


CC SM

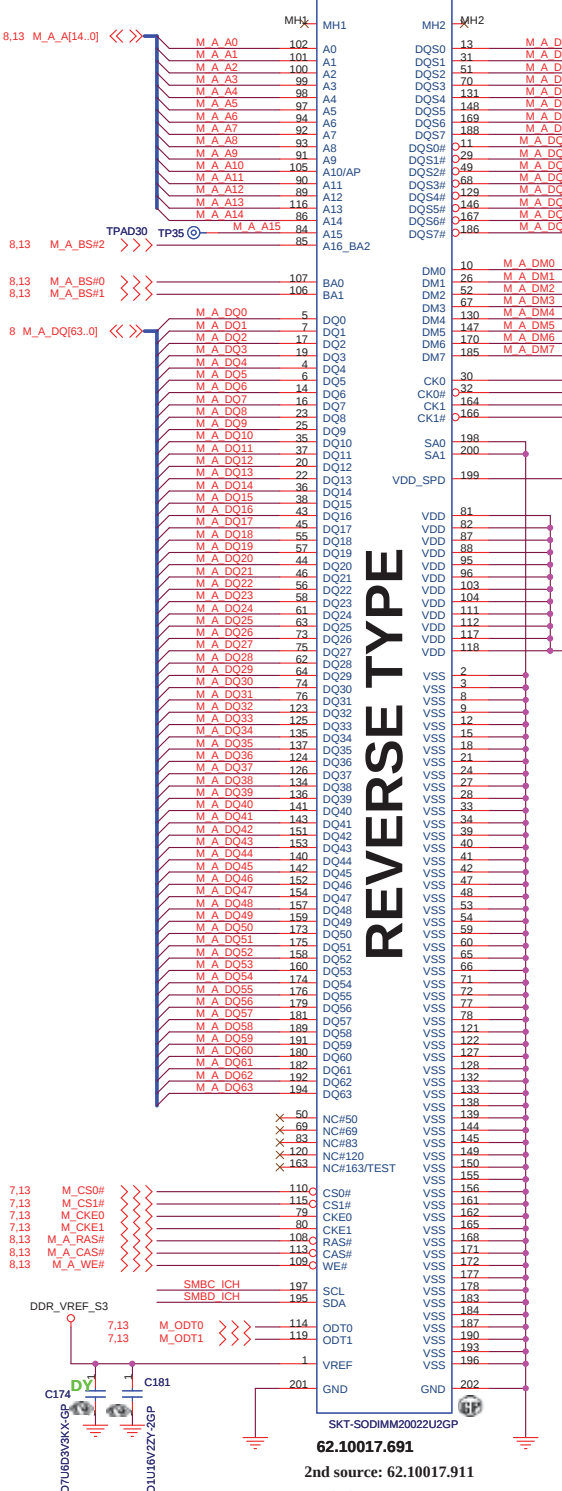
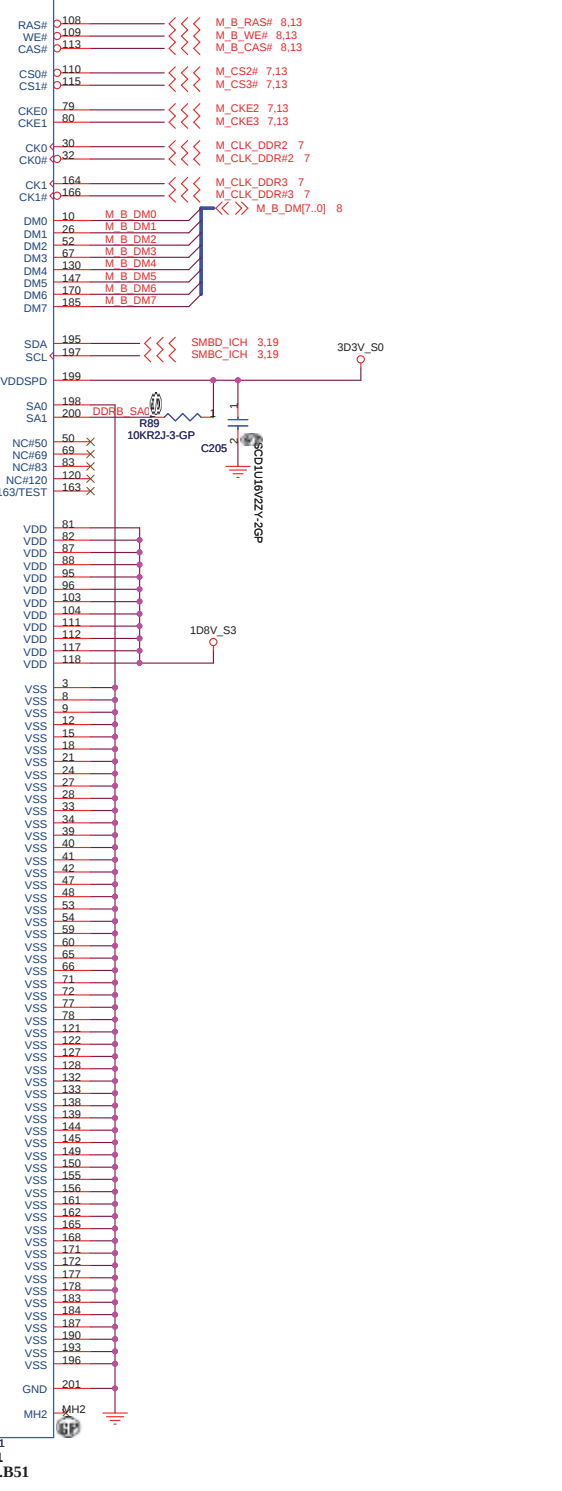








REVERSE TYPE



REVERSE TYPE

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

DDR2 Socket

Size

Document Number

Rev

Date

Thursday, July 05, 2007

Sheet

12

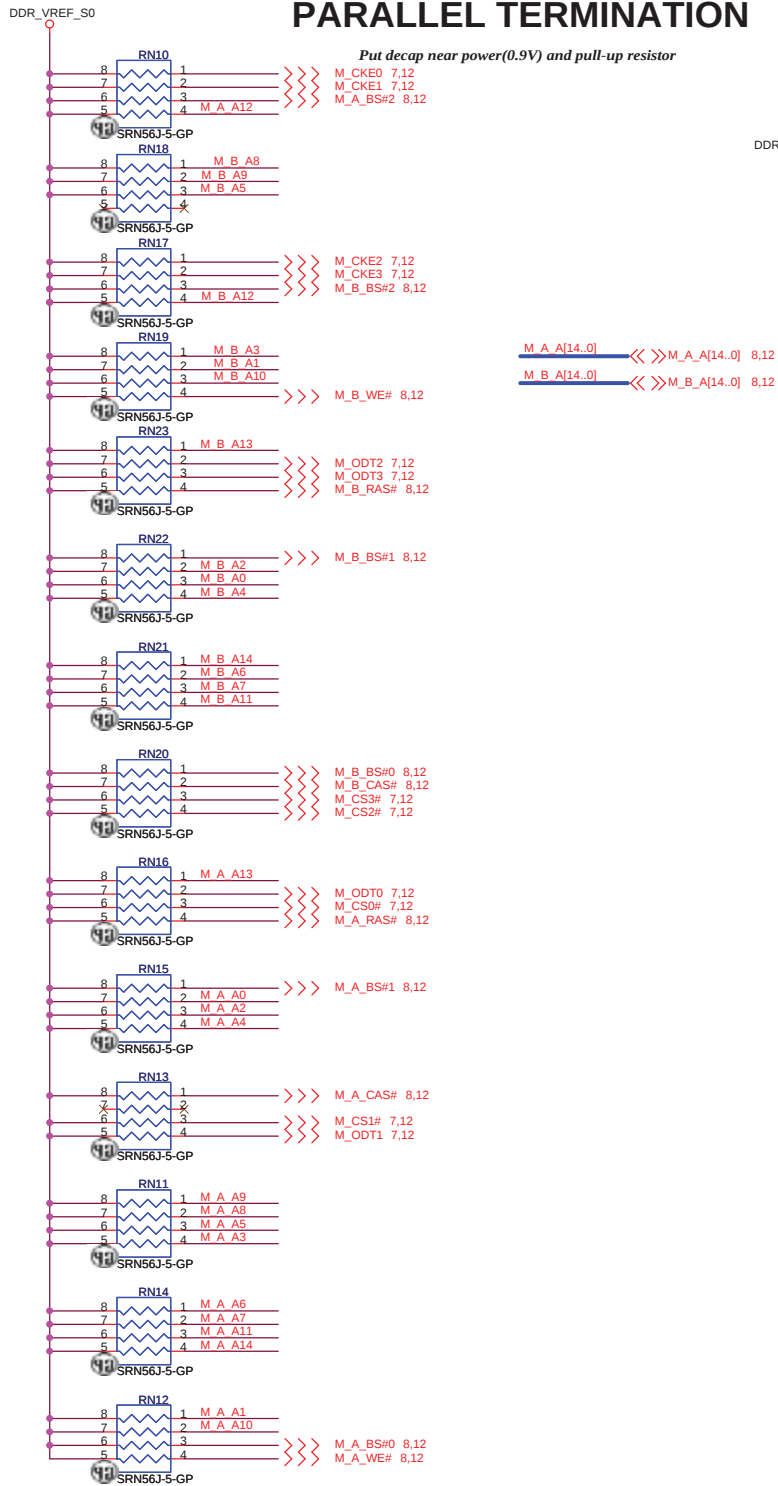
of

36

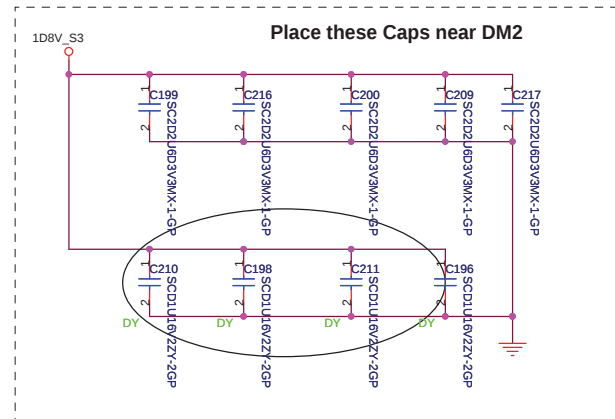
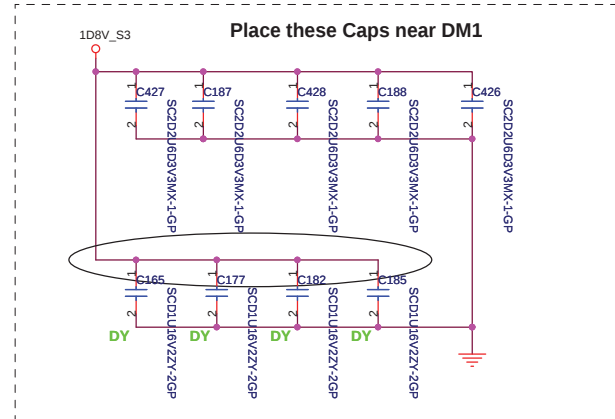
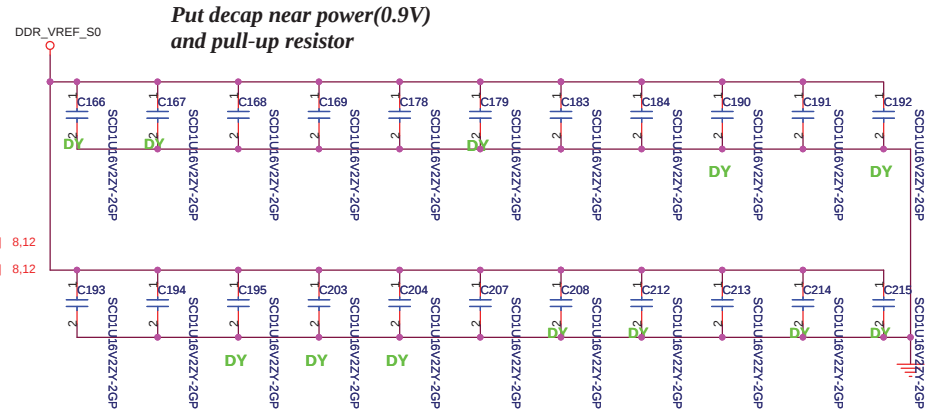
Volvi2

SA

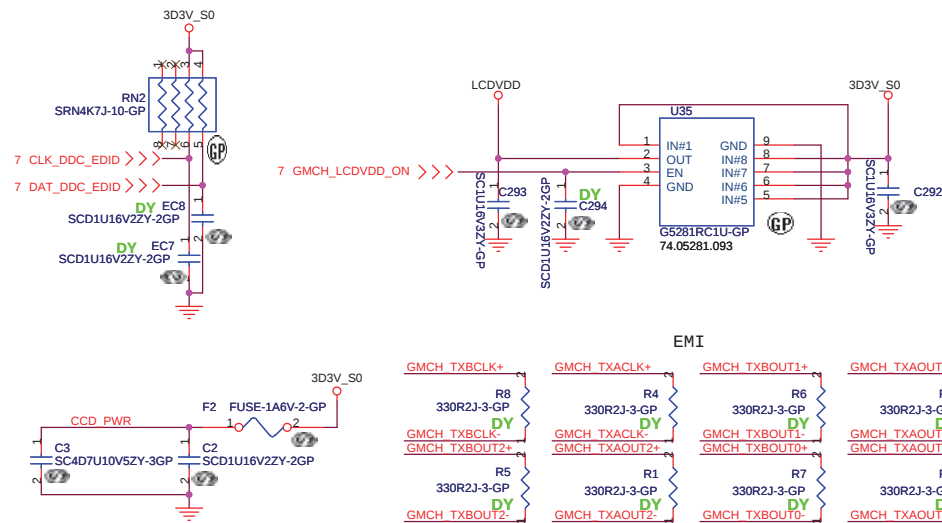
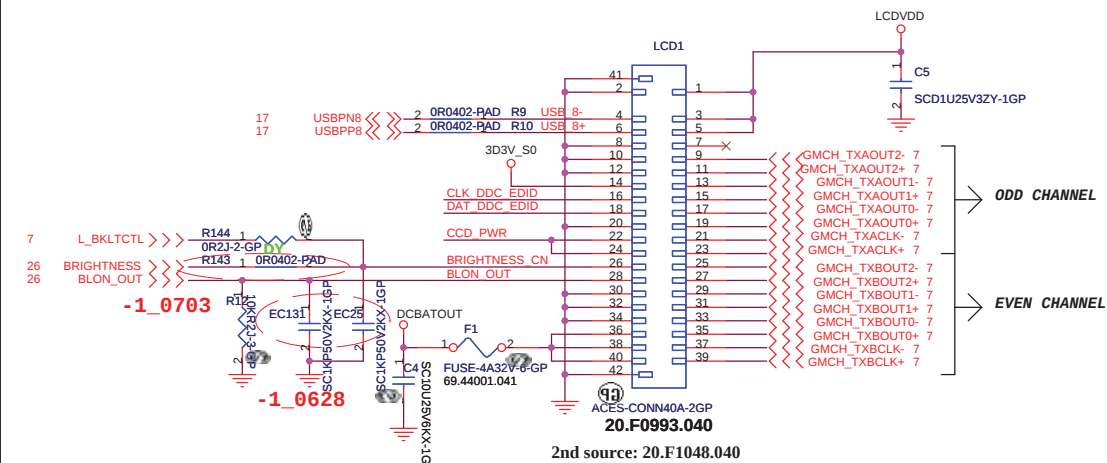
PARALLEL TERMINATION



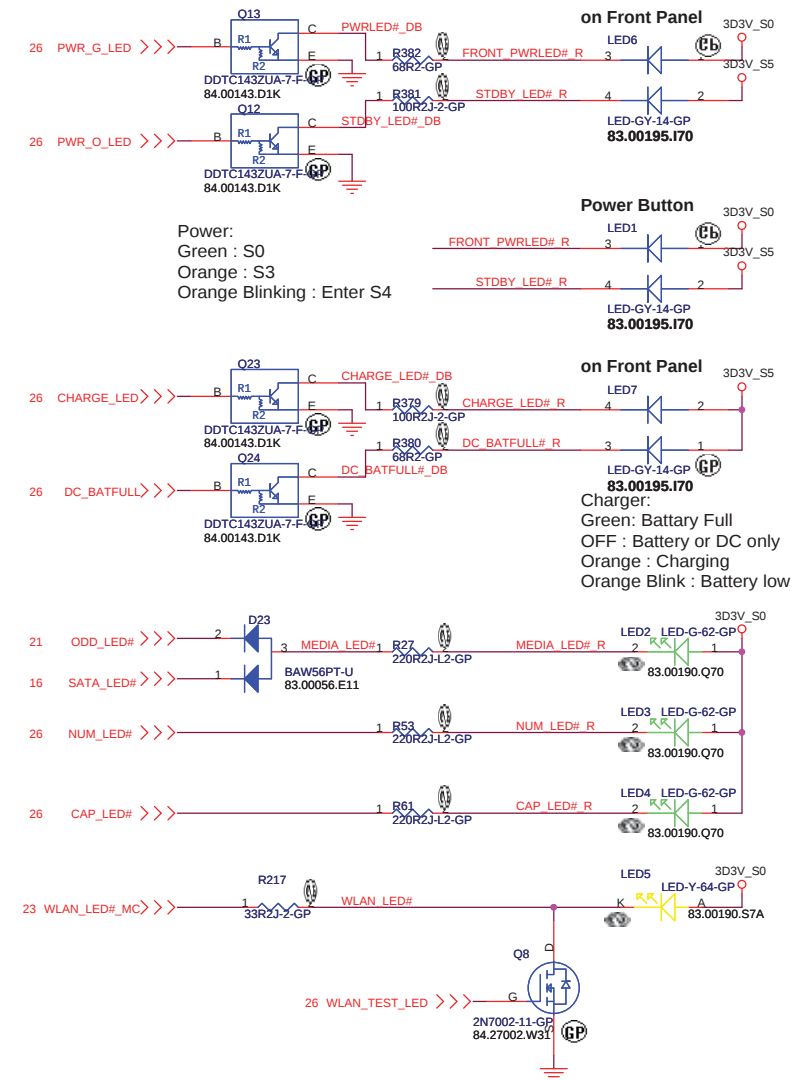
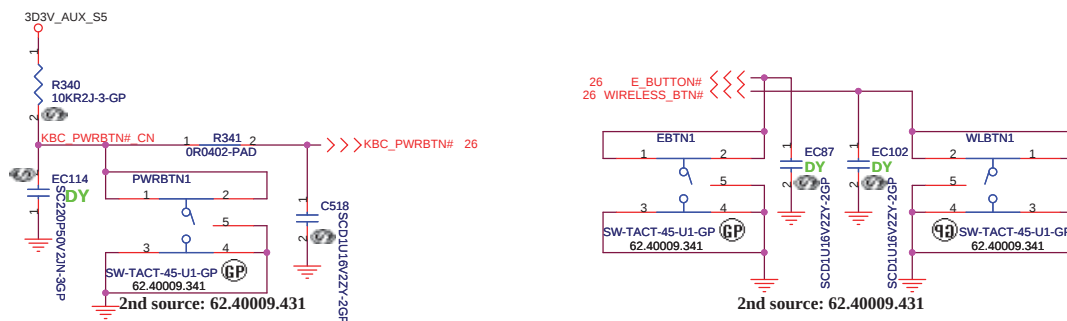
Decoupling Capacitor



LED

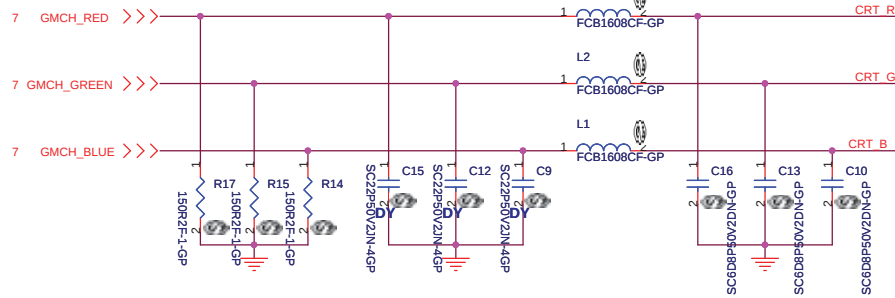


Buttons

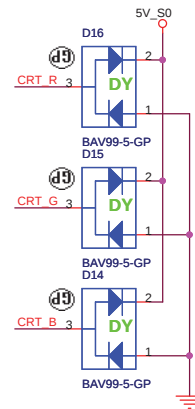


Layout Note:
Place these resistors
close to the CRT-out
connector

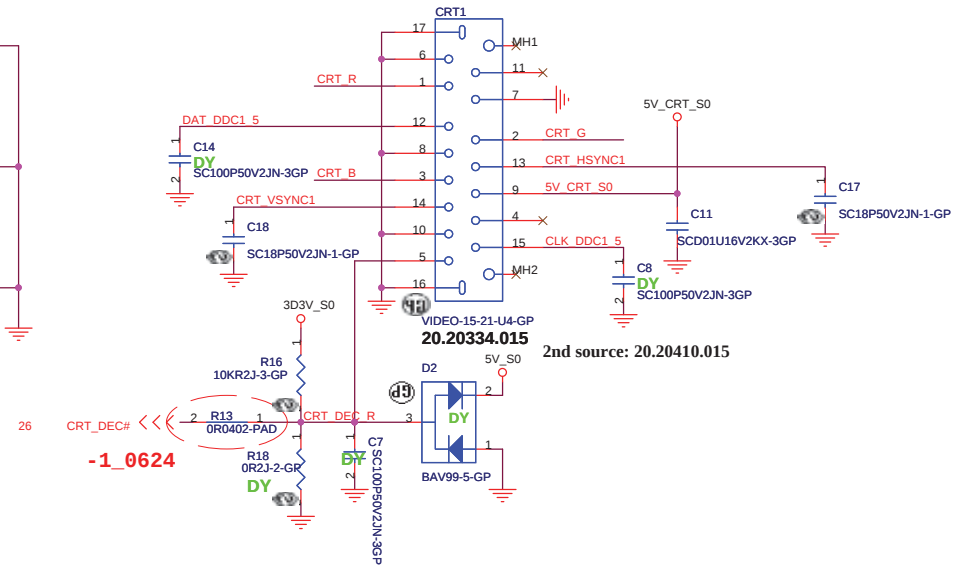
Ferrite bead impedance: 10 ohm@100MHz



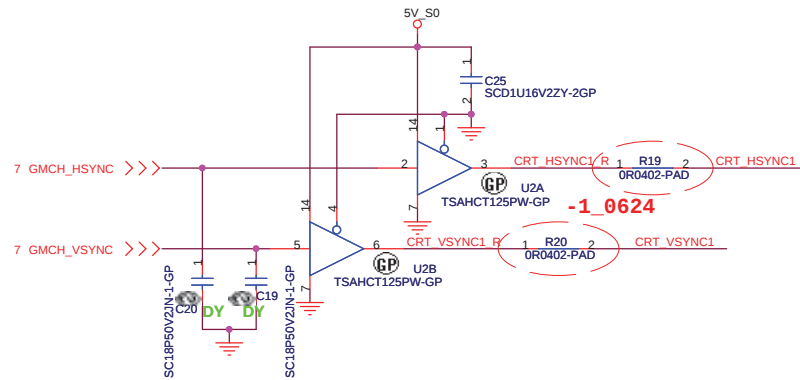
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



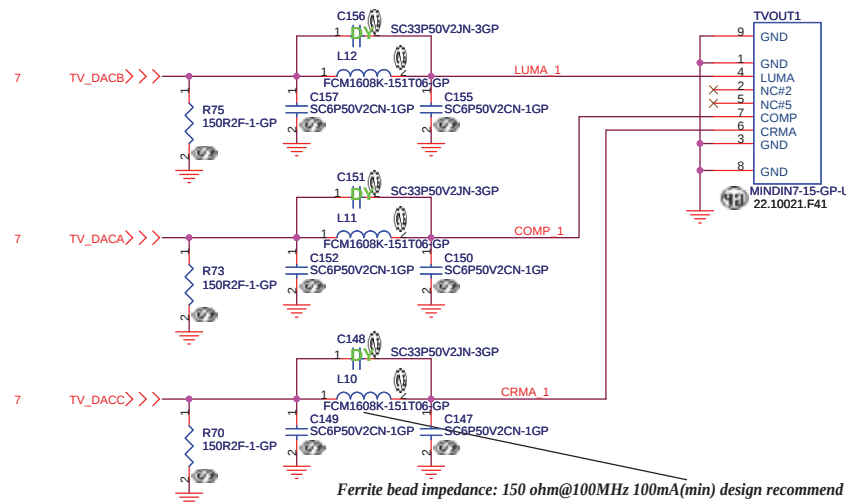
CRT I/F & CONNECTOR



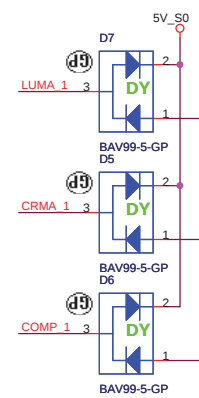
Hsync & Vsync level shift



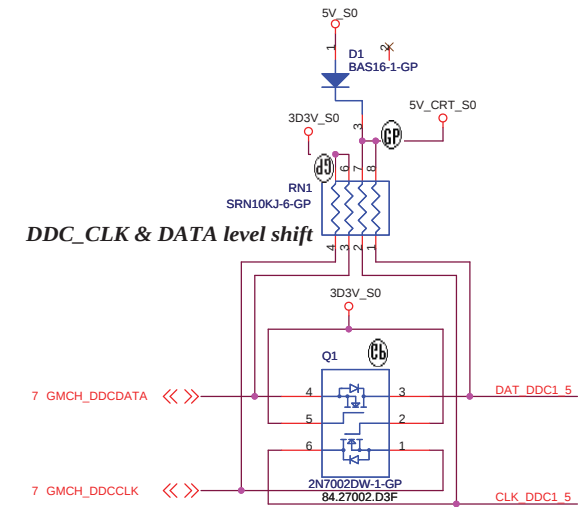
TV CONN



Ferrite bead impedance: 150 ohm@100MHz 100mA(min) design recommend

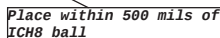
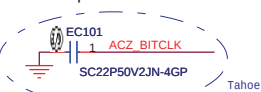
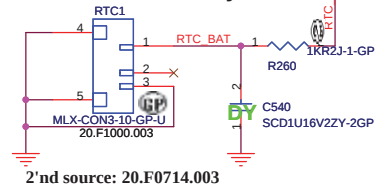


DDC_CLK & DATA level shift

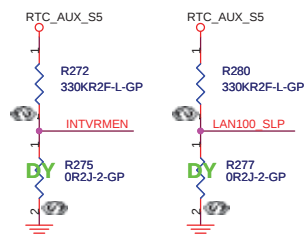


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

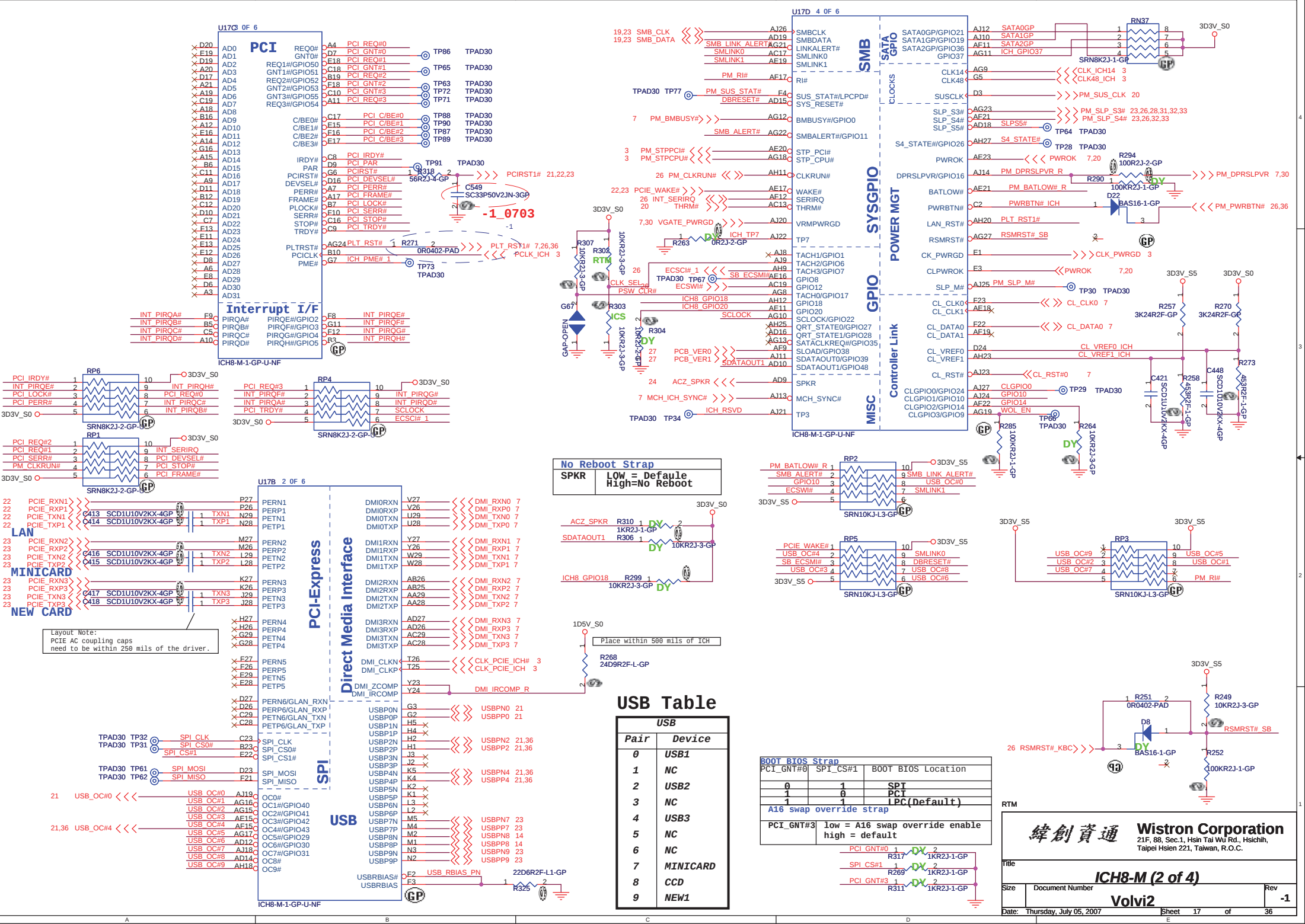
Title			
CRT/TV Connector			
Size	Document Number		Rev
	Volvi2		SA
Date:	Thursday, July 05, 2007	Sheet 15 of 36	



Change to 24.9 1% ohm when use SATA HD



RTM				
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title				
Size		Document Number		Rev
		ICH8-M (1 of 4)		SA
Date: Thursday, July 05, 2007		Volvi2		
	Sheet	16	of	36



No Reboot Strap
SPKR LOW = Default
High = No Reboot

USB Table

USB	
Pair	Device
0	USB1
1	NC
2	USB2
3	NC
4	USB3
5	NC
6	NC
7	MINICARD
8	CCD
9	NEW1

BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCT
1	1	LPC(Default)

A16 swap override strap

PCI_GNT#3	low = A16 swap override enable high = default
-----------	--

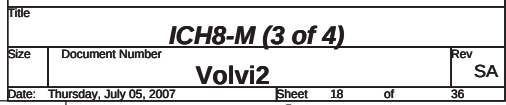
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ICH8-M (2 of 4)

Size: Document Number: Volvi2

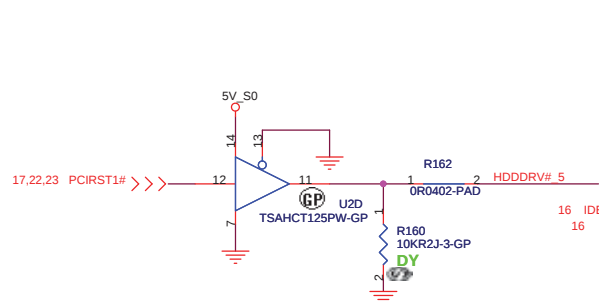
Date: Thursday, July 05, 2007 Sheet 17 of 36

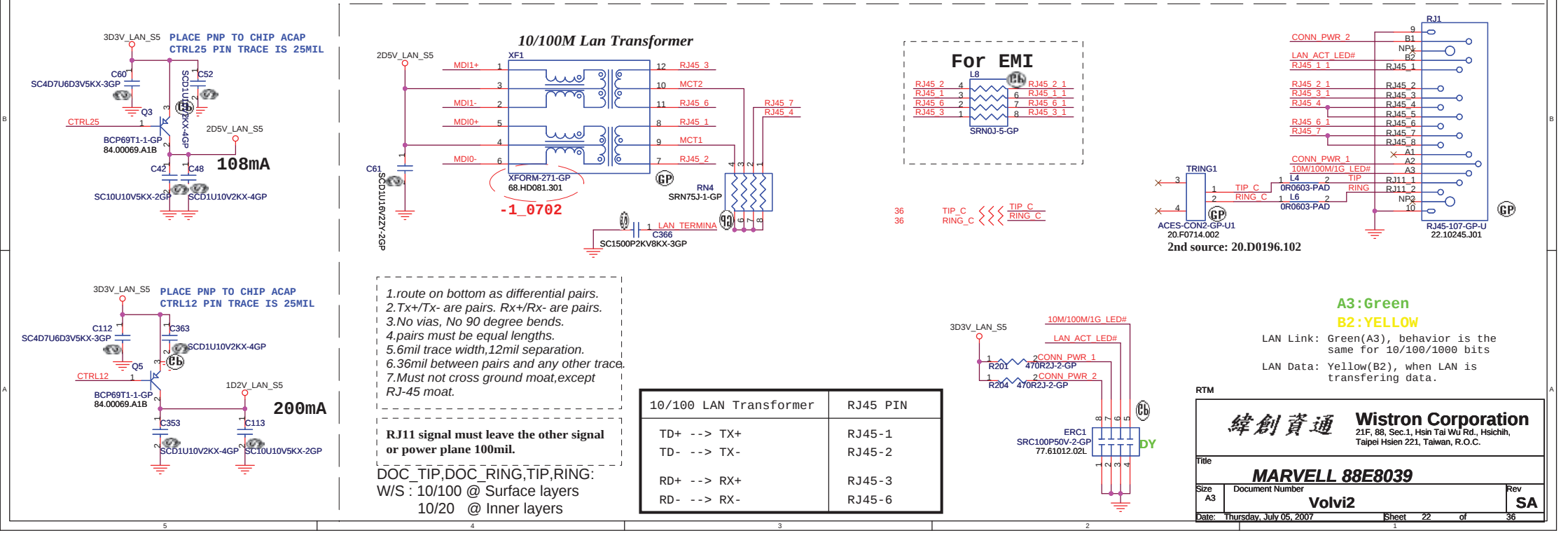
Rev: -1



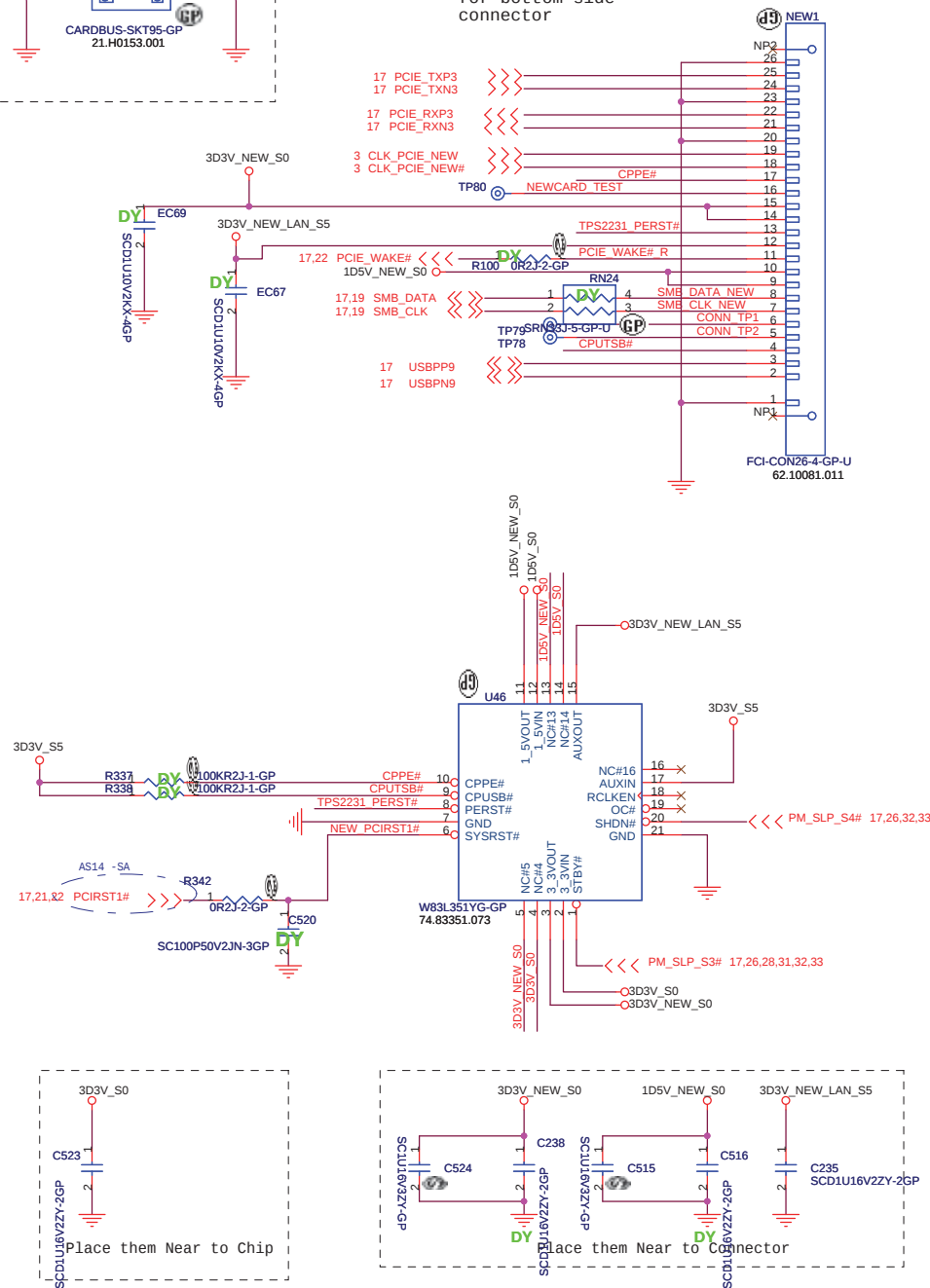
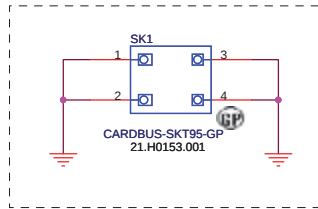
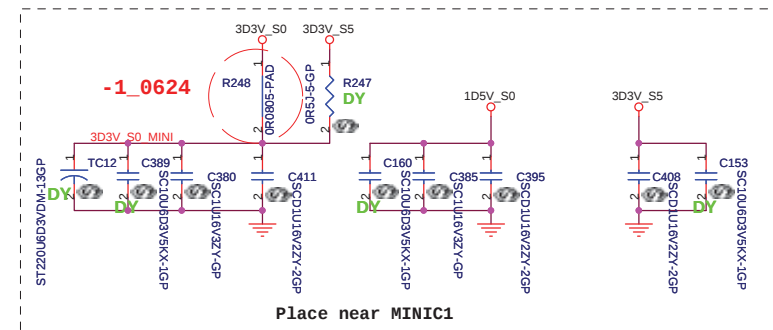


SMBUS

[illegible]



Reserve the symbol
for bottom side
connector

[illegible]

RTM

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

		Title
--	--	-------

MINI CARD / NEW CARD

Size

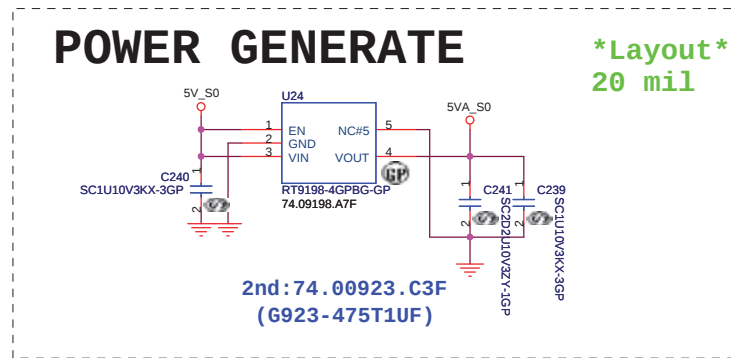
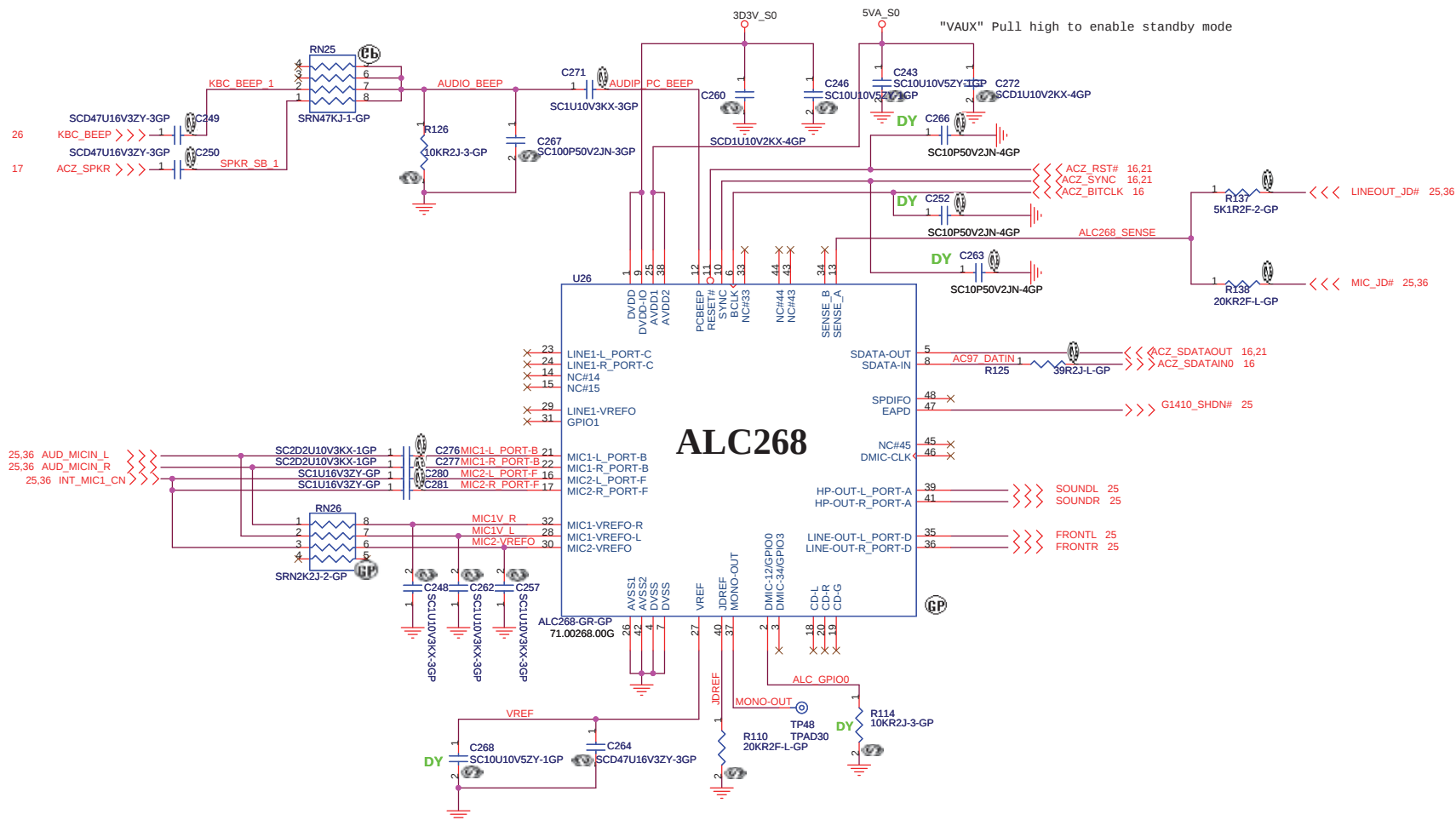
	Document Number
--	-----------------

Volvi2

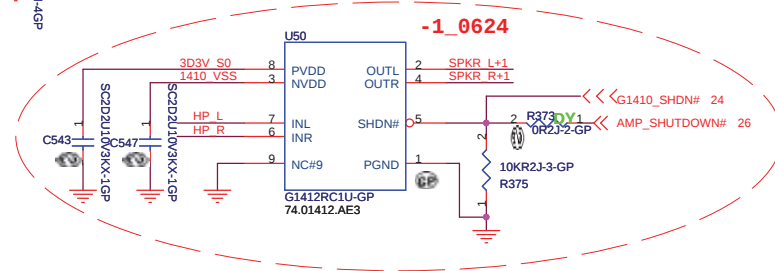
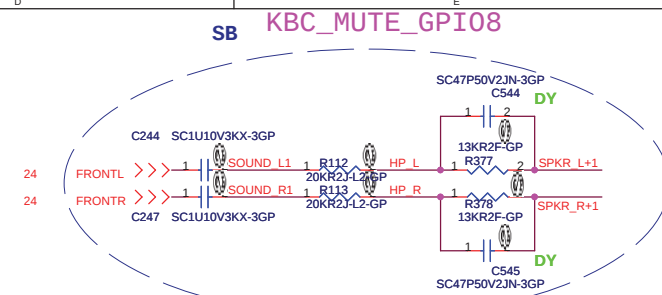
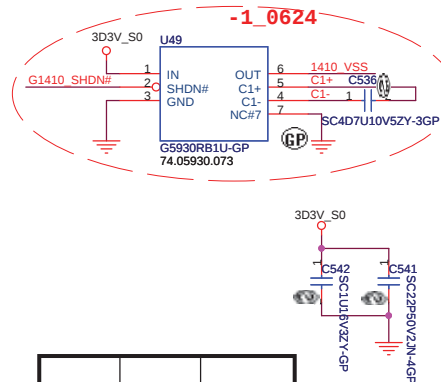
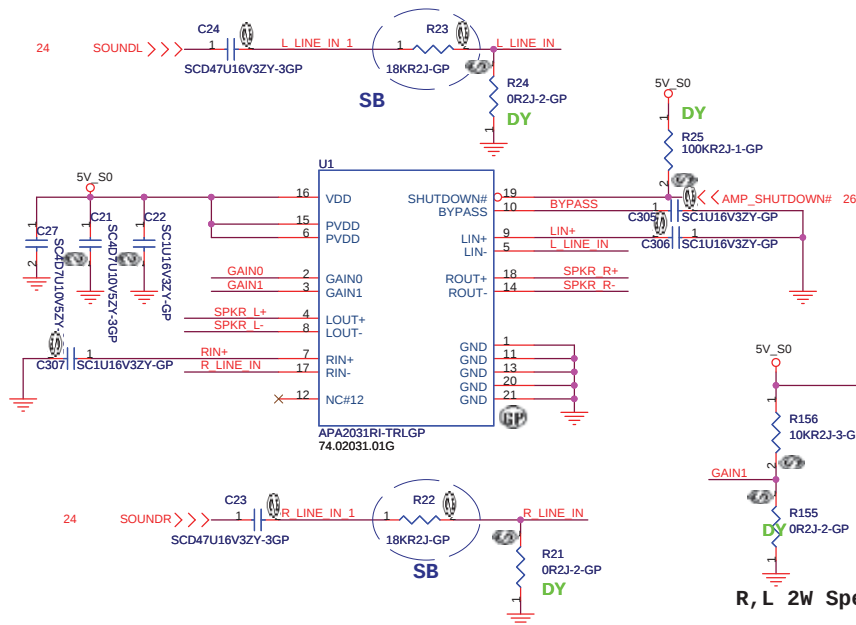
Date: Thursday, July 05, 2007

Sheet 23 of 36

SA



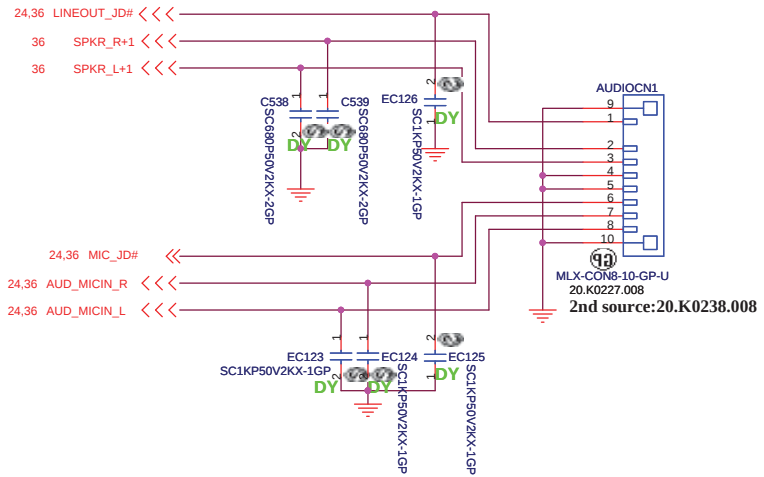
AUDIO OP AMPLIFIER



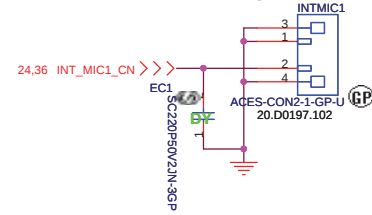
GAIN0	GAIN1	Av (dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6

R, L 2W Speaker

Audio Connector

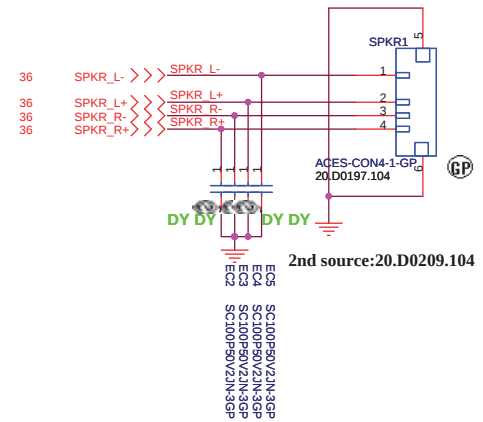


Internal Microphone



2nd source:20.D0209.102

Internal Speaker

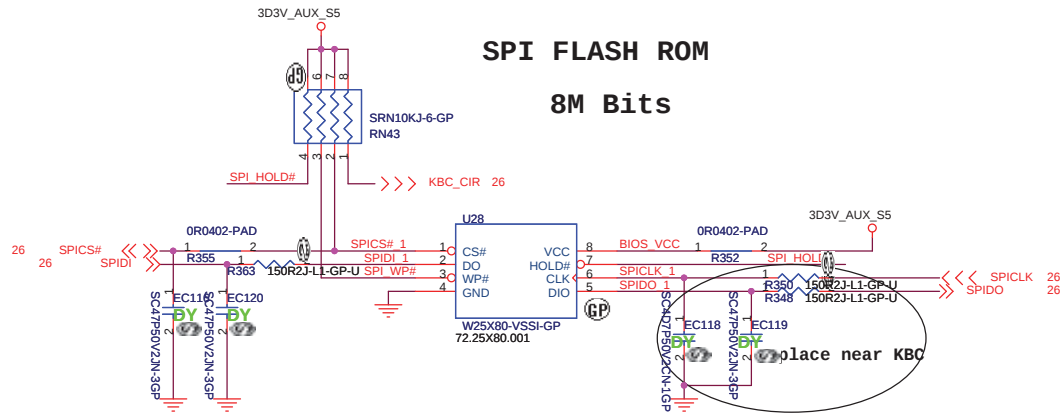


2nd source:20.D0209.104

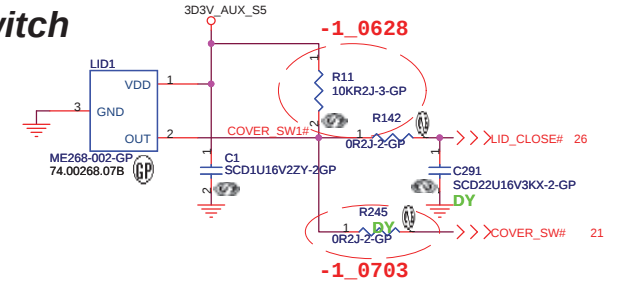
RTM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

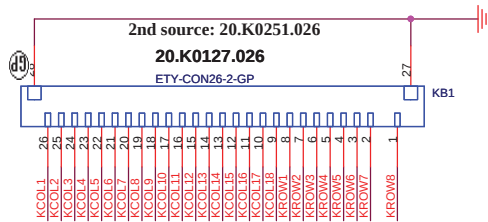
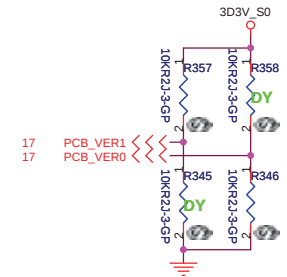




Hall Switch



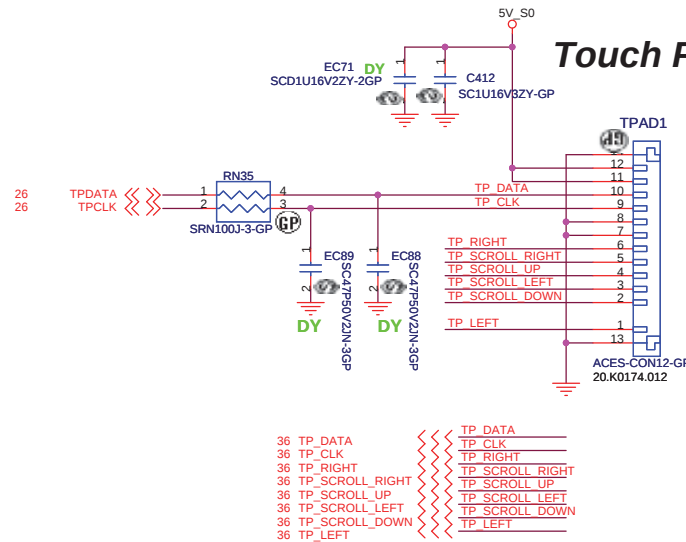
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1



EMI Bypass cap.

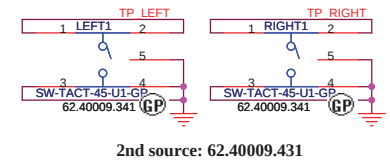
KCOL16	EC59	1	SC220P50V2JN-3GP
KCOL15	EC45	1	SC220P50V2JN-3GP
KCOL14	EC58	1	SC220P50V2JN-3GP
KCOL13	EC44	1	SC220P50V2JN-3GP
KCOL18	EC80	1	SC220P50V2JN-3GP
KCOL8	EC55	1	SC220P50V2JN-3GP
KCOL7	EC41	1	SC220P50V2JN-3GP
KCOL6	EC54	1	SC220P50V2JN-3GP
KCOL5	EC40	1	SC220P50V2JN-3GP
KCOL4	EC53	1	SC220P50V2JN-3GP
KCOL3	EC39	1	SC220P50V2JN-3GP
KCOL2	EC52	1	SC220P50V2JN-3GP
KCOL1	EC38	1	SC220P50V2JN-3GP
KROW8	EC64	1	SC220P50V2JN-3GP
KROW7	EC50	1	SC220P50V2JN-3GP
KROW6	EC63	1	SC220P50V2JN-3GP
KROW5	EC49	1	SC220P50V2JN-3GP
KCOL17	EC46	1	SC220P50V2JN-3GP
KROW4	EC62	1	SC220P50V2JN-3GP
KROW3	EC48	1	SC220P50V2JN-3GP
KROW2	EC61	1	SC220P50V2JN-3GP
KROW1	EC47	1	SC220P50V2JN-3GP
KCOL12	EC57	1	SC220P50V2JN-3GP
KCOL11	EC43	1	SC220P50V2JN-3GP
KCOL10	EC56	1	SC220P50V2JN-3GP
KCOL9	EC42	1	SC220P50V2JN-3GP

Internal KeyBoard CONN



Touch Pad CONN

Touch Pad Button



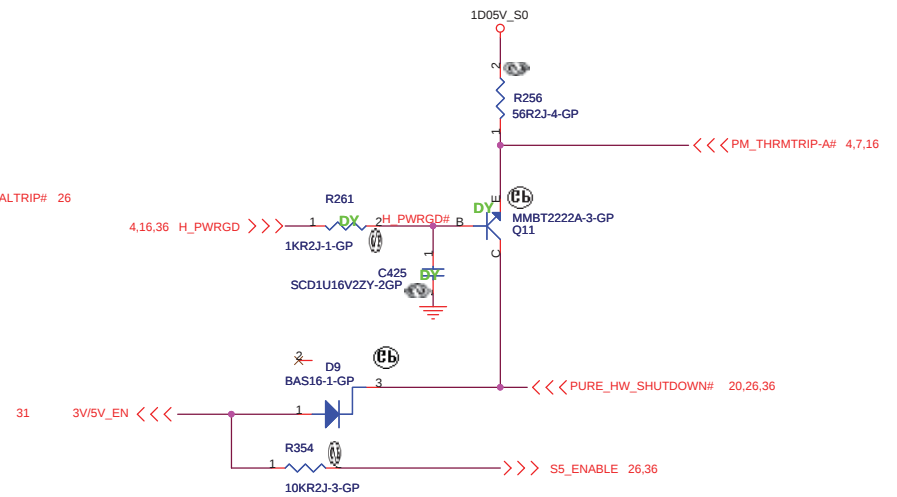
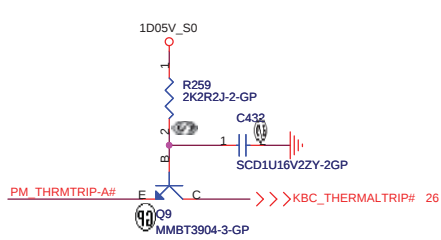
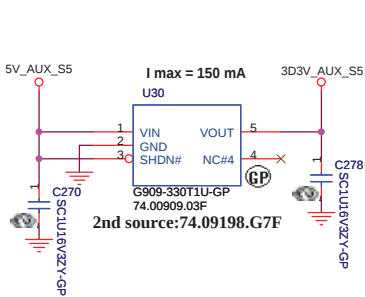
RTM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

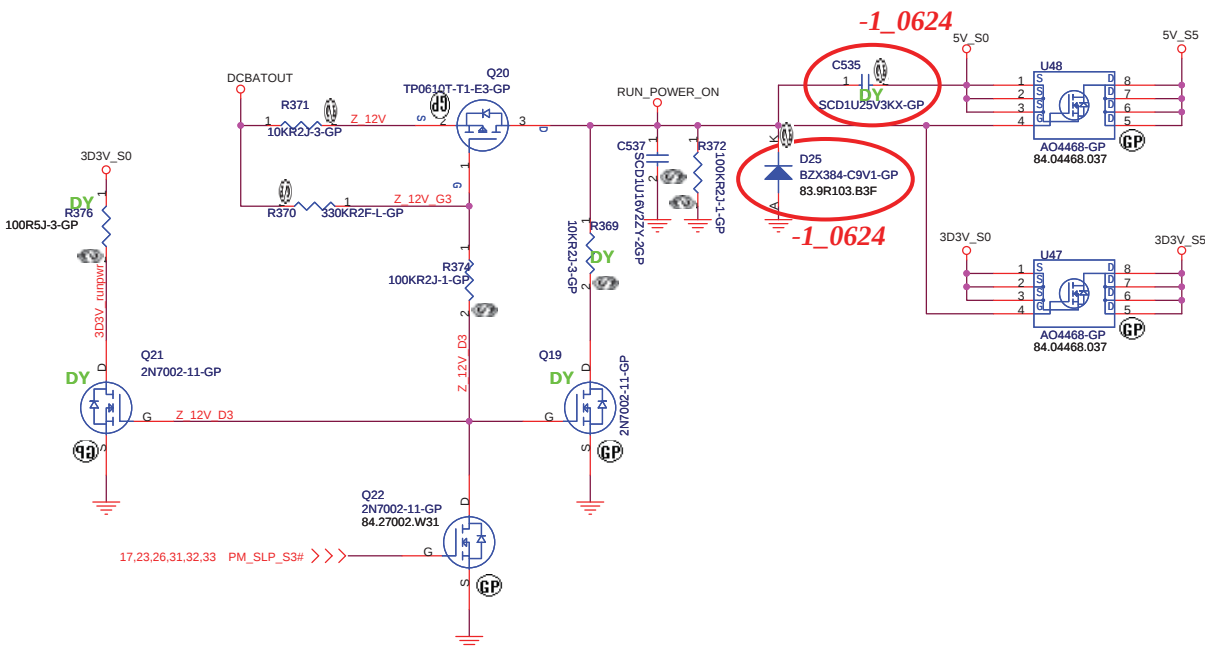
Title	BUTTONS / KB / TOUCHPAD / BIOS		
Size	Document Number	Rev	-1
Date	Thursday, July 05, 2007	Sheet 27 of 36	

Aux Power

3D3V_AUX_S5



Run Power



RTM

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

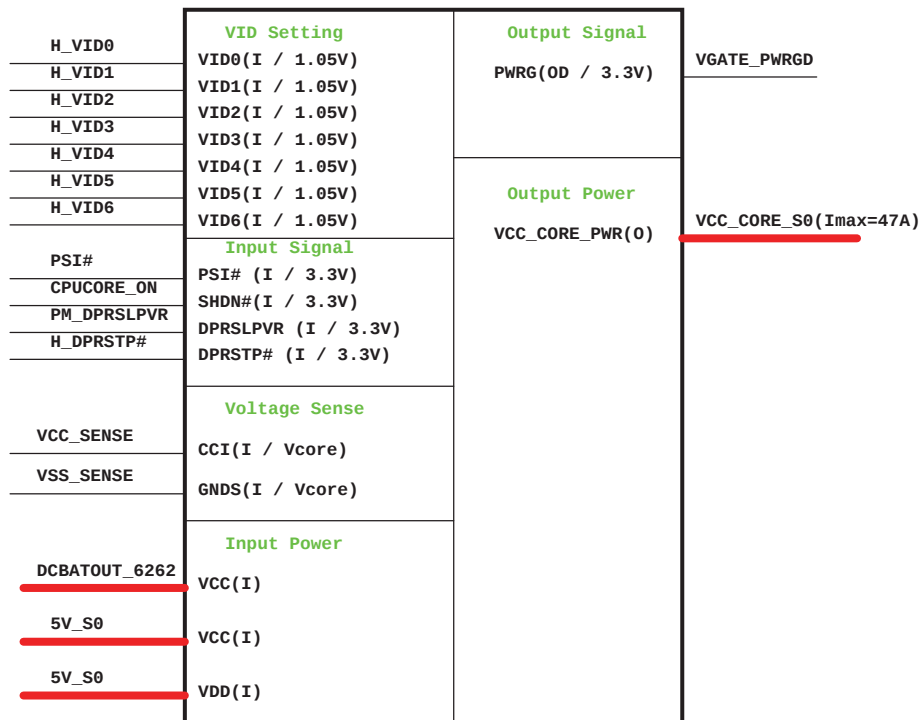
Title	<i>RUN POWER and 3D3V_AUX_S5</i>
-------	---

Size	Document Number	Rev
------	-----------------	-----

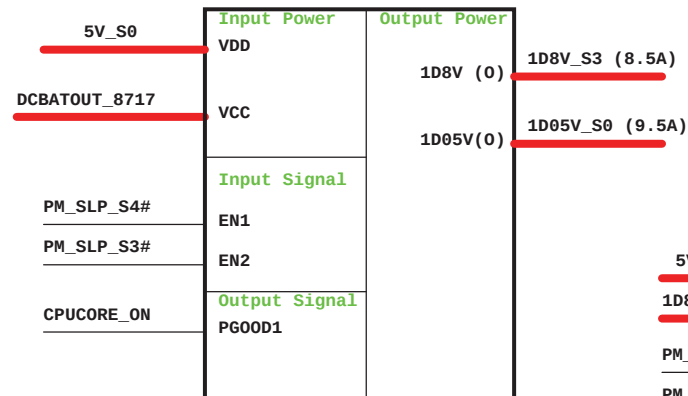
Date: Thursday, July 05, 2007

Sheet 28 of 36

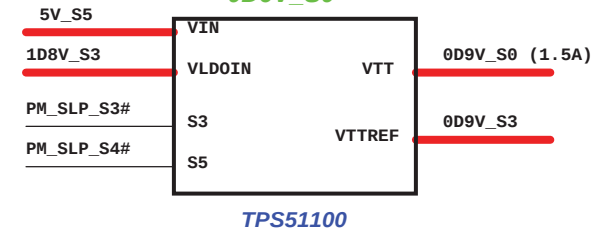
CPU_CORE MAX8770



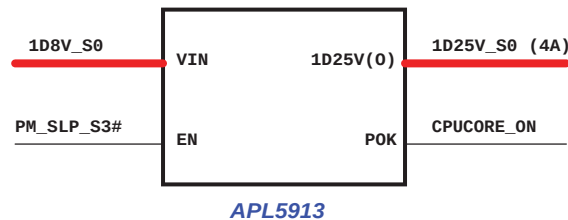
TPS51124 1D8V/1D05V



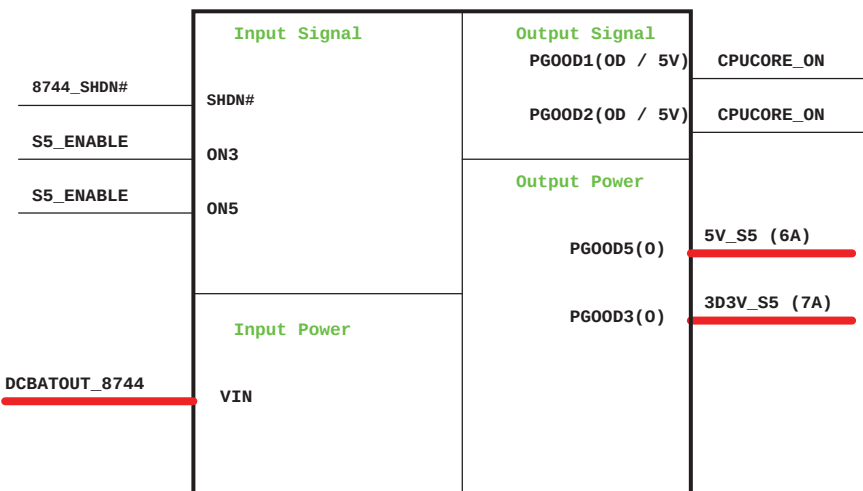
0D9V_S0



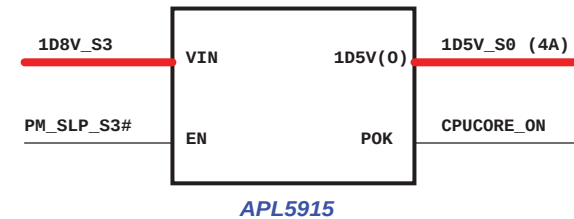
1D25V_S0



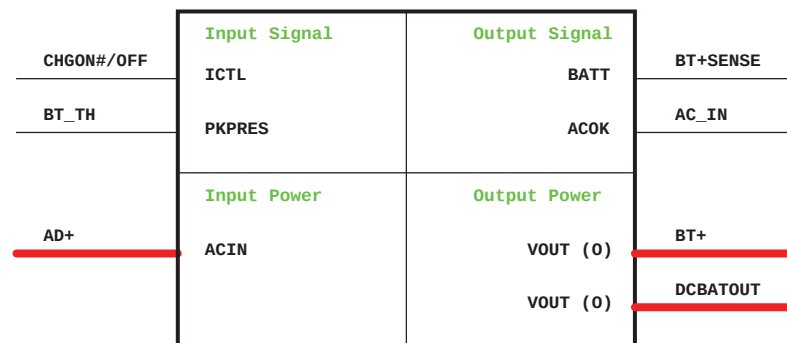
MAX8744 5V/3D3V

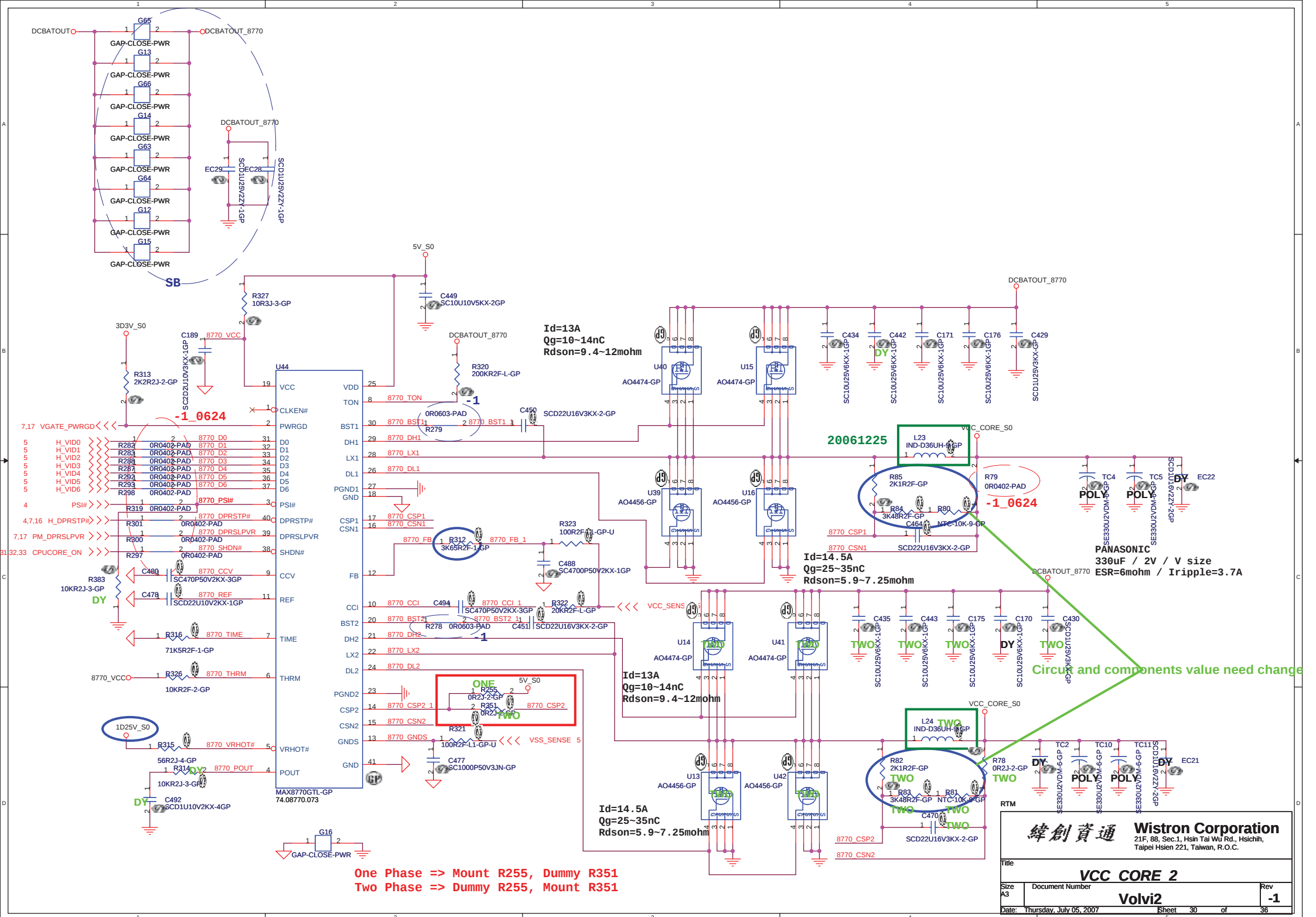


1D5V_S0



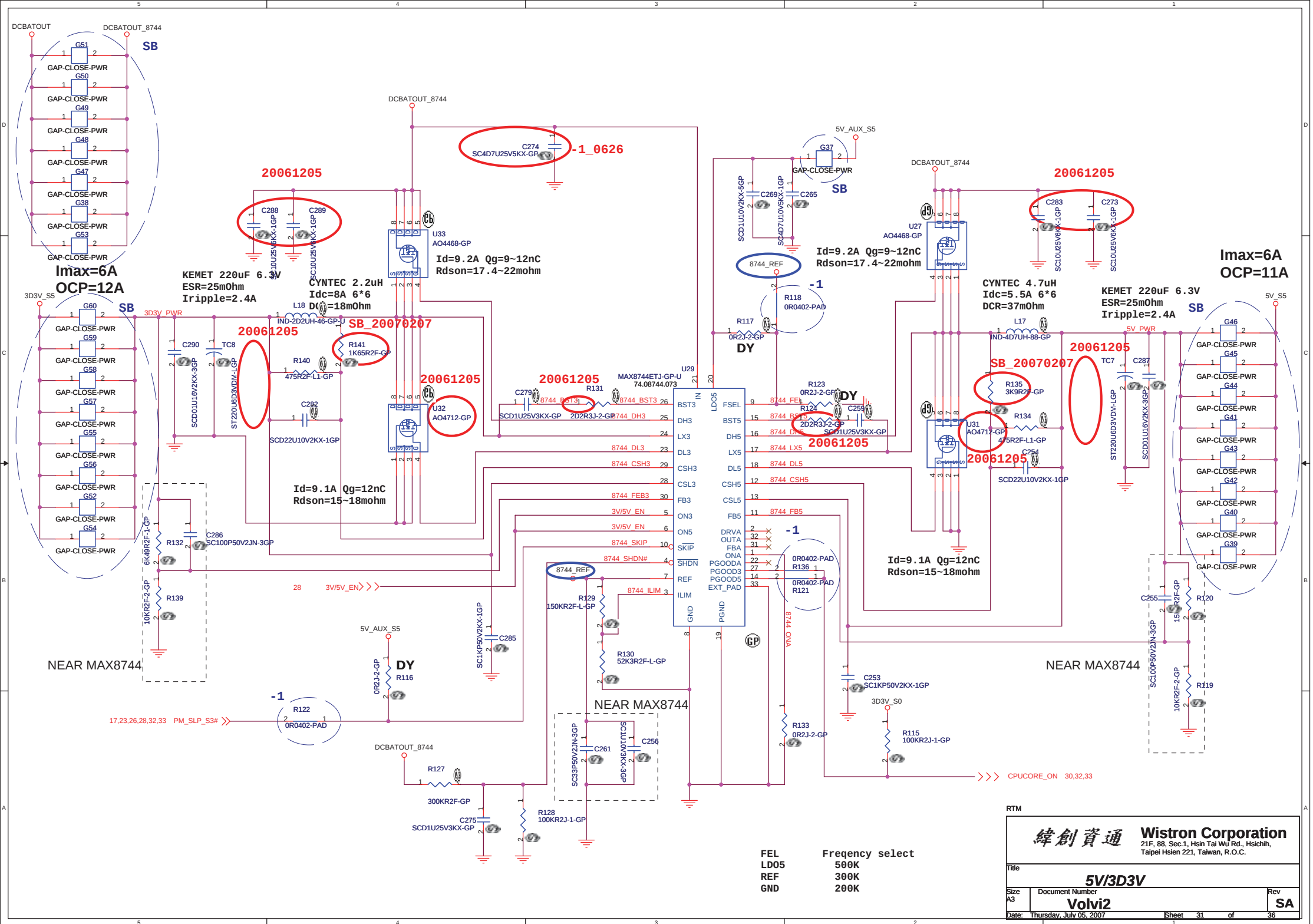
Charger MAX8731

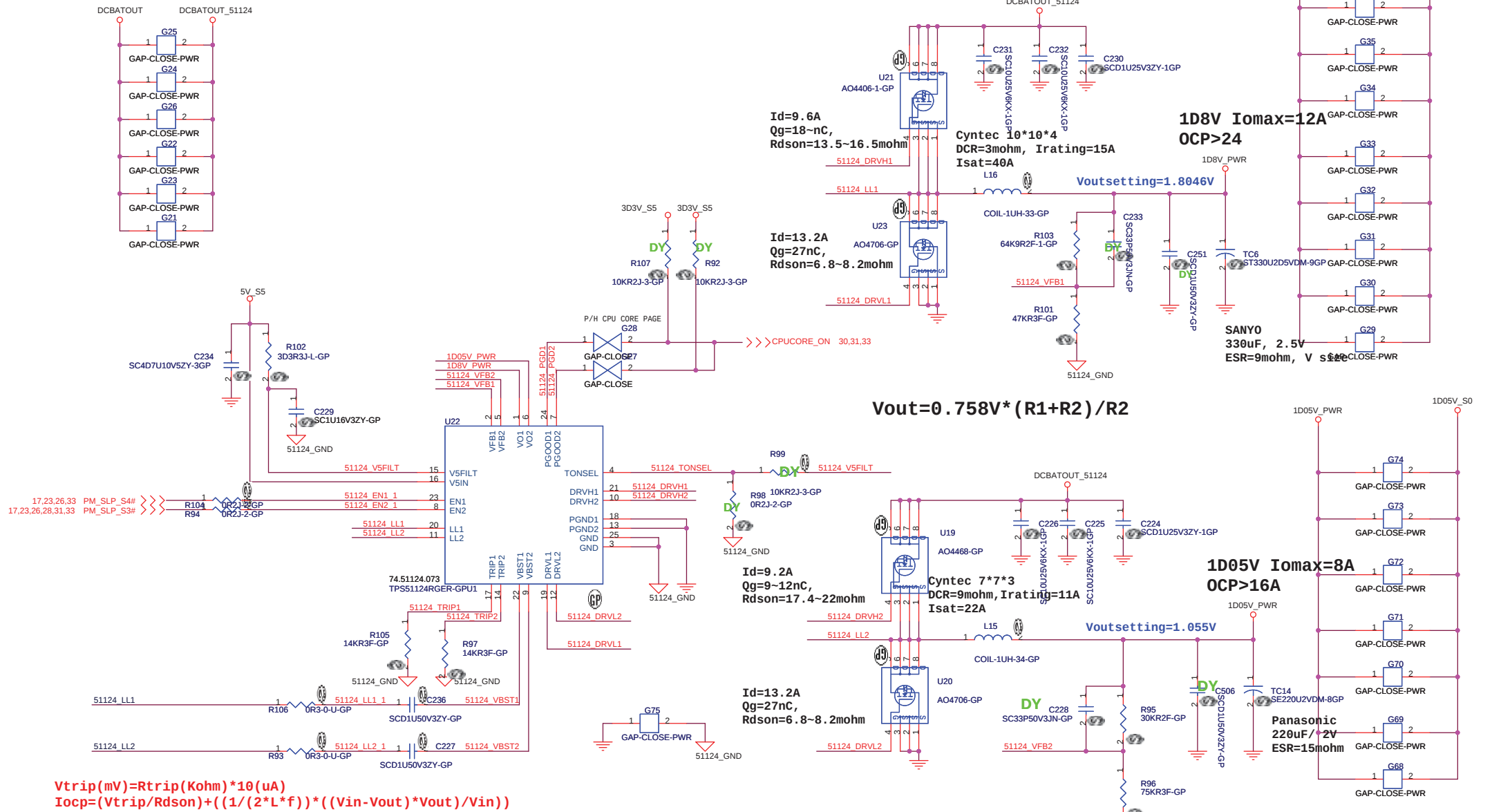




緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			VCC CORE 2		
Size	Document Number		Rev		
A3			Volvi2		-1
Date:	Thursday, July 05, 2007		Sheet	30	of 36



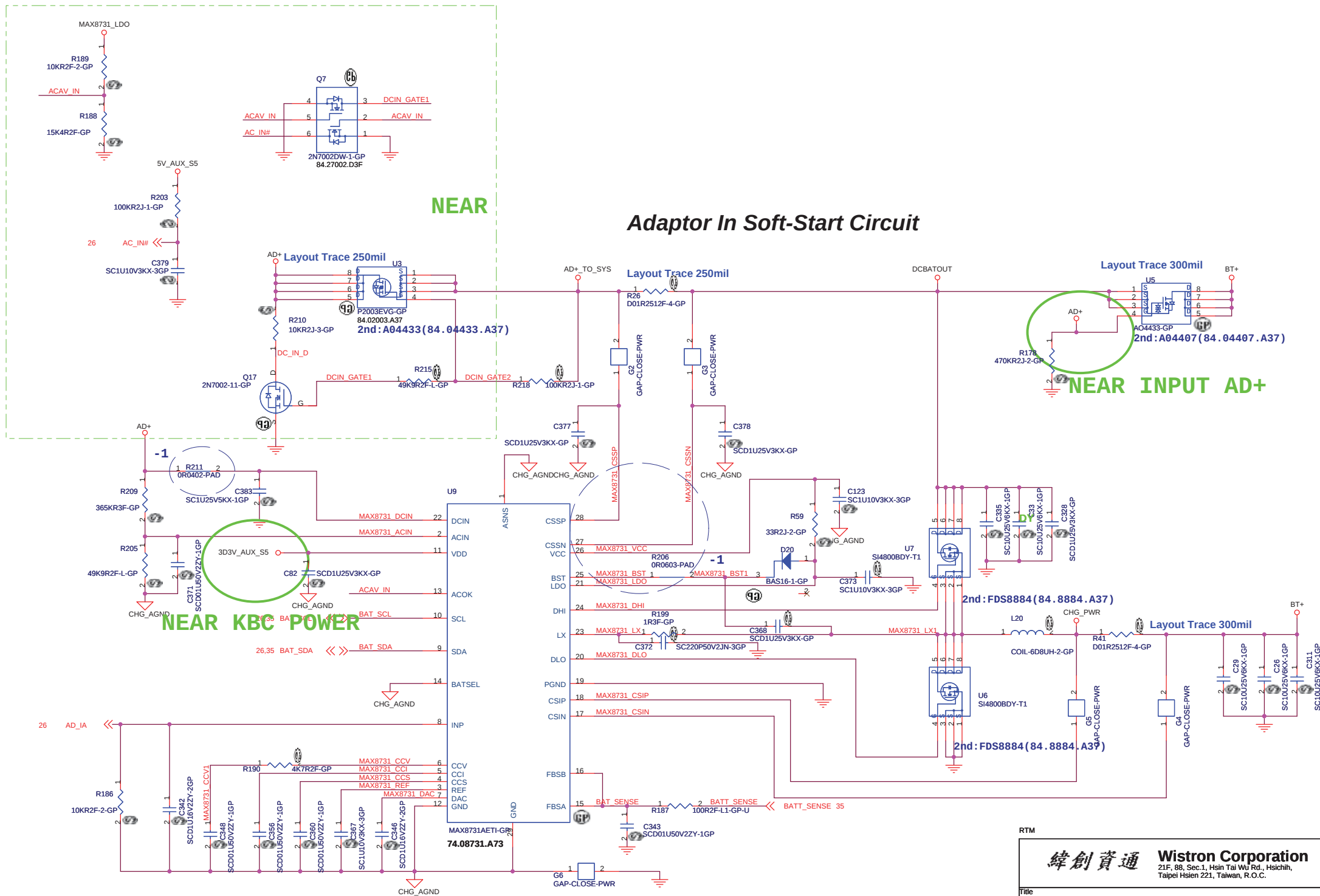


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

RTM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51124 1D8V 1D05V**
Size: A3 Document Number: **Volvi2** Rev: **SA**
Date: Thursday, July 05, 2007 Sheet 32 of 36



RTM

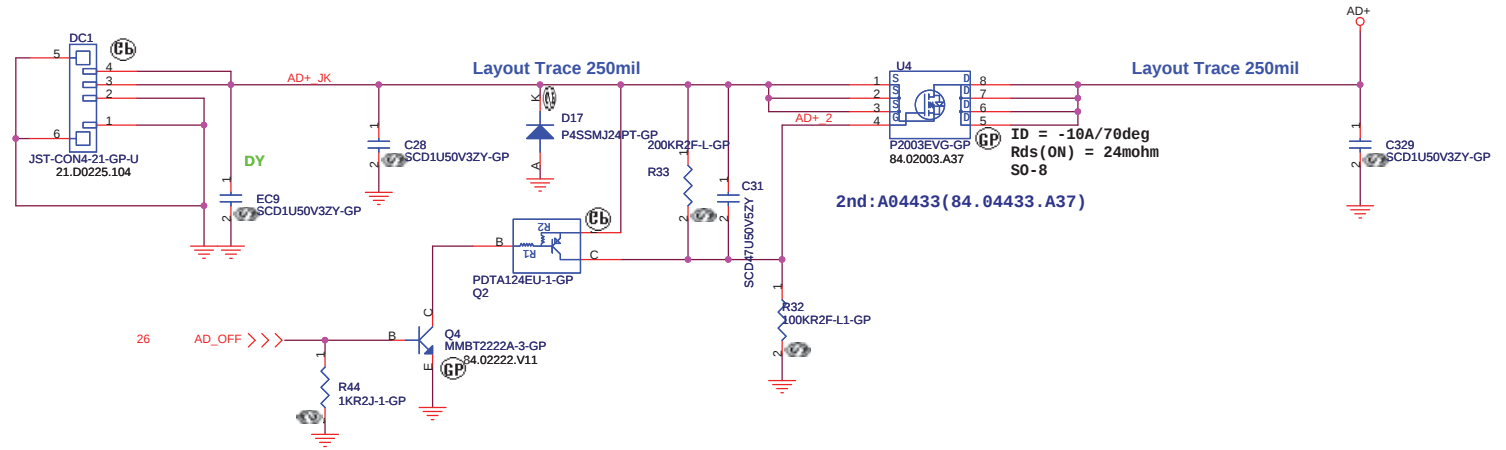
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
CHARGER MAX8731			
Size A3	Document Number		Rev
	Volvi960		SA
Date: Thursday, July 05, 2007		Sheet 34 of 36	

Adaptor in to generate DCBATOUT

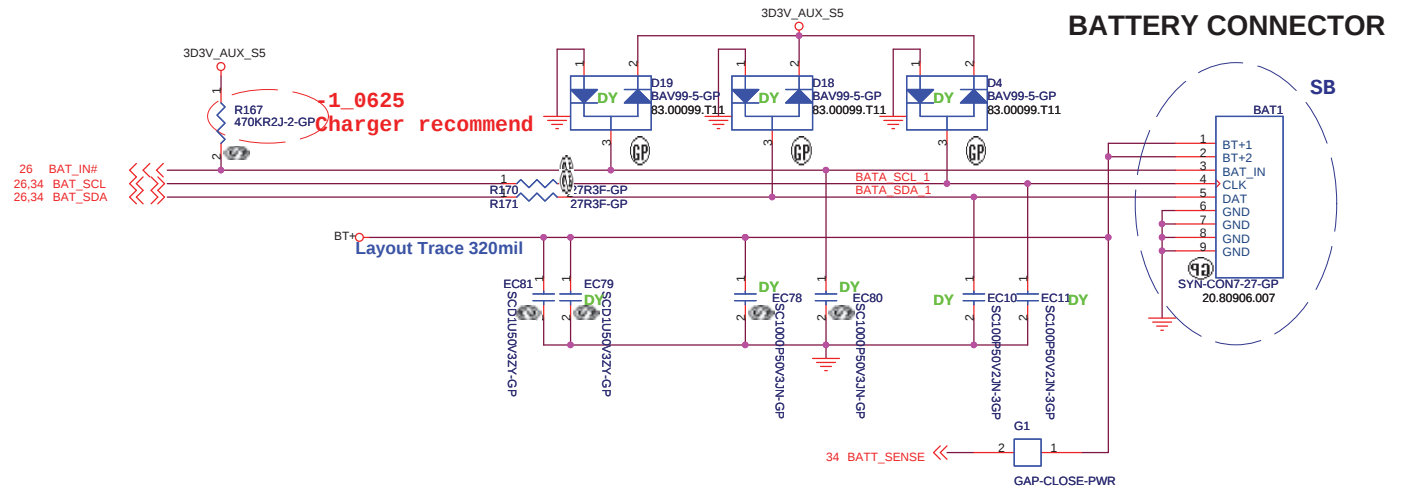
-1 Test Point

AD+ _JK TP167 TPAD30
AD+ _JK TP179 TPAD30



-1 Test Point

BATA_SCL_1 TP168 TPAD30
BATA_SDA_1 TP169 TPAD30
BAT_IN# TP170 TPAD30
BT+ TP171 TPAD30
BT- TP180 TPAD30



RTM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsinchu,
Taippei Hsien 221, Taiwan, R.O.C.

Title		
AD/BATT CONN		
Size	Document Number	Rev
A3	Volvi2	-1
Date:	Thursday, July 05, 2007	Sheet 35 of 36

