ZQA SOLE UMA SYSTEM DIAGRAM

AMD Smarter Choice

Danube Platform
(Main Stream)

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

IV@ -----> iGPU EV@ -----> dGPU
SPE@ -----> Option Notice

DDR3- SODIMM1 PAGE 5 — DDR3 channel A
DDR3- SODIMM2 PAGE 5 — DDR3 channel B

AMD Champlain
S1G4 Processor
35mm X 35mm
638P (PGA) 35W
PAGE 2,3,4

CPU THERMAL SENSOR
(Reserve Only)
PAGE 4

PWM FAN SCH. PAGE 33
CPU (PROCHOT)
E.C. (CPUFAN#)

CPU SideBand TemperatureSense I2C

HT3
1.8GHz

25MHz
32.768KHz

From SB
CLK GEN
SB820M
PAGE 10

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK

CLK_PCI_775
PCLK_DEBUG

NORTH BRIDGE
RS880M GFX Engine: 500MHz
A11
21mm X 21mm, 528pin BGA
TDP: 13W
0.95 ~ 1.1V
PAGE 6,7,8,9

PCI-Express 16X

ATI
Park XT
128-bit M2 Pkg
29mm X 29mm
PAGE 16,17,18,19,20,21

EXT HDMI — **HDMI** PAGE 23
EXT CRT — **CRT** PAGE 22
EXT LVDS — **LVDS** PAGE 22

VRAM DDR3
64MX16X4,64 bit
800MHz PAGE 21

INT HDMI
INT CRT
INT LVDS

PCI-Expresss

P0 — **LAN**
BROADCOM
PCIE-LAN
BCM57780
(10/100/1000)
PAGE 24
25MHz
RJ45 PAGE 25

P2 — **Mini PCI-E Card**
(Wireless LAN)
PAGE 26

A-LINK

SOUTH BRIDGE
SB820M
A12
23mm X 23mm, 605pin BGA
No PCI I/F
TDP: 4.9W
PAGE 10,11,12,13, 14

SATA - HDD PAGE 27 — SATA0 150MB 3 Gb/s
SATA - ODD PAGE 27 — SATA1 150MB 3 Gb/s

P0 — **USB2.0 Port** on board x1 PAGE 31
P9 — **Blue Tooth** PAGE 31
P13 — **Web-Camera** PAGE 22
FFC — **USB BOARD** USB2.0 Ports x3 PAGE 31

P4 — **Mini Card** WLAN & Debug PAGE 20
PCLK_DEBUG

P10 — **CardReader** AU6347 PAGE 30
12MHz

LPC
Azalia

CLK_PCI_775
Winbond KBC NPCE781L PAGE 34
CPU SideBand TemperatureSense I2C

Audio CODEC RTL ALC272X PAGE 28

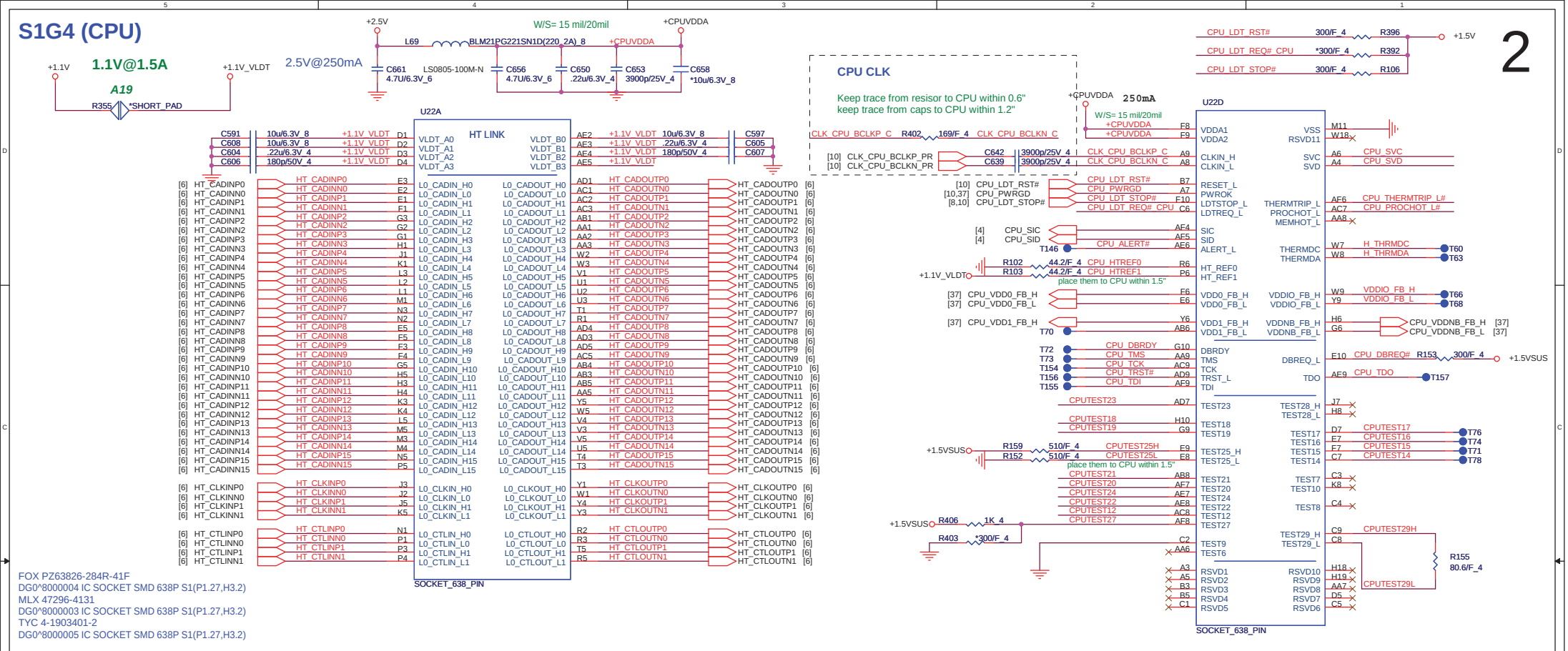
Keyboard TouchPad PAGE 33
SPI ROM PAGE 34
Digital MIC PAGE 28
AUDIO CONN (H.P./ MIC) PAGE 29
Speaker CN PAGE 29

CHARGER (ISL88731A) PAGE 35
AMD CPU CORE (ISL6265) PAGE 37 — *CPU*
NB_CORE (UP6111AQDD) PAGE 39 — *NB*
0.9V/DDR 1.5V(RT8207) PAGE 40
SYSTEM 5V/3V (RT8206) PAGE 36
1.1V(UP6111AQDD) PAGE 38
Discharge /Thermal protec PAGE 44

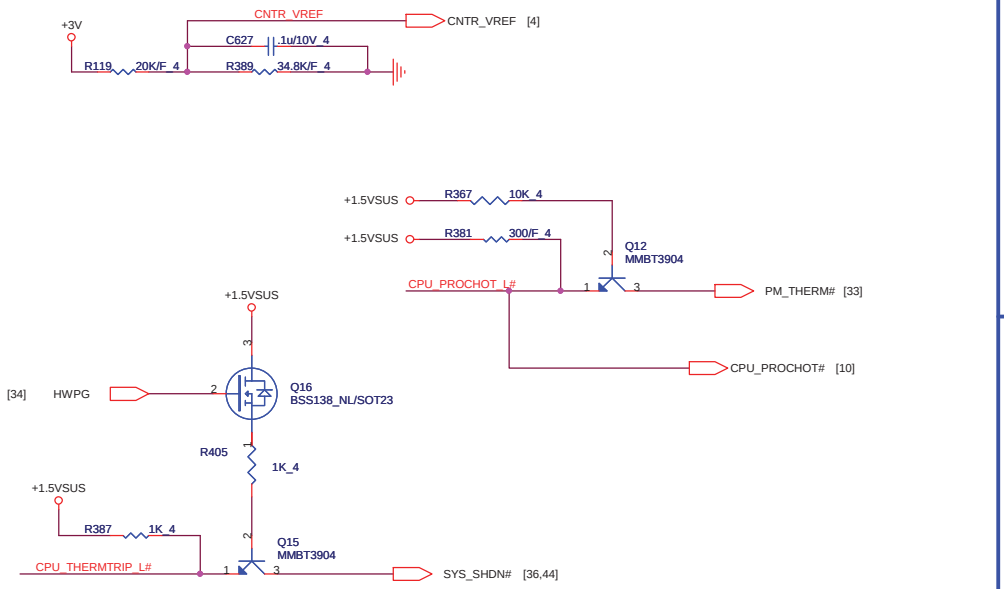
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, May 31, 2010	Sheet 1 of 48	

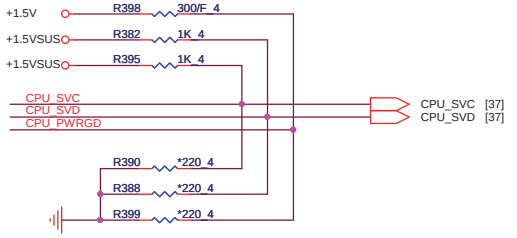
S1G4 (CPU)



FOX PZ63826-284R-41F
DG0^8000004 IC SOCKET SMD 638P S1(P1.27,H3.2)
MLX 47296-4131
DG0^8000003 IC SOCKET SMD 638P S1(P1.27,H3.2)
TYC 4-1903401-2
DG0^8000005 IC SOCKET SMD 638P S1(P1.27,H3.2)



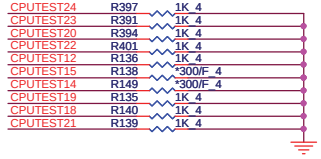
Serial VID



VFIX MODE — VID Override Circuit

SVC	SVD	Voltage Output
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

HDT Connector



PROJECT : ZQA
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Size	Document Number	Rev
	S1G4 HT,CTL I/F 1/3	1A
Date: Monday, May 31, 2010	Sheet 2 of 48	

35W CPU support 0.9V
45W CPU support 1.05V

VDDR=> 0.9V support 1066 / 800 DDR
VDDR= >1.05V support 1333 / 1066 / 800 DDR

VDDR=>1.75A

PLACE THEM CLOSE TO CPU WITHIN 1"

U22B

MEM:CMD/CTRL/CLK

SOCKET_638_PIN

Place close to socket

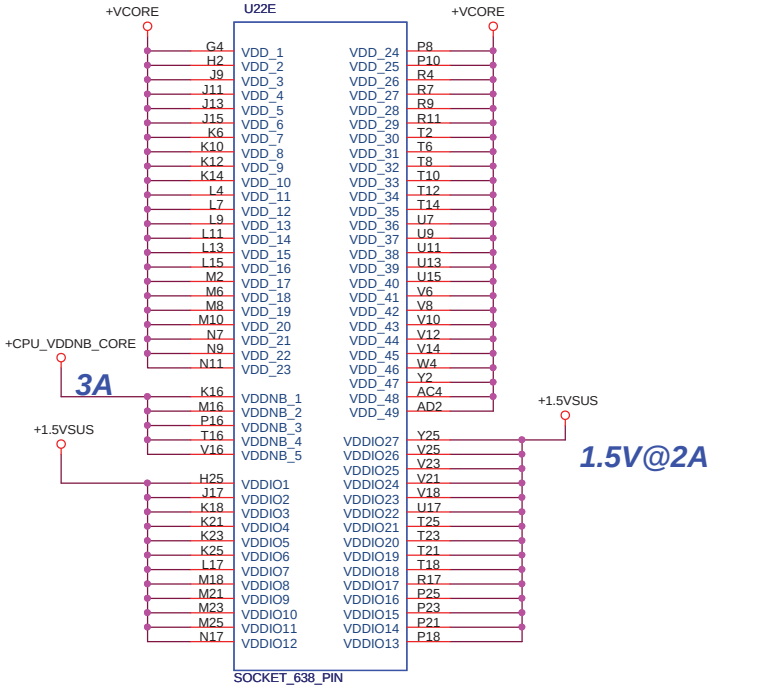
Processor Memory Interface

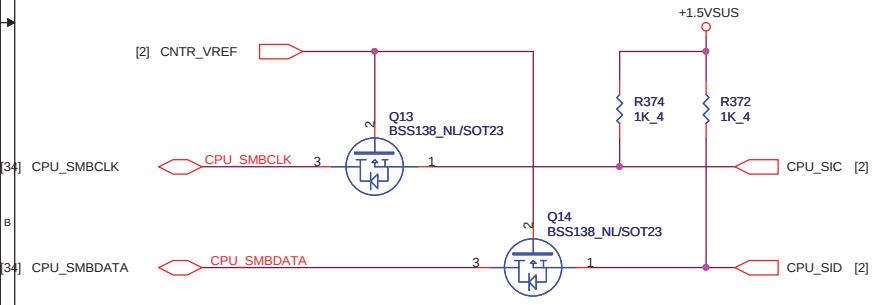
U22C

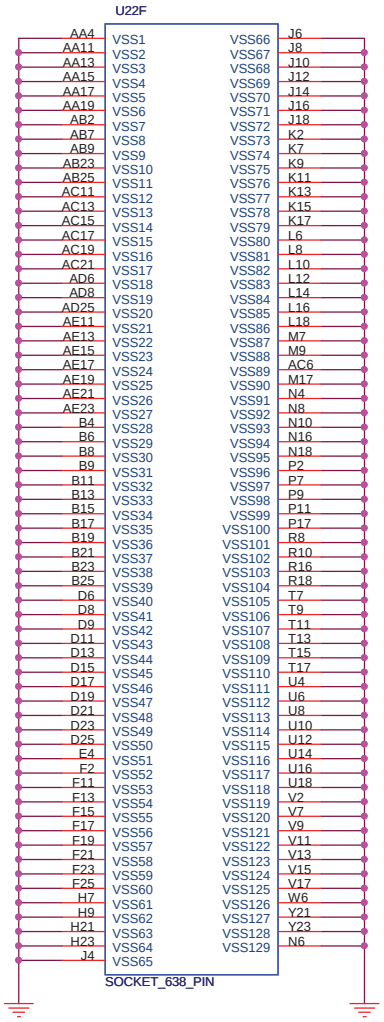
MEM:DATA

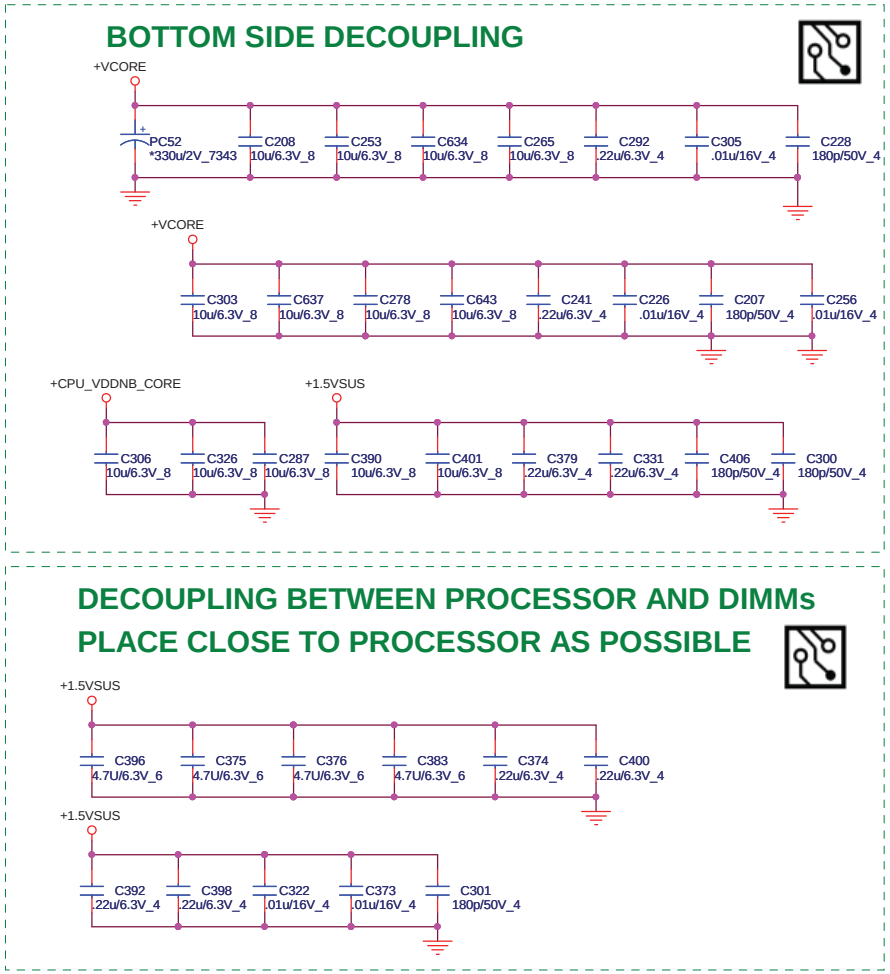
SOCKET_638_PIN

PROJECT : ZQA	
Quanta Computer Inc.	
Size	Document Number: S1G4 DDRIII MEMORY I/F 2/3 — Rev: 1A
Date: Monday, May 31, 2010	Sheet 3 of 48









PROCESSOR POWER AND GROUND

PROJECT : ZQA
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Size	Document Number	Rev
	S1G4 PWR & GND 3/3	1A
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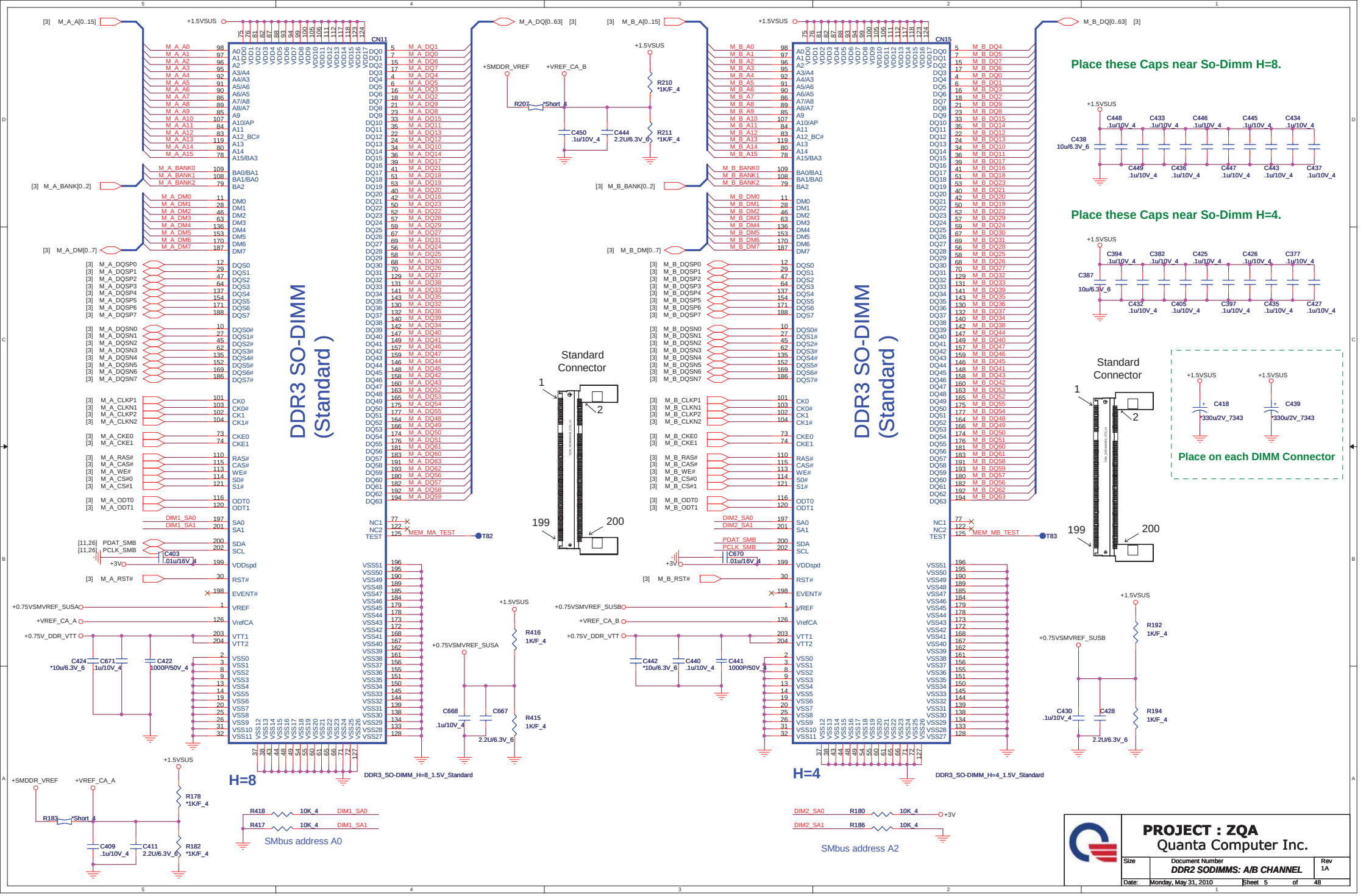
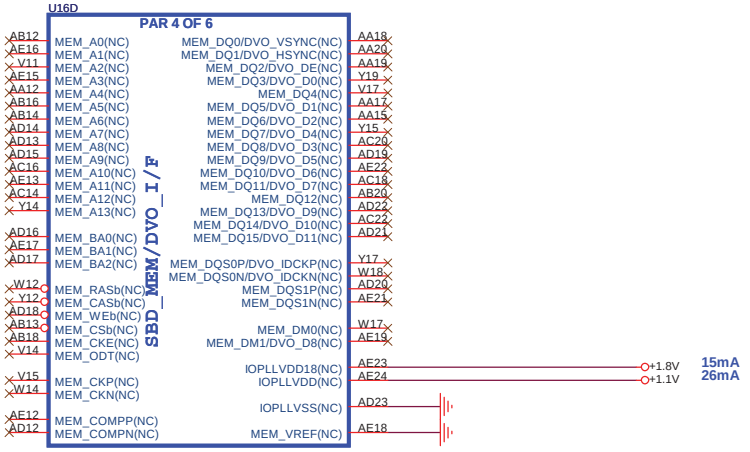

DDR3 SO-DIMM (Standard)
CN11
CN15
H=8
H=4
DDR3_SO-DIMM_H=8_1.5V_Standard
DDR3_SO-DIMM_H=4_1.5V_Standard
Standard Connector
Place these Caps near So-Dimm H=8.
Place these Caps near So-Dimm H=4.
Place on each DIMM Connector
SMbus address A0
SMbus address A2
PROJECT : ZQA
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
Monday, May 31, 2010

Signals	RS880	RX880
HT_TXCALP	Ra 301 ohm 1%	Ra 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	Rb 301 ohm 1%	Rb 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

This block is for Side-Port only



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Size	Document Number	Rev
	RS880M-HT LINK I/F 1/4	1A

Date: Monday, May 31, 2010 Sheet 6 of 48

RS880 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

[15] PEG_RXP[15..0] → PEG_RXP[15..0]
[15] PEG_RXN[15..0] → PEG_RXN[15..0]
[15] PEG_TXP[15..0] → PEG_TXP[15..0]
[15] PEG_TXN[15..0] → PEG_TXN[15..0]

U16B

PART 2 OF 6

PCIE I/F GFX

PEG_RXP15	D4	GFX_RX0P	GFX_TX0P	A5	PEG_TXP15_C	C568	EV@.1u/10V_4	PEG_TXP15
PEG_RXN15	C4	GFX_RX0N	GFX_TX0N	B5	PEG_TXN15_C	C570	EV@.1u/10V_4	PEG_TXN15
PEG_RXP14	A3	GFX_RX1P	GFX_TX1P	A4	PEG_TXP14_C	C561	EV@.1u/10V_4	PEG_TXP14
PEG_RXN14	B3	GFX_RX1N	GFX_TX1N	B4	PEG_TXN14_C	C562	EV@.1u/10V_4	PEG_TXN14
PEG_RXP13	C2	GFX_RX2P	GFX_TX2P	C3	PEG_TXP13_C	C557	EV@.1u/10V_4	PEG_TXP13
PEG_RXN13	C1	GFX_RX2N	GFX_TX2N	B2	PEG_TXN13_C	C559	EV@.1u/10V_4	PEG_TXN13
PEG_RXP12	E5	GFX_RX3P	GFX_TX3P	D1	PEG_TXP12_C	C553	EV@.1u/10V_4	PEG_TXP12
PEG_RXN12	F5	GFX_RX3N	GFX_TX3N	D2	PEG_TXN12_C	C556	EV@.1u/10V_4	PEG_TXN12
PEG_RXP11	G5	GFX_RX4P	GFX_TX4P	E2	PEG_TXP11_C	C549	EV@.1u/10V_4	PEG_TXP11
PEG_RXN11	G6	GFX_RX4N	GFX_TX4N	E1	PEG_TXN11_C	C552	EV@.1u/10V_4	PEG_TXN11
PEG_RXP10	H5	GFX_RX5P	GFX_TX5P	F4	PEG_TXP10_C	C541	EV@.1u/10V_4	PEG_TXP10
PEG_RXN10	H6	GFX_RX5N	GFX_TX5N	F3	PEG_TXN10_C	C548	EV@.1u/10V_4	PEG_TXN10
PEG_RXP9	J6	GFX_RX6P	GFX_TX6P	F1	PEG_TXP9_C	C537	EV@.1u/10V_4	PEG_TXP9
PEG_RXN9	J5	GFX_RX6N	GFX_TX6N	F2	PEG_TXN9_C	C540	EV@.1u/10V_4	PEG_TXN9
PEG_RXP8	J7	GFX_RX7P	GFX_TX7P	H4	PEG_TXP8_C	C527	EV@.1u/10V_4	PEG_TXP8
PEG_RXN8	J8	GFX_RX7N	GFX_TX7N	H3	PEG_TXN8_C	C536	EV@.1u/10V_4	PEG_TXN8
PEG_RXP7	L5	GFX_RX8P	GFX_TX8P	H1	PEG_TXP7_C	C535	EV@.1u/10V_4	PEG_TXP7
PEG_RXN7	L6	GFX_RX8N	GFX_TX8N	H2	PEG_TXN7_C	C539	EV@.1u/10V_4	PEG_TXN7
PEG_RXP6	M8	GFX_RX9P	GFX_TX9P	J2	PEG_TXP6_C	C518	EV@.1u/10V_4	PEG_TXP6
PEG_RXN6	L8	GFX_RX9N	GFX_TX9N	J1	PEG_TXN6_C	C525	EV@.1u/10V_4	PEG_TXN6
PEG_RXP5	P7	GFX_RX10P	GFX_TX10P	K4	PEG_TXP5_C	C523	EV@.1u/10V_4	PEG_TXP5
PEG_RXN5	M7	GFX_RX10N	GFX_TX10N	K3	PEG_TXN5_C	C526	EV@.1u/10V_4	PEG_TXN5
PEG_RXP4	P5	GFX_RX11P	GFX_TX11P	K1	PEG_TXP4_C	C530	EV@.1u/10V_4	PEG_TXP4
PEG_RXN4	M5	GFX_RX11N	GFX_TX11N	K2	PEG_TXN4_C	C529	EV@.1u/10V_4	PEG_TXN4
PEG_RXP3	R8	GFX_RX12P	GFX_TX12P	M4	PEG_TXP3_C	C522	EV@.1u/10V_4	PEG_TXP3
PEG_RXN3	P8	GFX_RX12N	GFX_TX12N	M3	PEG_TXN3_C	C521	EV@.1u/10V_4	PEG_TXN3
PEG_RXP2	R6	GFX_RX13P	GFX_TX13P	M1	PEG_TXP2_C	C532	EV@.1u/10V_4	PEG_TXP2
PEG_RXN2	R5	GFX_RX13N	GFX_TX13N	M2	PEG_TXN2_C	C531	EV@.1u/10V_4	PEG_TXN2
PEG_RXP1	P4	GFX_RX14P	GFX_TX14P	N2	PEG_TXP1_C	C520	EV@.1u/10V_4	PEG_TXP1
PEG_RXN1	P3	GFX_RX14N	GFX_TX14N	N1	PEG_TXN1_C	C519	EV@.1u/10V_4	PEG_TXN1
PEG_RXP0	T4	GFX_RX15P	GFX_TX15P	P1	PEG_TXP0_C	C534	EV@.1u/10V_4	PEG_TXP0
PEG_RXN0	T3	GFX_RX15N	GFX_TX15N	P2	PEG_TXN0_C	C533	EV@.1u/10V_4	PEG_TXN0

PCIE I/F GPP

[24] PCIE_RX1+	AE3	GPP_RX0P	GPP_TX0P	AC1	PCIE_TXP0_C	C546	.1u/10V_4	PCIE_TX1+ [24]
[24] PCIE_RX1-	AD4	GPP_RX0N	GPP_TX0N	AC2	PCIE_TXN0_C	C545	.1u/10V_4	PCIE_TX1- [24]
	AE2	GPP_RX1P	GPP_TX1P	AB4				
	AD3	GPP_RX1N	GPP_TX1N	AB3				
[26] PCIE_RXP2	AD1	GPP_RX2P	GPP_TX2P	AA2	PCIE_TXP2_C	C543	.1u/10V_4	PCIE_TXP2 [26]
[26] PCIE_RXN2	AD2	GPP_RX2N	GPP_TX2N	AA1	PCIE_TXN2_C	C544	.1u/10V_4	PCIE_TXN2 [26]
	V5	GPP_RX3P	GPP_TX3P	Y1				
	W6	GPP_RX3N	GPP_TX3N	Y2				
T33	U5	GPP_RX4P	GPP_TX4P	Y4	T32			
T34	U6	GPP_RX4N	GPP_TX4N	Y3	T96			
	U8	GPP_RX5P	GPP_TX5P	V1				
	U7	GPP_RX5N	GPP_TX5N	V2				

PCIE I/F SB

[10] A_RXP0	AA8	SB_RX0P	SB_TX0P	AD7	A_TXP0_C	C573	.1u/10V_4	A_TXP0 [10]
[10] A_RXN0	Y8	SB_RX0N	SB_TX0N	AE7	A_TXN0_C	C569	.1u/10V_4	A_TXN0 [10]
[10] A_RXP1	AA7	SB_RX1P	SB_TX1P	AE6	A_TXP1_C	C560	.1u/10V_4	A_TXP1 [10]
[10] A_RXN1	Y7	SB_RX1N	SB_TX1N	AD6	A_TXN1_C	C563	.1u/10V_4	A_TXN1 [10]
[10] A_RXP2	AA5	SB_RX2P	SB_TX2P	AB6	A_TXP2_C	C555	.1u/10V_4	A_TXP2 [10]
[10] A_RXN2	AA6	SB_RX2N	SB_TX2N	AC6	A_TXN2_C	C558	.1u/10V_4	A_TXN2 [10]
[10] A_RXP3	W5	SB_RX3P	SB_TX3P	AD5	A_TXP3_C	C547	.1u/10V_4	A_TXP3 [10]
[10] A_RXN3	Y5	SB_RX3N	SB_TX3N	AE5	A_TXN3_C	C551	.1u/10V_4	A_TXN3 [10]

PCE_CALRP(PCE_BCALRP)
PCE_CALRN(PCE_BCALRN)

AC8 NB_PCIECALRP R326 1.27K/F_4
AB8 NB_PCIECALRN R330 2K/F_4
+1.1V

RS880/RX881

LAN

WLAN

SB

INT HDMI

PEG_TXP15_C	C76	IV@.1u/10V_4	IV_TX2_HDMI+ [23]
PEG_TXN15_C	C78	IV@.1u/10V_4	IV_TX2_HDMI- [23]
PEG_TXP14_C	C73	IV@.1u/10V_4	IV_TX1_HDMI+ [23]
PEG_TXN14_C	C75	IV@.1u/10V_4	IV_TX1_HDMI- [23]
PEG_TXP13_C	C68	IV@.1u/10V_4	IV_TX0_HDMI+ [23]
PEG_TXN13_C	C71	IV@.1u/10V_4	IV_TX0_HDMI- [23]
PEG_TXP12_C	C64	IV@.1u/10V_4	IV_TXC_HDMI+ [23]
PEG_TXN12_C	C67	IV@.1u/10V_4	IV_TXC_HDMI- [23]

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-PCIE I/F 2/4	1A
Date: Monday, May 31, 2010	Sheet 7 of 48	

For Check list JTAG

R325 *4.7K_4 NB_PWRGD_IN
+3V R59 *4.7K_4 INT_EDIDDATA
R60 *4.7K_4 INT_EDIDCLK
+3V R58 *4.7K_4 IV_HDMI_DDC_DATA

For A11 version

(02/10) Don't need 49.9 ohm PD.

R53 *49.9/F_4 CLK_SBLINKP
R55 *49.9/F_4 CLK_SBLINKN

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

RS880M	
1 Disable	V
0 Enable	

INT_CRT_VSYNC R64 3K_4 +3V

RS880M: Enables Side port memory

RS880M:INT_CRT_HSYNC

Selects if Memory SIDE PORT is available or not

1 = Memory Side port Not available

0 = Memory Side port available

Register Readback of strap: NB_CLKCFG:CLK_TOP_SPARE_D[1]

INT_CRT_HSYNC R66 3K_4 +3V

For extrnal EEPROM Debug only

RS780/RX780/RS880

+NB_CORE_ON R328 2K/F_4

Display Port interface from PCIeGraphics (RS880/rs880M only)

RS880_AUX_CAL R57 *150/F_4

VGA

[22] INT_CRT_RED R74 IV@140/F_4
[22] INT_CRT_GRE R77 IV@150/F_4
[22] INT_CRT_BLU R79 IV@150/F_4
[22] INT_CRT_HSYNC
[22] INT_CRT_VSYNC
[22] INT_DDCDATA
[22] INT_DDCCLK
R80 715/F_4

DDC_DATA & DDC_CLK Not applicable to RX881

[11,14] NB_PWRGD_IN R21 300/F_4 [10,34] A_RST#_SB
[10] CLK_NB_HTREFP_PR
[10] CLK_NB_HTREFN_PR
[10] CLK_NB_REF_CLKP
[10] CLK_NB_REF_CLKN
R48 4.7K_4
R47 4.7K_4
T97 T95
[10] CLK_SBLINKP
[10] CLK_SBLINKN
[22] INT_EDIDDATA
[22] INT_EDIDCLK
[23] IV_HDMI_DDC_DATA
[23] IV_HDMI_DDC_CLK
[39] +NB_CORE_ON
T35

U16C — RS880/RX881 — PART 3 OF 6

AVDD1(NC)	F12		
AVDD2(NC)	E12	110mA	+3V_AVDD_NB
AVDDDI(NC)	F14	20mA	+1.8V_AVDDDI_NB
AVSSDI(NC)	G15	4mA	+1.8V_AVDDQ_NB
AVDDQ(NC)	H15		
AVSSQ(NC)	H14		
C_Pr(DFT_GPIO5)	E17		
Y(DFT_GPIO2)	F17		
COMP_Pb(DFT_GPIO4)	F15		
RED(DFT_GPIO0)	G18		
REDb(NC)	G17		
GREEN(DFT_GPIO1)	E18		
GREENb(NC)	F18		
BLUE(DFT_GPIO3)	E19		
BLUEb(NC)	F19		
DAC_HSYNC(PWM_GPIO4)	A11		
DAC_VSYNC(PWM_GPIO6)	B11		
DAC_SDA(PCE_TCALRN)	E8		
DAC_SCL(PCE_RCALRN)	F8		
DAC_RSET(PWM_GPIO1)	G14		
PLLVDD(NC)	A12		+1.1V_PLLVDD
PLLVDD18(NC)	D14		+1.8V_PLLVDD18
PLLVSS(NC)	B12		
VDDA18HTPLL	H17	20mA	+1.8V_VDDA18HTPLL
VDDA18PCIEPLL1	D7	120mA	+1.8V_VDDA18PCIEPLL
VDDA18PCIEPLL2	E7		
SYSRESETb	D8		
POWERGOOD	A10		
LDTSTOPb	C10		NB_LDT_STOP#
ALLOW_LDTSTOP	C12		NB_ALLOW_LDTSTOP
HT_REFCLKP	C25		
HT_REFCLKN	C24		
REFCLK_P/OSCIN(OSCIN)	E11		CLK_NB_REF_CLKP
REFCLK_N(PWM_GPIO3)	F11		CLK_NB_REF_CLKN
GFX_REFCLKP	T2		NBGFX_CLKP
GFX_REFCLKN	T1		NBGFX_CLKN
GPP_REFCLKP	U1		GPP_REFCLKP
GPP_REFCLKN	U2		GPP_REFCLKN
GPPSB_REFCLKP(SB_REFCLKP)	V4		
GPPSB_REFCLKN(SB_REFCLKN)	V3		
I2C_DATA	A9		
I2C_CLK	B9		IV_HDMI_DDC_DATA
DDC_DATA/AUX0N(NC)	B8		
DDC_CLK/AUX0P(NC)	A8		
AUX1P(NC)	B7		
AUX1N(NC)	A7		
STRP_DATA	B10		+NB_CORE_ON
RSVD	G11		
AUX_CAL(NC)	C8		RS880_AUX_CAL

CRT/TVOUT: TXOUT_L0P(NC) A22, TXOUT_L0N(NC) B22, TXOUT_L1P(NC) A21, TXOUT_L1N(NC) B21, TXOUT_L2P(NC) B20, TXOUT_L2N(DBG_GPIO0) A20, TXOUT_L3P(NC) A19, TXOUT_L3N(DBG_GPIO2) B19, TXOUT_U0P(NC) B18, TXOUT_U0N(NC) A18, TXOUT_U1P(PCIE_RESET_GPIO3) A17, TXOUT_U1N(PCIE_RESET_GPIO2) B17, TXOUT_U2P(NC) D20, TXOUT_U2N(NC) D21, TXOUT_U3P(PCIE_RESET_GPIO5) D18, TXOUT_U3N(NC) D19

LVTM: TXCLK_LP(DBG_GPIO1) B16, TXCLK_LN(DBG_GPIO3) A16, TXCLK_UP(PCIE_RESET_GPIO4) D16, TXCLK_UN(PCIE_RESET_GPIO1) D17

PLL PWR: VDDLTP18(NC) A13, VSSLTP18(NC) B13, VDDLT18_1(NC) A15, VDDLT18_2(NC) B15, VDDLT33_1(NC) A14, VDDLT33_2(NC) B14

PM: VSSLT1(VSS) C14, VSSLT2(VSS) D15, VSSLT3(VSS) C16, VSSLT4(VSS) C18, VSSLT5(VSS) C20, VSSLT6(VSS) E20, VSSLT7(VSS) C22

MIS.: TMDS_HPD(NC) D9, HPD(NC) D10, TVCLKIN(PWM_GPIO5) D12, THERMALDIODE_P AE8, THERMALDIODE_N AD8, TESTMODE D13

LA_DATAP0 [22], LA_DATAN0 [22], LA_DATAP1 [22], LA_DATAN1 [22], LA_DATAP2 [22], LA_DATAN2 [22]
LA_CLK [22], LA_CLK# [22]
+1.8V_VDDLTP18_NB 15mA
+1.8V_VDDLT_18_NB 300mA
LVDS_DIGON(PCE_TCALRP) E9, LVDS_BLON(PCE_RCALRP) F7, LVDS_ENA_BL(PWM_GPIO2) G12
INT_LVDS_DIGON [22], INT_DPST_PWM [22], INT_LVDS_BLON [22]
INT_HDMI_HPD [23]
SUS_STAT#_NB R324 *Short_4 SUS_STAT# [11]
R329 *3K_4
TEST_EN R68 1.8K/F_4

Made provision for external pull-down which is not installed by default. Pulled up externally for bypassing EEPROM strapping and using default values.

RS880M --- ADD

+3V L23 BLM18PG221SN1D(220_1.4A)_6 +3V_AVDD_NB
solve CRTflicker C118 22u/6.3V_8 C88 2.2U/6.3V_6
AVDD-DAC Analog not applicable to RX780

+1.1V L56 BLM18PG221SN1D(220_1.4A)_6 +1.1V_PLLVDD
C576 2.2U/6.3V_6
PLLVDD - Graphics PLL not applicable to RX780

+1.8V L19 BLM18PG221SN1D(220_1.4A)_6 +1.8V_VDDLTP18_NB
C91 2.2U/6.3V_6
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780

L57 BLM21PG221SN1D(220_2A)_8 +1.8V_VDDLT_18_NB
C578 4.7U/6.3V_6 C577 .1u/10V_4
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780

+1.8V +1.8V_AVDDDI_NB
C105 .1u/10V_4
AVDDI-DAC Digital not applicable to RX780

L21 BLM18PG221SN1D(220_1.4A)_6 +1.8V_AVDDQ_NB
C100 2.2U/6.3V_6
AVDDQ-DAC Bandgap Reference not applicable to RX780

+1.8V L20 BLM18PG221SN1D(220_1.4A)_6 +1.8V_PLLVDD18
C113 10u/6.3V_8 C93 4.7U/6.3V_6
PLLVDD18 - Graphics PLL not applicable to RX780

+1.8V VDDA18PCIEPLL -PCIE PLL 20mils width
L18 BLM18PG221SN1D(220_1.4A)_6 +1.8V_VDDA18PCIEPLL
C104 2.2U/6.3V_6

VDDA18HTPLL -HT LINK PLL 20mils width
L22 BLM18PG221SN1D(220_1.4A)_6 +1.8V_VDDA18HTPLL
C112 2.2U/6.3V_6

+1.8V 9/16 need modify PN R323 2.2K_4
DDR3 based CPU : Level shifted to 1.8 V on the Northbridge side using an open-drain buffer and pulled up to 1.8V_S0 through a 2.2k Ohm 5% resistor on the Northbridge side.

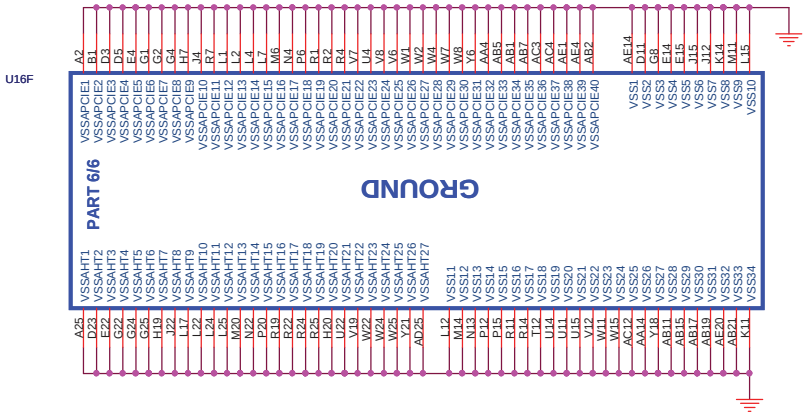
[2,10] CPU_LDT_STOP# U15 Open Drain 74LVC07 NB_LDT_STOP#

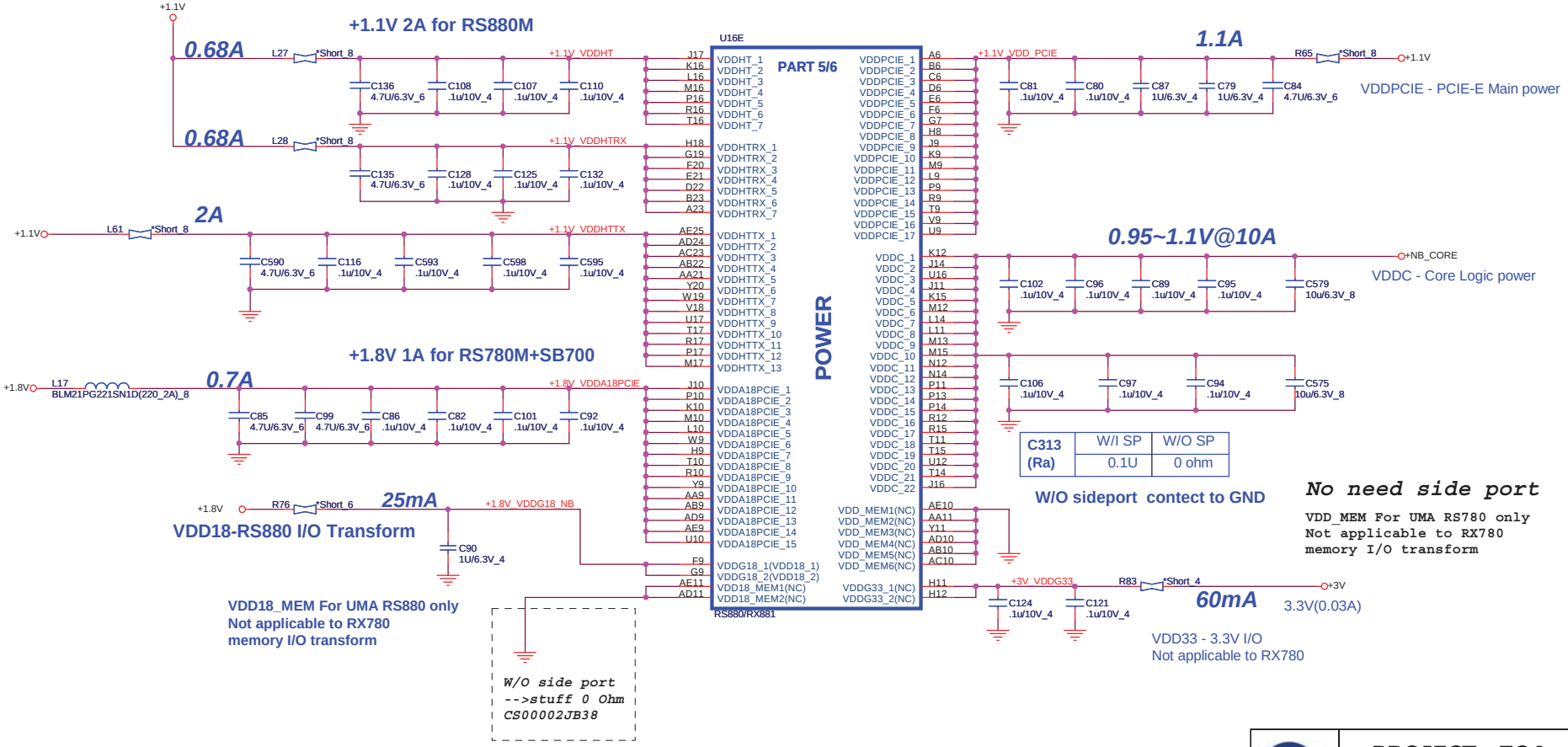
[10] ALLOW_LDTSTOP R331 *Short_4 NB_ALLOW_LDTSTOP R332 1K_4 +1.8V

The RS880 family does not support CLMC architecture
The LDTREQ# connection from the CPU to ALLOW_LDTSTOP of the Northbridge is no longer required.

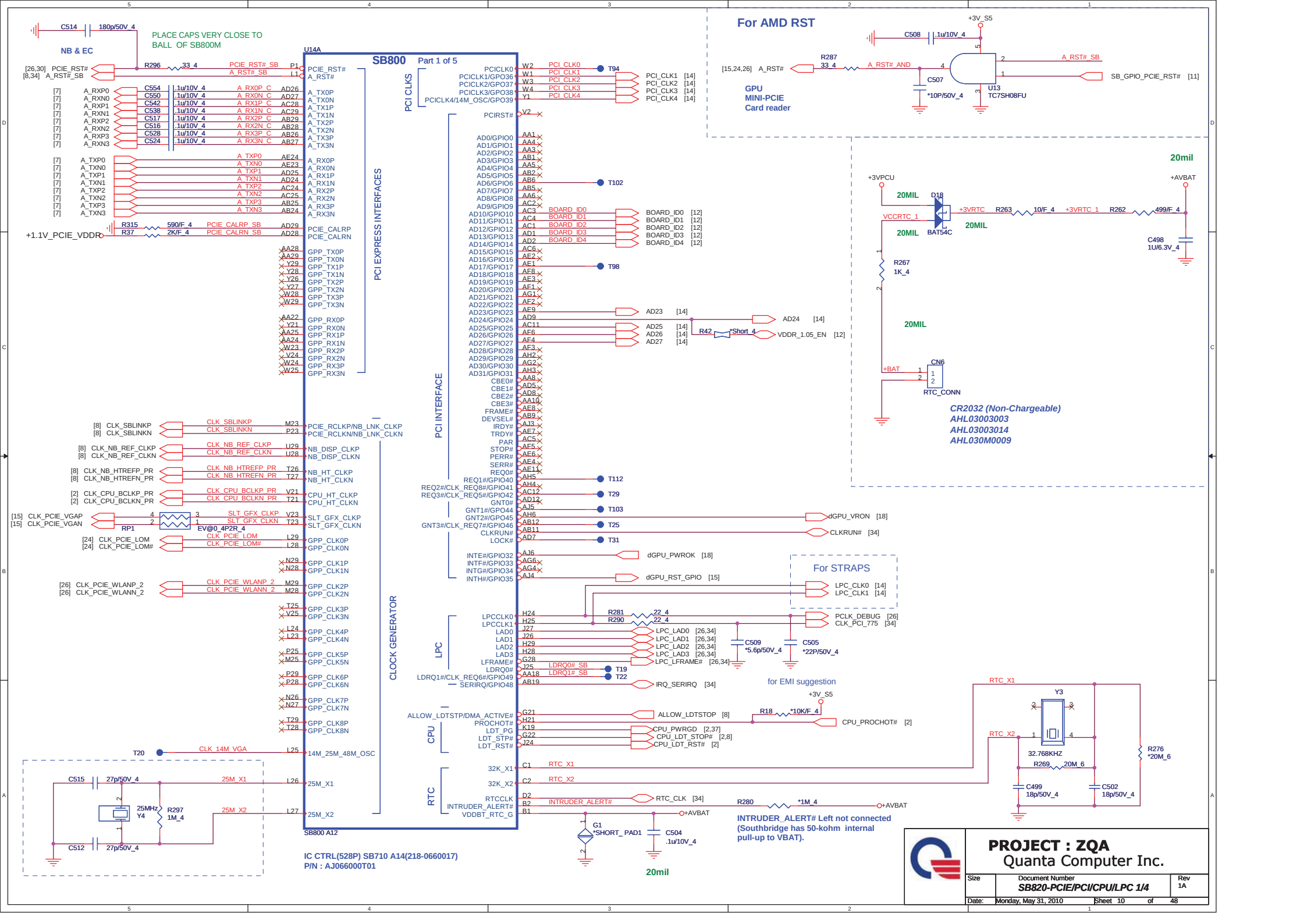
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	RS880M-SYSTEM I/F 3/4	1A
Date: Monday, May 31, 2010	Sheet 8 of 48	





PROJECT : ZQA Quanta Computer Inc.			
Size	Document Number RS880M-POWER4/4		Rev 1A
Date: Monday, May 31, 2010	Sheet 9 of 48		


For AMD RST
GPU
MINI-PCIE
Card reader
U13
TC7SH08FU
20mil
CR2032 (Non-Chargeable)
AHL03003003
AHL03003014
AHL030M0009
RTC_CONN
NB & EC
PLACE CAPS VERY CLOSE TO
BALL OF SB800M
U14A
SB800
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACES
PCI INTERFACE
CLOCK GENERATOR
LPC
CPU
RTC
For STRAPS
for EMI suggestion
INTRUDER_ALERT# Left not connected
(Southbridge has 50-kohm internal
pull-up to VBAT).
IC CTRL(528P) SB710 A14(218-0660017)
P/N : AJ066000T01
SB800 A12
PROJECT : ZQA
Quanta Computer Inc.
SB820-PCIE/PCI/CPU/LPC 1/4
Monday, May 31, 2010

NC only ,Can't be install

+3V_S5
R271 *2.2K_4 SB_TEST0
R32 *2.2K_4 SB_TEST1
R28 *2.2K_4 SB_TEST2

SCL0/SDATA0 is 3V tolerance. AMD datasheet define it
Clk Gen/ Robson/ TV tuner/ DDR2/ Thermal/ Accelerometer

+3V
R49 2.2K_4 PCLK_SMB
R51 2.2K_4 PDAT_SMB

SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

+3V_S5
R26 10K_4 SB_SMBCLK1
R25 10K_4 SB_SMBDATA1

SCL2/SDATA2 is 3V/S5 tolerance.
AMD datasheet define it

+3V_S5
R23 10K_4 SB_SCLK2
R22 10K_4 SB_SDATA2

+3V
R31 4.7K_4 SUS_STAT#

+3V
R54 8.2K_4 CLK_PCIE_LAN_REQ#
R56 8.2K_4 CLK_PCIE_2_REQ#

To Azalia

ACZ_SDOUT R294 33_4 ACZ_SDOUT_AUDIO [28]
C511 *10P/50V_4
ACZ_SYNC R295 33_4 ACZ_SYNC_AUDIO [28]
C513 *10P/50V_4
ACZ_BCLK R291 33_4 ACZ_BITCLK_AUDIO [28]
C510 *10P/50V_4
ACZ_RST# R298 33_4 ACZ_RST#_AUDIO [28]
ACZ_SDIN0 ACZ_SDIN0 [28]

USBCLK/41M_25M_48M_OSC pin is CLK input pin when EXT CLKGEN mode.
It is output CLK source when INT CLKGEN mode.

U14D

SB800
Part 4 of 5

T12 SB_PCI_PME# J2 PCI_PME#/GEVENT4#
K1 R#/GEVENT22#
D3 SPI_CS3#/GBE_STAT1/GEVENT21#
[34] SUSB# E1 SLP_S3#
[34] SUSC# SUSC# H1 SLP_S5#
[34] DNBSWON# F2 PWR_BTN#
[14] SB_PWRGD_IN H5 PWR_GOOD
[8] SUS_STAT# G6 SUS_STAT#
SB_TEST0 B3 TEST0
SB_TEST1 C4 TEST1/TMS
SB_TEST2 F6 TEST2
[34] SIO_A20GATE AD21 GA20IN/GEVENT0#
[34] SIO_RCIN# SIO_RCIN# AE21 KBRST#/GEVENT1#
LANLINK_STATE# K2 LPC_PME#/GEVENT3#
T92 J29 LPC_SMI#/GEVENT23#
[34] SIO_EXT_SMI# H2 GEVENT5#
[34] SIO_EXT_SCI# SYS_RST# J1 SYS_RESET#/GEVENT19#
T91 H6 WAKE#/GEVENT8#
[24] PCIE_WAKE# IR_RX1 E3 IR_RX1/GEVENT20#
T89 SB_THERMTRIP# J6 THRMTRIP#/SMBALERT#/GEVENT2#
T21 AC19 NB_PWRGD
[8,14] NB_PWRGD_IN
[34] ICH_RSMRST# G1 RSMRST#

ACPI / WAKE UP EVENTS

AD19 CLK_REQ4#/SATA_IS0#/GPIO64
AA16 CLK_REQ3#/SATA_IS1#/GPIO63
[10] SB_GPIO_PCIE_RST# SB_GPIO_PCIE_RST# AB21 SMARTVOLT1/SATA_IS2#/GPIO50
[24] CLK_PCIE_LAN_REQ# CLK_PCIE_LAN_REQ# AC18 CLK_REQ0#/SATA_IS3#/GPIO60
[18] dGPU_PWR_EN AE20 SATA_IS4#/FANOUT3/GPIO55
T30 SB_GPIO59 AE19 SATA_IS5#/FANIN3/GPIO59
[28] SPKR AF19 SPKR/GPIO66
[5,26] PCLK_SMB PCLK_SMB AD22 SCL0/GPIO43
[5,26] PDAT_SMB PDAT_SMB AE22 SDA0/GPIO47
SB_SMBCLK1 F5 SCL1/GPIO227
SB_SMBDATA1 F4 SDA1/GPIO228
[26] CLK_PCIE_2_REQ# AH21 CLK_REQ2#/FANIN4/GPIO62
AB18 CLK_REQ1#/FANOUT4/GPIO61
E1 IR_LED#/LLB#/GPIO184
AJ21 SMARTVOLT2/SHUTDOWN#/GPIO51
T93 H4 DDR3_RST#/GEVENT7#
D5 GBE_LED0/GPIO183
D7 GBE_LED1/GEVENT9#
G5 GBE_LED2/GEVENT10#
K3 GBE_STAT0/GEVENT11#
T28 E_SB_OSC AA20 CLK_REQG#/GPIO65/OSCIN

GPIO

[31] OC_7# H3 BLINK/USB_OC7#/GEVENT18#
[31] OC_6# D1 USB_OC6#/IR_TX1/GEVENT6#
SB_PM_THERM# E4 USB_OC5#/IR_TX0/GEVENT17#
T3 D4 USB_OC4#/IR_RX0/GEVENT16#
T8 OC_4# E8 USB_OC3#/AC_PRES/TDO/GEVENT15#
T1 SB_JTAG_TDO F7 USB_OC2#/TCK/GEVENT14#
T10 SB_JTAG_TCK E7 USB_OC1#/TDI/GEVENT13#
T7 SB_JTAG_TDI F8 USB_OC0#/TRST#/GEVENT12#
T11 SB_JTAG_RST#

USB OC

Eliot (02/26)
Current Agesa bios doesn't program ALERT_L and SB won't process alert.

HD audio interface is +3VS5 voltage

ACZ_BCLK M3 AZ_BITCLK
[14] ACZ_SDOUT ACZ_SDOUT N1 AZ_SDOUT
ACZ_SDIN0 L2 AZ_SDIN0/GPIO167
M2 AZ_SDIN1/GPIO168
M1 AZ_SDIN2/GPIO169
M4 AZ_SDIN3/GPIO170
ACZ_SYNC N2 AZ_SYNC
ACZ_RST# P2 AZ_RST#

HD AUDIO

+3V_S5
R299 10K_4 GBE_COL T1 GBE_COL
R300 10K_4 GBE_CRS T4 GBE_CRS
R33 10K_4 GBE_MDIO L6 GBE_MDCK
L5 GBE_MDIO
T9 GBE_RXCLK
U1 GBE_RXD3
U3 GBE_RXD2
T2 GBE_RXD1
U2 GBE_RXD0
R301 10K_4 GBE_RXERR T5 GBE_RXCTL/RXDV
V5 GBE_RXERR
P5 GBE_TXCLK
M5 GBE_TXD3
P9 GBE_TXD2
T7 GBE_TXD1
P7 GBE_TXD0
M7 GBE_TXCTL/TXEN
P4 GBE_PHY_PD
M9 GBE_PHY_RST#
R302 10K_4 GBE_PHY_INTR V7 GBE_PHY_INTR

GBE LAN

T9 ADP_PRES0 E23 PS2_DAT/SDA4/GPIO187
E24 PS2_CLK/SCL4/GPIO188
F21 SPI_CS2#/GBE_STAT2/GPIO166
G29 FC_RST#/GPO160
D27 PS2KB_DAT/GPIO189
E28 PS2KB_CLK/GPIO190
F29 PS2M_DAT/GPIO191
E27 PS2M_CLK/GPIO192

EMBEDDED CTRL

[02/22] AMD FAE and checklist request PL.

SB800 A12

A10 USB_14_48M T90
USBCLK/14M_25M_48M_OSC
G19 USB_RCOMP_SB R30 11.8K/F_6
USB_RCOMP

USB 1.1 USB MISC

USB_FSD1P/GPIO186 J10
USB_FSD1N H11
USB_FSD0P/GPIO185 H9 USB_FDS12P T13
USB_FSD0N J8 USB_FSD12N T17

USB_HSD13P B12 USBP13+ [22] CAMERA
USB_HSD13N A12 USBP13- [22]
USB_HSD12P F11 USBP12+ [31] USBX3 board
USB_HSD12N E11 USBP12- [31]
USB_HSD11P E14 USBP11+ [31] USBX3 board
USB_HSD11N E12 USBP11- [31]
USB_HSD10P J12 USBP10+ [30] Card reader
USB_HSD10N J14 USBP10- [30]
USB_HSD9P A13 USBP9+ [31] BLUETOOTH -1
USB_HSD9N B13 USBP9- [31]
USB_HSD8P D13 USBP8+ [31] BLUETOOTH -2
USB_HSD8N C13 USBP8- [31]
A04
USB_HSD7P G12
USB_HSD7N G14
USB_HSD6P G16
USB_HSD6N G18
USB_HSD5P D16
USB_HSD5N C16
USB_HSD4P B14 USBP4+ [26] WLAN Min-Card
USB_HSD4N A14 USBP4- [26]
USB_HSD3P E18
USB_HSD3N E16
USB_HSD2P J16
USB_HSD2N J18
USB_HSD1P B17 USBP1+ T6
USB_HSD1N A17 USBP1- T2
USB_HSD0P A16 USBP0+ [31]
USB_HSD0N B16 USBP0- [31]

USB 2.0

EHCI3/ OHCI3
EHCI2/ OHCI2
EHCI1/ OHCI1

On Board USB Connector
Only USB Port0 can be configured as debug port.

SCL2/GPIO193 D25 SB_SCLK2
SDA2/GPIO194 F23 SB_SDATA2
SCL3_LV/GPIO195 B26 SB_GPIO195
SDA3_LV/GPIO196 E26 SB_GPIO196
EC_PWM0/EC_TIMER0/GPIO197 F25 T87
EC_PWM1/EC_TIMER1/GPIO198 F22
EC_PWM2/EC_TIMER2/GPIO199 F22 GPIO199 [14]
EC_PWM3/EC_TIMER3/GPIO200 F21 GPIO200 [14]

KSI_0/GPIO201 G24
KSI_1/GPIO202 G25
KSI_2/GPIO203 E28
KSI_3/GPIO204 E29
KSI_4/GPIO205 D29
KSI_5/GPIO206 D28
KSI_6/GPIO207 C29
KSI_7/GPIO208 C28
KSO_0/GPIO209 B28
KSO_1/GPIO210 A27
KSO_2/GPIO211 B27
KSO_3/GPIO212 D26
KSO_4/GPIO213 A26
KSO_5/GPIO214 C26
KSO_6/GPIO215 A24
KSO_7/GPIO216 B25
KSO_8/GPIO217 A25
KSO_9/GPIO218 D24
KSO_10/GPIO219 B24
KSO_11/GPIO220 C24
KSO_12/GPIO221 B23
KSO_13/GPIO222 A23
KSO_14/GPIO223 D22
KSO_15/GPIO224 C22
KSO_16/GPIO225 A22
KSO_17/GPIO226 B22

EMBEDDED CTRL

Check list

SB_GPIO195 R284 10K_4
SB_GPIO196 R283 10K_4

PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number SB820-ACPI/GPIO/USB 2/4	Rev 1A
Date: Monday, May 31, 2010	Sheet 11 of 48	

Max trace length: 6"

SATA HDD

SATA ODD

SATA PORT 0,1,2,3 can support AHCI mode

Signal Name	Explanation
SATA_CALRP	SB800 A11: 800 ohm 1% resistor to GND. SB800 A12: 1K ohm 1% resistor to GND.
SATA_CALRN	SB800 A11: 931 ohm 1% resistor to VDDAN_11_SATA. SB800 A12: 931 ohm 1% resistor to VDDAN_11_SATA.

E-SATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB820

U14B

SB800
Part 2 of 5

SB800 A12

SERIAL ATA

FLASH

HW MONITOR

SPI ROM

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

Check list

BOM check

	1	0
ID0		
ID1	DIS	UMA
ID2		
ID3		
ID4		

VDDR_1.05_EN:
1 : VDDR =1.05V
0 : VDDR = 0.9V (Default)

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-SATA/IDE/SPI 3/4	1A

Date: Monday, May 31, 2010 Sheet 12 of 48

VDDQ--3.3V I/O power

PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

VDD-- S/B CORE power

U14C

SB800

Part 3 of 5

131mA

43mA

600mA

93mA

567mA

658mA

xx mA

510mA

400 mA

32mA

113mA

197mA

47mA

62mA

17mA

5mA

POWER

SB820 without GBE/ Connected to GND plane.

If the VDDIO_AZ_S power rail is configured for 1.5V_S5 then AZ_SDIN[3:0] can not be connected to 3.3-V devices.

For support USB wakeup-->3V_S5

(0212) AMD FAE confirmed

SB800 A12

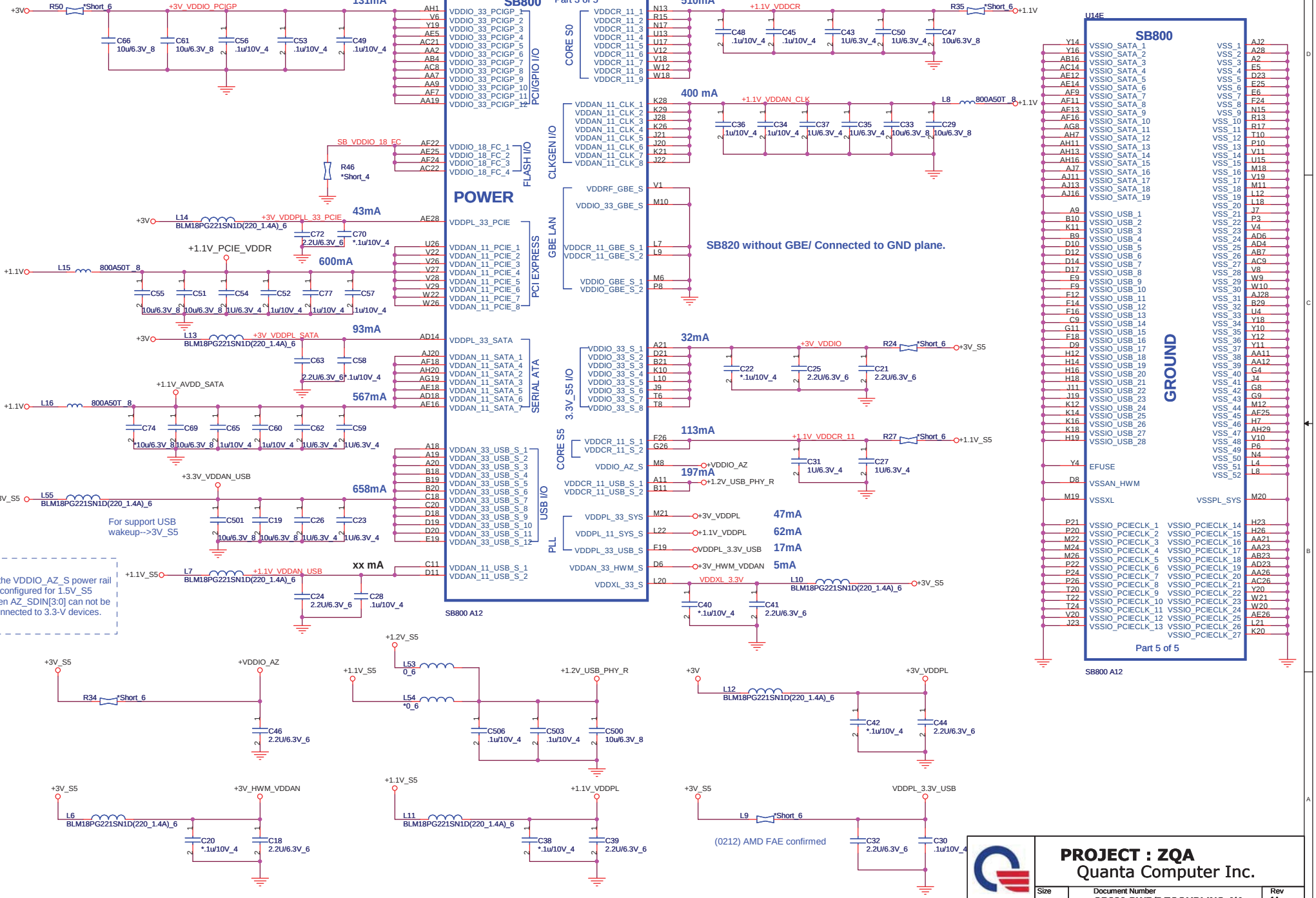
U14E

SB800

GROUND

Part 5 of 5

SB800 A12

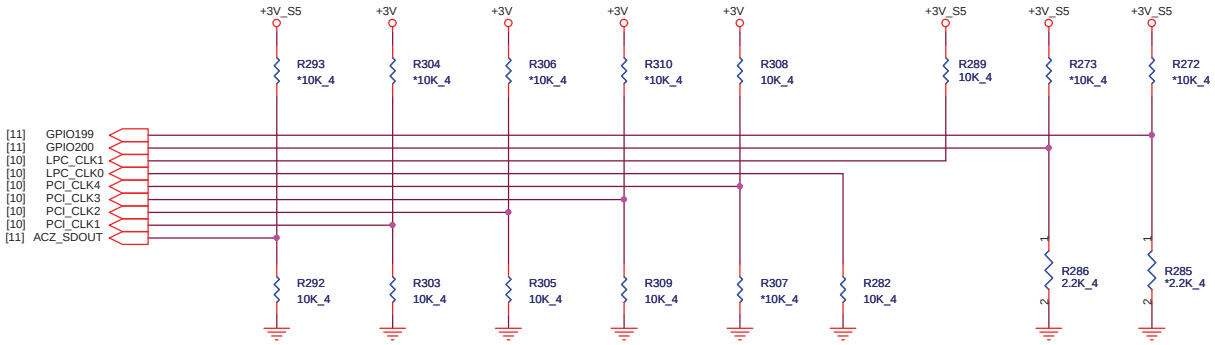


OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

SB820M is supported Gen.1 mode only.

For internal clock GEN.

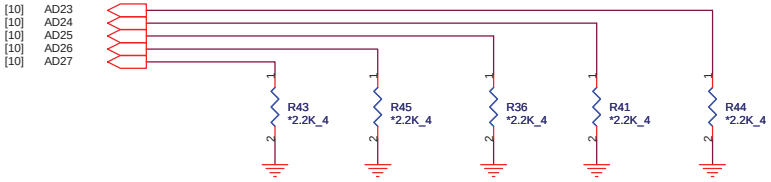


	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200 GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2	Watchdog Timer Enable	USE DEBUG STRAPS	non_Fusion CLOCK MODE DEFAULT	EC ENABLED	CLKGEN ENABLED DEFAULT	H, H=Reserved H, L=SPI ROM
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1 DEFAULT	Watchdog Timer Disable DEFAULT	IGNORE DEBUG STRAPS DEFAULT	Fusion CLOCK MODE	EC DISABLED DEFAULT	CLKGEN DISABLED	L, H=LPC ROM DEFAULT L, L=FWH ROM

internal have pull Hi 10K

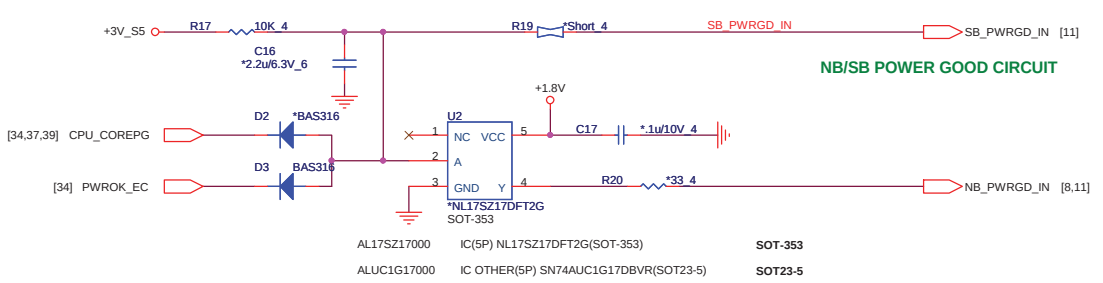
DEBUG STRAPS

SB800 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

NB_PWRGD_IN:
RS880/RX881 = 1.8V;
Do NOT share it with SB_PWRGD when use Internal Clk Gen (Need SB PLL initialize firstly)



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	SB820-STRAPS	1A

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U20A

[7] PEG_TXP[15..0] — PEG_TXP[15..0]
[7] PEG_TXN[15..0] — PEG_TXN[15..0]
[7] PEG_RXP[15..0] — PEG_RXP[15..0]
[7] PEG_RXN[15..0] — PEG_RXN[15..0]

PEG_TXP0	AA38	PCIE_RX0P	PCIE_TX0P	Y33	PEG_RXP0_C	C214	EV@.1u/10V_4	PEG_RXP0
PEG_TXN0	Y37	PCIE_RX0N	PCIE_TX0N	Y32	PEG_RXN0_C	C206	EV@.1u/10V_4	PEG_RXN0
PEG_TXP1	Y35	PCIE_RX1P	PCIE_TX1P	W33	PEG_RXP1_C	C219	EV@.1u/10V_4	PEG_RXP1
PEG_TXN1	W36	PCIE_RX1N	PCIE_TX1N	W32	PEG_RXN1_C	C216	EV@.1u/10V_4	PEG_RXN1
PEG_TXP2	W38	PCIE_RX2P	PCIE_TX2P	U33	PEG_RXP2_C	C227	EV@.1u/10V_4	PEG_RXP2
PEG_TXN2	V37	PCIE_RX2N	PCIE_TX2N	U32	PEG_RXN2_C	C220	EV@.1u/10V_4	PEG_RXN2
PEG_TXP3	V35	PCIE_RX3P	PCIE_TX3P	U30	PEG_RXP3_C	C229	EV@.1u/10V_4	PEG_RXP3
PEG_TXN3	U36	PCIE_RX3N	PCIE_TX3N	U29	PEG_RXN3_C	C243	EV@.1u/10V_4	PEG_RXN3
PEG_TXP4	U38	PCIE_RX4P	PCIE_TX4P	T33	PEG_RXP4_C	C258	EV@.1u/10V_4	PEG_RXP4
PEG_TXN4	T37	PCIE_RX4N	PCIE_TX4N	T32	PEG_RXN4_C	C246	EV@.1u/10V_4	PEG_RXN4
PEG_TXP5	T35	PCIE_RX5P	PCIE_TX5P	T30	PEG_RXP5_C	C264	EV@.1u/10V_4	PEG_RXP5
PEG_TXN5	R36	PCIE_RX5N	PCIE_TX5N	T29	PEG_RXN5_C	C272	EV@.1u/10V_4	PEG_RXN5
PEG_TXP6	R38	PCIE_RX6P	PCIE_TX6P	P33	PEG_RXP6_C	C274	EV@.1u/10V_4	PEG_RXP6
PEG_TXN6	P37	PCIE_RX6N	PCIE_TX6N	P32	PEG_RXN6_C	C286	EV@.1u/10V_4	PEG_RXN6
PEG_TXP7	P35	PCIE_RX7P	PCIE_TX7P	P30	PEG_RXP7_C	C289	EV@.1u/10V_4	PEG_RXP7
PEG_TXN7	N36	PCIE_RX7N	PCIE_TX7N	P29	PEG_RXN7_C	C295	EV@.1u/10V_4	PEG_RXN7
PEG_TXP8	N38	PCIE_RX8P	PCIE_TX8P	N33	PEG_RXP8_C	C297	EV@.1u/10V_4	PEG_RXP8
PEG_TXN8	M37	PCIE_RX8N	PCIE_TX8N	N32	PEG_RXN8_C	C309	EV@.1u/10V_4	PEG_RXN8
PEG_TXP9	M35	PCIE_RX9P	PCIE_TX9P	N30	PEG_RXP9_C	C321	EV@.1u/10V_4	PEG_RXP9
PEG_TXN9	L36	PCIE_RX9N	PCIE_TX9N	N29	PEG_RXN9_C	C310	EV@.1u/10V_4	PEG_RXN9
PEG_TXP10	L38	PCIE_RX10P	PCIE_TX10P	L33	PEG_RXP10_C	C323	EV@.1u/10V_4	PEG_RXP10
PEG_TXN10	K37	PCIE_RX10N	PCIE_TX10N	L32	PEG_RXN10_C	C333	EV@.1u/10V_4	PEG_RXN10
PEG_TXP11	K35	PCIE_RX11P	PCIE_TX11P	L30	PEG_RXP11_C	C334	EV@.1u/10V_4	PEG_RXP11
PEG_TXN11	J36	PCIE_RX11N	PCIE_TX11N	L29	PEG_RXN11_C	C341	EV@.1u/10V_4	PEG_RXN11
PEG_TXP12	J38	PCIE_RX12P	PCIE_TX12P	K33	PEG_RXP12_C	C347	EV@.1u/10V_4	PEG_RXP12
PEG_TXN12	H37	PCIE_RX12N	PCIE_TX12N	K32	PEG_RXN12_C	C342	EV@.1u/10V_4	PEG_RXN12
PEG_TXP13	H35	PCIE_RX13P	PCIE_TX13P	J33	PEG_RXP13_C	C353	EV@.1u/10V_4	PEG_RXP13
PEG_TXN13	G36	PCIE_RX13N	PCIE_TX13N	J32	PEG_RXN13_C	C348	EV@.1u/10V_4	PEG_RXN13
PEG_TXP14	G38	PCIE_RX14P	PCIE_TX14P	K30	PEG_RXP14_C	C358	EV@.1u/10V_4	PEG_RXP14
PEG_TXN14	F37	PCIE_RX14N	PCIE_TX14N	K29	PEG_RXN14_C	C369	EV@.1u/10V_4	PEG_RXN14
PEG_TXP15	F35	PCIE_RX15P	PCIE_TX15P	H33	PEG_RXP15_C	C354	EV@.1u/10V_4	PEG_RXP15
PEG_TXN15	E37	PCIE_RX15N	PCIE_TX15N	H32	PEG_RXN15_C	C357	EV@.1u/10V_4	PEG_RXN15

PCI EXPRESS INTERFACE

CLOCK

[10] CLK_PCIE_VGAP — AB35 — PCIE_REFCLKP
[10] CLK_PCIE_VGAN — AA36 — PCIE_REFCLKN

AJ21 — NC#1
AK21 — NC#2
AH16 — PWRGOOD

PCIE_RST_VGA# — AA30 — PERSTB

CALIBRATION

PCIE_CALRP — Y30 — R137 — EV@1.27K/F_4
PCIE_CALRN — Y29 — R142 — EV@2K/F_4 — +1V

+1.0V

For Madison and Park PCIE_VDDC is 1.0V

For Madison and Park the PWRGOOD ball must be connecccted to ground

R98 — EV@10K_4

EV@Park_M2

+3V_D
R375
EV@10K/F_4
PCIE_RST_VGA#
D22 EV@BAS316 — A_RST# [10,24,26]
D21 EV@BAS316 — dGPU_RST_GPIO [10]

PROJECT : ZQA
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Size	Document Number	Rev
	Madison/Park-PCIE 1/6	1A
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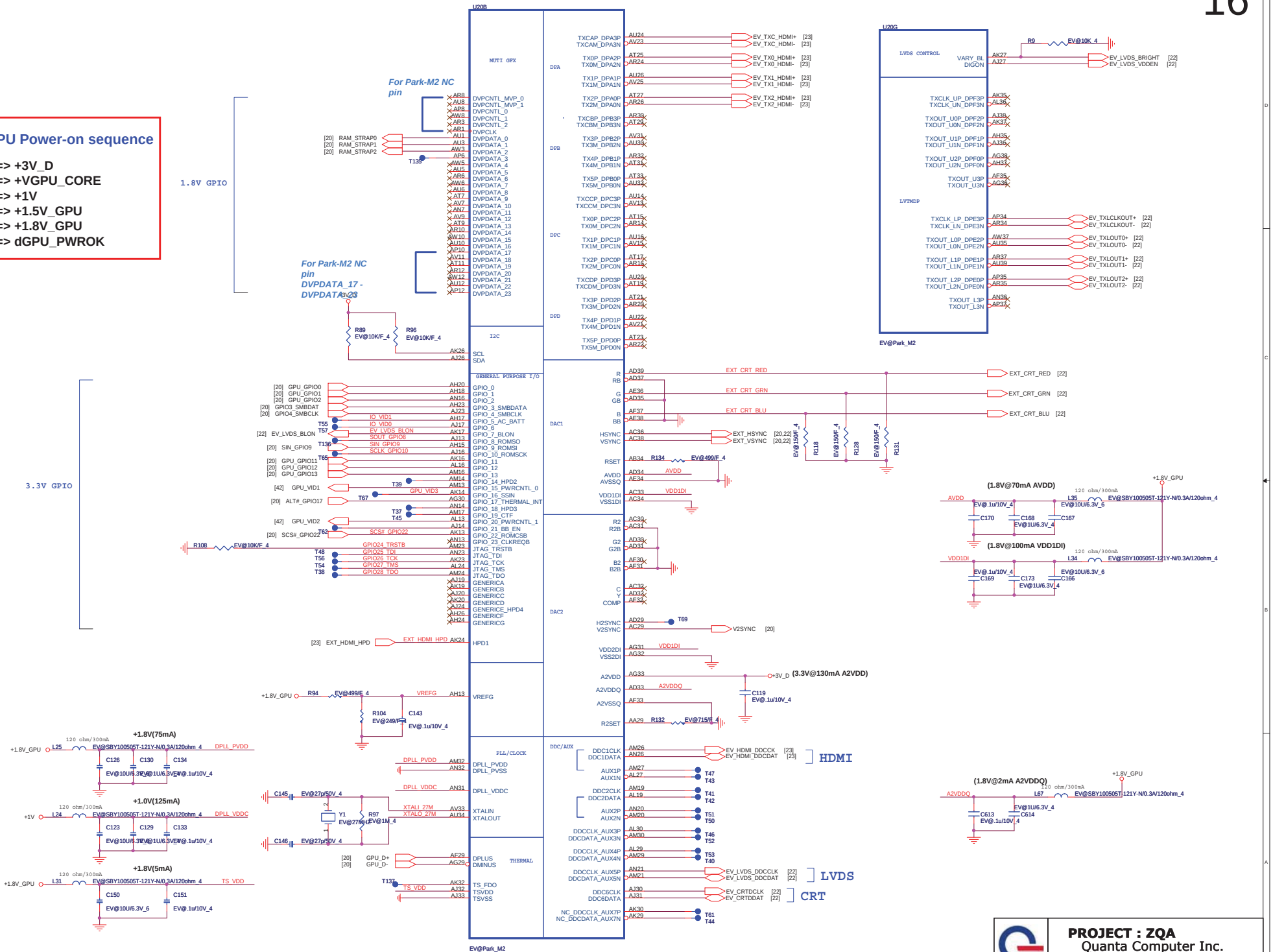
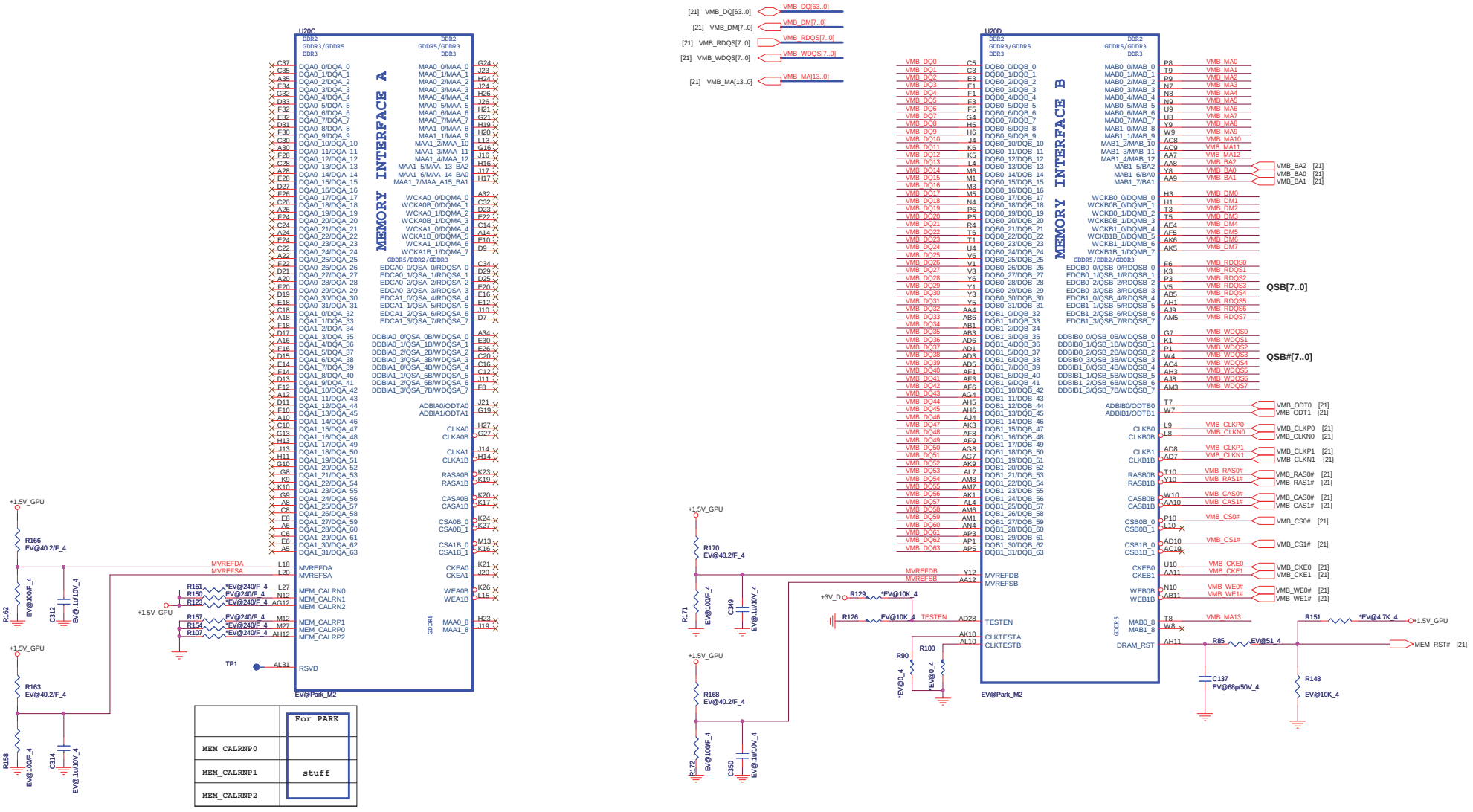
GPU Power-on sequence

1 => +3V_D
2 => +VGPU_CORE
3 => +1V
4 => +1.5V_GPU
5 => +1.8V_GPU
6 => dGPU_PWROK





DDR3/GDDR3 Memory Stuff Option

	GDDR5	GDDR3	DDR3
+1.5V_VGA	1.5V	1.8V/1.5V	1.5V
Ra	40.2R	40.2R	40.2R
Rb	100R	100R	100R

Designator	For M97-M2	For Mannhatton
Ra	10K	10K
Rb	0R/Short	680R
Rc	DNI	DNI
Ca	2.2nF	68pF

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Size	Document Number	Rev
	Madison/Park-MEM 3/6	1A

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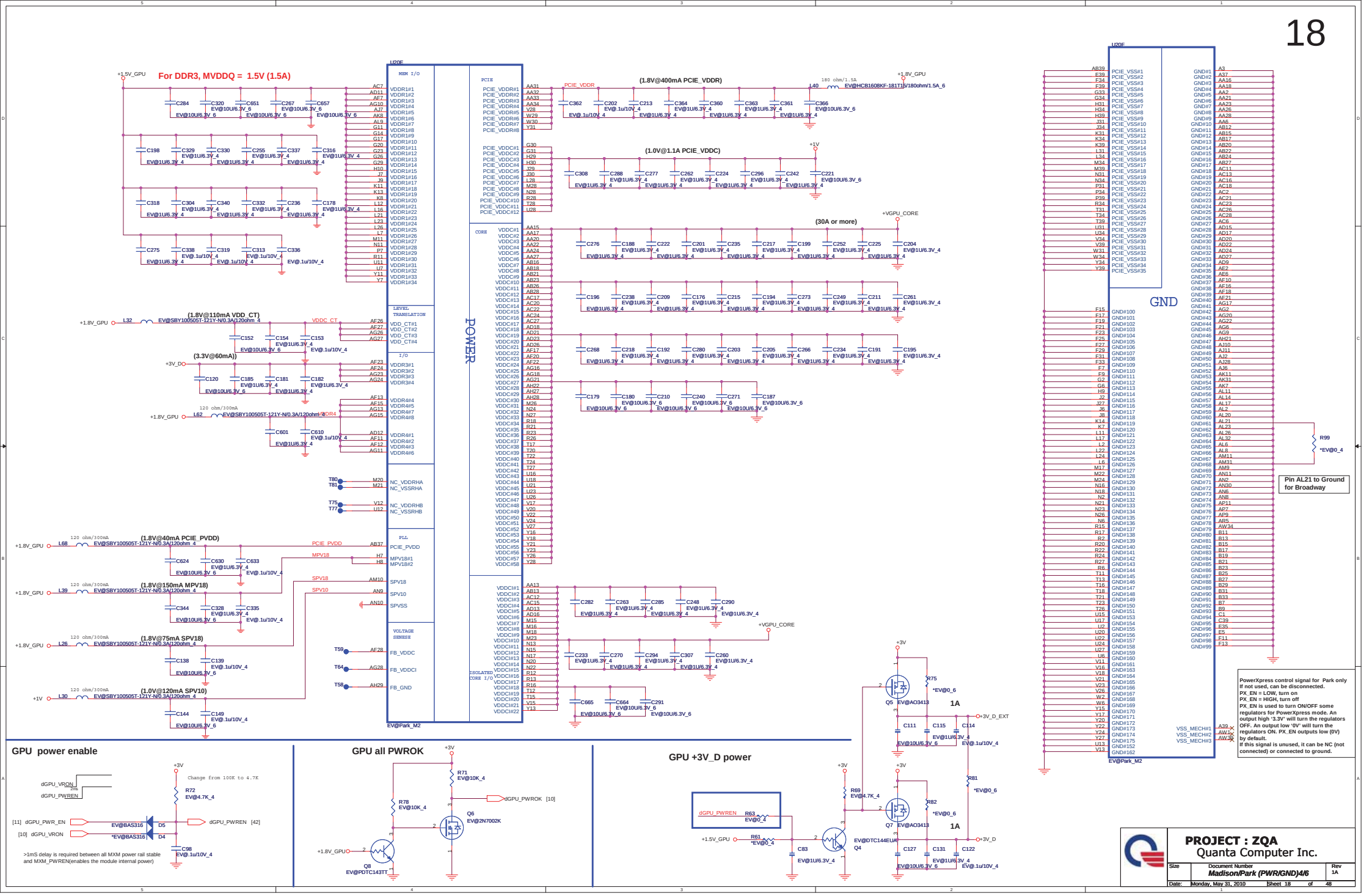
For DDR3, MVDDQ = 1.5V (1.5A)
U20E
POWER
MEM I/O
LEVEL TRANSLATION
I/O
PLL
VOLTAGE SENSE
PCIE
CORE
ISOLATED CORE I/O
(1.8V@400mA PCIE_VDDR)
(1.0V@1.1A PCIE_VDDC)
(30A or more)
(1.8V@110mA VDD_CT)
(3.3V@60mA))
(1.8V@40mA PCIE_PVDD)
(1.8V@150mA MPV18)
(1.8V@75mA SPV18)
(1.0V@120mA SPV10)
GND
Pin AL21 to Ground for Broadway
PowerXpress control signal for Park only
If not used, can be disconnected.
PX_EN = LOW, turn on
PX_EN = HIGH, turn off
PX_EN is used to turn ON/OFF some regulators for PowerXpress mode. An output high '3.3V' will turn the regulators OFF. An output low '0V' will turn the regulators ON. PX_EN outputs low (0V) by default.
If this signal is unused, it can be NC (not connected) or connected to ground.
GPU power enable
GPU all PWROK
GPU +3V_D power
>1mS delay is required between all MXM power rail stable and MXM_PWREN(enables the module internal power)
PROJECT : ZQA
Quanta Computer Inc.
Size
Document Number
Madison/Park (PWR/GND)4/6
Rev 1A
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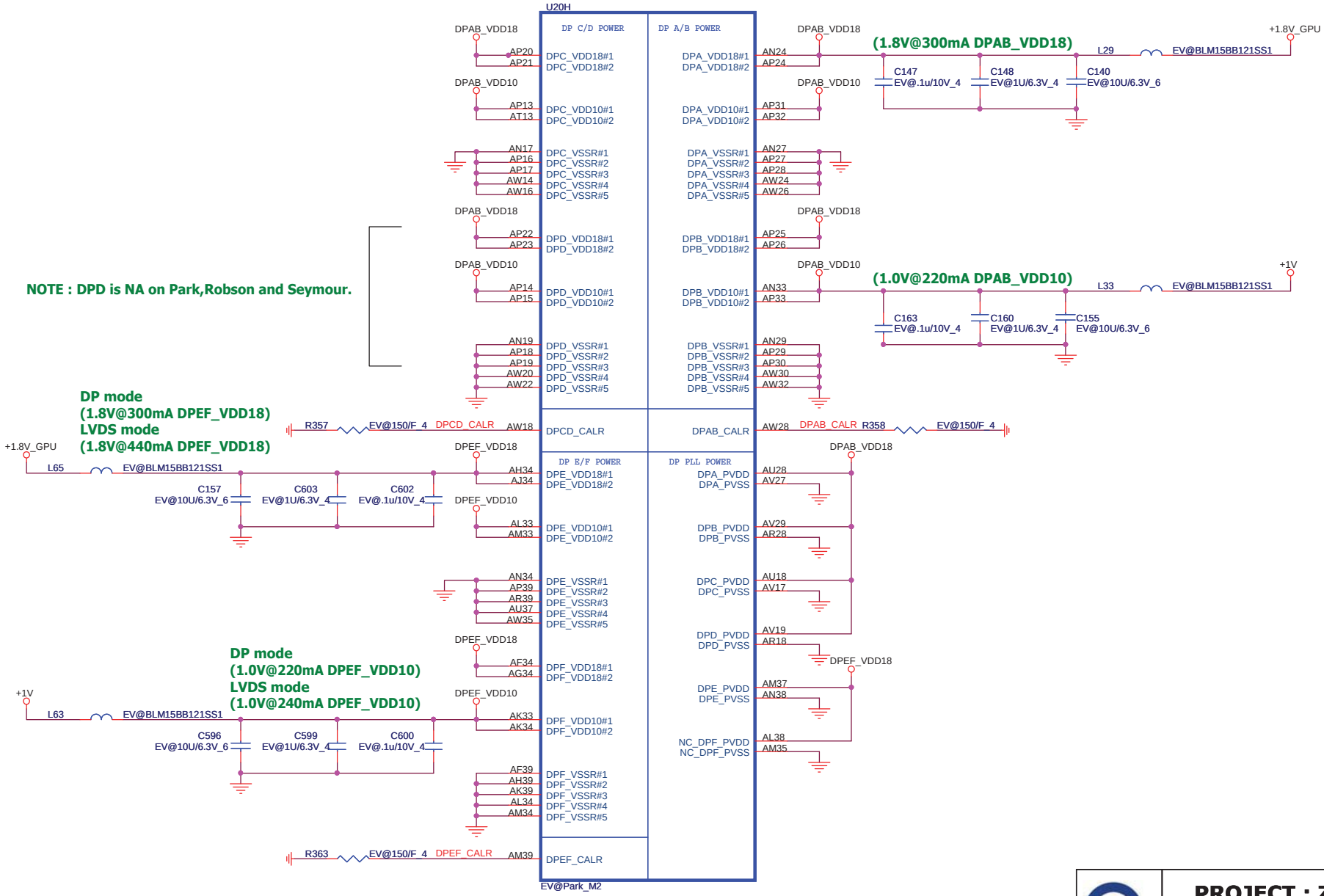

PROJECT : ZQA
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Size	Document Number	Rev
	Madison/Park (DP_PWR/GND)5/6	1A
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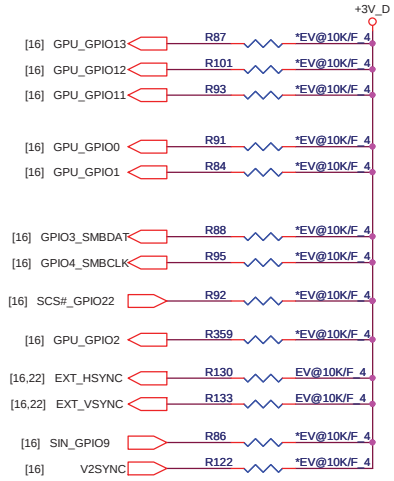
PIN STRAPS



Memory Aperture size	
GPIO[13:11]	Size
000	128MB
001	256MB
010	64MB
011	32MB

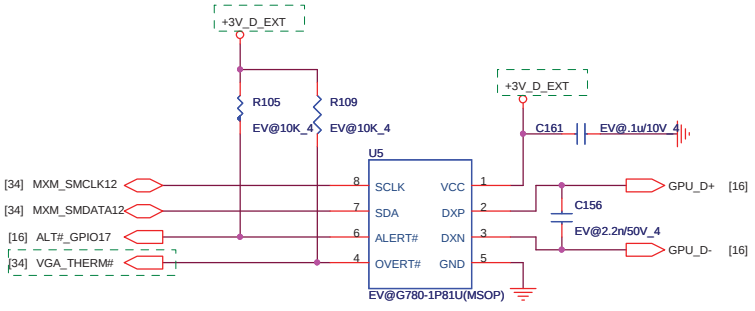
ROM Table		
EXT_HSYNC	EXT_VSYNC	Discription
0	0	No Audio
0	1	Any one by dectec
1	0	DP only
1	1	Both DP & HDMI

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	DEFAULT	REMARK
TX_PWRS_ENB	GPIO0	0 = 50% TX OUTPUT SWING 1 = FULL TX OUTPUT SWING	0	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED 0 = TX DE-EMPHASIS DISABLED 1 = TX DE-EMPHASIS ENABLED	0	
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM 0 = DISABLE 1 = ENABLE	0	
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT NUMONYX M25P10A : 101	000	See ROM table
BIF_GEN2_EN_A	GPIO2	0 = PCIE DEVICE AS 2.5GT/S CAPABLE 1 = PCIE DEVICE AS 5GT/S CAPABLE	0	
GPIO_8_ROMSO H2SYNC GPIO_21_BB_EN	GPIO8 H2SYNC GPIO21	Reserved Only	0	
AUD[1] AUD[0]	HSYNC VSYNC	AUD[1:0] 00: NO AUDIO FUNCTION. 01: AUDIO FOR DISPLAYPORT AND HDMI IF ADAPTER IS DETECTED. 10: AUDIO FOR DISPLAYPORT ONLY. 11: AUDIO FOR BOTH DISPLAYPORT AND HDMI.	11	See Audio table
GPIO_9_ROMSI	GPIO9	0 = VGA controller capacity enable	0	
VIP_DEVICE_STRAP_ENA	V2SYNC	0 = DRIVER would ignore the value sample on VHAD_0 during RESET.	0	

Thermal Sensor

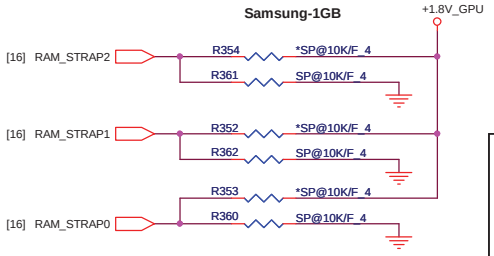


Address ID: 98H

DDR3 Memory Aperture size

DDR3 Memory Aperture size

Vendor	Vendor P/N	STN B/S P/N	Size	RAM_STRAP2 DVPDATA_2	RAM_STRAP1 DVPDATA_1	RAM_STRAP0 DVPDATA_0
Hynix			512MB	1	1	0
	H5TQ1G63BFR-12C	AKD5LZGTW04 (64M*16)	1GB	1	0	0
			2GB	1	1	1
Samsung			512MB	0	1	0
	K4W1G1646E-HC12	AKD5LGGT506 (64M*16)	1GB	0	0	0
	K4W2G1646B-HC12	AKD5MGGT500	2GB	0	0	1



RAM_STRAP2 SET DDR3 Vendor
RAM_STRAP[1:0] SET SIZE.

PROJECT : ZQA
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Size	Document Number	Rev
	Medison/Park Strip/Thermal 6/6	1A
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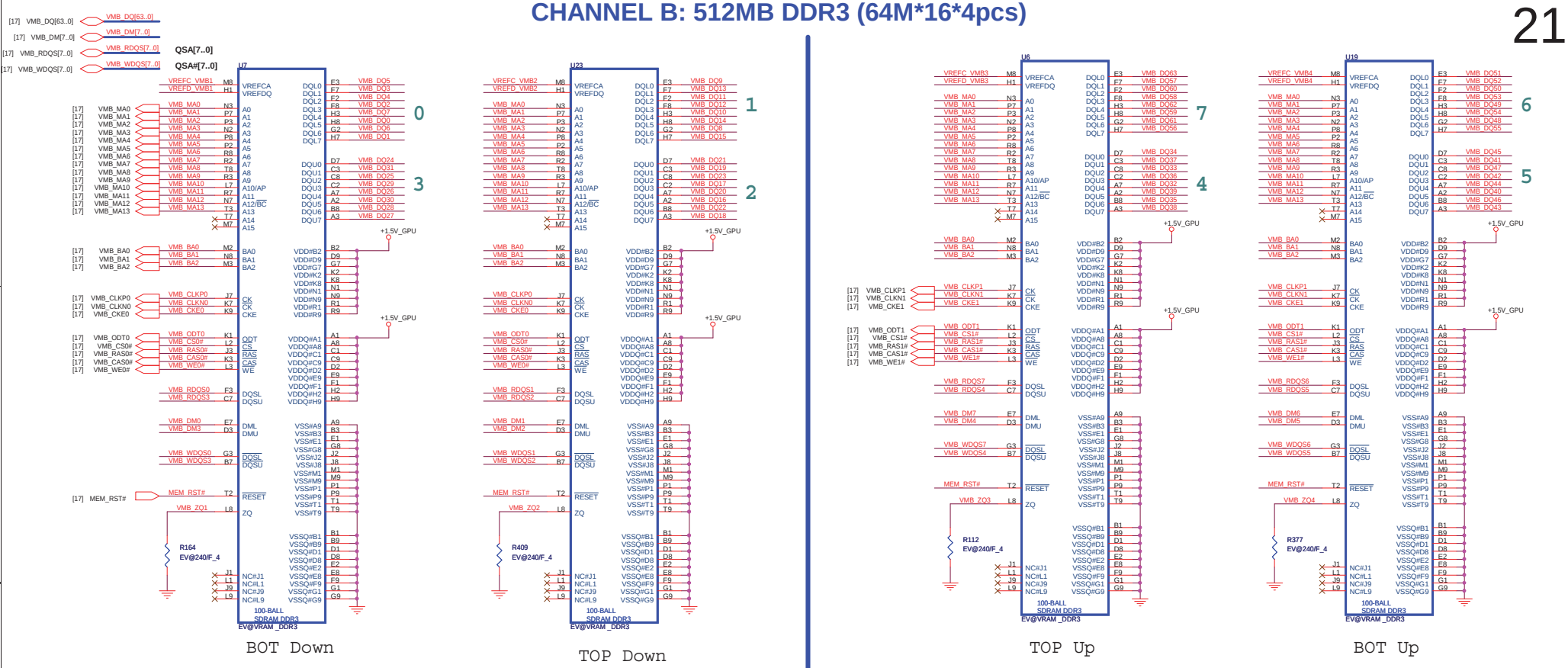
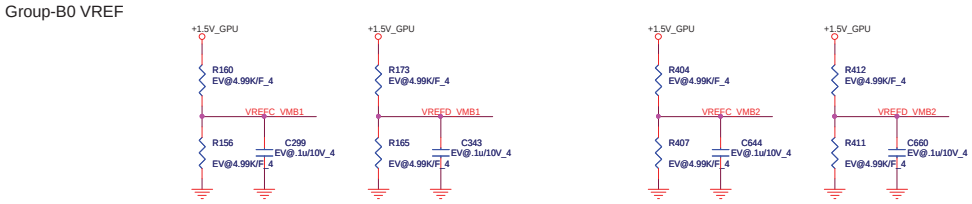
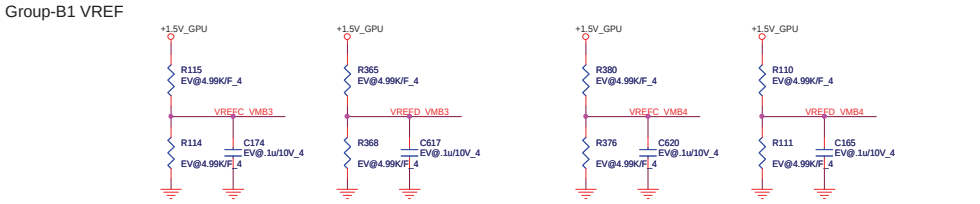
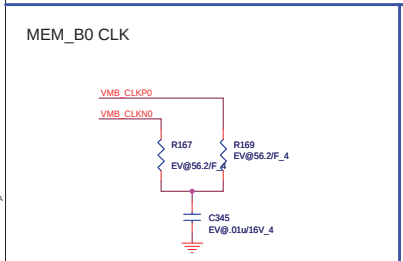
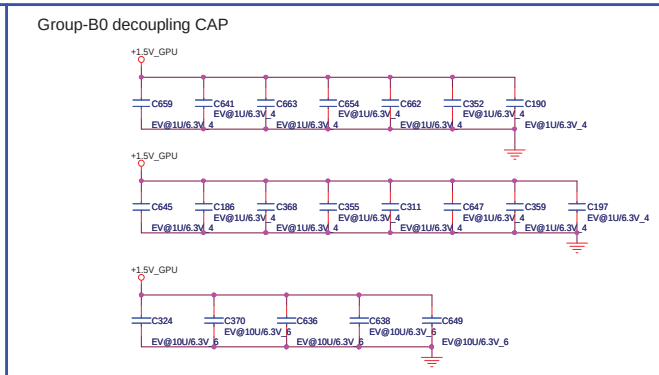
CHANNEL B: 512MB DDR3 (64M*16*4pcs)

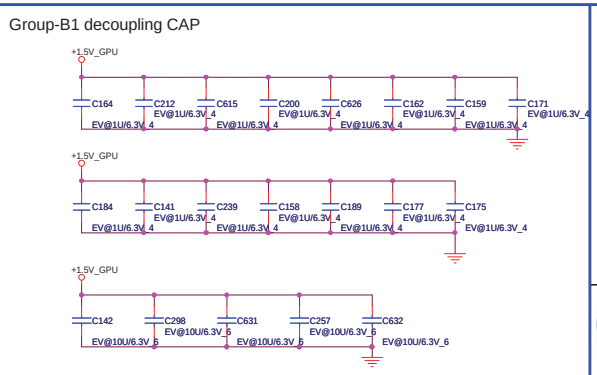


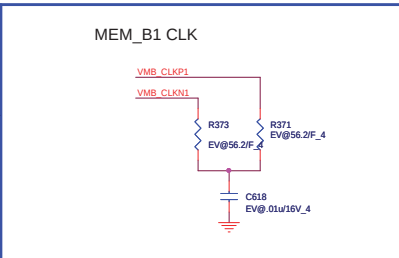












PROJECT : ZQA
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Size	Document Number	Rev
	MEMORY 2 channel B	1A

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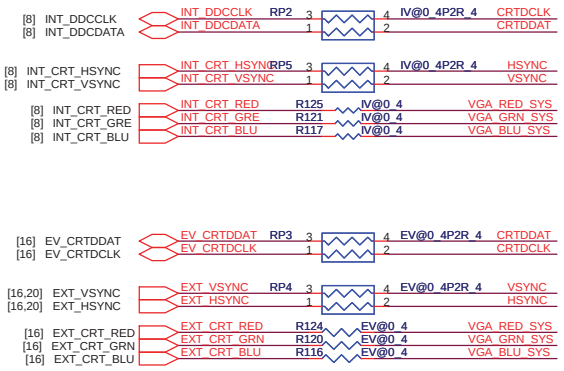
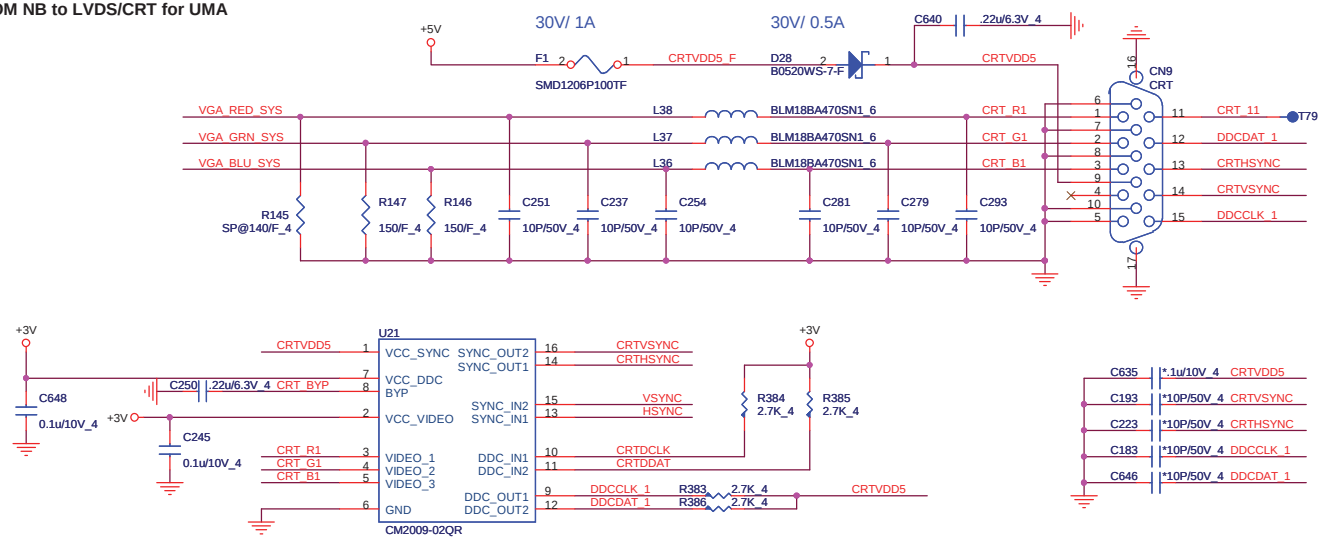
CRT

OPTION SIGNAL FROM NB to CRT for UMA



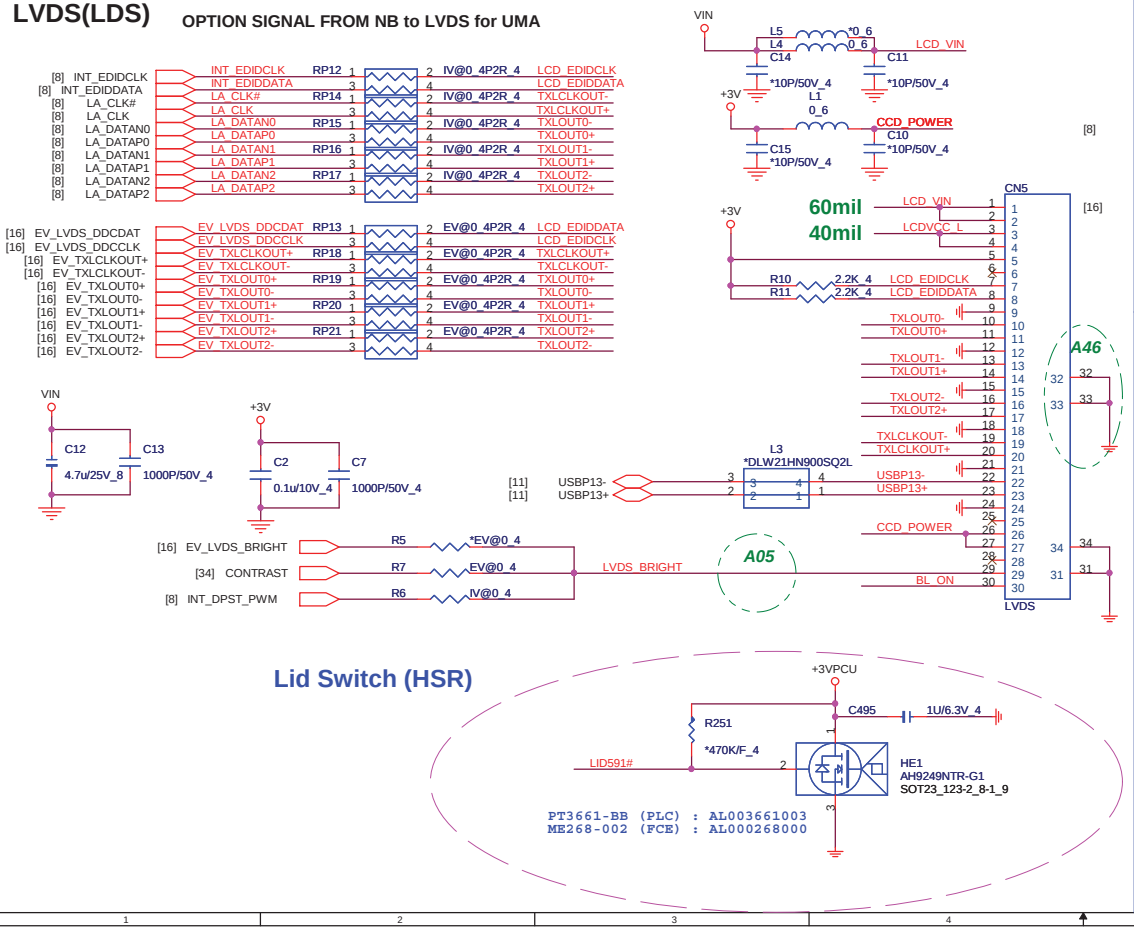
OPTION SIGNAL FROM NB to LVDS/CRT for UMA



OPTION LCDVCC SIGNAL FROM NB to LVDS for UMA

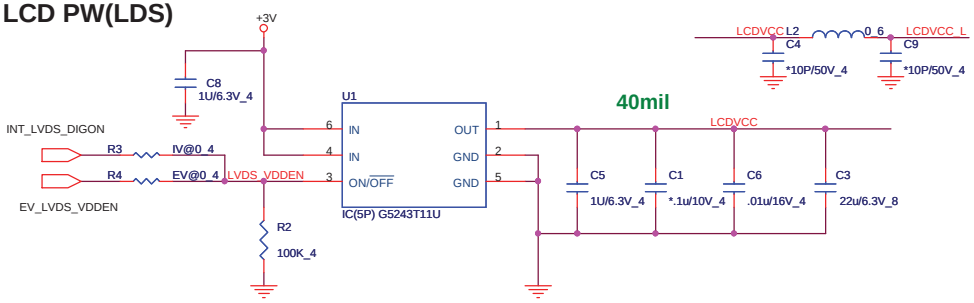
LVDS(LDS)

OPTION SIGNAL FROM NB to LVDS for UMA

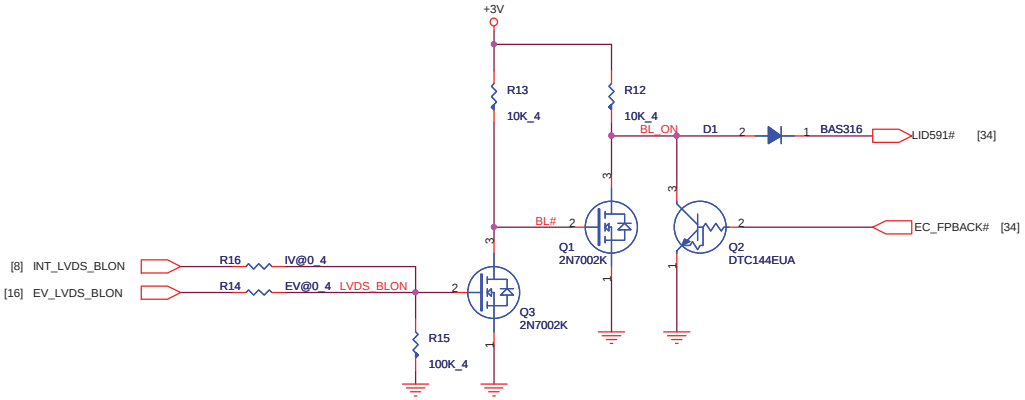


Lid Switch (HSR)

LCD PW(LDS)



Backlight Control(LDS)



PROJECT : ZQA
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	CRT/LVDS/LID	1A
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HDMI SDVO I2C Control

UMA Close to HDMI Connector

[8] IV_HDMI_DDC_DATA
[8] IV_HDMI_DDC_CLK
IV@0_4P2R_4
RP6
HDMI_DDCDATA
HDMI_DDCCLK

DIS

[16] EV_HDMI_DDCDAT
R433 *EV@4.7K_4
R432 EV@0_4
Q20 *EV@2N7002K
HDMI_DDCDATA

[16] EV_HDMI_DDCCK
R438 *EV@4.7K_4
R437 EV@0_4
Q21 *EV@2N7002K
HDMI_DDCCLK

HDMI HPD SENSE (HDM)

UMA use +3V for the detect pin
Dis use +3V_DELAY for the detect pin

[16] EXT_HDMI_HPD
R422 EV@10K_4
Q18 EV@2N7002K
R190 10K_4
Q19 2N7002K
HDMI_DET_R R423 200K/F_4
HDMI_DET
R421 200K/F_4

[8] INT_HDMI_HPD
R191 IV@10K_4
Q9 IV@2N7002K
HDMI_HPD_EC# [34]

23

HDMI (HDM)

Close to HDMI Connector

Q17 2N7002K
R420 100K/F_4
HDMI_PLUG_MOS

R440	EV@499/F_4	TX2_HDMI+
R441	EV@499/F_4	TX2_HDMI-
R435	EV@499/F_4	TX1_HDMI+
R434	EV@499/F_4	TX1_HDMI-
R439	EV@499/F_4	TX0_HDMI+
R436	EV@499/F_4	TX0_HDMI-
R431	EV@499/F_4	TXC_HDMI+
R430	EV@499/F_4	TXC_HDMI-

Due to HDMI item7-2 is fail,
Change to CS16492FB13.

UMA RS880M
Stuff 715 ohm CS17152FB17

DIS Park-M2
Stuff 499 ohm CS14992FB24

EMI reserve for HDMI(EMC)

Close connector

TX2_HDMI+	R212	*100/F_4
TX2_HDMI-		
TX1_HDMI+	R205	*100/F_4
TX1_HDMI-		
TX0_HDMI+	R206	*100/F_4
TX0_HDMI-		
TXC_HDMI+	R200	*100/F_4
TXC_HDMI-		

for Layout concern
,placement close HDMI conn

[7] IV_TX2_HDMI+	RP10	IV@0_4P2R_4	TX2_HDMI+
[7] IV_TX2_HDMI-			TX2_HDMI-
[7] IV_TX1_HDMI+	RP8	IV@0_4P2R_4	TX1_HDMI+
[7] IV_TX1_HDMI-			TX1_HDMI-
[7] IV_TX0_HDMI+	RP9	IV@0_4P2R_4	TX0_HDMI+
[7] IV_TX0_HDMI-			TX0_HDMI-
[7] IV_TXC_HDMI+	RP7	IV@0_4P2R_4	TXC_HDMI+
[7] IV_TXC_HDMI-			TXC_HDMI-

[16] EV_TX2_HDMI+	C695	EV@.1u/10V_4	TX2_HDMI+
[16] EV_TX2_HDMI-	C696	EV@.1u/10V_4	TX2_HDMI-
[16] EV_TX1_HDMI+	C691	EV@.1u/10V_4	TX1_HDMI+
[16] EV_TX1_HDMI-	C690	EV@.1u/10V_4	TX1_HDMI-
[16] EV_TX0_HDMI+	C694	EV@.1u/10V_4	TX0_HDMI+
[16] EV_TX0_HDMI-	C693	EV@.1u/10V_4	TX0_HDMI-
[16] EV_TXC_HDMI+	C688	EV@.1u/10V_4	TXC_HDMI+
[16] EV_TXC_HDMI-	C687	EV@.1u/10V_4	TXC_HDMI-

HDMI PORT (HDM)

CN13
QJ1119C-NK01-8F

D12 CH501H-40PT
D11 CH501H-40PT
R428 2K/F_4
R426 2K/F_4
HDMI_DDCCLK
HDMI_DDCDATA

F2 SMD1206P100TF
+5V_HDMI_F
D10 RSX101M-30
30V/ 1A
Becuase HDMI item7-11 is fail,
Change to BC101M30Z00.
+5V_HDMI
HDMI_DET

C429 .22u/6.3V_4
C725 *1000P/50V_4
C729 *1000P/50V_4
A17

TX2_HDMI+	1
TX2_HDMI-	3
TX1_HDMI+	4
TX1_HDMI-	6
TX0_HDMI+	7
TX0_HDMI-	9
TXC_HDMI+	10
TXC_HDMI-	12
HDMI_DDCCLK	15
HDMI_DDCDATA	16
+5V_HDMI	18
HDMI_DET	19

SHELL1 D2+SHELL3 D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL4 SHELL2
20 22 23 21

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	HDMI	1A
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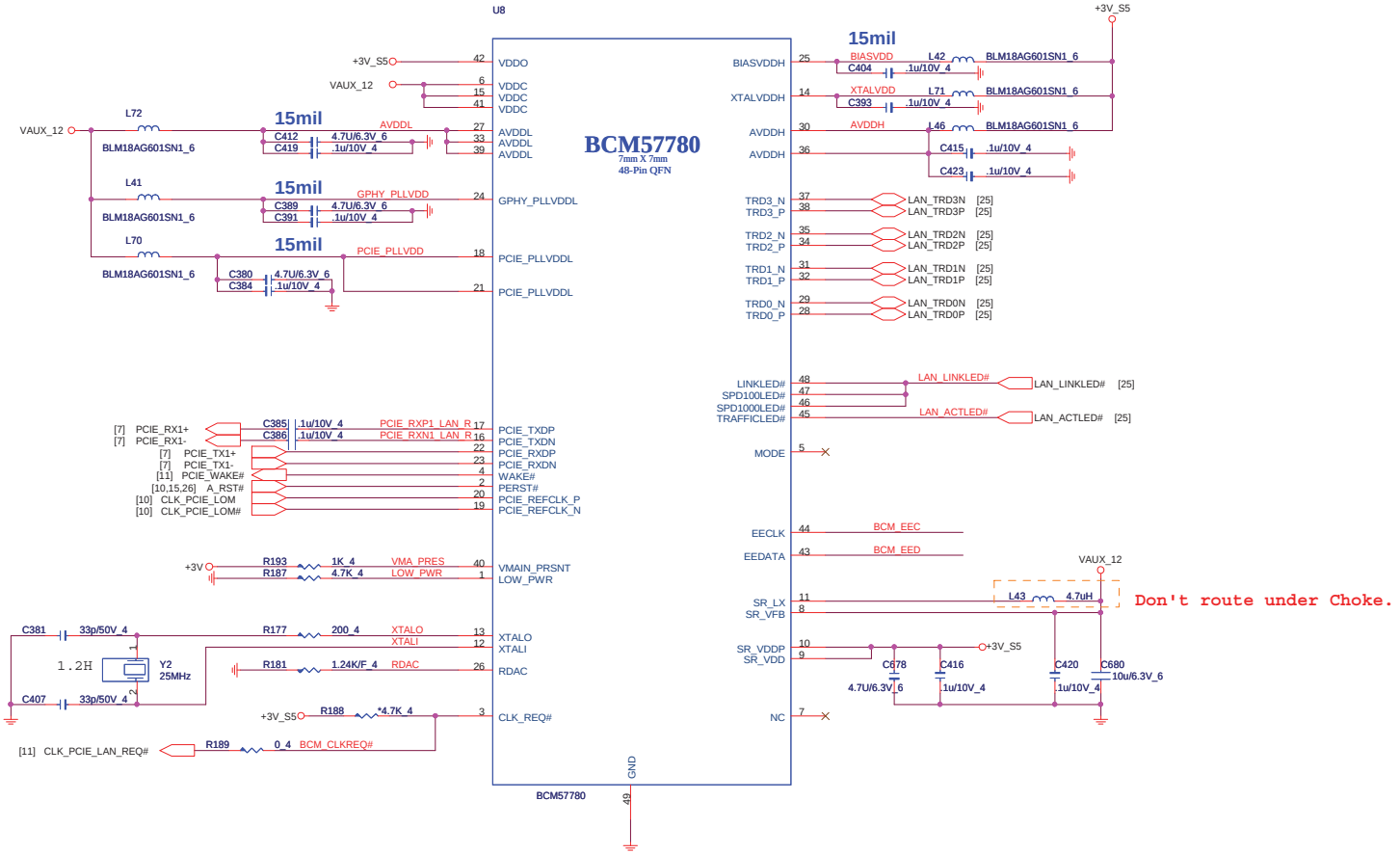
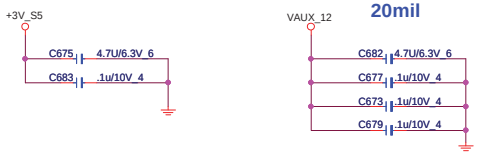
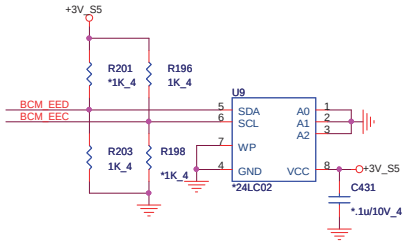
Giga-LAN BCM57780



LAN POWER



EEPROM



EEPROM Strapping

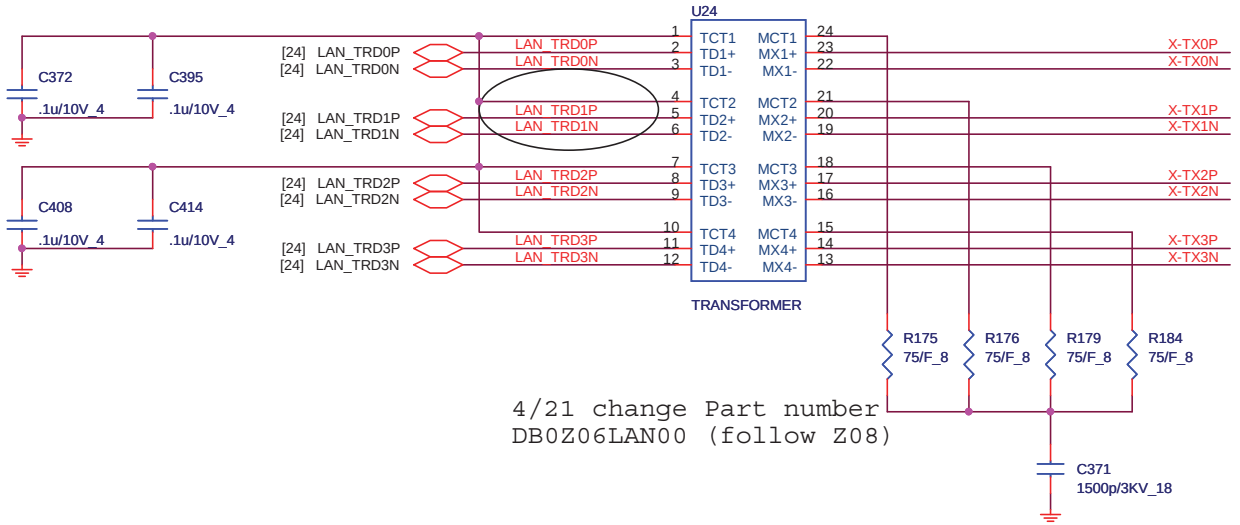
EEPROM Type	EECLK	EEDATA
24LC02	1	1
Internal	1	0

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	GLAN BCM57780	1A
Date: Monday, May 31, 2010	Sheet 24 of 48	

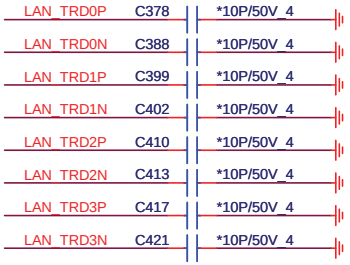
TRANSFORMER

4/27 modify it

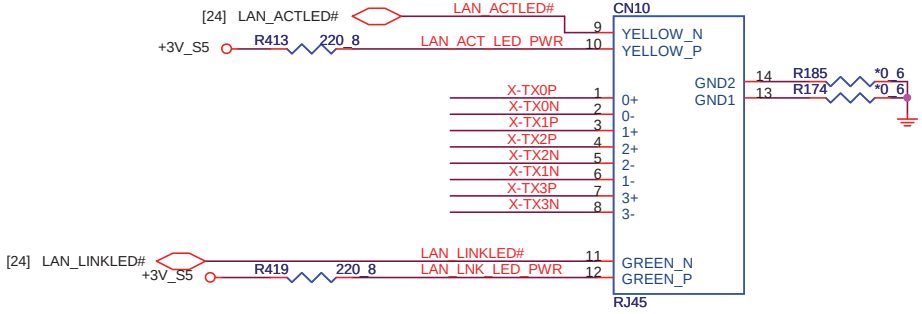


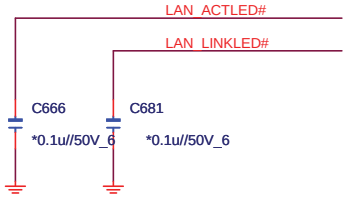
4/21 change Part number
DB0Z06LAN00 (follow Z08)

For EMI



RJ45 Conn





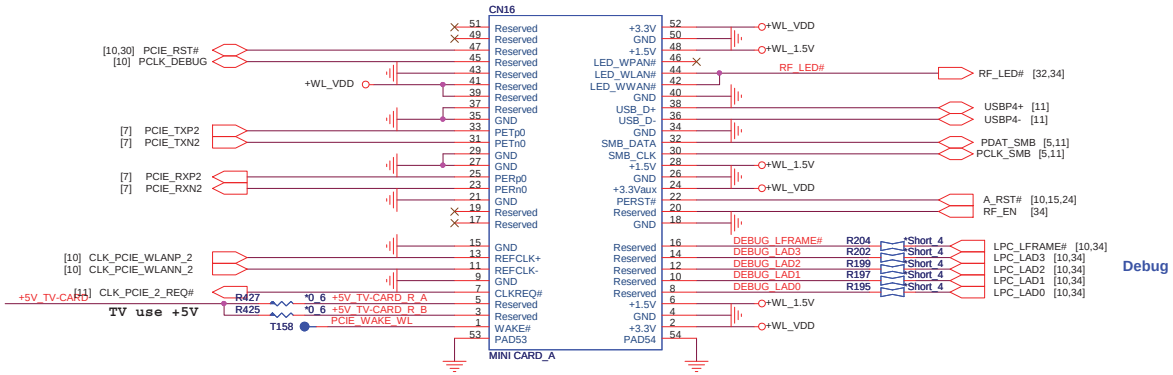
PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	LAN Transformer and RJ45	1A
Date: Monday, May 31, 2010	Sheet 25 of 48	

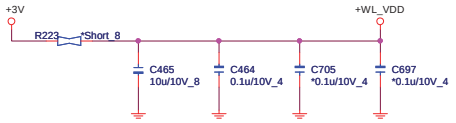
MINI-CARD WLAN(MPC)

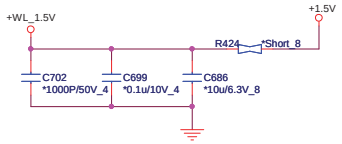
+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

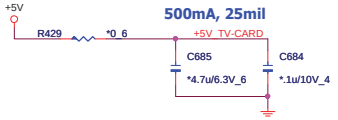
Check LED signal. (active high or low)



Debug

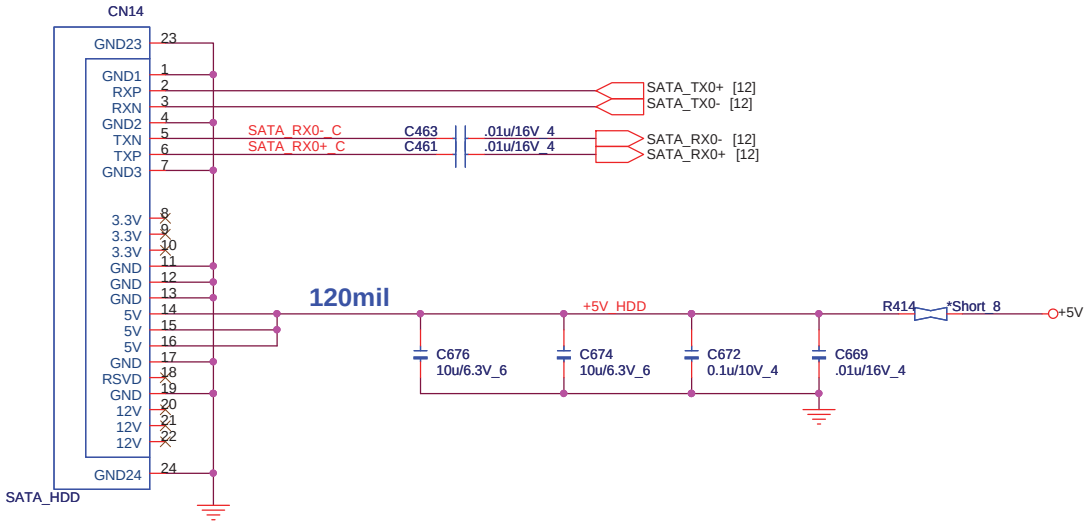




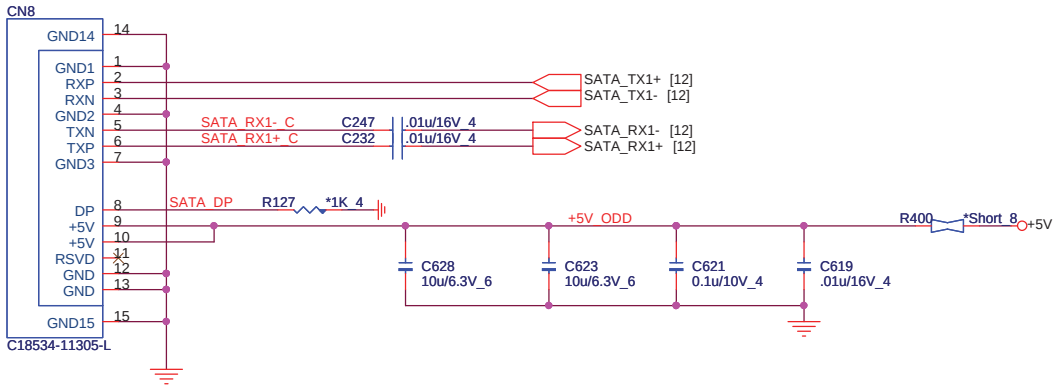


PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number *MINI PCI-E card/TV*	Rev 1A
Date: Monday, May 31, 2010	Sheet 26 of 48	

SATA HDD

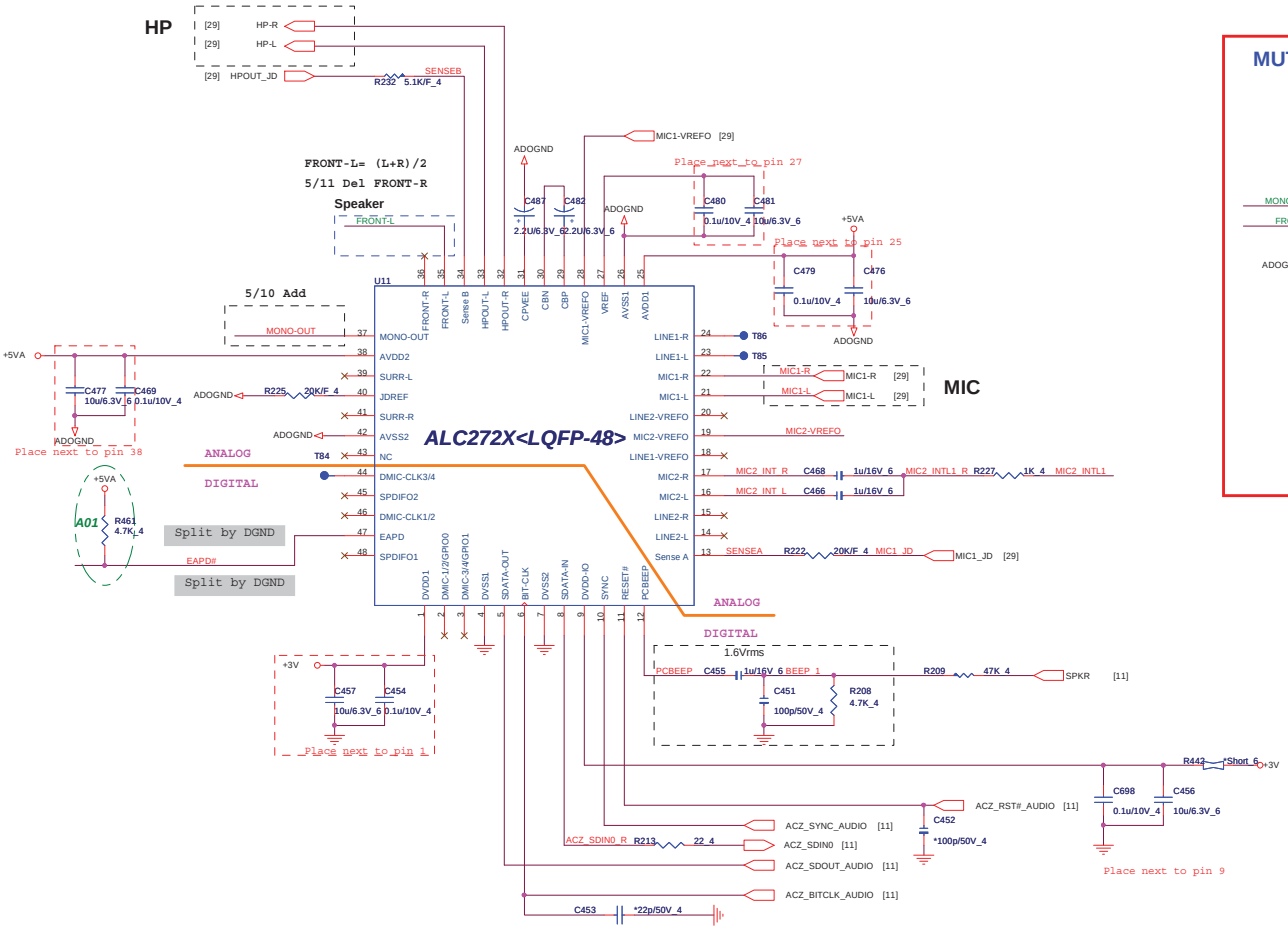


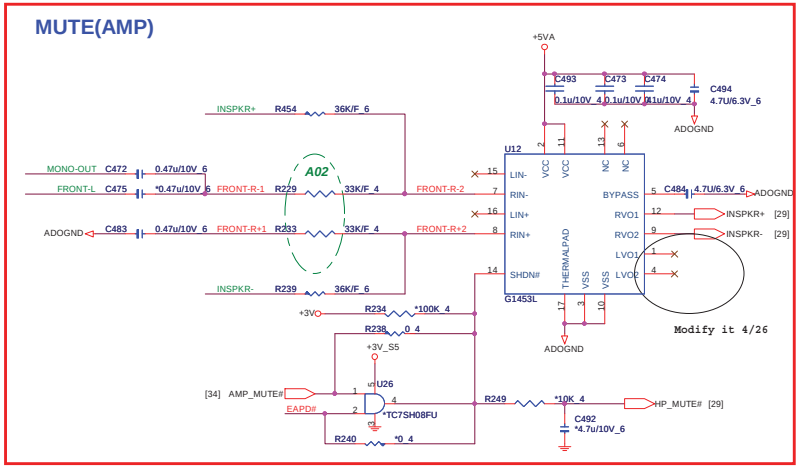
SATA ODD

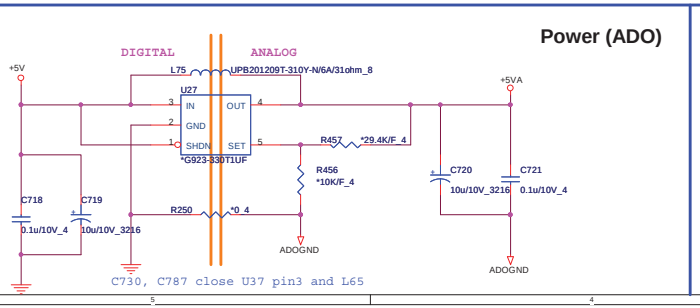


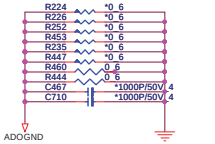
PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number SATA-HDD/ODD/HOLE	Rev 1A
Date: Monday, May 31, 2010	Sheet 27 of 48	

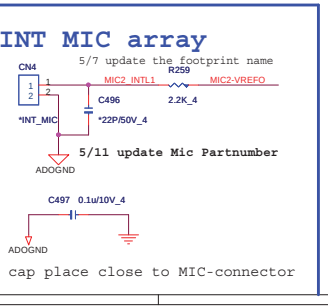
Codec(ADO)











PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	REALTEK ALC663&888/MDC	1A
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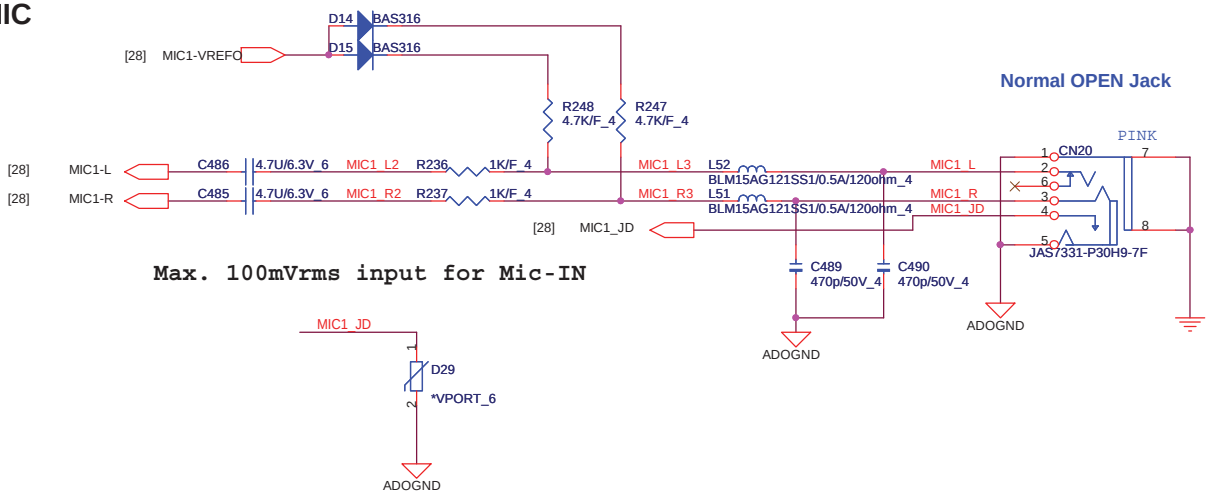
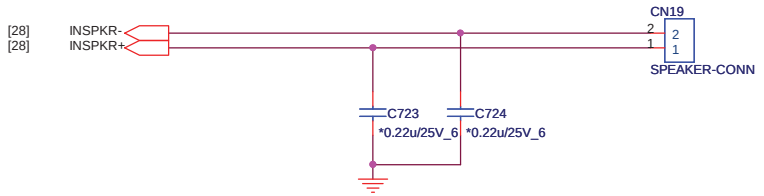
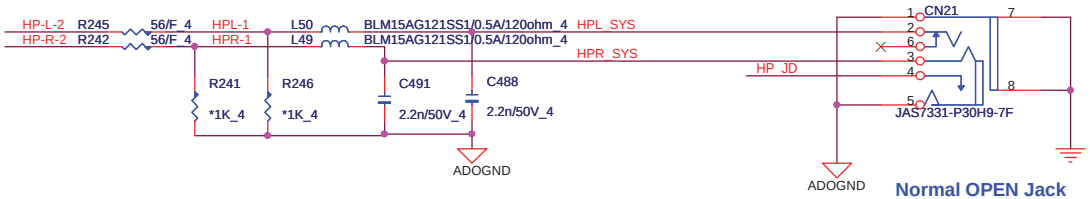
MIC

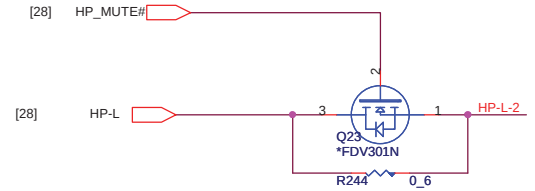


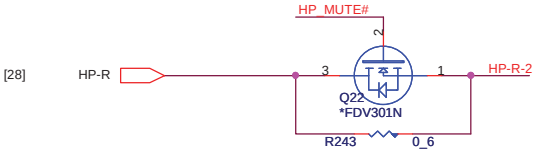
Internal Speaker

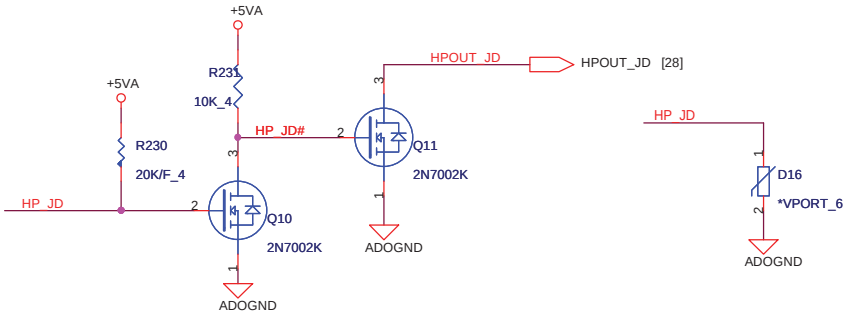


HP









PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	1A
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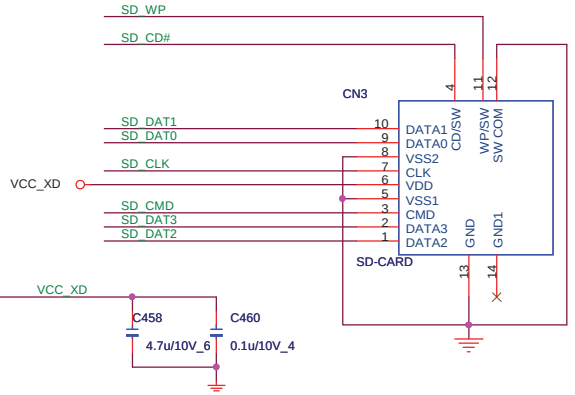
2 IN 1 CARD READER (MMC)

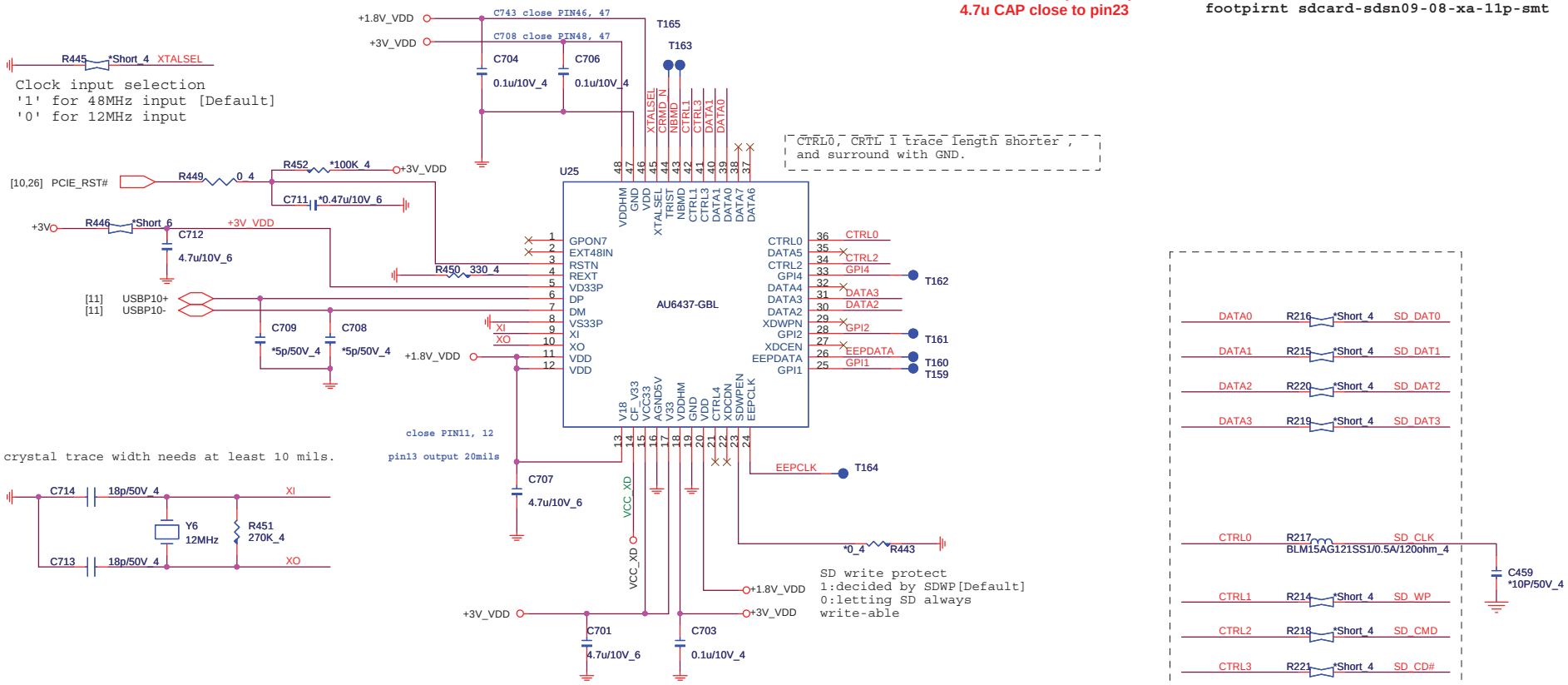
CARD READER Controller



Main	DFHS11FR011
Second	DFHS11FR033

Close to CNxx pin 14 & pin23
4.7u CAP close to pin23

5/10 change Card Redaer conn
footpirnt sdcard-sdsn09-08-xa-11p-smt



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	AU6433 CardReader	1A
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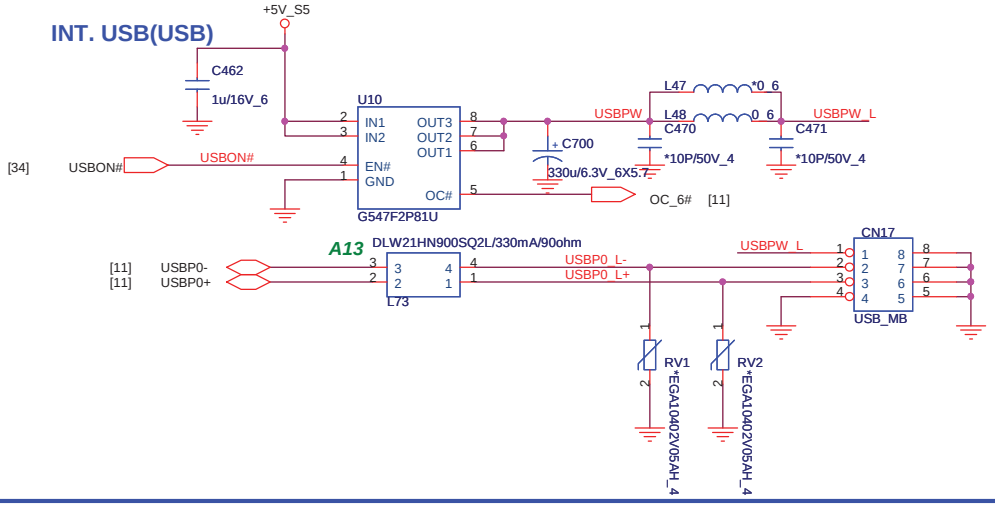
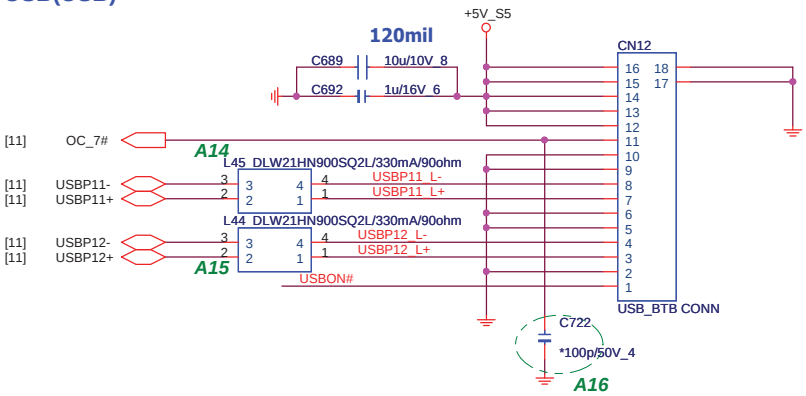
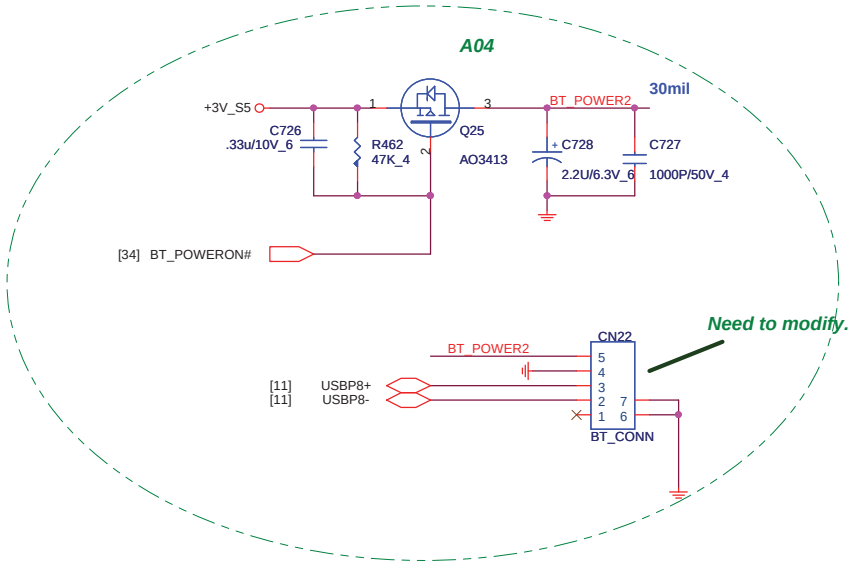
INT. USB(USB)



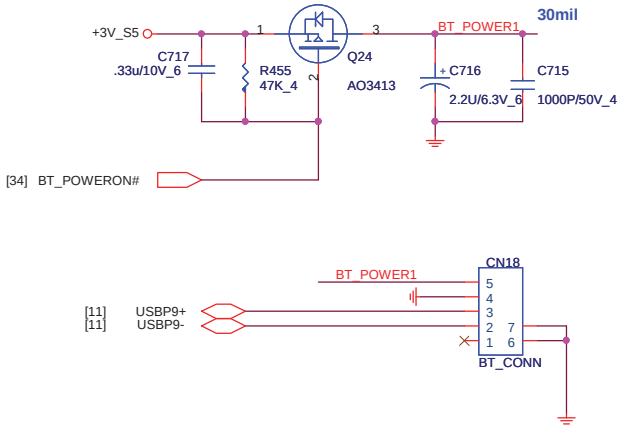
EXT. USB(USB)



BLUETOOTH V2.1 CONN(BTM)



BLUETOOTH V3.0 CONN(BTM)



PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number *USB/BT/TP*	Rev 1A
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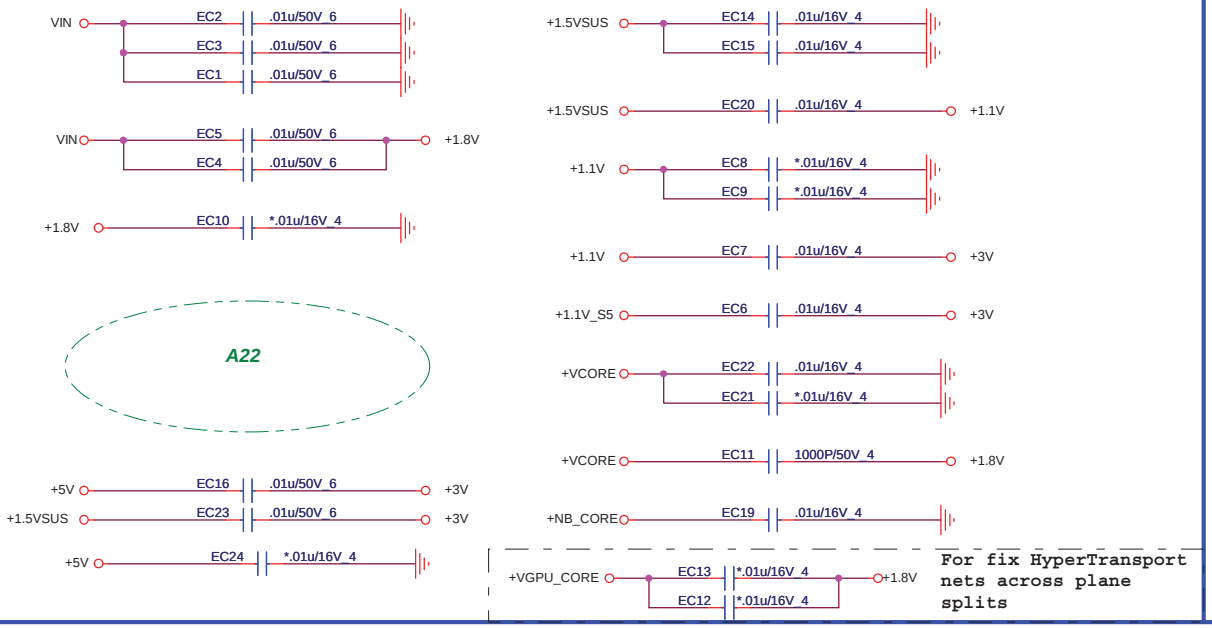
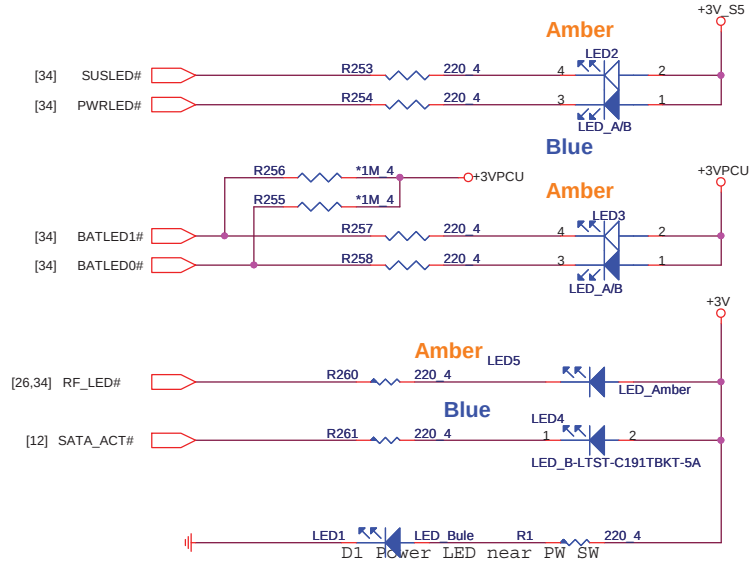
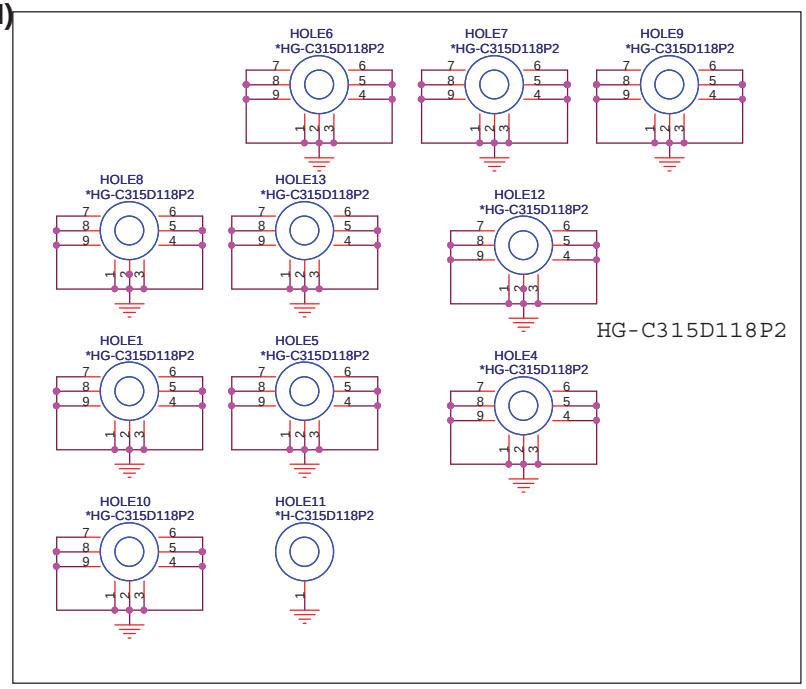
EE RETURN-PATH CAPACITORS(EMC)

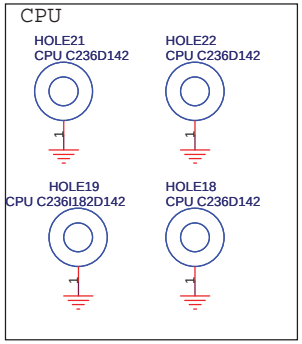


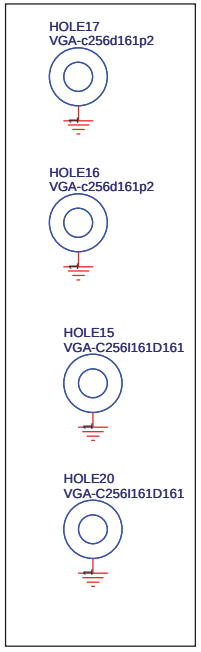
LED(UIF)

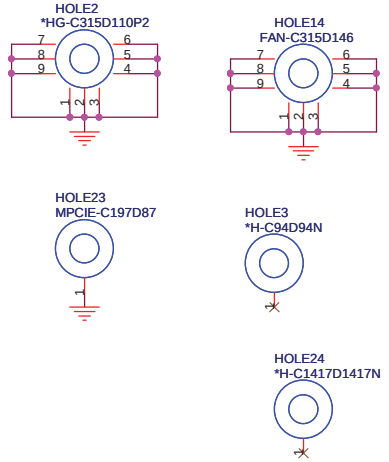


HOLE(OTH)









PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	POWER/USB/BT/TP/MDC	1A
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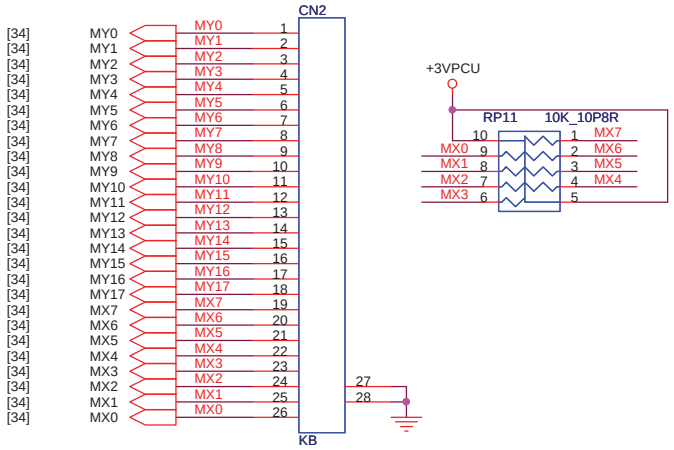
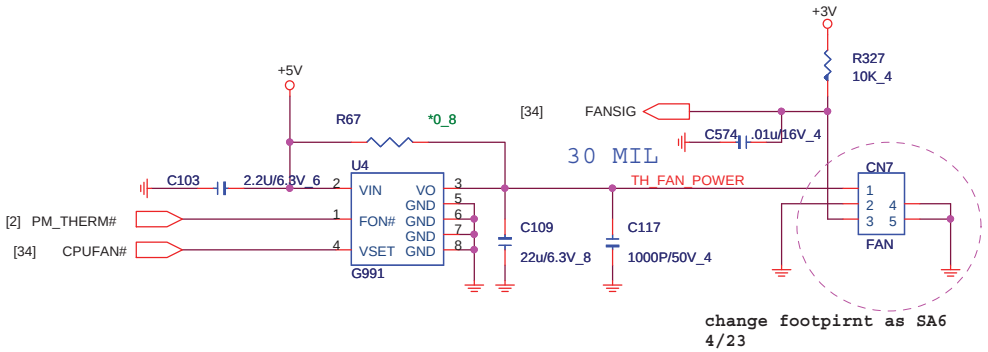
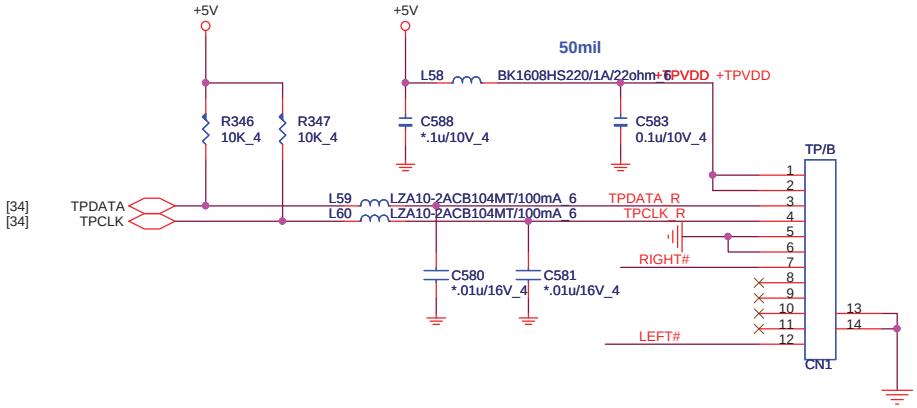
K/B(KBC)

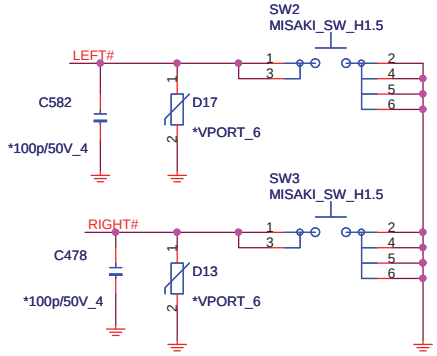


CPU FAN(THM)



TOUCHPAD BOARD CONN(TPD)





PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	KB/FAN/EE RETURN CAP	1A
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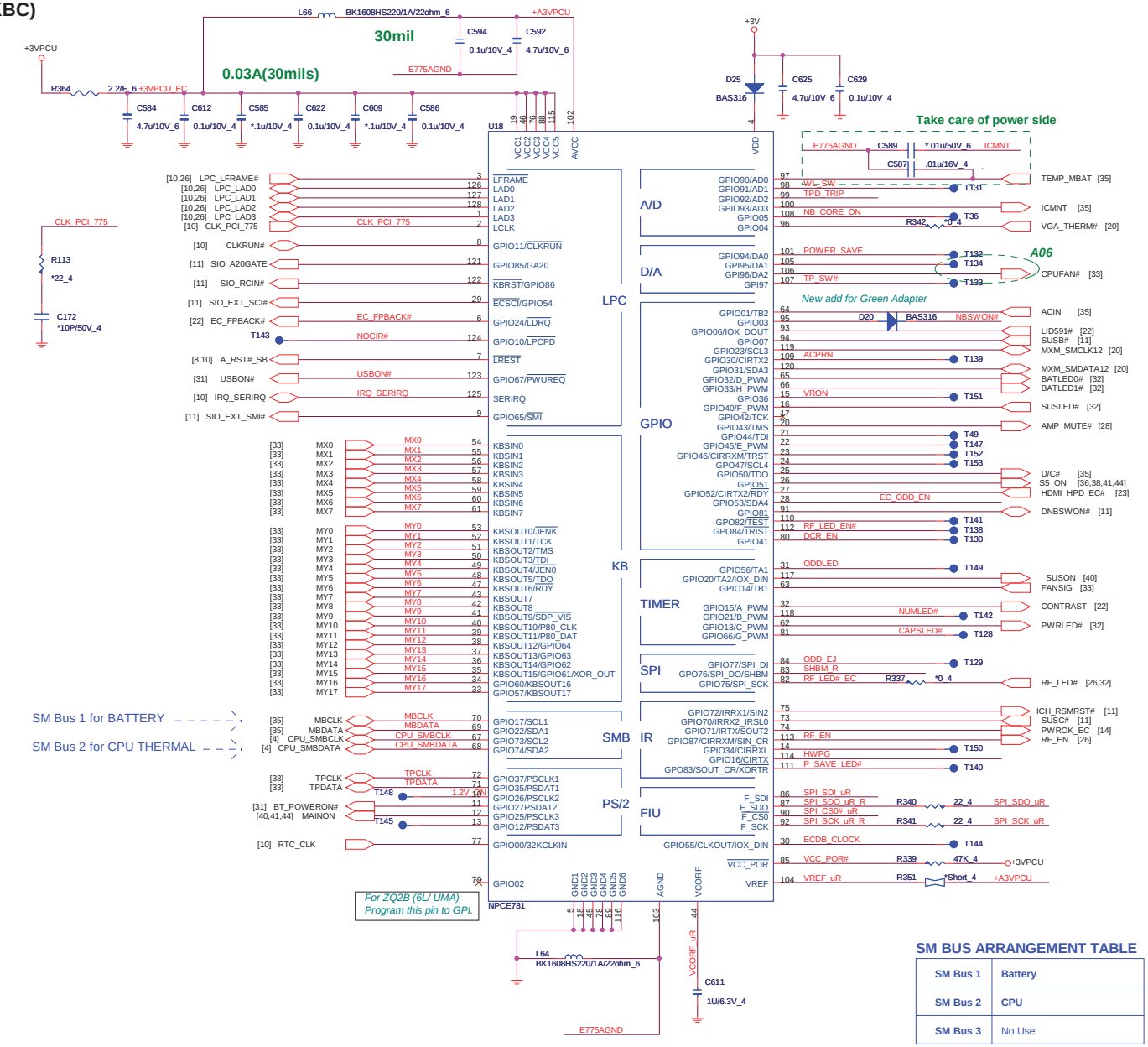
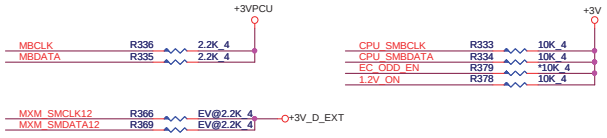
EC(KBC)



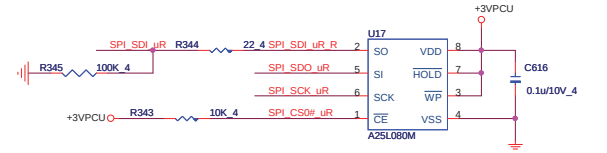
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	CPU
SM Bus 3	No Use

SM BUS PU(KBC)



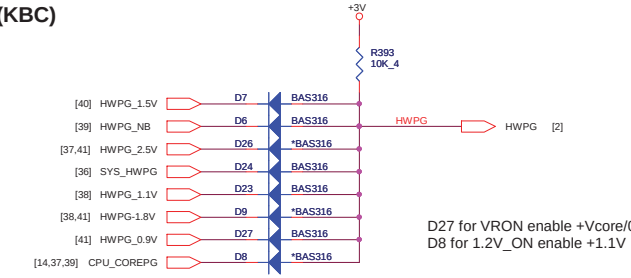
SPI FLASH(KBC)



If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

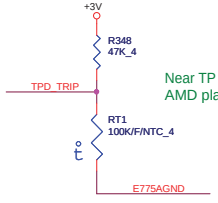
Winbond	W25X16AVSSIG	AKE38ZP0N01
MXIC	MX25L1605AM2C-15G	AKE37FP0Z13
EON	EN25F16-100HIP	AKE38ZA0Q00
AMIC	A25L016	AKE38ZN0800

HWPG(KBC)



D27 for VRON enable +Vcore/0.9V
D8 for 1.2V_ON enable +1.1V

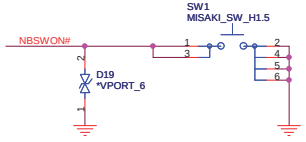
PALM REST THERMAL SENSOR (THM)



Near TP on TOP side and only for AMD platform Palm Rest use.

(02/25)
Per QSMC SMT request, change to Mitsubishi.
Main: CU4100B0000
Second: CU410000Z07 (MIT)

POWER-ON SWITCH (KBC)



POWER-ON SWITCH (KBC)

SHBM=0: Enable shared memory with host BIOS

Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	WPCE775C_0DG & FLASH	1A
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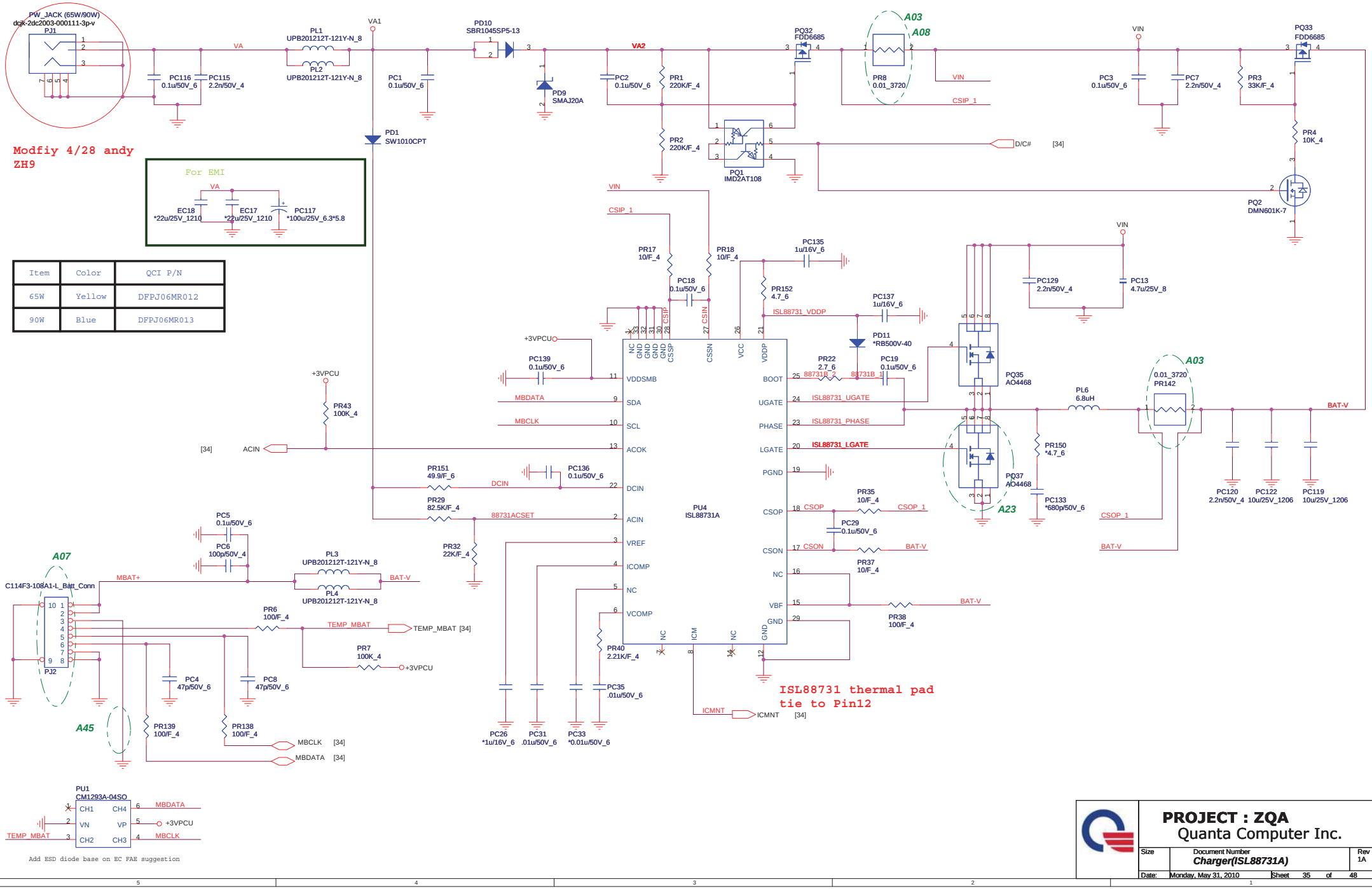
PW_JACK (65W/90W)
dcjk-2dc2003-000111-3p-v
PJ1
PC116 0.1u/50V_6
PC115 2.2n/50V_4
PL1 UPB201212T-121Y-N_8
PL2 UPB201212T-121Y-N_8
PD10 SBR1045SP5-13
PD9 SMAJ20A
PD1 SW1010CPT
PC1 0.1u/50V_6
PC2 0.1u/50V_6
PR1 220K/F_4
PR2 220K/F_4
PQ32 FDD6685
PQ1 IMD2AT108
PR8 0.01_3720
PC3 0.1u/50V_6
PC7 2.2n/50V_4
PR3 33K/F_4
PR4 10K_4
PQ33 FDD6685
PQ2 DMN601K-7
Modfiy 4/28 andy
ZH9
For EMI
EC18 *22u/25V_1210
EC17 *22u/25V_1210
PC117 *100u/25V_6.3*5.8
Item | Color | QCI P/N
65W | Yellow | DFPJ06MR012
90W | Blue | DFPJ06MR013
PR17 10/F_4
PR18 10/F_4
PC18 0.1u/50V_6
PR152 4.7_6
PC135 1u/16V_6
PC137 1u/16V_6
PD11 *RB500V-40
PC139 0.1u/50V_6
PR22 2.7_6
PC19 0.1u/50V_6
PU4 ISL88731A
PC129 2.2n/50V_4
PC13 4.7u/25V_8
PQ35 AO4468
PQ37 AO4468
PL6 6.8uH
PR150 *4.7_6
PC133 *680p/50V_6
PR142 0.01_3720
PC120 2.2n/50V_4
PC122 10u/25V_1206
PC119 10u/25V_1206
PR43 100K_4
PR151 49.9/F_6
PC136 0.1u/50V_6
PR29 82.5K/F_4
PR32 22K/F_4
PC5 0.1u/50V_6
PC6 100p/50V_4
PL3 UPB201212T-121Y-N_8
PL4 UPB201212T-121Y-N_8
PR35 10/F_4
PC29 0.1u/50V_6
PR37 10/F_4
PR38 100/F_4
PR40 2.21K/F_4
PC35 .01u/50V_6
PC26 *1u/16V_6
PC31 .01u/50V_6
PC33 *0.01u/50V_6
ISL88731 thermal pad
tie to Pin12
C114F3-108A1-L_Batt_Conn
PJ2
PR6 100/F_4
PR7 100K_4
PC4 47p/50V_6
PC8 47p/50V_6
PR139 100/F_4
PR138 100/F_4
PU1 CM1293A-04SO
Add ESD diode base on EC FAE suggestion
PROJECT : ZQA
Quanta Computer Inc.
Size
Document Number
Charger(ISL88731A)
Rev 1A
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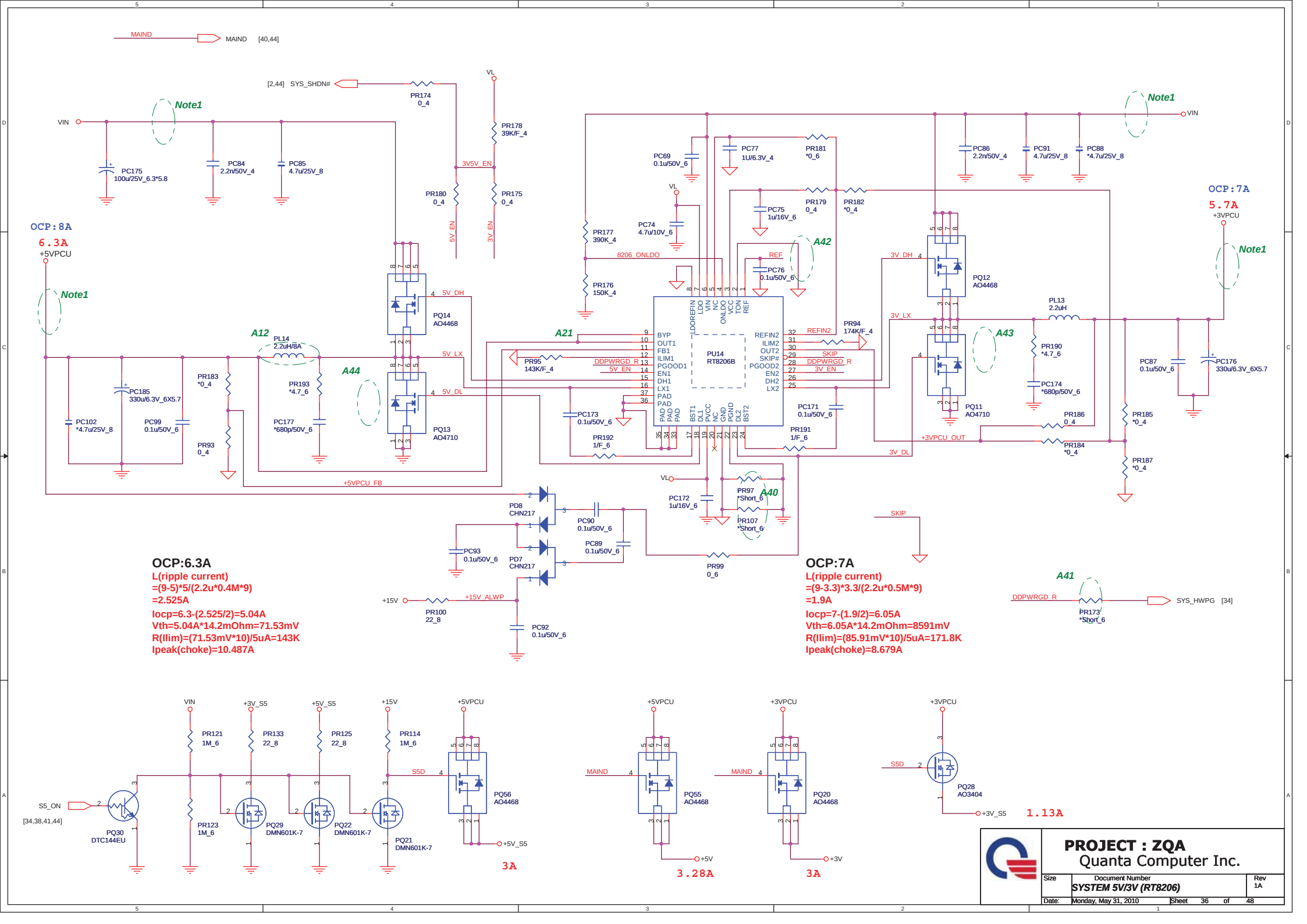

MAIND
MAIND [40,44]
[2,44] SYS_SHDN#
VIN
VL
Note1
PR174 0_4
PR178 39K/F_4
PR180 0_4
PR175 0_4
3V5V_EN
5V_EN
3V_EN
PC175 100u/25V_6.3*5.8
PC84 2.2n/50V_4
PC85 4.7u/25V_8
OCP:8A
6.3A
+5VPCU
PQ14 AO4468
PQ13 AO4710
5V_DH
5V_LX
5V_DL
A12
PL14 2.2uH/8A
A44
PC185 330u/6.3V_6X5.7
PC102 *4.7u/25V_8
PC99 0.1u/50V_6
PR183 *0_4
PR193 *4.7_6
PC177 *680p/50V_6
PR93 0_4
+5VPCU_FB
PR177 390K_4
PR176 150K_4
8206_ONLDO
PC69 0.1u/50V_6
PC74 4.7u/10V_6
PC77 1U/6.3V_4
PR181 *0_6
PR179 0_4
PR182 *0_4
PC75 1u/16V_6
REF
PC76 0.1u/50V_6
A42
A21
PU14 RT8206B
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
LDOREFIN
LDO
VIN
NC
ONLDO
VCC
TON
REF
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
BST1
PVCC
GND
PGND
DL2
BST2
PR95 143K/F_4
DDPWRGD_R
PR94 174K/F_4
REFIN2
SKIP
PC173 0.1u/50V_6
PC171 0.1u/50V_6
PR192 1/F_6
PR191 1/F_6
PC172 1u/16V_6
PR97 *Short_6
PR107 *Short_6
A40
PD8 CHN217
PD7 CHN217
PC90 0.1u/50V_6
PC89 0.1u/50V_6
PC93 0.1u/50V_6
PC92 0.1u/50V_6
PR99 0_6
+15V
+15V_ALWP
PR100 22_8
SKIP
OCP:6.3A
L(ripple current)
=(9-5)*5/(2.2u*0.4M*9)
=2.525A
Iocp=6.3-(2.525/2)=5.04A
Vth=5.04A*14.2mOhm=71.53mV
R(Ilim)=(71.53mV*10)/5uA=143K
Ipeak(choke)=10.487A
OCP:7A
L(ripple current)
=(9-3.3)*3.3/(2.2u*0.5M*9)
=1.9A
Iocp=7-(1.9/2)=6.05A
Vth=6.05A*14.2mOhm=8591mV
R(Ilim)=(85.91mV*10)/5uA=171.8K
Ipeak(choke)=8.679A
OCP:7A
5.7A
+3VPCU
PQ12 AO4468
PQ11 AO4710
3V_DH
3V_LX
3V_DL
A43
PL13 2.2uH
PR190 *4.7_6
PC174 *680p/50V_6
PR186 0_4
PR184 *0_4
+3VPCU_OUT
PC87 0.1u/50V_6
PC176 330u/6.3V_6X5.7
PR185 *0_4
PR187 *0_4
PC86 2.2n/50V_4
PC91 4.7u/25V_8
PC88 *4.7u/25V_8
A41
DDPWRGD_R
PR173 *Short_6
SYS_HWPG [34]
VIN
+3V_S5
+5V_S5
+15V
+5VPCU
PR121 1M_6
PR133 22_8
PR125 22_8
PR114 1M_6
S5D
S5_ON
[34,38,41,44]
PQ30 DTC144EU
PR123 1M_6
PQ29 DMN601K-7
PQ22 DMN601K-7
PQ21 DMN601K-7
PQ56 AO4468
+5V_S5
3A
MAIND
PQ55 AO4468
+5V
3.28A
PQ20 AO4468
+3V
3A
+3VPCU
PQ28 AO3404
+3V_S5
1.13A
PROJECT : ZQA
Quanta Computer Inc.
Size
Document Number
SYSTEM 5V/3V (RT8206)
Rev 1A
Date: Monday, May 31, 2010
Sheet 36 of 48

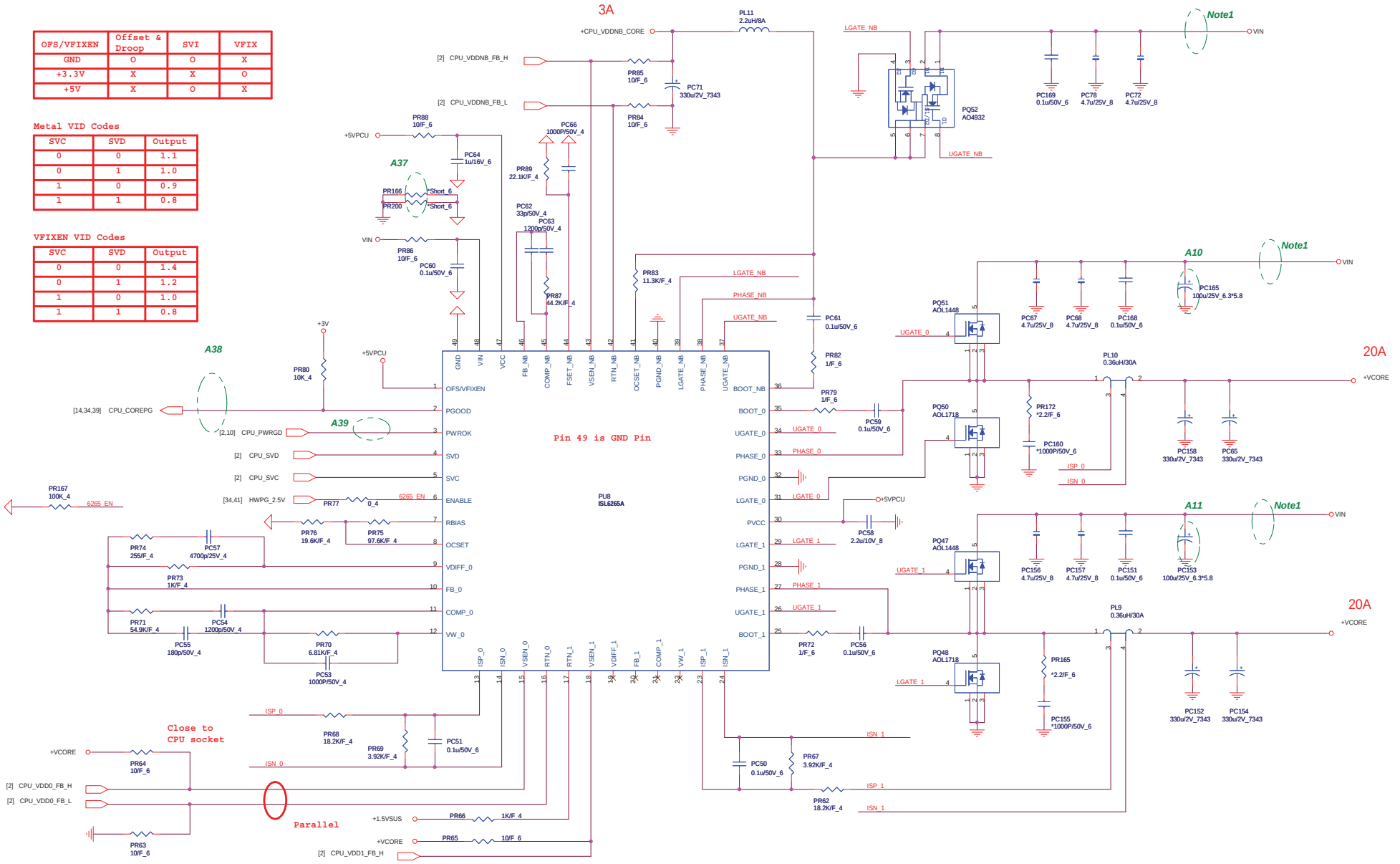
OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	O	O	X
+3.3V	X	X	O
+5V	X	O	X

Metal VID Codes

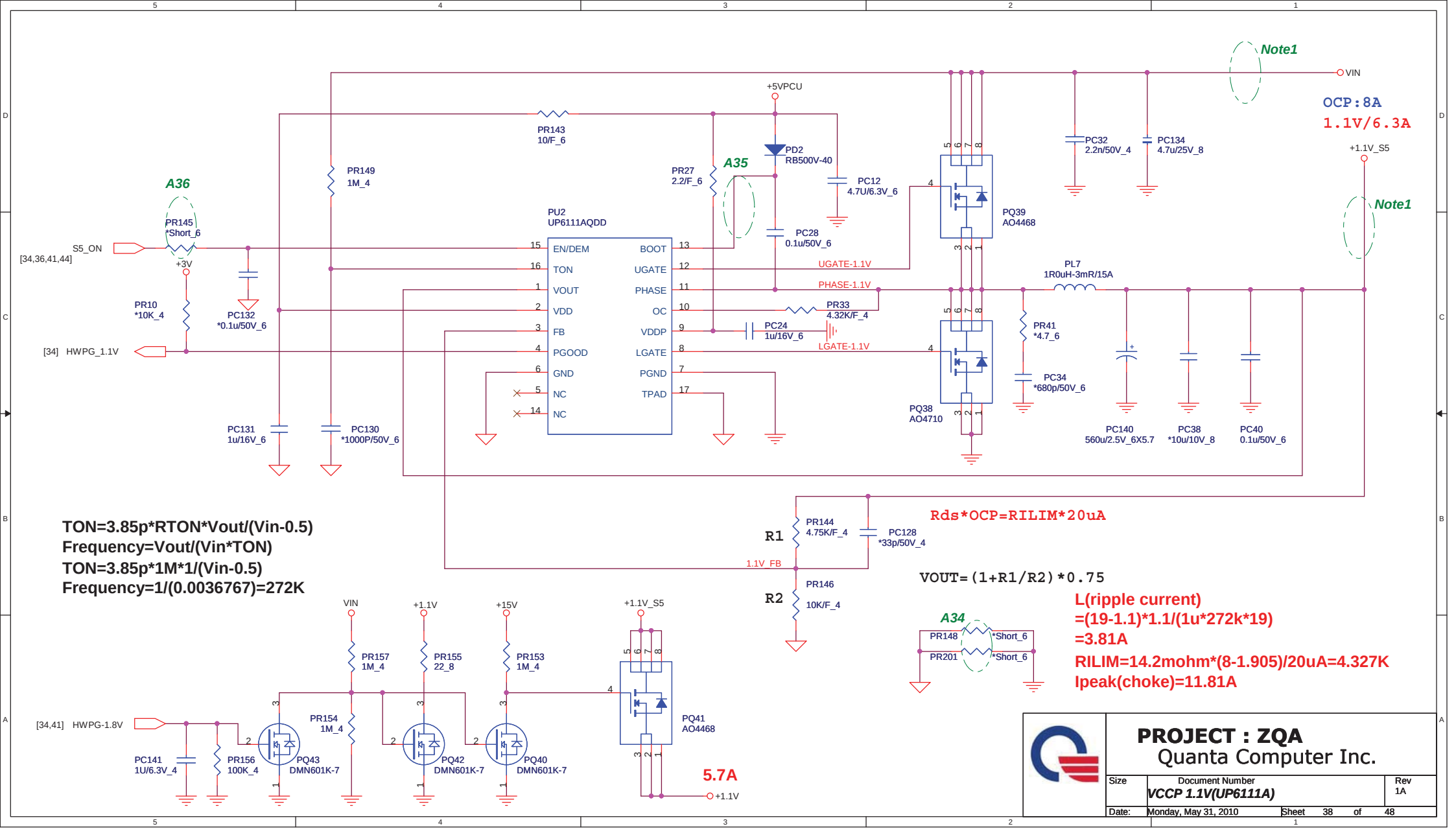
SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

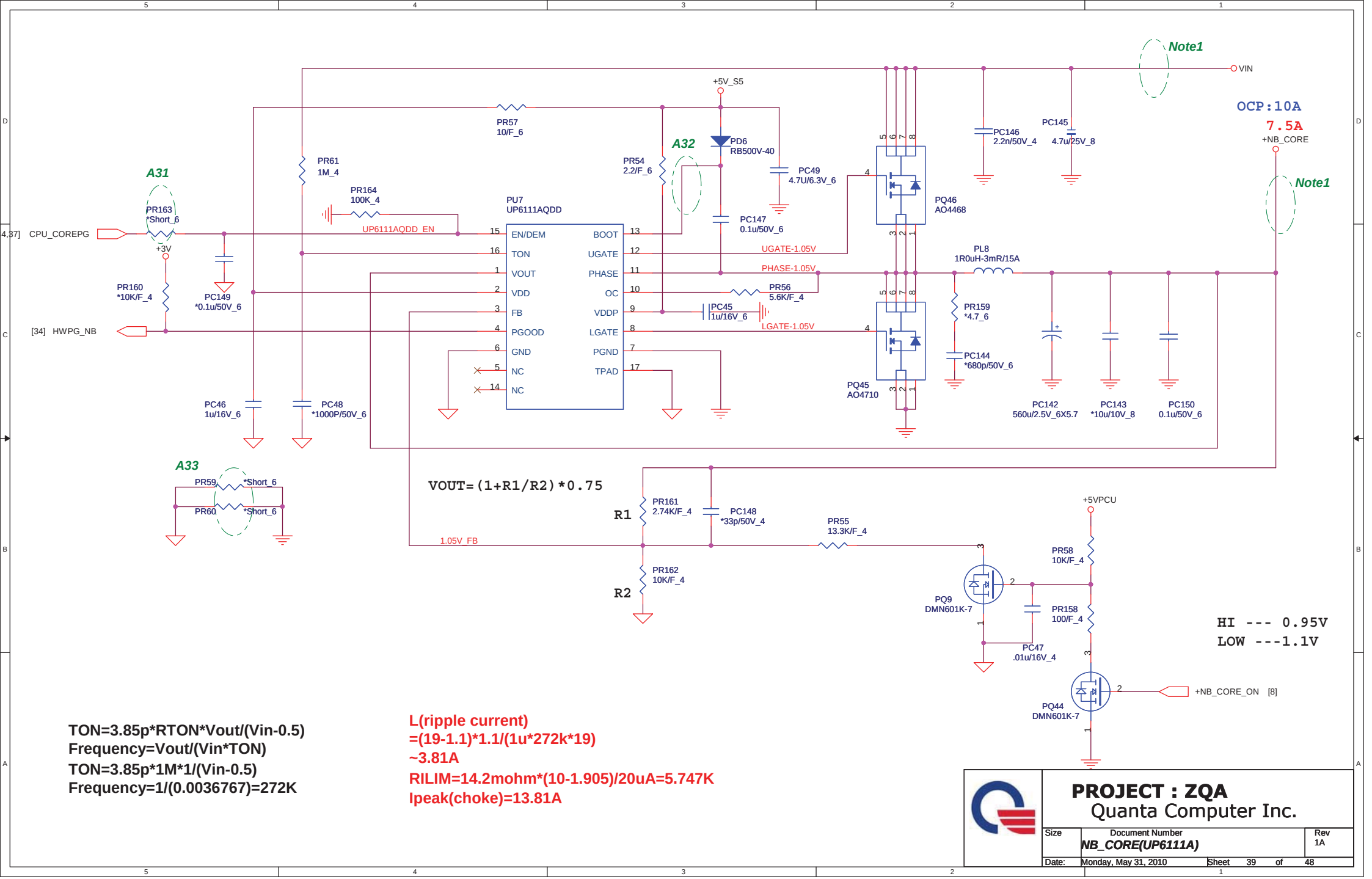
VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8



	PROJECT : ZQA Quanta Computer Inc.		
Size	Document Number: *CPU Core (ISL6265)*		Rev 1A
Date: Monday, May 31, 2010	Sheet 37 of 48		


Note1
VIN
OCP:8A
1.1V/6.3A
+5VPCU
PR143
10/F_6
PD2
RB500V-40
PC12
4.7U/6.3V_6
PC32
2.2n/50V_4
PC134
4.7u/25V_8
+1.1V_S5
Note1
A36
A35
PR149
1M_4
PR27
2.2/F_6
PU2
UP6111AQDD
PR145
*Short_6
S5_ON
[34,36,41,44]
+3V
PR10
*10K_4
PC132
*0.1u/50V_6
[34] HWPG_1.1V
EN/DEM
TON
VOUT
VDD
FB
PGOOD
GND
NC
NC
BOOT
UGATE
PHASE
OC
VDDP
LGATE
PGND
TPAD
UGATE-1.1V
PHASE-1.1V
LGATE-1.1V
PC28
0.1u/50V_6
PR33
4.32K/F_4
PC24
1u/16V_6
PQ39
AO4468
PQ38
AO4710
PL7
1R0uH-3mR/15A
PR41
*4.7_6
PC34
*680p/50V_6
PC140
560u/2.5V_6X5.7
PC38
*10u/10V_8
PC40
0.1u/50V_6
PC131
1u/16V_6
PC130
*1000P/50V_6
TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K
R1
PR144
4.75K/F_4
PC128
*33p/50V_4
1.1V_FB
R2
PR146
10K/F_4
Rds*OCP=RILIM*20uA
VOUT=(1+R1/R2)*0.75
A34
PR148
*Short_6
PR201
*Short_6
L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
=3.81A
RILIM=14.2mohm*(8-1.905)/20uA=4.327K
Ipeak(choke)=11.81A
VIN
+1.1V
+15V
+1.1V_S5
PR157
1M_4
PR155
22_8
PR153
1M_4
PR154
1M_4
[34,41] HWPG-1.8V
PC141
1U/6.3V_4
PR156
100K_4
PQ43
DMN601K-7
PQ42
DMN601K-7
PQ40
DMN601K-7
PQ41
AO4468
5.7A
+1.1V
PROJECT : ZQA
Quanta Computer Inc.
Size
Document Number
VCCP 1.1V(UP6111A)
Rev
1A
Date: Monday, May 31, 2010
Sheet 38 of 48

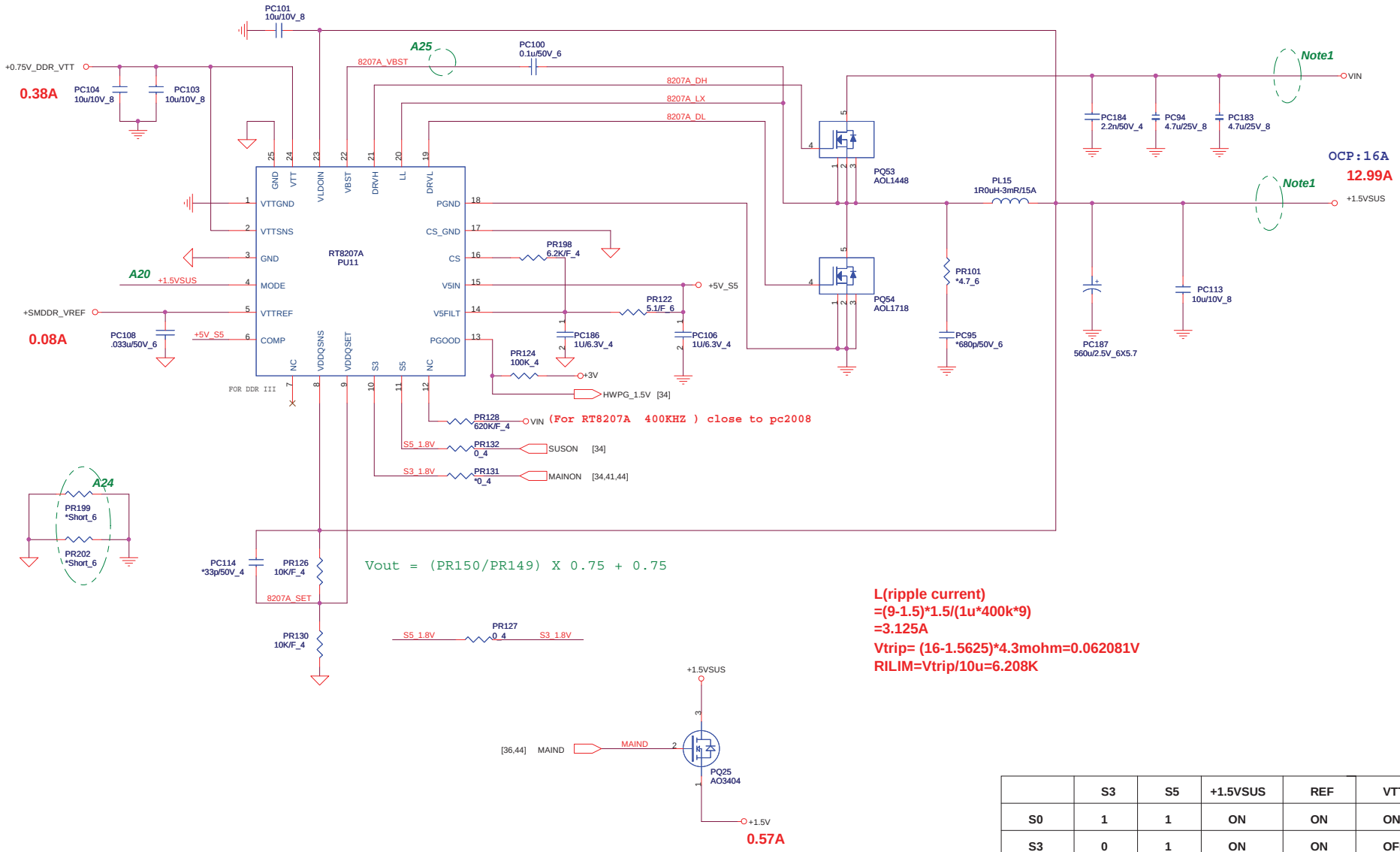


TON=3.85p*RTON*Vout/(Vin-0.5)
Frequency=Vout/(Vin*TON)
TON=3.85p*1M*1/(Vin-0.5)
Frequency=1/(0.0036767)=272K

L(ripple current)
=(19-1.1)*1.1/(1u*272k*19)
~3.81A
RILIM=14.2mohm*(10-1.905)/20uA=5.747K
Ipeak(choke)=13.81A

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	NB_CORE(UP6111A)	1A
Date: Monday, May 31, 2010	Sheet 39 of 48	

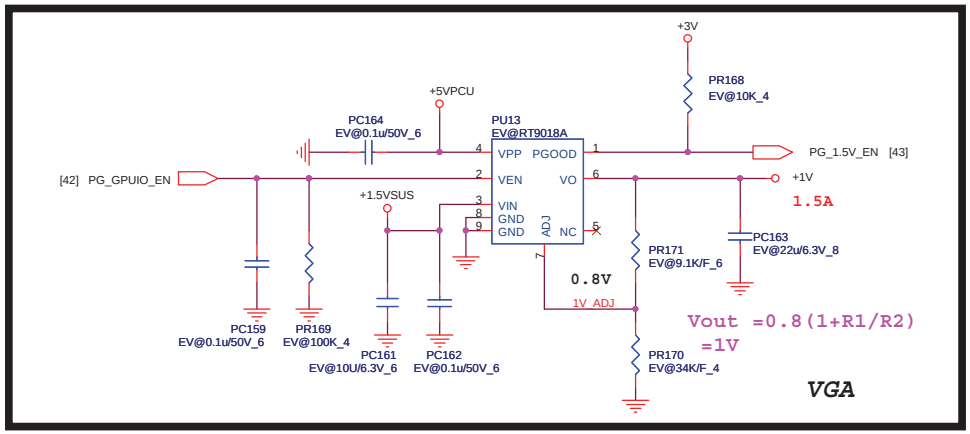


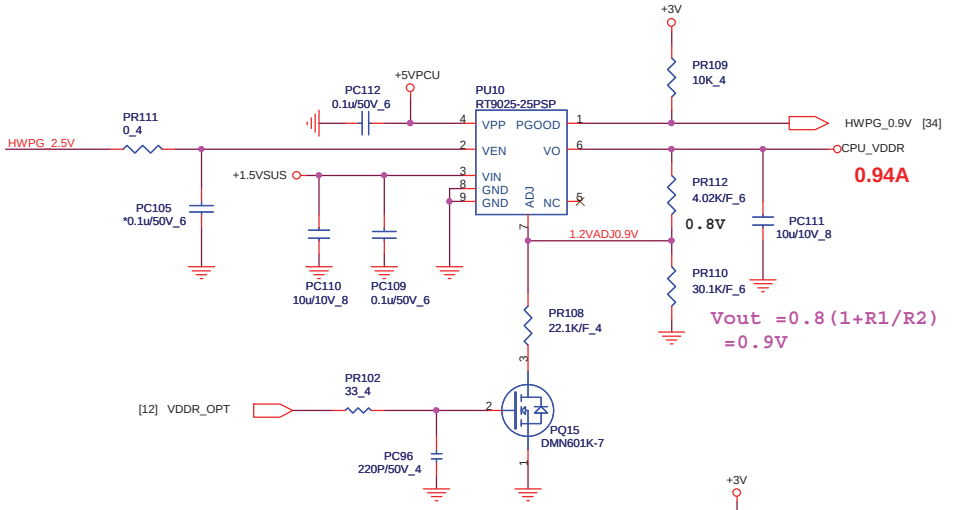
L(ripple current)
=(9-1.5)*1.5/(1u*400k*9)
=3.125A
Vtrip= (16-1.5625)*4.3mohm=0.062081V
RILIM=Vtrip/10u=6.208K

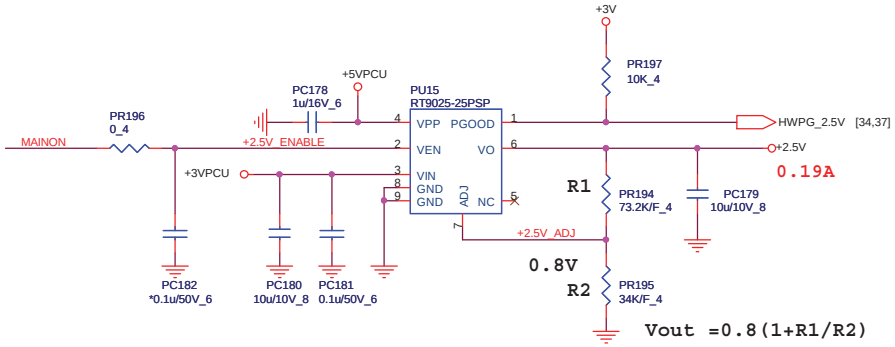
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF

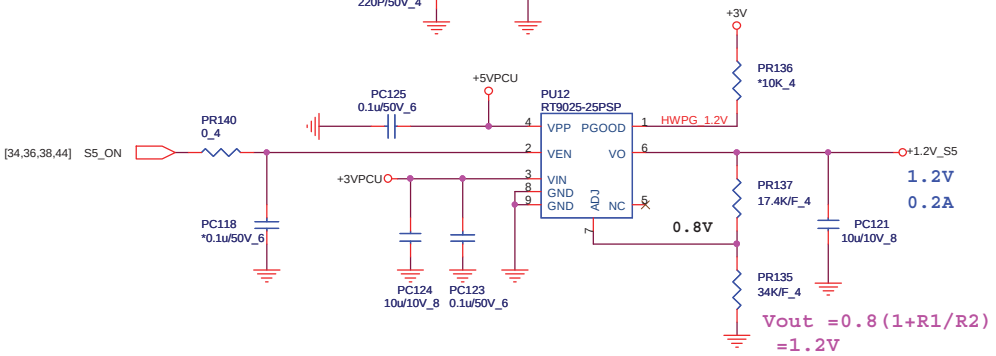
PROJECT : ZQA
Quanta Computer Inc.

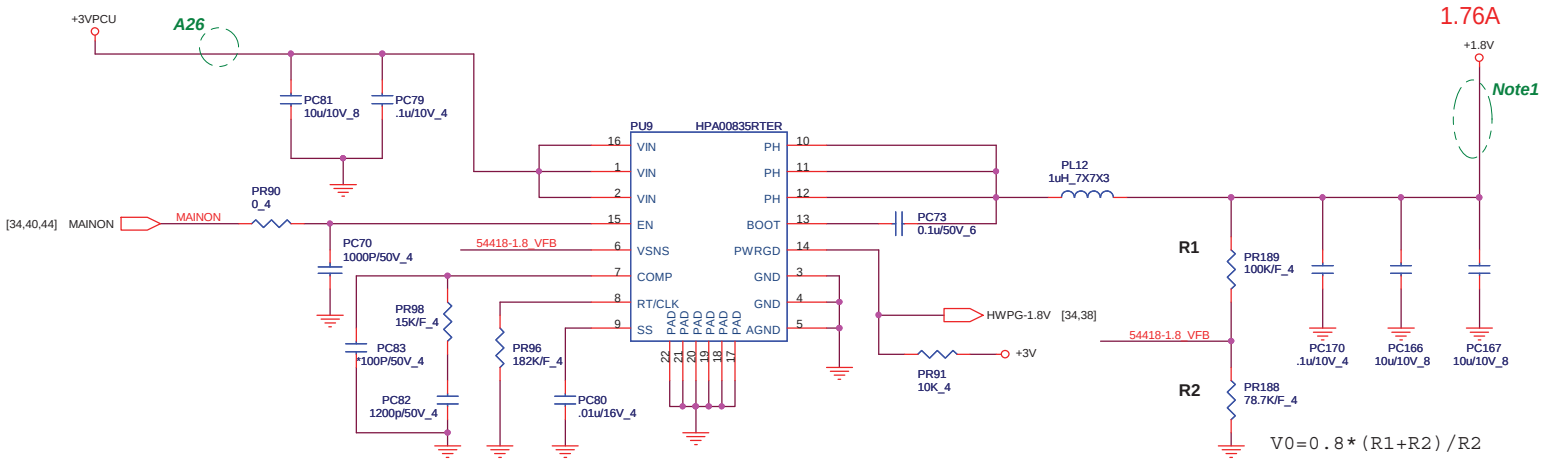
Size	Document Number	Rev
	DDR 1.5V(TPS51116)	1A
Date: Monday, May 31, 2010	Sheet 40 of 48	





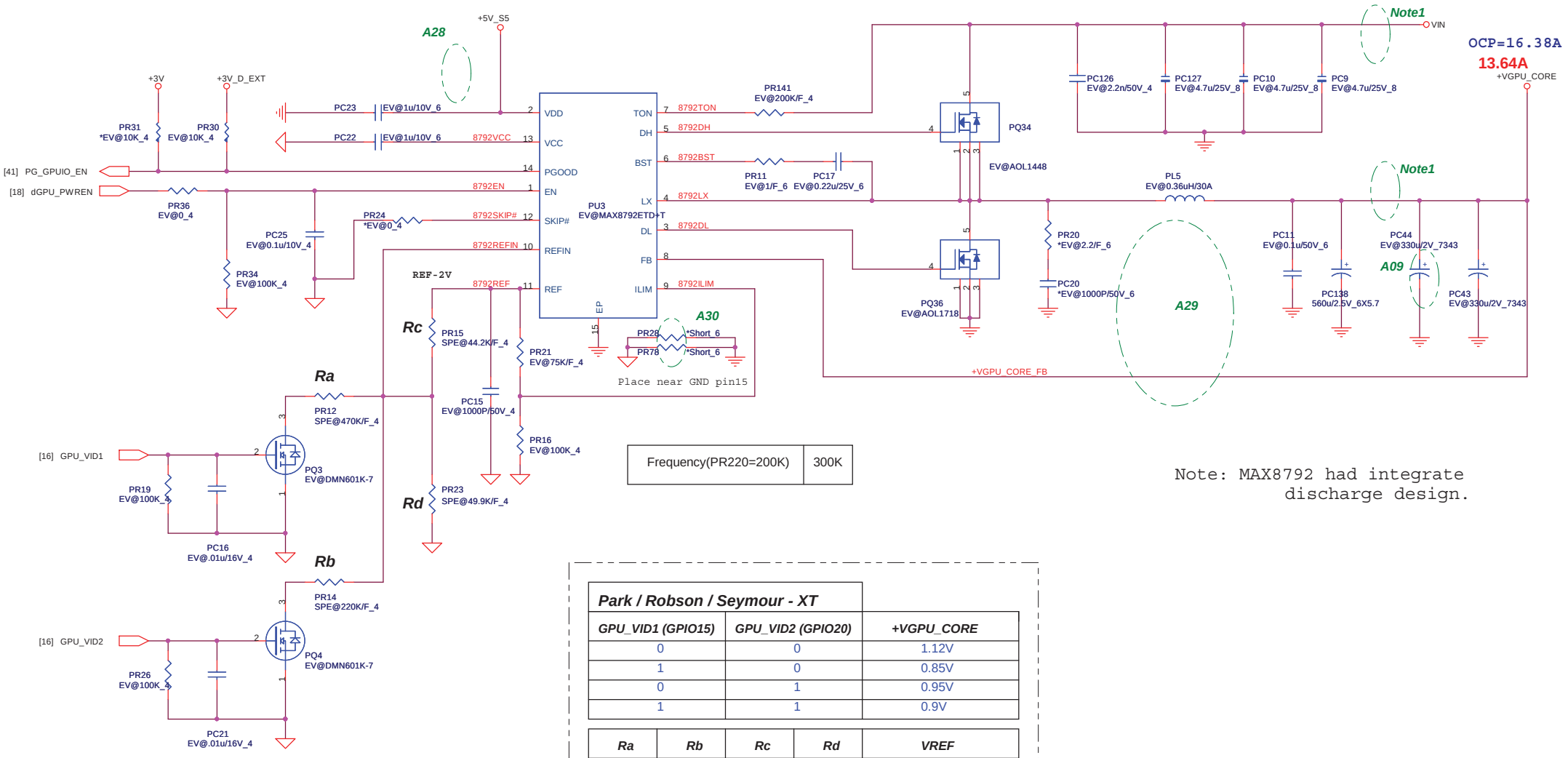






PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	LDO	1A
Date: Monday, May 31, 2010	Sheet 41 of 48	



Frequency(PR220=200K)	300K

Note: MAX8792 had integrate discharge design.

Park / Robson / Seymour - XT

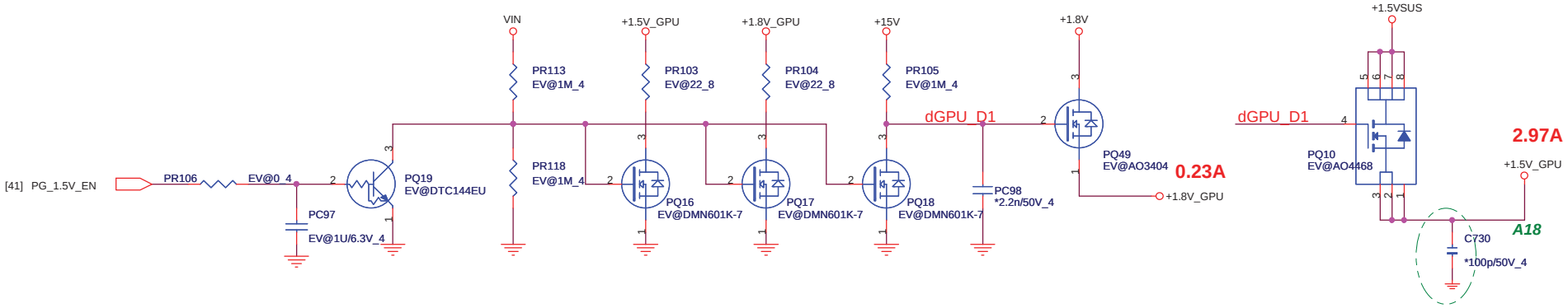
GPU_VID1 (GPIO15)	GPU_VID2 (GPIO20)	+VGPU_CORE
0	0	1.12V
1	0	0.85V
0	1	0.95V
1	1	0.9V

Ra	Rb	Rc	Rd	VREF
332K	130K	39.2K	49.9K	2V

Rc --> 39.2K/F_4 (CS33922FB15)
Ra --> 332K/F_4 (CS43322FB15)
Rb --> 130K/F_4 (CS41302FB00)

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	GPU CORE(MAX8792)	1A
Date: Monday, May 31, 2010	Sheet 42 of 48	

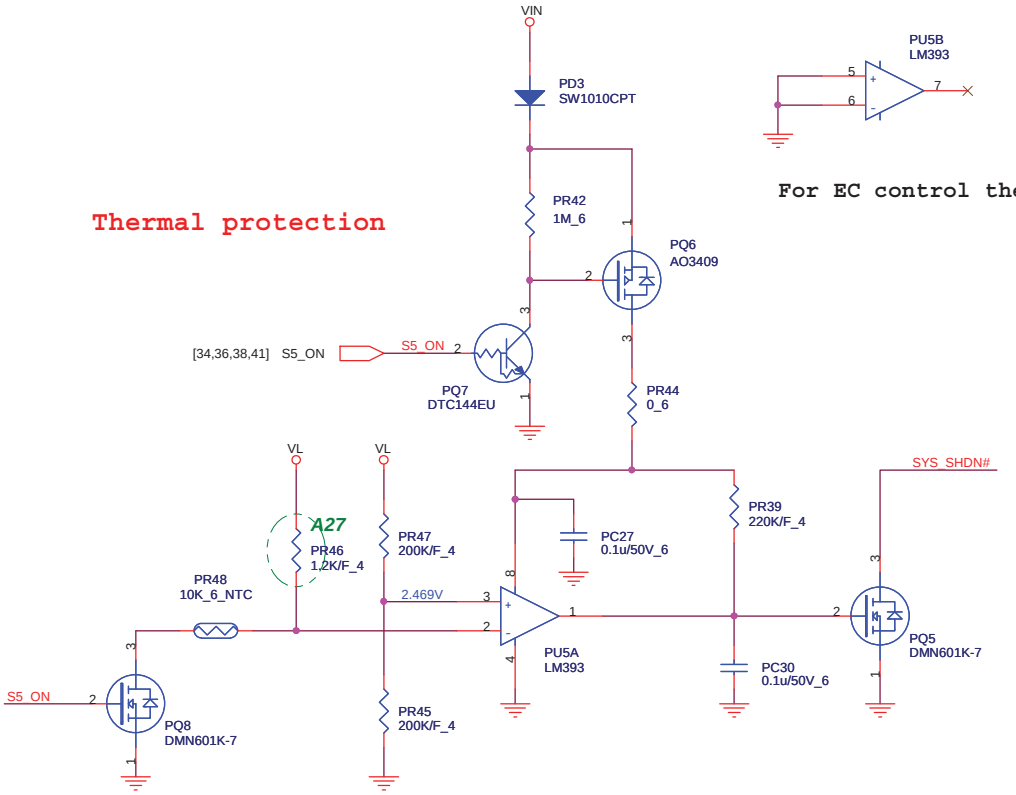


PROJECT : ZQA

Quanta Computer Inc.

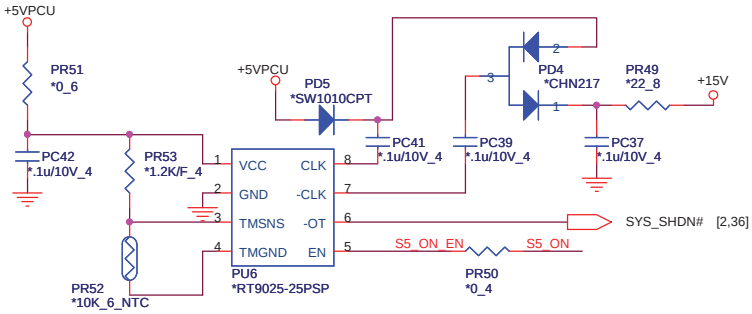
Size	Document Number	Rev
	GPU POWER	1A
Date: Monday, May 31, 2010	Sheet 43 of 48	

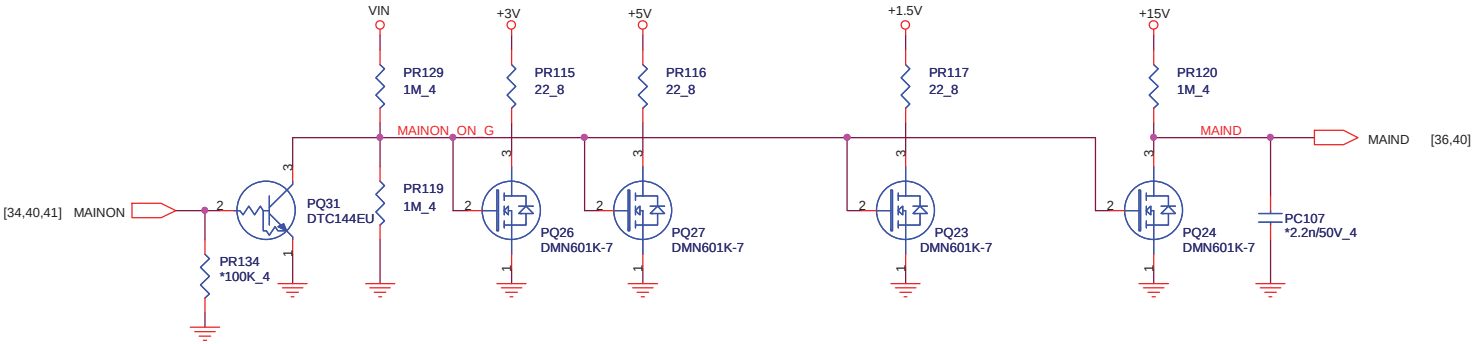
Thermal protection



For EC control thermal protection (output 3.3V)

POWER TEST : Thermal & Charge pump test circuit





PROJECT : ZQA
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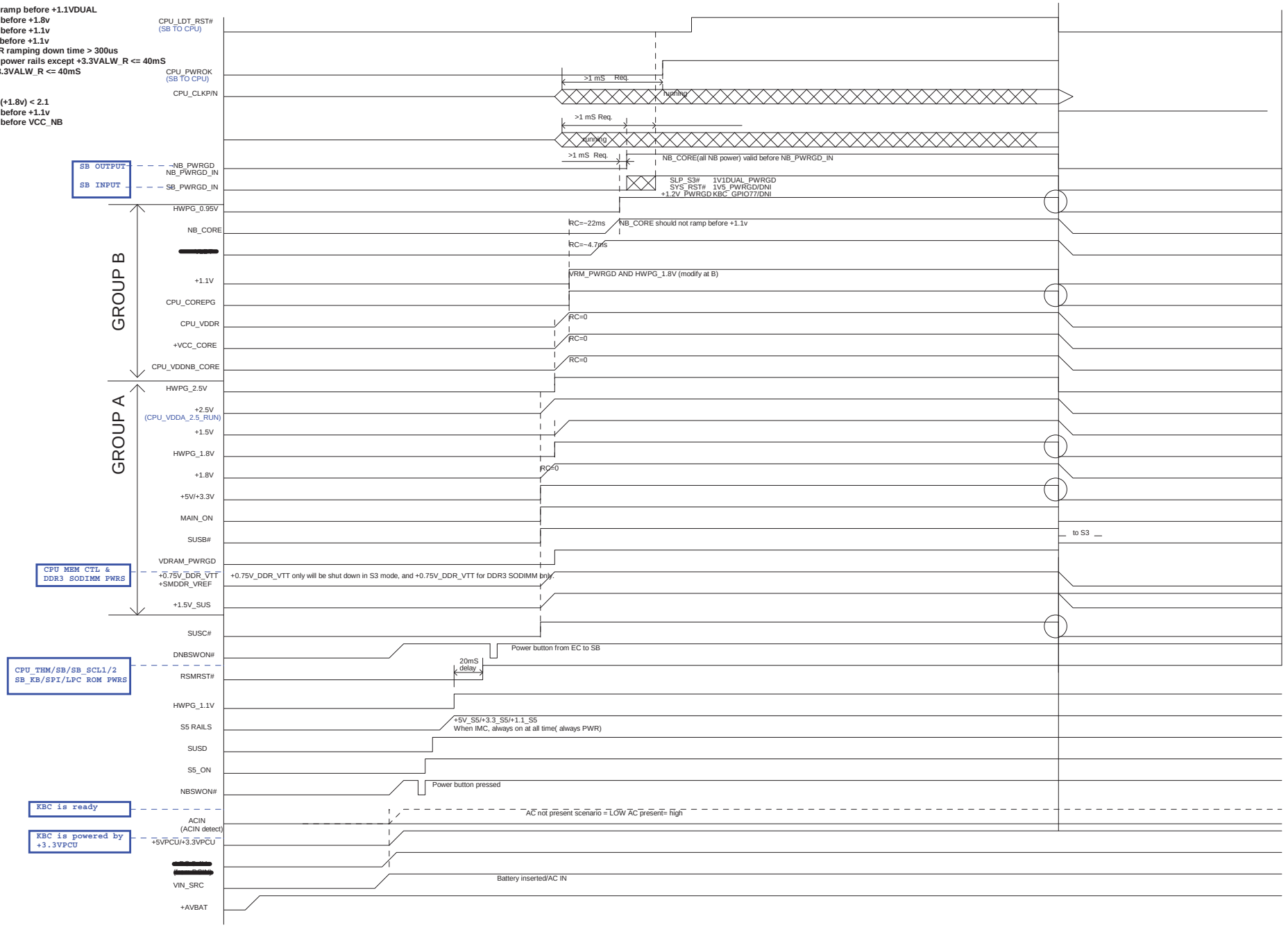
Size	Document Number	Rev
	Thermal protect	1A
Date: Monday, May 31, 2010	Sheet 44 of 48	

Power on Sequence required:

SB800:
1, +3.3VDUAL ramp before +1.1VDUAL
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

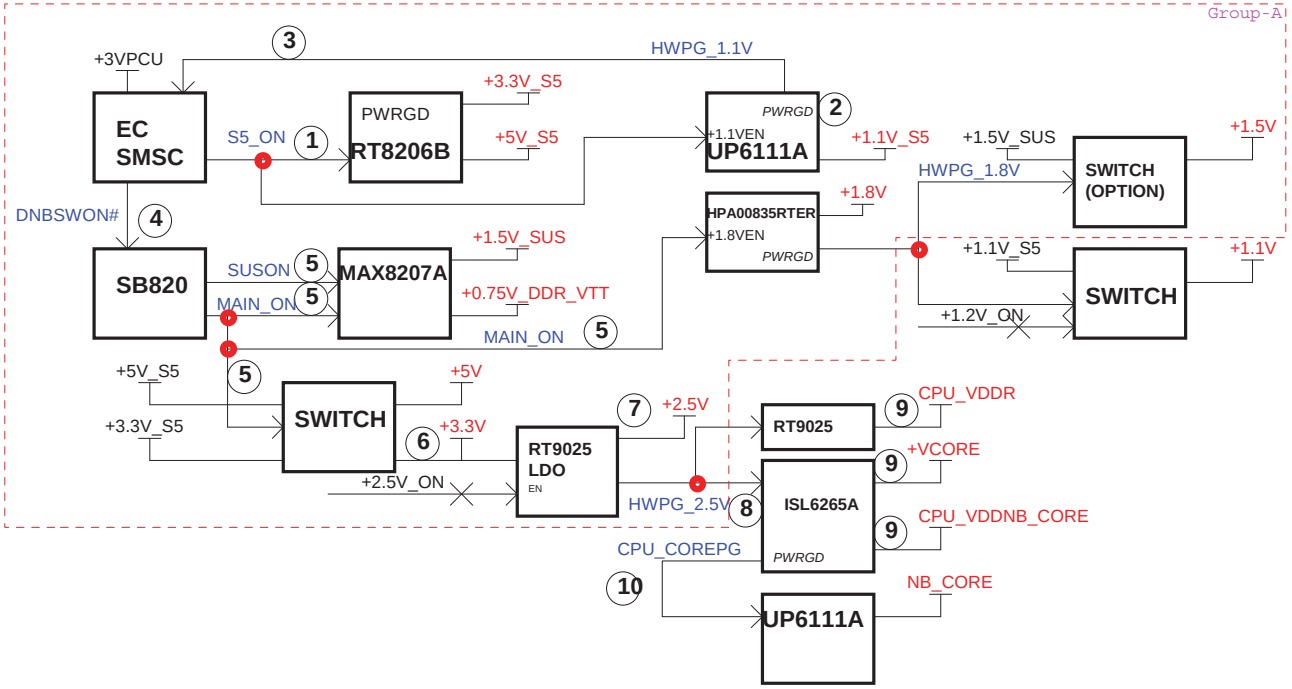
RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	Power Squence Chart	1A

Date: Monday, May 31, 2010 Sheet 45 of 48

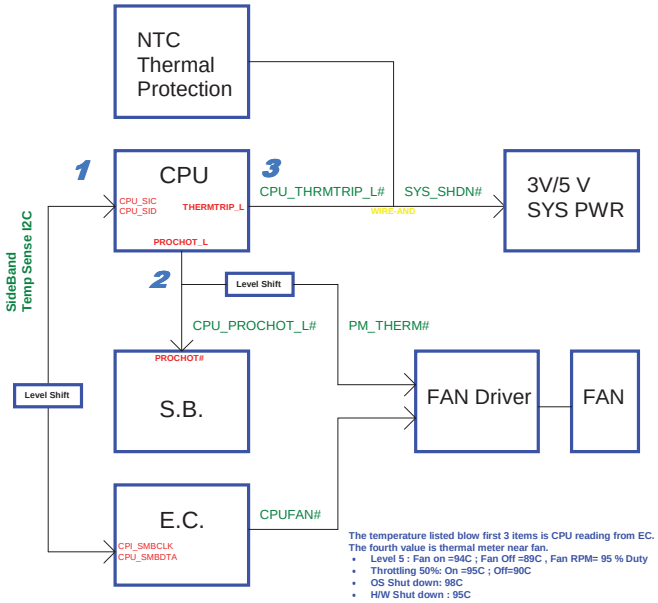


Power on Sequence required:

SB800:
1, +3.3V_S5 ramp before +1.1_S5
2, +3.3V ramp before +1.8v
3, +1.8V ramp before +1.1v
4, +3.3v ramp before +1.1v
5, +3.3VALW_R ramping down time > 300us
6, 50uS <= All power rails except +3.3VALW_R <= 40mS
7, 100uS <= +3.3VALW_R <= 40mS

RS880:
1, 0 <(+3.3V) - (+1.8v) < 2.1
2, +1.8V ramp before +1.1v
3. +1.1V ramp before VCC_NB

H/W Thermal Follow Chart



POWER RAILS Sequencing

1	S5_ON	13	+1.8V
2	+3.3V_S5	14	HWPG_1.8V
3	+5V_S5	15	+1.5V
4	+1.1V_S5	16	+2.5V
5	HWPG_1.1V	17	HWPG_2.5V
6	DNBSWON#	18	CPU_VDDNB_CORE
7	SUSON	19	+VCC_CORE
8	+1.5V_SUS	20	CPU_VDDR
9	+SMDDR_VTERM	21	CPU_COREPG
10	MAIN_ON	22	+1.1V
11	+5V	23	NB_CORE
12	+3.3V	24	

SB820 Sequencing

1	+3.3V_S5
2	ICH_RSMRST#
3	S0 POWER
4	PCIE_RCLKP/N
5	PCICLK[4:0]
6	SB_PWRGD_IN
7	NB_PWRGD_IN
8	LDT_PG
9	KBRST#
10	A_RST#
11	PCIRST#
12	LDT_RST#

RS880 Sequencing

1	+3.3V
2	NB POWER RAILS
3	ATX PS_PWRGD
4	NB INPUT CLOCKS
5	CPUCLK
6	NB_PWRGD
7	SB_PWRGD
8	LDT_PG/CPU_PWRGD
9	PCIRST#,NB_RST#
10	LDT_RST#
11	
12	

EC Sequencing

1	3VPCU
2	NBSWON#
3	VIN_ON
4	S5_ON
5	ICH_RSMRST#
6	-DNBSWON#
7	SUSB#/SUSC#
8	SUSON/USB_ON#
9	MAIN_ON/HWPG
10	VRON
11	PWROK
12	

PROJECT : ZQA
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Size	Document Number	Rev
	PWR ON SEQ and THERM POLICY	1A
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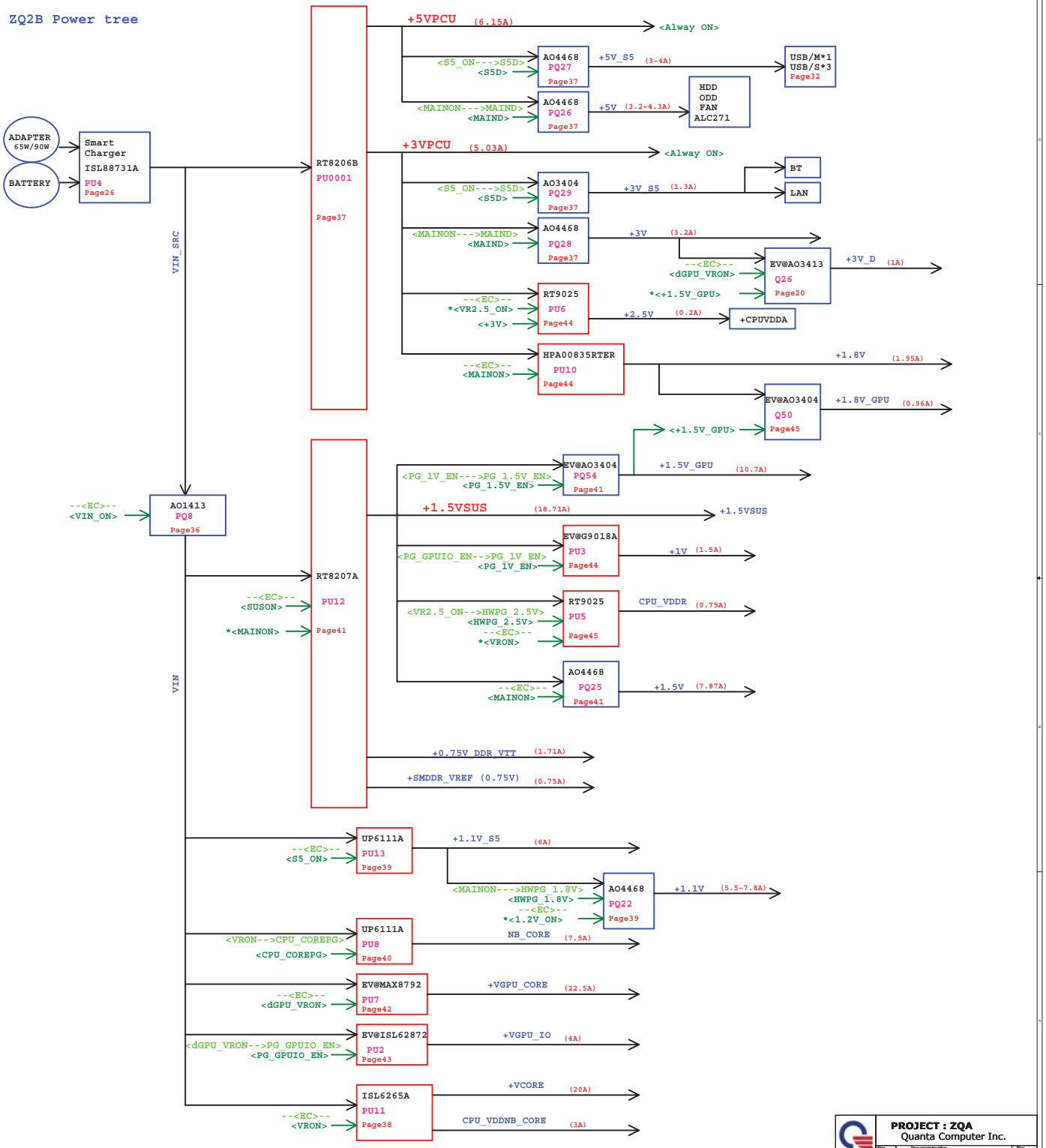
ZQ2B Power tree



PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
	Power Tree	1A

Date: Monday, May 31, 2010 Sheet 47 of 48

MODEL	REV
ZQA M/B	3A

CHANGE LIST

A01 PAGE28 : Add pull high resistor 4.7kohm on PD# pin, the reason is prevent speaker no sound.
A02 PAGE28 : Change R229,R223 to 33K for speaker 1W.
A03 PAGE35 : Change PR8,PR142 from 1m ohm to 10m ohm.
A04 PAGE31 : Add BT2.1 design for Customer request.
A05 PAGE22 : Delete R8 bead.
A06 PAGE34 : The connection of CPUFAN# is changed from 105pin to 106pin.
A07 PAGE35 : Change P/N
A08 PAGE35 : Change PR8 Package to 3720
A09 PAGE42 : Stuff PC44
A10 PAGE37 : Stuff PC165
A11 PAGE37 : Stuff PC153
A12 PAGE36 : Change P/N
A13 PAGE31 : Stuff L73
A14 PAGE31 : Stuff L45
A15 PAGE31 : Stuff L44
A16 PAGE31 : Add 100p for EMI
A17 PAGE23 : Add 1000p for EMI
A18 PAGE23 : Add 1000p for EMI
A19 PAGE02 : Delete R356
A20
A21
A22 PAGE32 : Delete EC25,EC26,EC27,EC28
A23
A24
A25
A26
A27 PAGE44 : Change PR46 from 1.7K ohm to 1.2K ohm.
A28
A29
A30

Note :
1. Remove Jumper : JP5,JP16,JP6,JP14,JP3,JP13,JP11,JP2,JP8,JP9,JP10,JP15,JP17,JP12,JP1,JP7
2. Remove 0 ohm :
R355,R356,R370,183,R207,R73,R331,L61,R76,R65,R83,R42,R50,L9,R35,R24,R27,R448,R228,R204,R202,R199,
R197,R195,R223,R424,R414,R400,R442,R459,R458,R446,R62,R70,R351.
3. Change footprint :
C119,C139,C149,C153,C154,C181,C182,C185,C191,C192,C195,C198,C199,C201,C202,C204,C205,C209,
C217,C218,C222,C224,C225,C233,C234,C235,C236,C242,C248,C249,C252,C255,C260,C261,C262,C263,
C266,C268,C270,C273,C275,C277,C280,C285,C304,C307,C313,C314,C316,C318,C328,C329,C330,C332,
C335,C336,C337,C338,C340,C361,C362,C363,C364,L30,L39,R9,R84,R89,R95,R96,R98,R123,R126,R134,
R158,R363,C296,C308,C213

Model	KN1A M/B BOARD	
Page	From	To
1	1A	3A
2	1A	3A
3	1A	3A
4	1A	3A
5	1A	3A
6	1A	3A
7	1A	3A
8	1A	3A
9	1A	3A
10	1A	3A
11	1A	3A
12	1A	3A
13	1A	3A
14	1A	3A
15	1A	3A
16	1A	3A
17	1A	3A
18	1A	3A
19	1A	3A
20	1A	3A
21	1A	3A
22	1A	3A
23	1A	3A
24	1A	3A
25	1A	3A
26	1A	3A
27	1A	3A
28	1A	3A
29	1A	3A
30	1A	3A
31	1A	3A
32	1A	3A
33	1A	3A
34	1A	3A
35	1A	3A
36	1A	3A
37	1A	3A
38	1A	3A
39	1A	3A
40	1A	3A
41	1A	3A
42	1A	3A
43	1A	3A
44	1A	3A
45	1A	3A
46	1A	3A
47	1A	3A
48	1A	3A

PROJECT : ZQA
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHANGE LIST - 3A	3A
Date: Monday, June 21, 2010	Sheet 48 of 48	

Quanta Computer Inc. ZQA	PROJECT: ZQA	PCBA NO.	REV: 3A	DOC. NO :
	APPROVED BY : Johnny O	CHECK BY : Darren Liao	DRAWING BY : Bowen Chuang	DATE :06/11/2010 SHEET 1