

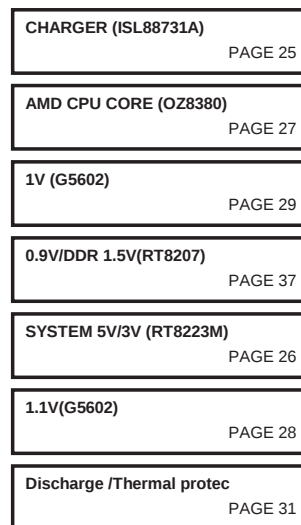
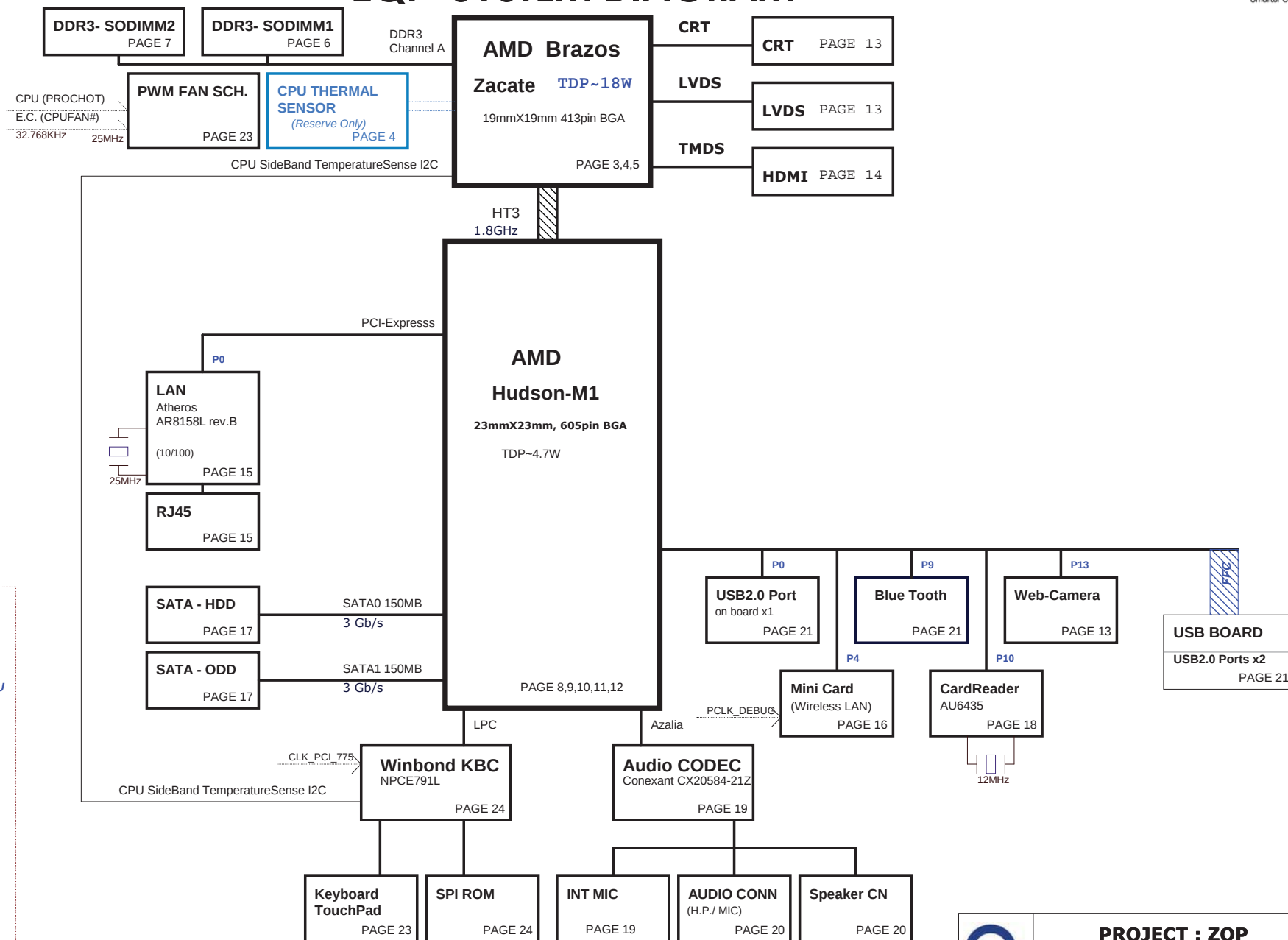
ZQP SYSTEM DIAGRAM

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

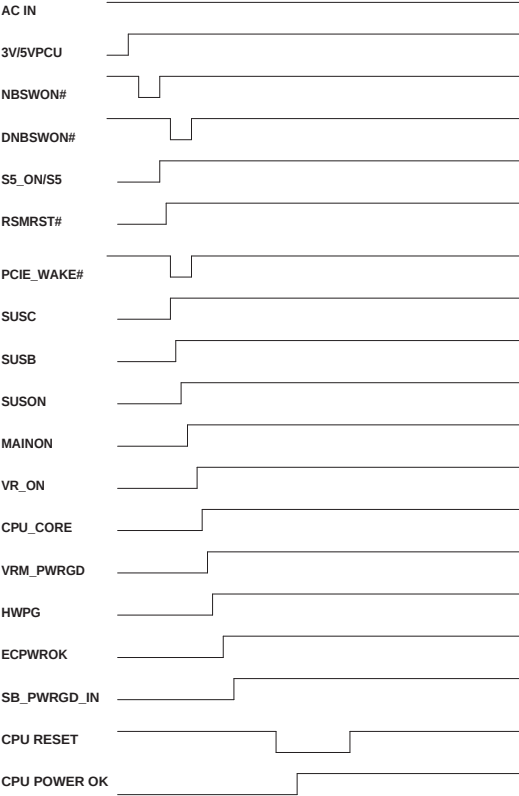
HDMI@ ----> HDMI option
SP@ ----> Board ID/Strap pin
H@ ----> 家電下鄉

UMA REV: B



PAGE#	DESCRIPTION	NOTE
1	BLOCK DIAGRAM	
2	SYSTEM INFORMATION	
3	ONTARIO MEM & PCIE I/F(1/3)	
4	ONTATIO DISPLAY/CLK/M(2/3)	
5	ONTARIO POWER & DECOUP(3/3)	
6	DDR3 SO-DIMM (STD=8)	
7	DDR3 SO-DIMM (STD=4)	
8	HUDSON PCIE/LPC/CPU IF(1/5)	
9	HUDSON ACPI/GPIO/USB(2/5)	
10	HUDSON SATA/BIDs(3/5)	
11	HUDSON PWR/GND(4/5)	
12	HUDSON STRAPS/PWRGD(5/5)	
13	CRT/LVDS/CCD	
14	HDMI	
15	LAN AR8152	
16	MINI PCI-E	
17	HDD /ODD	
18	CARD READER	
19	AUDIO - CONEXANT 20584	
20	AUDIO JACK CONN	
21	USB / BT /TP	
22	LED / NUT	
23	KB/FAN/TP	
24	WPCE791 /FLASH	
25	CHARGER (ISL88731A)	
26	SYSTEM 5V/3V (RT8223M)	
27	CPU CORE (OZ8380)	
28	VCCP 1.1V (G5602)	
29	+1V(G5602)	
30	DDR 1.5V (RT8207A)	
31	+1.8V/Discharge/Thermal Protection	
32	Change list	

Power Sequence



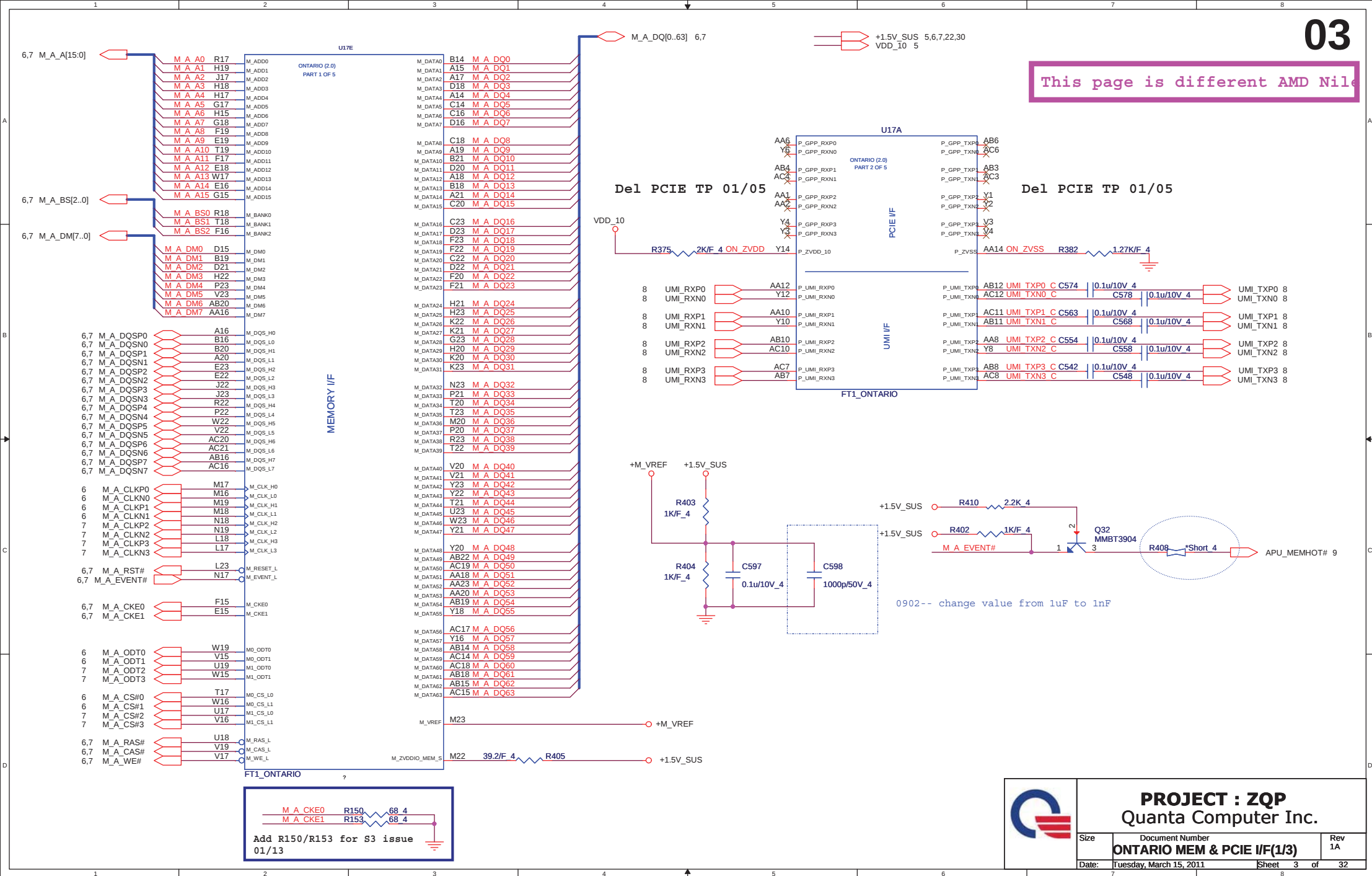
Hudson M1 SM BUS

SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

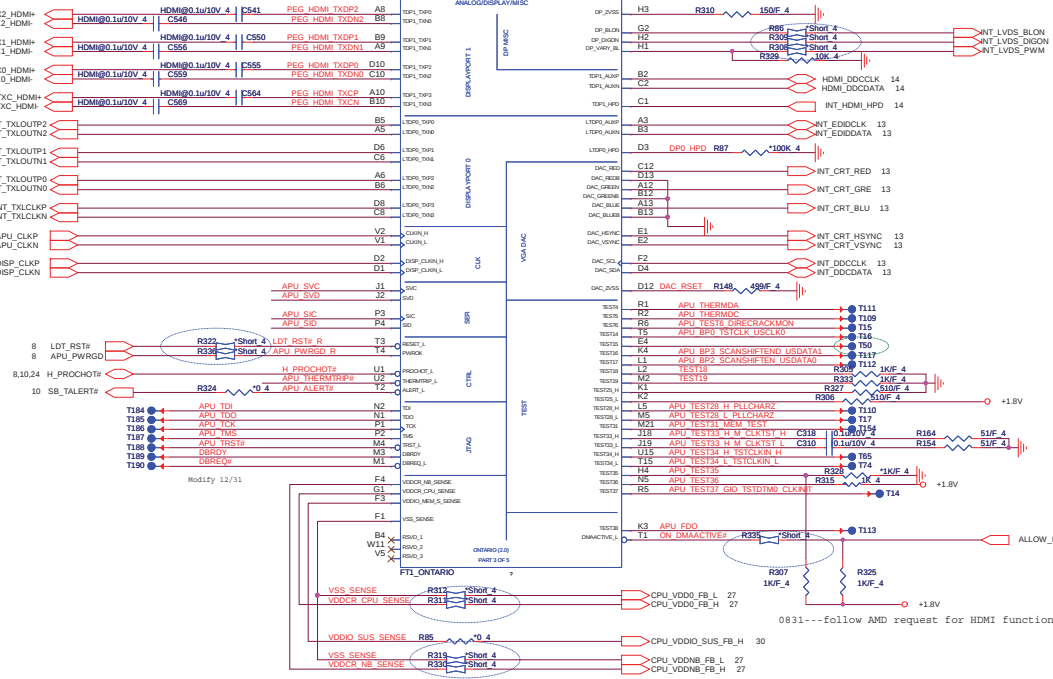
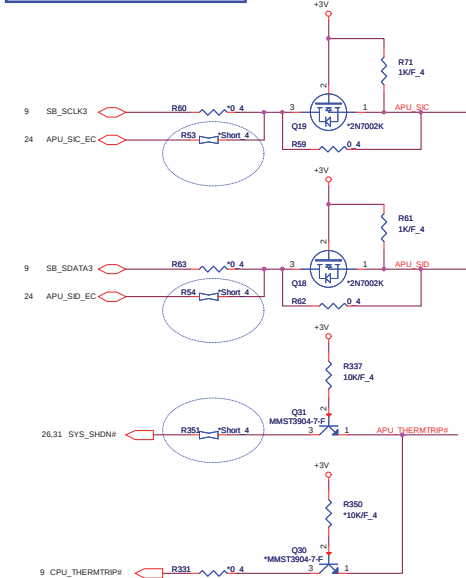
KBC(EC) SM BUS

KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal

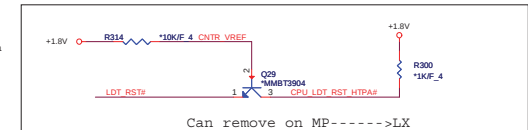
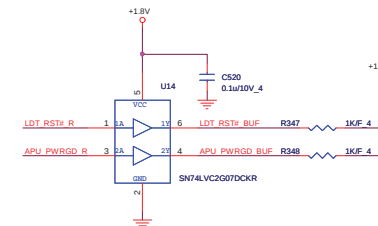
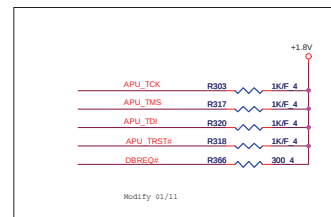
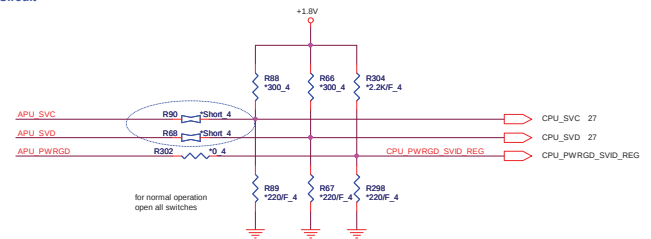
This page is different AMD Nile



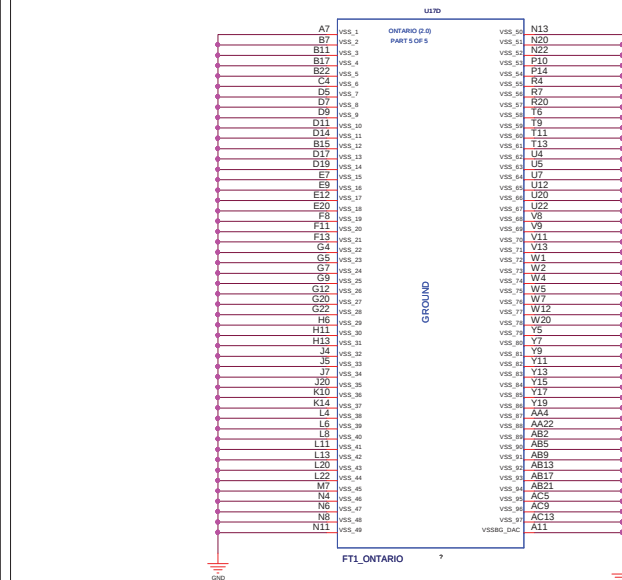
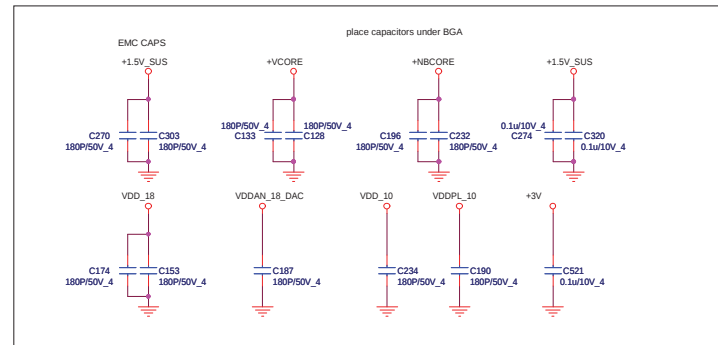
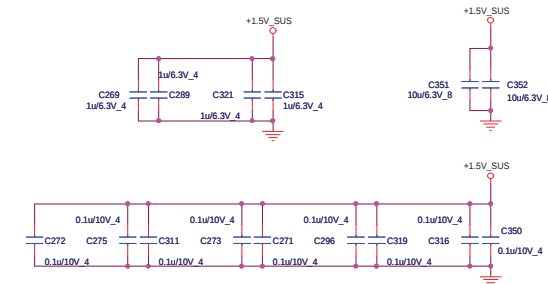
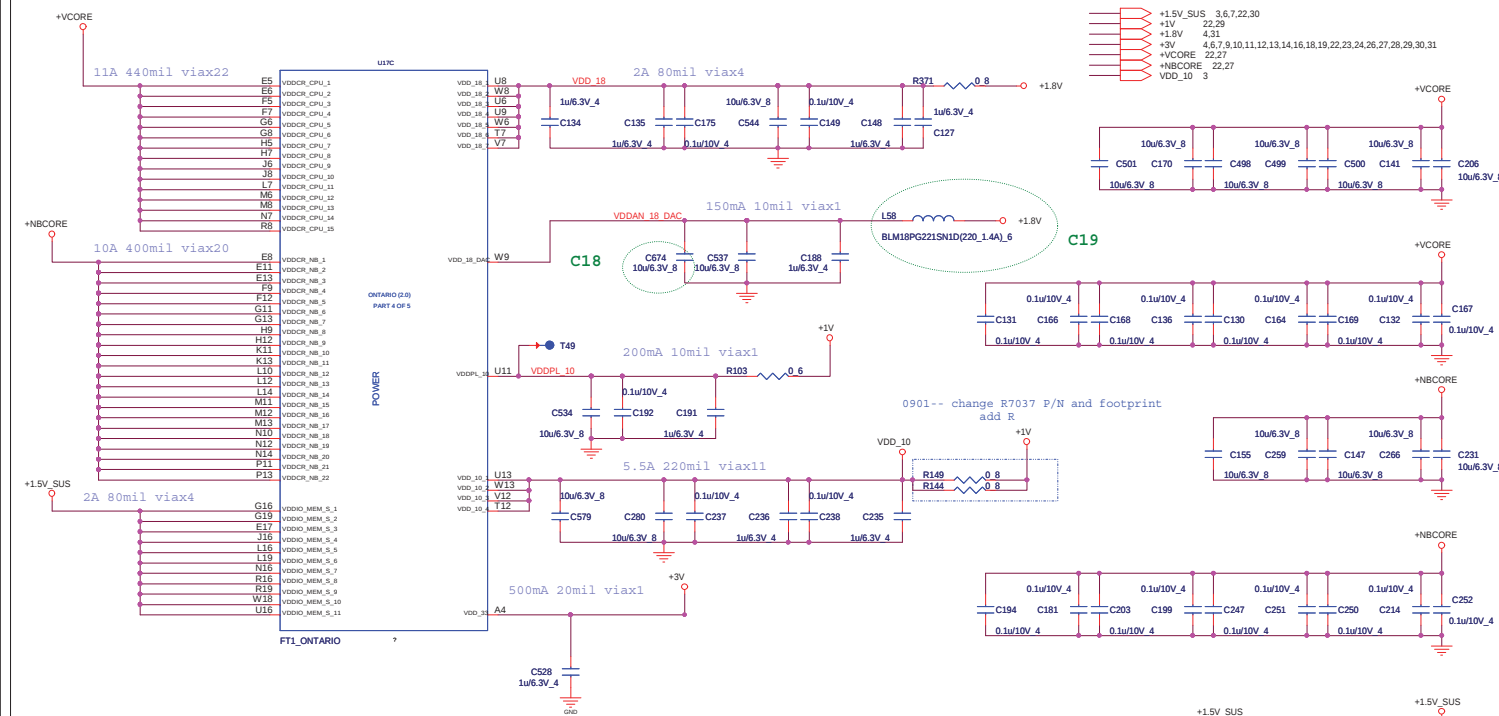
+1.8V
 R70 1K 1/4W 4 APU_SVC
 R69 1K 1/4W 4 APU_S2D
 R301 300 1/4W 4 LDT_RST#
 R326 300 1/4W 4 APU_PWPGD
 -3V
 R345 1K 1/4W 4 APU_THERMTRIP#
 R334 1K 1/4W 4 APU_ALERT#
 R323 1K 1/4W 4 H_PROCHOT#
 GND
 2K 1/16W F-4 R357 INT CRT RED
 2K 1/16W F-4 R376 INT CRT GRN
 2K 1/16W F-4 R380 INT CRT BLU
 1500V 4
 1500V 4
 1500V 4
 -3V
 2K 1/16W F-4 R357 INT EDODCLK
 2K 1/16W F-4 R355 INT EDODATA



VID Override Circuit

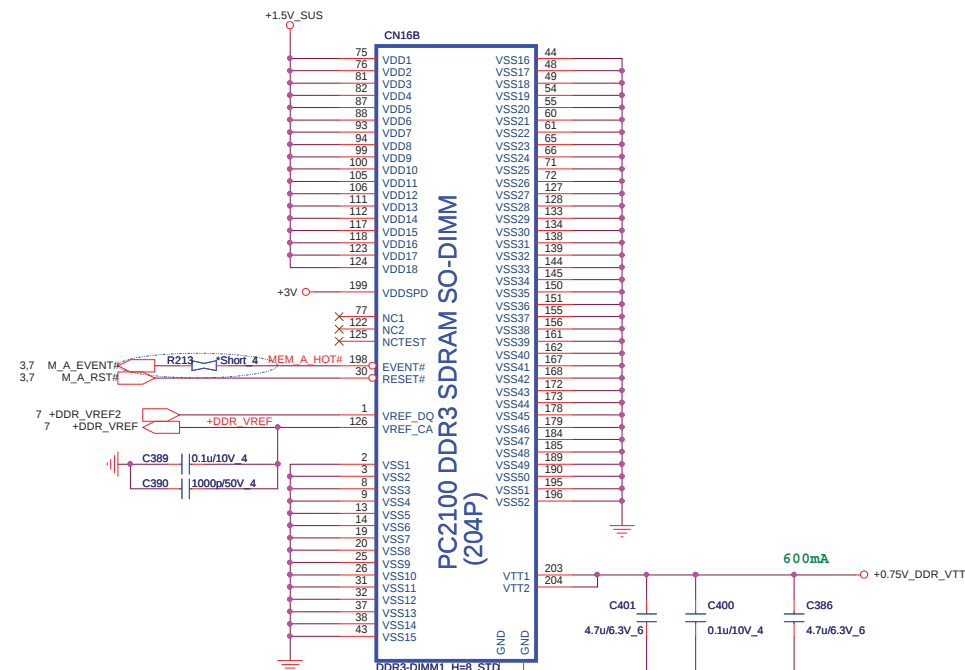
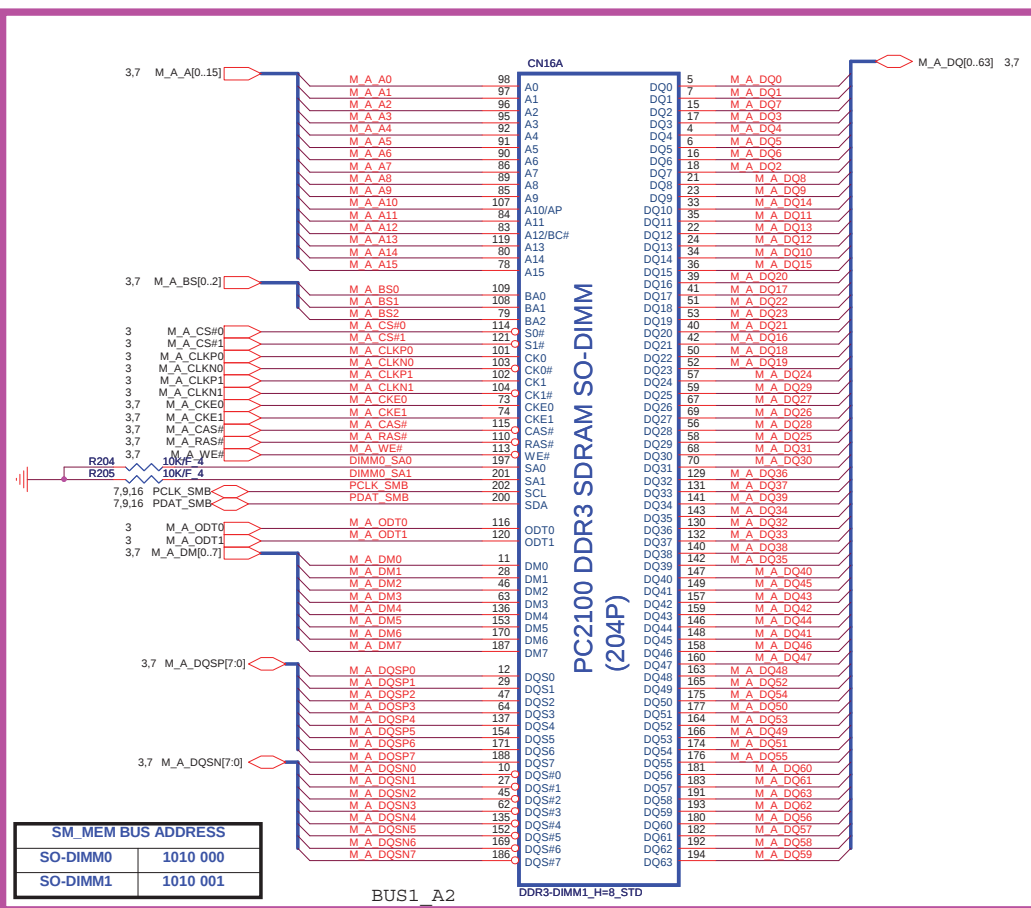


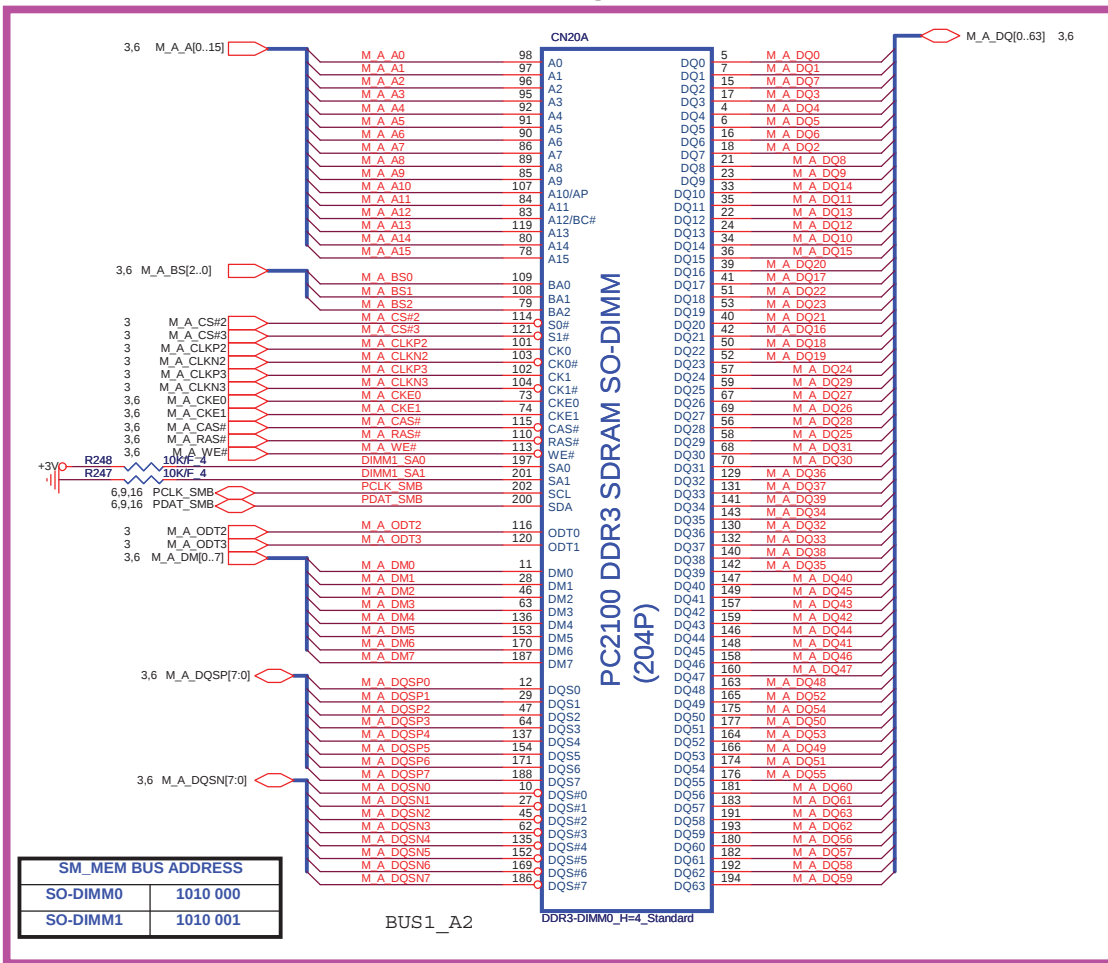
This page is different AMD Nil.

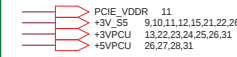
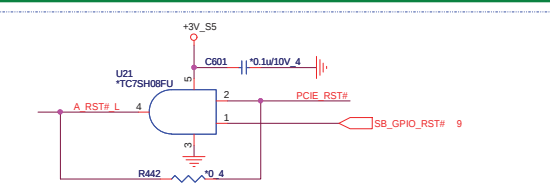
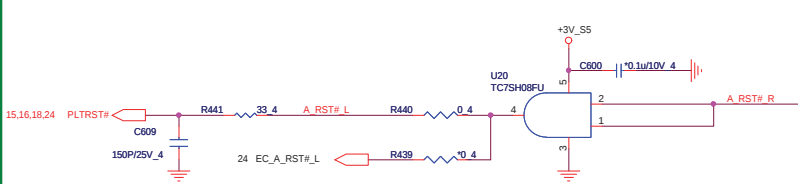


0830--P/N and footprint are follow ZR7B

+1.5V_SUS 3.5,7,22,30
+0.75V_DDR_VTT 7,30
+3V 4,5,7,9,10,11,12,13,14,16,18,19,22,23,24,26,27,28,29,30,31

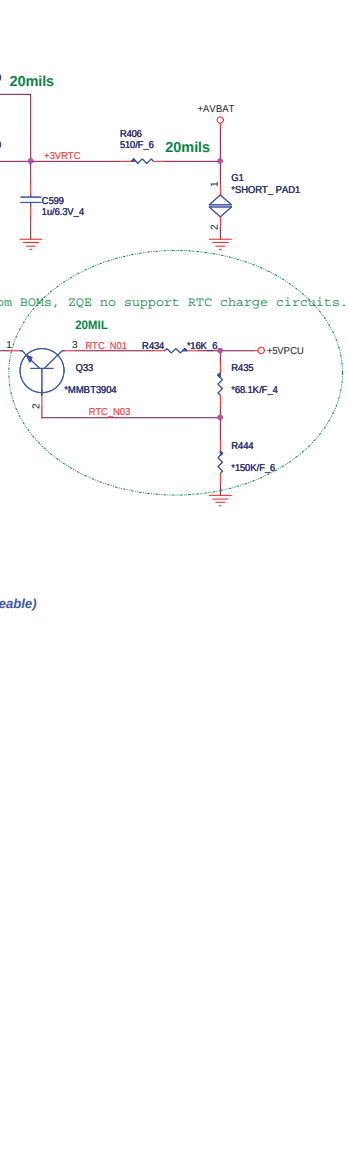
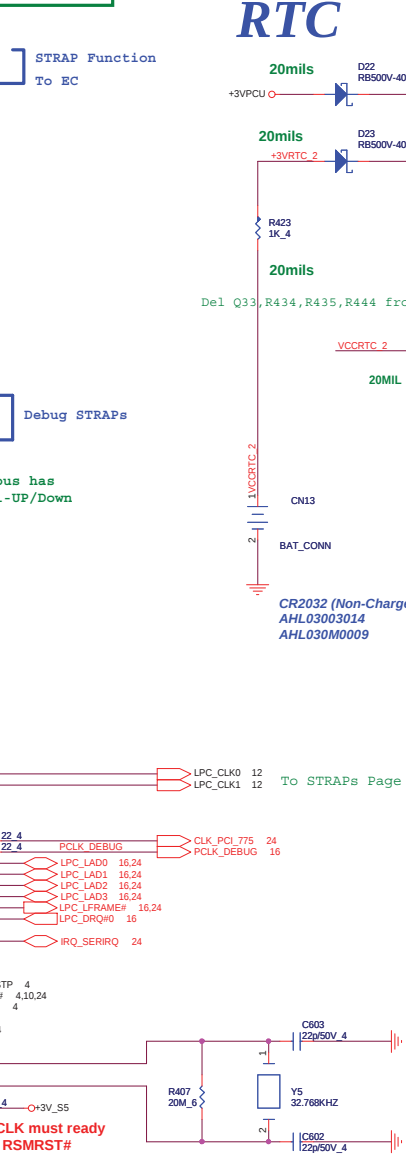
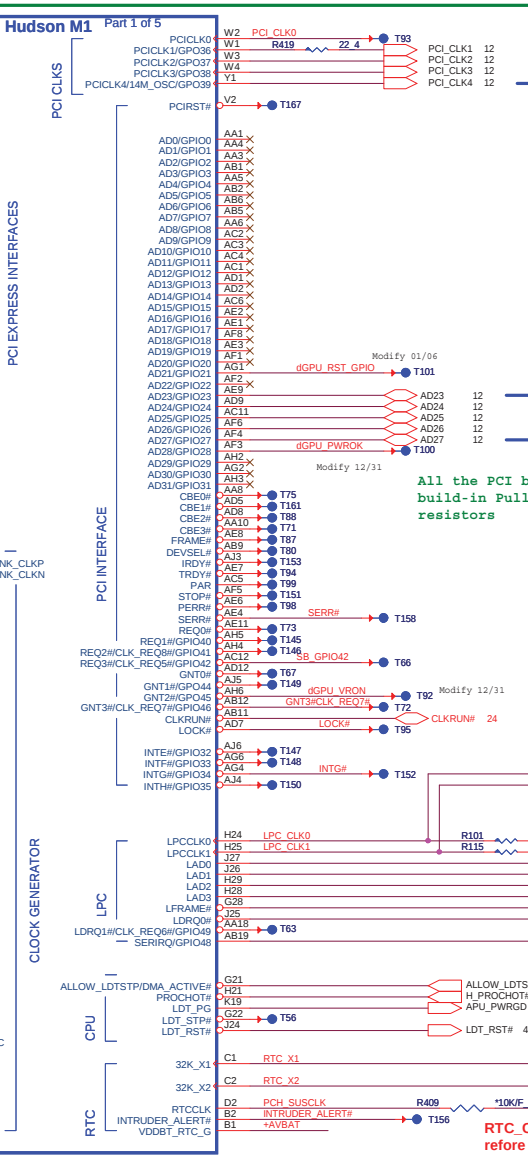
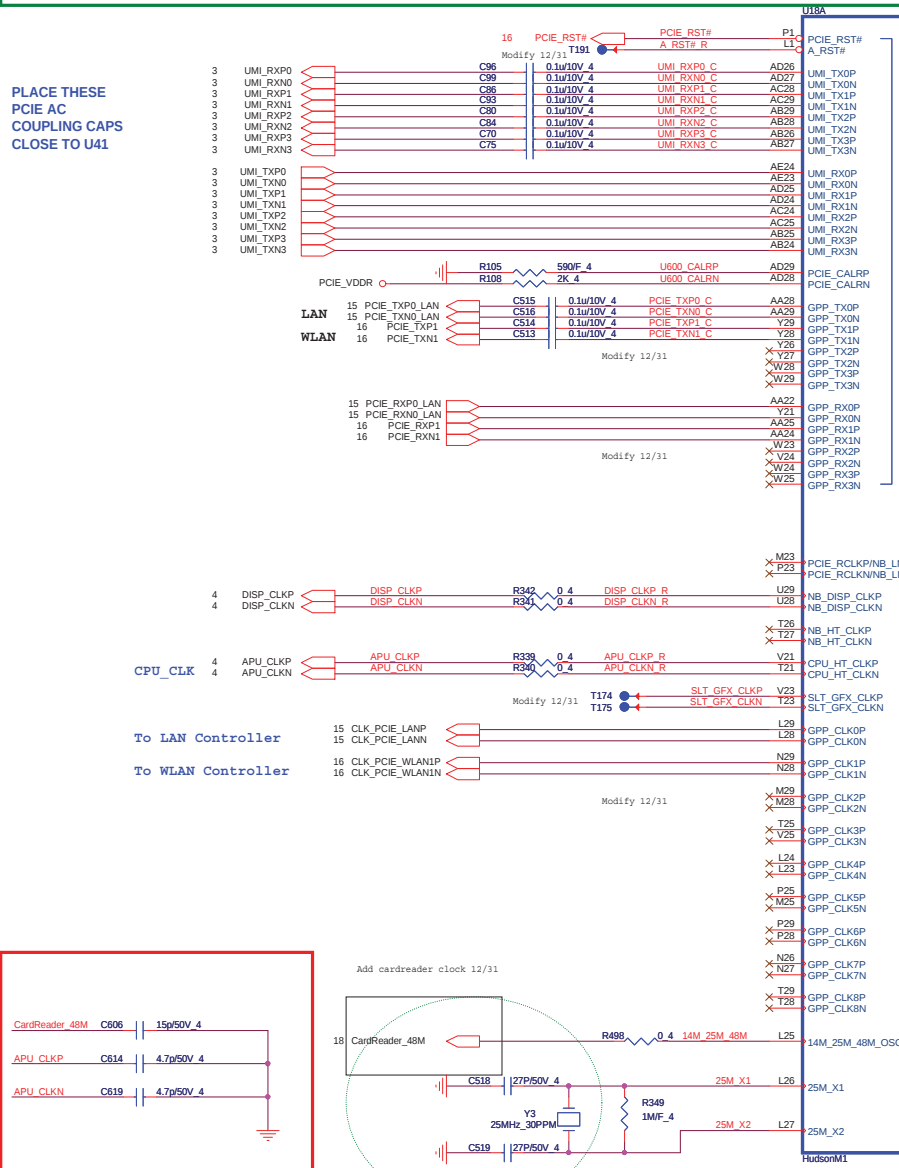






This page is different AMD Nil expect RTC circuit

PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U41



Add C606,C614,C619 for strong clock
02/15 REV:B

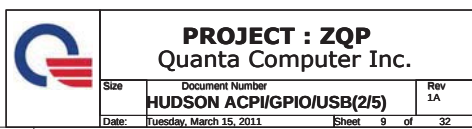
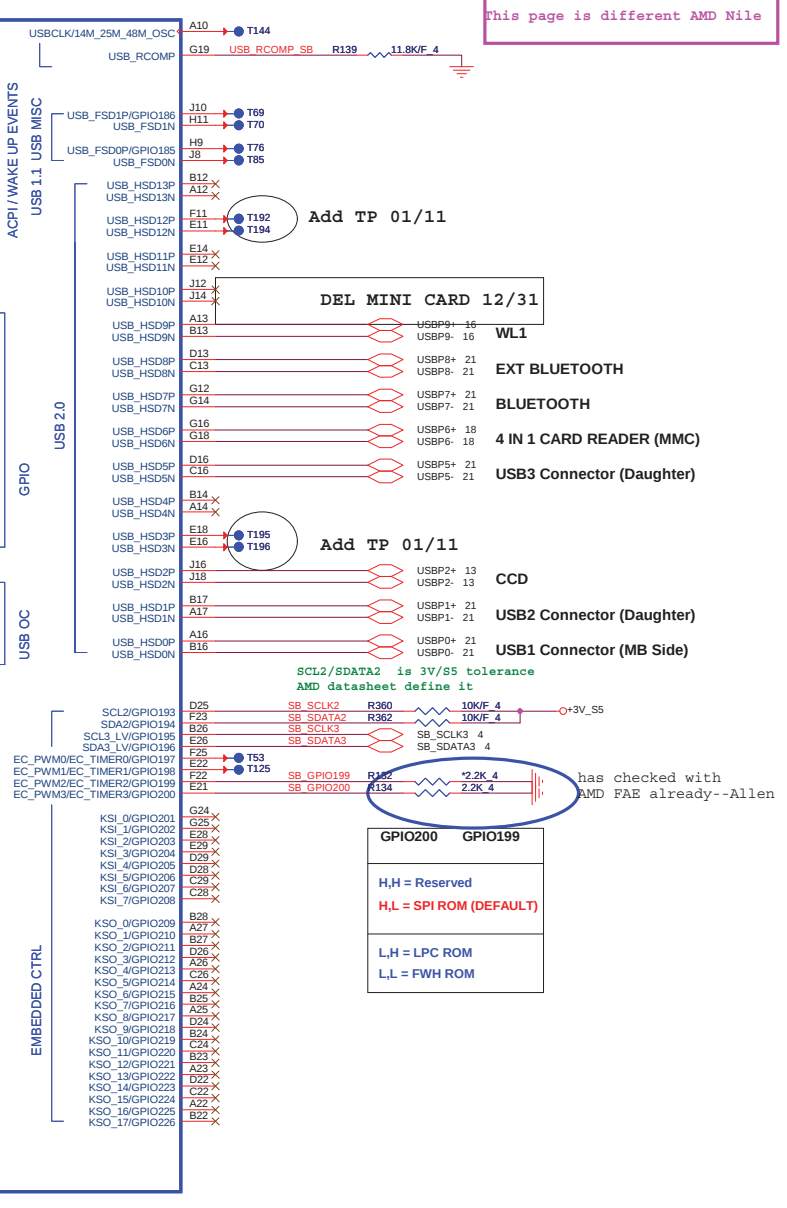
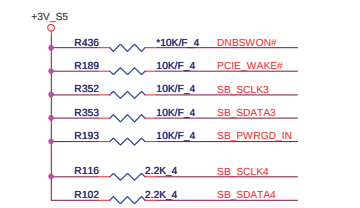
BG625000486

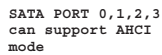
INTRUDER_ALERT# Left not connected (Southbridge has 50-kohm internal pull-up to VBAT).



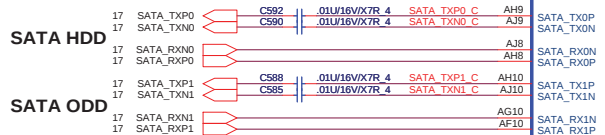
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	Hudson PCIE/LPC/CPU IF(1/5)	1A
Date:	Tuesday, March 15, 2011	Sheet 8 of 32





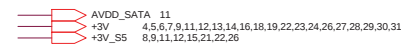
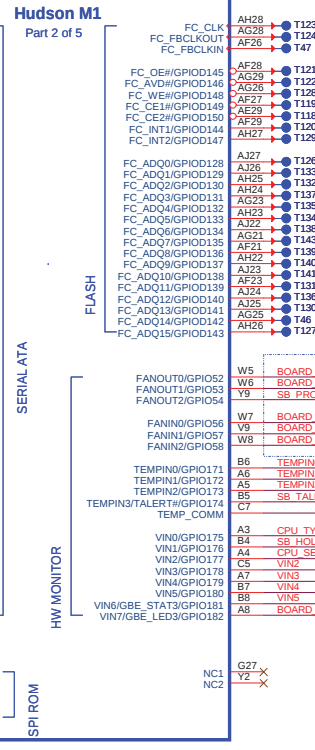
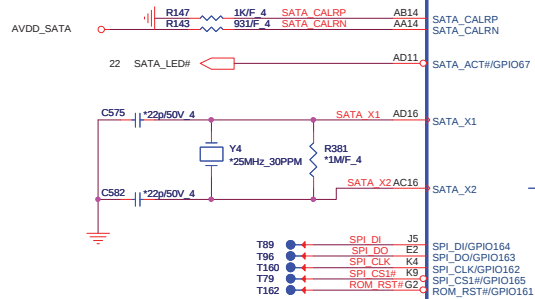
PLACE SATA AC COUPLING
CAPS CLOSE TO Hudson M1



PLACE SATA_CAL RES
VERY CLOSE TO BALL
OF Hudson M1

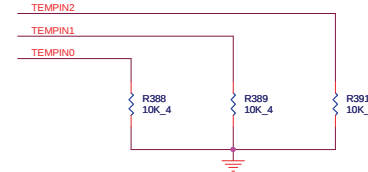
```
XTLVDD_SATA-- SATA
crystal power

PLVDD_SATA--
SATA PLL
POWER
```



This page is different AMD Nile

AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2
can not maintain on floating stages when without usage.
Do not care pull high or pull down.

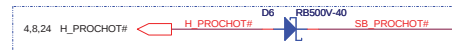


0831--modify location

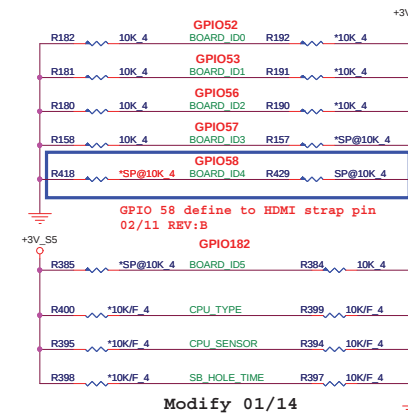
MB ID

CPU THERMAL	GPIO52
External	1
SB-TSI	0
SB8XX Hold Time	GPIO53
1.2V	1
1.1V	0
DU1/MK2	GPIO56
MK2.0 AMD	1
DU1.0 AMD	0

	GPIO57
(Dis) SW	1
UMA	0
	GPIO58
With HDMI	1
Without HDMI	0
	GPIO182
PX4.0	1
PX3.0	0



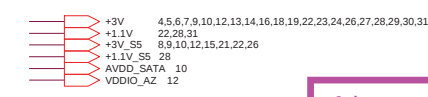
0831--add circuit



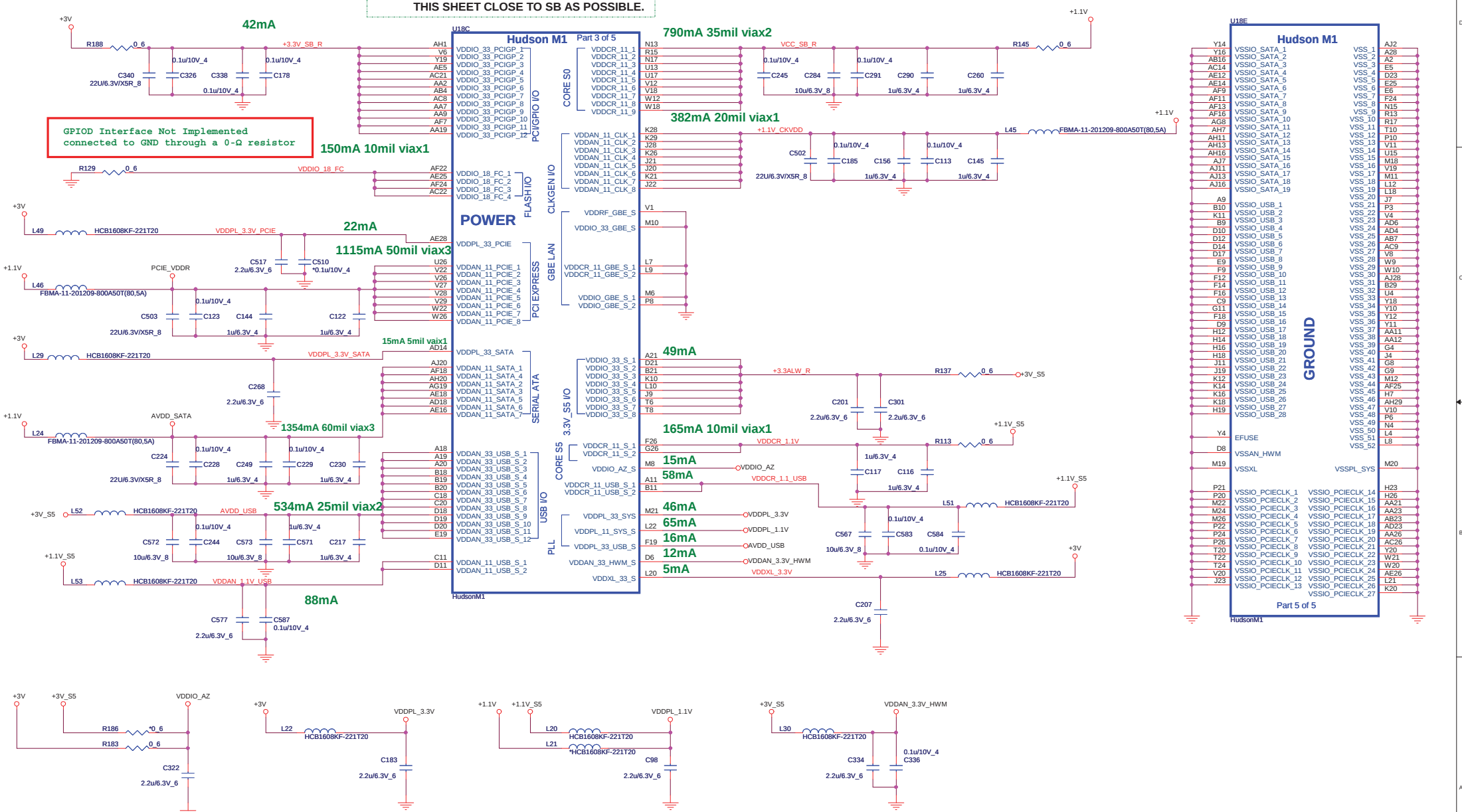
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number HUDSON SATA/BID_S(3/5)	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 10 of 32

This page is different AMD Nile



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

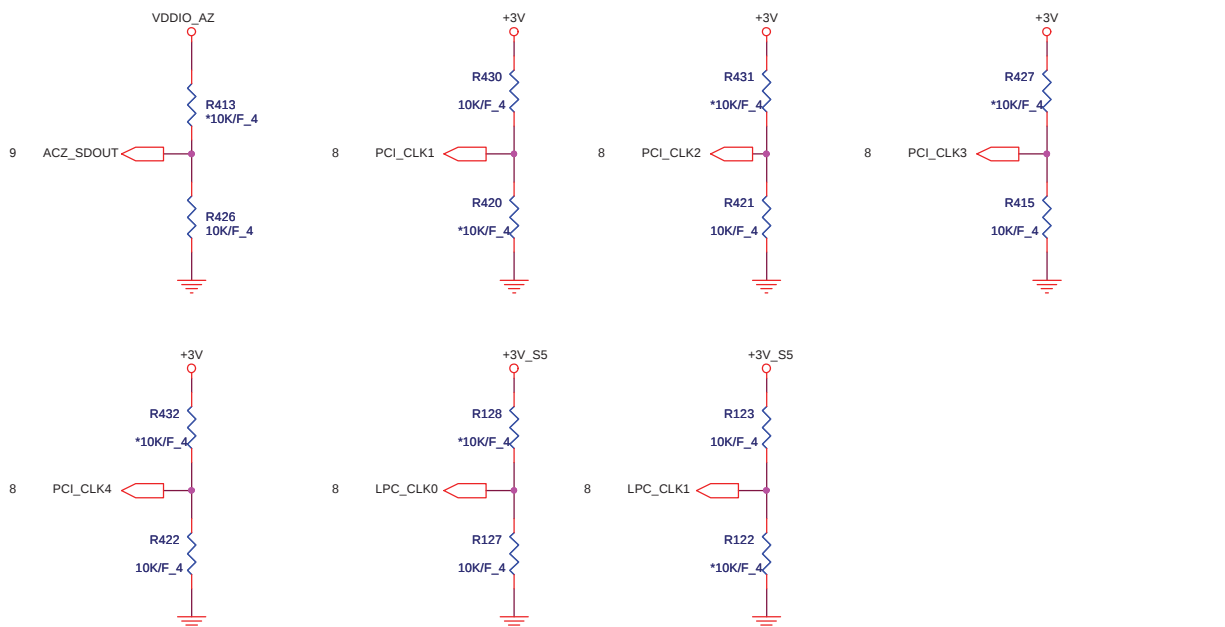




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

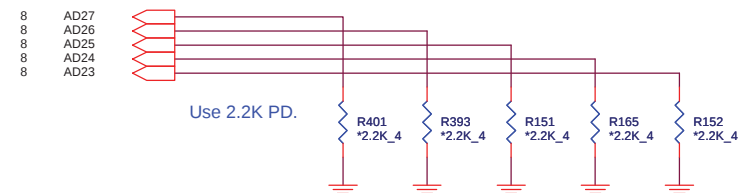
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

VDDIO_AZ 11
+3V 4,5,6,7,9,10,11,13,14,16,18,19,22,23,24,26,27,28,29,30,31
+3V_S5 8,9,10,11,15,21,22,26

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



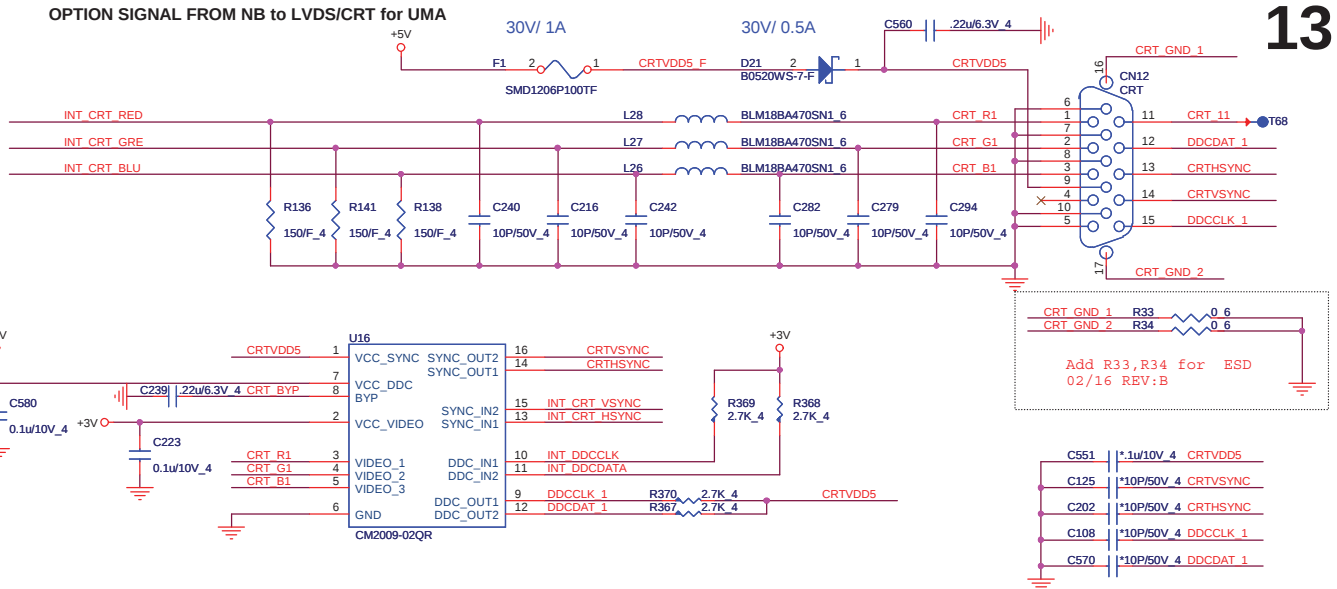
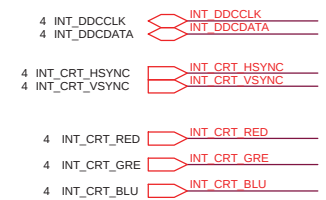
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



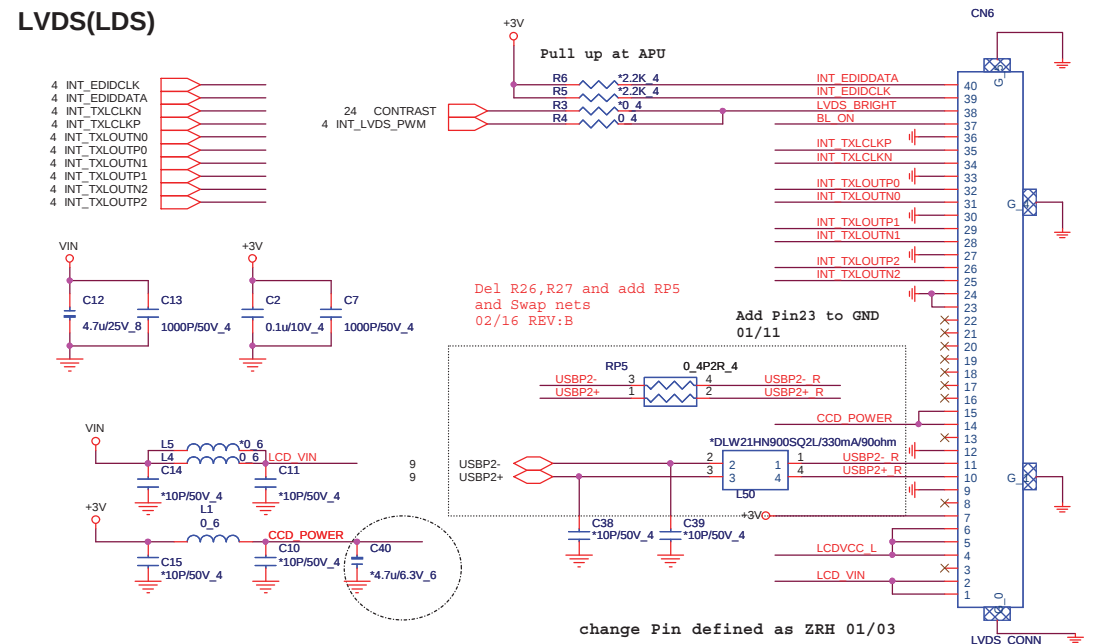
PROJECT : ZQP
Quanta Computer Inc.

Size Document Number
HUDSON STRAPS/PWRGD(5/5) Rev 1A
Date: Tuesday, March 15, 2011 Sheet 12 of 32

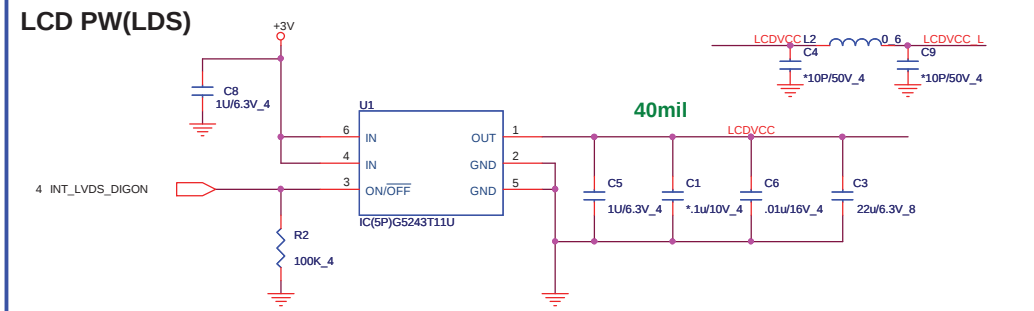
CRT



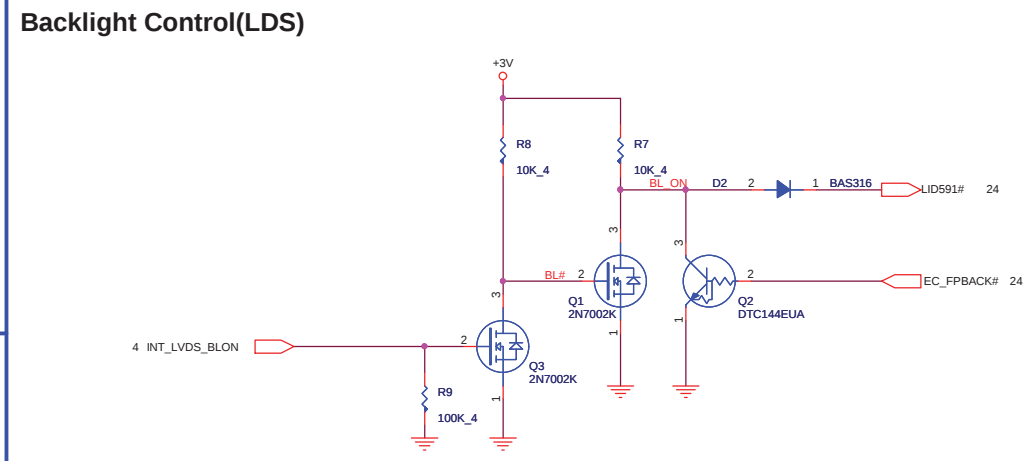
LVDS(LDS)



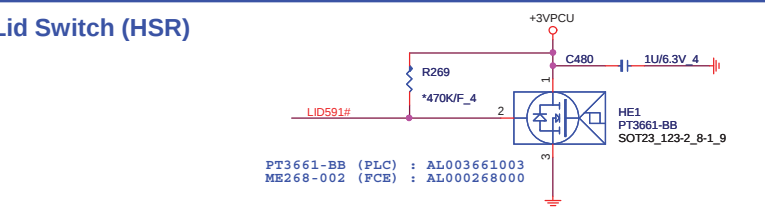
LCD PW(LDS)



Backlight Control(LDS)



Lid Switch (HSR)

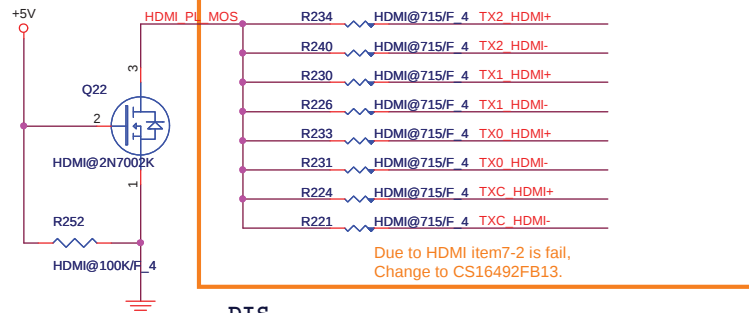


HDMI SDVO I2C Control



HDMI (HDM)

Close to HDMI Connector

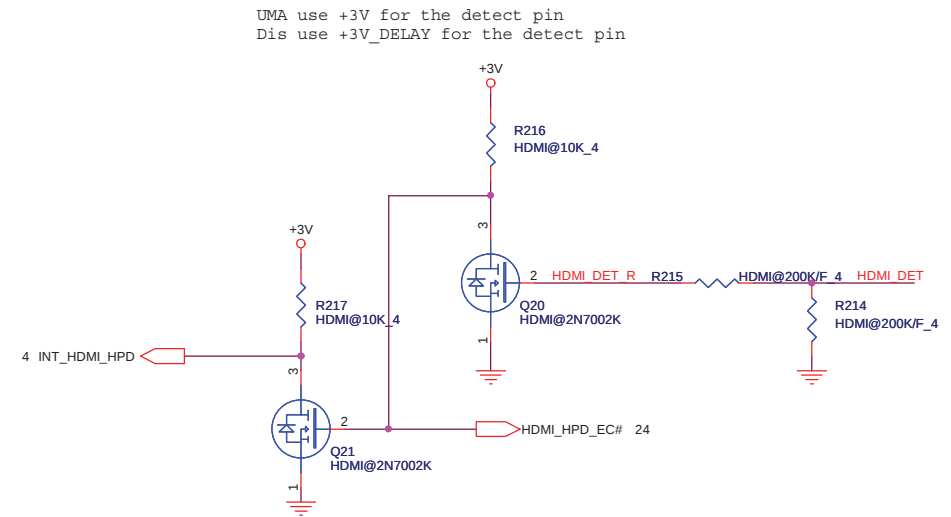
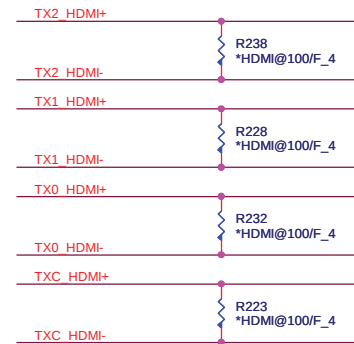


DIS
Stuff 499 ohm CS14992FB24



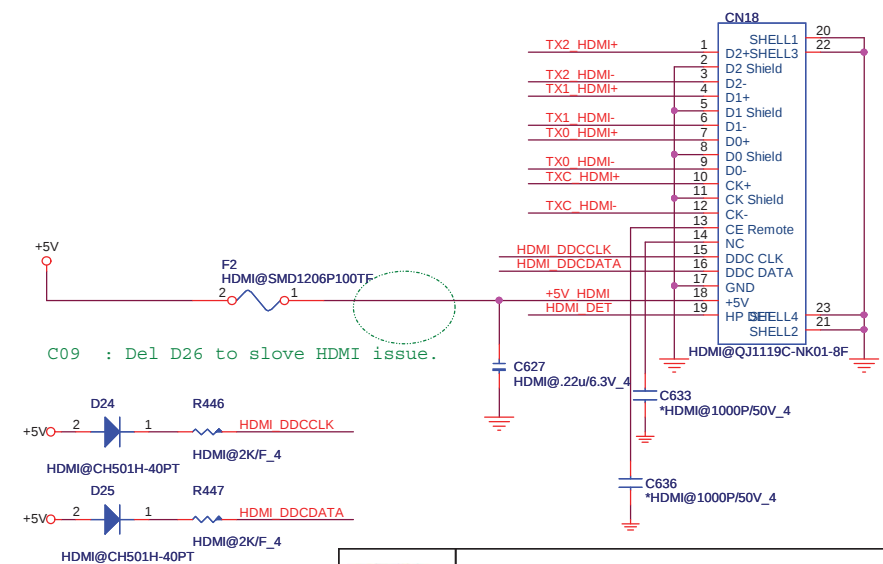
EMI reserve for HDMI(EMC)

Close connector



Added HDMI function
01/19 REV:B

HDMI PORT (HDM)



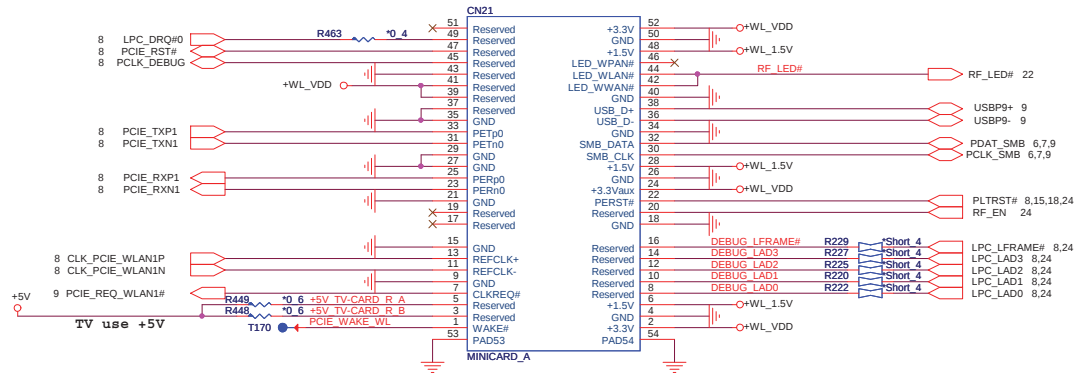
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number HDMI	Rev 1A
Date:	Tuesday, March 15, 2011	Sheet 14 of 32

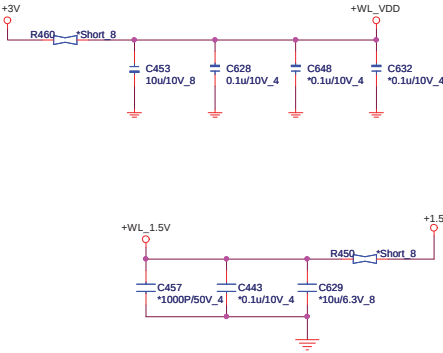
MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

Check LED signal. (active high or low)



Debug



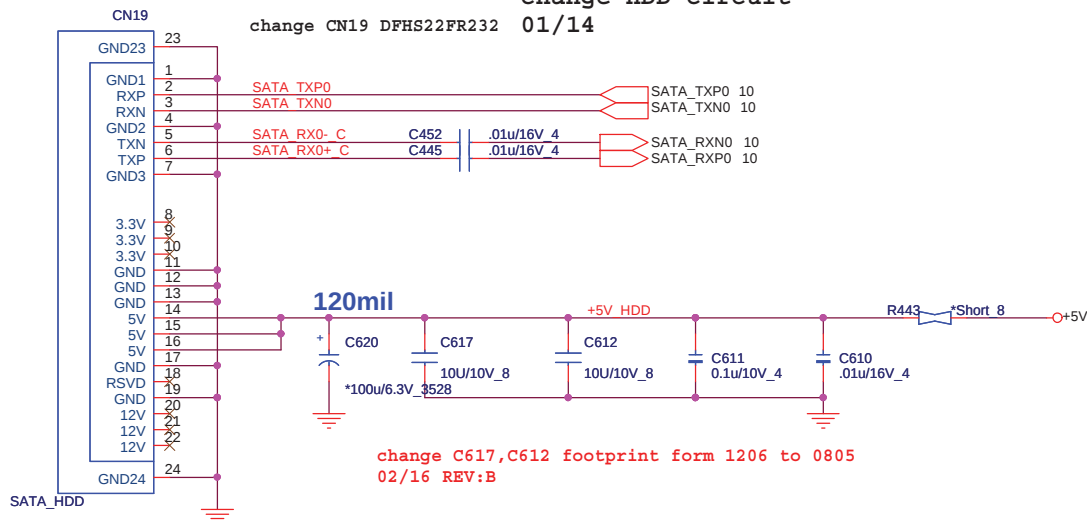
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	MINI PCI-E card	1A
Date:	Tuesday, March 15, 2011	Sheet 16 of 32

SATA HDD

change HDD circuit

change CN19 DFHS22FR232 01/14

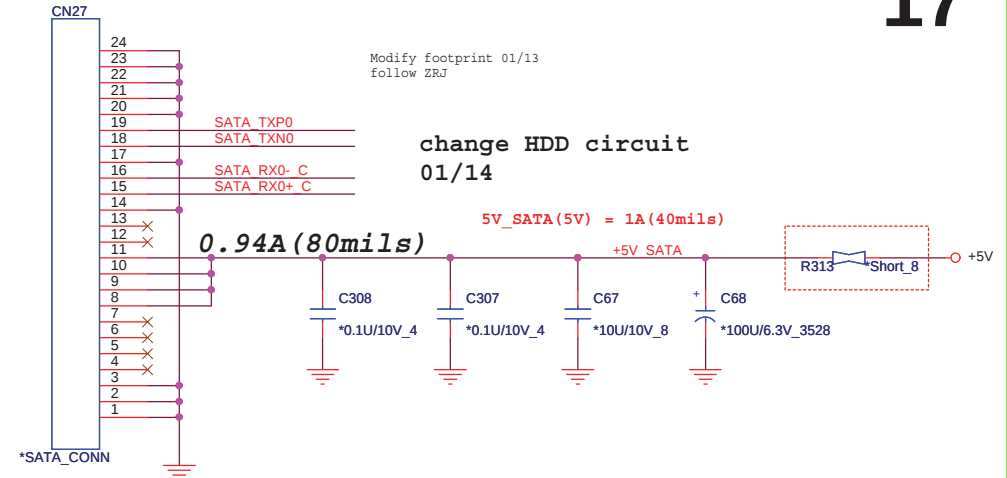


SATA HDD(HDD)

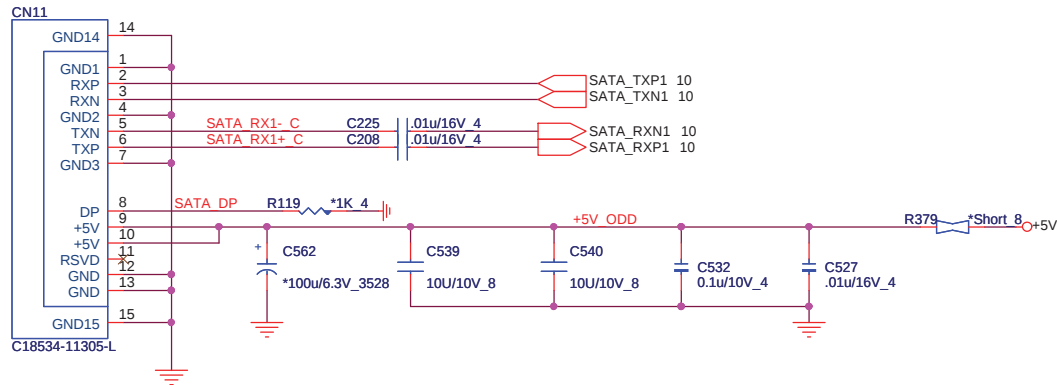
17

Modify footprint 01/13
follow ZRJ

change HDD circuit
01/14



SATA ODD



			PROJECT : ZQP Quanta Computer Inc.	
Size	Document Number		Rev	
	SATA-HDD/ODD/HOLE		1A	
Date:	Tuesday, March 15, 2011	Sheet	17 of	32

Port Configuration

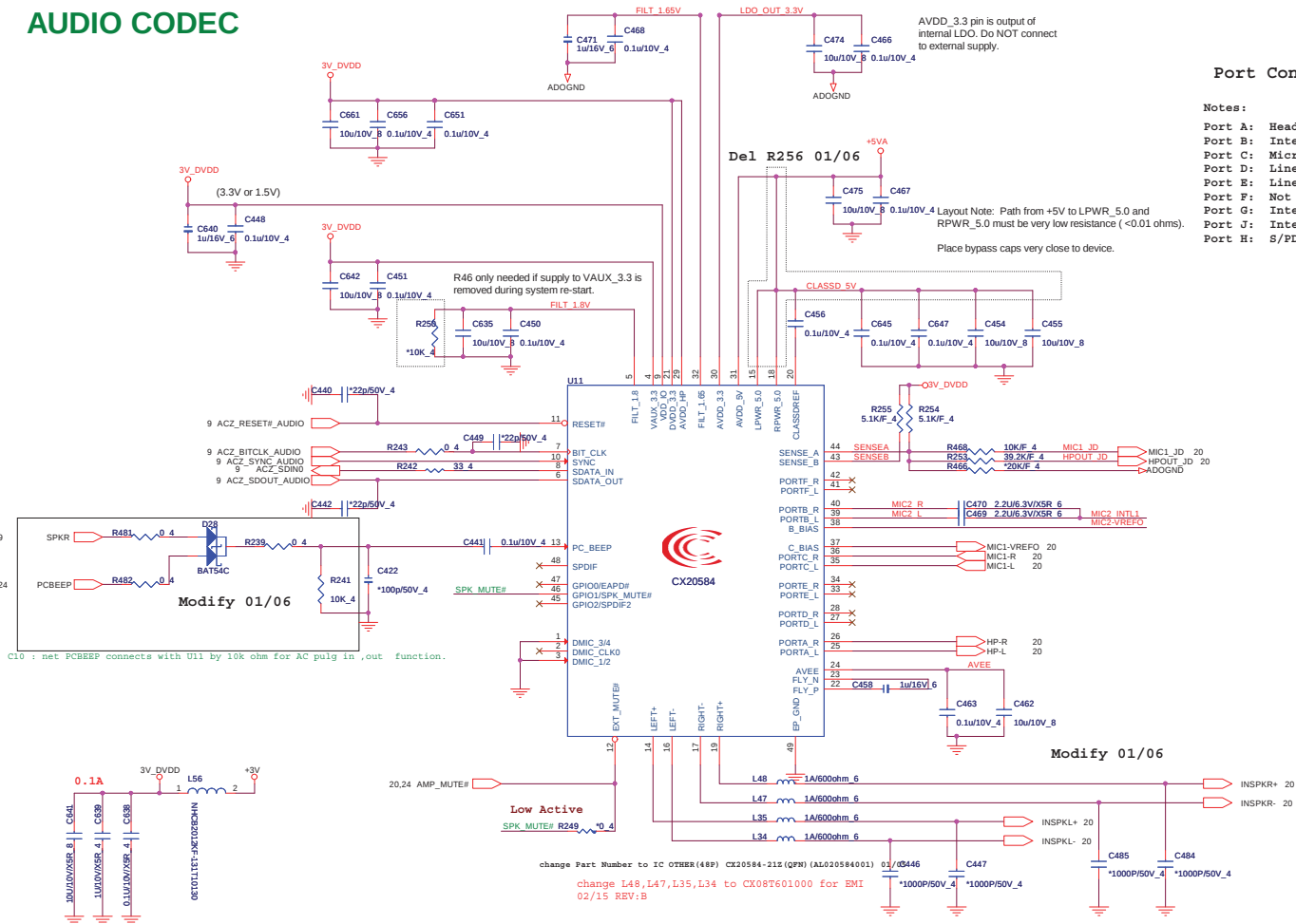
Notes:

- Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal MIC (mono or stereo)
Port C: Microphone/LI/LO jack
Port D: Line Out jack (Optional)
Port E: Line In jack (Optional)
Port F: Not used.
Port G: Internal stereo speakers
Port J: Internal stereo digital mic (Optional)
Port H: S/PDIF (jack shared with headphone)

Del R256 01/06

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

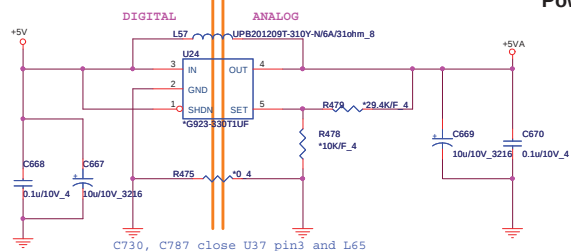
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



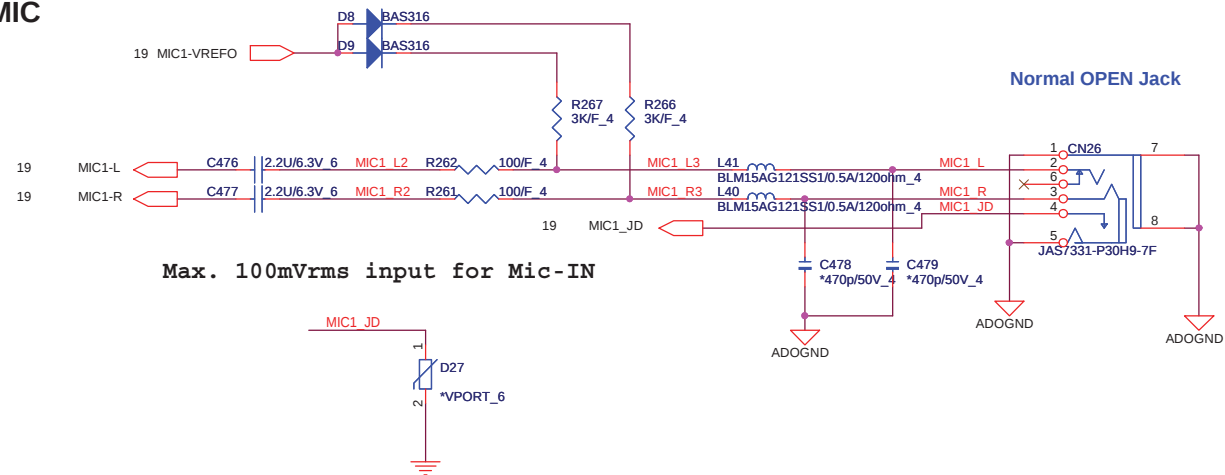
Modify 01/06

1. The VDD_IO and VAUX_3.3 pins should be connected to same power supply domain as HDA bus controller so that the HDA controller and codec bus interface will power-up at the same time. This will avoid bus leakage issues if using HDA controller with bus pull-up strap options. See other FET option on this page if these supplies are not on same domain as HDA controller.
2. To support Wake-on-Jack, the codec VAUX_3.3 pin must be powered from a Standby supply.
3. C309, C310, C311 are optional. Do not install unless needed for EMI/ISI.

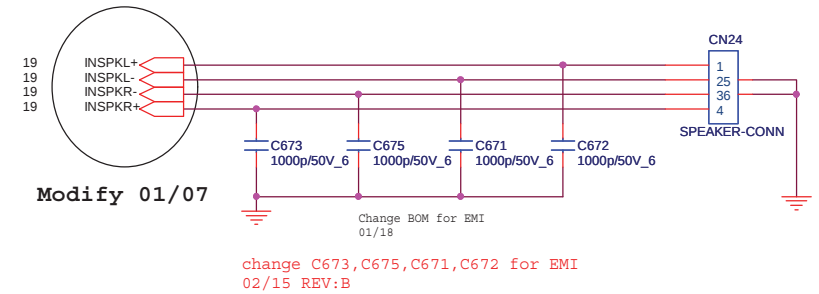
Power (ADO)



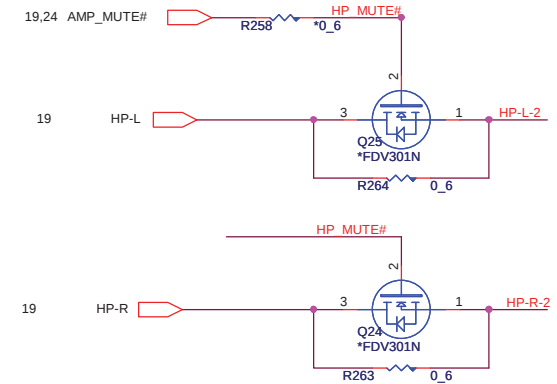
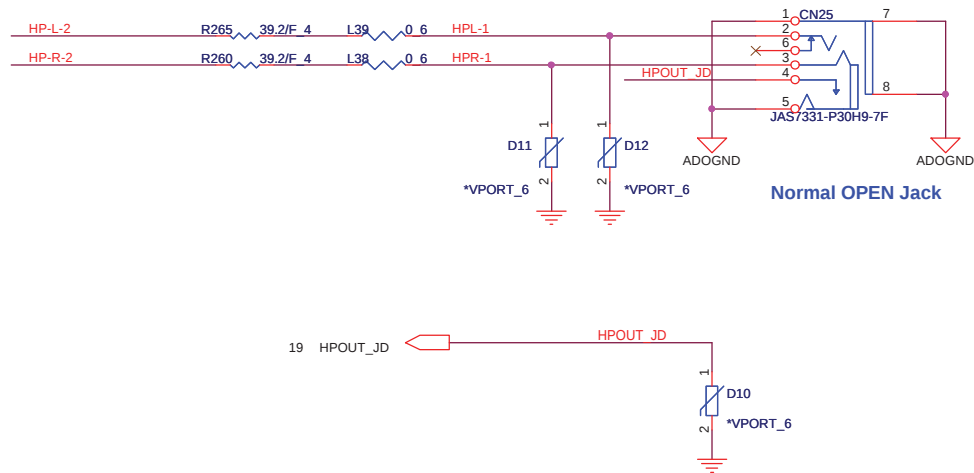
MIC



Internal Speaker



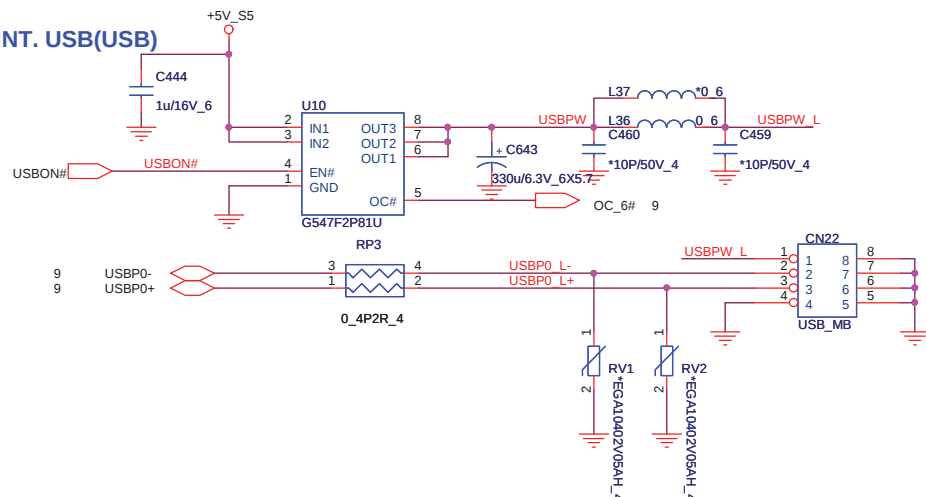
HP



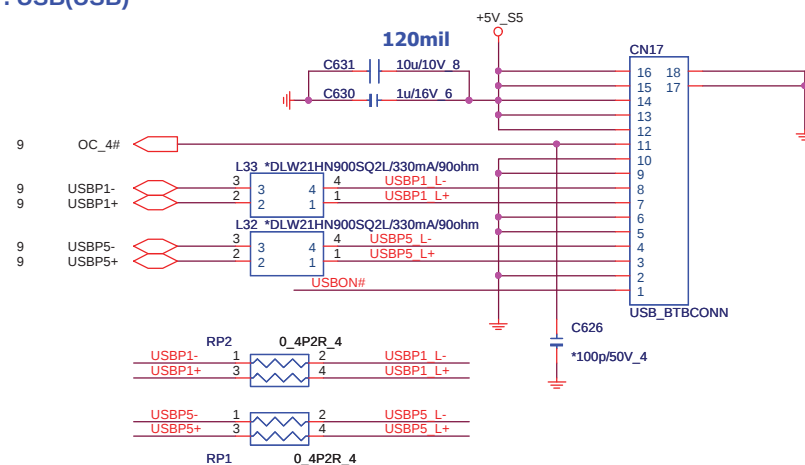
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	AUDIO JACK CONN	1A
Date:	Tuesday, March 15, 2011	Sheet 20 of 32

INT. USB(USB)

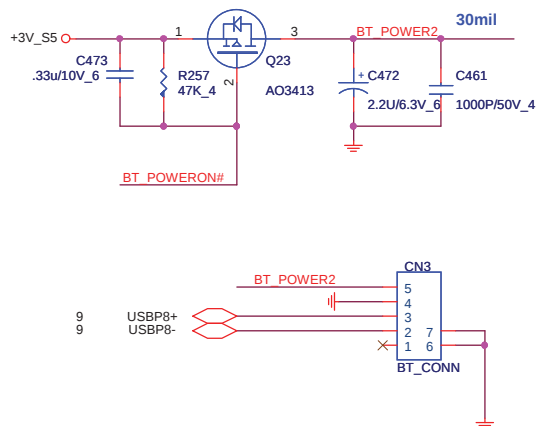


EXT. USB(USB)

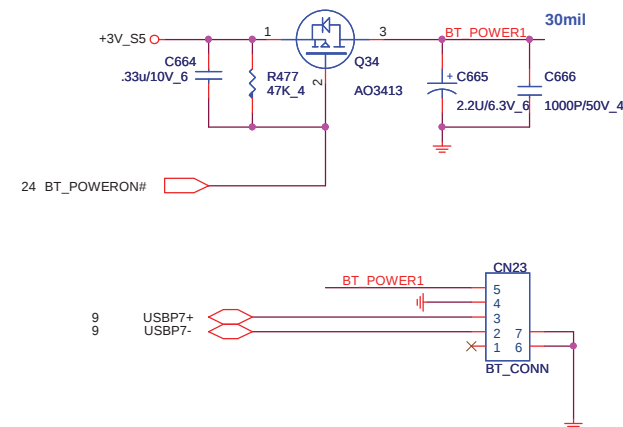


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BLUETOOTH V2.1 CONN(BTM)



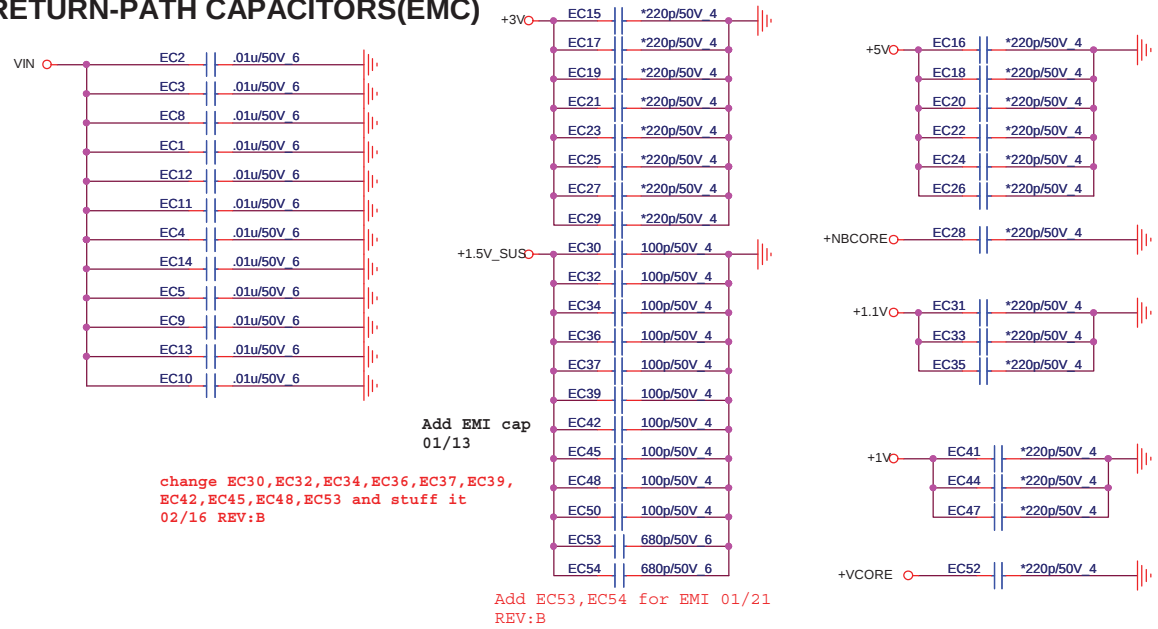
BLUETOOTH V3.0 CONN(BTM)



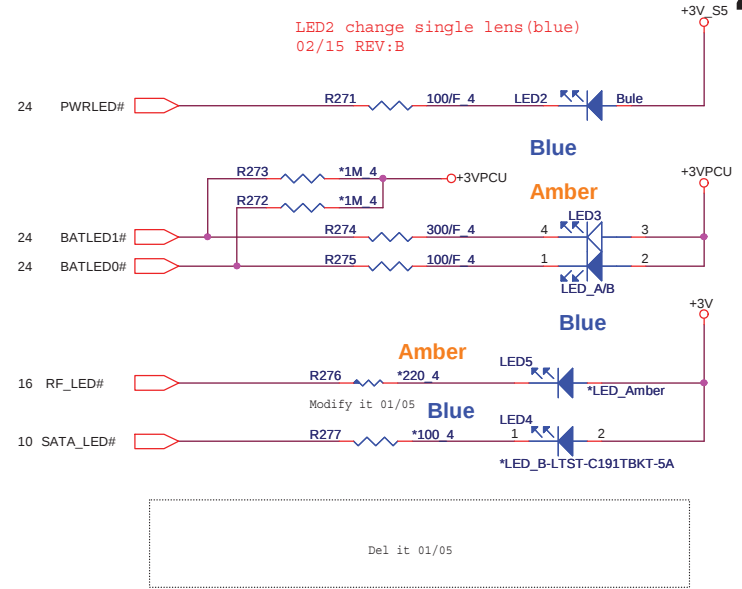
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number USB/BT	Rev 1A
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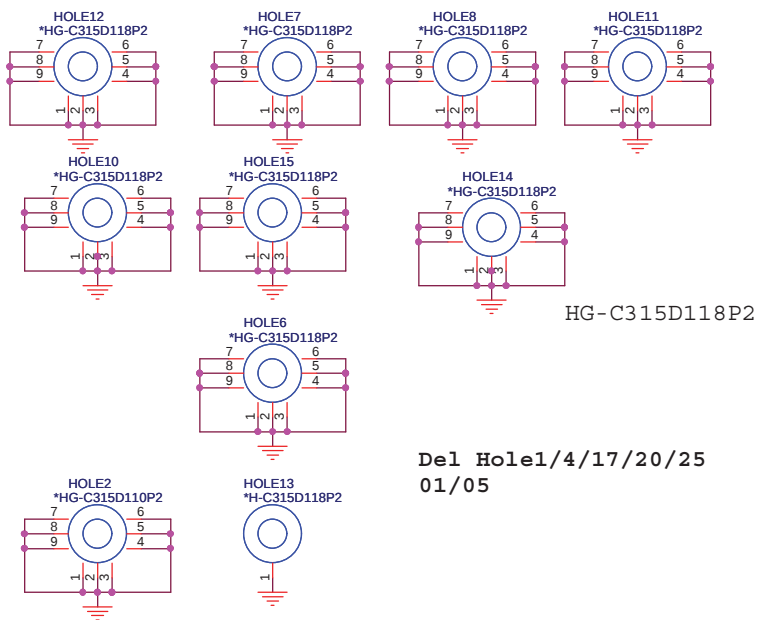
EE RETURN-PATH CAPACITORS(EMC)



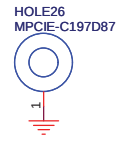
LED(UIF)



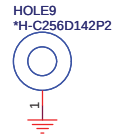
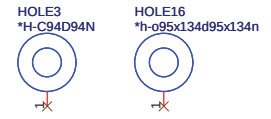
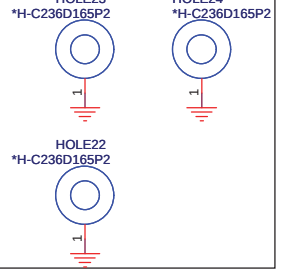
HOLE(OTH)



mini PCI



cpu

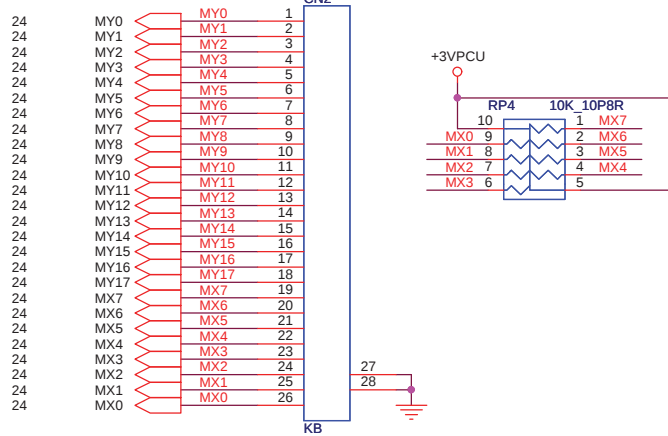


CPU nut PN : FBBU1001010 x 3 @ SHOLE1~3

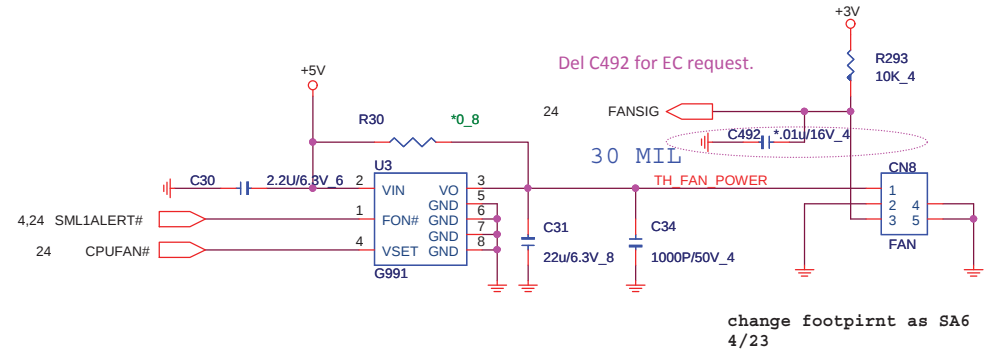
No stuff HOLE9 REV:B 02/17

PROJECT : ZQP Quanta Computer Inc.		
Size	Document Number	Rev
	LED/ EMI/ Screw Hole& Nut	1A
Date:	Tuesday, March 15, 2011	Sheet 22 of 32

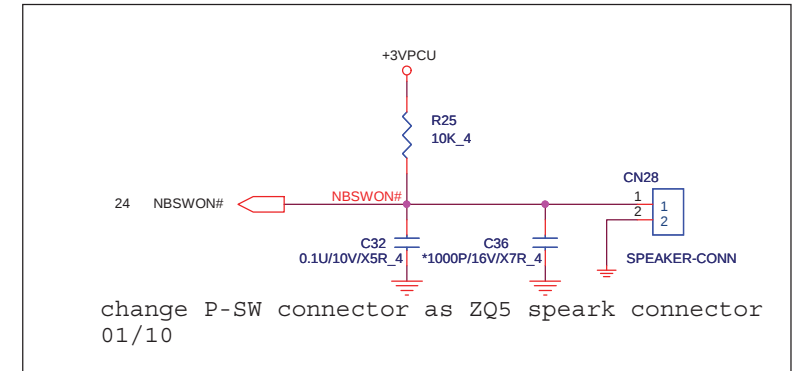
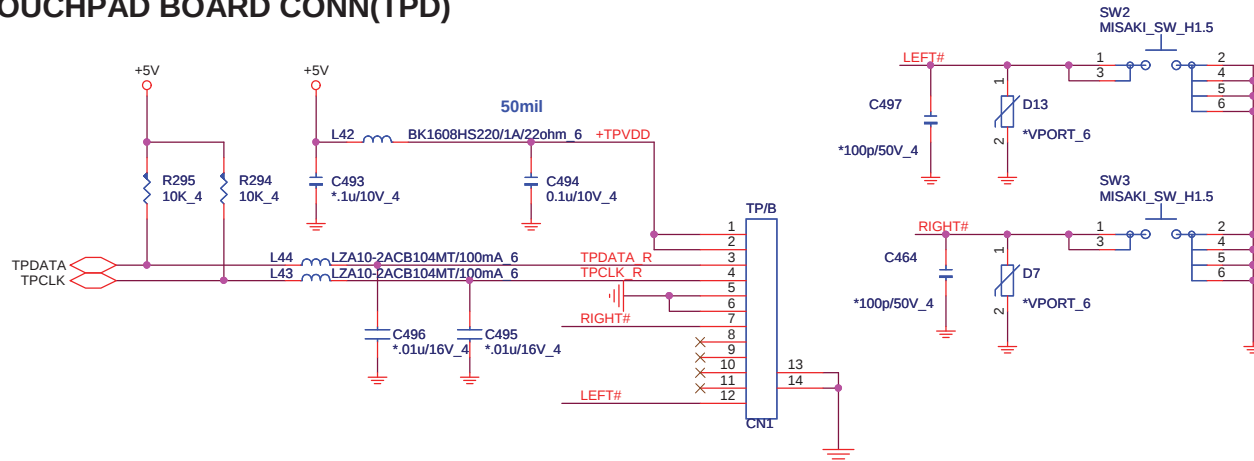
K/B(KBC)



CPU FAN(THM)



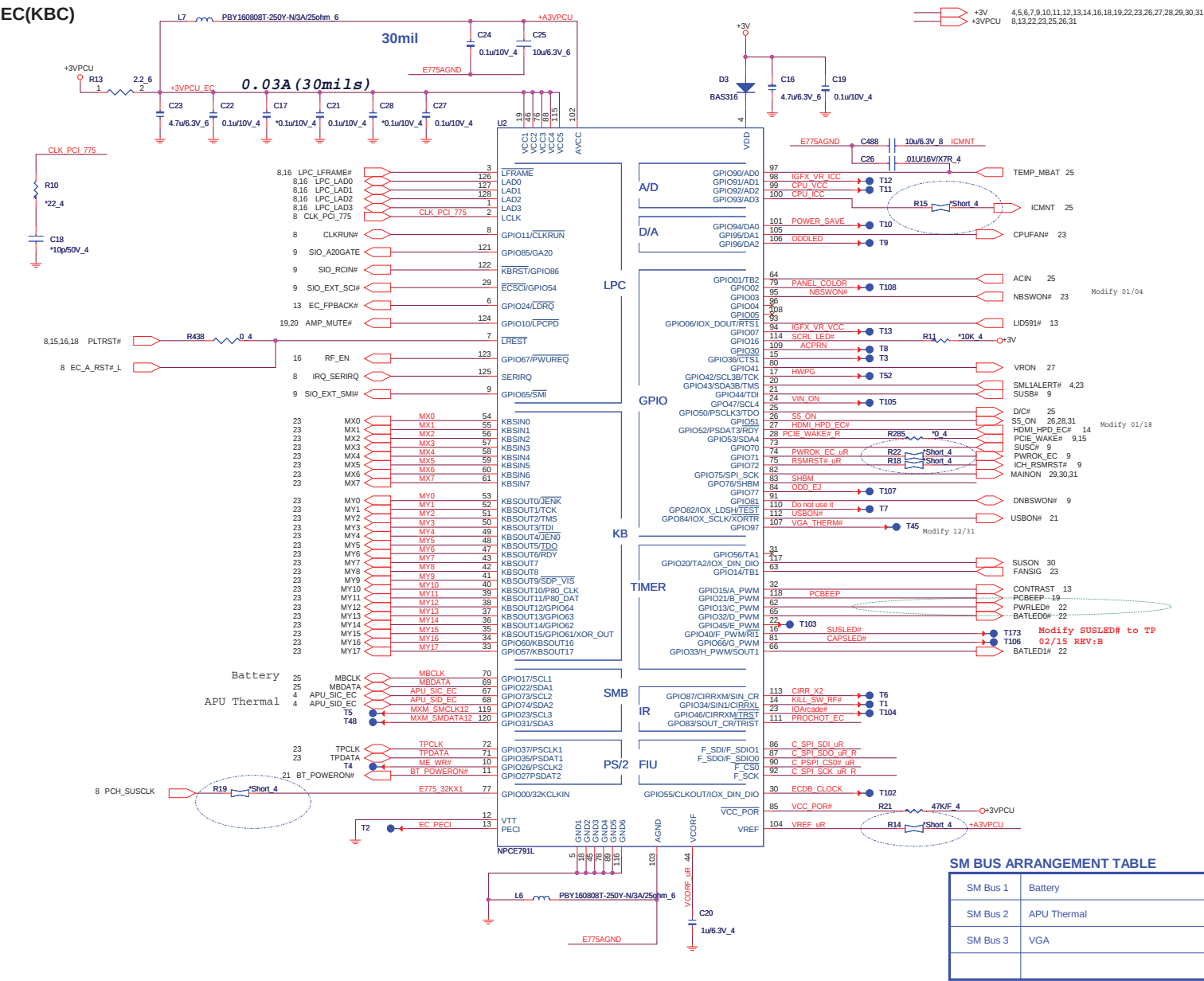
TOUCHPAD BOARD CONN(TPD)



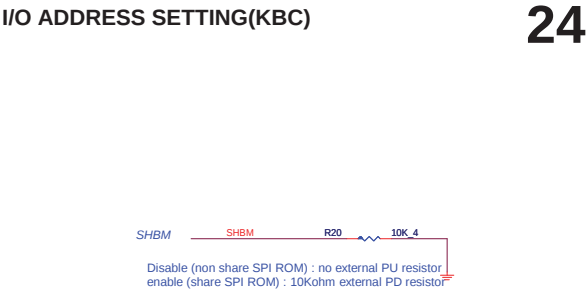
PROJECT : ZQP
Quanta Computer Inc.

Size	Document Number	Rev
	KB/TP/FAN	1A
Date:	Tuesday, March 15, 2011	Sheet 23 of 32

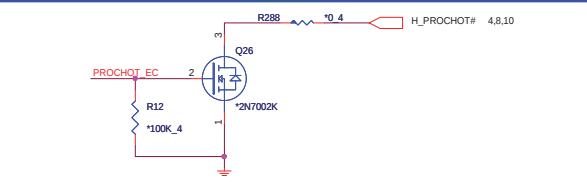
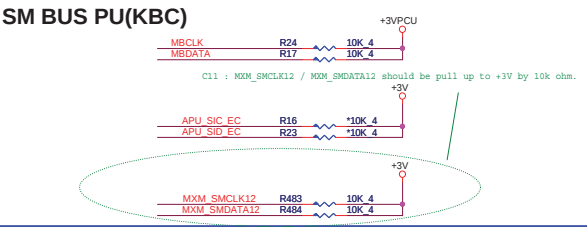
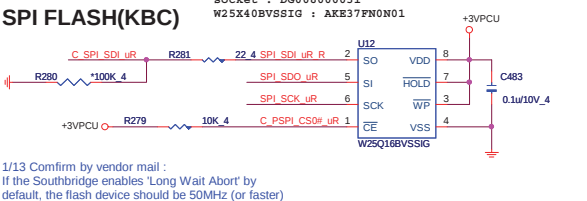
EC(KBC)



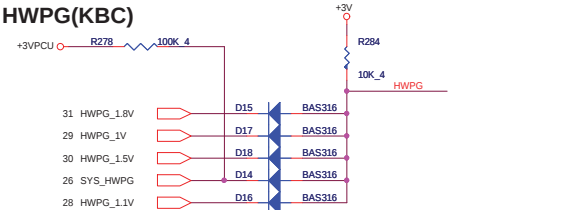
I/O ADDRESS SETTING(KBC)



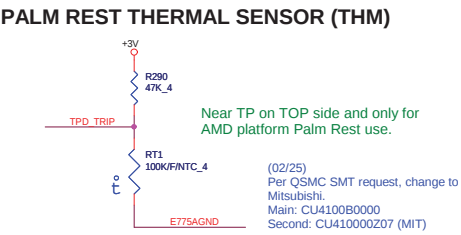
SM BUS PU(KBC)

**SPI FLASH(KBC)**

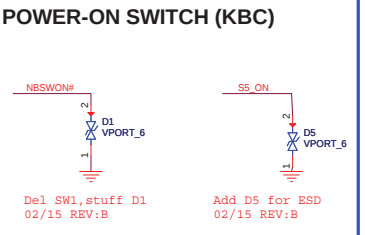
HWPG(KBC)



PALM REST THERMAL SENSOR (THM)

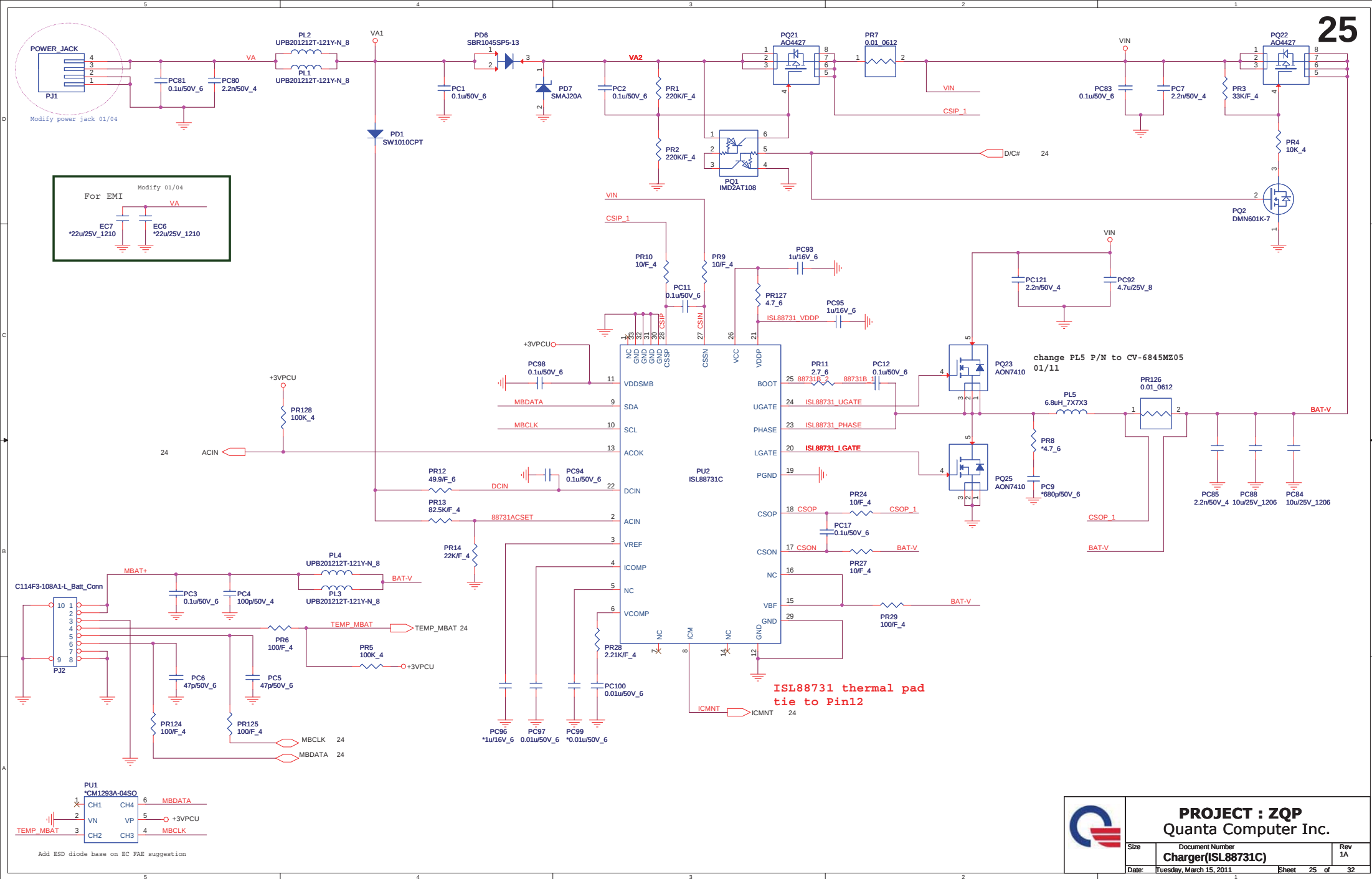


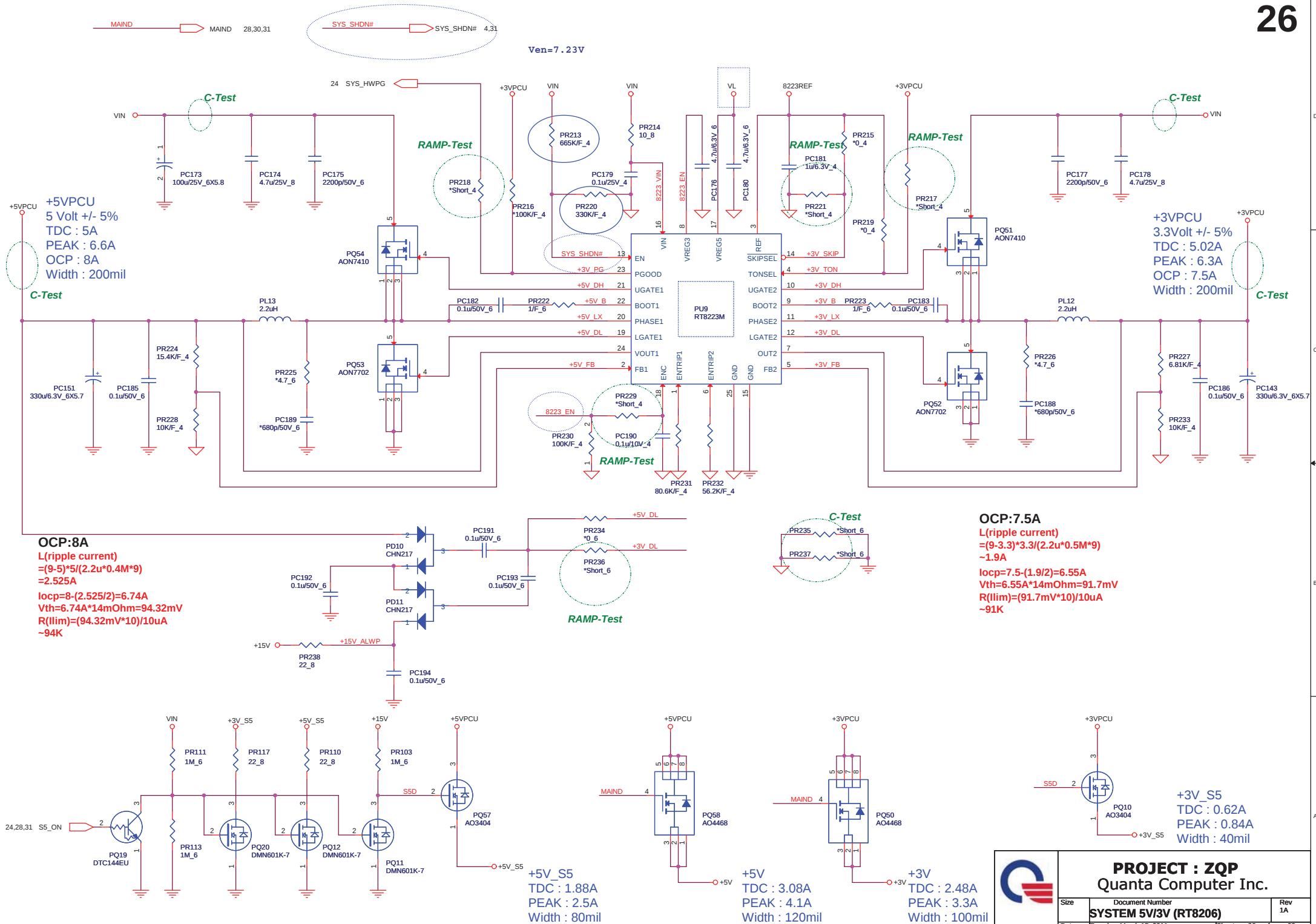
POWER-ON SWITCH (KBC)



SM BUS ARRANGEMENT TABLE

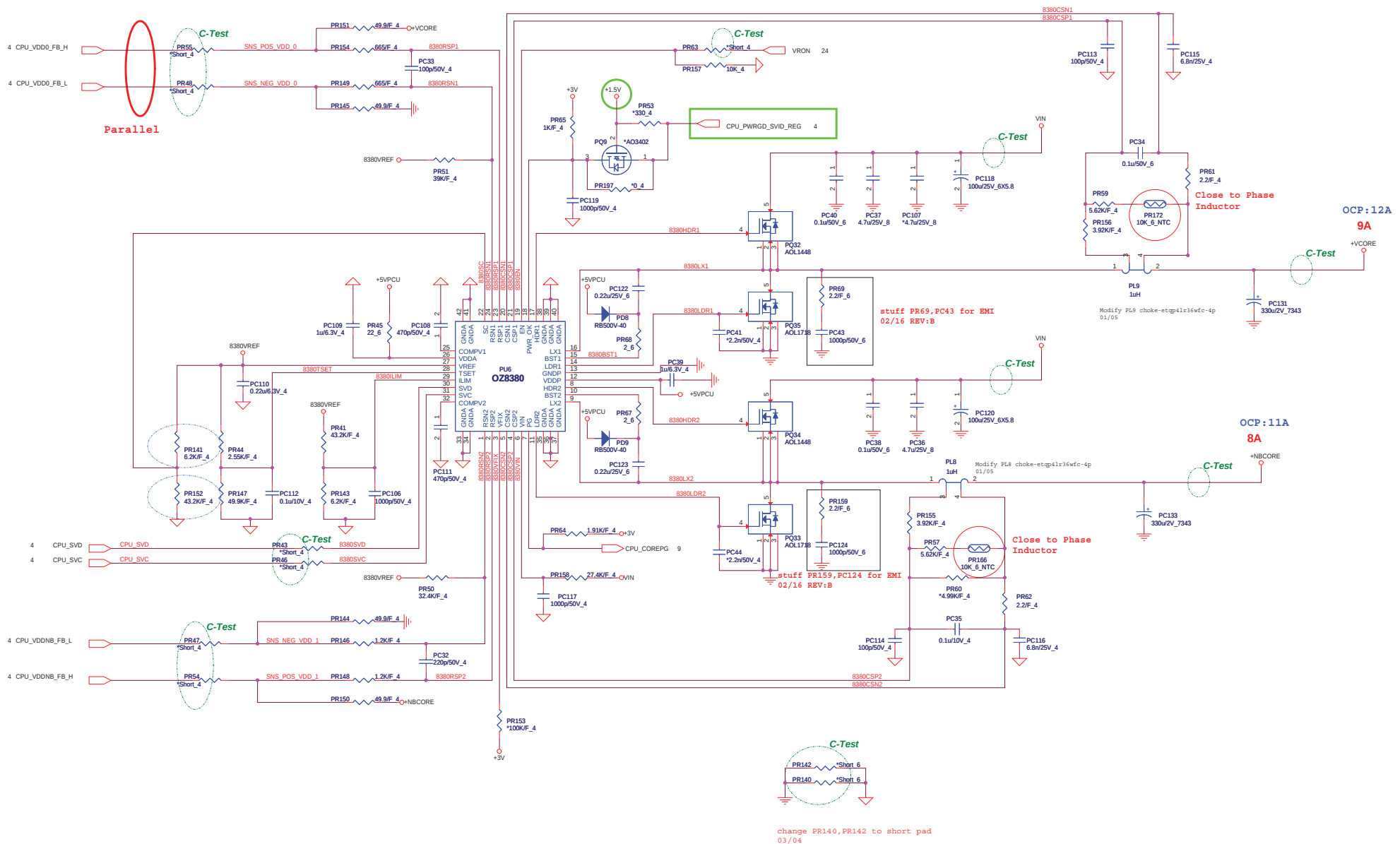
SM Bus 1	Battery
SM Bus 2	APU Thermal
SM Bus 3	VGA

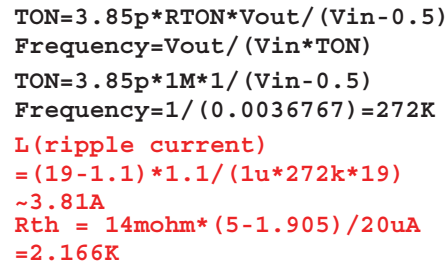




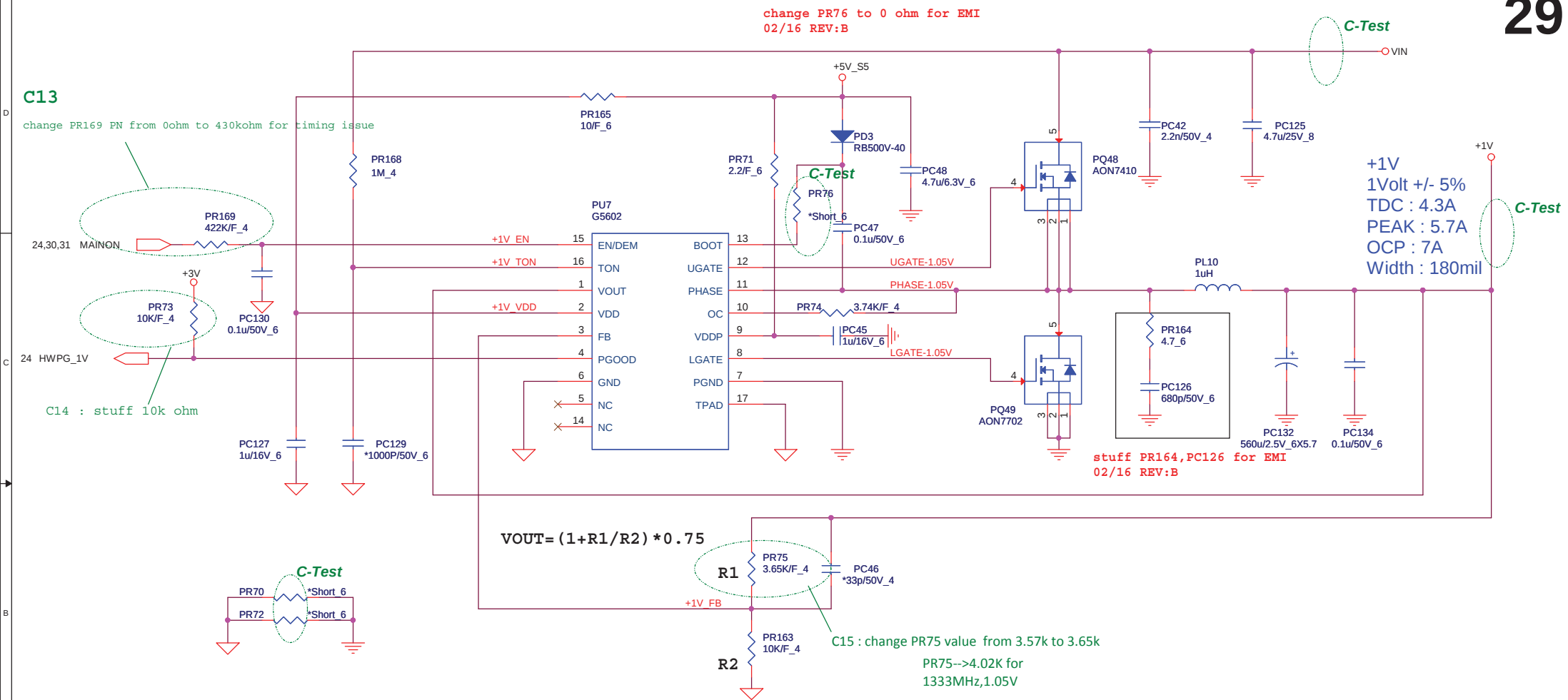
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Quanta Computer Inc.

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	SYSTEM 5V/3V (RT8206)	1A
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	Size	Document Number	Rev
		VCCP 1.1V(UP6111A)	1A
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$$\text{TON} = 3.85 \mu\text{s} \cdot \text{RTON} \cdot \text{Vout} / (\text{Vin} - 0.5)$$

$$\text{Frequency} = \text{Vout} / (\text{Vin} \cdot \text{TON})$$

$$\text{TON} = 3.85 \mu\text{s} \cdot 1\text{M} \cdot 1 / (\text{Vin} - 0.5)$$

$$\text{Frequency} = 1 / (0.0036767) = 272\text{K}$$

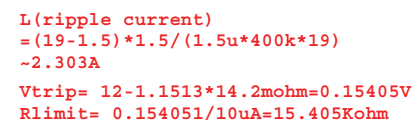
$$L(\text{ripple current}) = (19 - 1) \cdot 1 / (1 \mu\text{s} \cdot 272\text{k} \cdot 19)$$

$$\sim 3.483\text{A}$$

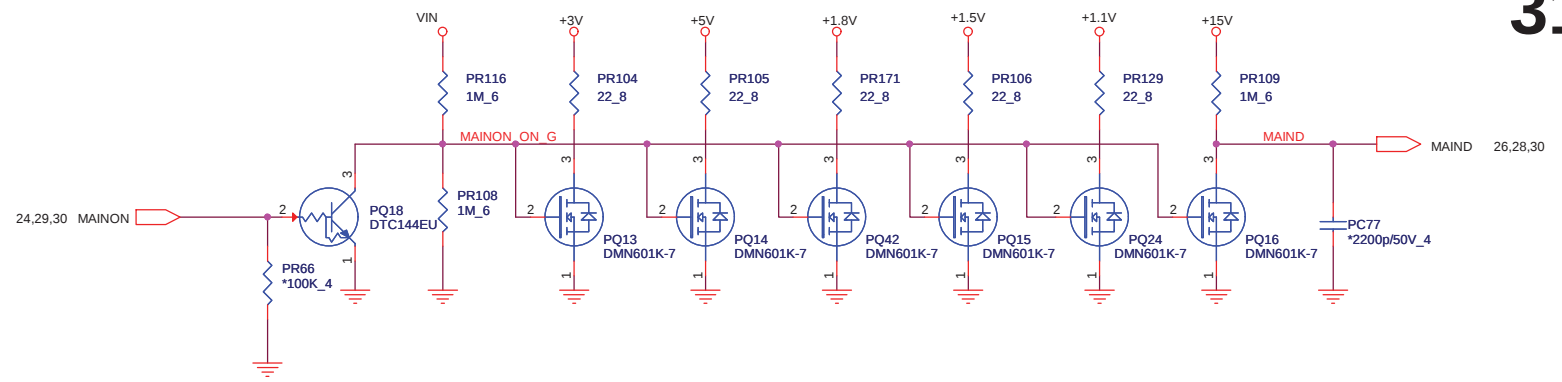
$$R_{\text{th}} = 14\text{mohm} \cdot (10 - 1.741) / 20\text{uA}$$

$$= 3.68\text{Kohm}$$

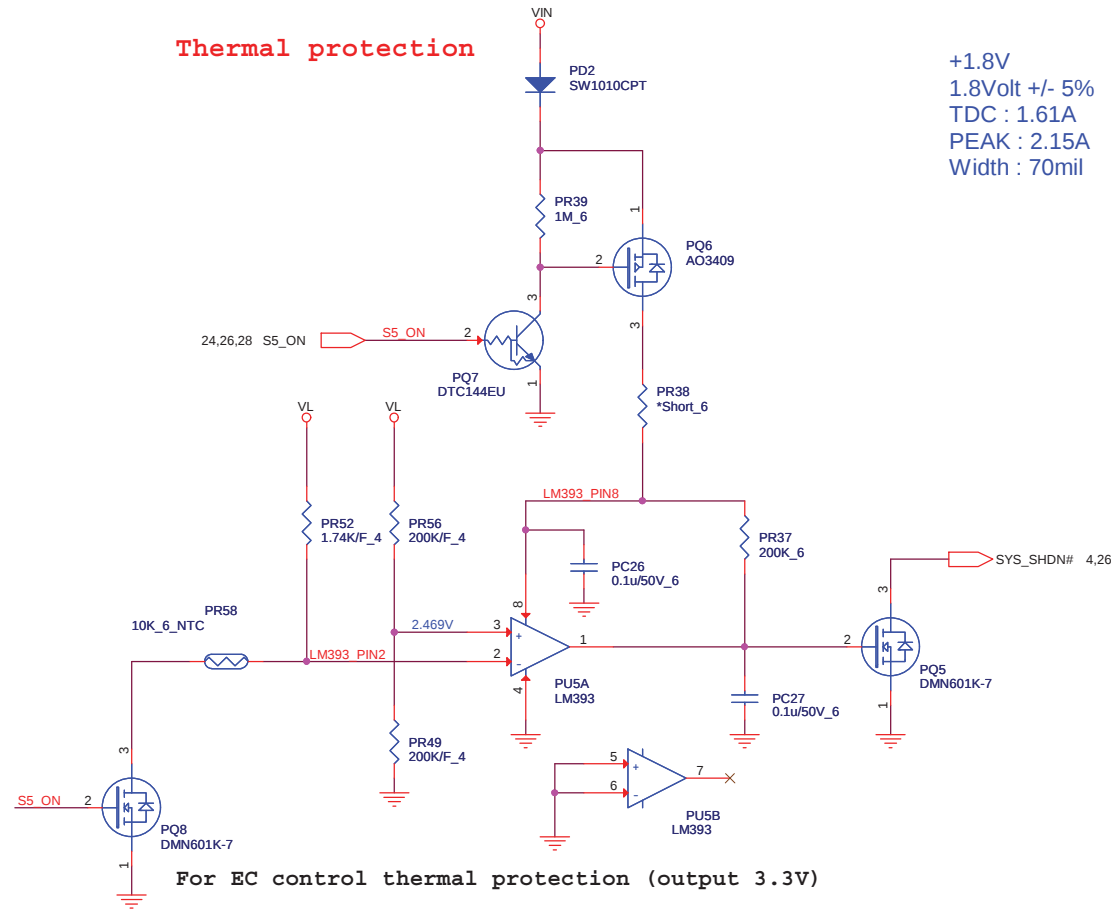
	PROJECT : ZQP Quanta Computer Inc.		
	Size	Document Number +1V(G5602)	Rev 1A
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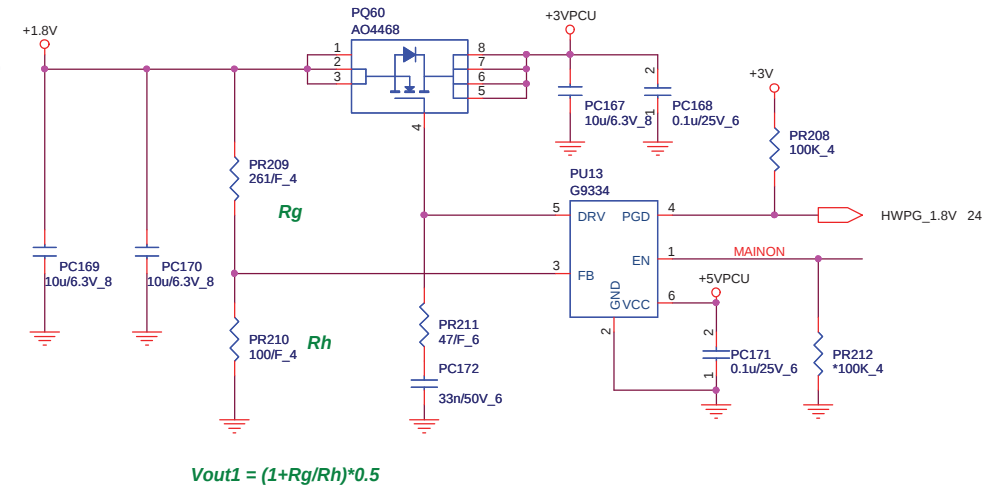
	S3	S5	+1.5VSUS	REF	VTT
S0	1	1	ON	ON	ON
S3	0	1	ON	ON	OFF
S4/S5	0	0	OFF	OFF	OFF



Thermal protection



+1.8V
1.8V ± 5%
TDC : 1.61A
PEAK : 2.15A
Width : 70mil



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	Discharge /Thermal protection	1A
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MODEL	REV	CHANGE LIST	Model ZQE/G M/B BOARD			
			Page	From	To	
ZQP/Q M/B	A	First Release	1	1A	3A	
			2	1A	3A	
			3	1A	3A	
01.P14: Add HDMI function 02.P22: Add EC53,EC54 for EMI 03.P20: Stuff C673/C675/C671/C672 for EMI 04.P15: Stuff ESD protector at R31/R32 for EMI 05.P10: GPIO 58 define to HDMI strap pin 06.P08: Add C606,C614,C619 for strong clock 07.P20:change C673,C675,C671,C672 for EMI 08.P19:change L48,L47,L35,L34 to CX08T601000 for EMI 09.P24:No stuff SW1,stuff D1 10.P24:Add D5 on S5_ON for ESD 11.P22:LED2 change single lens(blue) 12.P08:Del C623 13.P24:Del SW1 14.P13:Del R26,R27 and add RP5 for EMI 15.P15:Add EC38,EC40,EC43,EC46 for EMI 16.P28:change PR79 to 0 ohm and stuff PR77 and PC51 for EMI 17.P29:change PR76 to 0 ohm and stuff PR164,PC126 for EMI 18.P27:stuff PR69,PC43 for EMI 19.P17:change C617,C612,C539,C540 footprint form 1206 to 0805 20.P13:Swap USB nets between L50 and PR5 21.P13:Add R33,R34 for ESD 22.P15:change C354 to CH122GK1I10 for EMI 23.P22:change EC30,EC32,EC34,EC36,EC37,EC39,EC42,EC45,EC48,EC53 and stuff it for EMI 24.P26:Remove JP20,JP21,JP22,JP23 and change to short pad PR235,PR237 25.P27:Remove JP10,JP9,JP6,JP8 and change to short pad PR55,PR48,PR43,PR46,PR47,PR54,PR63,PR142,PR140 26.P28:Remove JP24,JP25 27.P29:Remove JP16,JP17 and change to short pad PR70,PR72 28.P30:Remove JP18,JP19 and change to short pad PR196,PR107 29.P22:No stuff HOLE9	B	4	1A	3A		
		5	1A	3A		
		6	1A	3A		
		7	1A	3A		
		8	1A	3A		
		9	1A	3A		
		10	1A	3A		
		11	1A	3A		
		12	1A	3A		
		13	1A	3A		
		14	1A	3A		
		15	1A	3A		
		16	1A	3A		
		17	1A	3A		
		18	1A	3A		
		19	1A	3A		
		20	1A	3A		
		21	1A	3A		
		22	1A	3A		
		23	1A	3A		
		24	1A	3A		
		25	1A	3A		
		26	1A	3A		
		27	1A	3A		
		28	1A	3A		
		29	1A	3A		
		01.P15:change RJ45 connector without LED 02.P27:change PR140,PR142 to short pad 03.P30:change PR119,PR123,PR102 to short pad 04.P26:change PR217,PR218,PR221,PR229,PR236 to short pad 05.P29:change PR76 to short pad 06.P28:change PR79 to short pad	B	30	1A	3A
				31	1A	3A
				32	1A	3A
33	1A			3A		
34	1A			3A		
35	1A			3A		
36	1A			3A		
37	1A			3A		
38	1A			3A		
39	1A			3A		
40	1A			3A		
			41	1A	3A	
Quanta Computer Inc. ZQP/Q		PROJECT : ZQP Quanta Computer Inc. Size Document Number CHANGE LIST - 3A Date: Tuesday, March 15, 2011 Rev 1A Sheet 32 of 32				
				DOC. NO :		
APPROVED BY : Andy Lin		CHECK BY : JC Huang	DRAWING BY : Andy Chen	DATE :10/18/2010	SHEET 1	