# Compal Confidential

## JALB0 Schematics Document

### AMD Griffin Processor with RS780M+SB700

### (With ATI MXM/B)

**2008-8-14**

**REV:2.0**



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| | | | Date: Thursday, August 14, 2008 / Sheet 1 of 50 |

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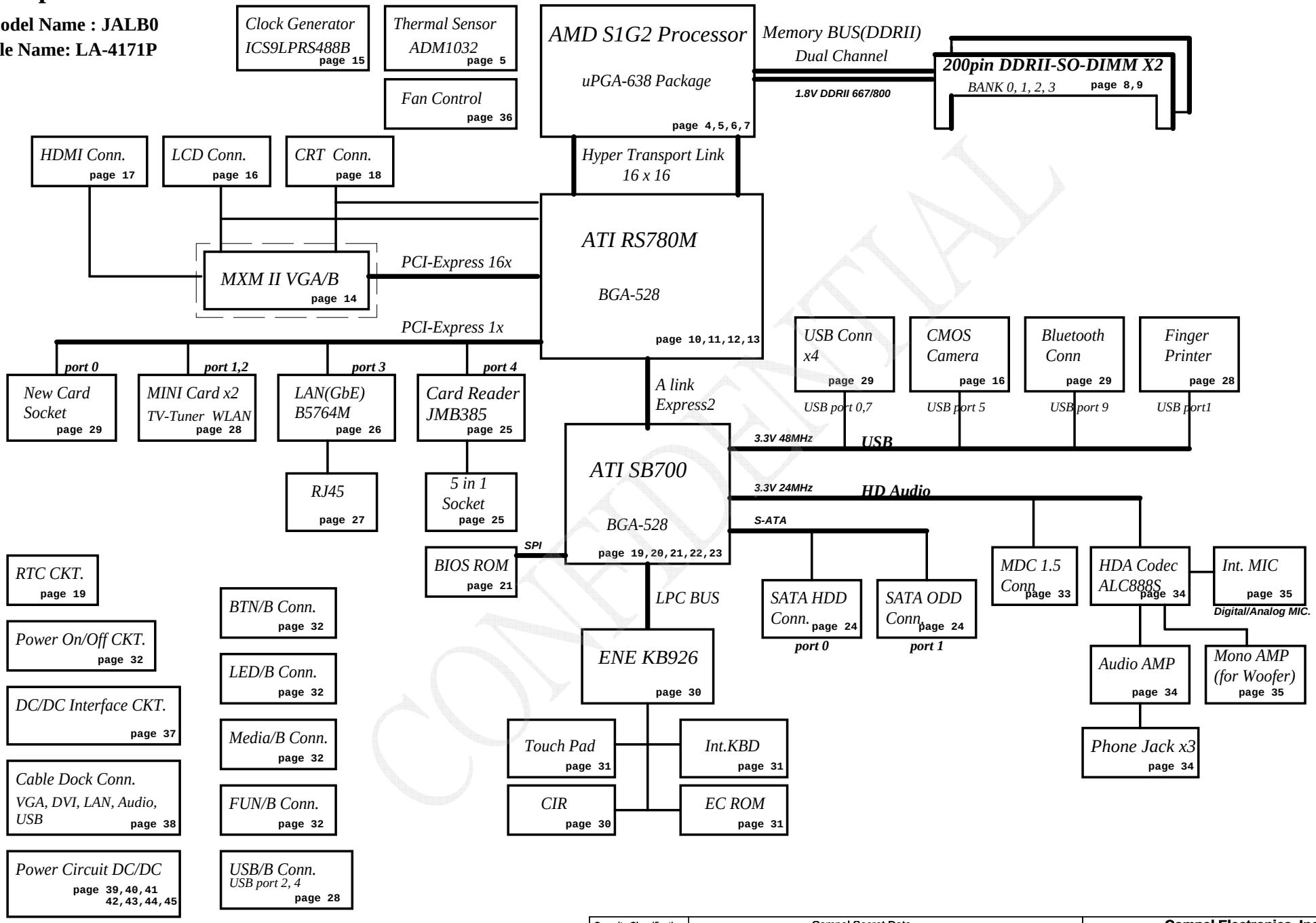
**Model Name : JALB0**
**File Name: LA-4171P**



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## Voltage Rails

| Power Plane | Description | S1 | S3 | S5 |
|---|---|---|---|---|
| VIN | Adapter power supply (19V) | N/A | N/A | N/A |
| B+ | AC or battery power rail for power circuit. | N/A | N/A | N/A |
| +CPU_CORE_0 | Core voltage for CPU | ON | OFF | OFF |
| +CPU_CORE_1 | Core voltage for CPU | ON | OFF | OFF |
| +CPU_CORE_NB | Core voltage for CPU | ON | OFF | OFF |
| +0.9V | 0.9V switched power rail for DDR terminator | ON | ON | OFF |
| +1.1VS | 1.05V switched power rail | ON | OFF | OFF |
| +1.2V_HT | 1.25V switched power rail | ON | OFF | OFF |
| +NB_CORE | 1.0V~1.1V switched power rail for NB VDDC | ON | OFF | OFF |
| +1.5VS | 1.5V power rail for PCIE Card | ON | OFF | OFF |
| +1.8V | 1.8V power rail for CPU VDDIO and DDR | ON | ON | OFF |
| +1.8VS | 1.8V switched power rail | ON | OFF | OFF |
| +2.5VS | 2.5V for CPU_VDDA and MXM/B | ON | OFF | OFF |
| +3VALW | 3.3V always on power rail | ON | ON | ON* |
| +3V_LAN | 3.3V power rail for LAN | ON | ON | ON |
| +3VS | 3.3V switched power rail | ON | OFF | OFF |
| +5VALW | 5V always on power rail | ON | ON | ON* |
| +5VS | 5V switched power rail | ON | OFF | OFF |
| +VSB | VSB always on power rail | ON | ON | ON* |
| +RTCVCC | RTC power | ON | ON | ON |

**Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.**

## External PCI Devices

| Device | IDSEL# | REQ#/GNT# | Interrupts |
|---|---|---|---|

No PCI device

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 011X b |
| EEPROM(24C16/02) | 1010 000X b |
| MXM GMT G781-1 | 1001 101X b |

## EC SM Bus2 address

| Device | Address |
|---|---|
| ADI ADM1032 | 1001 100X b |
| CPU SB | 1001 101X b |

## SB700 SM Bus 0 address

| Device | Address |
|---|---|
| Clock Generator (ICS9LPRS365) | 1101 001Xb |
| DDR DIMM0 | 1001 000Xb |
| DDR DIMM2 | 1001 010Xb |
| Minicard | |
| Minicard | |

## SB700 SM Bus 1 address

| Device | Address |
|---|---|
| New card | |
| Lan | |

| STATE \ SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |

## Board ID / SKU ID Table for AD channel

| | |
|---|---|
| Vcc | 3.3V +/- 5% |
| Ra/Rc/Re | 100K +/- 5% |

| Board ID | Rb / Rd / Rf | $V_{AD\_BID}$ min | $V_{AD\_BID}$ typ | $V_{AD\_BID}$ max |
|---|---|---|---|---|
| 0 | 0 | 0 V | 0 V | 0 V |
| 1 | 8.2K +/- 5% | 0.216 V | 0.250 V | 0.289 V |
| 2 | 18K +/- 5% | 0.436 V | 0.503 V | 0.538 V |
| 3 | 33K +/- 5% | 0.712 V | 0.819 V | 0.875 V |
| 4 | 56K +/- 5% | 1.036 V | 1.185 V | 1.264 V |
| 5 | 100K +/- 5% | 1.453 V | 1.650 V | 1.759 V |
| 6 | 200K +/- 5% | 1.935 V | 2.200 V | 2.341 V |
| 7 | NC | 2.500 V | 3.300 V | 3.300 V |

## BOARD ID Table

| Board ID | PCB Revision |
|---|---|
| 0 | 0.1 |
| 1 | 0.2 |
| * 2 | 0.3 0.4 1.0 |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |

## BTO Option Table

| BTO Item | BOM Structure |
|---|---|
| Discrete | VGA@ |
| UMA | UMA@ |
| | |
| | |
| | |
| | |
| | |

## PROJECT ID Table

| Board ID | PROJECT |
|---|---|
| 0 | JALB0 |
| 1 | JALC0 |
| 2 | |
| 3 | |
| 4 | |
| 5 | |
| 6 | |
| 7 | |



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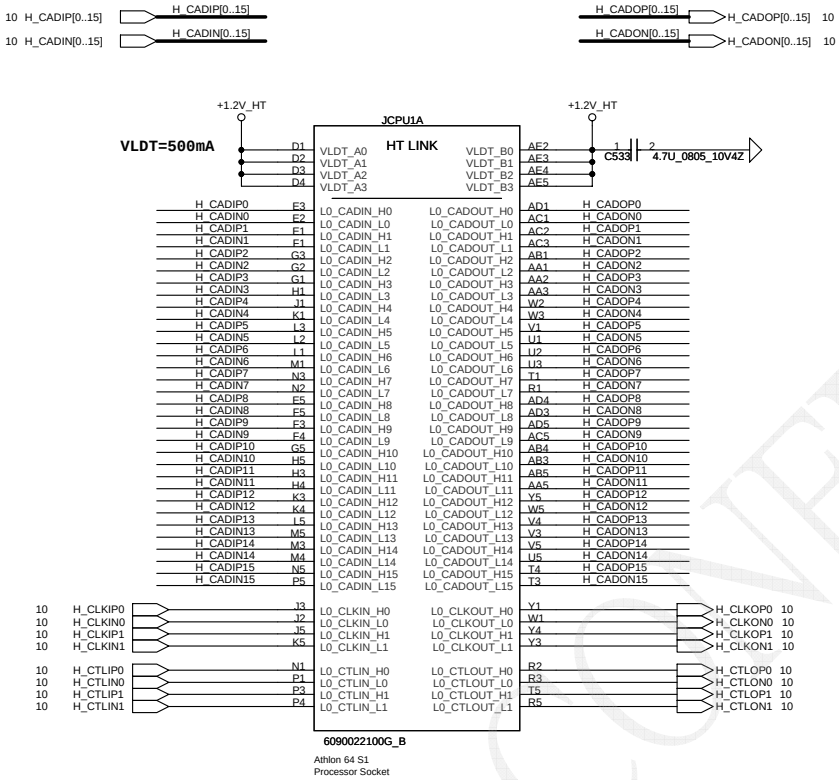


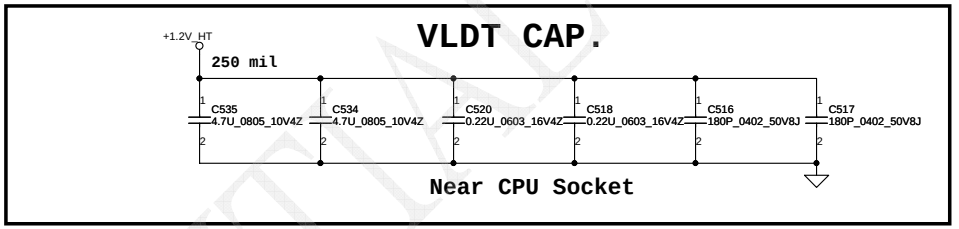




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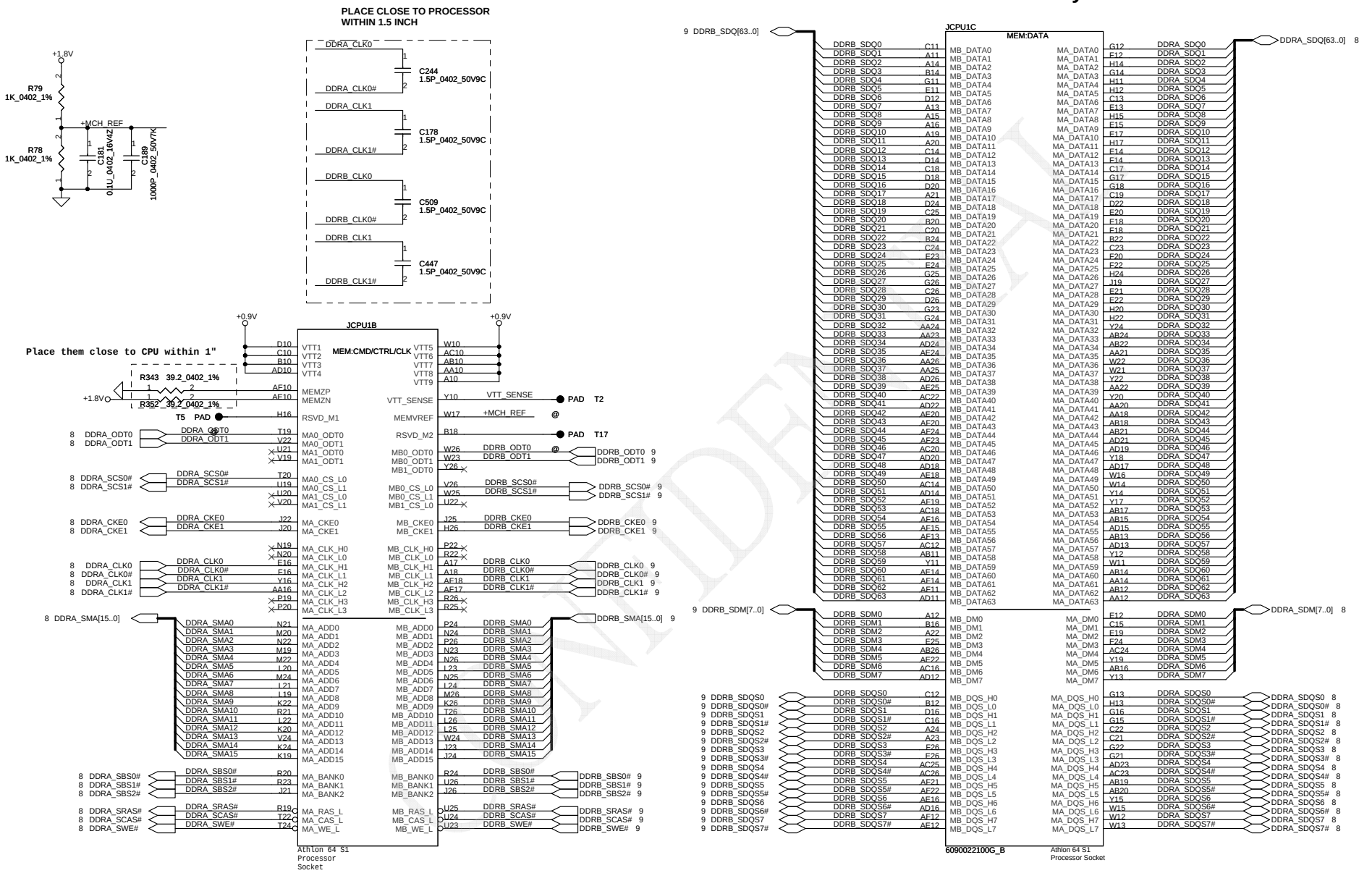
# Processor DDR2 Memory Interface



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A:Need to re-Link "SGN00000200"

+2.5VS

L33 FBM_L11_201209_300L_0805

+2.5VDDA VDDA=300mA

3300P_0402_50V7K

C282 150U_D2_6.3VM

C264 4.7U_0805_10V4Z

C255

C261 0.22U_0603_16V4Z

<BOM Structure>

JCPU1D

6090022100G_B

15 CLK_CPU_BCLK C531 3900P_0402_50V7K CPU_CLKIN_SC_P

CPU_CLKIN_SC_N

R409 169_0402_1%

15 CLK_CPU_BCLK# C532 3900P_0402_50V7K

11 CPU_LDT_REQ#

Address:100_1100

Place close to CPU wihtin 1.5"

+1.8VS

R420 300_0402_5%

19 LDT_RST# C554 0.01U_0402_16V7K

R419 300_0402_5%

19 H_PWRGD C553 0.01U_0402_16V7K

R113 300_0402_5%

11,19 LDT_STOP# C245 0.01U_0402_16V7K

+CPU_CORE_0 R92 10_0402_5% R95 10_0402_5% Close to CPU

+CPU_CORE_1 R80 10_0402_5% R81 10_0402_5%

+1.2V_HT R82 44.2_0402_1% R86 44.2_0402_1%

R356 1K_0402_5%

T10 PAD T27 PAD T28 PAD T21 PAD T22 PAD T23 PAD T24 PAD T25 PAD T26 PAD

R108 510_0402_5% R107 510_0402_5% R418 0_0402_5%

CPU internal thermal sensor

C436 0.1U_0402_16V4Z

R351 20K_0402_5%

R360 34.8K_0402_1%~N

+3VS

2.09V for Gate

R361 2.2K_0402_5%

R564 0_0402_5%

Q31 FDV301N_NL_SOT23-3

R565 0_0402_5%

Q30 FDV301N_NL_SOT23-3

R365 2.2K_0402_5%

R566 0_0402_5%

R567 0_0402_5%

R568 0_0402_5%

R569 0_0402_5%

ICH_SMBDATA1 20,26,29

EC_SMB_DA1 14,30,40

ICH_SMBCLK1 20,26,29

EC_SMB_CK1 14,30,40

EC is PU to 5VALW

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

C446 0.1U_0402_16V4Z

C449 2200P_0402_50V7K

U27 ADM1032ARMZ_MSOP8

THERMDA_CPU THERMDC_CPU

EC_SMB_CK2 EC_SMB_CK2 30,31

EC_SMB_DA2 EC_SMB_DA2 30,31

2200p change to
1000p for ADT7421

Address:100_1101

R364 10K_0402_5%

R358 300_0402_5%

Q32 MMBT3904_NL_SOT23-3

CPU_THERMTRIP#_R

R335 @0_0402_5%

R334 0_0402_5%

MAINPWON 40,41

H_THERMTRIP# 20

R357 300_0402_5%

H_PROCHOT#

R370 0_0402_5%

H_PROCHOT# 19

R353 300_0402_5%

CPU_THERMTRIP#_R

H_PROCHOT#

CPU_MEMHOT# 1.8V

+1.8V

THERMDC_CPU

THERMDA_CPU

T30 T29 @PAD @PAD

+1.8V sense no support

CPU_VDD0_FB_H CPU_VDD0_FB_L

CPU_VDD1_FB_H CPU_VDD1_FB_L

CPU_VDDNB_FB_H CPU_VDDNB_FB_L

+CPU_CORE_NB R101 10_0402_5% R106 10_0402_5% Close to CPU

CPU_DBRDY CPU_TMS CPU_TCK CPU_TRST# CPU_TDI

CPU_DBREQ# CPU_TDO

CPU_TEST23_TSTUPD

CPU_TEST18_PLLTEST1 CPU_TEST19_PLLTEST0

CPU_TEST21_SCANEN CPU_TEST20_SCANCLK2 CPU_TEST24_SCANCLK1 CPU_TEST22_SCANSHIFTEN CPU_TEST12_SCANSHIFTENB CPU_TEST27_SINGLECHAIN

CPU_TEST28_H_PLLCHRZ_P CPU_TEST28_L_PLLCHRZ_N

route as differential as short as possible testpoint under package

CPU_TEST17_BP3 CPU_TEST16_BP2 CPU_TEST15_BP1 CPU_TEST14_BP0

PAD T3 PAD T4 PAD T16 PAD T7 PAD T6 PAD T9

CPU_TEST29_H_FBCLKOUT_P CPU_TEST29_L_FBCLKOUT_N

PAD T8 PAD T15

0718 AMD --> 1K ohm

CPU_SVC CPU_SVD

R415 1K_0402_5% R416 1K_0402_5%

CPU_TEST21_SCANEN CPU_TEST24_SCANCLK1 R538 300_0402_5% R539 300_0402_5%

JP29 ACES_85201-1005N

HDT Connector

JP1 SAMTEC_ASP-68200-07

R112 220_0402_5% R115 220_0402_5% R118 220_0402_5% R119 220_0402_5% R123 300_0402_5%

NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.

R93 0_0402_5%

U8 @NC7SZ08P5X_NL_SC70-5

HDT_RST# LDT_RST# SB_PWRGD 20,32



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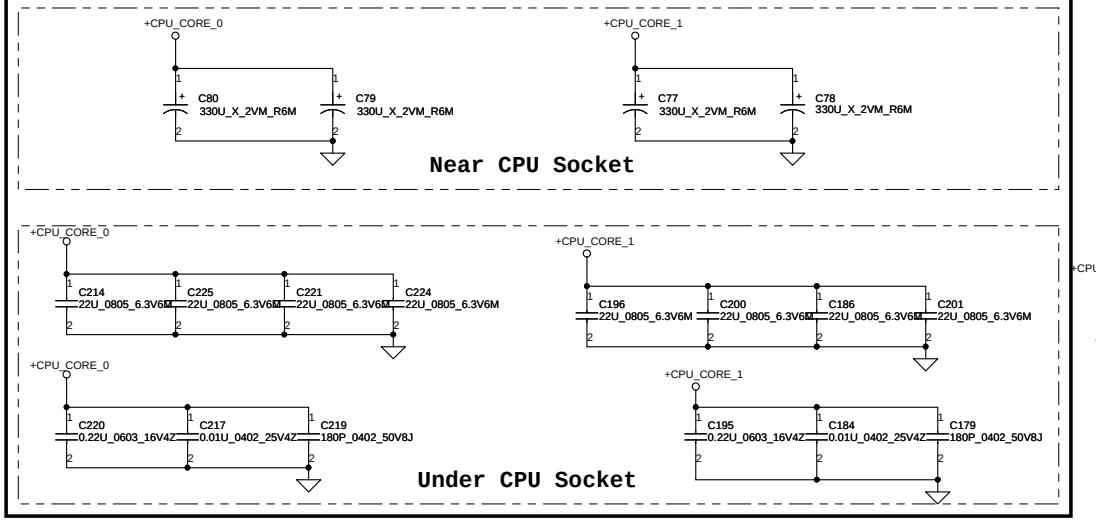
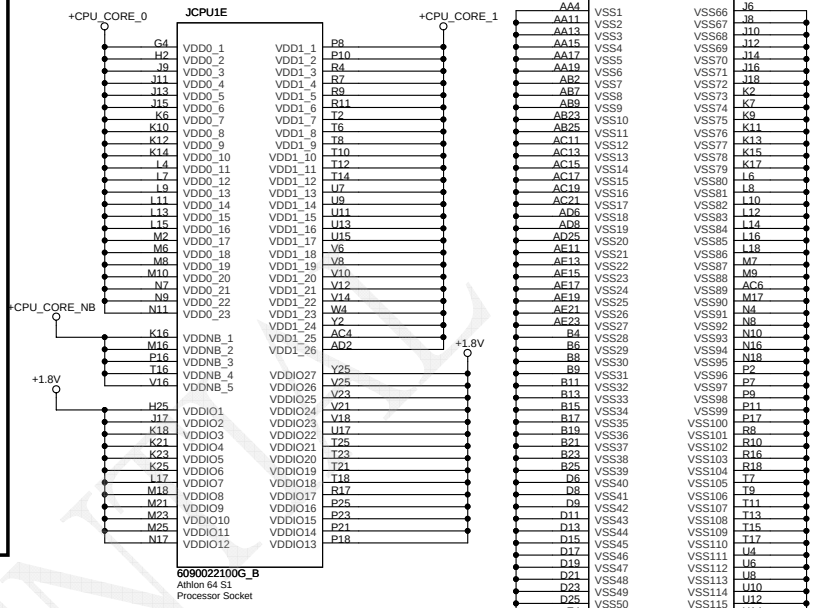
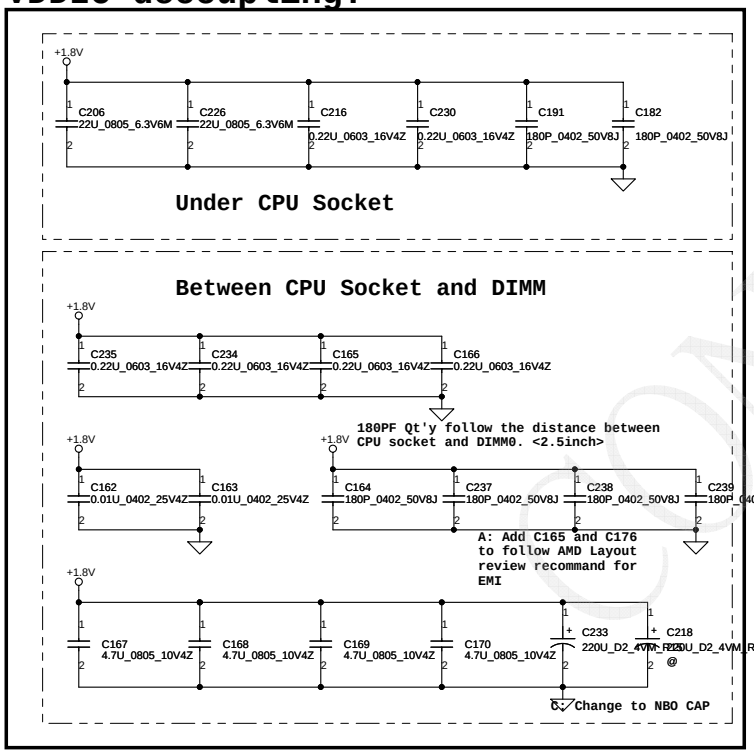
# VDD(+CPU_CORE) decoupling.

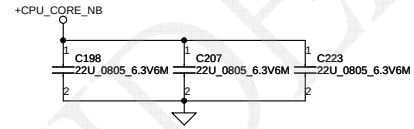


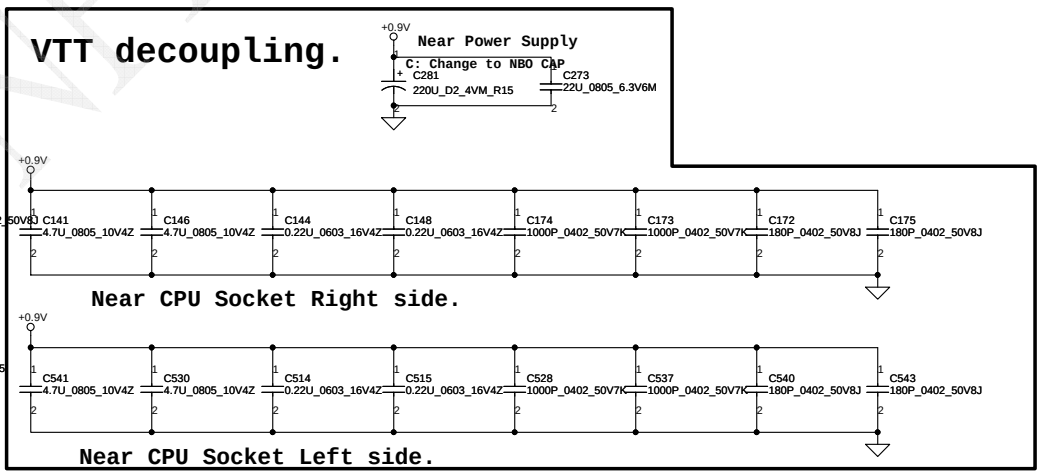

# VDDIO decoupling.




# +CPU_CORE_NB decoupling.




# VTT decoupling.



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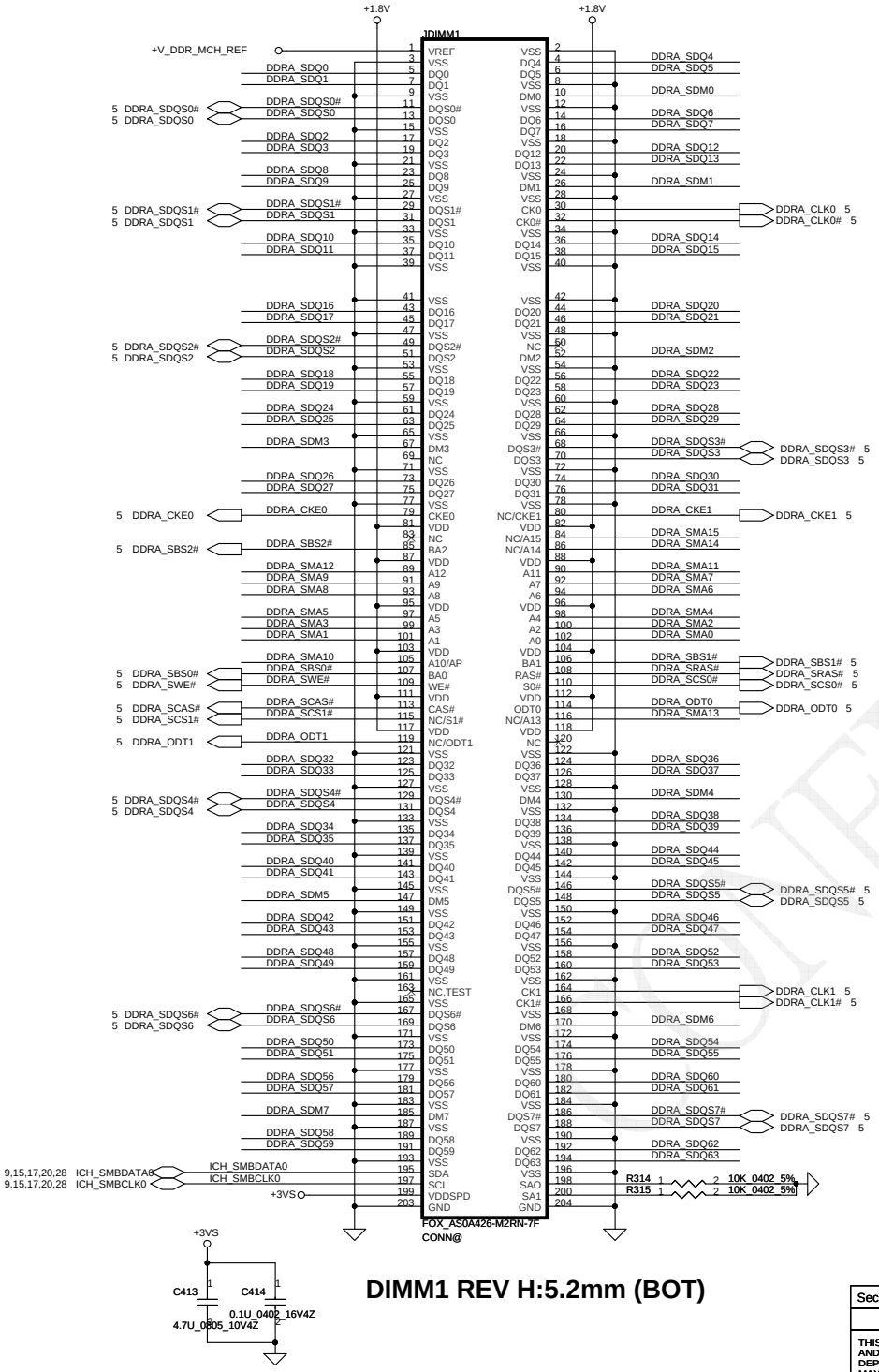
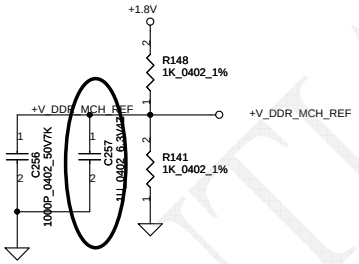
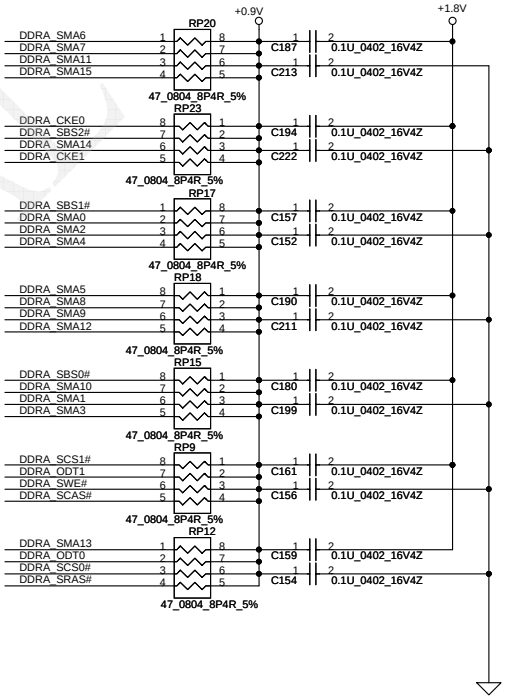



**DIMM1 REV H:5.2mm (BOT)**

DDRA_SDQ[0..63] → DDRA_SDQ[0..63] 5
DDRA_SDM[0..7] → DDRA_SDM[0..7] 5
DDRA_SMA[0..15] → DDRA_SMA[0..15] 5




RESERVE
+V_DDR_MCH_REF BUFFER CIRCUIT



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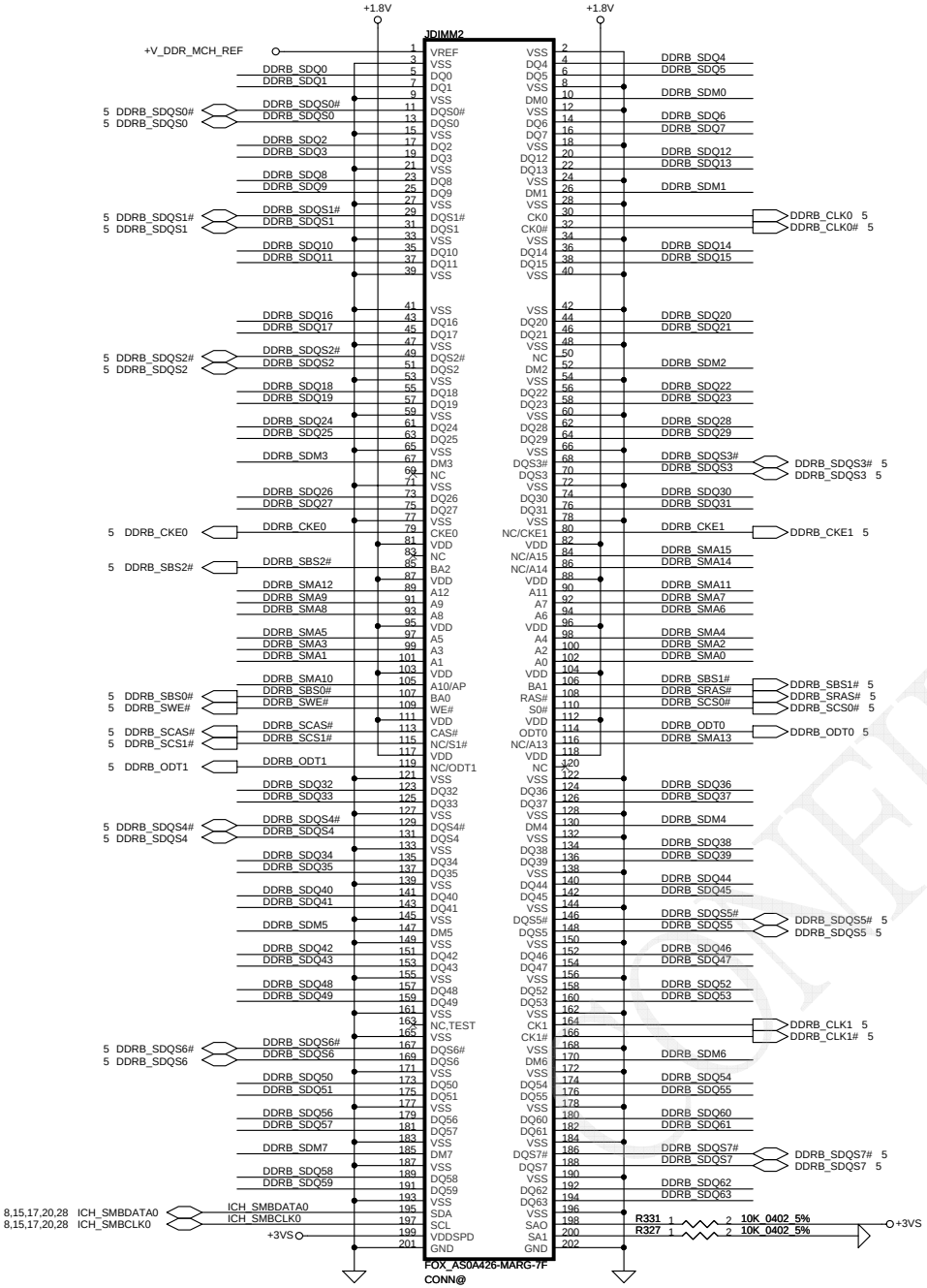
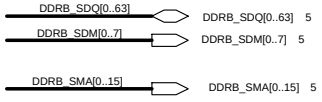
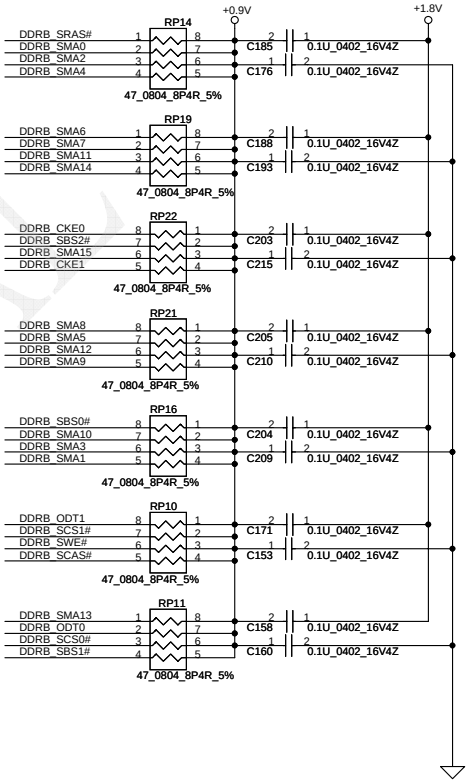



**DIMM1 REV H:9.2mm (BOT)**



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14 PCIE_GTX_C_MRX_P[0..15] → PCIE_GTX_C_MRX_P[0..15]

14 PCIE_GTX_C_MRX_N[0..15] → PCIE_GTX_C_MRX_N[0..15]

PCIE_MTX_C_GRX_P[0..15] → PCIE_MTX_C_GRX_P[0..15] 14

PCIE_MTX_C_GRX_N[0..15] → PCIE_MTX_C_GRX_N[0..15] 14

U25B

**PART 2 OF 6**

**PCIE I/F GFX**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| PCIE_GTX_C_MRX_P0 | D4 | GFX_RX0P | GFX_TX0P | A5 | PCIE_MTX_GRX_P0 | | C451 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P0 |
| PCIE_GTX_C_MRX_N0 | C4 | GFX_RX0N | GFX_TX0N | B5 | PCIE_MTX_GRX_N0 | C450 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N0 |
| PCIE_GTX_C_MRX_P1 | A3 | GFX_RX1P | GFX_TX1P | A4 | PCIE_MTX_GRX_P1 | | C467 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P1 |
| PCIE_GTX_C_MRX_N1 | B3 | GFX_RX1N | GFX_TX1N | B4 | PCIE_MTX_GRX_N1 | C466 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N1 |
| PCIE_GTX_C_MRX_P2 | C2 | GFX_RX2P | GFX_TX2P | C3 | PCIE_MTX_GRX_P2 | | C453 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P2 |
| PCIE_GTX_C_MRX_N2 | C1 | GFX_RX2N | GFX_TX2N | B2 | PCIE_MTX_GRX_N2 | C452 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N2 |
| PCIE_GTX_C_MRX_P3 | E5 | GFX_RX3P | GFX_TX3P | D1 | PCIE_MTX_GRX_P3 | | C469 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P3 |
| PCIE_GTX_C_MRX_N3 | F5 | GFX_RX3N | GFX_TX3N | D2 | PCIE_MTX_GRX_N3 | C468 1 | 2 | 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N3 |
| PCIE_GTX_C_MRX_P4 | G5 | GFX_RX4P | GFX_TX4P | E2 | PCIE_MTX_GRX_P4 | | C455 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P4 |
| PCIE_GTX_C_MRX_N4 | G6 | GFX_RX4N | GFX_TX4N | E1 | PCIE_MTX_GRX_N4 | C454 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N4 |
| PCIE_GTX_C_MRX_P5 | H5 | GFX_RX5P | GFX_TX5P | F4 | PCIE_MTX_GRX_P5 | | C471 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P5 |
| PCIE_GTX_C_MRX_N5 | H6 | GFX_RX5N | GFX_TX5N | F3 | PCIE_MTX_GRX_P6 | C470 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N5 |
| PCIE_GTX_C_MRX_P6 | J6 | GFX_RX6P | GFX_TX6P | F1 | PCIE_MTX_GRX_N6 | | C457 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P6 |
| PCIE_GTX_C_MRX_N6 | J5 | GFX_RX6N | GFX_TX6N | F2 | PCIE_MTX_GRX_P7 | C456 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N6 |
| PCIE_GTX_C_MRX_P7 | J7 | GFX_RX7P | GFX_TX7P | H4 | PCIE_MTX_GRX_N7 | | C473 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P7 |
| PCIE_GTX_C_MRX_N7 | J8 | GFX_RX7N | GFX_TX7N | H3 | PCIE_MTX_GRX_P8 | C472 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N7 |
| PCIE_GTX_C_MRX_P8 | L5 | GFX_RX8P | GFX_TX8P | H2 | PCIE_MTX_GRX_N8 | | C459 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P8 |
| PCIE_GTX_C_MRX_N8 | L6 | GFX_RX8N | GFX_TX8N | H1 | PCIE_MTX_GRX_P9 | C458 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N8 |
| PCIE_GTX_C_MRX_P9 | M8 | GFX_RX9P | GFX_TX9P | J2 | PCIE_MTX_GRX_N9 | | C475 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P9 |
| PCIE_GTX_C_MRX_N9 | L8 | GFX_RX9N | GFX_TX9N | J1 | PCIE_MTX_GRX_P10 | C474 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N9 |
| PCIE_GTX_C_MRX_P10 | P7 | GFX_RX10P | GFX_TX10P | K4 | PCIE_MTX_GRX_N10 | | C461 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P10 |
| PCIE_GTX_C_MRX_N10 | M7 | GFX_RX10N | GFX_TX10N | K3 | PCIE_MTX_GRX_P11 | C460 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N10 |
| PCIE_GTX_C_MRX_P11 | P5 | GFX_RX11P | GFX_TX11P | K1 | PCIE_MTX_GRX_N11 | | C477 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P11 |
| PCIE_GTX_C_MRX_N11 | M5 | GFX_RX11N | GFX_TX11N | K2 | PCIE_MTX_GRX_P12 | C476 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N11 |
| PCIE_GTX_C_MRX_P12 | R8 | GFX_RX12P | GFX_TX12P | M4 | PCIE_MTX_GRX_N12 | | C463 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P12 |
| PCIE_GTX_C_MRX_N12 | P8 | GFX_RX12N | GFX_TX12N | M3 | PCIE_MTX_GRX_P13 | C462 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N12 |
| PCIE_GTX_C_MRX_P13 | R6 | GFX_RX13P | GFX_TX13P | M1 | PCIE_MTX_GRX_N13 | | C479 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P13 |
| PCIE_GTX_C_MRX_N13 | R5 | GFX_RX13N | GFX_TX13N | M2 | PCIE_MTX_GRX_P14 | C478 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N13 |
| PCIE_GTX_C_MRX_P14 | P4 | GFX_RX14P | GFX_TX14P | N2 | PCIE_MTX_GRX_N14 | | C465 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P14 |
| PCIE_GTX_C_MRX_N14 | P3 | GFX_RX14N | GFX_TX14N | N1 | PCIE_MTX_GRX_P15 | C464 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N14 |
| PCIE_GTX_C_MRX_P15 | T4 | GFX_RX15P | GFX_TX15P | P1 | PCIE_MTX_GRX_N15 | | C481 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_P15 |
| PCIE_GTX_C_MRX_N15 | T3 | GFX_RX15N | GFX_TX15N | P2 | PCIE_MTX_GRX_P0 | C480 1 | 2 | ΔVGA@ 0.1U_0402_16V7K | PCIE_MTX_C_GRX_N15 |

**PCIE I/F GPP**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 29 PCIE_PTX_C_IRX_P0 | AE3 | GPP_RX0P | GPP_TX0P | AC1 | PCIE_ITX_PRX_P0 | C18 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_P0 29 |
| 29 PCIE_PTX_C_IRX_N0 | AD4 | GPP_RX0N | GPP_TX0N | AC2 | PCIE_ITX_PRX_N0 | C19 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_N0 29 |
| 28 PCIE_PTX_C_IRX_P1 | AE2 | GPP_RX1P | GPP_TX1P | AB4 | PCIE_ITX_PRX_P1 | C31 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_P1 28 |
| 28 PCIE_PTX_C_IRX_N1 | AD3 | GPP_RX1N | GPP_TX1N | AB3 | PCIE_ITX_PRX_N1 | C30 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_N1 28 |
| 28 PCIE_PTX_C_IRX_P2 | AD1 | GPP_RX2P | GPP_TX2P | AA2 | PCIE_ITX_PRX_P2 | C21 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_P2 28 |
| 28 PCIE_PTX_C_IRX_N2 | AD2 | GPP_RX2N | GPP_TX2N | AA1 | PCIE_ITX_PRX_N2 | C20 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_N2 28 |
| 26 PCIE_PTX_C_IRX_P3 | V5 | GPP_RX3P | GPP_TX3P | Y1 | PCIE_ITX_PRX_P3 | C23 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_P3 26 |
| 26 PCIE_PTX_C_IRX_N3 | W6 | GPP_RX3N | GPP_TX3N | Y2 | PCIE_ITX_PRX_N3 | C22 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_N3 26 |
| 25 PCIE_PTX_C_IRX_P4 | U5 | GPP_RX4P | GPP_TX4P | Y4 | PCIE_ITX_PRX_P4 | C33 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_P4 25 |
| 25 PCIE_PTX_C_IRX_N4 | U6 | GPP_RX4N | GPP_TX4N | Y3 | PCIE_ITX_PRX_N4 | C32 1 | 2 | 0.1U_0402_16V7K | PCIE_ITX_C_PRX_N4 25 |
| | U8 | GPP_RX5P | GPP_TX5P | V1 | | | | | |
| | U7 | GPP_RX5N | GPP_TX5N | V2 | | | | | |

**PCIE I/F SB**

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 19 SB_RX0P | AA8 | SB_RX0P | SB_TX0P | AD7 | SB_TX0P_C | C271 1 | 2 | 0.1U_0402_16V7K | SB_TX0P 19 |
| 19 SB_RX0N | Y8 | SB_RX0N | SB_TX0N | AE7 | SB_TX0N_C | C268 1 | 2 | 0.1U_0402_16V7K | SB_TX0N 19 |
| 19 SB_RX1P | AA7 | SB_RX1P | SB_TX1P | AE6 | SB_TX1P_C | C290 1 | 2 | 0.1U_0402_16V7K | SB_TX1P 19 |
| 19 SB_RX1N | Y7 | SB_RX1N | SB_TX1N | AD6 | SB_TX1N_C | C295 1 | 2 | 0.1U_0402_16V7K | SB_TX1N 19 |
| 19 SB_RX2P | AA5 | SB_RX2P | SB_TX2P | AB6 | SB_TX2P_C | C263 1 | 2 | 0.1U_0402_16V7K | SB_TX2P 19 |
| 19 SB_RX2N | AA6 | SB_RX2N | SB_TX2N | AC6 | SB_TX2N_C | C265 1 | 2 | 0.1U_0402_16V7K | SB_TX2N 19 |
| 19 SB_RX3P | W5 | SB_RX3P | SB_TX3P | AD5 | SB_TX3P_C | C262 1 | 2 | 0.1U_0402_16V7K | SB_TX3P 19 |
| 19 SB_RX3N | Y5 | SB_RX3N | SB_TX3N | AE5 | SB_TX3N_C | C260 1 | 2 | 0.1U_0402_16V7K | SB_TX3N 19 |

PCE_CALRP(PCE_BCALRP)

PCE_CALRN(PCE_BCALRN)

AC8 R33 1 2 1.27K_0402_1%

AB8 R31 1 2 2K_0402_1%

+1.1VS

RS780M_FCBGA528

**RS780M Display Port Support (muxed on GFX)**

| | |
|---|---|
| DP0 | GFX_TX0,TX1,TX2 and TX3<br>AUX0 and HPD0 |
| DP1 | GFX_TX4,TX5,TX6 and TX7<br>AUX1 and HPD1 |

New Card
TV Tuner
WLAN
GLAN
Card Reader

4 H_CADOP[0..15] → H_CADOP[0..15]

4 H_CADON[0..15] → H_CADON[0..15]

H_CADIP[0..15] → H_CADIP[0..15] 4

H_CADIN[0..15] → H_CADIN[0..15] 4

U25A

**PART 1 OF 6**

**HYPER TRANSPORT CPU I/F**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| H_CADOP0 | Y25 | HT_RXCAD0P | HT_TXCAD0P | D24 | H_CADIP0 |
| H_CADON0 | Y24 | HT_RXCAD0N | HT_TXCAD0N | D25 | H_CADIN0 |
| H_CADOP1 | V22 | HT_RXCAD1P | HT_TXCAD1P | E24 | H_CADIP1 |
| H_CADON1 | V23 | HT_RXCAD1N | HT_TXCAD1N | E25 | H_CADIN1 |
| H_CADOP2 | V25 | HT_RXCAD2P | HT_TXCAD2P | F24 | H_CADIP2 |
| H_CADON2 | V24 | HT_RXCAD2N | HT_TXCAD2N | F25 | H_CADIN2 |
| H_CADOP3 | U24 | HT_RXCAD3P | HT_TXCAD3P | F23 | H_CADIP3 |
| H_CADON3 | U25 | HT_RXCAD3N | HT_TXCAD3N | F22 | H_CADIN3 |
| H_CADOP4 | T25 | HT_RXCAD4P | HT_TXCAD4P | H23 | H_CADIP4 |
| H_CADON4 | T24 | HT_RXCAD4N | HT_TXCAD4N | H22 | H_CADIN4 |
| H_CADOP5 | P22 | HT_RXCAD5P | HT_TXCAD5P | J25 | H_CADIP5 |
| H_CADON5 | P23 | HT_RXCAD5N | HT_TXCAD5N | J24 | H_CADIN5 |
| H_CADOP6 | P25 | HT_RXCAD6P | HT_TXCAD6P | K24 | H_CADIP6 |
| H_CADON6 | P24 | HT_RXCAD6N | HT_TXCAD6N | K25 | H_CADIN6 |
| H_CADOP7 | N24 | HT_RXCAD7P | HT_TXCAD7P | K23 | H_CADIP7 |
| H_CADON7 | N25 | HT_RXCAD7N | HT_TXCAD7N | K22 | H_CADIN7 |
| H_CADOP8 | AC24 | HT_RXCAD8P | HT_TXCAD8P | F21 | H_CADIP8 |
| H_CADON8 | AC25 | HT_RXCAD8N | HT_TXCAD8N | G21 | H_CADIN8 |
| H_CADOP9 | AB25 | HT_RXCAD9P | HT_TXCAD9P | G20 | H_CADIP9 |
| H_CADON9 | AB24 | HT_RXCAD9N | HT_TXCAD9N | H21 | H_CADIN9 |
| H_CADOP10 | AA24 | HT_RXCAD10P | HT_TXCAD10P | J20 | H_CADIP10 |
| H_CADON10 | AA25 | HT_RXCAD10N | HT_TXCAD10N | J21 | H_CADIN10 |
| H_CADOP11 | Y22 | HT_RXCAD11P | HT_TXCAD11P | J18 | H_CADIP11 |
| H_CADON11 | Y23 | HT_RXCAD11N | HT_TXCAD11N | K17 | H_CADIN11 |
| H_CADOP12 | W21 | HT_RXCAD12P | HT_TXCAD12P | L19 | H_CADIP12 |
| H_CADON12 | W20 | HT_RXCAD12N | HT_TXCAD12N | J19 | H_CADIN12 |
| H_CADOP13 | V21 | HT_RXCAD13P | HT_TXCAD13P | M19 | H_CADIP13 |
| H_CADON13 | V20 | HT_RXCAD13N | HT_TXCAD13N | L18 | H_CADIN13 |
| H_CADOP14 | U20 | HT_RXCAD14P | HT_TXCAD14P | M21 | H_CADIP14 |
| H_CADON14 | U21 | HT_RXCAD14N | HT_TXCAD14N | P21 | H_CADIN14 |
| H_CADOP15 | U19 | HT_RXCAD15P | HT_TXCAD15P | P18 | H_CADIP15 |
| H_CADON15 | U18 | HT_RXCAD15N | HT_TXCAD15N | M18 | H_CADIN15 |

| | | | | | |
|---|---|---|---|---|---|
| 4 H_CLKOP0 | T22 | HT_RXCLK0P | HT_TXCLK0P | H24 | H_CLKIP0 4 |
| 4 H_CLKON0 | T23 | HT_RXCLK0N | HT_TXCLK0N | H25 | H_CLKIN0 4 |
| 4 H_CLKOP1 | AB23 | HT_RXCLK1P | HT_TXCLK1P | L21 | H_CLKIP1 4 |
| 4 H_CLKON1 | AA22 | HT_RXCLK1N | HT_TXCLK1N | L20 | H_CLKIN1 4 |

| | | | | | |
|---|---|---|---|---|---|
| 4 H_CTLOP0 | H_CTLOP0 M22 | HT_RXCTL0P | HT_TXCTL0P | M24 | H_CTLIP0 H_CTLIP0 4 |
| 4 H_CTLON0 | H_CTLON0 M23 | HT_RXCTL0N | HT_TXCTL0N | M25 | H_CTLIN0 H_CTLIN0 4 |
| 4 H_CTLOP1 | H_CTLOP1 R21 | HT_RXCTL1P | HT_TXCTL1P | P19 | H_CTLIP1 H_CTLIP1 4 |
| 4 H_CTLON1 | H_CTLON1 R20 | HT_RXCTL1N | HT_TXCTL1N | R18 | H_CTLIN1 H_CTLIN1 4 |

1 R75 2 C23

301_0402_1%

0718 Place within 1" layout 1:2

HT_RXCALP A24

HT_RXCALN

HT_TXCALP B24

HT_TXCALN B25

1 R76 2

301_0402_1%

0718 Place within 1" layout 1:2

RS780M_FCBGA528



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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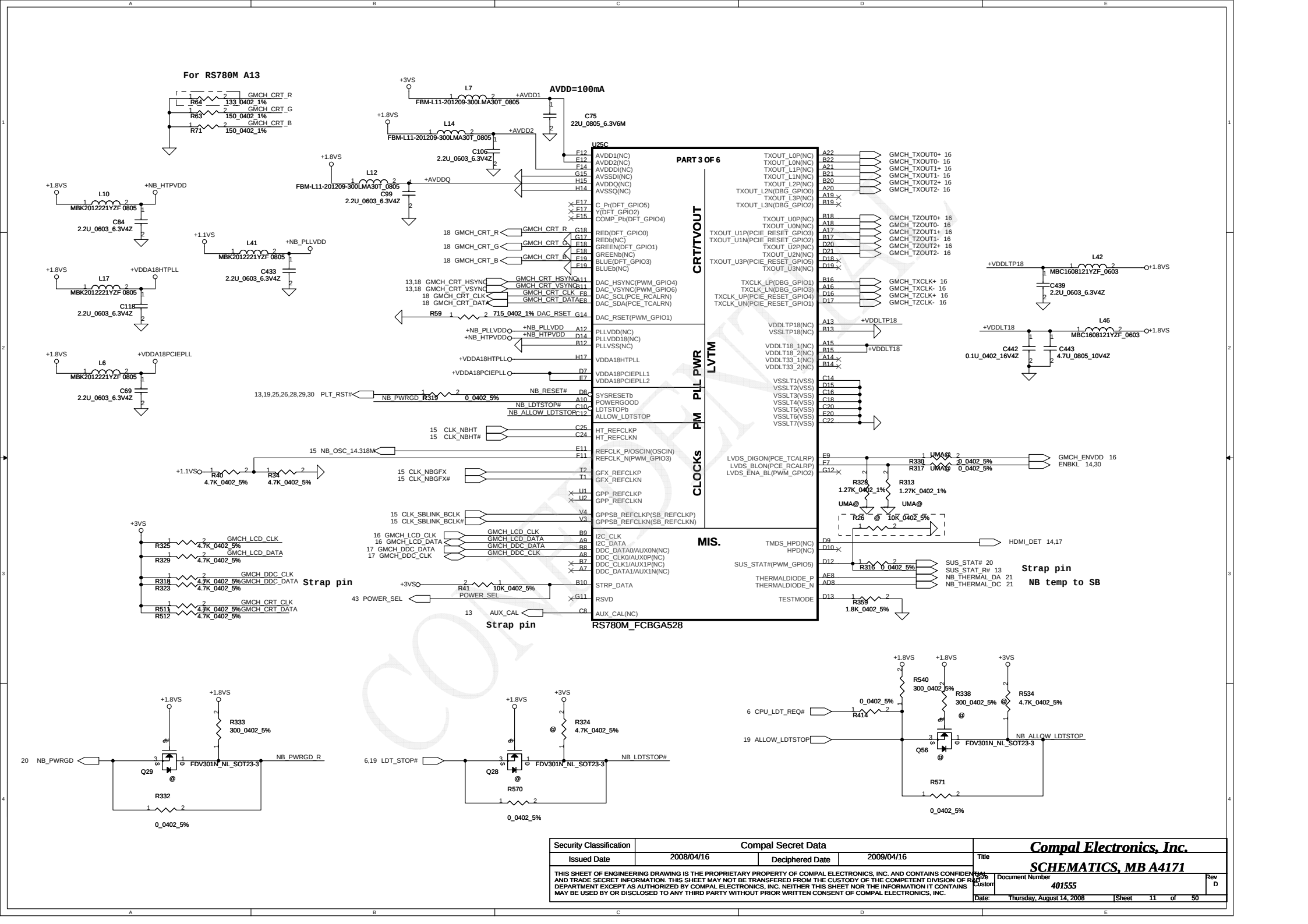
| Rev | D |
| Date: Thursday, August 14, 2008 | Sheet 10 of 50 |

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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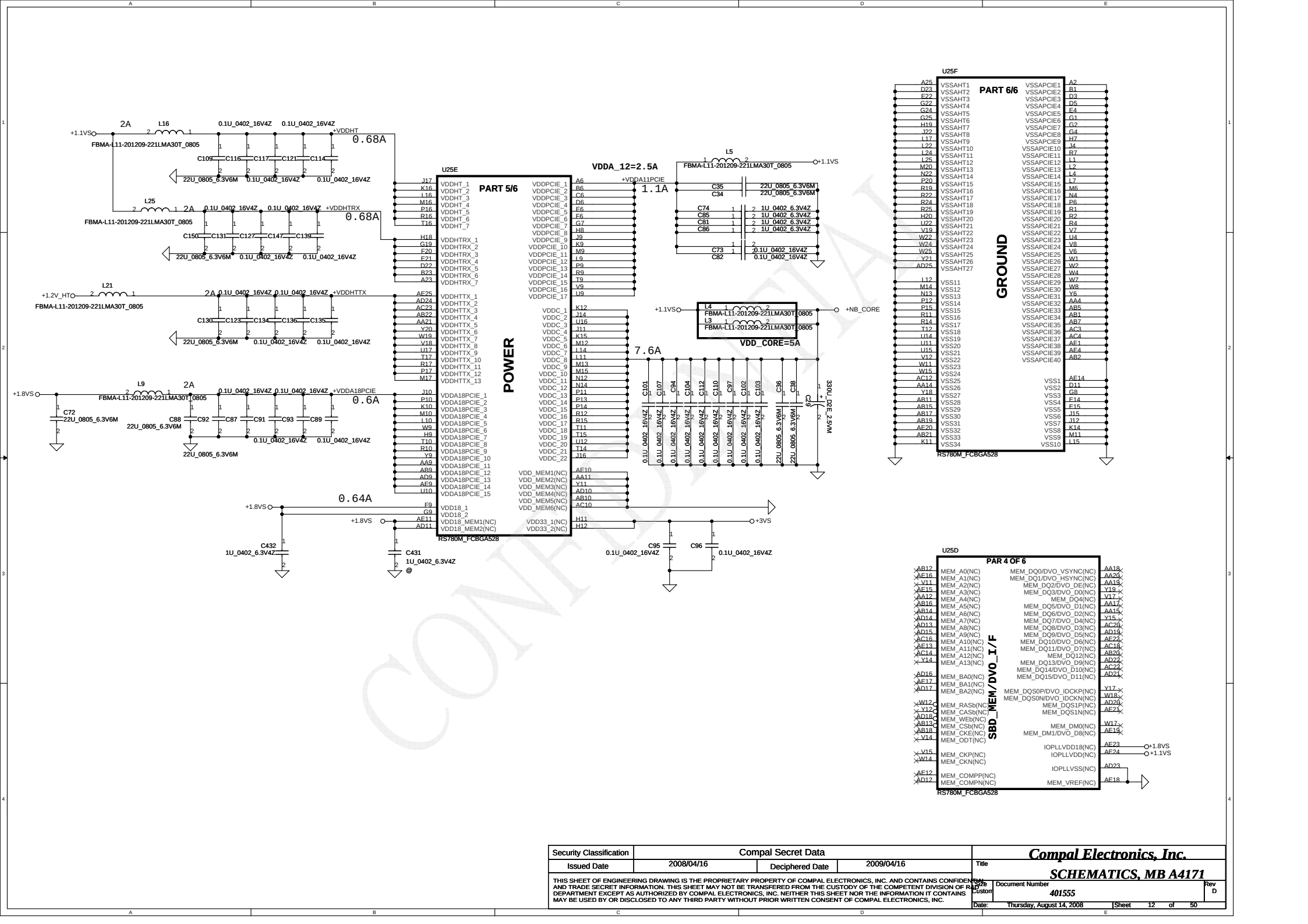
| Size | Document Number | Rev |
|---|---|---|
| Custom | 401555 | D |

Date: Thursday, August 14, 2008 | Sheet 11 of 50



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| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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|---|---|
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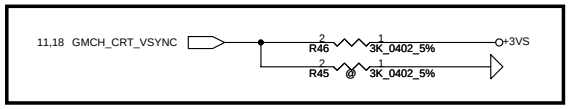
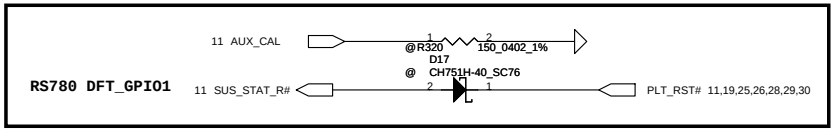
| Size: Custom | Document Number: 401555 |
| Rev | D |
| Date: Thursday, August 14, 2008 | Sheet 12 of 50 |



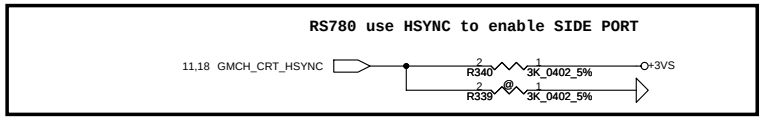

**DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb**

```
Enables the Test Debug Bus using GPIO. (VSYNC)
1 : Disable (RS780)
0 : Enable (Rs780)
```




**DFT_GPIO1: LOAD_EEPROM_STRAPS**

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
default values if not connected
RS740/RX780: DFT_GPIO1  RS780:SUS_STAT
```




**RS780 use HSYNC to enable SIDE PORT**

```
RS740/RS780: Enables Side port memory ( RS780 use HSYNC#)
0.   Enable (RS780)
1 :  Disable(RS780)
```



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
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| Size: Custom | Document Number: 401555 | Rev: D |
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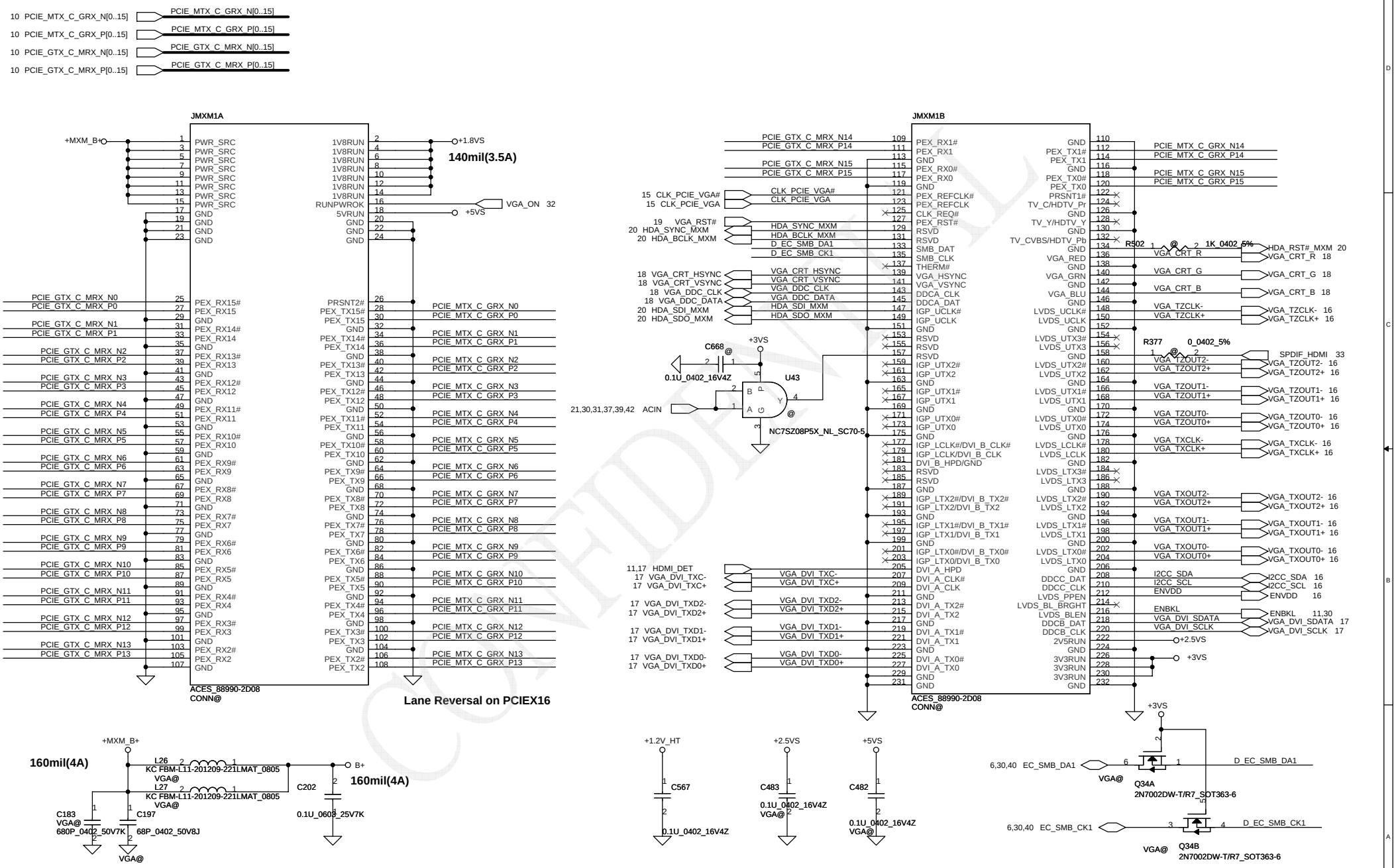




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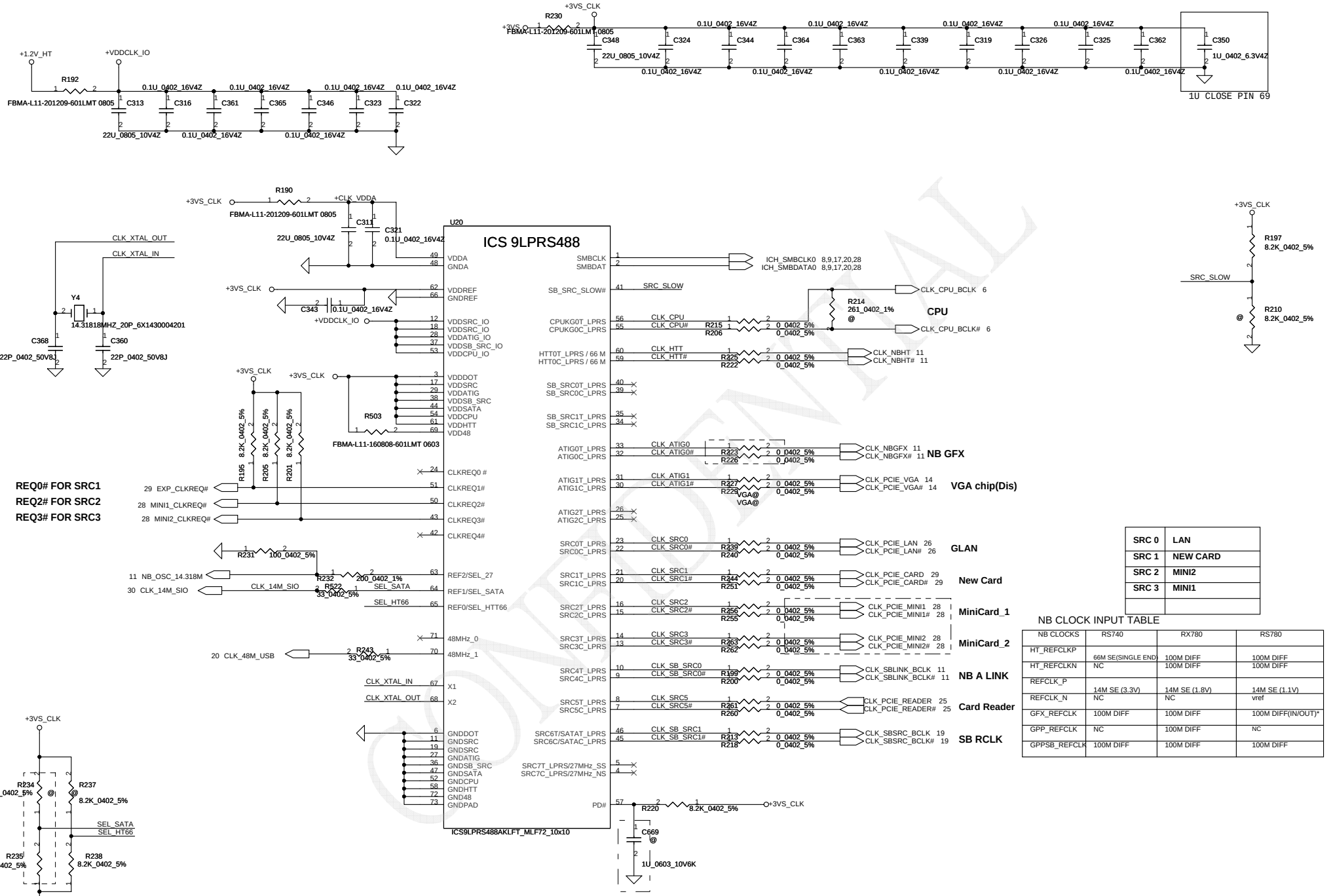
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |
| Title | SCHEMATICS, MB A4171 | | |
| Size B | Document Number 401555 | | Rev D |
| Date: Thursday, August 14, 2008 | Sheet 14 of 50 | | |




| | |
|---|---|
| SRC 0 | LAN |
| SRC 1 | NEW CARD |
| SRC 2 | MINI2 |
| SRC 3 | MINI1 |
| | |

NB CLOCK INPUT TABLE

| NB CLOCKS | RS740 | RX780 | RS780 |
|---|---|---|---|
| HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF |
| HT_REFCLKN | NC | 100M DIFF | 100M DIFF |
| REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V) |
| REFCLK_N | NC | NC | vref |
| GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)* |
| GPP_REFCLK | NC | 100M DIFF | NC |
| GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF |

| | | |
|---|---|---|
| SEL_HTT66 | 1 | configure as single-ended 66MHz output |
| | 0* | configure as differential 100MHz output |
| SEL_SATA | 1* | 100M_SATA SRC6 output |
| | 0 | SPREAD 100M_SATA SRC6 output |

* default

| | | |
|---|---|---|
| NB_OSC_14.318M | 1 | configure as 27M and 27M_SS output |
| | 0* | configure as SRC_7 output |

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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|---|---|---|
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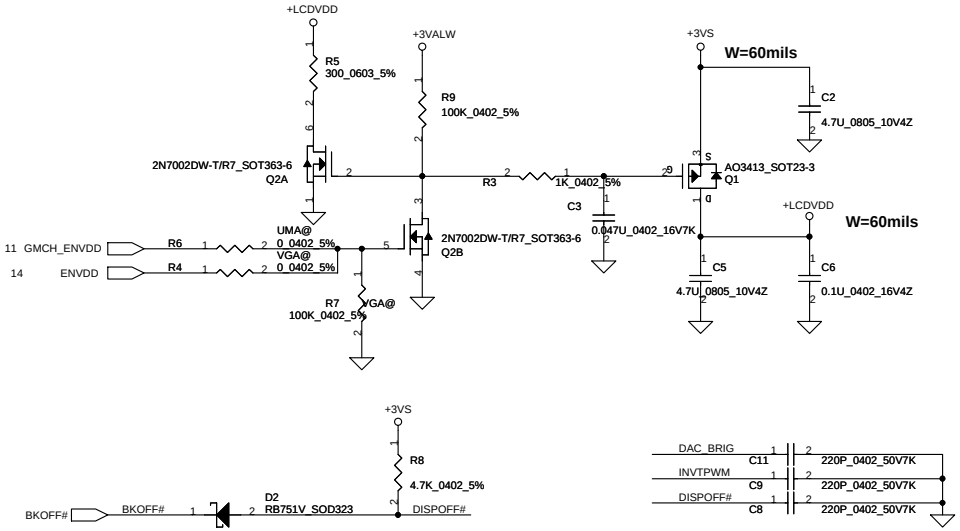
| Date: Thursday, August 14, 2008 | Sheet 15 of 50 | |

## LCD POWER CIRCUIT

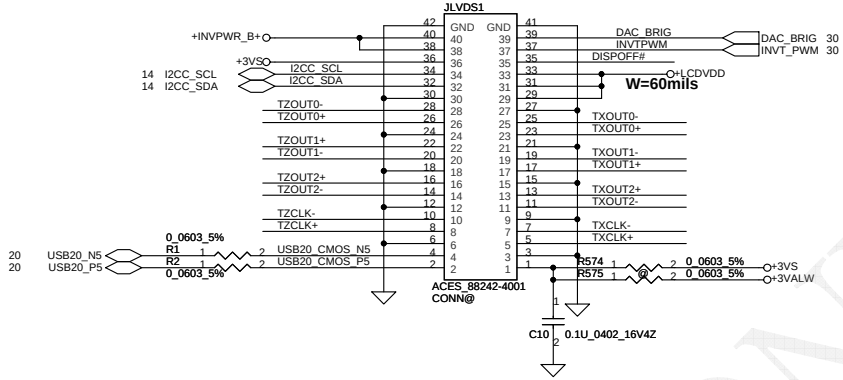


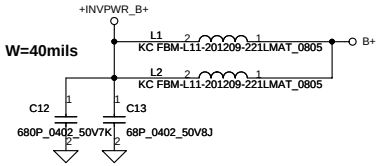


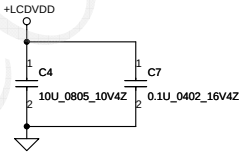


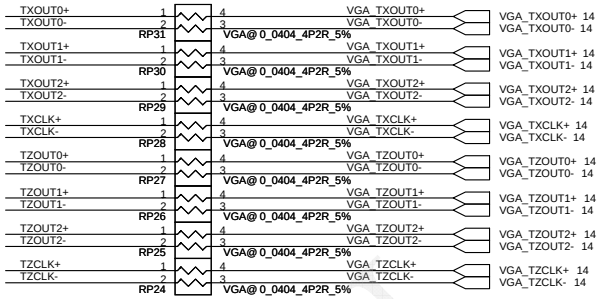


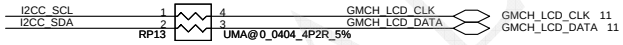

## LCD/PANEL BD. Conn.

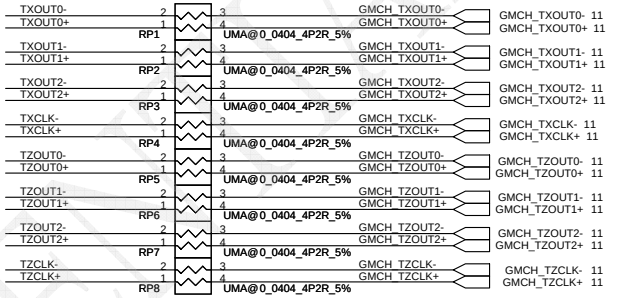


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| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
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reserve HDMI I2C ESD diode

## DDC to Docking

38 EC_DOCKIN
11 GMCH_DDC_CLK
14 VGA_DVI_SCLK
14 VGA_DVI_SDATA
11 GMCH_DDC_DATA
R89 UMA@ 0_0402_5%
R88 VGA@ 0_0402_5%
R98 VGA@ 0_0402_5%
R94 UMA@ 0_0402_5%
VGA_DVI_SCLK_R
VGA_DVI_SDATA_R
+HDMI_5V_OUT
R90 2K_0402_5%
R91 2K_0402_5%
Q48 BSH111 1N_SOT23-3
Q47 BSH111 1N_SOT23-3
D_DVI_SCLK 38
D_DVI_SDATA 38

## DDC to HDMI CONN

18,33,38 EC_DOCKIN#_S0
R84 6.8K_0402_5%
R87 6.8K_0402_5%
Q50 BSH111 1N_SOT23-3
Q49 BSH111 1N_SOT23-3
HDMI_SCLK
HDMI_SDATA
Place closed to JHDMI1

JHDMI1
HDMI_HPD
HDMI_SDATA
HDMI_SCLK
HDMI_R_CK-
HDMI_R_CK+
HDMI_R_D0-
HDMI_R_D0+
HDMI_R_D1-
HDMI_R_D1+
HDMI_R_D2-
HDMI_R_D2+
HP_DET
+5V
DDC/CEC_GND
SDA
SCL
Reserved
CEC
CK-
CK_shield
CK+
D0-
D0_shield
D0+
D1-
D1_shield
D1+
D2-
D2_shield
D2+
GND
TYCO_1939864-1
CONN@

U41 SN74CBTD3306CPWR_TSSOP8 @
U42 SN74CBTD3306CPWR_TSSOP8 @
1A 2A 1OE# 2OE# VCC 1B 2B GND
D_DVI_SCLK D_DVI_SDATA
HDMI_SCLK HDMI_SDATA

D6 RB491D_SC59-3
F1 1.1A_6VDC_FUSE
W=40mils
+5VS
C177 0.1U_0402_16V4Z

R524 0_0402_5%
D_DVI_DET 38
C243 0.1U_0402_16V7K
R123 2.2K_0402_5%
+3VS
HDMI_DET 11,14
U9 SN74AHCT1G125GW_SOT353-5
R105 100K_0402_5%
C242 0.1U_0402_16V7K
HDMI_HPD

R382 R383 R384 R385 R386 R387 R388 R390 0_0402_5%
L50 L51 L52 L53 @WCM-2012-900T_0805
HDMI_CLK- HDMI_CLK+ HDMI_TX0- HDMI_TX0+ HDMI_TX1- HDMI_TX1+ HDMI_TX2- HDMI_TX2+
HDMI_R_CK- HDMI_R_CK+ HDMI_R_D0- HDMI_R_D0+ HDMI_R_D1- HDMI_R_D1+ HDMI_R_D2- HDMI_R_D2+

R393 4.7K_0402_5%
R392 @ 0_0402_5%
D22 RB751V_SOD323
R400 4.7K_0402_5%
MS
OE

D21 SS1040_SOD123
+3VS_D80
C486 0.1U_0402_16V4Z
C485 0.1U_0402_16V4Z

NOTE: L : D-->A
H: D-->B

U28 PI3HDMI412ADZBE_TQFN56_8X8
14 VGA_DVI_TXC+
14 VGA_DVI_TXC-
14 VGA_DVI_TXD0+
14 VGA_DVI_TXD0-
14 VGA_DVI_TXD1+
14 VGA_DVI_TXD1-
14 VGA_DVI_TXD2+
14 VGA_DVI_TXD2-
D0+ D0- D1+ D1- D2+ D2- D3+ D3-
T12 PAD
T13 PAD @
SEL_OUT SEL_IN
8,9,15,20,28 ICH_SMBCLK0
8,9,15,20,28 ICH_SMBDATA0
SCL/S3 SDA/S2
T11 PAD @
MS TEST_OUT TEST_IN OE
A0/S4 A1/S5 A2/S6 A3/S7
NC T-pad
HDMI_TX2- HDMI_TX2+ HDMI_TX1- HDMI_TX1+ HDMI_TX0- HDMI_TX0+ HDMI_CLK- HDMI_CLK+
D_DVI_TXD2- D_DVI_TXD2+ D_DVI_TXD1- D_DVI_TXD1+ D_DVI_TXD0- D_DVI_TXD0+ D_DVI_TXC- D_DVI_TXC+

R395 R396 R397 R398 @4.7K_0402_5%
R401 R402 R403 R404 0_0402_5%
A0 A1 A2 A3

SMBus Address: 1100 000X (b)



| | | | |
|---|---|---|---|
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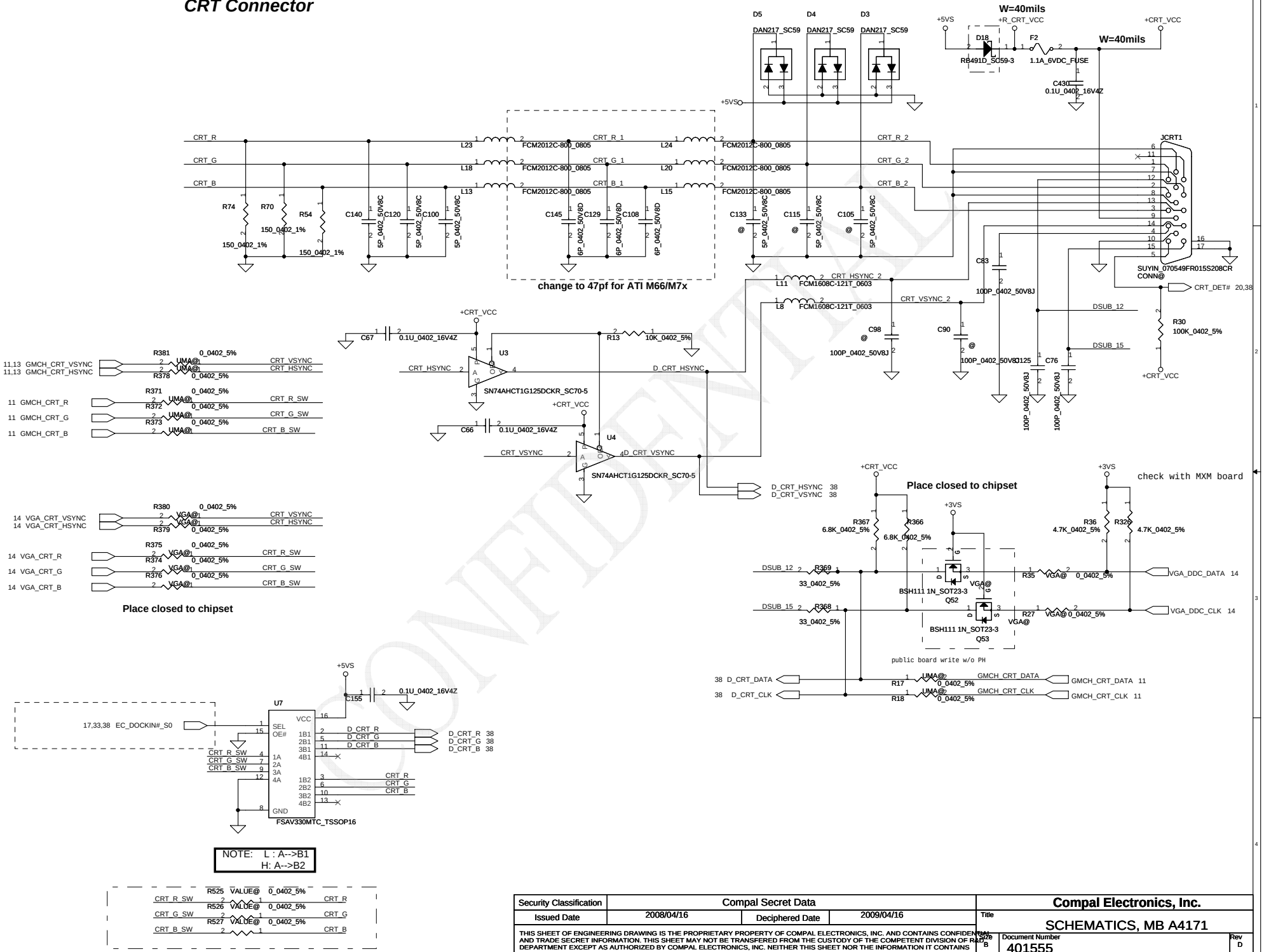
# CRT Connector






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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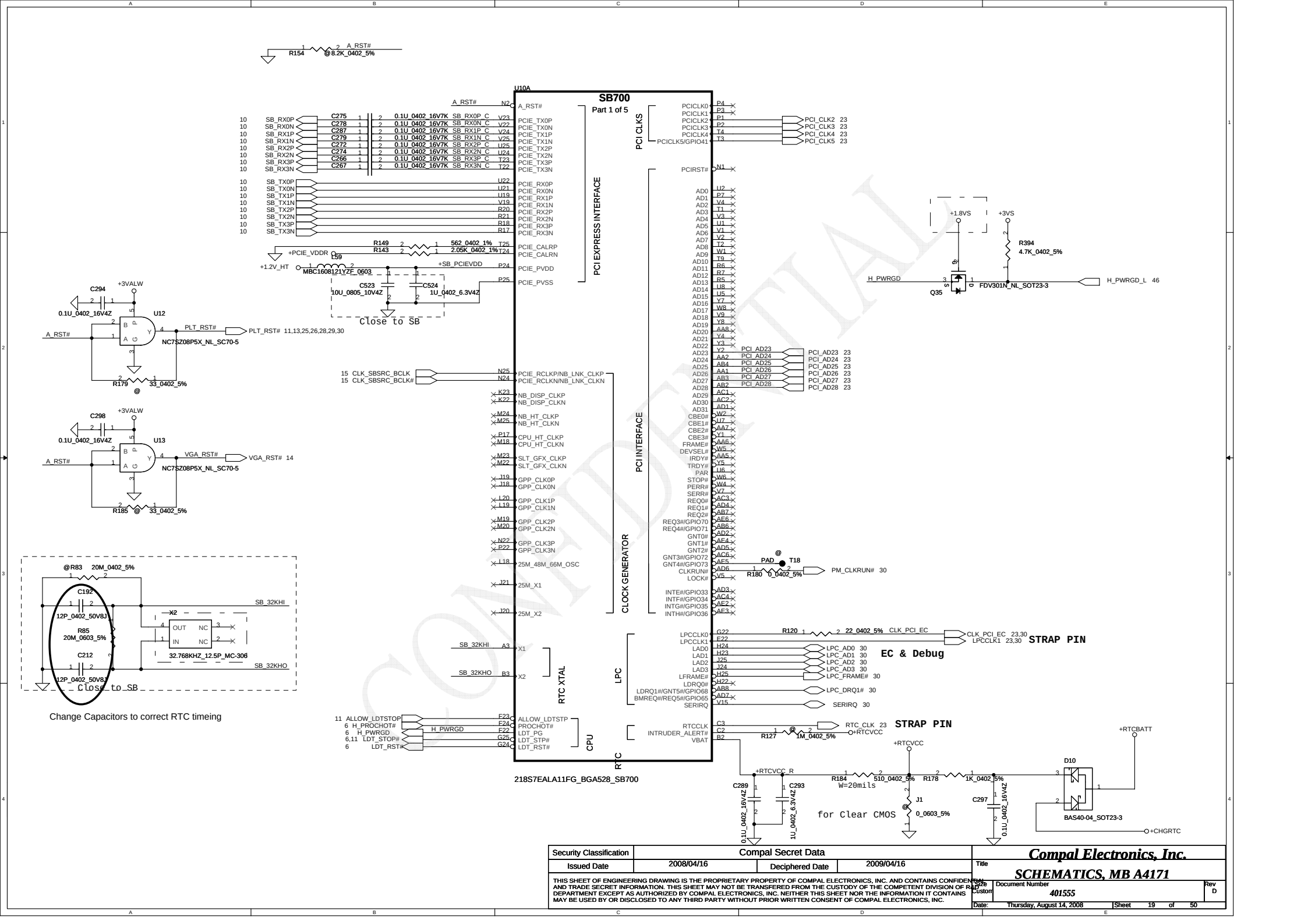


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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| SKU-ID | R509 | R510 |
|---|---|---|
| UMA | | POP |
| DIS | POP | |

demo circuit LID use RI#

SB700 has internal PD

STRAP PIN

FOR Nvidia VGA/B

SB Power Domain :S5

High: CRT Plugged

| | | | |
|---|---|---|---|
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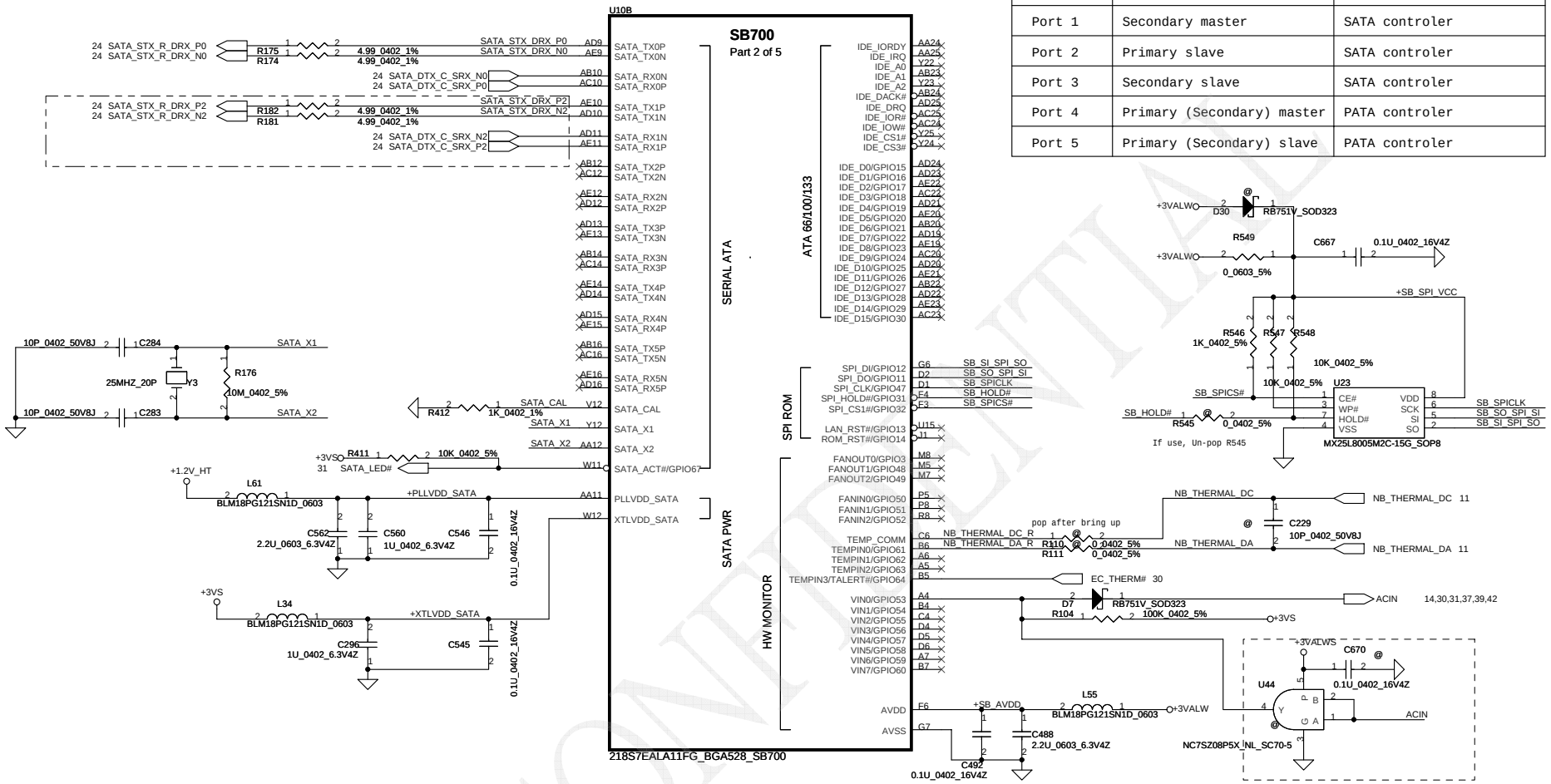
| Port Number | Pri/SEC,Mas/Slave assignment | SATA drive controlled by |
|---|---|---|
| Port 0 | Primary master | SATA controler |
| Port 1 | Secondary master | SATA controler |
| Port 2 | Primary slave | SATA controler |
| Port 3 | Secondary slave | SATA controler |
| Port 4 | Primary (Secondary) master | PATA controler |
| Port 5 | Primary (Secondary) slave | PATA controler |






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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|---|---|
| Compal Electronics, Inc. | |
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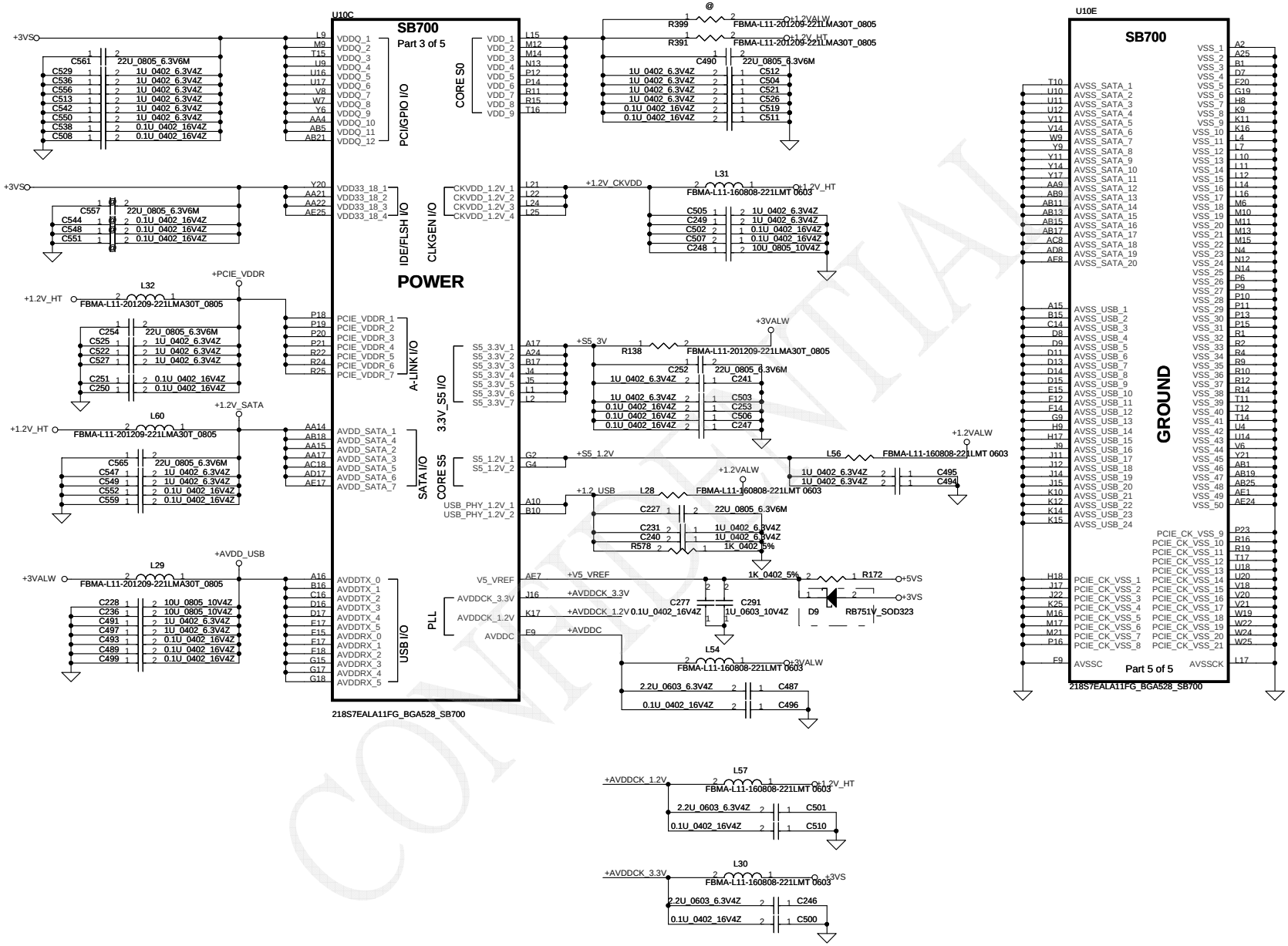
FOR SB700 ALL issue
A12 Will change to +1.2V_HT



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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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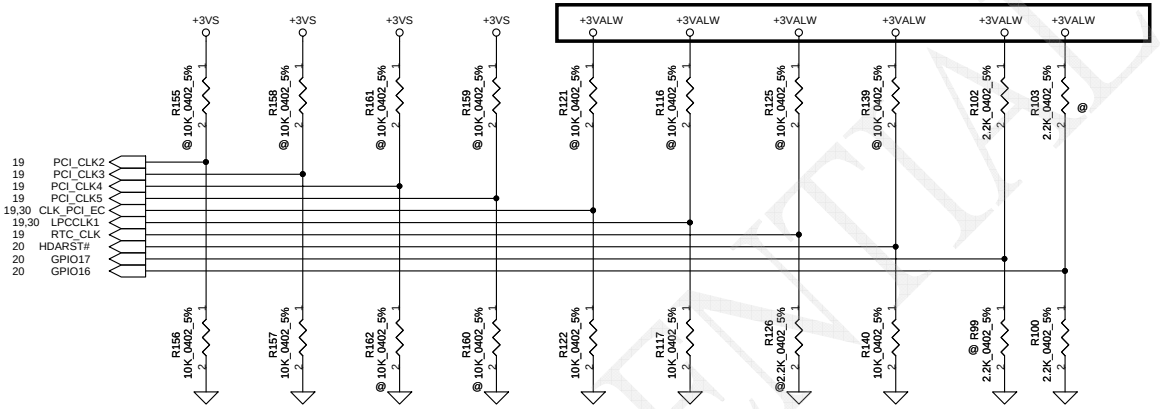
# REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

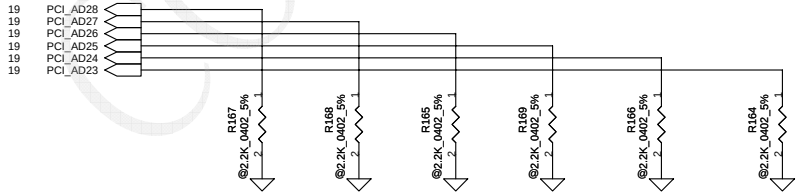
| | PCI_CLK2<br>CLK_PCI_PCM | PCI_CLK3<br>CLK_PCI_DBG | PCI_CLK4 | PCI_CLK5 | LPC_CLK0<br>CLK_PCI_EC | LPC_CLK1 | RTC_CLK | AZ_RST_CD# | GP17 GP16 |
|---|---|---|---|---|---|---|---|---|---|
| **PULL HIGH** | BOOTFAIL TIMER ENABLED | USE DEBUG STRAPS | RESERVED | RESERVED | ENABLE PCI MEM BOOT | CLKGEN ENABLED | **INTERNAL RTC** **DEFAULT** | EC ENABLED | Internal pull up<br>H,H = Reserved<br>H,L = SPI ROM<br>**L,H = LPC ROM (Default L,NC)**<br>L,L = FWH ROM |
| **PULL LOW** | **BOOTFAIL TIMER DISABLED** **DEFAULT** | **IGNORE DEBUG STRAPS** **DEFAULT** | | | **DISABLE PCI MEM BOOT** **DEFAULT** | **CLKGEN DISABLED** **DEFAULT** | **EXT. RTC** (PD on X1, apply 32KHz to RTC_CLK) | **EC DISABLED** **DEFAULT** | |




# DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

| | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 |
|---|---|---|---|---|---|---|
| **PULL HIGH** | **USE LONG RESET** **DEFAULT** | **USE PCI PLL** **DEFAULT** | **USE ACPI BCLK** **DEFAULT** | **USE IDE PLL** **DEFAULT** | **USE DEFAULT PCIE STRAPS** **DEFAULT** | **RESERVED** |
| **PULL LOW** | USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | |






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2008/04/16 | Deciphered Date | 2009/04/16 |



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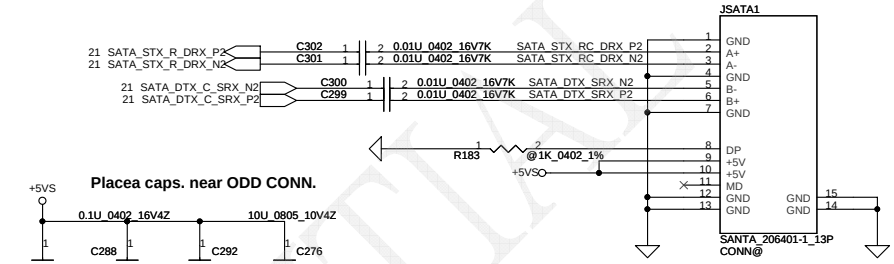
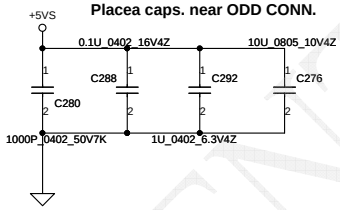
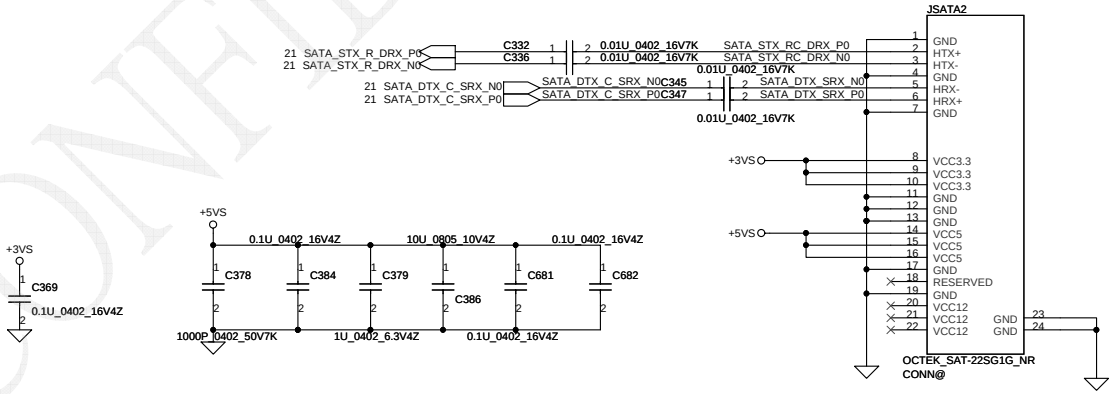
## SATA ODD Conn.




**Placea caps. near ODD CONN.**




## SATA HDD Conn.









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| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
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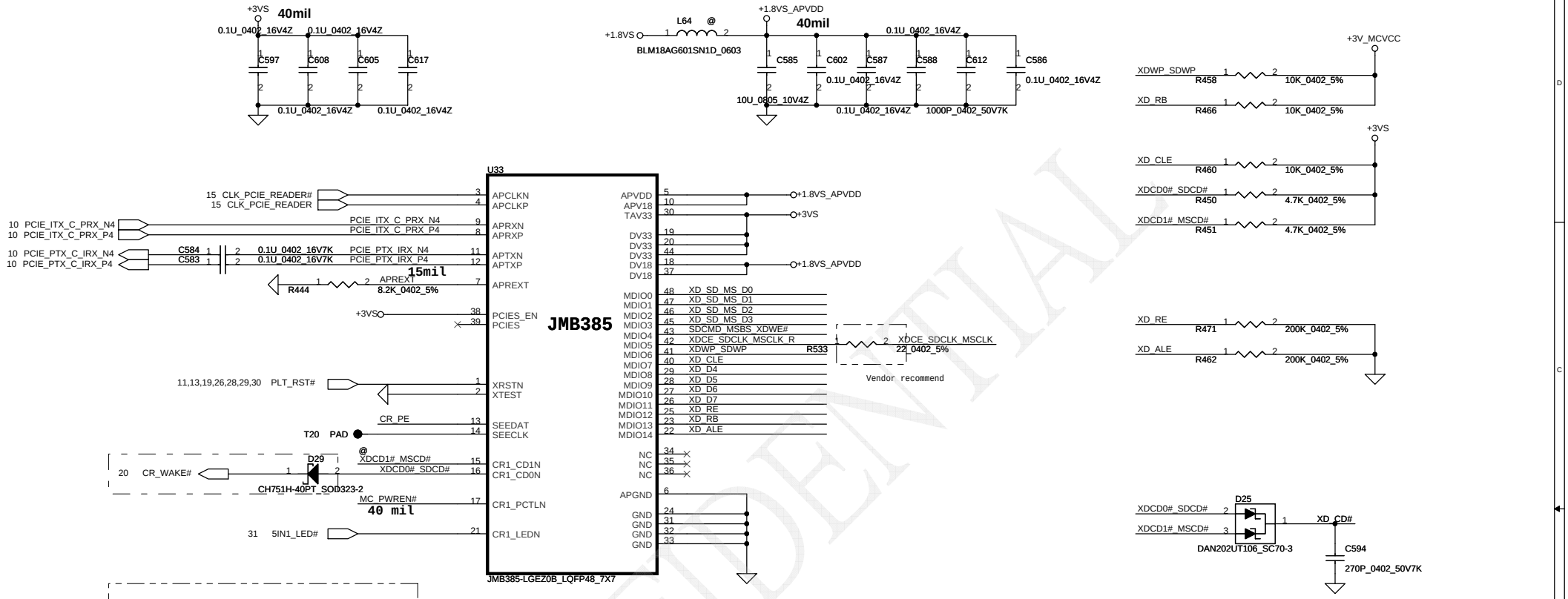
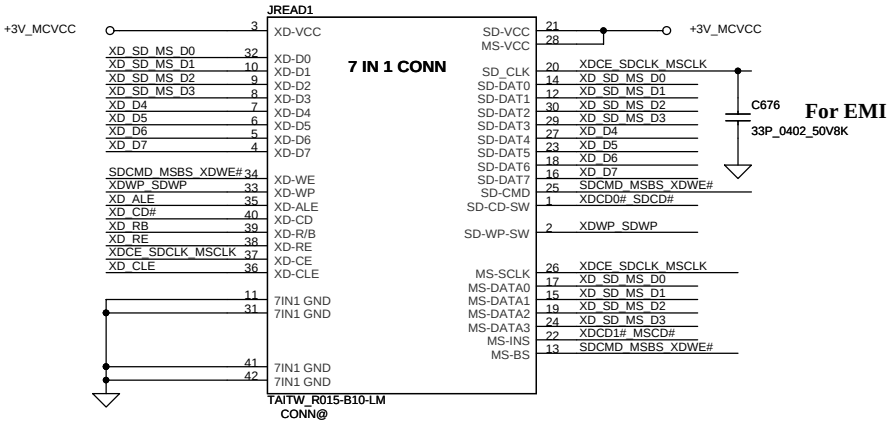



## 4 IN 1 Socket Push Type(New)



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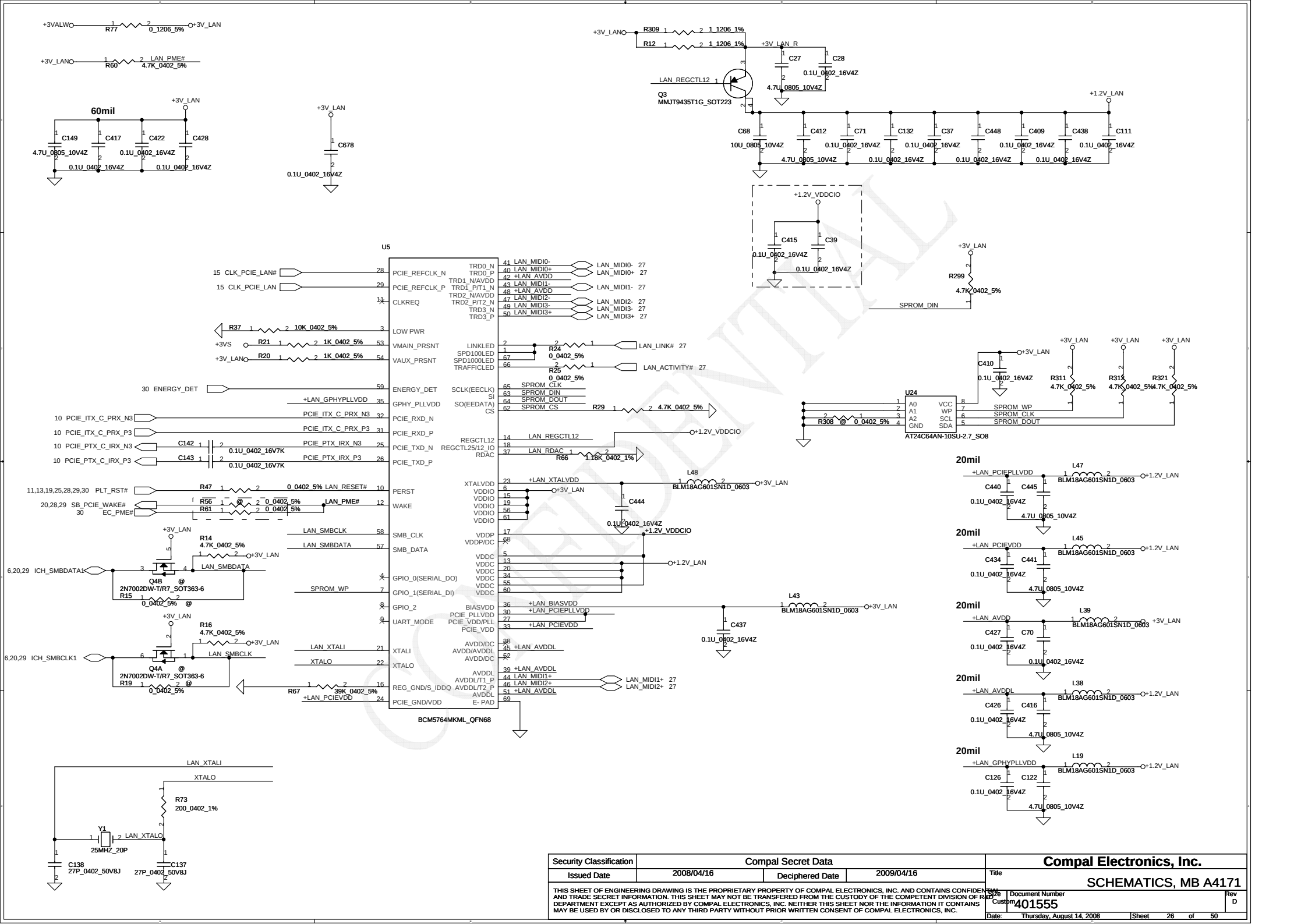




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
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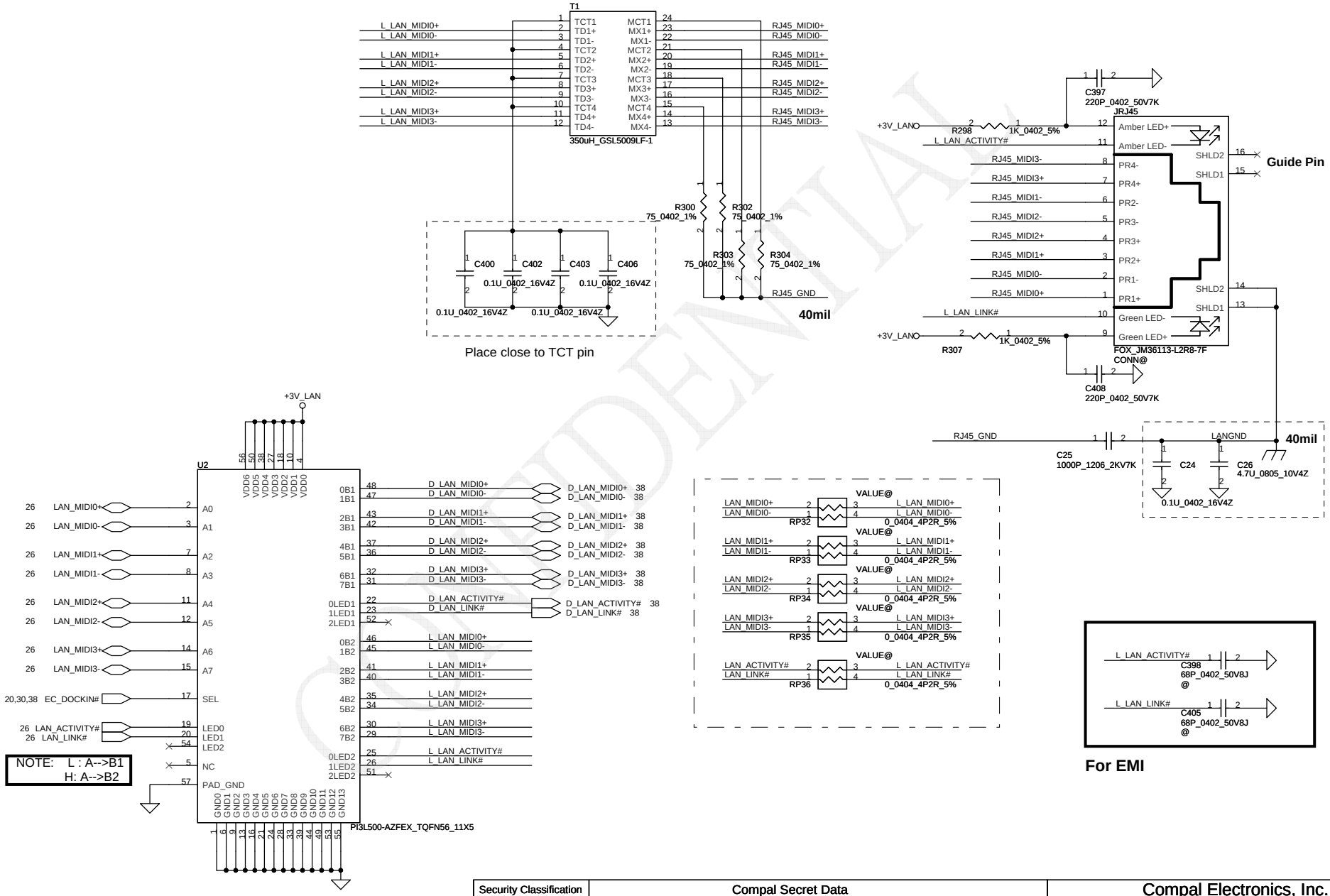




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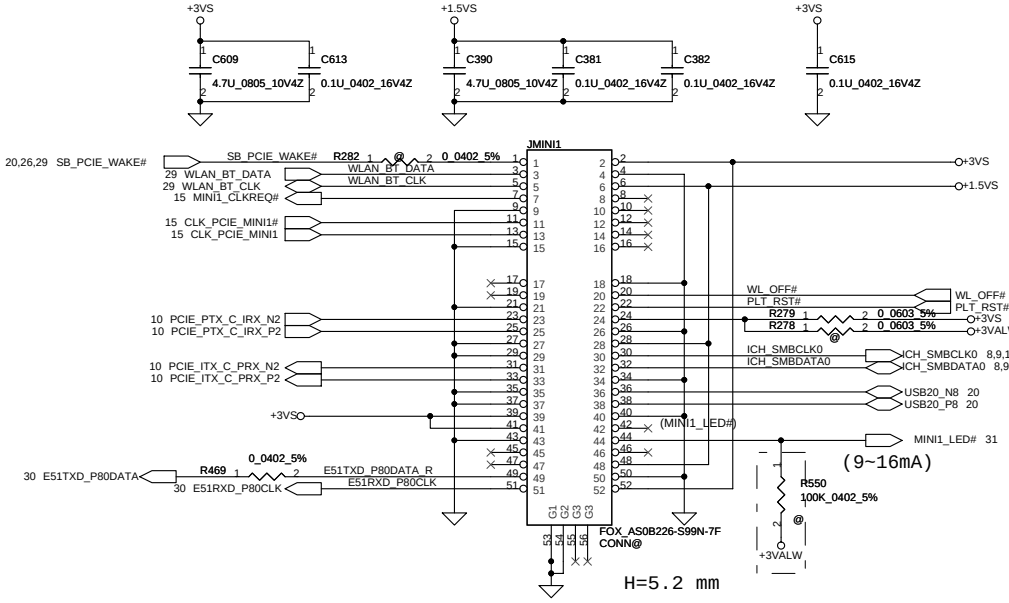
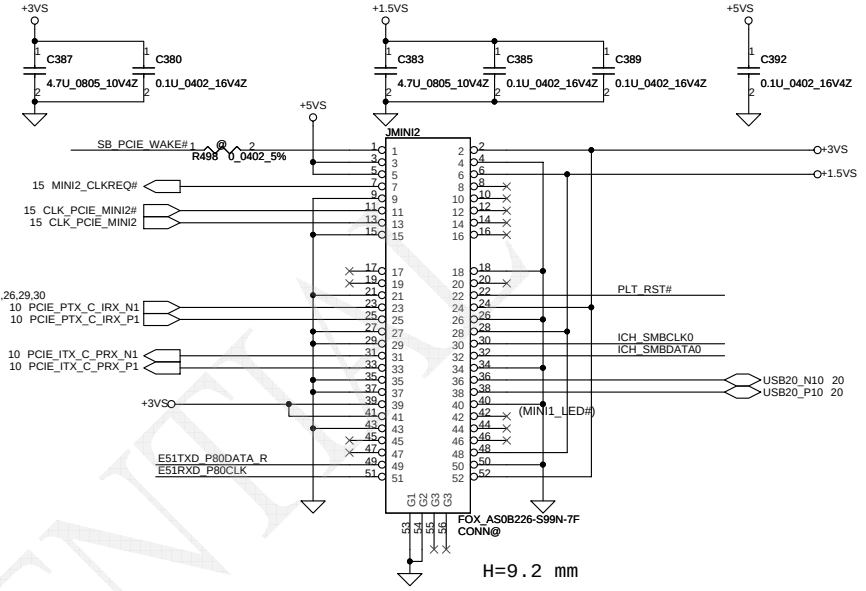
## For Wireless LAN

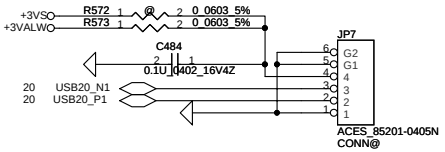



## For TV-Tuner/HW MPEG

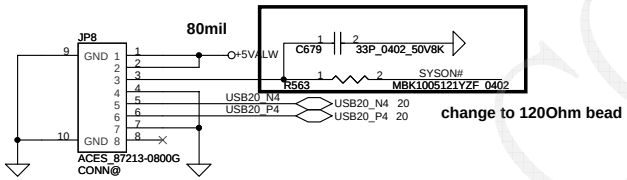



| Mini Card Power Rating | | | |
|---|---|---|---|
| Power | Primary Power (mA) | | Auxiliary Power (mA) |
| | Peak | Normal | Normal |
| +3VS | 1000 | 750 | |
| +3V | 330 | 250 | 250 (wake enable) |
| +1.5VS | 500 | 375 | 5 (Not wake enable) |

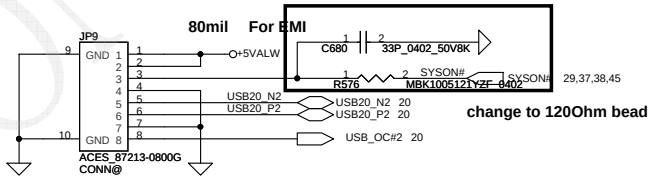
## Fingerprint Conn

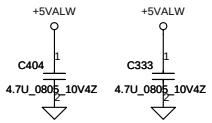


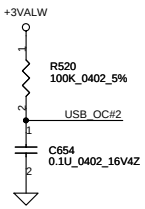

## To USB/B Connector




## To USB/B Connector



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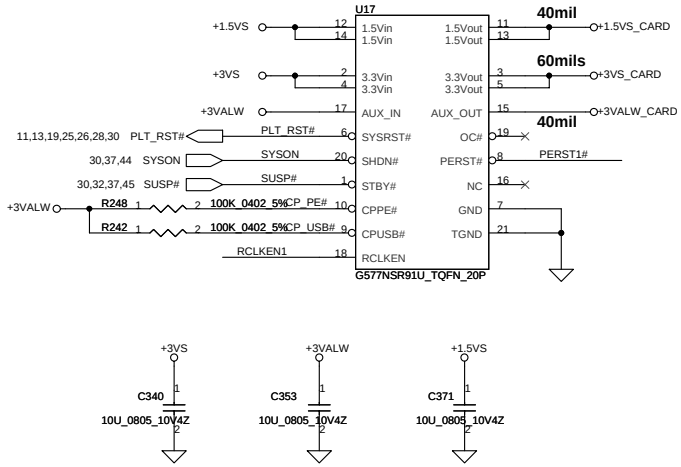
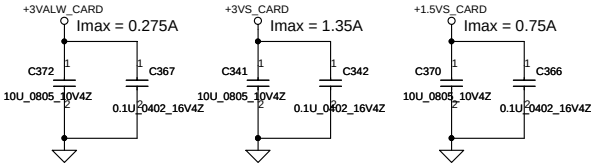
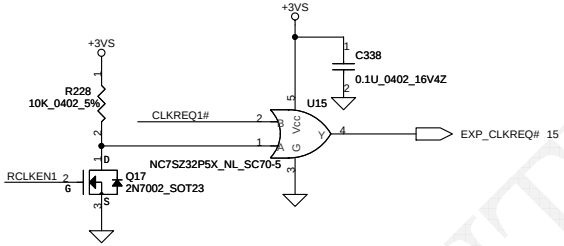
## New Card Power Switch



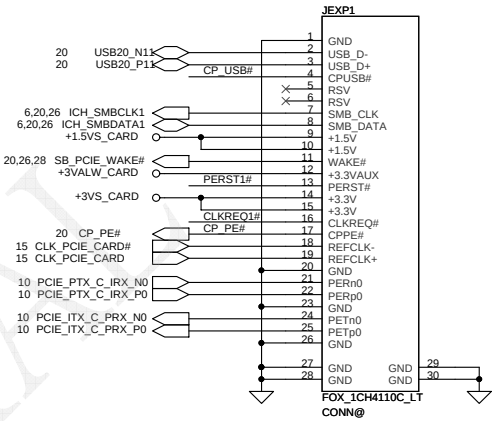




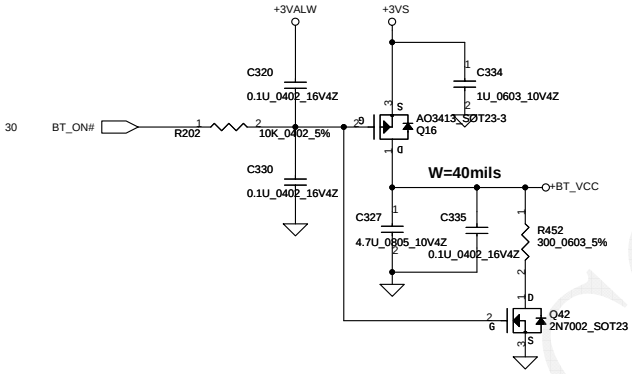


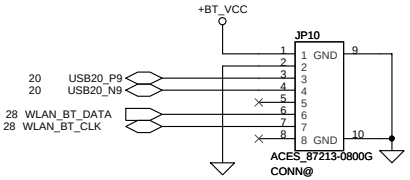



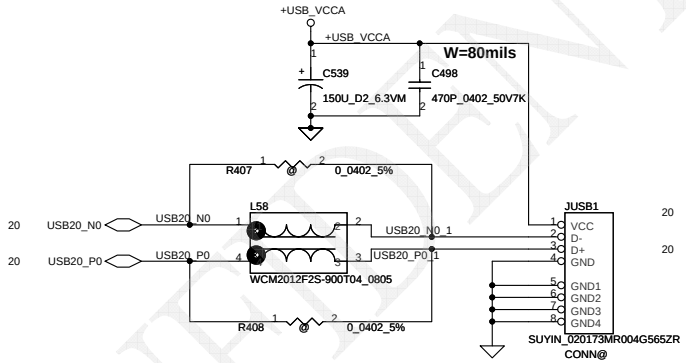

## New Card Socket (Left/TOP)

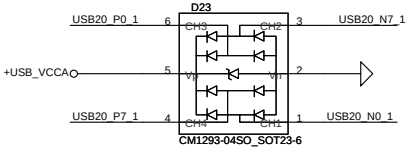


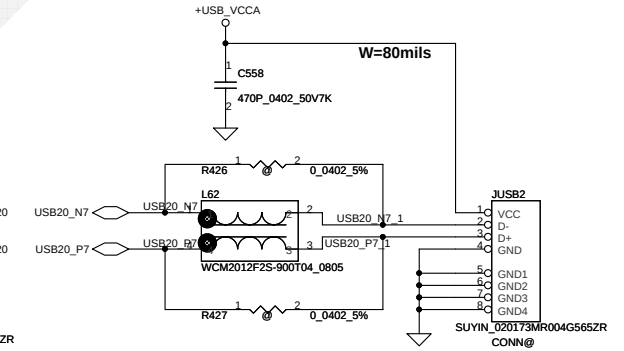

## Bluetooth Conn.

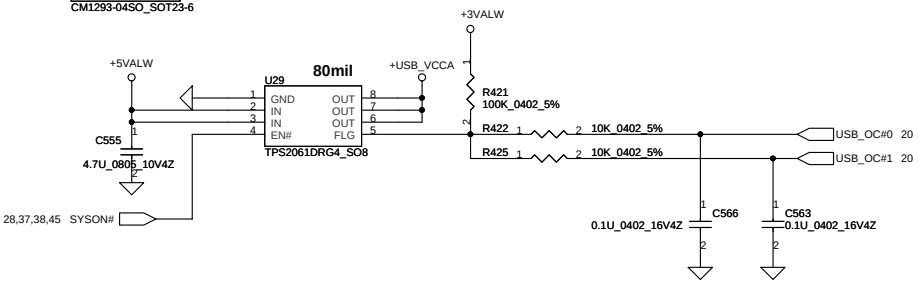


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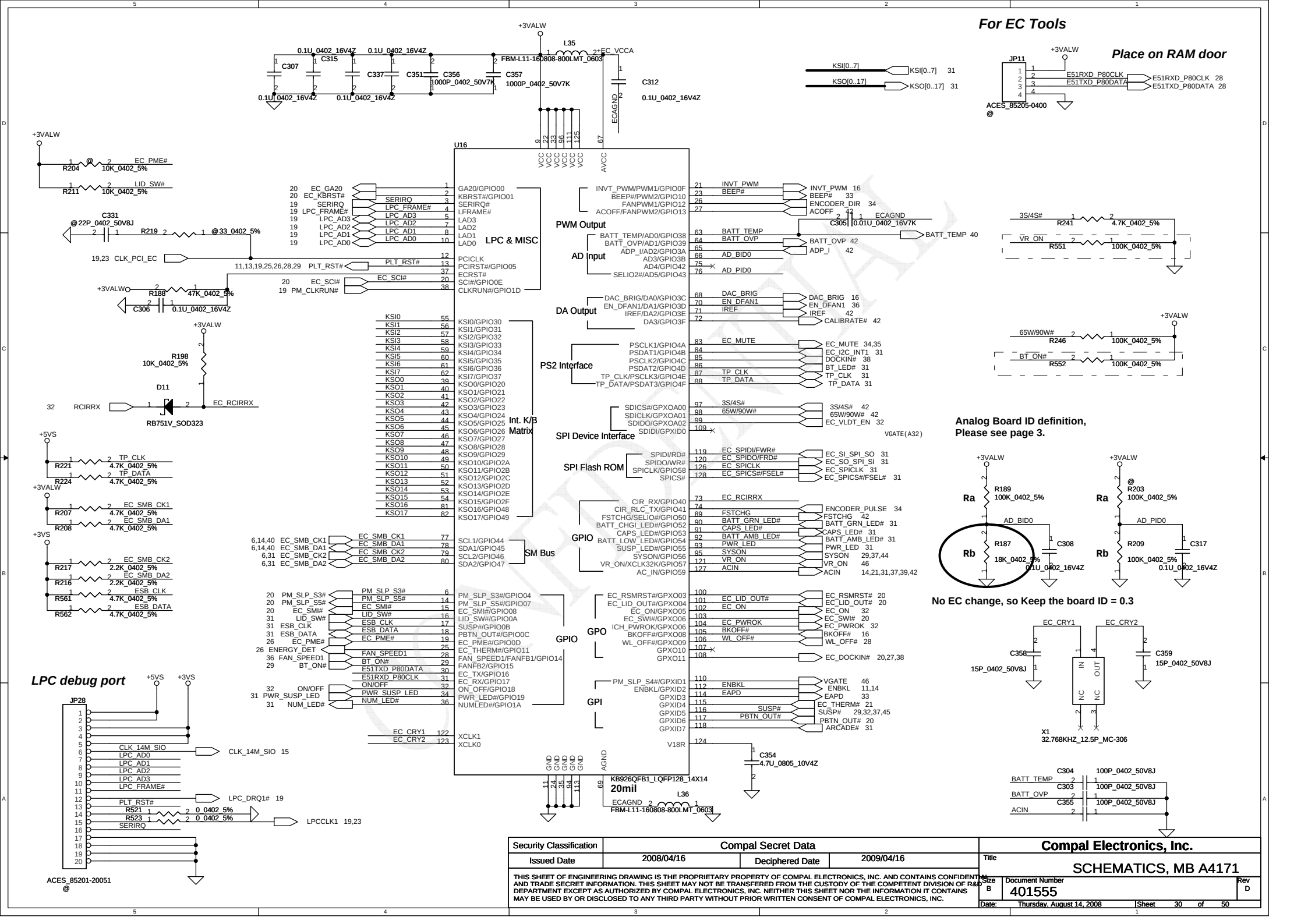
For EC Tools
Place on RAM door
LPC debug port
U16
KB926QFB1_LQFP128_14X14
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Analog Board ID definition, Please see page 3.
No EC change, so Keep the board ID = 0.3
ACES_85205-0400
ACES_85201-20051
Security Classification
Compal Secret Data
Issued Date
2008/04/16
Deciphered Date
2009/04/16
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SCHEMATICS, MB A4171
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50
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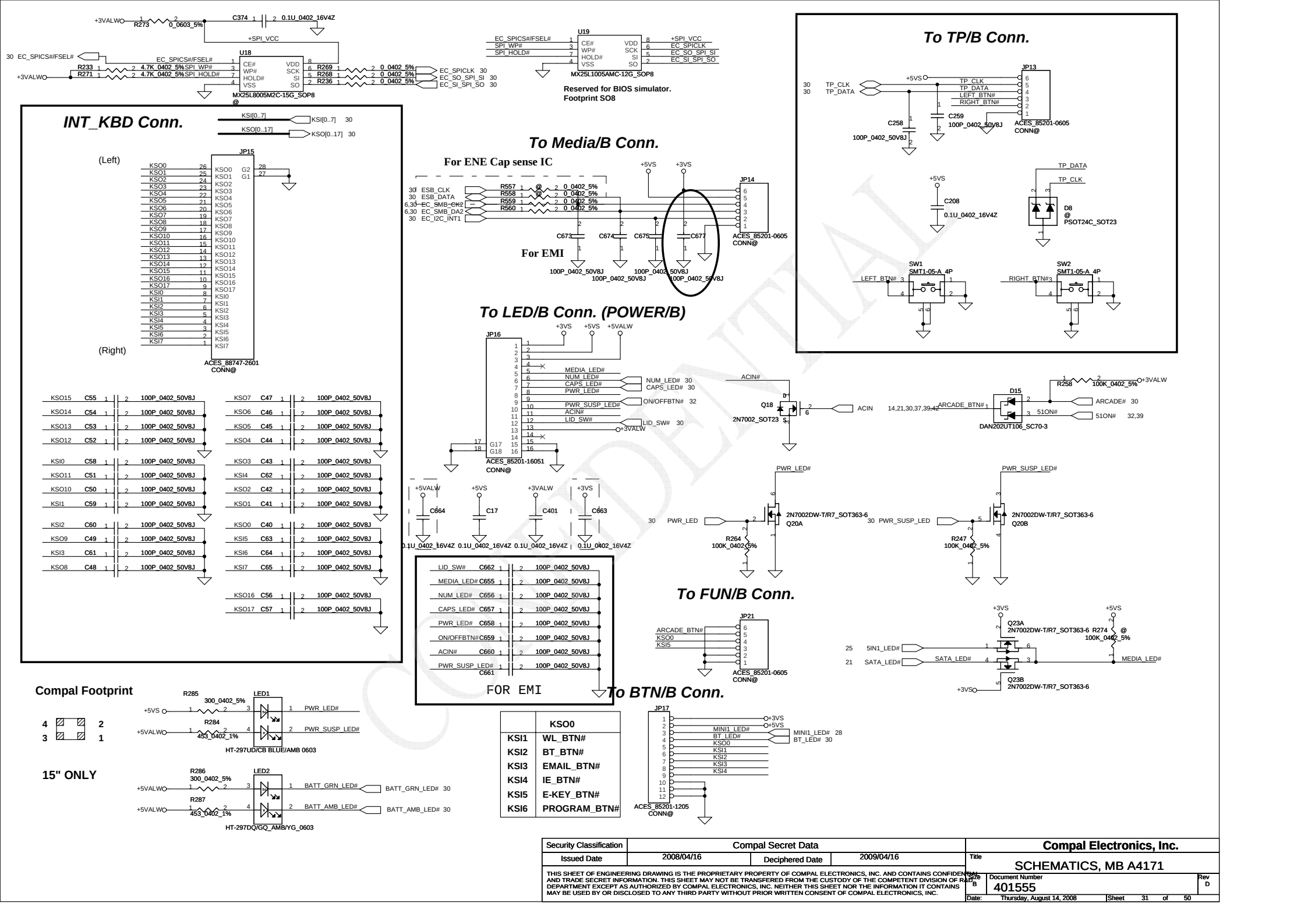




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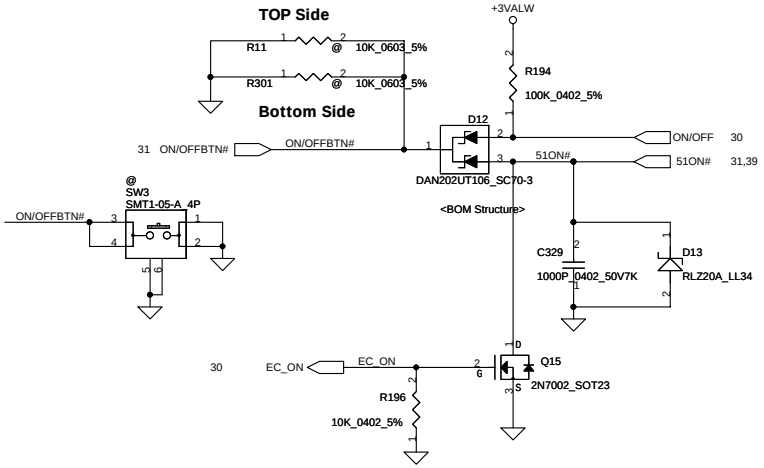
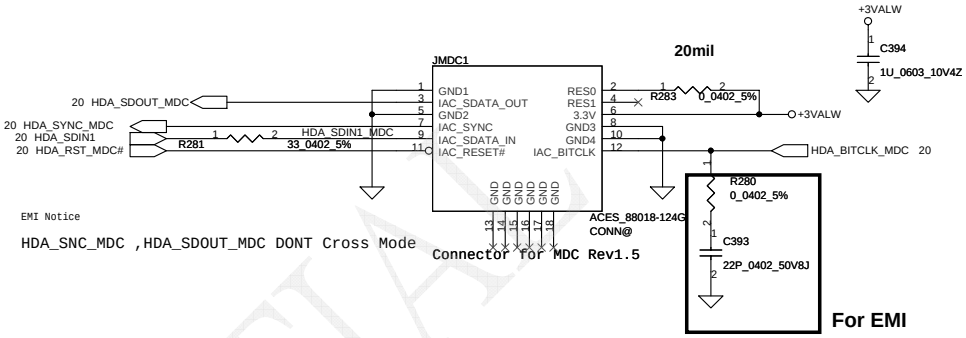
## Power Button

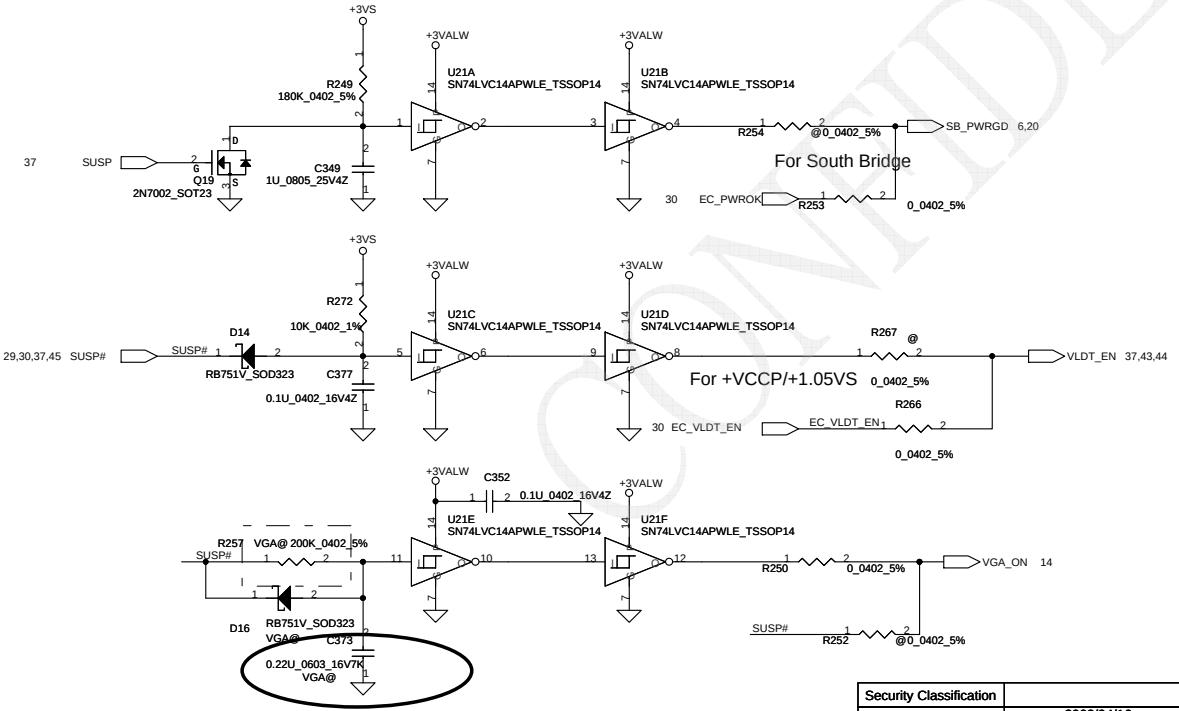
ON/OFF switch



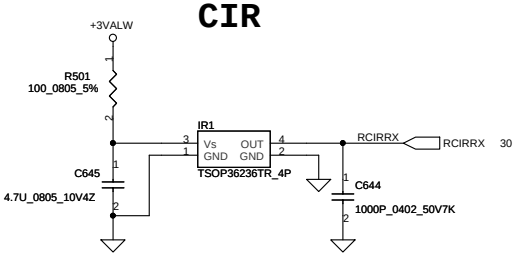

## HDA MDC Conn.




## Power ON Circuit




## CIR



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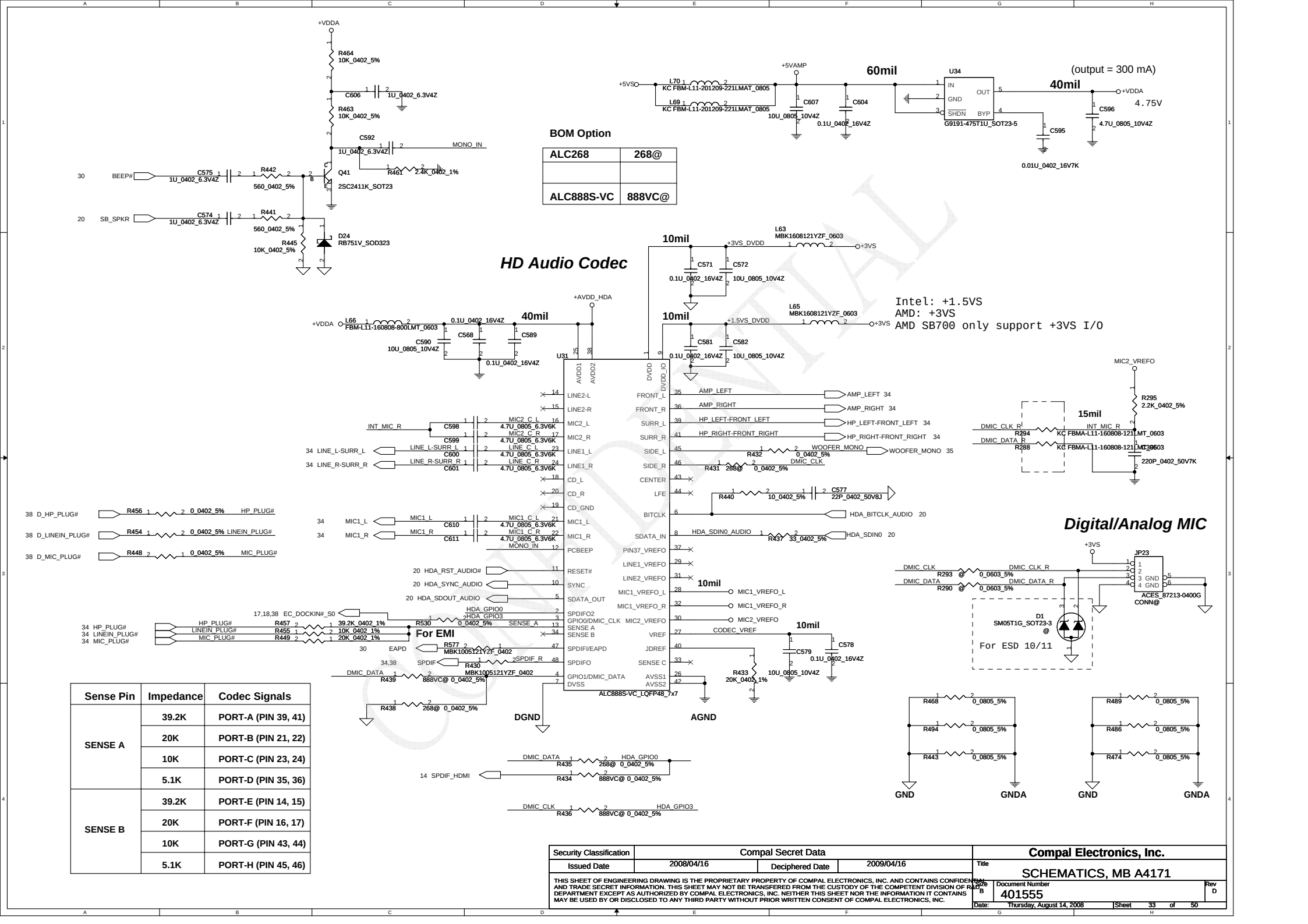




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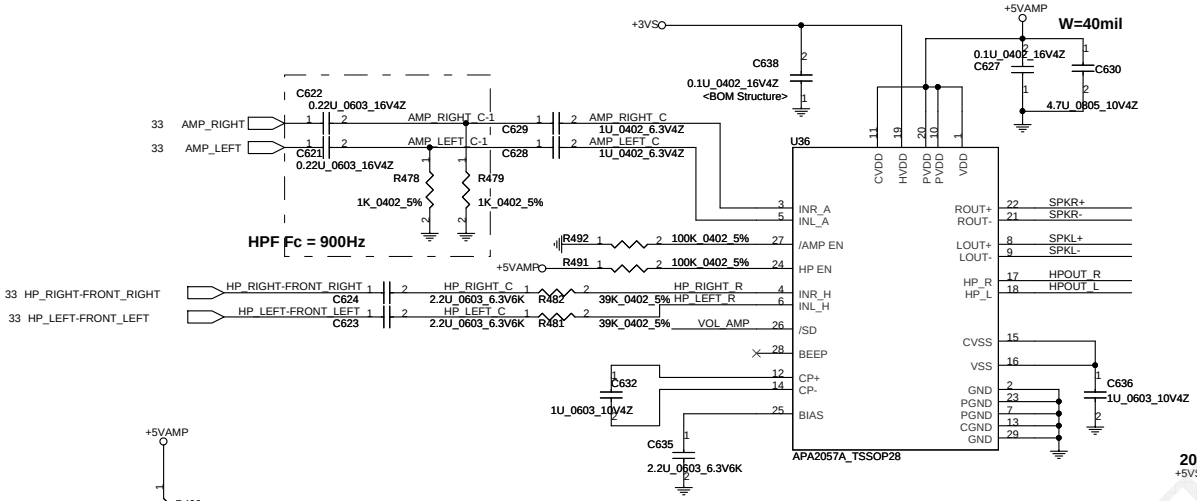
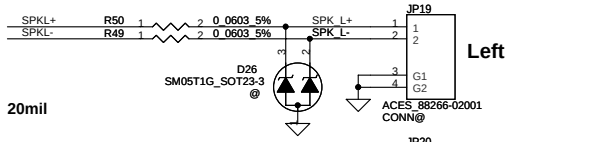
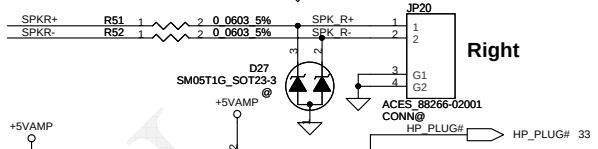
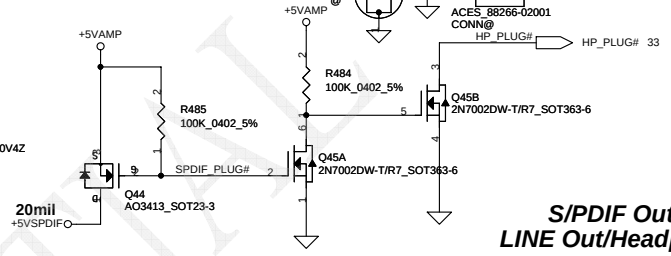


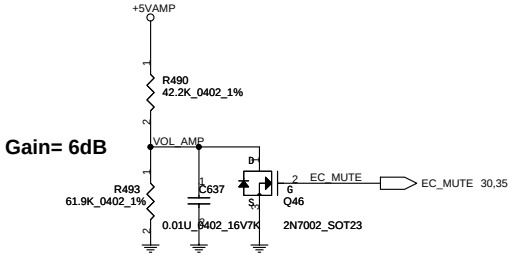

## Int. Speaker Conn.

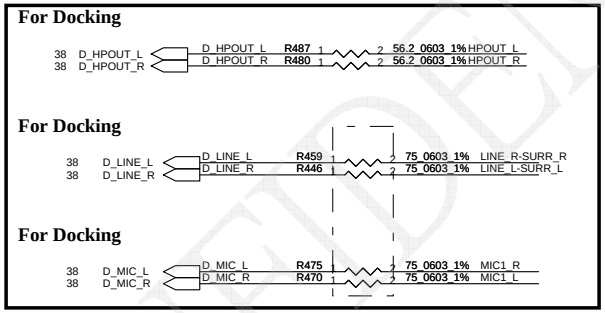


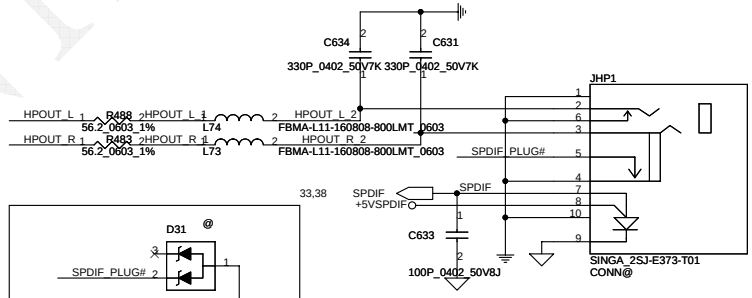




## S/PDIF Out JACK
## LINE Out/Headphone Out



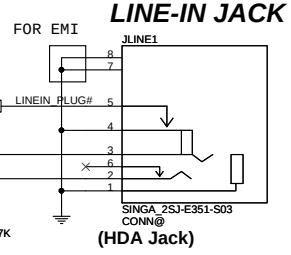



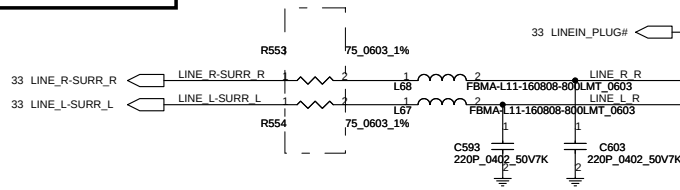





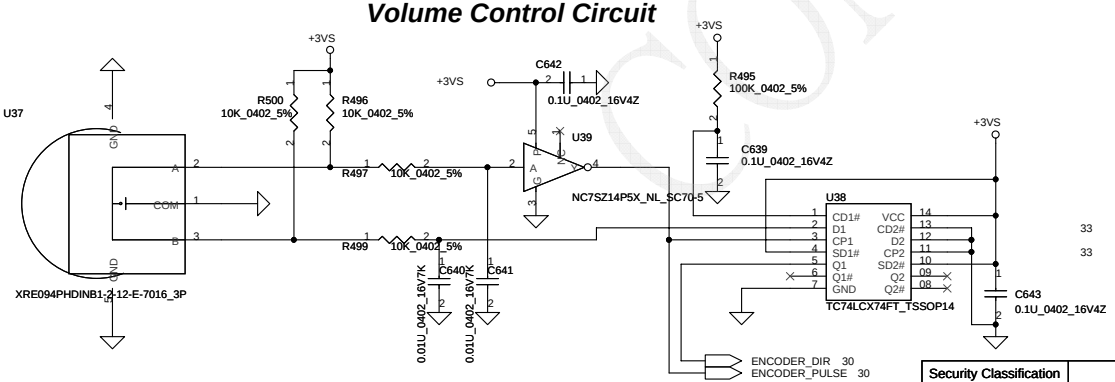


## LINE-IN JACK

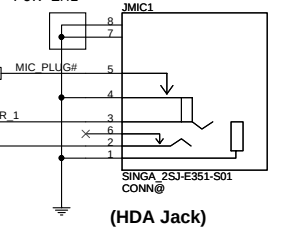


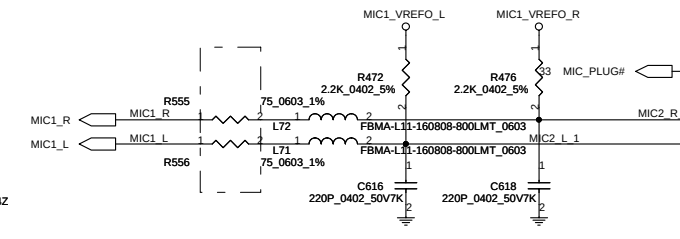




## Volume Control Circuit




## MIC JACK



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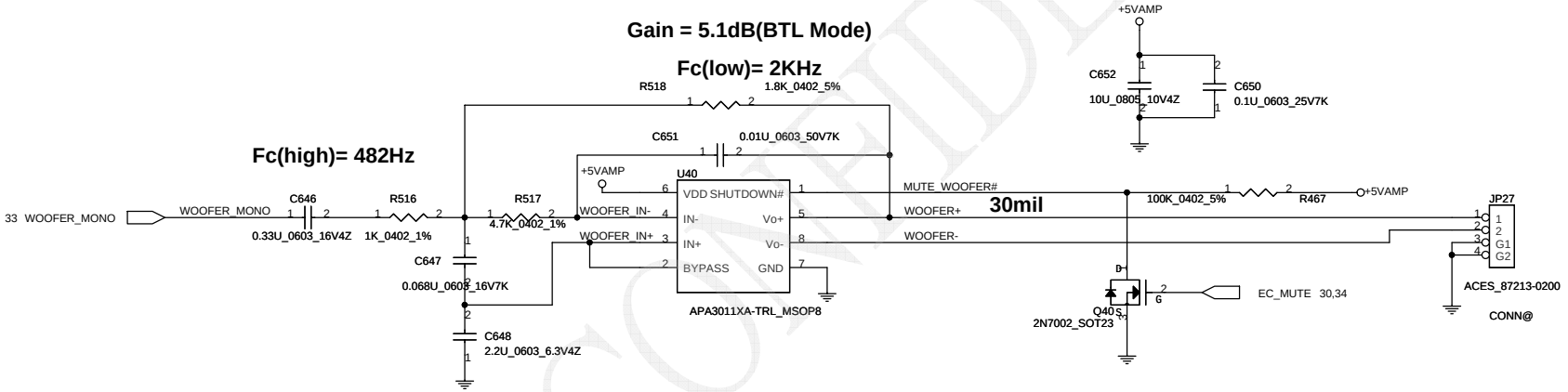




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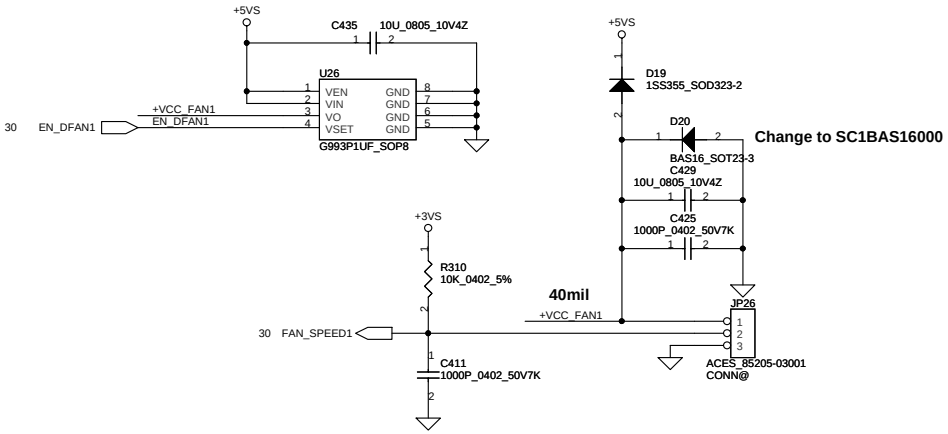
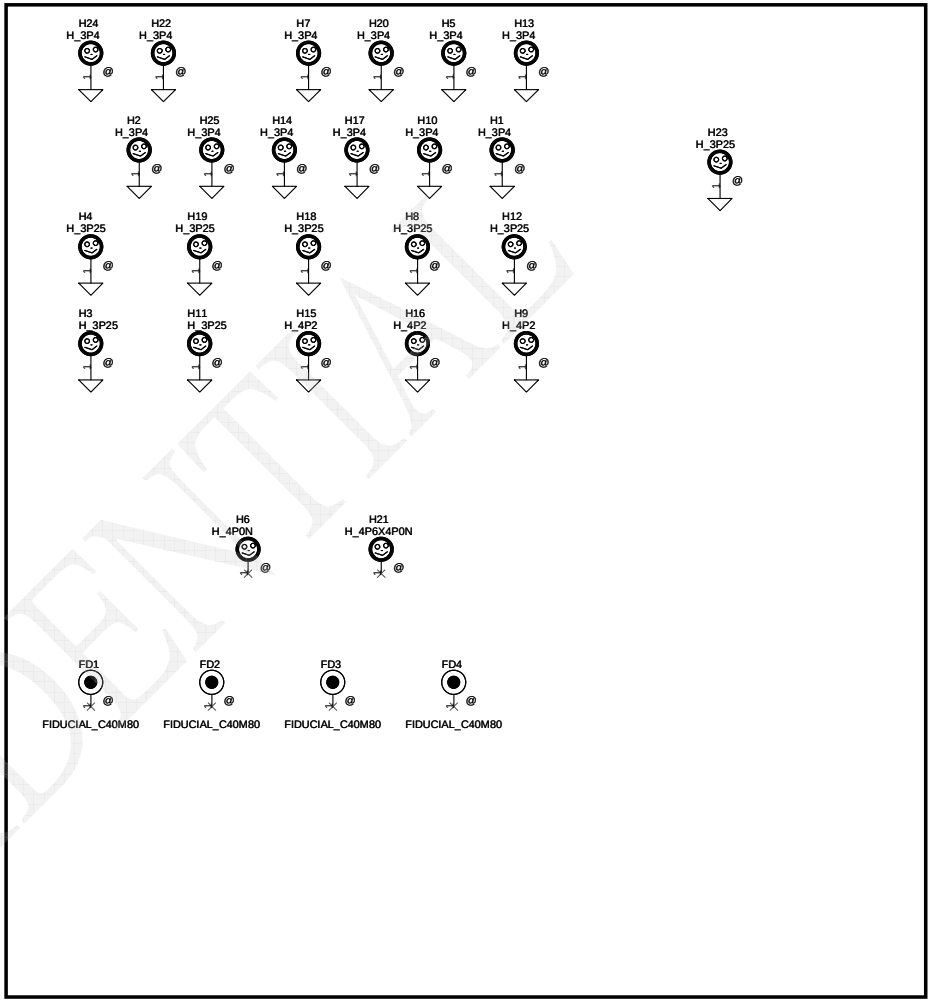
## FAN1 Conn



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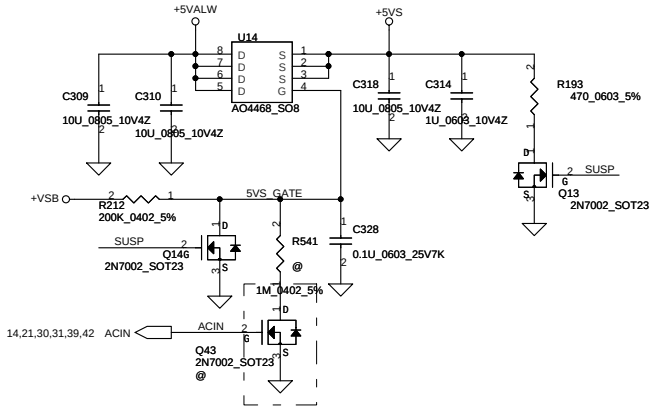
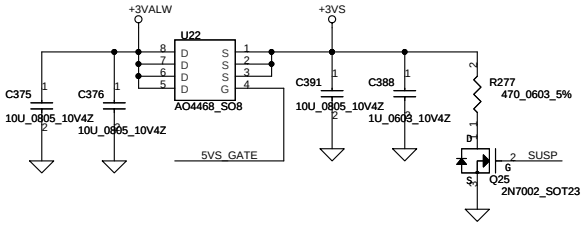
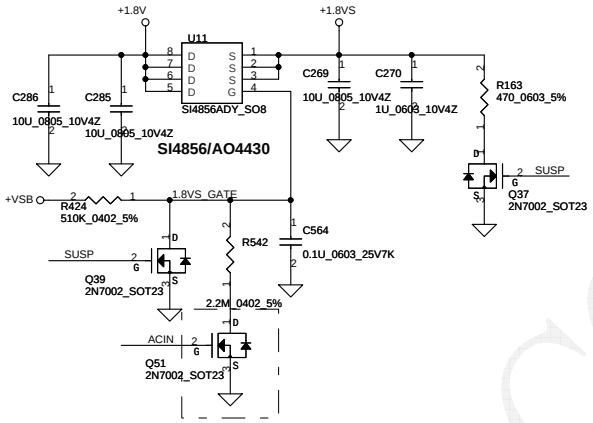
## +5VALW TO +5VS

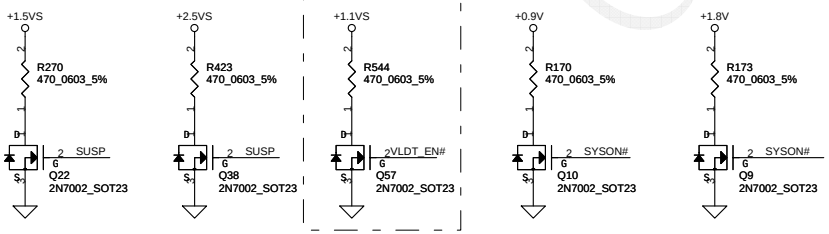


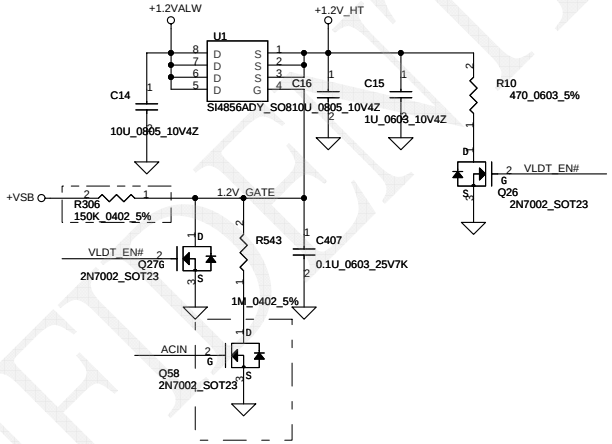

## +3VALW TO +3VS

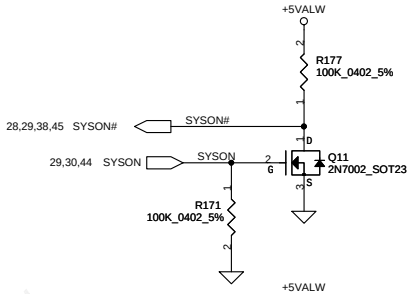


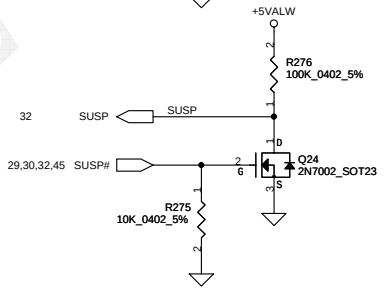

## +1.8V to +1.8VS

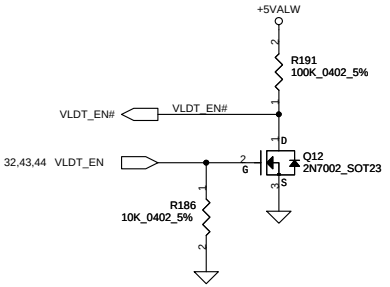


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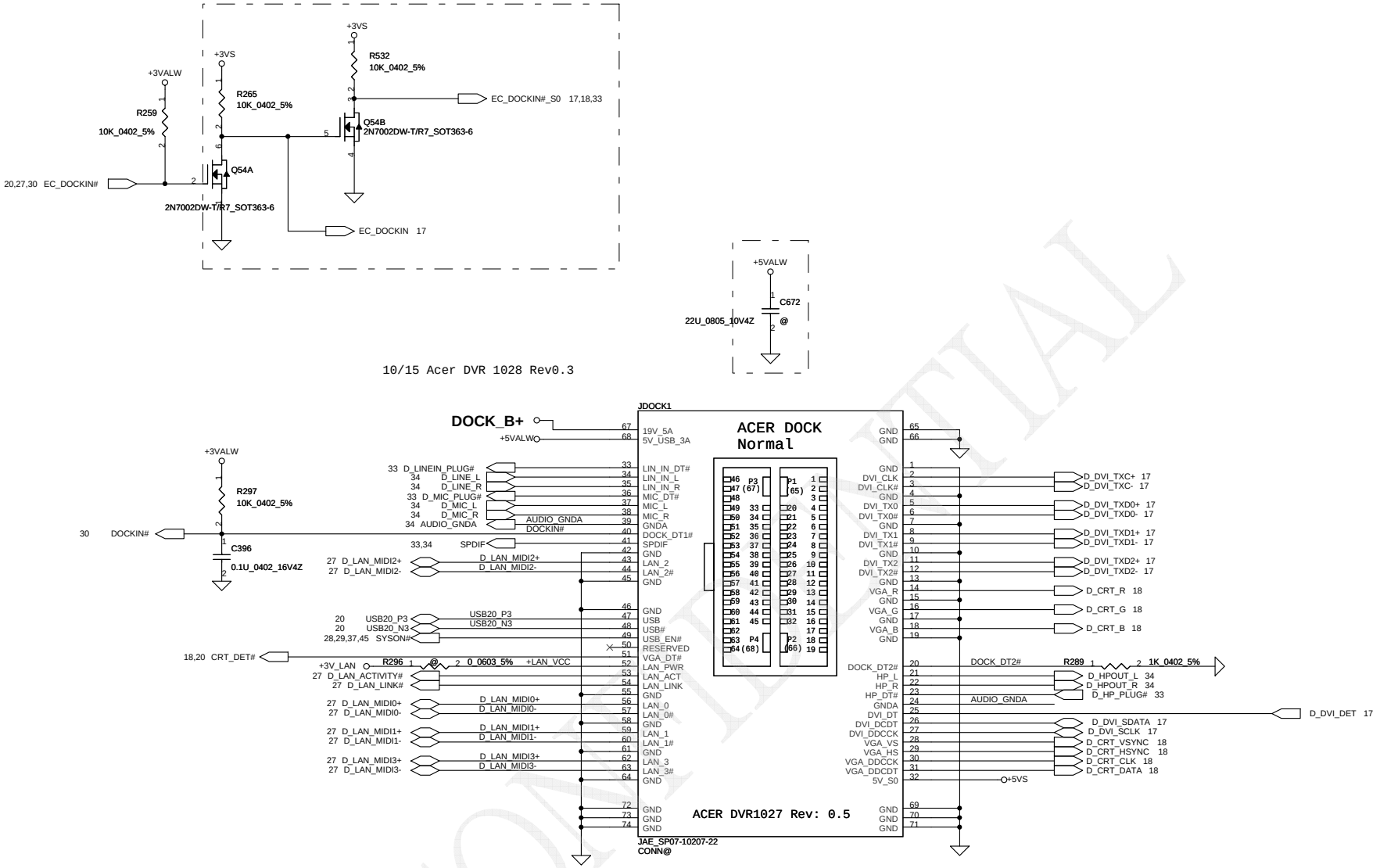




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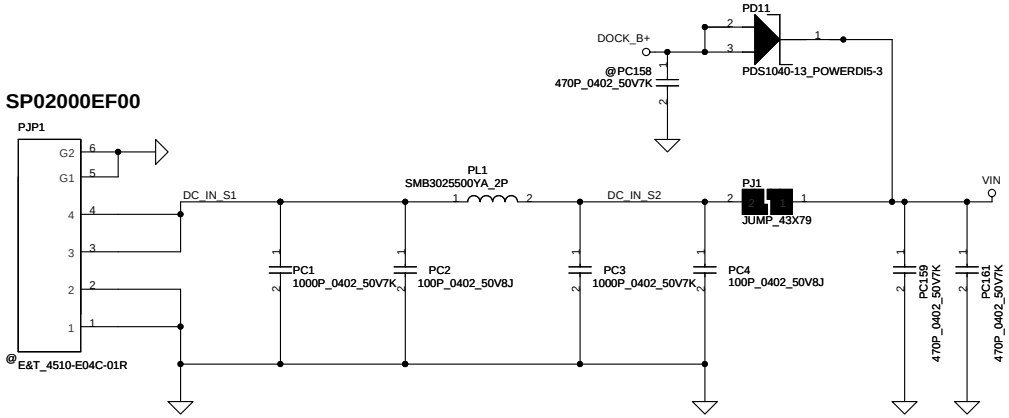
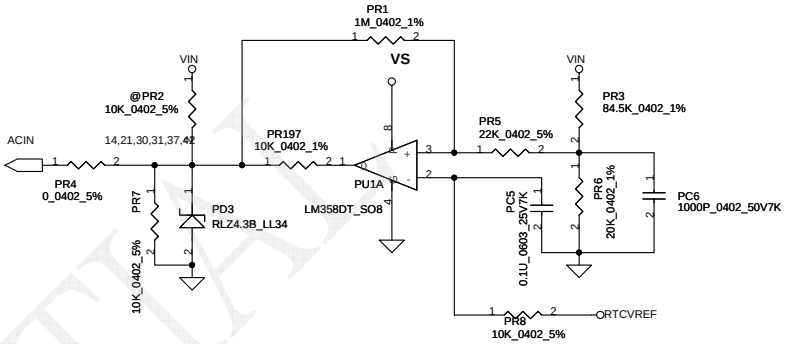
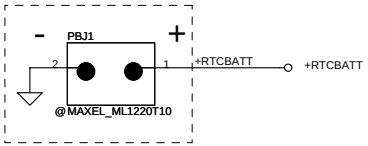


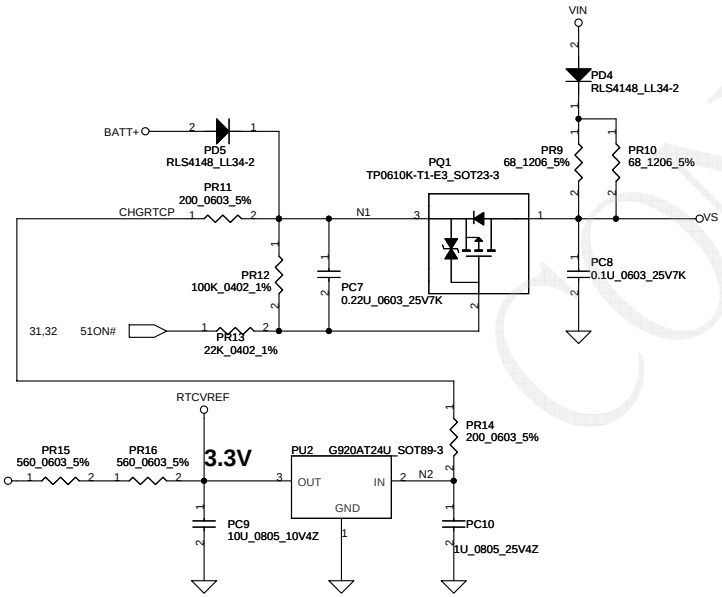

## RTC Battery

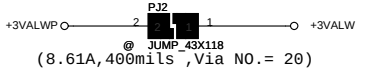



**SP093MX0000**

**Vin Dectector**

| | Min. | Typ | Max. |
|---|---|---|---|
| H-->L | 16.976V | 17.525V | 17.728V |
| L-->H | 17.430V | 17.901V | 18.384V |

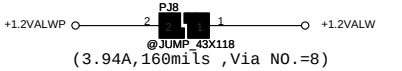


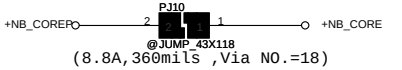

(8.61A,400mils ,Via NO.= 20)


(8.61A,400mils ,Via NO.= 20)


(120mA,40mils ,Via NO.= 2)

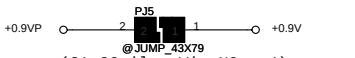



(3.94A,160mils ,Via NO.=8)

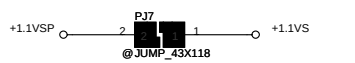



(8.8A,360mils ,Via NO.=18)

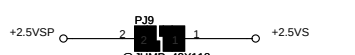

(12.06A,480mils ,Via NO.=24)




(2A,80mils ,Via NO.= 4)




(1.9A,80mils ,Via NO.=4)




(1.0A,40mils ,Via NO.=2)


(1.0A,40mils ,Via NO.=2)



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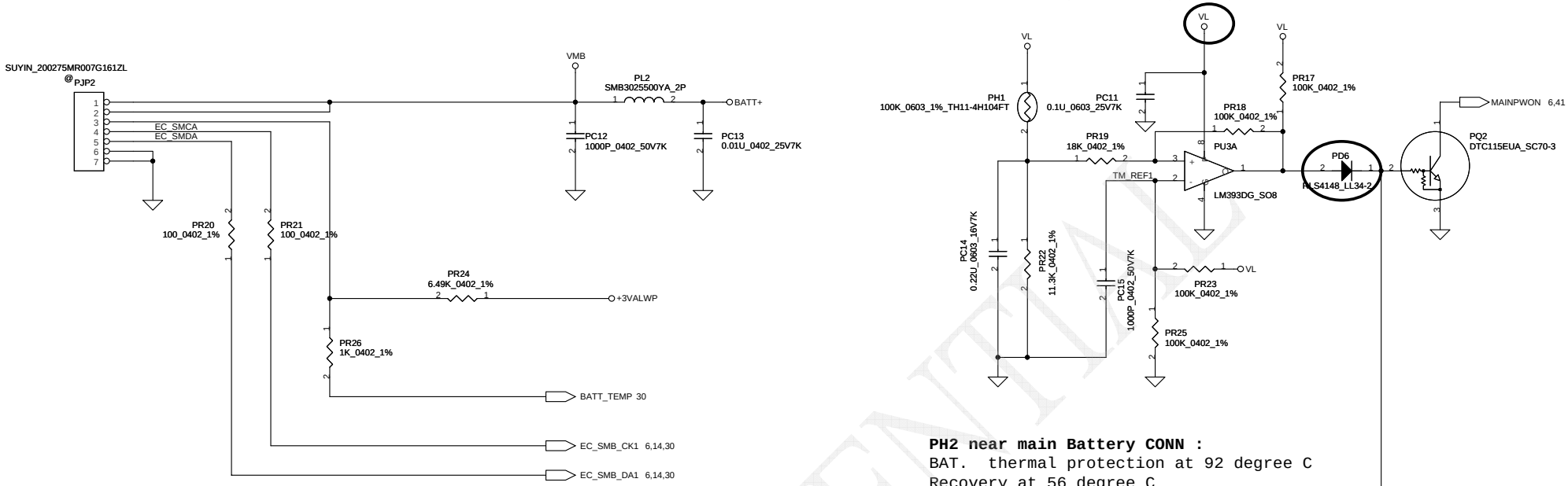
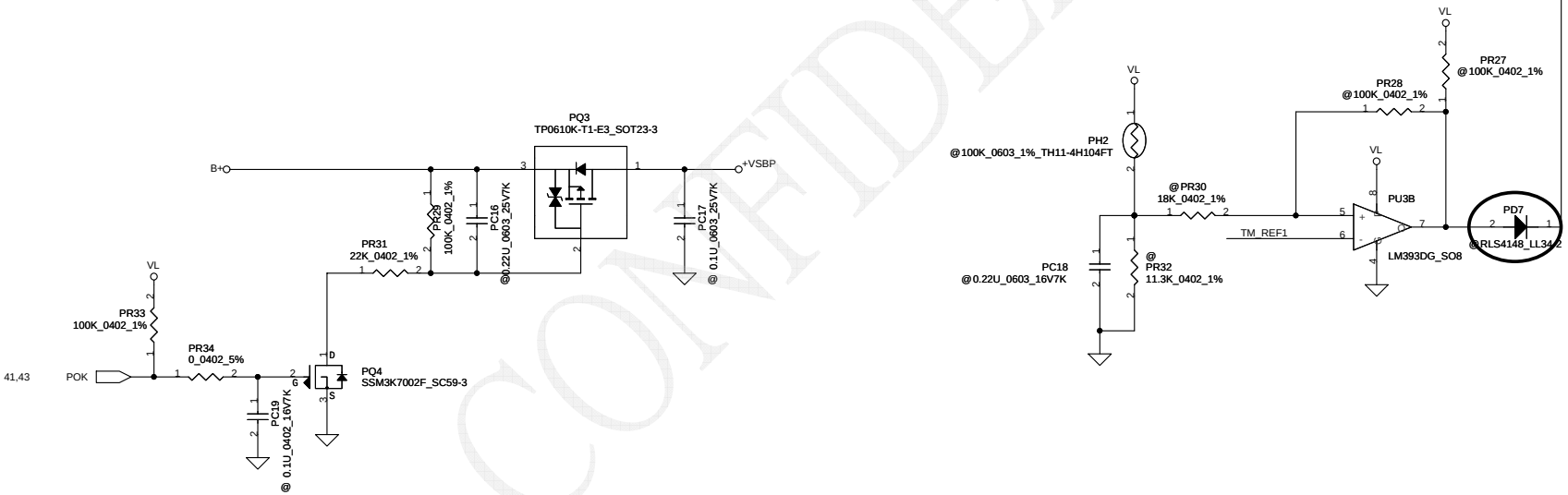
**PH1 under CPU botten side :**
CPU thermal protection at 92 degree C
Recovery at 56 degree C




**PH2 near main Battery CONN :**
BAT. thermal protection at 92 degree C
Recovery at 56 degree C



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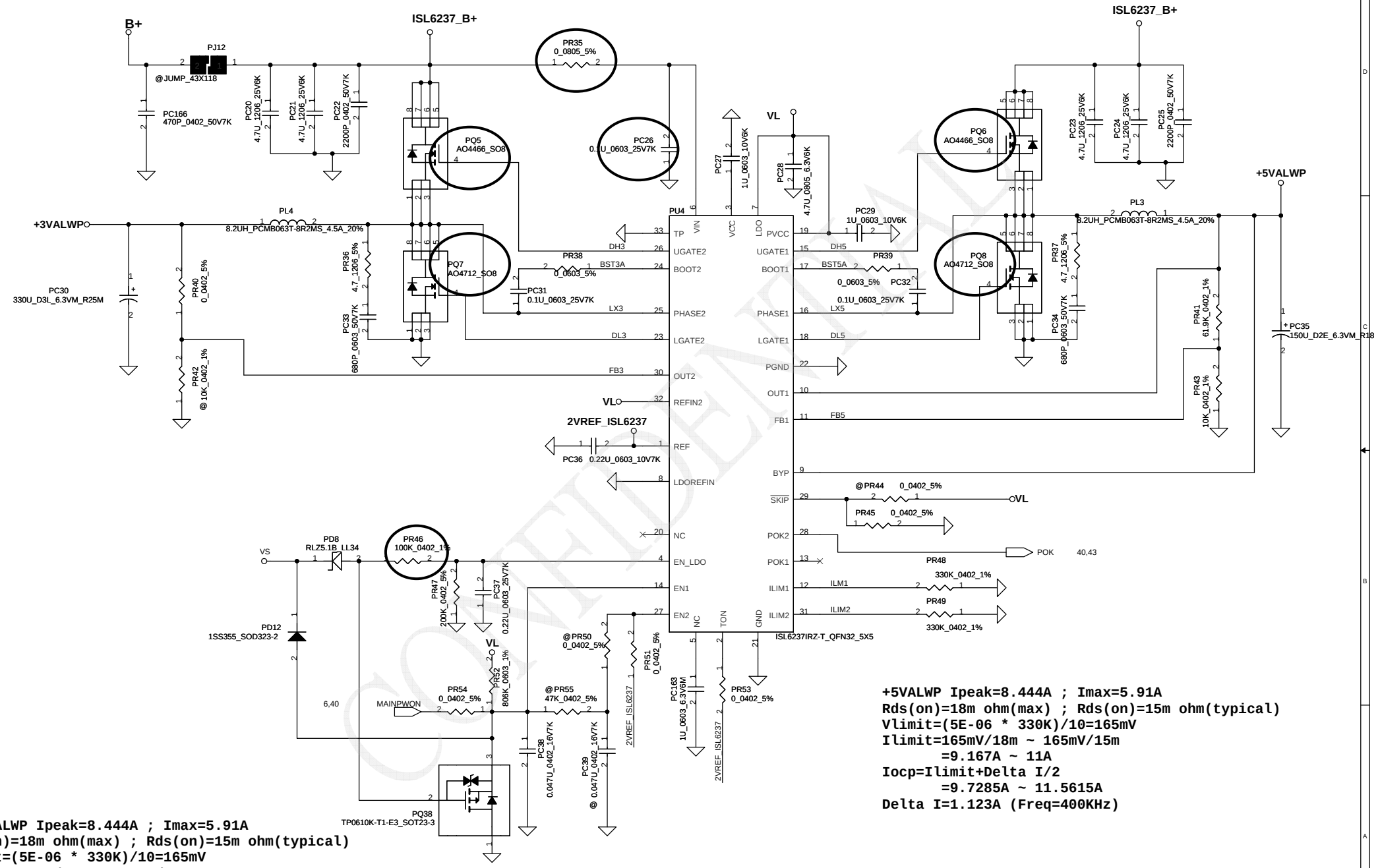


+3.3VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.721A ~ 11.554A
Delta I=1.108A (Freq=300KHz)

+5VALWP Ipeak=8.444A ; Imax=5.91A
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Vlimit=(5E-06 * 330K)/10=165mV
Ilimit=165mV/18m ~ 165mV/15m
=9.167A ~ 11A
Iocp=Ilimit+Delta I/2
=9.7285A ~ 11.5615A
Delta I=1.123A (Freq=400KHz)



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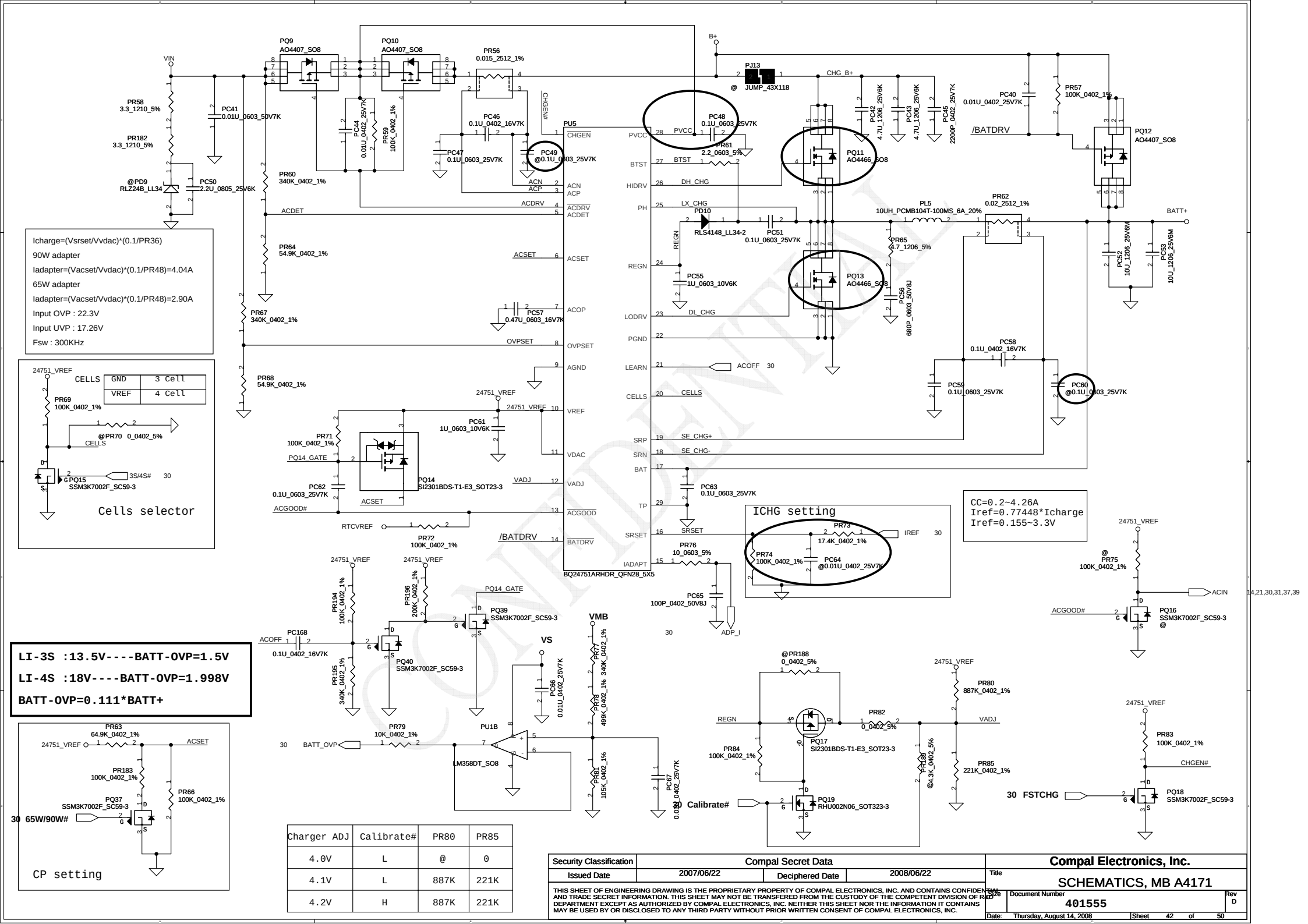




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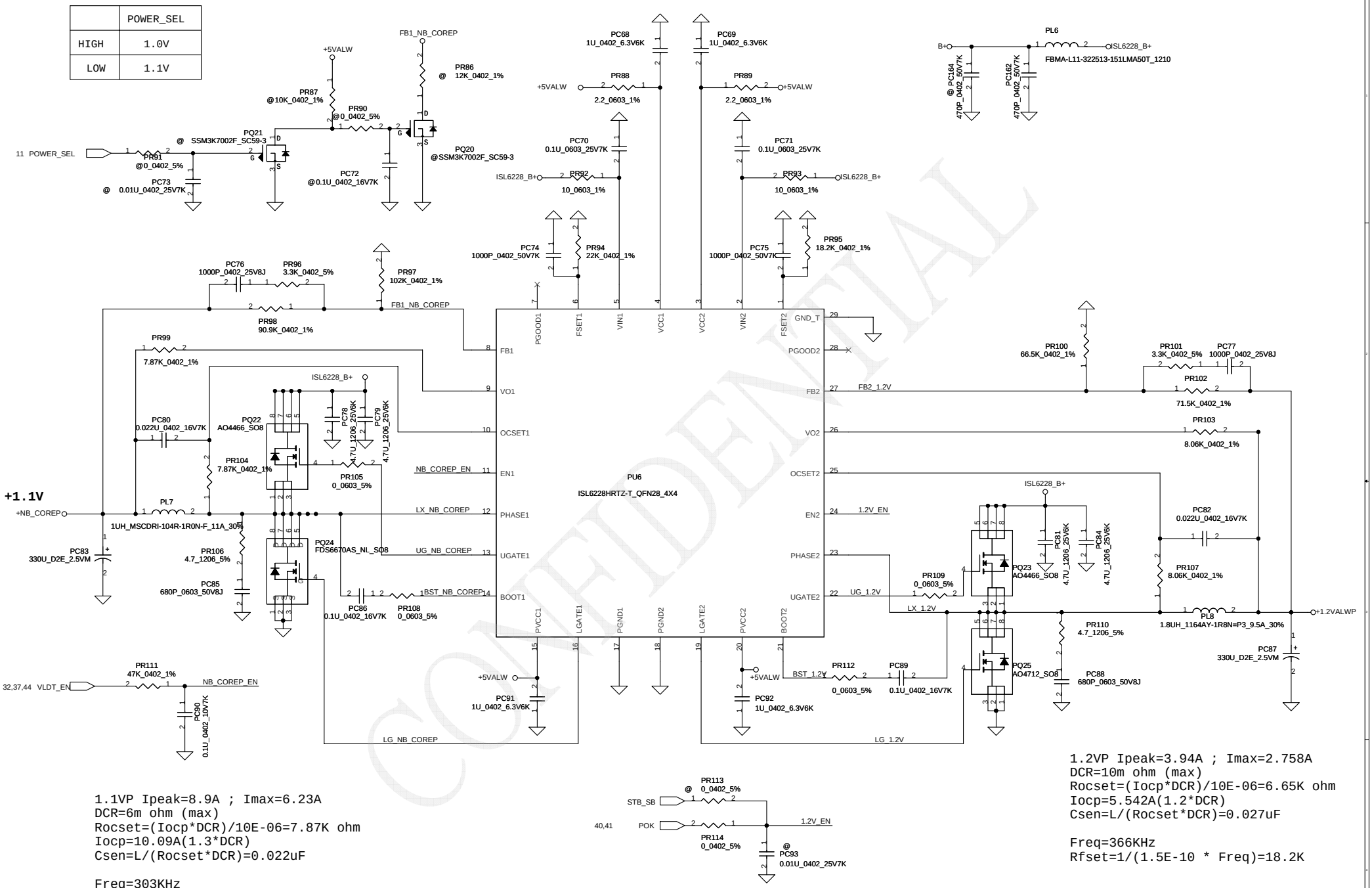
| | POWER_SEL |
|---|---|
| HIGH | 1.0V |
| LOW | 1.1V |




1.1VP Ipeak=8.9A ; Imax=6.23A
DCR=6m ohm (max)
Rocset=(Iocp*DCR)/10E-06=7.87K ohm
Iocp=10.09A(1.3*DCR)
Csen=L/(Rocset*DCR)=0.022uF

Freq=303KHz
Rfset=1/(1.5E-10 * Freq)=22K

1.2VP Ipeak=3.94A ; Imax=2.758A
DCR=10m ohm (max)
Rocset=(Iocp*DCR)/10E-06=6.65K ohm
Iocp=5.542A(1.2*DCR)
Csen=L/(Rocset*DCR)=0.027uF

Freq=366KHz
Rfset=1/(1.5E-10 * Freq)=18.2K



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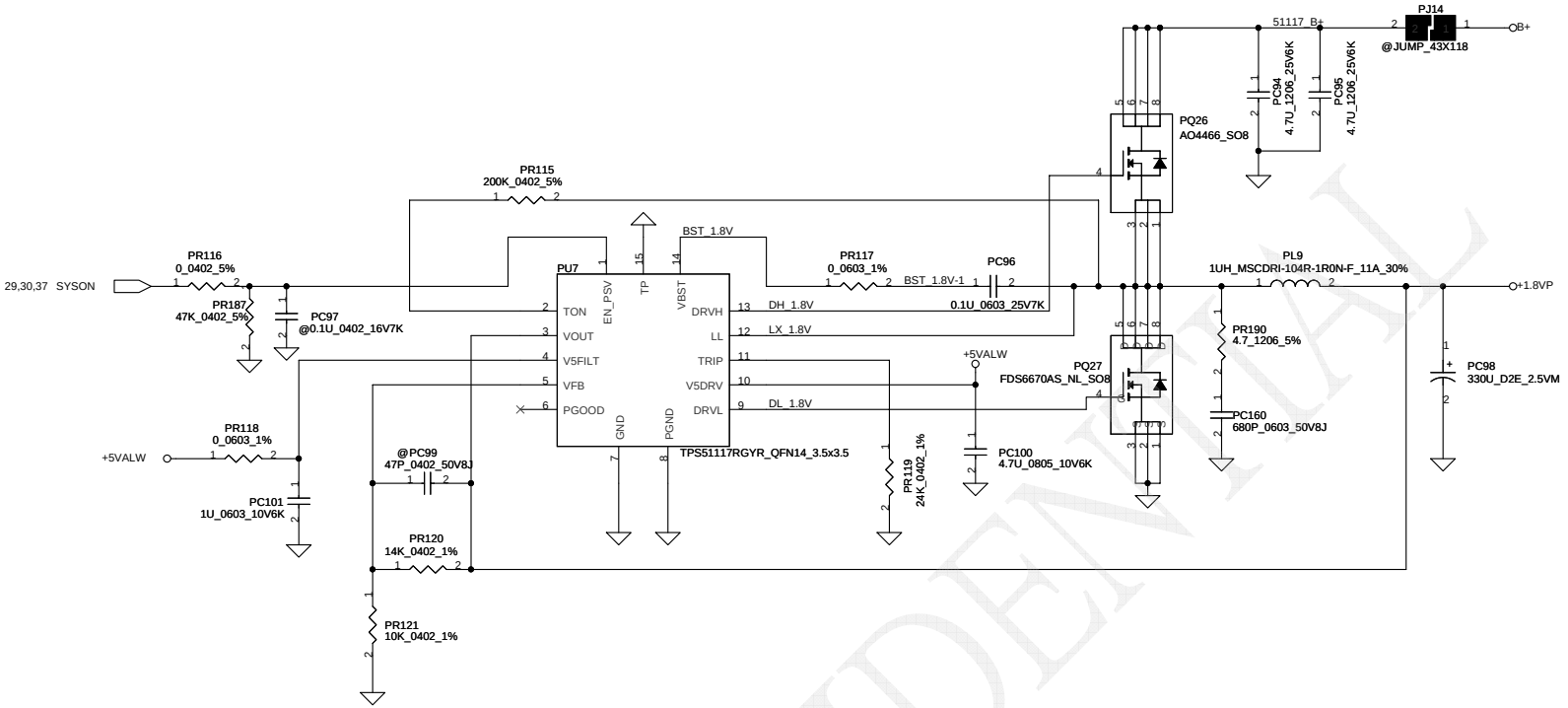
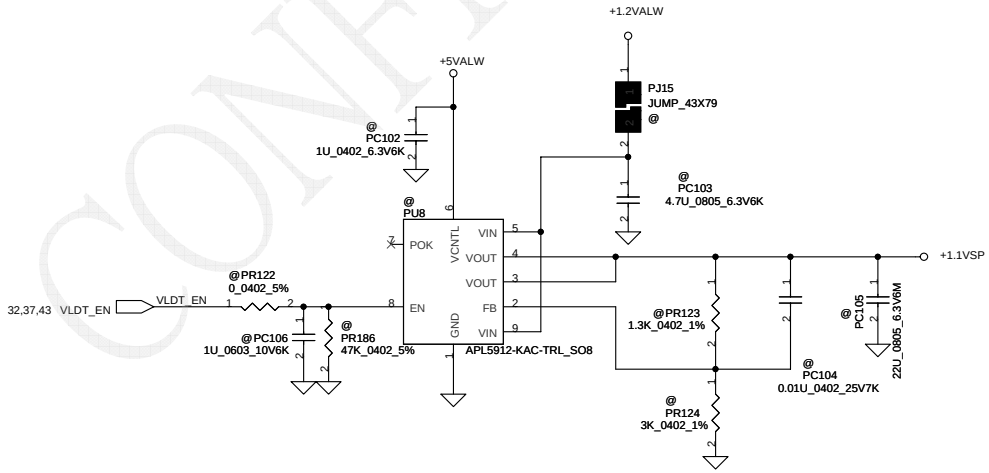



VFB=0.75V
Vo=VFB*(1+PR120/PR121)=1.8V
Ton=19E-12*Ron*(((2/3)*Vo+100mV)/Vin)+50ns=3.1E-07
Freq=305KHz

Cesr=15m ohm
Ipeak=12.6A  Imax=8.82A
Delta I=((19-1.8)*(1.8/19))/(L*Freq)=5.332A
Vtrip=Rtrip*10uA=0.24V
Iocp-min=Vtrip/Rdsonmax*1.4+2.666=17.573A
Iocp-max=Vtrip/Rdsontyp*1.2+2.666=26.908A
Iocp=17.573~26.908A



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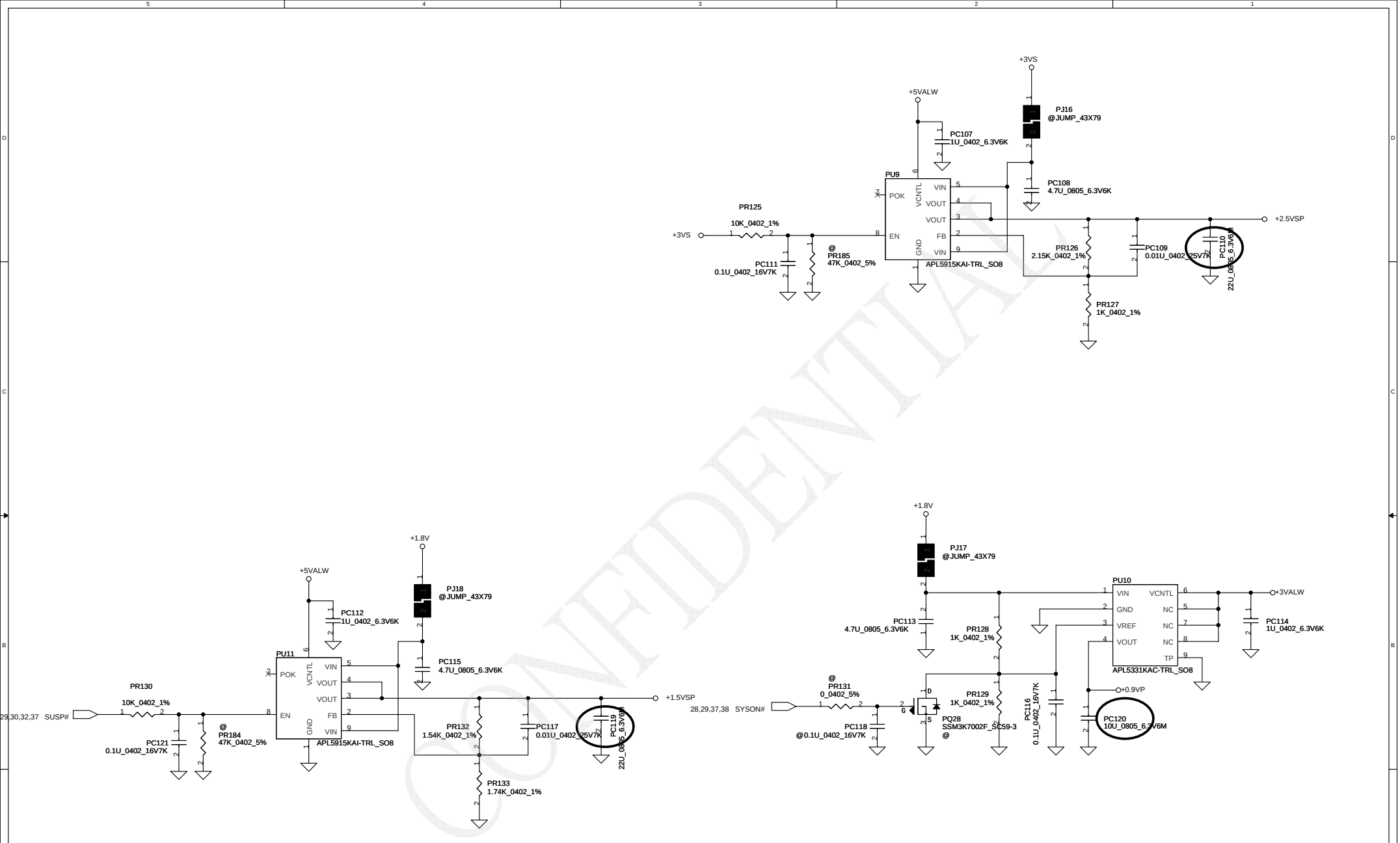




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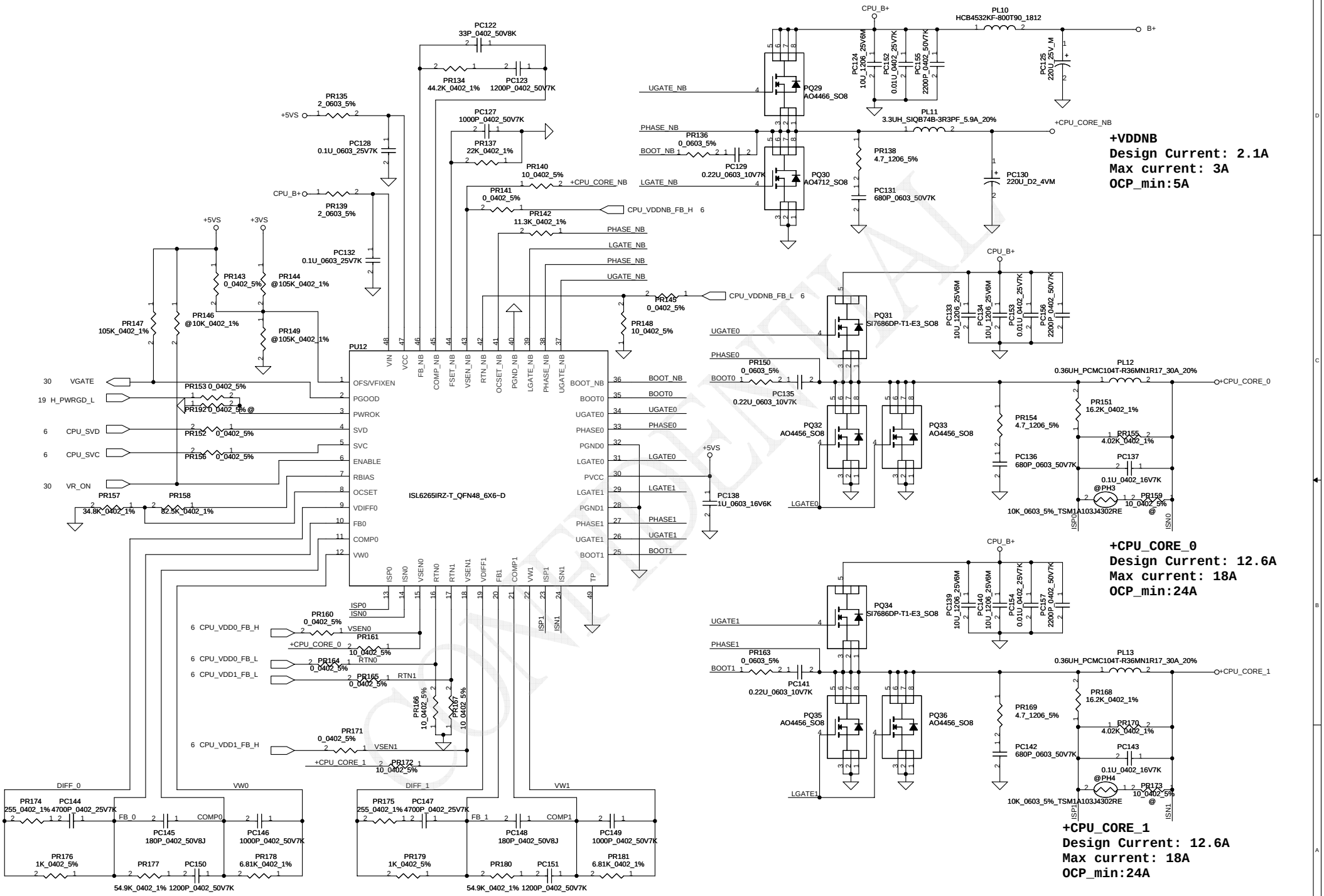


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|---|---|---|---|---|
| 7/9 | | DCIN | Change PL1 to bead coil | link to SM010008E10 |
| 7/9 | | DCIN | Link RTC battery symbol | link to SP093MX0000 |
| 7/9 | | Battery conn | Change PL2 to bead coil | link to SM010008E10 |
| 7/9 | | Battery conn | Change PD3,PD4 to RLS4148 | For low cost |
| 7/9 | | Battery conn | Change PU2 pin8 to VL | Design change |
| 7/9 | | Charger | Delete PU3 PVCC resistor and change PC26 to 1U | avoid PQ6 false turn-on when AC plug-in |
| 7/9 | | Charger | Change PQ7,PQ9 to AO4466 | For low cost |
| 7/9 | | Charger | Change PU4 pin8 to +5VALW | Design change |
| 7/9 | | Charger | Unpop PC28, PC37 | avoid interfere by other signal |
| 7/9 | | 3V/5V | Change PR54 and PC51 | Add design margine |
| 7/9 | | 3V/5V | Change MOSFET to AO4466+AO4712 | For low cost |
| 7/9 | | 1.8V/1.5V | Change MOSFET to AO4466+AO4712 | For low cost |
| 7/9 | | 1.8V/1.5V | Change PR75 to 2.2ohm | Design change |
| 7/9 | | 1.05V/1.25V/0.9V | Change MOSFET to AO4466+AO4712 | For low cost |
| 7/9 | | 1.05V/1.25V/0.9V | Change PC94 to 330U | Decrease overshoot |
| 7/9 | | 1.05V/1.25V/0.9V | Change PU7 PVCC source to +5VS | Design change |
| 7/9 | | 1.05V/1.25V/0.9V | Change PC105,PC108 size to 0805 | For low cost |
| 7/9 | | CPU CORE | Change input MLCC to 4pcs | Design change |
| 7/9 | | CPU CORE | Unpop PC111 | Reserve for high frequency noise |
| 7/10 | | Charger | Change PR38, PR39 and unpop PC32 | increase resistor to reduce power loss on resistor divider |
| 7/10 | | Charger | Change PR45, PR47 and unpop PC41 | increase resistor to reduce power loss on resistor divider |
| 7/10 | | Charger | Change PR43 to 100K | increase resistor to reduce power loss |
| 7/10 | | 3V/5V | Change PR65 to 100K_1% | Let BOM clear |
| 7/10 | | Charger/0.9V | Change PQ4,PQ11,PQ12,PQ13,PQ24 to SB000009080 | For low cost |
| 8/1 | | Charger | Change PR30 to 0.015ohm and PR38 to 80.6K | Change over power protection point |





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|---|---|---|---|---|
| | 12/11 | p.11 | DEL R26 | |
| | 12/11 | P.15 | UN-POP R234,POP R235 | |
| | 12/11 | P.17 | Change R123 to 2.2K | |
| | 12/11 | P.18 | ADD R525,R526,R527 | For non-Dockin sku |
| | 12/11 | P.20 | Del R128 | |
| | 12/11 | P.23 | Change R103 to 2.2k | |
| | 12/11 | P.25 | DEL U35,Q43,R473 | |
| | 12/11 | P.27 | ADD RP32,RP33,RP34,RP35,RP36 | For non-Dockin sku |
| | 12/11 | P.29 | Change U17 P/N to SA000029E00 | |
| | 12/11 | P.31 | Change JP14.4 Net to EC_SMB_CK2,JP14.5 Net to EC_SMB_DA2 | |
| | 12/11 | P.31 | Change LED1,LED2 P/N to SC597UDB000 | |
| | 12/11 | P.35 | Change U40.3 to WOOFER_IN+,U40,4 to WOOFER_IN- | |
| | 12/11 | P.38 | Del R291,R292 | |
| | 12/14 | P.30 | Raise KB926 pin.75 | |
| | 12/12 | P.14 | ADD D28 and pull high R529 to +3VS to AC_IN form JMXM1.157 | |
| | 12/12 | P.17 | Change Q47,Q48,Q49,Q50 P/N to SB501110010 | |
| | 12/12 | P.18 | DEL Q5,ADD Q52,Q53 | |
| | 12/12 | P.33 | Change U31 P/N to SA000026V00 | |
| | 12/12 | P.30 | Change Board ID | |
| | 12/12 | P.26 | Un-pop R56, POP R61 | |
| | 12/13 | P.25 | DEL U35,R473,Q43 | |
| | 12/13 | P.7 | DEL C762,C763 | |
| | | | | |
| | 12/14 | P.38 | update dock footprint and add CRT_Det# | |
| | 12/19 | P.18 | change CRT_DET to CRT_DET# from CRT to Q36 and output CRT_DET TO U10.J2 | |
| | 12/14 | P.26 | DEL U23,R305,C399,R28 | |
| | 12/14 | P.6 | Change R420, R419, R113 pull-up change to +1.8VS | |
| | 12/14 | P.12 | Delete U6, R68, R65, Q6, R55, C119, C113, C128, C151,C124 | Remove 1.35V LDO circuit |
| | 12/14 | P.12 | Del L22, POP L21 | Change VDDHTTX from 1.35V to 1.2V |
| | 12/14 | P.14 | Change C183 to 0402 package | |
| | 12/14 | P.16 | Change C12 to 0402 package | |
| | 12/14 | P.17 | Change R90,R91 from 1.5K to 2K | |
| | 12/14 | P.22 | Delete R399, add R391 | VDD should connect to S0 power on A12 |
| | 12/14 | P.34 | Change R480, R487 from 0Ohm to 75Ohm | |
| | 12/14 | P.37 | Change R306 to 10K | |
| | 12/14 | P.32 | Change D16.1 from +3VS to SUSP# | 1.2V_HT should faster than NB_CORE |
| | 12/19 | P.25 | Connect U33.16 to U10.AD18 (CR_WAKE#) through D29; U33.13 to U10.F2 (CR_PE#) through a MOS(Q55) | VGA_ON should drop before +3VS |
| | | | | |
| | 12/17 | P.28 | DEL TV_THERM#,ADD Port80 Signal to JMINI2.49,JMINI2.51 | |
| | 12/17 | P.19 | Delete R179,R185, add U12, U13 | |



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|---|---|---|---|---|
| | 12/17 | P.26 | Del BCM5787 Co-lay part | |
| | 12/17 | P.38 | ADD EC_DOCKIN#_S0 | |
| | 12/18 | P.25 | ADD R533 | |
| | 12/19 | P.11 | ADD Q54,R534 Level shift, and CPU_LDT_REQ#,ALLOW_LDTSTOP Pull high 300 to 1.8vs | |
| | 12/19 | P.20 | Change New Card CP_PE# to SB GPM5# | |
| | | | Change CRT_DET to SB GPM7# | |
| | | | Change EC_LID_OUT# to SB GPM4# | |
| | | | Del USB_OC#4 | |
| | 12/19 | P.6 | ADD R129,R538,R539 | |
| | 12/19 | P.21 | change R104 from 10K to 100K | |
| | 12/19 | P.34 | Change R488,R483 to 75 ohm | |
| | 12/19 | P.37 | Change R306 from 10K to 150K | |
| | 12/19 | P.6 | POP R93 | |
| | 12/19 | P.18 | change D18 from RB411 to RB491 | |
| | 12/19 | P.19 | Change Y2 location to X2 and p/n change to SJ132P7K220 | |
| | 12/19 | P.30 | EC_SMB_CK1,EC_SMB_DA1 Pull high to +3VALW,EC_SMB_CK2,EC_SMB_CK2 pull high to +3VS | |
| | 12/20 | P.37 | Reserve R541,R542,R543 | |
| | 12/20 | P.33 | Change R294,R288 P/N to SM010016720 | |
| | 12/20 | P.31 | ADD C655,C656,C657,C658,C659,C660,C661,C662 for EMI | |
| | 12/20 | P.37 | ADD Q57,R544 | |
| | 12/20 | P.34 | JMIC1.7,JMIC1.8,JLINE1.7,JLINE1.8 connect to AGND, | |
| | 12/21 | P.21 | Change SATA HDD Port to U10 SATA port 1 | |
| | 12/24 | P.21/P22. | Change D7,D9 P/N to SC1B751V010 | |
| | 12/24 | P.34 | Change L73,L74,L67,L68,L71,L72 P/N to SM010015410 | |
| | 12/24 | P.21 | ADD SPI ROM Schematic for SB700 | |
| | 12/24 | P.34 | JHP1.6,JHP1.10 connect to AGND | |
| | 12/24 | P.29 | Add U17 .21 to gnd | |
| | 12/24 | P.26 | Change U5.18,U5.17,U5.5,U5.33 connect to +1.2_VDDCIO | |
| | 12/26 | P.34 | Change R490 to 42.2K, R478,R479 to 1K,C621,C622 to 0.22u | |
| | 12/26 | P.35 | Change R516 to 6.8K | |
| | 1/22 | P.15 | Reversal MiniCard1 & MiniCard2 PCIE CLK Signal | |
| | 1/22 | P.37 | Change R275 from 100K to 10K | |
| | 1/22 | P.37 | Change Q57.2 to VLDT_EN# | |
| | 1/31 | P.6 | POP CPU internal themal sensor schematic | |
| | 1/31 | P.11 | change R64 to 133 ohm | |
| | 1/31 | P.14 | Add AND GATE | |
| | 1/31 | P.15 | Add C669 | |
| | 1/31 | P.17 | Change EC_DOCKIN#_S0 to Q50.2/Q49.2 | |
| | 1/31 | P.18 | Change EC_DOCKIN#_S0 to U7.1 | |
| | 1/31 | P.20 | Change CRT_DET to U10.H7,add EC_DOCKIN# to U10.B9 | |



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|---|---|---|---|---|
| | 1/31 | P.21 | Reserve AND gate form ACIN to U10.A4 | |
| | 1/31 | P.28 | Reserve MINI1_LED# Pull high 100K to +3VS | |
| | 1/31 | P.30 | ADD R551,R552 (VR_ON pull down 100k,BT_ON# Pull 100k) | |
| | 1/31 | P.30 | Del JP12 | |
| | 1/31 | P.33 | Change R257 from 200k to 330k | |
| | 1/31 | P.33 | ADD EC_DOCKIN#_S0 to R530.1 | |
| | 1/31 | P.34 | Change R459,R446,R475,R470 to 75ohm | |
| | 1/31 | P.34 | Add R553,R554,R555,R556 | |
| | 1/31 | P.38 | Add C672 | |
| | 2/4 | P.25 | For EMI request,add C676 | |
| | 2/4 | P.31 | For EMI request,add C673,C674,C675 | |
| | 2/4 | P.34 | For EMI request,add D31 | |
| | 2/12 | P.6 | Change R361,R365 to 2.2k | |
| | 2/12 | P.30/31 | ADD ESB_CLK/ESB/DATA (add R557,R558,R559,R560,R561,R562) | |
| | 2/13 | P.28 | ADD R563 | |
| | 2/14 | P.6/20 | UPDATE cpu internal themal sensor schematic (add R564,R565,R566,R567,R568,R569,ADD CPU_SIC_SB,CPU_SID_SB) | |
| | 3/12 | | R493=>61.9K (SD034619280)<br>R516=>1K (SD028100180)<br>R517=>4.7K (SD028470180)<br>R518=>1.8K (SD028180180)<br>C647=> 0.068u (SE026683K80) | |
| | 3/12 | P.33 | For EMI request,Change R440 to SD028100A80 | |
| | 3/12 | P.12 | Change C109,C150,C130,C88,C92,C35,C34,C36,C38 to SE000000I10 (22U) | |
| | 3/12 | P.7 | Change C77,C78,C79,C80 to SGA00002380 | |
| | 3/12 | P.37 | Change R186 to10K | |
| | 3/17 | P.11 | ADD R570,R571, Un-pop Q28,Q56,R324,R534 | |
| | 3/26 | P.6 | Un-pop R351,C436,R360,R566,R568,Q31,Q30 | |
| | 3/26 | P.19 | Change C192,C22 to 22p | |
| | 3/26 | P.34 | Change R487,R480,R488,R483 to 56.2 | |
| | 4/16 | P.8 | Change C257 from 0.1U to 1UF | |
| | 4/16 | P.19 | Change C192, C212 to 12P for RTC Timer issue | |
| | 4/16 | P.28 | Add L, C on SYSON# signal close to USB/B connector and TV/B connector | |
| | 4/16 | P.30 | Change the board ID back to R0.3 for BIOS identify issue | |
| | 4/16 | P.31 | Add 100pF capacitor on +3VS close to MEDIA/B | |
| | 4/16 | P.32 | Change C373 to 0.22U_0603_X7R for VGA power sequence | |
| | 4/16 | P.32 | Remove power on/off button SW3 for MP BOM | |
| | 4/16 | P.37 | Reserve voltage divider circuit on Power MOS | |
| | 4/23 | P.31 | change R285,R286 resistor value to 300 ohm | |
| | 4/23 | P.31 | change R284,R287 resistor value to 453 ohm | |
| | 4/30 | P.30 | change R216,R217 resistor value to 2.2k ohm | |
| | 5/20 | P.22 | Add R578 | |
| | 5/20 | P.24 | Add C681,C682 | |



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