

# ACER\_BAP31

## MAIN BOARD

2008.12.29

|                         |            |     |
|-------------------------|------------|-----|
|                         |            |     |
|                         |            |     |
|                         |            |     |
|                         |            |     |
|                         |            |     |
| Tuesday, March 10, 2009 |            | X01 |
| DATE                    | CHANGE NO. | REV |

|                         |    |      |       |      |                    |      |                       |     |
|-------------------------|----|------|-------|------|--------------------|------|-----------------------|-----|
|                         | EE | DATE | POWER | DATE | INVENTEC           |      |                       |     |
| DRAWER                  |    |      |       |      | TITLE<br>ACER_JM31 |      |                       |     |
| DESIGN                  |    |      |       |      |                    |      |                       |     |
| CHECK                   |    |      |       |      |                    |      |                       |     |
| RESPONSIBLE             |    |      |       |      |                    |      |                       |     |
| SIZE=                   |    |      |       |      | SIZE               | CODE | DOC NUMBER            | REV |
| FILE NAME: XX00XXXXXX00 |    |      |       |      | C                  | X01  | D-CS-1310A2264501.AJG | X01 |
| P/N   XX0000000000      |    |      |       |      | SHEET 1 of 36      |      |                       |     |

# 1. Schematic Page Description :

## Montevina Schematic Ver : X01

1. Title

2. Schematic Page DESCR

3. Block Diagram

4. Annotations

5. Schematic Modify

6. Timing Diagram

7. Power Block Diagram

8. Adaptor in/Charge

9. 5VLA/5VA/3VA

10. 3VS/5VS/1.5V (DDR3)

11. 1.05VS/1.5S/1.8V/1.5VA

12. Power Latch/1.5VS/SCREW HOLE

13. CPU Core Power

14. GPU Core Power

15. Penryn Processor(1/2)

16. Penryn Processor(2/2)

17. CPU Thermal

18. Cantiga Host(1/6)

19. Cantiga DMI/Graph(2/6)

20. Cantiga DDRII(3/6)

21. Cantiga Power(4/6)

22. Cantiga Power(5/6)

23. Cantiga Ground(6/6)
24. Clock Generator

25. DDR3 SDRAM SO-DIMM0

26. DDR3 SDRAM SO-DIMM1

27. ICH9M CPU/IDE/SATA(1/4)

28. ICH9M PCI/PCIE/DMI/USB(2/4)

29. ICH9M GPIO(3/4)

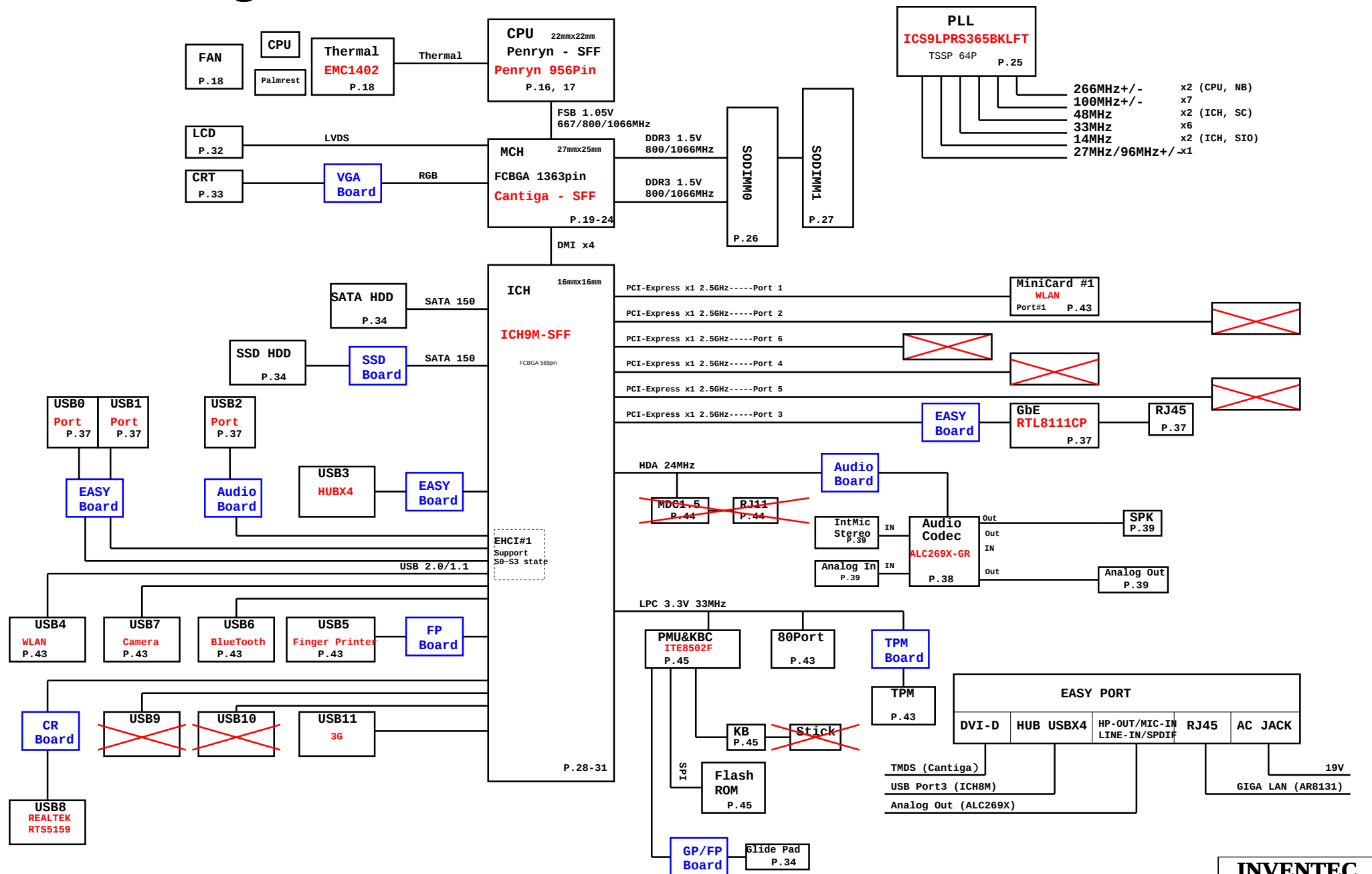
30. ICH9M Power/GND(4/4)

31. LCD CNN/SATA/3G/WLAN

32. KBC ITE8512F

33. IO CN

# 3. Block Diagram :



# 4. Net name Description :

## Voltage Rails

|                 |                                                                                             |
|-----------------|---------------------------------------------------------------------------------------------|
| DCIN            | Primary DC system power supply                                                              |
| +5VLA           | 5.0V always on power rail by LATCH or ACIN                                                  |
| +5VA            | 5.0V always on power rail by ECPWON                                                         |
| +3VA            | 3.3V always on power rail by ECPWON                                                         |
| +5VS            | 5.0V switched power rail by SLP_S3#_3R                                                      |
| +3VS            | 3.3V switched power rail by SLP_S3#_3R                                                      |
| +1.8VS          | 1.8V switched power rail by SLP_S3#_3R                                                      |
|                 |                                                                                             |
| VCC_CORE        | Core Voltage for CPU                                                                        |
| +1.05VS         | 1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R                          |
| +1.25VS         | 1.25V switched power rail by SLP_S3#_3R                                                     |
| +1.5VS          | 1.5V power rail for CPU PLL/DMI;PCIE;DDRIII DLLs for GMCH/Core;PCIE for ICH9M by SLP_S3#_3R |
|                 |                                                                                             |
| +1.5V           | 1.5V power rail for DDRII by SLP_S5#_3R                                                     |
| 0.75VDDT_DDRIII | 0.75V DDRII Termination Voltage by SLP_S3#_3R                                               |

## Part Naming Conventions

|    |   |                        |
|----|---|------------------------|
| C  | = | Capacitor              |
| CN | = | Connector              |
| D  | = | Diode                  |
| F  | = | Fuse                   |
| L  | = | Inductor               |
| Q  | = | Transistor             |
| R  | = | Resistor               |
| RP | = | Resistor Pack          |
| U  | = | Arbitrary Logic Device |
| Y  | = | Crystal and Osc        |

## Net Name Suffix

|   |   |                   |
|---|---|-------------------|
| # | = | Active Low signal |
|---|---|-------------------|

# 5. Board Stack up Description

## PCB Layers

|         |  |                                         |
|---------|--|-----------------------------------------|
| Layer 1 |  | Component Side, Microstrip signal Layer |
| Layer 2 |  | Ground Plane                            |
| Layer 3 |  | Stripline Layer                         |
| Layer 4 |  | Power Plane                             |
| Layer 5 |  | Stripline Layer                         |
| Layer 6 |  | Stripline Layer                         |
| Layer 7 |  | Ground Plane                            |
| Layer 8 |  | Solder Side, Microstrip signal Layer    |

|             | Differential Impedance for Microstrip | Differential Impedance for Stripline |
|-------------|---------------------------------------|--------------------------------------|
| Host Clock  | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| PCI-E Clock | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| DDR3 CLK    | 75 ohm +/- 20%                        | 75 ohm +/- 20%                       |
| DDR3 Strobe | 90 ohm +/- 20%                        | 90 ohm +/- 20%                       |
| DMI Bus     | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| PCIE Bus    | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| SDVO        | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| SATA        | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| USB         | 90 ohm +/- 20%                        | 90 ohm +/- 20%                       |
| LVDS        | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |
| Lan         | 95 ohm +/- 20%                        | 95 ohm +/- 20%                       |

| Power Rail      | Destination                                                                                                                                                                                                                                                                       | Voltage                                                                                                                                                                                                                           | S0 Current                                                                                                  |
|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|
| VCC_CORE        | Penryn SFF HFM:<br>LFM:                                                                                                                                                                                                                                                           | 1.3319V-1.4375V-1.4591V<br>0.9221V-0.9625V-0.9739V                                                                                                                                                                                | 18A                                                                                                         |
| 1.05VS          | Penryn SFF : AGTL+ termination<br>Cantiga GS: Core<br>Cantiga GS: PCIE<br>Cantiga GS:Core+HMEL+HSIO<br>Cantiga GS:VCC_GMCH<br>Cantiga GS:VCCA_SM_CK and NCTF<br>Cantiga GS:VCC_DMI<br>Cantiga GS:VCCA_SM<br>Cantiga GS:VTT<br>ICH9M:VCC1_05<br>ICH9M:DMI<br>ICH9M:CPU_IO          | 1V-1.05V-1.10V<br>0.997V-1.05V-1.102V<br>0.9975V-1.05V-1.1025V<br>0.9975V-1.05V-1.1025V<br>0.997V-1.05V-1.102V<br>0.997V-1.05V-1.102V<br>0.997V-1.05V-1.102V<br>0.997V-1.05V-1.102V<br>0.997V-1.05V-1.102V<br>0.997V-1.05V-1.102V | 4.5A<br>8.7A<br>1.78A<br>2.898A<br>10.154A<br>37.95mA<br>456mA<br>747.5mA<br>852mA<br>1.634A<br>48mA<br>2mA |
| 1.5VS           | Penryn SFF PLL<br>Cantiga GS: QDAC<br>Cantiga GS: LVDS<br>Cantiga GS: TVDAC<br>Cantiga GS: Various PLLS analog supply<br>Cantiga GS: VCC_SM_CK<br>Cantiga GS: VCC_SM<br>ICH9M:PCIE_ICH<br>ICH9M:SATA_ICH<br>ICH9M:VCC_GLAN<br>Mini Card:<br>Express Card:                         | 1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V<br>1.71V-1.8V-1.89V<br>1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V<br>1.425V-1.5V-1.575V            | 130mA<br>0.5mA<br>60.31mA<br>35mA<br>485mA<br>149.5mA<br>3.1625A<br>646mA<br>1.342A<br>80mA<br>650mA        |
| 1.5V            | Cantiga GS: DDRIII System Memory                                                                                                                                                                                                                                                  | 1.425V-1.5V-1.575V                                                                                                                                                                                                                | 3.1A(800M) 4.1A(1067M)                                                                                      |
| 0.75VDDT_DDRIII | DDRIII Terminator:                                                                                                                                                                                                                                                                | 0.7125V-0.75V-0.7875V                                                                                                                                                                                                             | 1.0A                                                                                                        |
| 3VS             | Cantiga GS: HV CMOS<br>Cantiga GS: VCCS_TV DAC<br>ICH9M:VCC3_3<br>ICH9M:VCCGLAN3_3<br>Thermal Sensor:<br>Mini Card: UMTS<br>Express Card:<br>CLK Generator: ICS9LPRS365BKLFT<br>Mini Card: WirelessLan<br>Bluetooth:<br>Super I/O: IT8305E<br>Azalia Codec: ALC262<br>Azalia MDC: | 3.135V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.0V-3.3V-3.6V<br>3.135V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.0V-3.3V-3.6V<br>3.0V-3.3V-3.6V                                            | 105.3mA<br>78mA<br>308mA<br>1mA<br>5mA<br>1.3A<br>500mA                                                     |
| 1.8VS           | DVI                                                                                                                                                                                                                                                                               | 3.0V-3.3V-3.6V                                                                                                                                                                                                                    | 120mA                                                                                                       |
| 3VA             | ICH9M: RTC<br>ICH9M:VCCSUS3_3<br>ICH9M:VCCCL3_3<br>ICH9M:VCCLAN3_3<br>LCD:<br>Lan:AR8131<br>Azalia MDC:<br>Flash ROM: BIOS                                                                                                                                                        | 2V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.135V-3.3V-3.465V<br>3.0V-3.3V-3.6V<br>3.0V-3.3V-3.6V<br>3.0V-3.3V-3.6V                                                                                            | 6uA<br>212mA<br>73mA<br>78mA<br>2A<br>1A                                                                    |
| 5VS             | Cardreader: RTS5159<br>Azalia Codec: ALC269<br>HDD: SATA<br>ODD: SATA<br>Audio AMP: G1432<br>Inverter:<br>WebCam                                                                                                                                                                  | 3.0V-3.3V-3.6V<br>3.0V-3.3V-3.6V<br>4.75V-5.0V-5.25V<br>4.75V-5.0V-5.25V                                                                                                                                                          | Max: 1.5A ; R/W: 460mA ; STDBY: 70mA<br>Max: 1.5A ; R/W: 900mA ; STDBY: 45mA                                |
| 5VA             | USB: x 2 ports<br>USB                                                                                                                                                                                                                                                             | 4.75V-5.0V-5.25V<br>5VA<br>5VA                                                                                                                                                                                                    | 1A<br>2A<br>1.5A                                                                                            |
| 5VLA            | Control Power                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                   |                                                                                                             |
| 3VLA            | EC: ITE8512E                                                                                                                                                                                                                                                                      | 3.0V-3.3V-3.6V                                                                                                                                                                                                                    | 300mA                                                                                                       |

# 6.Schematic modify Item and History :

2009.0108

- 1. ADD USB P3 for Docking, USB P5 for Finger printer, Modify CN5 -----P28
- 2. Modify CN20 to 50pin-----P33
- 3. Move PWR\_SWIN# from CN14 to CN20
- 4. ADD TPM module-----P34

2009.0109

- 1. ADD DOCK\_USB\_EN, DOCK\_CRT\_IN#-----P32,33

2009.0112

- 1. Change power item: R490,R291,BAT CNN TH PIN

INVENTEC

TITLE

BAP31 (Penryn+Cantiga+ICH9M)SFF

SIZE

Custom

CODE

X01

DOC NUMBER

D-CS-1310A2264501.ALG

REV

X01

CHANGE by

Miles Liu

DATE

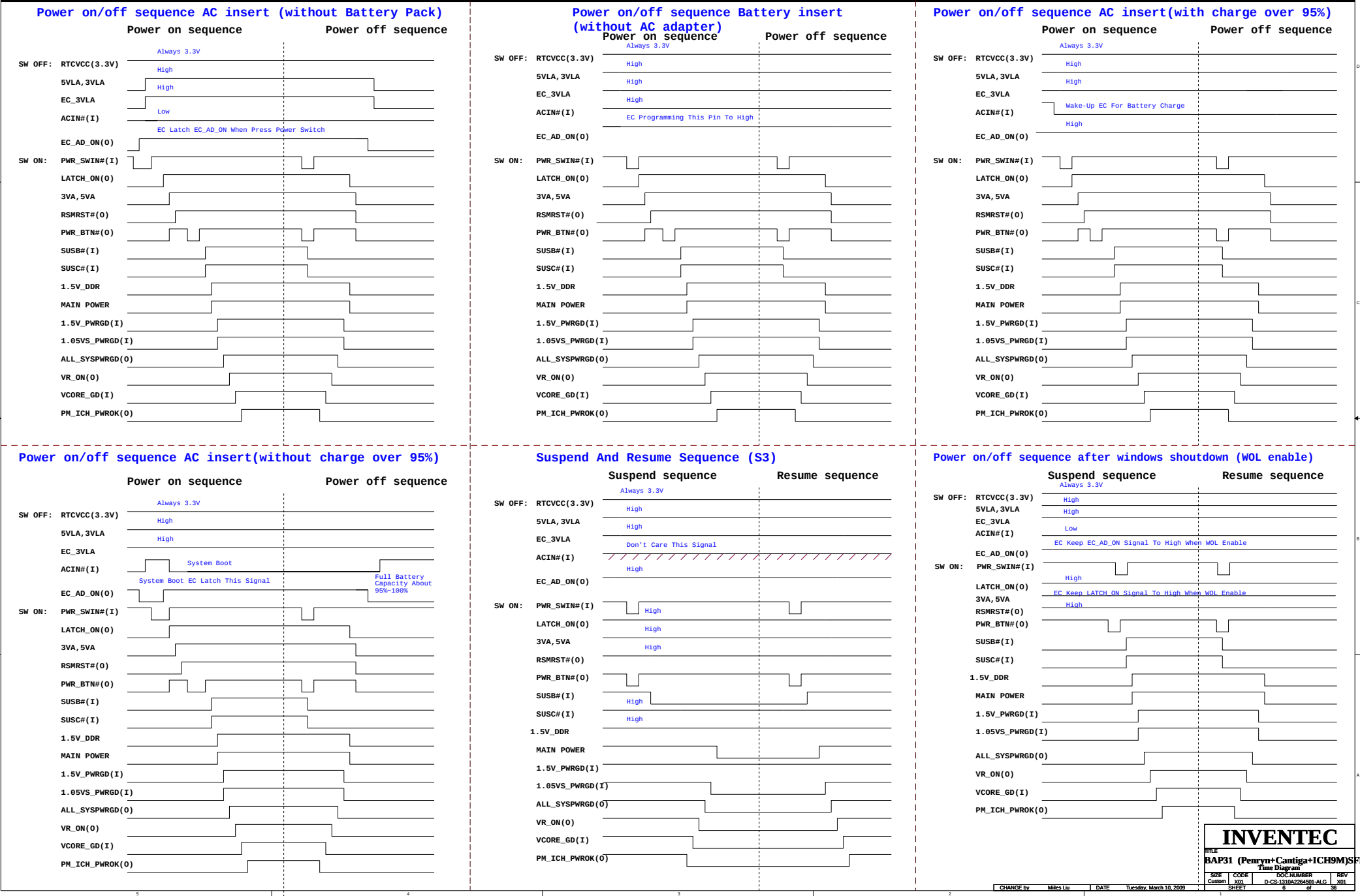
Tuesday, March 10, 2009

1

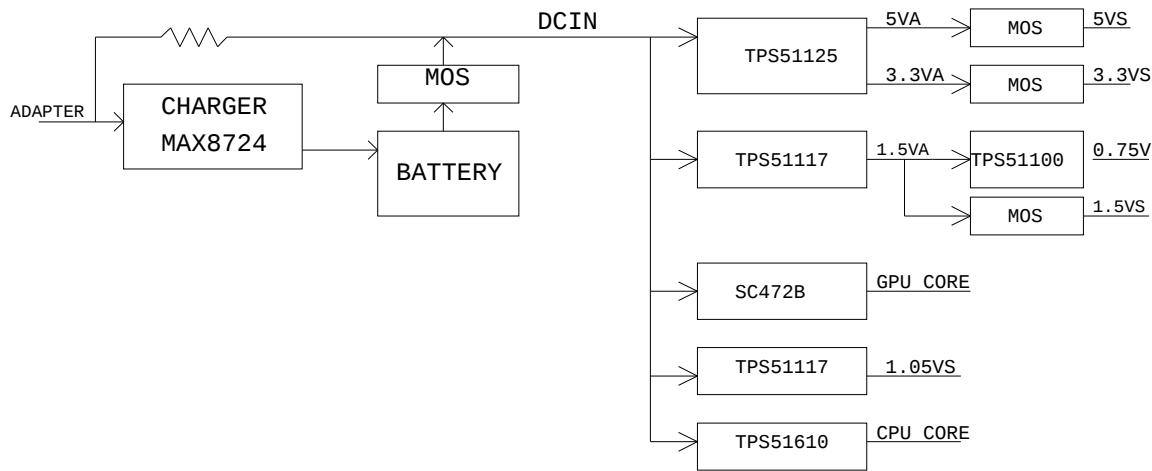
SHEET

SYSTEM POWER ON/OFF SEQUENCE

Drawing : Wendy, Huang



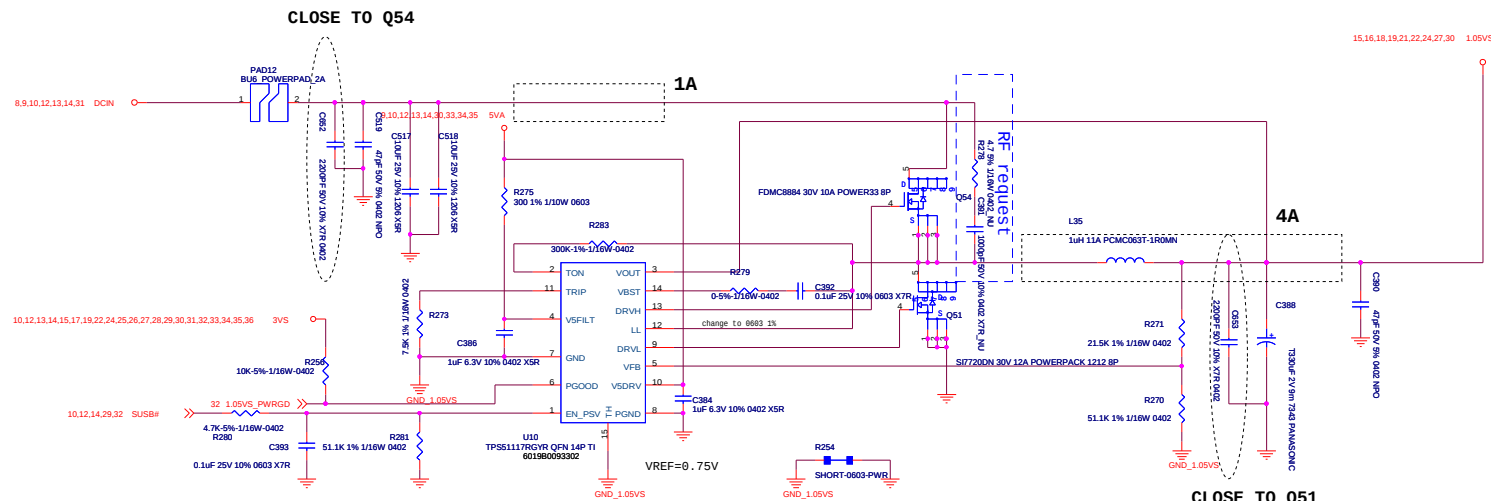
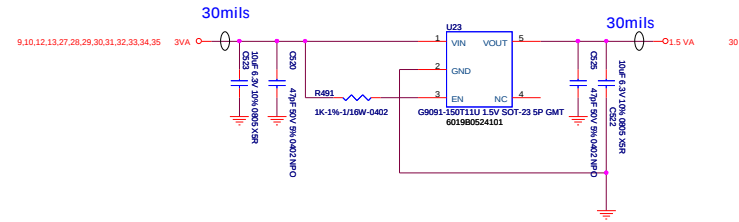
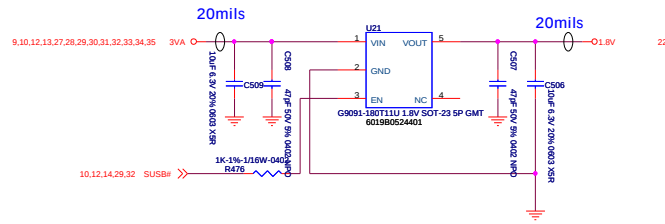
# Power Block Diagram :





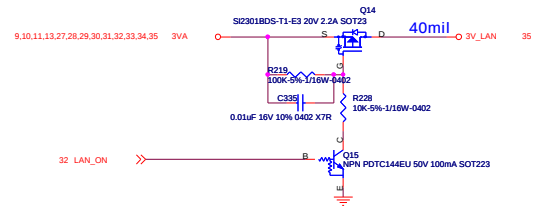
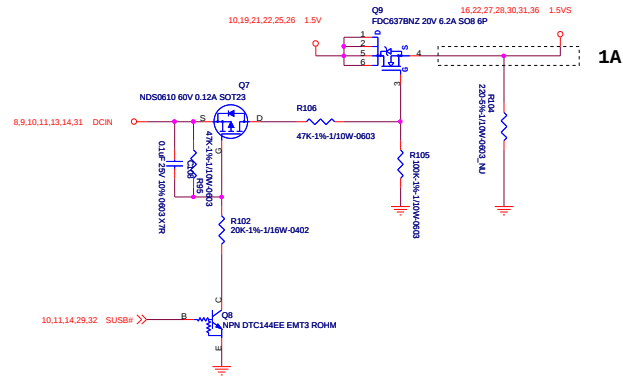






| INVENTEC                       |      |                       |     |
|--------------------------------|------|-----------------------|-----|
| TITLE                          |      |                       |     |
| BAP31 (Penryn+Cantiga+ICH9M)SF |      |                       |     |
| 1.05VS/1.5V/1.8V/1.5VA         |      |                       |     |
| SIZE                           | CODE | DOC NUMBER            | REV |
| Custom                         | X01  | D-CS-1310A2264501-ALG | X01 |

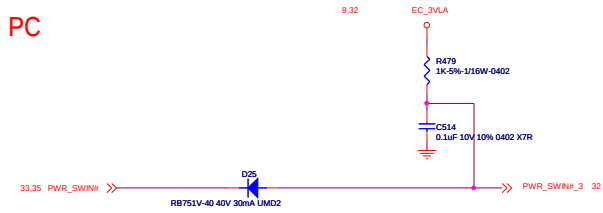
# 1.5VS



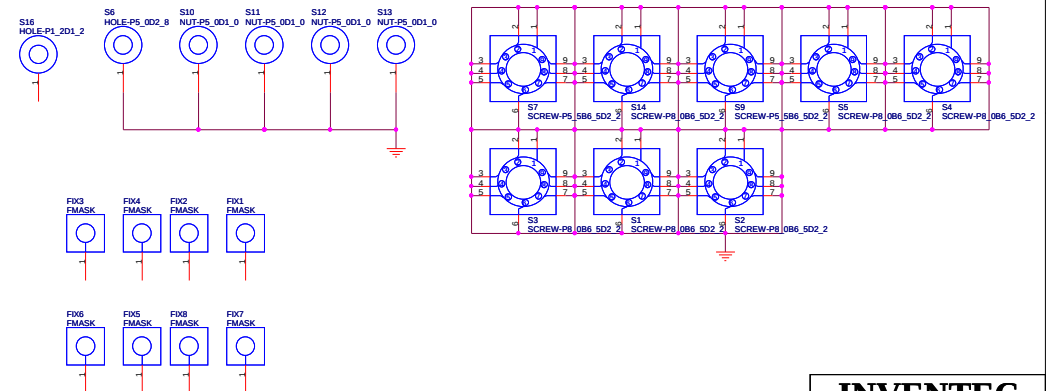
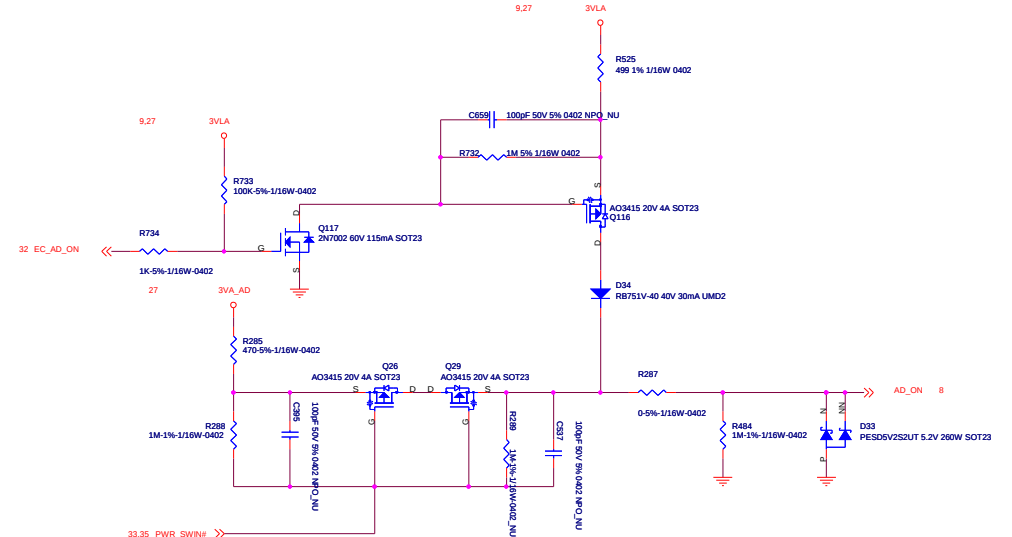
# EMI Cap



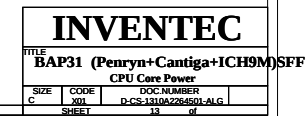
# For Green PC

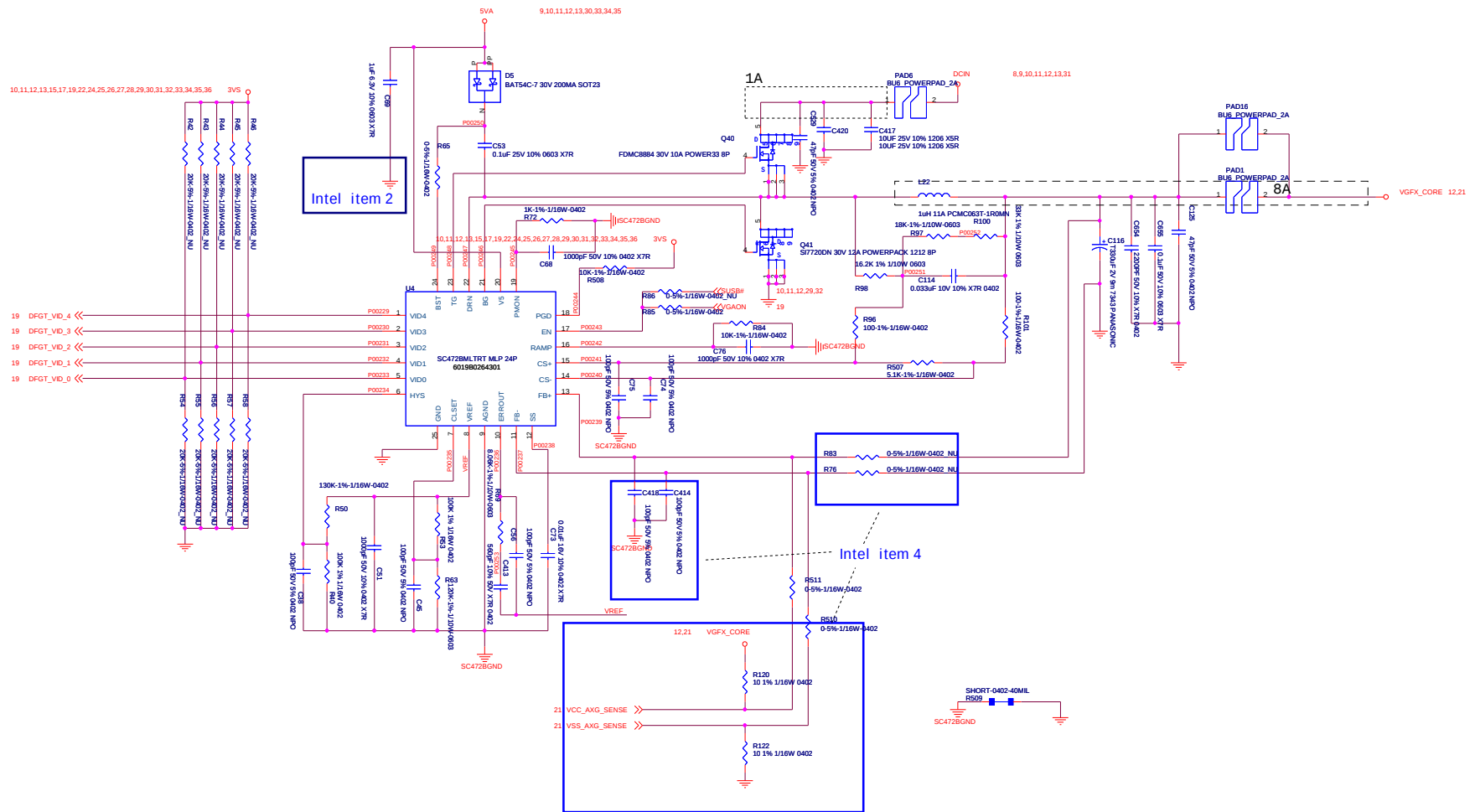


# None Green PC ---- NU



| INVENTEC                      |      |                         |          |
|-------------------------------|------|-------------------------|----------|
| BAP31 (Penryn+Catiga+ICH9M)SF |      |                         |          |
| Power on latch                |      |                         |          |
| SIZE                          | CORE | DOC NUMBER              | REV      |
| Custom                        | X01  | D-CS-1310A224501-ALG    | X01      |
| CHANGE by                     |      | DATE                    | SHEET    |
| Mills Liu                     |      | Tuesday, March 10, 2009 | 12 of 36 |

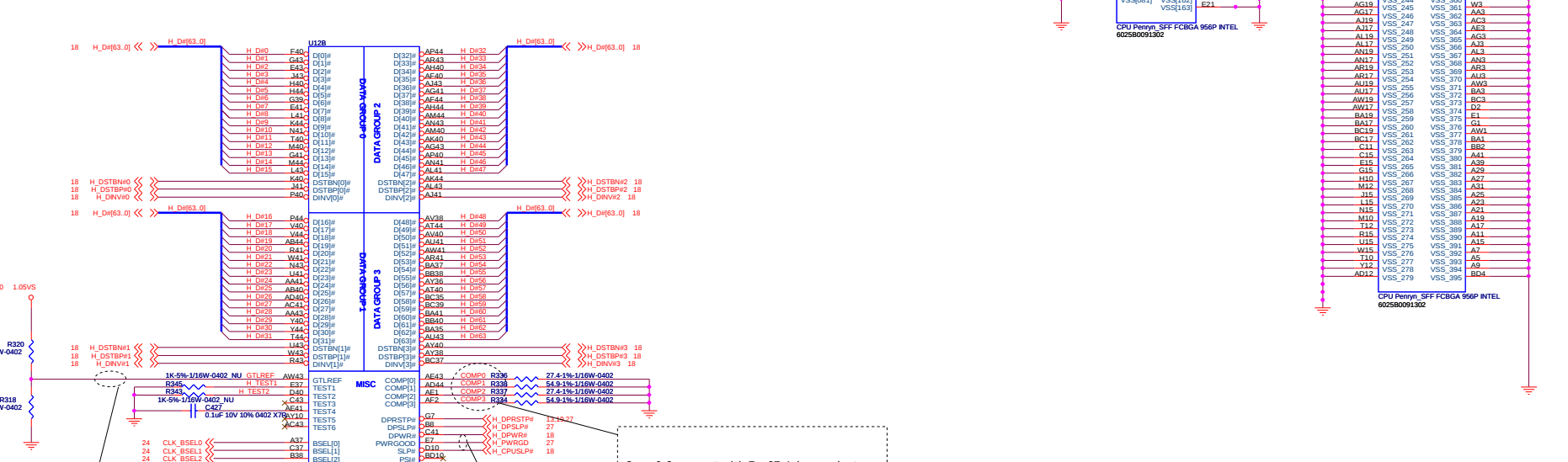






Should be connect to ICH9 and Cantiga without T-ing(no stub)  
XDP P/U & P/D  
XDP DBRESET# R308 1K 5%-1/16W-0402 3V5  
XDP TDO R331 54.9-1%-1/16W-0402 NU 1.05V5  
XDP TMS R311 54.9-1%-1/16W-0402 NU 1.05V5  
XDP BPMMS R321 54.9-1%-1/16W-0402 NU 1.05V5  
XDP TRST# R309 649-1%-1/16W-0402  
XDP TCK R319 54.9-1%-1/16W-0402

Route to TP via and place gnd via w/in 100mils  
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality



Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.  
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils.  
H\_PWRGD rise time : Max : 15ns  
Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.  
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

INVENTEC

BAP31 (Penryn+Catiga+ICH9M)SFF

Penryn Processor(1/2)

SIZE

CODE

X01

DOC NUMBER

D-C-1310A264501.ALG

REV

X01

CHANGE by

Miles Liu

DATE

Tuesday, March 10, 2009

SHEET

1

Place these inside socket cavity on L8  
(North side secondary)

Place these inside socket cavity on  
L8 (South side secondary)

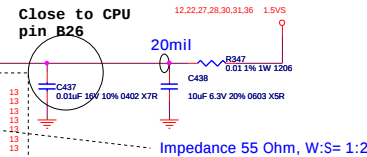
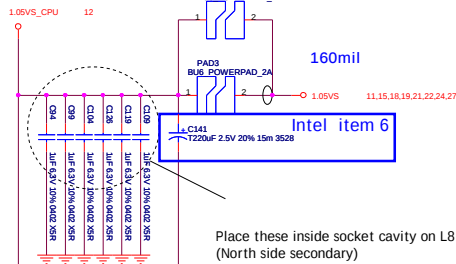
Place these inside socket cavity on L1  
(North side Primary)

Place these inside socket cavity on L1  
(South side Primary)

North side secondary

South side secondary

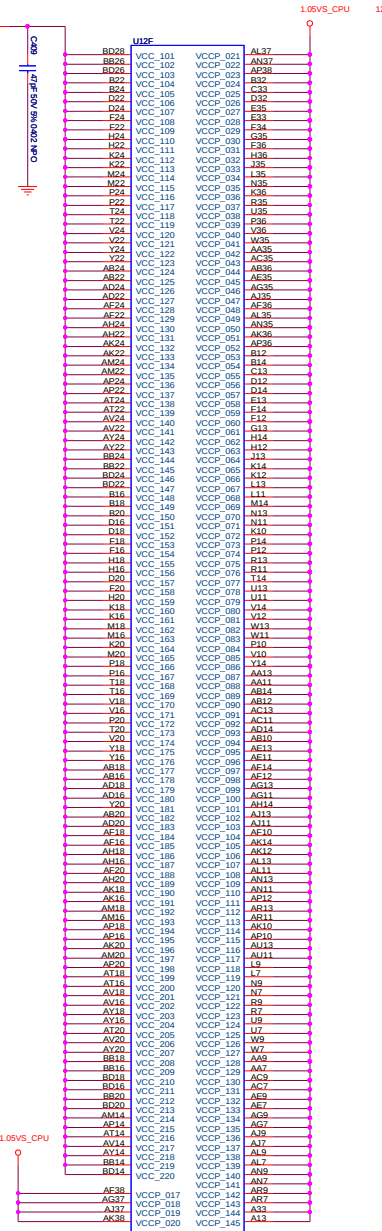
| U12C |          |          |      |
|------|----------|----------|------|
| F32  | VCC[001] | VCC[008] | AB28 |
| F32  | VCC[002] | VCC[009] | AD28 |
| H32  | VCC[010] | VCC[017] | Y26  |
| J33  | VCC[004] | VCC[011] | Y26  |
| L33  | VCC[005] | VCC[012] | AD28 |
| N33  | VCC[007] | VCC[014] | AE28 |
| P32  | VCC[008] | VCC[015] | AD28 |
| R32  | VCC[009] | VCC[016] | AE28 |
| S32  | VCC[010] | VCC[017] | AD28 |
| T32  | VCC[011] | VCC[018] | AE28 |
| V32  | VCC[012] | VCC[019] | AD28 |
| W32  | VCC[013] | VCC[020] | AE28 |
| X32  | VCC[014] | VCC[021] | AD28 |
| Y32  | VCC[015] | VCC[022] | AE28 |
| Z32  | VCC[016] | VCC[023] | AD28 |
| AA32 | VCC[017] | VCC[024] | AE28 |
| AB32 | VCC[018] | VCC[025] | AD28 |
| AC32 | VCC[019] | VCC[026] | AE28 |
| AD32 | VCC[020] | VCC[027] | AD28 |
| AE32 | VCC[021] | VCC[028] | AE28 |
| AF32 | VCC[022] | VCC[029] | AD28 |
| AG32 | VCC[023] | VCC[030] | AE28 |
| AH32 | VCC[024] | VCC[031] | AD28 |
| AI32 | VCC[025] | VCC[032] | AE28 |
| AJ32 | VCC[026] | VCC[033] | AD28 |
| AK32 | VCC[027] | VCC[034] | AE28 |
| AL32 | VCC[028] | VCC[035] | AD28 |
| AM32 | VCC[029] | VCC[036] | AE28 |
| AN32 | VCC[030] | VCC[037] | AD28 |
| AO32 | VCC[031] | VCC[038] | AE28 |
| AP32 | VCC[032] | VCC[039] | AD28 |
| AQ32 | VCC[033] | VCC[040] | AE28 |
| AR32 | VCC[034] | VCC[041] | AD28 |
| AS32 | VCC[035] | VCC[042] | AE28 |
| AT32 | VCC[036] | VCC[043] | AD28 |
| AV32 | VCC[037] | VCC[044] | AE28 |
| AW32 | VCC[038] | VCC[045] | AD28 |
| AX32 | VCC[039] | VCC[046] | AE28 |
| AY32 | VCC[040] | VCC[047] | AD28 |
| AZ32 | VCC[041] | VCC[048] | AE28 |
| BA32 | VCC[042] | VCC[049] | AD28 |
| BB32 | VCC[043] | VCC[050] | AE28 |
| BC32 | VCC[044] | VCC[051] | AD28 |
| BD32 | VCC[045] | VCC[052] | AE28 |
| BE32 | VCC[046] | VCC[053] | AD28 |
| BF32 | VCC[047] | VCC[054] | AE28 |
| BG32 | VCC[048] | VCC[055] | AD28 |
| BH32 | VCC[049] | VCC[056] | AE28 |
| BI32 | VCC[050] | VCC[057] | AD28 |
| BJ32 | VCC[051] | VCC[058] | AE28 |
| BK32 | VCC[052] | VCC[059] | AD28 |
| BL32 | VCC[053] | VCC[060] | AE28 |
| BM32 | VCC[054] | VCC[061] | AD28 |
| BN32 | VCC[055] | VCC[062] | AE28 |
| BO32 | VCC[056] | VCC[063] | AD28 |
| BP32 | VCC[057] | VCC[064] | AE28 |
| BQ32 | VCC[058] | VCC[065] | AD28 |
| BR32 | VCC[059] | VCC[066] | AE28 |
| BS32 | VCC[060] | VCC[067] | AD28 |
| BT32 | VCC[061] | VCC[068] | AE28 |
| BU32 | VCC[062] | VCC[069] | AD28 |
| BV32 | VCC[063] | VCC[070] | AE28 |
| BW32 | VCC[064] | VCC[071] | AD28 |
| BX32 | VCC[065] | VCC[072] | AE28 |
| BY32 | VCC[066] | VCC[073] | AD28 |
| BZ32 | VCC[067] | VCC[074] | AE28 |
| CA32 | VCC[068] | VCC[075] | AD28 |
| CB32 | VCC[069] | VCC[076] | AE28 |
| CC32 | VCC[070] | VCC[077] | AD28 |
| CD32 | VCC[071] | VCC[078] | AE28 |
| CE32 | VCC[072] | VCC[079] | AD28 |
| CF32 | VCC[073] | VCC[080] | AE28 |
| CG32 | VCC[074] | VCC[081] | AD28 |
| CH32 | VCC[075] | VCC[082] | AE28 |
| CI32 | VCC[076] | VCC[083] | AD28 |
| CJ32 | VCC[077] | VCC[084] | AE28 |
| CK32 | VCC[078] | VCC[085] | AD28 |
| CL32 | VCC[079] | VCC[086] | AE28 |
| CM32 | VCC[080] | VCC[087] | AD28 |
| CN32 | VCC[081] | VCC[088] | AE28 |
| CO32 | VCC[082] | VCC[089] | AD28 |
| CP32 | VCC[083] | VCC[090] | AE28 |
| CQ32 | VCC[084] | VCC[091] | AD28 |
| CR32 | VCC[085] | VCC[092] | AE28 |
| CS32 | VCC[086] | VCC[093] | AD28 |
| CT32 | VCC[087] | VCC[094] | AE28 |
| CU32 | VCC[088] | VCC[095] | AD28 |
| CV32 | VCC[089] | VCC[096] | AE28 |
| CW32 | VCC[090] | VCC[097] | AD28 |
| CX32 | VCC[091] | VCC[098] | AE28 |
| CY32 | VCC[092] | VCC[099] | AD28 |
| CZ32 | VCC[093] | VCC[100] | AE28 |



Route VCCSENSE and VSSSENSE traces  
at 27.4 ohms. Place PU and PD within  
2 inch of CPU

Mismatch 25mil

18mil  
7mil space  
25mil space with other

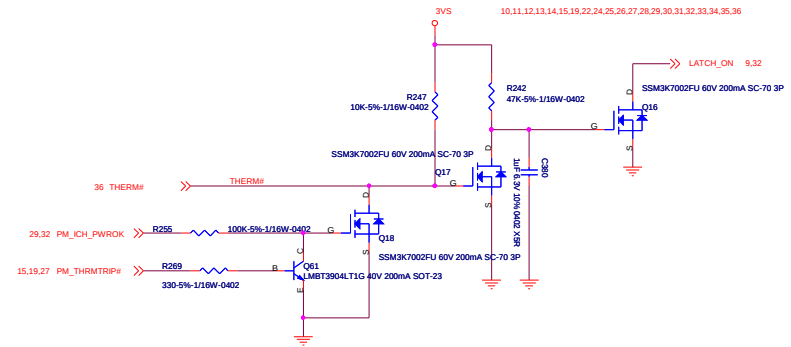
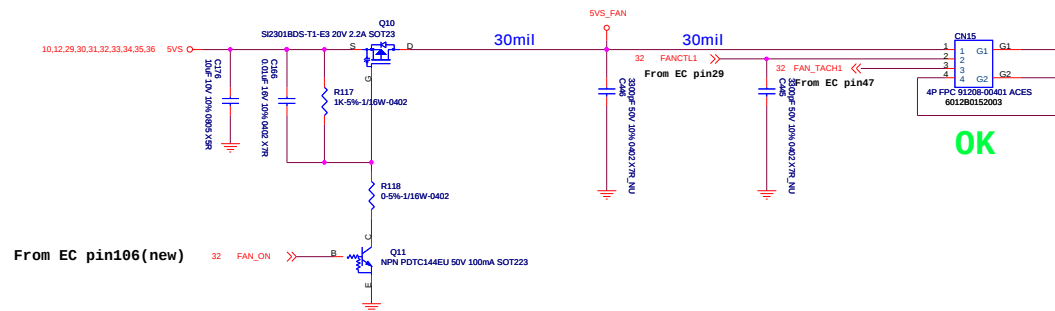


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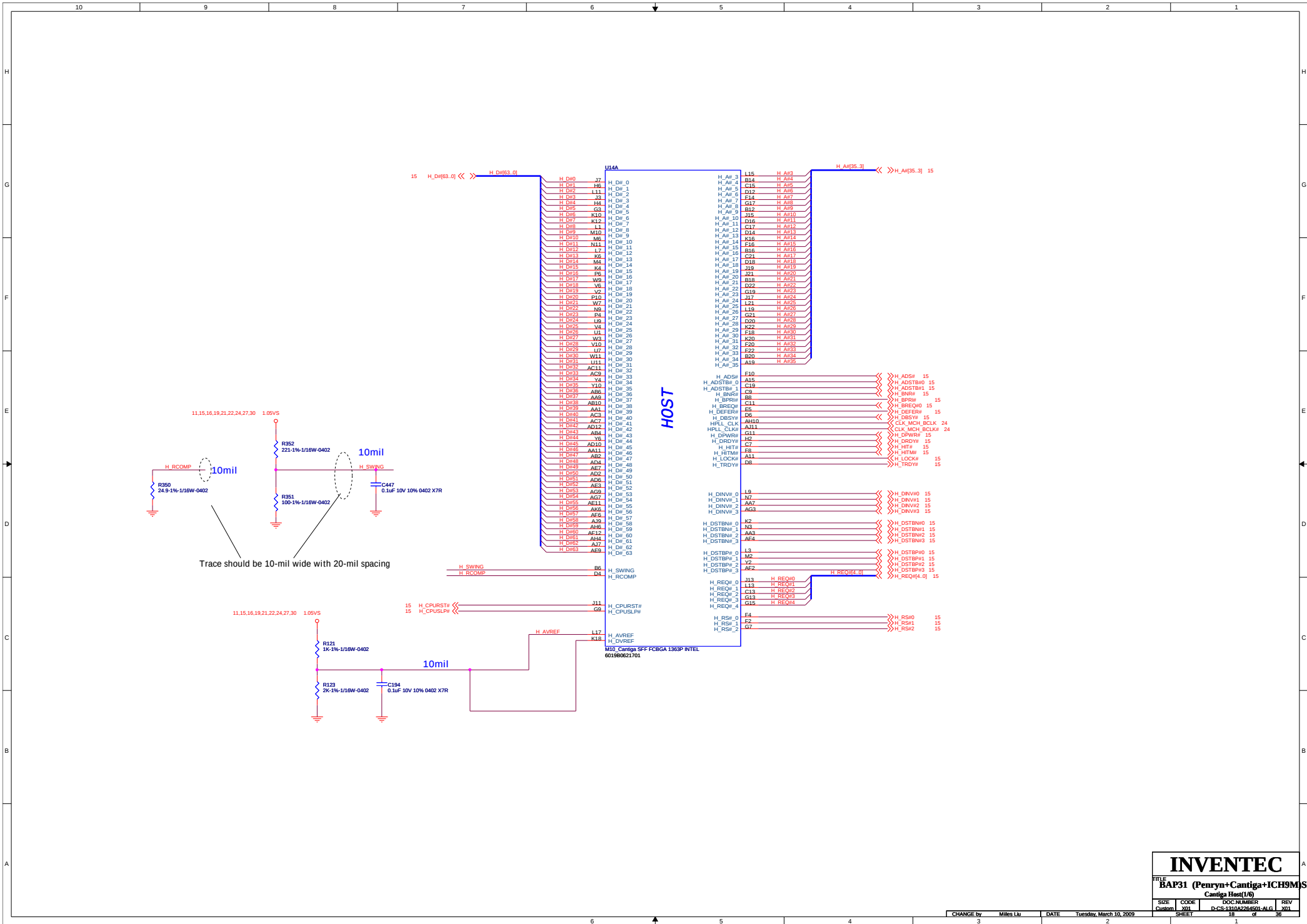
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BAP31 (Penryn+Caniga+ICH9M)SFF  
Penryn Processor(2/2)

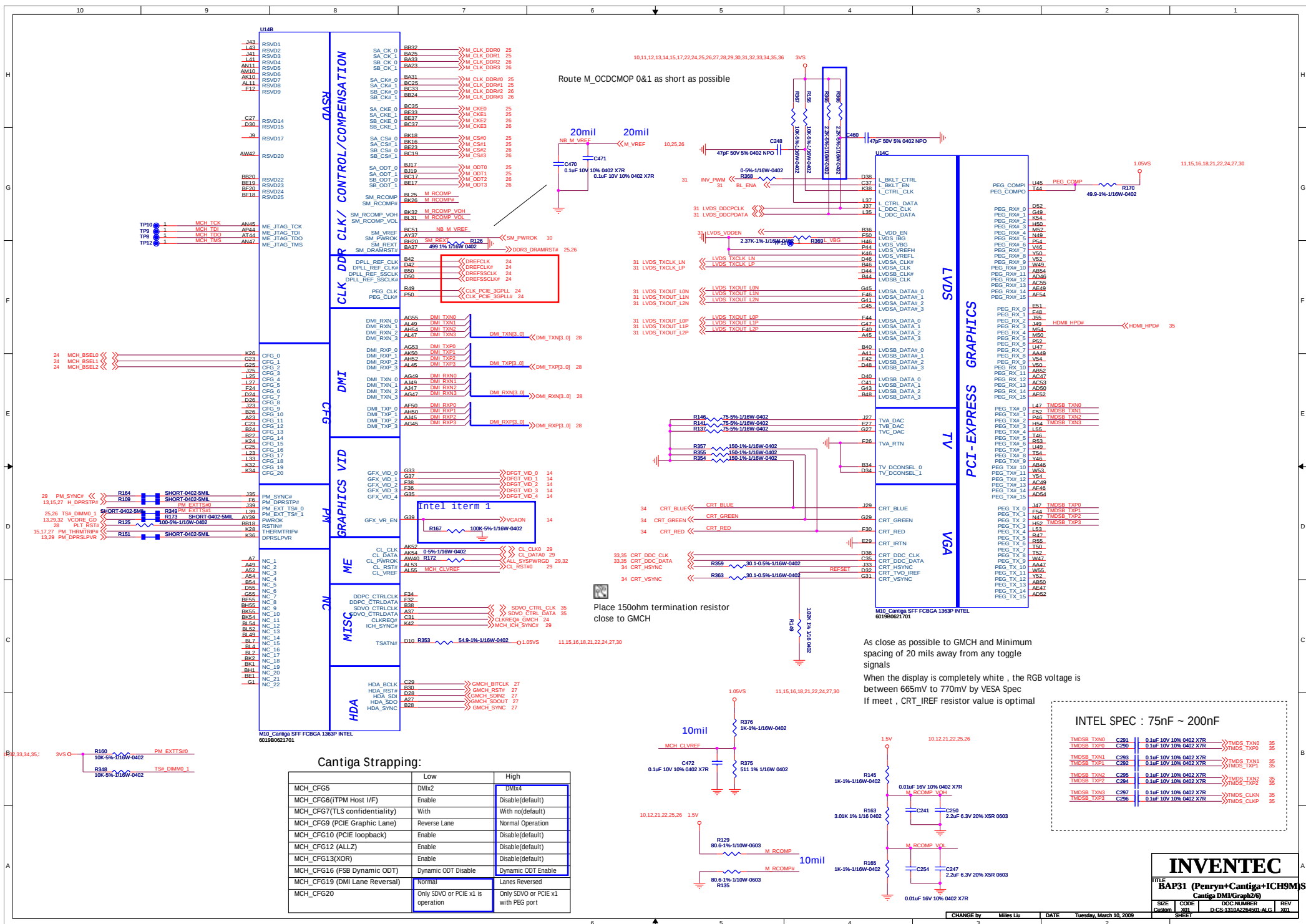
CHANGE by Milen Liu DATE Tuesday, March 10, 2009

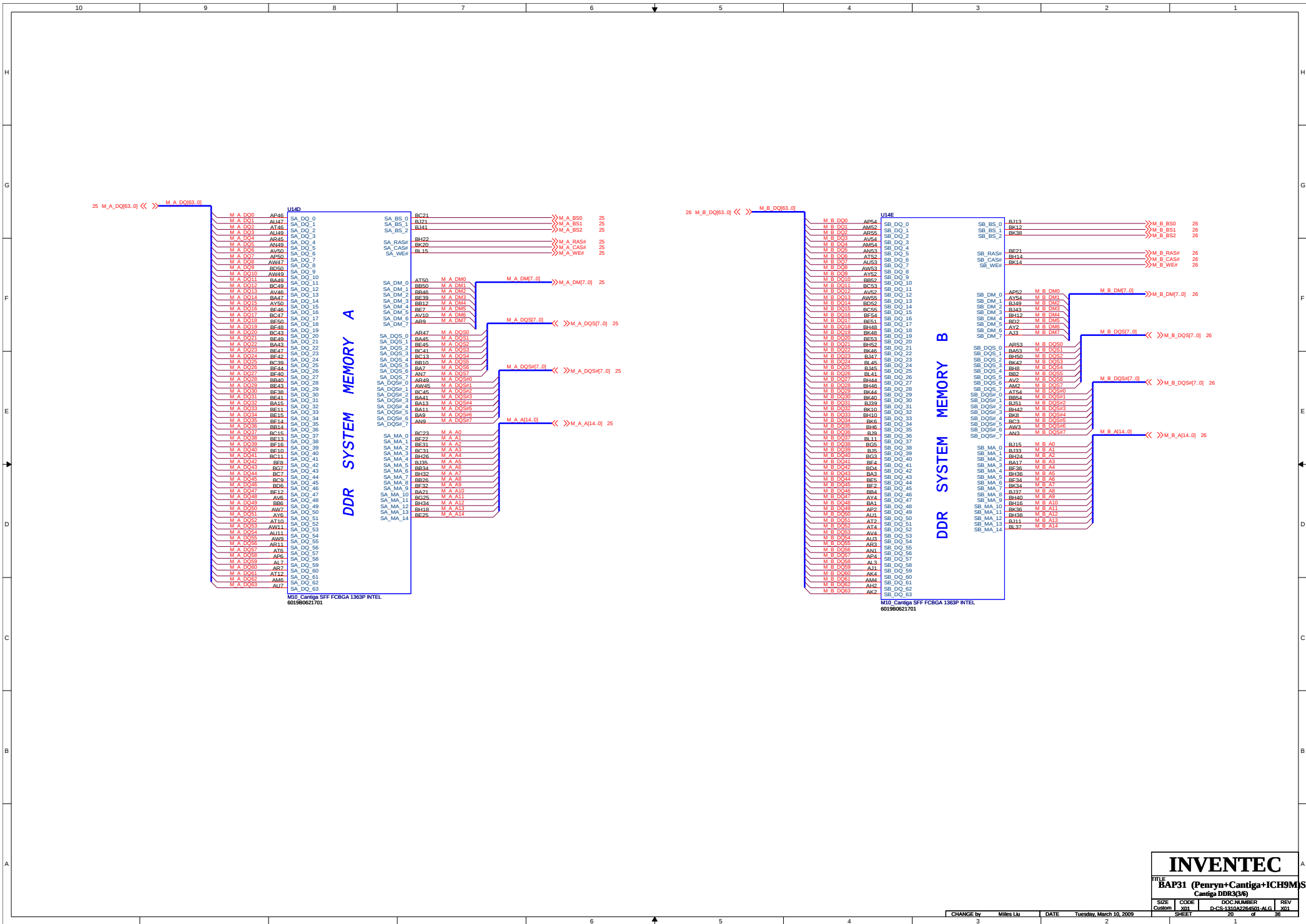
SIZE CODE SHEET 16 of 36

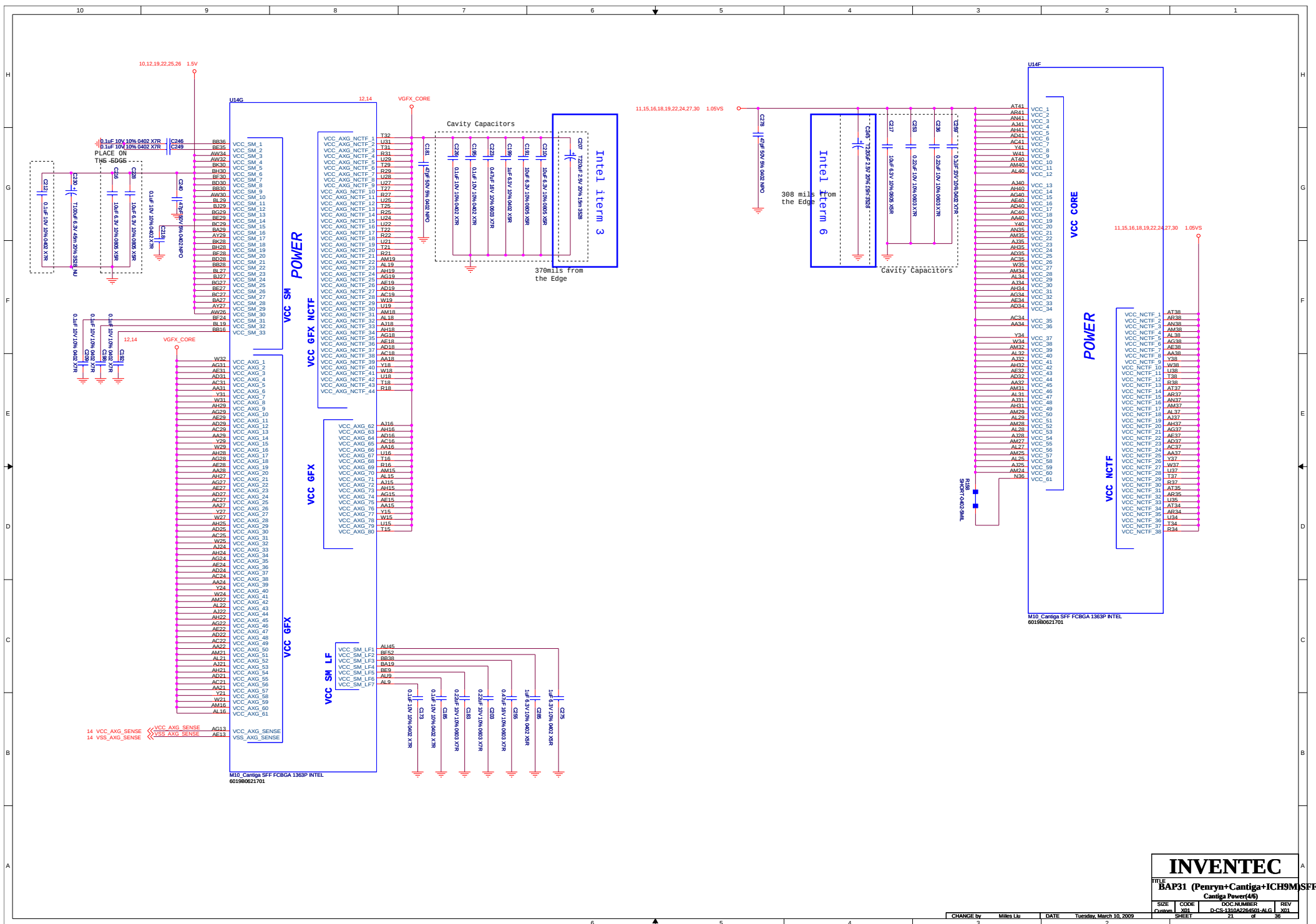
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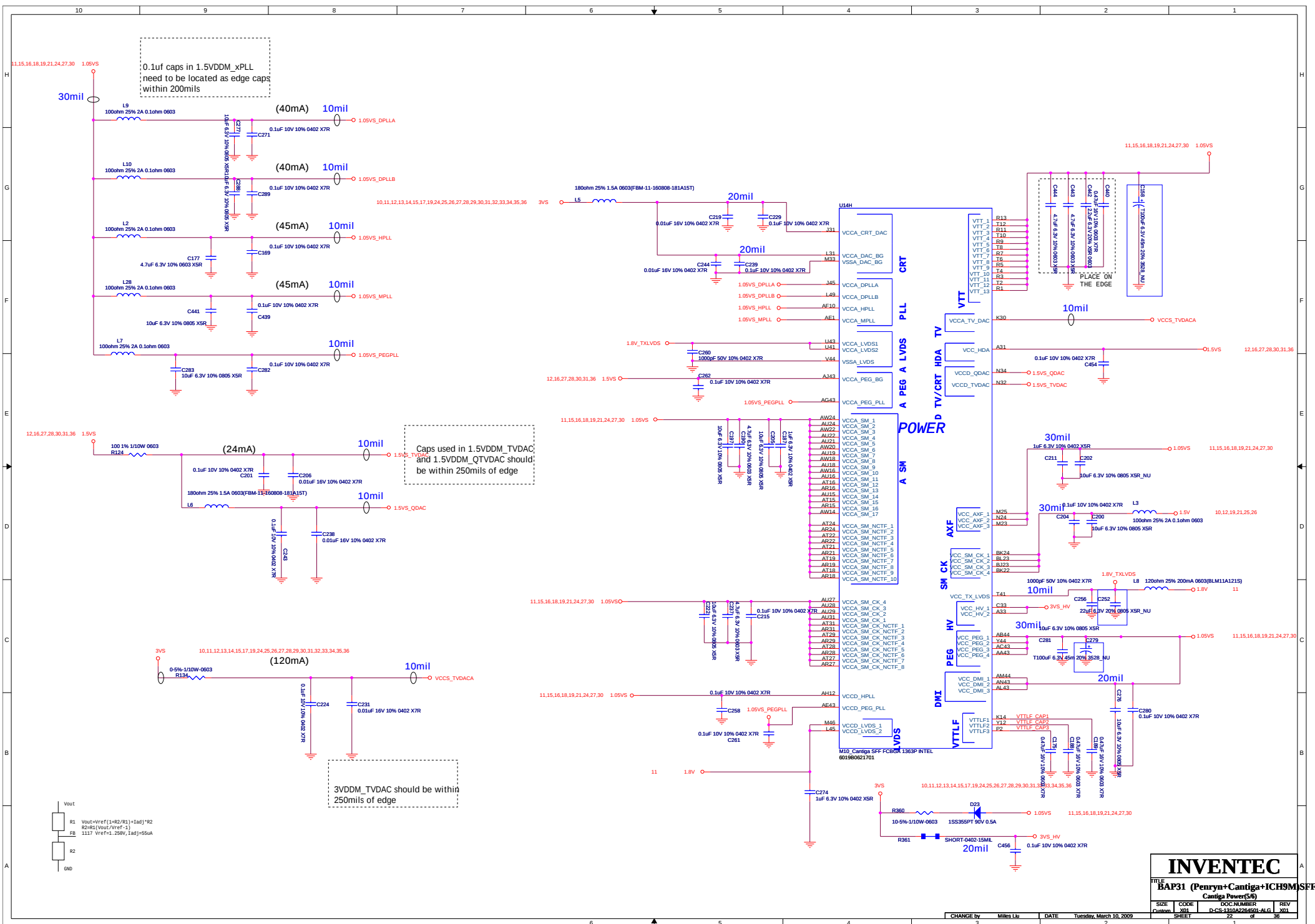
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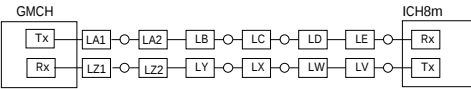
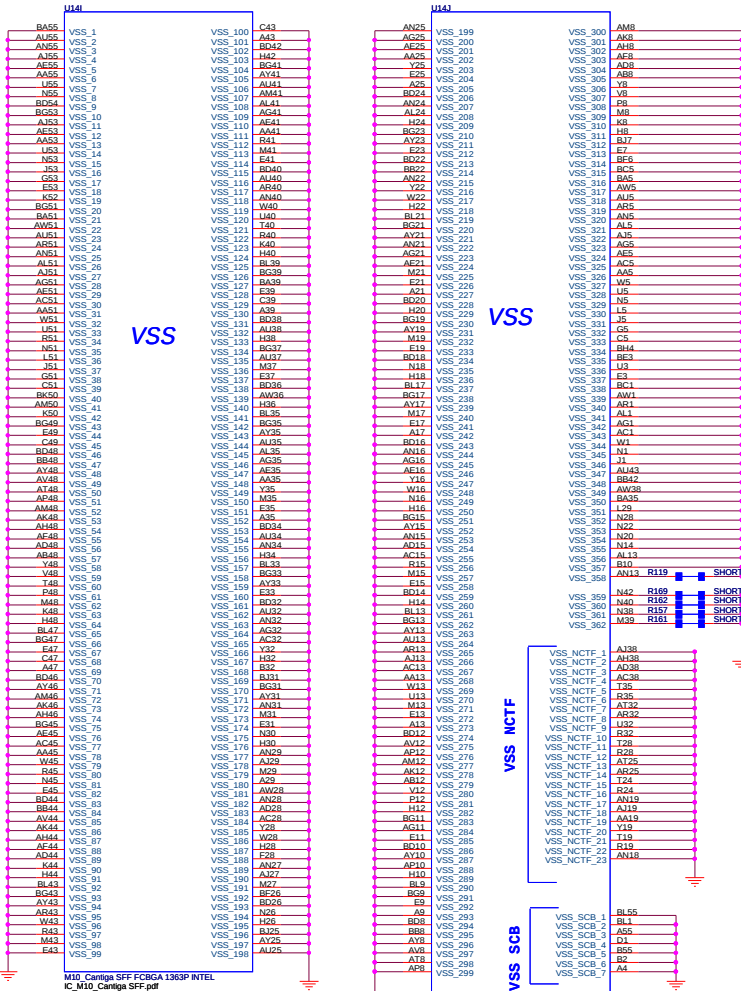






# DMI Routing Guideline

# PCIe Routing Guideline

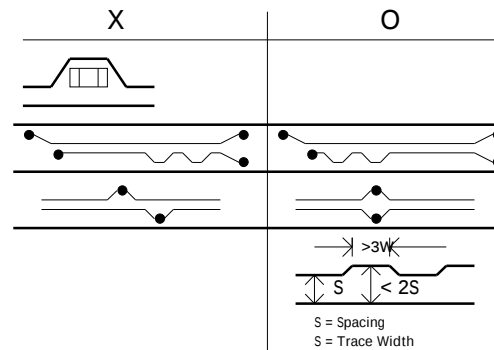


| Breakout/in LA/LZ | Main Route LB/LY            | Breakout/in LE/LV           |
|-------------------|-----------------------------|-----------------------------|
| Microstrip        | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |
| Microstrip        | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |
| Microstrip        | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |
| Stripline         | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |
| Stripline         | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |
| Stripline         | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |
| Stripline         | Same Routing layer as LA/LZ | Same Routing layer as LE/LV |

| Parameter                                | Main Route Guideline                                  | Breakout Guideline                                    |
|------------------------------------------|-------------------------------------------------------|-------------------------------------------------------|
| Uncoupled Single End Impedance           | 55 +/- 15%                                            | 55 +/- 15%                                            |
| Nominal Trace Width                      | Inner Layer : 4 mils<br>Outer Layer : 5 mils          | Inner Layer : 4 mils<br>Outer Layer : 5 mils          |
| Nominal Diferential Pair-Pitch           | Inner Layer : 7 mils<br>Outer Layer : 7 mils          | Inner Layer : 4 mils<br>Outer Layer : 5 mils          |
| Pair-to-Pair Pitch                       | Inner Layer : 37 mils<br>Outer Layer : 37 mils        | Inner Layer : 27 mils<br>Outer Layer : 27 mils        |
| Bus-to-Bus Pitch                         | Inner Layer : 22 mils<br>Outer Layer : 20 mils        | Inner Layer : 15 mils<br>Outer Layer : 12 mils        |
| Reference Plane                          | Ground                                                | Ground                                                |
| Splits/Voids                             | No routing over plane splits<br>No routing over voids | No routing over plane splits<br>No routing over voids |
| Trace Length-LA (GMCH Breakout)          | Max = 250 mils                                        |                                                       |
| Trace Length-LB (GMCH Breakout to Via2)  | Max = 3600 mils                                       |                                                       |
| Trace Length-LC (Via2 to Via3)           | Max = 5900 mils                                       |                                                       |
| Trace Length-LD (Via3 to ICH7m Breakout) | Max = 3600 mils                                       |                                                       |
| Trace Length-LE (ICH7m Breakout)         | Max = 400 mils                                        |                                                       |
| Trace Length-L1 (LA+LB+LC+LD+LE)         | Max = 8000 mils                                       |                                                       |
| Trace Length-LY (ICH7m Breakout)         | Max = 400 mils                                        |                                                       |
| Trace Length-LW (ICH7m Breakout to Via2) | Max = 3600 mils                                       |                                                       |
| Trace Length-LX (Via2 to Via3)           | Max = 5900 mils                                       |                                                       |
| Trace Length-LZ (Via3 to GMCH Breakout)  | Max = 3600 mils                                       |                                                       |
| Trace Length-LZ (GMCH Breakout)          | Max = 400 mils                                        |                                                       |
| Trace Length-L2 (LV+LW+LX+LY+LZ)         | Max = 8000 mils                                       |                                                       |

\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane

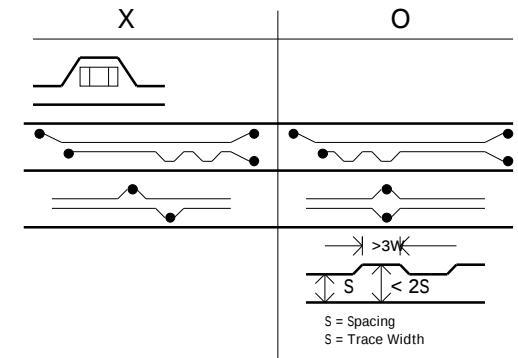
\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



| Breakout/in<br>LA/LZ                        | Main Route<br>LB/LC/LY                                | Main Route<br>LD/LW                            | Breakout/in<br>LE/LV |
|---------------------------------------------|-------------------------------------------------------|------------------------------------------------|----------------------|
| Stripline                                   | Microstrip                                            | Same Routing layer as LE/LV                    | Microstrip           |
|                                             |                                                       |                                                |                      |
| Parameter                                   | Main Route Guideline                                  | Breakout Guideline                             |                      |
| Uncoupled Single End Impedance              | 55 +/- 15%                                            | 55 +/- 15%                                     |                      |
| Nominal Trace Width                         | Inner Layer : 4 mils<br>Outer Layer : 5 mils          |                                                |                      |
| Nominal Differential Trace Space            | Inner Layer : 7 mils<br>Outer Layer : 7 mils          | Inner Layer : 4 mils<br>Outer Layer : 5 mils   |                      |
| Pair-to-Pair Pitch                          | Inner Layer : 37 mils<br>Outer Layer : 37 mils        | Inner Layer : 27 mils<br>Outer Layer : 27 mils |                      |
| Bus-to-Bus Pitch                            | Inner Layer : 20 mils<br>Outer Layer : 20 mils        | Inner Layer : 15 mils<br>Outer Layer : 12 mils |                      |
| Reference Plane                             | Ground                                                | Ground                                         |                      |
| Splits/Voids                                | No routing over plane splits<br>No routing over voids |                                                |                      |
| Trace Length-LA (ICH7m Breakout)            | Max = 400 mils                                        |                                                |                      |
| Trace Length-LB (ICH7m Breakout to AC cap)  | Max = 10750 mils                                      |                                                |                      |
| Trace Length-LC (AC cap to PCIe CN)         | Max = 10750 mils                                      |                                                |                      |
| Trace Length-L1 (LA+LB+LC)                  | Max = 12000 mils                                      |                                                |                      |
|                                             |                                                       |                                                |                      |
| Trace Length-LY (PCIe CN to ICH7m Breakout) | Max = 11950 mils                                      |                                                |                      |
| Trace Length-LZ (ICH7m Breakout)            | Max = 400 mils                                        |                                                |                      |
| Trace Length-L2 (LY+LZ)                     | Max = 12000 mils                                      |                                                |                      |

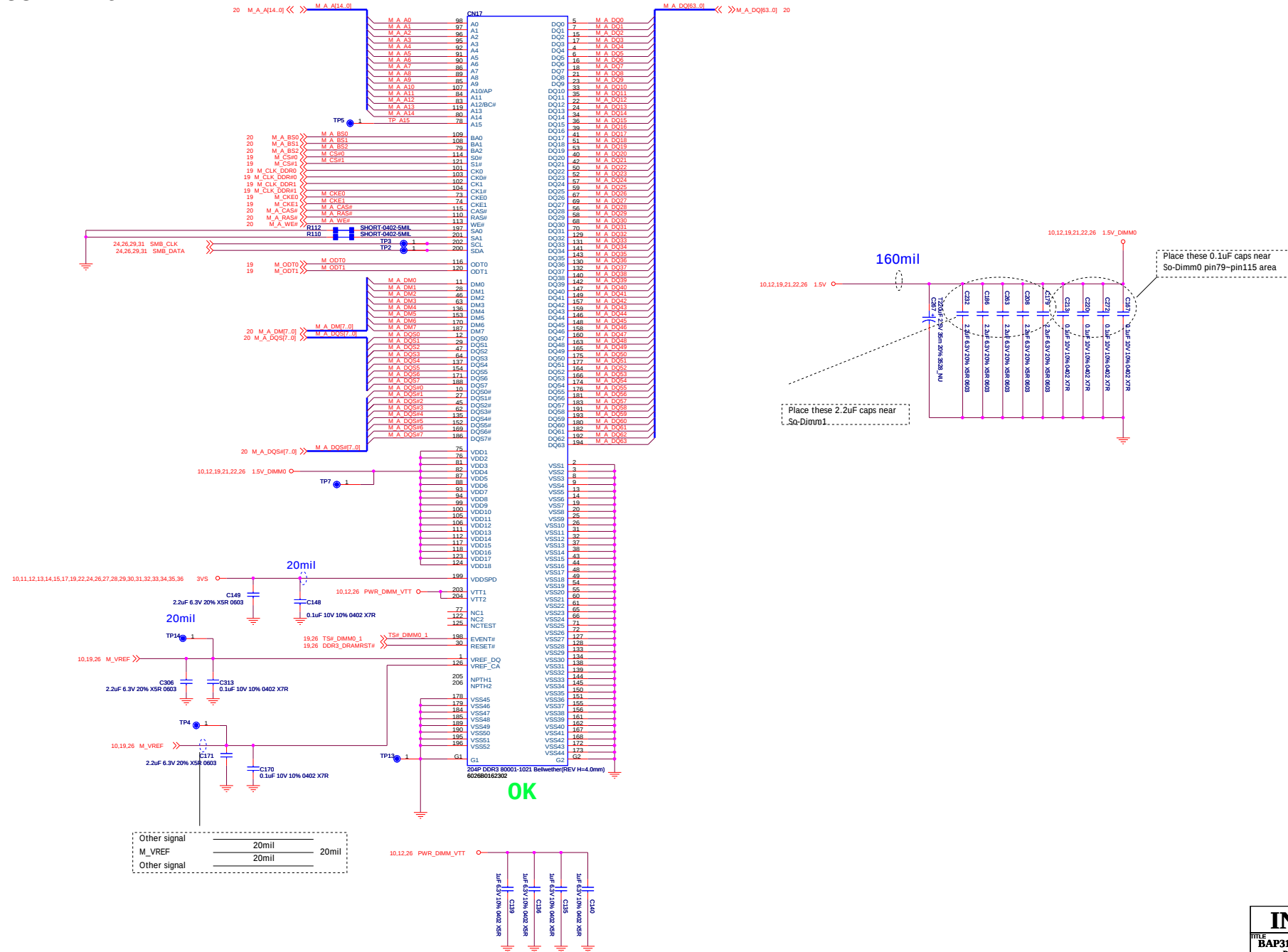
\*\*\* When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane

\*\*\* Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils





# SO-DIMM0



**INVENTEC**

|                                          |             |                                    |            |
|------------------------------------------|-------------|------------------------------------|------------|
| TITLE<br>BAP31 (Penryn+Cantiga+ICH9M)SFF |             |                                    |            |
| DDR3 SDRAM SO-DIMM0                      |             |                                    |            |
| SIZE<br>Custom                           | CODE<br>X01 | DOC NUMBER<br>D-CS-1310A264501.ALG | REV<br>X01 |
| SHEET                                    |             |                                    |            |

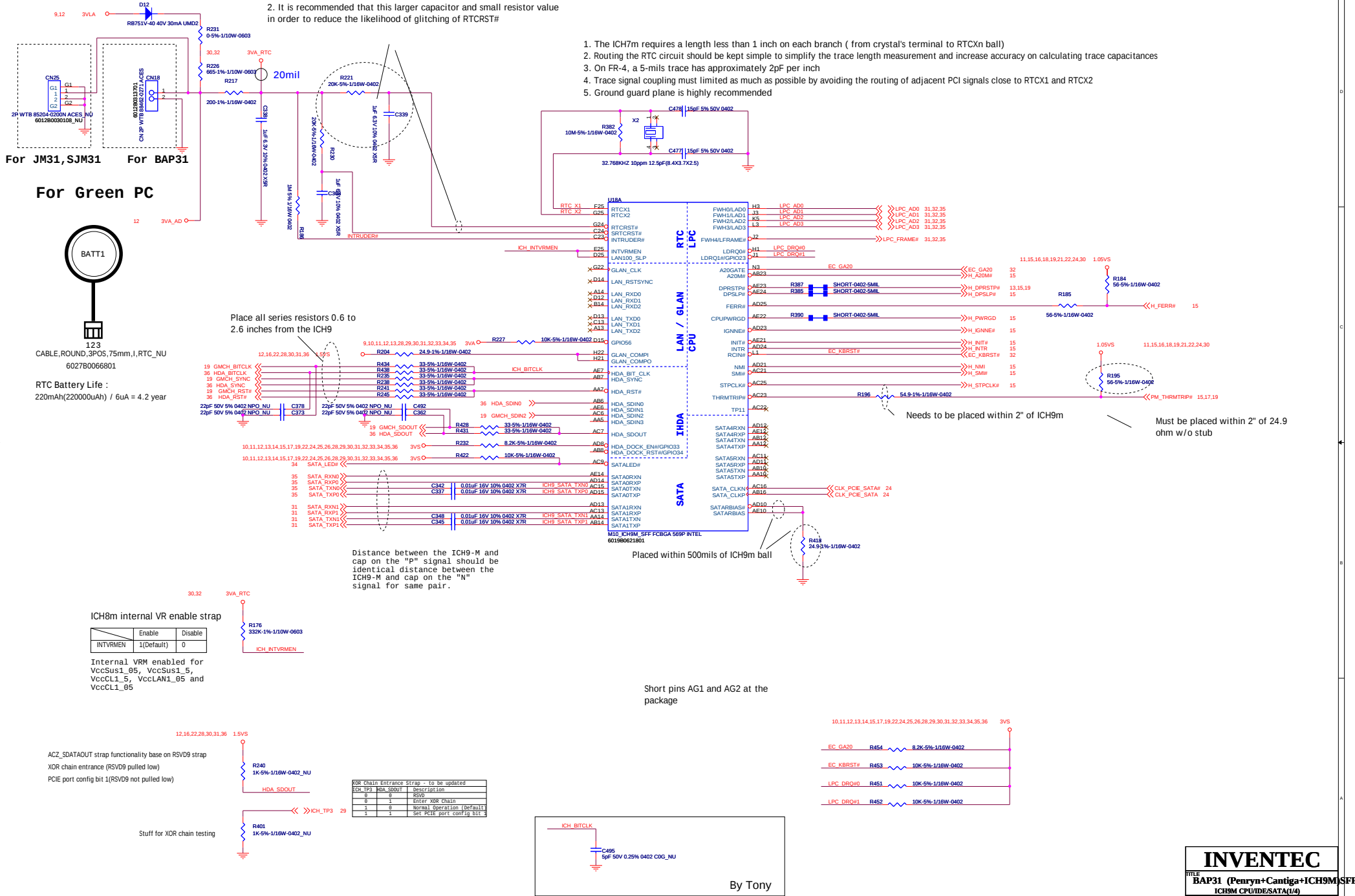
The diagram illustrates the PCB layout for the SO-DIMM1 module. It includes the following components and features:

- Memory Module:** A 2048 DDR3 800MHz 1021-1021 Belwaether (STD H=4.0mm) 6026B0164601 module is shown with its pin connections to the PCB.
- Power and Ground Connections:**
  - 3V5:** Connected to pins 20, 24, 25, 29, 31, 32, 33, 34, 35, 36.
  - 1.5V\_DIMM1:** Connected to pins 10, 12, 19, 21, 22, 25.
  - 10.12.25 PWR\_DIMM\_VTT:** Connected to pins 10, 12, 25.
  - 10.12.25 M\_VREF:** Connected to pins 10, 12, 25.
  - 10.12.25 PWR\_DIMM\_VTT:** Connected to pins 10, 12, 25.
- Test Points:**
  - TP6:** Located near the memory module.
  - TP7:** Located near the memory module.
  - TP8:** Located near the memory module.
  - TP9:** Located near the memory module.
  - TP10:** Located near the memory module.
  - TP11:** Located near the memory module.
  - TP12:** Located near the memory module.
  - TP13:** Located near the memory module.
  - TP14:** Located near the memory module.
  - TP15:** Located near the memory module.
  - TP16:** Located near the memory module.
  - TP17:** Located near the memory module.
  - TP18:** Located near the memory module.
  - TP19:** Located near the memory module.
  - TP20:** Located near the memory module.
  - TP21:** Located near the memory module.
  - TP22:** Located near the memory module.
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  - TP24:** Located near the memory module.
  - TP25:** Located near the memory module.
  - TP26:** Located near the memory module.
  - TP27:** Located near the memory module.
  - TP28:** Located near the memory module.
  - TP29:** Located near the memory module.
  - TP30:** Located near the memory module.
  - TP31:** Located near the memory module.
  - TP32:** Located near the memory module.
  - TP33:** Located near the memory module.
  - TP34:** Located near the memory module.
  - TP35:** Located near the memory module.
  - TP36:** Located near the memory module.
  - TP37:** Located near the memory module.
  - TP38:** Located near the memory module.
  - TP39:** Located near the memory module.
  - TP40:** Located near the memory module.
  - TP41:** Located near the memory module.
  - TP42:** Located near the memory module.
  - TP43:** Located near the memory module.
  - TP44:** Located near the memory module.
  - TP45:** Located near the memory module.
  - TP46:** Located near the memory module.
  - TP47:** Located near the memory module.
  - TP48:** Located near the memory module.
  - TP49:** Located near the memory module.
  - TP50:** Located near the memory module.
  - TP51:** Located near the memory module.
  - TP52:** Located near the memory module.
  - TP53:** Located near the memory module.
  - TP54:** Located near the memory module.
  - TP55:** Located near the memory module.
  - TP56:** Located near the memory module.
  - TP57:** Located near the memory module.
  - TP58:** Located near the memory module.
  - TP59:** Located near the memory module.
  - TP60:** Located near the memory module.
  - TP61:** Located near the memory module.
  - TP62:** Located near the memory module.
  - TP63:** Located near the memory module.
  - TP64:** Located near the memory module.
  - TP65:** Located near the memory module.
  - TP66:** Located near the memory module.
  - TP67:** Located near the memory module.
  - TP68:** Located near the memory module.
  - TP69:** Located near the memory module.
  - TP70:** Located near the memory module.
  - TP71:** Located near the memory module.
  - TP72:** Located near the memory module.
  - TP73:** Located near the memory module.
  - TP74:** Located near the memory module.
  - TP75:** Located near the memory module.
  - TP76:** Located near the memory module.
  - TP77:** Located near the memory module.
  - TP78:** Located near the memory module.
  - TP79:** Located near the memory module.
  - TP80:** Located near the memory module.
  - TP81:** Located near the memory module.
  - TP82:** Located near the memory module.
  - TP83:** Located near the memory module.
  - TP84:** Located near the memory module.
  - TP85:** Located near the memory module.
  - TP86:** Located near the memory module.
  - TP87:** Located near the memory module.
  - TP88:** Located near the memory module.
  - TP89:** Located near the memory module.
  - TP90:** Located near the memory module.
  - TP91:** Located near the memory module.
  - TP92:** Located near the memory module.
  - TP93:** Located near the memory module.
  - TP94:** Located near the memory module.
  - TP95:** Located near the memory module.
  - TP96:** Located near the memory module.
  - TP97:** Located near the memory module.
  - TP98:** Located near the memory module.
  - TP99:** Located near the memory module.
  - TP100:** Located near the memory module.
- Other Components:**
  - C151:** 2.2uF 6.3V 20% XSR 0803
  - C146:** 0.1uF 10V 10% 0402 X7R
  - C172:** 2.2uF 6.3V 20% XSR 0803
  - C174:** 0.1uF 10V 10% 0402 X7R
  - C307:** 2.2uF 6.3V 20% XSR 0803
  - C314:** 0.1uF 10V 10% 0402 X7R
  - C317:** 0.1uF 10V 10% 0402 X7R
  - C318:** 0.1uF 10V 10% 0402 X7R
  - C319:** 0.1uF 10V 10% 0402 X7R
  - C320:** 0.1uF 10V 10% 0402 X7R
  - C321:** 0.1uF 10V 10% 0402 X7R
  - C322:** 0.1uF 10V 10% 0402 X7R
  - C323:** 0.1uF 10V 10% 0402 X7R
  - C324:** 0.1uF 10V 10% 0402 X7R
  - C325:** 0.1uF 10V 10% 0402 X7R
  - C326:** 0.1uF 10V 10% 0402 X7R
  - C327:** 0.1uF 10V 10% 0402 X7R
  - C328:** 0.1uF 10V 10% 0402 X7R
  - C329:** 0.1uF 10V 10% 0402 X7R
  - C330:** 0.1uF 10V 10% 0402 X7R
  - C331:** 0.1uF 10V 10% 0402 X7R
  - C332:** 0.1uF 10V 10% 0402 X7R
  - C333:** 0.1uF 10V 10% 0402 X7R
  - C334:** 0.1uF 10V 10% 0402 X7R
  - C335:** 0.1uF 10V 10% 0402 X7R
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  - C338:** 0.1uF 10V 10% 0402 X7R
  - C339:** 0.1uF 10V 10% 0402 X7R
  - C340:** 0.1uF 10V 10% 0402 X7R
  - C341:** 0.1uF 10V 10% 0402 X7R
  - C342:** 0.1uF 10V 10% 0402 X7R
  - C343:** 0.1uF 10V 10% 0402 X7R
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  - C345:** 0.1uF 10V 10% 0402 X7R
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  - C351:** 0.1uF 10V 10% 0402 X7R
  - C352:** 0.1uF 10V 10% 0402 X7R
  - C353:** 0.1uF 10V 10% 0402 X7R
  - C354:** 0.1uF 10V 10% 0402 X7R
  - C355:** 0.1uF 10V 10% 0402 X7R
  - C356:** 0.1uF 10V 10% 0402 X7R
  - C357:** 0.1uF 10V 10% 0402 X7R
  - C358:** 0.1uF 10V 10% 0402 X7R
  - C359:** 0.1uF 10V 10% 0402 X7R
  - C360:** 0.1uF 10V 10% 0402 X7R
  - C361:** 0.1uF 10V 10% 0402 X7R
  - C362:** 0.1uF 10V 10% 0402 X7R
  - C363:** 0.1uF 10V 10%

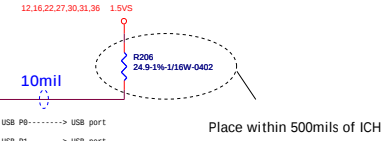
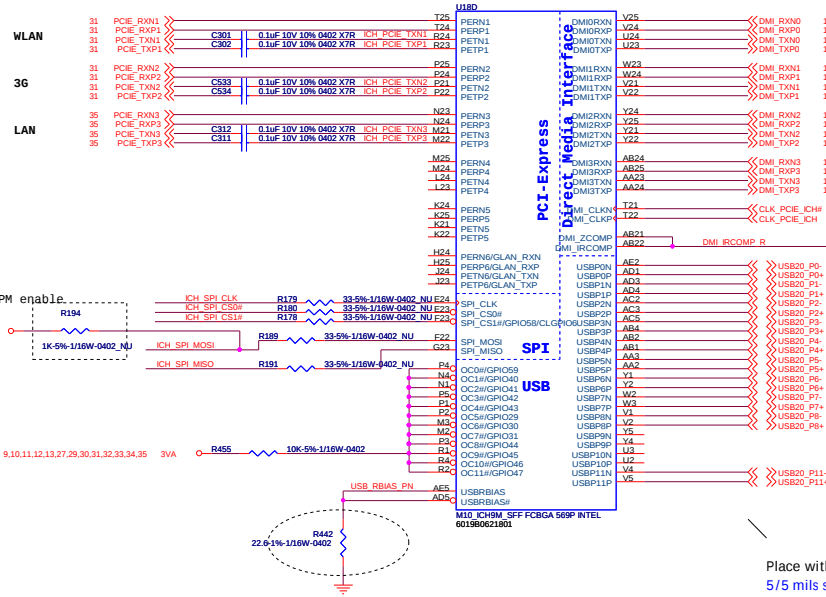
# RTC Circuit

1. RC delay time should be in the range of 18-25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch ( from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended

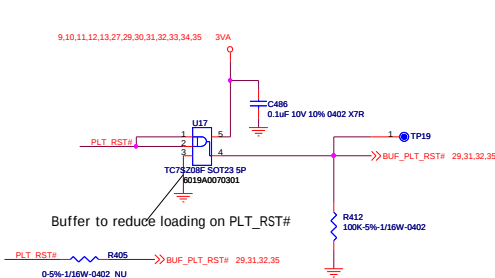
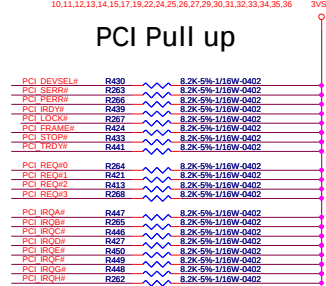
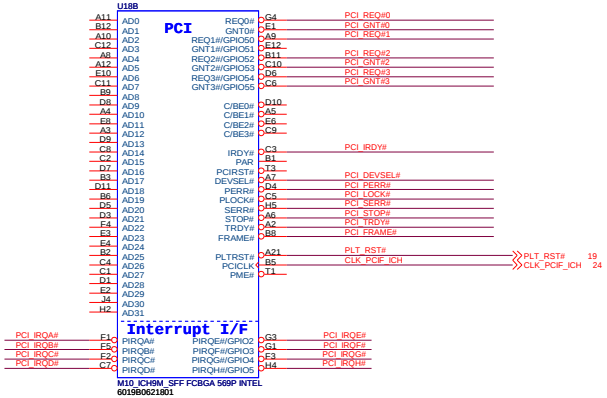


PCIe AC coupling caps need to be within 250mils of the driver



Place within 500mils of ICH

Place within 500mils of ICH  
5/5 mils spacing on microstrip

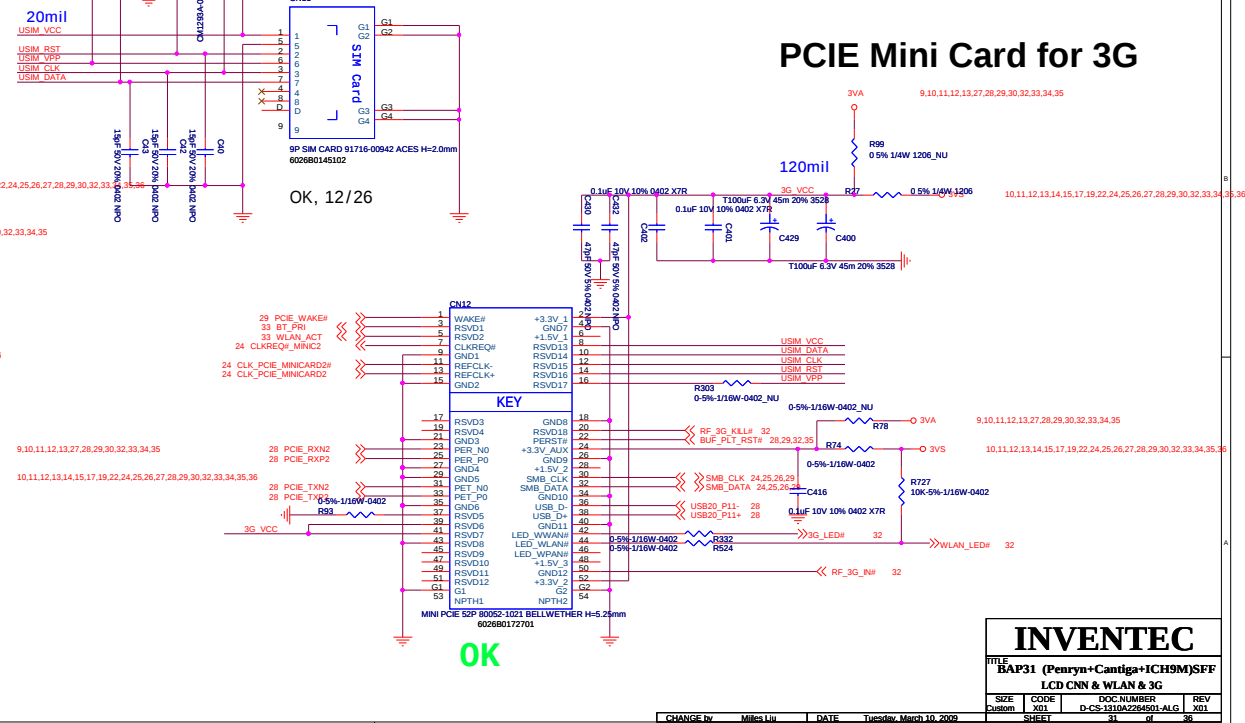
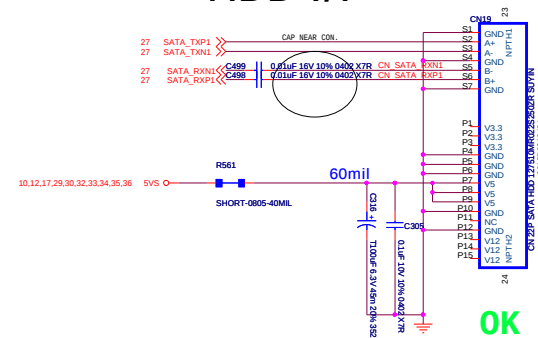
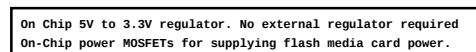
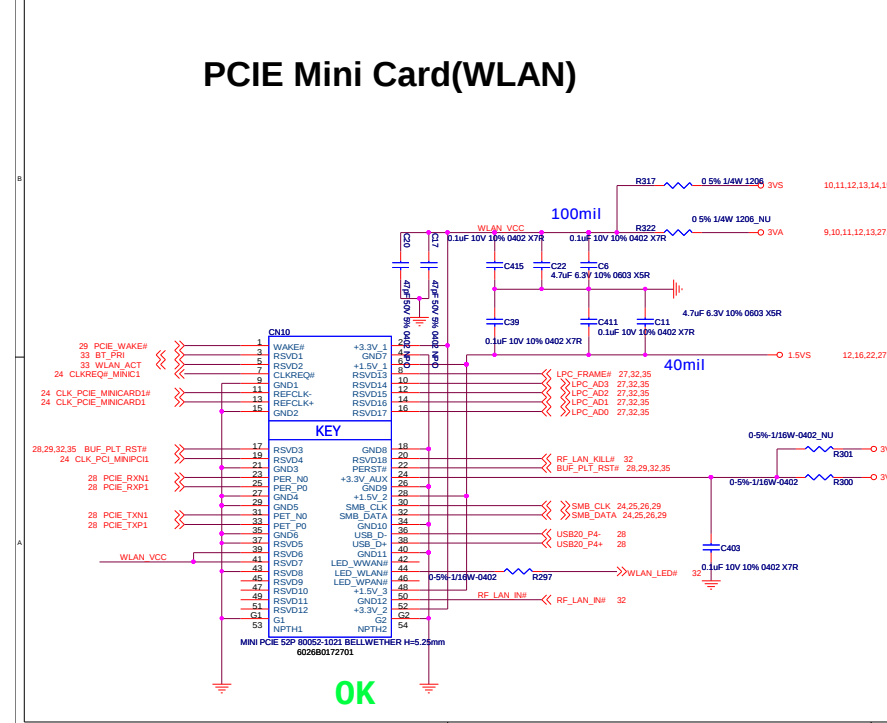
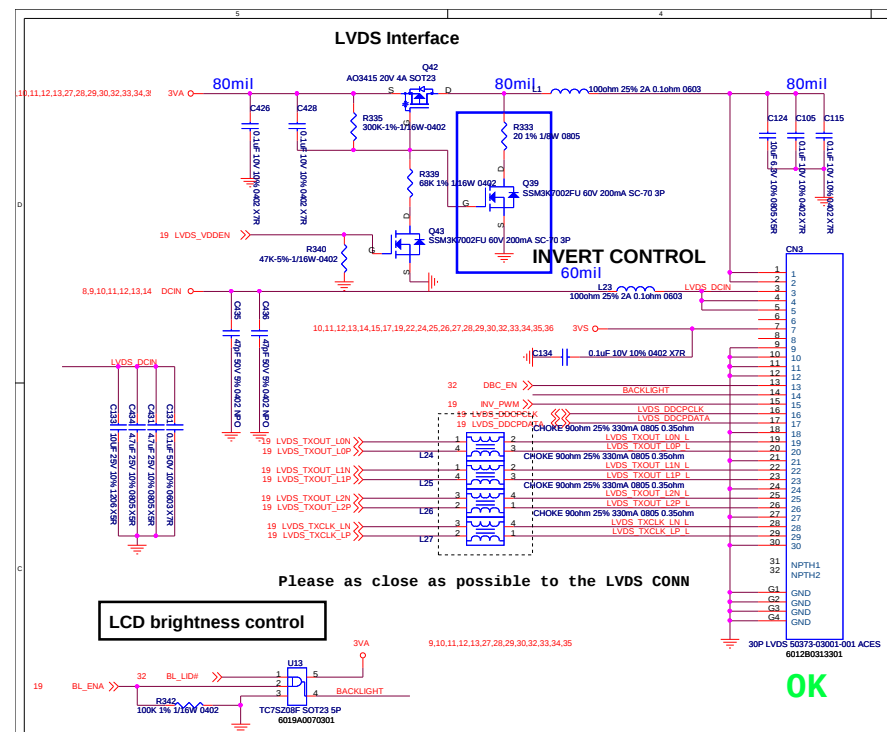


|           |                                                        |
|-----------|--------------------------------------------------------|
| PCI_GNT#3 | No stuff : by default<br>Stuff : For A16 swap override |
| PCI_GNT#0 | SPI_CS1#                                               |
| 1         | 1                                                      |
| 1         | 0                                                      |
| 0         | 1                                                      |

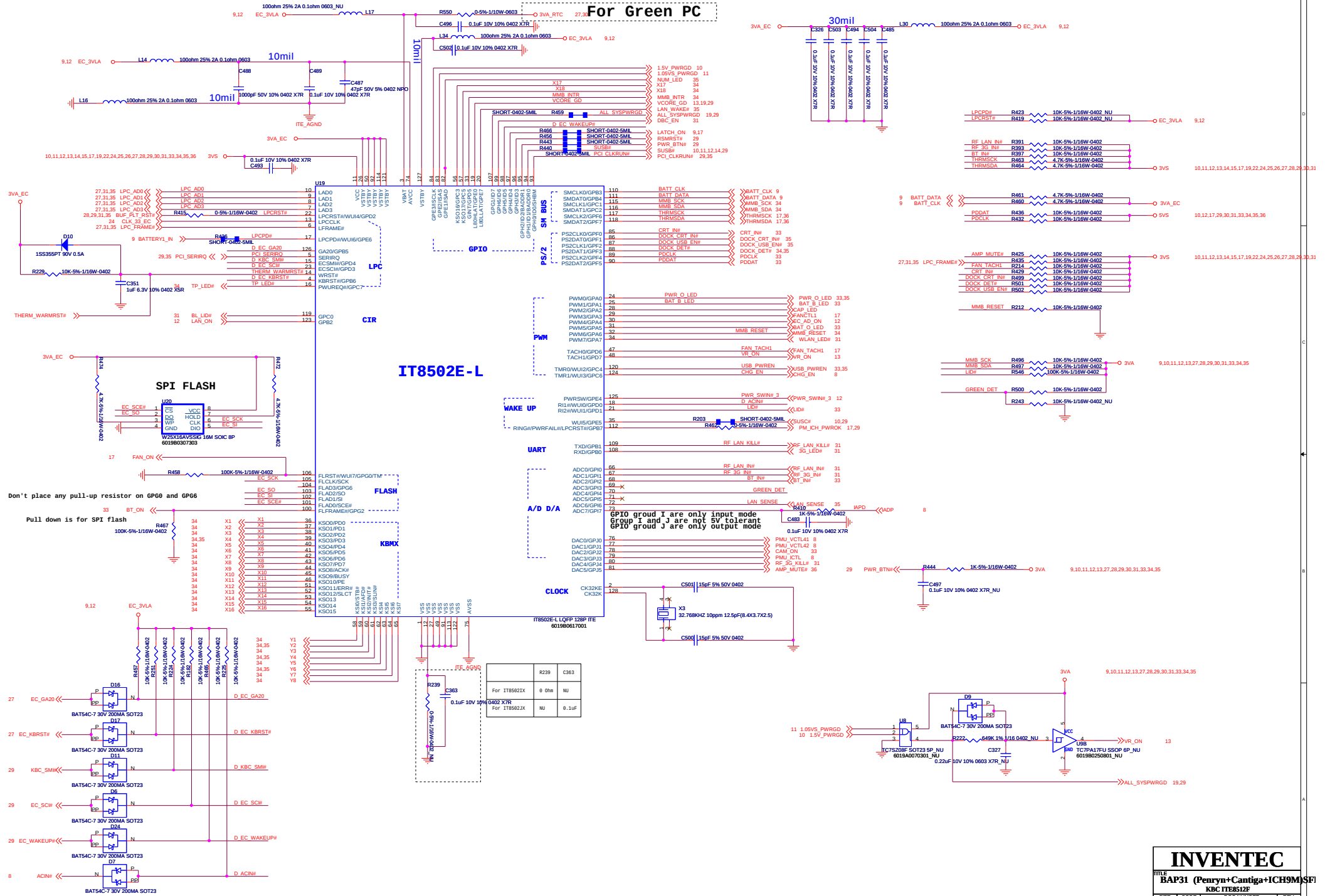
Check BIOS type







For Green PC



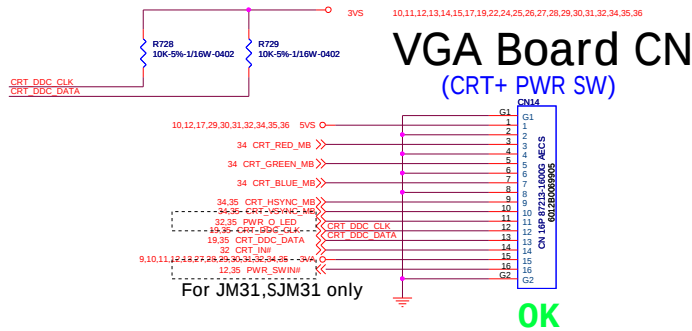
INVENTEC

TITLE BAP31 (Penryn+Contiga+ICH9M)SF  
KBC IT8512F

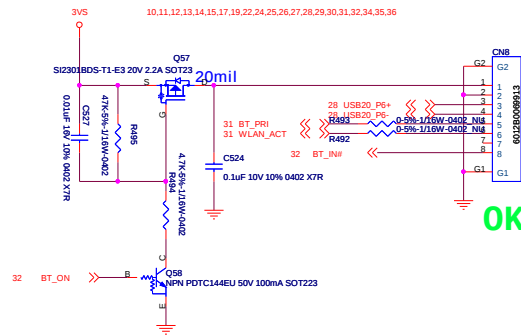
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DOC NUMBER D-CS-131042264501-ALG  
REV X01

CHANGE IN Millicu DATE Tuesday, March 10, 2009

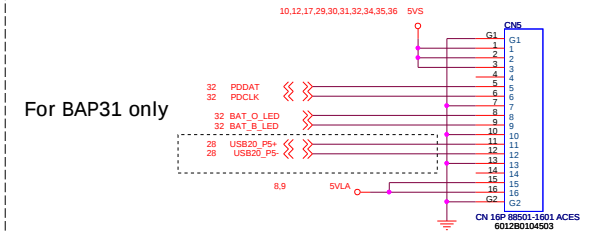
SHEET 32 of 36



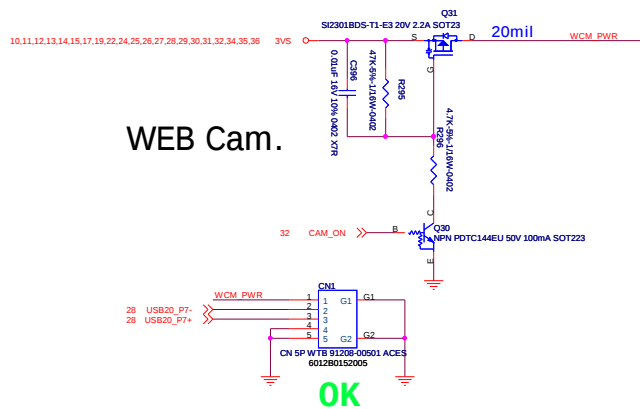
## Bluetooth CON.



## GLIDE PAD Board

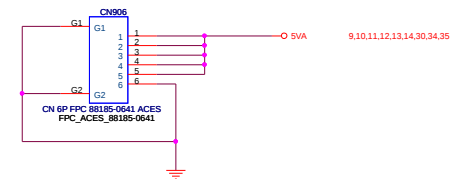
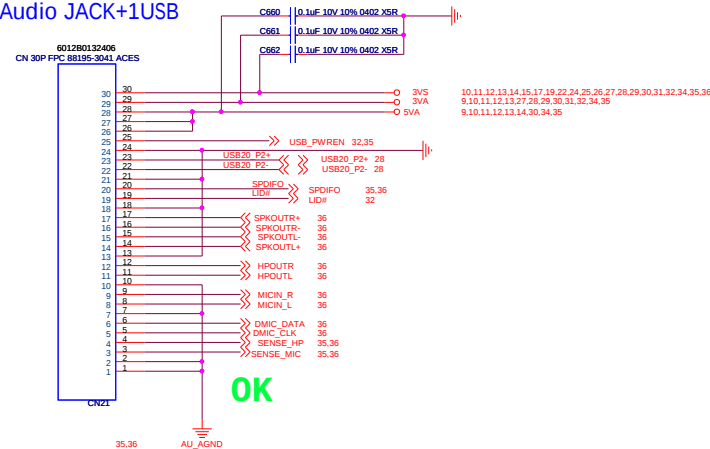


## WEB Cam.



## AUDIO Board CN

(Audio JACK+1USB)

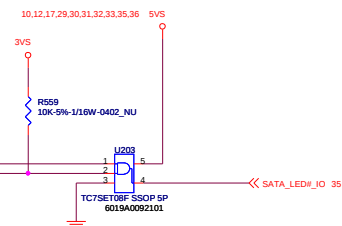
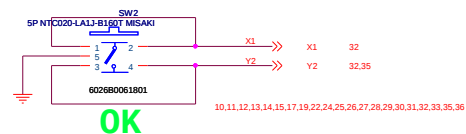
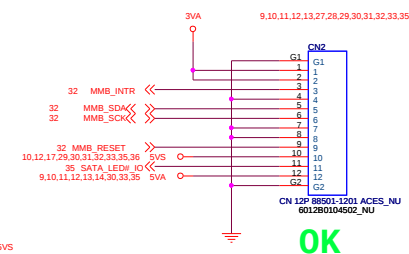
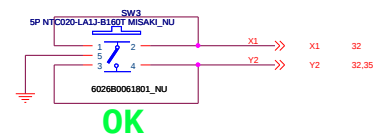
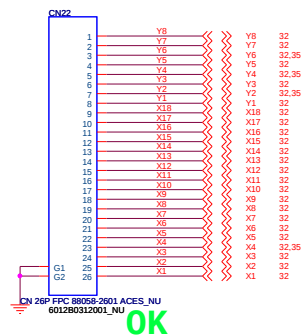
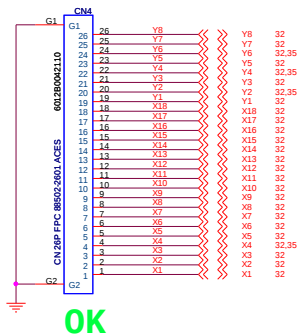


**INVENTEC**

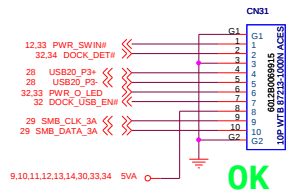
**BAP31 (Penryn+Cantiga+ICH9M) Motherboard**

SIZE CODE DOC NUMBER REV  
Custom X01 D-CS-1310A2264501-ALG X01  
SHEET 33 of 36

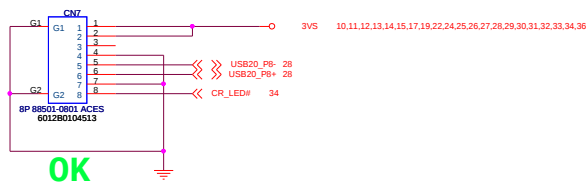
CHANGE by Miles Liu DATE Tuesday, March 10, 2009



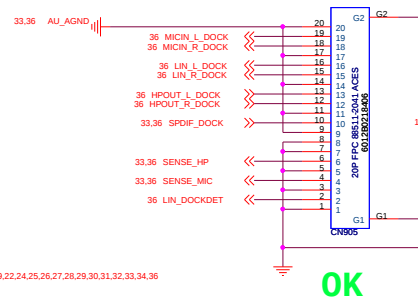
## MB(USB) TO EASY/B



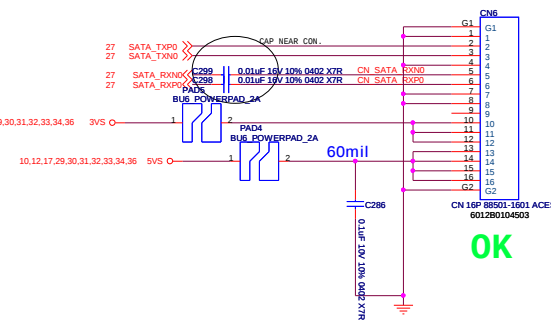
## Card Reader BOARD CN



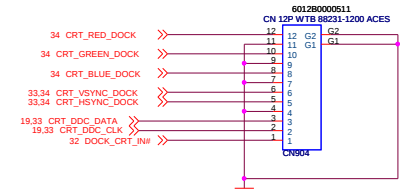
## MB(AUDIO) TO EASY/B(For BAP31)



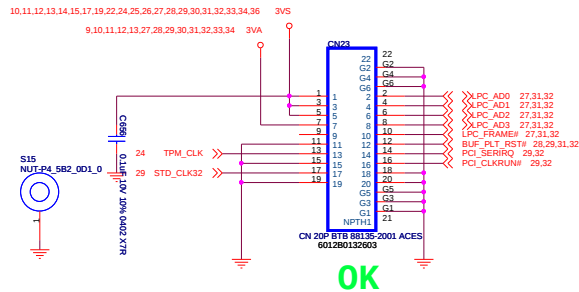
## SSD I/F



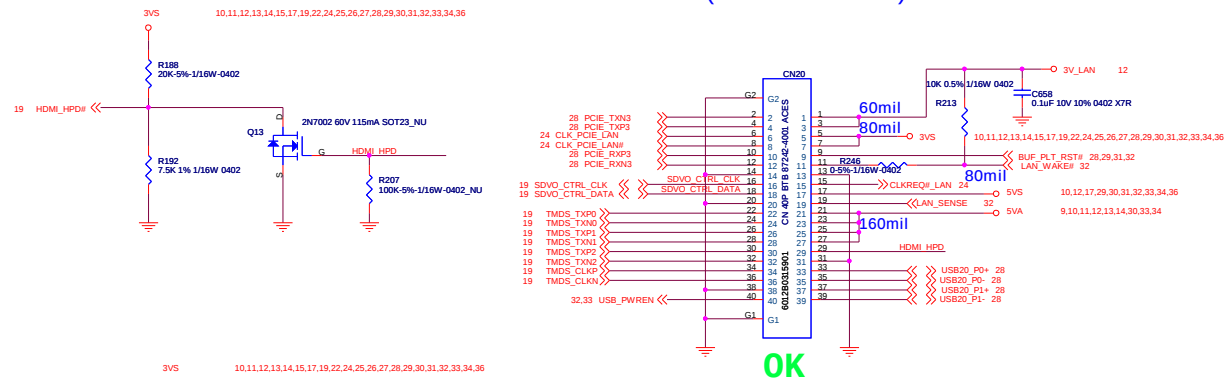
## MB(RGB) TO EASY/B



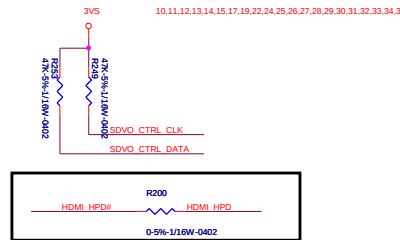
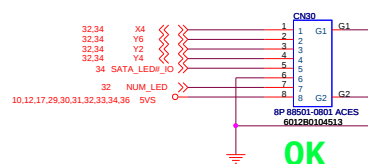
## TPM CN



## USB Board CN (LAN+HDMI+2USB)



## SW/B CN



**INVENTEC**

MODEL  
BAP31 (Penryn+Cantiga+ICH9M)SFF

| SIZE   | CODE | DOC NUMBER            | REV |
|--------|------|-----------------------|-----|
| Custom | X01  | D-CS-1310A2264501-ALG | X01 |

| CHANGE by | Miles Lin | DATE | Tuesday, March 10, 2009 | SHEET | 35 | of | 36 |
|-----------|-----------|------|-------------------------|-------|----|----|----|
|-----------|-----------|------|-------------------------|-------|----|----|----|

