

Garda-3 Block Diagram

(Discrete)

CLK GEN.

IDT CV125PA
(ICS 954206) 3

Mobile CPU

Yonah 478

G791/G792

19

Project code: 91.4P401.001

PCB P/N : 55.4P401.XXX

REVISION : 06208-2

(Hannstar, GCE)

DATE:2006/07/??

PCB STACKUP

TOP
VCC
S
S
GND
BOTTOM

SYSTEM

TPS51120

40

INPUTS

OUTPUTS

DCBATOUT

5V_S5
3D3V_S5

SYSTEM DC/DC

APL5912

43

INPUTS

OUTPUTS

1D8V_S3

1D05V_S0

TPS51116

41

DCBATOUT

1D8V_S3
DDR_VREF_S0

APL5332KAC

3D3V_S0

2D5V_S0

43

APL5912

1D8V_S3

1D5V_S0

43

MAXIM CHARGER

ISL6255

42

INPUTS

OUTPUTS

DCBATOUT

CHG_PWR
18V 4.0A
UP+5V
5V 100mA

CPU

ISL6262

38,39

INPUTS

OUTPUTS

DCBATOUT

VCC_CORE_S0
0~1.3V
44A

ATI M52 DC/DC

ISL6269

52

INPUTS

OUTPUTS

DCBATOUT

VGA_CORE_S0

APL5331

1D8V_S0

1D2V_S0

43

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

BLOCK DIAGRAM

Size

A3

Document Number

AG3

Rev

2

Date: Thursday, April 20, 2006

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A

B

ICH7M Integrated Pull-up
and Pull-down Resistors

ICH7-M EDS 17837 1.5V1

EE_DIN,EE_DOUT, GNT[3:0], GPIO[25], GNT[4]#/GPIO48, GNT[5]#/GPO17, PME#, LAD[3:0]#/FHW[3:0]#, LAN_RXD[2:0] LDRQ[0], LDRQ[1]/GPIO[41], PWRBTN#, TP[3]	ICH7 internal 20K pull-ups
DD[7], DDREQ	ICH7 internal 11.5K pull-downs
ACZ_BIT_CLK, ACZ_RST#, ACZ_SDIN[2:0], ACZ_SDOUT,ACZ_SYNC, DPRSLPVR/GPIO16, EE_CS,SPI_ARB, SPI_CLK, SPKR,	ICH7 internal 20K pull-downs
USB[7:0][P,N]	ICH7 internal 15K pull-downs
SATALED#	ICH7 internal 15K pull-up
LAN_CLK	ICH7 internal 100K pull-down

3

ICH7M IDE Integrated Series
Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm
--	----------------------

ICH7M Functional Strap Definitions

page 16

Signal	Usage/When Sampled	Comment
ACZ_SDOUT	XOR Chain Entrance/ PCIE Port Config bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
ACZ_SYNC	PCIE bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
EE_CS	Reserved	This signal should not be pull high.
EE_DOUT	Reserved	This signal should not be pull low.
GNT2#	Reserved	This signal should not be pull low.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT5#/ GPIO17#, GNT4#/ GPIO48	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT5# is MSB, 01-SPI, 10-PCI, 11-LPC.
DPRSLPVR	Reserved	This signal should not be pull high.
GPIO25	Reserved. Rising Edge of RSMRST#.	This signal should not be pull low.
INTVRMEN	Integrated VccSus1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05 VRM when sampled high
LINKALERT#	Reserved	Requires an external pull-up resistor.
REQ[4:1]#	XOR Chain Selection. Rising Edge of PWROK.	TBD, Chapter 8.
SATALED#	Reserved	This signal should not be pull low.
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH7 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.

C

954305D 27Mhz/LCDCLK Spread
and Frequency Selection Table

SS3 Byte9 bit 7	SS2 bit6	SS1 bit5	SS0 bit4	Spread Amount%
0	0	0	0	-0.50 Down
0	0	0	1	-1.00 Down
0	0	1	0	-1.50 Down
0	0	1	1	-2.00 Down
0	1	0	0	-0.75 Down
0	1	0	1	-1.25 Down
0	1	1	0	-1.75 Down
0	1	1	1	-2.25 Down
1	0	0	0	+0.25 Center
1	0	0	1	+0.5 Center
1	0	1	0	+0.75 Center
1	0	1	1	+1.0 Center
1	1	0	0	+0.25 Center
1	1	0	1	+0.5 Center
1	1	1	0	+0.75 Center
1	1	1	1	+1.0 Center

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PCI Routing

page 16

	IDSEL	INT -> PIRQ	REQ/GNT
1410	22	A->G	0
MiniPCI	21	A/C B/D -> E	1
LAN	23	A -> H	2
1394	17	A->B, B->F,	3

History

D

E

Calistoga Strapping Signals and
Configuration

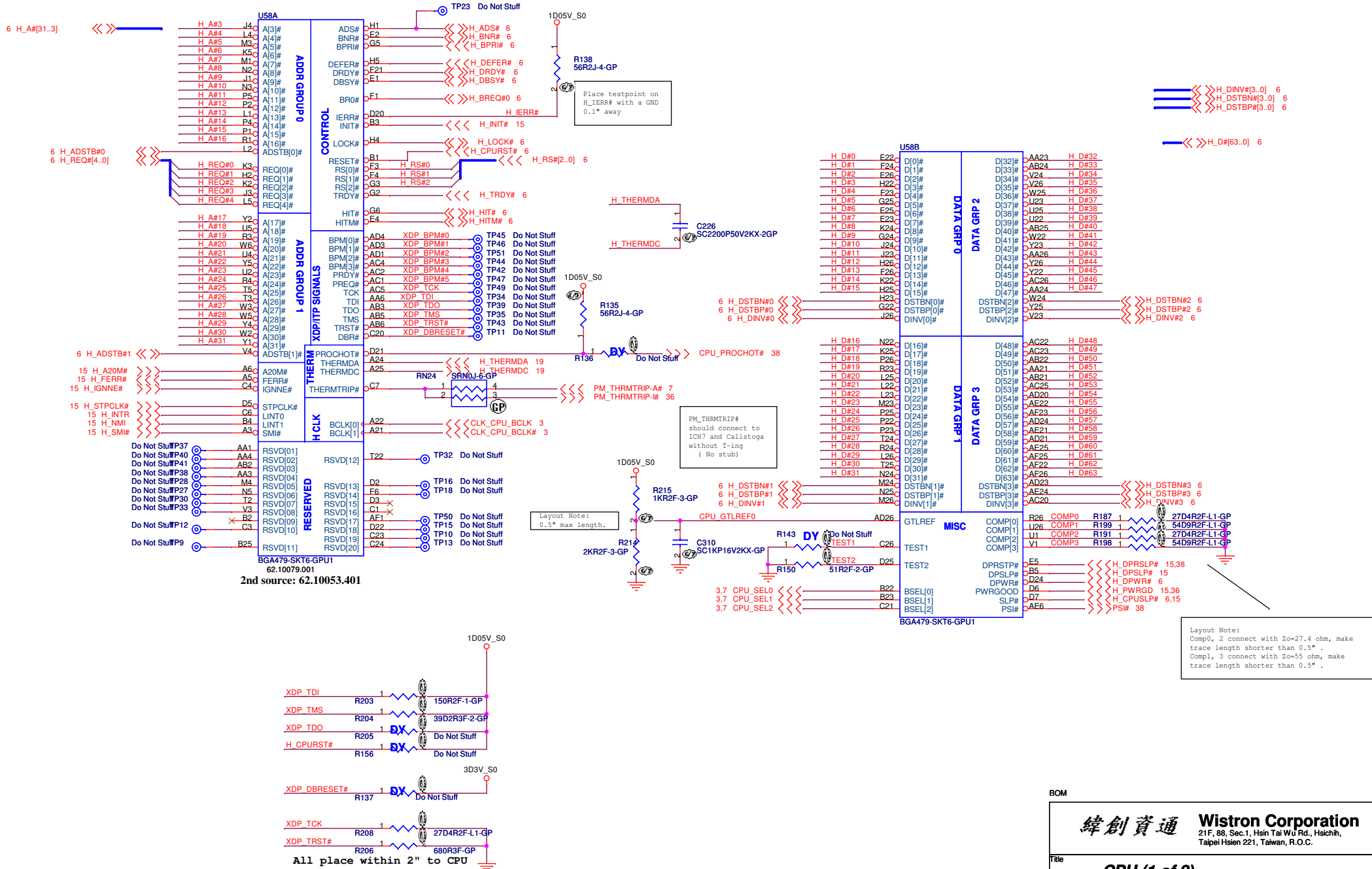
EDS 17050 0.71 page 7

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	001 = FSB533 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 =Mobile CPU(Default)
CFG8	Reserved	
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. 1= Normal operation(Default):Lane Numbered in order
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled 11 = Normal Operation (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled (Default)
CFG17	Global R-comp Disable (All R-comps)	0 = All R-comp Disable 1 = Normal Operation (Default)
CFG18	VCC Select	0 = 1.05V (Default) 1 = 1.5V
CFG19	DMI Lane Reversal	0 = Normal operation (Default):lane Numbered in order 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	0 = Only SDVO or PCIE x1 is operational (Default) 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCTRL _DATA	SDVO Present	0 = No SDVO Card present (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading
edge of the Calistoga GMCH PWORK in signal.

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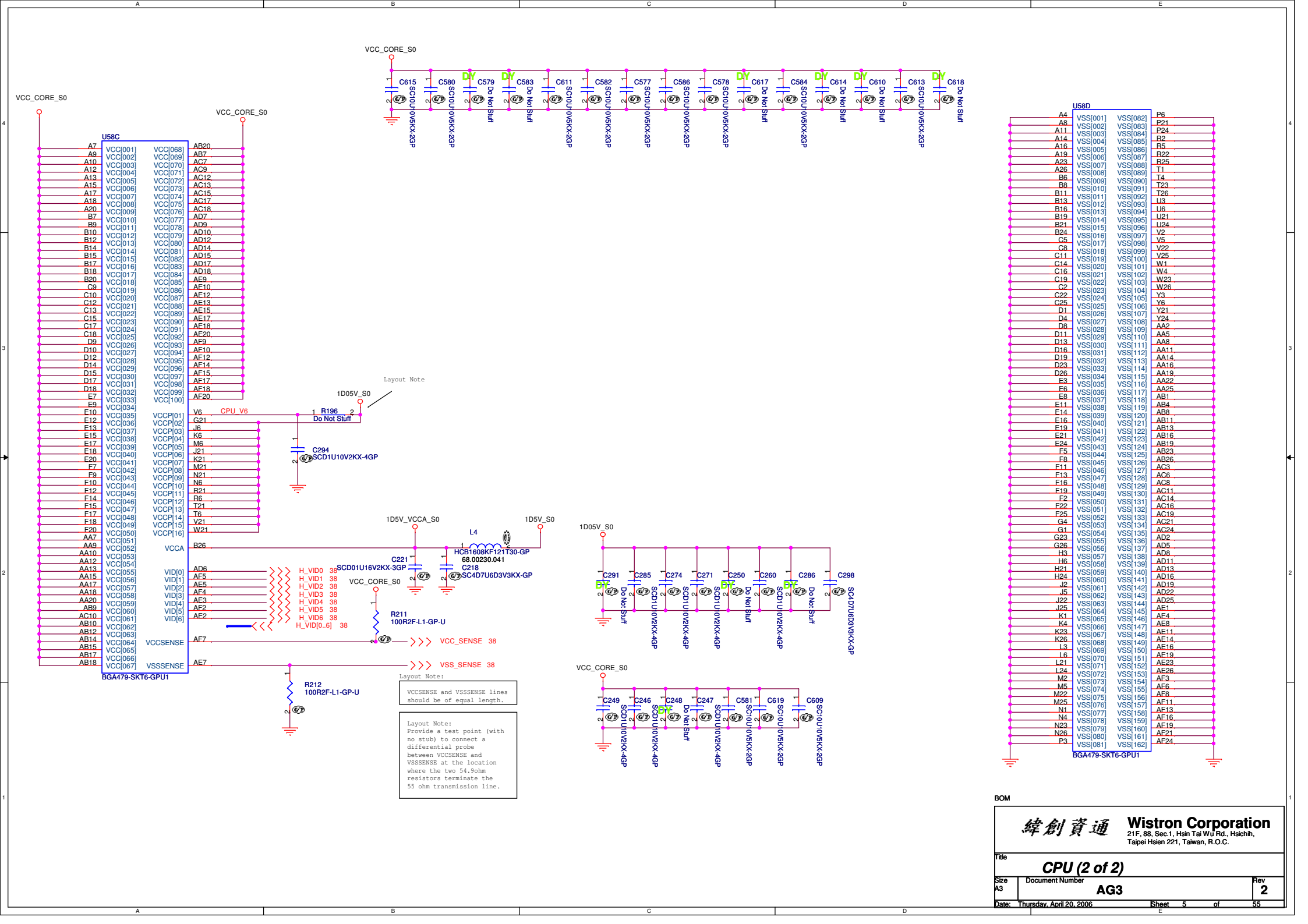
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
Size	Document Number		Rev
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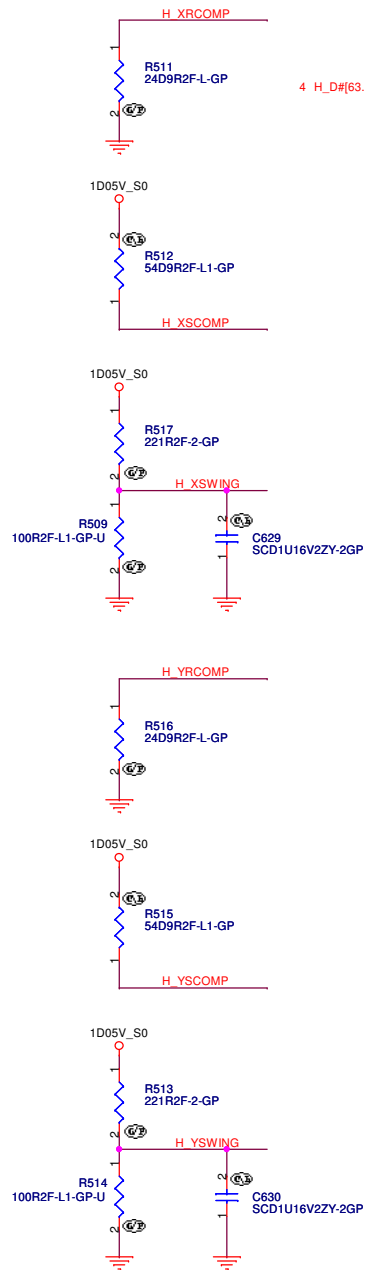


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Size A3 Document Number: **AG3** Rev: **2**
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4 H_D#[63..0] <<<

3 CLK_MCH_BCLK# <<<
3 CLK_MCH_BCLK# <<<

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	K2	H_D#_4
H_D#5	G1	H_D#_5
H_D#6	G2	H_D#_6
H_D#7	K9	H_D#_7
H_D#8	K1	H_D#_8
H_D#9	K7	H_D#_9
H_D#10	J8	H_D#_10
H_D#11	H4	H_D#_11
H_D#12	J3	H_D#_12
H_D#13	K11	H_D#_13
H_D#14	G4	H_D#_14
H_D#15	T10	H_D#_15
H_D#16	T3	H_D#_16
H_D#17	U7	H_D#_17
H_D#18	U9	H_D#_18
H_D#19	U11	H_D#_19
H_D#20	T11	H_D#_20
H_D#21	W9	H_D#_21
H_D#22	T1	H_D#_22
H_D#23	T8	H_D#_23
H_D#24	T4	H_D#_24
H_D#25	W7	H_D#_25
H_D#26	U5	H_D#_26
H_D#27	T9	H_D#_27
H_D#28	T5	H_D#_28
H_D#29	J5	H_D#_29
H_D#30	AB7	H_D#_30
H_D#31	AA9	H_D#_31
H_D#32	W4	H_D#_32
H_D#33	W3	H_D#_33
H_D#34	Y3	H_D#_34
H_D#35	Y7	H_D#_35
H_D#36	W5	H_D#_36
H_D#37	Y10	H_D#_37
H_D#38	AB8	H_D#_38
H_D#39	W2	H_D#_39
H_D#40	AA4	H_D#_40
H_D#41	AA7	H_D#_41
H_D#42	AA2	H_D#_42
H_D#43	AA6	H_D#_43
H_D#44	AA10	H_D#_44
H_D#45	Y8	H_D#_45
H_D#46	AA1	H_D#_46
H_D#47	AB4	H_D#_47
H_D#48	AC9	H_D#_48
H_D#49	AB11	H_D#_49
H_D#50	AC11	H_D#_50
H_D#51	AB3	H_D#_51
H_D#52	AC2	H_D#_52
H_D#53	AD1	H_D#_53
H_D#54	AD9	H_D#_54
H_D#55	AC1	H_D#_55
H_D#56	AD7	H_D#_56
H_D#57	AC6	H_D#_57
H_D#58	AB5	H_D#_58
H_D#59	AD10	H_D#_59
H_D#60	AD4	H_D#_60
H_D#61	AC8	H_D#_61
H_D#62		H_D#_62
H_D#63		H_D#_63

H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING

H_CLKIN	AG2	H_CLKIN
H_CLKIN#	AG1	H_CLKIN#

U56A

HOST

H_A#_3	H9	H_A#3
H_A#_4	C9	H_A#4
H_A#_5	E11	H_A#5
H_A#_6	G11	H_A#6
H_A#_7	F11	H_A#7
H_A#_8	G12	H_A#8
H_A#_9	E9	H_A#9
H_A#_10	H11	H_A#10
H_A#_11	J12	H_A#11
H_A#_12	G14	H_A#12
H_A#_13	D9	H_A#13
H_A#_14	J14	H_A#14
H_A#_15	H13	H_A#15
H_A#_16	J15	H_A#16
H_A#_17	F14	H_A#17
H_A#_18	D12	H_A#18
H_A#_19	A11	H_A#19
H_A#_20	C11	H_A#20
H_A#_21	A12	H_A#21
H_A#_22	A13	H_A#22
H_A#_23	E13	H_A#23
H_A#_24	G13	H_A#24
H_A#_25	F12	H_A#25
H_A#_26	B12	H_A#26
H_A#_27	C12	H_A#27
H_A#_28	A14	H_A#28
H_A#_29	C14	H_A#29
H_A#_30	D14	H_A#30
H_A#_31		H_A#31

H_ADS#	E8	H_ADS#
H_ADSTB#_0	B9	H_ADSTB#_0
H_ADSTB#_1	C13	H_ADSTB#_1
H_VREF	J13	H_VREF
H_BNR#	C6	H_BNR#
H_BPRI#	F6	H_BPRI#
H_BREQ#	C7	H_BREQ#
H_CPURST#	B7	H_CPURST#
H_DBSY#	A7	H_DBSY#
H_DEFER#	C3	H_DEFER#
H_DPWR#	J9	H_DPWR#
H_DRDY#	H8	H_DRDY#
H_VREF_1	K13	H_VREF_1

H_DINV#_0	J7	H_DINV#0
H_DINV#_1	W8	H_DINV#1
H_DINV#_2	U3	H_DINV#2
H_DINV#_3	AB10	H_DINV#3

H_DSTBN#_0	K4	H_DSTBN#0
H_DSTBN#_1	T7	H_DSTBN#1
H_DSTBN#_2	Y5	H_DSTBN#2
H_DSTBN#_3	AC4	H_DSTBN#3

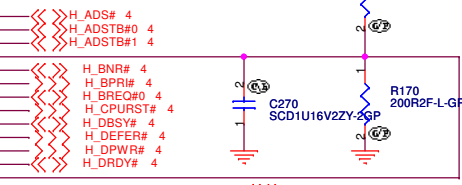
H_DSTBP#_0	K3	H_DSTBP#0
H_DSTBP#_1	T6	H_DSTBP#1
H_DSTBP#_2	AA5	H_DSTBP#2
H_DSTBP#_3	AC5	H_DSTBP#3

H_HIT#	D3	H_HIT#
H_HITM#	D4	H_HITM#
H_LOCK#	B3	H_LOCK#

H_REQ#_0	D8	H_REQ#0
H_REQ#_1	G8	H_REQ#1
H_REQ#_2	B8	H_REQ#2
H_REQ#_3	F8	H_REQ#3
H_REQ#_4	A8	H_REQ#4

H_RS#_0	B4	H_RS#0
H_RS#_1	E6	H_RS#1
H_RS#_2	D6	H_RS#2

H_SLPCPU#	E3	H_SLPCPU#
H_TRDY#	E7	H_TRDY#



H_DINV#(3..0]	4
---------------	---

H_DSTBN#(3..0]	4
----------------	---

H_DSTBP#(3..0]	4
----------------	---

H_HIT#	4
H_HITM#	4
H_LOCK#	4

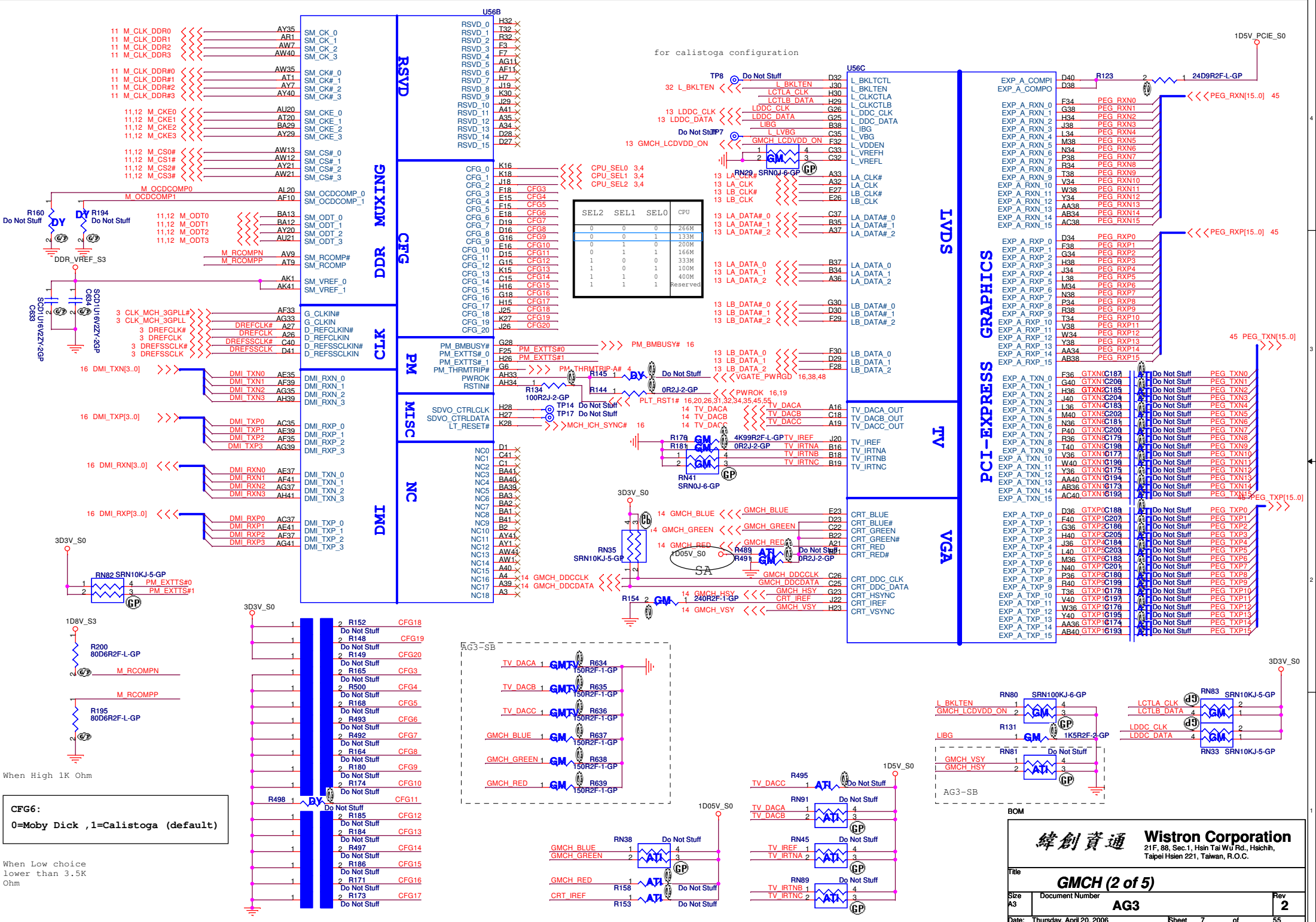
H_REQ#(4..0]	4
--------------	---

H_RS#(2..0]	4
-------------	---

H_CPUSLP#	4,15
H_TRDY#	4

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for calistoga configuration

SEL2	SEL1	SEL0	CPU
0	0	0	266M
0	0	1	133M
0	1	0	200M
0	1	1	166M
1	0	0	333M
1	0	1	100M
1	1	0	400M
1	1	1	Reserved

CFG6:
0=Moby Dick ,1=Calistoga (default)

When Low choice
lower than 3.5K
Ohm

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Size

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GMCH (2 of 5)

A3

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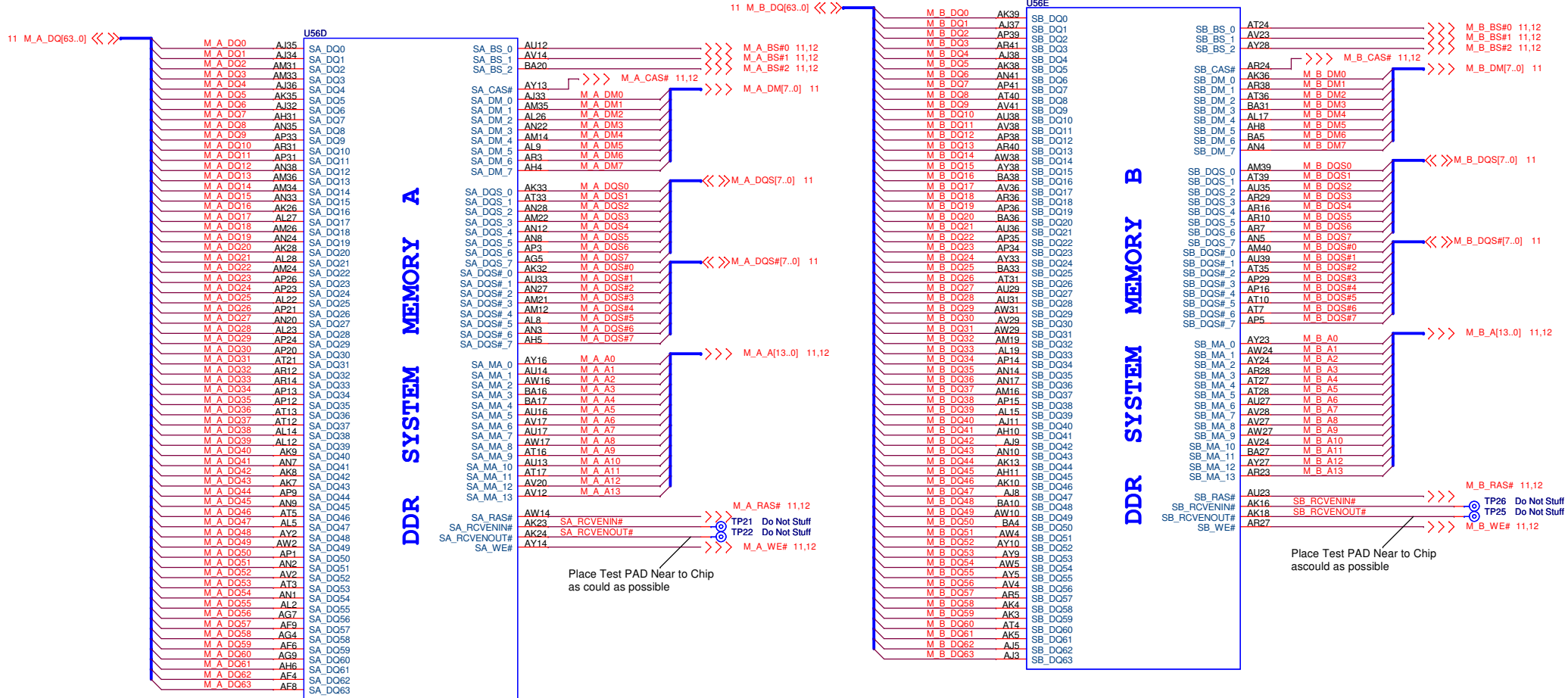
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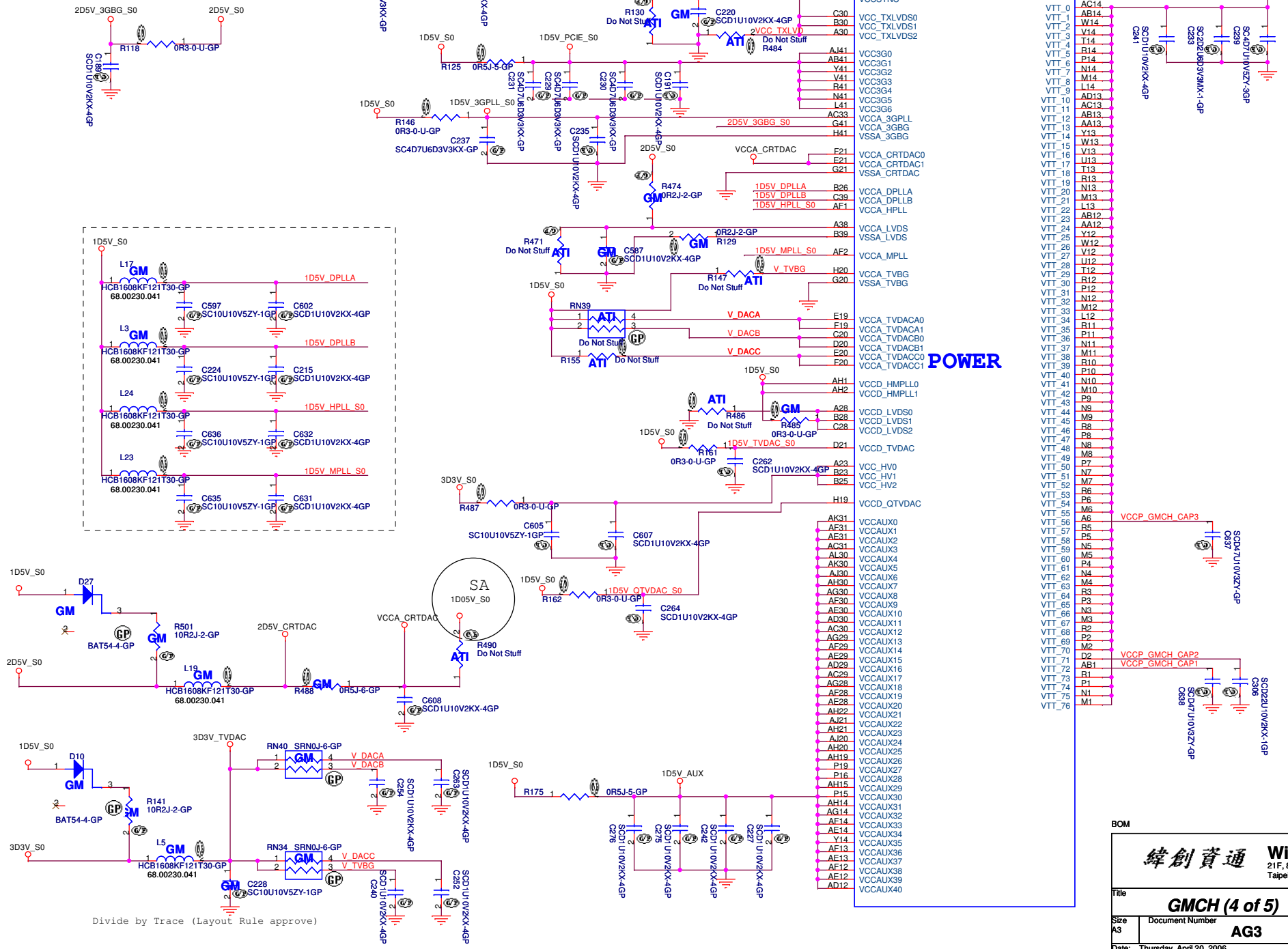
AG3

Rev

2



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[illegible]

Put decap near power(0.9V) and pull-up resistor

The diagram illustrates the PCB layout for the DDR3 SDRAM section of a board. It shows a horizontal bus connected to a vertical bus. The horizontal bus is labeled 'DDR_VREF_S0' at the top left. The vertical bus is labeled 'DDR_VREF_S0' at the bottom left. The layout includes several components: decoupling capacitors (labeled 'C262', 'C266', 'C273', 'C277', 'C278', 'C285', 'C287', 'C288', 'C296', 'C297', 'C298', 'C299', 'C300', 'C301', 'C302', 'C303', 'C304', 'C305', 'C306', 'C307', 'C308', 'C309', 'C310', 'C311', 'C312', 'C313', 'C314', 'C315', 'C316', 'C317', 'C318', 'C319', 'C320', 'C321', 'C322', 'C323', 'C324', 'C325', 'C326', 'C327', 'C328', 'C329', 'C330', 'C331', 'C332', 'C333', 'C334', 'C335', 'C336', 'C337', 'C338', 'C339', 'C340', 'C341', 'C342', 'C343', 'C344', 'C345', 'C346', 'C347', 'C348', 'C349', 'C350', 'C351', 'C352', 'C353', 'C354', 'C355', 'C356', 'C357', 'C358', 'C359', 'C360', 'C361', 'C362', 'C363', 'C364', 'C365', 'C366', 'C367', 'C368', 'C369', 'C370', 'C371', 'C372', 'C373', 'C374', 'C375', 'C376', 'C377', 'C378', 'C379', 'C380', 'C381', 'C382', 'C383', 'C384', 'C385', 'C386', 'C387', 'C388', 'C389', 'C390', 'C391', 'C392', 'C393', 'C394', 'C395', 'C396', 'C397', 'C398', 'C399', 'C400', 'C401', 'C402', 'C403', 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Place these Caps near DM1

1D8V_S3

SC02D2UB9V0ANX-1-GP

C234

DY

Do Not Sufit

SC02D2UB9V0ANX-1-GP

C245

DY

Do Not Sufit

SC02D2UB9V0ANX-1-GP

C255

DY

Do Not Sufit

SC02D2UB9V0ANX-1-GP

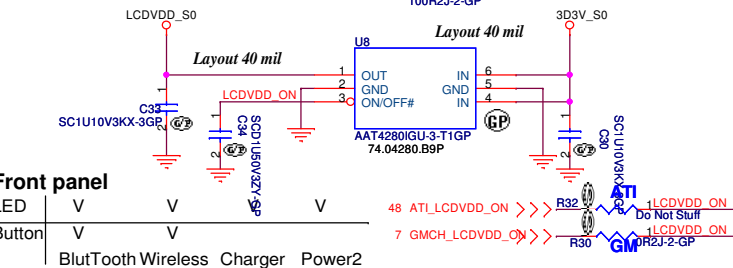
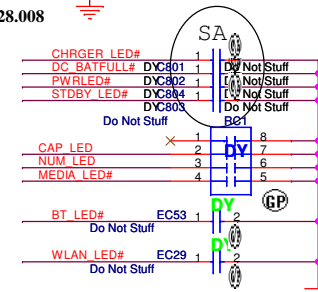
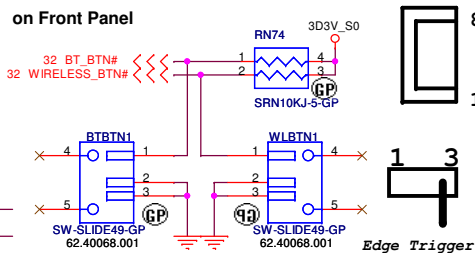
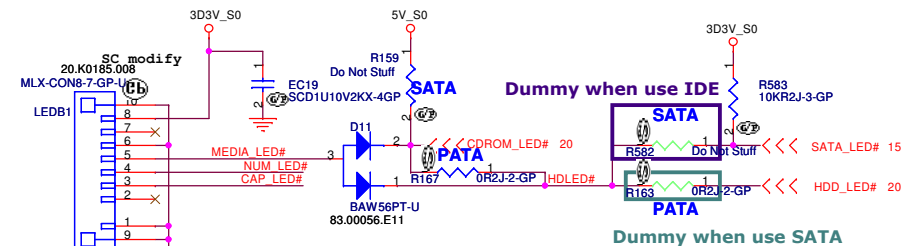
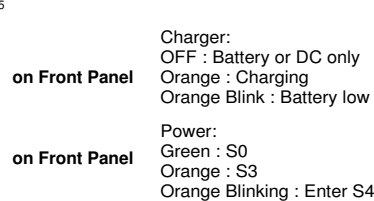
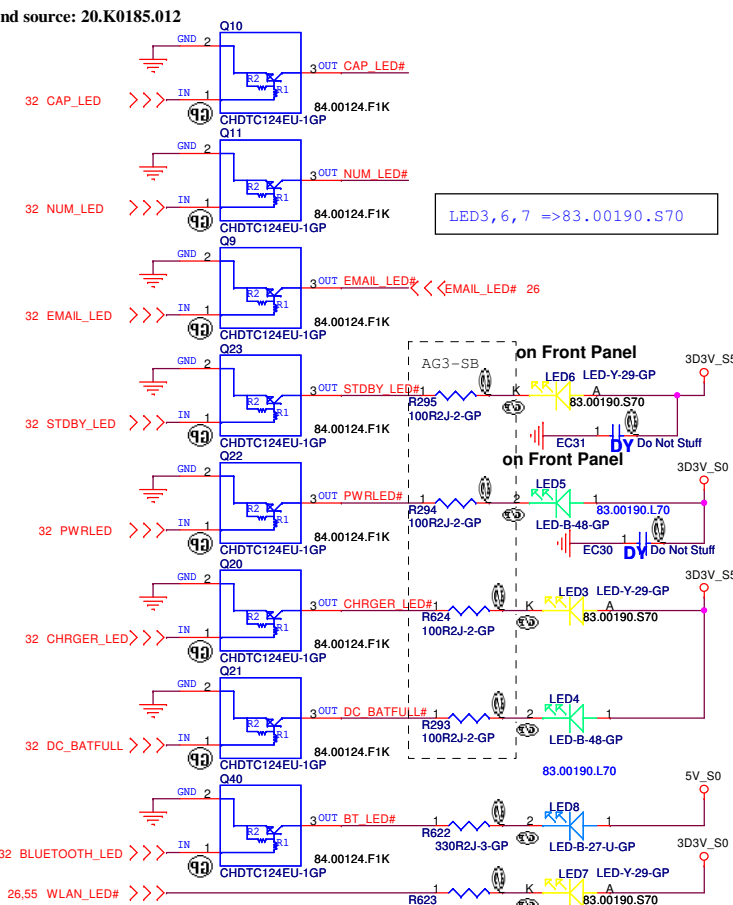
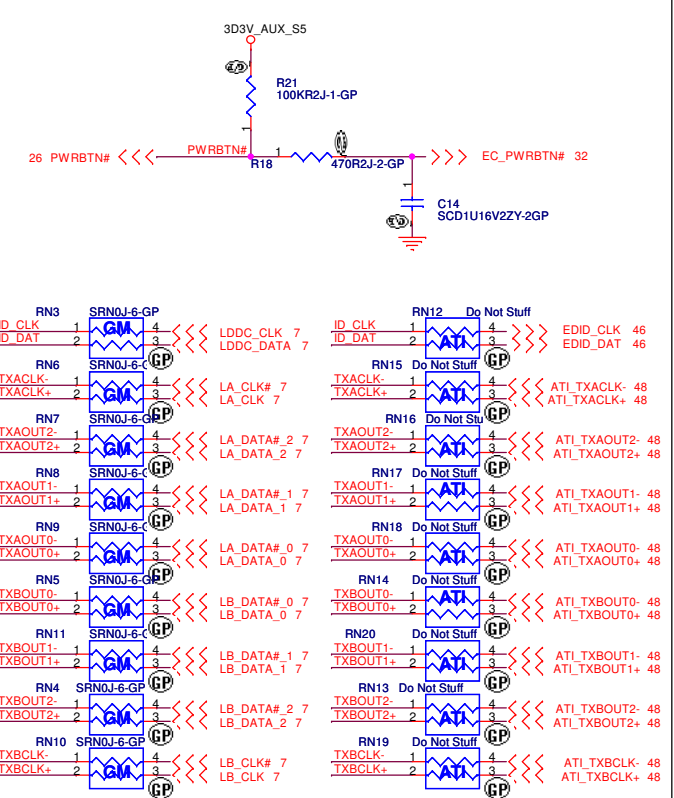
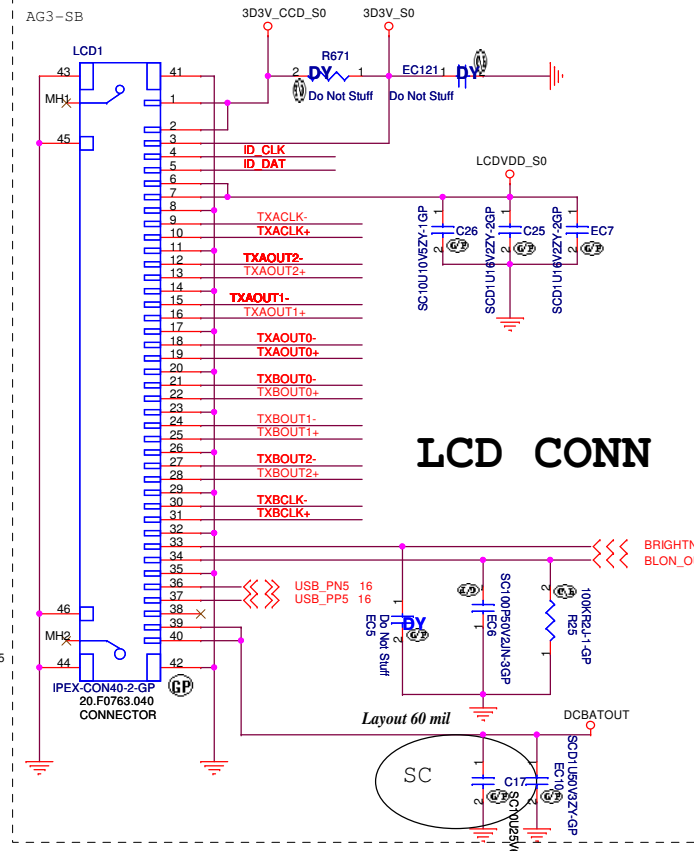
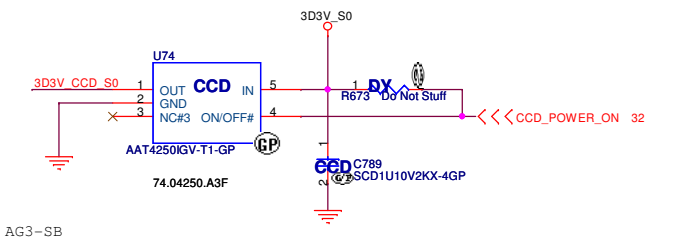
C232

DY

Do Not Sufit

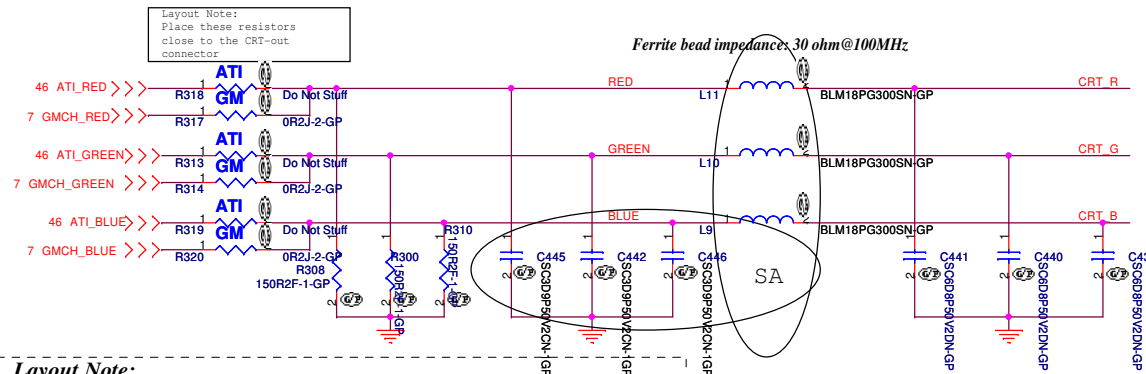
Place these Caps near DM2

Title			
DDR2 Termination Resistor			
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Date:	Friday, April 21, 2006	Sheet 12 of	55

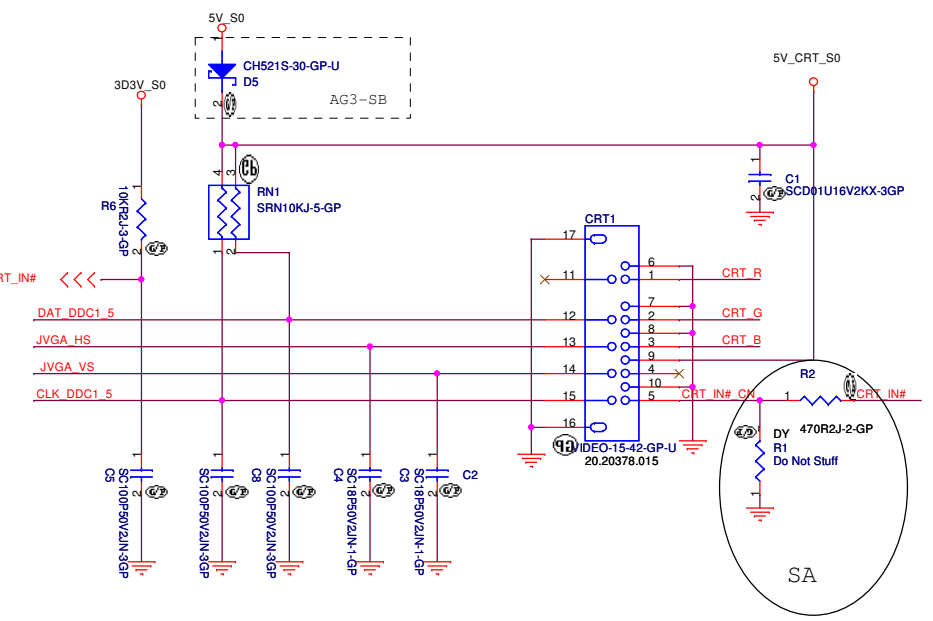


BOM			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LCD / LAUNCH / LEDS			
Size A3	Document Number	Rev	
	AG3	2	
Date:	Friday, April 21, 2006	Sheet	13 of 55

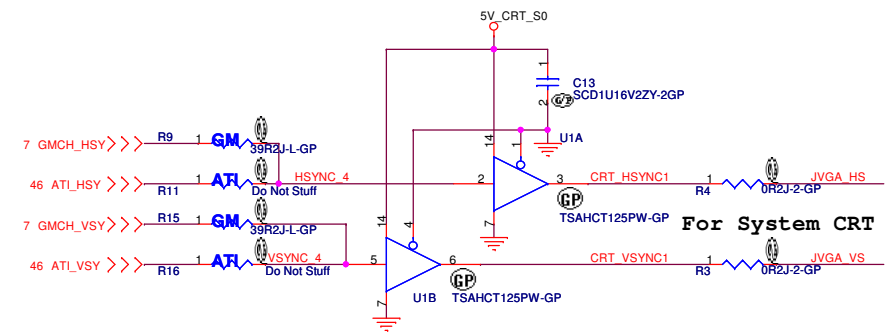
CRT I/F & CONNECTOR



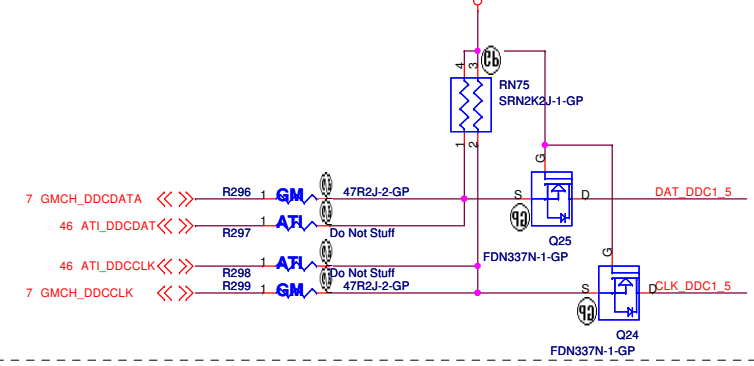
Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.



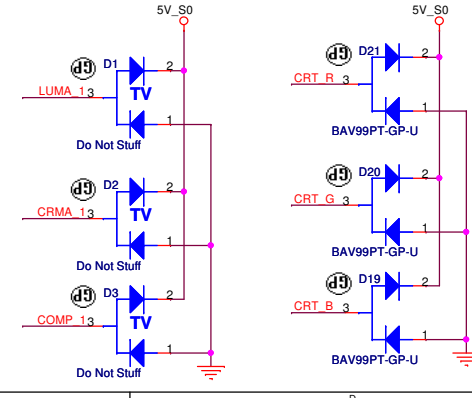
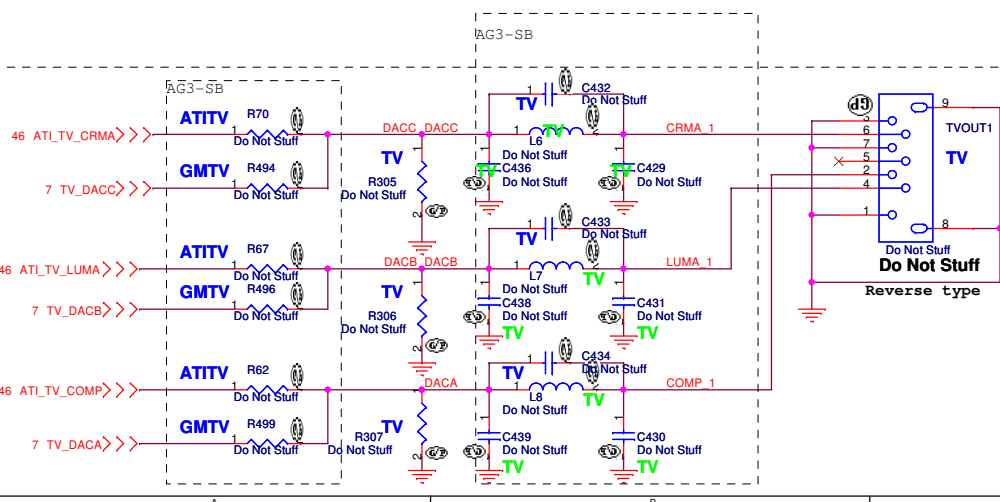
Hsync & Vsync level shift

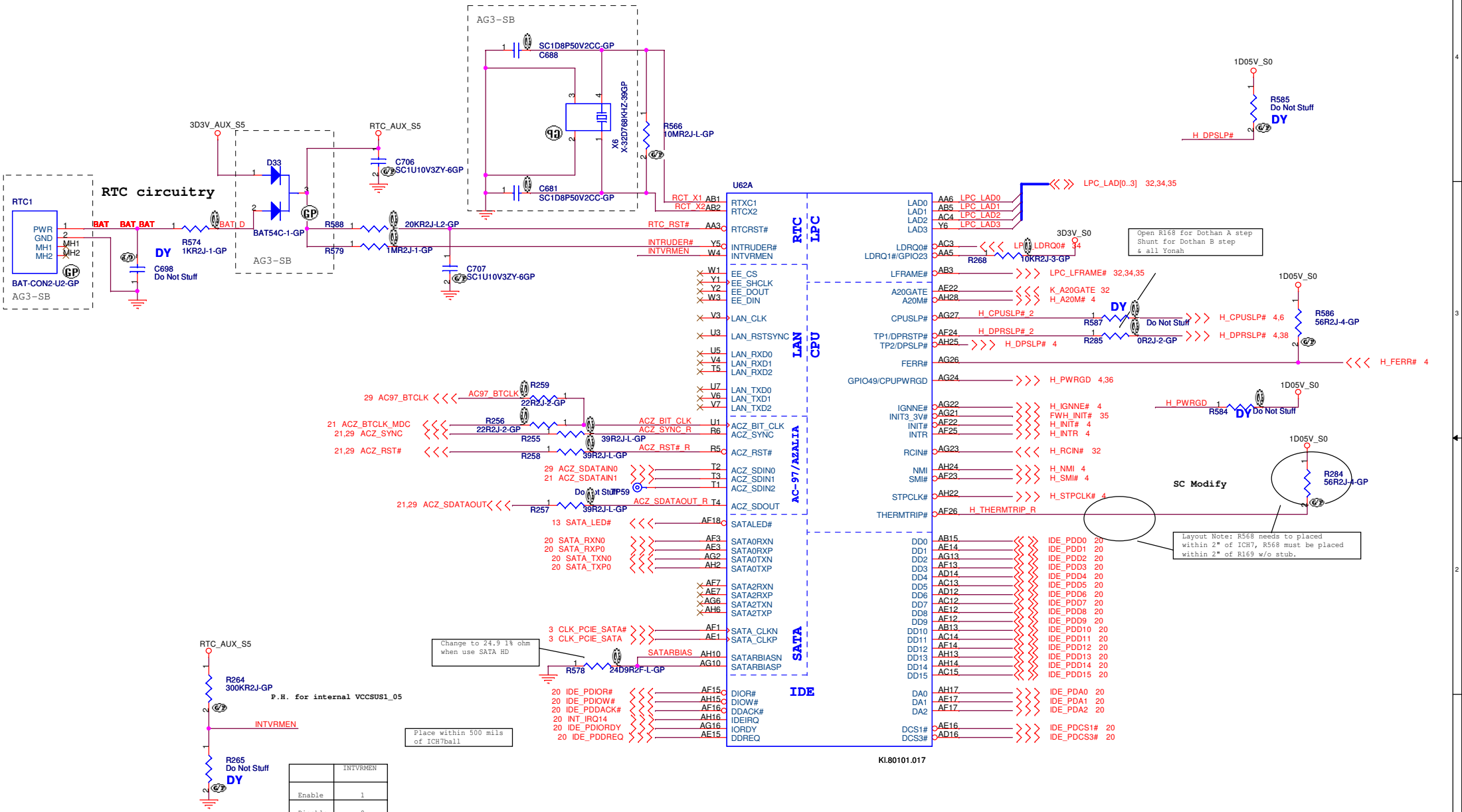


DDC_CLK & DATA level shift



TV OUT CONN





Placement Note:
Distance between the ICH-7 M and cap on the "P" signal should be identical distance between the ICH-7 M and cap on the "N" signal for same pair.

	INTVRMEN
Enable	1
Disable	0

緯創資通

Wistron Corporation

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Title

ICH7-M (1 of 4)

Size

A3

Document Number

AG3

Date

Friday, April 21, 2006

Sheet

15

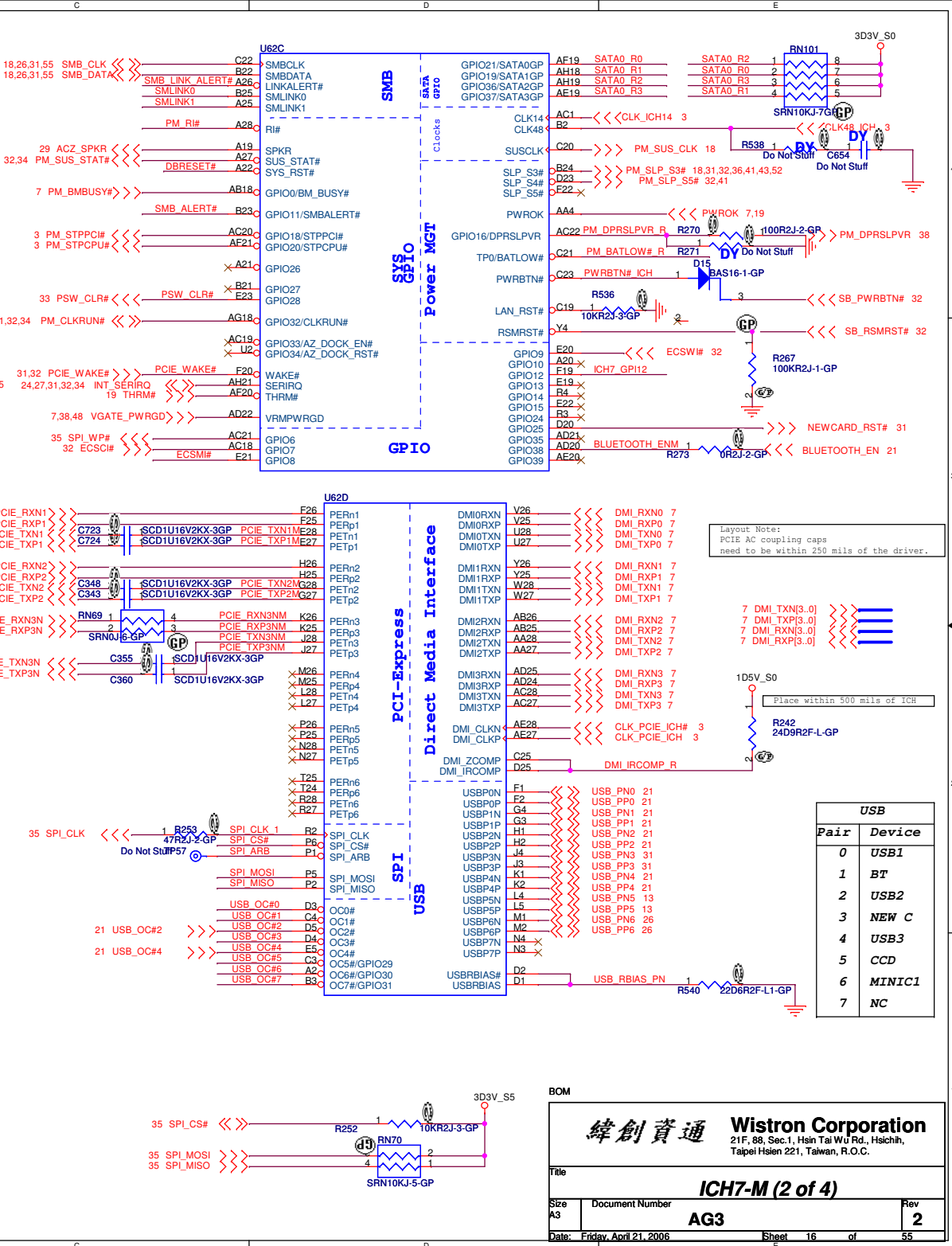
of

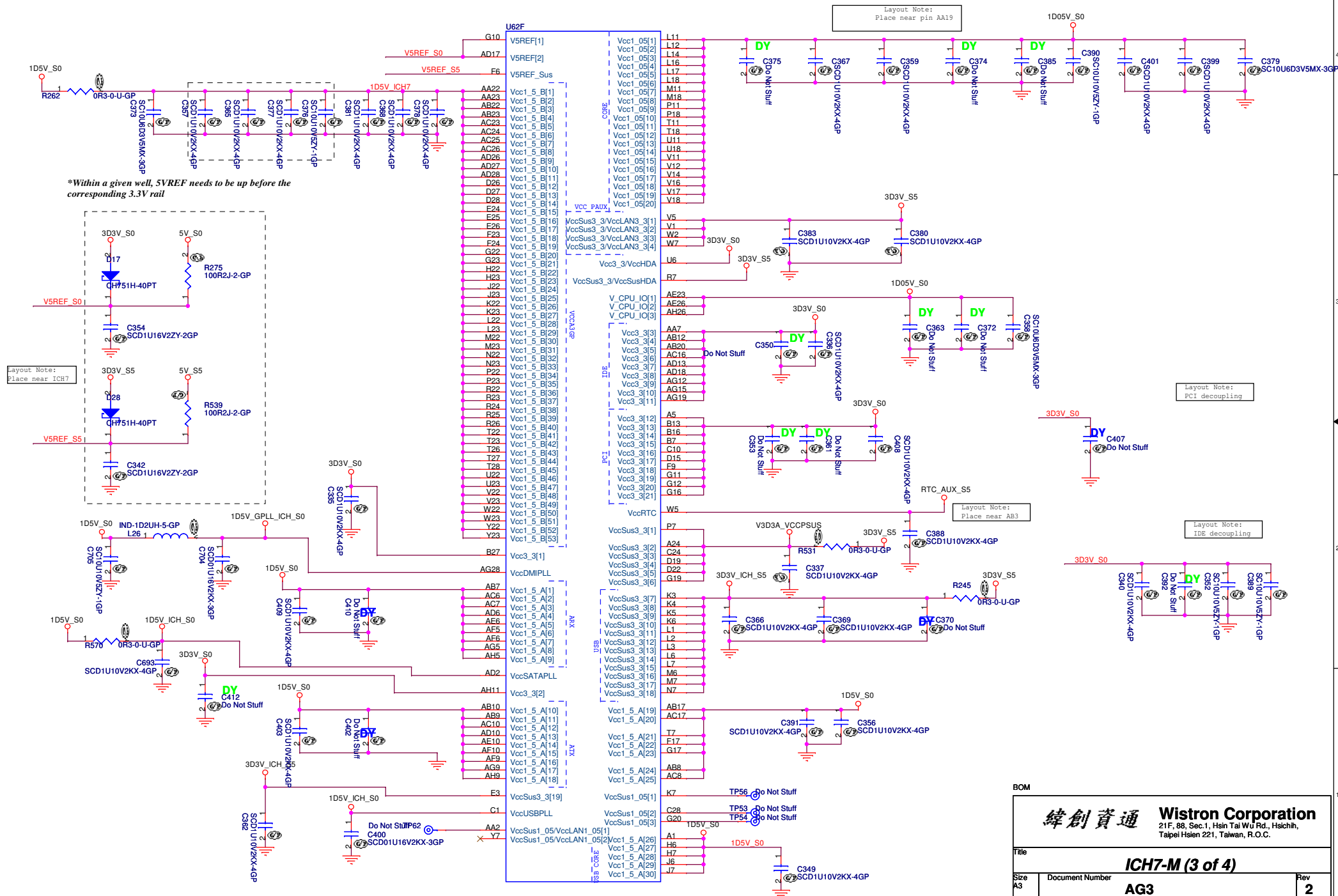
55

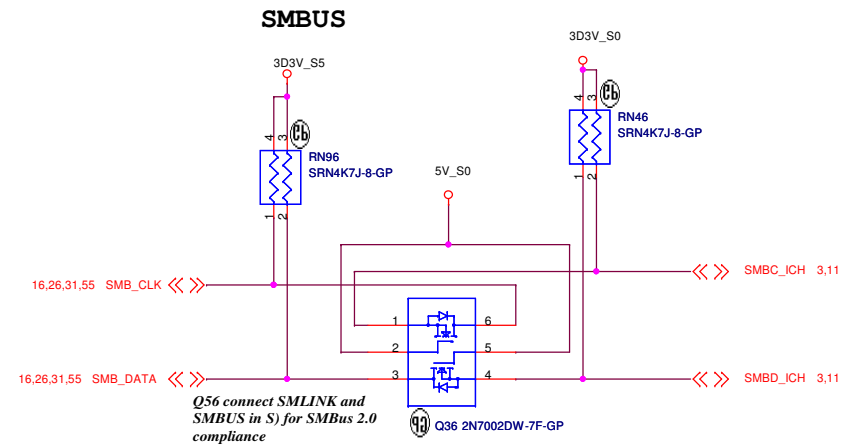
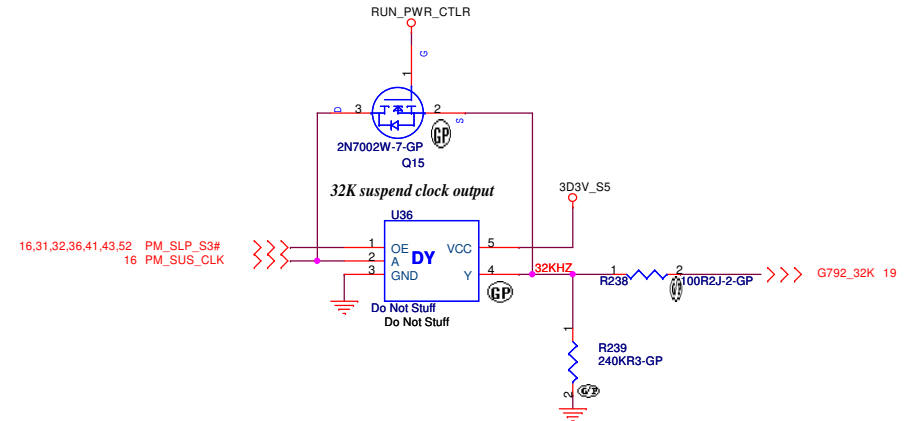
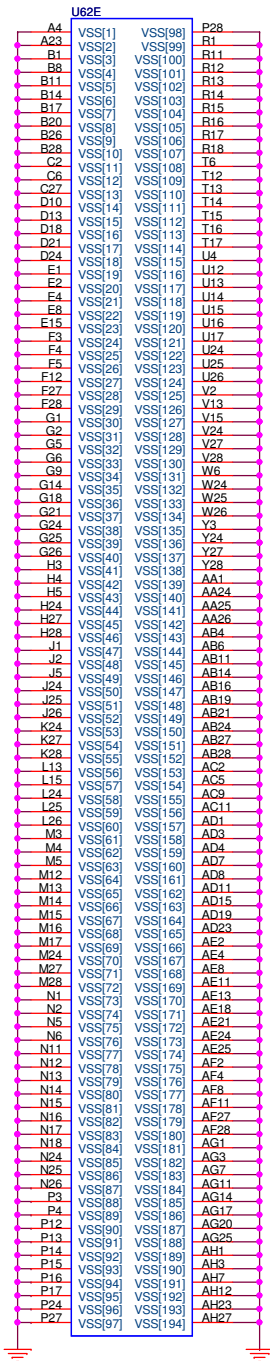
Rev

2

K180101.017



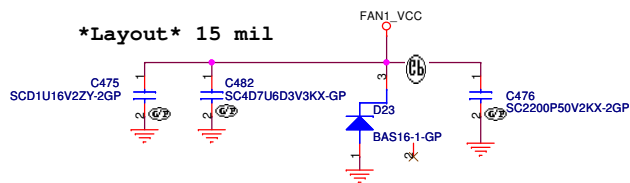




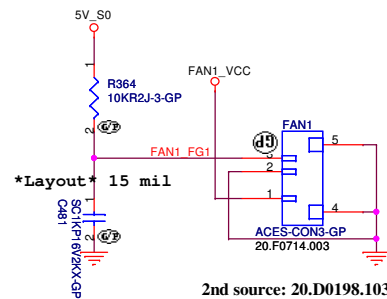
BOM

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
ICH7-M (4 of 4)			
Size A3	Document Number	Rev 2	
AG3			
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***Layout* 15 mil**

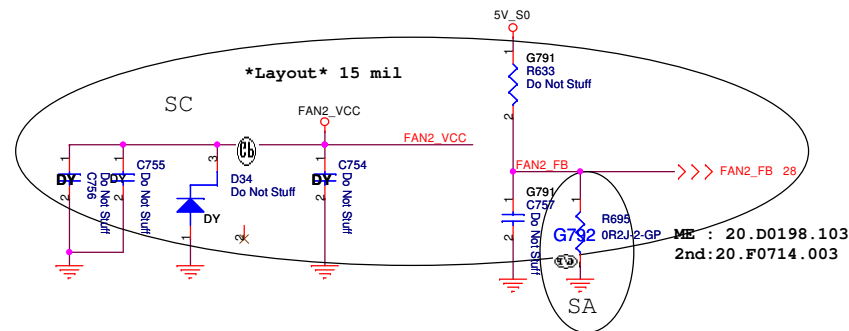


***Layout* 15 mil**



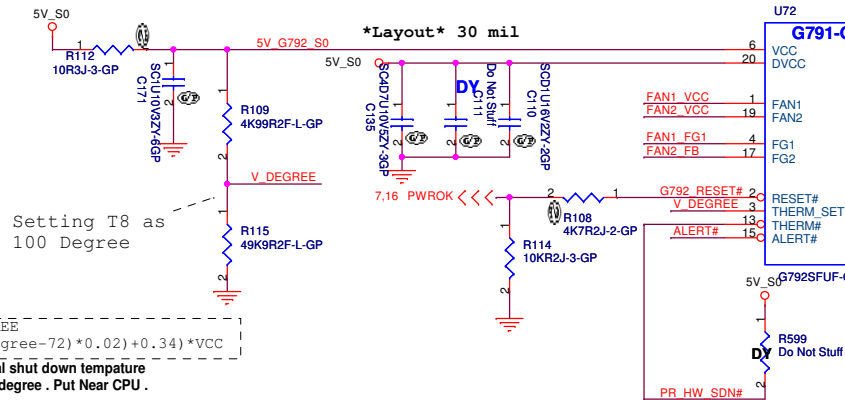
2nd source: 20.D0198.103

***Layout* 15 mil**



ME : 20.D0198.103
2nd: 20.F0714.003

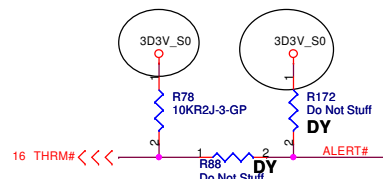
***Layout* 30 mil**



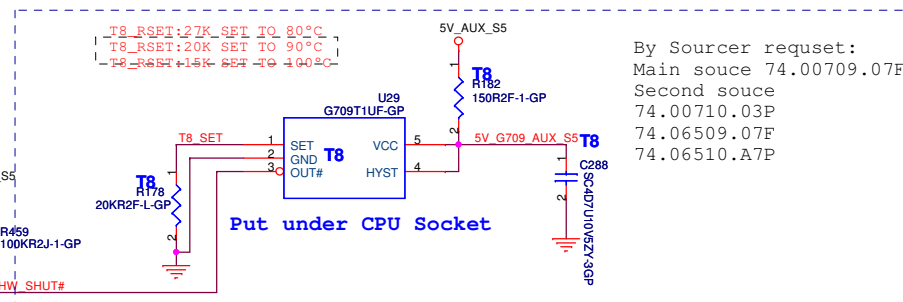
Setting T8 as
100 Degree

V_DEGREE
= (((Degree-72)*0.02)+0.34)*VCC
HW thermal shut down temperature
setting 95 degree . Put Near CPU .

DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree



32.36 PURE_HW_SHUTDOWN# <<<



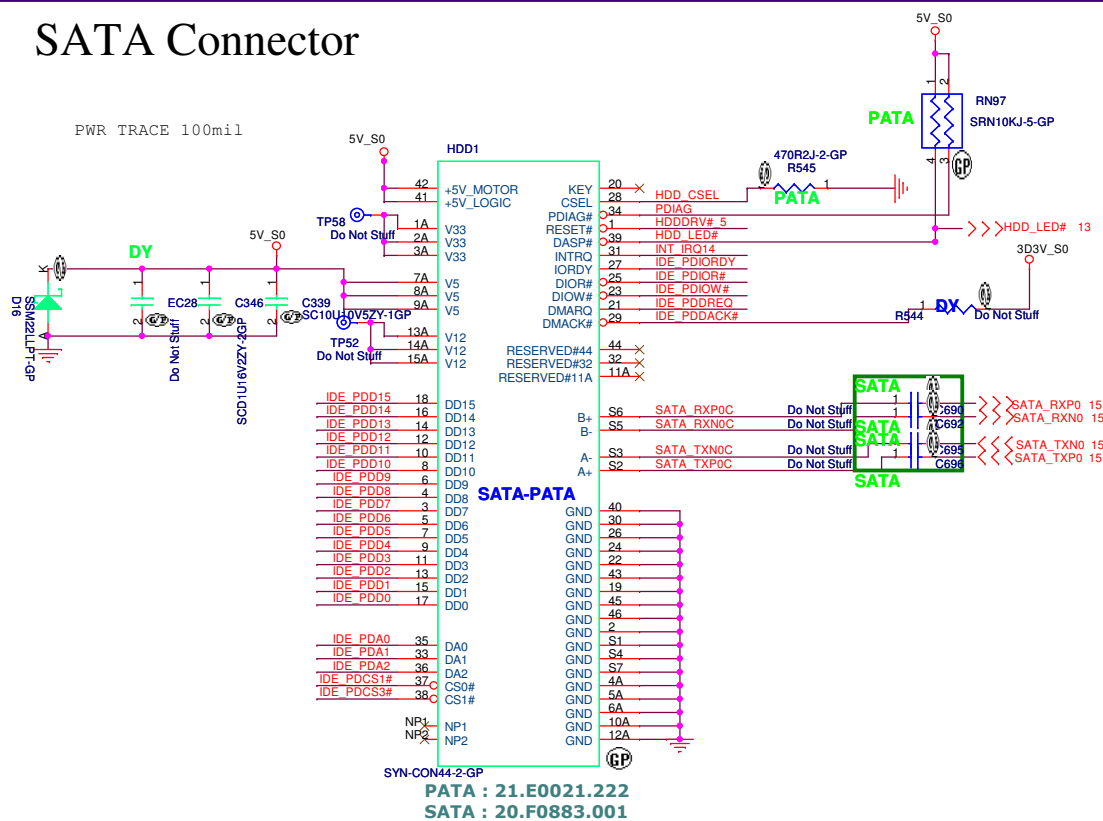
Put under CPU Socket

By Sourcer request:
Main souce 74.00709.07F
Second souce
74.00710.03P
74.06509.07F
74.06510.A7P

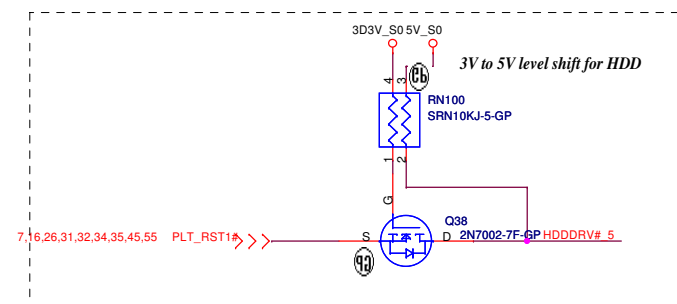
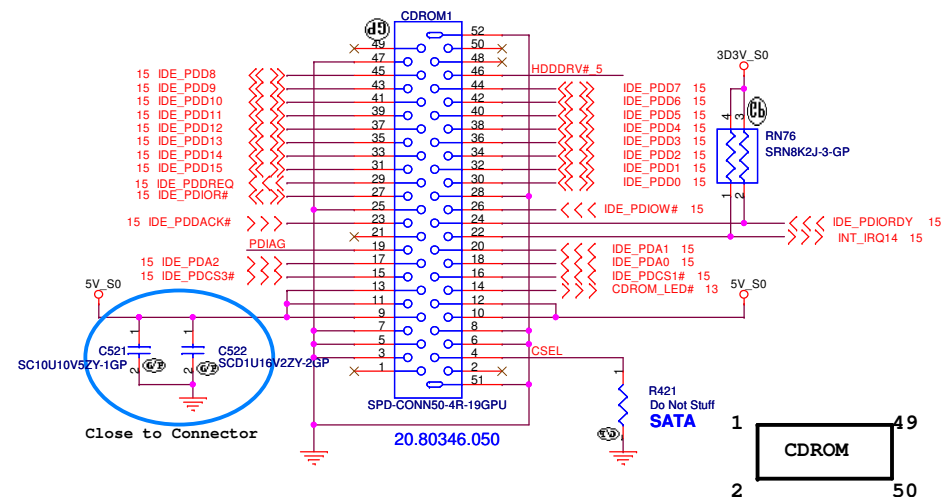
BOM

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		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Thermal/Fan Controller G792</i>			
Size	Document Number	Rev	
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SATA Connector



CDROM Connector



BOM

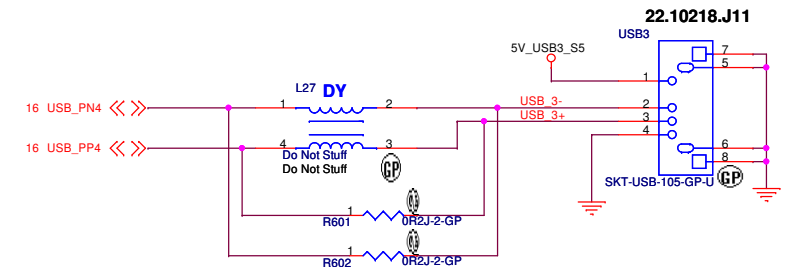
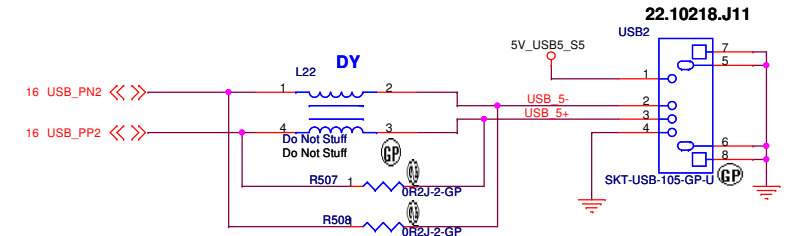
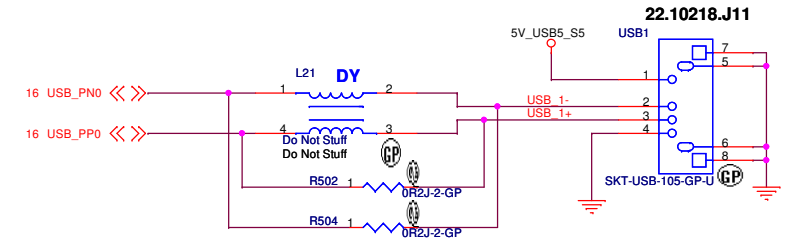
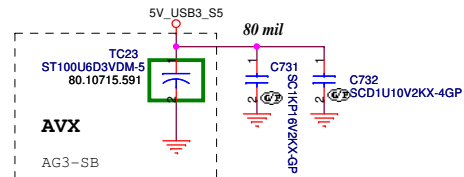
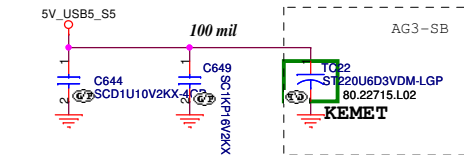
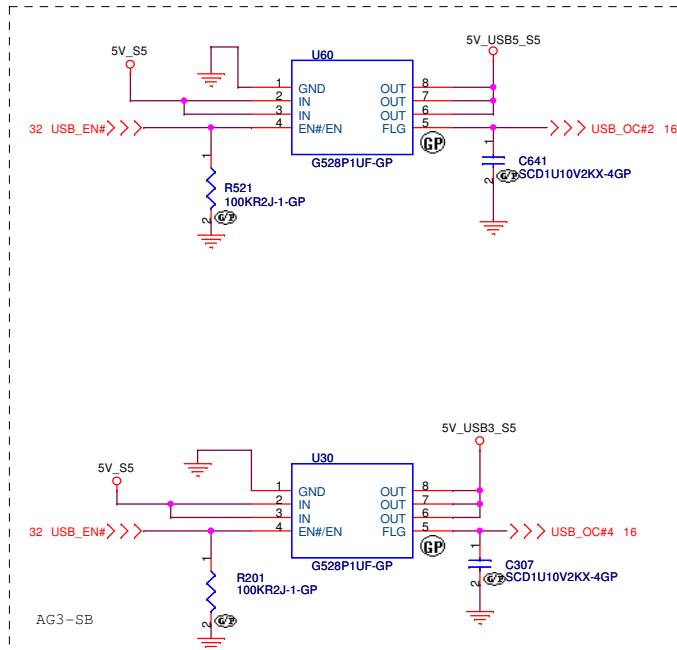
緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

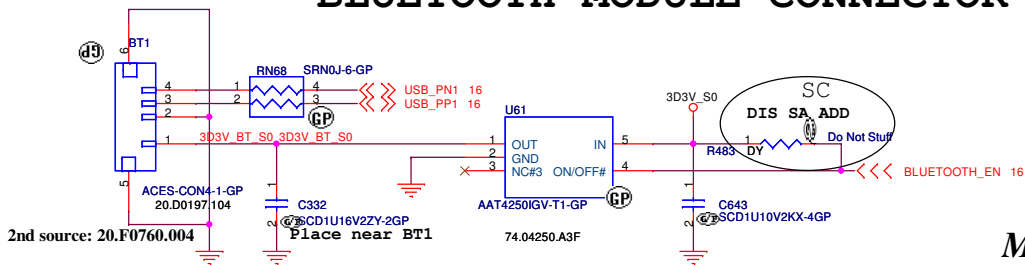
Title	SATA/PATA HDD / ODD
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Size A3	Document Number AG3	Rev 2
Date: Thursday, April 20, 2006		Sheet 20 of 55

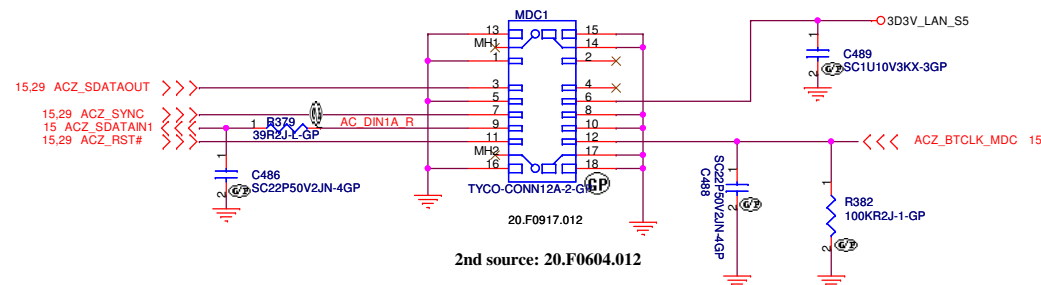
USB PORT



BLUETOOTH MODULE CONNECTOR



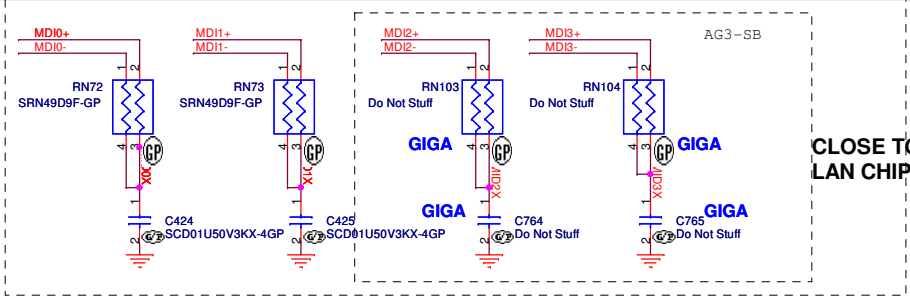
MDC 1.5 CONN



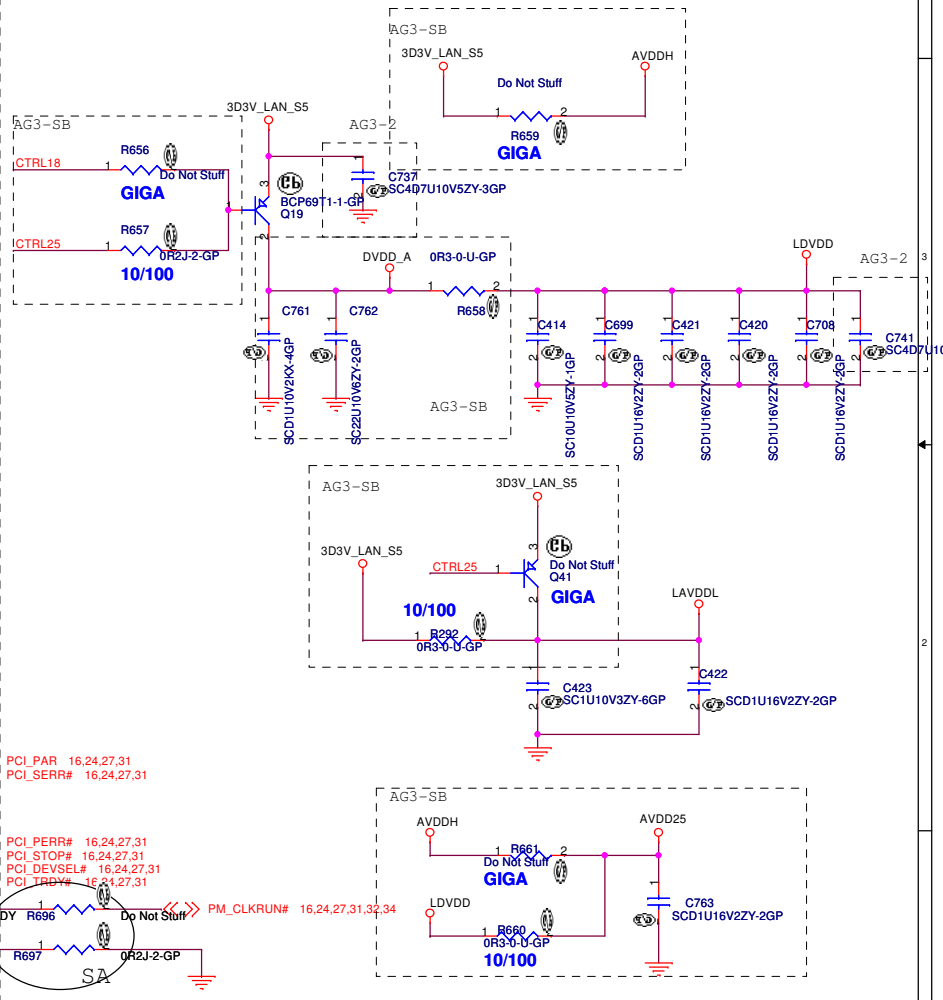
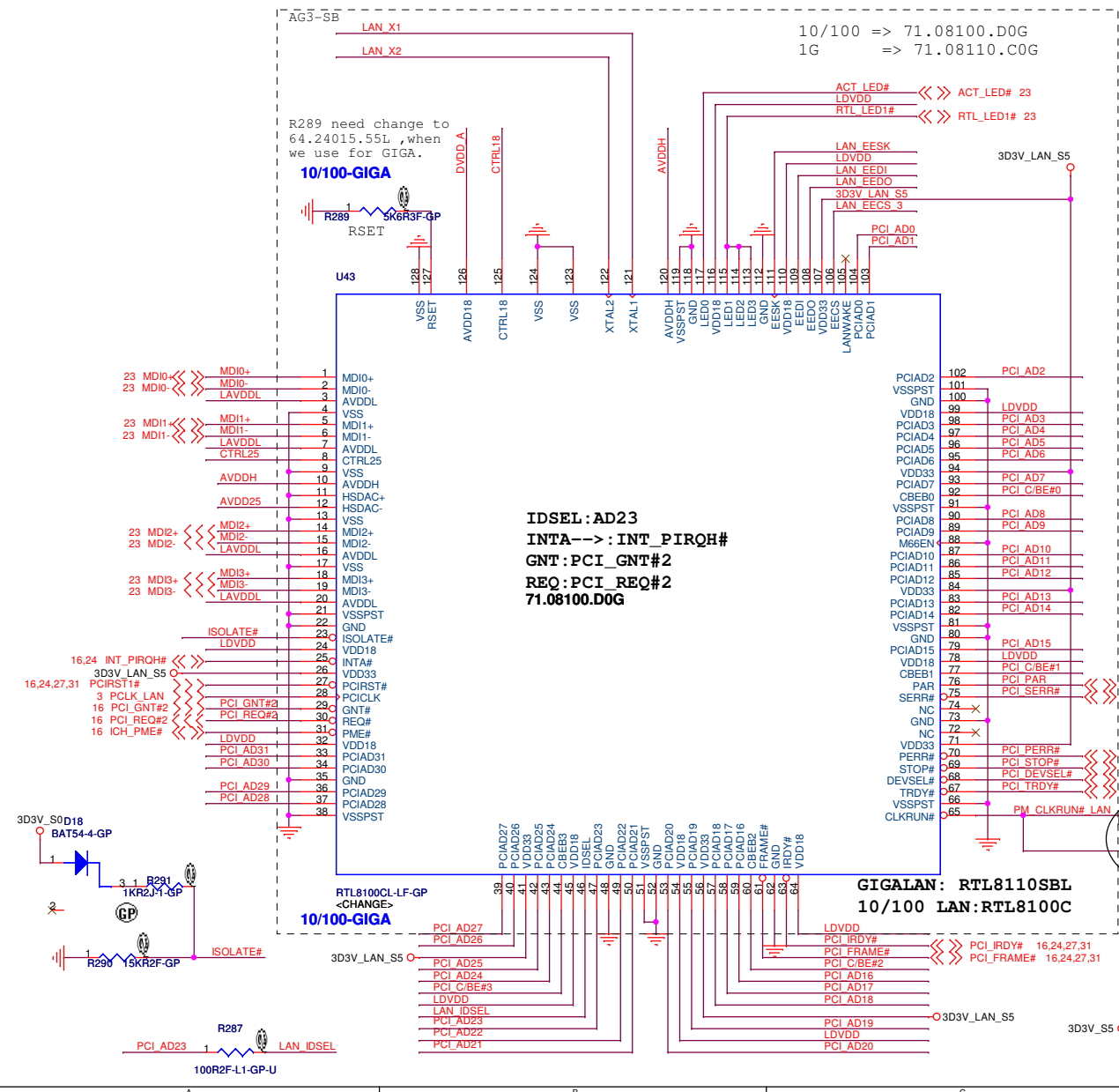
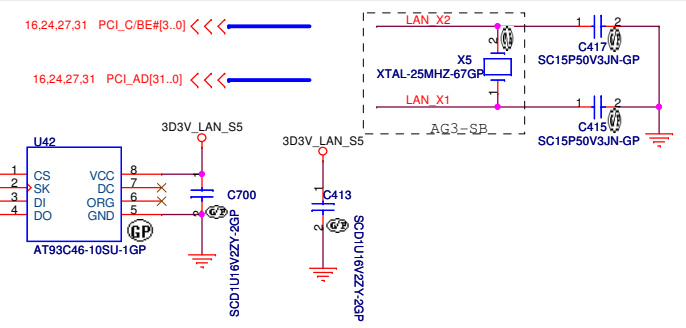
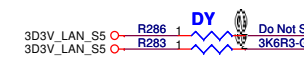
BOM

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Taipei Hsien 221, Taiwan, R.O.C.

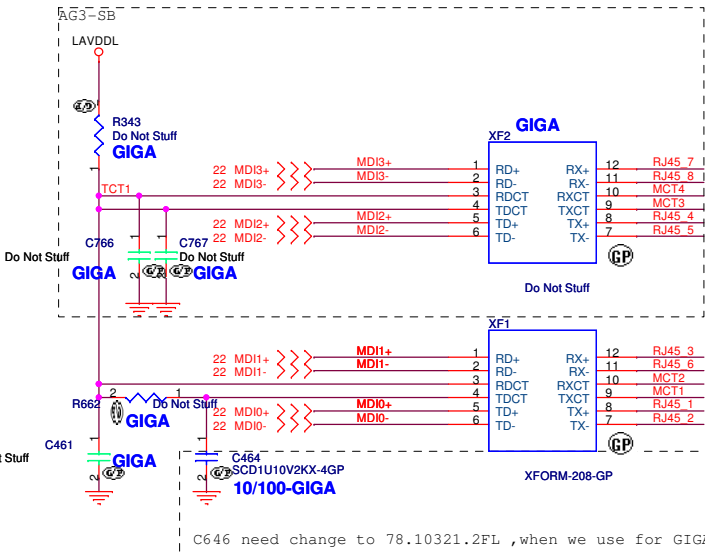
Title			
USB and MDC I/F			
Size	Document Number	Rev	
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EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)



PIN NAME	8110SBL (Giga)	8100CL (10/100)	SIGNAL NAME
VDD33	3.3	3.3	3D3V_LAN_S5
AVDDH	3.3	N.C.	AVDDH
VDD18	1.2	2.5	DVDD
AVDD18	1.2	2.5	DVDD_A
AVDDL	2.5	3.3	AVDDL
V_12P	3.3	2.5	V_12P



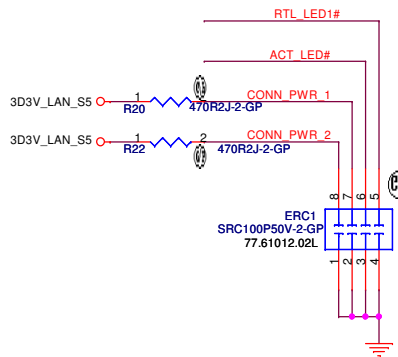
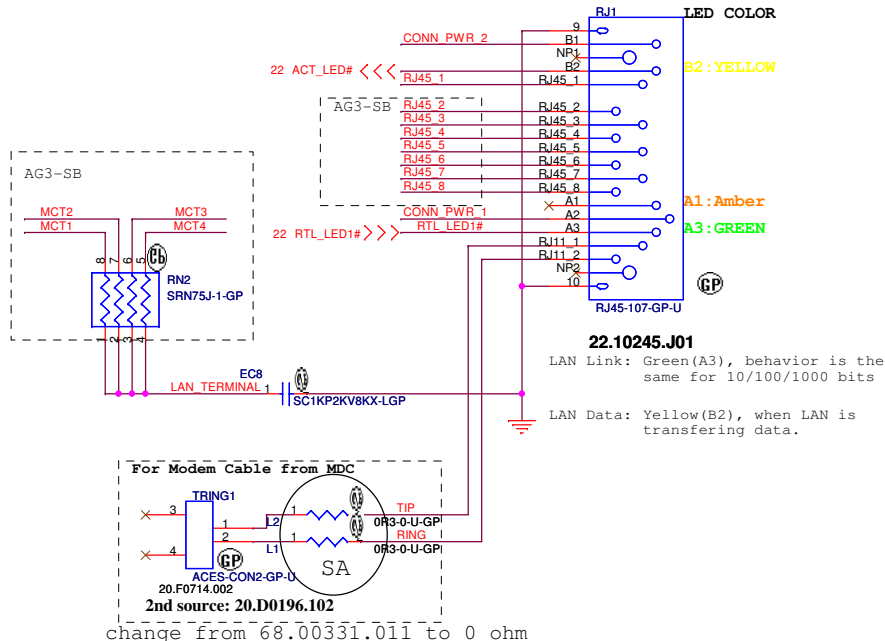
1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

LAN Connector



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Title

LAN Connector

Size
A3

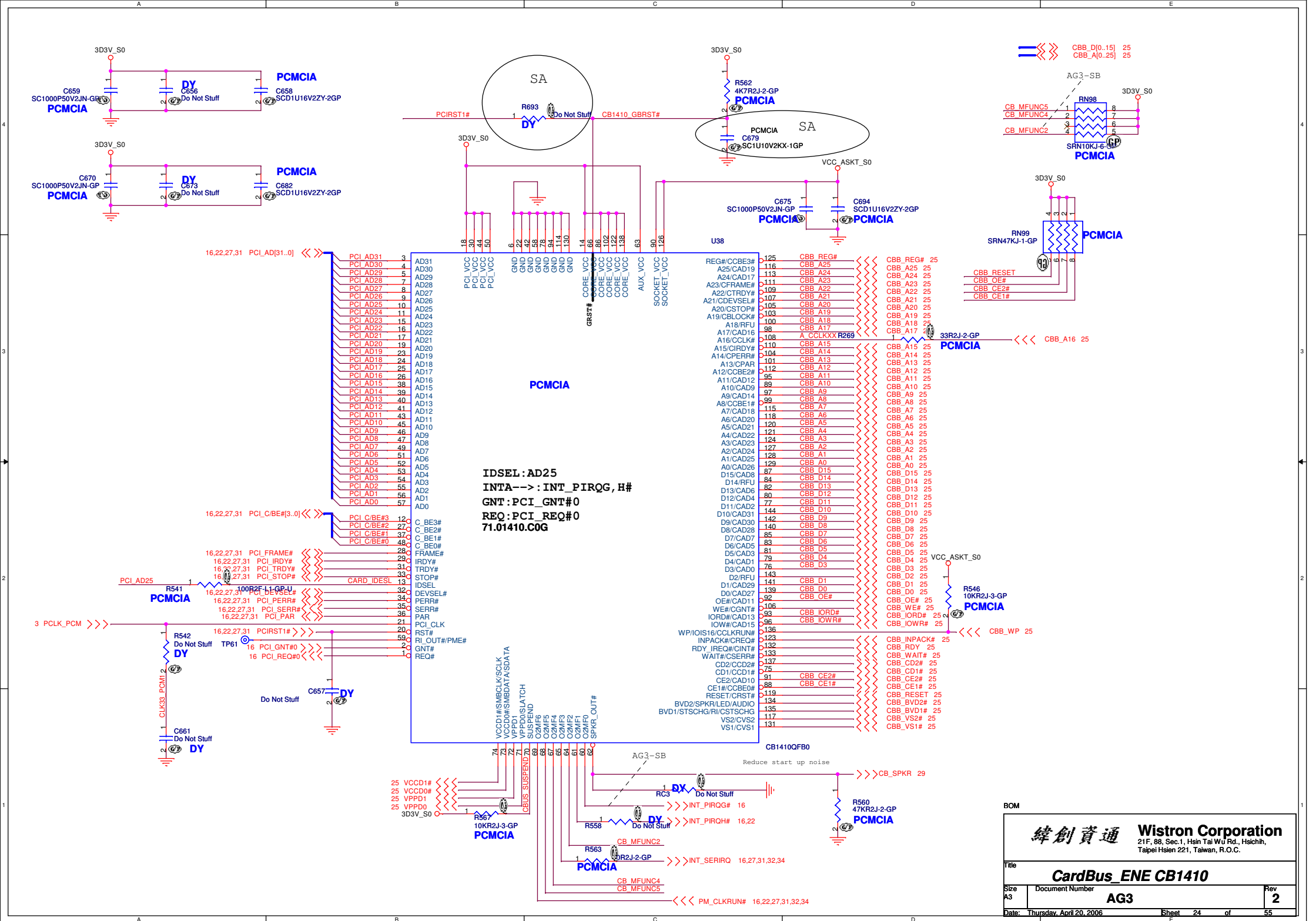
Document Number

AG3

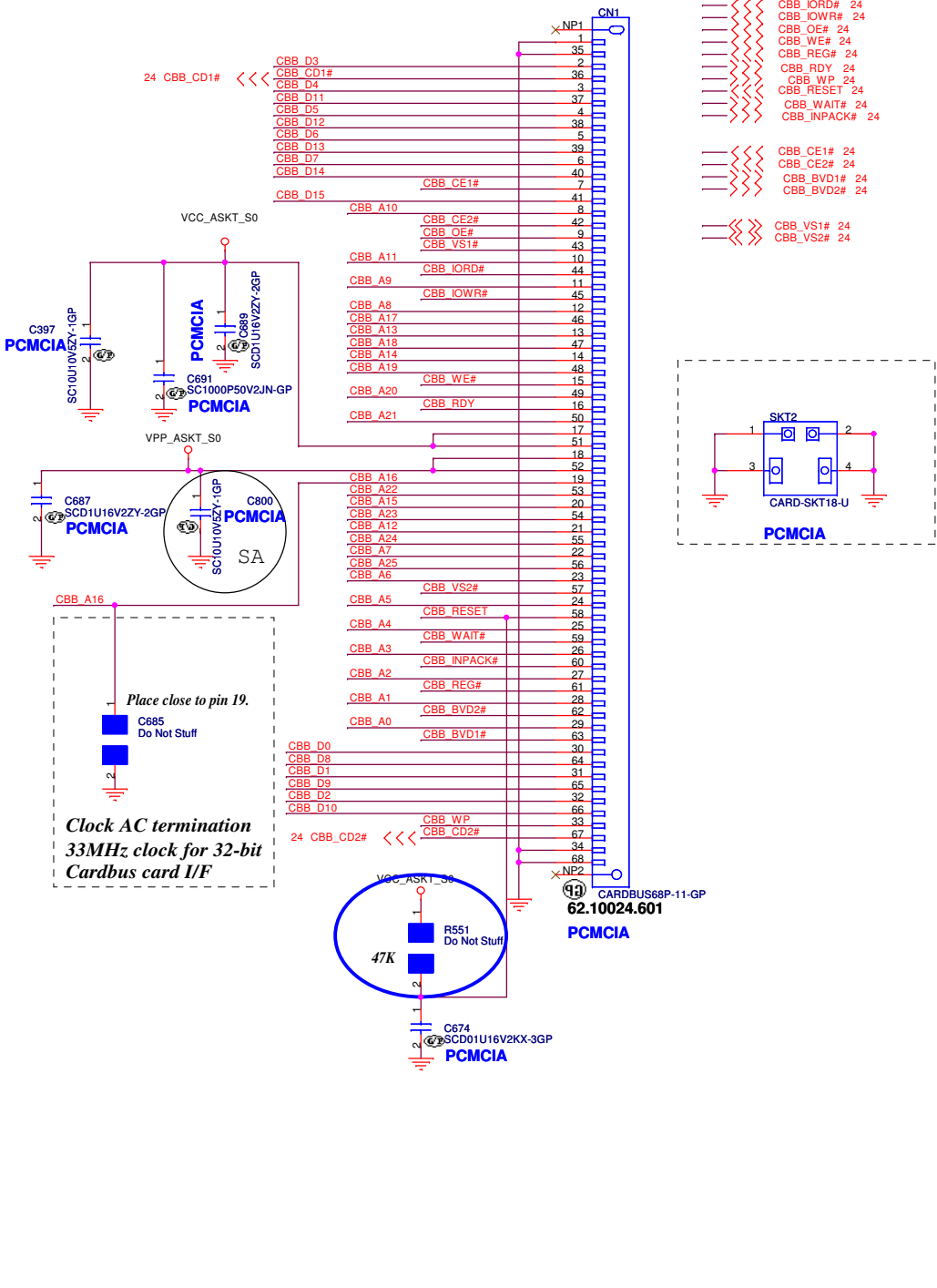
Date: Thursday, April 20, 2006

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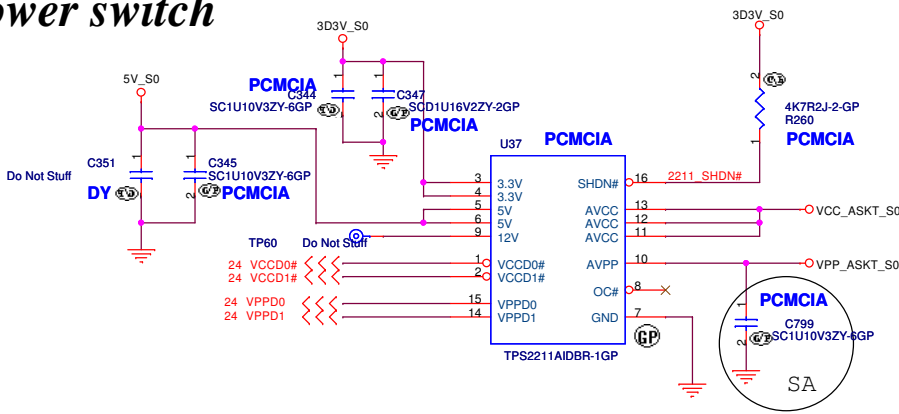
Rev	2
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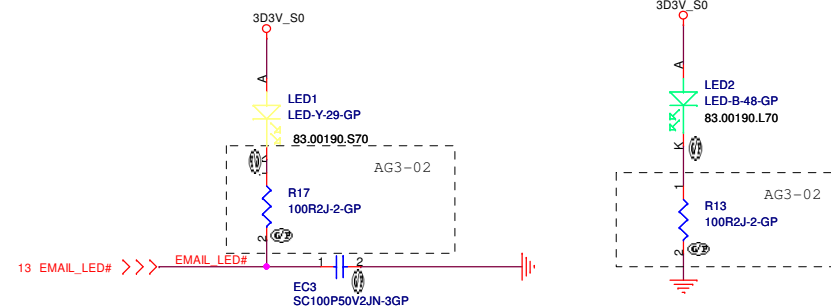
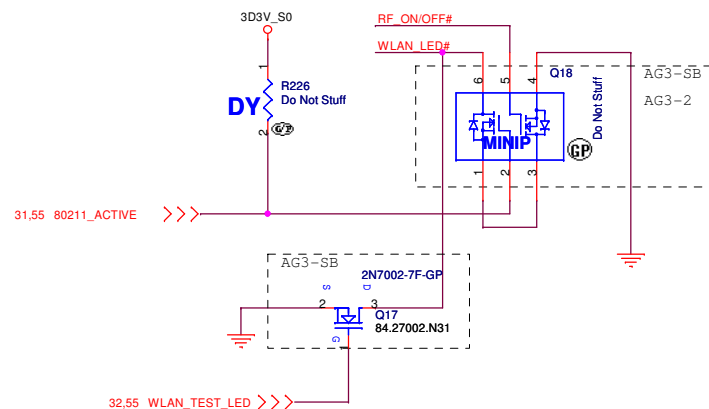
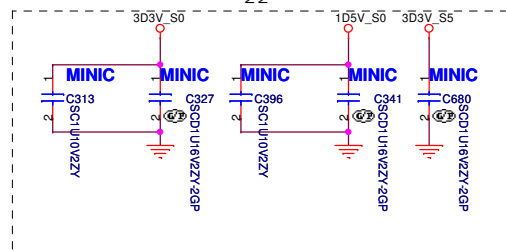
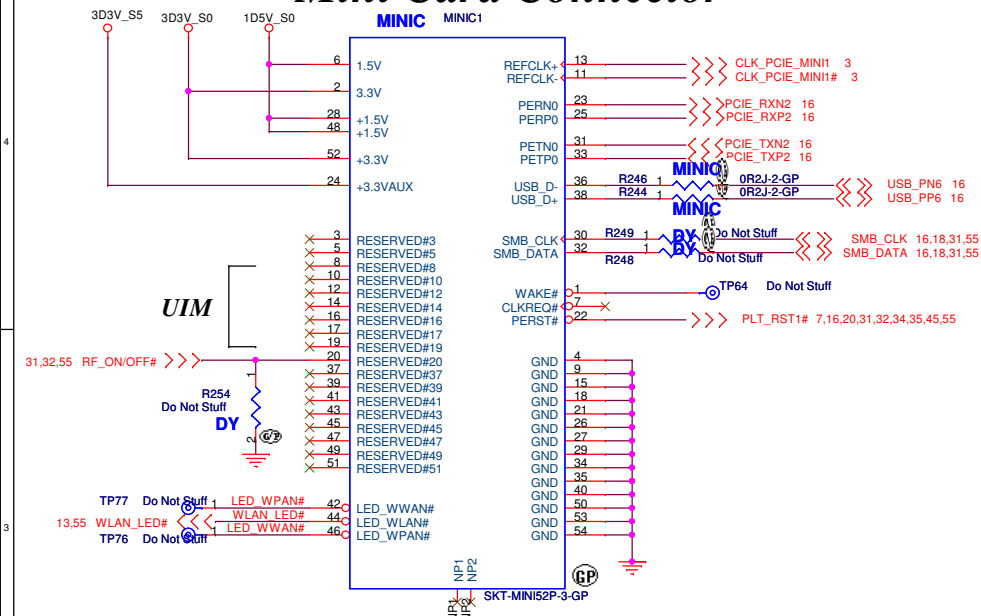
PCMCIA Socket



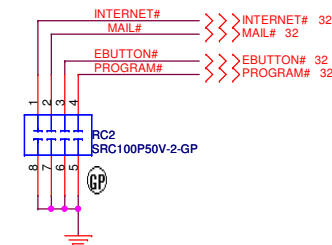
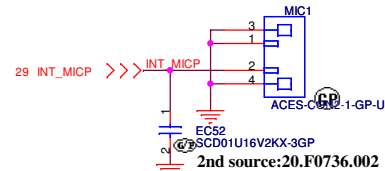
Power switch



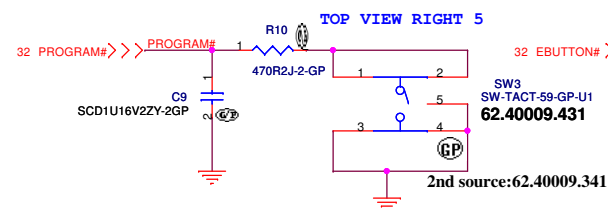
Mini Card Connector



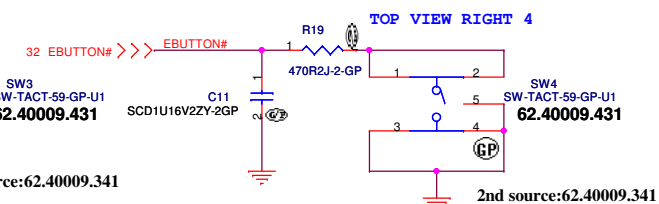
Internal Microphone



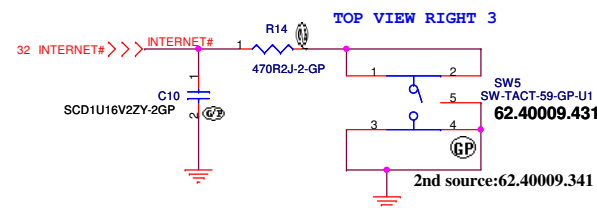
Program Button



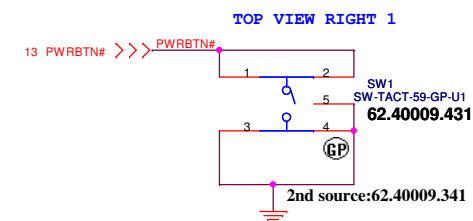
E-Button



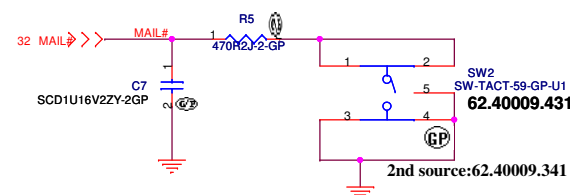
Internet Button

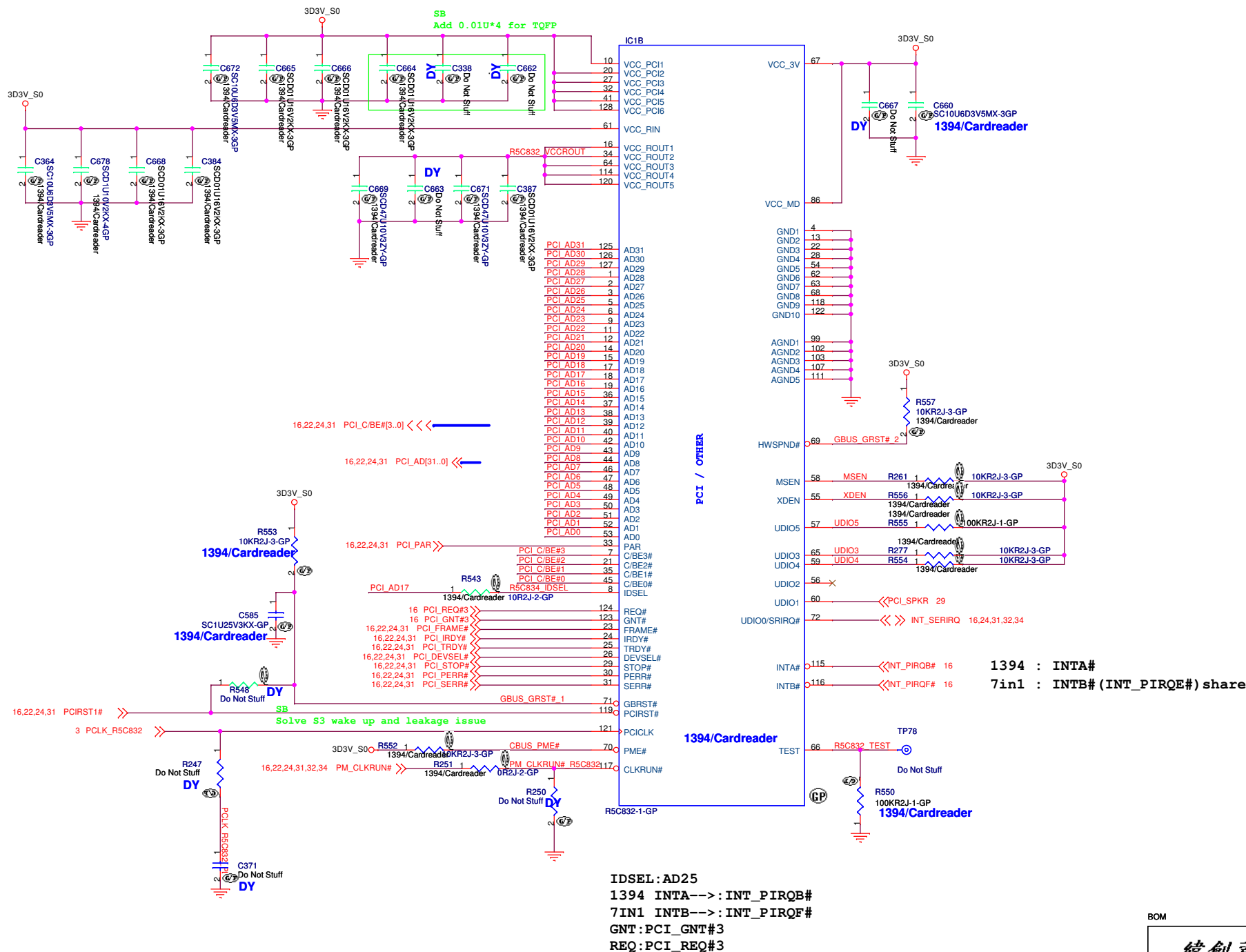


Power Button

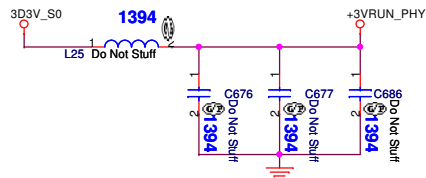
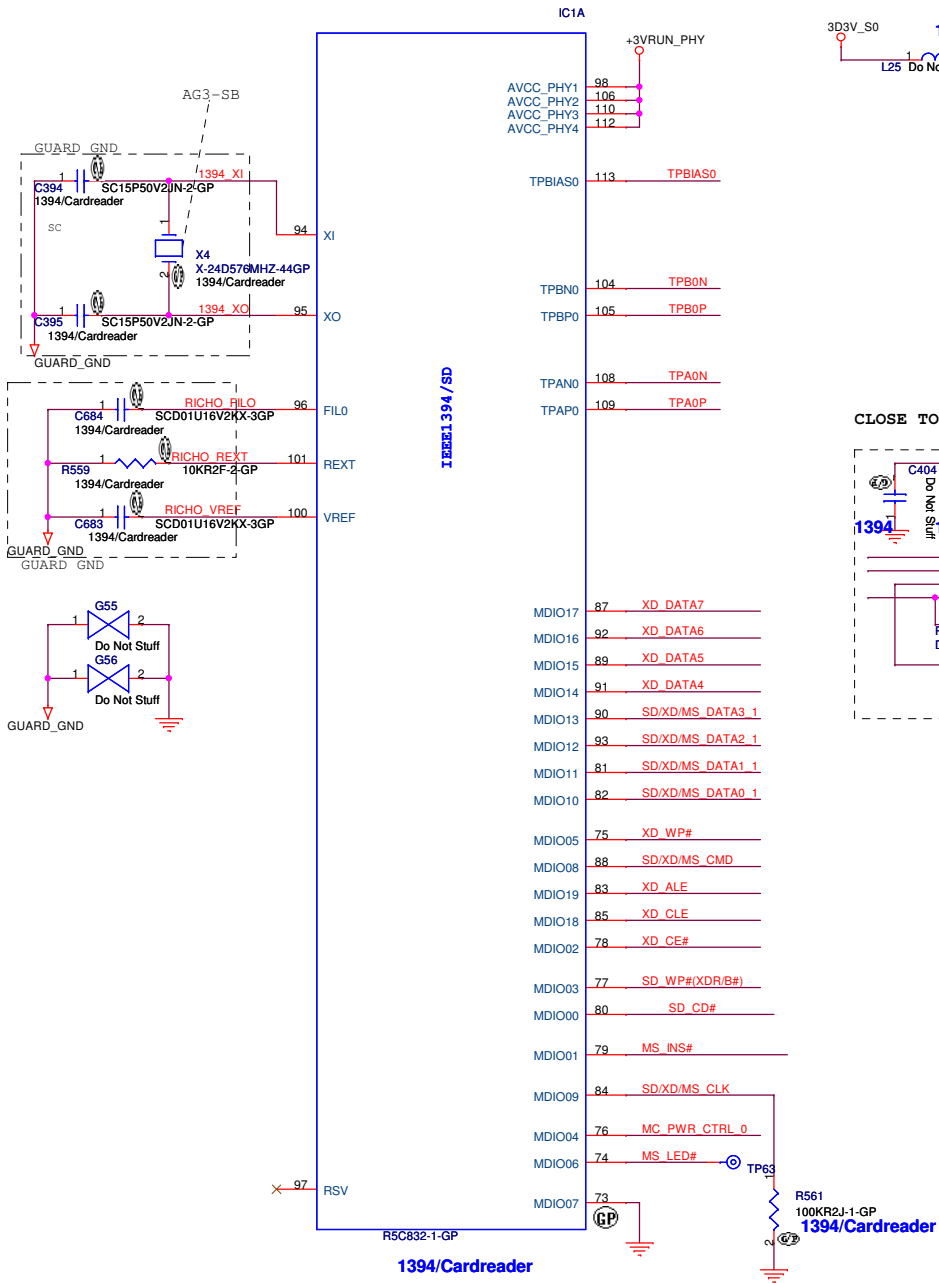


Mail Button
TOP VIEW RIGHT 2

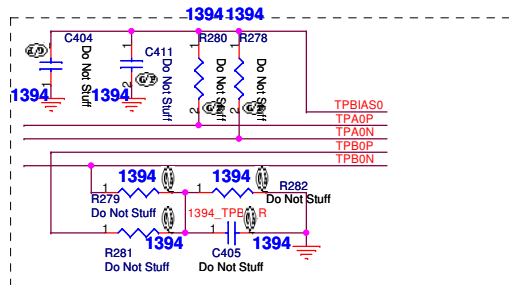




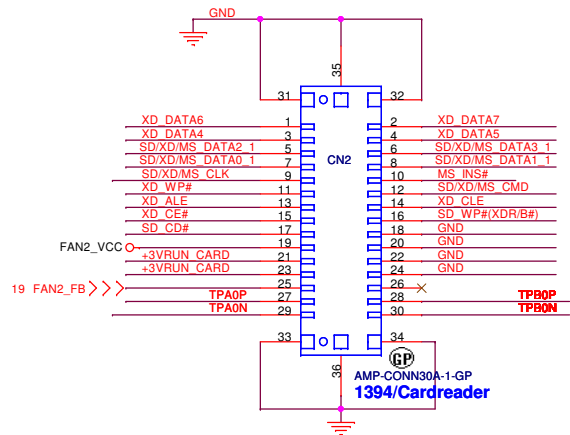
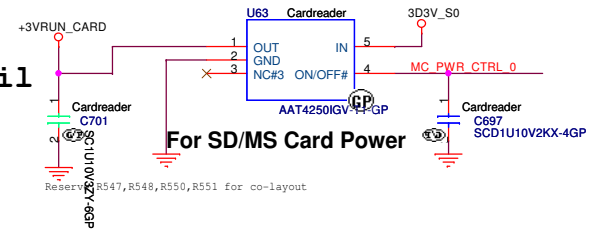
BOM



CLOSE TO CHIP

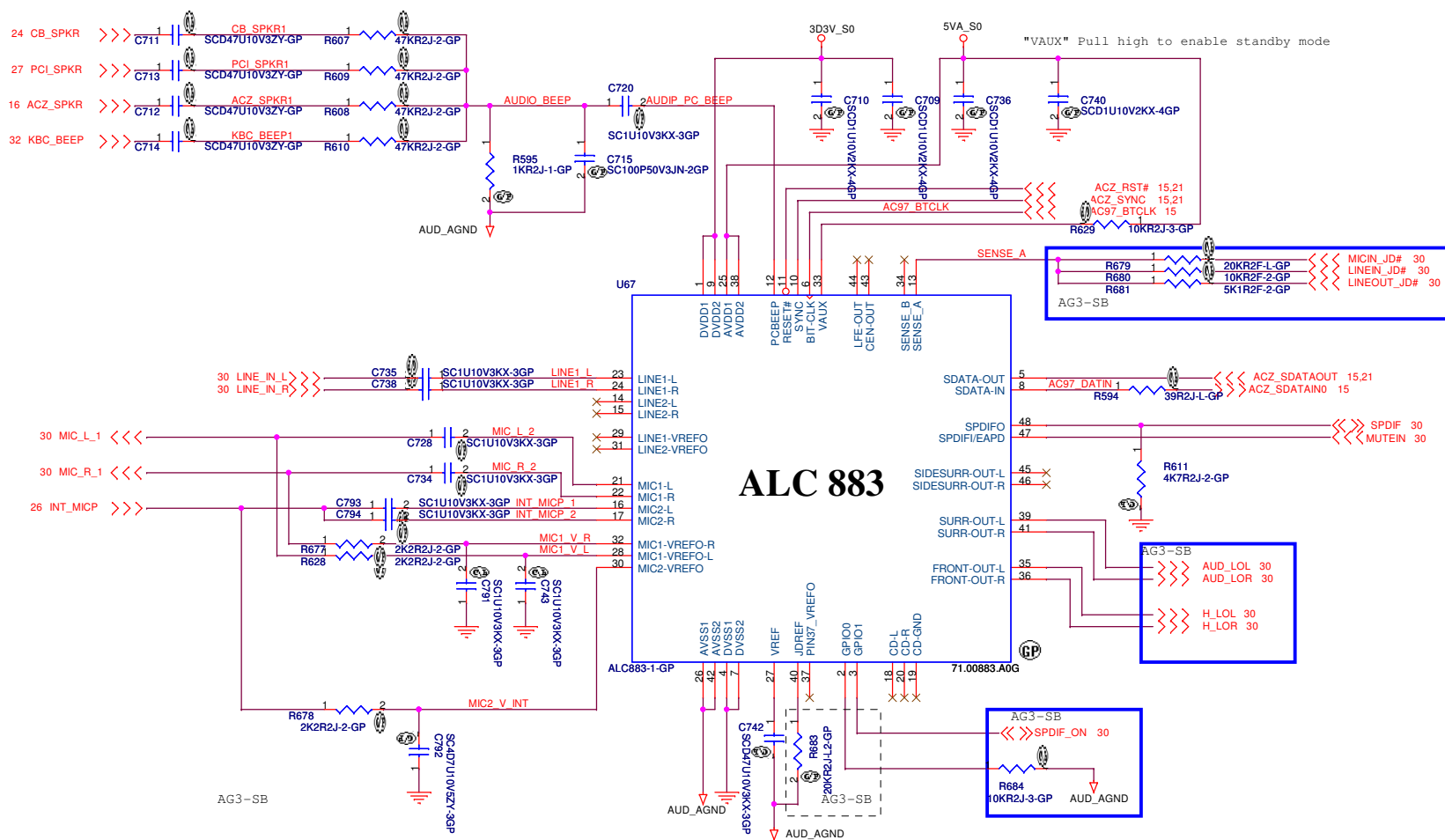


20mi1



BOM

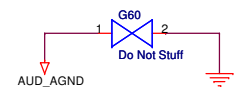
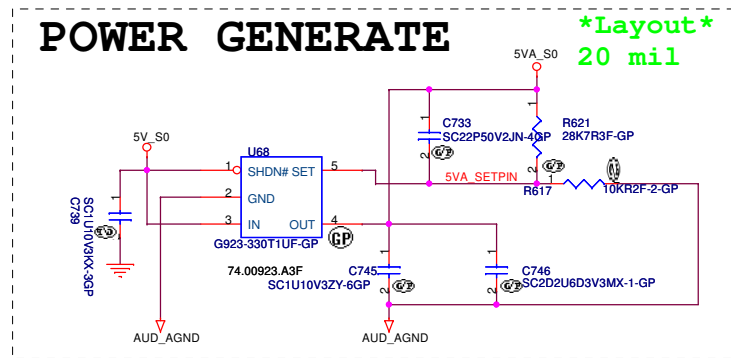
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title R5C832_1394_7IN1(2/2)		
Size A3	Document Number AG3	Rev 2
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1) When GPIO0 is asserted, AMP should be muted.
 2) SPDIFO should be turned off when not used.

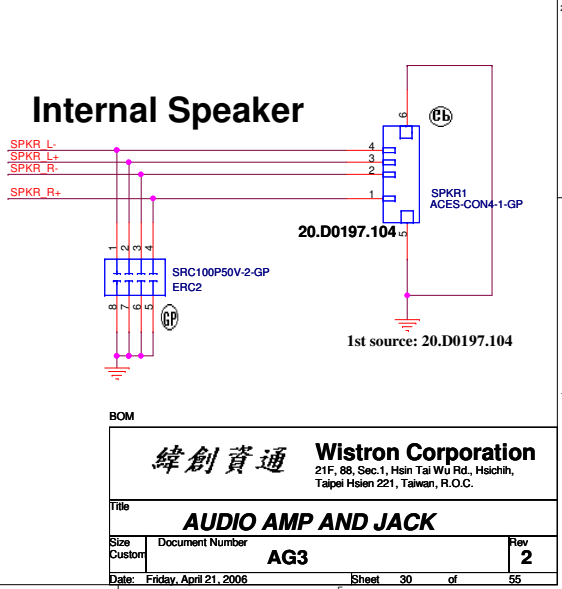
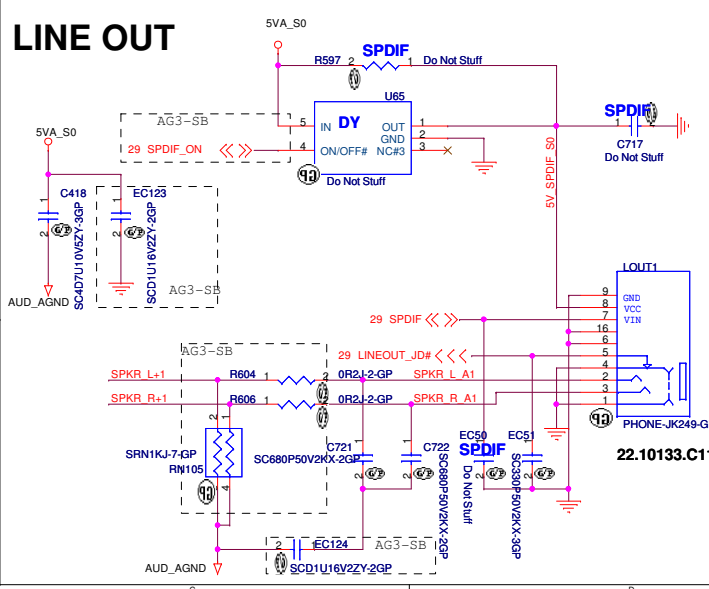
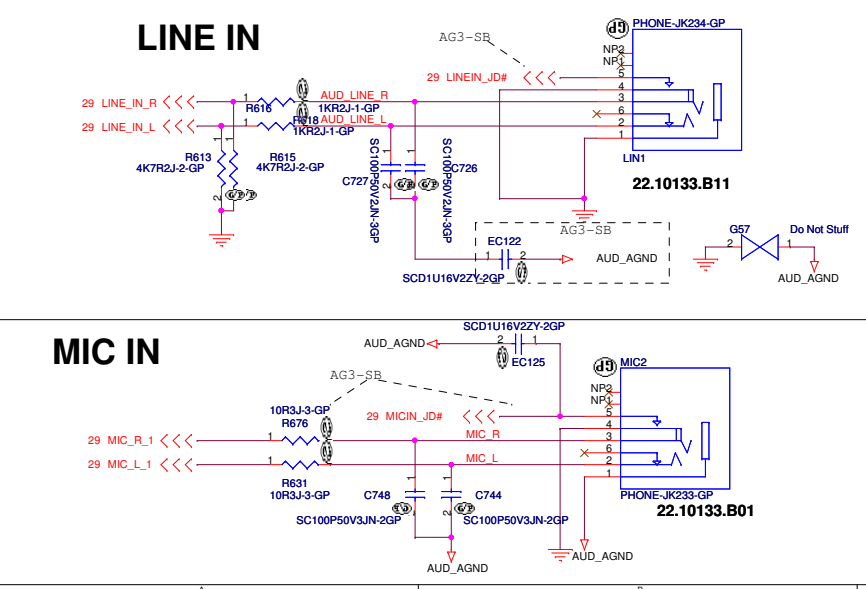
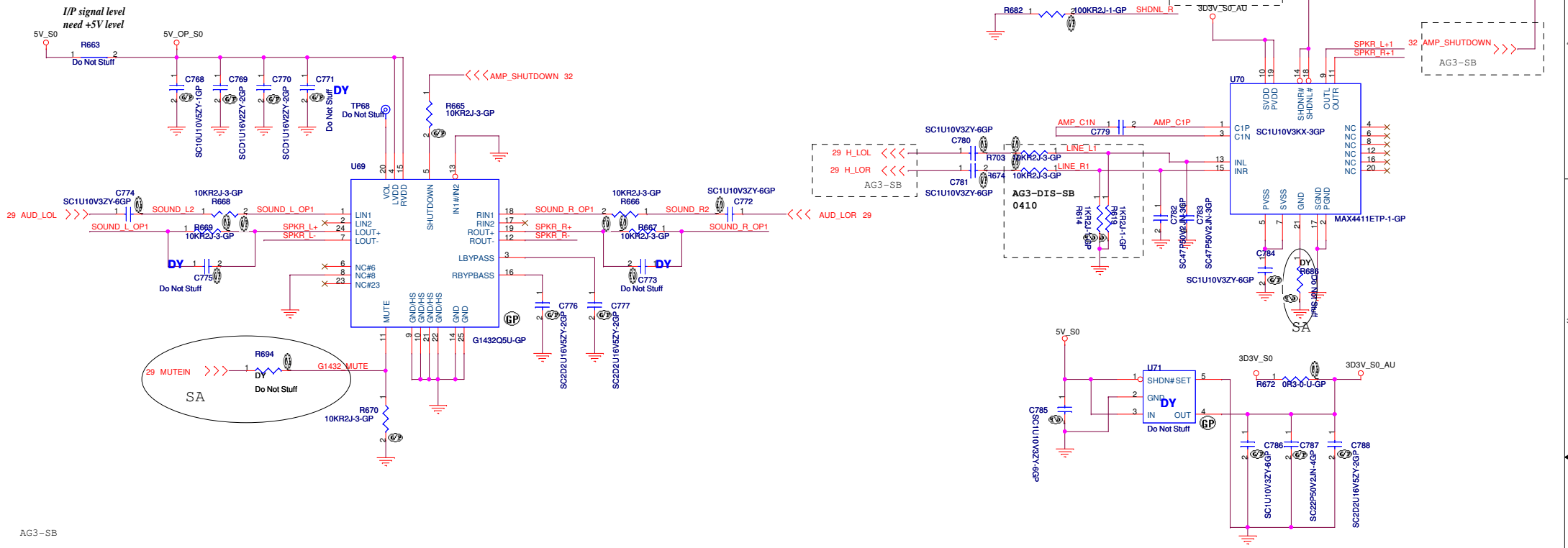
Configuration:
 (3 External Jacks, 1 internal Mic, 1 stereo output Speaker Amp.

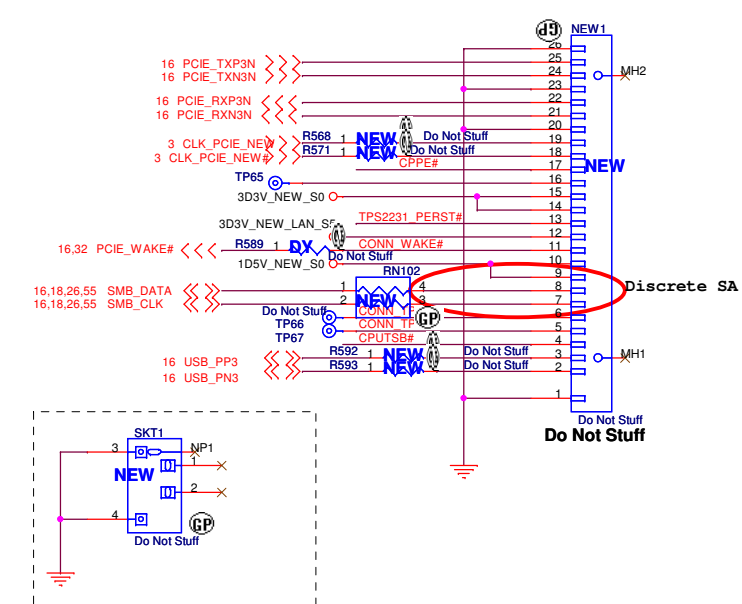
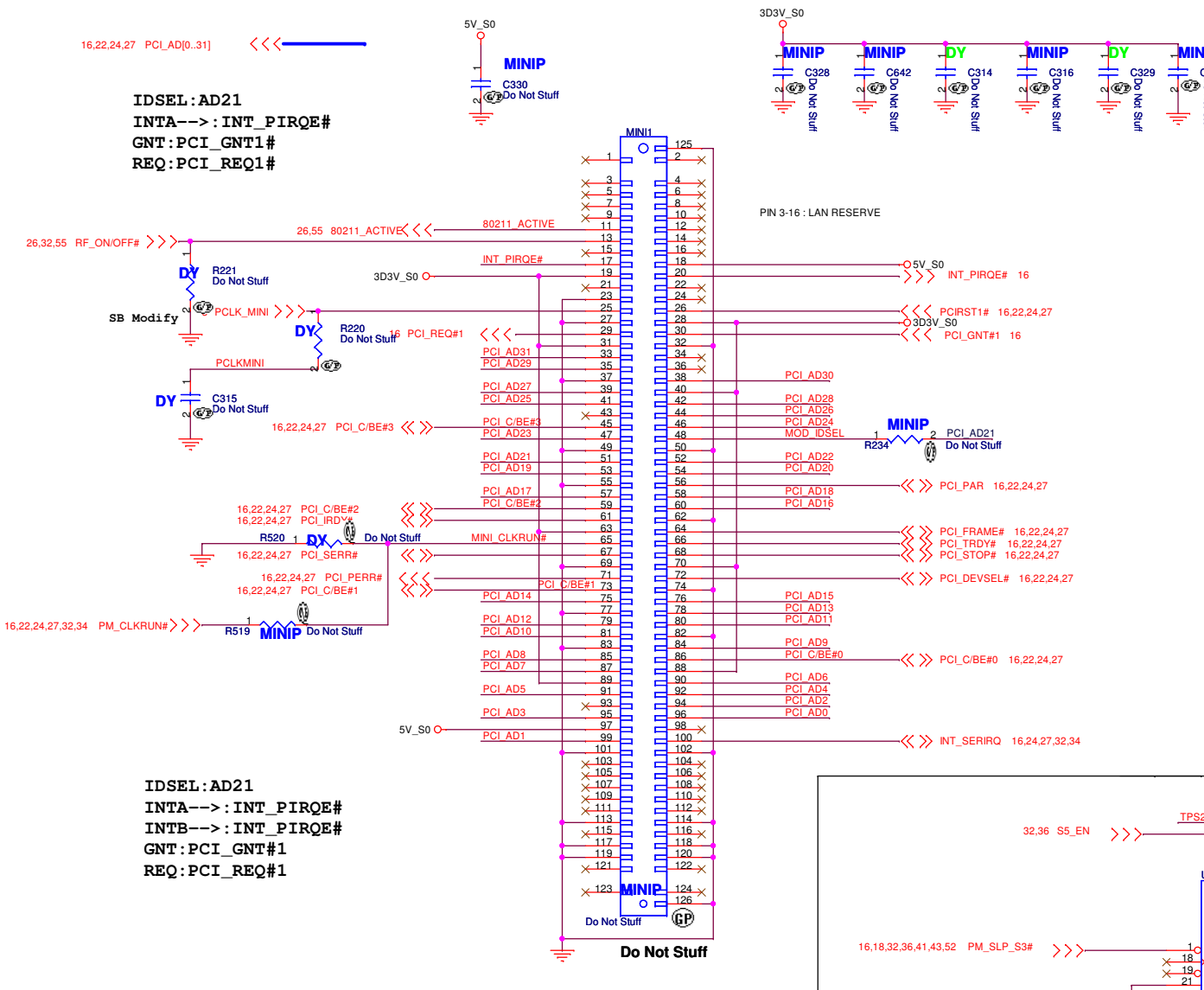
Pin	Symbol	Location	Re-tasking
35/36	FRONT	AMP, Jack1	AMP output, line input
39/41	SURR	X	X
43/44	CEN/LEFT	X	SURR-VREFO-L/R
45/46	SIDESURR	X	SIDESURR-L is MIC2-VREFO-R, SIDESURR-R is LINE2-VREFO-R
23/24	LINE1	Jack 2	Line input, line output
21/22	MIC1	Jack 3	Mic input, line output
14/15	LINE2	X	X
16/17	MIC2	Int. Mic	Mic input



BOM

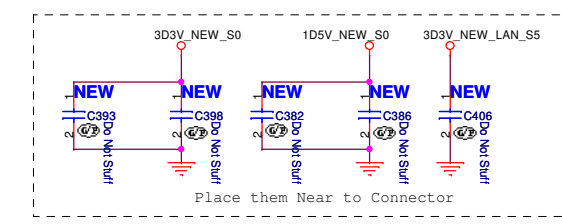
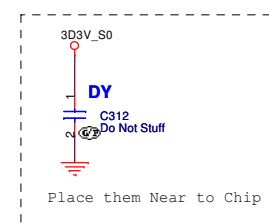
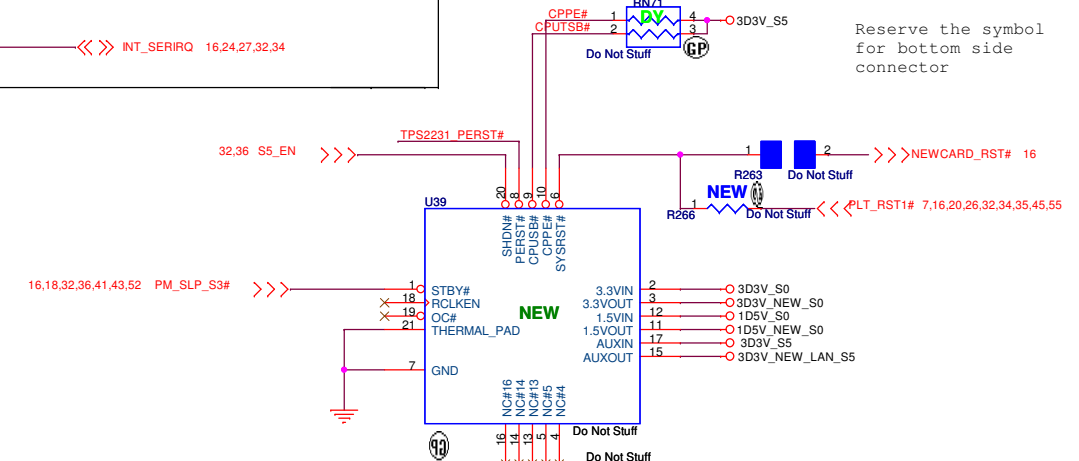
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Azalia codec ALC883	
Size A3	Document Number AG3
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NEWCARD Connector

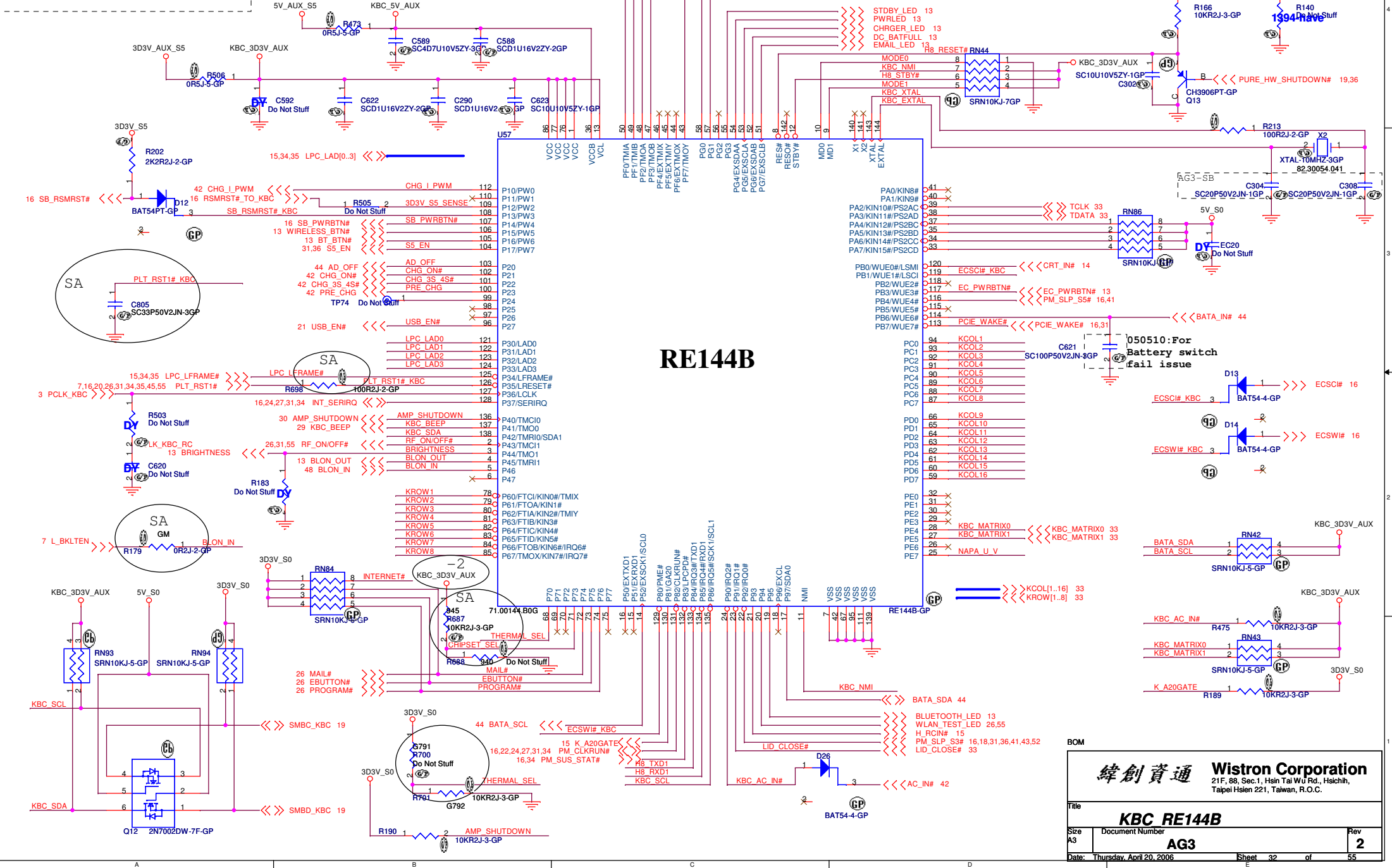
Reserve the symbol
for bottom side
connector



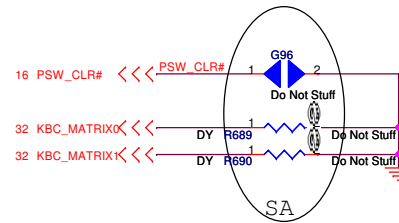
BOM			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
File			
AG3			
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For S/W Debug

Pin No.			Pin No.
1	3D3V_AUX_KBC		
		TP24	MODE1
3	H8 RESET#	TP48	MODE0
		TP31	
5	KBC_AC_IN#	TP73	H8_TXD1
		TP29	
7	LID_CLOSE#	TP19	H8_RXD1
		TP36	
9	PM_SLP_S3#	TP20	GND
			10



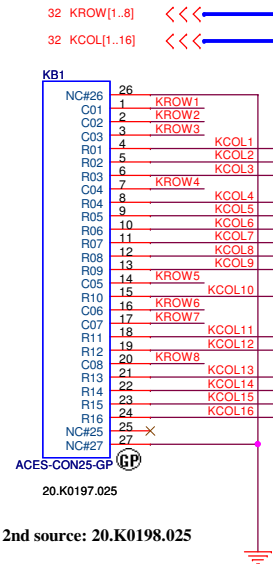
Internal KeyBoard Connector



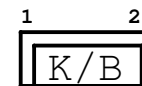
Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

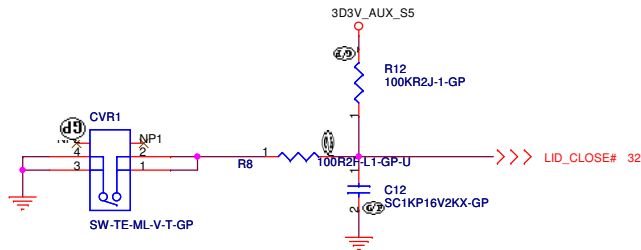
	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON



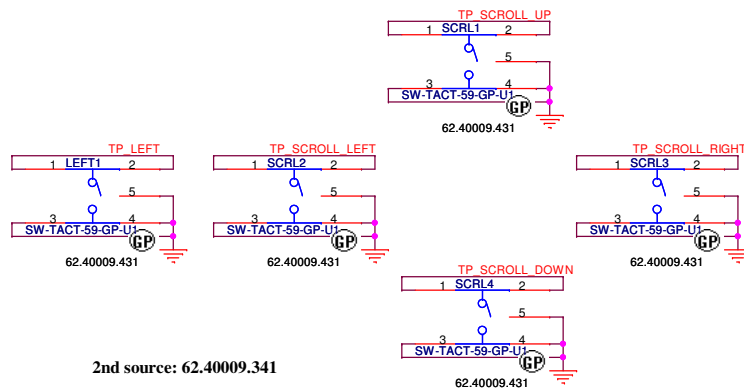
2nd source: 20.K0198.025



COVER SWITCH

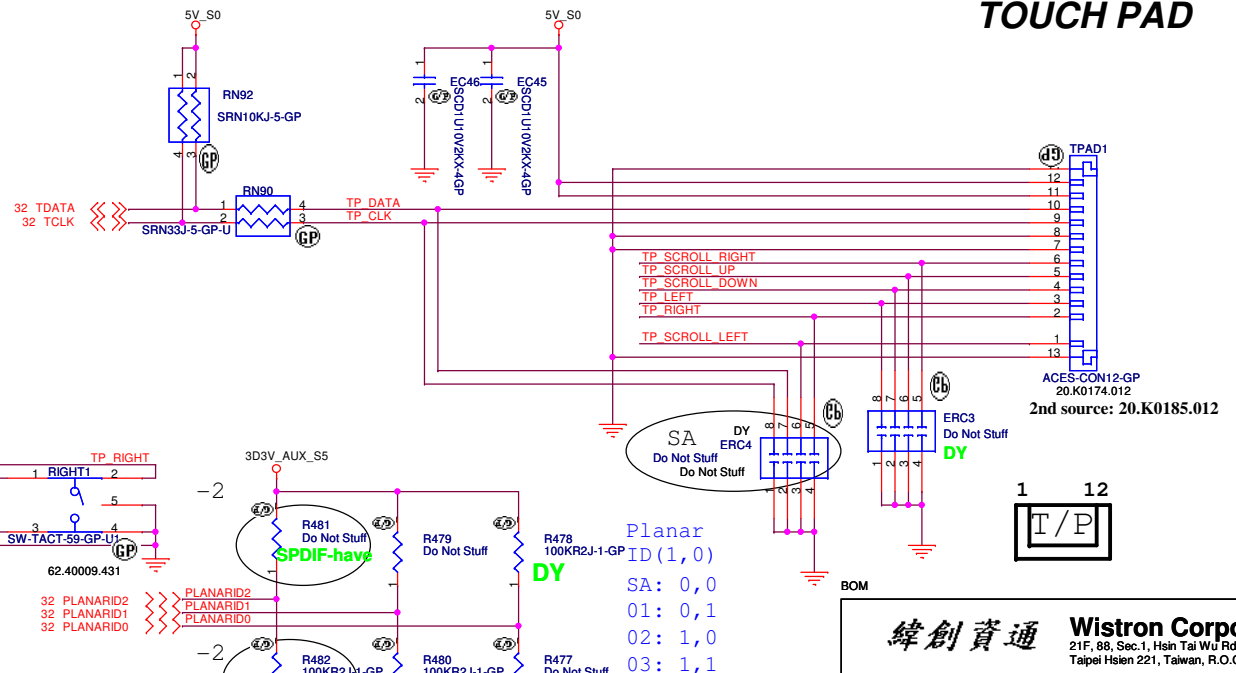


SCROLL KEY

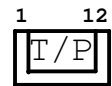


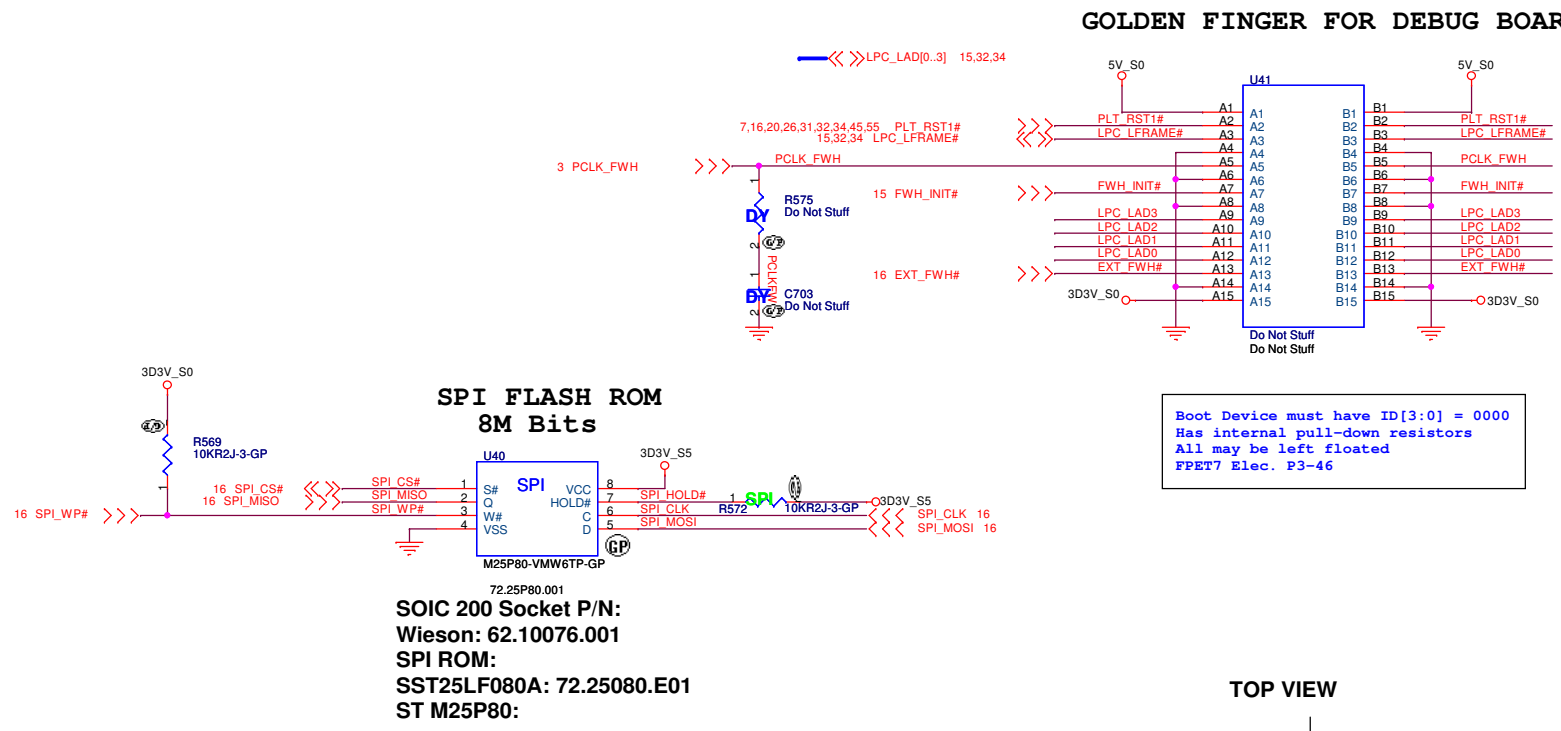
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TOUCH PAD

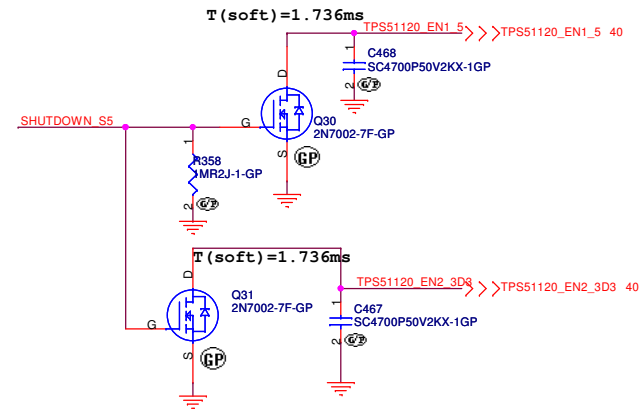
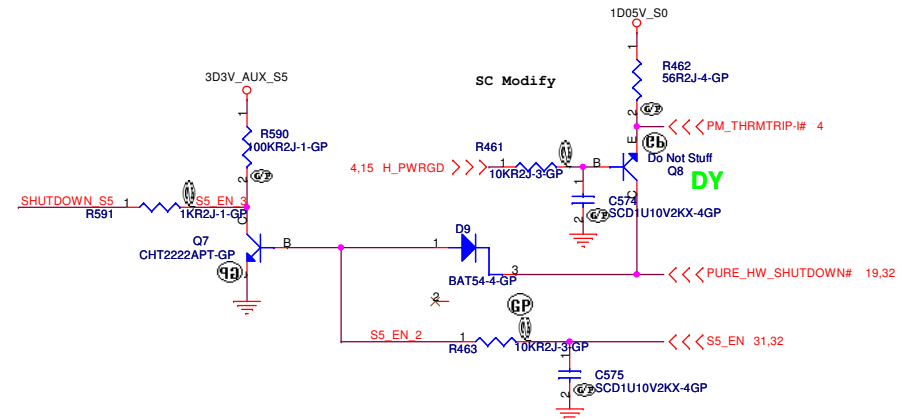
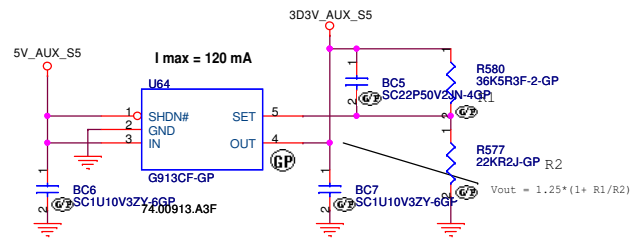
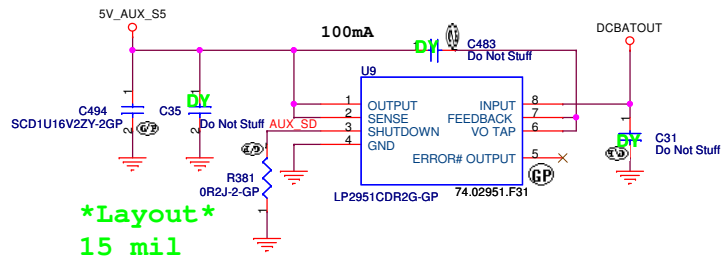


2nd source: 20.K0185.012

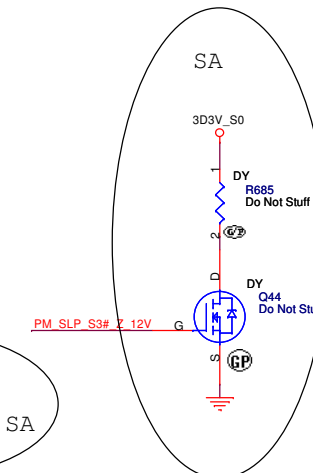
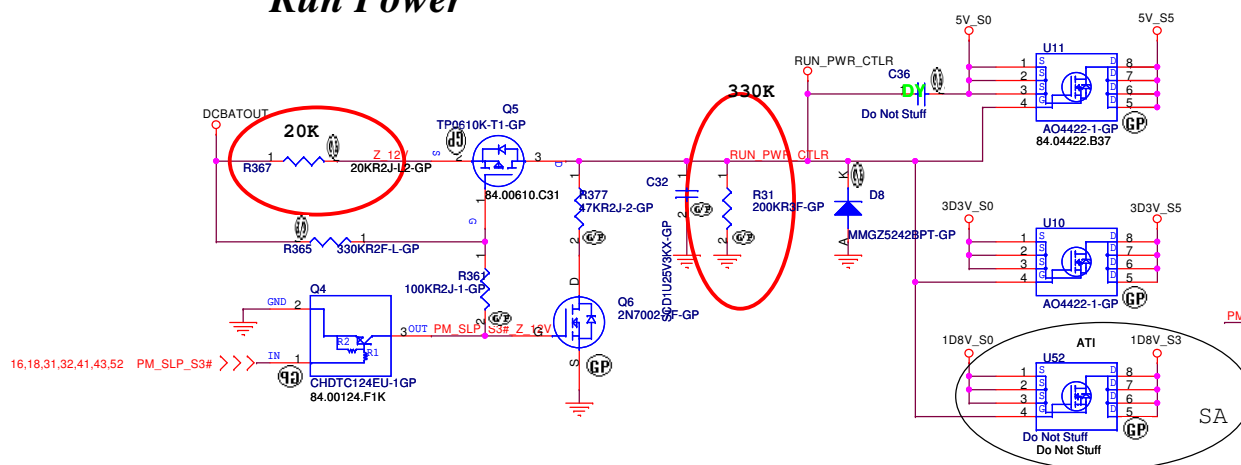




Aux Power



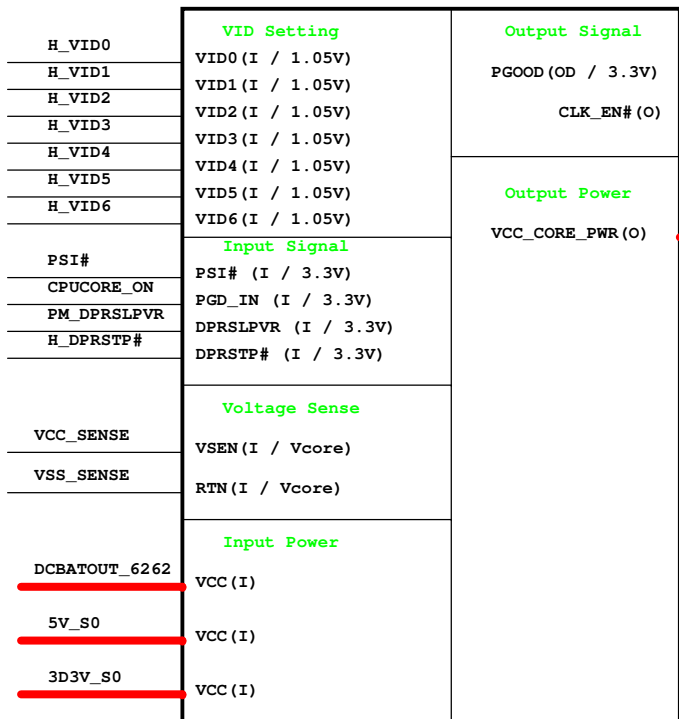
Run Power



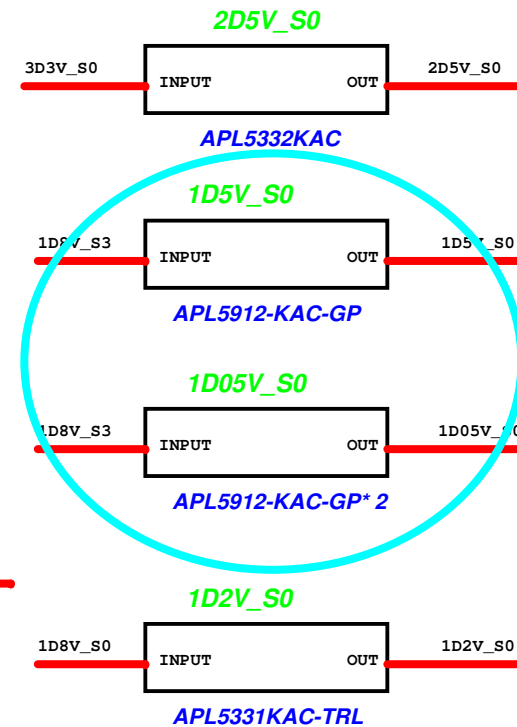
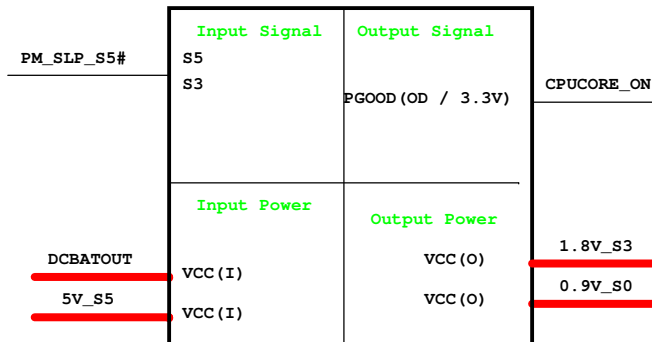
BOM

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
File RUN and AUX POWER	
Size A3	Document Number AG3
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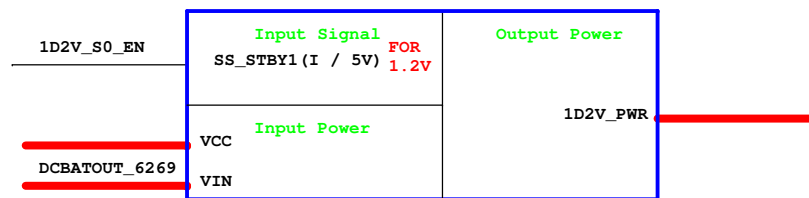
CPU_CORE
Intersil ISL6262



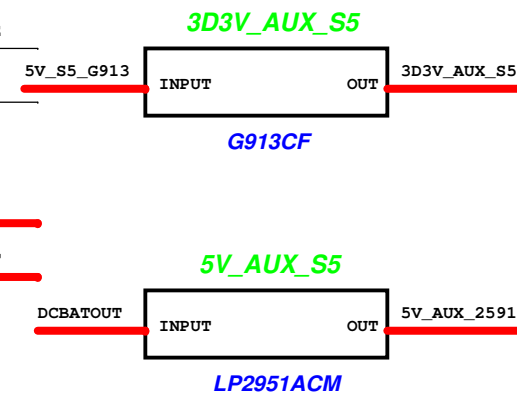
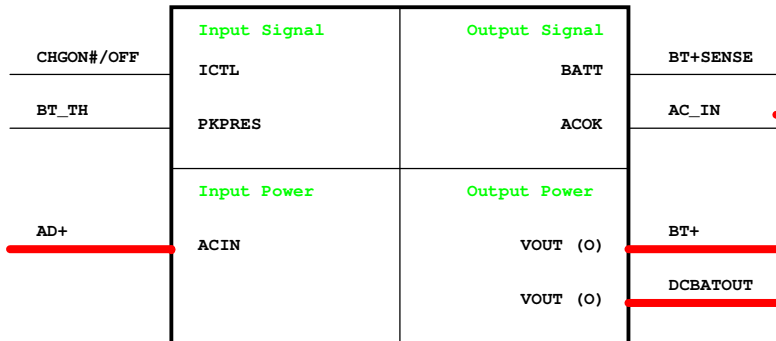
TI TPS51116
1.8V / 0.9V



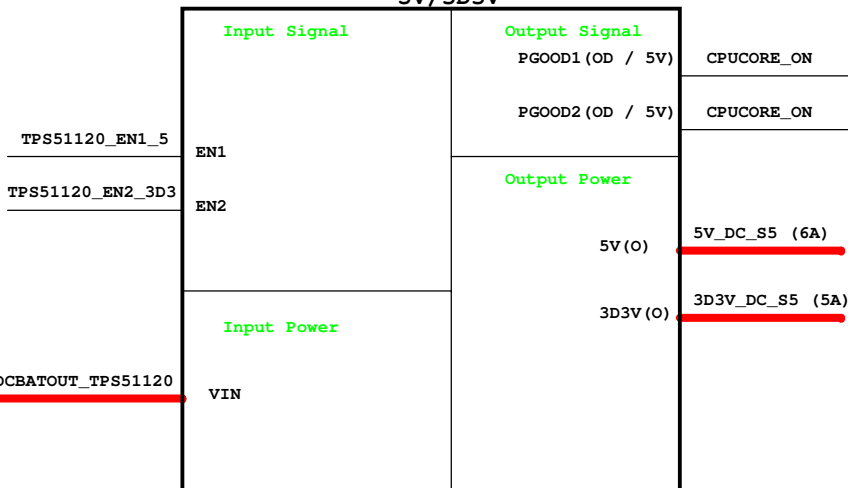
ISL6269_1D2V



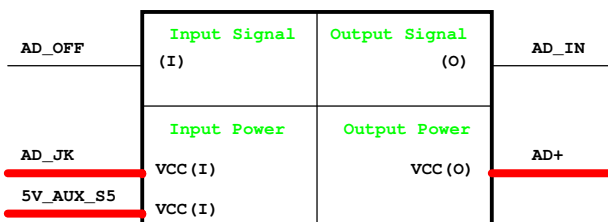
CHARGER ISL6225



TPS51120
5V/3D3V



Adapter



Place close to phase 1 choke
If NTC=330Kohm, R10=8.66K

5 H_VID[0..6]

40,41,43,48 CPUCORE_ON
16 PM DPRSLPVR
4,15 H DPRSLP#
3 CLK_EN#

Switching Frequency=300KHz

When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184

PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.

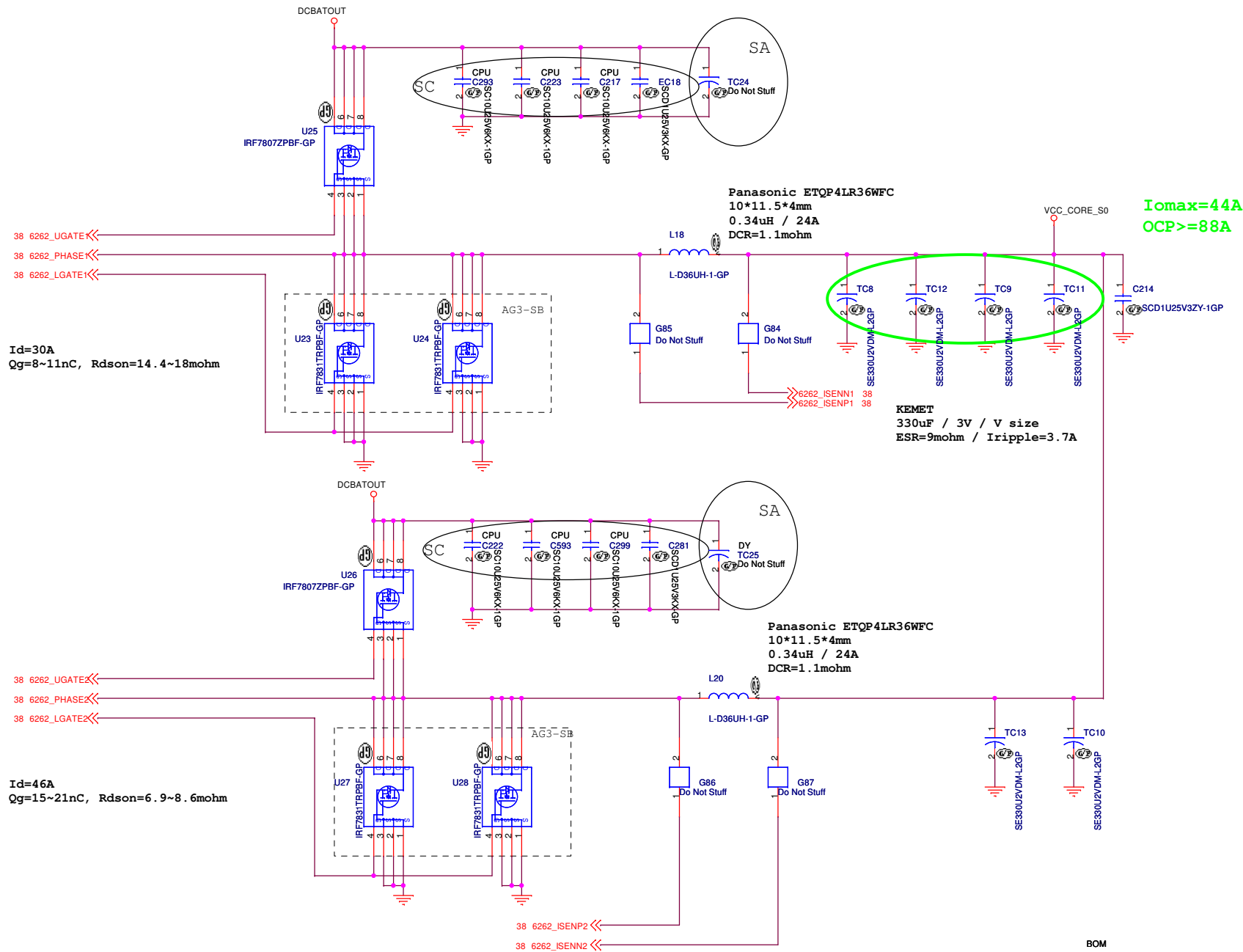
Place close to phase 1 choke

Load Line

BOM

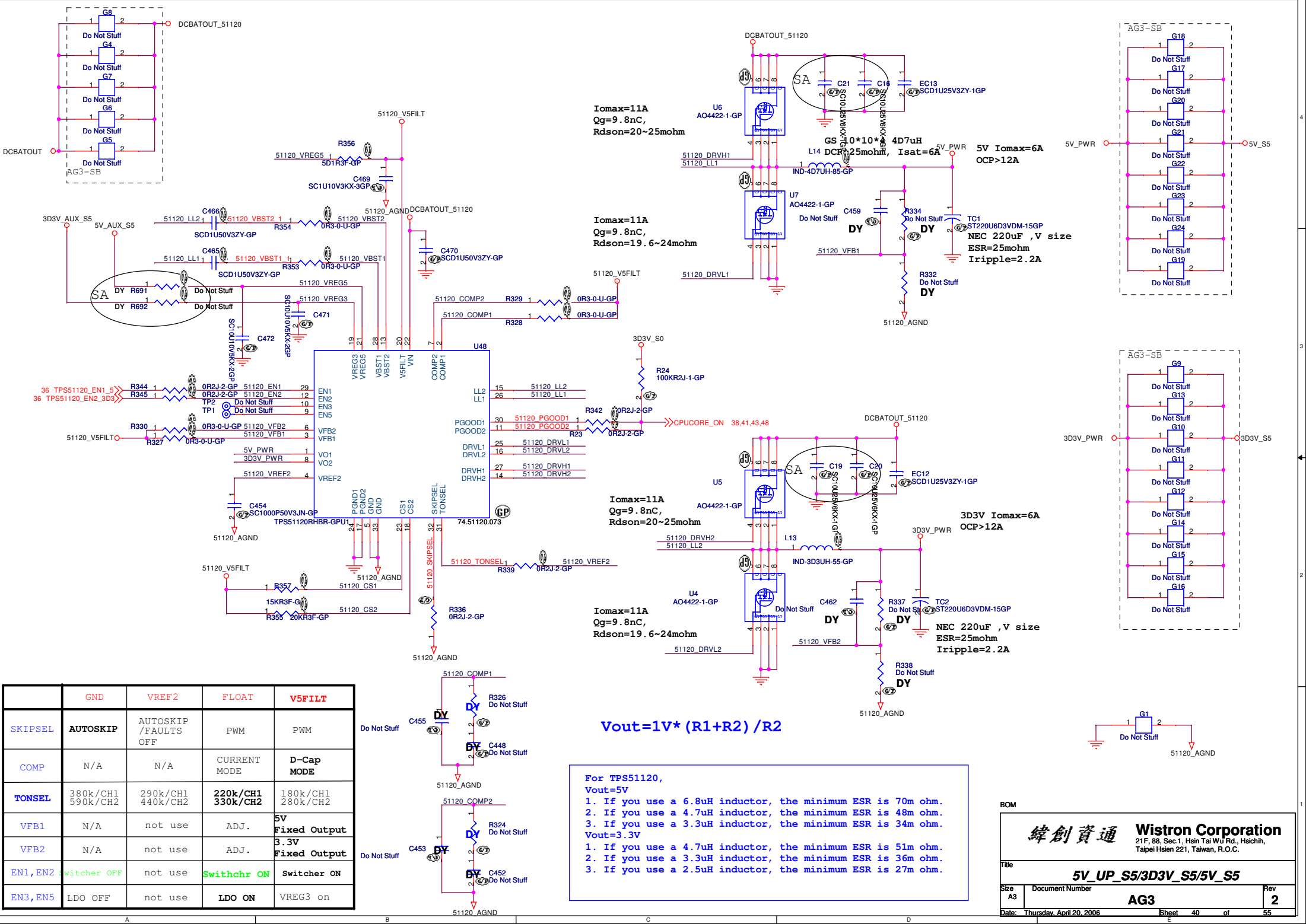
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU Vcore Power_1	
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 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

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CPU Vcore Power_2/2		AG3		2
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	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP / FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

Vout=1V* (R1+R2) /R2

For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

BOM

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Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

5V_UP_S5/3D3V_S5/5V_S5

Size A3

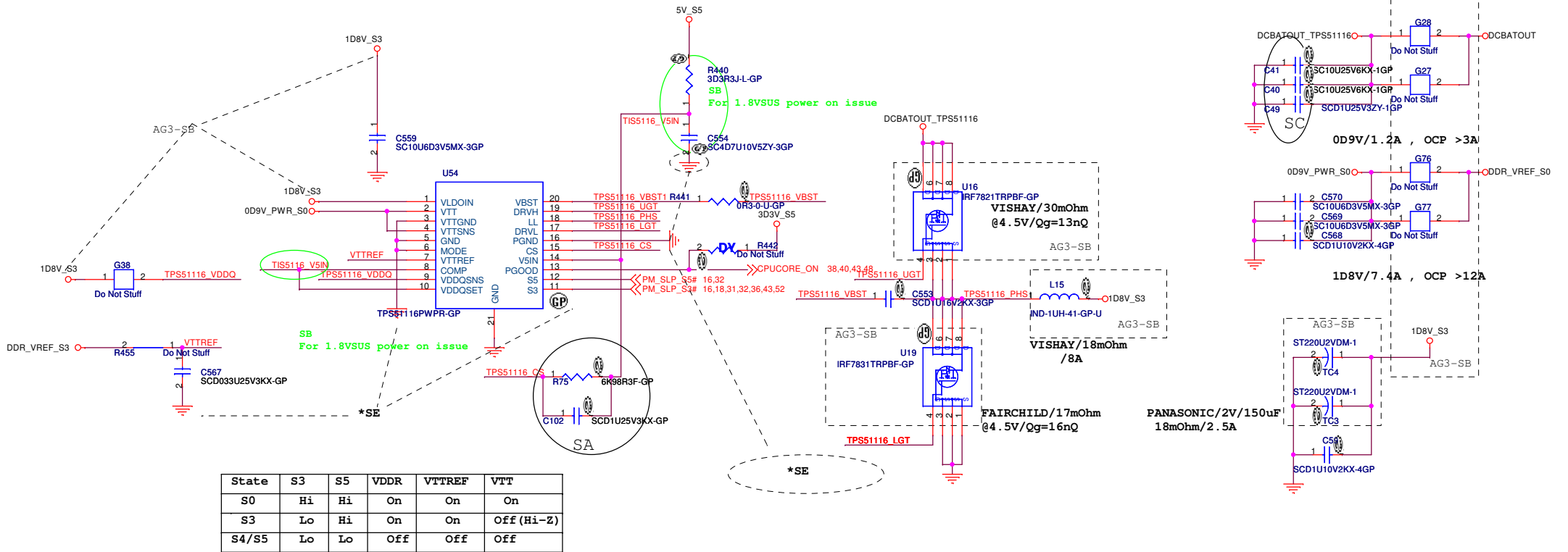
Document Number

Rev 2

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TI TPS51116 for 1D8V and 0D9V



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

BOM

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

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Title	Author	Date	Page	Page	Page	Page	Page				

DC to DC 1.8V & 0.9V

Size	A3
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	Document Number
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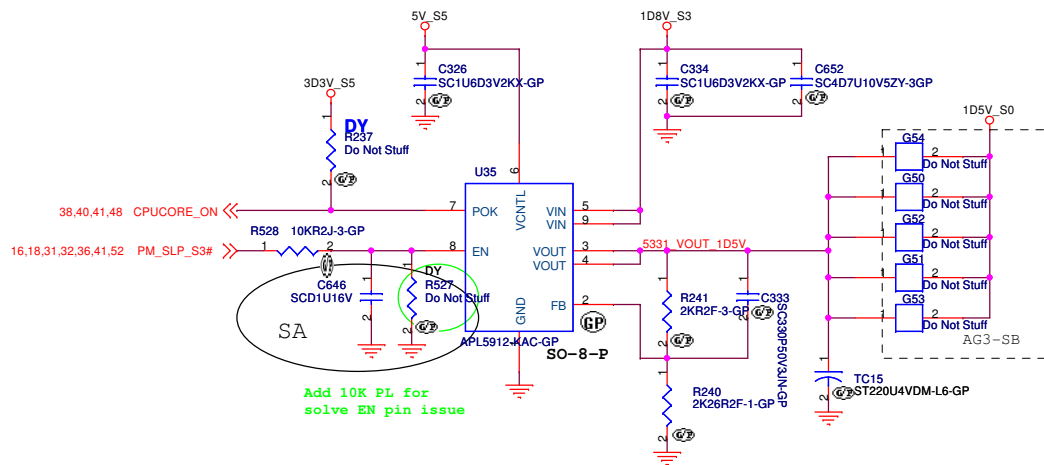
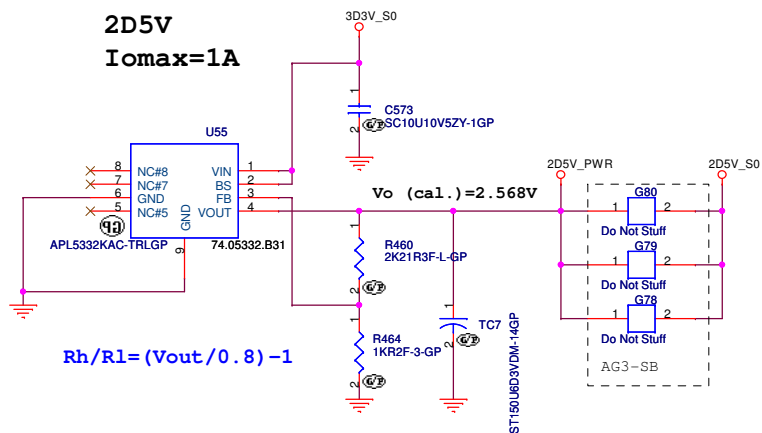
AG3

2

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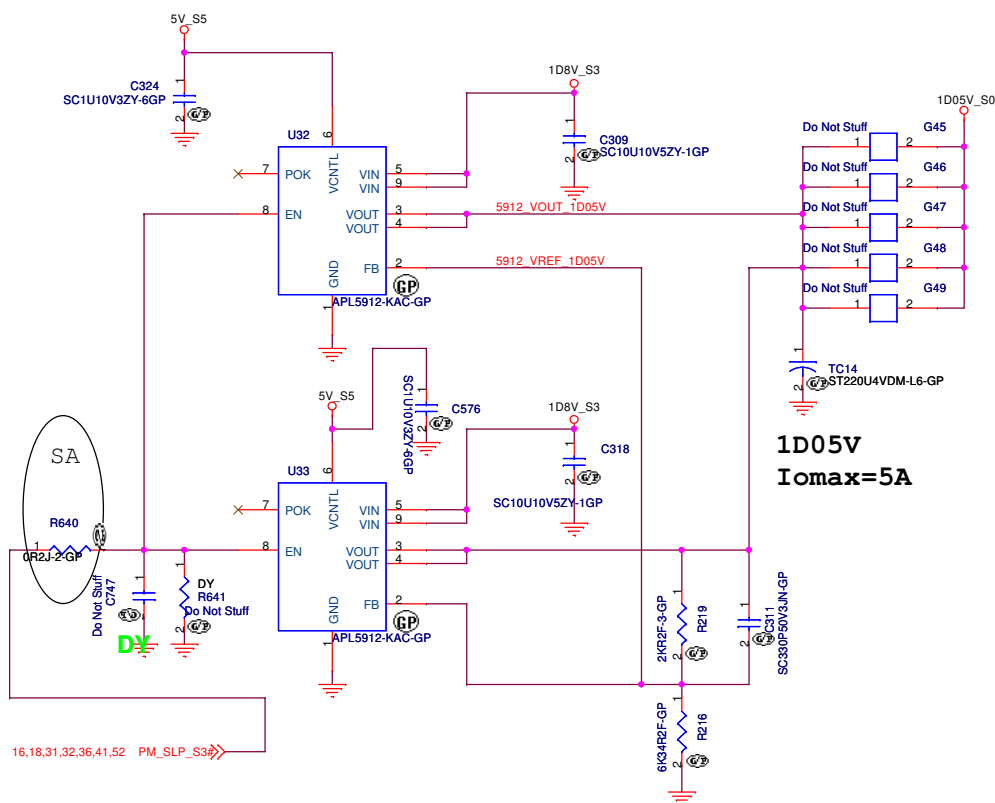
2D5V Iomax=1A



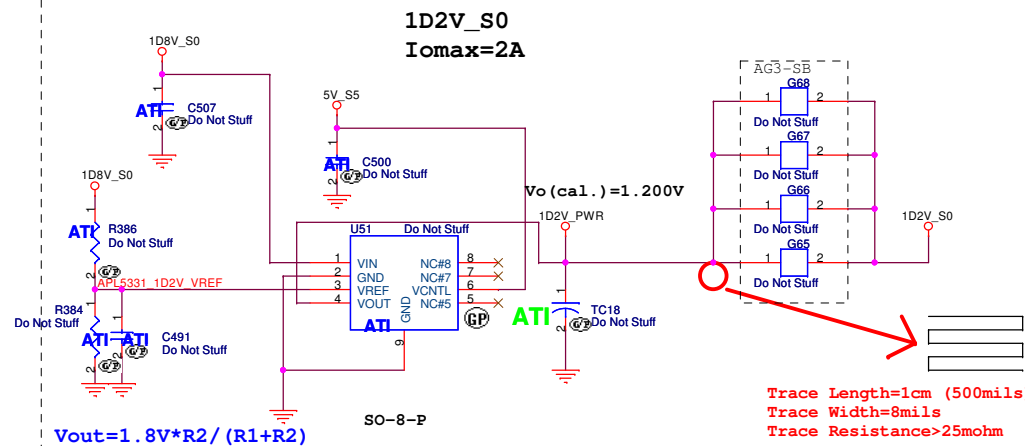
KEMET
100uF, 6V, B2 Size
ESR=40mohm

$$Vo = 0.8 * (1 + (R1/R2))$$

AG3-SB



1D05V Iomax=5A

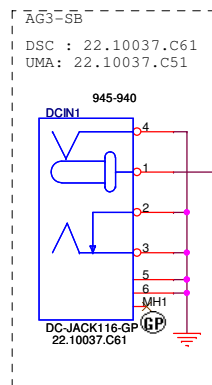


1D2V_S0 Iomax=2A

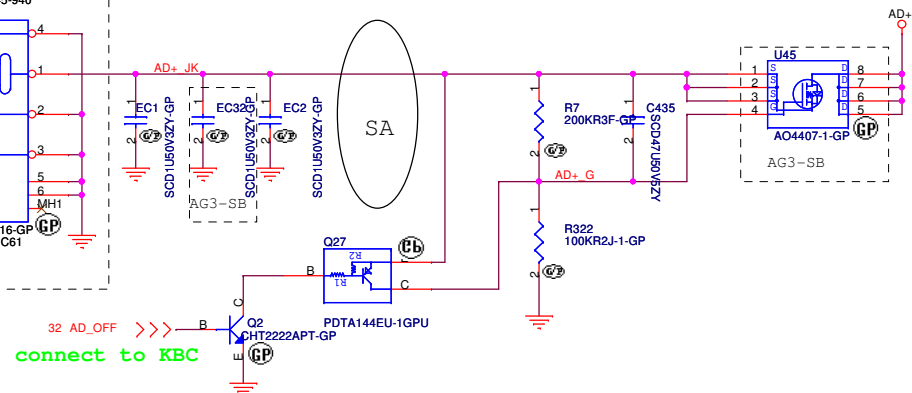
Trace Length=1cm (500mils)
Trace Width=8mils
Trace Resistance>25mohm

BOM

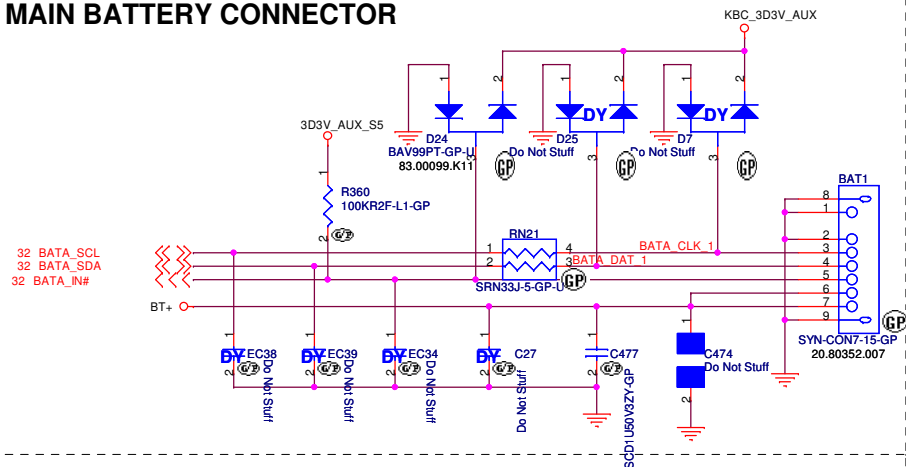
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
1D2V/1D5V/2D5V/1D05V_S0		
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ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



BOM

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size

A3

Document Number

AG3

Rev

2

Date: Friday, April 21, 2006

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**PCIE TEST POINTS MUST BE WITHIN 250 MILS
OF THE ASIC BALL WITH POSITIVE AND NEGATIVE
SIGNALS THE SAME DISTANCE**

REFER TO PCI EXPRESS DESIGN GUIDE
FOR RECOMMENDED AC COUPLING CAPS
PLACEMENT ALONG THE TX INTERCONNECT



```
M56: 71.0M56P.M01
M54: 71.0M54P.B0U
M52: 71.0M52P.B0U
```

MEM_ID0	MEM_ID2 MEM_ID1	MEM_ID3		MEM	SIZE	VENDOR	CHIP
1	0	1	0	64M	16M*16	Infinion	x2
0	1	1	AM	0	16W*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x2
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256G	32M*16	Infinitec	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256G	32M*16	Hynix	x4

[illegible]

```
When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11
```

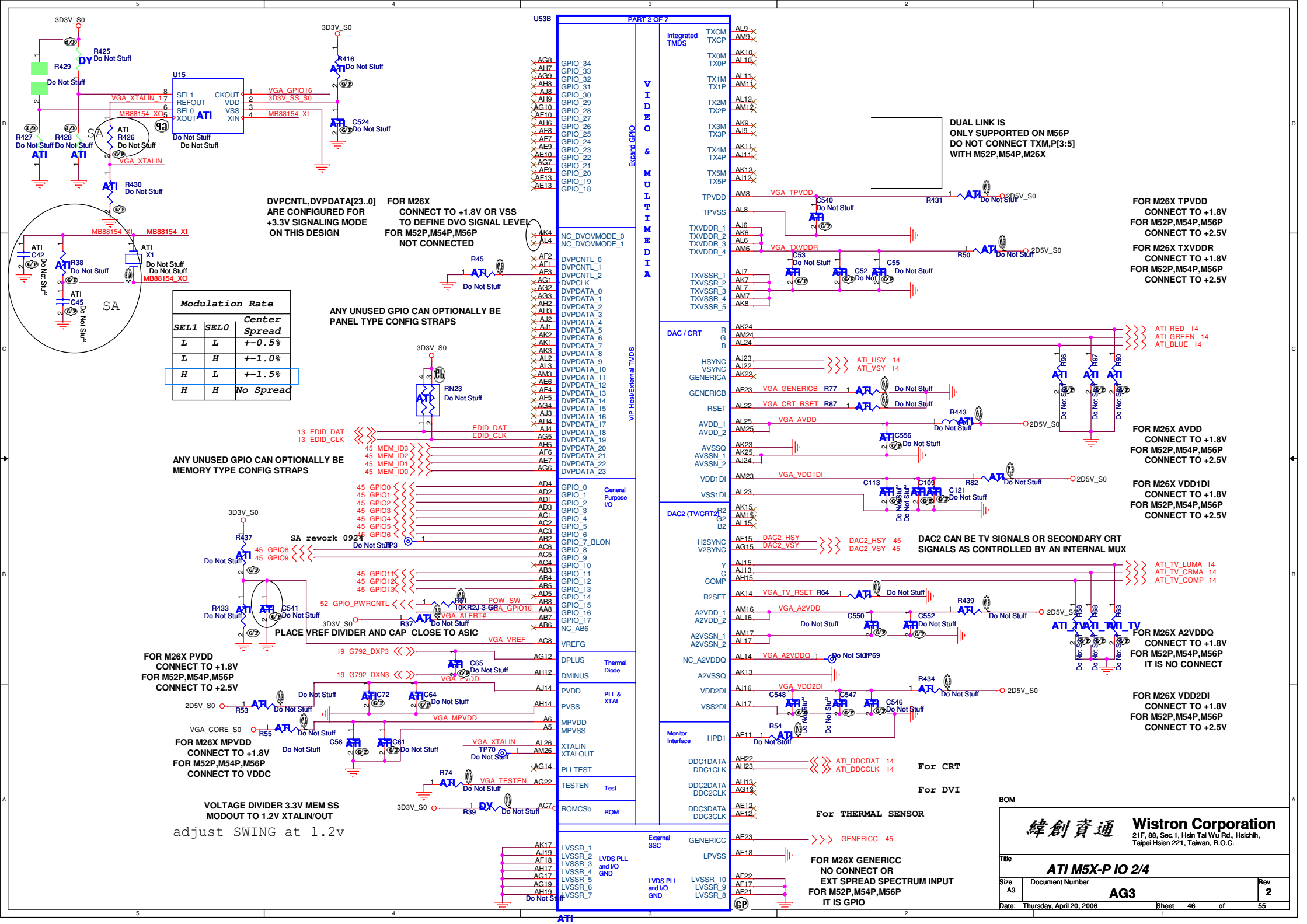
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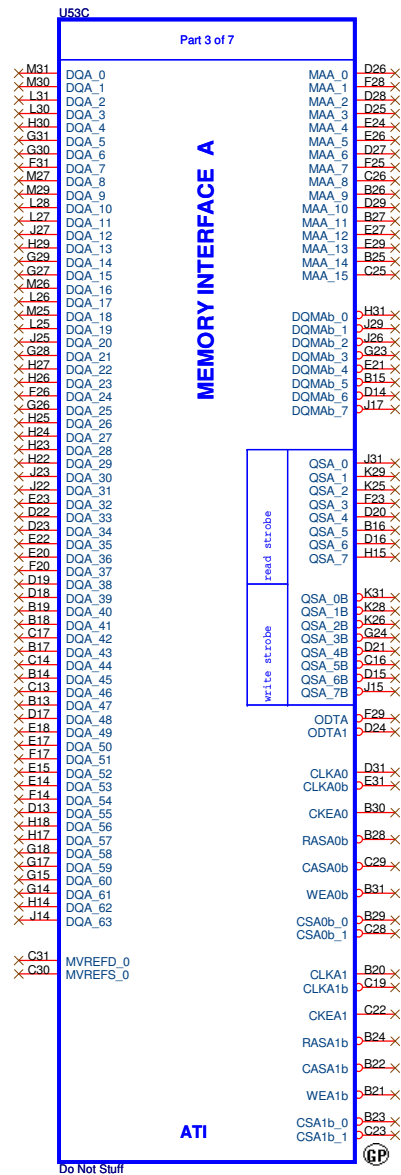
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATI M5X-P PCIE 1/4
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Size A3	Document Number AG3	Rev 2
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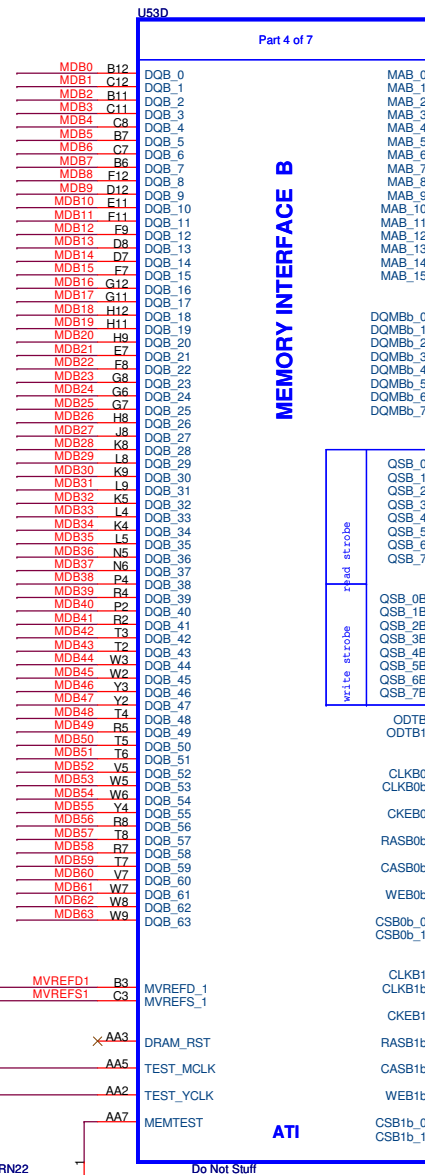
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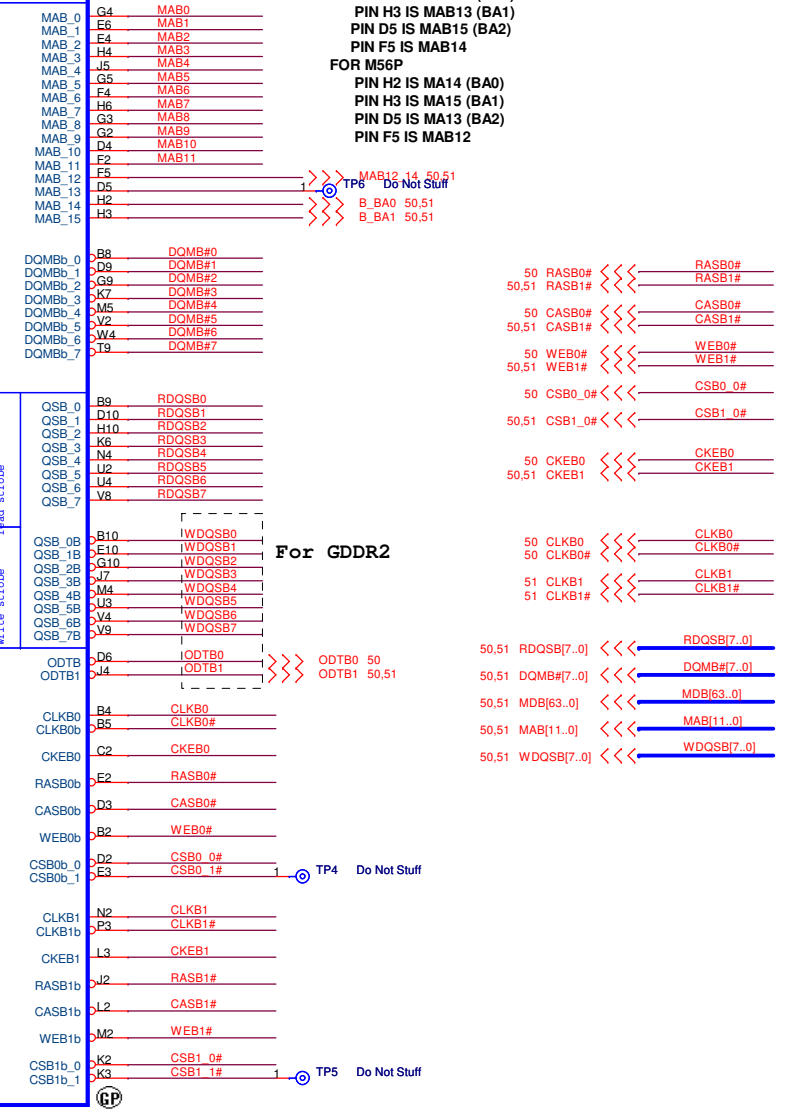
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

Ch-A
FOR M52P,M54P,M26X
PIN B25 IS MA12 (BA0)
PIN C25 IS MA13 (BA1)
PIN E29 IS MA15 (BA2)
PIN E27 IS MA14
FOR M56P
PIN B25 IS MA14 (BA0)
PIN C25 IS MA15 (BA1)
PIN E29 IS MA13 (BA2)
PIN E27 IS MA12



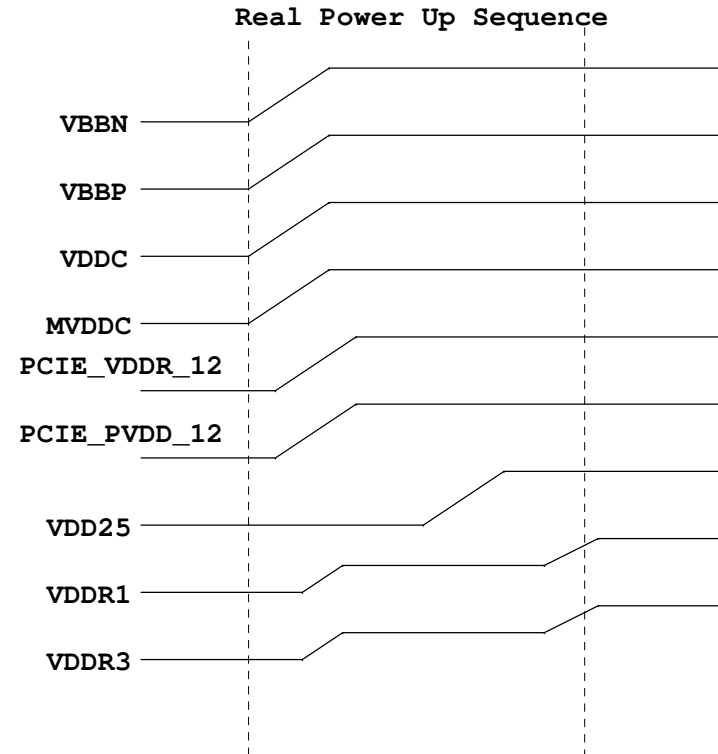
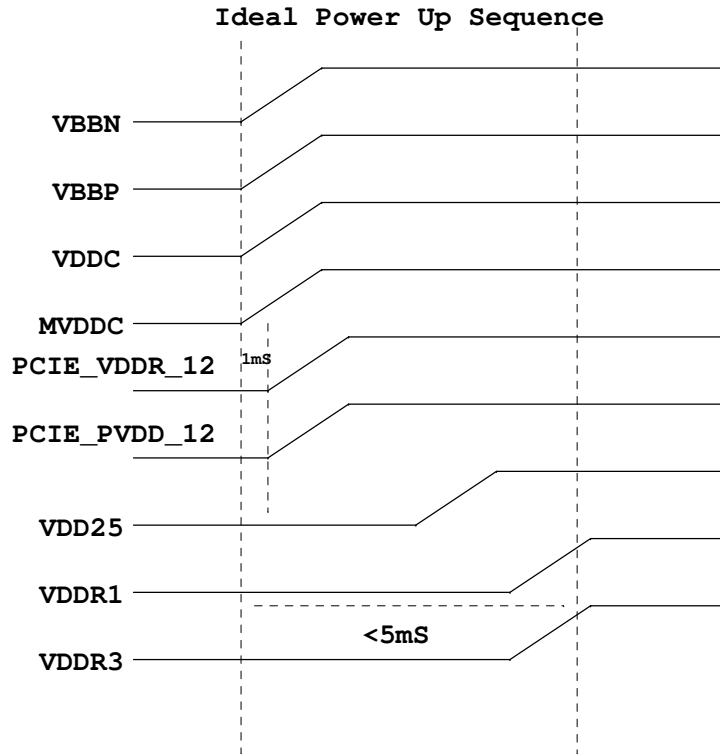
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

Ch-B
FOR M52P,M54P,M26X
PIN H2 IS MAB12 (BA0)
PIN H3 IS MAB13 (BA1)
PIN D5 IS MAB15 (BA2)
PIN F5 IS MAB14
FOR M56P
PIN H2 IS MA14 (BA0)
PIN H3 IS MA15 (BA1)
PIN D5 IS MA13 (BA2)
PIN F5 IS MAB12



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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,.....

General Guidelines:

- BBN and BBP must ramp up before or at the same time as VDDC but not after.
- VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).
- All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).
- VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
- The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory I/Os) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:
Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

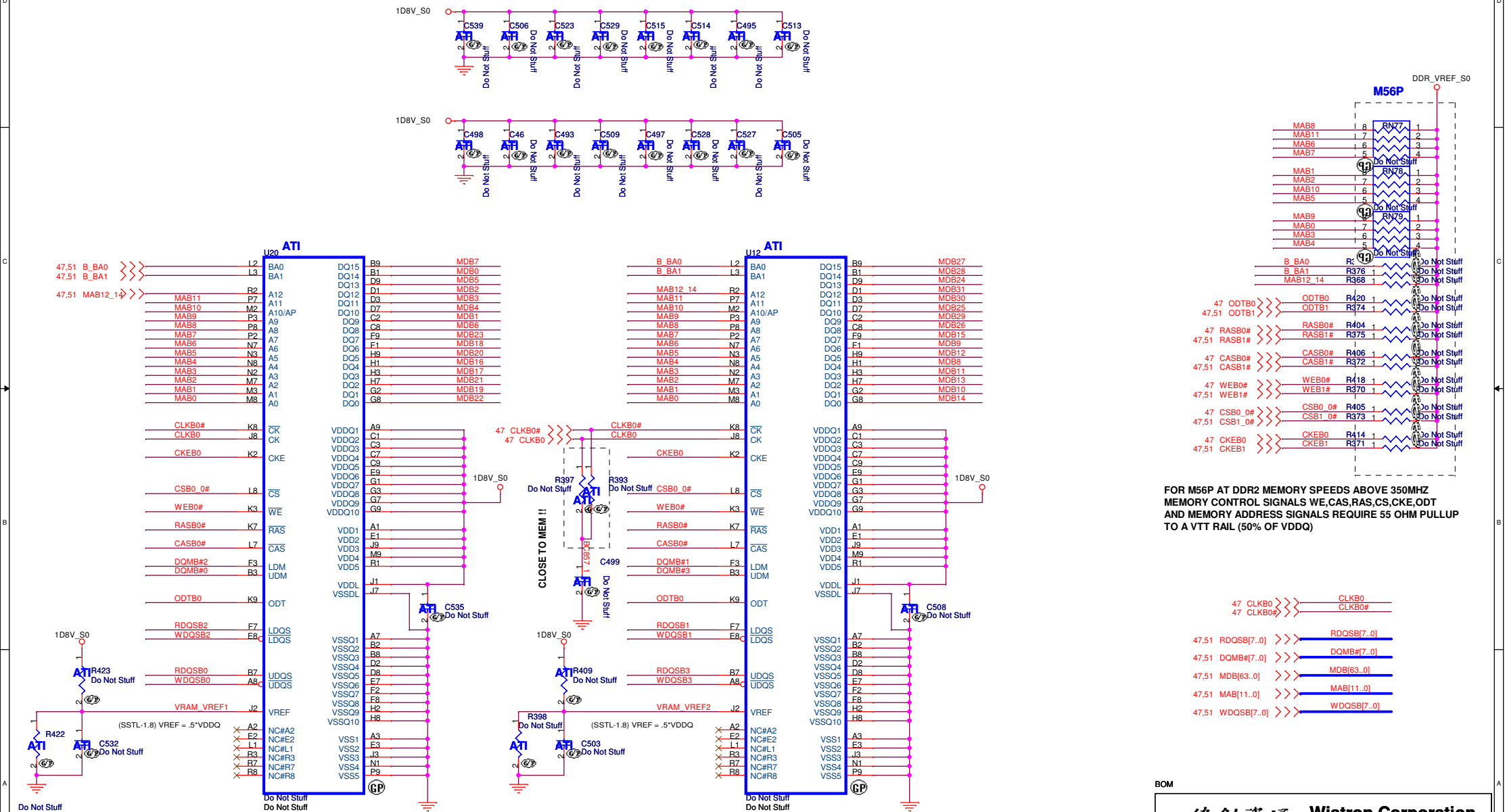
Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

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CHAN B DDR2 84BGA 32MX16 MEMORY



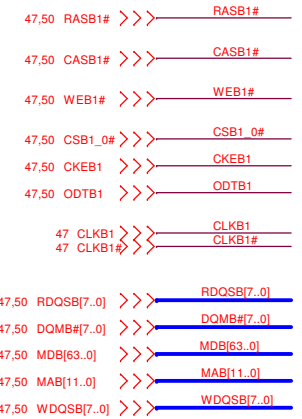
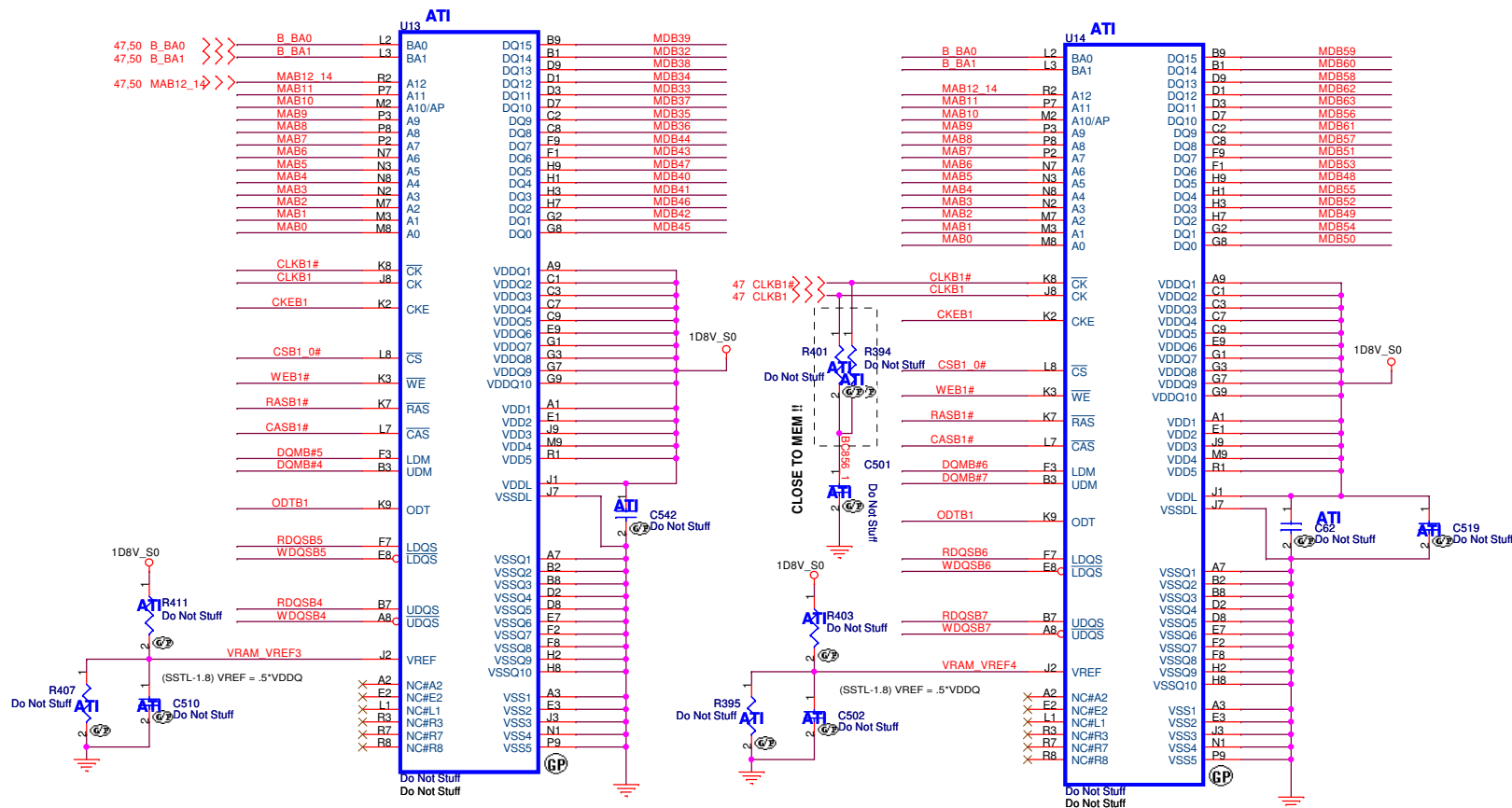
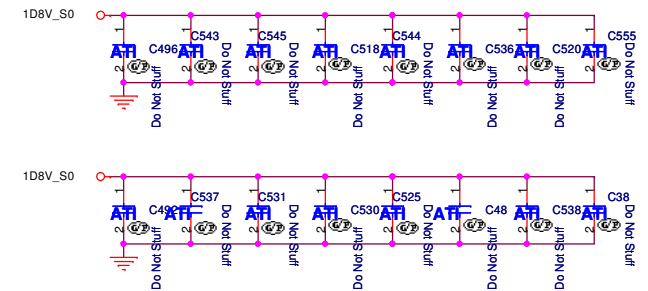
FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ
MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT
AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP
TO A VTT RAIL (50% OF VDDQ)

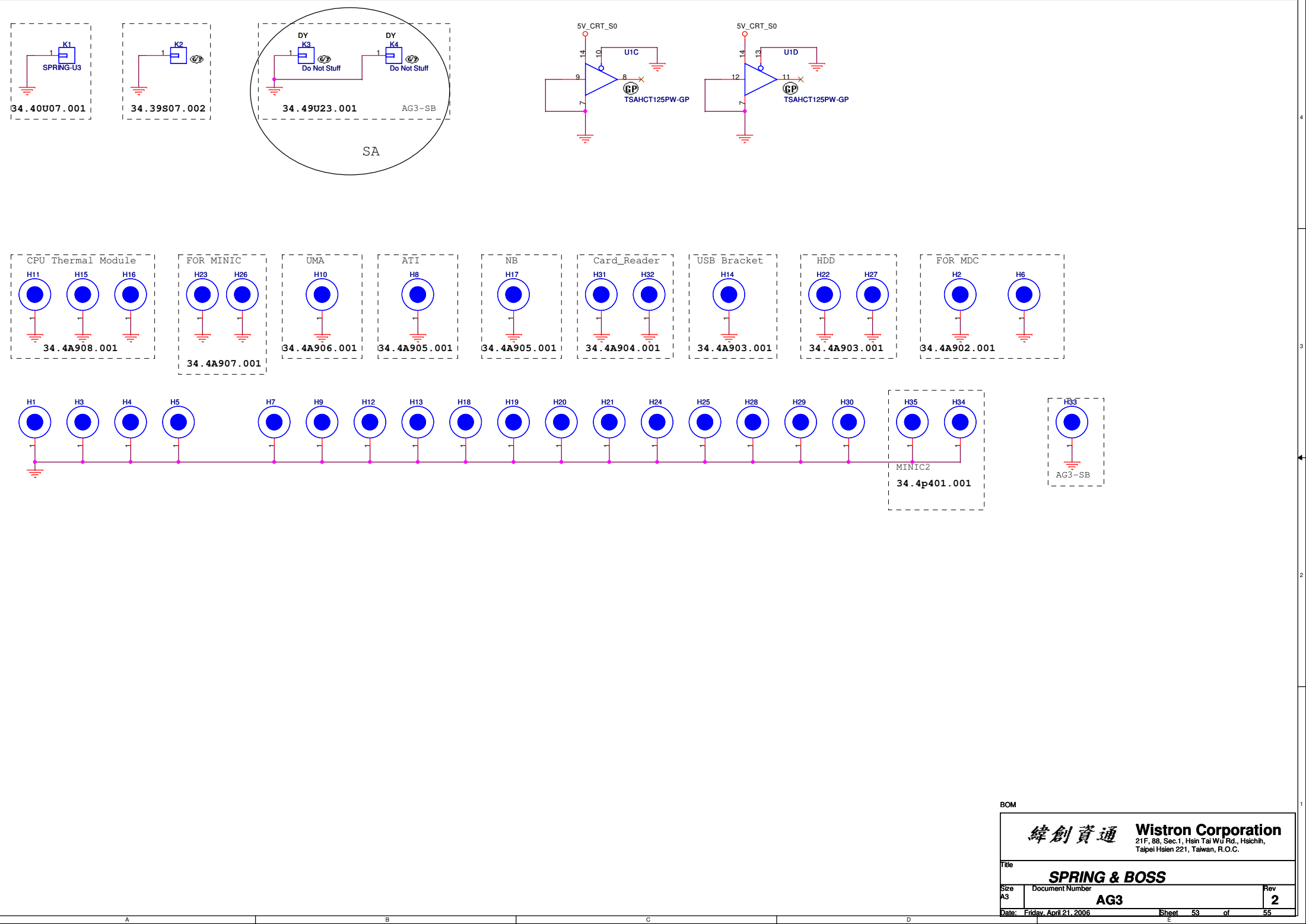
- 47 CLKB0 >>> CLKB0
- 47 CLKB0# >>> CLKB0#
- 47,51 RDQSB[7..0] >>> RDQSB[7..0]
- 47,51 DQMB[7..0] >>> DQMB[7..0]
- 47,51 MDB[63..0] >>> MDB[63..0]
- 47,51 MAB[11..0] >>> MAB[11..0]
- 47,51 WDQSB[7..0] >>> WDQSB[7..0]

72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 350Mhz)
72.18256.B0U IC VRAM HYB18T256161AFL25 BGA (16M*16, 350Mhz)
72.18512.A0U IC VRAM HYB18T512161BF-25 BGA (32M*16, 400Mhz)

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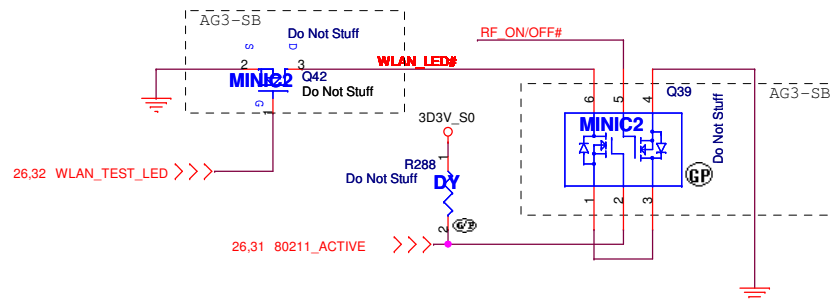
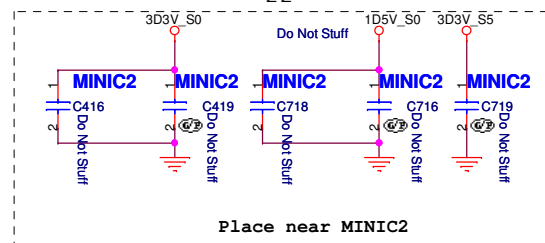
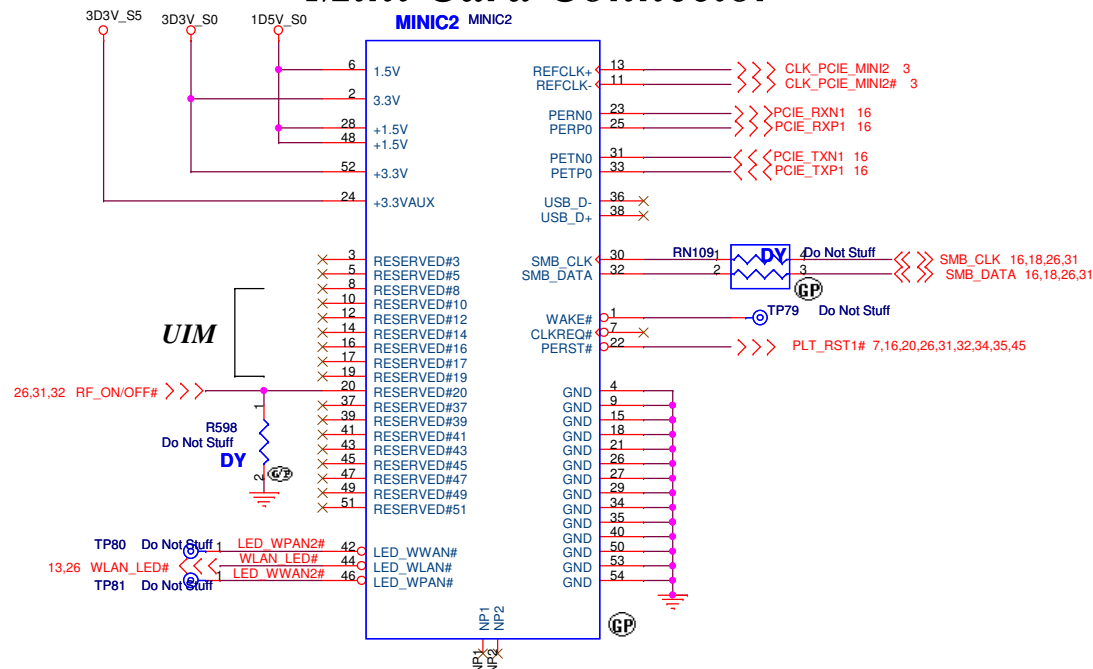
EMI CAP

AG3-SB



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Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsein 221, Taiwan, R.O.C.		
2		
Rev		
AG3		
Document Number		
SPRING & BOSS		

Mini Card Connector



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緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

MINICARD 2

Size

Document Number

AG3

Rev

2

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