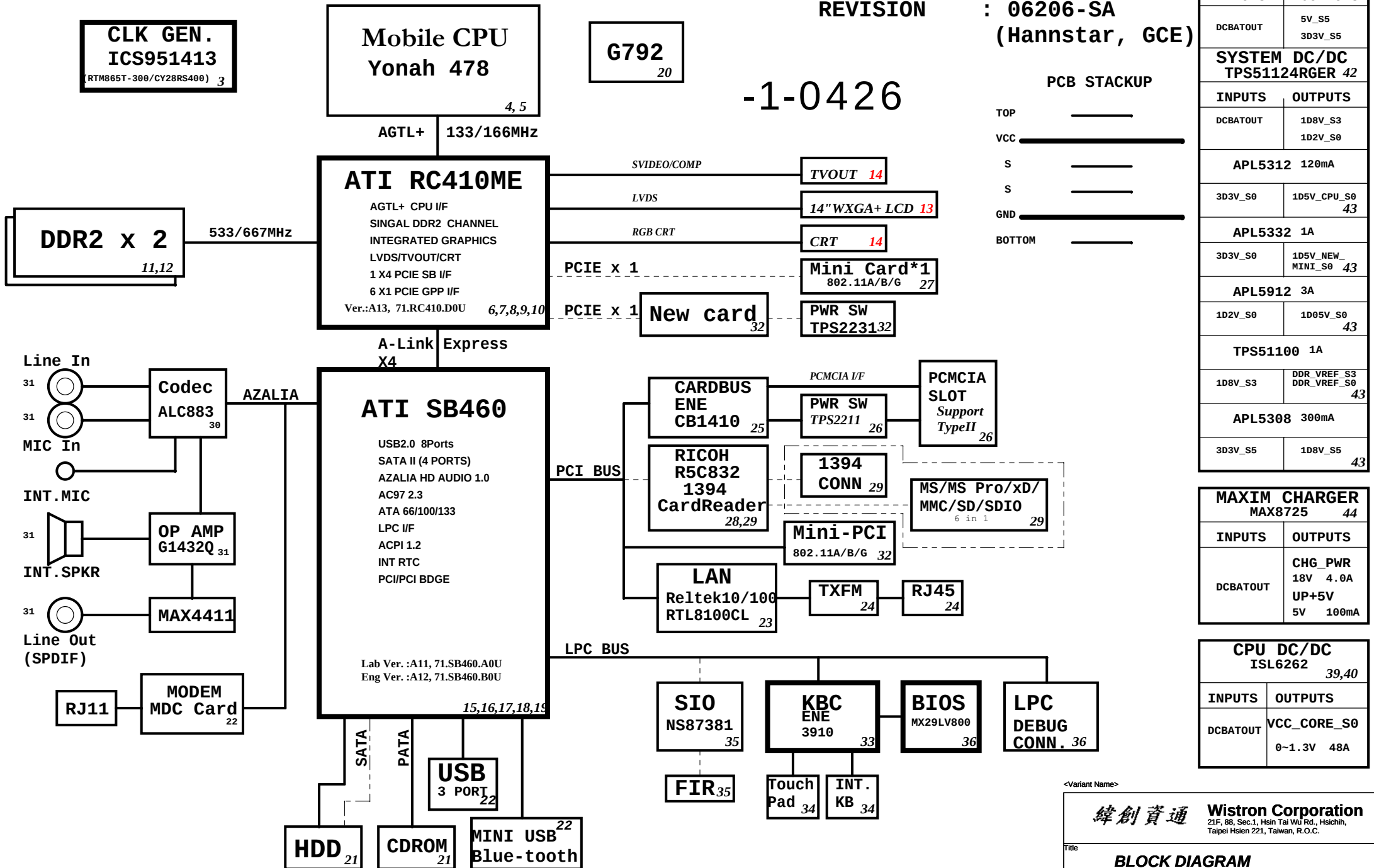


Garda-5 Block Diagram

Project code: 91.4Q201.001
PCB P/N : 55.4Q201.XXX
REVISION : 06206-SA
(Hannstar, GCE)



<Variant Name>

Pair

Device

0

USB1

1

BT

2

USB2

3

NEW C

4

USB3

5

CCD

6

MINIC1

7

NC

PCI_CLK0

PCM

PCI_CLK1

IEEE1394

PCI_CLK2

LAN

PCI_CLK3

MINI

PCI_CLK4

KBC

PCI_CLK5

FWH

PCI_CLK6

SIO

PCI_CLK7

SPDIFOUT

PCI ROUTING TABLE

DEVICE	IDSEL	IRQ(Default)	REQ# / GNT#
MiniPCI	AD22	H	REQ#1/ GNT#1
R5C832	AD20	F : 1394 H : 6 in 1	REQ#3/ GNT#3
LAN(RTL8100CL)	AD17	E	REQ#2/ GNT#2
CARDBUS CB1410	AD16	G	REQ#0 / GNT#0
USB UHCI	AD29	A, B, C, D	
USB 2.0 EHCI	AD29	A	
DMI-to-PCI AC97 Modem AC97 Audio	AD30	B A	REQ#1 / GNT#1
LPC Bridge IDE SATA SMBus	AD31	A B B	
PCI Express	AD28	A, B, C, D	
Azalia Controller	AD27	A	

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,.....

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

History

2006/04/26 (-1 Modify)

1. page 27, change R8/R226 to 100 ohm due to power/email to dark.
2. page 15, change C286/C287 from 18pf to 15pf due to frequence shift(from -6.7 to 4ppm).
3. page 23, change C295/C294 from 15p to 12p due to frequence shift(from -23.3 to 7.9ppm).
4. EMI Solution for USB/MDC
 a. Change L23, L24, L31, L32 to "69.10084.071".
 b. del R353,R354,R356,R360,R445,R446.
 c. Change L1, L2 to "68.00331.011".
5. Page 44, change C12/C14 to 78.10699.43L due to 78.10699.42L Obsoleted.

2006/04/13 (-1 Modify)

1. Page 31, R447/R448 tp 33ohm.
2. Page 45, Add D4:83.P4SSM.0AM.
3. Page 44, Change C321 from 78.10492.4BL to 78.10224.2BL(1000P, 50V, K0603).
4. Page 23, change R209 from 5.6K to 5.37K.
5. Page 24, change XF1 from 68.68161.30A to 68.01201.30A.
6. Page 46, Mini card stand-off(銅柱) need to be changed from 34.4P401.001 to 34.4A907.001.
7. change 84.27002.L04 to 84.27002.F31.

2006/04/10 (-1 Modify)

1. Page 8, add "LVDS DIGON" solution from ATI PA note.
2. Page 31, Add R to GND and serial R for U60 pin13/15.

2006/04/03 (SB Modify)

1. Page 40, Dummy C593.
2. Page 44, Del C32.
3. Page 41, DCBATOUT 51120 change to DCBATOUT (Del G4,G5,G6,G7,G8)
4. Page 4/5, updae CPU symbol.
5. Page 15, Change X5 to same as X1 due to ME high limit issue, Cap. the same as X1 but should fine-tune.
6. Page 39/41/42, change "GAP-CLOSE-PWR" to 0 ohm PAD due to layout concern.

2006/03/31 (SB Modify)

1. Page 3, change R139 to bead and C211 to 2.2u for CRT Jitter.
2. Page 6, change R105 from 1.8K to 4.7K.
3. Page 8, change C165 to 2.2u for ATI recommend.
4. Page 8, SIV EDID_CLK/DAT issue, change RN53 to 4.7K.
5. Page 14, SIV RBG fail:
6. Page 15,
 a. PCIRST1#(1394) shoulder: Add 33 ohm @ SB.
 b. PLT_RST1# overshoot : change R144 to 33ohm & R141 to 100P.
 c. Add 0ohm for RTC power for ATI recommend.
7. Page 40 , add 10U Cap.
8. Page 13/27, change Green LED4/LED5/LED1 to 83.00190.L70.
 (manual change yellow LED6/LED3/LED8/LED2 to 83.00190.S70).
9. EMI request:
 a. Page 13, USB PP5,USB PN5 add COMMON CHOKE.
 b. EC28,EC34,C208 add 0.1uCap.
 c. CLK48_ICH(near CLK GEN.),SB_CLK33_FWH(near R177) add 20p Cap..

2006/03/28 (SB Modify)

1. Page 14, change Q15/Q14 to 2N7002 for SIV CRT SMBus bug.
2. Page 15, Change C248/C261/C264/C263/C252 from 78.10491.4FL to 78.10523.5F1,
 and C262 from 78.10693.41L to 78.10623.51L.
3. Page 8, Add "LCDVDD_ON" PL 100K.
4. Page 41, change U7 To A04406(84.04406.A37).
5. Page 33, KBC GPIO09 for 1394.
6. Page 33, add 1u Cap. for ENE ECRST# spec. 2ms.
7. Page 31, add audio popo noise solution.
8. Page 25, change C520 to 1U for "GBRST#".
9. Page 28, change "GBUS_GRST#_1" timing.

Wistron Corporation

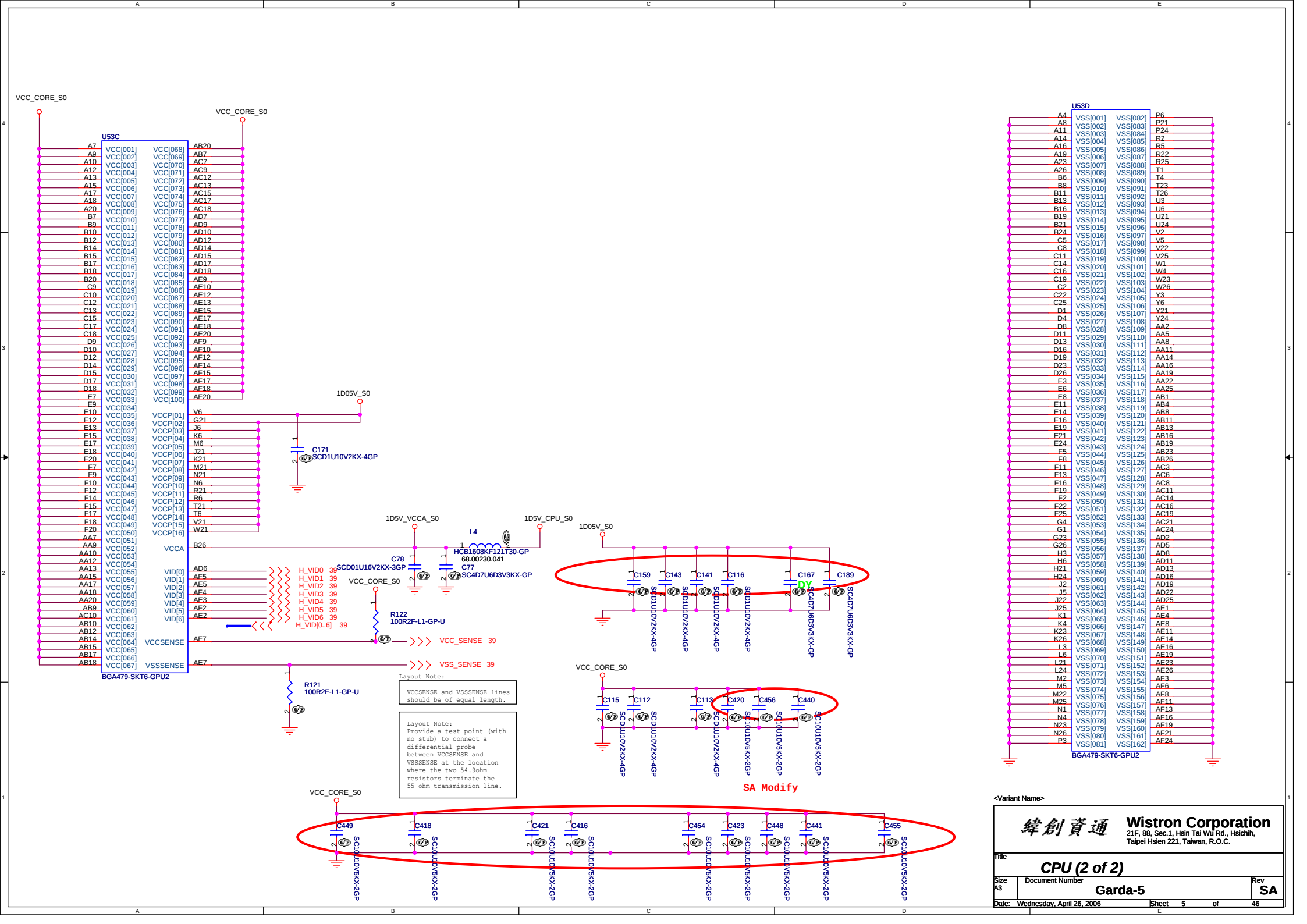
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

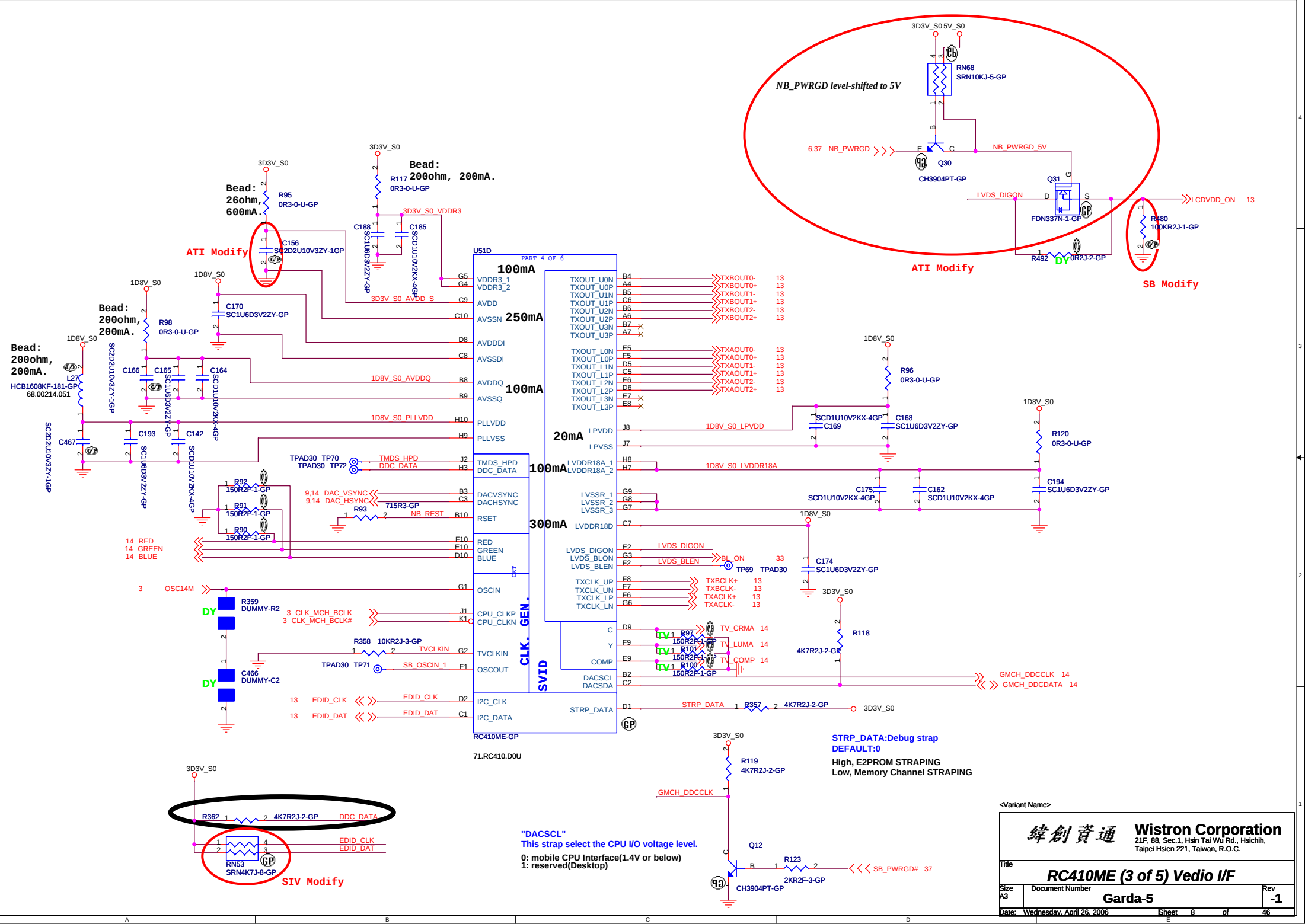
Reference

Garda-5

Date: Wednesday, April 26, 2006

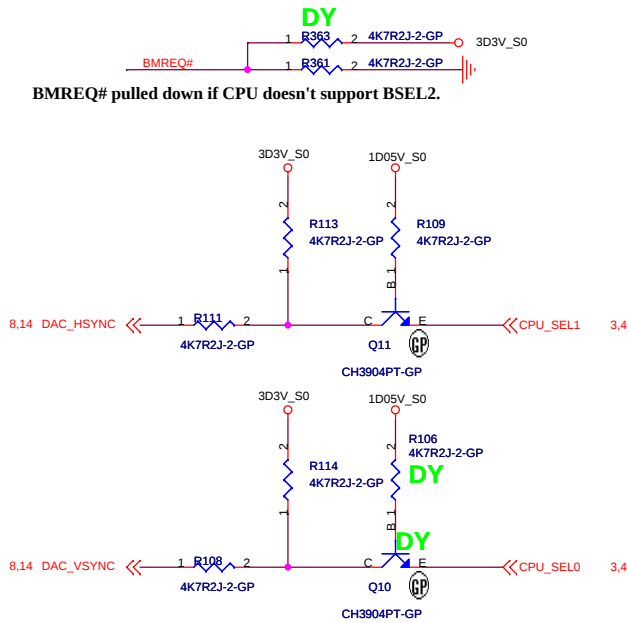
Sheet 2 of 46





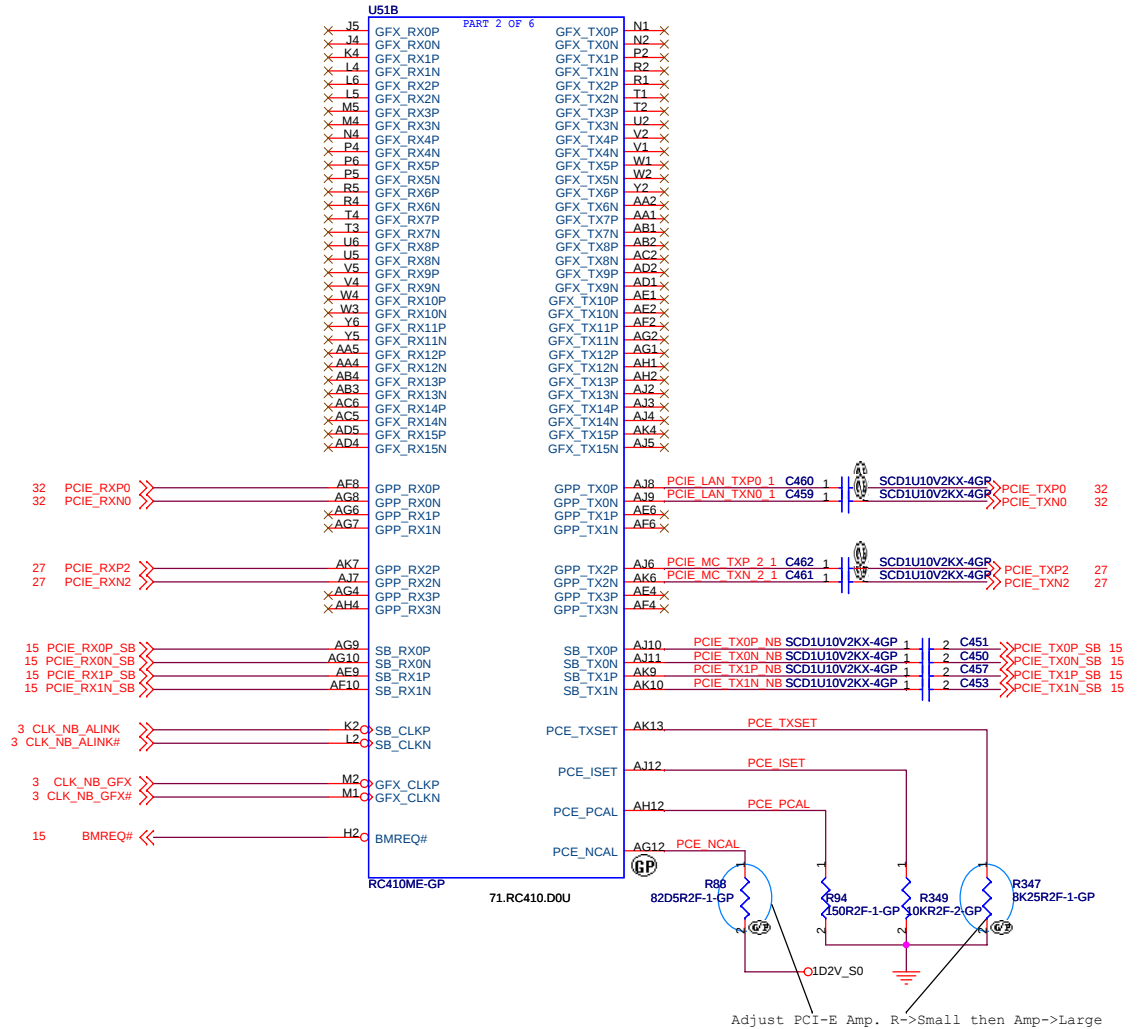
NB Strap pins

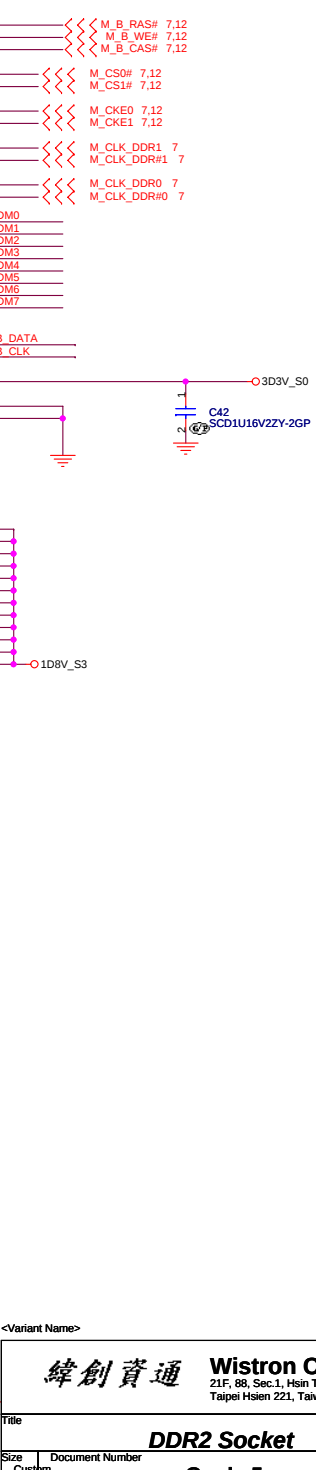
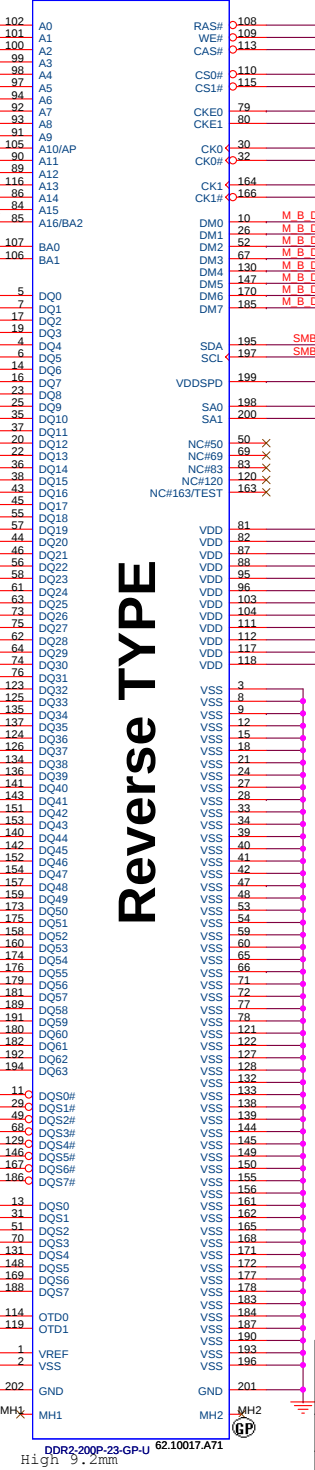
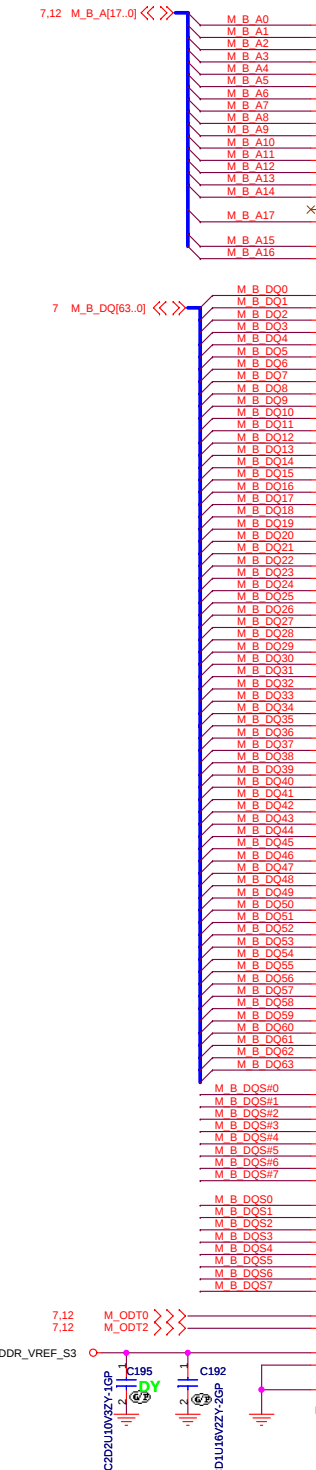
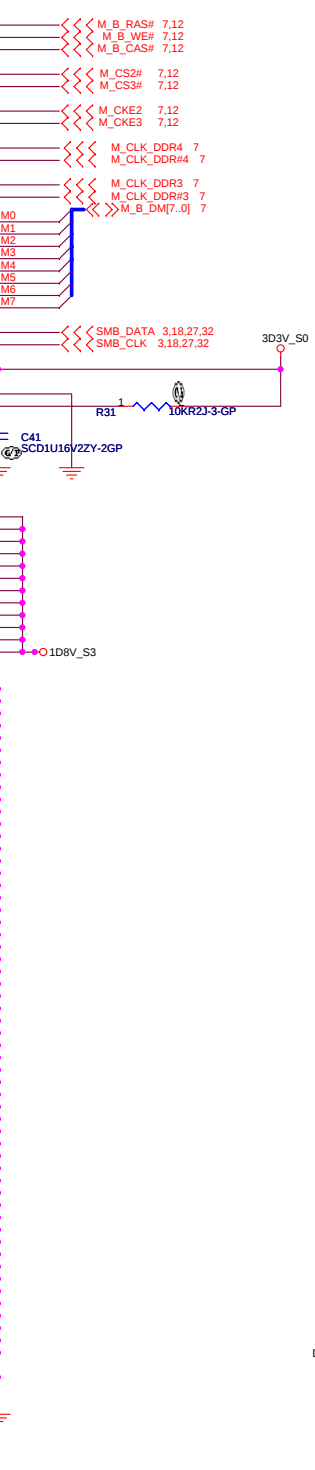
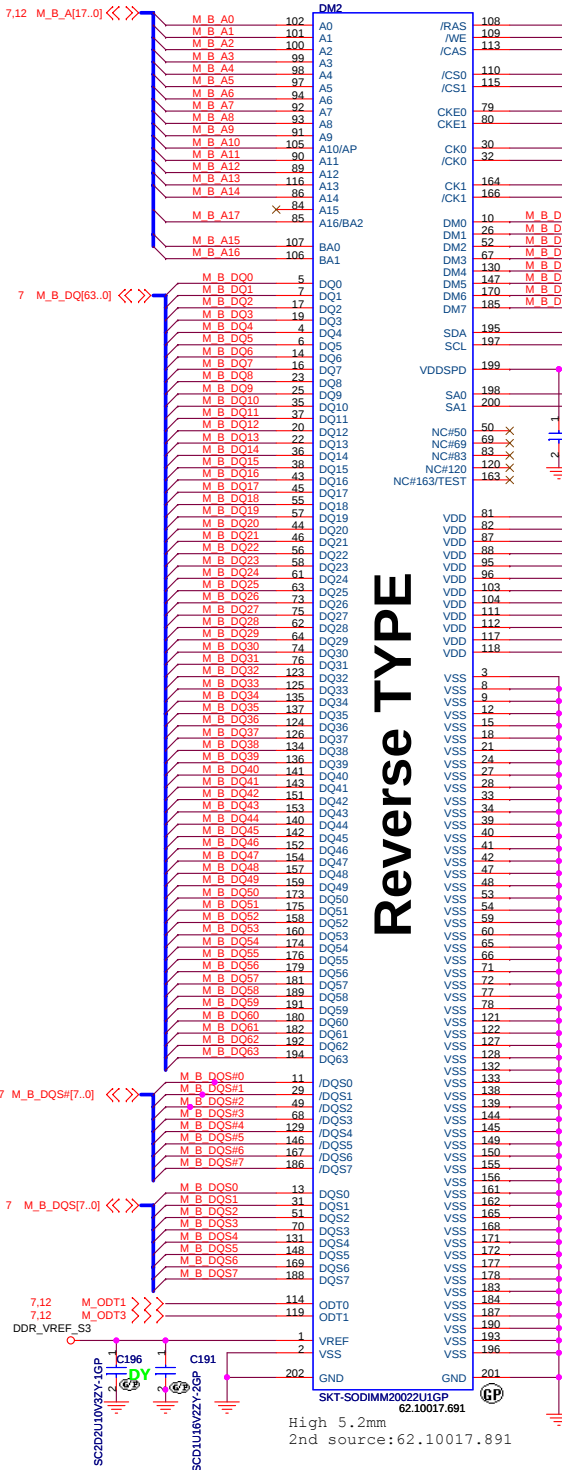
All pull-up and pull-down resistors are 4.7kohm.



Select the FSB SPEED

BMREQ#	HSYNC	VSYNC	Freq.
0	0	0	100MHZ
0	0	1	133MHZ
0	1	0	-----
0	1	1	166MHZ
1	0	0	100MHZ
1	0	1	100MHZ
1	1	0	-----
1	1	1	-----





<Variant Name>

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Title

DDR2 Socket

Size Custom

Document Number

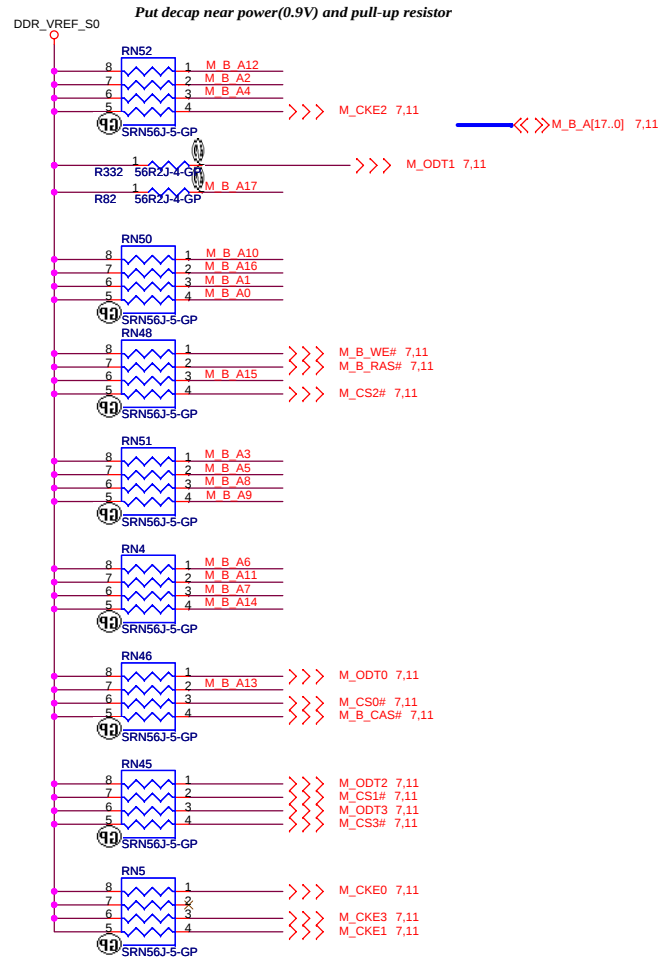
Garda-5

Rev SA

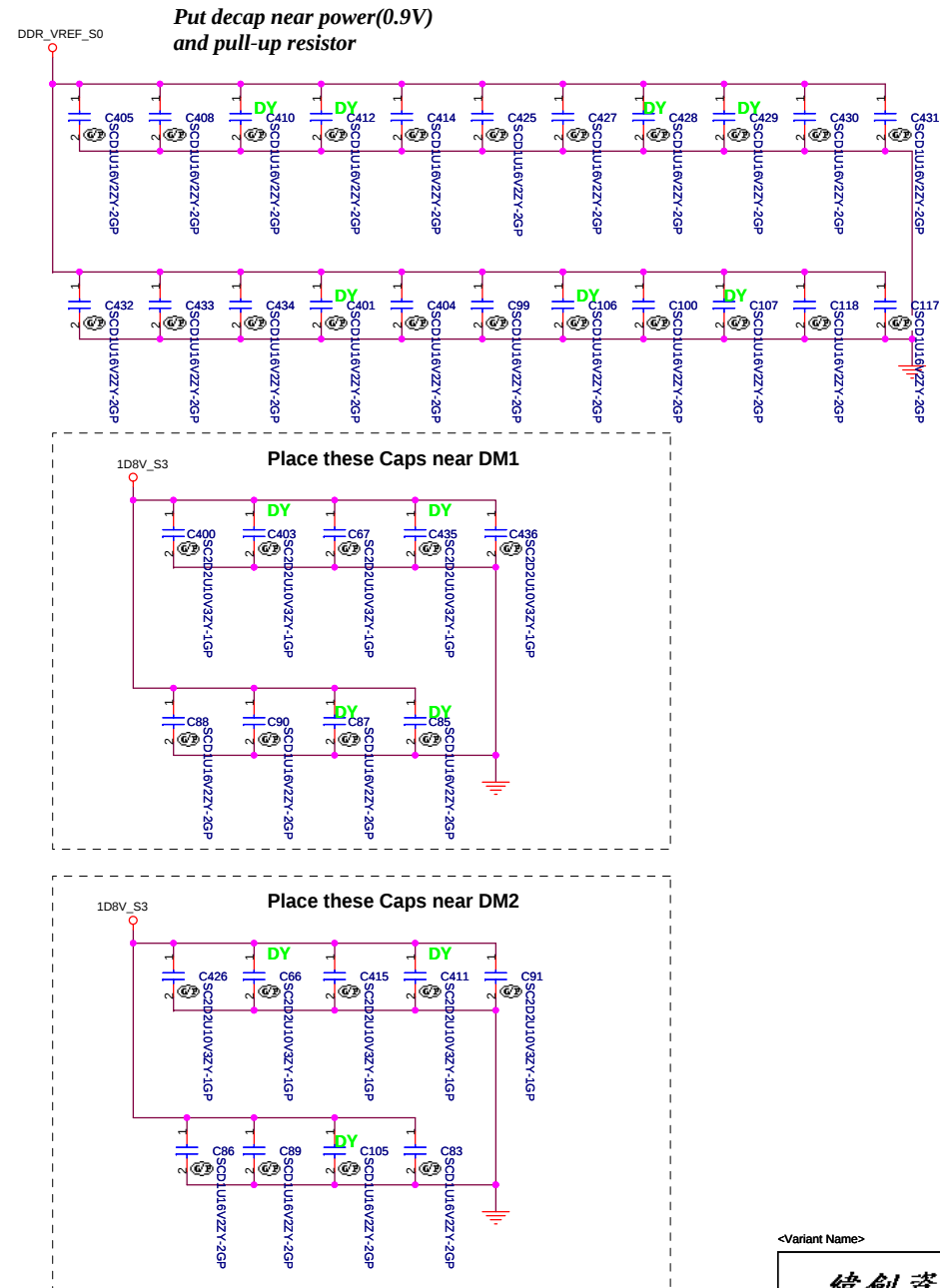
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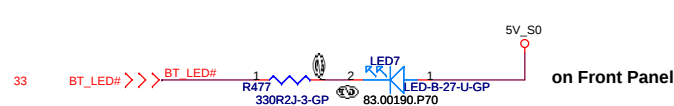
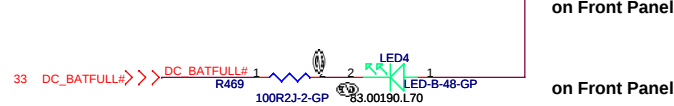
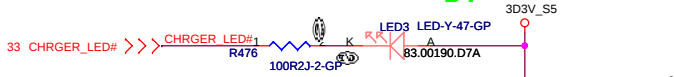
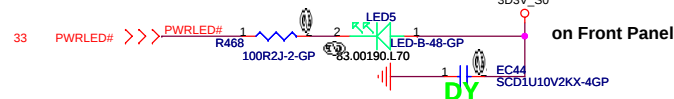
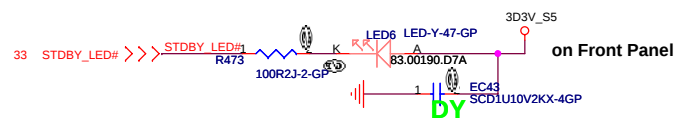
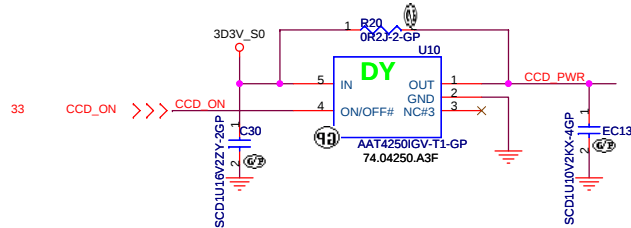
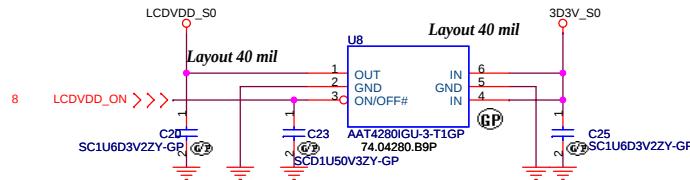
Sheet 11 of 46

PARALLEL TERMINATION



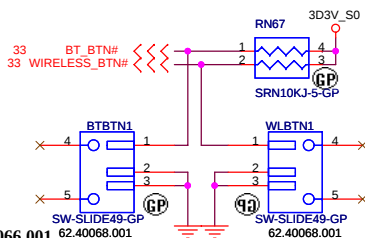
Decoupling Capacitor





LED	V	V	V	V
Button	V	V	V	V
	Bluetooth	Wireless	Charger	Power2

2nd source: 62.40066.001

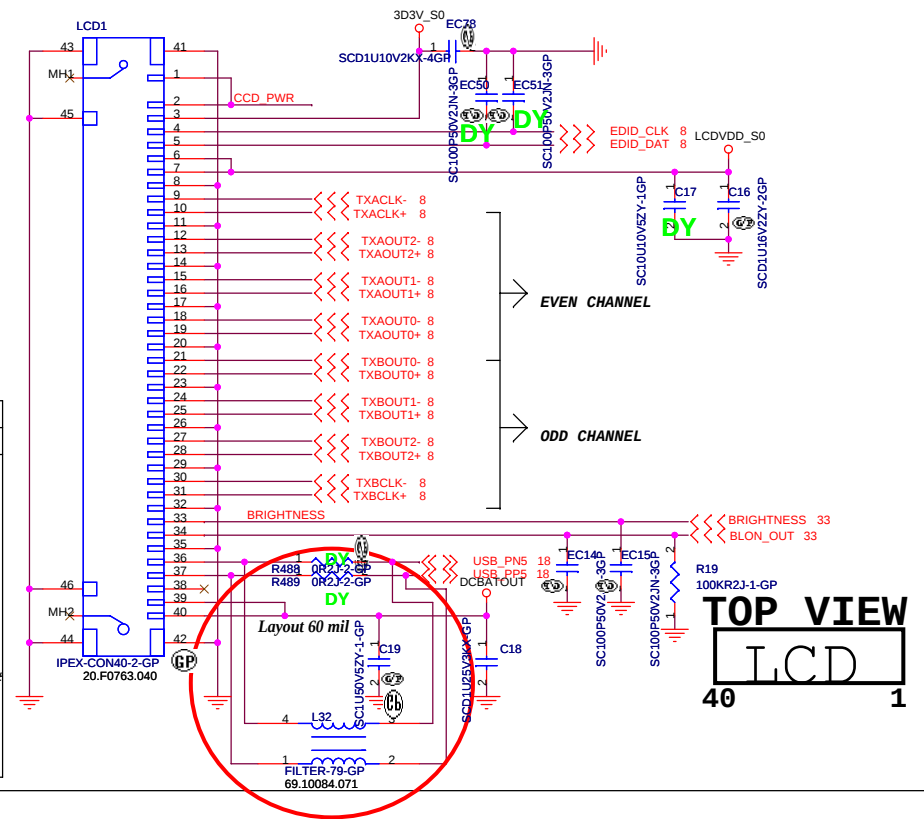


Pin	Symbol
1	3.3V
2	USB-
3	USB+
4	GND
5	GND

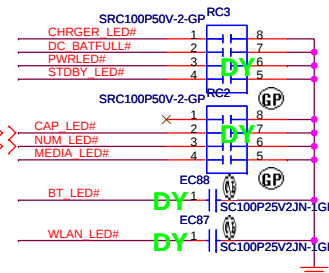
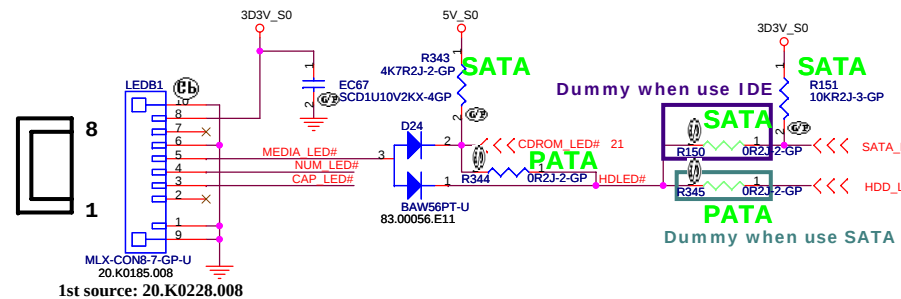
Pin	Symbol
1	Vin
2	Vin
3	PWM
4	BLON
5	GND
6	GND

Pin	Symbol
1	3V_S0
2	PWRBTN#
3	PROGRAM#
4	EBUTTON#
5	INTERNET#
6	MAIL#
7	NC
8	MAIL_LED#
9	PWR_B_LED#
10	NC
11	INT_MICP
12	INT_MICN

LCD/INVERTER/CCD CONN



LED BD CONN



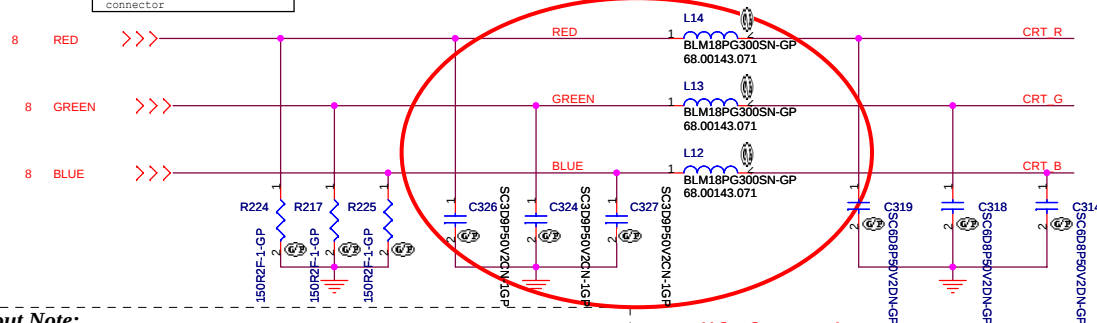
<Variant Name>

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Title			
LCD / LAUNCH / LEDs			
Size A3	Document Number Gards-5		Rev -1
Date:	Wednesday, April 26, 2006	Sheet 13	of 46

CRT I/F & CONNECTOR

Layout Note:
Place these resistors
close to the CRT-out
connector

Ferrite bead impedance: 30 ohm@100MHz

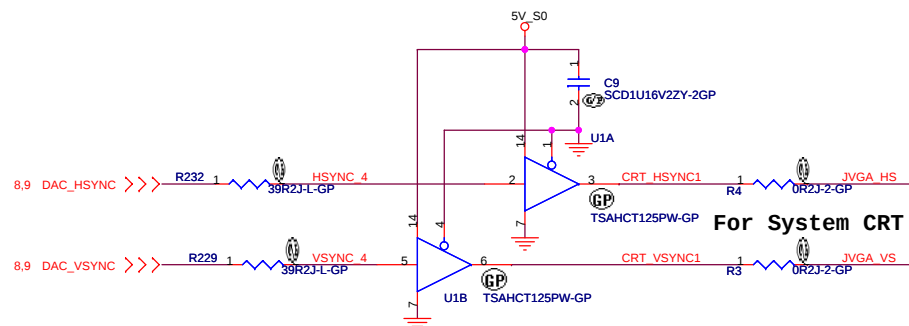


Layout Note:

* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

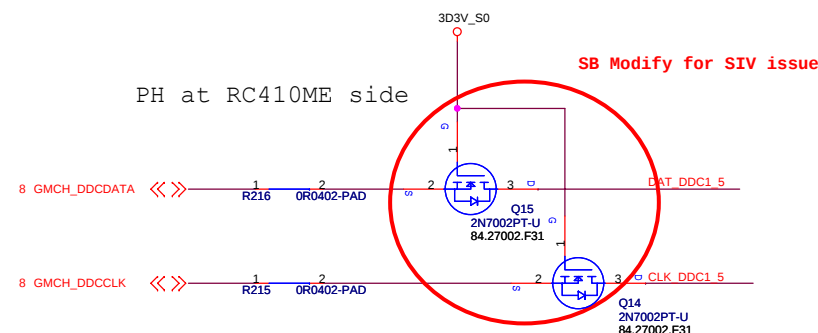
SB Modify for SIV issue

Hsync & Vsync level shift



For System CRT

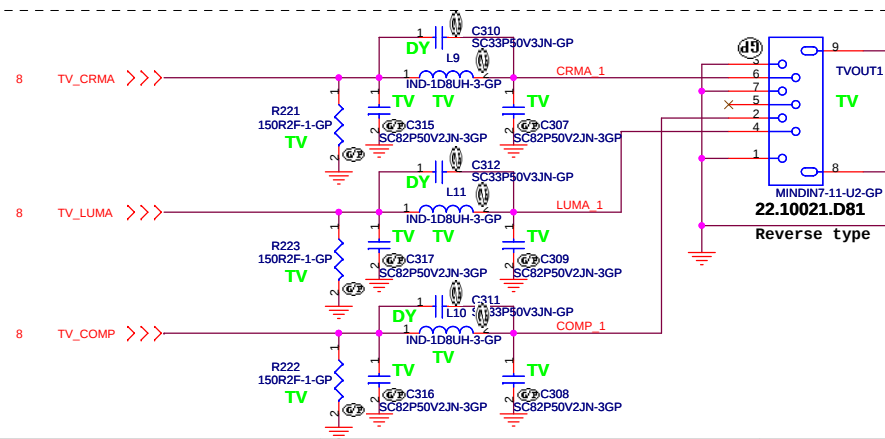
DDC_CLK & DATA level shift



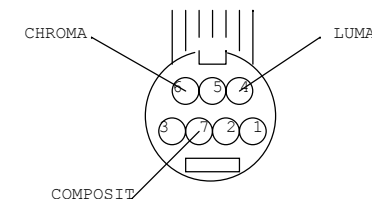
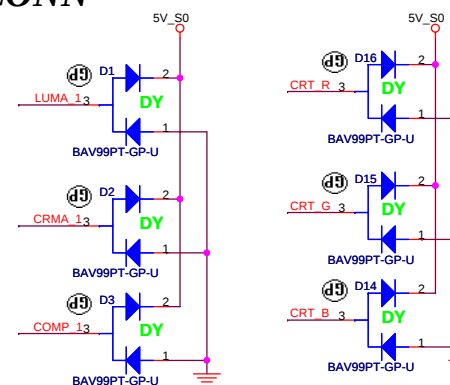
SB Modify for SIV issue

PH at RC410ME side

TV OUT CONN



Reverse type



<Variant Name>

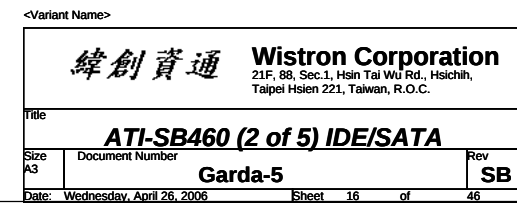
緯創資通

Wistron Corporation

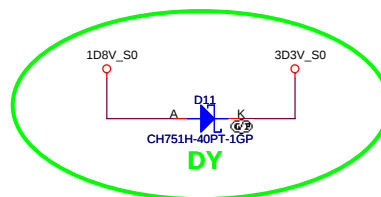
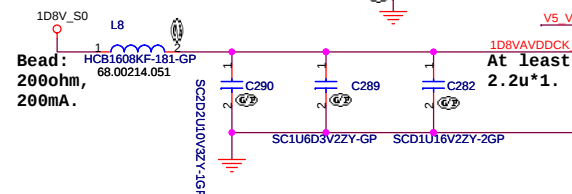
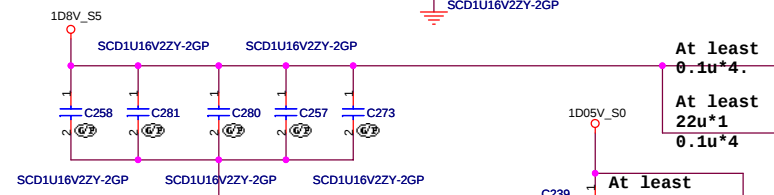
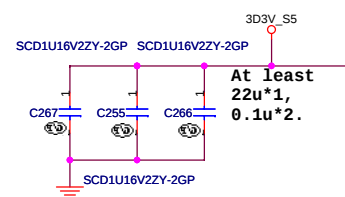
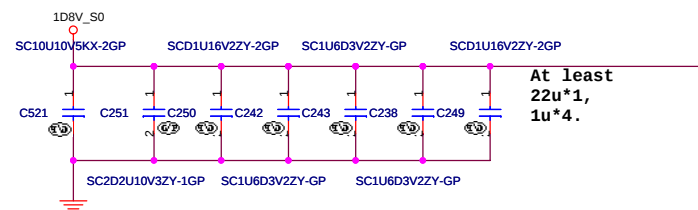
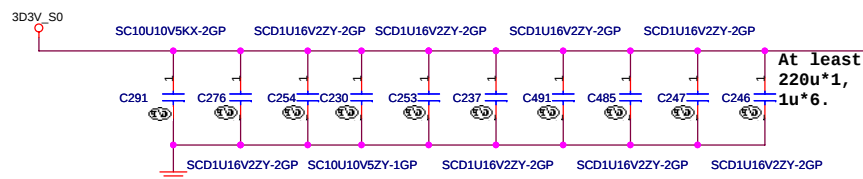
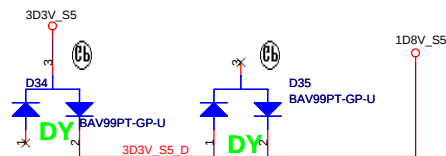
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CRT/TV Connector			Rev
Size A3	Document Number	Garda-5	SB
Date: Wednesday, April 26, 2006	Sheet 14	of 46	

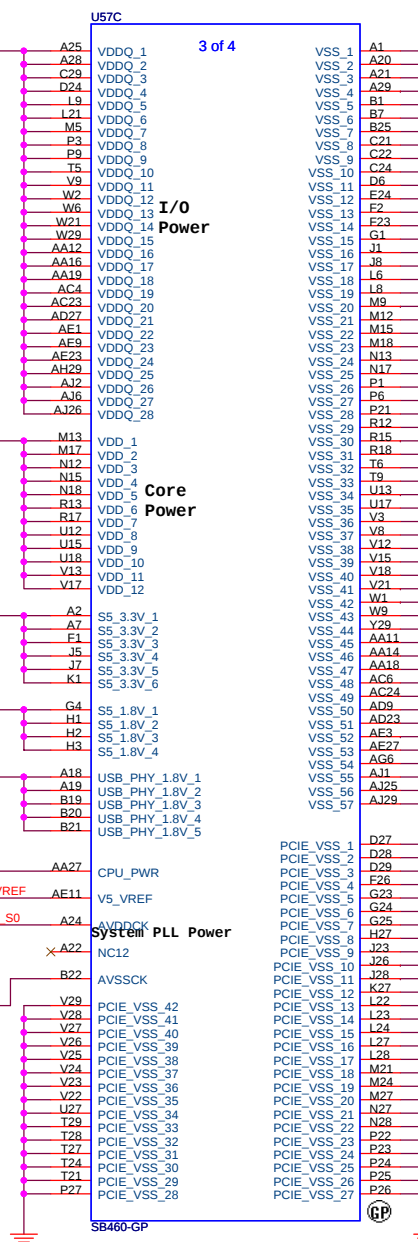




3D3V_S0 must never exceed V5_VREF by more than 0.6V.



1D8V_S0 must never exceed 3D3V_S0 by more than 0.6V.
1D8V_S0 must start ramping up within 1ms of 3D3V_S0 starting to ramp p.



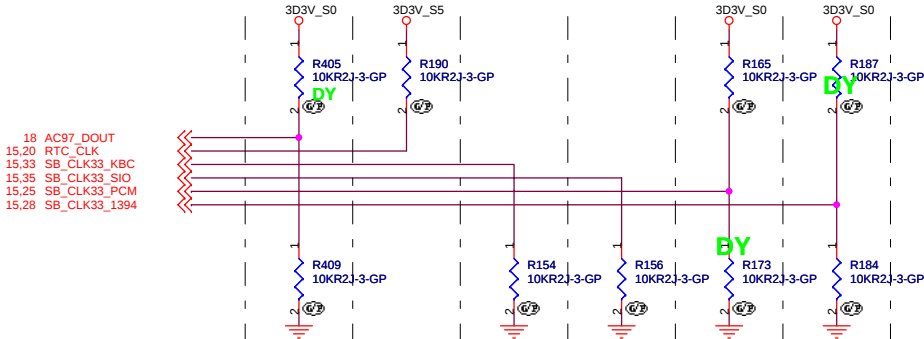
<Variant Name>

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title **ATI-SB460 (3 of 5) POWER**

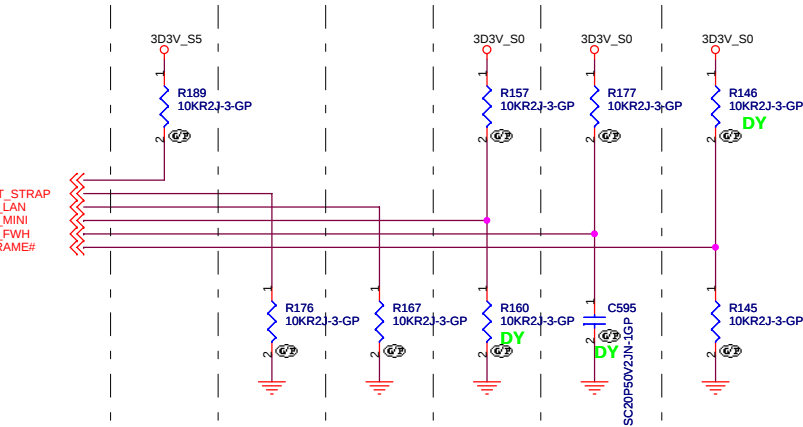
Size A3	Document Number Garda-5	Rev SA
Date: Wednesday, April 26, 2006	Sheet 17 of 46	

REQUIRED STRAPS



18 AC97_DOUT
15,20 RTC_CLK
15,33 SB_CLK33_KBC
15,35 SB_CLK33_SIO
15,25 SB_CLK33_PCM
15,28 SB_CLK33_1394

15 RTC_IRQ#
15 SPDIF_OUT_STRAP
15,23 SB_CLK33_LAN
15,32 SB_CLK33_MINI
15,36 SB_CLK33_FWH
15,33,35,36 LPC_LFRAME#



PCI_CLK0 PCM
PCI_CLK1 IEEE1394
PCI_CLK2 LAN
PCI_CLK3 MINI
PCI_CLK4 KBC
PCI_CLK5 FWH
PCI_CLK6 SIO
PCI_CLK7 SPDIFOUT

	SB460				SB600	
	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INT. USB PLL48	CPU IF=K8	ROM TYPE: H, H = PCI ROM H, L = LPC I ROM	ROM TYPE: H, H = PCI ROM H, L = SPI ROM
PULL LOW	DISABLE DEBUG STRAPS	EXTERNAL RTC	USE EXT. USB 48MHZ SOURCE	CPU IF=P4	L, H = LPC II ROM L, L = FWH ROM	L, H = LPC ROM L, L = FWH ROM

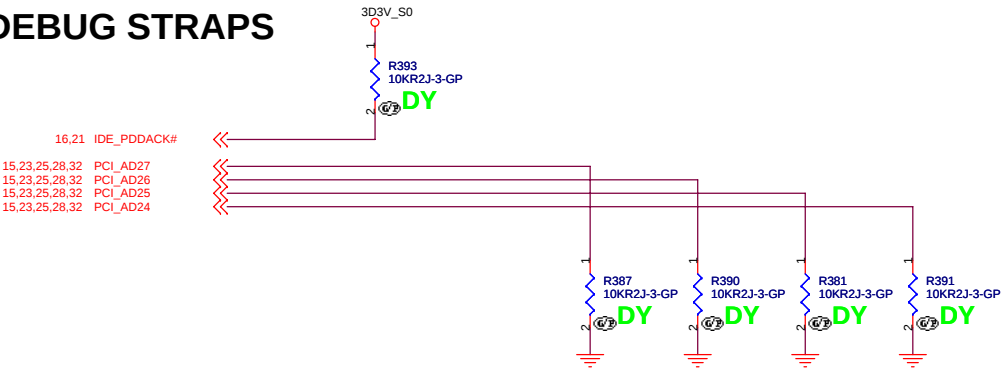
NOTE: FOR SB460, PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

Require upper 12 addr bits set to "1".

	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON	SIO 24MHz	48M XTAL MODE	USB PHY POWERDOWN DISABLE	PCIE LANE AUTO DETECT	ENABLE THERMTRIP#
PULL LOW	AUTO PWR ON	SIO 48MHz	48MHZ OSC MODE	USB PHY POWERDOWN ENABLE	PCIE LANE FORCING TO 2 LANES	DISABLE THERMTRIP#

USB wake from S5 supported.

DEBUG STRAPS

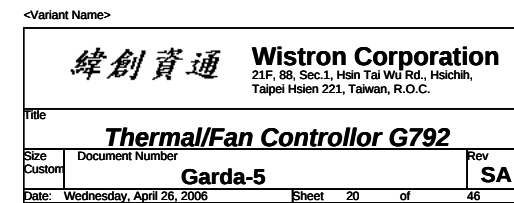
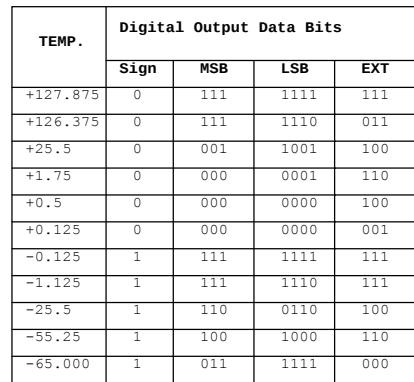


16,21 IDE_PDDACK#
15,23,25,28,32 PCI_AD27
15,23,25,28,32 PCI_AD26
15,23,25,28,32 PCI_AD25
15,23,25,28,32 PCI_AD24

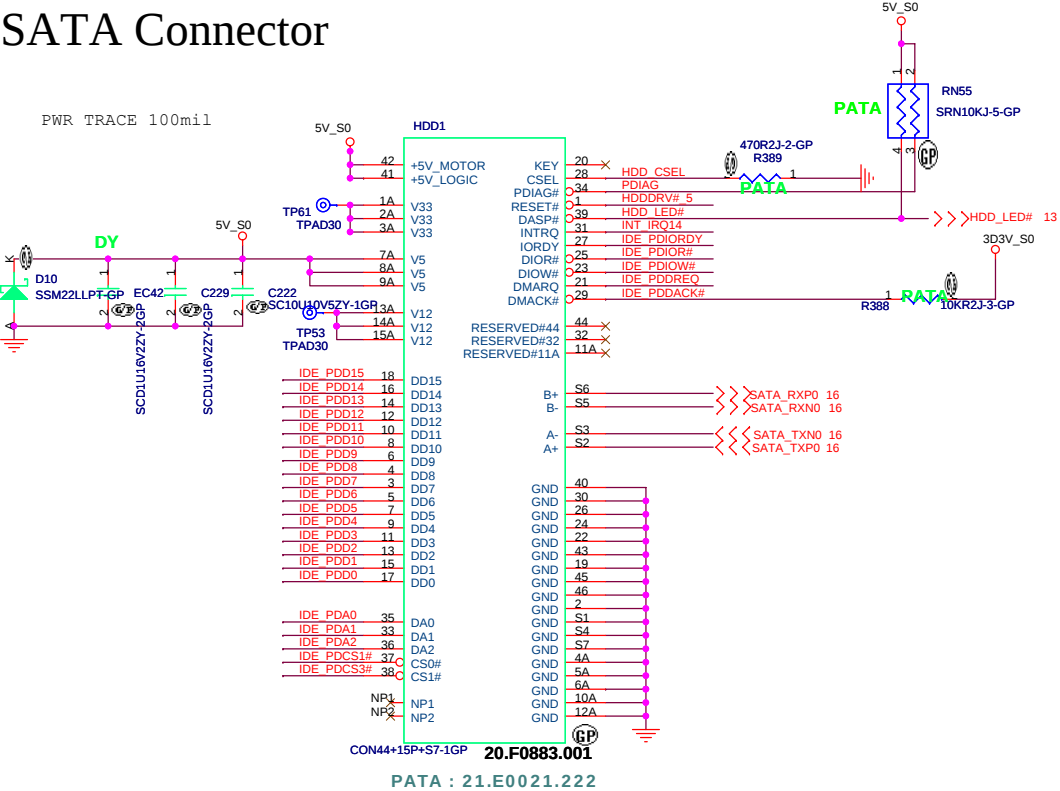
	IDE_DACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET		BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	
PULL LOW	USE SHORT RESET		USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	NOTE: FOR SB460, PCI_AD23 IS RESERVED

SB460 ONLY SB600 ONLY

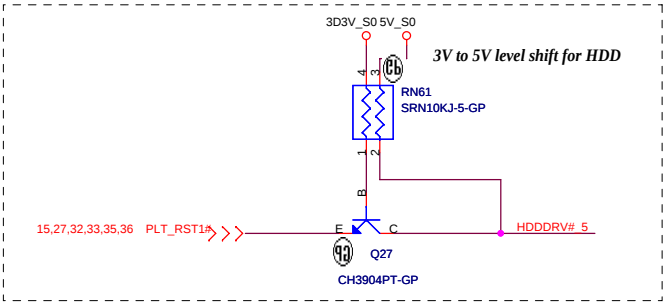
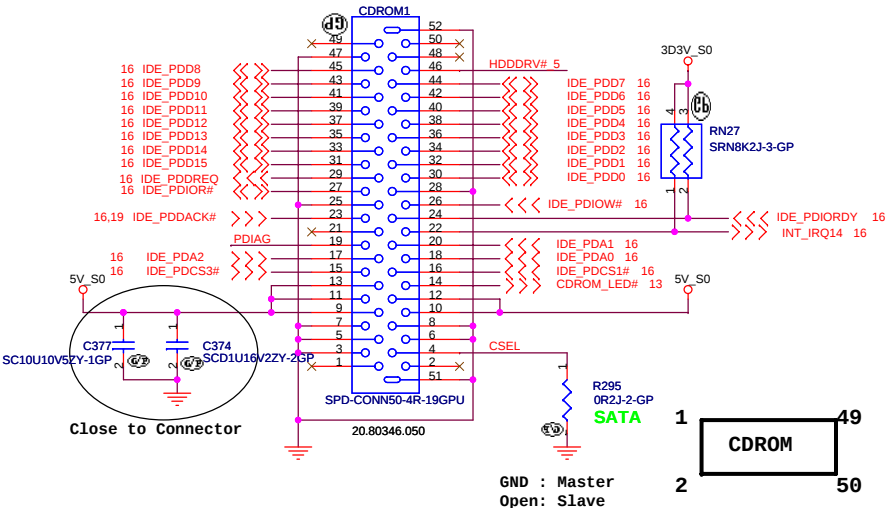
SB600 ONLY



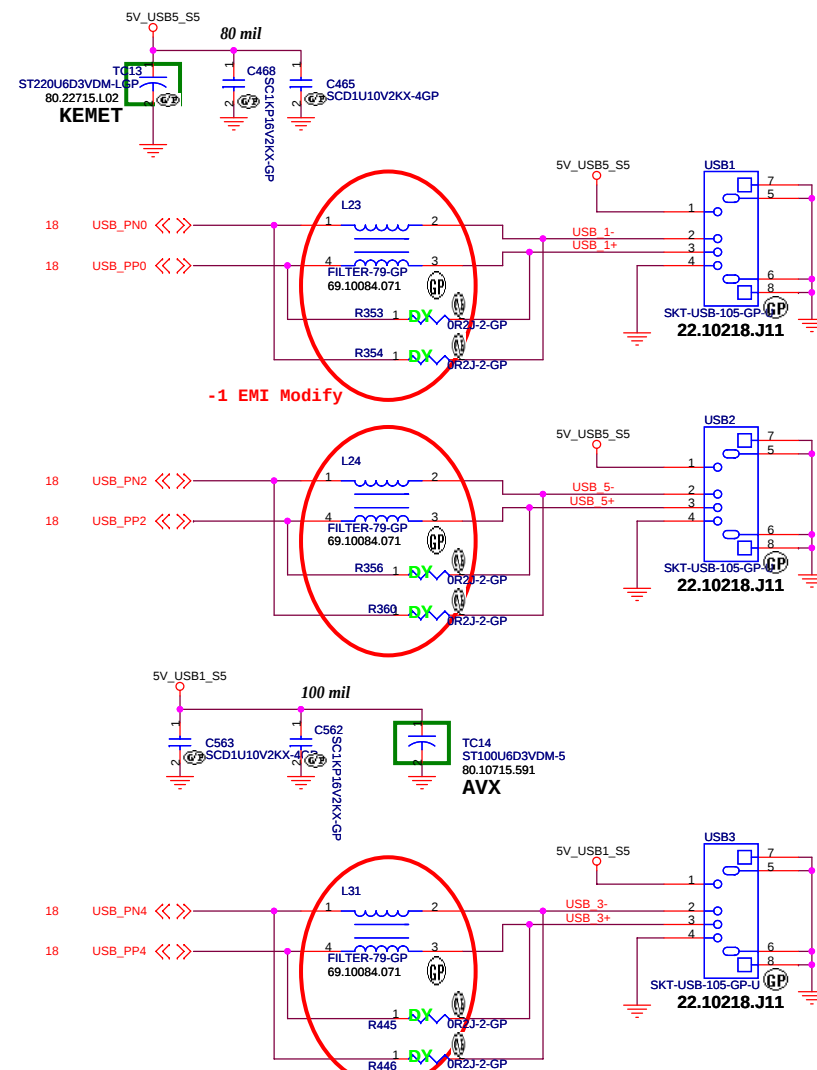
SATA Connector



CDROM Connector



USB PORT

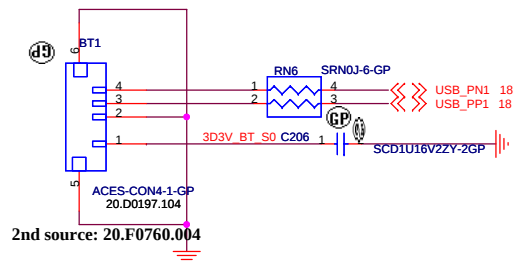
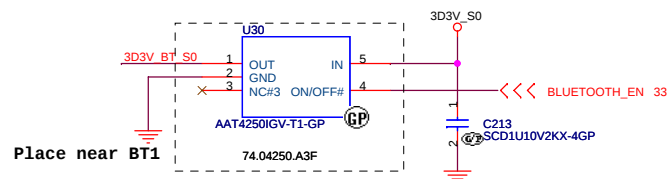
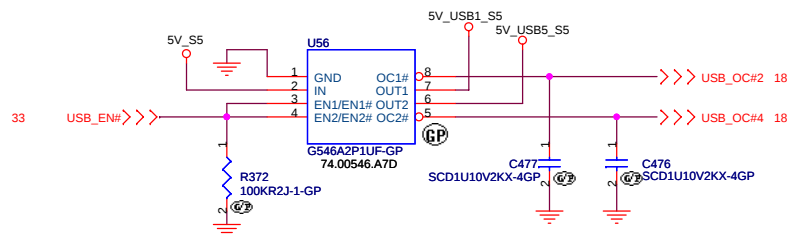


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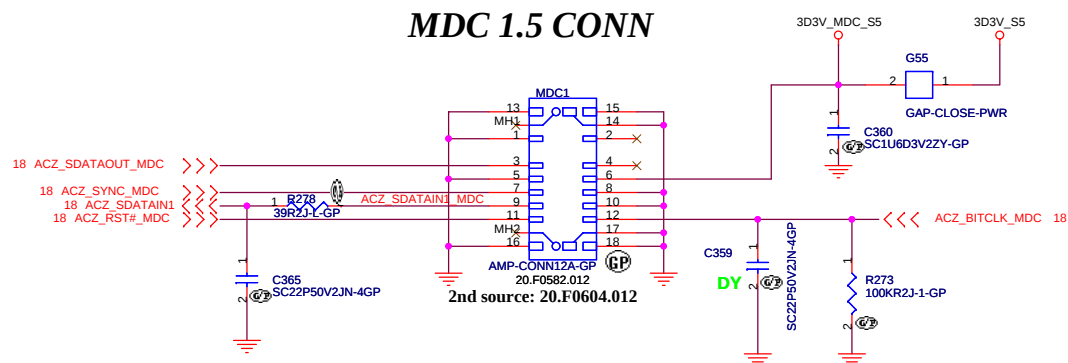
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

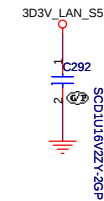
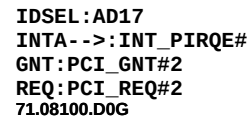
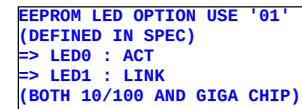
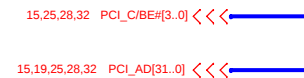
Title			Rev
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A3			-1
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BLUETOOTH MODULE CONNECTOR



MDC 1.5 CONN





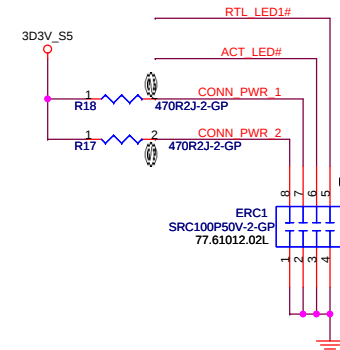
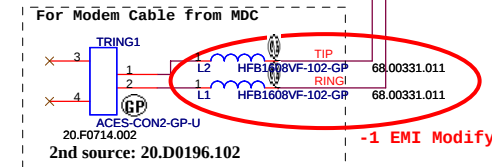
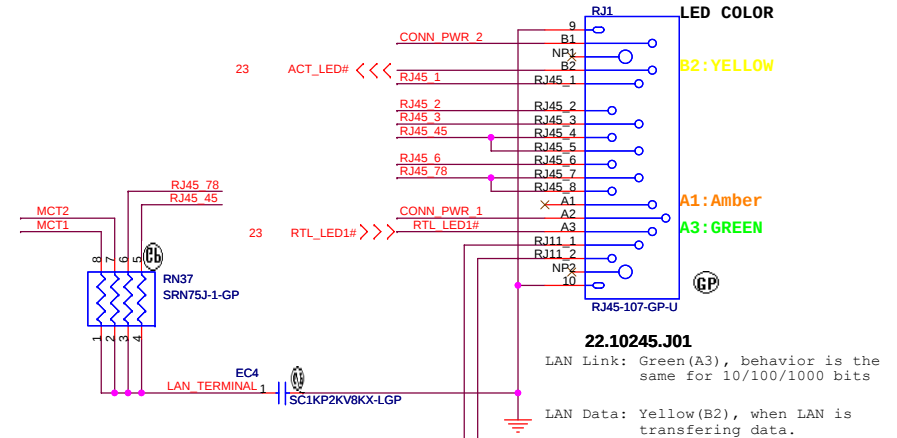
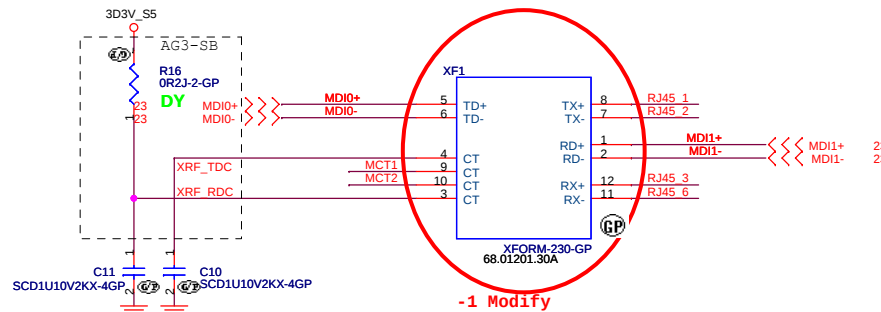
LAN Connector

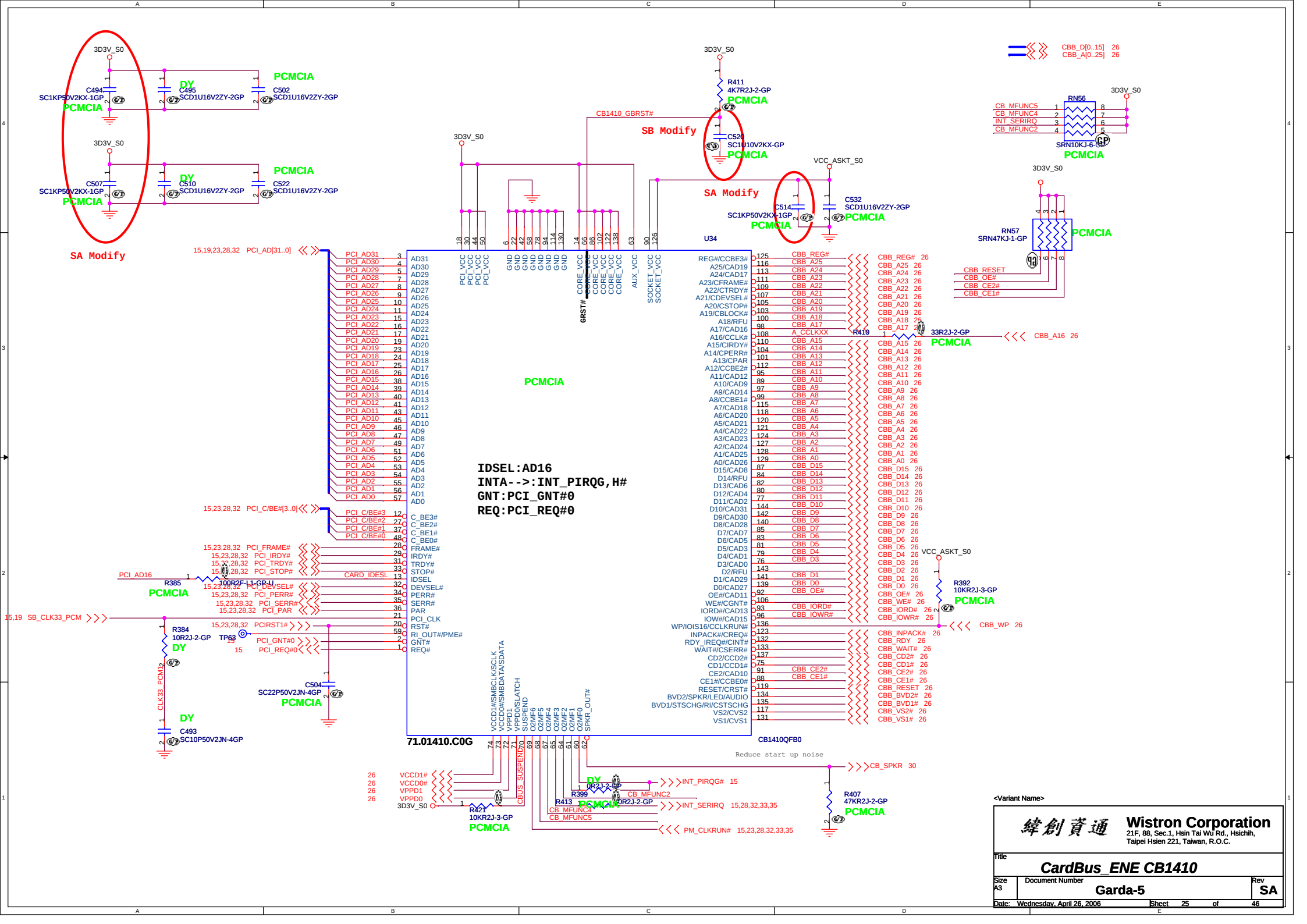
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width,12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat,except RJ-45 moat.

RJ11 signal must leave the other signal or power plane 100mil.

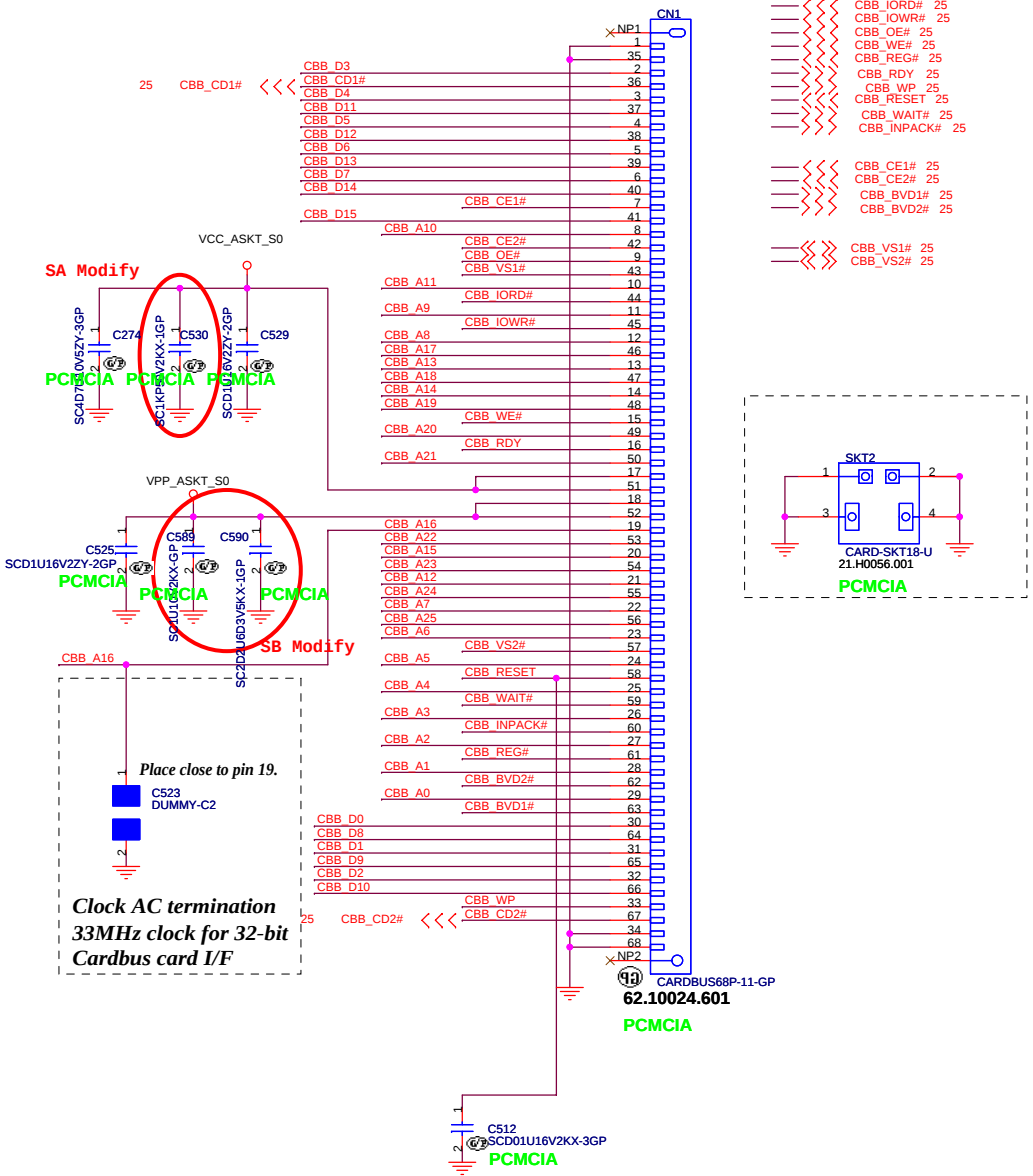
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

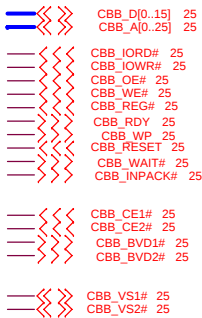




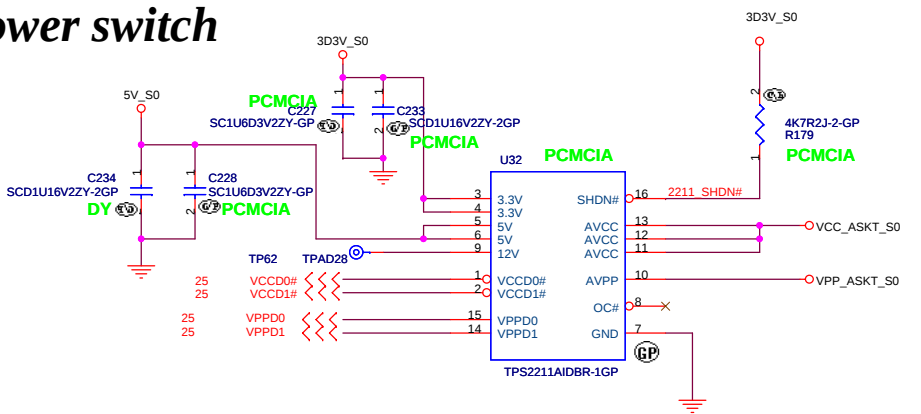
PCMCIA Socket



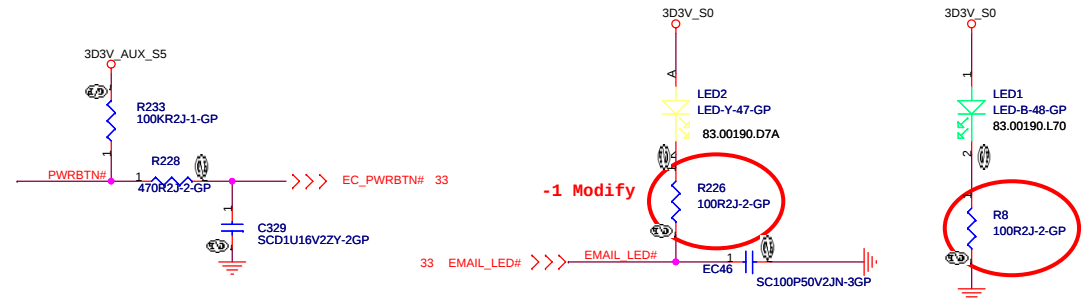
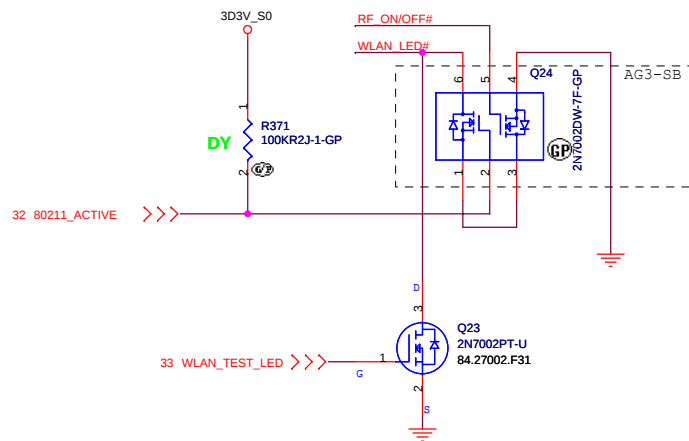
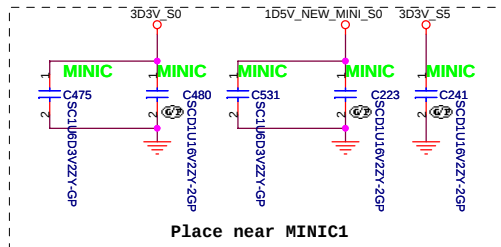
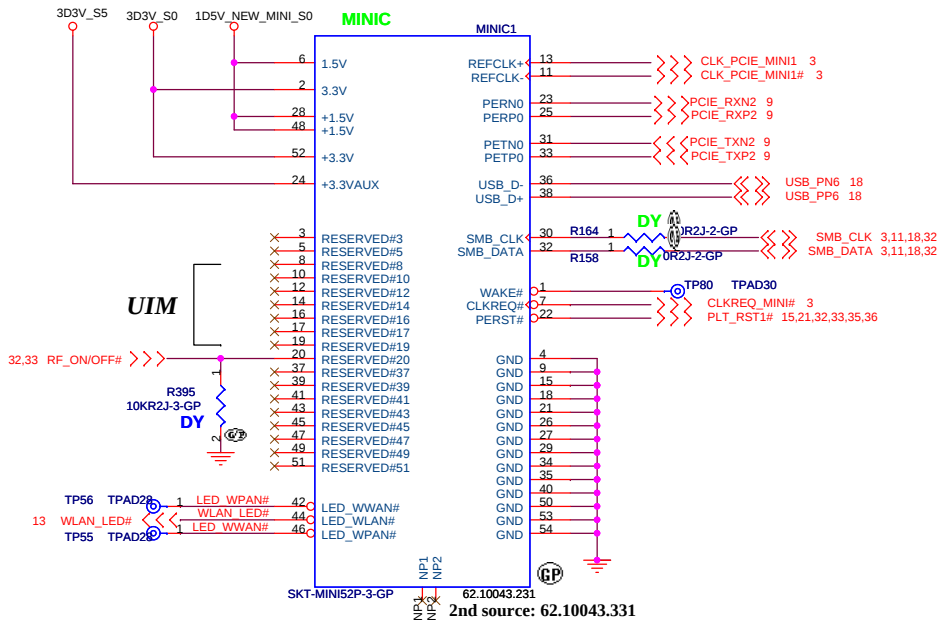
Cardbus I/F



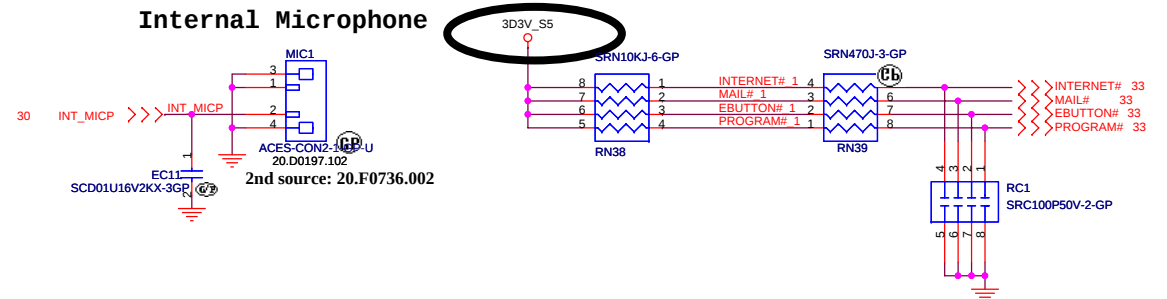
Power switch



Mini Card Connector

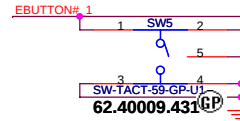


Internal Microphone



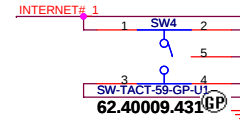
E-Button

TOP VIEW RIGHT 4



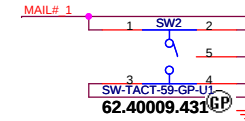
Internet Button

TOP VIEW RIGHT 3



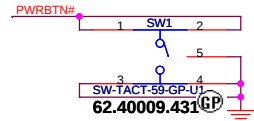
Mail Button

TOP VIEW RIGHT 2



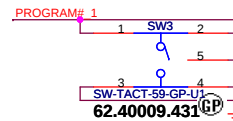
Power Button

TOP VIEW RIGHT 1



Program Button

TOP VIEW RIGHT 5



LED	V	V	V	V	V
Button	Program Button	E-Button	Internet Button	Mail Button	Power Button

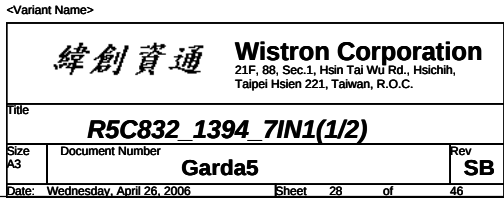
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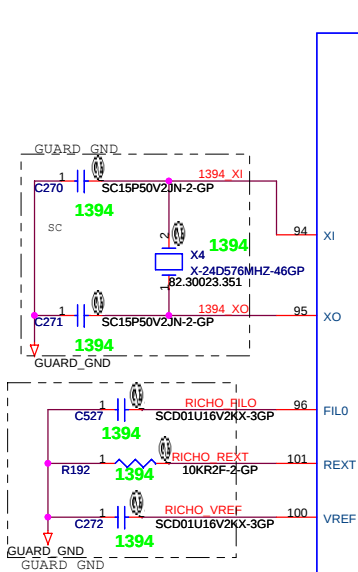
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI CARD / Launch Button**

Size A3 Document Number: **Garda-5** Rev: **-1**

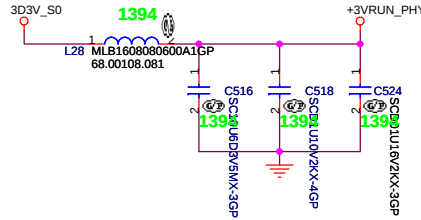
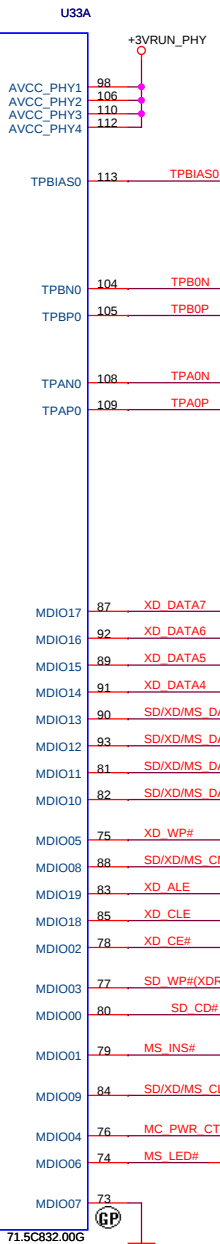
Date: Wednesday, April 26, 2006 Sheet 27 of 46



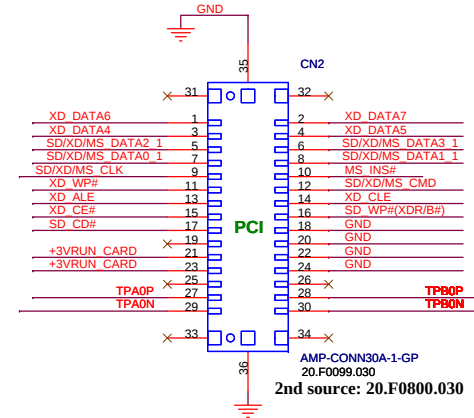
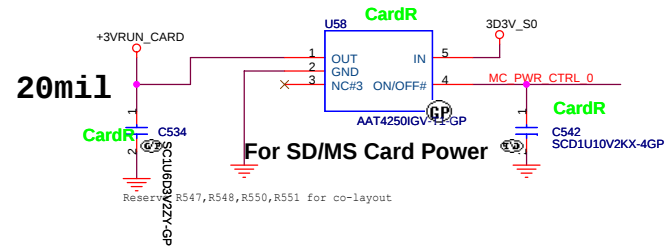
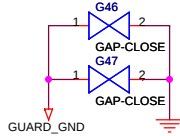
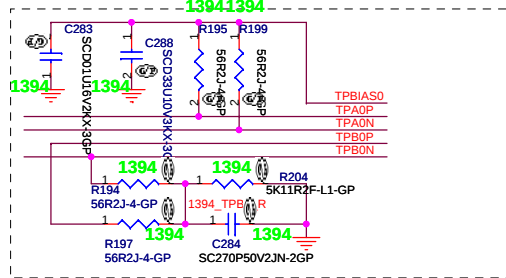


IEEE1394/SD

PCI



CLOSE TO CHIP

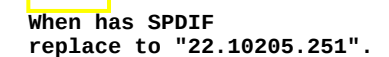


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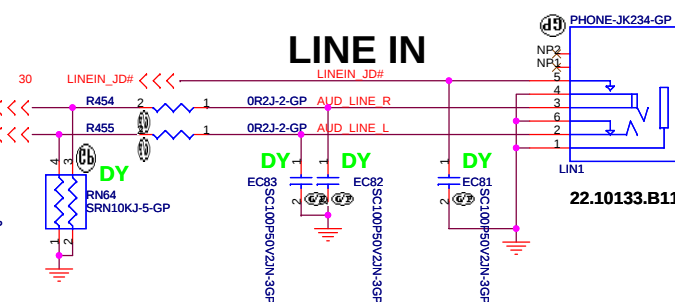
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

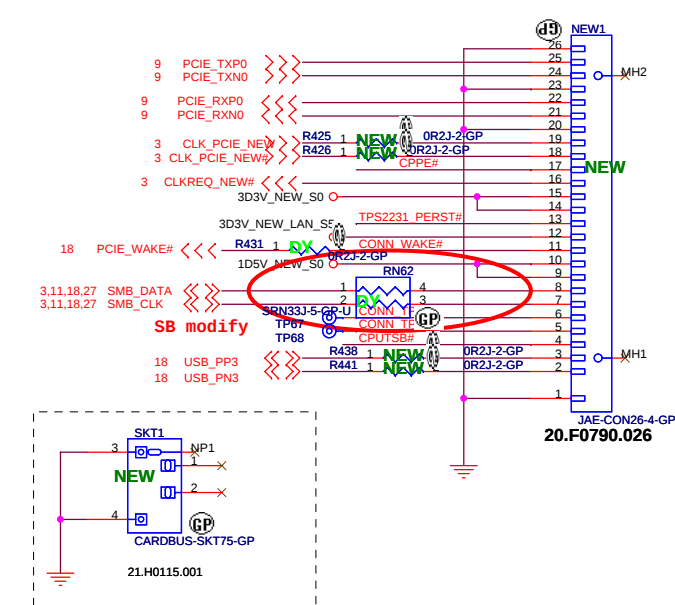
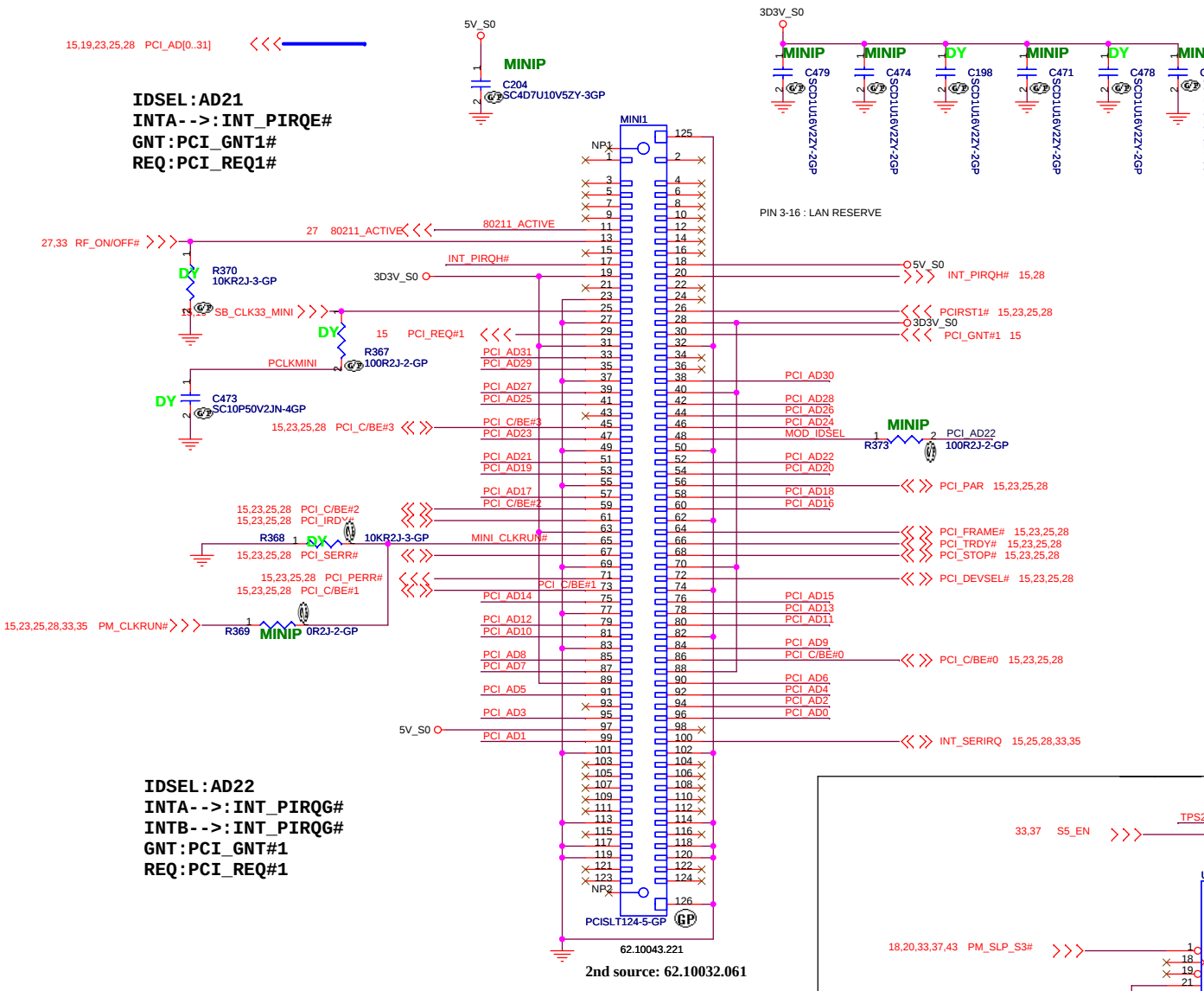
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Size	Document Number	Rev	
A3	Garda-5	SA	
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**I/P signal level
need +5V level**



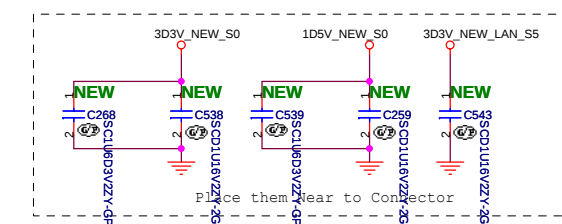
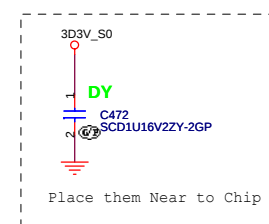
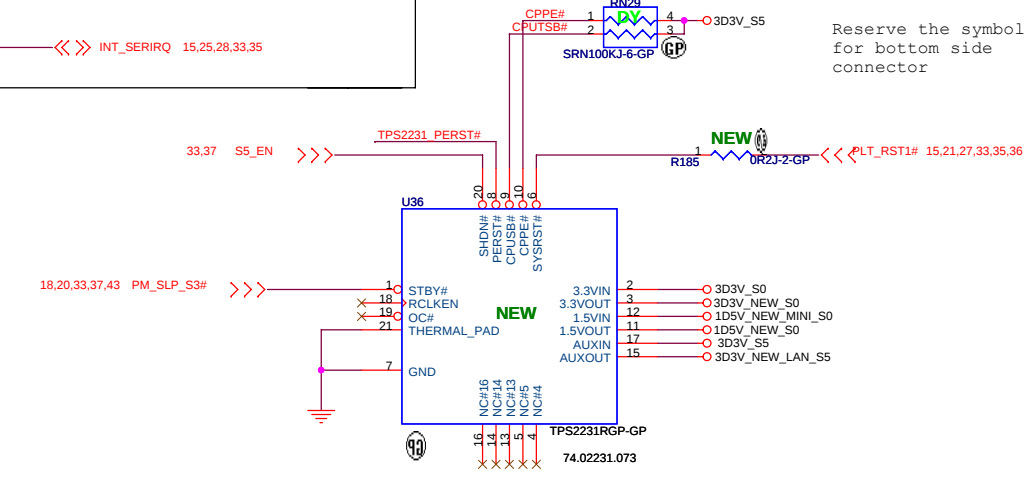
LINE IN



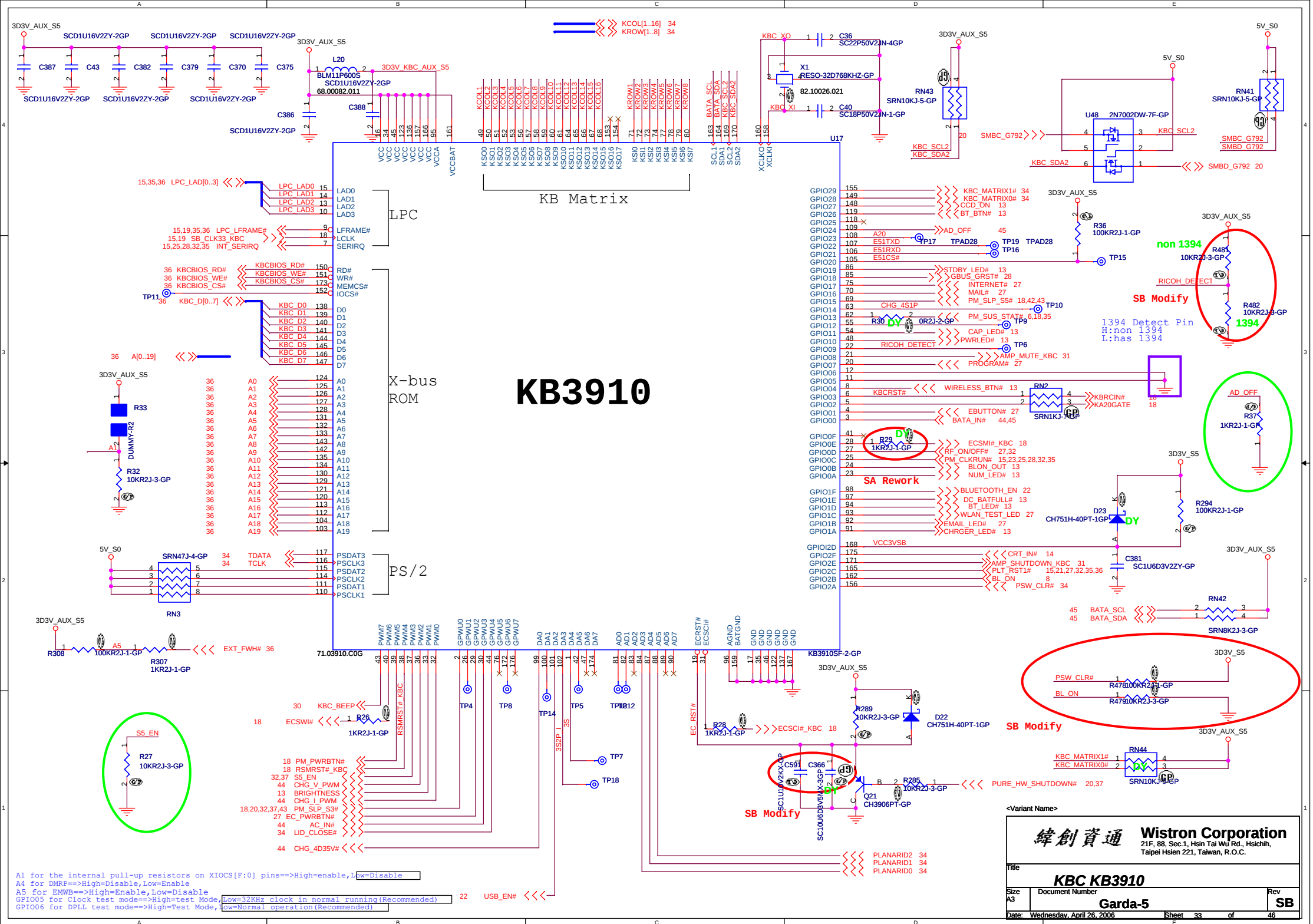


NEWCARD Connector

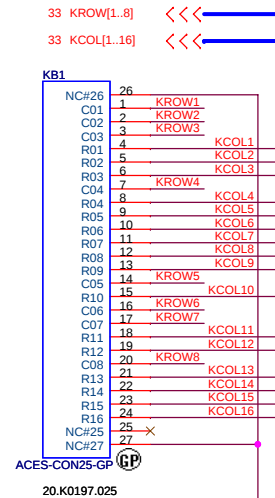
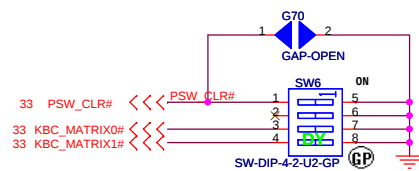
Reserve the symbol
for bottom side
connector



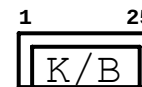
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Size	Document Number	Rev
A3	Garda5	SB
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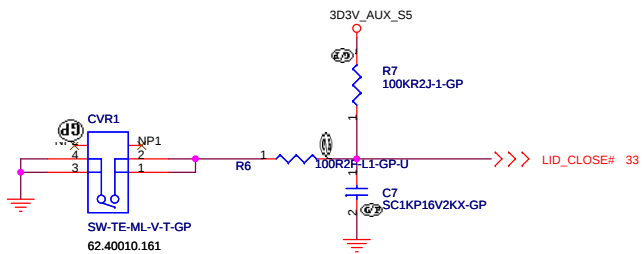
Internal KeyBoard Connector



2nd source: 20.K0198.025



COVER SWITCH

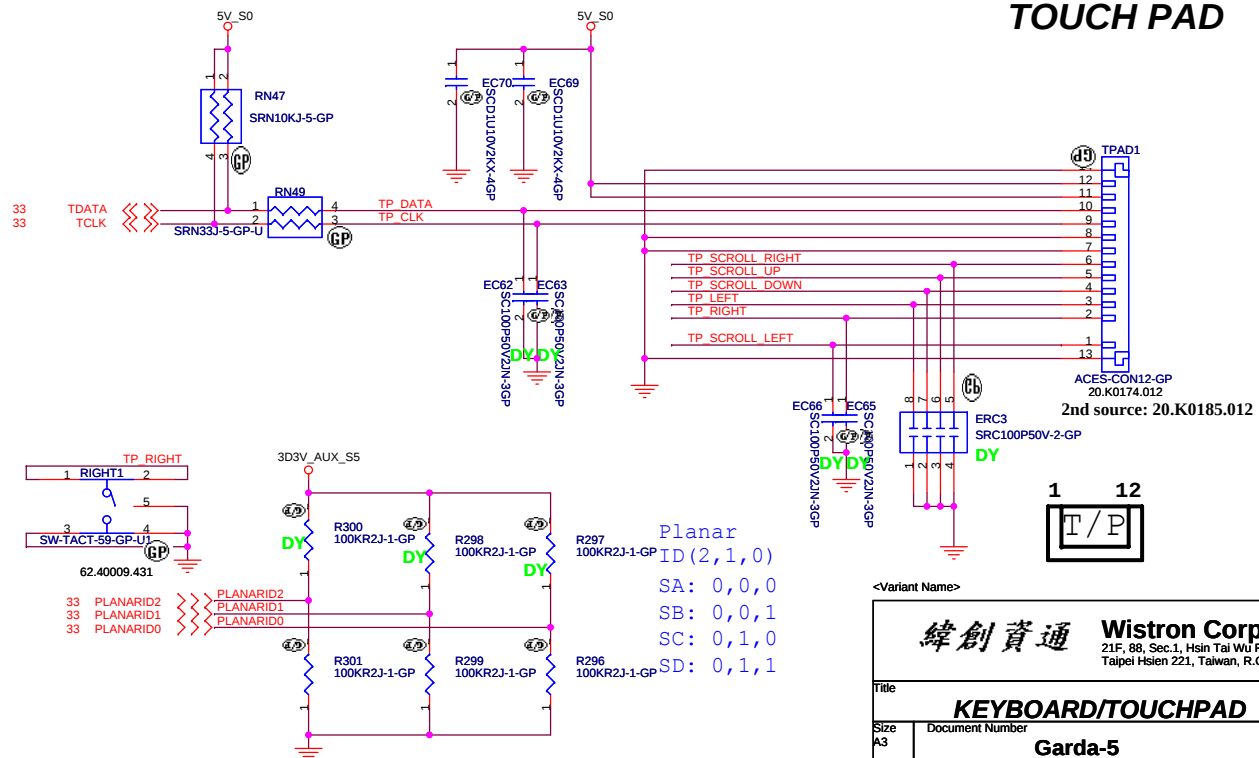
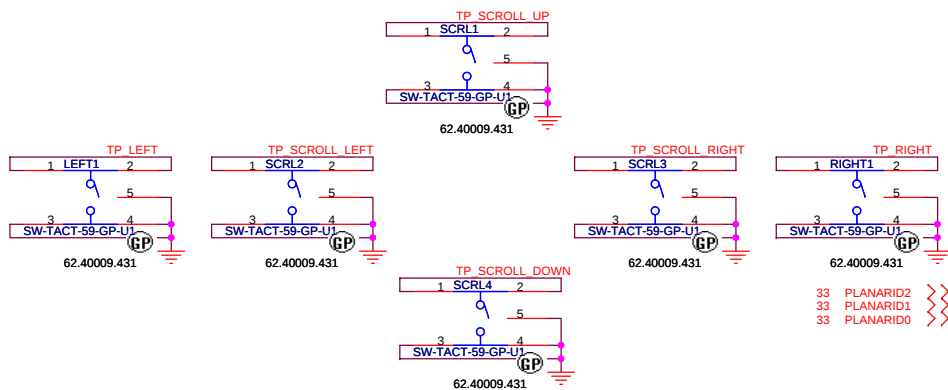


Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0

	Low Active
PSW_CLR#	1 - 5 ON
NC	2 - 6 ON
KBC_MATRIX1	3 - 7 ON
KBC_MATRIX2	4 - 8 ON

SCROLL KEY



<Variant Name>

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

KEYBOARD/TOUCHPAD

Size

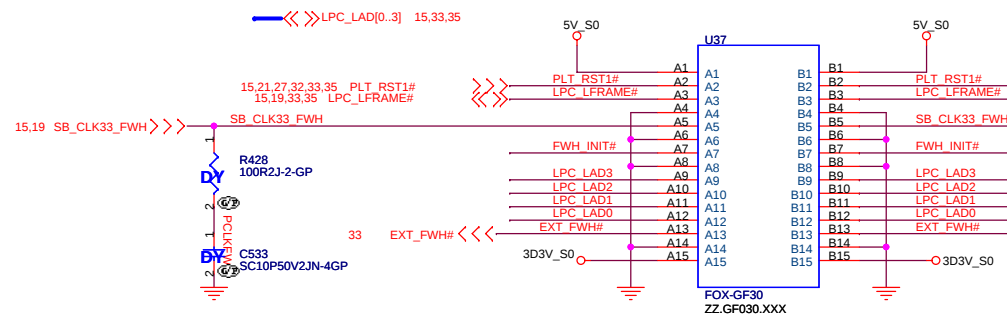
Document Number

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Rev	
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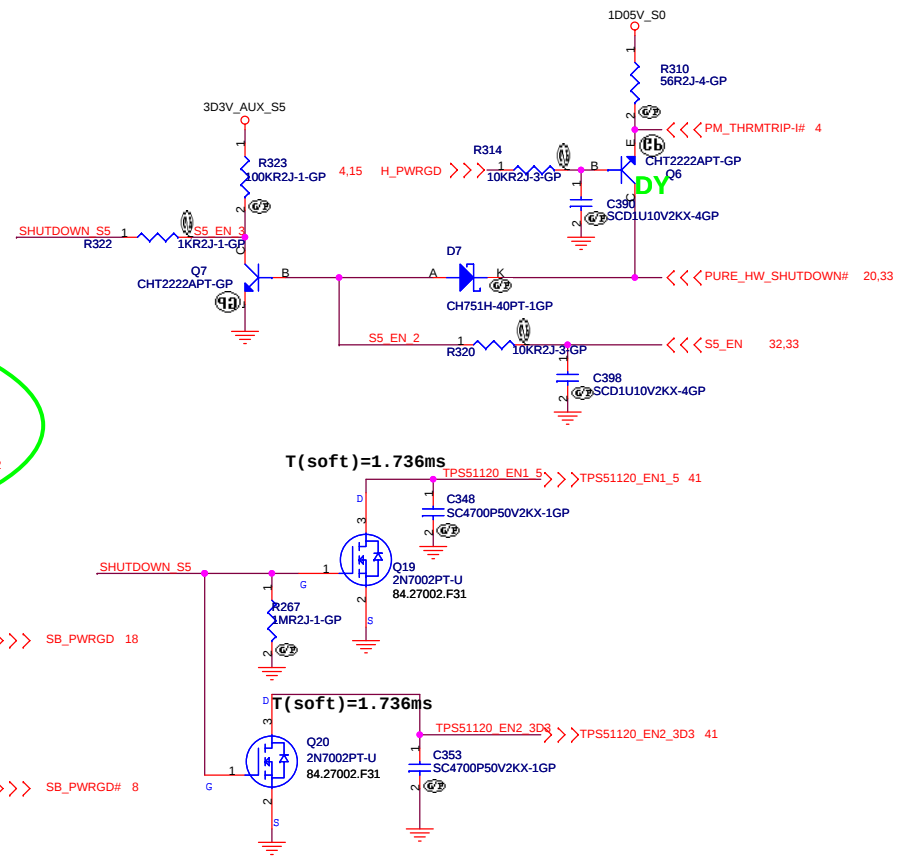
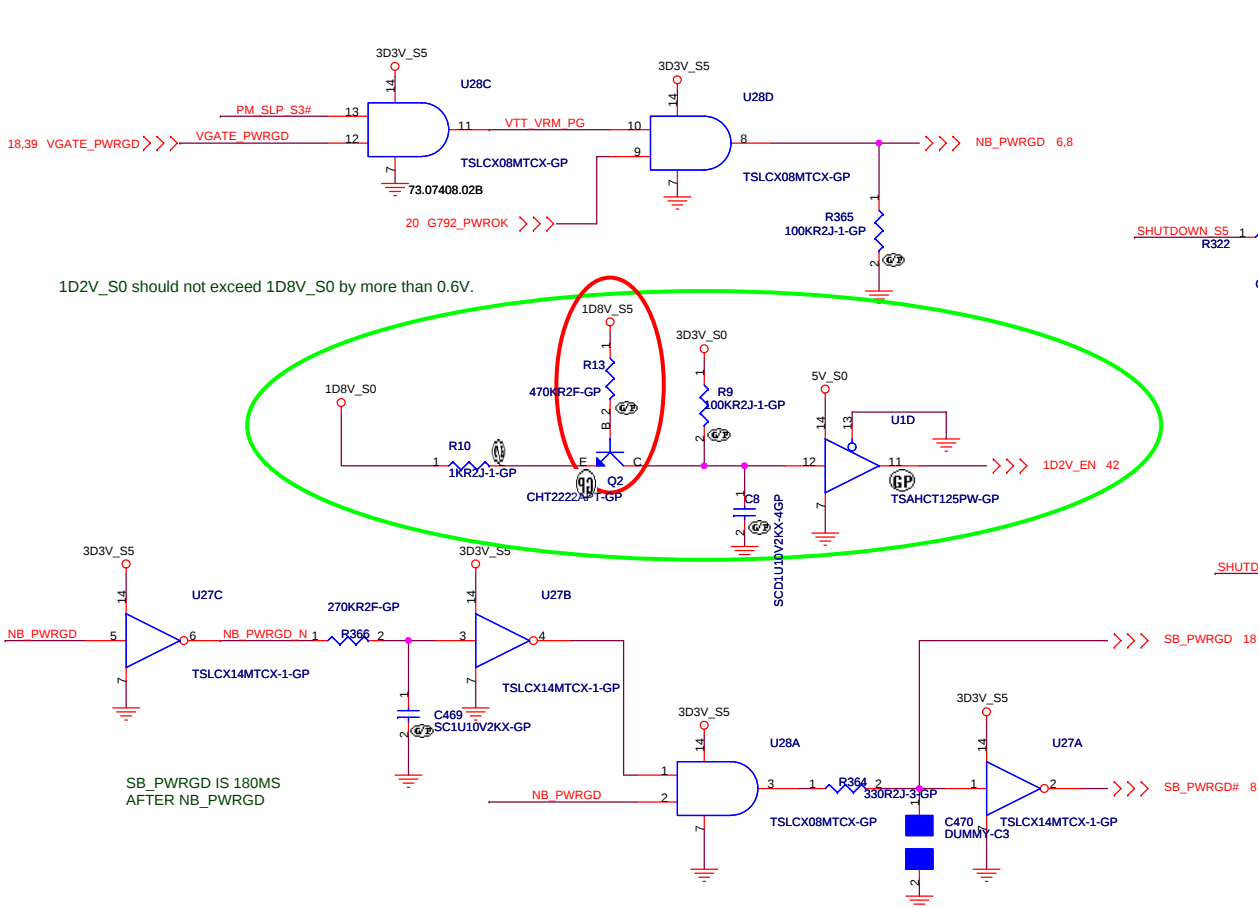
Date: Wednesday, April 26, 2006

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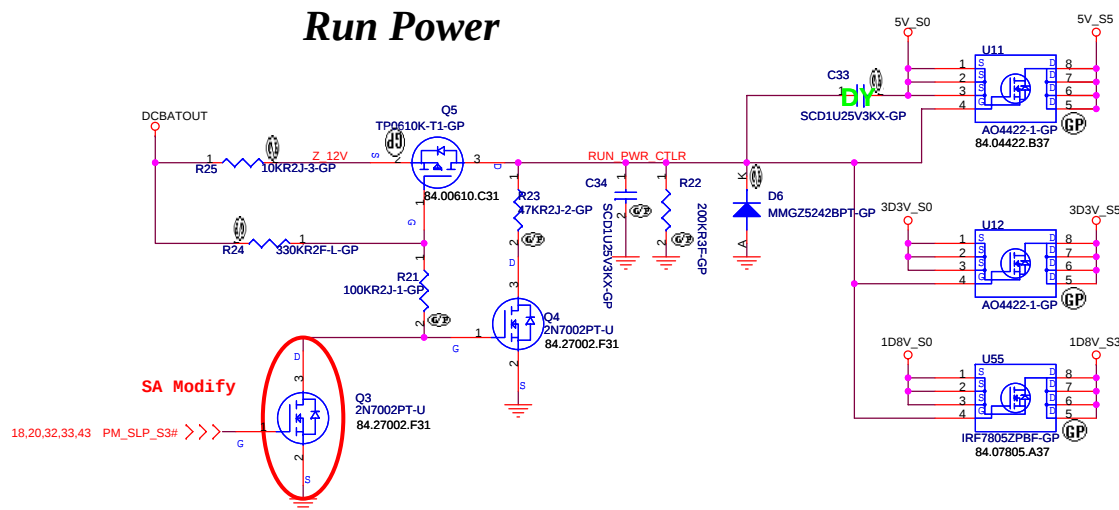


TOP VIEW

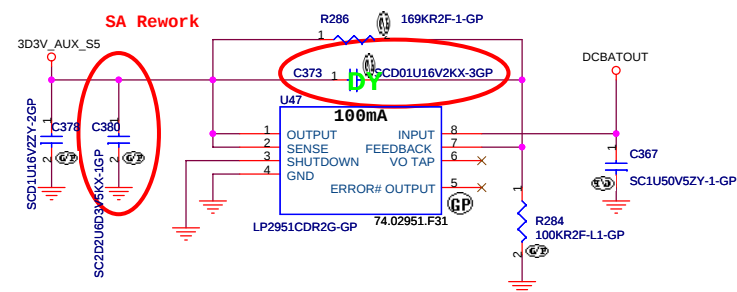




Run Power

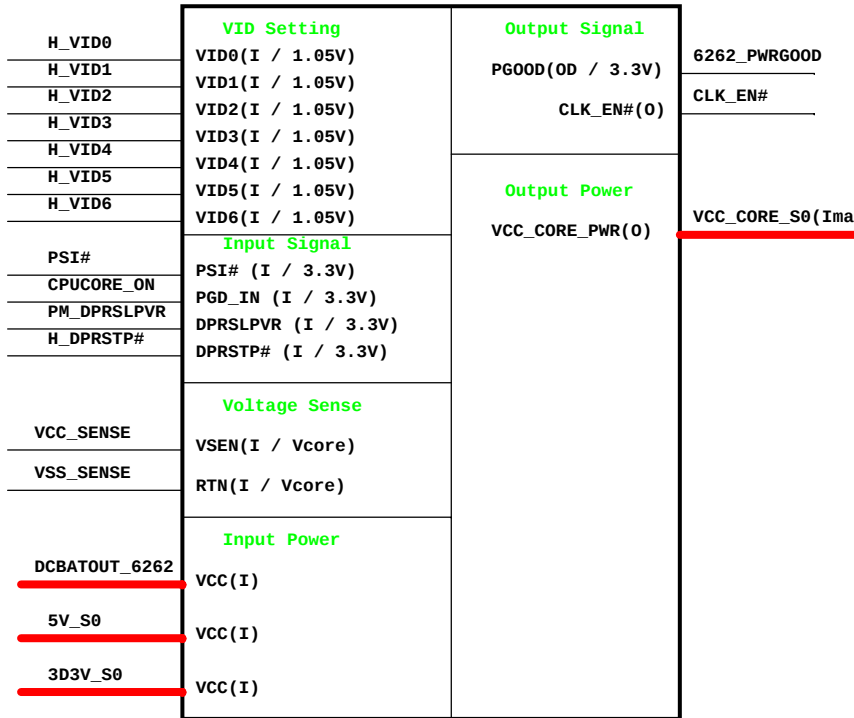


Aux Power

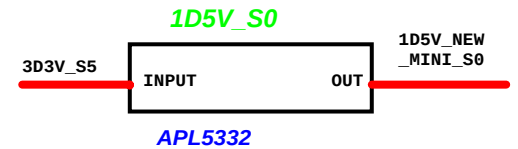
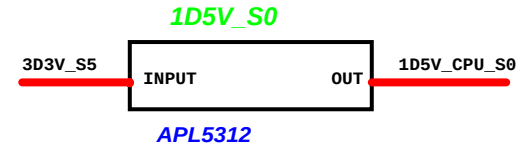
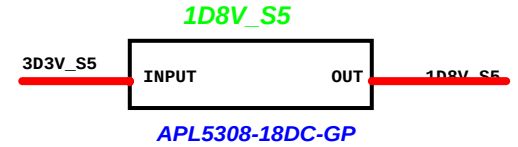
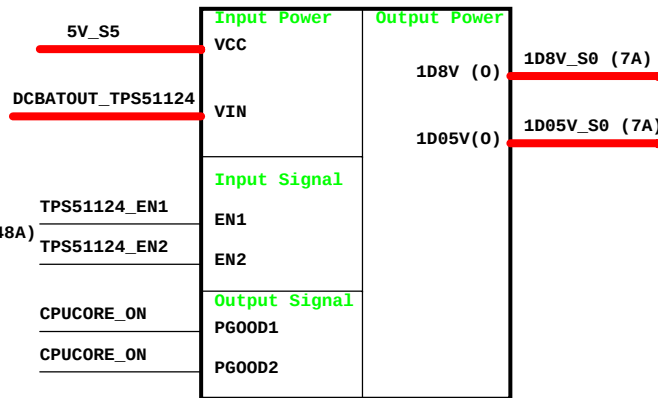


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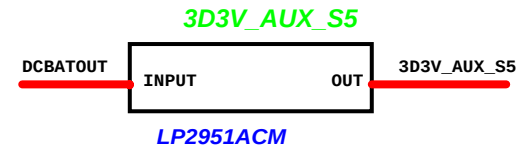
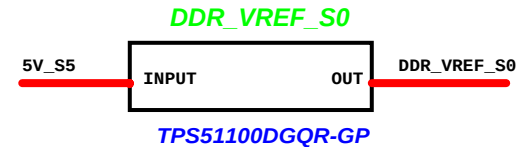
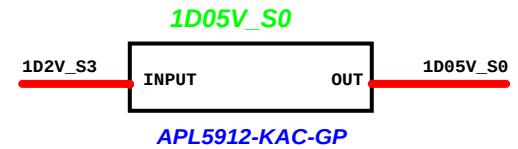
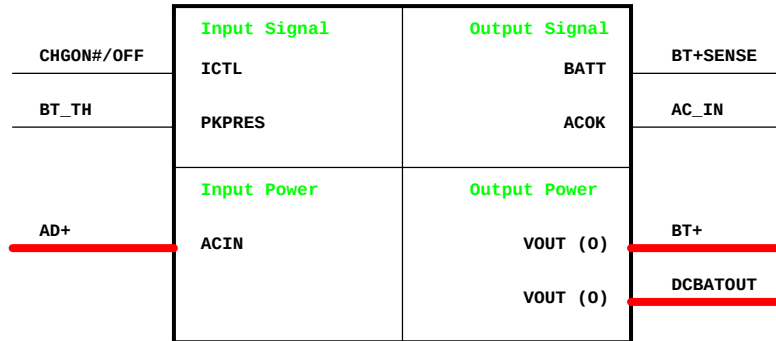
CPU_CORE
Intersil ISL6262



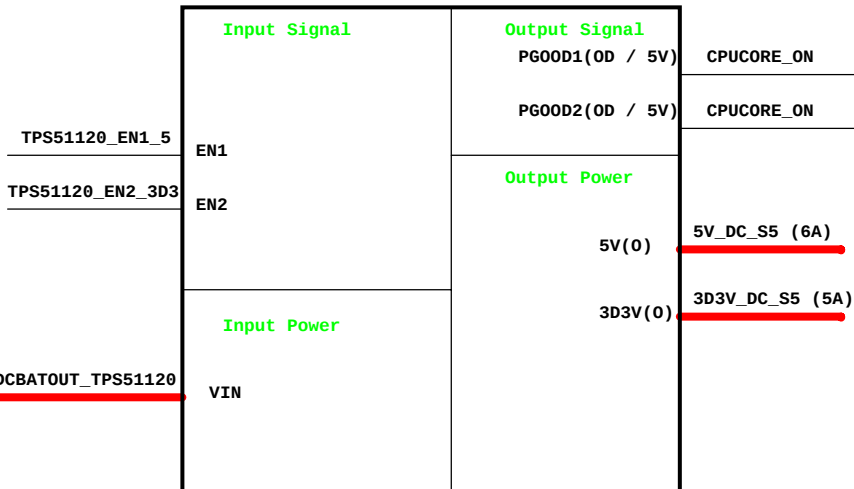
TPS51124
1D8V/1D05V



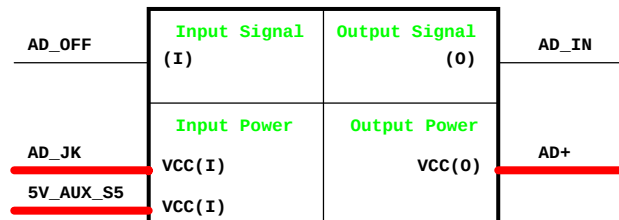
CHARGER MAX8725

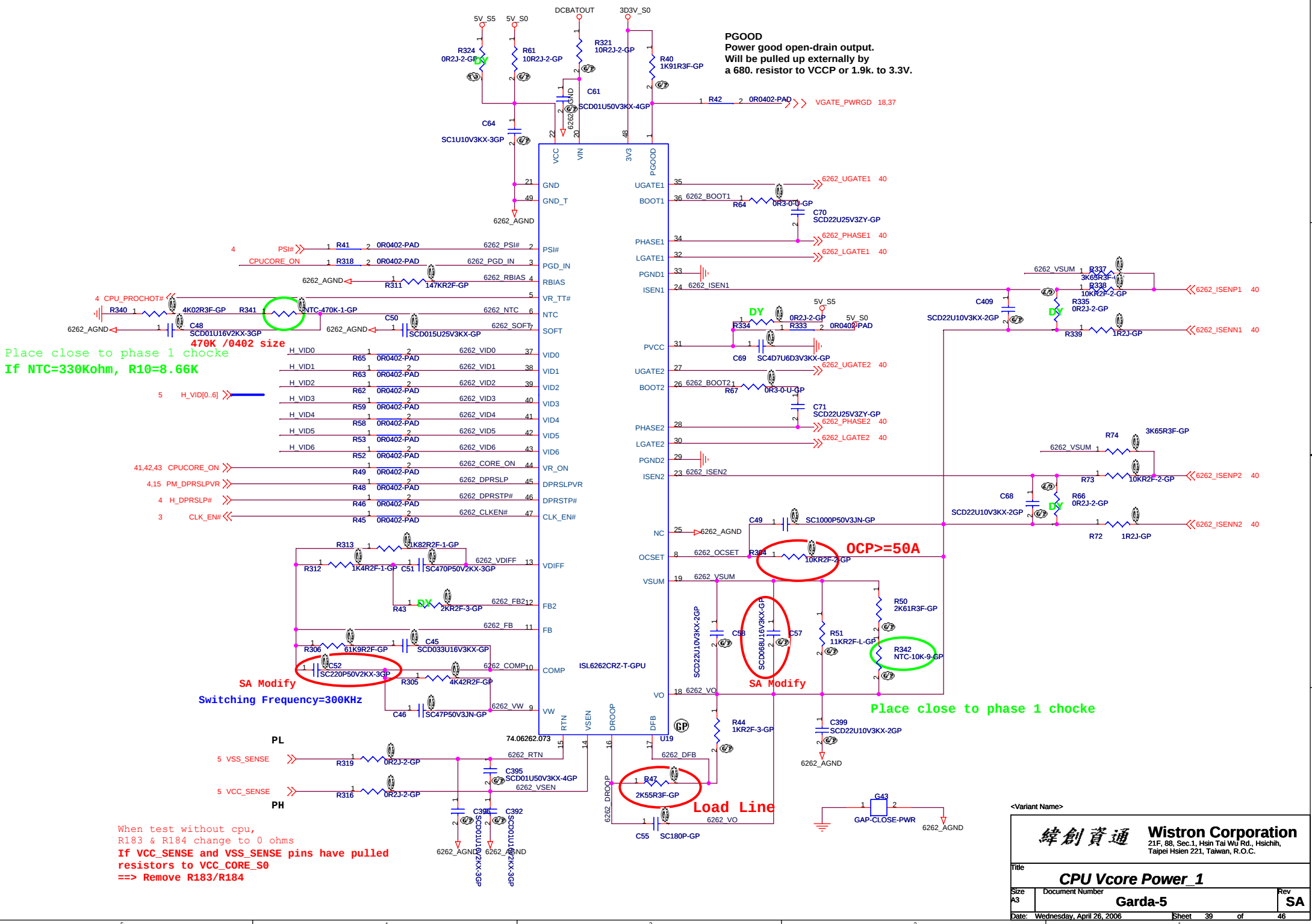


TPS51120
5V/3D3V



Adapter





PGOOD
Power good open-drain output.
Will be pulled up externally by
a 680. resistor to VCCP or 1.9k. to 3.3V.

Place close to phase 1 choke
If NTC=330Kohm, R10=8.66K

SA Modify
Switching Frequency=300KHz

When test without cpu,
R183 & R184 change to 0 ohms
If VCC_SENSE and VSS_SENSE pins have pulled
resistors to VCC_CORE_S0
==> Remove R183/R184

Load Line

Place close to phase 1 choke

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU Vcore Power_1

Size

A3

Document Number

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Date

Wednesday, April 26, 2006

Rev

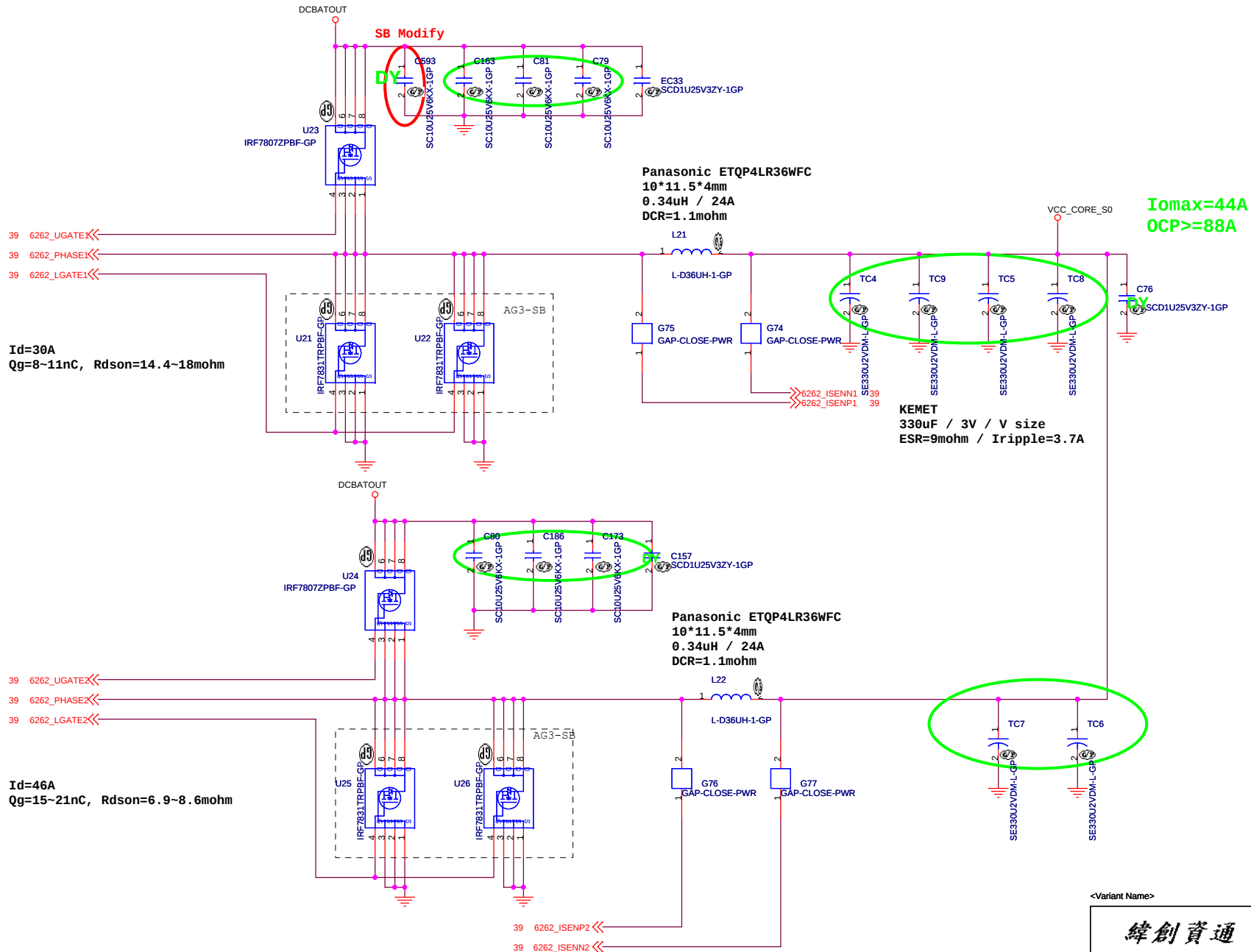
SA

Sheet

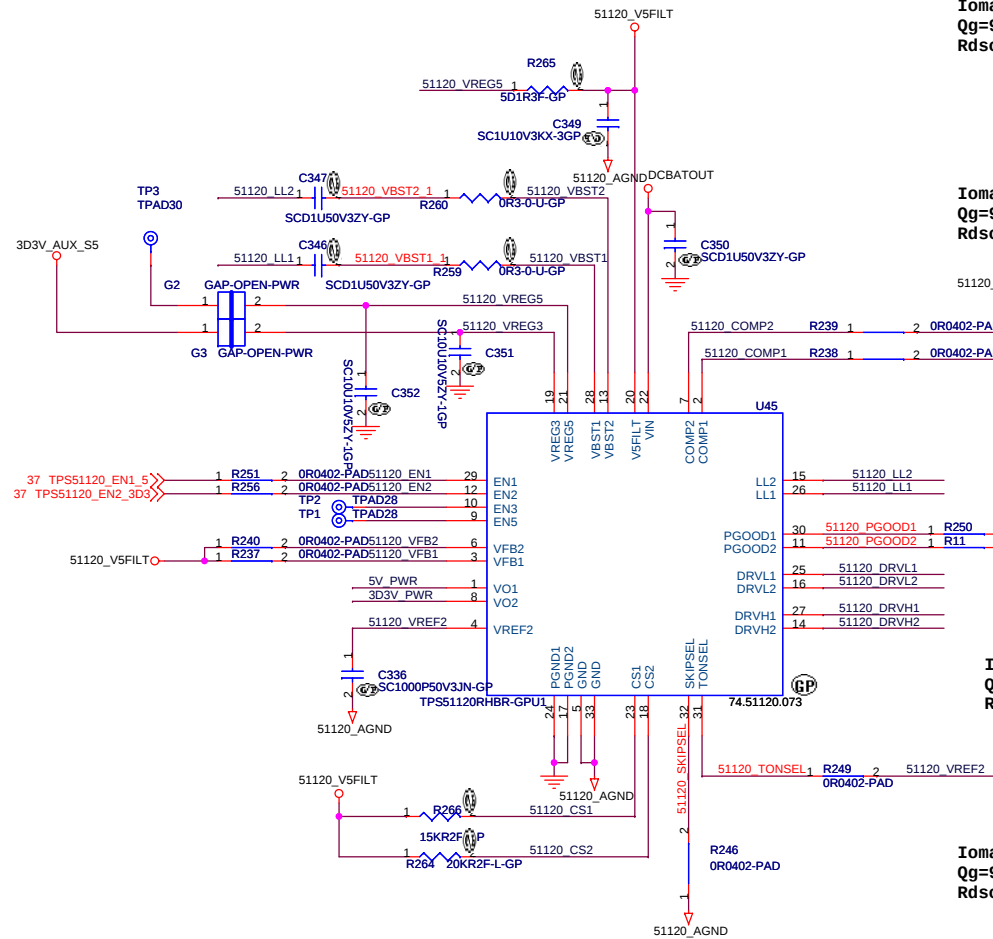
39

of

46



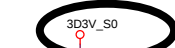
	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switcher ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on



Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

SB Modify



Iomax=11A
Qg=9.8nC,
Rdson=20~25mohm

Iomax=11A
Qg=9.8nC,
Rdson=19.6~24mohm

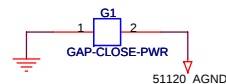
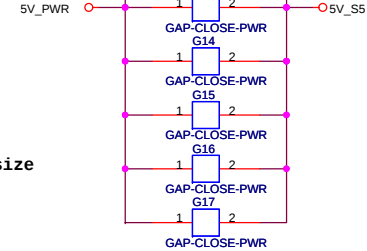
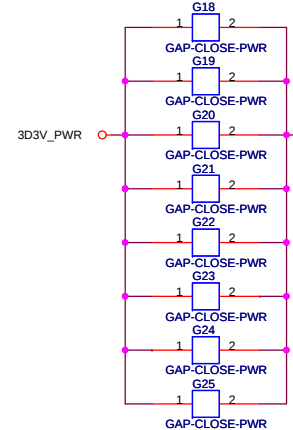
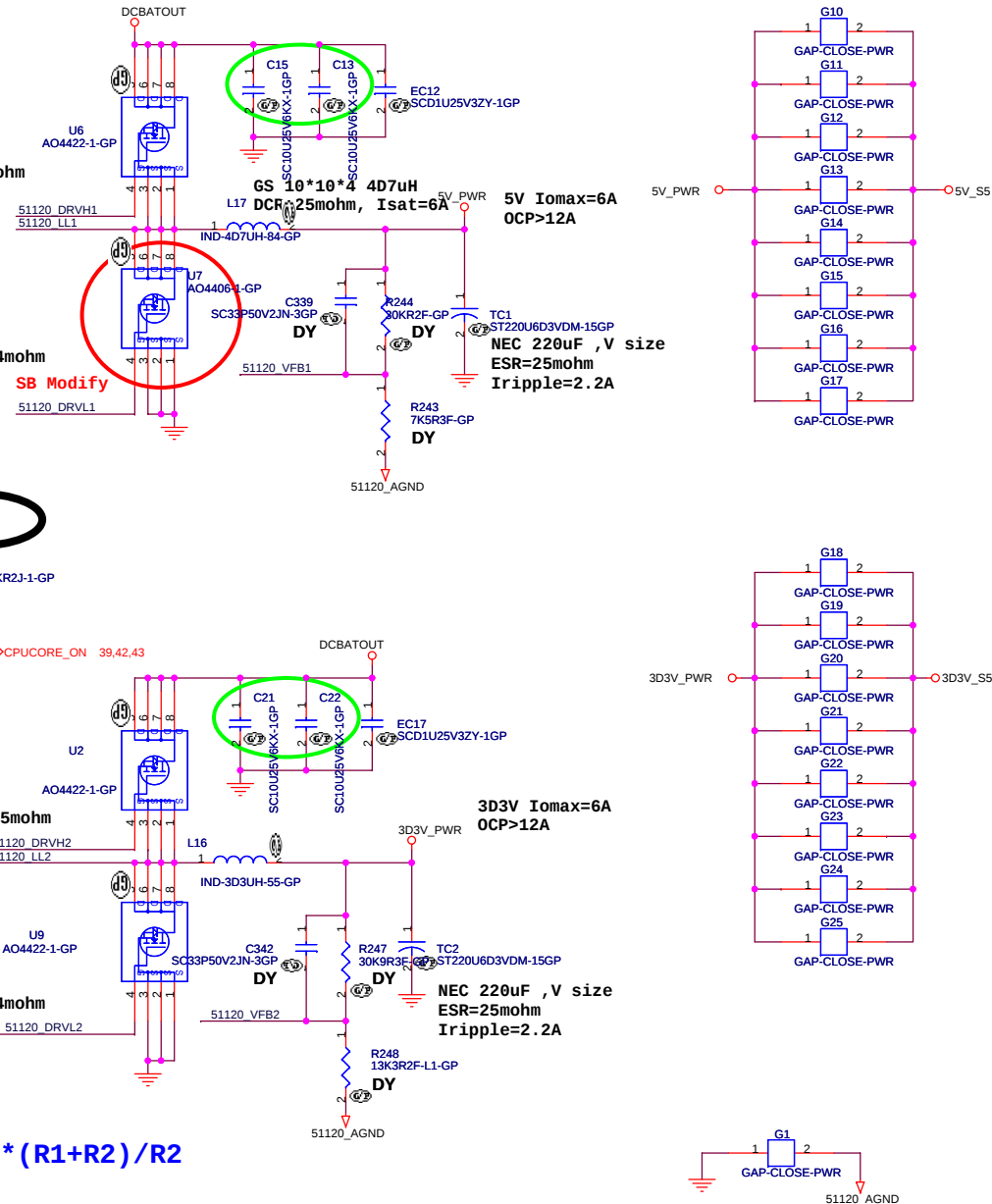
$$V_{out} = 1V \cdot (R1 + R2) / R2$$

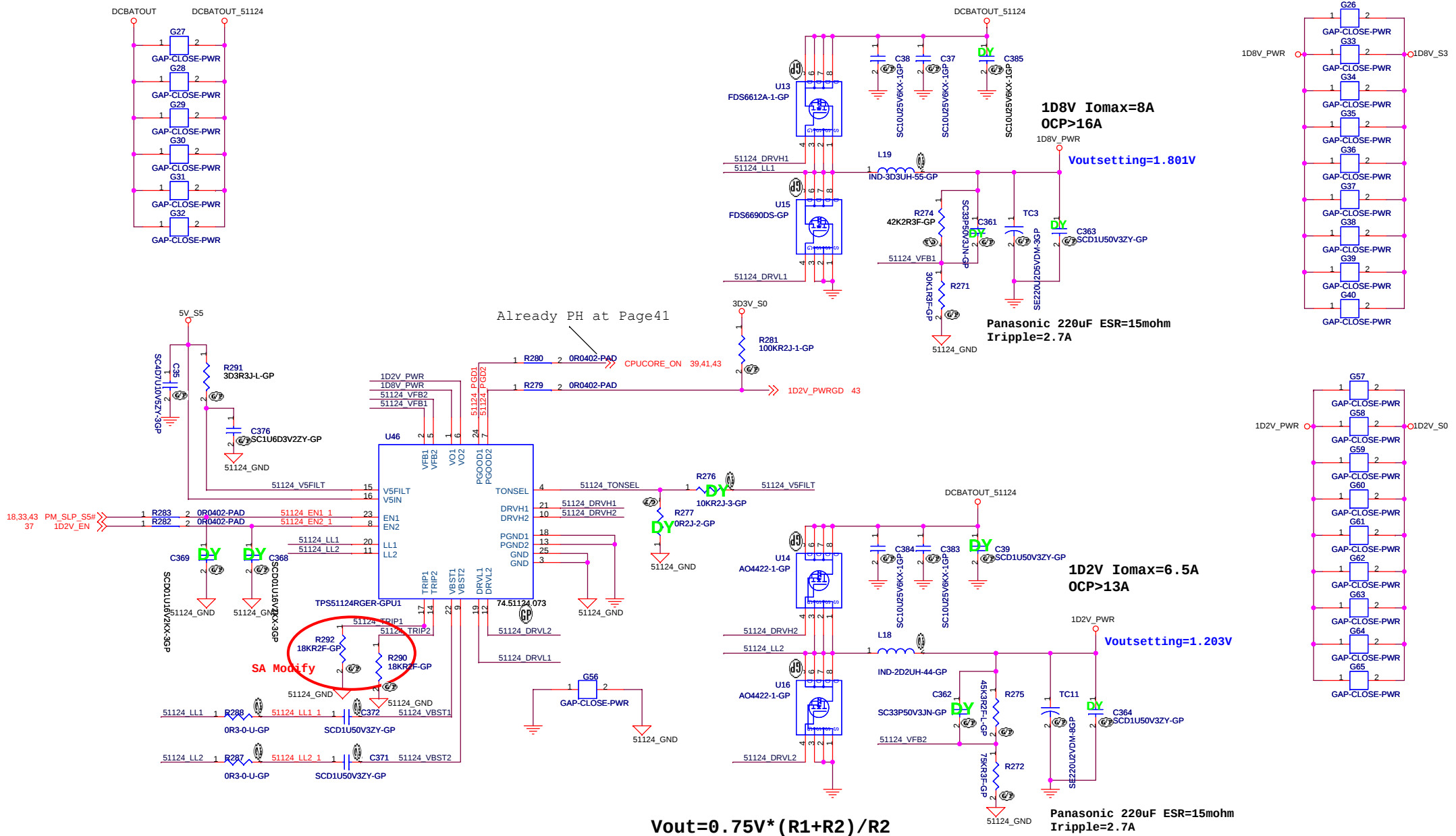
For TPS51120,
Vout=5V

1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V

1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.



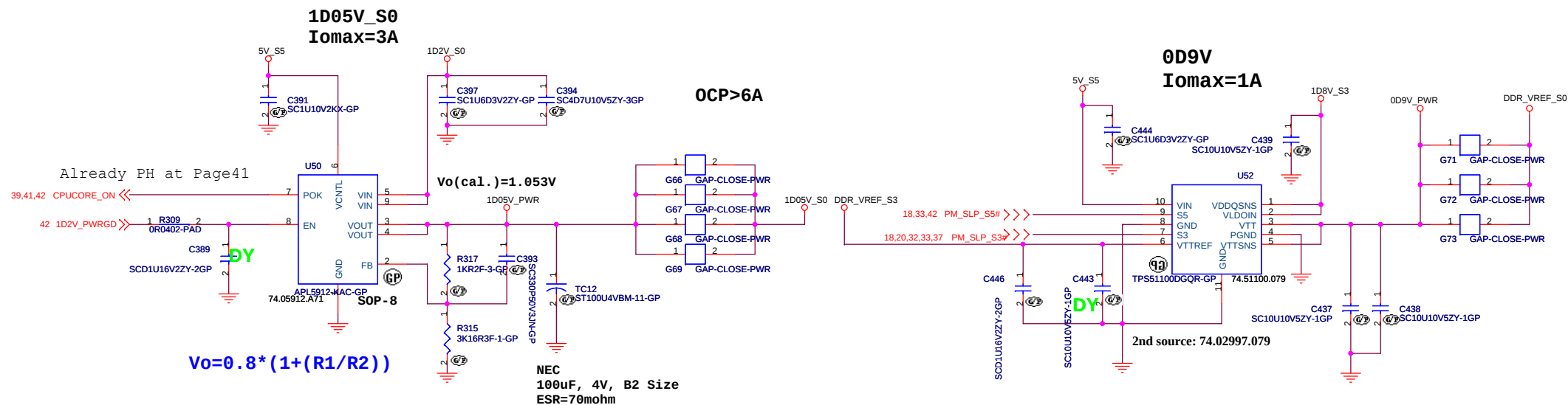


	GND	OPEN	V5FILT
TONSEL	230k/CH1 283k/CH2	283k/CH1 346k/CH2	346k/CH1 423k/CH2

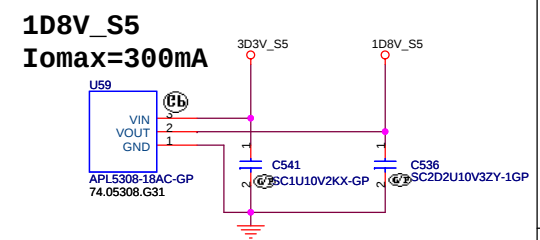
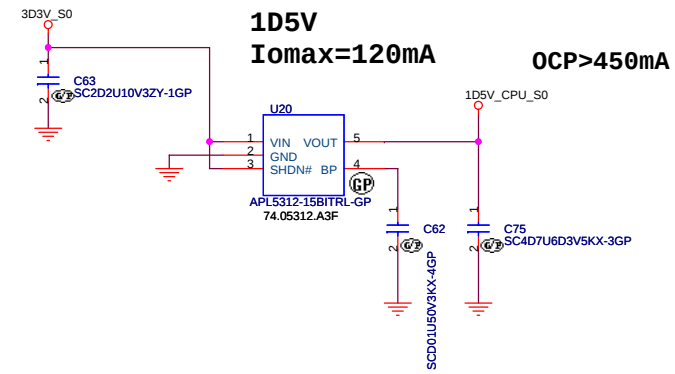
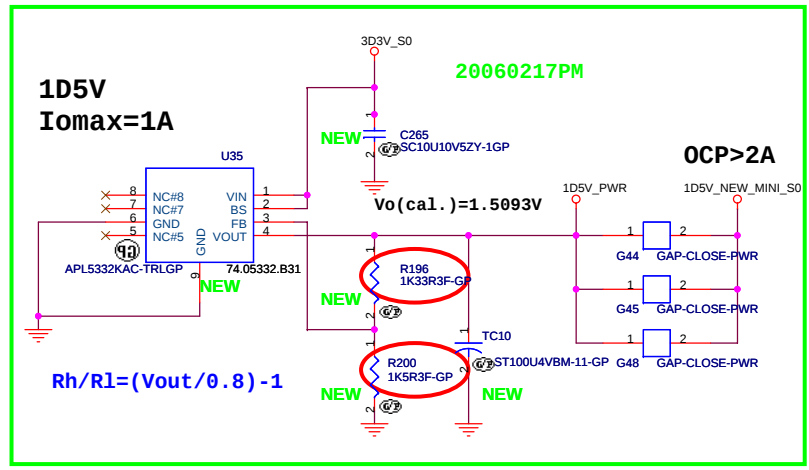
$$V_{trip}(mV) = R_{trip}(Kohm) * 10(uA)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2*L*f)) * ((V_{in} - V_{out}) * V_{out})/V_{in})$$

<Variant Name>



For New Card/MINI Card solution



AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V

SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V

When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable

V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell

ISOURCE_MAX = (0.075/R950)*(VCLS/VREF)

Current limit setting
Adapter=65W, Total_Power=58W(58W/20V=2.9A)

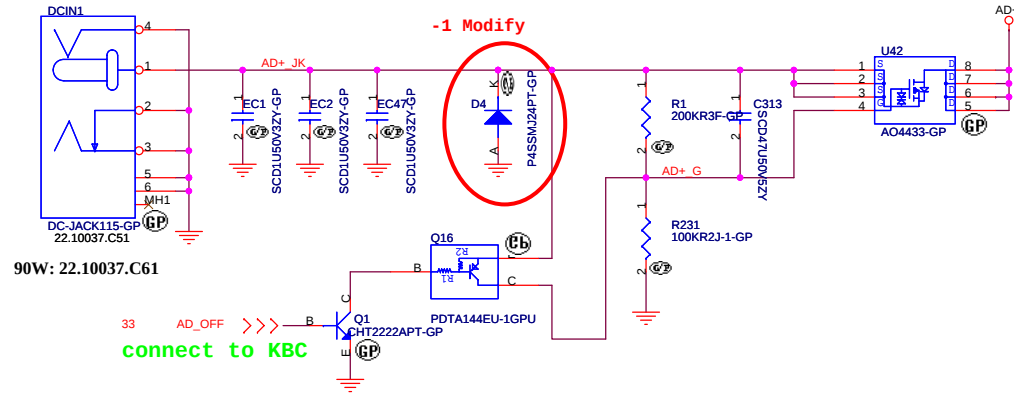
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

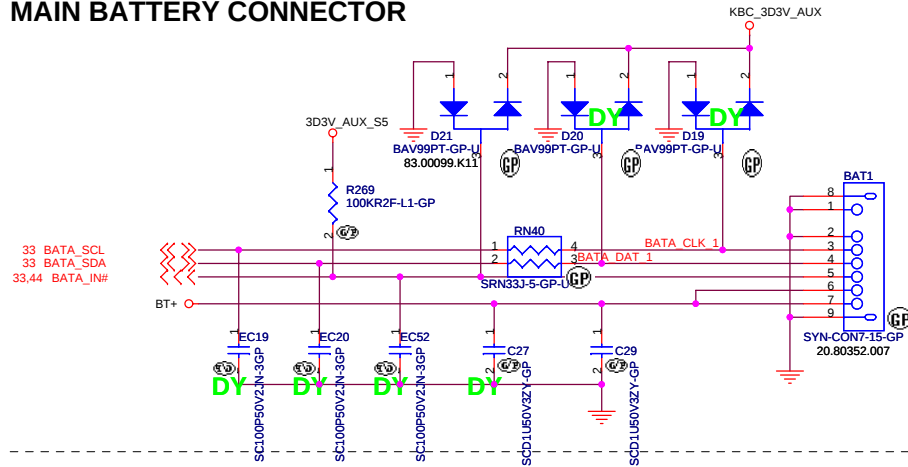
CHARGER MAX8725

Title	Document Number	Rev
Size	Custom	Garda-5
Date: Wednesday, April 26, 2006	Sheet 44 of 46	-1

ADAPTER IN CIRCUIT



MAIN BATTERY CONNECTOR



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size
A3

Document Number

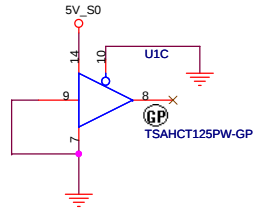
Garda-5

Rev

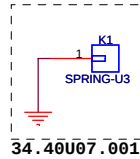
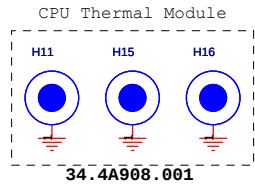
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Date: Wednesday, April 26, 2006

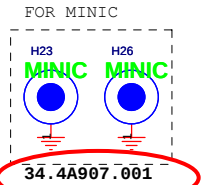
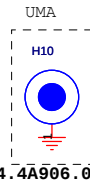
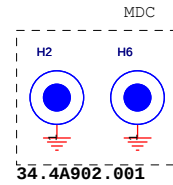
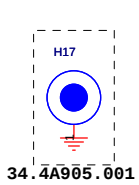
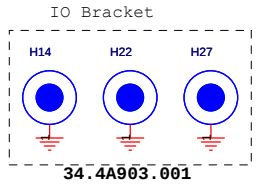
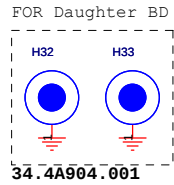
Sheet 45 of 46



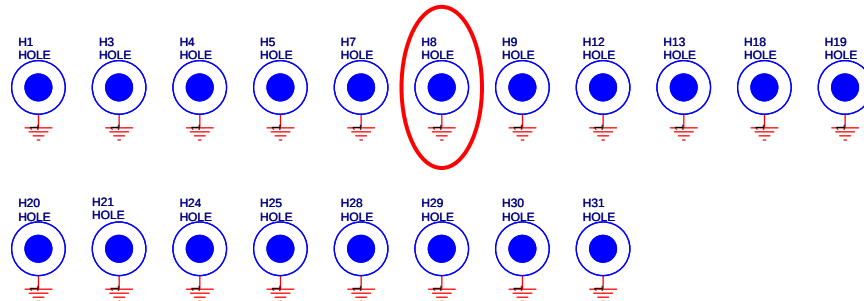
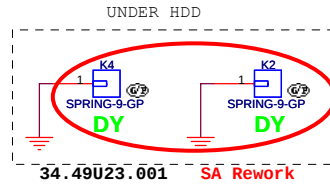
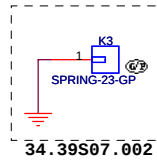
TOP SIDE:



BOTTOM SIDE:



-1 Modify



EMI CAP

