ZR3

CPU CORE
MAXIM
MAX8774 Page:28
VCC_CORE

+1.2V
+1.8VSUS/+1.8V
+0.9V_VTER
TI
TPS51116/51117 Page:29
+1.2V
+1.8VSUS
+1.8V
+0.9V_VTER

+3VPCU/+5VPCU
+3V_S5
+3V/+5V
+3VSUS/+5VSUS
TI
TPS51120 Page:30
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5VSUS
+5V

+1.5V/+2.5V
GMT
G966/913-C Page:31
+1.5V
+2.5V

BATTERY CHARGER
MAXIM
ISL6251 Page:27
BATTERY

AMD S1
Turion 64 Rev.F Dual-Core/
Sempron Rev.F Single-Core
Dual-Core 35W / Single-Core 25W
(638 S1g1 socket)
Page:3, 4, 5, 6

DDR-II SODIMM1 Page: 7
DDR-II SODIMM2 Page: 7
DDR-II 533/667MHz

CPU THERMAL SENSOR Page:5

X'TAL 14.31818MHz
Clock generator
ICS951462
Page:12

HT_LINK

NB
ATi RS485
465-Pins FCBGA Package
Page: 8, 9 ,10, 11

S-Video Page: 21
TV-OUT

mini CARD Page: 20
PCIE

RGB
CRT Page: 21

LVDS
LVDS Page: 21

2X PCIE

Manufacturing Option
SATA HDD Page: 22
PATA HDD Page: 22
IDE-ODD Page: 22

SATA
ATA 66/100

SB
ATi SB460
549-Pins BGA Package
Page: 13, 14, 15, 16

X'TAL 32.768KHz

RTC Page: 14

PCI BUS 33MHZ
USB 2.0
LPC 33MHZ
Azalia

REALTEK 8100SBL/CL 10/100 LAN
AD18
REQ0# / GNT0#
INTE# Page: 17

TRANSFORMER Page: 17
RJ45 Page: 17

ENE CB714/1410 Cardbus controller
AD17
REQ3# / GNT3#
INTH#,INTG#
Page: 18

PCMCIA SLOT Page: 19
CARD READER Page: 19

MINI-PCI Wireless LAN
AD20
REQ2# / GNT2#
INTG#,
INTE# Page: 20

MIC-IN Page: 24
LINE-IN Page: 24

AUDIO CODEC
REALTEK- ALC883
48-pins Package
Page: 23

Audio AMP MAX4411 Page: 23
Audio AMP MAX9710 Page: 24

LINEOUT Page: 24
SPEAKER Page: 24

MODEM
FOXCONN MDC
Page: 23

RJ11 (External)

KBC
NS PC97541V
176-Pins Package
Page: 25

BIOS
SST39VF080
Page: 25

Touchpad Page: 26
Keyboard Page: 26
FAN Page: 26

Bluetooth USB interface Page:20
USB6

SYSTEM USB PORT*3 Page: 20
USB0,1,4

USB CAMERA Page: 20
USB2

Power State Table

Power Name	Control Signal	Power State
+VCC_CORE	VRON	S0
+2.5V	MAINON	S0
+3VPCU	N/A	ALWAYS
+3VS5	S5_ON	S0-S5
+3VSUS	SUSD	S0-S3
+3V	MAIND	S0
+5VPCU	N/A	ALWAYS
+5VSUS	SUSD	S0-S3
+5V	MAIND	S0
+1.2V	MAINON	S0
+0.9V_VTER	MAINON	S0
+1.8VS5	S5_ON	S0-S5
+1.8VSUS	SUSON	S0-S3
+1.8V	MAIND	S0
+1.5V	MAINON	S0

PROJECT : ZR3
Quanta Computer Inc.

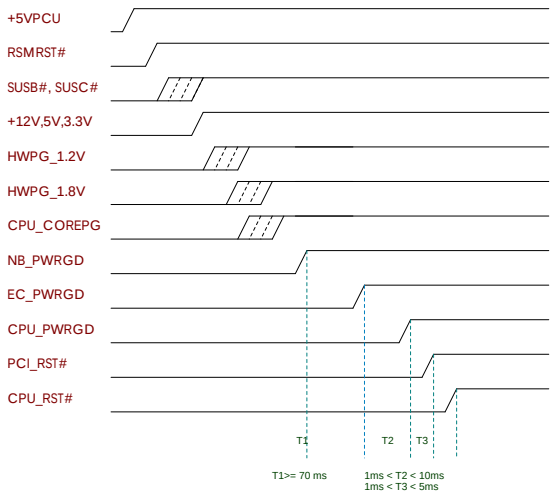
Size	Document Number	Rev
	BLOCK DIAGRAM	1A

Date: Wednesday, October 18, 2006 Sheet 1 of 31

TABLE OF CONTENTS

	POWER	VOLTAGE	ACTIVE SCOPE	PAGE
SYSTEM	+12V	+12V	S0	
	+5V	+5V	S0	
	+3V	+3.3V	S0	
	+5VPCU	+5V	ALWAYS	
	+3VPCU	+3.3V	ALWAYS	
	+5VSUS	+5V	S0-S3	
	+3VSUS	+3.3V	S0-S3	
	+3V_S5	+3.3V	S0	
CPU	VCCCORE	VID[0..5]	S0	
	VDDA_RUN	+2.5V	S0	
	VLDT_RUN	+1.2V	S0	
	+0.9V_VTER	+0.9V	S0	
	+1.8V	+1.8V	S0	
	+1.8VSUS	+1.8V	S0-S3	
DDR2	+1.8V	+1.8V	S0	
	+1.8VSUS	+1.8V	S0-S3	
	+0.9V_VTER	+0.9V	S0	
RC485 NB	+1.8V	+1.8V	S0	
	+1.8VSUS	+1.8V	S0-S3	
	+3V	+3.3V	S0	
	VDDC	+1.2V	S0	
	VDD_HT	+1.2V	S0	
	VDDA12	+1.2V	S0	
	VDD18	+1.8V	S0	
	VDDA18	+1.8V	S0	
	VDD_DVO	+1.8V	S0	
	VDDR3	+3.3V	S0	
	AVDD_NB	+3.3V	S0	
	AVDDQ	+1.8V	S0	
	PLLVDD	+1.8V	S0	
	LPVDD	+1.8V	S0	
	LPVDD18A	+1.8V	S0	
SB460 SB	+3V	+3.3V	S0	
	+1.8V	+1.8V	S0	
	+3V_S5	+3.3V	S0	
	+1.8V_S5	+1.8V	S0	
	VDD	+1.8V	S0	
	AVDD_CK	+1.8V	S0	
	AVDD_SATA	+1.8V	S0	
	XTLVDD_ATA	+1.8V	S0	
	PLLVDD_ATA	+1.8V	S0	
	PCIE_PVDD	+1.8V	S0	
	PCIE_VDDR	+1.8V	S0	
	CPU-PWR	+1.2V	S0	
	VDDQ	+3.3V	S0	
	V5_VREF	+5V	S0	
	+1.8V_SUB_PHY	+1.8V	S0	
	+3VSUS	+3.3V	S0-S3	
	+SB_S5_3V	+3.3V	S0	
	+SB_S5_1.8V	+1.8V	S0	

POWER UP SEQUENCE



PROJECT : ZR3

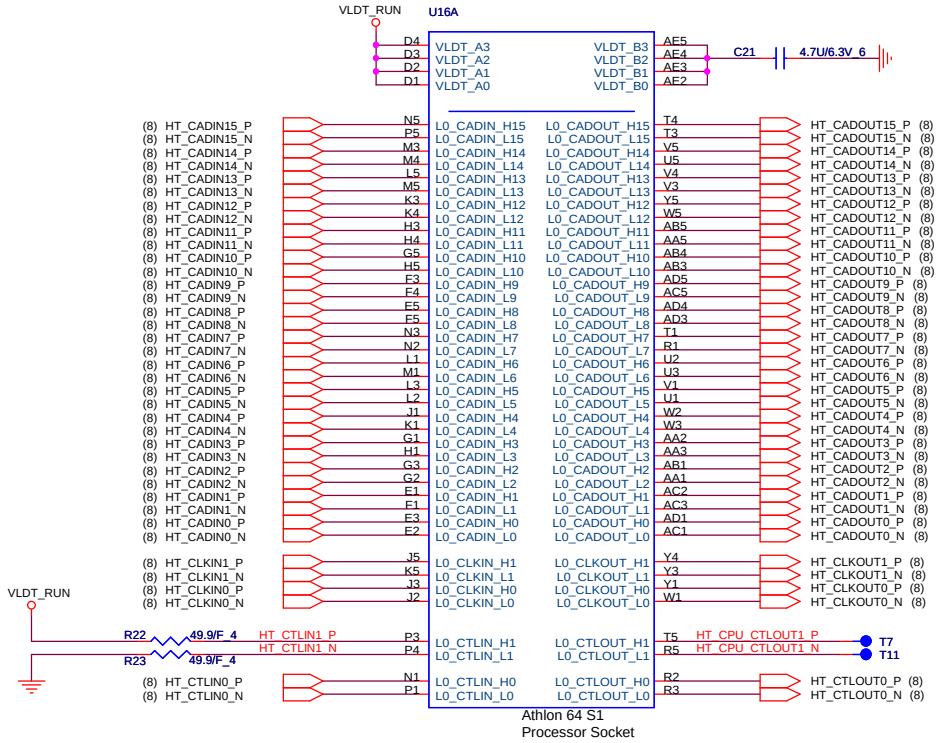
Quanta Computer Inc.

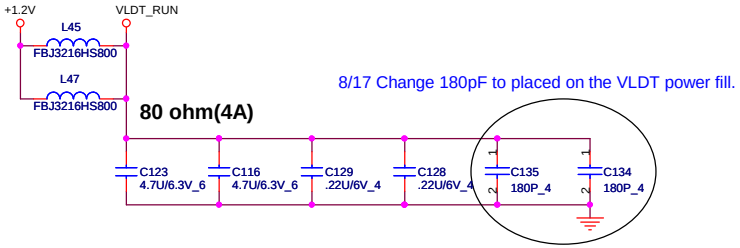
Size	Document Number	Rev
	TABLE OF CONTENTS	1A

Date: Wednesday, October 18, 2006 Sheet 2 of 31

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE





LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 HT I/F	1A
Date: Wednesday, October 18, 2006	Sheet 3 of 31	

Processor DDR2 Memory Interface

VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

PLACE THEM CLOSE TO CPU WITHIN 1"

U16B

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

U16C

To SODIMM socket B (Far)

To SODIMM socket A (near)

DDR: DATA

Athlon 64 S1
Processor Socket

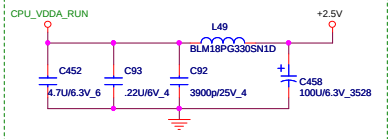
PROJECT : ZR3
Quanta Computer Inc.

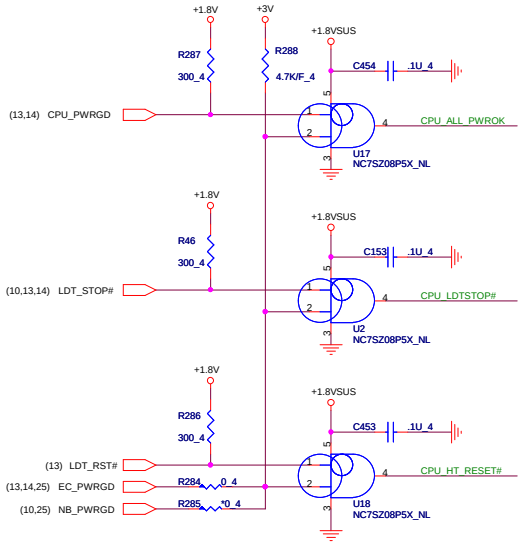
Size	Document Number	Rev
	ATHLON64 DDRII MEMORY I/F	1A
Date: Wednesday, October 18, 2006	Sheet 4 of 31	

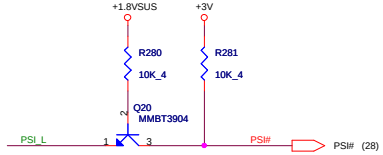
ATHLON Control and Debug

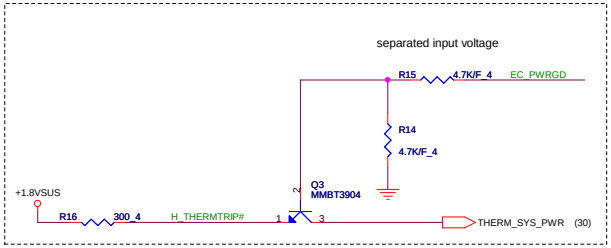
LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

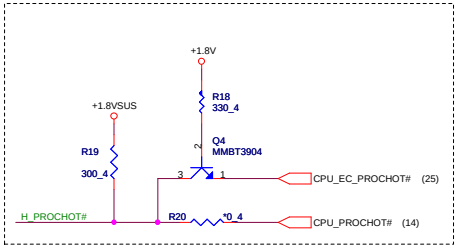
CPU_VDDA_RUN



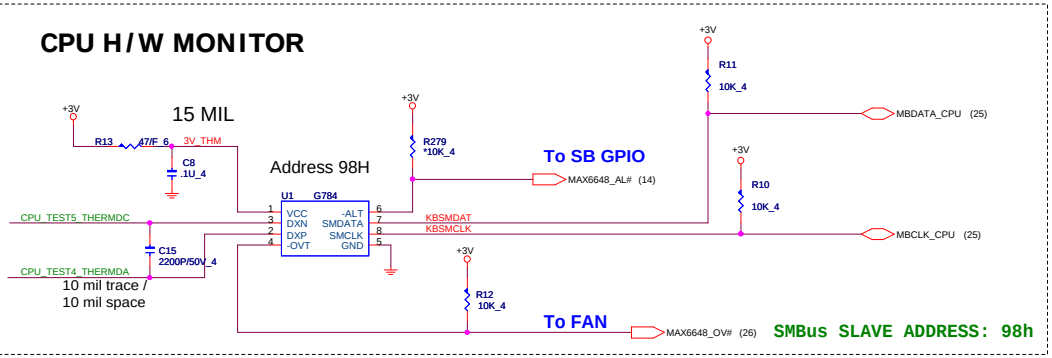








CPU H/W MONITOR

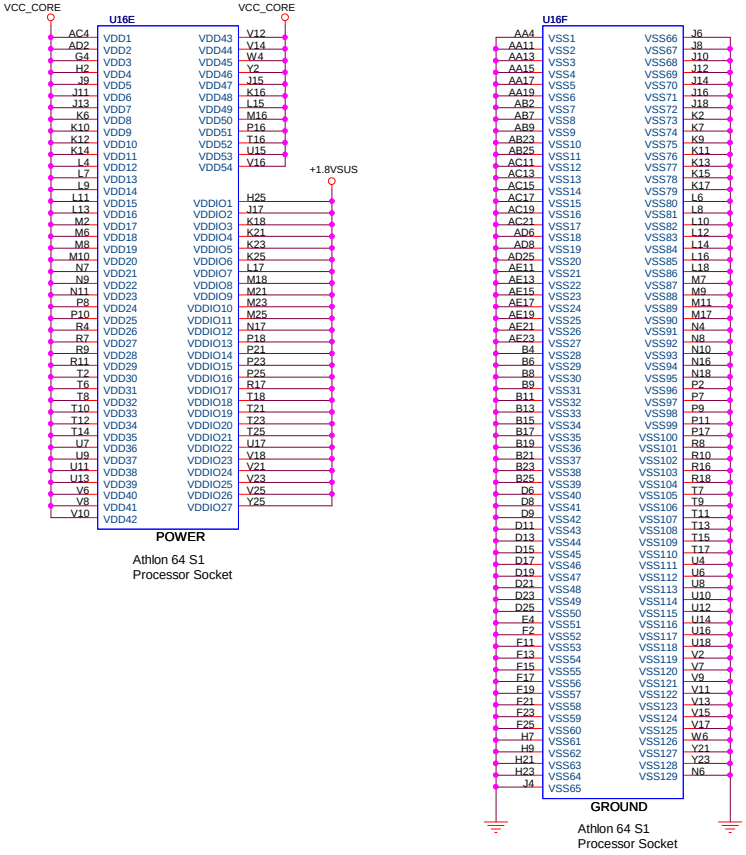


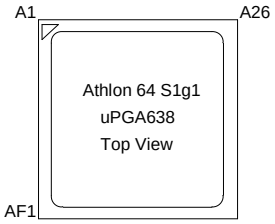
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- (±5%) pulldown to VSS.

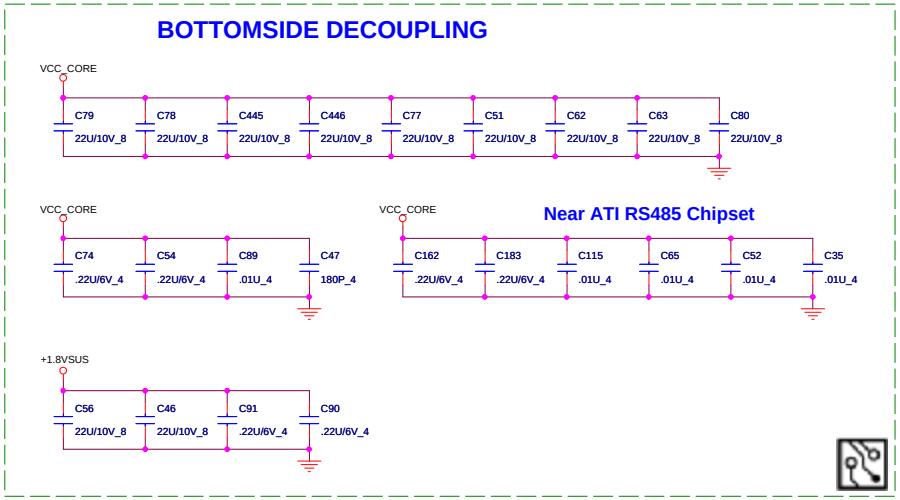
Place them to CPU within 1"

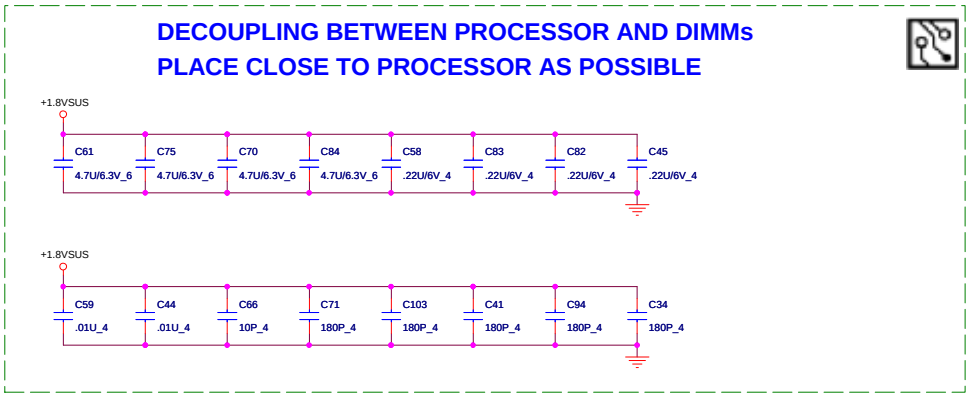
PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	ATHLON64 CTRL & DEBUG	1A
Date: Wednesday, October 18, 2006	Sheet 5 of 31	







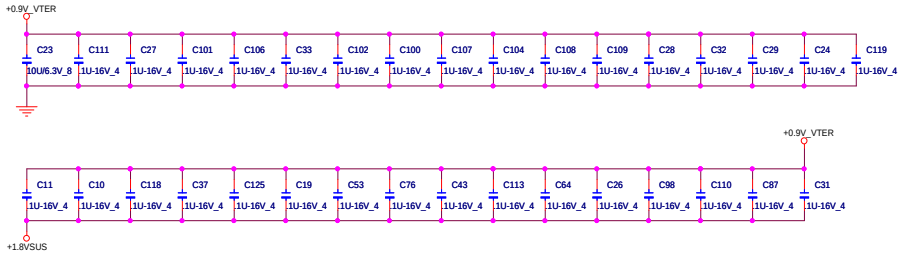


PROCESSOR POWER AND GROUND

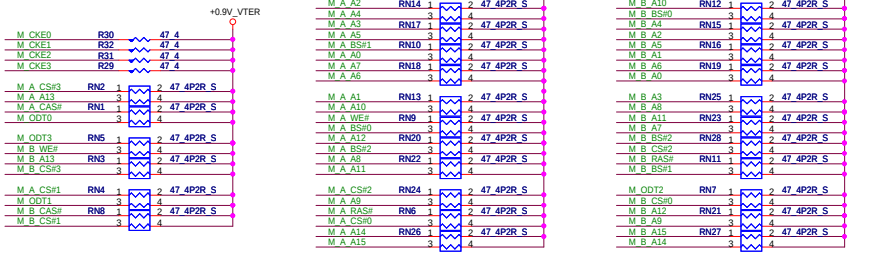
PROJECT : ZR3
Quanta Computer Inc.

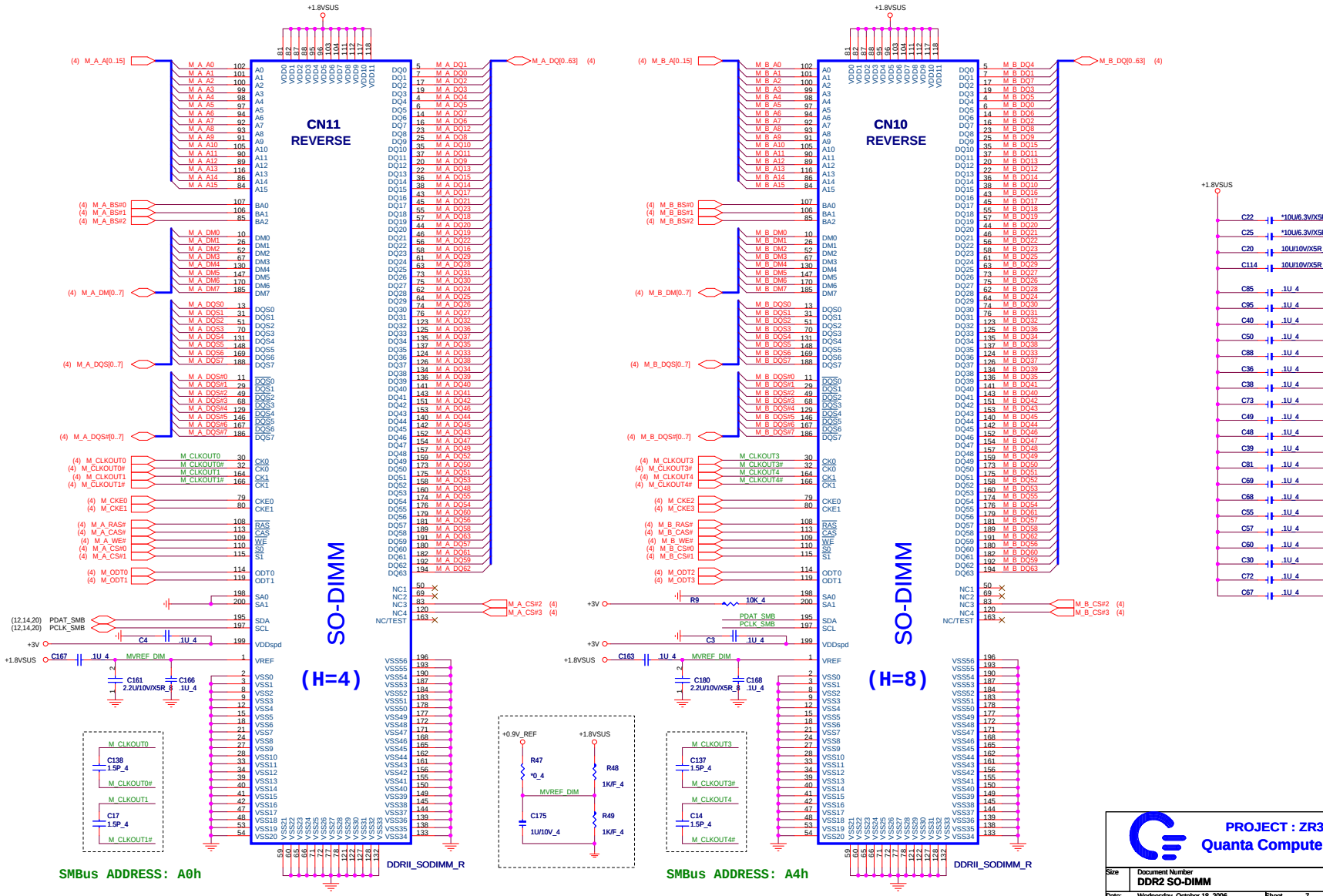
Size	Document Number	Rev
	ATHLON64 PWR & GND	1A
Date: Wednesday, October 18, 2006	Sheet 6 of 31	

TERMINATOR DECOUPLING CAPACITOR



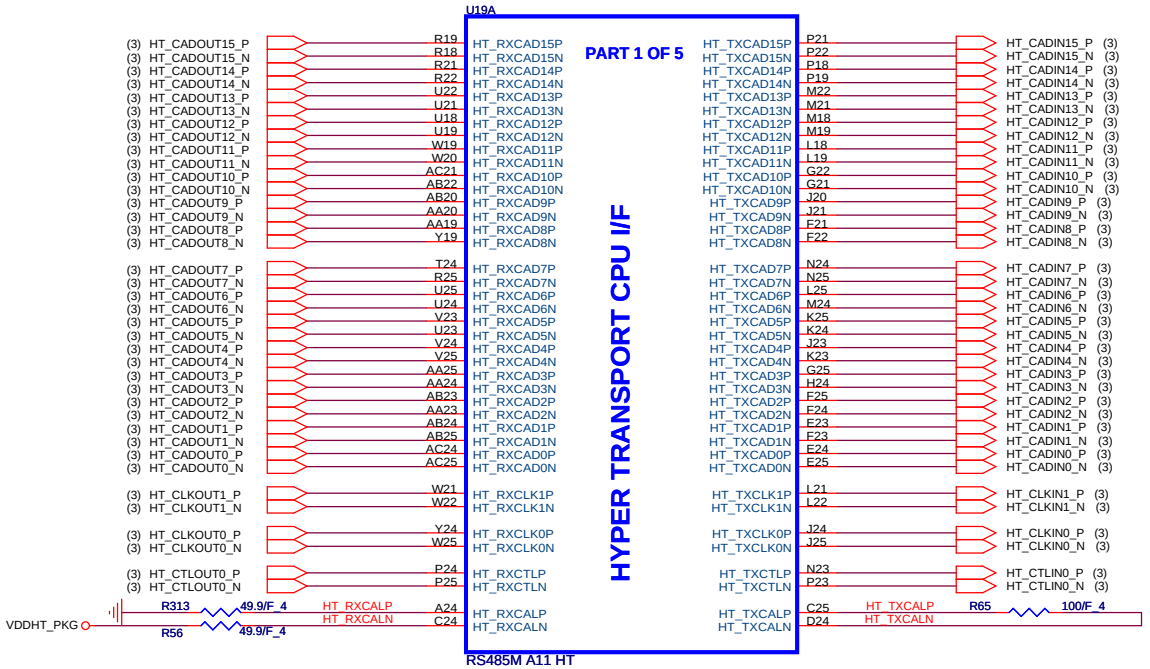
DDR2 TERMINATOR





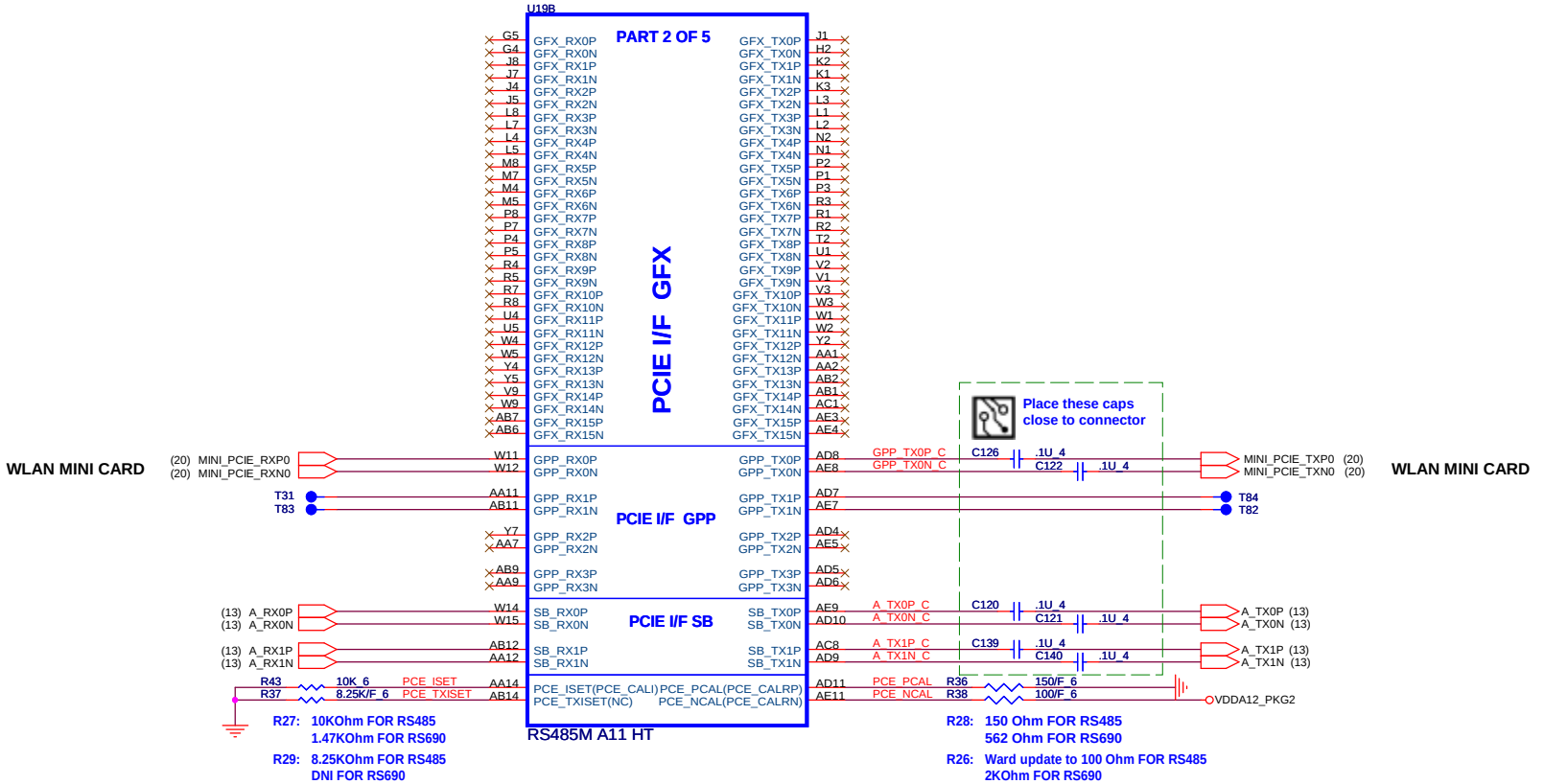
PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	DDR2 SO-DIMM	1A
Date: Wednesday, October 18, 2006	Sheet 7 of 31	



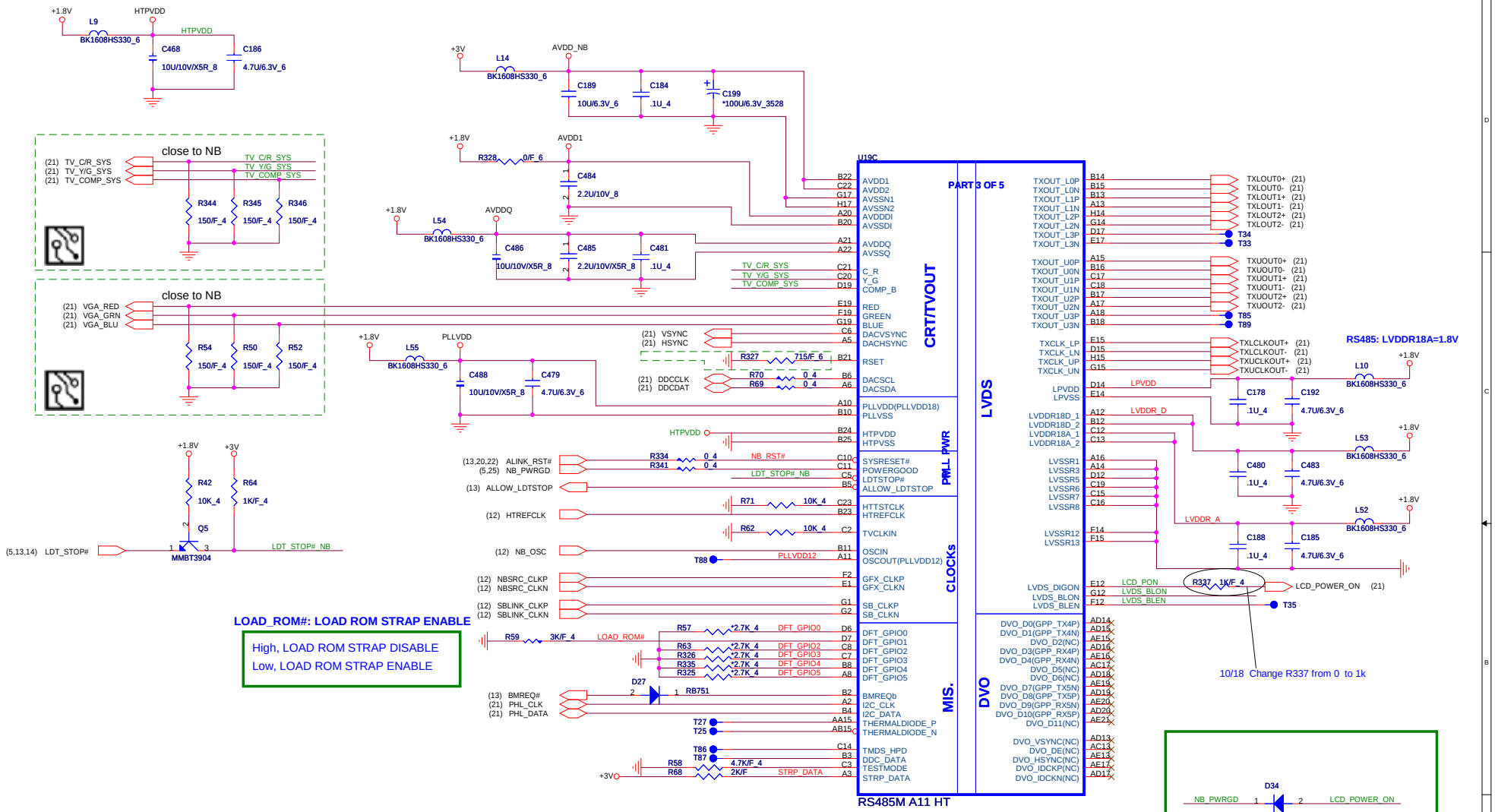
PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-HT LINK0 I/F	1A
Date: Wednesday, October 18, 2006	Sheet 8 of 31	



PROJECT : ZR3
Quanta Computer Inc.

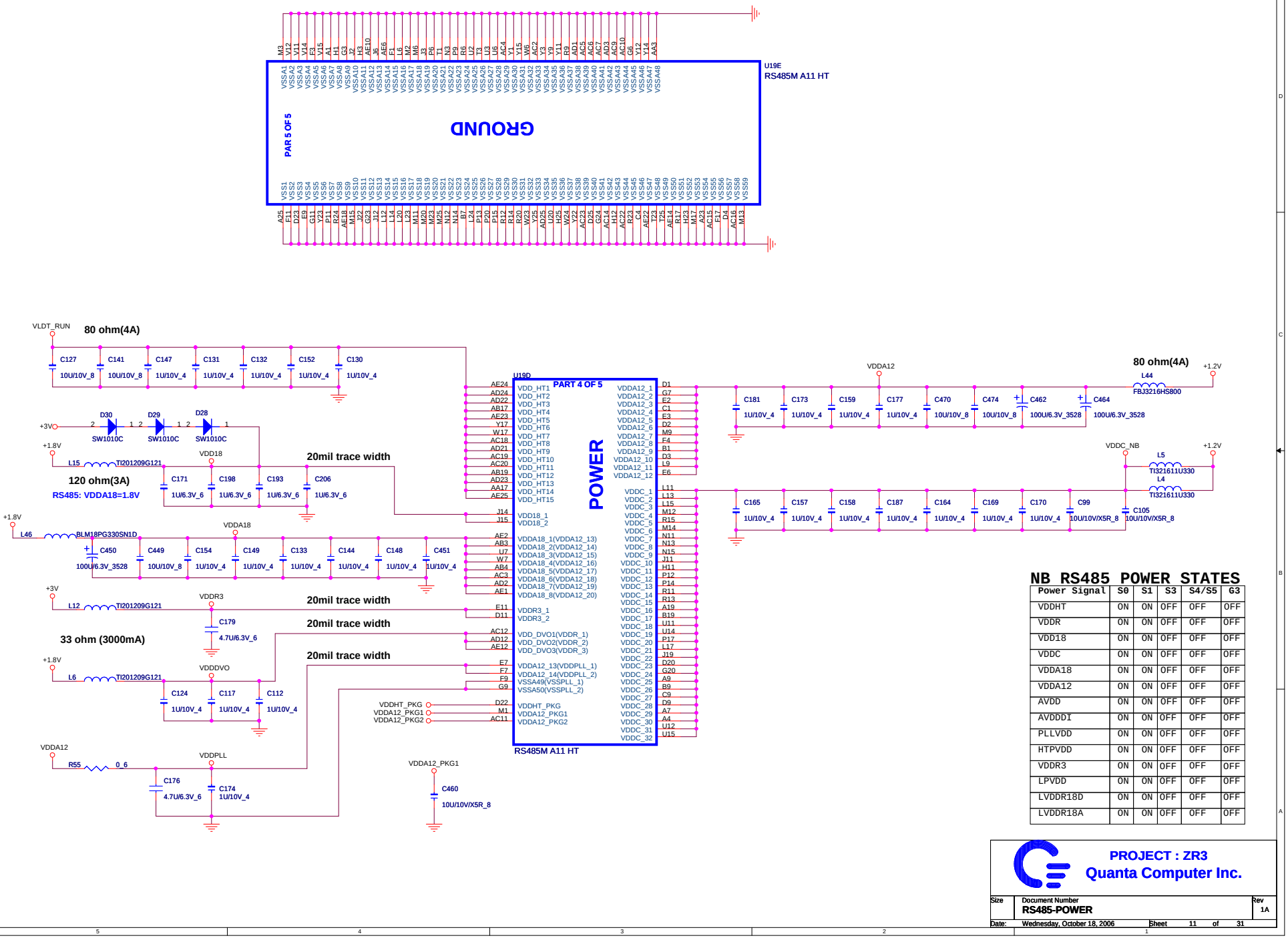
Size	Document Number	Rev
	RS485-PCIE LINK I/F	1A
Date: Wednesday, October 18, 2006	Sheet 9 of 31	



	RS485	RS690
OSCOUT(A11)	OSCOUT	PLLVDD12
DVO_D0(AD14)	DVO_D0	GPP_TX4P
DVO_D1(AD15)	DVO_D1	GPP_TX4N
DVO_D3(AD16)	DVO_D3	GPP_RX4P
DVO_D4(AE16)	DVO_D4	GPP_RX4N
DVO_D7(AE19)	DVO_D7	GPP_TX5N
DVO_D8(AD19)	DVO_D8	GPP_TX5P
DVO_D9(AE20)	DVO_D9	GPP_RX5N
DVO_D10(AD20)	DVO_D10	GPP_RX5P

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-SYSTEM I/F & DVO	1A
Date: Friday, October 20, 2006	Sheet 10 of 31	

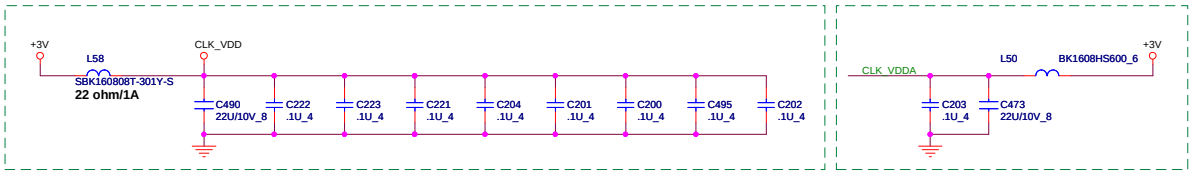


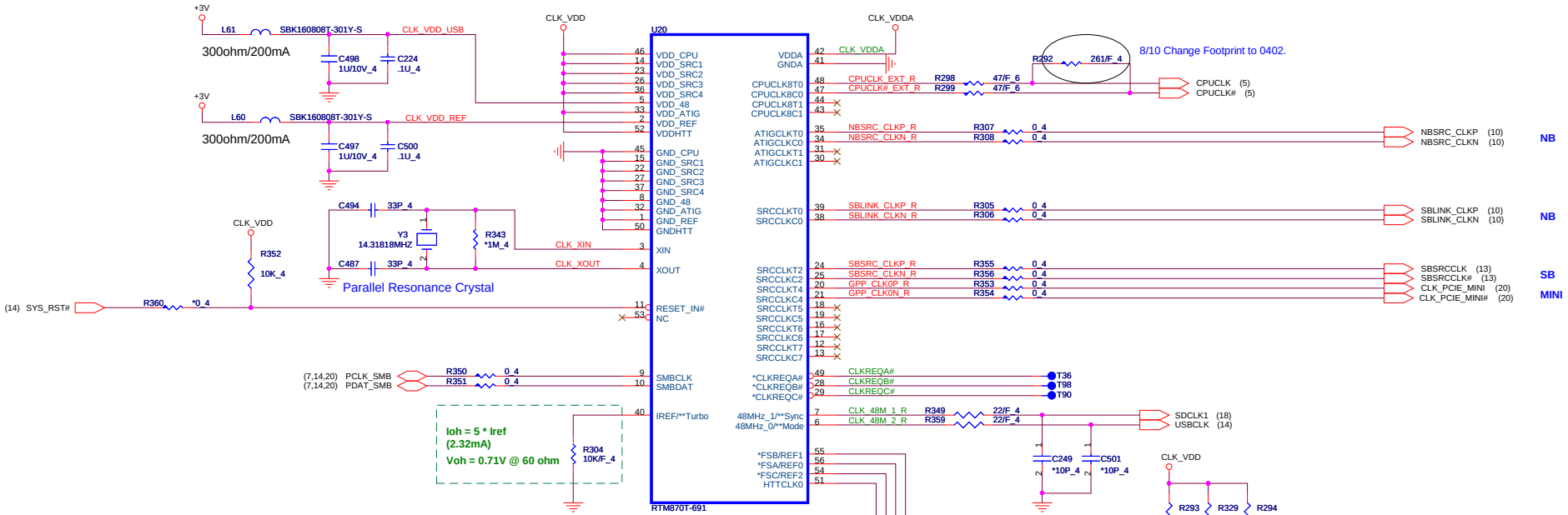
NB RS485 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR	ON	ON	OFF	OFF	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	RS485-POWER	1A
Date: Wednesday, October 18, 2006	Sheet 11 of 31	





Note: * internal 150K pull up ,
** internal 150K pull down

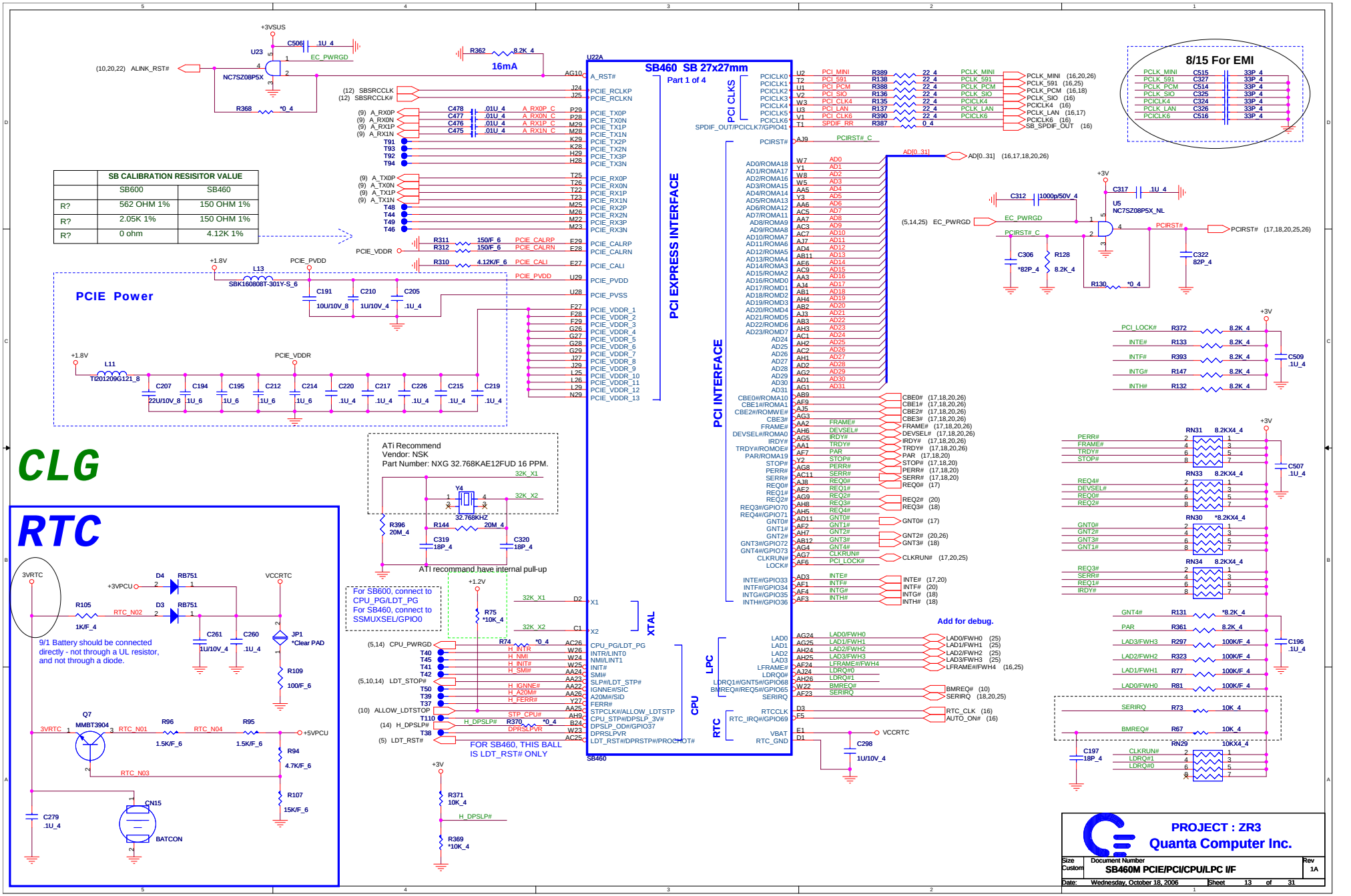
EXT CLK FREQUENCY SELECT TABLE(MHZ)

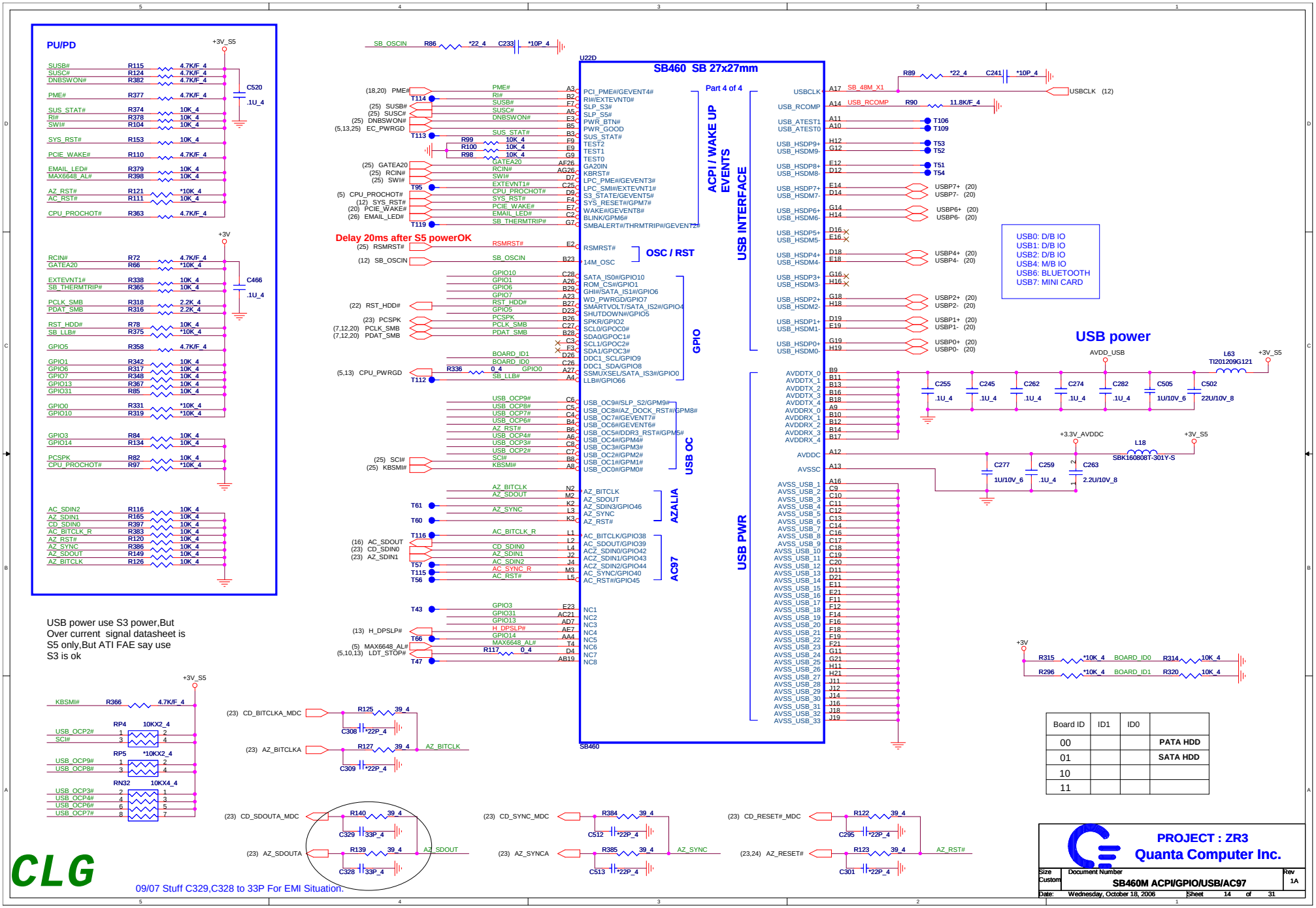
FS2	FS1	FS0	CPU	HTT	SRC	ATIG	USB1	SSC
0	0	0	266.67	66.66	100	100	48.00	+/- 0.25%
0	0	1	133.33	66.66	100	100	48.00	+/- 0.25%
0	1	0	200.00	66.66	100	100	48.00	+/- 0.25%
0	1	1	166.67	66.66	100	100	48.00	+/- 0.25%
1	0	0	333.33	66.66	100	100	48.00	+/- 0.25%
1	0	1	100.00	66.66	100	100	48.00	+/- 0.25%
1	1	0	400.00	66.66	100	100	48.00	+/- 0.25%
1	1	1	200.00	66.66	100	100	48.00	+/- 0.25%

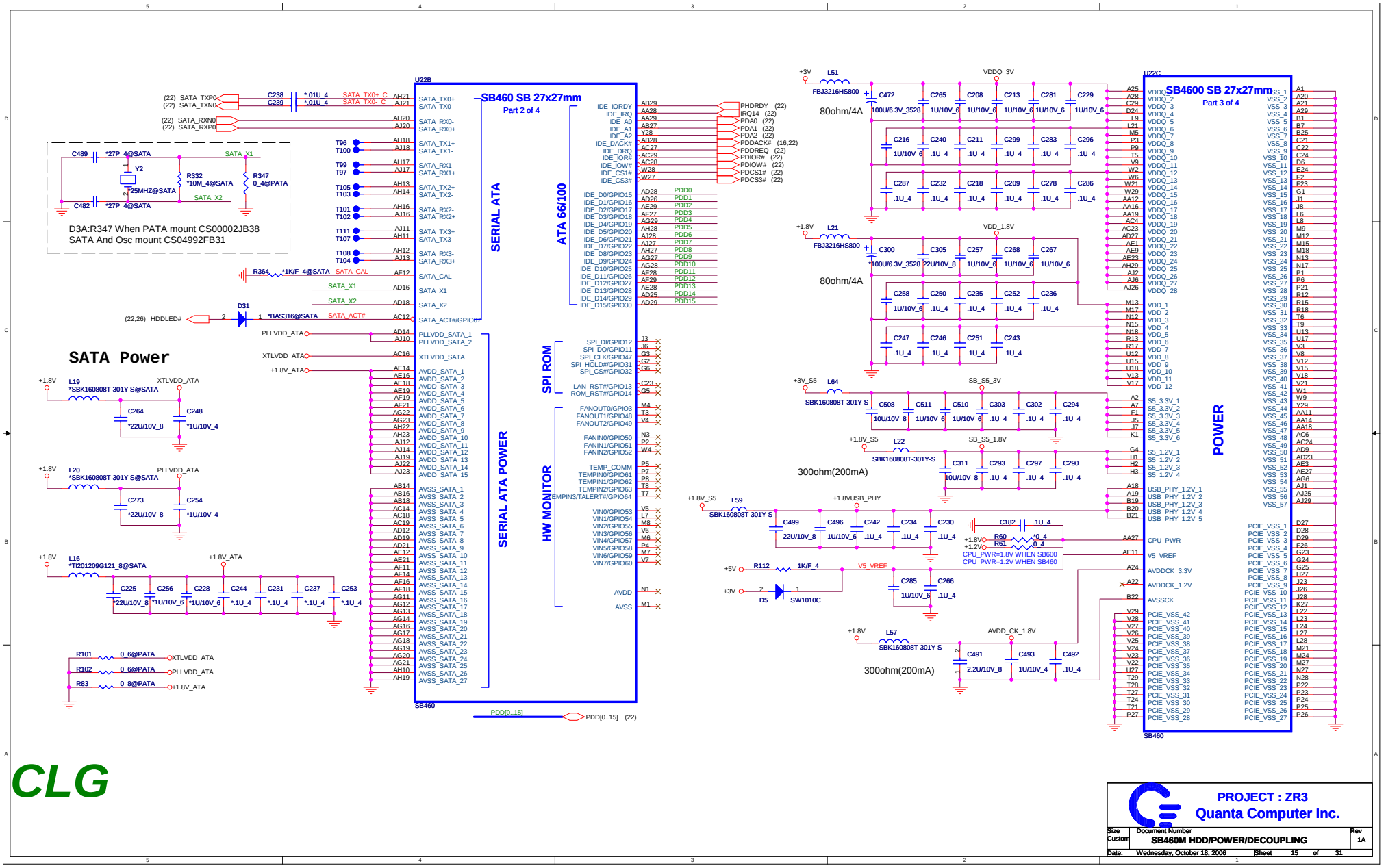
Check AMD clock

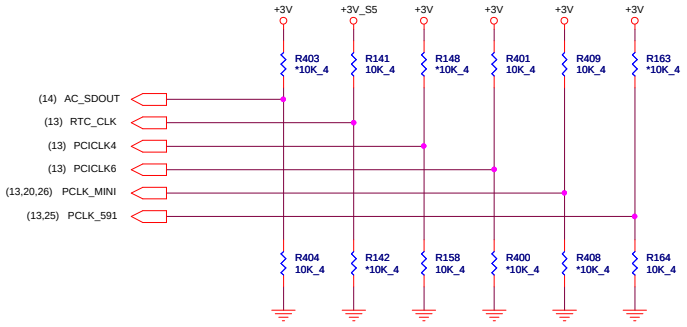
PROJECT : ZR3
Quanta Computer Inc.

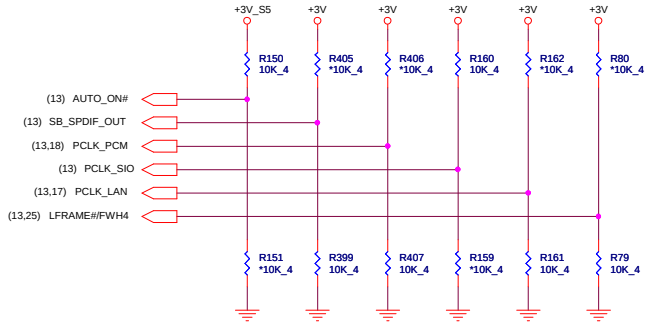
Size	Document Number	Rev
	EXTERNAL CLOCK GENERATOR	1A
Date: Wednesday, October 18, 2006	Sheet 12 of 31	


SB460 SB 27x27mm
Part 1 of 4
U22A
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
SB460
16mA
8/15 For EMI
SB CALIBRATION RESISITOR VALUE
SB600
SB460
R?
562 OHM 1%
150 OHM 1%
2.05K 1%
150 OHM 1%
0 ohm
4.12K 1%
PCIE Power
CLG
RTC
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
ATi recommand have internal pull-up
For SB600, connect to CPU_PG/LDT_PG
For SB460, connect to SSMUXSEL/GPIO0
FOR SB460, THIS BALL IS LDT_RST# ONLY
Add for debug.
9/1 Battery should be connected directly - not through a UL resistor, and not through a diode.
PROJECT : ZR3
Quanta Computer Inc.
SB460M PCIE/PCI/CPU/LPC I/F
Wednesday, October 18, 2006
Sheet 13 of 31


PU/PD
+3V_S5
SUSB# R115 4.7K/F_4
SUSC# R124 4.7K/F_4
DNBSWON# R382 4.7K/F_4
C520 .1U_4
PME# R377 4.7K/F_4
SUS_STAT# R374 10K_4
RI# R378 10K_4
SWI# R104 10K_4
SYS_RST# R153 10K_4
PCIE_WAKE# R110 4.7K/F_4
EMAIL_LED# R379 10K_4
MAX6648_AL# R398 10K_4
AZ_RST# R121 *10K_4
AC_RST# R111 10K_4
CPU_PROCHOT# R363 4.7K/F_4
+3V
RCIN# R72 4.7K/F_4
GATEA20 R66 *10K_4
C466 .1U_4
EXTEVNT1# R338 10K_4
SB_THERMTRIP# R365 10K_4
PCLK_SMB R318 2.2K_4
PDAT_SMB R316 2.2K_4
RST_HDD# R78 10K_4
SB_LLB# R375 *10K_4
GPIO5 R358 4.7K/F_4
GPIO1 R342 10K_4
GPIO6 R317 10K_4
GPIO7 R348 10K_4
GPIO13 R367 10K_4
GPIO31 R85 10K_4
GPIO0 R331 *10K_4
GPIO10 R319 *10K_4
GPIO3 R84 10K_4
GPIO14 R134 10K_4
PCSPK R82 10K_4
CPU_PROCHOT# R97 *10K_4
AC_SDIN2 R116 10K_4
AZ_SDIN1 R165 10K_4
CD_SDIN0 R397 10K_4
AC_BITCLK_R R383 10K_4
AZ_RST# R120 10K_4
AZ_SYNC R386 10K_4
AZ_SDOUT R149 10K_4
AZ_BITCLK R126 10K_4
USB power use S3 power,But
Over current signal datasheet is
S5 only,But ATI FAE say use
S3 is ok
SB_OSCIN R86 *22_4 C233 *10P_4
U22D
SB460 SB 27x27mm
Part 4 of 4
(18,20) PME#
T114
(25) SUSB#
(25) SUSC#
(25) DNBSWON#
(5,13,25) EC_PWRGD
T113
R99 10K_4
R100 10K_4
R98 10K_4
SUS_STAT#
(25) GATEA20
(25) RCIN#
(25) SWI#
T95
(5) CPU_PROCHOT#
(12) SYS_RST#
(20) PCIE_WAKE#
(26) EMAIL_LED#
T119
PME#
RI#
SUSB#
SUSC#
DNBSWON#
GATEA20
RCIN#
SWI#
EXTEVNT1#
CPU_PROCHOT#
SYS_RST#
PCIE_WAKE#
EMAIL_LED#
SB_THERMTRIP#
PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN
KBRST#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT12#
ACPI / WAKE UP EVENTS
USB INTERFACE
Delay 20ms after S5 powerOK
(25) RSMRST#
(12) SB_OSCIN
RSMRST#
SB_OSCIN
RSMRST#
14M_OSC
OSC / RST
GPIO10
GPIO1
GPIO6
GPIO7
(22) RST_HDD#
GPIO5
(23) PCSPK
(7,12,20) PCLK_SMB
(7,12,20) PDAT_SMB
BOARD_ID1
BOARD_ID0
(5,13) CPU_PWRGD
R336 0_4 GPIO0
T112
SB_LLB#
SATA_IS0#/GPIO10
ROM_CS#/GPIO1
GHI#/SATA_IS1#/GPIO6
WD_PWRGD/GPIO7
SMARTVOLT/SATA_IS2#/GPIO4
SHUTDOWN#/GPIO5
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
SSMUXSEL/SATA_IS3#/GPIO0
LLB#/GPIO66
GPIO
USB_OCP9#
USB_OCP8#
USB_OCP7#
AZ_RST#
USB_OCP4#
USB_OCP3#
USB_OCP2#
(25) SCI#
(25) KBSMI#
SCI#
KBSMI#
USB_OC9#/SLP_S2/GPM9#
USB_OC8#/AZ_DOCK_RST#/GPM8#
USB_OC7#/GEVENT7#
USB_OC6#/GEVENT6#
USB_OC5#/DDR3_RST#/GPM5#
USB_OC4#/GPM4#
USB_OC3#/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#
USB OC
AZ_BITCLK
AZ_SDOUT
AZ_SYNC
T61
T60
(16) AC_SDOUT
(23) CD_SDIN0
(23) AZ_SDIN1
T116
T57
T115
T56
AC_BITCLK_R
CD_SDIN0
AZ_SDIN1
AC_SDIN2
AC_SYNC_R
AC_RST#
AZ_BITCLK
AZ_SDOUT
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AC_BITCLK/GPIO38
AC_SDOUT/GPIO39
ACZ_SDIN0/GPIO42
ACZ_SDIN1/GPIO43
ACZ_SDIN2/GPIO44
AC_SYNC/GPIO40
AC_RST#/GPIO45
AZALIA
AC97
T43
(13) H_DPSLP#
T66
(5) MAX6648_AL#
(5,10,13) LDT_STOP#
T47
GPIO3
GPIO31
GPIO13
H_DPSLP#
GPIO14
MAX6648_AL#
R117 0_4
NC1
NC2
NC3
NC4
NC5
NC6
NC7
NC8
SB460
USB PWR
R89 *22_4 C241 *10P_4
USBCLK
SB_48M_X1
USB_RCOMP
R90 11.8K/F_4
USB_ATEST1
USB_ATEST0
T106
T109
USB_HSDP9+
USB_HSDM9-
T53
T52
USB_HSDP8+
USB_HSDM8-
T51
T54
USB_HSDP7+
USB_HSDM7-
USBP7+ (20)
USBP7- (20)
USB_HSDP6+
USB_HSDM6-
USBP6+ (20)
USBP6- (20)
USB_HSDP5+
USB_HSDM5-
USB_HSDP4+
USB_HSDM4-
USBP4+ (20)
USBP4- (20)
USB_HSDP3+
USB_HSDM3-
USB_HSDP2+
USB_HSDM2-
USBP2+ (20)
USBP2- (20)
USB_HSDP1+
USB_HSDM1-
USBP1+ (20)
USBP1- (20)
USB_HSDP0+
USB_HSDM0-
USBP0+ (20)
USBP0- (20)
USB0: D/B IO
USB1: D/B IO
USB2: D/B IO
USB4: M/B IO
USB6: BLUETOOTH
USB7: MINI CARD
USB power
AVDD_USB
L63 TI201209G121
+3V_S5
AVDDTX_0
AVDDTX_1
AVDDTX_2
AVDDTX_3
AVDDTX_4
AVDDRX_0
AVDDRX_1
AVDDRX_2
AVDDRX_3
AVDDRX_4
C255 .1U_4
C245 .1U_4
C262 .1U_4
C274 .1U_4
C282 .1U_4
C505 1U/10V_6
C502 22U/10V_8
+3.3V_AVDDC
+3V_S5
L18 SBK160808T-301Y-S
AVDDC
AVSSC
C277 1U/10V_6
C259 .1U_4
C263 2.2U/10V_8
AVSS_USB_1
AVSS_USB_2
AVSS_USB_3
AVSS_USB_4
AVSS_USB_5
AVSS_USB_6
AVSS_USB_7
AVSS_USB_8
AVSS_USB_9
AVSS_USB_10
AVSS_USB_11
AVSS_USB_12
AVSS_USB_13
AVSS_USB_14
AVSS_USB_15
AVSS_USB_16
AVSS_USB_17
AVSS_USB_18
AVSS_USB_19
AVSS_USB_20
AVSS_USB_21
AVSS_USB_22
AVSS_USB_23
AVSS_USB_24
AVSS_USB_25
AVSS_USB_26
AVSS_USB_27
AVSS_USB_28
AVSS_USB_29
AVSS_USB_30
AVSS_USB_31
AVSS_USB_32
AVSS_USB_33
+3V
R315 *10K_4 BOARD_ID0 R314 10K_4
R296 *10K_4 BOARD_ID1 R320 10K_4
Board ID | ID1 | ID0
00 | | | PATA HDD
01 | | | SATA HDD
10 | | |
11 | | |
+3V_S5
KBSMI# R366 4.7K/F_4
RP4 10KX2_4
USB_OCP2#
SCI#
RP5 *10KX2_4
USB_OCP9#
USB_OCP8#
RN32 10KX4_4
USB_OCP3#
USB_OCP4#
USB_OCP6#
USB_OCP7#
(23) CD_BITCLKA_MDC
R125 39_4
C308 *22P_4
(23) AZ_BITCLKA
R127 39_4
C309 *22P_4
AZ_BITCLK
(23) CD_SDOUTA_MDC
R140 39_4
C329 33P_4
(23) AZ_SDOUTA
R139 39_4
C328 33P_4
AZ_SDOUT
(23) CD_SYNC_MDC
R384 39_4
C512 *22P_4
(23) AZ_SYNCA
R385 39_4
C513 *22P_4
AZ_SYNC
(23) CD_RESET#_MDC
R122 39_4
C295 *22P_4
(23,24) AZ_RESET#
R123 39_4
C301 *22P_4
AZ_RST#
09/07 Stuff C329,C328 to 33P For EMI Situation.
CLG
PROJECT : ZR3
Quanta Computer Inc.
Size Custom
Document Number
SB460M ACPI/GPIO/USB/AC97
Rev 1A
Date: Wednesday, October 18, 2006
Sheet 14 of 31


SB460 SB 27x27mm
Part 2 of 4
SERIAL ATA
ATA 66/100
SPI ROM
HW MONITOR
SERIAL ATA POWER
SATA Power
D3A:R347 When PATA mount CS00002JB38
SATA And Osc mount CS04992FB31
SB4600 SB 27x27mm
Part 3 of 4
POWER
80ohm/4A
300ohm(200mA)
CPU_PWR=1.8V WHEN SB600
CPU_PWR=1.2V WHEN SB460
PROJECT : ZR3
Quanta Computer Inc.
SB460M HDD/POWER/DECOUPLING
Wednesday, October 18, 2006
Sheet 15 of 31



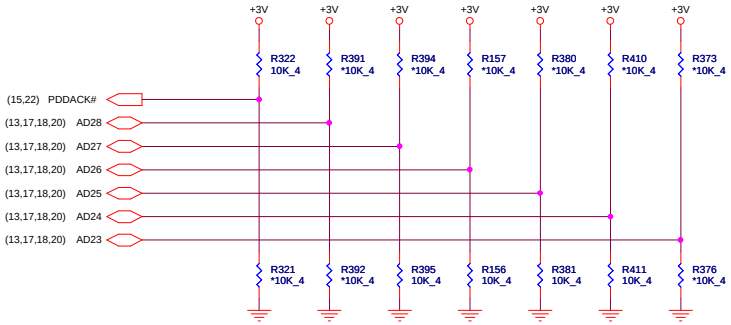


REQUIRED STRAPS

	AC_SDOUT	RTC_CLK	PCI_CLK4	PCI_CLK6	PCLK_MINI PCLK_591
					PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = LPC TYPE I ROM DEFAULT L, H = LPC TYPE II ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC	USE EXT. 48MHZ DEFAULT	CPU IF=P4	NOTE:FOR SB460,PCICLK[8:7] ARE CONNECTED TO SUBSTRATE BALLS PCICLK[1:0]

	AUTO_ON#	SB_SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCLK_LAN	LFRAME#
	ACPWRON	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK5	LFRAME#
PULL HIGH	MANUAL PWR ON DEFAULT	SIO 24MHz	XTAL MODE NOT SUPPORTED	USB PHY POWERDOWN DISABLE DEFAULT	PCIE_CM_SET HIGH	ENABLE THERMTRIP#
PULL LOW	AUTO PWR ON	SIO 48MHz DEFAULT	48MHZ OSC MODE DEFAULT	USB PHY POWERDOWN ENABLE	PCIE_CM_SET HLOW DEFAULT	DISABLE THERMTRIP# DEFAULT

BIOS ENABLE AFTER STARTUP



DEBUG STRAPS

	PDACK#	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE SHORT RESET		USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

CLG

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB460M STRAPS	1A
Date: Wednesday, October 18, 2006	Sheet 16 of 31	

ID Select : AD18
Interrupt Pin : INTF#
Request Indicate : REQ0#
Grant Indicate : GNT0#

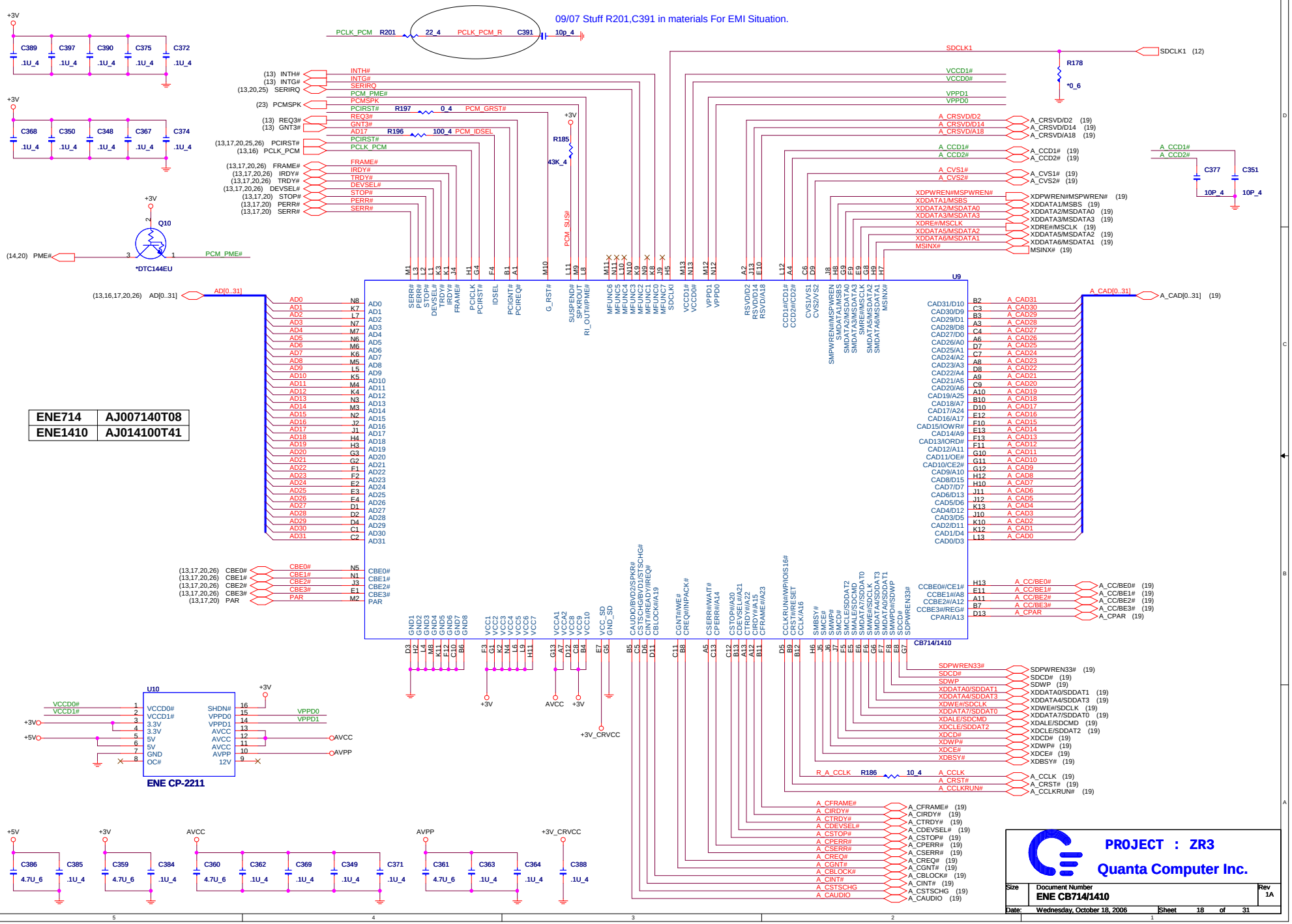
U6
RTL8110SBL
RTL8100CL
PCI
VDD33---+3.3V DIGITAL
AVDDH------+3.3V ANALOG
AVDDL-----+2.5V ANALOG
DVDD-----+1.2V DIGITAL
DVDD_A----+1.2V ANALOG
VDD33---+3.3V DIGITAL
AVDDL-----+3.3V ANALOG
DVDD-----+2.5V DIGITAL
AVDDH------+2.5V ANALOG
RTL8100CL

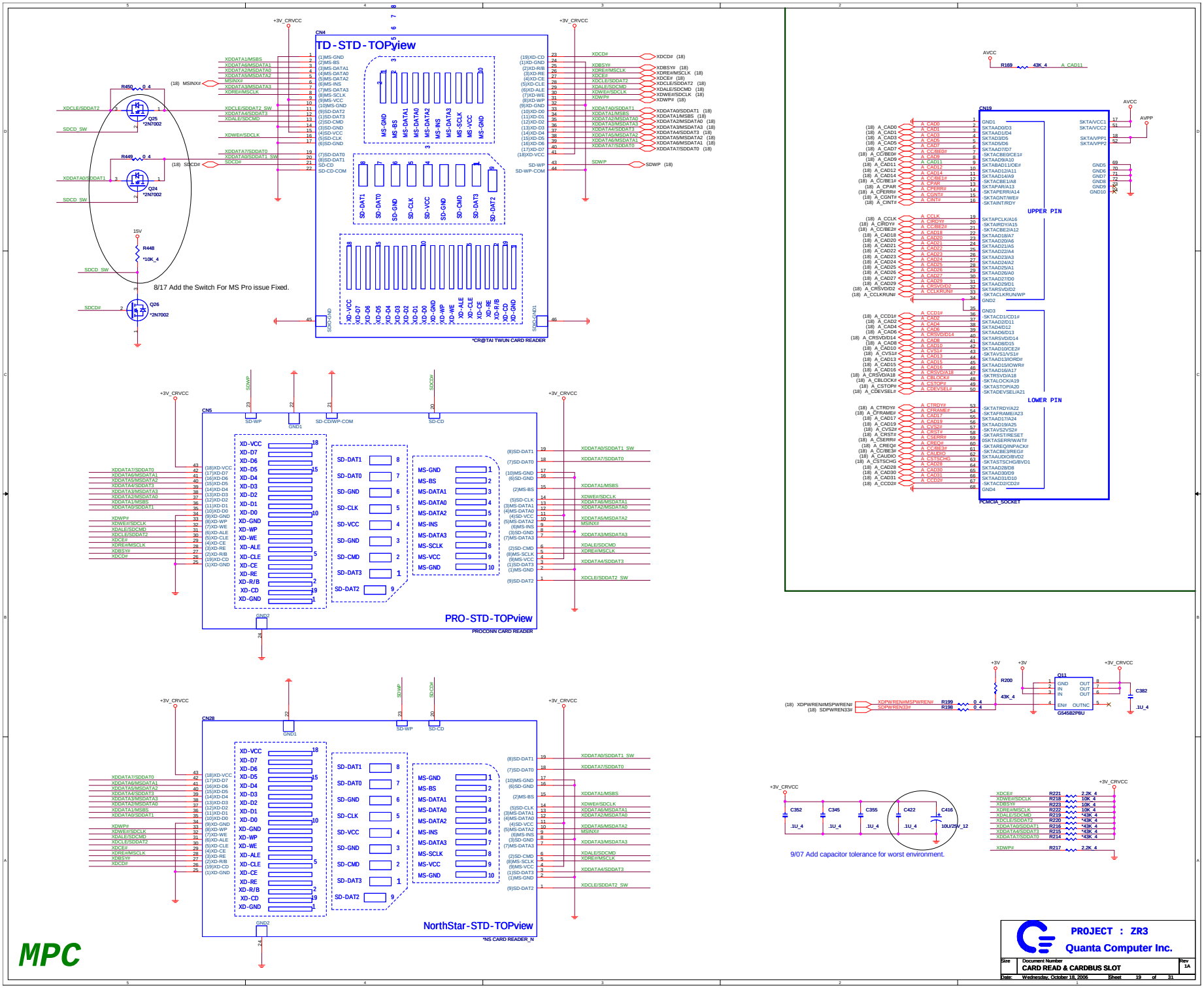
8/16 Reserve circuit For close Lan chips.
Near Lan chipset
8/16 Change 27P To Match the frequency stability
93C46-3GR
LAN

Near Transformer
NS681687
9/11 Change to 0.01uF For different from reference design.
RJ45

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	LAN RTL8110SBL/8100CL	1A
Date: Wednesday, October 18, 2006	Sheet 17 of 31	


09/07 Stuff R201,C391 in materials For EMI Situation.
ENE714 AJ007140T08
ENE1410 AJ014100T41
U9
CB714/1410
U10
ENE CP-2211
PROJECT : ZR3
Quanta Computer Inc.
Size
Document Number
ENE CB714/1410
Rev
1A
Date: Wednesday, October 18, 2006
Sheet 18 of 31


TD-STD-TOPview
CN4
*CR@TAI TWUN CARD READER
8/17 Add the Switch For MS Pro issue Fixed.
PRO-STD-TOPview
CN5
PROCONN CARD READER
NorthStar-STD-TOPview
CN28
*NS CARD READER_N
CN19
PCMCIA_SOCKET
UPPER PIN
LOWER PIN
9/07 Add capacitor tolerance for worst environment.
PROJECT : ZR3
Quanta Computer Inc.
CARD READ & CARDBUS SLOT
Wednesday, October 18, 2006
MPC

ID Select : AD20
Interrupt Pin : INTF# , INTG#
Request Indicate : REQ2#
Grant Indicate : GNT2#

MINI-PCI

CN24 MINIPCI

09/07 Stuff R431,C542 in materials For EMI Situation.

*DTC144EU

MPC

CN17 *MINIPCI_50P_H9

Close Minicard connector

USB

TPS2061DGNR

CN14 USB

*DLW21HN900SQ2L

CN9 B2B

BLUETOOTH MODULE CONNECTOR

*DLW21HN900SQ2L

CN16 USB_BT

AO3403

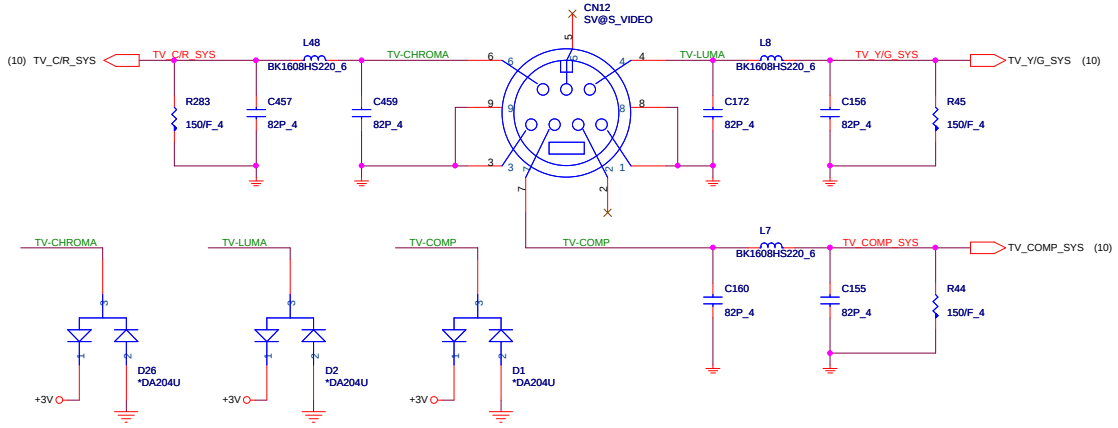
FOR EMI

PROJECT : ZR3
Quanta Computer Inc.

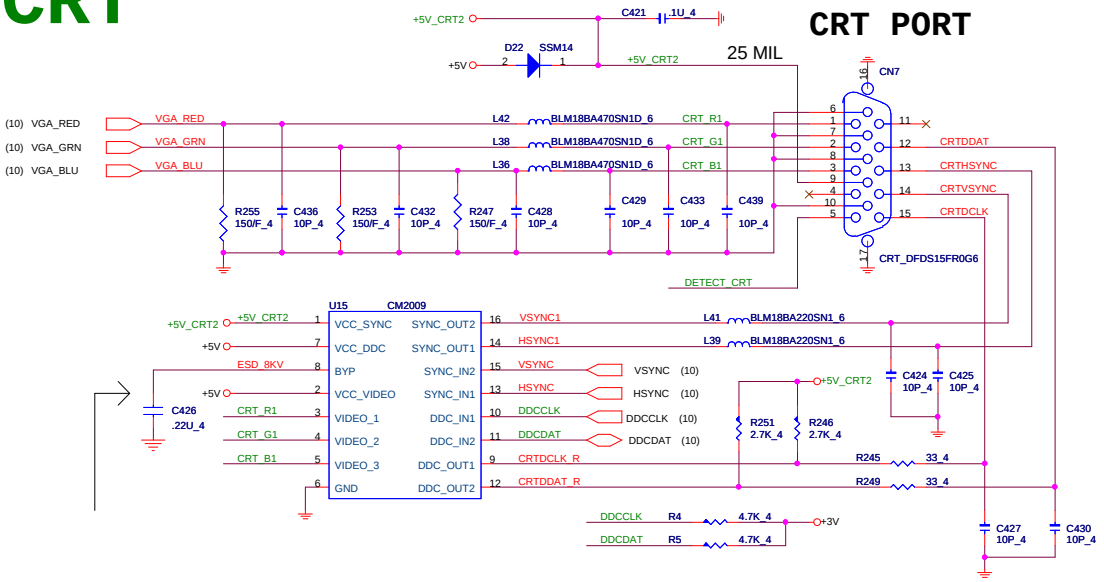
Size	Document Number	Rev
	MINI PCI&PCI-E,USB PORT	1A

Date: Wednesday, October 18, 2006 Sheet 20 of 31

S-VIDEO



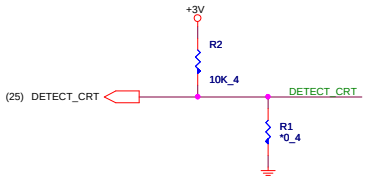
CRT

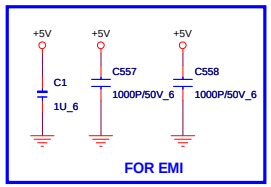


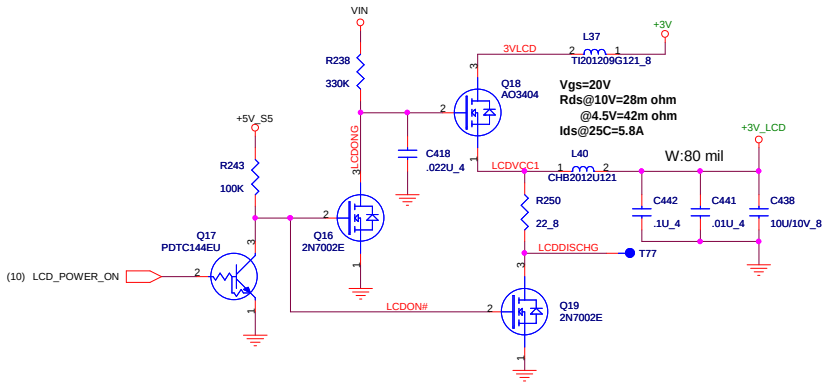
increase capability of ESD, from +-4KV improve to +-8KV.

System Auto Detect External CRT Device

	R247	R248	R249
Enable	Not stuffed	Stuffed	Stuffed
Disable (Default)	Stuffed	Not stuffed	Stuffed

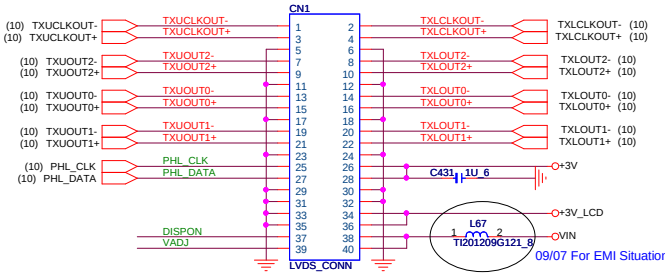




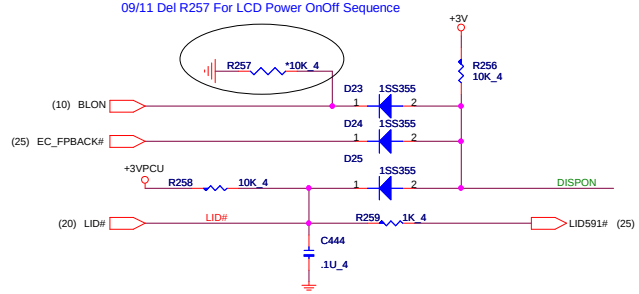


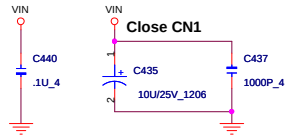
LVDS

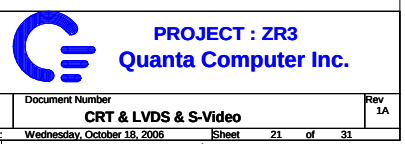
LCD Connector



09/11 Del R257 For LCD Power OnOff Sequence

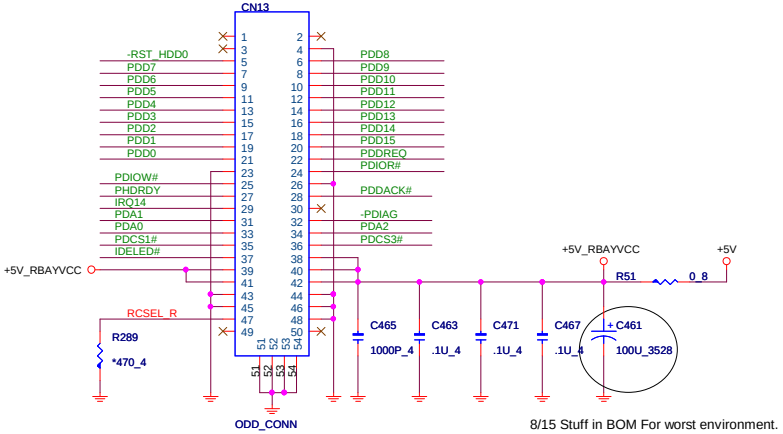






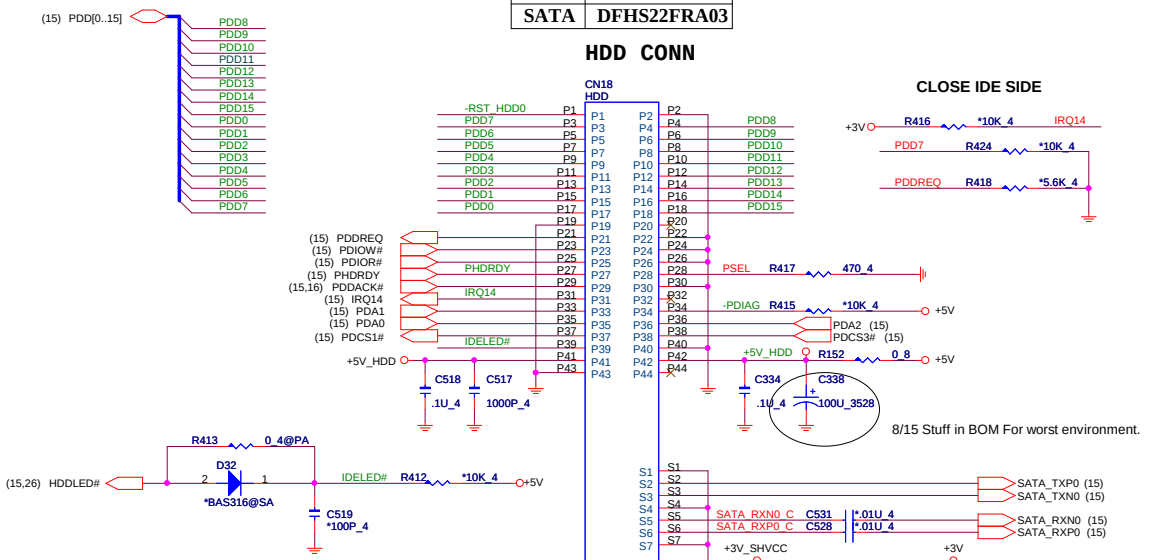
PATA	DFHS44FRD28
SATA	DFHS22FRA03

ODD CONN

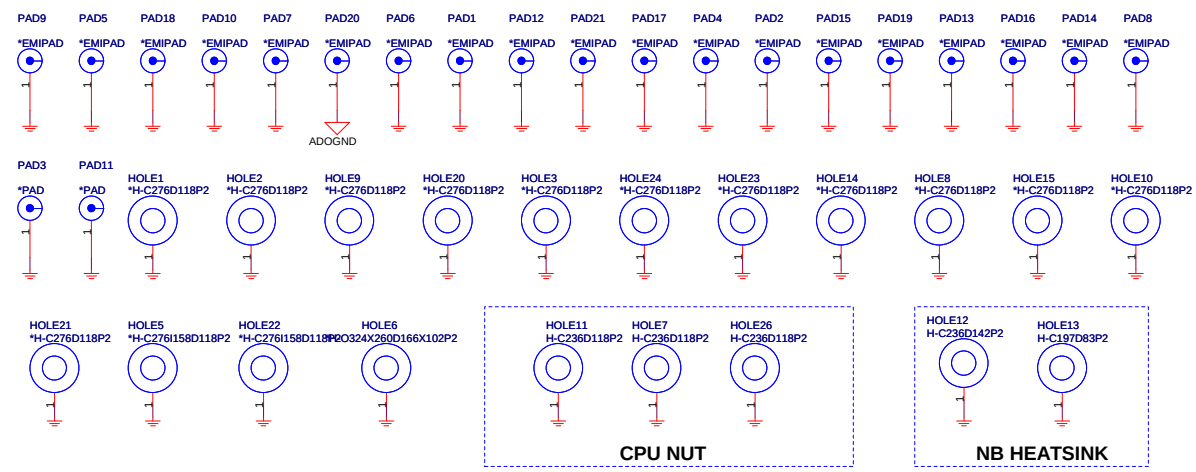


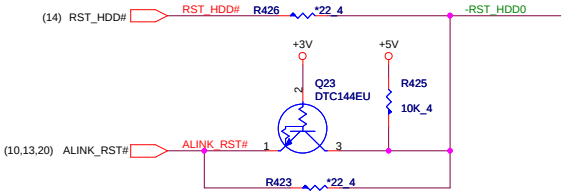
8/15 Stuff in BOM For worst environment.

HDD CONN



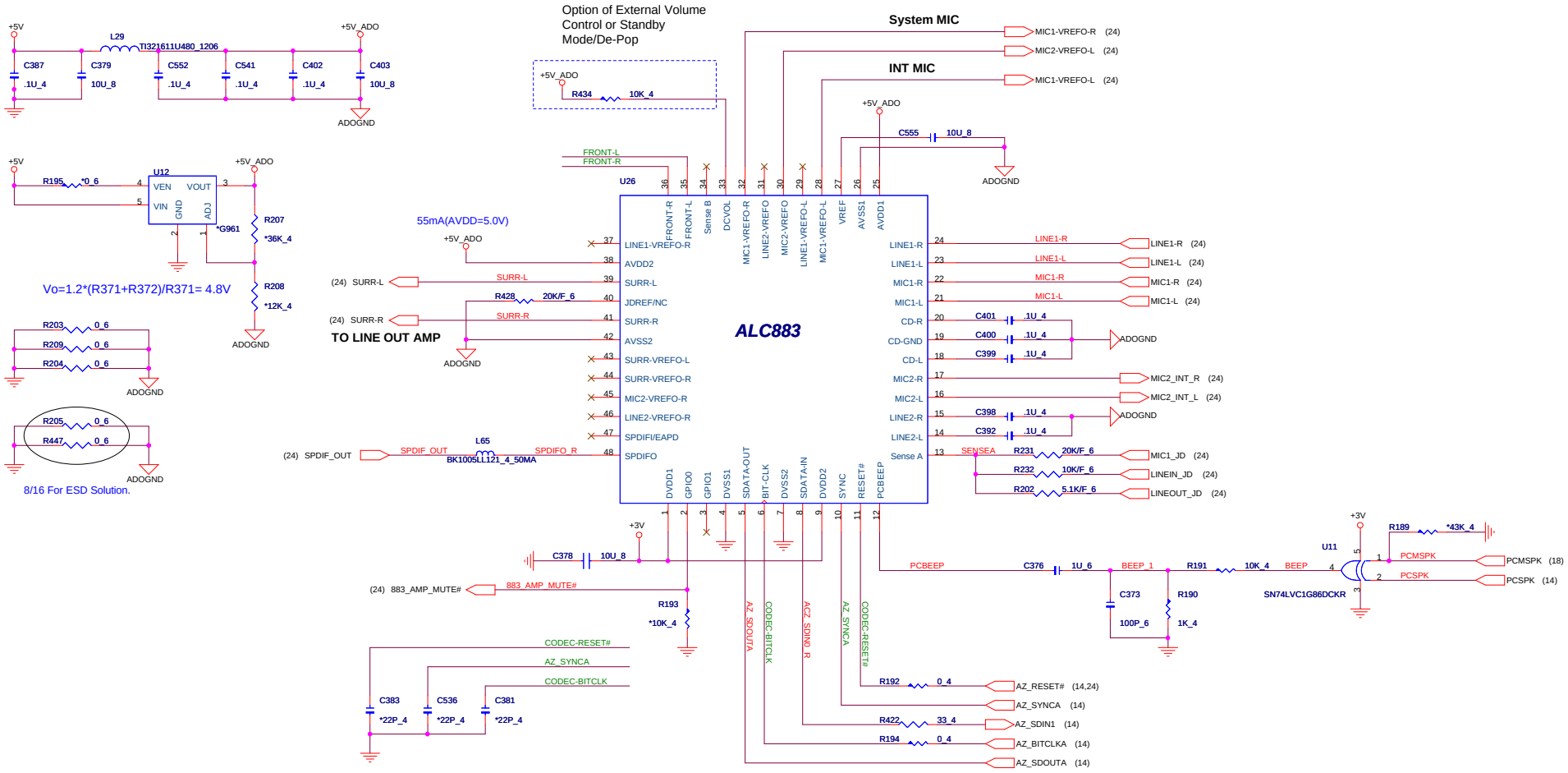
8/15 Stuff in BOM For worst environment.





PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	HDD & CDROM & HOLES	1A
Date: Wednesday, October 18, 2006	Sheet 22 of 31	



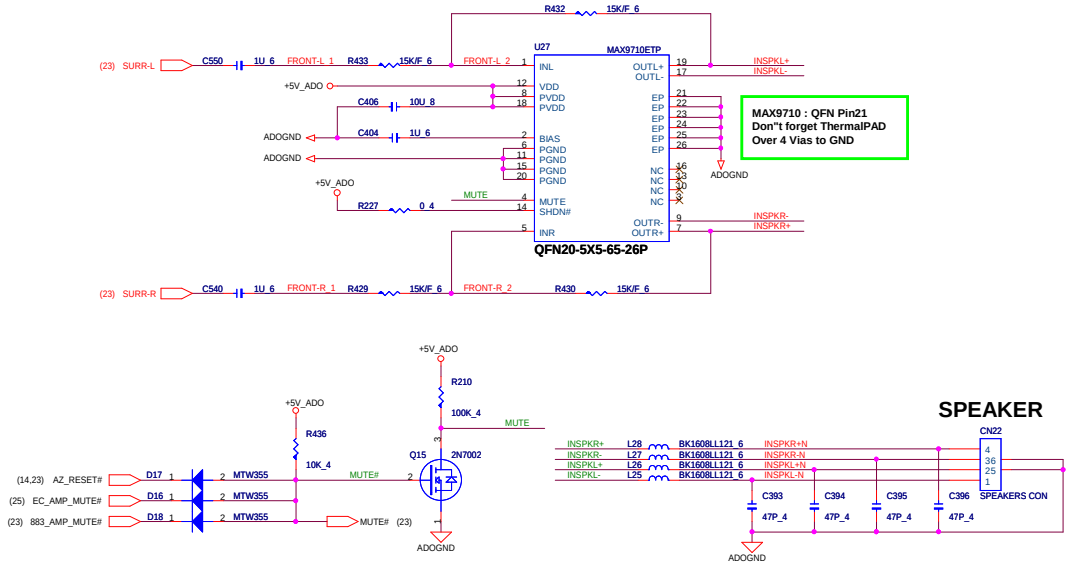
LINE OUT AMPLIFIER

MDC Module

PROJECT : ZR3
Quanta Computer Inc.

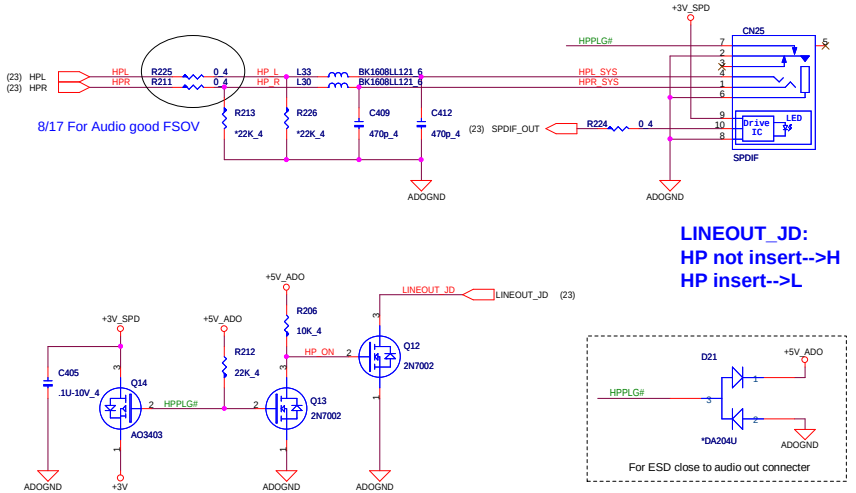
Size	Document Number	Rev
Custom	ALC883 & MDC & HP AMP	1A
Date: Wednesday, October 18, 2006	Sheet 23 of 31	

Speaker Amplifier MAX9710



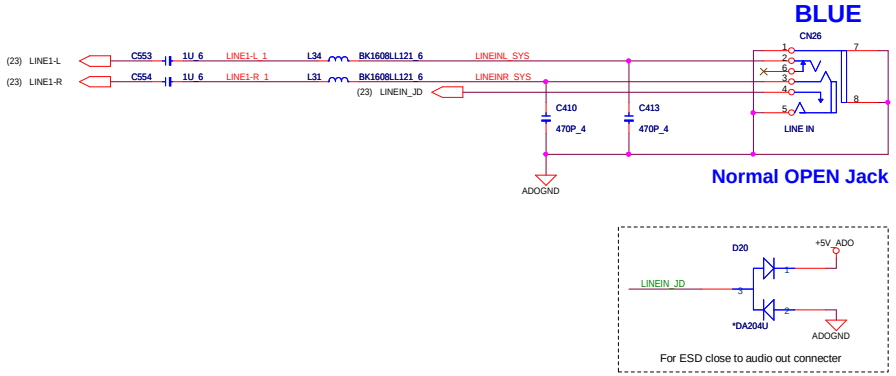
SYSTEM LINE OUT/SPDIF

BLACK



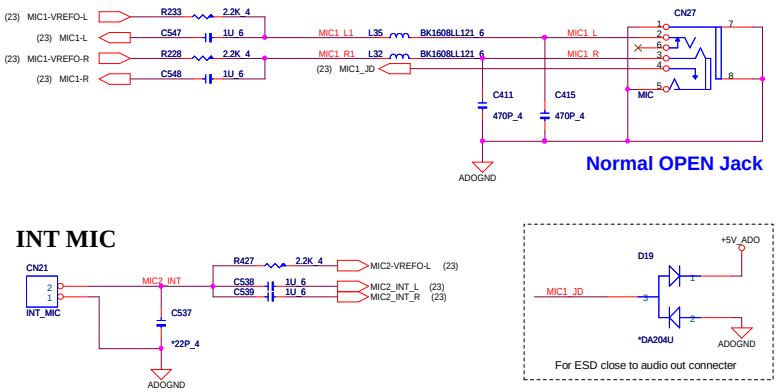
SYSTEM LINE IN

BLUE

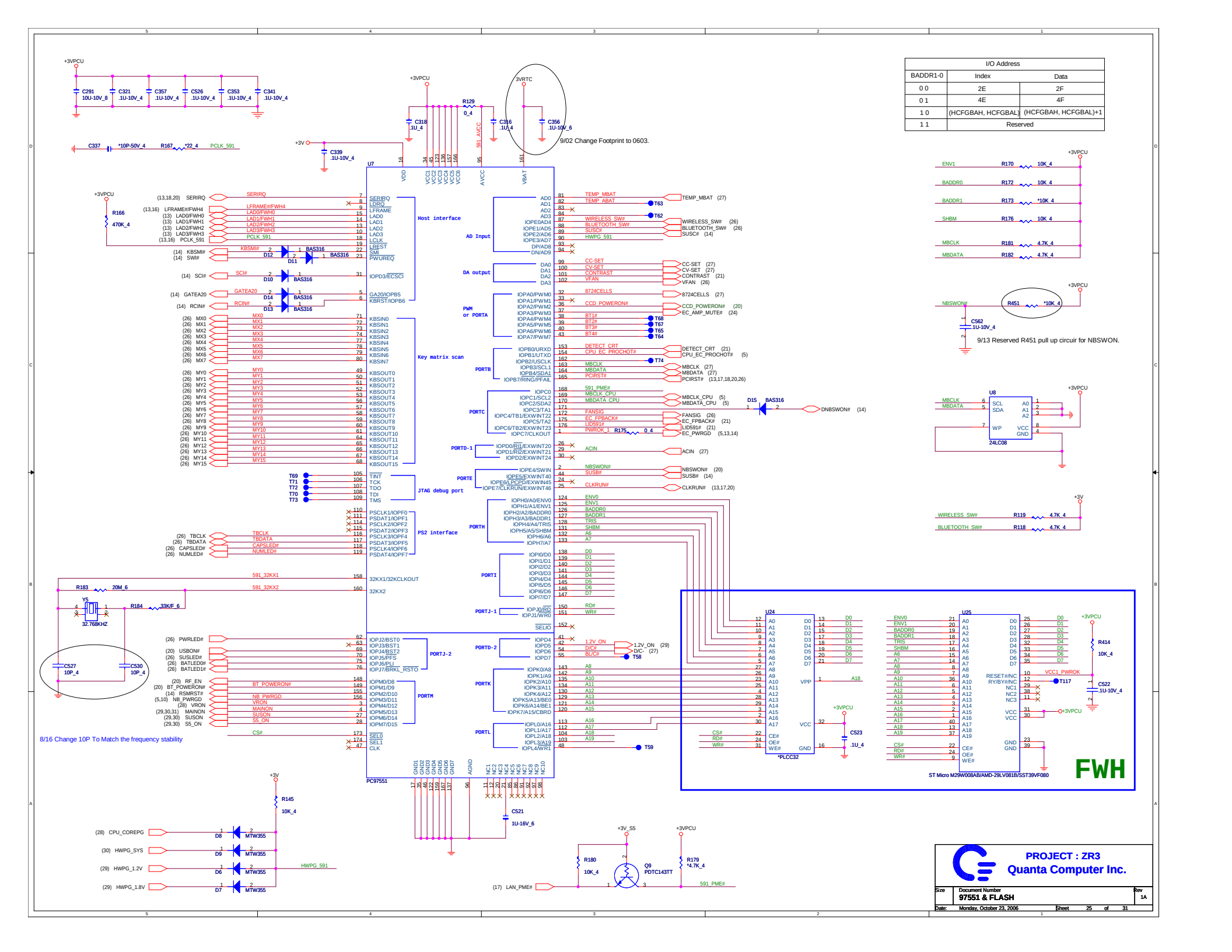


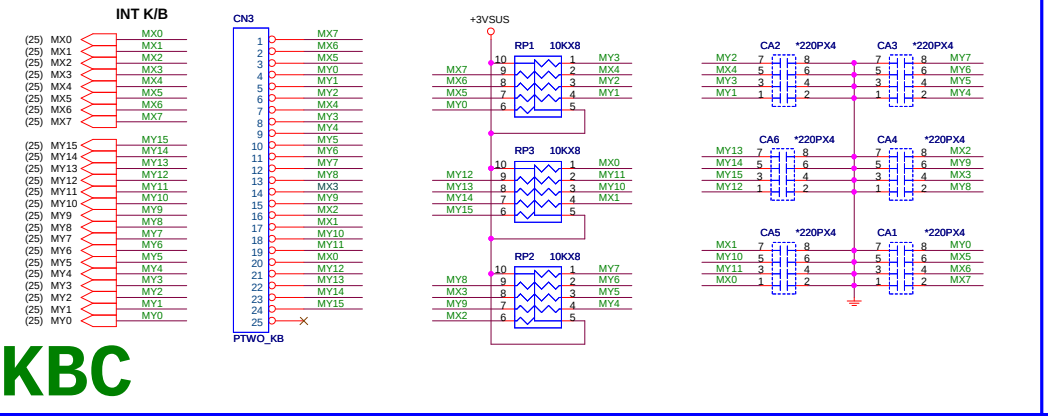
SYSTEM MIC

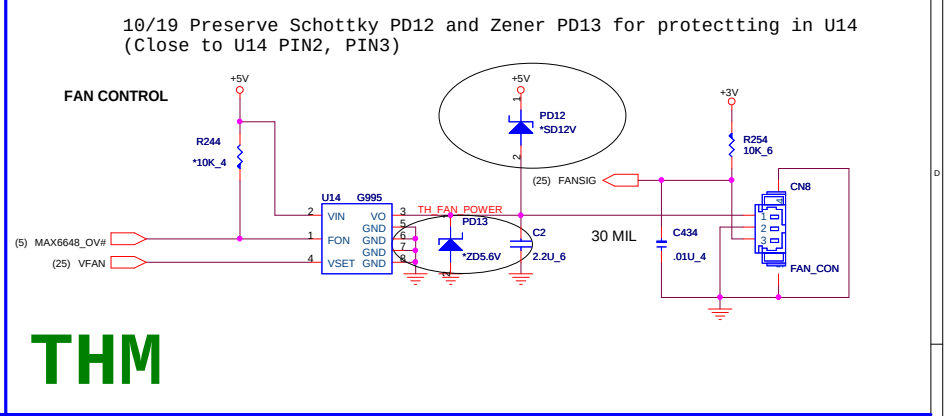
PINK

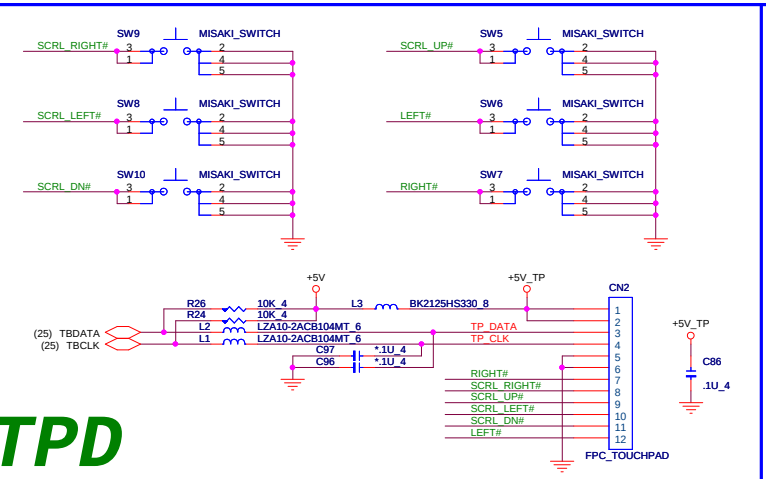


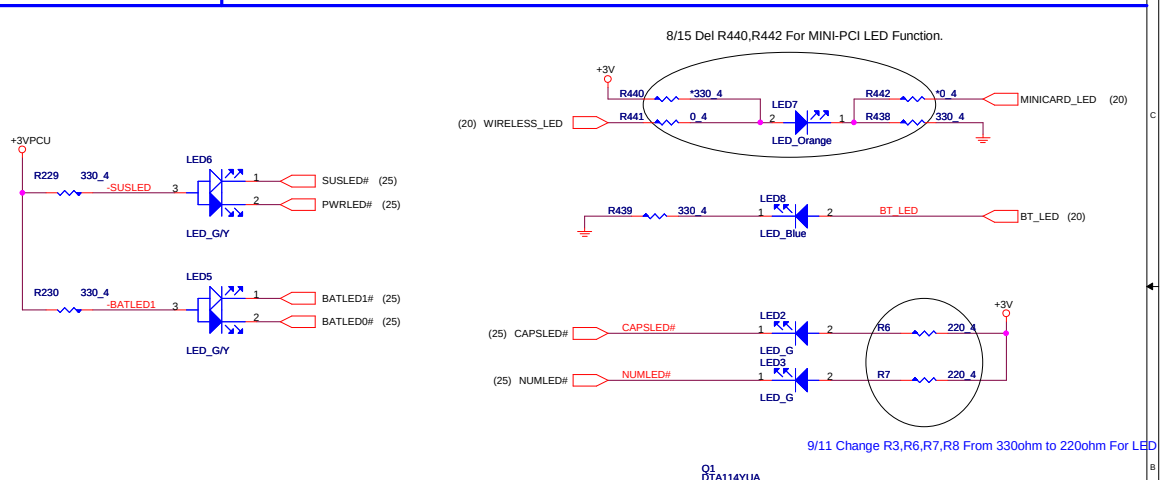
PROJECT : ZR3		
Quanta Computer Inc.		
Size: Custom	Document Number: SPEAKER AMP / JACK	Rev: 1A
Date: Wednesday, October 18, 2006	Sheet 24 of 31	

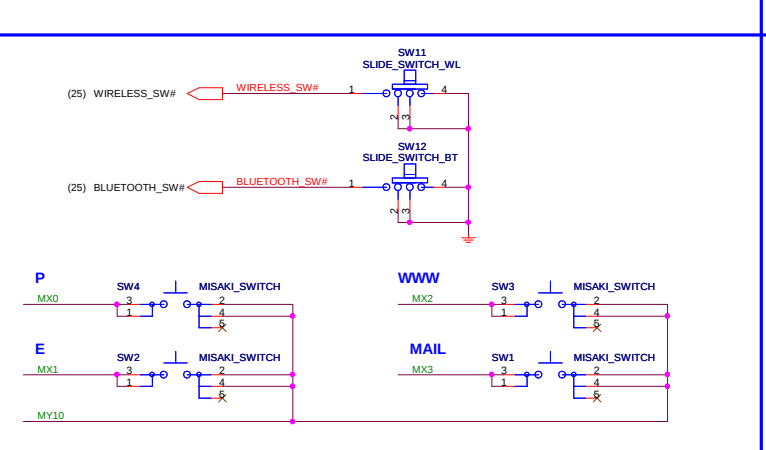

I/O Address
BADDR1-0 | Index | Data
0 0 | 2E | 2F
0 1 | 4E | 4F
1 0 | (HCFGBAH, HCFGBAL) | (HCFGBAH, HCFGBAL)+1
1 1 | Reserved
9/02 Change Footprint to 0603.
9/13 Reserved R451 pull up circuir for NBSWON.
8/16 Change 10P To Match the frequency stability
U7
PC97551
Host interface
AD Input
DA output
PWM or PORTA
Key matrix scan
PORTB
PORTC
PORTD-1
PORTE
JTAG debug port
PS2 interface
PORTH
PORTI
PORTJ-1
PORTD-2
PORTJ-2
PORTK
PORTM
PORTL
U24
*PLCC32
U25
ST Micro M29W008AB/AMD-29LV081B/SST39VF080
U8
24LC08
FWH
PROJECT : ZR3
Quanta Computer Inc.
Document Number
97551 & FLASH
Rev
1A
Date: Monday, October 23, 2006
Sheet 25 of 31

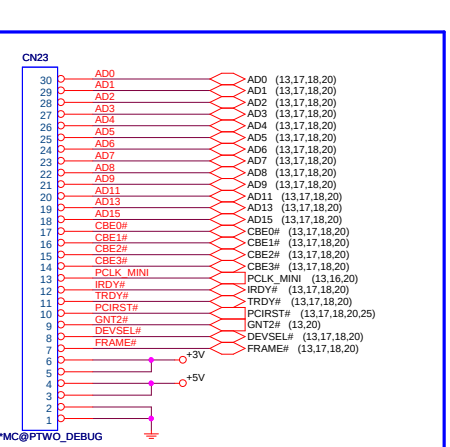

INT K/B
CN3
PTWO_KB
+3VSUS
RP1 10KX8
RP3 10KX8
RP2 10KX8
CA2 *220PX4
CA3 *220PX4
CA6 *220PX4
CA4 *220PX4
CA5 *220PX4
CA1 *220PX4
KBC

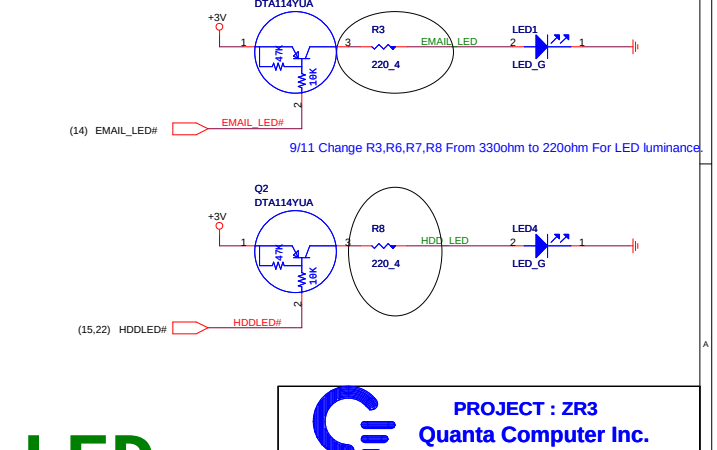

10/19 Preserve Schottky PD12 and Zener PD13 for protectting in U14
(Close to U14 PIN2, PIN3)
FAN CONTROL
R244
*10K_4
U14 G995
VIN VO
GND
FON GND
GND
VSET GND
(5) MAX6648_OV#
(25) VFAN
TH_FAN_POWER
PD13
*ZD5.6V
C2
2.2U_6
PD12
*SD12V
(25) FANSIG
30 MIL
C434
.01U_4
R254
10K_6
CN8
FAN_CON
THM

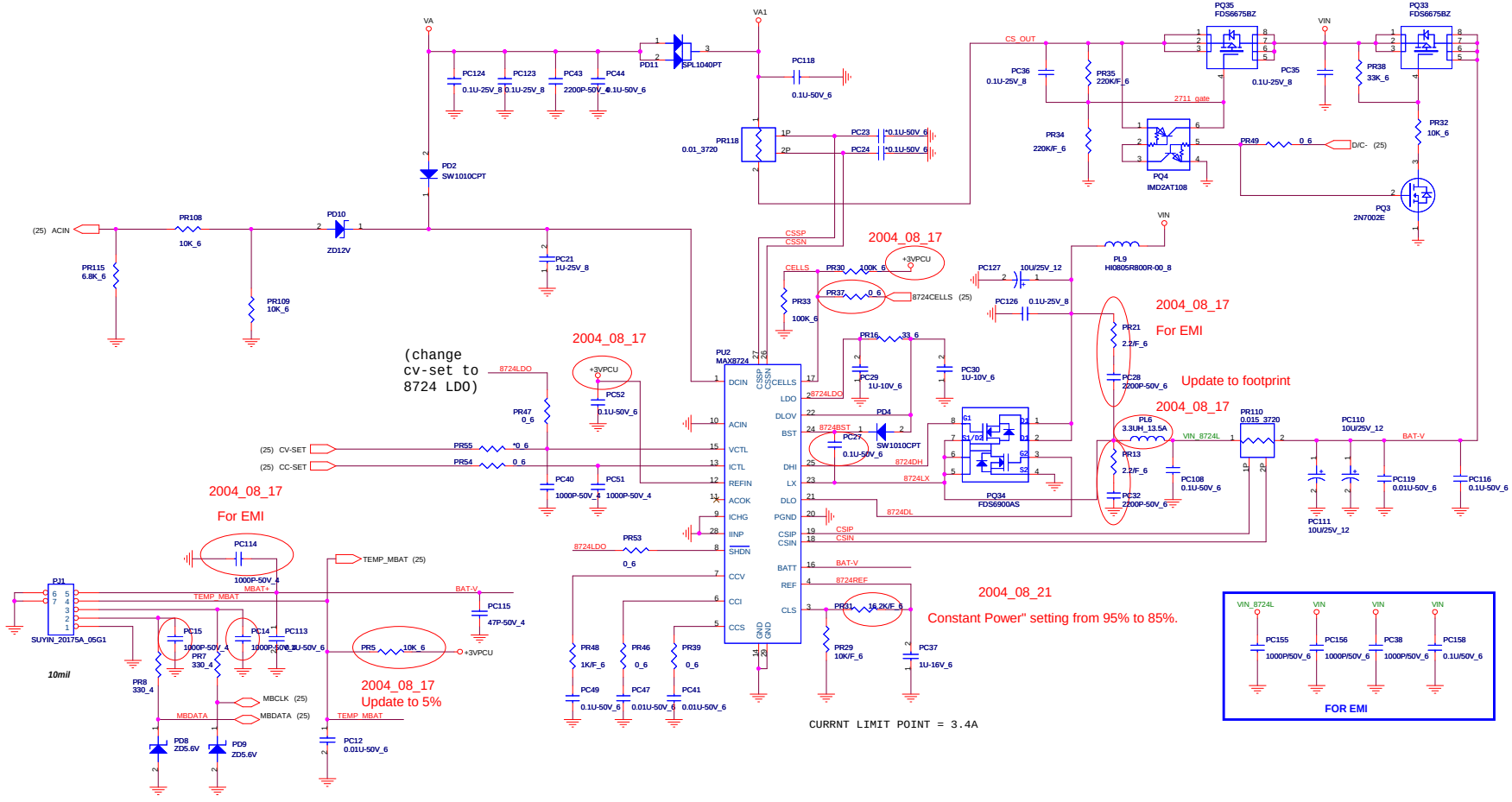

SW9 MISAKI_SWITCH SCRL_RIGHT#
SW8 MISAKI_SWITCH SCRL_LEFT#
SW10 MISAKI_SWITCH SCRL_DN#
SW5 MISAKI_SWITCH SCRL_UP#
SW6 MISAKI_SWITCH LEFT#
SW7 MISAKI_SWITCH RIGHT#
+5V
+5V_TP
R26 10K_4
R24 10K_4
L3 BK2125HS330_8
L2 LZA10-2ACB104MT_6
L1 LZA10-2ACB104MT_6
C97 *1U_4
C96 *1U_4
(25) TBDATA
(25) TBCLK
TP_DATA
TP_CLK
CN2
FPC_TOUCHPAD
C86 .1U_4
TPD


8/15 Del R440,R442 For MINI-PCI LED Function.
+3VPCU
R229 330_4 -SUSLED
R230 330_4 -BATLED1
LED6
LED5
LED_G/Y
SUSLED# (25)
PWRLED# (25)
BATLED1# (25)
BATLED0# (25)
+3V
R440 *330_4
R441 0_4
LED7
LED_Orange
R442 *0_4
R438 330_4
(20) WIRELESS_LED
MINICARD_LED (20)
R439 330_4
LED8
LED_Blue
BT_LED
BT_LED (20)
(25) CAPSLED#
CAPSLED#
LED2
LED_G
R6 220_4
(25) NUMLED#
NUMLED#
LED3
R7 220_4
9/11 Change R3,R6,R7,R8 From 330ohm to 220ohm For LED
Q1
DTA114YUA
R3 220_4
EMAIL_LED
LED1
(14) EMAIL_LED#
9/11 Change R3,R6,R7,R8 From 330ohm to 220ohm For LED luminance.
Q2
DTA114YUA
R8 220_4
HDD_LED
LED4
(15,22) HDDLED#
LED


SW11 SLIDE_SWITCH_WL
(25) WIRELESS_SW#
WIRELESS_SW#
SW12 SLIDE_SWITCH_BT
(25) BLUETOOTH_SW#
BLUETOOTH_SW#
P
MX0
SW4 MISAKI_SWITCH
E
MX1
SW2 MISAKI_SWITCH
MY10
WWW
MX2
SW3 MISAKI_SWITCH
MAIL
MX3
SW1 MISAKI_SWITCH
QUICK KEY SWITCH


CN23
AD0 (13,17,18,20)
AD1 (13,17,18,20)
AD2 (13,17,18,20)
AD3 (13,17,18,20)
AD4 (13,17,18,20)
AD5 (13,17,18,20)
AD6 (13,17,18,20)
AD7 (13,17,18,20)
AD8 (13,17,18,20)
AD9 (13,17,18,20)
AD11 (13,17,18,20)
AD13 (13,17,18,20)
AD15 (13,17,18,20)
CBE0# (13,17,18,20)
CBE1# (13,17,18,20)
CBE2# (13,17,18,20)
CBE3# (13,17,18,20)
PCLK_MINI (13,16,20)
IRDY# (13,17,18,20)
TRDY# (13,17,18,20)
PCIRST# (13,17,18,20,25)
GNT2# (13,20)
DEVSEL# (13,17,18,20)
FRAME# (13,17,18,20)
+3V
+5V
*MC@PTWO_DEBUG
Debug card interface

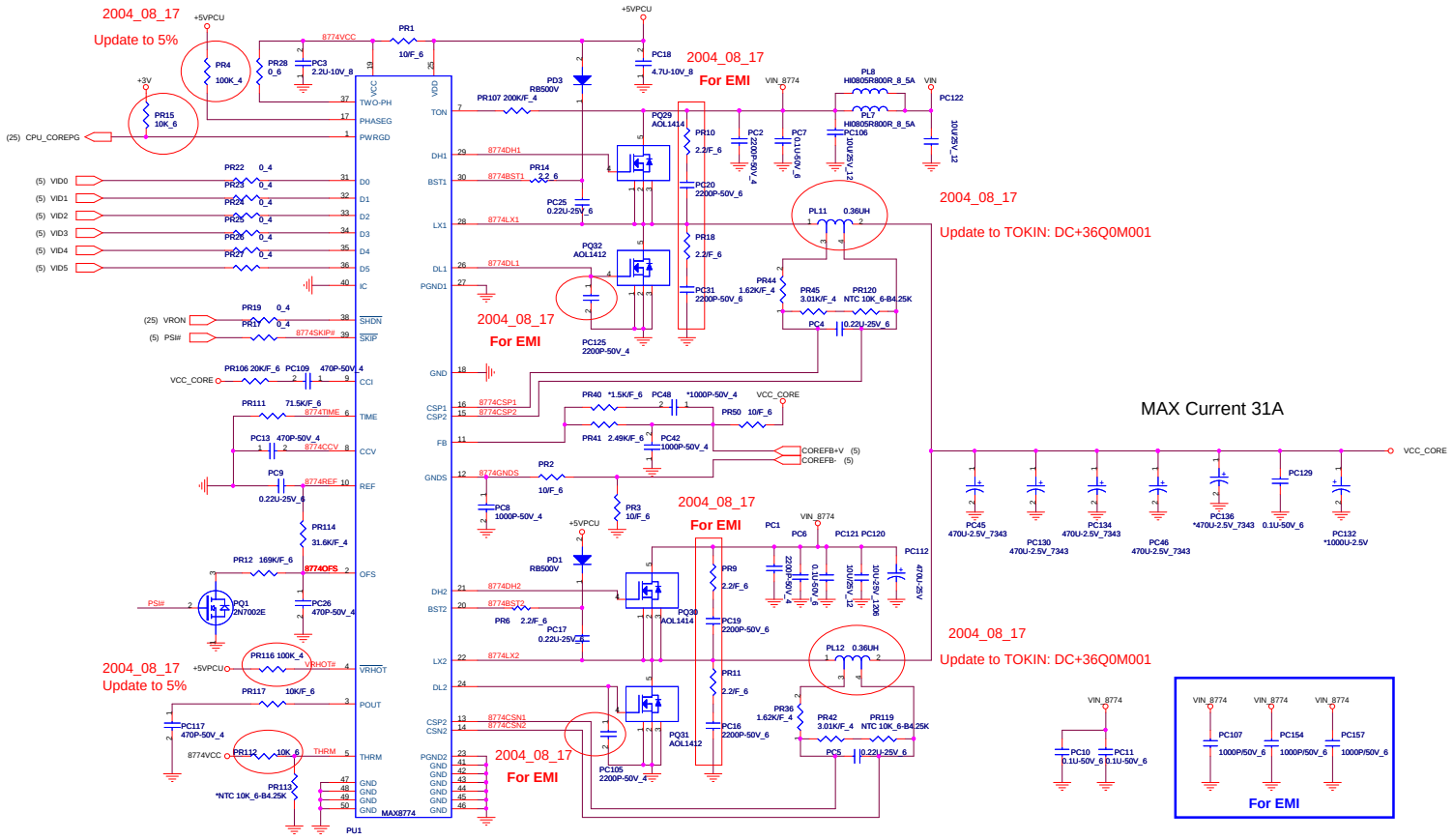

LED
PROJECT : ZR3
Quanta Computer Inc.
Size
Document Number
T/P,FAN,SWITCH,LED,K/B
Rev
1A
Date: Monday, October 23, 2006
Sheet 26 of 31

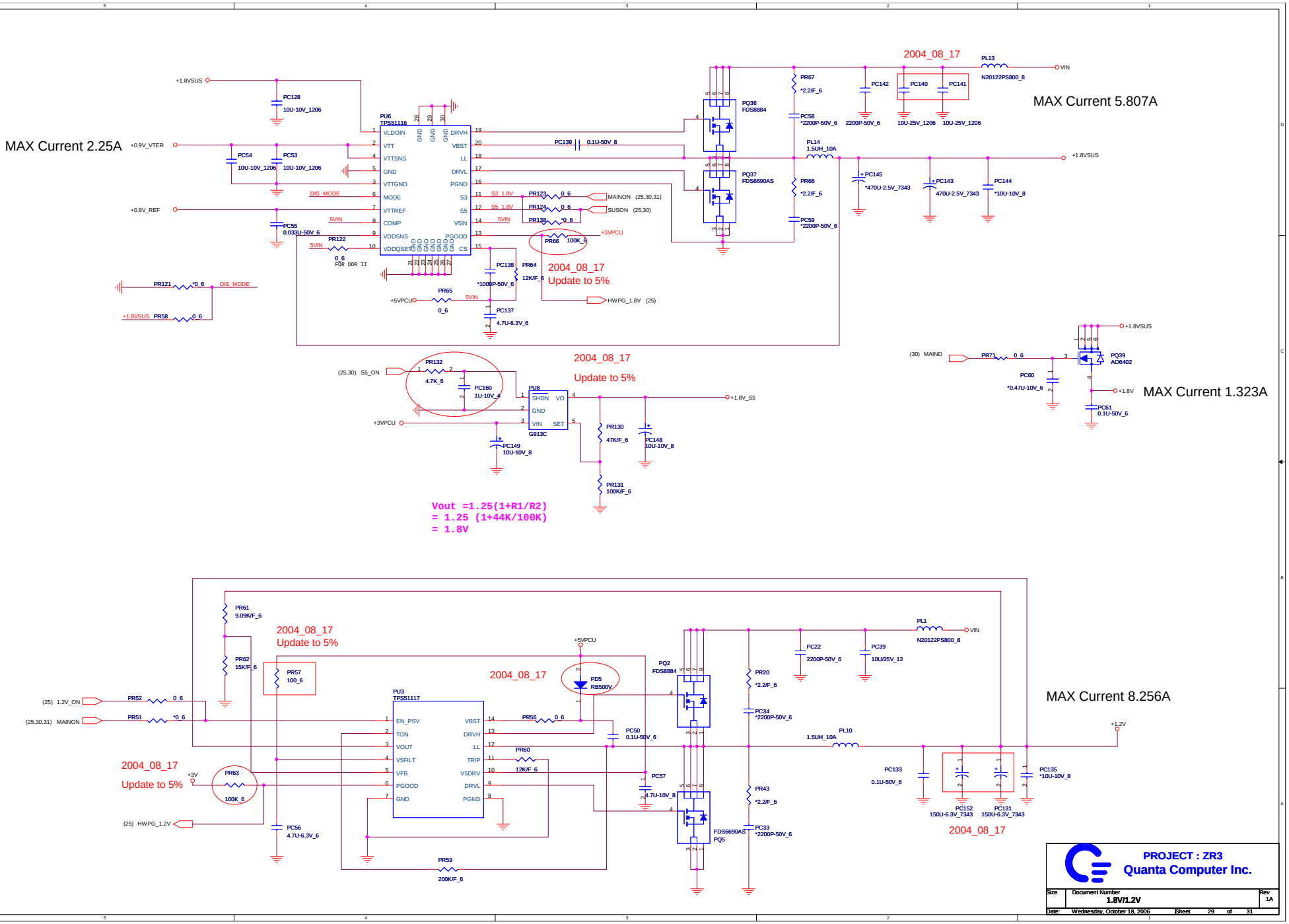


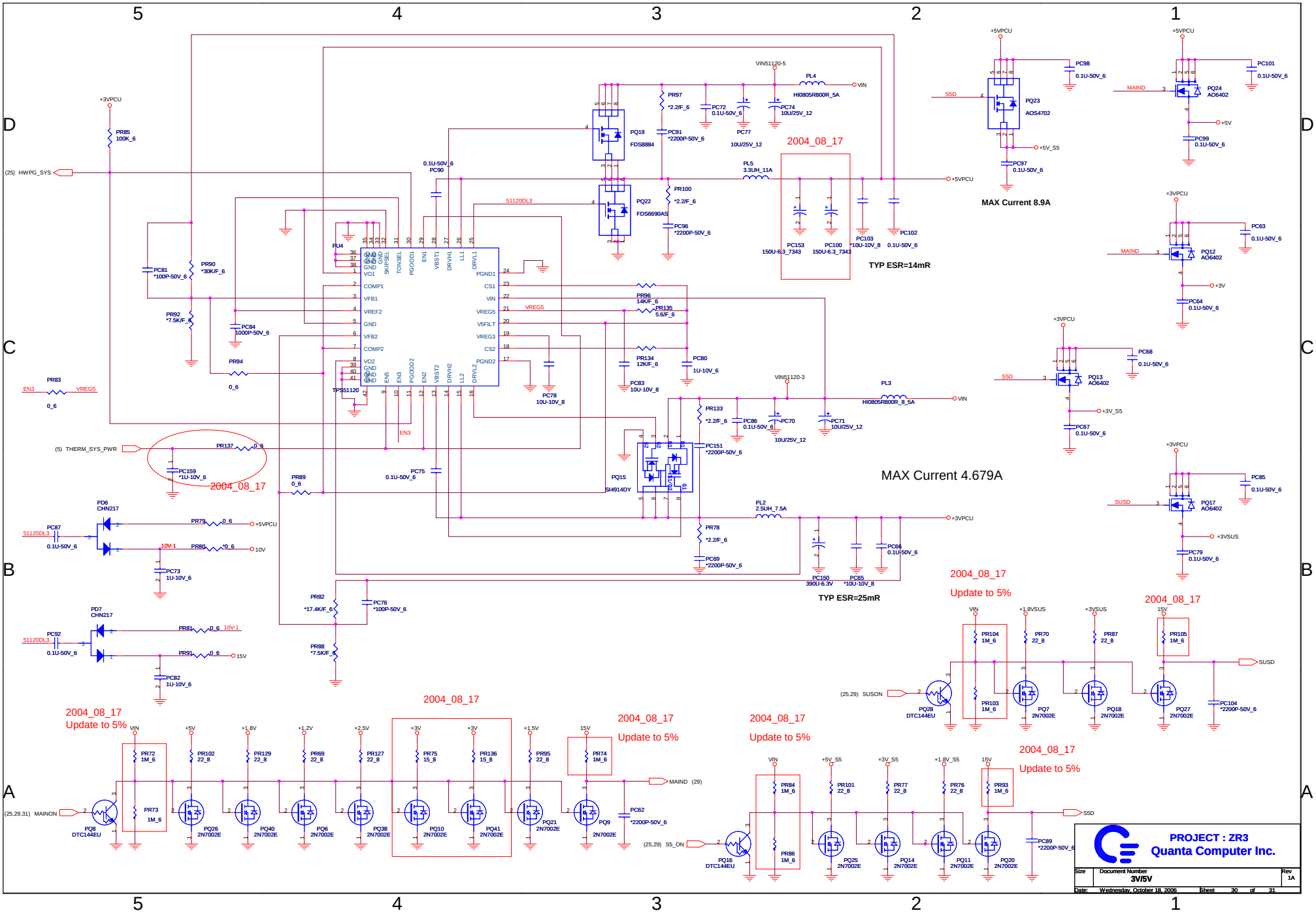
PROJECT :ZR3
Quanta Computer Inc.

Size	Document Number	Rev
C	BATTERY CHARGER	1A

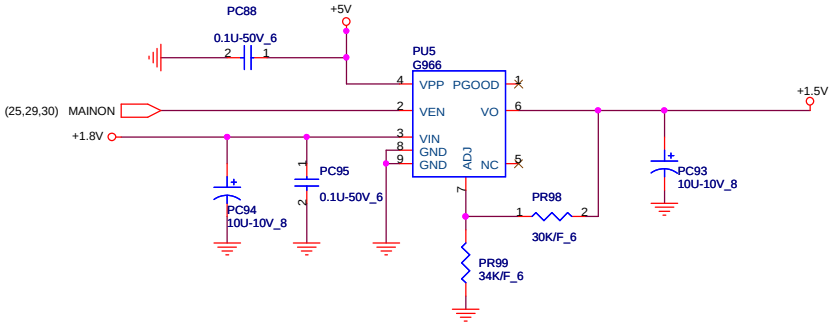
Date: Monday, October 23, 2006 Sheet 27 of 31


2004_08_17
Update to 5%
2004_08_17
For EMI
2004_08_17
Update to TOKIN: DC+36Q0M001
MAX Current 31A
MAX8774
PU1
PROJECT : ZR3
Quanta Computer Inc.
Document Number
MAX8774
Rev
1A
Wednesday, October 18, 2006
Sheet 28 of 31


MAX Current 2.25A
2004_08_17
Update to 5%
MAX Current 5.807A
MAX Current 1.323A
Vout =1.25(1+R1/R2)
= 1.25 (1+44K/100K)
= 1.8V
MAX Current 8.256A
PROJECT : ZR3
Quanta Computer Inc.
1.8V/1.2V
Wednesday, October 18, 2006
Sheet 29 of 31

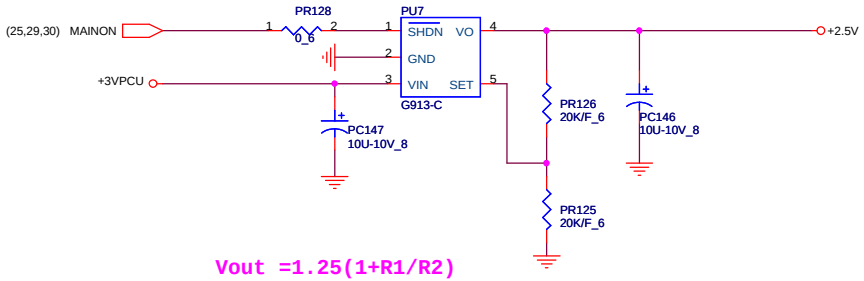

MAX Current 8.9A
TYP ESR=14mR
MAX Current 4.679A
TYP ESR=25mR
2004_08_17
Update to 5%
TPS51120
PROJECT : ZR3
Quanta Computer Inc.
3V/5V

MAX Current 1A



Vout =0.8(R1+R2)/R2
= 0.8(30+34)/34 =
1.5V

MAX Current 0.3A



Vout =1.25(1+R1/R2)
= 1.25 (1+20K/20K)
= 2.5V

PROJECT : ZR3
Quanta Computer Inc.

Size	Document Number	Rev
	+1.5V/+2.5V	1A
Date:	Wednesday, October 18, 2006	Sheet 31 of 31