See 'TEXT' in 0MEMO or 1MEMO property in component

Bolsena-E(AB2) Block Diagram

Project Code: 91.4G401.001
REVISION: 05236-SA

Dummy when use '10/100'
Dummy when use 'GIGA'
Dummy when use 'UMA'
Dummy when use 'DIS'
Dummy when use 'SATA'
Dummy when use 'IDE'

PCB Layer Stackup
L1: Signal 1
L2:VCC
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

Power Block Diag -> Page 40

AMD CPU 35W/25W 4,5,6,7
DDR 333/400
200-PIN DDR SODIMM
DDR x2 8,9,10
HyperTransport 6.4GB/S 16b/8b
ATI RS482M
AGTL+ CPU I/F + UMA 11,12,13,14
PCI Express x16
ATI M52P 49,50,51,52,53
VRAM x4 54,55
LVDS
tv 16
LCD 16
RGB CRT
CRT 15
PCI-Express x2
ATI SB450
PCI
ACPI 2.0
6xUSB 2.0
AZALIA
LPC I/F
ATA 133 17,18,19,20,21
CLK GEN IDT CV137 3
LEDs 16
RTC BAT. 17
BUTTONs 33
PWR SW CP2211 26
PCMCIA SLOT Support TypeII 26
PCMCIA I/F
ENE CB1410
1* Slot Cardbus 25
MS/MS Pro/xD/MMC/SD 5 in 1 28
1394 CONN 28
RICOH R5C832 1394 CardReader 27,28
Mini-PCI 802.11a/b/g 29
PCI Bus / 33MHz
RJ45 31
TXFM 31
TXFM 31
1000Mb
10/100Mb
PCI LAN Realtek RTL8110SBL 1000/100/10 RTL8100C 100/10 30
USB x 4 24
BlueTooth miniUSB 23
CODEC ALC883 32
Line In MIC In 3
AZALIA
MODEM MDC Card 23
RJ11 CONN 31
OP AMP G1421 33
Line Out 33
Int. SPKR 33
LPC Bus / 33MHz
NS SIO PC87381 37
FIR TFDU6102 37
Thermal & Fan G792 23
KBC KB3910 34
XBUS
Touch Pad 35
Int. KB 35
ISA ROM 36
SATA 24
PIDE
HDD 24
SIDE
DVD/CD-RW 24

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Bolsena-E | Rev: SA
Date: Thursday, October 13, 2005 | Sheet 1 of 58

PCI Routing

	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	17	G (1394)	3
7411	17	E (FlashMedia)	3

```
Ref.  function    schematic         BOM
-------------------------
U81  cpu socket    62.10055.121  (DON'T CHANGE)  (3mm high)
U80  north bridge  71.RS482.M03  71.RS482.M03  (ver A12)
U43  south bridge  71.SB400.B0U  71.SB400.D0U  (ver A13)
U32  clock gen.    71.00137.C0W  71.00137.C0W

---
U70  VGA M52     71.0M52P.A0U
U64  VRAM FOR M52
U65  VRAM FOR M52
U69  VRAM FOR M52
U71  VRAM FOR M52




---
U66  BIOS SOCKET  72.39040.G03  62.10002.032   (NO NEED WHEN PD)
U66  BIOS IC      72.39040.G03  72.39040.H03  (DIP STAGE IN LAB, SMT IN PD)
---
U75 GIGA LAN    71.08110.00G 71.08110.A0G
U75 10/100 LAN  71.08110.00G 71.08100.C0G
```

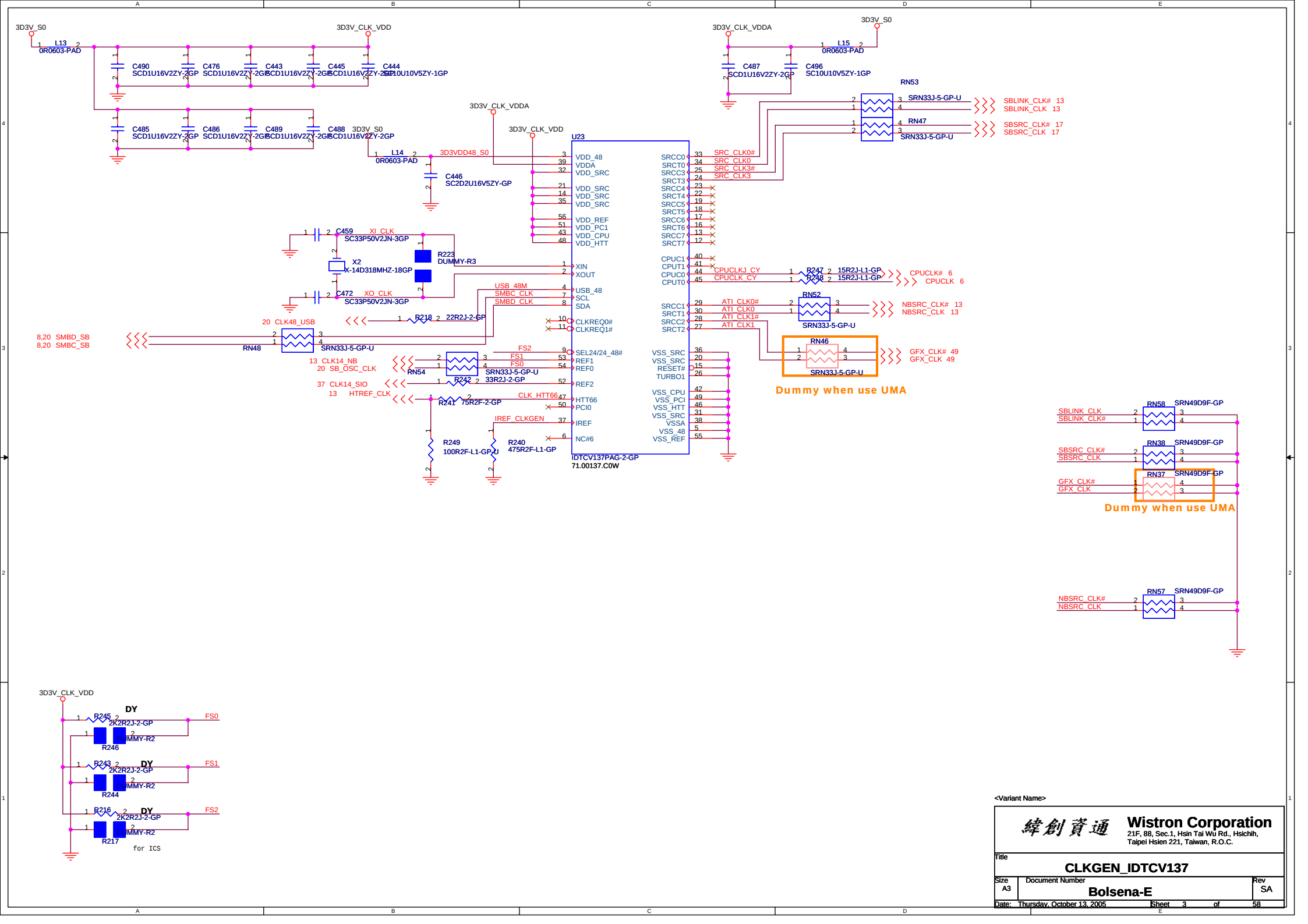
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HISTORY**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 2 of 58



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

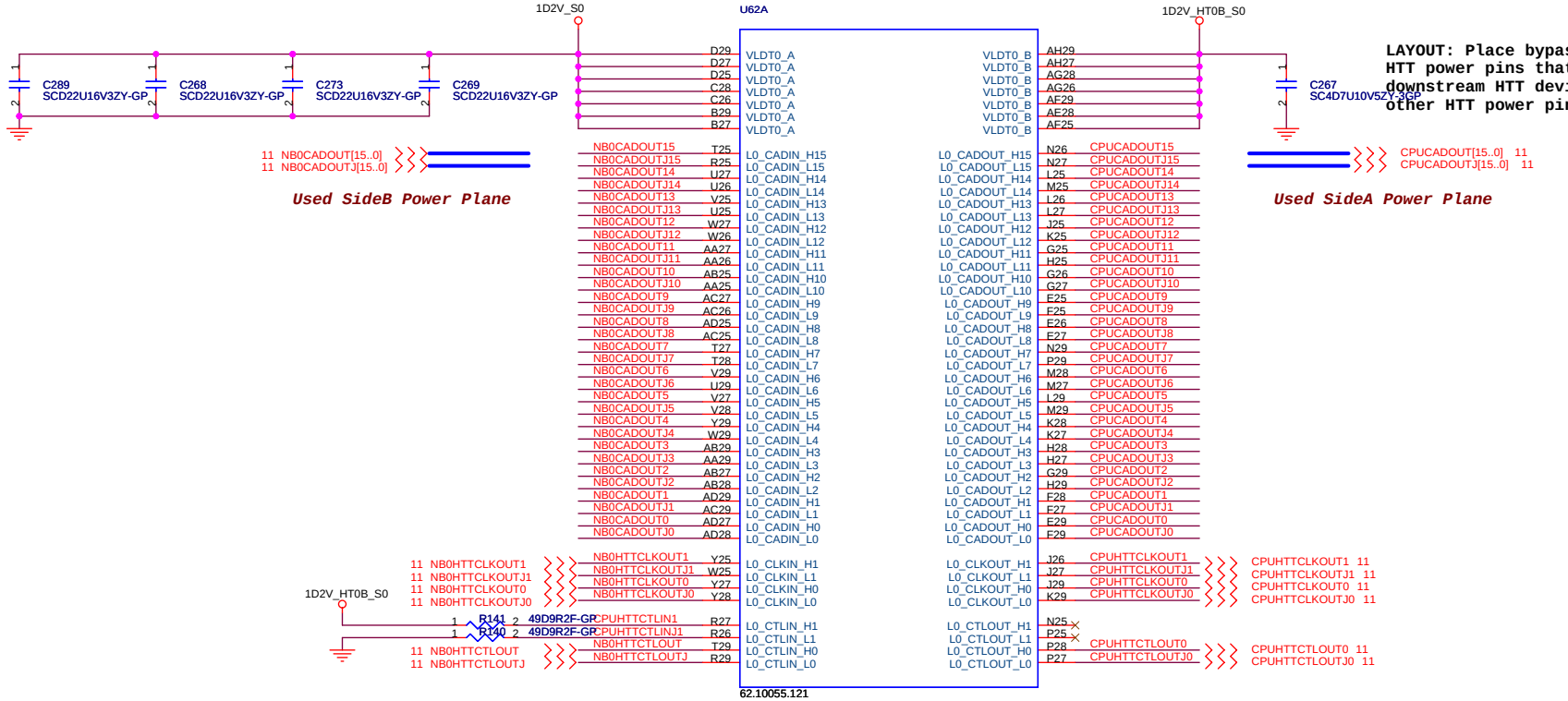
Title: CLKGEN_IDTCV137

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 3 of 58

HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power



LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

ME : 62.10055.121
2nd:62.10055.101

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(1/4)_HyperTransport I/F**

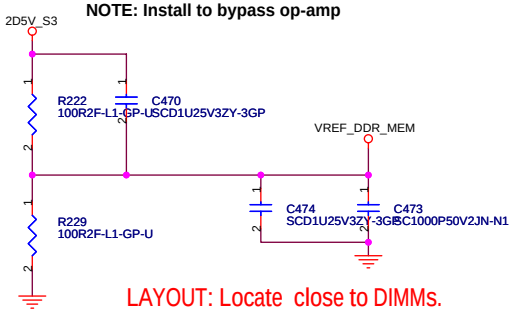
Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 4 of 58

VREF_DDR_MEM

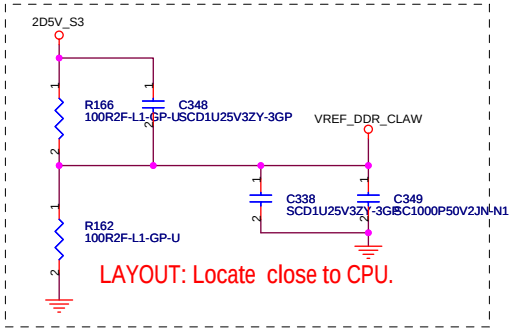
NOTE: Test with passive probes only.

NOTE: Install to bypass op-amp

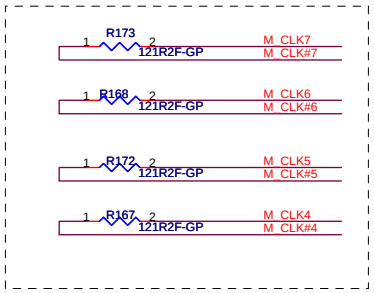


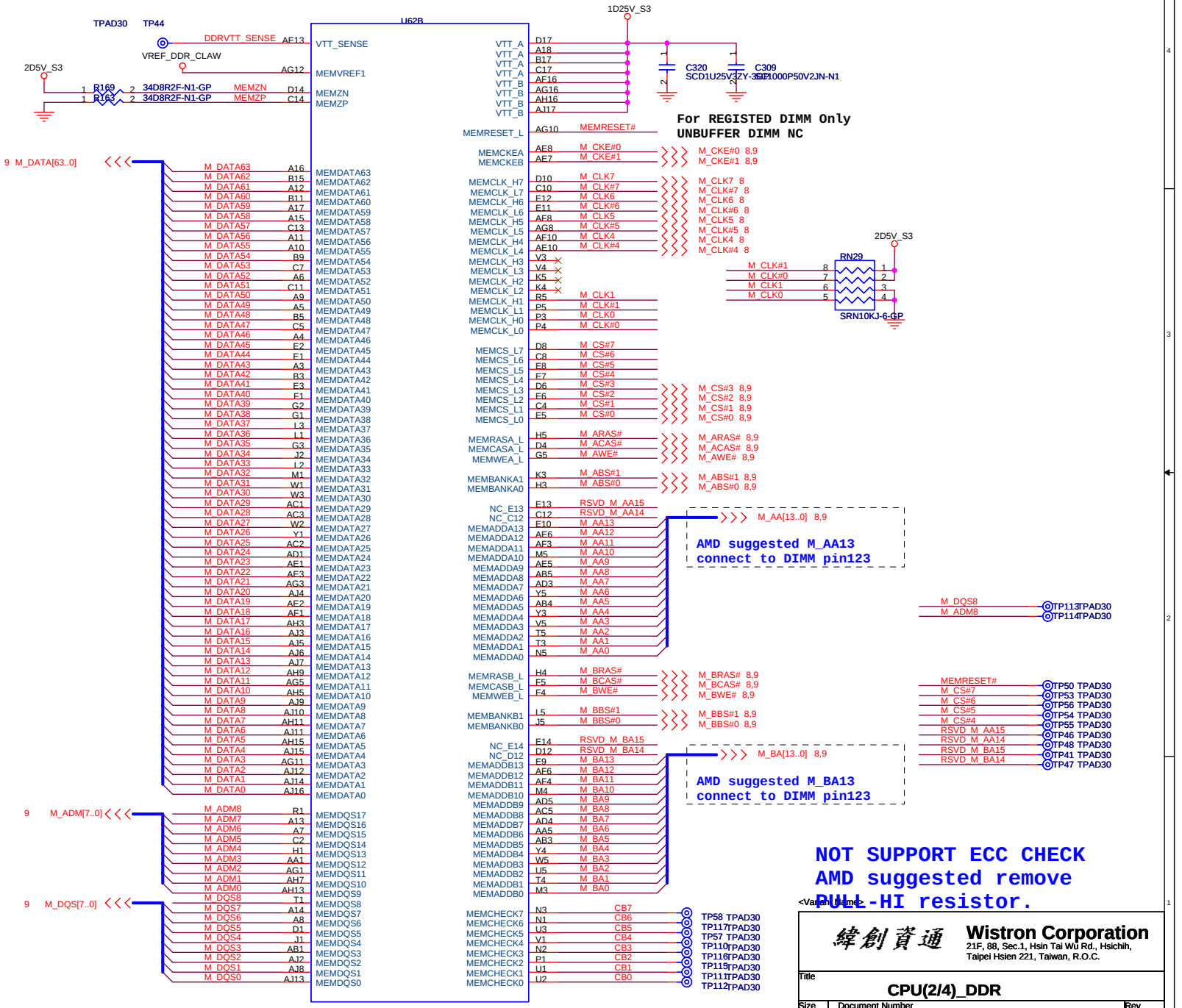
NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



Place it near CPU





緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU(2/4)_DDR**	
Size A3	Document Number **Bolsena-E**	Rev SA
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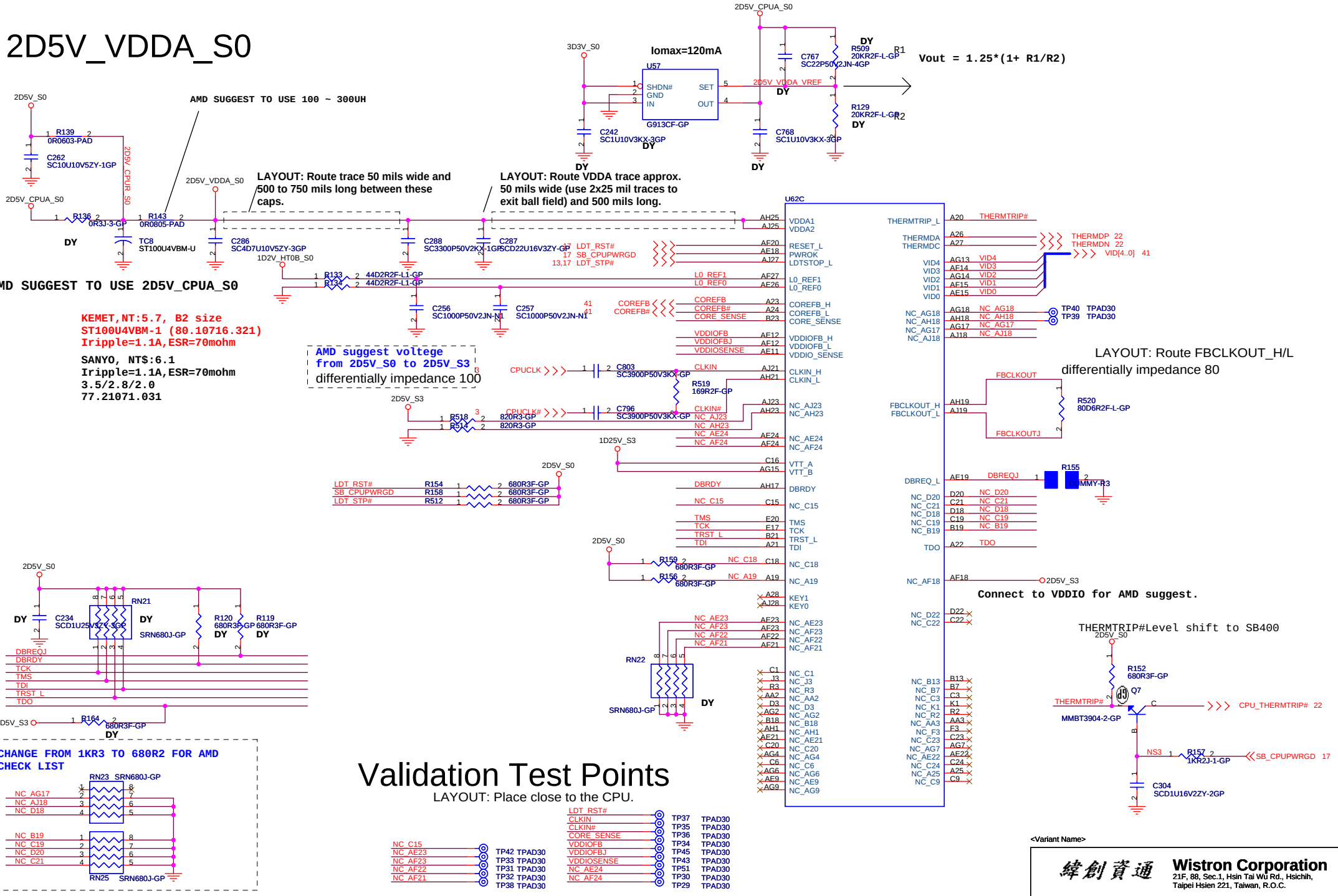
2D5V_VDDA_S0



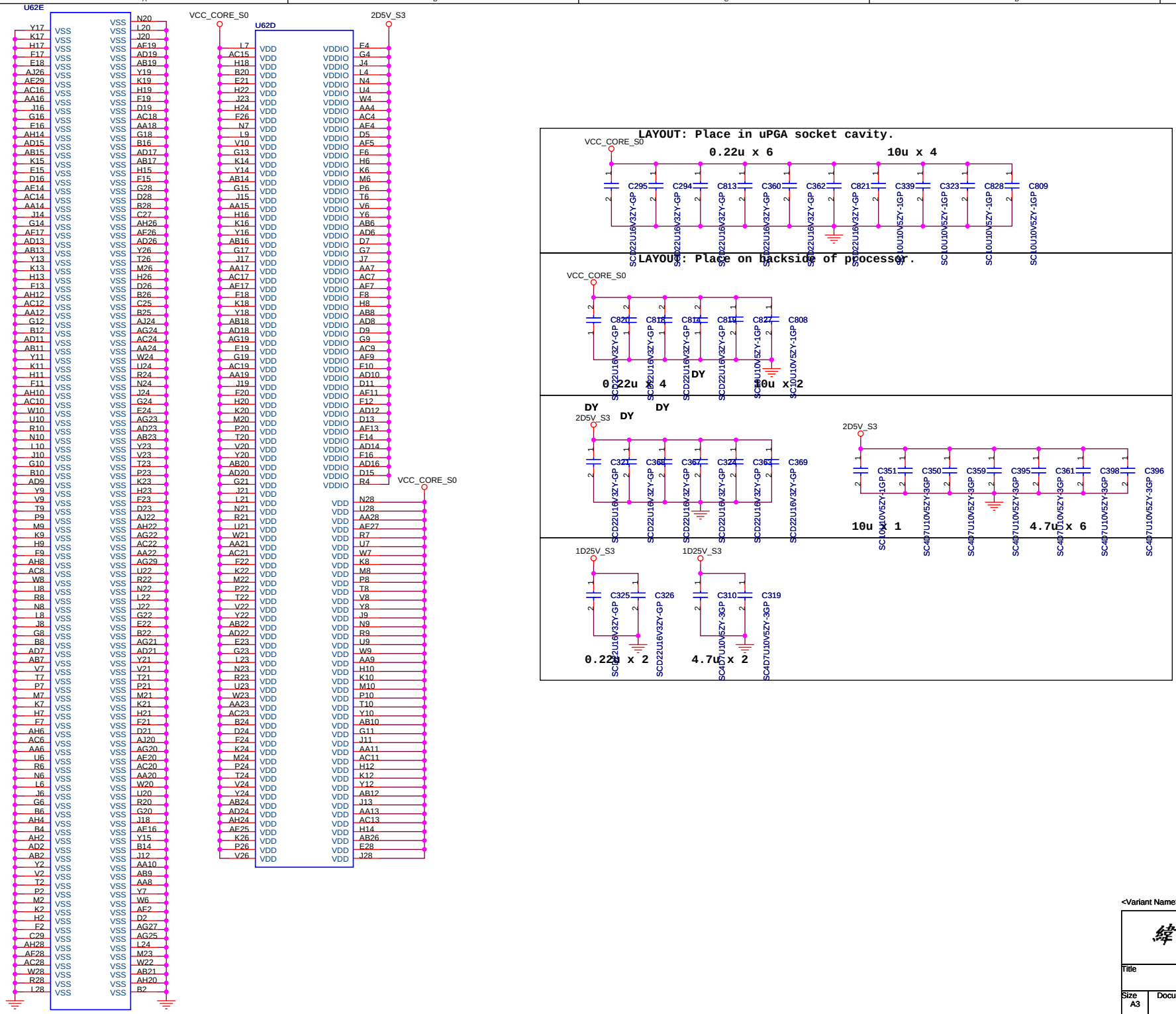
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(3/4)_Control & Debug**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 6 of 58



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4)_Power**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

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DDR1

REVERSE TYPE 5.2MM

M_AA0 M_AA1 M_AA2 M_AA3 M_AA4 M_AA5 M_AA6 M_AA7 M_AA8 M_AA9 M_AA10 M_AA11 M_AA12

M_ABS#0 M_ABS#1

M_DATA_R_0 … M_DATA_R_63

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 / AP A11 A12

BA0 BA1

DQ0 … DQ63

CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7

NC#85 NC#86/(RESET#) NC#97/A13 NC#98/BA2 NC#123 NC#124 NC#200

M_AA13

/RAS /CAS /WE

M_ARAS# M_ACAS# M_AWE#

VREF_DDR_MEM

VREF VREF VDDSPD VDDID

Layout trace 20 mil

C493 SCD1U25V3ZY-3GP

C492 SCD1U25V3ZY-3GP

3D3V_S0

TP59 TPAD30

GND

/CS0 /CS1

M_CS#0 5,9

M_CS#1 5,9

CKE0 CKE1

M_CKE#0

M_CKE#0 5,9

DQS0 … DQS8

M_DQS_R0 … M_DQS_R7

DM0 … DM8

M_ADM_R0 … M_ADM_R7

M_ADM#0
M_ADM#1
M_ADM#2
M_ADM#3
M_ADM#4
M_ADM#5
M_ADM#6
M_ADM#7

CK0 /CK0 CK1 /CK1 CK2 /CK2

M_CLK5 5
M_CLK#5 5
M_CLK7 5
M_CLK#7 5

DDR_CLK0
DDR_CLK#0

SCL SDA

SMBC_SB
SMBD_SB

SA0 SA1 SA2

VDD

2D5V_S3

VSS

NOT SUPPORT ECC CHECK
AMD suggested pull-low

1ST 62.10017.701 - 2ND 62.10017.201

Part Number = 62.10017.701

SKT-SODIMM200-24GP

ME : 62.10017.701
2nd :62.10017.691

DDR2

REVERSE TYPE 9.2MM

M_BA0 M_BA1 M_BA2 M_BA3 M_BA4 M_BA5 M_BA6 M_BA7 M_BA8 M_BA9 M_BA10 M_BA11 M_BA12

M_BBS#0 M_BBS#1

M_DATA_R_0 … M_DATA_R_63

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 / AP A11 A12

BA0 BA1

DQ0 … DQ63

CB0 CB1 CB2 CB3 CB4 CB5 CB6 CB7

NC#85 NC#86/(RESET#) NC#97/A13 NC#98/BA2 NC#123 NC#124 NC#200

M_BA13

/RAS /CAS /WE

M_BRAS# M_BCAS# M_BWE#

VREF_DDR_MEM

VREF VREF VDDSPD VDDID

Layout trace 20 mil

C515 SCD1U25V3ZY-3GP

C516 SCD1U25V3ZY-3GP

3D3V_S0

TP60 TPAD30

GND

/CS0 /CS1

M_CS#2 5,9

M_CS#3 5,9

CKE0 CKE1

M_CKE#1 5,9

! NOT THIS LIBRARY

DQS0 … DQS8

M_DQS_R0 … M_DQS_R7

DM0 … DM8

M_ADM_R0 … M_ADM_R7

M_ADM#0
M_ADM#1
M_ADM#2
M_ADM#3
M_ADM#4
M_ADM#5
M_ADM#6
M_ADM#7

CK0 /CK0 CK1 /CK1 CK2 /CK2

M_CLK4 5
M_CLK#4 5
M_CLK6 5
M_CLK#6 5

DDR_CLK1
DDR_CLK#1

SCL SDA

SMBC_SB 3,20
SMBD_SB 3,20

SA0 SA1 SA2

DM_SA0 — R255 4K7R2J-2-GP — 3D3V_S0

VDD

2D5V_S3

VSS

62.10017.391

ME : 62.10017.391

SKT-SODIMM2006U1GP

M_ADM_R[7..0] 9

M_DATA_R_[63..0] 9

M_DQS_R[7..0] 9

M_AA[13..0] 5,9

M_ABS#[1..0] 5,9

M_BA[13..0] 5,9

M_BBS#[1..0] 5,9

RN62

DDR_CLK#1 8 1
DDR_CLK#0 7 2
DDR_CLK1 6 3
DDR_CLK0 5 4

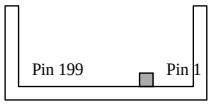
2D5V_S3

SRN10KJ-6-GP

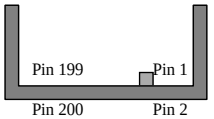
AMD CPU

MD63 SMA11 SMA10 SMA0 SMA14 SMA12 MD0

DDR1(Reverse 5.2mm)



DDR2(Reverse 9.2mm)



(Bottom view)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR SO-DIMM SKT

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 8 of 58

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

SRN10J-3

M_DATA4	8	9	M_DATA_R_4
M_DATA5	7	10	M_DATA_R_5
M_ADM0	6	11	M_ADM_R0
M_DATA6	5	12	M_DATA_R_6
M_DATA7	4	13	M_DATA_R_7
M_DATA13	3	14	M_DATA_R_13
M_DATA12	2	15	M_DATA_R_12
M_ADM1	1	16	M_ADM_R1

RN40

SRN10J-3

M_DATA1	8	9	M_DATA_R_1
M_DATA0	7	10	M_DATA_R_0
M_DQS0	6	11	M_DQS_R0
M_DATA2	5	12	M_DATA_R_2
M_DATA3	4	13	M_DATA_R_3
M_DATA8	3	14	M_DATA_R_8
M_DATA9	2	15	M_DATA_R_9
M_DQS1	1	16	M_DQS_R1

RN31

SRN10J-3

M_DATA14	8	9	M_DATA_R_14
M_DATA15	7	10	M_DATA_R_15
M_DATA21	6	11	M_DATA_R_21
M_DATA20	5	12	M_DATA_R_20
M_ADM2	4	13	M_ADM_R2
M_DATA23	3	14	M_DATA_R_23
M_DATA22	2	15	M_DATA_R_22
M_DATA28	1	16	M_DATA_R_28

RN41

SRN10J-3

M_DATA11	8	9	M_DATA_R_11
M_DATA10	7	10	M_DATA_R_10
M_DATA17	6	11	M_DATA_R_17
M_DATA16	5	12	M_DATA_R_16
M_DQS2	4	13	M_DQS_R2
M_DATA19	3	14	M_DATA_R_19
M_DATA18	2	15	M_DATA_R_18
M_DATA25	1	16	M_DATA_R_25

RN32

RN42 SRN10J-5-GP

M_DATA29	4	5	M_DATA_R_29
M_ADM3	3	6	M_ADM_R3
M_DATA31	2	7	M_DATA_R_31
M_DATA30	1	8	M_DATA_R_30
M_DATA24	4	5	M_DATA_R_24
M_DQS3	3	6	M_DQS_R3
M_DATA26	2	7	M_DATA_R_26
M_DATA27	1	8	M_DATA_R_27

RN33 SRN10J-5-GP

RN43 SRN10J-5-GP

M_DATA37	4	5	M_DATA_R_37
M_DATA36	3	6	M_DATA_R_36
M_ADM4	2	7	M_ADM_R4
M_DATA39	1	8	M_DATA_R_39

RN34 SRN10J-5-GP

M_DATA32	4	5	M_DATA_R_32
M_DATA33	3	6	M_DATA_R_33
M_DQS4	2	7	M_DQS_R4
M_DATA34	1	8	M_DATA_R_34

SRN10J-3

M_DATA35	8	9	M_DATA_R_35
M_DATA41	7	10	M_DATA_R_41
M_DATA40	6	11	M_DATA_R_40
M_DQS5	5	12	M_DQS_R5
M_DATA42	4	13	M_DATA_R_42
M_DATA43	3	14	M_DATA_R_43
M_DATA49	2	15	M_DATA_R_49
M_DATA48	1	16	M_DATA_R_48

RN35

SRN10J-3

M_DATA38	8	9	M_DATA_R_38
M_DATA45	7	10	M_DATA_R_45
M_DATA44	6	11	M_DATA_R_44
M_ADM5	5	12	M_ADM_R5
M_DATA47	4	13	M_DATA_R_47
M_DATA46	3	14	M_DATA_R_46
M_DATA53	2	15	M_DATA_R_53
M_DATA52	1	16	M_DATA_R_52

RN44

SRN10J-3

M_DQS6	8	9	M_DQS_R6
M_DATA50	7	10	M_DATA_R_50
M_DATA51	6	11	M_DATA_R_51
M_DATA56	5	12	M_DATA_R_56
M_DATA57	4	13	M_DATA_R_57
M_DQS7	3	14	M_DQS_R7
M_DATA58	2	15	M_DATA_R_58
M_DATA59	1	16	M_DATA_R_59

RN36

SRN10J-3

M_ADM6	8	9	M_ADM_R6
M_DATA54	7	10	M_DATA_R_54
M_DATA55	6	11	M_DATA_R_55
M_DATA61	5	12	M_DATA_R_61
M_DATA60	4	13	M_DATA_R_60
M_ADM7	3	14	M_ADM_R7
M_DATA62	2	15	M_DATA_R_62
M_DATA63	1	16	M_DATA_R_63

RN45

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

SRN68J-4-GP

M_ADM_R1	8	9	4
M_DATA_R_13	7	10	3
M_DATA_R_12	6	11	2
M_DATA_R_7	5	12	1
M_DATA_R_6	4	13	
M_ADM_R0	3	14	
M_DATA_R_5	2	15	
M_DATA_R_4	1	16	

RN113

5	M_DATA_R_32		
6	M_DATA_R_33		
7	M_DQS_R4		
8	M_DATA_R_35		

RN56 SRN68J-3-GP

4	5	M_DATA_R_36	
3	6	M_DATA_R_37	
2	7	M_ADM_R4	
1	8	M_DATA_R_38	

RN116 SRN68J-3-GP

SRN68J-4-GP

M_DATA_R_1	8	9	M_DATA_R_48
M_DATA_R_0	7	10	M_DATA_R_49
M_DQS_R0	6	11	M_DATA_R_43
M_DATA_R_2	5	12	M_DATA_R_42
M_DATA_R_3	4	13	M_DQS_R5
M_DATA_R_8	3	14	M_DATA_R_41
M_DATA_R_9	2	15	M_DATA_R_40
M_DQS_R1	1	16	M_DATA_R_34

RN59

SRN68J-4-GP

M_DATA_R_28	8	9	M_DATA_R_39
M_DATA_R_23	7	10	M_DATA_R_44
M_DATA_R_22	6	11	M_DATA_R_45
M_ADM_R2	5	12	M_ADM_R5
M_DATA_R_21	4	13	M_DATA_R_46
M_DATA_R_20	3	14	M_DATA_R_47
M_DATA_R_15	2	15	M_DATA_R_52
M_DATA_R_14	1	16	M_DATA_R_53

RN114

SRN68J-4-GP

M_DATA_R_11	8	9	M_DATA_R_59
M_DATA_R_10	7	10	M_DATA_R_58
M_DATA_R_16	6	11	M_DQS_R7
M_DATA_R_17	5	12	M_DATA_R_57
M_DQS_R2	4	13	M_DATA_R_56
M_DATA_R_19	3	14	M_DATA_R_51
M_DATA_R_18	2	15	M_DATA_R_50
M_DATA_R_24	1	16	M_DQS_R6

RN60

RN61 SRN68J-3-GP

M_DATA_R_27	1	8	
M_DATA_R_26	2	7	
M_DQS_R3	3	6	
M_DATA_R_25	4	5	

M_DATA_R_31	4	5	
M_DATA_R_30	3	6	
M_ADM_R3	2	7	
M_DATA_R_29	1	8	

RN115 SRN68J-3-GP

SRN68J-4-GP

M_DATA_R_39	9	8	
M_DATA_R_44	10	7	
M_DATA_R_45	11	6	
M_ADM_R5	12	5	
M_DATA_R_46	13	4	
M_DATA_R_47	14	3	
M_DATA_R_52	15	2	
M_DATA_R_53	16	1	

RN66

SRN68J-4-GP

M_DATA_R_59	9	8	
M_DATA_R_58	10	7	
M_DQS_R7	11	6	
M_DATA_R_57	12	5	
M_DATA_R_56	13	4	
M_DATA_R_51	14	3	
M_DATA_R_50	15	2	
M_DQS_R6	16	1	

RN67

SRN68J-4-GP

M_ADM_R6	9	8	
M_DATA_R_54	10	7	
M_DATA_R_55	11	6	
M_DATA_R_60	12	5	
M_DATA_R_61	13	4	
M_ADM_R7	14	3	
M_DATA_R_62	15	2	
M_DATA_R_63	16	1	

RN112

1D25V_S3

SRN47J-7-GP

M_CKE#0	1	4	
M_AA12	2	3	

RN50

SRN47J-7-GP

M_BA12	1	4	
M_BA5	2	3	

RN55

SRN47J-6-GP

M_AA11	8	9	
M_AA9	7	10	
M_AA7	6	11	
M_AA5	5	12	
M_AA4	4	13	
M_AA8	3	14	
M_AA6	2	15	
M_AA3	1	16	

RN63

SRN47J-4-GP

M_CS#3	4	5	
M_BCAS#	3	6	
M_BRAS#	2	7	
M_BBS#1	1	8	

RN109

RN65 SRN47J-7-GP

M_AWE#	1	4	
M_ABS#0	2	3	

RN68

SRN47J-7-GP

M_BA3	1	4	
M_BA7	2	3	

SRN47J-6-GP

M_AA1	8	9	
M_AA10	7	10	
M_AA2	6	11	
M_AA0	5	12	
M_ABS#1	4	13	
M_ARAS#	3	14	
M_CS#2	2	15	
M_BA13	1	16	

RN64

SRN47J-6-GP

M_BA9	8	9	
M_BA6	7	10	
M_BA10	6	11	
M_BA1	5	12	
M_BA2	4	13	
M_BA0	3	14	
M_BBS#0	2	15	
M_BWE#	1	16	

RN69

SRN47J-4-GP

M_BA4	4	5	
M_BA8	3	6	
M_BA11	2	7	
M_CKE#1	1	8	

RN108

SRN47J-4-GP

M_AA13	4	5	
M_CS#0	3	6	
M_CS#1	2	7	
M_ACAS#	1	8	

RN51

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8

M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8

M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8

M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

5,8 M_CKE#0 M_CKE#0
5,8 M_CKE#1 M_CKE#1

<Variant Name>

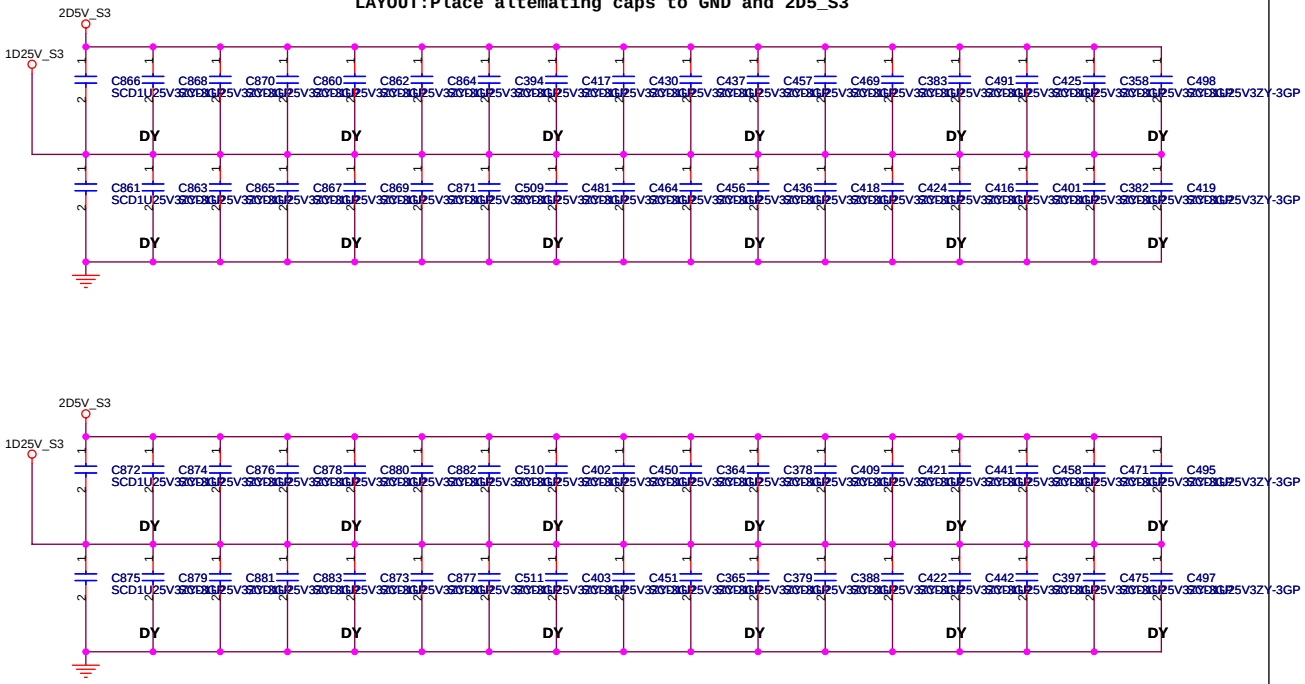
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

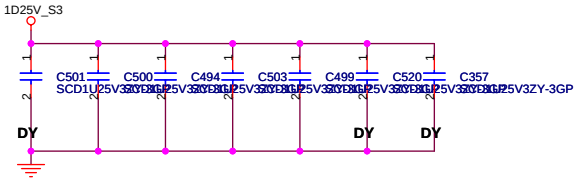
Title: **DDR DAMPING & TERMINATION**

Size	Document Number	Rev
A3	Bolsena-E	SA

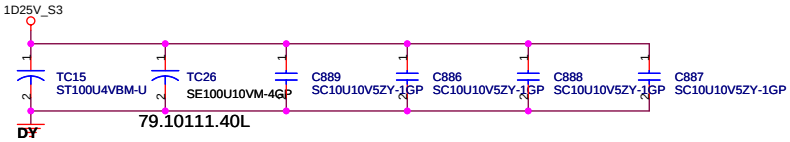
Date: Thursday, October 13, 2005 Sheet 9 of 58

LAYOUT:Place altemating caps to GND and 2D5_S3

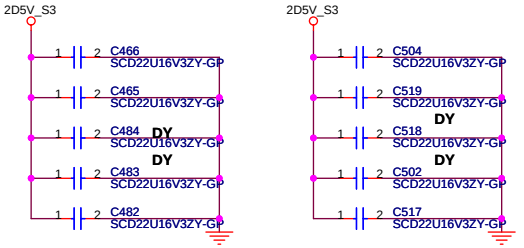




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DECOUPLING**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

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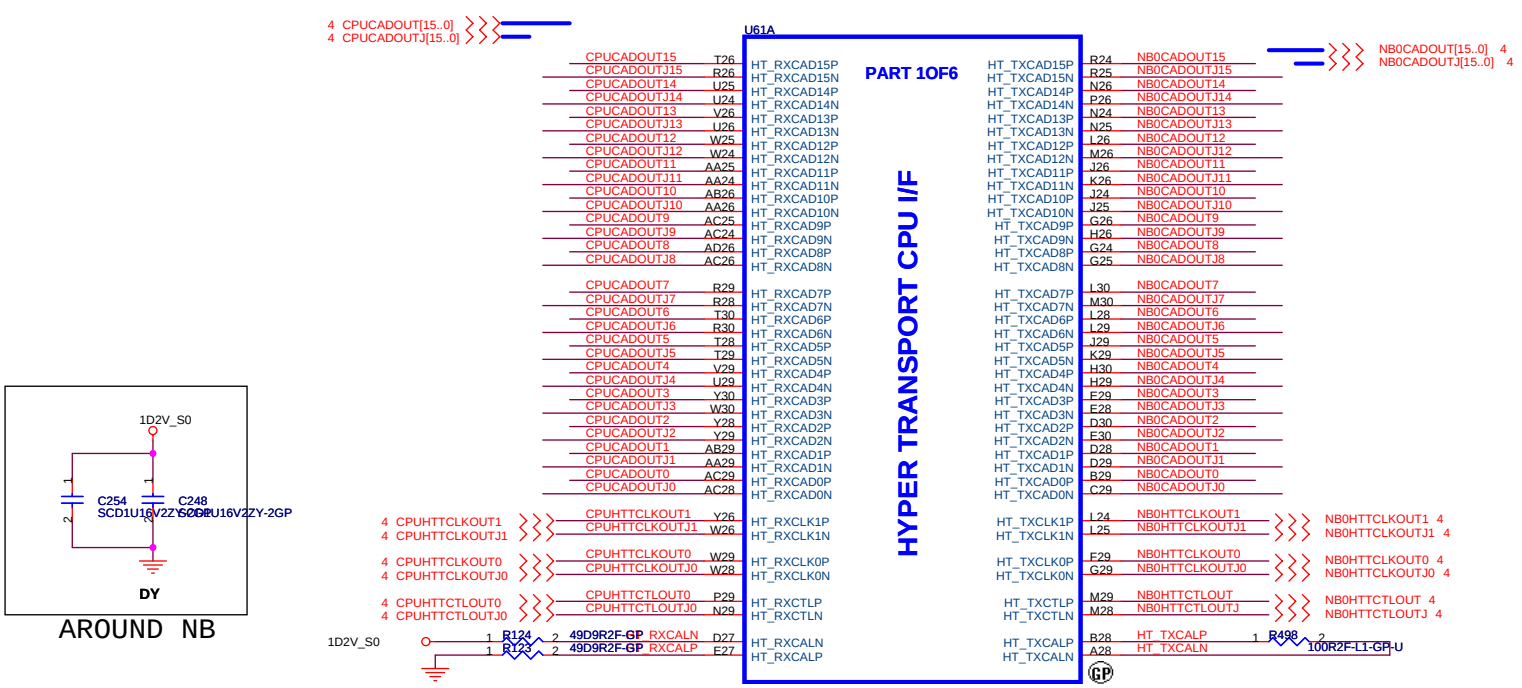
CLAW HAMMER TO NB

NB TO CLAW HAMMER



AROUND NB

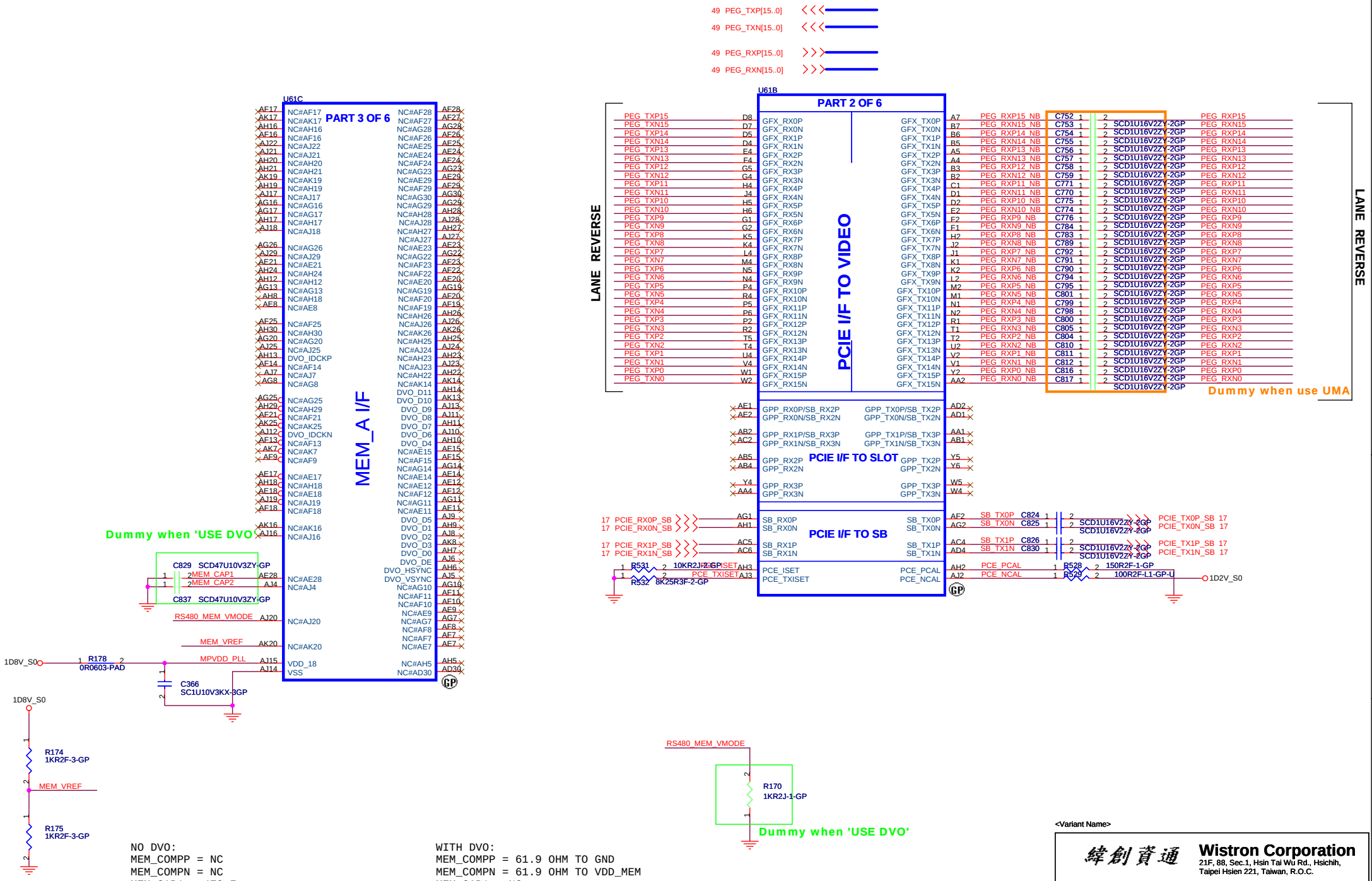
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS482M (1 of 4) HT

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 11 of 58



NO DVO:
MEM_COMPP = NC
MEM_COMPN = NC
MEM_CAP1 = 470nF
MEM_CAP2 = 470nF
MEM_VMODE = GND (IF VDD_MEM = 2.5V)
MEM_VREF = VDD_MEM / 2

WITH DVO:
MEM_COMPP = 61.9 OHM TO GND
MEM_COMPN = 61.9 OHM TO VDD_MEM
MEM_CAP1 = NC
MEM_CAP2 = NC
MEM_VMODE = 1.8V(IF VDD_MEM = 1.8V)
MEM_VREF = VDD_MEM / 2

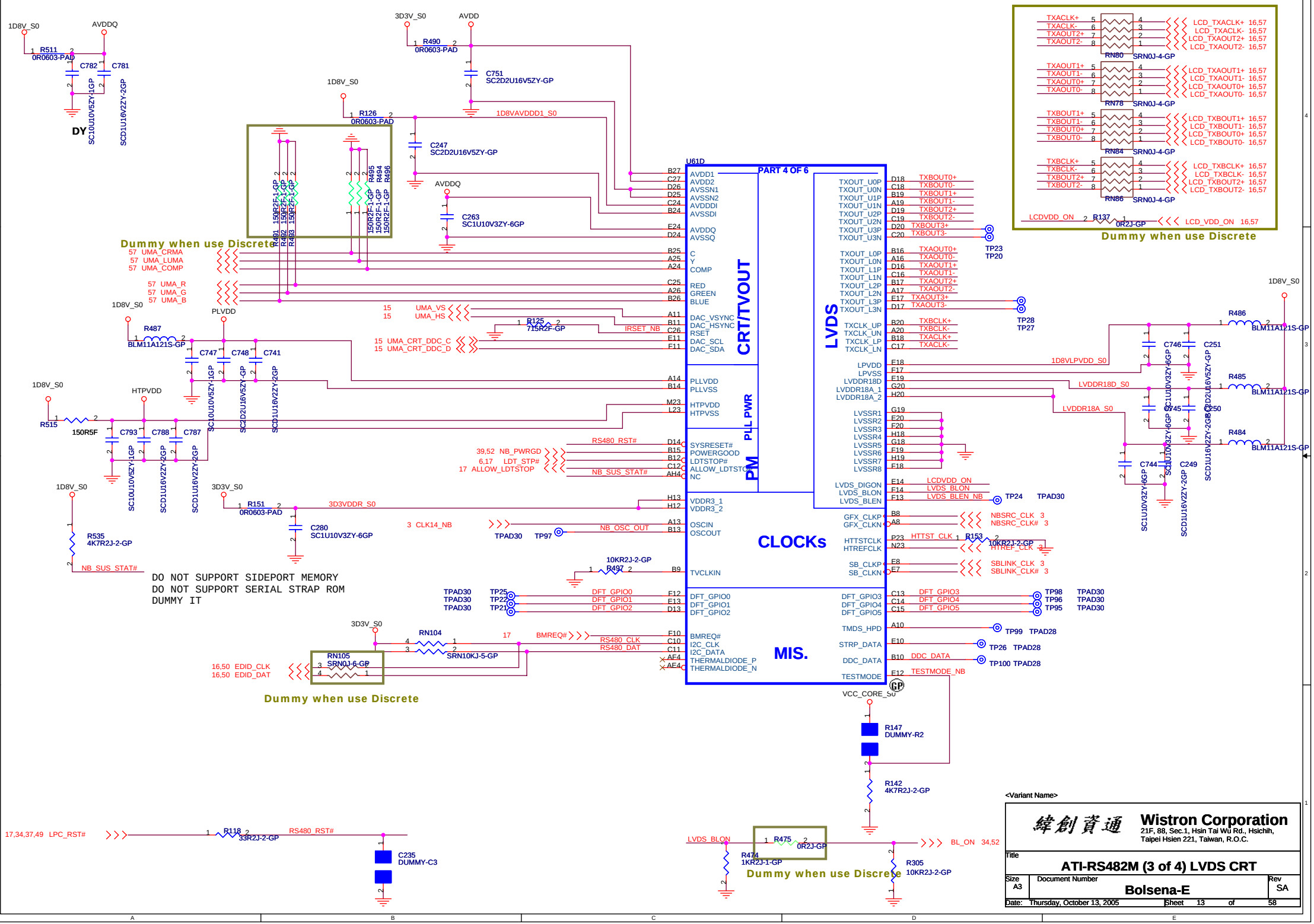
<Variant Name>

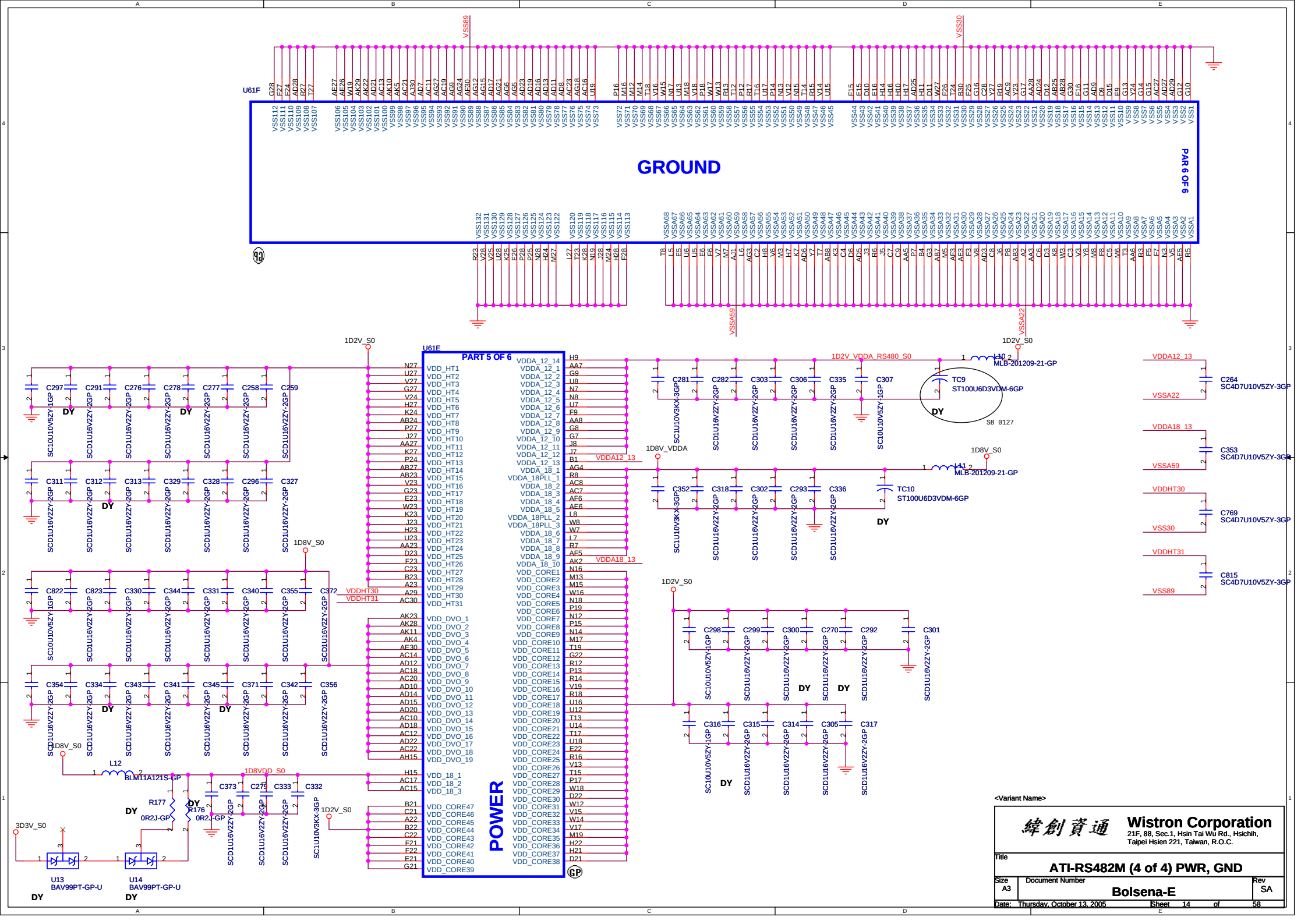
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS482M (2 of 4) PCIE**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 12 of 58


U61D
PART 4 OF 6
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C
Y
COMP
RED
GREEN
BLUE
DAC_VSYNC
DAC_HSYNC
RSET
DAC_SCL
DAC_SDA
PLLVDD
PLLVSS
HTPVDD
HTPVSS
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
NC
VDDR3_1
VDDR3_2
OSCIN
OSCOUT
TVCLKIN
DFT_GPIO0
DFT_GPIO1
DFT_GPIO2
BMREQ#
I2C_CLK
I2C_DATA
THERMALDIODE_P
THERMALDIODE_N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
LPVDD
LPVSS
LVDDR18D
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
GFX_CLKP
GFX_CLKN
HTTSTCLK
HTREFCLK
SB_CLKP
SB_CLKN
TMDS_HPD
STRP_DATA
DDC_DATA
TESTMODE
Dummy when use Discrete
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
ATI-RS482M (3 of 4) LVDS CRT
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 13 of 58



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS482M (4 of 4) PWR, GND

Size: A3 | Document Number: Bolsena-E | Rev: SA

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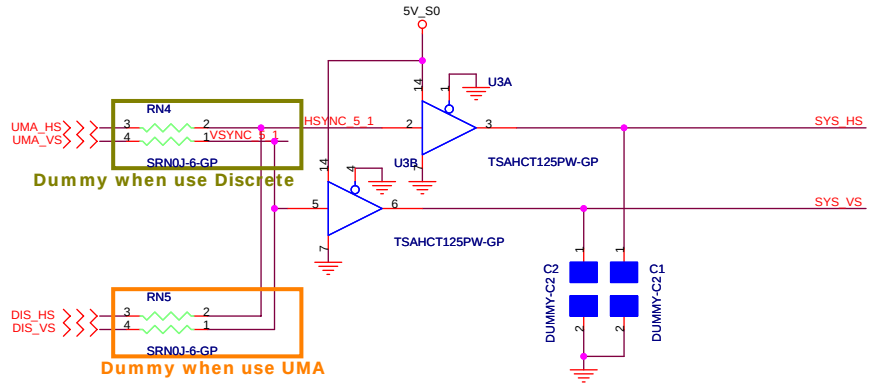
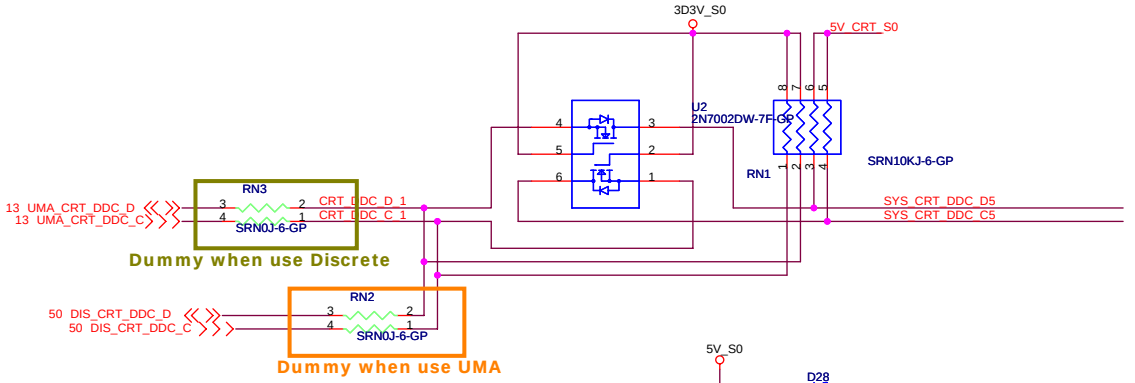
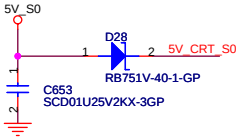
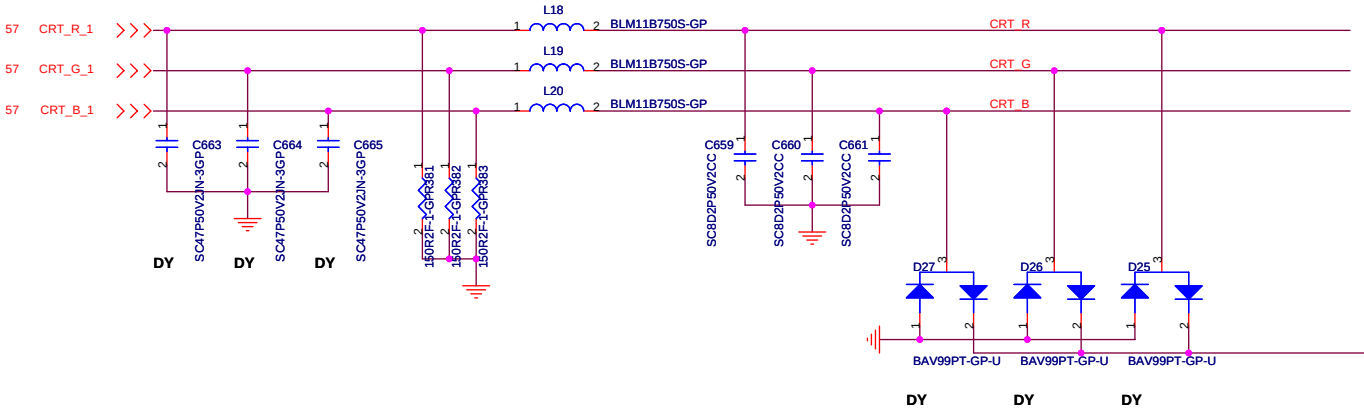
CRT CONN

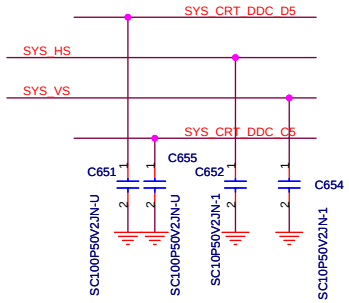
200mA Rating/Spec 500mA

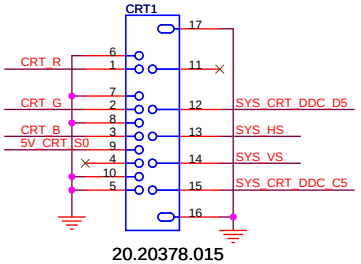


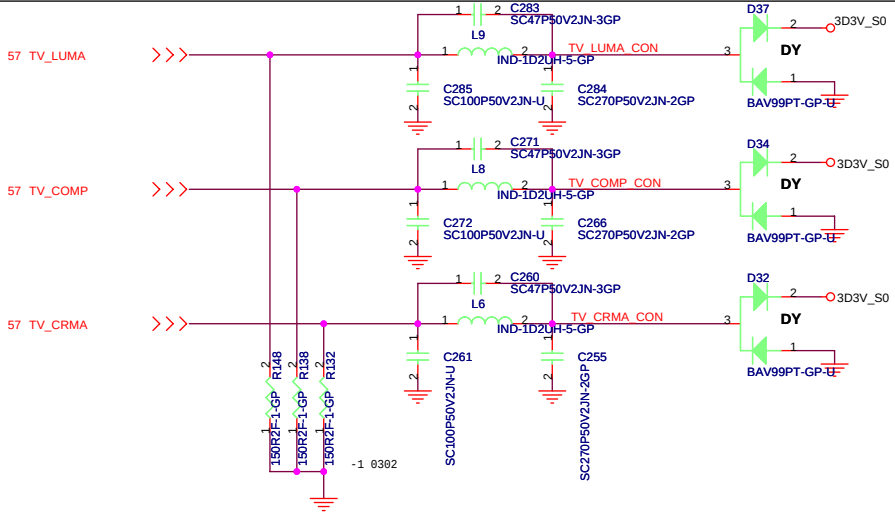


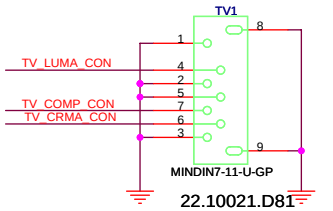




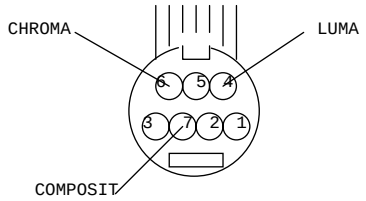








TV CONN

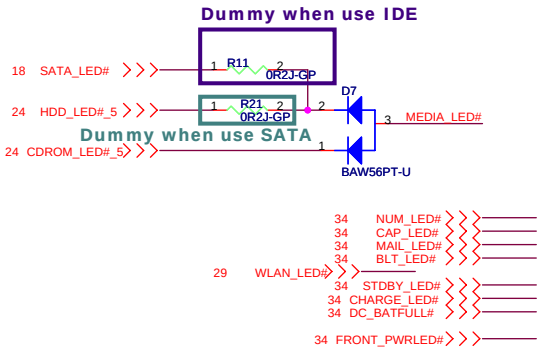


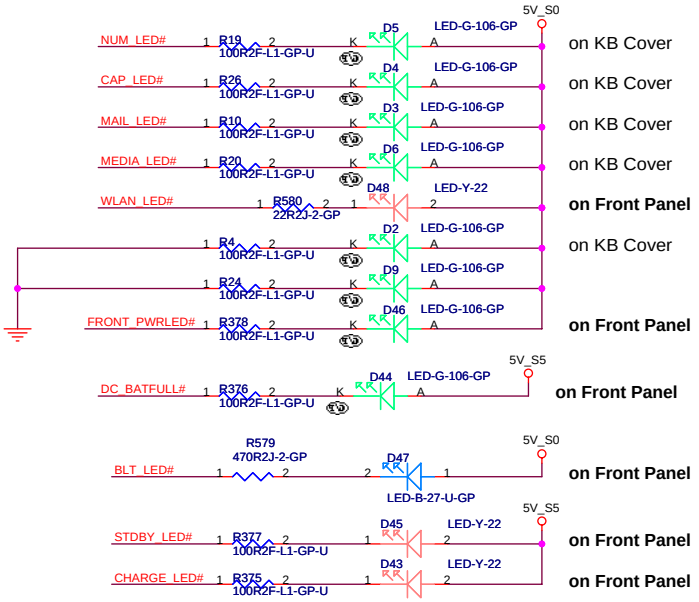
<Variant Name>

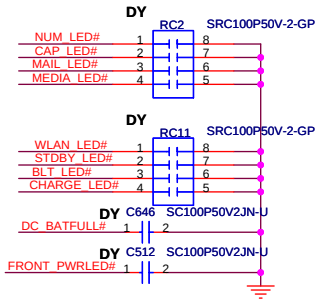
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT/TV		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 15 of 58	

LEDs







on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

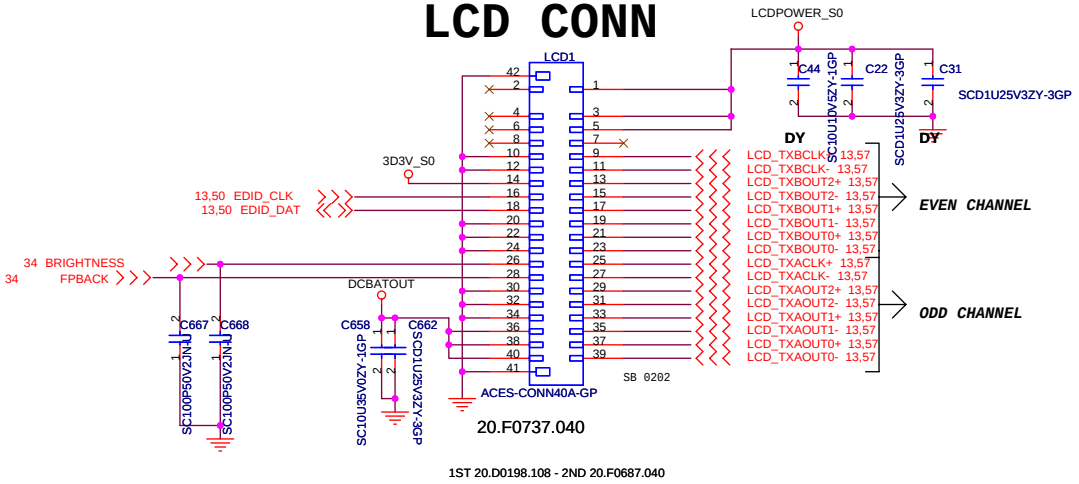
LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

Charger:
Green : DC only with Battery full with DC
Orange : Charging
Orange Blink : Battery low

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

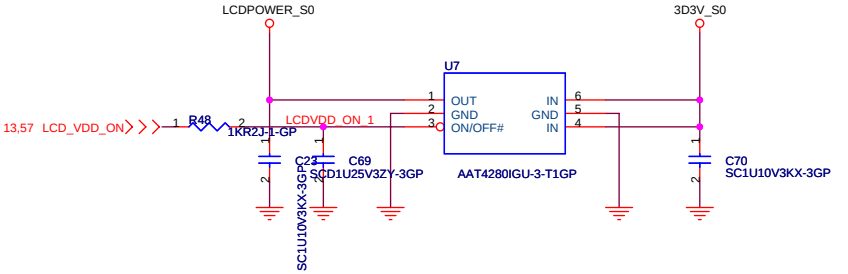
LCD CONN



1ST 20.D0198.108 - 2ND 20.F0687.040

LCD POWER

Layout 40 mil



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD / LEDs**

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A3	**Bolsena-E**	SA

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MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS

32K suspend clock output

PCIRST# 3V to 5V level shift for HDD & CDROM

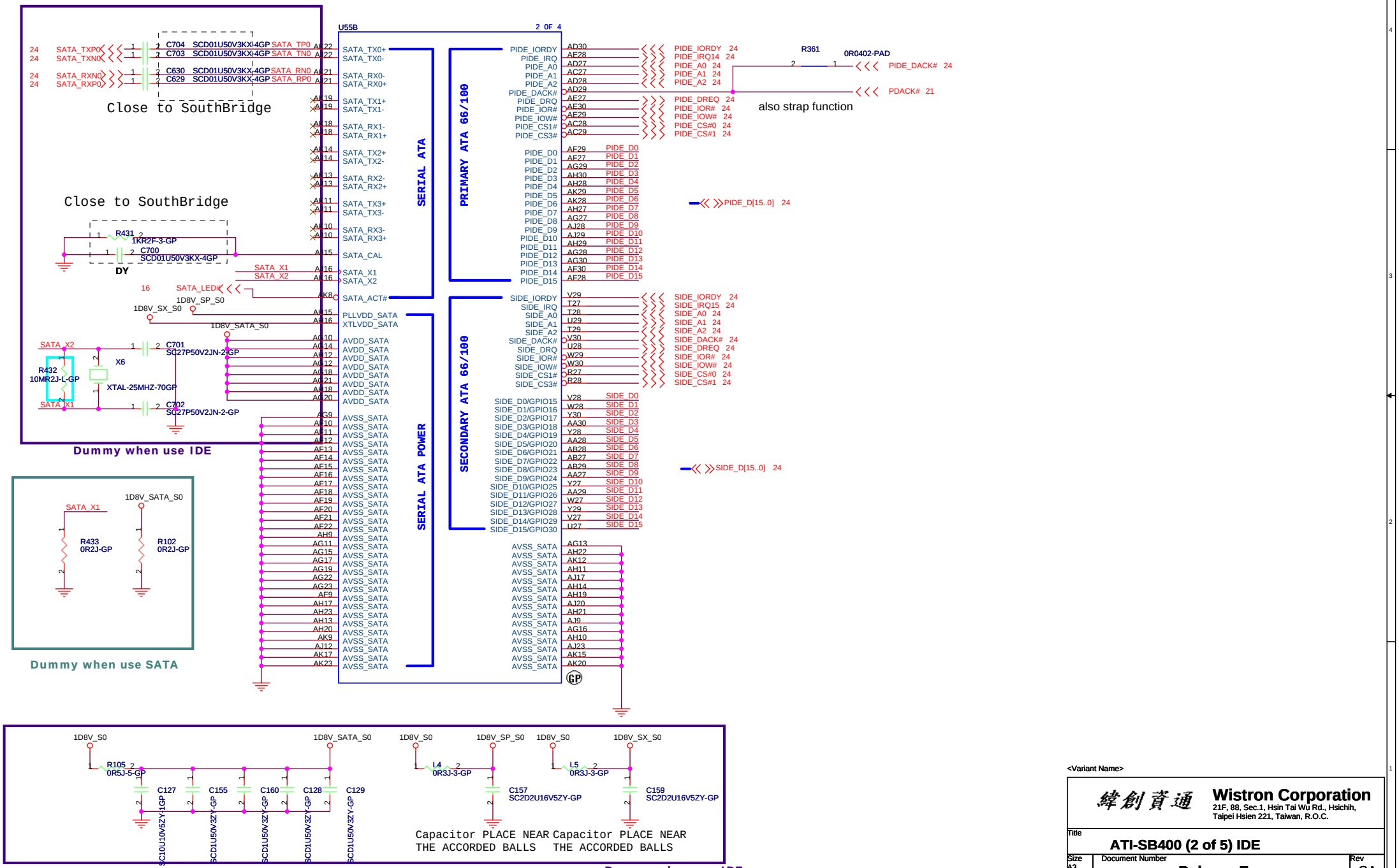
SB400 asserts PLTRST# to reset devices on the platform.

Secondary PCI Bus reset signal.

Close to chip

PCB-Ver

Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ATI-SB450 (1 of 5) PCI, PCIE	
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 17 of 58	



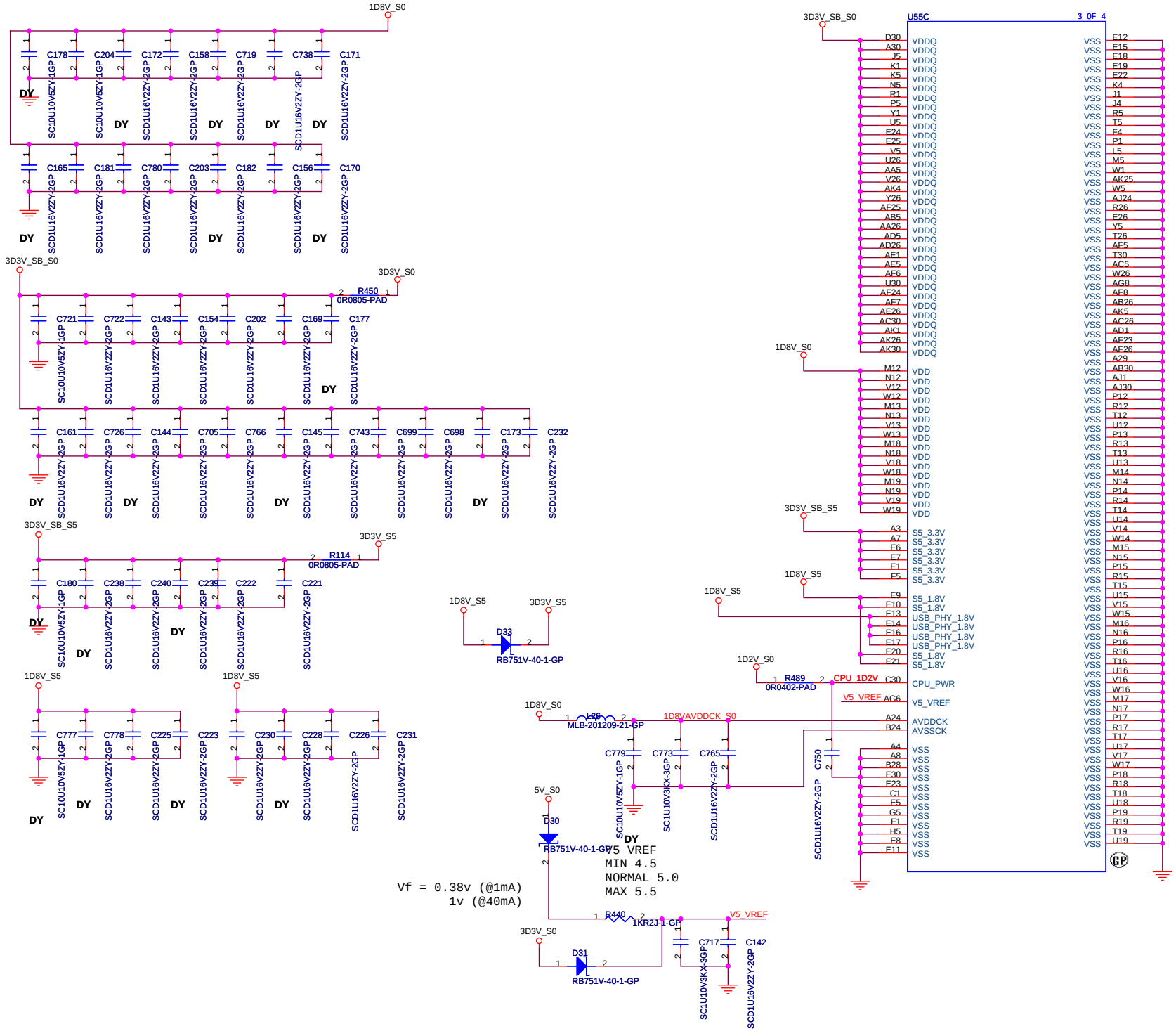
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (2 of 5) IDE

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 18 of 58



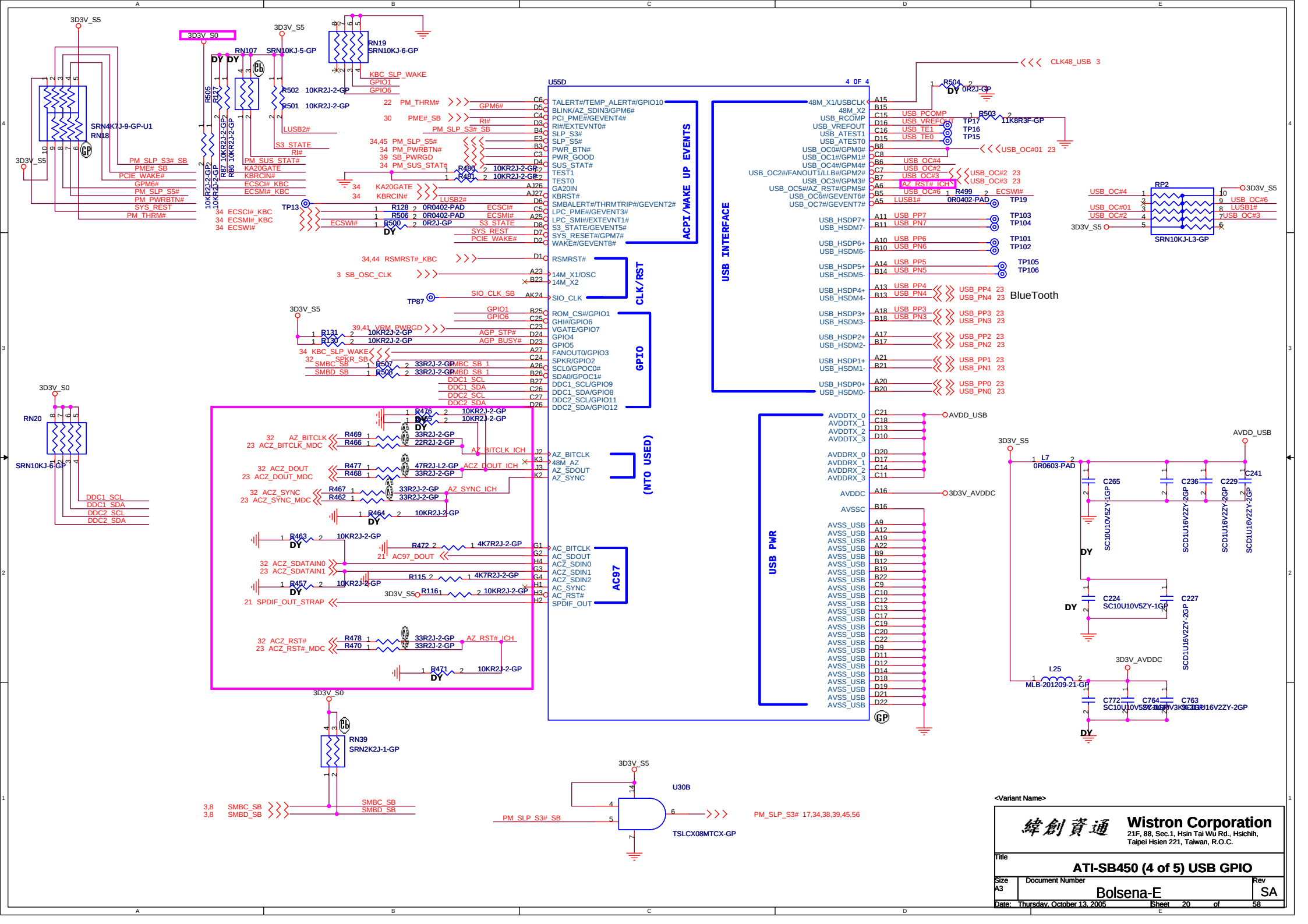
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (3 of 5) POWER

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 19 of 58



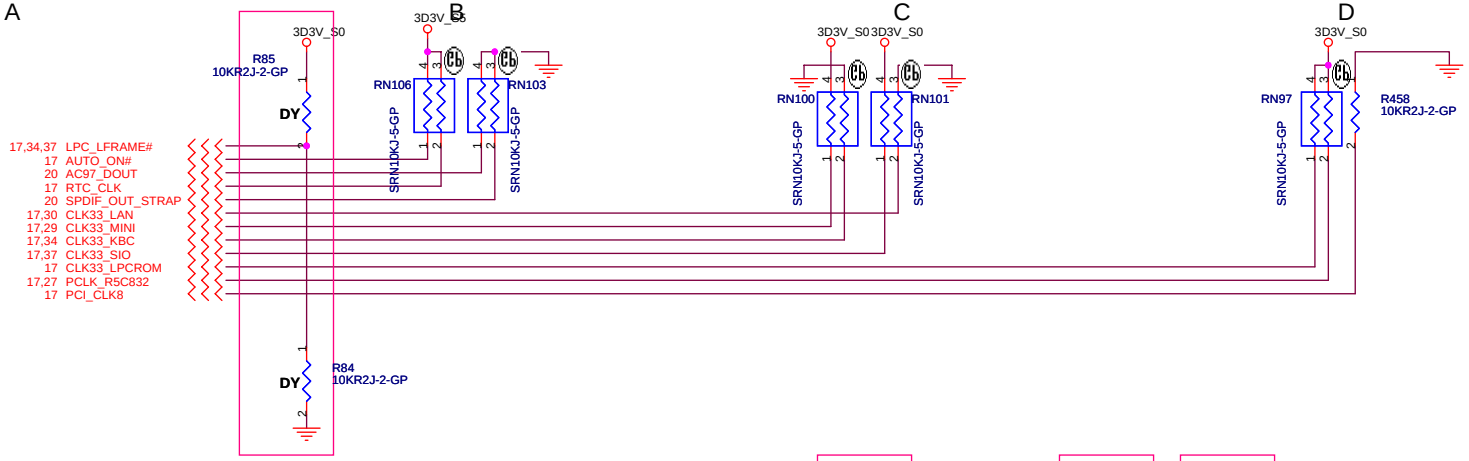
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<variant_name>

Title: ATI-SB450 (4 of 5) USB GPIO

Size: A3 | Document Number: Bolsena-E | Rev: SA

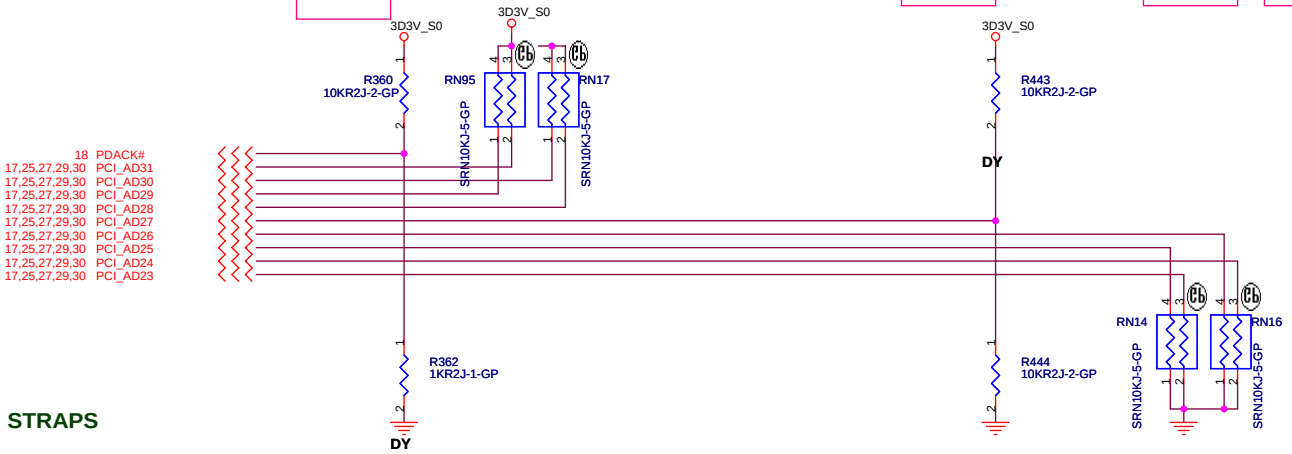
Date: Thursday, October 13, 2005 | Sheet 20 of 58



Place these R close to SouthBridge if possible

REQUIRED SYSTEM STRAPS

	LFRAME#	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 (CLK33_LAN)	PCI_CLK3 (CLK33_MINI)	PCI_CLK4 (CLK33_KBC)	PCI_CLK5 (CLK33_SIO)	PCI_CLK6 (CLK33_LPCROM)	PCI_CLK7 (PCLK_R5C832) PCI_CLK8
STRAP HIGH	Thermal Trip is not enable as default Optional	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ -Crytsal Pad	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48	PCIE_CM_SET HIGH DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	Thermal Trip is enable as default Optional	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ Use External only	PCIE_CM_SET LOW	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

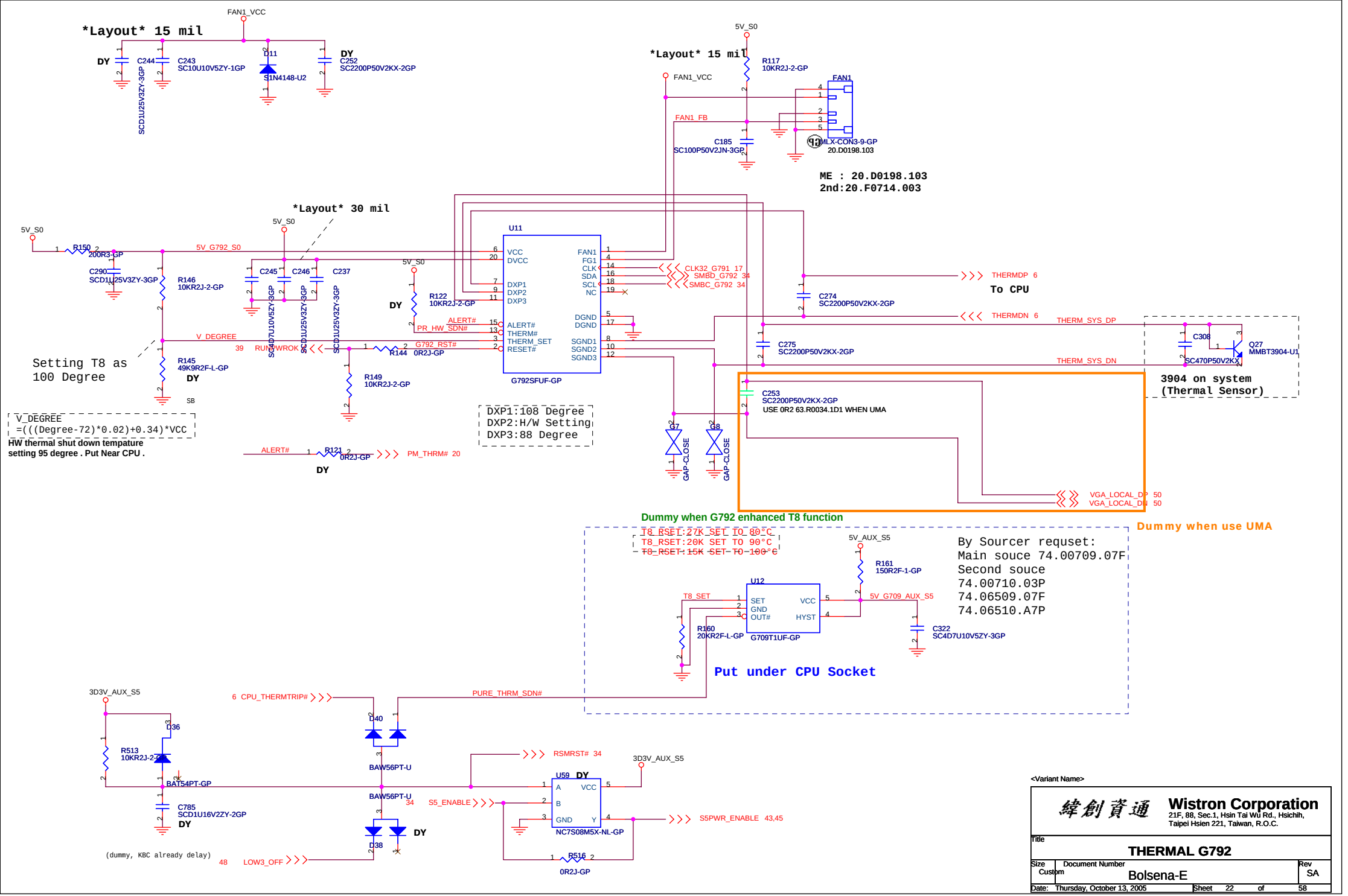
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 STRAPPING(5 of 5)

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 21 of 58



<Variant Name>

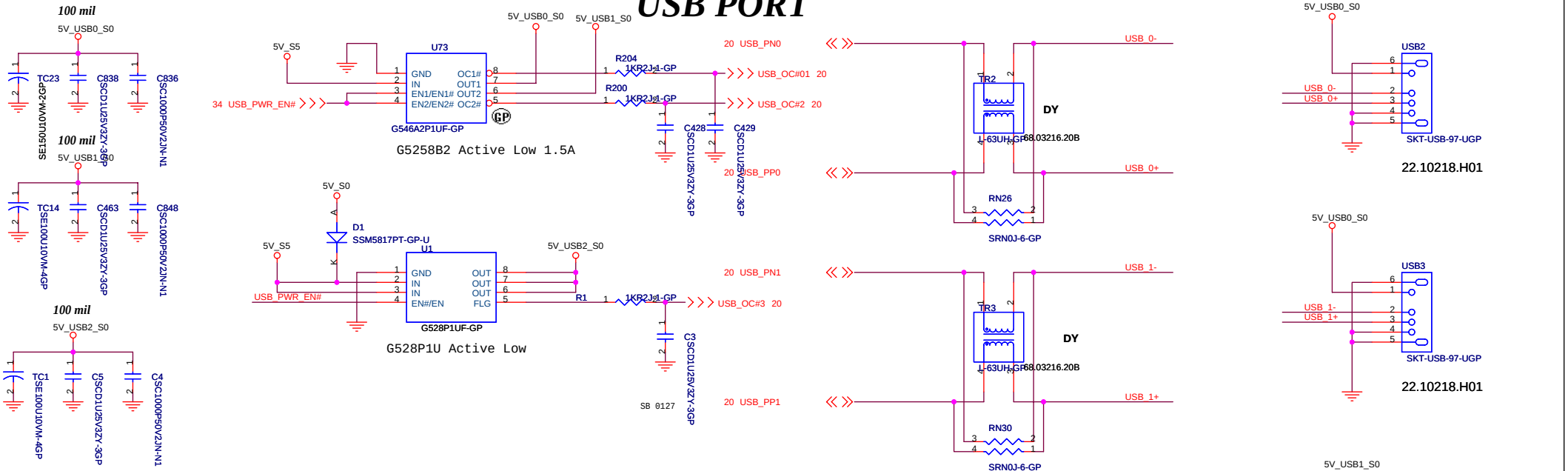
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **THERMAL G792**

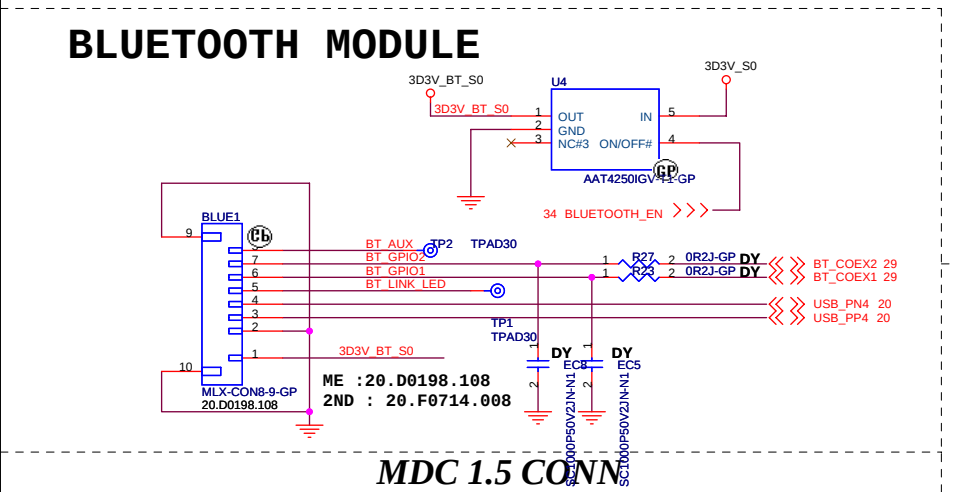
Size	Document Number	Rev
Custom	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 22 of 58

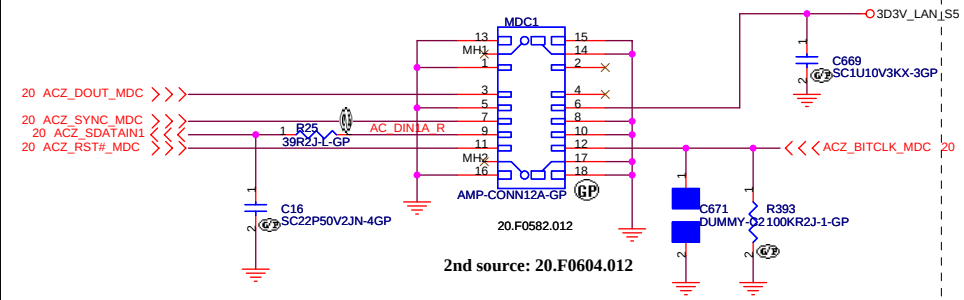
USB PORT



BLUETOOTH MODULE



MDC 1.5 CONN

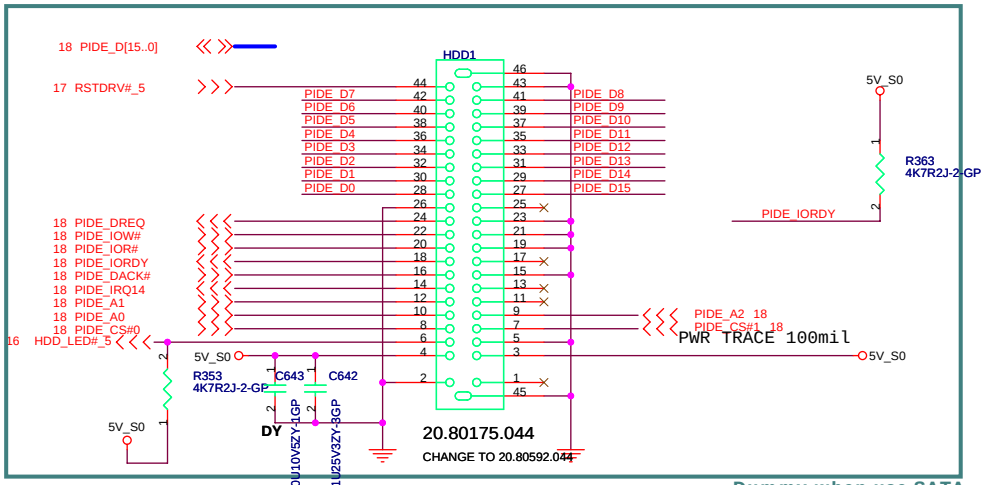


ME : 22.10218.H01
2ND : 22.10245.H11

<Variant Name>

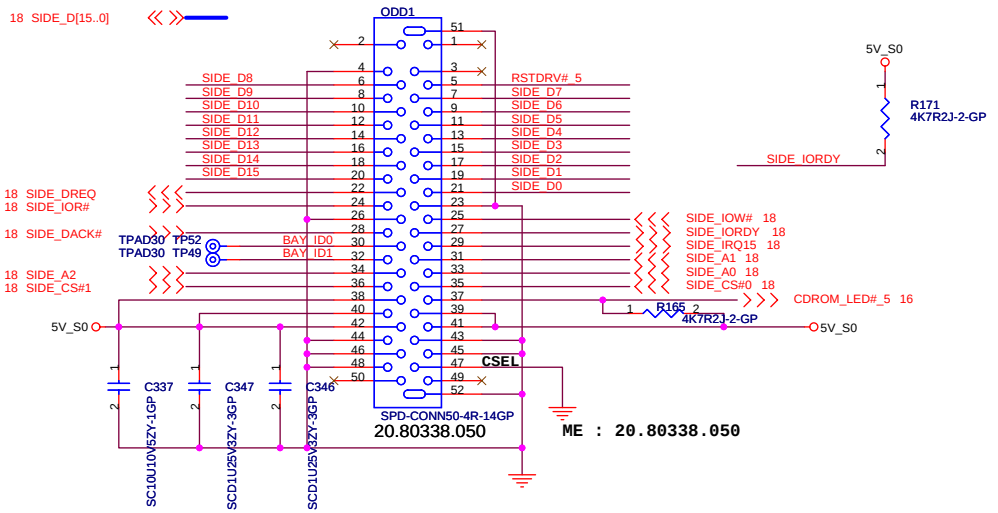
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: USB / MDC / BLUETOOTH		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 23 of 58	

HDD



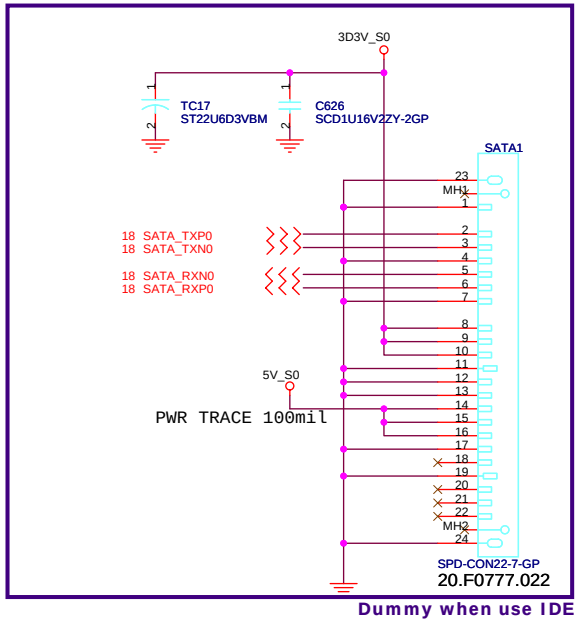
ME : 20.80592.044
(DIFFERENT FROM ORCAD P/N)

CDROM



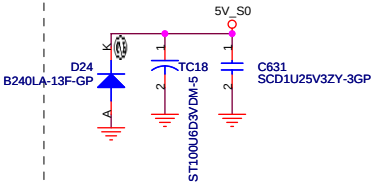
ME : 20.80338.050

SATA Connector



ME : 20.F0777.022

For HDD & SATA both



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM / SATA**

Size	Document Number	Rev
A3	Bolsena-E	SA

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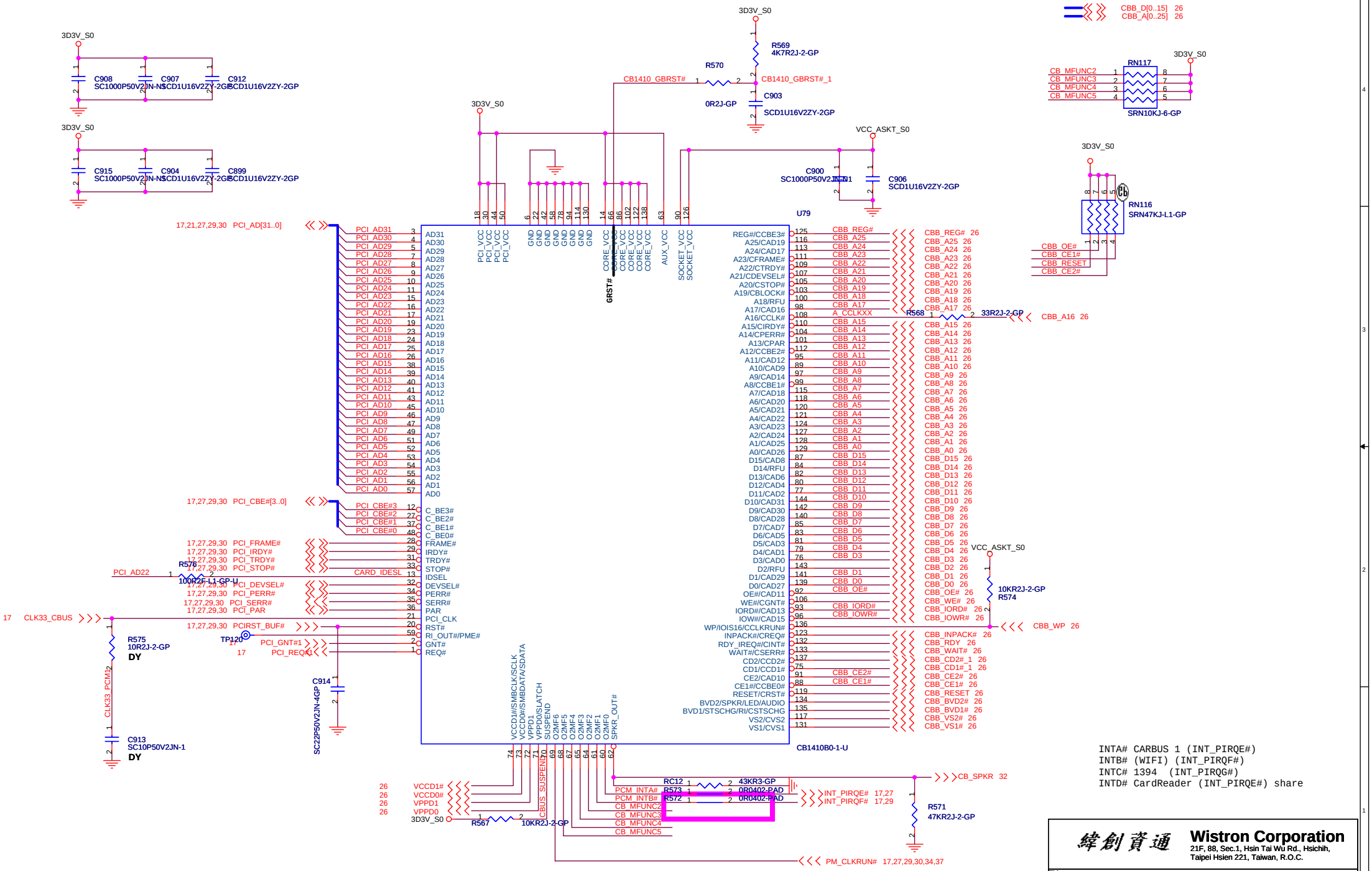
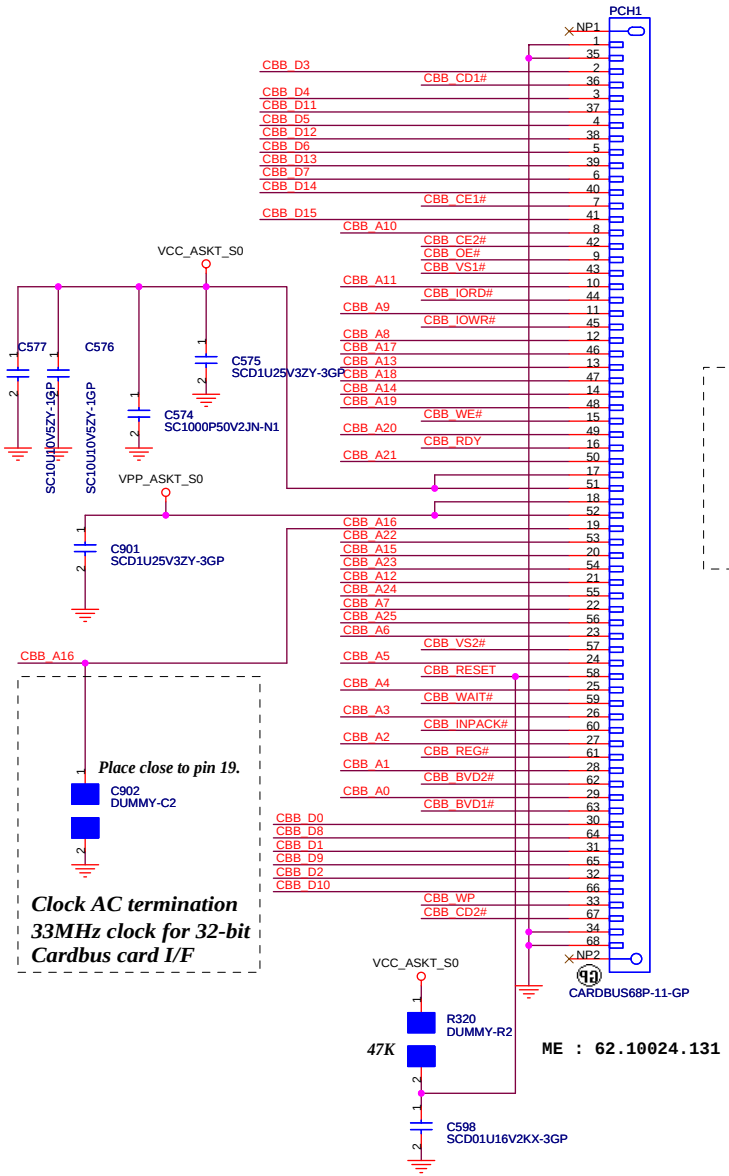
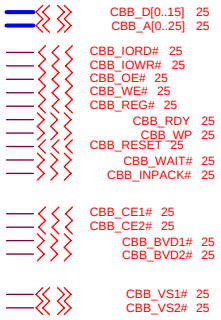


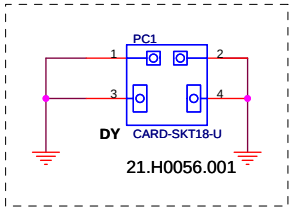
緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**CardBus_ENE CB1410**
Size A3	Document Number **Bolsena-E** Rev **SA**
Date: Thursday, October 13, 2005	Sheet 25 of 58

PCMCIA Socket



Cardbus I/F

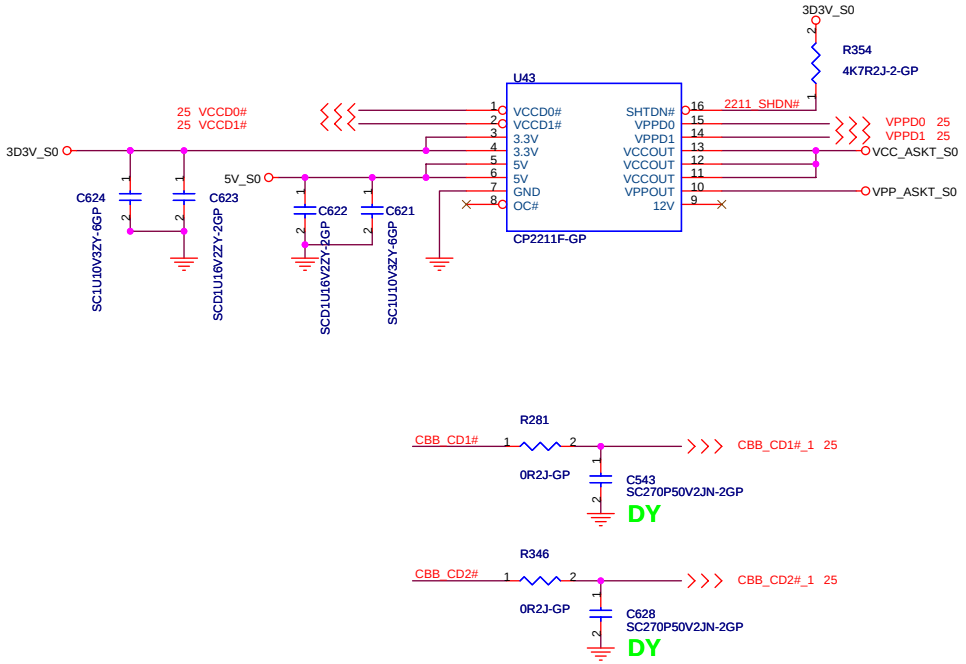




ME : 21.H0056.001

ME : 62.10024.131

Power switch



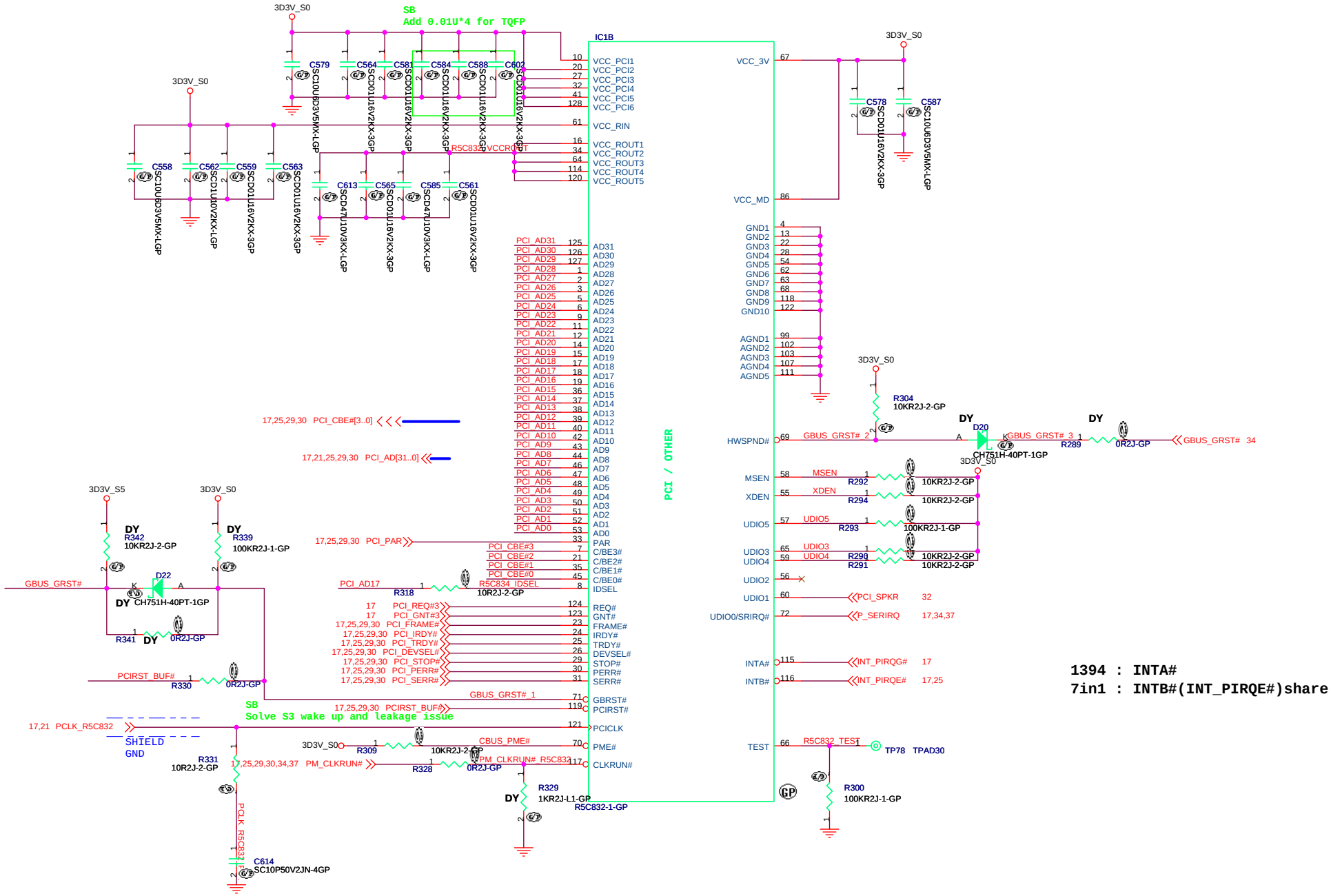
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

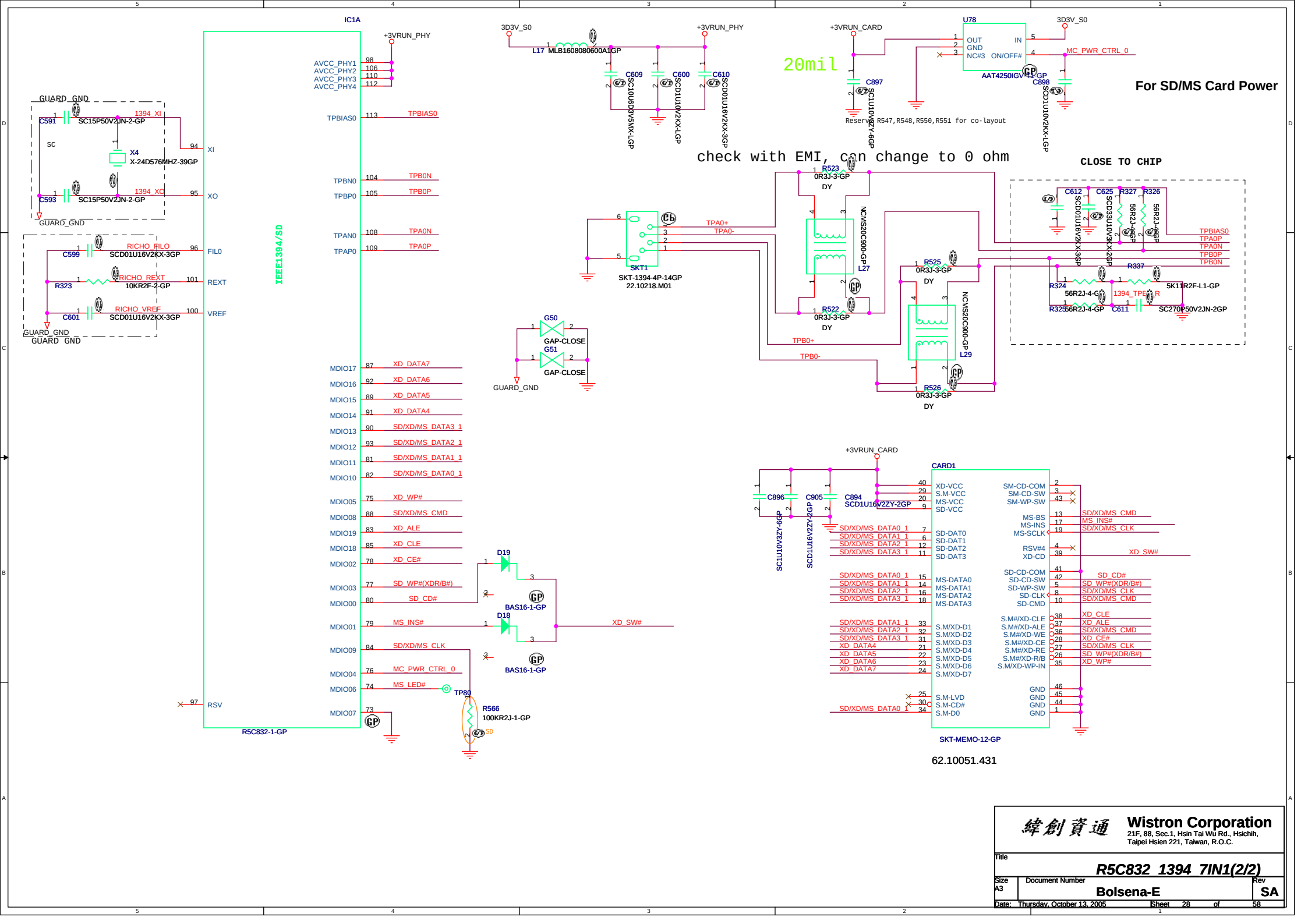
Title: PCMCA / 1394 / CARD READER

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 26 of 58

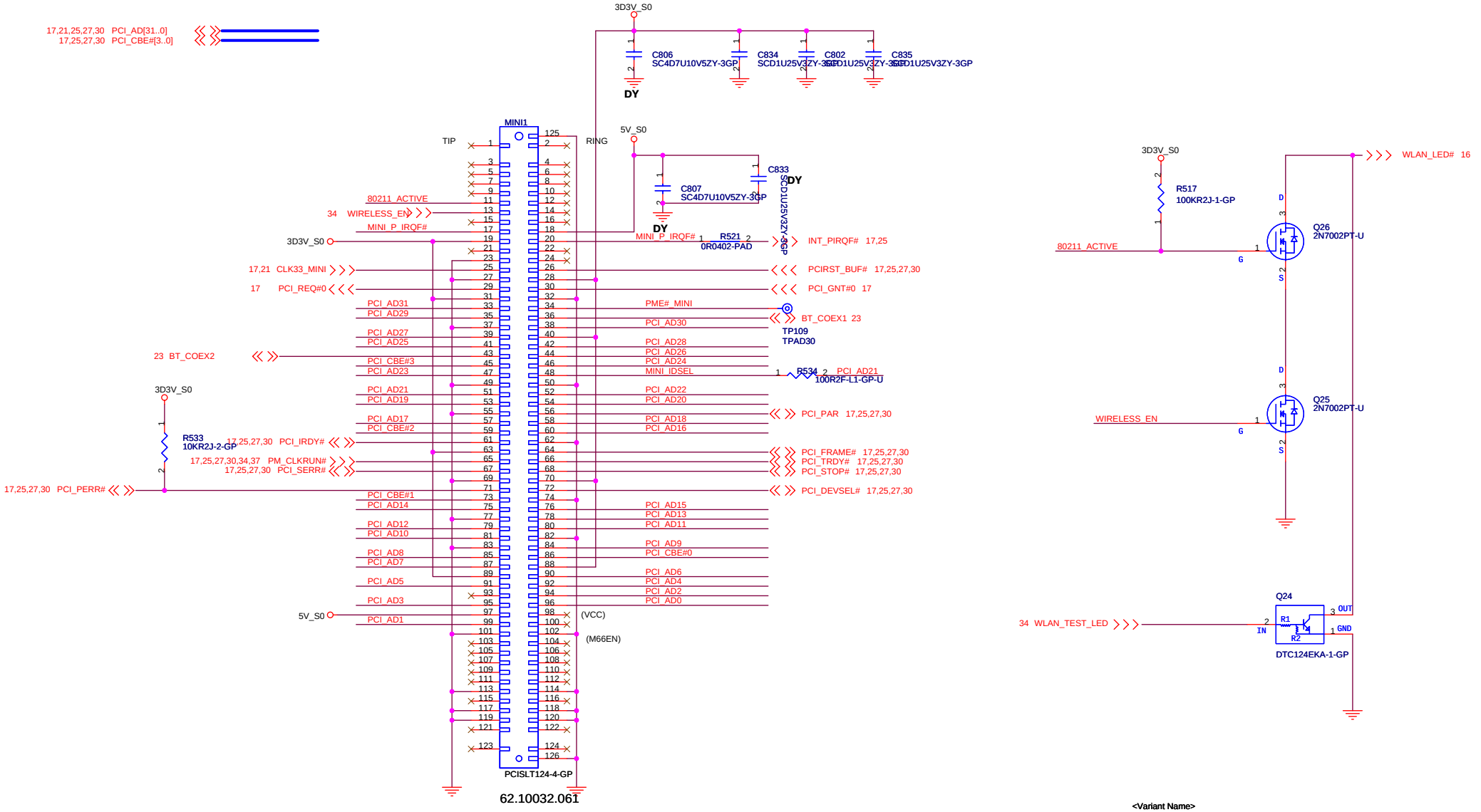


Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	R5C832_1394_7IN1(2/2)		
Size A3	Document Number Bolsena-E		Rev SA
Date: Thursday, October 13, 2005	Sheet 27 of 58		



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	R5C832_1394_7IN1(2/2)
Size A3	Document Number Bolsena-E
Rev	SA
Date: Thursday, October 13, 2005	Sheet 28 of 58

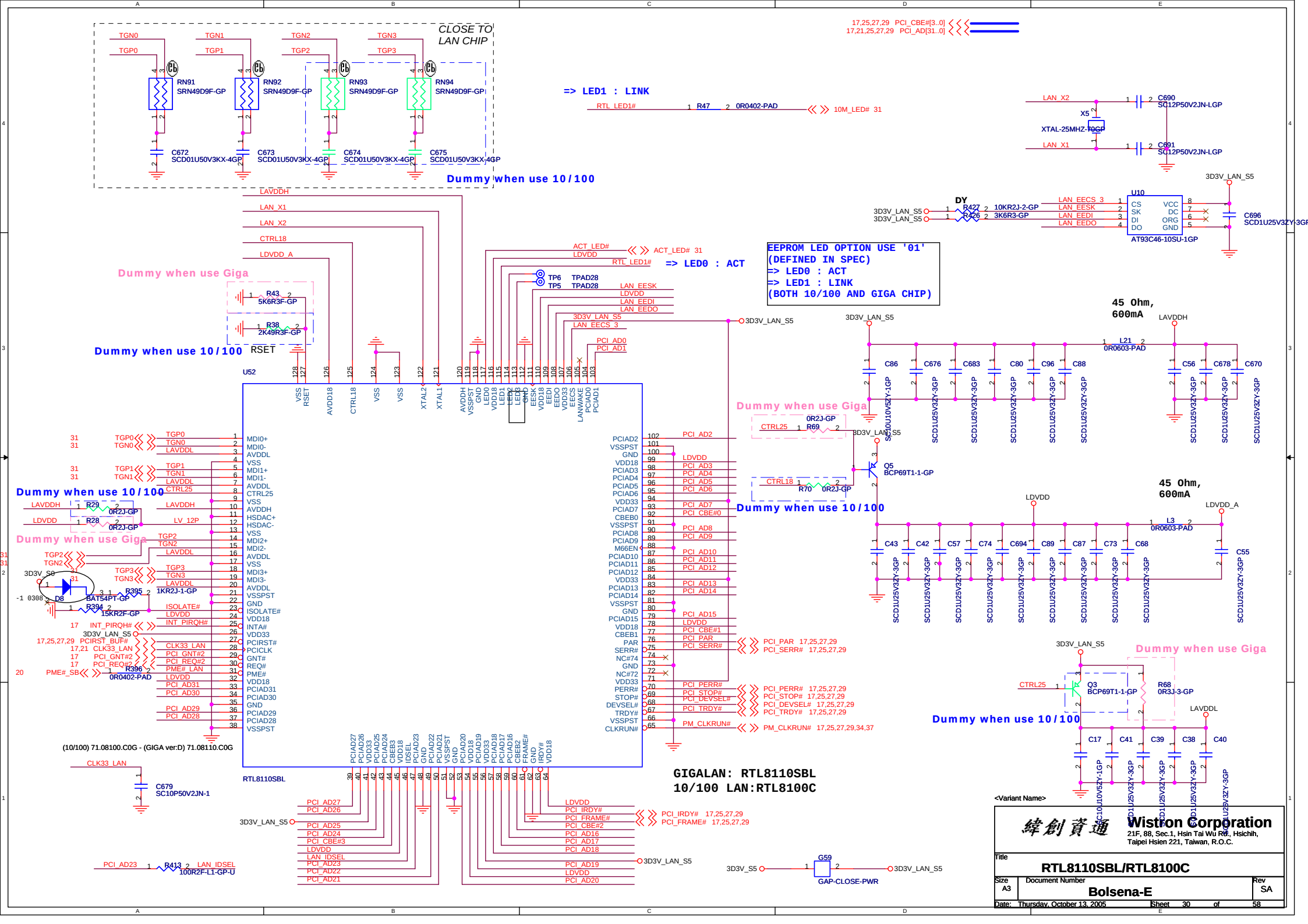
MINI-PCI



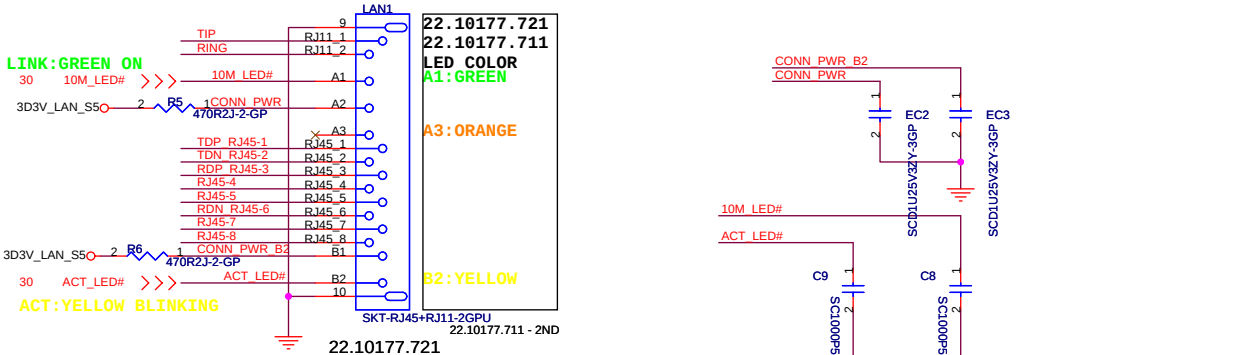
<Variant Name>

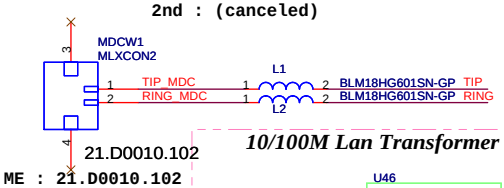
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

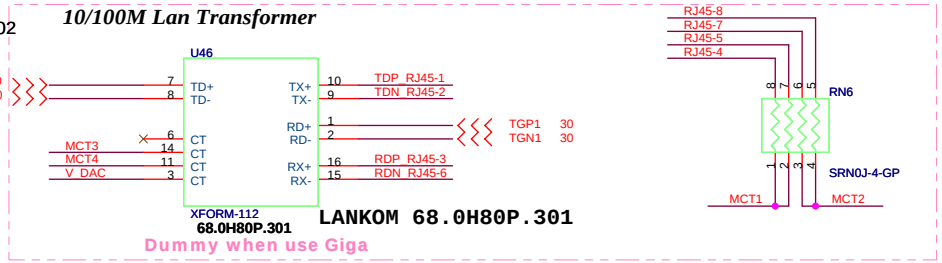
Title	MINI-PCI	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 29 of 58	

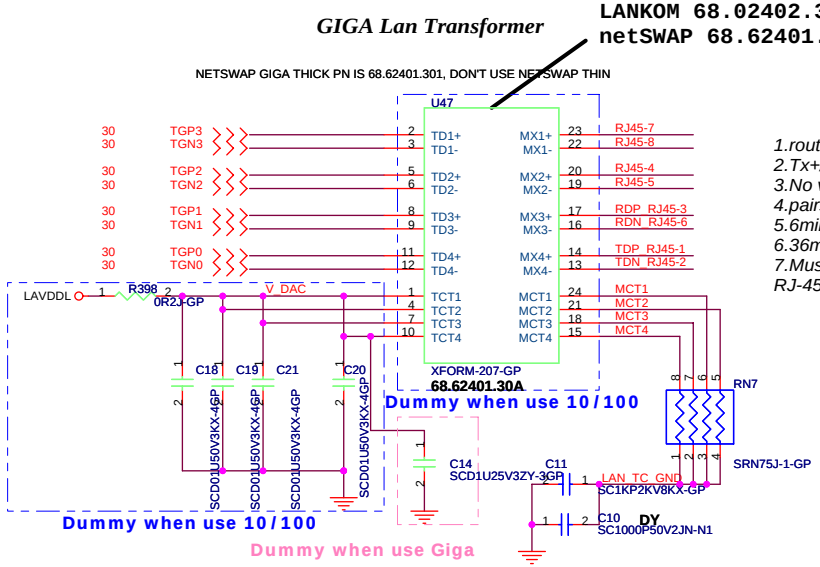

CLOSE TO LAN CHIP
RN91 SRN49D9F-GP
RN92 SRN49D9F-GP
RN93 SRN49D9F-GP
RN94 SRN49D9F-GP
C672 SCD01U50V3KX-4GP
C673 SCD01U50V3KX-4GP
C674 SCD01U50V3KX-4GP
C675 SCD01U50V3KX-4GP
Dummy when use 10/100
=> LED1 : LINK
RTL_LED1# R47 0R0402-PAD 10M_LED# 31
17,25,27,29 PCI_CBE#[3..0]
17,21,25,27,29 PCI_AD[31..0]
LAN_X2 C690 SC12P50V2JN-LGP
X5 XTAL-25MHZ-10GP
LAN_X1 C691 SC12P50V2JN-LGP
3D3V_LAN_S5
DY R427 10KR2J-2-GP
R426 3K6R3-GP
LAN_EECS_3 LAN_EESK LAN_EEDI LAN_EEDO
U10 CS SK DI DO VCC DC ORG GND
AT93C46-10SU-1GP
C696 SCD1U25V3ZY-3GP
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
Dummy when use Giga
R43 5K6R3F-GP
R38 2K49R3F-GP
Dummy when use 10/100
RSET
LAVDDH
LAN_X1
LAN_X2
CTRL18
LDVDD_A
ACT_LED# ACT_LED# 31
LDVDD
RTL_LED1#
TP6 TPAD28
TP5 TPAD28
LAN_EESK
LDVDD
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
U52
VSS RSET AVDDH CTRL18 VSS VSS XTAL2 XTAL1 AVDDH VSSPST GND LED0 VDD18 LED1 LED2 LED3 GND EESK VDD18 EEDI EEDO VDD33 EECS LANWAKE PCIAD0 PCIAD1
MDI0+ MDI0- AVDDL VSS MDI1+ MDI1- AVDDL CTRL25 VSS AVDDH HSDAC+ HSDAC- VSS MDI2+ MDI2- AVDDL VSS MDI3+ MDI3- AVDDL VSSPST GND ISOLATE# VDD18 INTA# VDD33 PCIRST# PCICLK GNT# REQ# PME# VDD18 PCIAD31 PCIAD30 GND PCIAD29 PCIAD28 VSSPST
PCIAD2 VSSPST GND VDD18 PCIAD3 PCIAD4 PCIAD5 PCIAD6 VDD33 PCIAD7 CBEB0 VSSPST PCIAD8 PCIAD9 M66EN PCIAD10 PCIAD11 PCIAD12 VDD33 PCIAD13 PCIAD14 VSSPST GND PCIAD15 VDD18 CBEB1 PAR SERR# NC#74 GND NC#72 VDD33 PERR# STOP# DEVSEL# TRDY# VSSPST CLKRUN#
PCI_AD2 LDVDD PCI_AD3 PCI_AD4 PCI_AD5 PCI_AD6 PCI_AD7 PCI_CBE#0 PCI_AD8 PCI_AD9 PCI_AD10 PCI_AD11 PCI_AD12 PCI_AD13 PCI_AD14 PCI_AD15 LDVDD PCI_CBE#1 PCI_PAR PCI_SERR# PCI_PERR# PCI_STOP# PCI_DEVSEL# PCI_TRDY# PM_CLKRUN#
PCI_PAR 17,25,27,29
PCI_SERR# 17,25,27,29
PCI_PERR# 17,25,27,29
PCI_STOP# 17,25,27,29
PCI_DEVSEL# 17,25,27,29
PCI_TRDY# 17,25,27,29
PM_CLKRUN# 17,25,27,29,34,37
Dummy when use Giga
CTRL25 R69 0R2J-GP
CTRL18 R70 0R2J-GP
Q5 BCP69T1-1-GP
Dummy when use 10/100
45 Ohm, 600mA
L21 0R0603-PAD
C86 C676 C683 C80 C96 C88 SCD1U10V5ZY-1GP SCD1U25V3ZY-3GP
C56 C678 C670 SCD1U25V3ZY-3GP
LDVDD
LDVDD_A
L3 0R0603-PAD
C43 C42 C57 C74 C694 C89 C87 C73 C68 C55 SCD1U25V3ZY-3GP
Dummy when use Giga
Q3 BCP69T1-1-GP
R68 0R3J-3-GP
Dummy when use 10/100
LAVDDL
C17 C41 C39 C38 C40 SC10U10V5ZY-1GP SCD1U25V3ZY-3GP
TGP0 TGN0 TGP1 TGN1 TGP2 TGN2 TGP3 TGN3
LV_12P
R29 0R2J-GP
R28 0R2J-GP
Dummy when use 10/100
Dummy when use Giga
3D3V_S0
D8 BAT54PT-GP
R395 1KR2J-1-GP
R394 15KR2F-GP
ISOLATE#
INT_PIRQH#
CLK33_LAN
PCI_GNT#2
PCI_REQ#2
PME#_LAN
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
17,25,27,29 PCIRST_BUF#
17,21 CLK33_LAN
17 PCI_GNT#2
17 PCI_REQ#2
20 PME#_SB
R396 0R0402-PAD
(10/100) 71.08100.C0G - (GIGA ver:D) 71.08110.C0G
RTL8110SBL
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
CLK33_LAN
C679 SC10P50V2JN-1
PCIAD27 PCIAD26 VDD33 PCIAD25 PCIAD24 CBEB3 VDD18 IDSEL PCIAD23 GND PCIAD22 PCIAD21 VSSPST GND PCIAD20 VDD18 PCIAD19 VDD33 PCIAD18 PCIAD17 PCIAD16 CBEB2 FRAME# GND IRDY# VDD18
PCI_AD27 PCI_AD26 PCI_AD25 PCI_AD24 PCI_CBE#3 LDVDD LAN_IDSEL PCI_AD23 PCI_AD22 PCI_AD21
LDVDD PCI_IRDY# PCI_FRAME# PCI_CBE#2 PCI_AD16 PCI_AD17 PCI_AD18 PCI_AD19 LDVDD PCI_AD20
PCI_IRDY# 17,25,27,29
PCI_FRAME# 17,25,27,29
PCI_AD23 R413 100R2F-L1-GP-U LAN_IDSEL
3D3V_S5 G59 GAP-CLOSE-PWR 3D3V_LAN_S5
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title RTL8110SBL/RTL8100C
Size A3 Document Number Bolsena-E Rev SA
Date: Thursday, October 13, 2005 Sheet 30 of 58

Link: Green - 10Mbps/802.11b Activity: Yellow
Orange - 100Mbps/802.11a
Yellow - 1Gbps









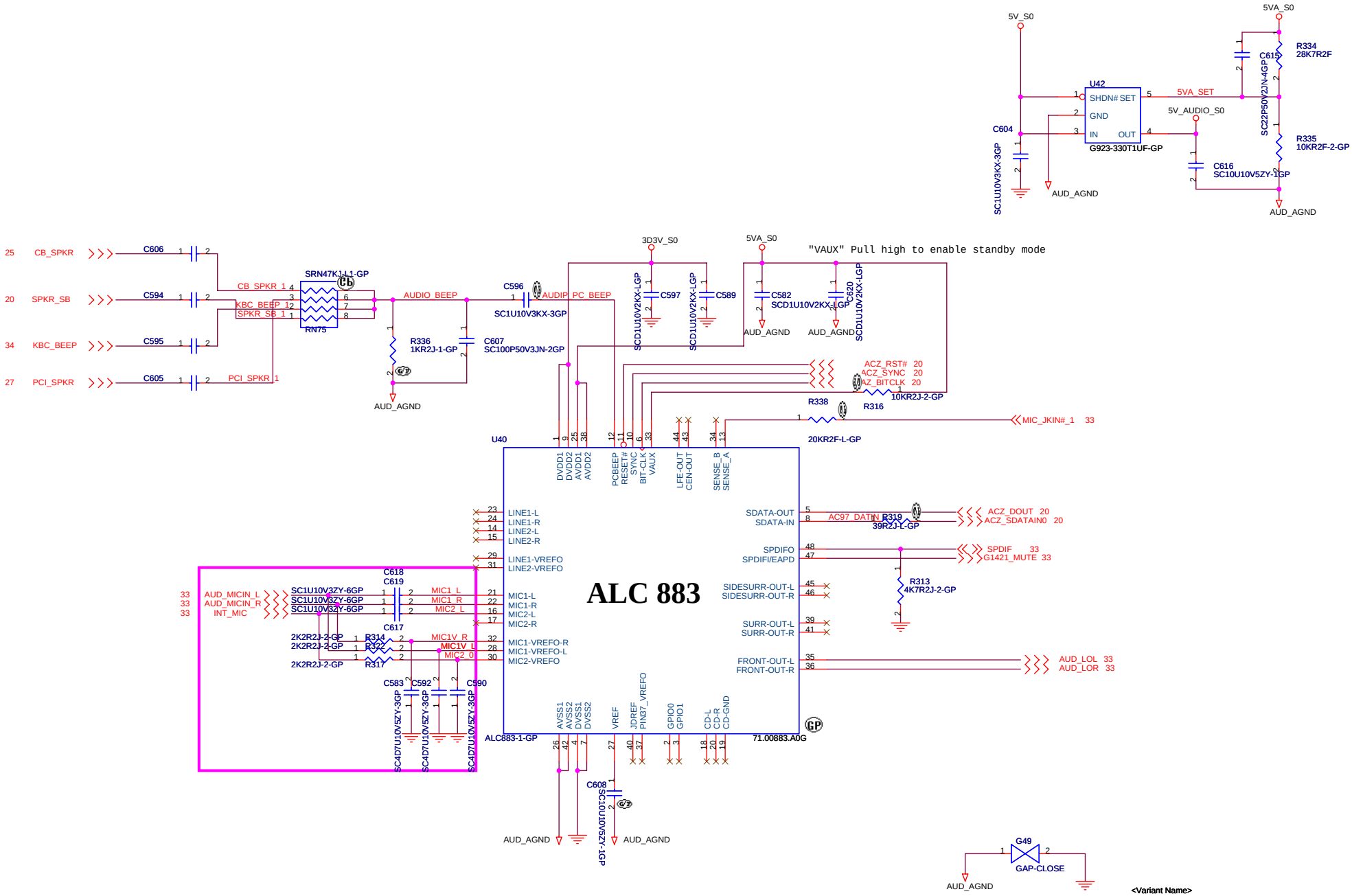
1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 31 of 58



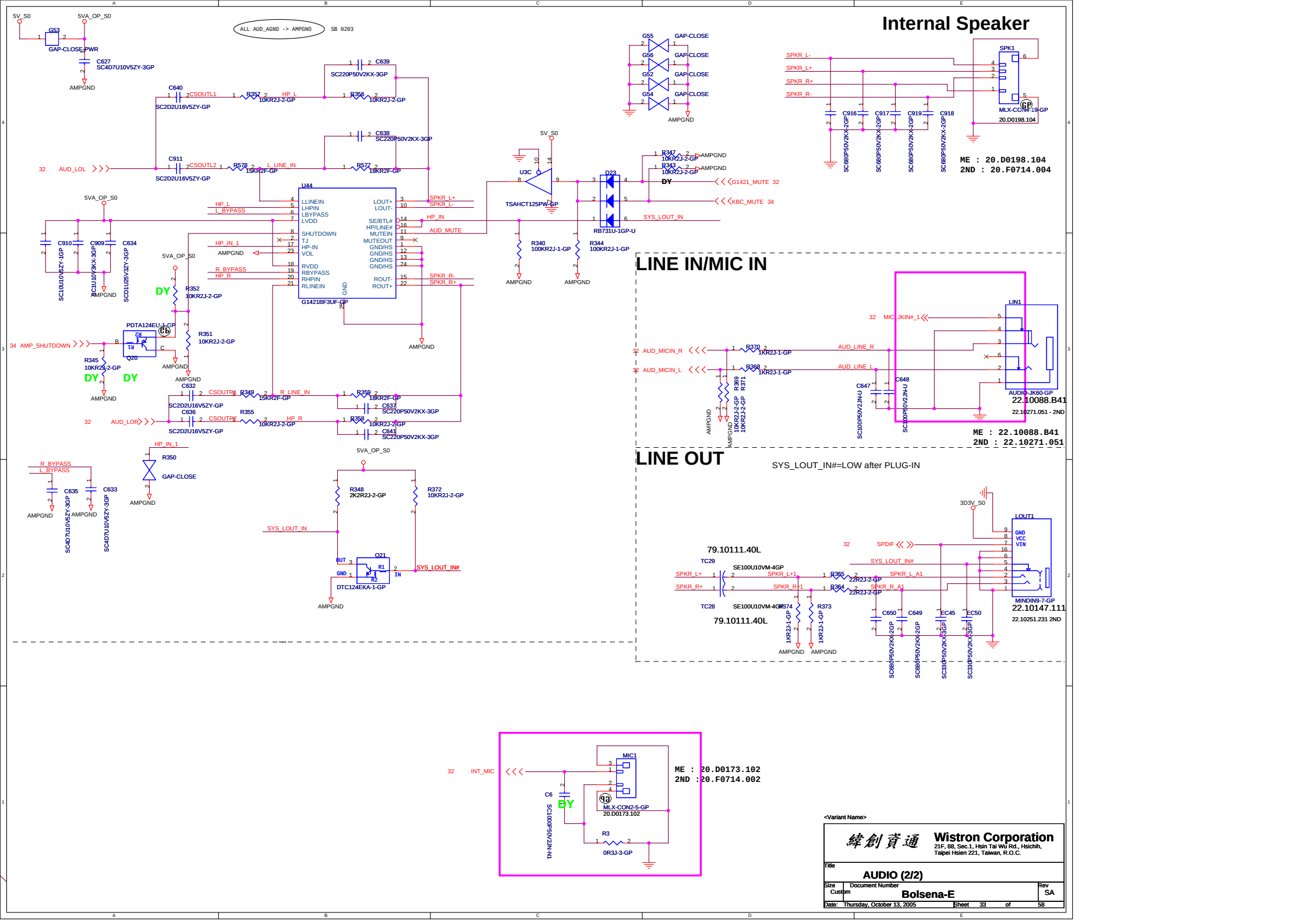
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

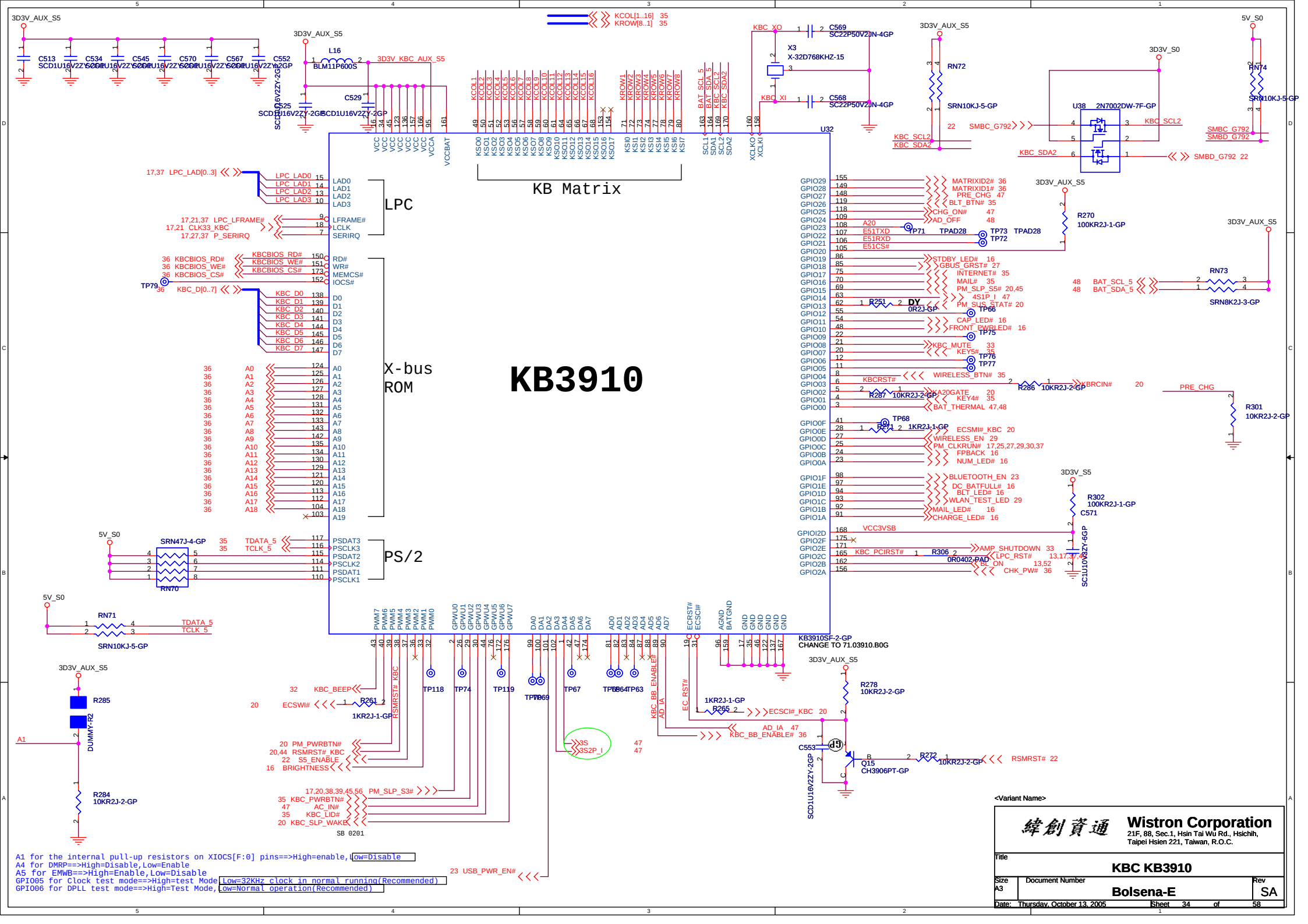
<Variant Name>

Title: AUDIO (1/2) -- CODEC ALC655

Size: A3 | Document Number: Bolsena-E | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 32 of 58


Internal Speaker
LINE IN/MIC IN
LINE OUT
SYS_LOUT_IN#=LOW after PLUG-IN
ALL AUD_AGND -> AMPGND
SB 0203
U44
G1421BF3UF-GP
TSAHCT125PW-GP
RB731U-1GP-U
PDTA124EU-1-GP
DTC124EKA-1-GP
SE100U10VM-4GP
MLX-CON2-19-GP
MLX-CON2-5-GP
AUDIO-JK60-GP
MINDIN9-7-GP
ME : 20.D0198.104
2ND : 20.F0714.004
ME : 22.10088.B41
2ND : 22.10271.051
ME : 20.D0173.102
2ND :20.F0714.002
22.10088.B41
22.10271.051 - 2ND
79.10111.40L
22.10147.111
22.10251.231 2ND
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (2/2)
Size
Custom
Document Number
Bolsena-E
Rev
SA
Date: Thursday, October 13, 2005
Sheet 33 of 58


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
3D3V_AUX_S5
5V_S0
3D3V_S0
3D3V_KBC_AUX_S5
KCOL[1..16] 35
KROW[8..1] 35
KBC_XO
KBC_XI
X3
X-32D768KHZ-15
C569 SC22P50V2JN-4GP
C568 SC22P50V2JN-4GP
RN72 SRN10KJ-5-GP
RN74 SRN10KJ-5-GP
U38 2N7002DW-7F-GP
SMBC_G792
SMBD_G792
KBC_SCL2
KBC_SDA2
U32
LPC_LAD[0..3]
LFRAME#
LCLK
SERIRQ
KBCBIOS_RD#
KBCBIOS_WE#
KBCBIOS_CS#
KBC_D[0..7]
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A16
A17
A18
A19
TDATA_5
TCLK_5
PSDAT3
PSCLK3
PSDAT2
PSCLK2
PSDAT1
PSCLK1
SRN47J-4-GP
RN70
RN71
SRN10KJ-5-GP
KB3910SF-2-GP
CHANGE TO 71.03910.B0G
R285
DUMMY-R2
R284 10KR2J-2-GP
R261 1KR2J-1-GP
R265 1KR2J-1-GP
R278 10KR2J-2-GP
R272 10KR2J-2-GP
Q15 CH3906PT-GP
C553 SCD1U16V2ZY-2GP
R270 100KR2J-1-GP
R302 100KR2J-1-GP
C571 SC1U10V3ZY-6GP
R251 DY 0R2J-GP
R286 10KR2J-2-GP
R287 10KR2J-2-GP
R301 10KR2J-2-GP
R306 0R0402-PAD
RN73 SRN8K2J-3-GP
TP66
TP67
TP68
TP71
TP72
TP73
TP74
TP75
TP76
TP77
TP118
TP119
TPAD28
GPIO29 MATRIXID2# 36
GPIO28 MATRIXID1# 36
GPIO27 PRE_CHG 47
GPIO26 BLT_BTN# 35
GPIO25 CHG_ON# 47
GPIO24 AD_OFF 48
GPIO23 A20
GPIO22 E51TXD
GPIO21 E51RXD
GPIO20 E51CS#
GPIO19 STDBY_LED# 16
GPIO18 GBUS_GRST# 27
GPIO17 INTERNET# 35
GPIO16 MAIL# 35
GPIO15 PM_SLP_S5# 20,45
GPIO14 4S1P_I 47
GPIO13 PM_SUS_STAT# 20
GPIO12
GPIO11 CAP_LED# 16
GPIO10 FRONT_PWRLED# 16
GPIO09
GPIO08 KBC_MUTE 33
GPIO07 KEY5# 35
GPIO06
GPIO05
GPIO04 WIRELESS_BTN# 35
GPIO03 KBCRST#
GPIO02 A20GATE 20
GPIO01 KEY4# 35
GPIO00 BAT_THERMAL 47,48
GPIO0F
GPIO0E ECSMI#_KBC 20
GPIO0D WIRELESS_EN 29
GPIO0C PM_CLKRUN# 17,25,27,29,30,37
GPIO0B FPBACK 16
GPIO0A NUM_LED# 16
GPIO1F BLUETOOTH_EN 23
GPIO1E DC_BATFULL# 16
GPIO1D BLT_LED# 16
GPIO1C WLAN_TEST_LED 29
GPIO1B MAIL_LED# 16
GPIO1A CHARGE_LED# 16
GPIOI2D VCC3VSB
GPIO2F
GPIO2E AMP_SHUTDOWN 33
GPIO2C KBC_PCIRST# LPC_RST# 13,17,37,42
GPIO2B BL_ON 13,52
GPIO2A CHK_PW# 36
PRE_CHG
BAT_SCL_5
BAT_SDA_5
KBRCIN# 20
ECSCI#_KBC 20
RSMRST# 22
SMBD_G792 22
AD_IA 47
KBC_BB_ENABLE# 36
EC_RST#
KBC_BB_ENABLE#
AD_IA
RSMRST# KBC
KBC_BEEP 32
ECSWI# 20
PM_PWRBTN# 20
RSMRST# KBC 20,44
S5_ENABLE 22
BRIGHTNESS 16
PM_SLP_S3# 17,20,38,39,45,56
KBC_PWRBTN# 35
AC_IN# 47
KBC_LID# 35
KBC_SLP_WAKE# 20
USB_PWR_EN# 23
SB 0201
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC KB3910
Size A3
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Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
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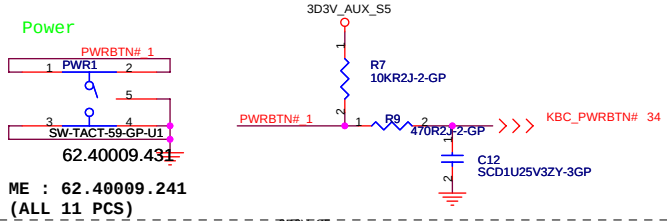
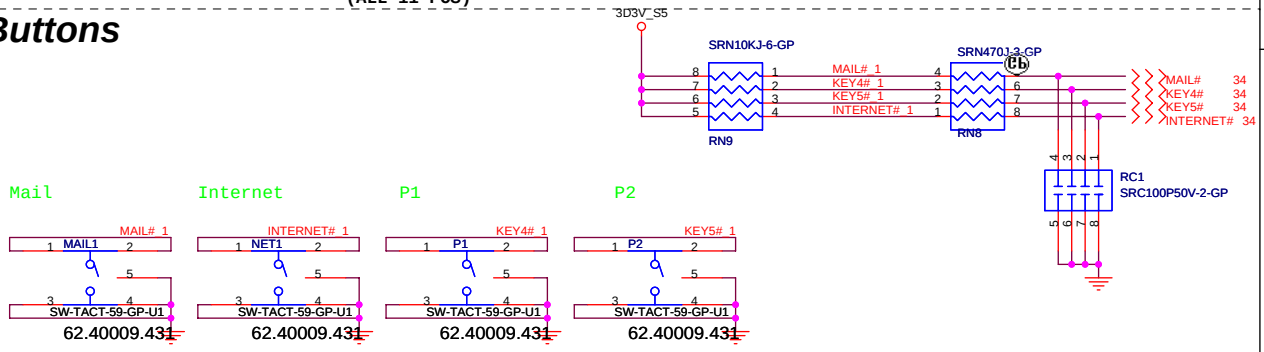
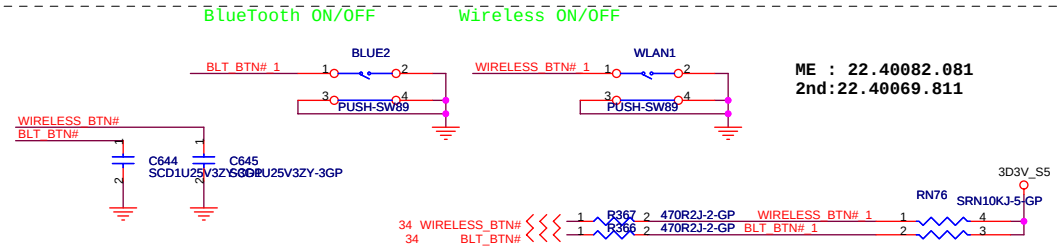
POWER BUTTON



ME : 62.40009.241
(ALL 11 PCS)

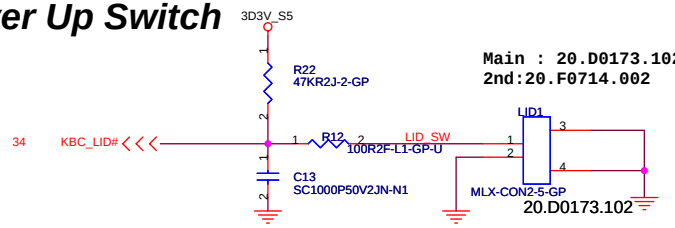
Buttons





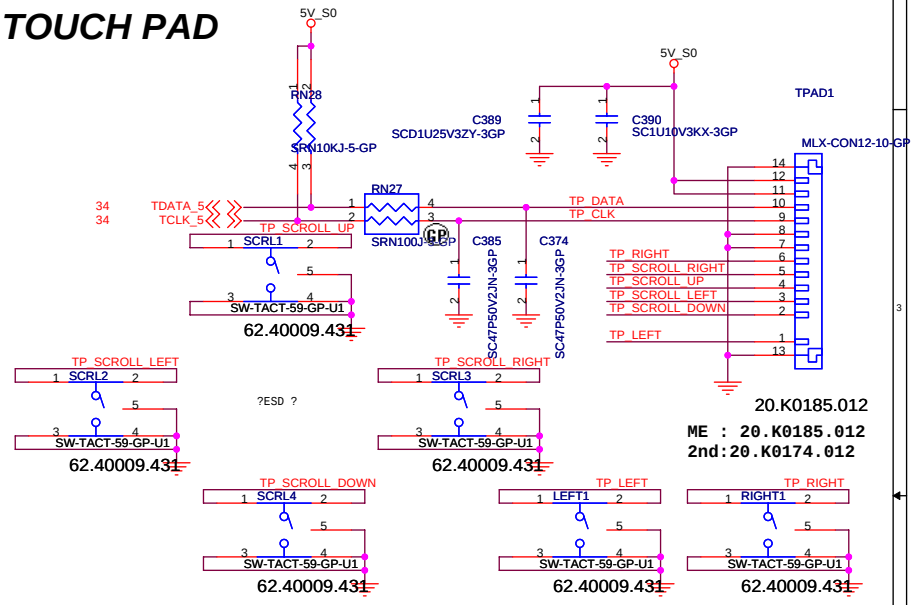
ME : 22.40082.081
2nd:22.40069.811

Cover Up Switch



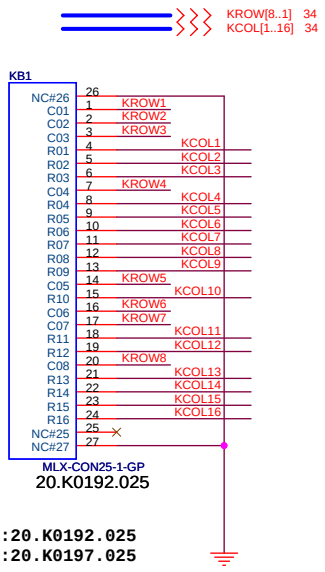
Main : 20.D0173.102
2nd:20.F0714.002

TOUCH PAD



20.K0185.012
ME : 20.K0185.012
2nd:20.K0174.012

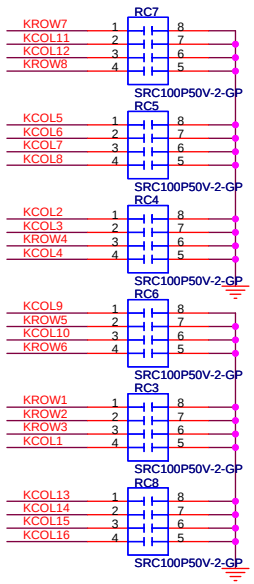
Internal KeyBoard CONN

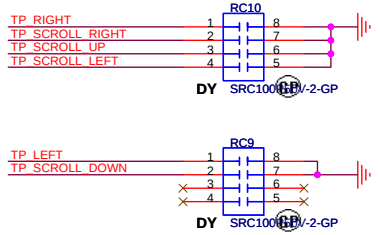


ME :20.K0192.025
2nd:20.K0197.025

Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.

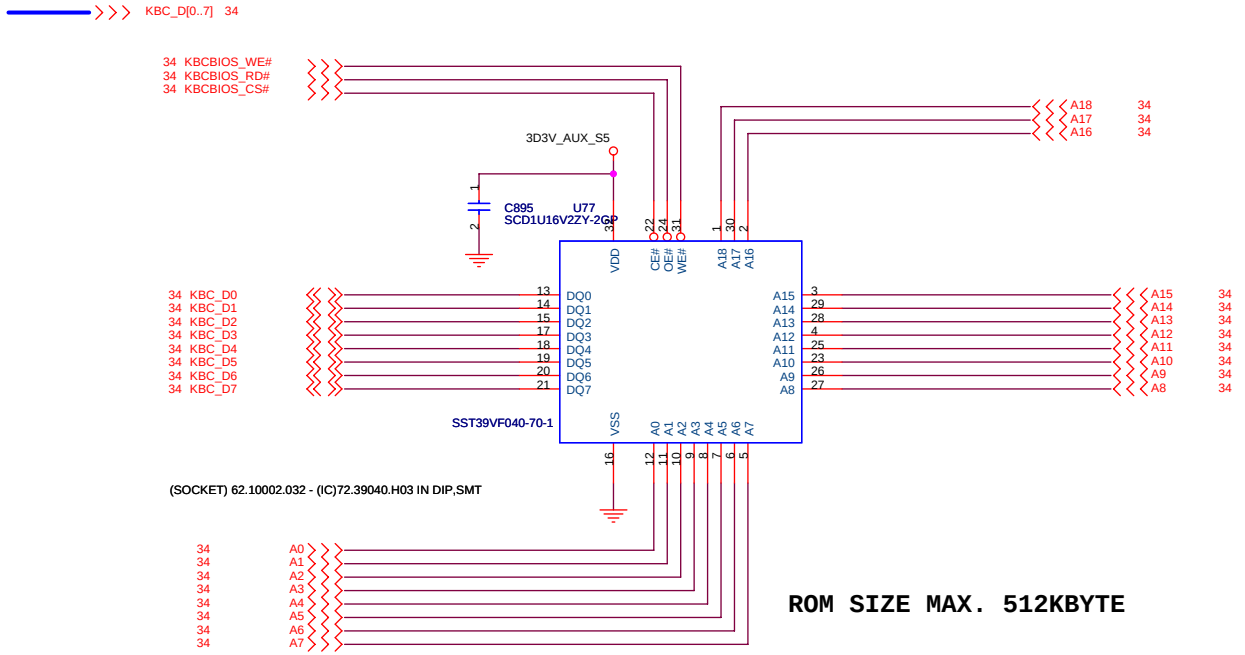




<Variant Name>

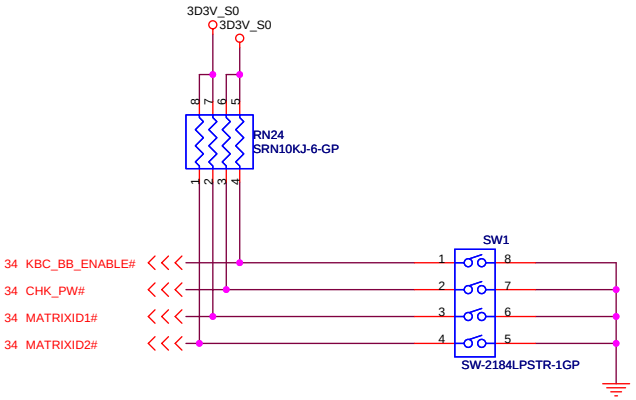
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BUTTONs / KB / TOUCHPAD
Size: A3 | Document Number: Bolsena-E | Rev: SA
Date: Thursday, October 13, 2005 | Sheet 35 of 58



ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

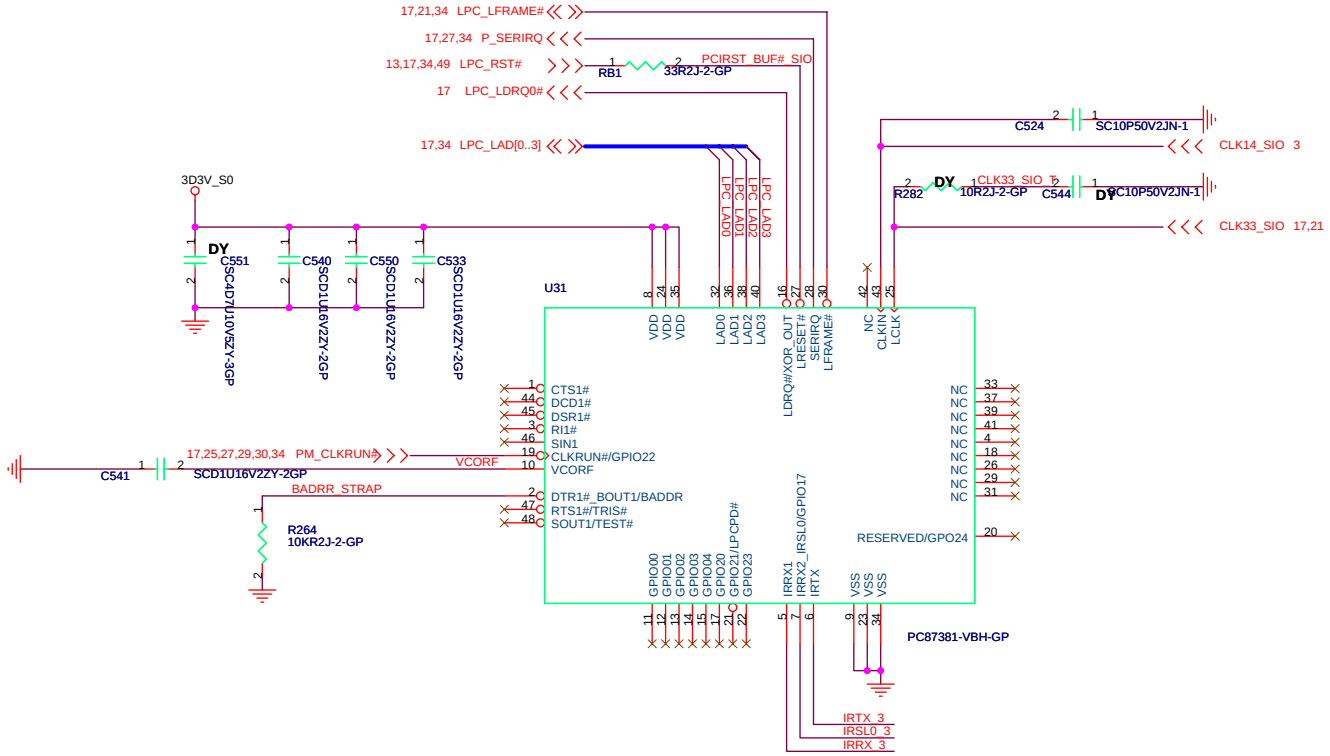
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

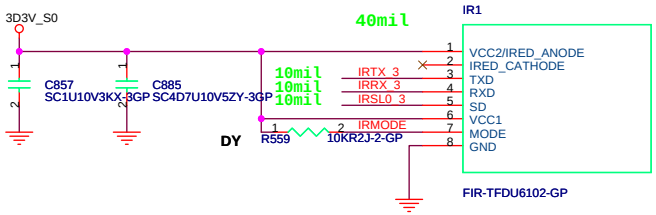
Title: **BIOS ROM**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 36 of 58



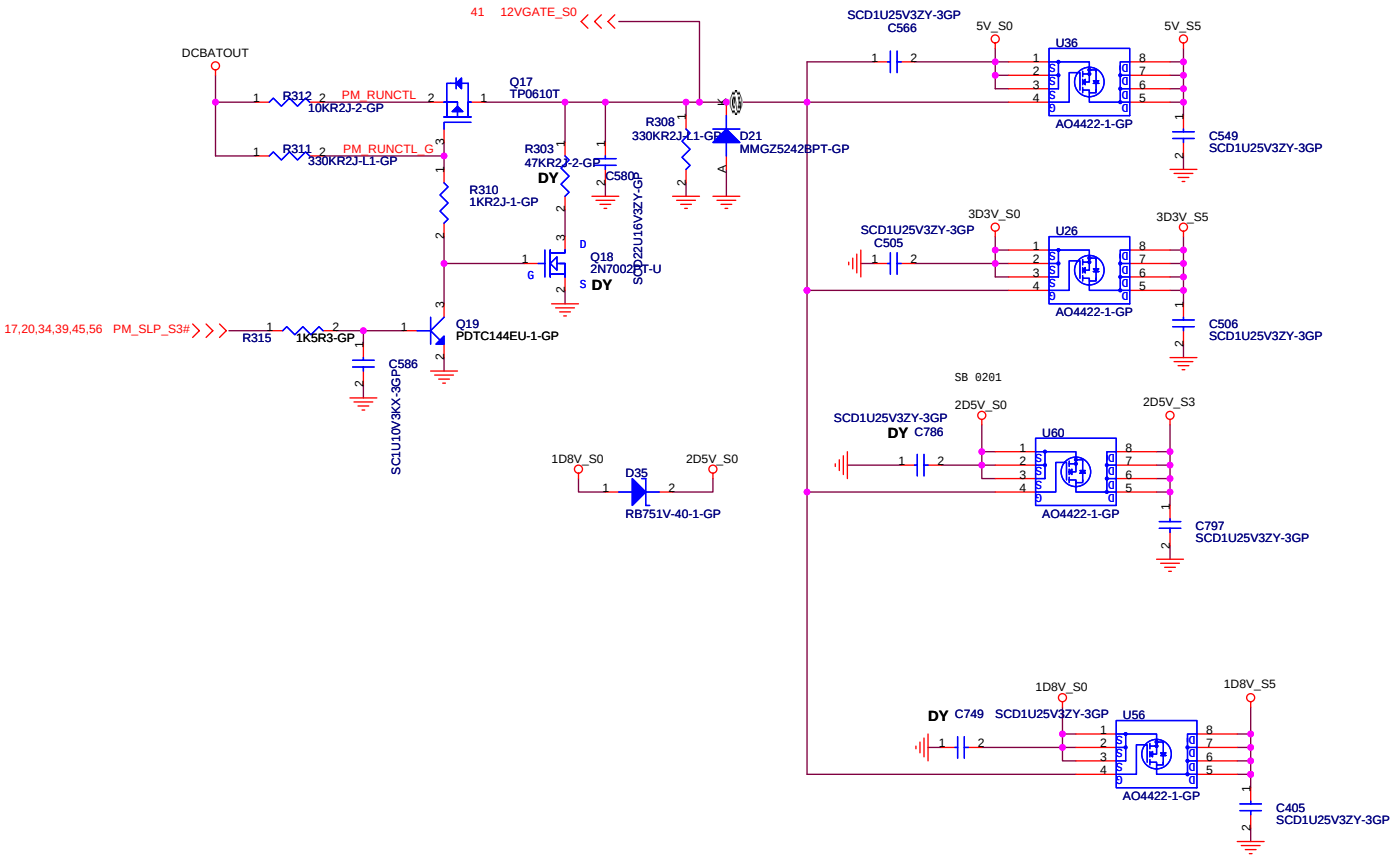
Infineon FIR Module



56.15001.051

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SUPER IO NC87381		
Size: A3	Document Number: SNIPE	Rev: -2
Date: Thursday, October 13, 2005	Sheet 37 of 58	

Run Power



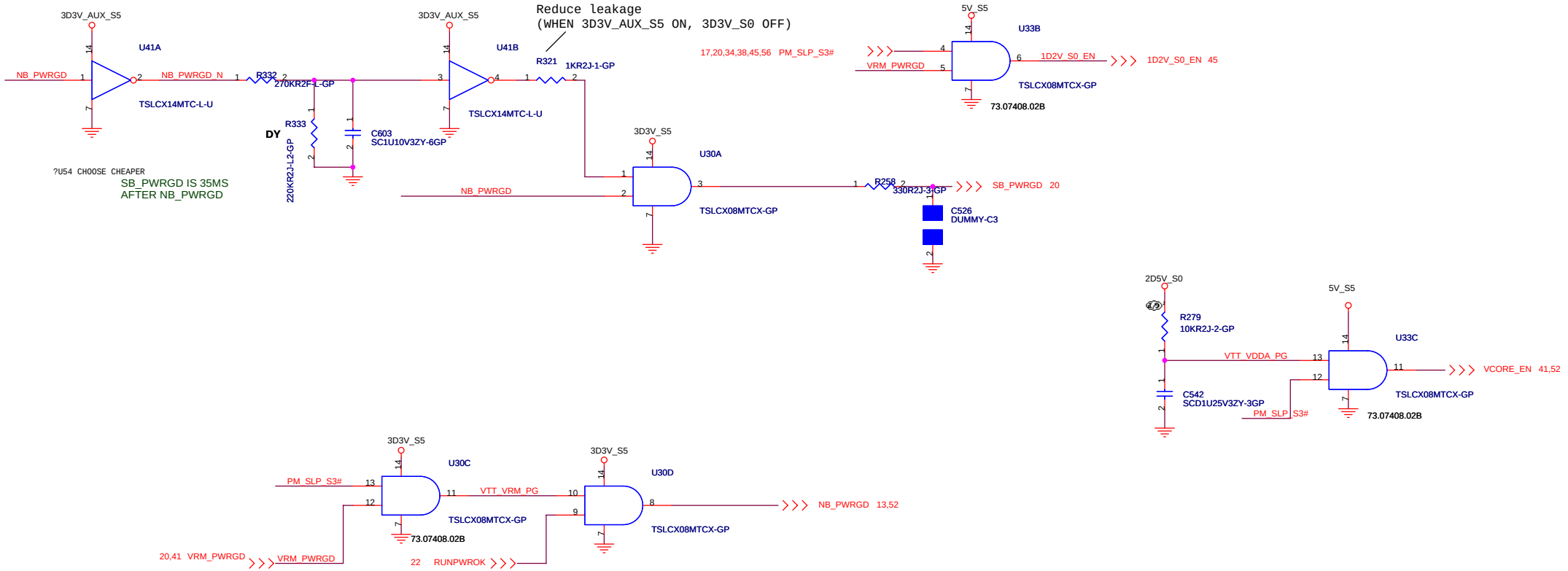
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWR CTL LOGIC / PWR PLANE**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

Date: Thursday, October 13, 2005 Sheet 38 of 58



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWERGOOD&ENABLES**

Size	Document Number	Rev
Custom	**Bolsena-E**	SA

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CPU_CORE
MAX1544ETL

VID0_PWM
VID1_PWM
VID2_PWM
VID3_PWM
VID4_PWM

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)

Output Signal
VROK()

MAX1544_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=27.3A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS5130
2D5V/1D2V/1D8V

PM_SLP_S5#
1D2V_S0_EN
S5PWR_ENABLE
GND
DCBATOUT_5130
DCBATOUT_5130

Input Signal
SS_STBY1(I / 5V) FOR 2.5V
SS_STBY2(I / 5V) FOR 1.2V
SS_STBY3(I / 5V) FOR 1.8V
STBY_LDO(I / 5V)
STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)

Output Signal
PGOUT(OD / 5V)

Pull High (5V)

Output Power
2D5(O)
1D2V(O)
1D8V(O)
LDO(O)

2D5V (9A)
1D2V (5A)
1D8V (5A)

DCBATOUT
5V_S5
5V_AUX_S5
5V_S0

Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT

5V_AUX_S5

DCBATOUT
AUX_SD

INPUT
SD
OUT

5V_AUX_S5

LP2951ACM

1D25V_S3

2D5V_S3
5V_S5
APL5331_1D25V_VREF

VIN
VCNTL
VREF
VOUT

1D25V_S0

APL5331KAC

FAN5234_VGA_Core
1D15V or 1D20V

5V_S0
DCBATOUT
PM_SLP_S3#

Input Power
VCC
VIN

Input Signal
EN

Output Signal
PG

Output Power
1D15V (O)
or
1D20V (O)

1D15V (5.2A)
or
1D20V (9A)

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Input Power
VCC(I)
VCC(I)

Output Signal
(O)

Output Power
VCC(O)

AD_IN
AD+

TPS51120
5V/3D3V

SHUTDOWN_S5
SHUTDOWN_S5
DCBATOUT
PM_SLP_S3#

Input Signal
ON3
ON5
SHDN#
SKIP#

Input Power
V+

DCBATOUT

Output Signal
PGOOD(OD / 5V)

MAX1999_PGD

Output Power
5V(O)
3D3V(O)
LDO5(O)
LDO3 (O)

5V_S5 (6A)
3D3V_S5 (4A)
MAX1999_LDO5 (30mA)
MAX1999_LDO3 (30mA)

Charger_Max8725

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

AD+

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Input Power
DCIN (I)

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

Output Power
VCC (O)
VCC (O)

AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+

(Power Team)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWER BLOCK DIAGRAM**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 40 of 58

CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz

For Dummy Phase 2

For alone test==>short C395 pin1 and pin2

VCC_CORE_S0 feedback

From KBC

(Power Team)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore 1

Size: A3 | Document Number: Bolsena-E | Rev: SA

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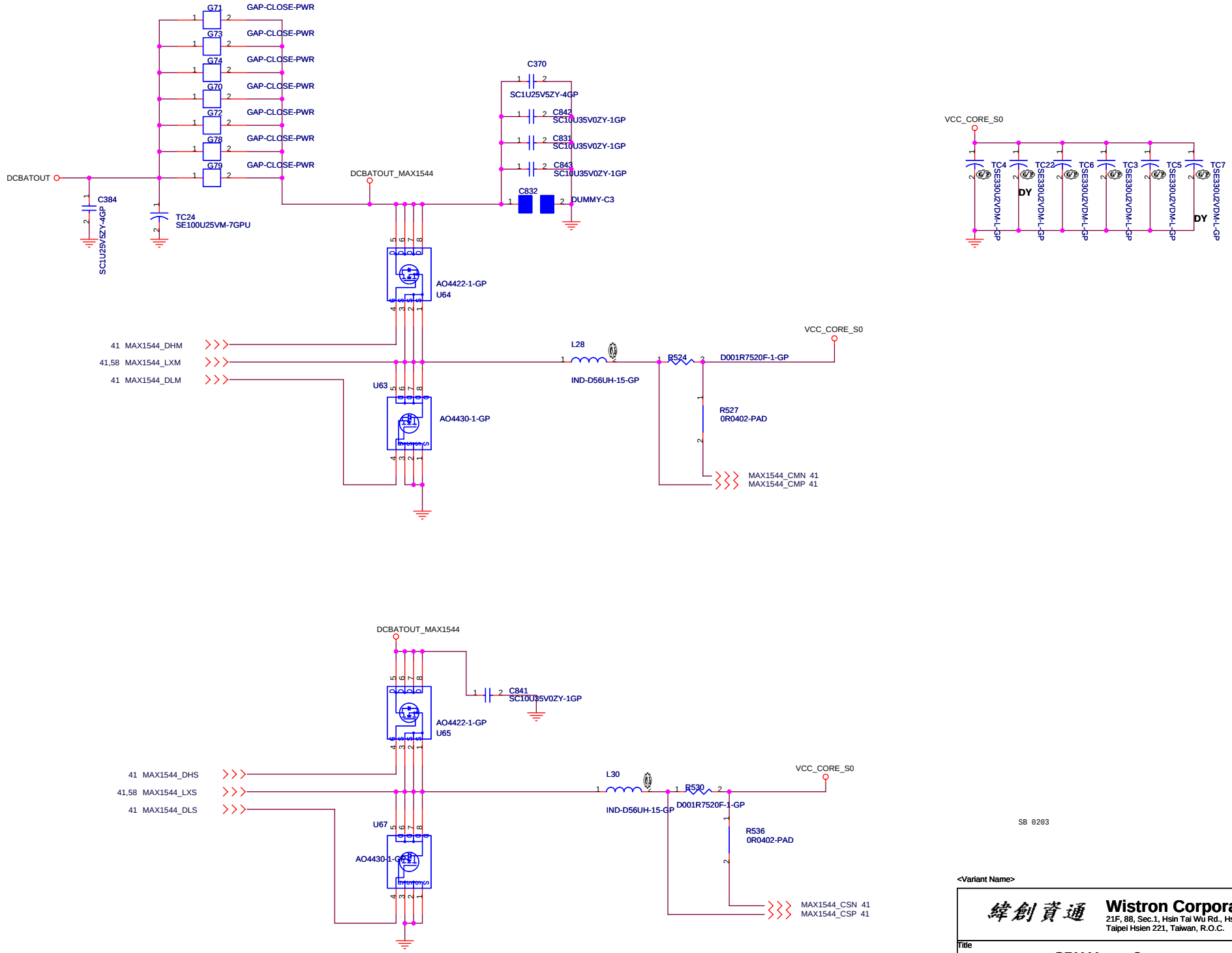

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore 2**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

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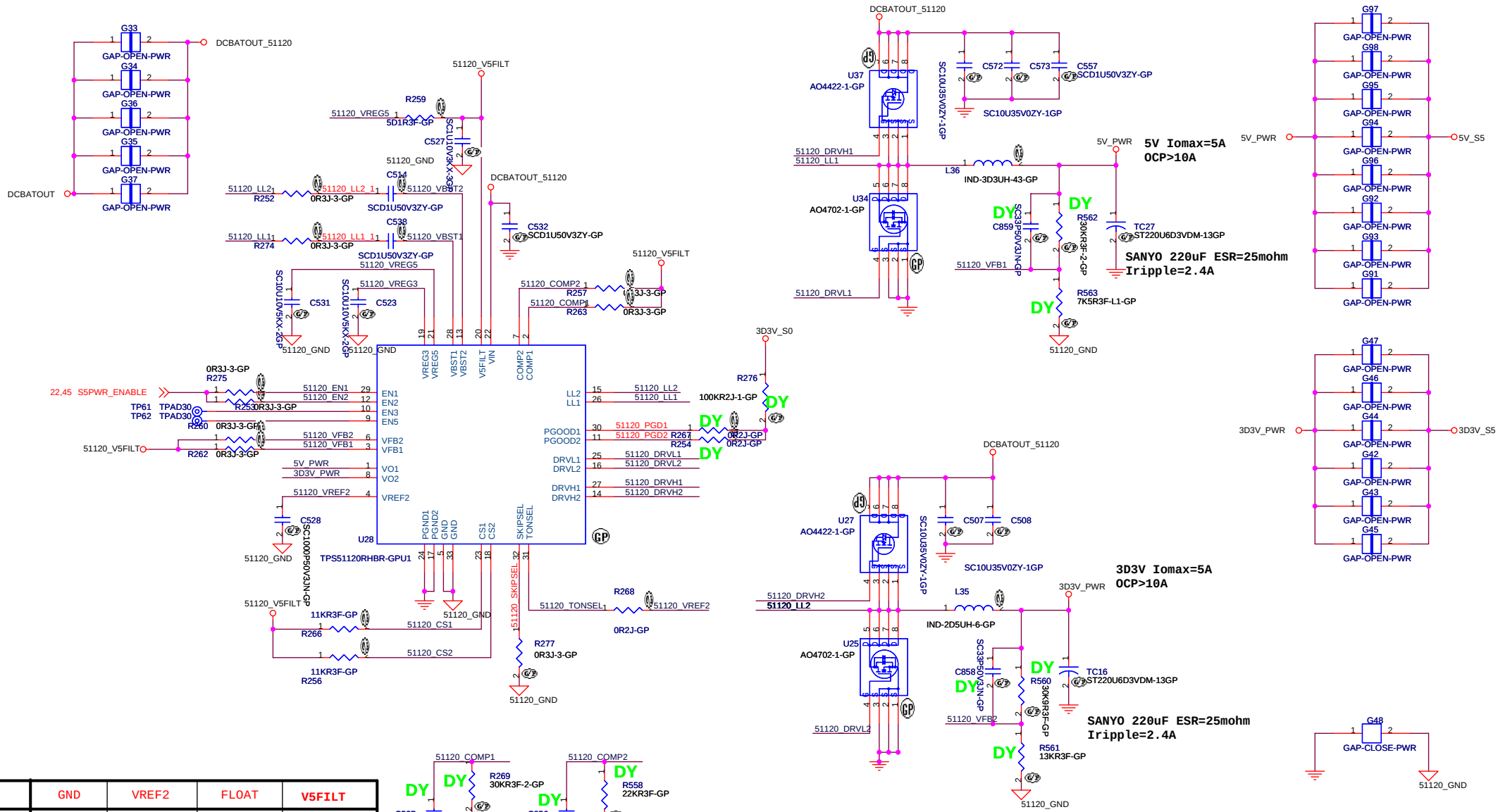

	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51120 / 3D3V / 5V

Size: A3 | Document Number: Bolsena-E | Rev: -1

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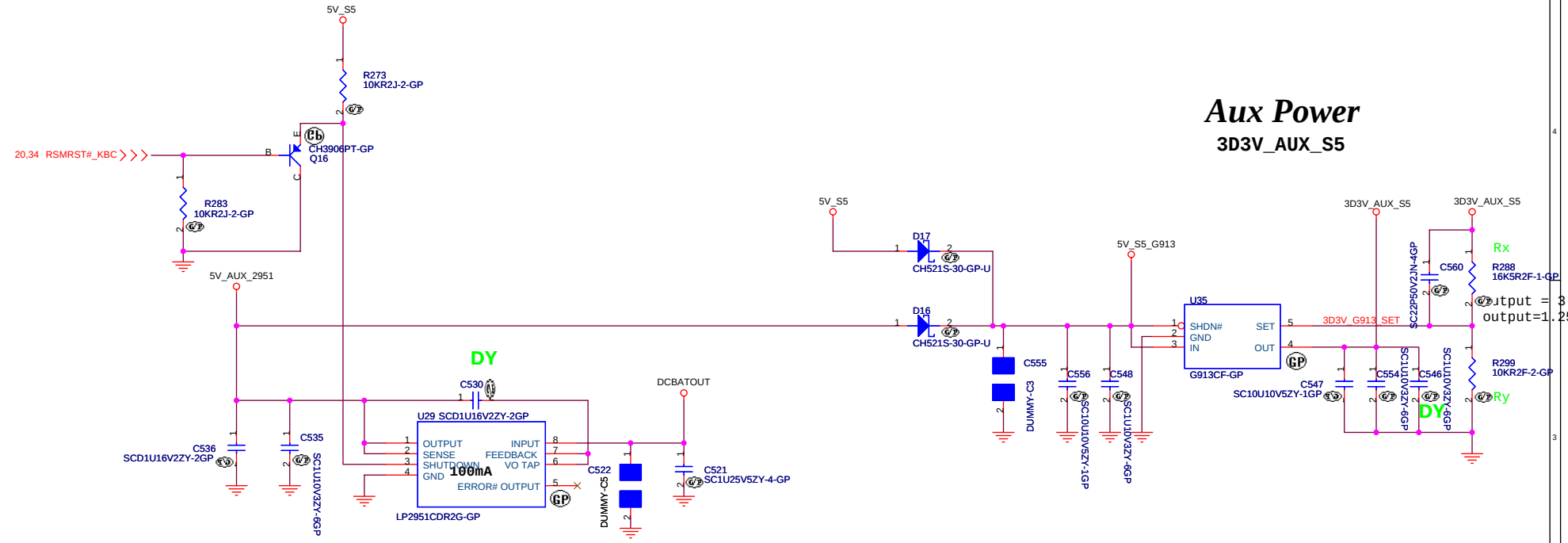
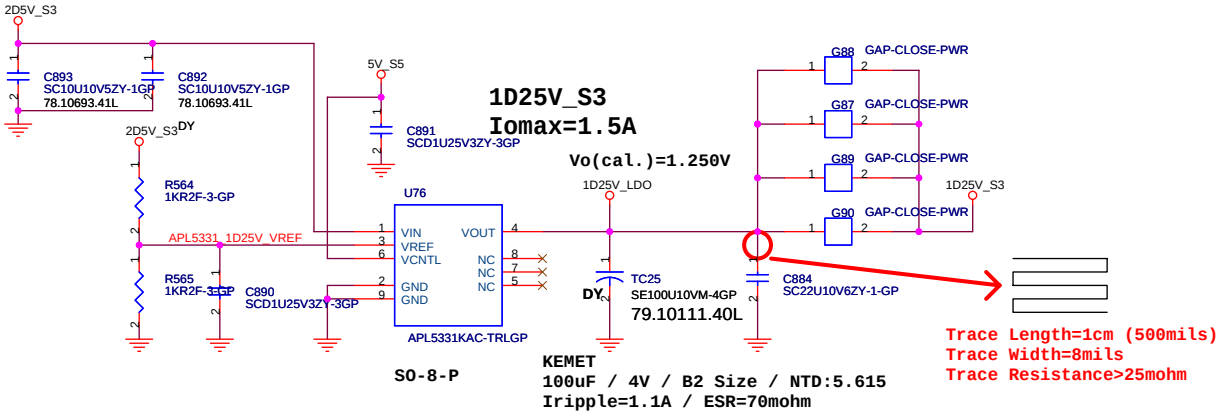
Aux Power

3D3V_AUX_S5





(Power Team)

<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D2V_S3 / 3D3V_AUX		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 44 of 58	

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

For 2.5V
SETTING=2.516V

For 1.8V
SETTING=1.8275V

For 1.2V
SETTING=1.2172V

close to IC

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

T(soft)=1.736ms

1D2V_OCP
close to IC
OCP
8.4A=>R226=13K
10A=>R226=22K

1D8V_OCP
close to IC
OCP
8.4A=>R229=12.65K
10A=>R229=22K

2D5V_OCP
close to IC
OCP
12A=>R225=18K
18A=>R225=28K

LDO SETTING

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5130 1D2V/1D8V2D5V/ (1/2)

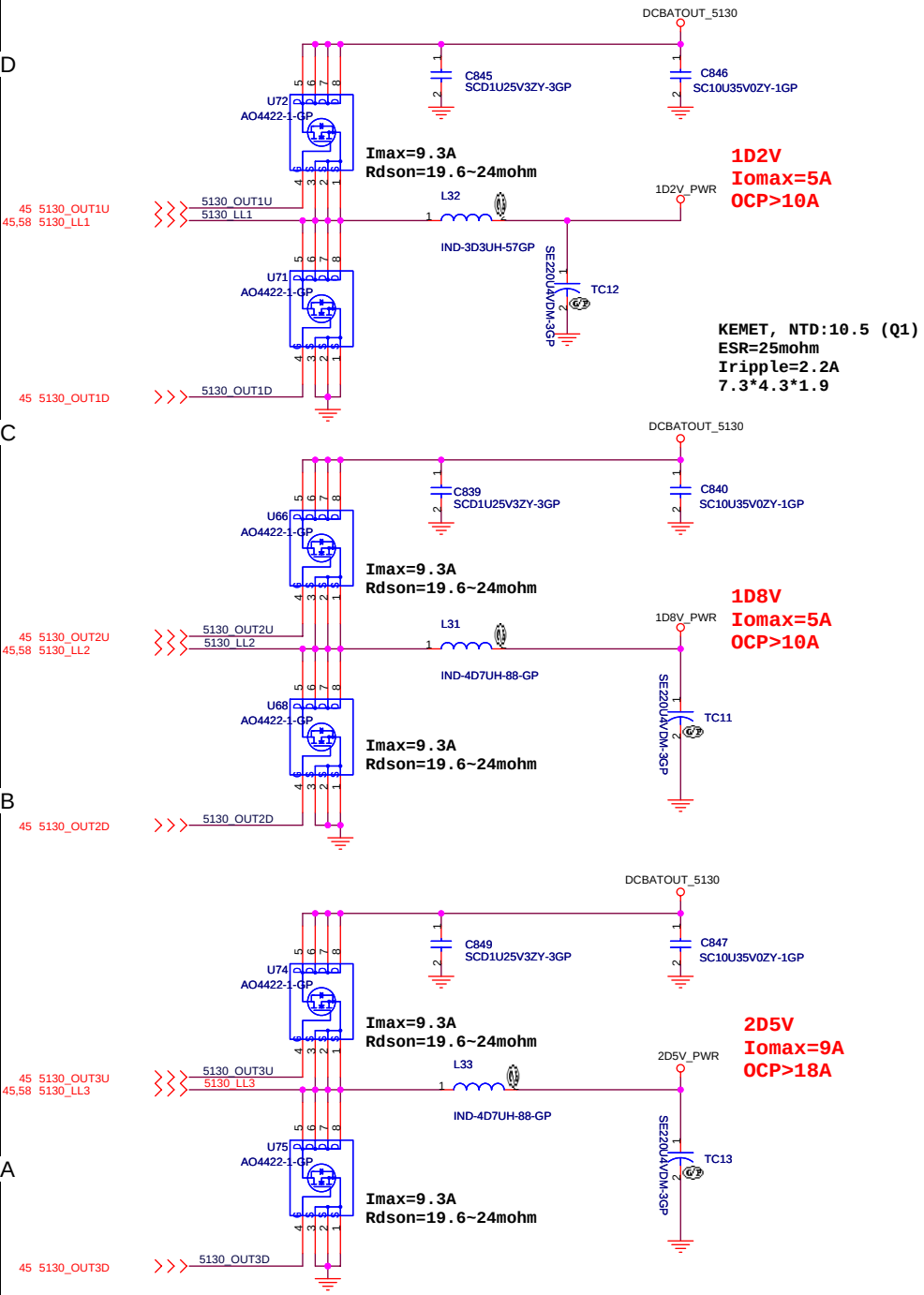
Size: A3 | Document Number: Bolsena-E | Rev: SA

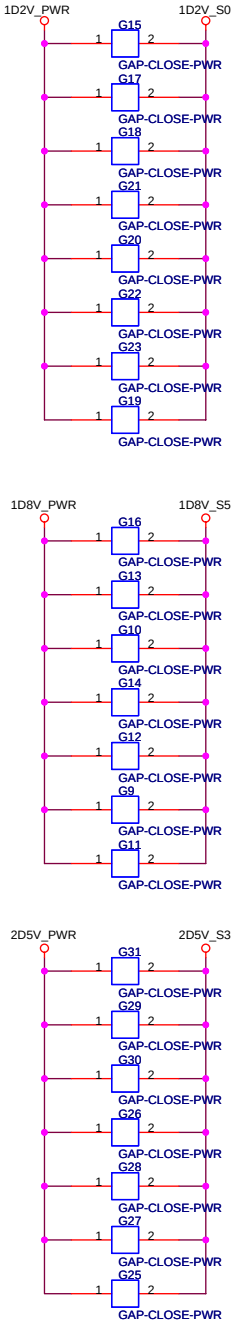
Date: Thursday, October 13, 2005 | Sheet 45 of 58

(Power Team)

TI TPS5130 for 2D5V, 1D2V, 1D8V

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)





(Power Team)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5130 1D2V/1D8V2D5V/ (2/2)**

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A3	**Bolsena-E**	SA

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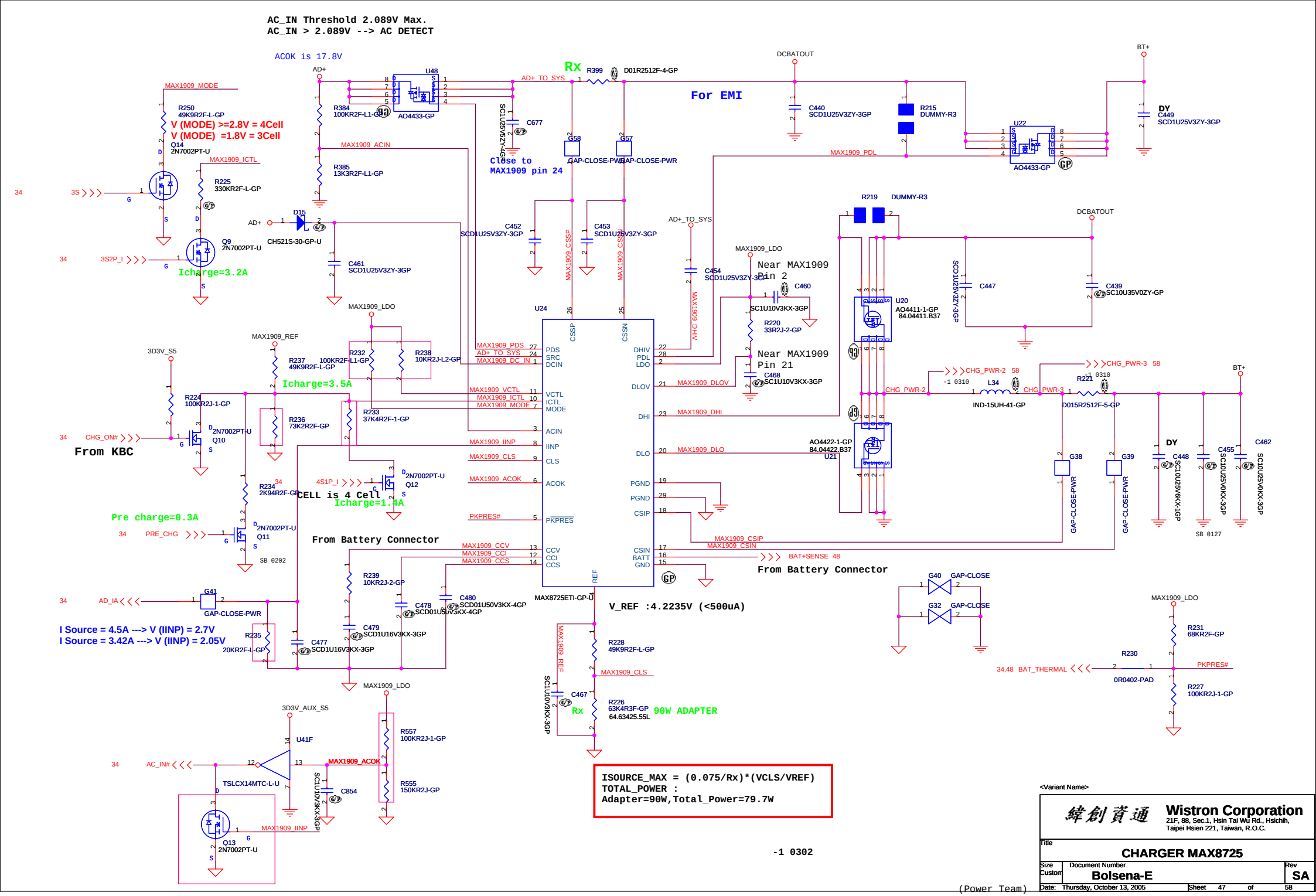
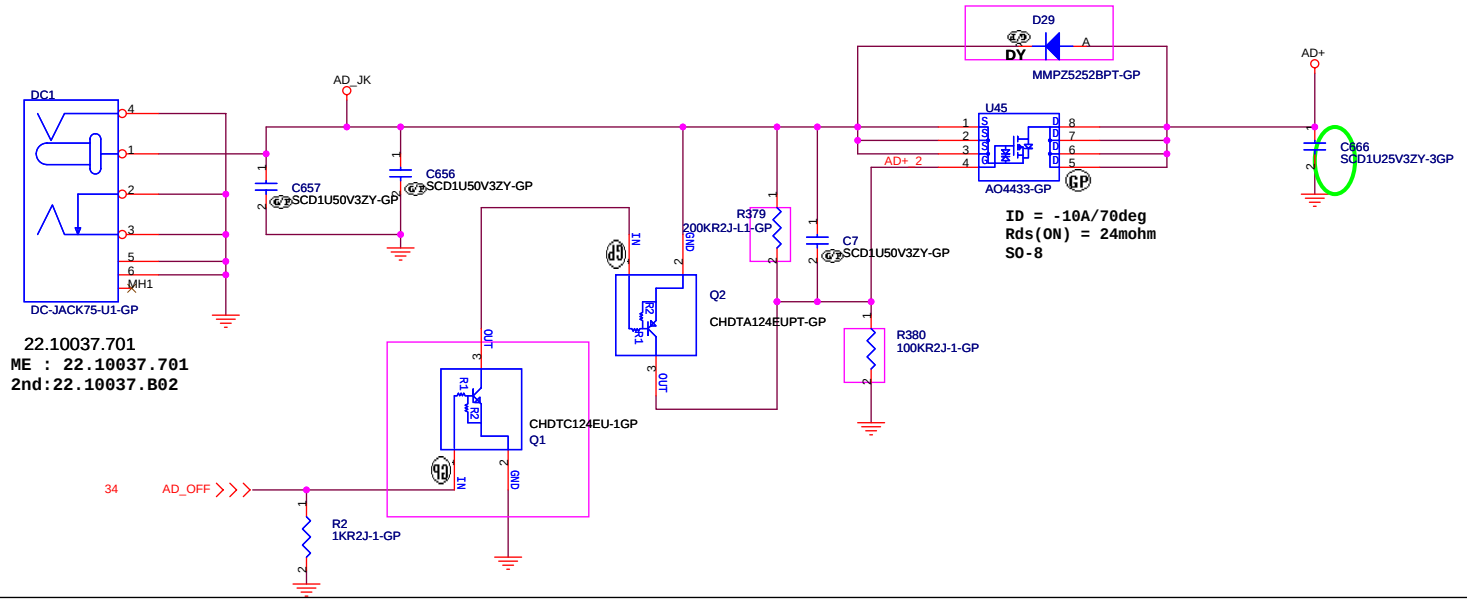
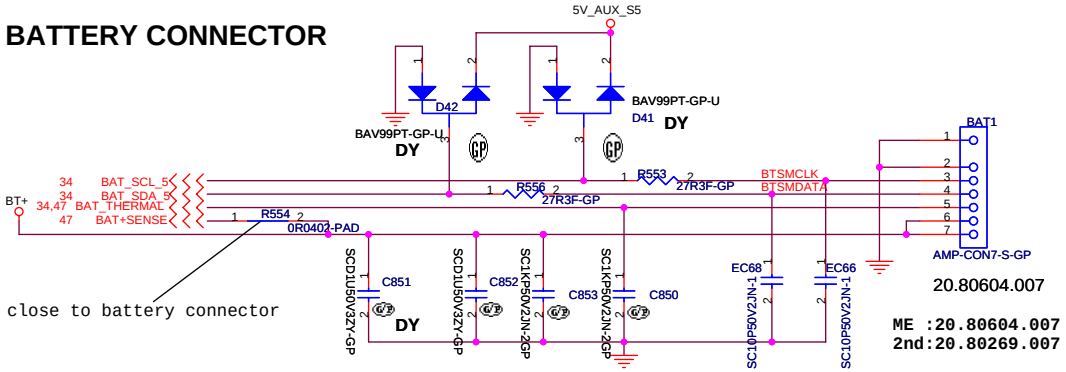

AC_IN Threshold 2.089V Max.
AC_IN > 2.089V --> AC DETECT
ACOK is 17.8V
V (MODE) >=2.8V = 4Cell
V (MODE) =1.8V = 3Cell
Close to MAX1909 pin 24
Rx
For EMI
Near MAX1909 Pin 2
Near MAX1909 Pin 21
Icharge=3.2A
Icharge=3.5A
Icharge=1.4A
Pre charge=0.3A
From KBC
From Battery Connector
From Battery Connector
CELL is 4 Cell
I Source = 4.5A ---> V (IINP) = 2.7V
I Source = 3.42A ---> V (IINP) = 2.05V
V_REF :4.2235V (<500uA)
90W ADAPTER
ISOURCE_MAX = (0.075/Rx)*(VCLS/VREF)
TOTAL_POWER :
Adapter=90W,Total_Power=79.7W
-1 0302
(Power Team)
MAX8725ETI-GP-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CHARGER MAX8725
Bolsena-E
SA
Thursday, October 13, 2005

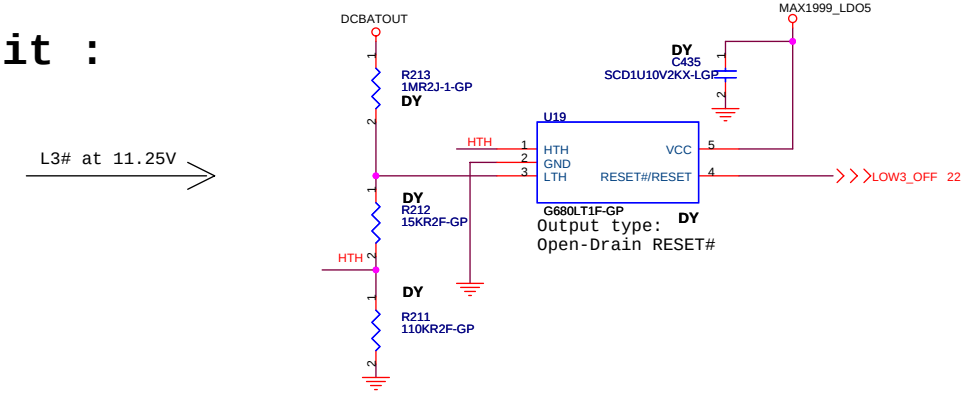
Adaptor in to generate DCBATOUT

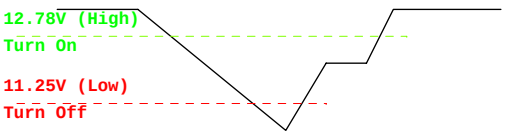


BATTERY CONNECTOR



Low3 Circuit :





<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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A3	Bolsena-E	SA

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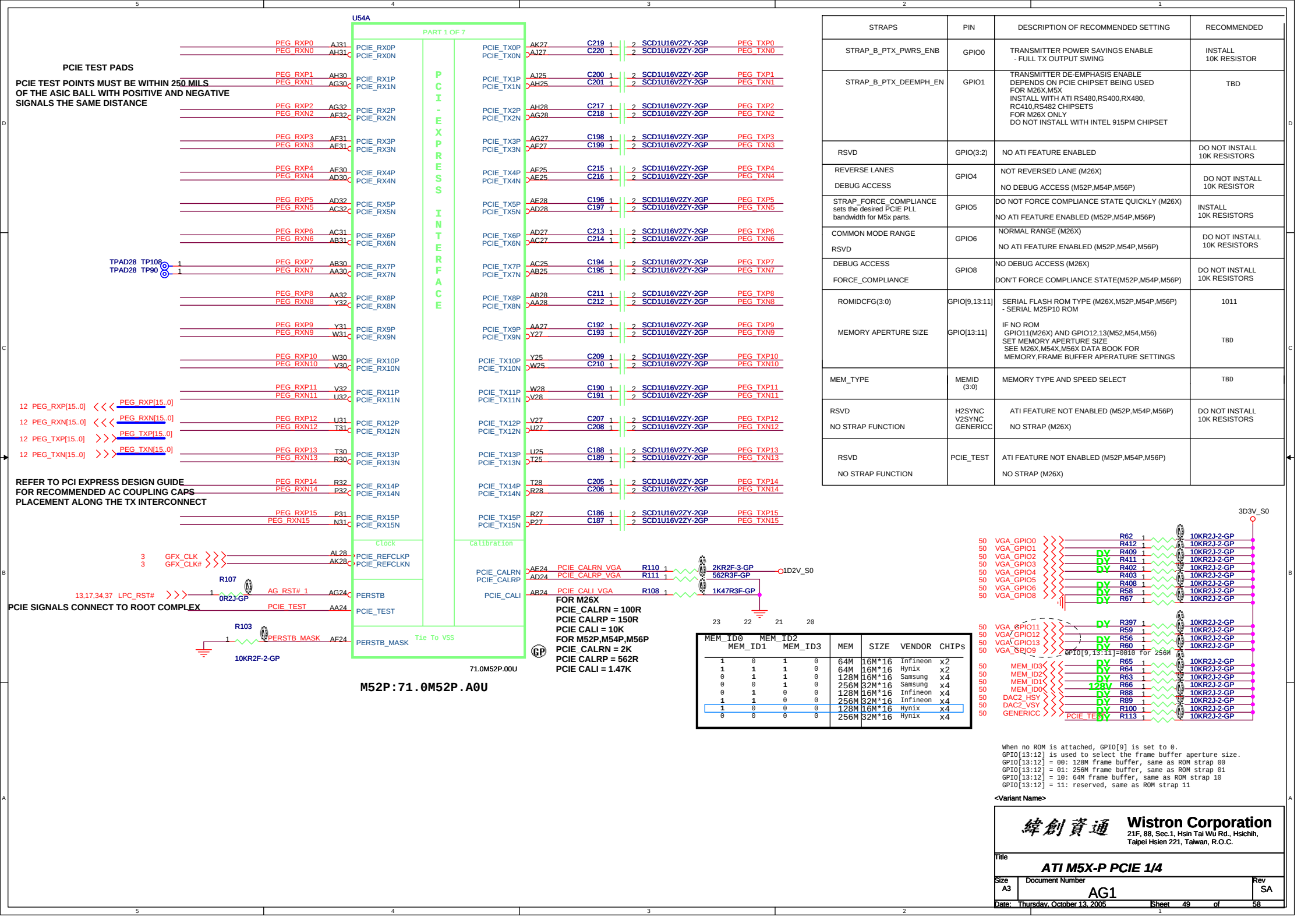

STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0) MEMORY APERTURE SIZE	GPIO[9,13:11] GPIO[13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	1011 TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPs
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P PCIE 1/4

Size: A3 | Document Number: AG1 | Rev: SA

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[USE ICS MK1726-08]

adjust SWING at 1.2v

DVPCNTL,DVPDATA[23..0] ARE CONFIGURED FOR +3.3V SIGNALING MODE ON THIS DESIGN

FOR M26X
CONNECT TO +1.8V OR VSS
TO DEFINE DVO SIGNAL LEVEL
FOR M52P,M54P,M56P
NOT CONNECTED

Modulation Rate		
SEL1	SEL0	Center Spread
L	L	+-0.5%
L	H	+-1.0%
H	L	+-1.5%
H	H	No Spread

ANY UNUSED GPIO CAN OPTIONALLY BE PANEL TYPE CONFIG STRAPS

ANY UNUSED GPIO CAN OPTIONALLY BE MEMORY TYPE CONFIG STRAPS

PLACE VREF DIVIDER AND CAP CLOSE TO ASIC

FOR M26X PVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X MPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO VDDC

VOLTAGE DIVIDER 3.3V MEM SS MODOUT TO 1.2V XTALIN/OUT

adjust SWING at 1.2v

Placed close to ASIC end.

DUAL LINK IS ONLY SUPPORTED ON M56P
DO NOT CONNECT TXM,P[3:5] WITH M52P,M54P,M26X

FOR M26X TPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X TXVDDR
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X AVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

FOR M26X VDD1DI
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

DAC2 CAN BE TV SIGNALS OR SECONDARY CRT SIGNALS AS CONTROLLED BY AN INTERNAL MUX

FOR M26X A2VDDQ
CONNECT TO +1.8V
FOR M52P,M54P,M56P
IT IS NO CONNECT

FOR M26X VDD2DI
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V

For CRT

For DVI

For THERMAL SENSOR

FOR M26X GENERICC
NO CONNECT OR
EXT SPREAD SPECTRUM INPUT
FOR M52P,M54P,M56P
IT IS GPIO

<Variant Name>

Wistron Corporation
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Title: ATI M5X-P IO 2/4

Size: A3 | Document Number: Bolsena-E | Rev: SA

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U54C

Part 3 of 7

MEMORY INTERFACE A

DQA_0 DQA_1 DQA_2 DQA_3 DQA_4 DQA_5 DQA_6 DQA_7 DQA_8 DQA_9 DQA_10 DQA_11 DQA_12 DQA_13 DQA_14 DQA_15 DQA_16 DQA_17 DQA_18 DQA_19 DQA_20 DQA_21 DQA_22 DQA_23 DQA_24 DQA_25 DQA_26 DQA_27 DQA_28 DQA_29 DQA_30 DQA_31 DQA_32 DQA_33 DQA_34 DQA_35 DQA_36 DQA_37 DQA_38 DQA_39 DQA_40 DQA_41 DQA_42 DQA_43 DQA_44 DQA_45 DQA_46 DQA_47 DQA_48 DQA_49 DQA_50 DQA_51 DQA_52 DQA_53 DQA_54 DQA_55 DQA_56 DQA_57 DQA_58 DQA_59 DQA_60 DQA_61 DQA_62 DQA_63

MVREFD_0 MVREFS_0

MAA_0 MAA_1 MAA_2 MAA_3 MAA_4 MAA_5 MAA_6 MAA_7 MAA_8 MAA_9 MAA_10 MAA_11 MAA_12 MAA_13 MAA_14 MAA_15

DQMAb_0 DQMAb_1 DQMAb_2 DQMAb_3 DQMAb_4 DQMAb_5 DQMAb_6 DQMAb_7

read strobe: QSA_0 QSA_1 QSA_2 QSA_3 QSA_4 QSA_5 QSA_6 QSA_7

write strobe: QSA_0B QSA_1B QSA_2B QSA_3B QSA_4B QSA_5B QSA_6B QSA_7B

ODTA ODTA1

CLKA0 CLKA0b

CKEA0

RASA0b

CASA0b

WEA0b

CSA0b_0 CSA0b_1

CLKA1 CLKA1b

CKEA1

RASA1b

CASA1b

WEA1b

CSA1b_0 CSA1b_1

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

Ch-A
FOR M52P,M54P,M26X
PIN B25 IS MA12 (BA0)
PIN C25 IS MA13 (BA1)
PIN E29 IS MA15 (BA2)
PIN E27 IS MA14
FOR M56P
PIN B25 IS MA14 (BA0)
PIN C25 IS MA15 (BA1)
PIN E29 IS MA13 (BA2)
PIN E27 IS MA12

1D8V_S0

R71 100R2F-L1-GP-U

R72 100R2F-L1-GP-U

C90 SCD1U16V2KX-1GP

MVREFD1 MVREFS1

MEM_RST

1D8V_S0

R49 100R2F-L1-GP-U

R55 100R2F-L1-GP-U

C75 SCD1U16V2KX-1GP

RN10 SRN4K7J-6-GP

PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC

U54D

Part 4 of 7

MEMORY INTERFACE B

MDB0 MDB1 MDB2 MDB3 MDB4 MDB5 MDB6 MDB7 MDB8 MDB9 MDB10 MDB11 MDB12 MDB13 MDB14 MDB15 MDB16 MDB17 MDB18 MDB19 MDB20 MDB21 MDB22 MDB23 MDB24 MDB25 MDB26 MDB27 MDB28 MDB29 MDB30 MDB31 MDB32 MDB33 MDB34 MDB35 MDB36 MDB37 MDB38 MDB39 MDB40 MDB41 MDB42 MDB43 MDB44 MDB45 MDB46 MDB47 MDB48 MDB49 MDB50 MDB51 MDB52 MDB53 MDB54 MDB55 MDB56 MDB57 MDB58 MDB59 MDB60 MDB61 MDB62 MDB63

DQB_0 DQB_1 DQB_2 DQB_3 DQB_4 DQB_5 DQB_6 DQB_7 DQB_8 DQB_9 DQB_10 DQB_11 DQB_12 DQB_13 DQB_14 DQB_15 DQB_16 DQB_17 DQB_18 DQB_19 DQB_20 DQB_21 DQB_22 DQB_23 DQB_24 DQB_25 DQB_26 DQB_27 DQB_28 DQB_29 DQB_30 DQB_31 DQB_32 DQB_33 DQB_34 DQB_35 DQB_36 DQB_37 DQB_38 DQB_39 DQB_40 DQB_41 DQB_42 DQB_43 DQB_44 DQB_45 DQB_46 DQB_47 DQB_48 DQB_49 DQB_50 DQB_51 DQB_52 DQB_53 DQB_54 DQB_55 DQB_56 DQB_57 DQB_58 DQB_59 DQB_60 DQB_61 DQB_62 DQB_63

MVREFD_1 MVREFS_1

DRAM_RST TEST_MCLK TEST_YCLK MEMTEST

MAB_0 MAB_1 MAB_2 MAB_3 MAB_4 MAB_5 MAB_6 MAB_7 MAB_8 MAB_9 MAB_10 MAB_11 MAB_12 MAB_13 MAB_14 MAB_15

DQMBb_0 DQMBb_1 DQMBb_2 DQMBb_3 DQMBb_4 DQMBb_5 DQMBb_6 DQMBb_7

rbad strobe: QSB_0 QSB_1 QSB_2 QSB_3 QSB_4 QSB_5 QSB_6 QSB_7

write strobe: QSB_0B QSB_1B QSB_2B QSB_3B QSB_4B QSB_5B QSB_6B QSB_7B

ODTB ODTB1

CLKB0 CLKB0b

CKEB0

RASB0b

CASB0b

WEB0b

CSB0b_0 CSB0b_1

CLKB1 CLKB1b

CKEB1

RASB1b

CASB1b

WEB1b

CSB1b_0 CSB1b_1

Ch-B
FOR M52P,M54P,M26X
PIN H2 IS MAB12 (BA0)
PIN H3 IS MAB13 (BA1)
PIN D5 IS MAB15 (BA2)
PIN F5 IS MAB14
FOR M56P
PIN H2 IS MA14 (BA0)
PIN H3 IS MA15 (BA1)
PIN D5 IS MA13 (BA2)
PIN F5 IS MAB12

MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11

MAB12_14_54,55 TP8 TPAD28

B_BA0 54,55
B_BA1 54,55

DQMB#0 DQMB#1 DQMB#2 DQMB#3 DQMB#4 DQMB#5 DQMB#6 DQMB#7

RDQSB0 RDQSB1 RDQSB2 RDQSB3 RDQSB4 RDQSB5 RDQSB6 RDQSB7

For GDDR2

WDQSB0 WDQSB1 WDQSB2 WDQSB3 WDQSB4 WDQSB5 WDQSB6 WDQSB7

ODTB0 54
ODTB1 54,55

CLKB0 CLKB0#

CKEB0

RASB0#

CASB0#

WEB0#

CSB0_0# CSB1_1# TP81 TPAD28

CLKB1 CLKB1#

CKEB1

RASB1#

CASB1#

WEB1#

CSB1_0# CSB1_1# TP4 TPAD28

54 RASB0# RASB1#
54,55 RASB0# RASB1#

54 CASB0# CASB1#
54,55 CASB0# CASB1#

54 WEB0# WEB1#
54,55 WEB0# WEB1#

54 CSB0_0#
54,55 CSB1_0#

CSB0_0#
CSB1_0#

54 CKEB0 CKEB1
54,55 CKEB0 CKEB1

54 CLKB0 CLKB0#
54 CLKB0 CLKB0#

55 CLKB1 CLKB1#
55 CLKB1 CLKB1#

54,55 RDQSB[7..0]
54,55 DQMB#[7..0]
54,55 MDB[63..0]
54,55 MAB[11..0]
54,55 WDQSB[7..0]

RDQSB[7..0]
DQMB#[7..0]
MDB[63..0]
MAB[11..0]
WDQSB[7..0]

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: ATI M5X-P MEM 3/4

Size: A3 | Document Number: Bolsena-E | Rev: SA

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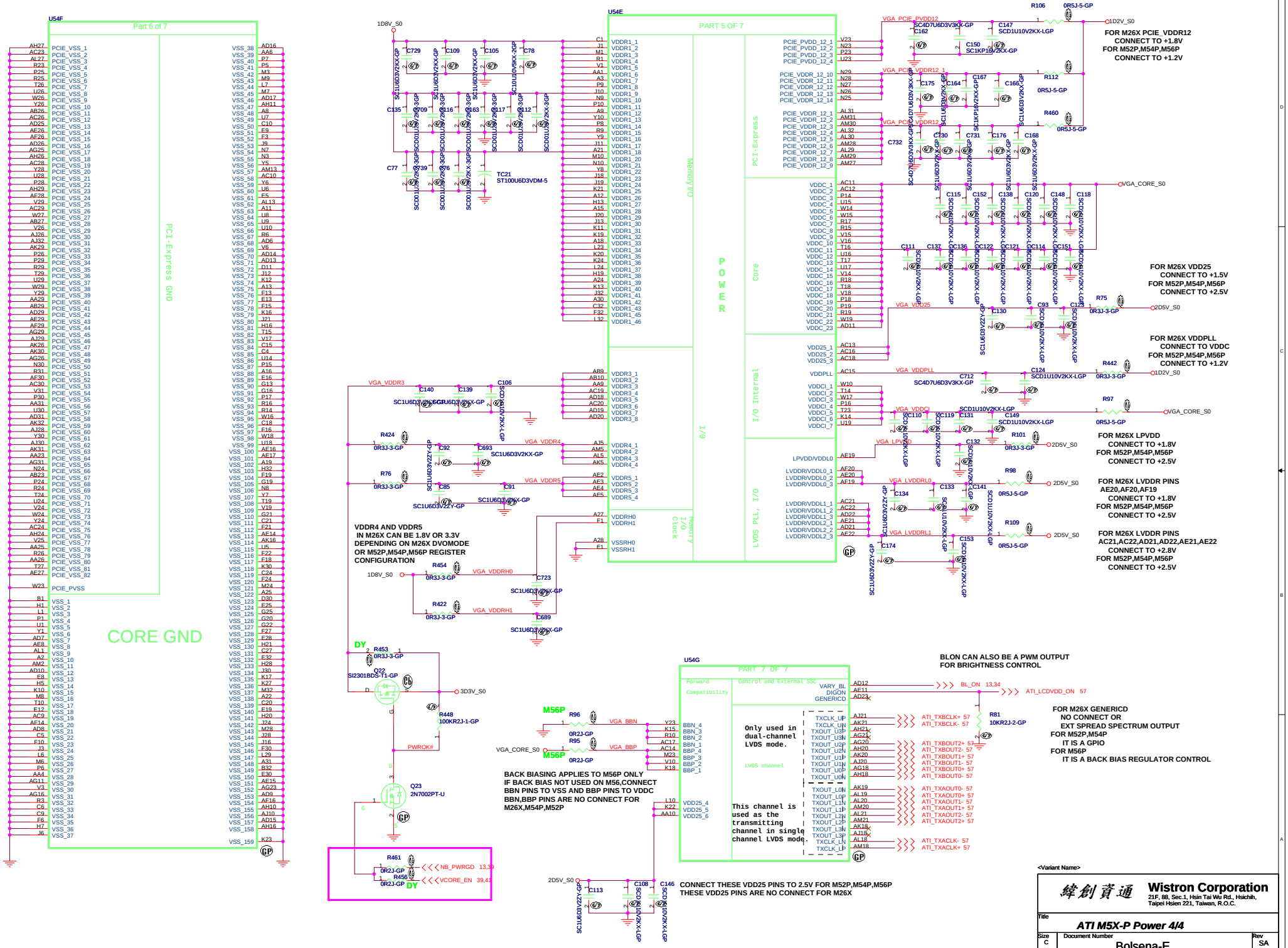
U54F
Part 6 of 7
PCIE_VSS_1
PCIE_VSS_2
PCIE_VSS_3
PCIE_VSS_4
PCIE_VSS_5
PCIE_VSS_6
PCIE_VSS_7
PCIE_VSS_8
PCIE_VSS_9
PCIE_VSS_10
PCIE_VSS_11
PCIE_VSS_12
PCIE_VSS_13
PCIE_VSS_14
PCIE_VSS_15
PCIE_VSS_16
PCIE_VSS_17
PCIE_VSS_18
PCIE_VSS_19
PCIE_VSS_20
PCIE_VSS_21
PCIE_VSS_22
PCIE_VSS_23
PCIE_VSS_24
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PCIE_VSS_26
PCIE_VSS_27
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PCIE_VSS_72
PCIE_VSS_73
PCIE_VSS_74
PCIE_VSS_75
PCIE_VSS_76
PCIE_VSS_77
PCIE_VSS_78
PCIE_VSS_79
PCIE_VSS_80
PCIE_VSS_81
PCIE_VSS_82
PCIE_PVSS
PCI-Express GND
CORE GND
U54E
PART 5 OF 7
VDDR1_1
VDDR1_2
VDDR1_3
VDDR1_4
VDDR1_5
VDDR1_6
VDDR1_7
VDDR1_8
VDDR1_9
VDDR1_10
VDDR1_11
VDDR1_12
VDDR1_13
VDDR1_14
VDDR1_15
VDDR1_16
VDDR1_17
VDDR1_18
VDDR1_19
VDDR1_20
VDDR1_21
VDDR1_22
VDDR1_23
VDDR1_24
VDDR1_25
VDDR1_26
VDDR1_27
VDDR1_28
VDDR1_29
VDDR1_30
VDDR1_31
VDDR1_32
VDDR1_33
VDDR1_34
VDDR1_35
VDDR1_36
VDDR1_37
VDDR1_38
VDDR1_39
VDDR1_40
VDDR1_41
VDDR1_42
VDDR1_43
VDDR1_45
VDDR1_46
Memory I/O
PCIE_PVDD_12_1
PCIE_PVDD_12_2
PCIE_PVDD_12_3
PCIE_PVDD_12_4
PCIE_VDDR_12_10
PCIE_VDDR_12_11
PCIE_VDDR_12_12
PCIE_VDDR_12_13
PCIE_VDDR_12_14
PCIE_VDDR_12_1
PCIE_VDDR_12_2
PCIE_VDDR_12_3
PCIE_VDDR_12_4
PCIE_VDDR_12_5
PCIE_VDDR_12_6
PCIE_VDDR_12_7
PCIE_VDDR_12_8
PCIE_VDDR_12_9
PCI-Express
VDDC_1
VDDC_2
VDDC_3
VDDC_4
VDDC_5
VDDC_6
VDDC_7
VDDC_8
VDDC_9
VDDC_10
VDDC_11
VDDC_12
VDDC_13
VDDC_14
VDDC_15
VDDC_16
VDDC_17
VDDC_18
VDDC_19
VDDC_20
VDDC_21
VDDC_22
VDDC_23
Core
POWER
VDD25_1
VDD25_2
VDD25_3
VDDPLL
VDDCI_1
VDDCI_2
VDDCI_3
VDDCI_4
VDDCI_5
VDDCI_6
VDDCI_7
I/O Internal
LPVDD/VDDL0
LVDDR/VDDL0_1
LVDDR/VDDL0_2
LVDDR/VDDL0_3
LVDDR/VDDL1_1
LVDDR/VDDL1_2
LVDDR/VDDL1_3
LVDDR/VDDL2_1
LVDDR/VDDL2_2
LVDDR/VDDL2_3
LVDS PLL, I/O
VDDR3_1
VDDR3_2
VDDR3_3
VDDR3_4
VDDR3_5
VDDR3_6
VDDR3_7
VDDR3_8
VDDR4_1
VDDR4_2
VDDR4_3
VDDR4_4
VDDR5_1
VDDR5_2
VDDR5_3
VDDR5_4
VDDRH0
VDDRH1
VSSRH0
VSSRH1
Memory I/O Clock
U54G
PART 7 OF 7
Forward Compatibility
Control and External SSC
VARY_BL
DIGON
GENERICD
Only used in dual-channel LVDS mode.
LVDS channel
This channel is used as the transmitting channel in single channel LVDS mode.
TXCLK_UP
TXCLK_UN
TXOUT_U3P
TXOUT_U3N
TXOUT_U2P
TXOUT_U2N
TXOUT_U1P
TXOUT_U1N
TXOUT_U0P
TXOUT_U0N
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
BBN_4
BBN_3
BBN_2
BBN_1
BBP_4
BBP_3
BBP_2
BBP_1
VDD25_4
VDD25_5
VDD25_6
1D8V_S0
VGA_PCIE_PVDD12
VGA_PCIE_VDDR12_1
VGA_PCIE_VDDR12
VGA_CORE_S0
VGA_VDD25
VGA_VDDPLL
VGA_VDDCI
VGA_LPVDD
VGA_LVDDRL0
VGA_LVDDRL1
VGA_VDDR3
VGA_VDDR4
VGA_VDDR5
VGA_VDDRH0
VGA_VDDRH1
1D2V_S0
2D5V_S0
3D3V_S0
VGA_BBN
VGA_BBP
ATI_TXBCLK+ 57
ATI_TXBCLK- 57
ATI_TXBOUT2+ 57
ATI_TXBOUT2- 57
ATI_TXBOUT1+ 57
ATI_TXBOUT1- 57
ATI_TXBOUT0+ 57
ATI_TXBOUT0- 57
ATI_TXAOUT0- 57
ATI_TXAOUT0+ 57
ATI_TXAOUT1- 57
ATI_TXAOUT1+ 57
ATI_TXAOUT2- 57
ATI_TXAOUT2+ 57
ATI_TXACLK- 57
ATI_TXACLK+ 57
BL_ON 13,34
ATI_LCDVDD_ON 57
NB_PWRGD 13,39
VCORE_EN 39,41
PWROK#
TC21
ST100U6D3VDM-5
Q22
SI2301BDS-T1-GP
Q23
2N7002PT-U
M56P
DY
FOR M26X PCIE_VDDR12
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +1.2V
FOR M26X VDD25
CONNECT TO +1.5V
FOR M52P,M54P,M56P
CONNECT TO +2.5V
FOR M26X VDDPLL
CONNECT TO VDDC
FOR M52P,M54P,M56P
CONNECT TO +1.2V
FOR M26X LPVDD
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V
FOR M26X LVDDR PINS
AE20,AF20,AF19
CONNECT TO +1.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V
FOR M26X LVDDR PINS
AC21,AC22,AD21,AD22,AE21,AE22
CONNECT TO +2.8V
FOR M52P,M54P,M56P
CONNECT TO +2.5V
VDDR4 AND VDDR5
IN M26X CAN BE 1.8V OR 3.3V
DEPENDING ON M26X DVOMODE
OR M52P,M54P,M56P REGISTER
CONFIGURATION
BACK BIASING APPLIES TO M56P ONLY
IF BACK BIAS NOT USED ON M56,CONNECT
BBN PINS TO VSS AND BBP PINS TO VDDC
BBN,BBP PINS ARE NO CONNECT FOR
M26X,M54P,M52P
CONNECT THESE VDD25 PINS TO 2.5V FOR M52P,M54P,M56P
THESE VDD25 PINS ARE NO CONNECT FOR M26X
BLON CAN ALSO BE A PWM OUTPUT
FOR BRIGHTNESS CONTROL
FOR M26X GENERICD
NO CONNECT OR
EXT SPREAD SPECTRUM OUTPUT
FOR M52P,M54P
IT IS A GPIO
FOR M56P
IT IS A BACK BIAS REGULATOR CONTROL
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI M5X-P Power 4/4
Size C
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
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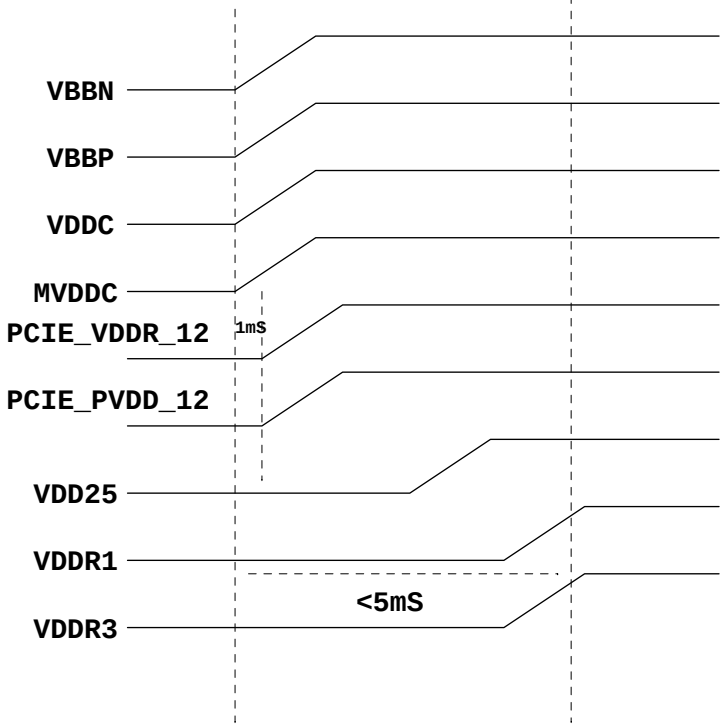
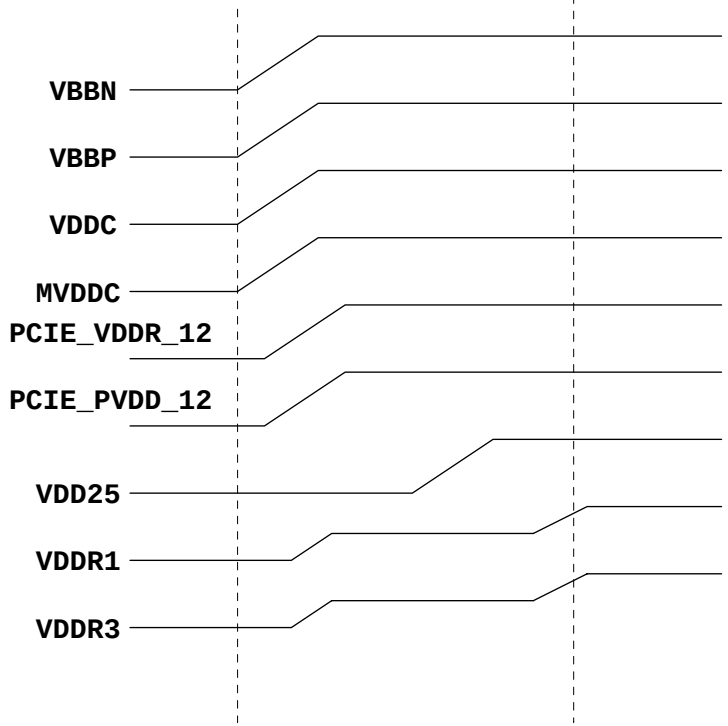
Ideal Power Up Sequence



Real Power Up Sequence



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

General Guidelines:
• BBN and BBP must ramp up before or at the same time as VDDC but not after.
• VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).
• All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).
• VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
• The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).

The real power up sequence will appear as follows:

Figure 2-2. Real Power Up Sequence

As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

<Variant Name>

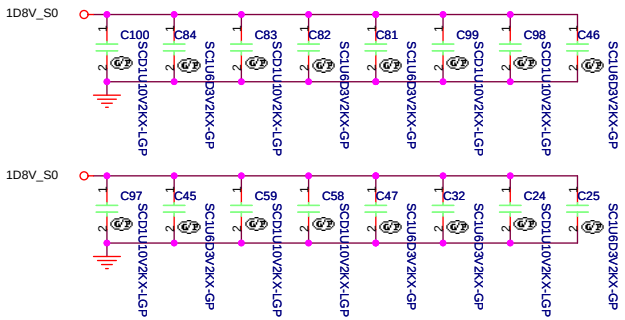
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

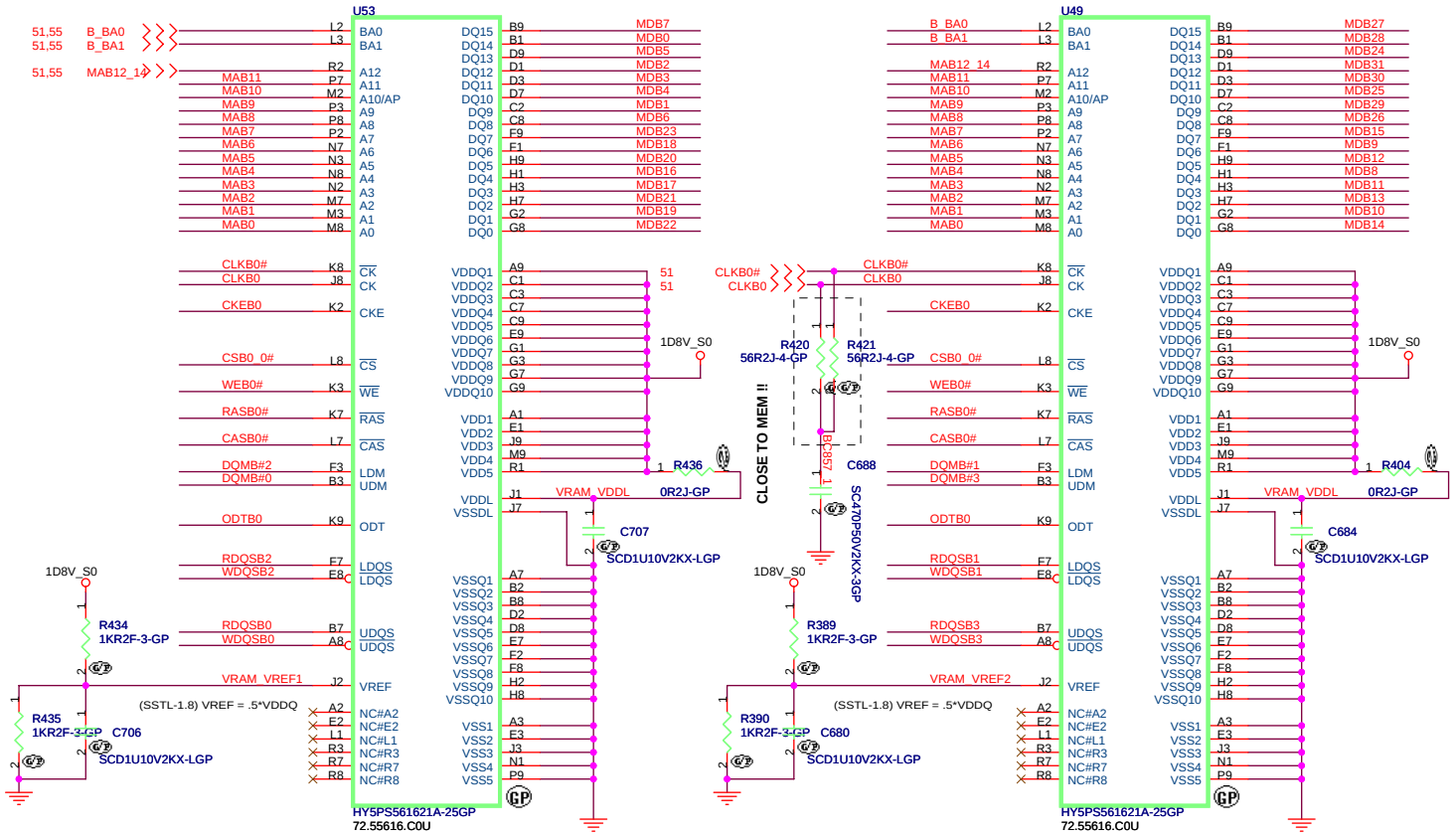
Title: ***ATI M5X-P POWER SEQUENCE***

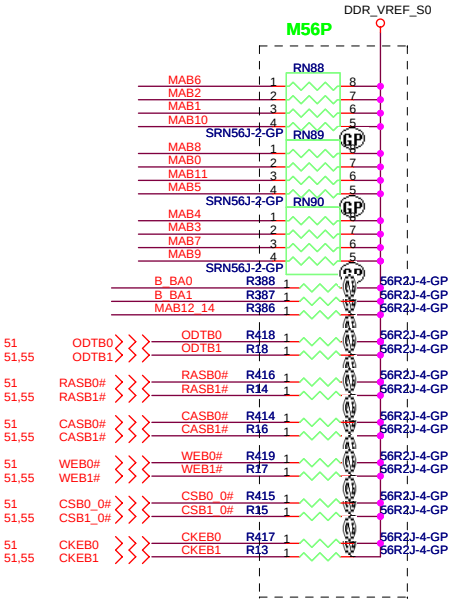
Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 53 of 58

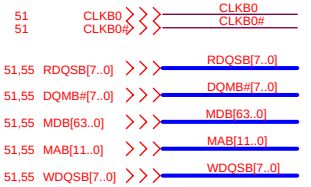
CHAN B DDR2 84BGA 32MX16 MEMORY







FOR M56P AT DDR2 MEMORY SPEEDS ABOVE 350MHZ MEMORY CONTROL SIGNALS WE,CAS,RAS,CS,CKE,ODT AND MEMORY ADDRESS SIGNALS REQUIRE 55 OHM PULLUP TO A VTT RAIL (50% OF VDDQ)



72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 400Mhz)
72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***VRAM 1/2***

Size	Document Number	Rev
A3	Bolsena-E	SA

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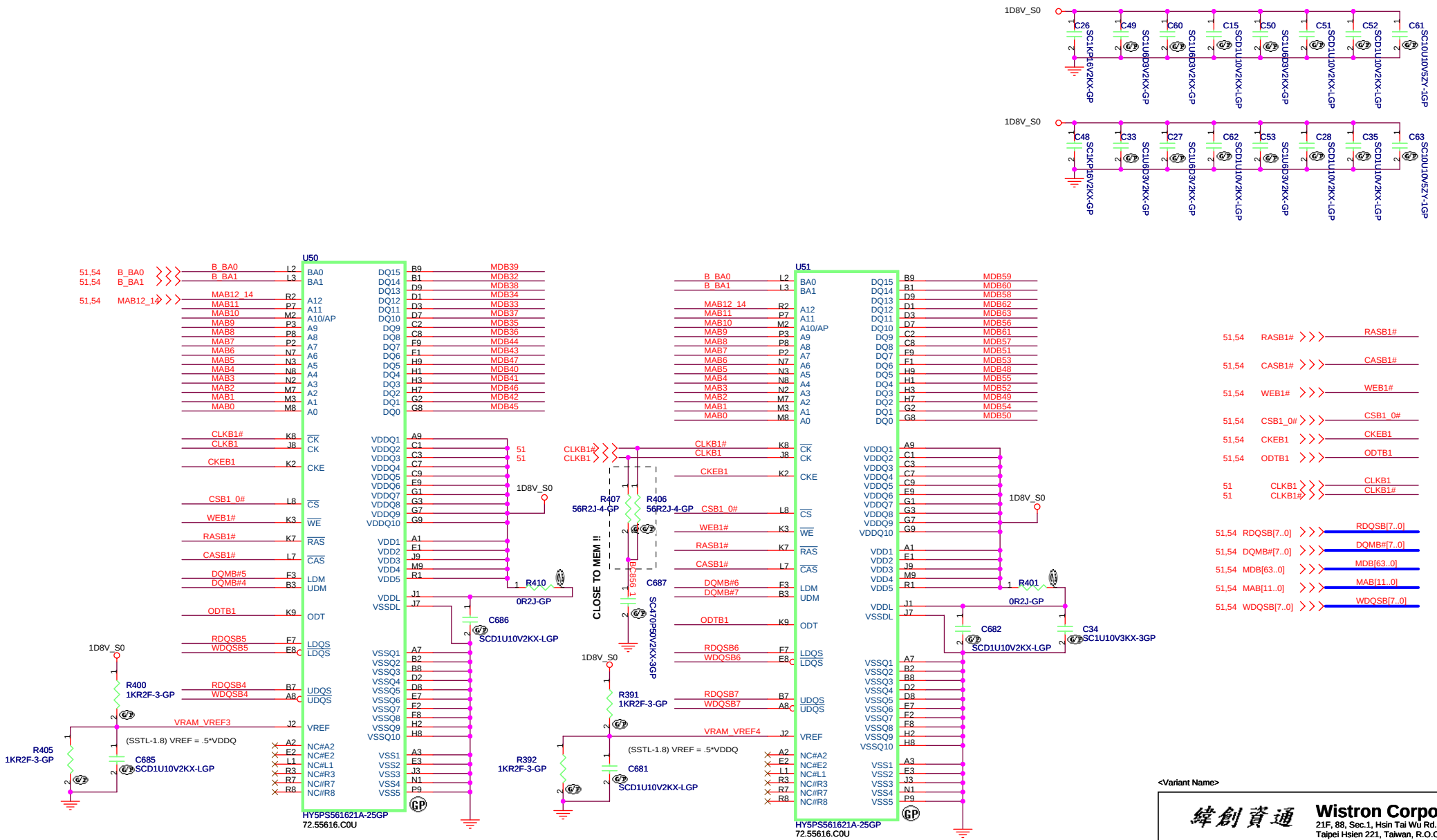

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VRAM 2/2**

Size	Document Number	Rev
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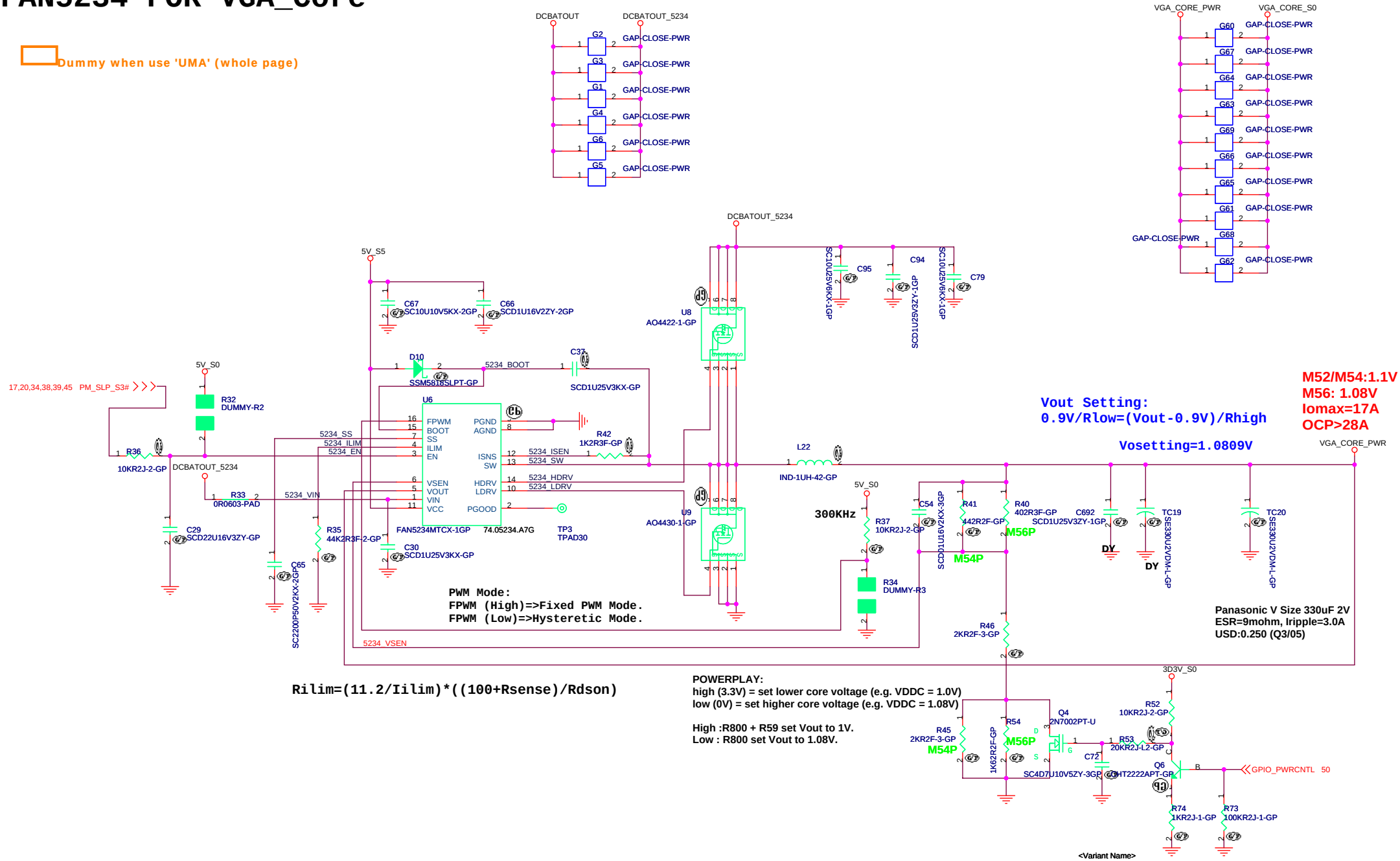
FAN5234 FOR VGA_Core

Dummy when use 'UMA' (whole page)



Vout Setting:
0.9V/Rlow=(Vout-0.9V)/Rhigh

Vosetting=1.0809V

M52/M54:1.1V
M56: 1.08V
Iomax=17A
OCP>28A

PWM Mode:
FPWM (High)=>Fixed PWM Mode.
FPWM (Low)=>Hysteretic Mode.

Rilim=(11.2/Iilim)*((100+Rsense)/Rdson)

POWERPLAY:
high (3.3V) = set lower core voltage (e.g. VDDC = 1.0V)
low (0V) = set higher core voltage (e.g. VDDC = 1.08V)

High :R800 + R59 set Vout to 1V.
Low : R800 set Vout to 1.08V.

Panasonic V Size 330uF 2V
ESR=9mohm, Iripple=3.0A
USD:0.250 (Q3/05)

(Power Team)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **VGA CORE 1D1V**

Size	Document Number	Rev
A3	**Bolsena-E**	SA

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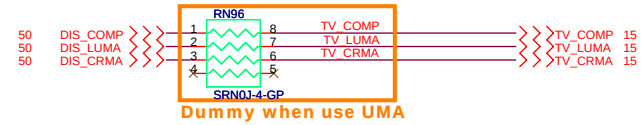
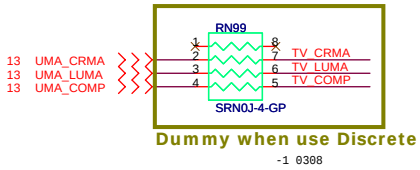
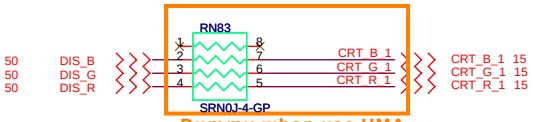
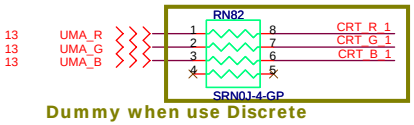
TV SWITCH

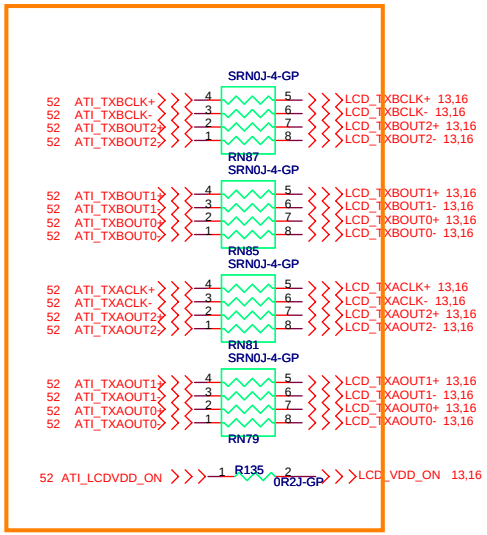
Function	S
A to B0	L
A to B1	H











<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA SELECTOR

Size: A3 | Document Number: Bolsena-E | Rev: SA

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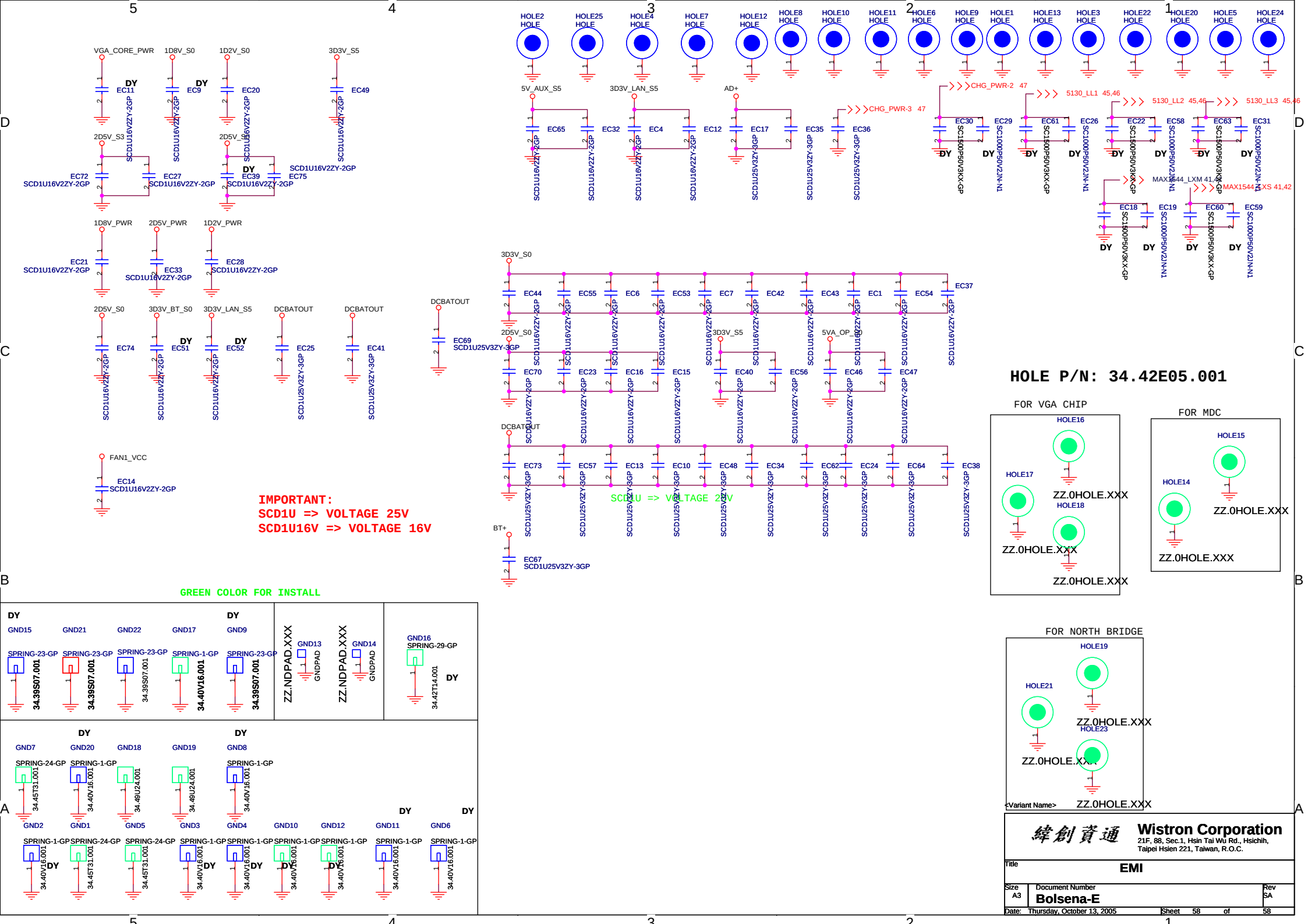
VGA_CORE_PWR
1D8V_S0
1D2V_S0
3D3V_S5
EC11
EC9
EC20
EC49
2D5V_S3
2D5V_S5
EC72
EC27
EC39
EC75
1D8V_PWR
2D5V_PWR
1D2V_PWR
EC21
EC33
EC28
2D5V_S0
3D3V_BT_S0
3D3V_LAN_S5
DCBATOUT
DCBATOUT
EC74
EC51
EC52
EC25
EC41
EC69
FAN1_VCC
EC14
SCD1U16V2ZY-2GP
IMPORTANT:
SCD1U => VOLTAGE 25V
SCD1U16V => VOLTAGE 16V
HOLE2 HOLE
HOLE25 HOLE
HOLE4 HOLE
HOLE7 HOLE
HOLE12 HOLE
HOLE8 HOLE
HOLE10 HOLE
HOLE11 HOLE
HOLE6 HOLE
HOLE9 HOLE
HOLE1 HOLE
HOLE13 HOLE
HOLE3 HOLE
HOLE22 HOLE
HOLE20 HOLE
HOLE5 HOLE
HOLE24 HOLE
5V_AUX_S5
3D3V_LAN_S5
AD+
CHG_PWR-2 47
CHG_PWR-3 47
5130_LL1 45,46
5130_LL2 45,46
5130_LL3 45,46
MAX1544_LXM 41,42
MAX1544_LXS 41,42
EC65
EC32
EC4
EC12
EC17
EC35
EC36
EC30
EC29
EC61
EC26
EC22
EC58
EC63
EC31
EC18
EC19
EC60
EC59
3D3V_S0
2D5V_S0
3D3V_S5
5VA_OP
DCBATOUT
BT+
EC44
EC55
EC6
EC53
EC7
EC42
EC43
EC1
EC54
EC37
EC70
EC23
EC16
EC15
EC40
EC56
EC46
EC47
EC73
EC57
EC13
EC10
EC48
EC34
EC62
EC24
EC64
EC38
EC67
SCD1U => VOLTAGE 25V
HOLE P/N: 34.42E05.001
FOR VGA CHIP
FOR MDC
FOR NORTH BRIDGE
HOLE16
HOLE17
HOLE18
HOLE15
HOLE14
HOLE19
HOLE21
HOLE23
ZZ.0HOLE.XXX
GREEN COLOR FOR INSTALL
GND15
GND21
GND22
GND17
GND9
SPRING-23-GP
SPRING-1-GP
34.39S07.001
34.40V16.001
ZZ.NDPAD.XXX
GND13
GND14
GNDPAD
GND16
SPRING-29-GP
34.42T14.001
GND7
GND20
GND18
GND19
GND8
SPRING-24-GP
34.45T31.001
34.40V16.001
34.48U24.001
GND2
GND1
GND5
GND3
GND4
GND10
GND12
GND11
GND6
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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