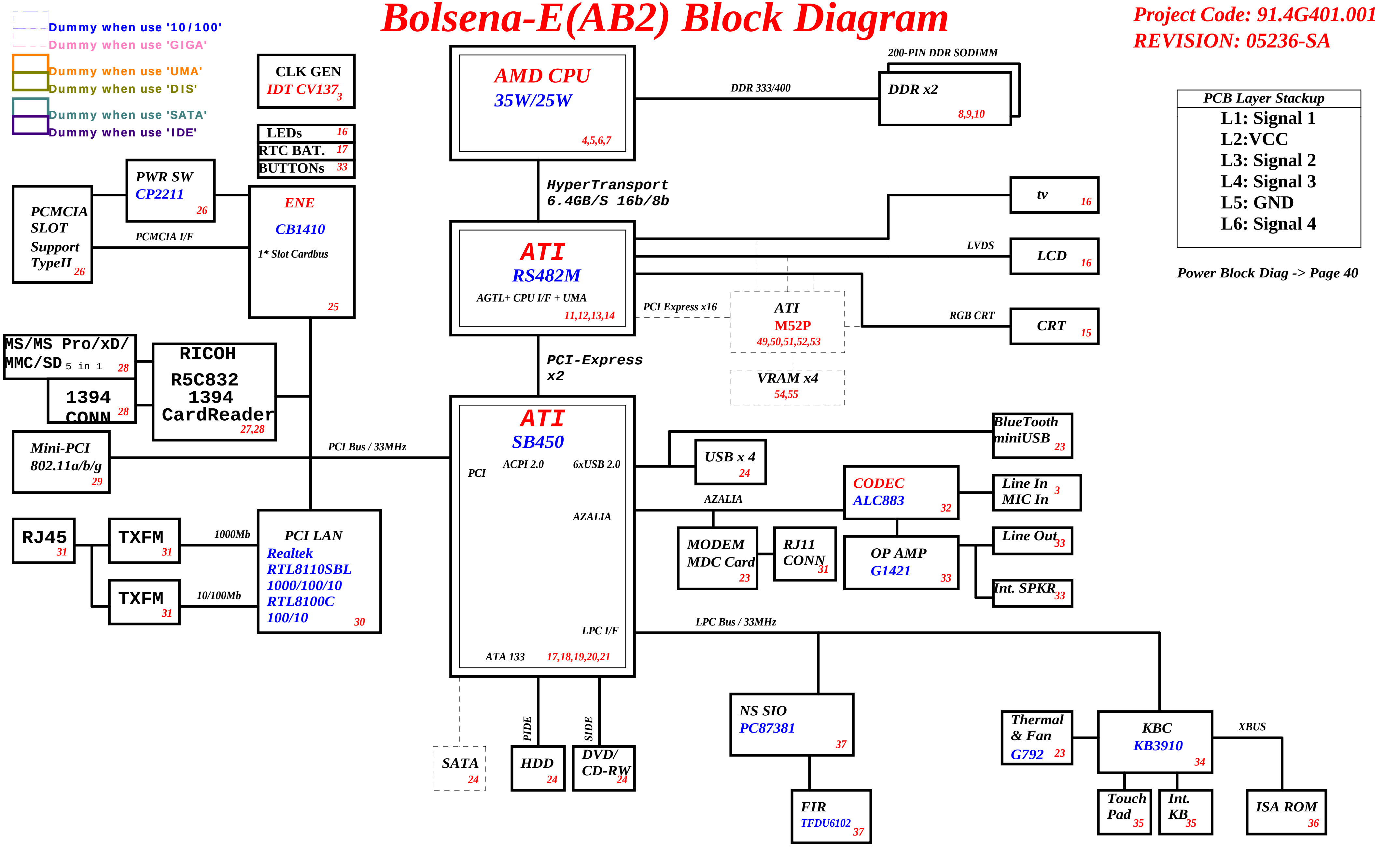
See 'TEXT' in 0MEMO or 1MEMO property in component

Bolsena-E(AB2) Block Diagram

Project Code: 91.4G401.001
REVISION: 05236-SA



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 1 of 58	

PCI Routing

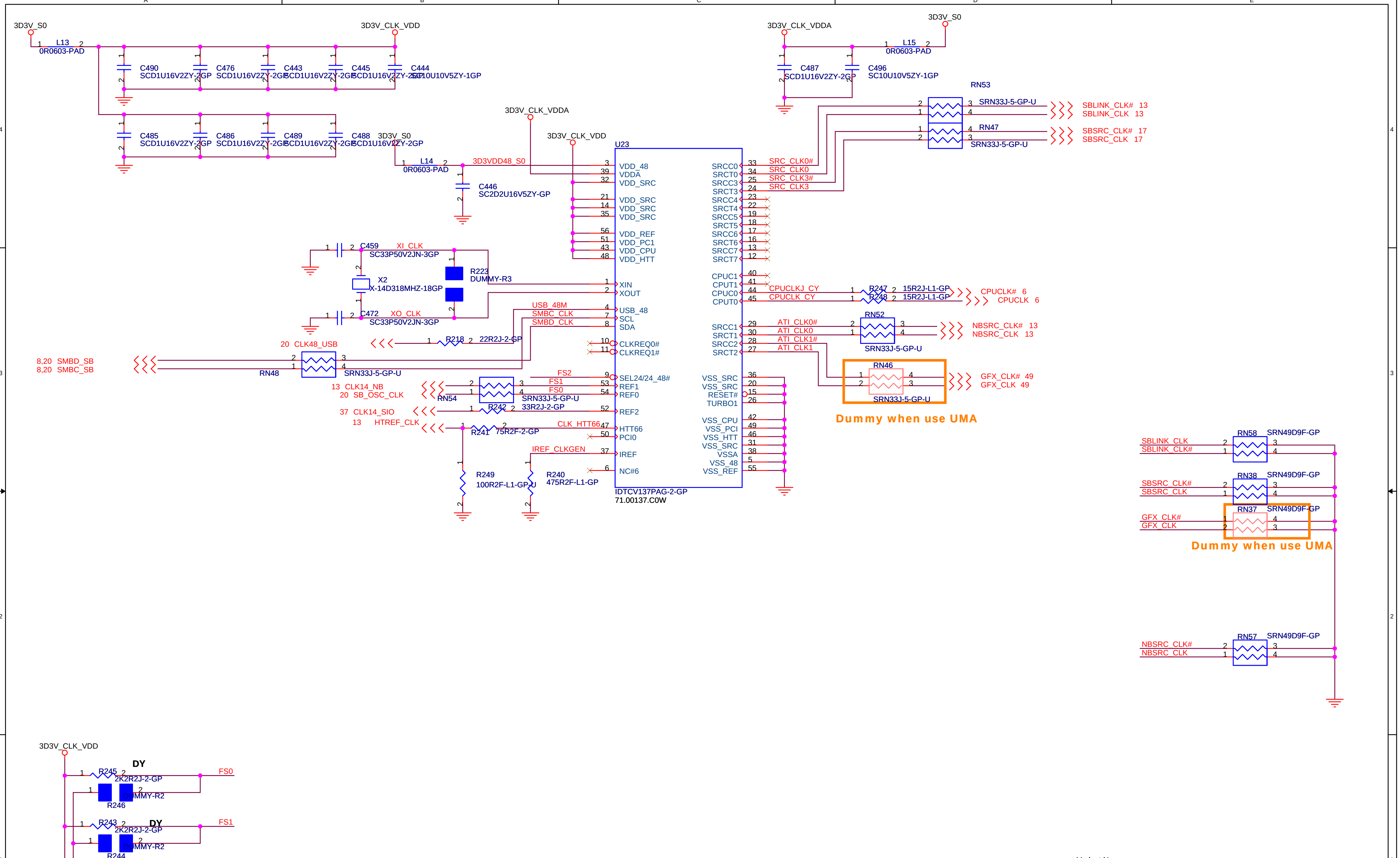
	IDSEL	IRQ	REQ/GNT
MiniPCI	21	F	0
LAN	23	H	2
7411	22	E (CardBus)	1
7411	17	G (1394)	3
7411	17	E (FlashMedia)	3

```
Ref.  function    schematic         BOM
-------------------------
U81  cpu socket    62.10055.121  (DON'T CHANGE)  (3mm high)
U80  north bridge  71.RS482.M03  71.RS482.M03  (ver A12)
U43  south bridge  71.SB400.B0U  71.SB400.D0U  (ver A13)
U32  clock gen.    71.00137.C0W  71.00137.C0W

---
U70  VGA M52     71.0M52P.A0U
U64  VRAM FOR M52
U65  VRAM FOR M52
U69  VRAM FOR M52
U71  VRAM FOR M52

---
U66  BIOS SOCKET  72.39040.G03  62.10002.032   (NO NEED WHEN PD)
U66  BIOS IC      72.39040.G03  72.39040.H03  (DIP STAGE IN LAB, SMT IN PD)
---
U75  GIGA LAN   71.08110.00G  71.08110.A0G
U75  10/100 LAN  71.08110.00G  71.08100.C0G
```

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

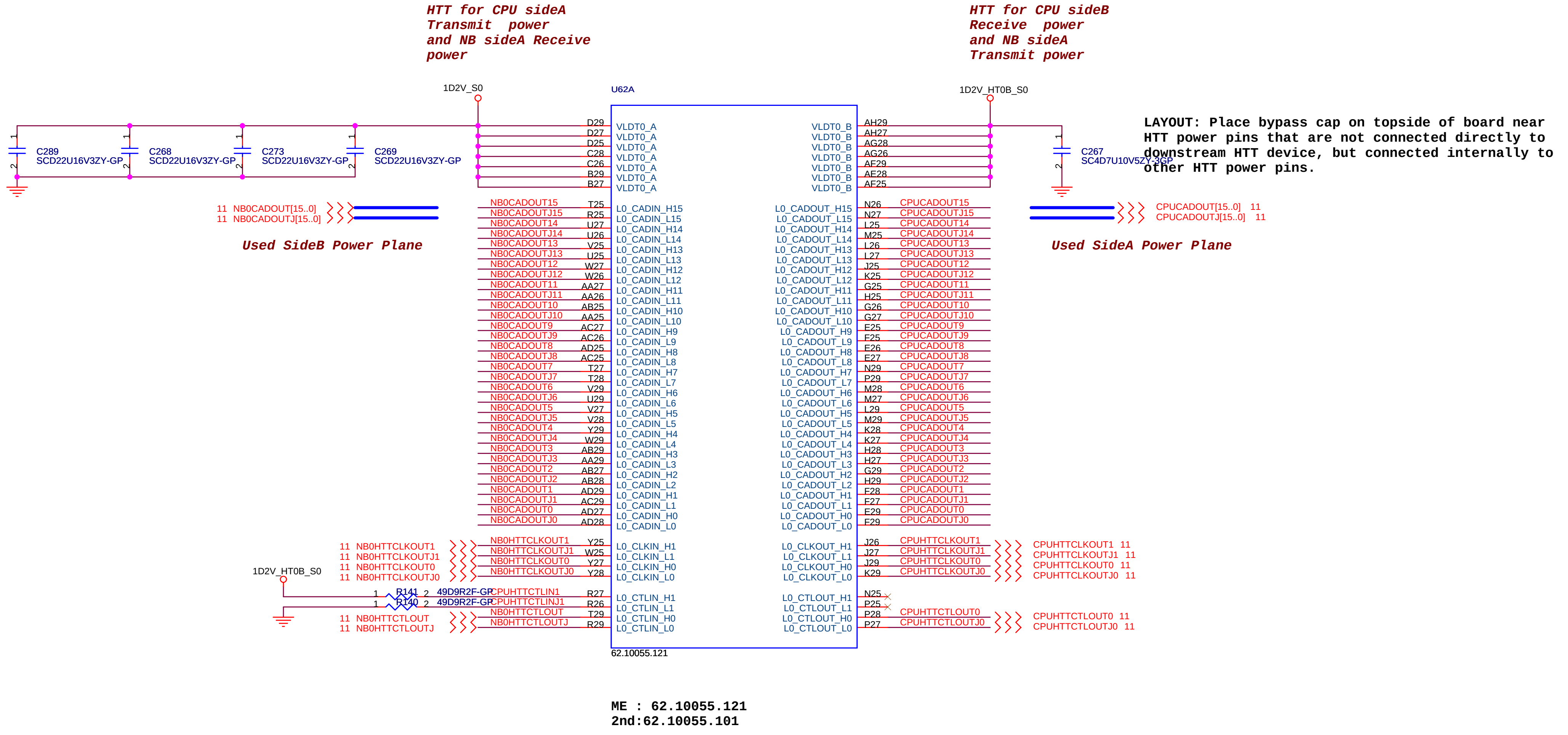
Title		
HISTORY		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 2 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

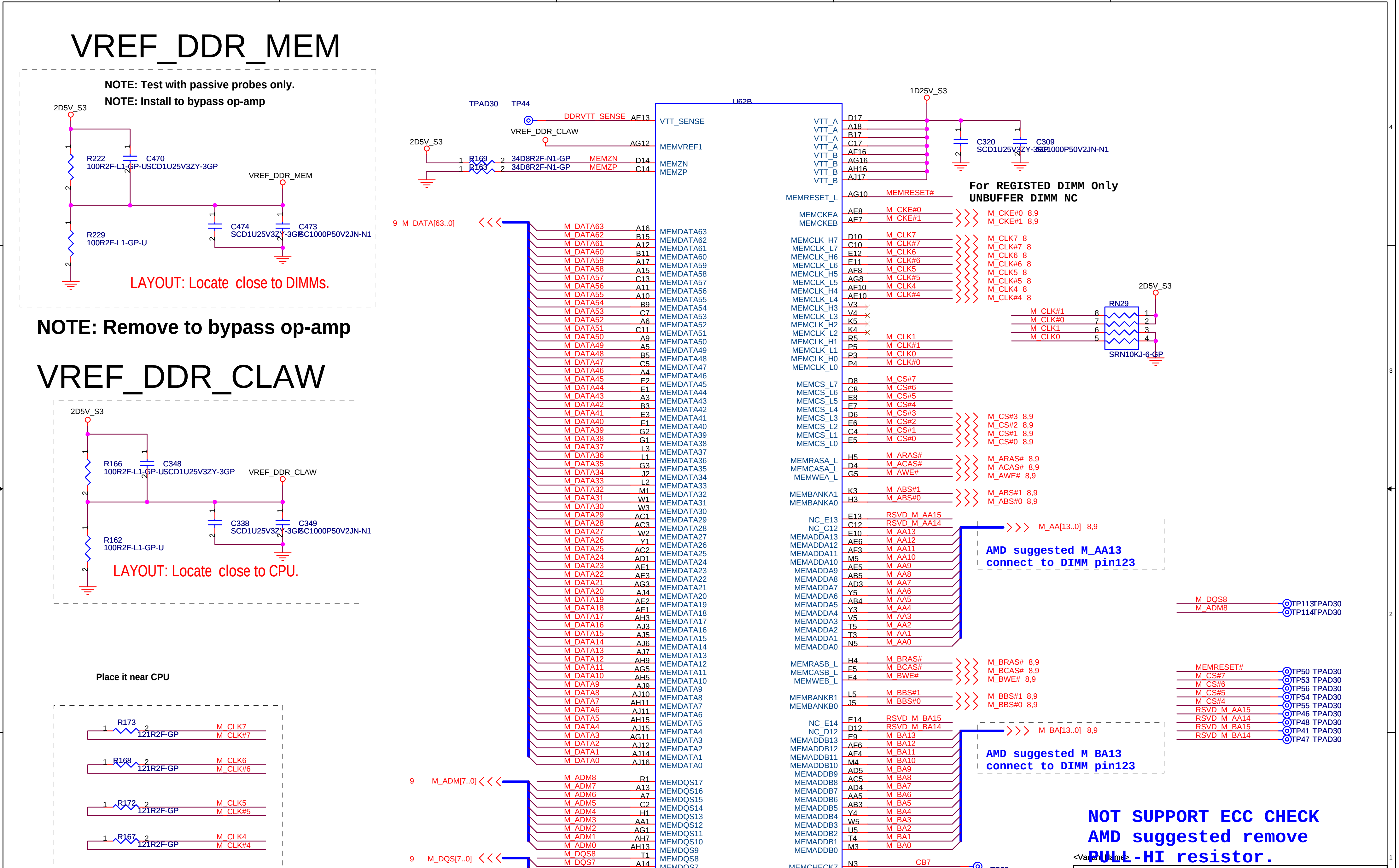
Title		
CLKGEN_IDTCV137		
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 3 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

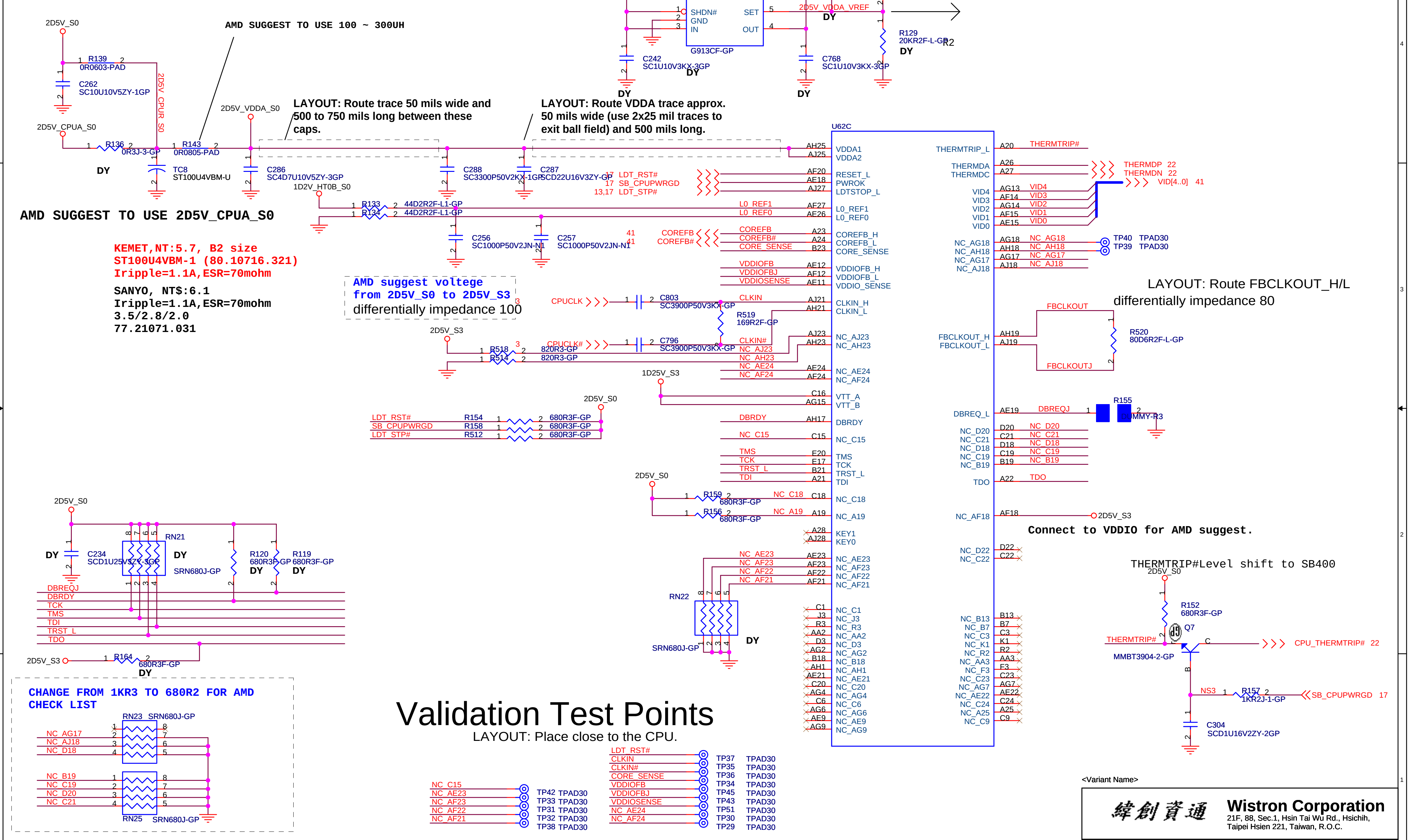
Title		
CPU(1/4)_HyperTransport I/F		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 4 of 58	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(2/4)_DDR	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 5 of 58	

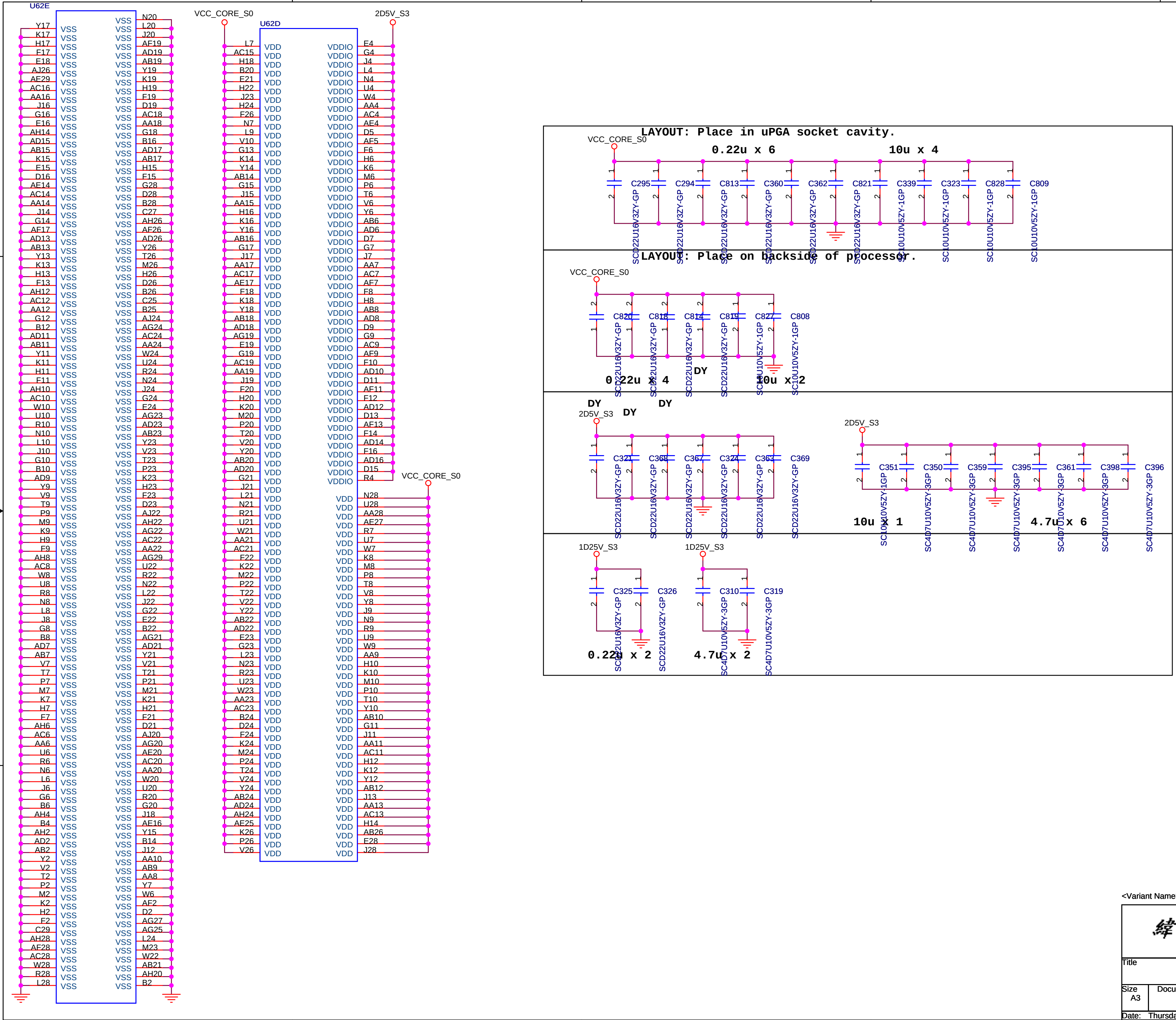
2D5V_VDDA_S0



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU(3/4)_Control & Debug	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 6 of 58	



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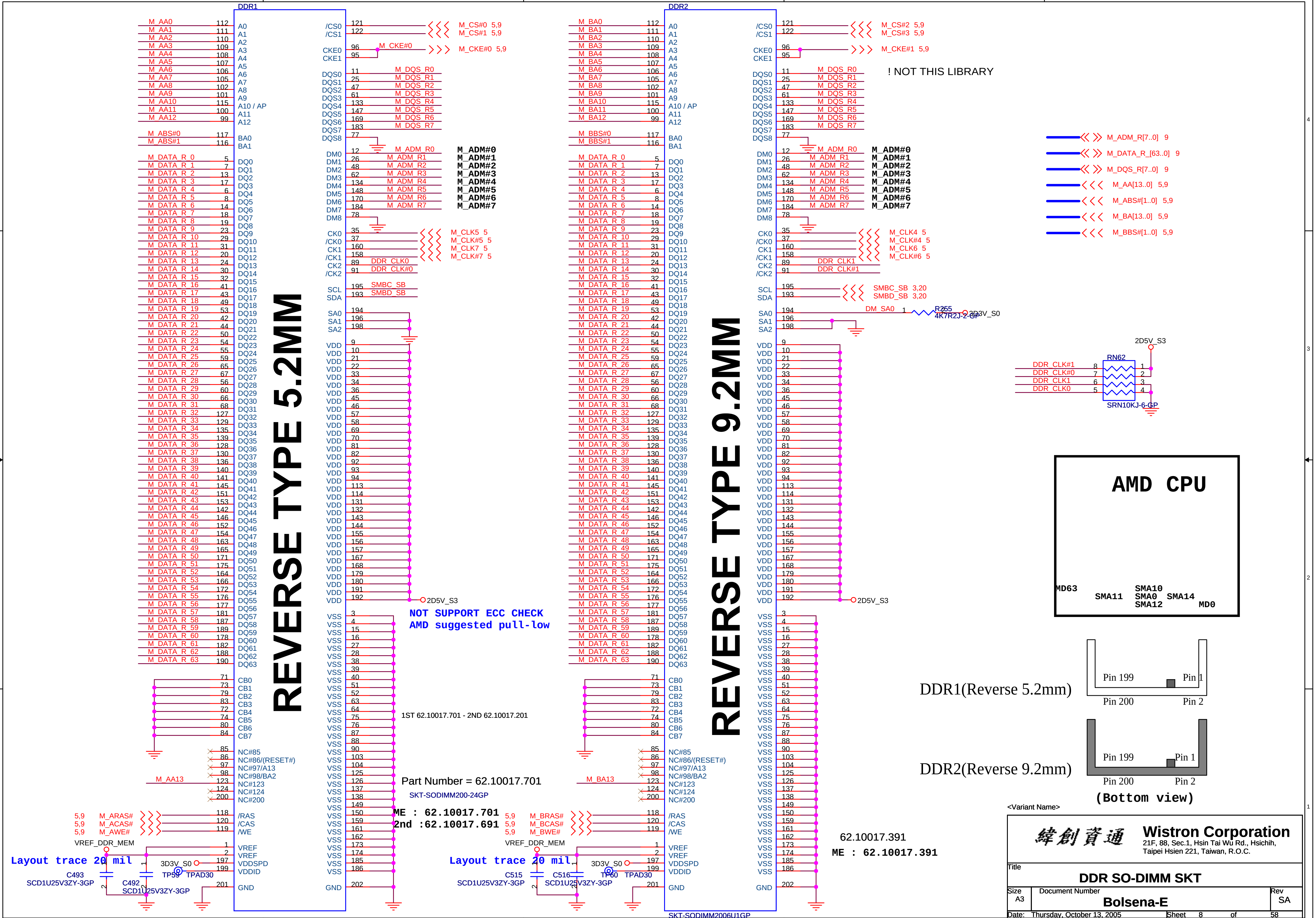
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU(4/4)_Power		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 7 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
DDR SO-DIMM SKT		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 8 of 58	

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS, CB PINS

PARALLEL TERMINATION

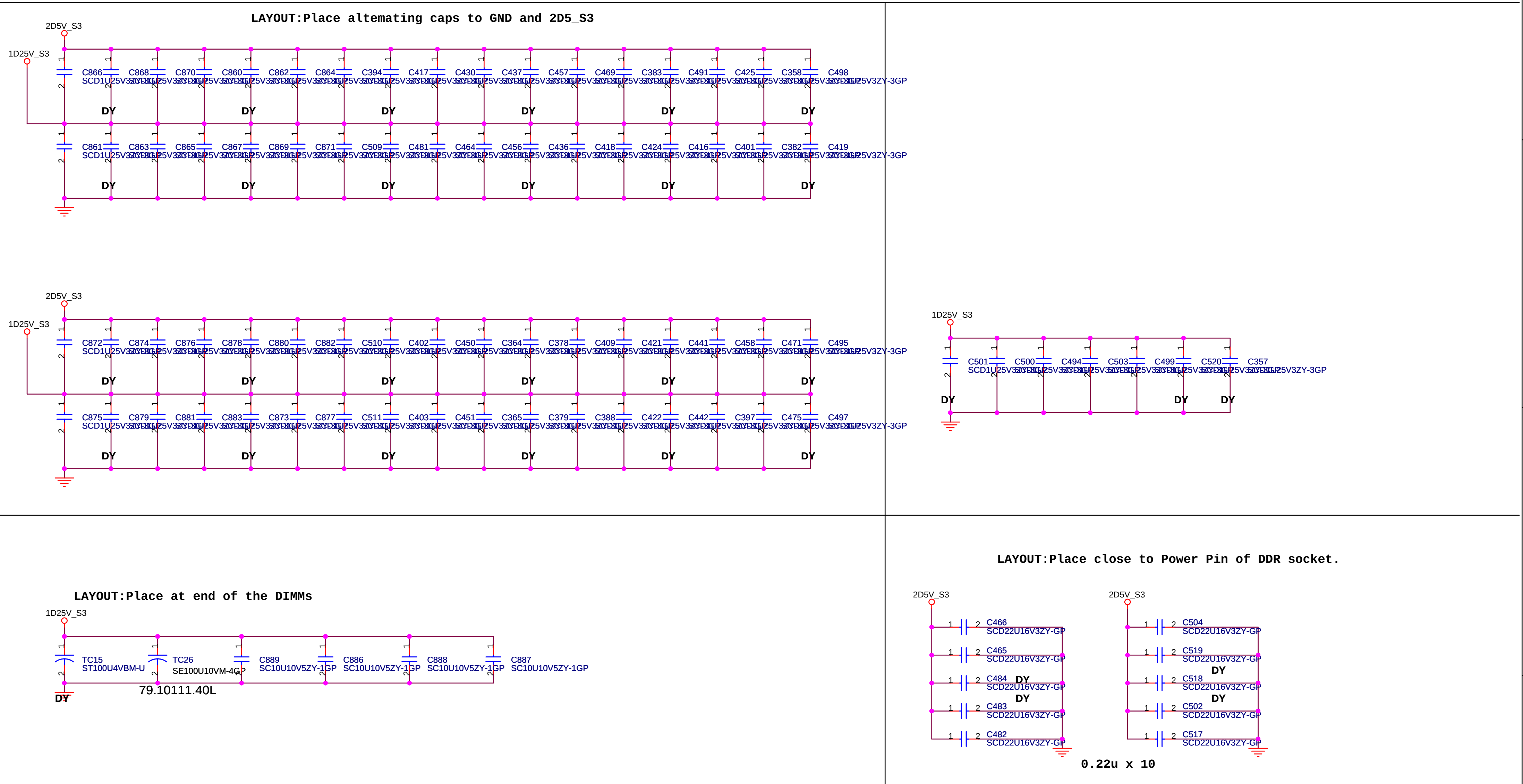
PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

05/10
Remove the damping resistor for AMD suggest.

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	DDR DAMPING & TERMINATION	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 9 of 58	



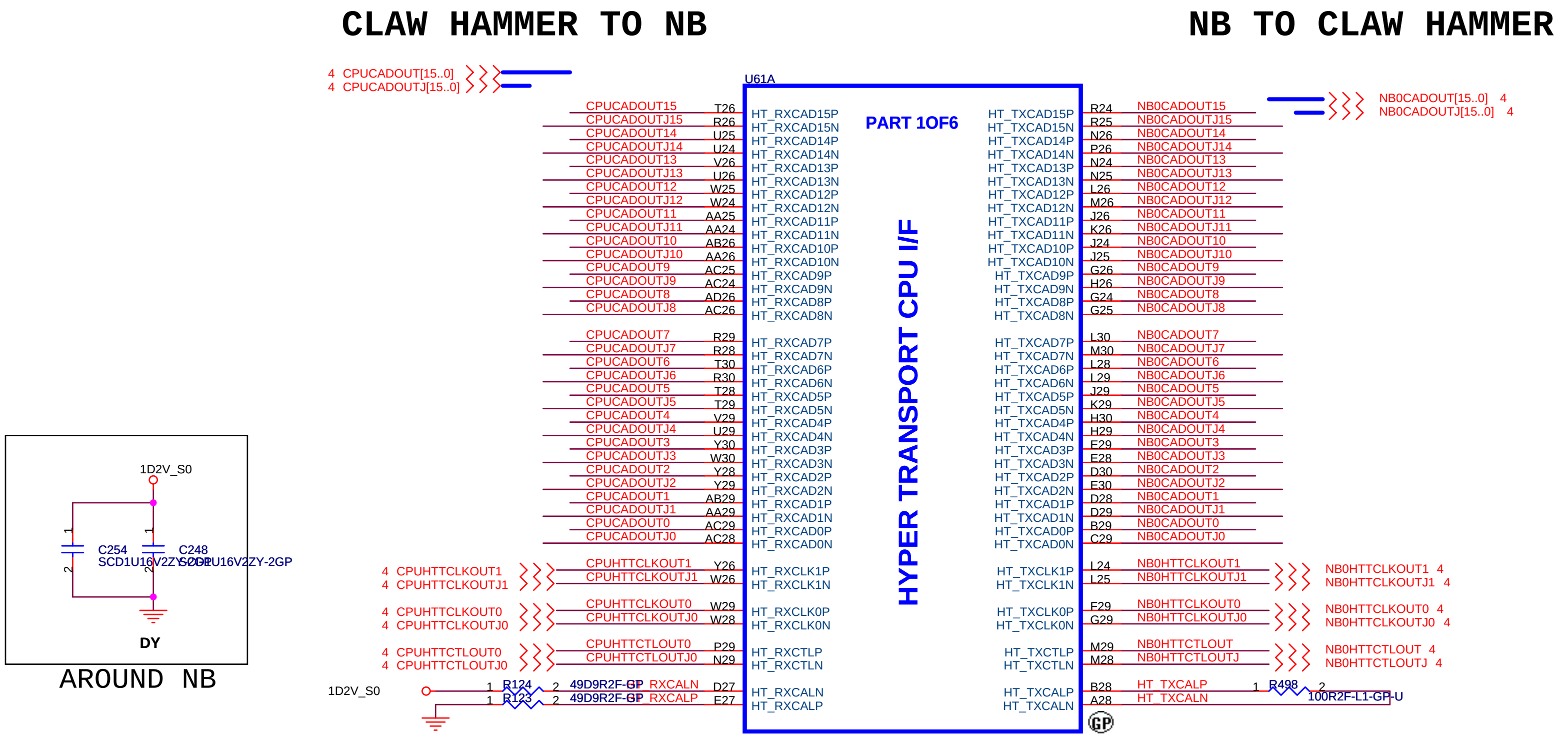
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR DECOUPLING**

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 | Sheet 10 of 58



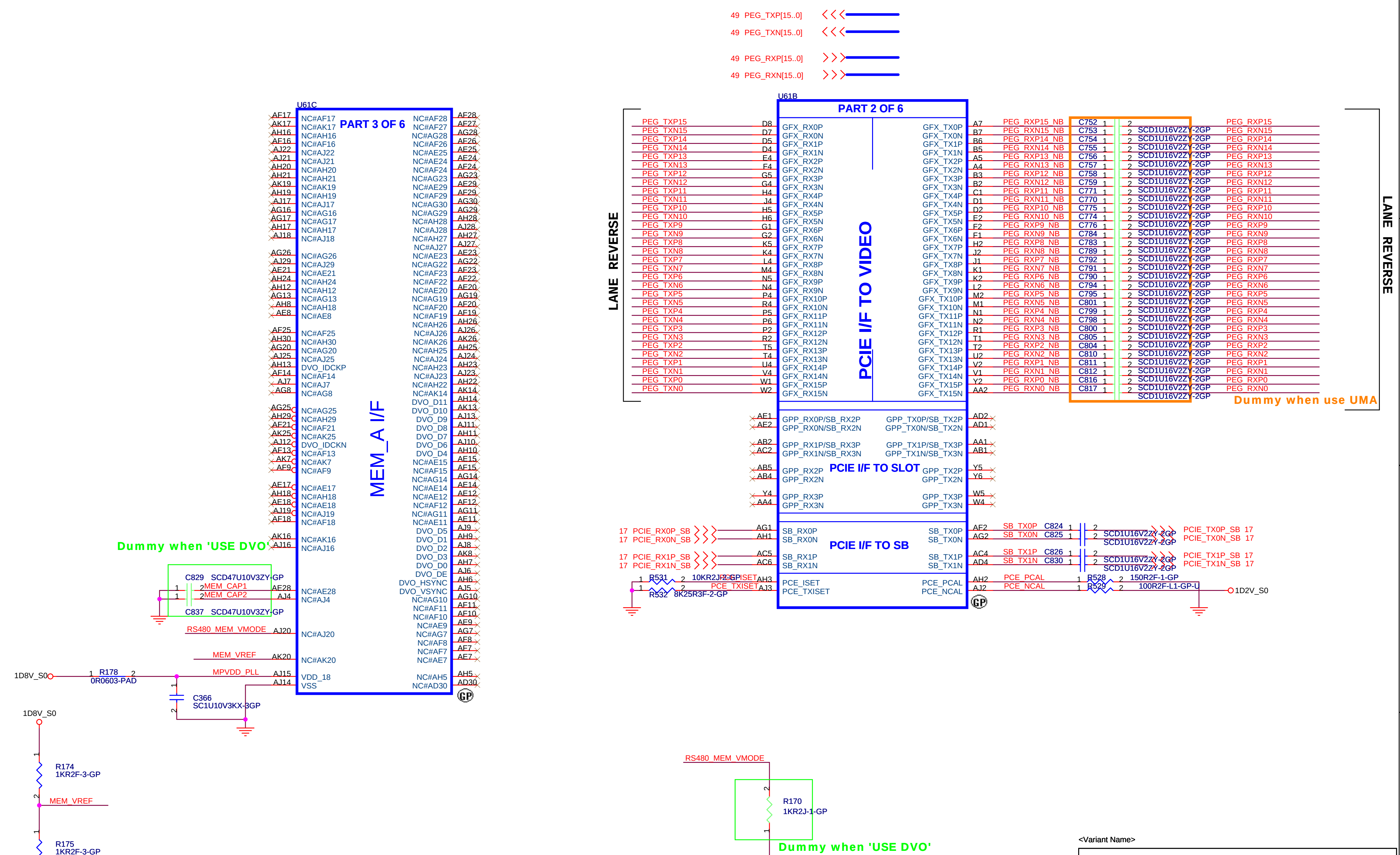
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS482M (1 of 4) HT

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 11 of 58



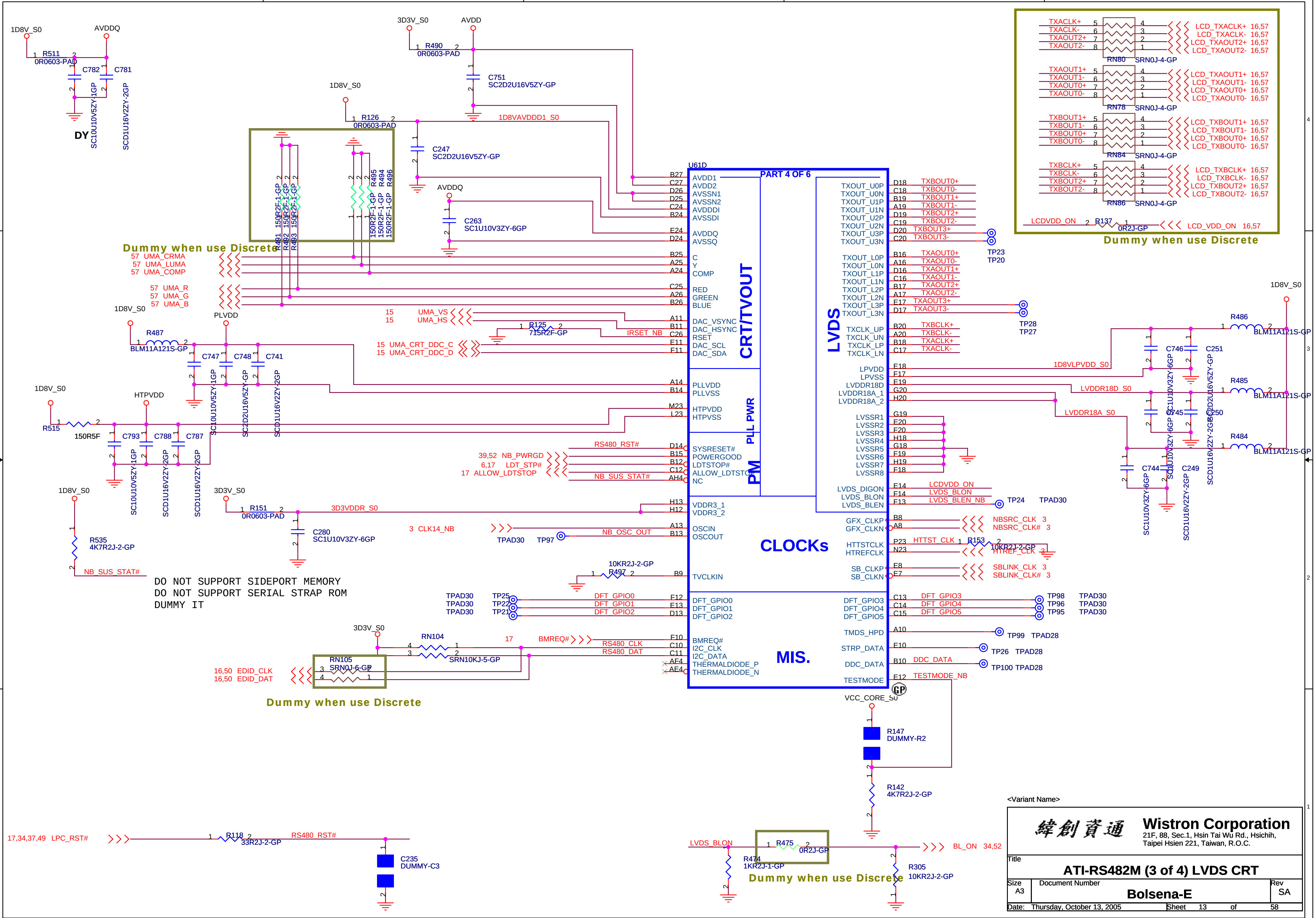
NO DVO:
MEM_COMPP = NC
MEM_COMPN = NC
MEM_CAP1 = 470nF
MEM_CAP2 = 470nF
MEM_VMODE = GND (IF VDD_MEM = 2.5V)
MEM_VREF = VDD_MEM / 2

WITH DVO:
MEM_COMPP = 61.9 OHM TO GND
MEM_COMPN = 61.9 OHM TO VDD_MEM
MEM_CAP1 = NC
MEM_CAP2 = NC
MEM_VMODE = 1.8V(IF VDD_MEM = 1.8V)
MEM_VREF = VDD_MEM / 2

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
ATI-RS482M (2 of 4) PCIE		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 12 of 58	

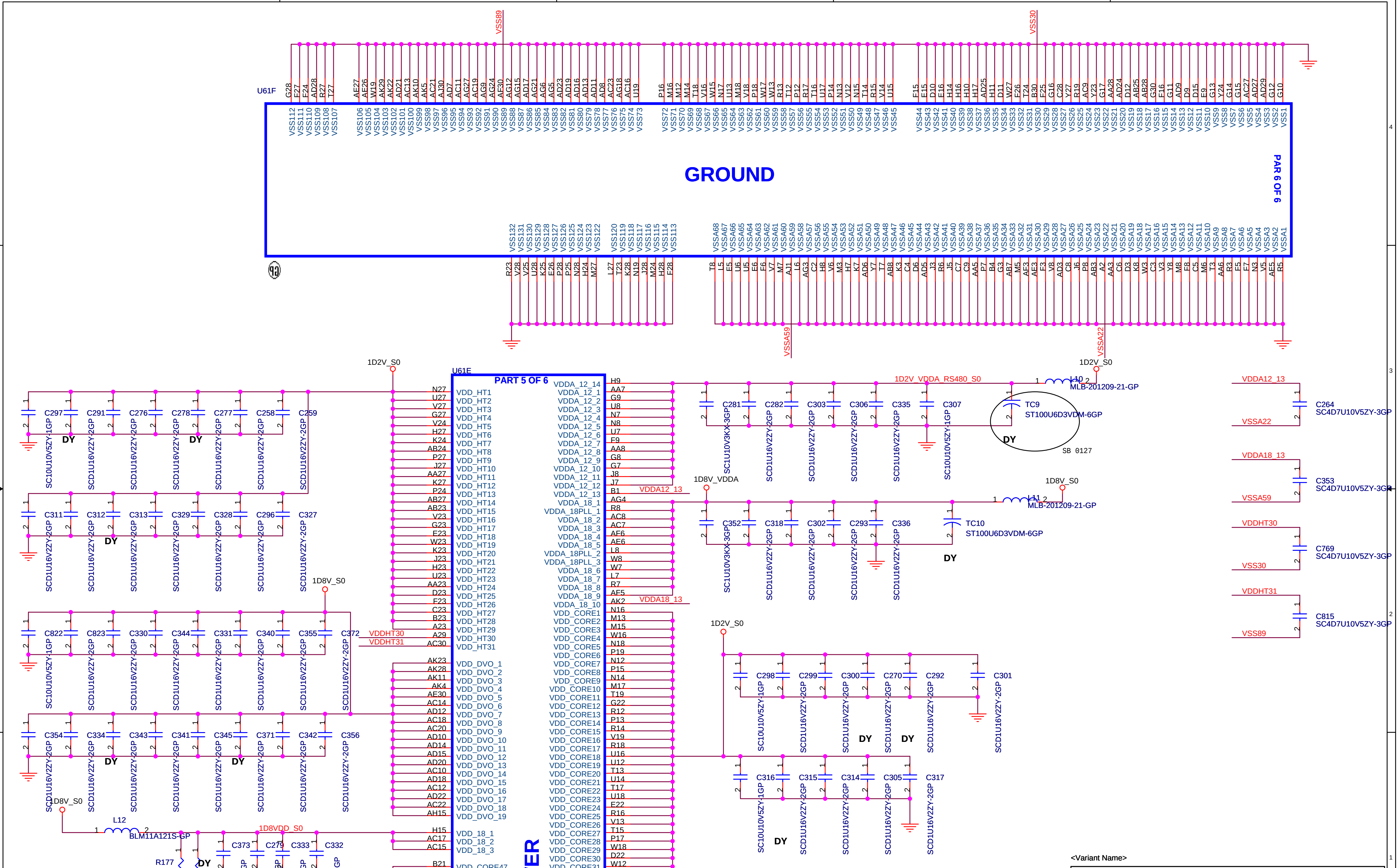


<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
ATI-RS482M (3 of 4) LVDS CRT		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 13 of 58	



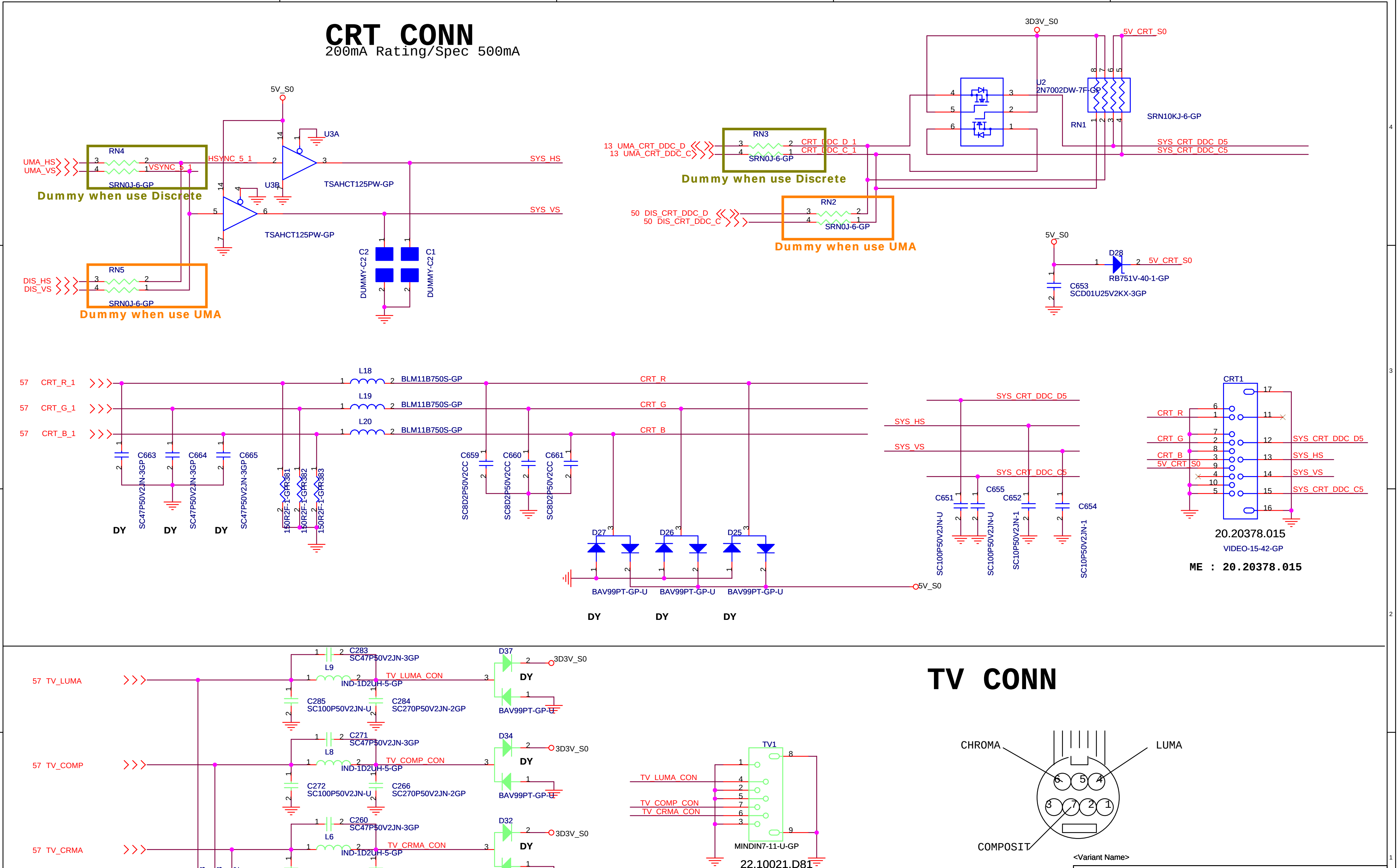
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-RS482M (4 of 4) PWR, GND**

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 14 of 58



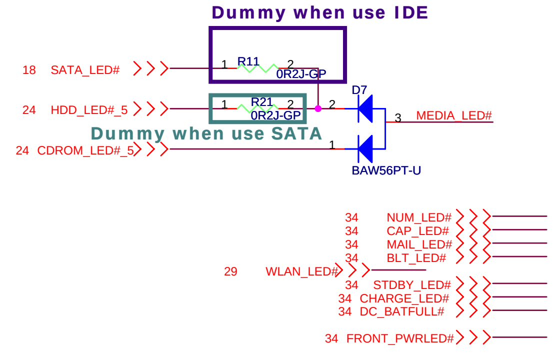
<Variant Name>

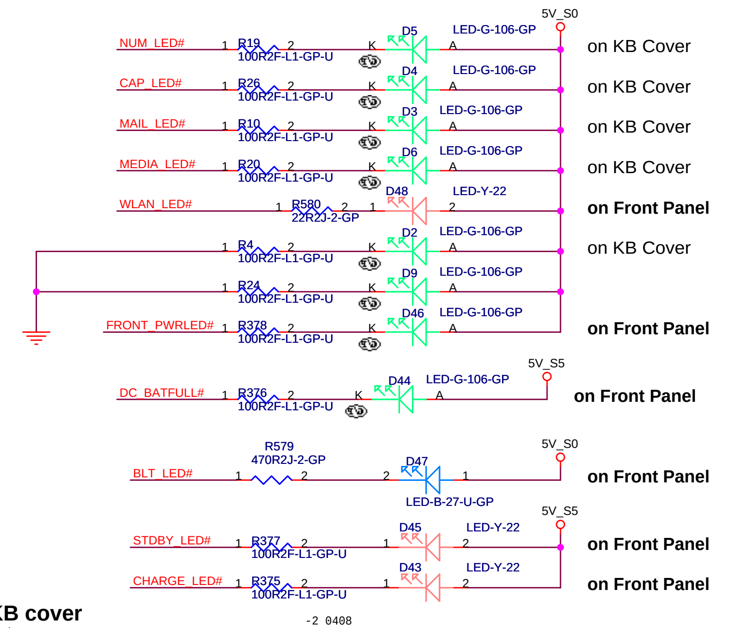
緯創資通 **Wistron Corporation**

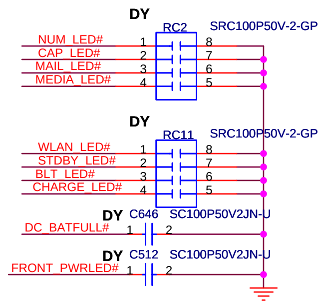
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT/TV	
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 15 of 58	

LEDs







on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER1	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

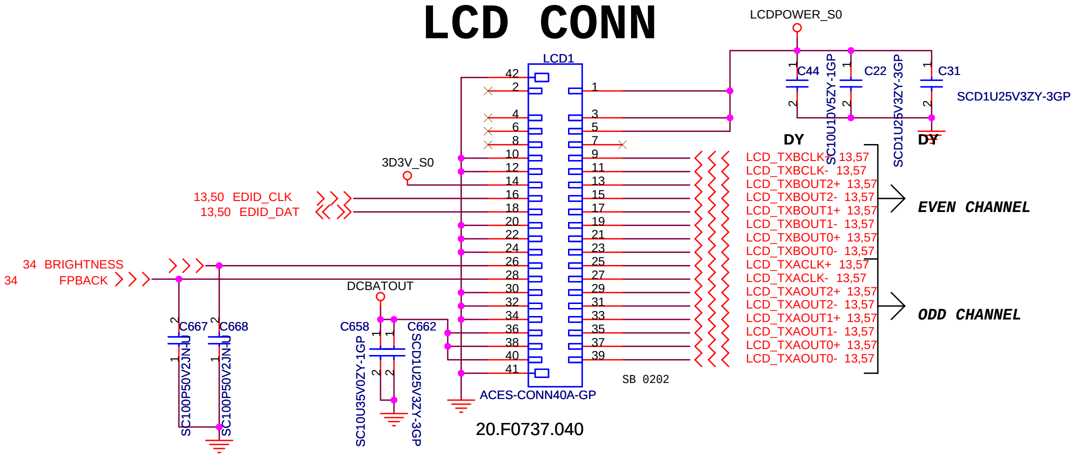
LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power2

Charger:
Green : DC only with Battery full with DC
Orange : Charging
Orange Blink : Battery low

Power2:
Green : S0
Orange : S3
Orange Blinking : Enter S4

(Please See M.E. drawing LED position)

LCD CONN

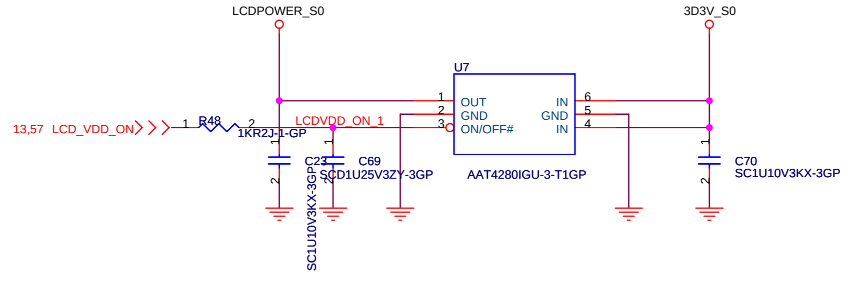


20.F0737.040

1ST 20.D0198.108 - 2ND 20.F0687.040

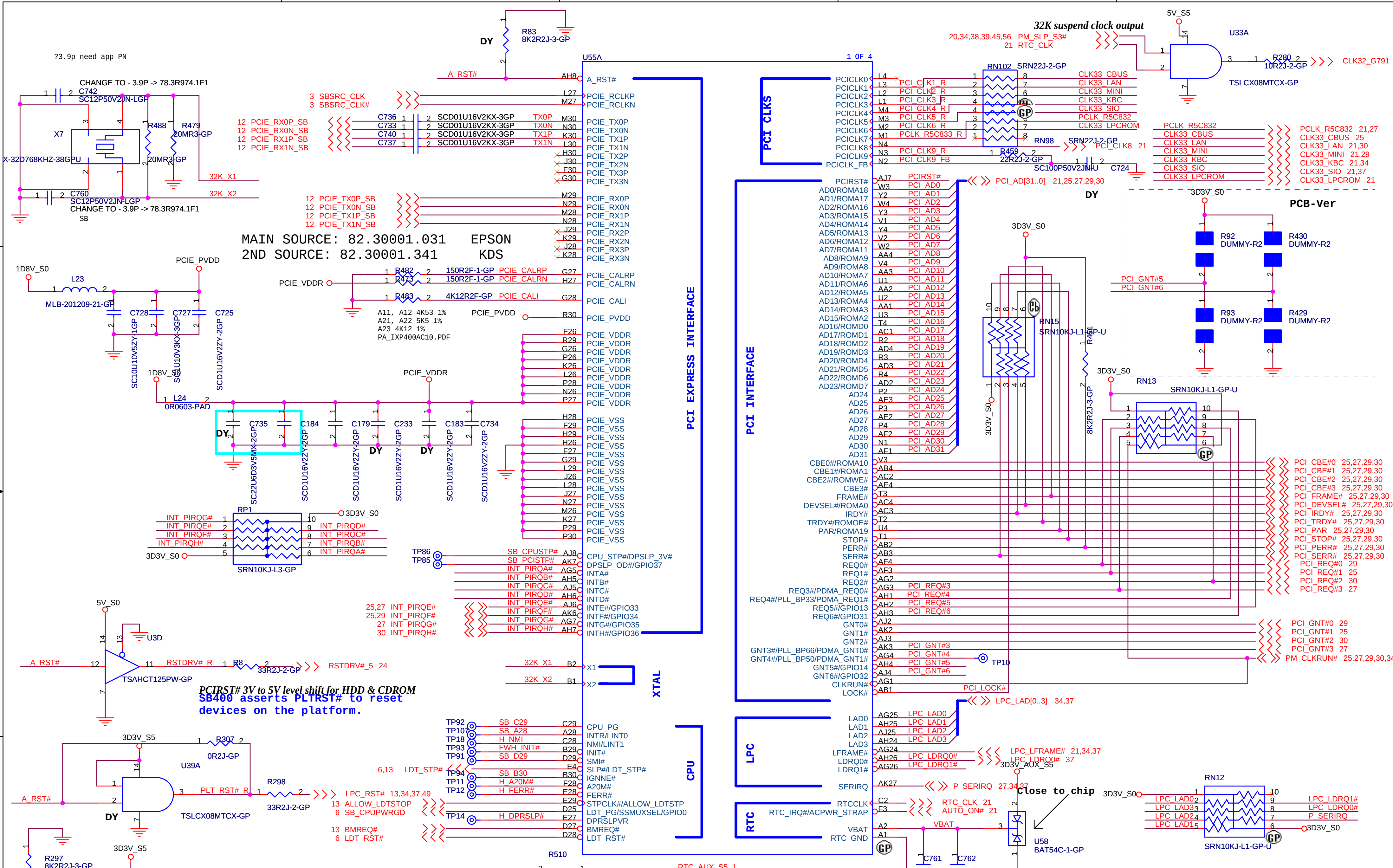
LCD POWER

Layout 40 mil



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LCD / LEDs**	
Size A3	Document Number **Bolsena-E**	Rev SA
Date: Thursday, October 13, 2005	Sheet 16 of 58	

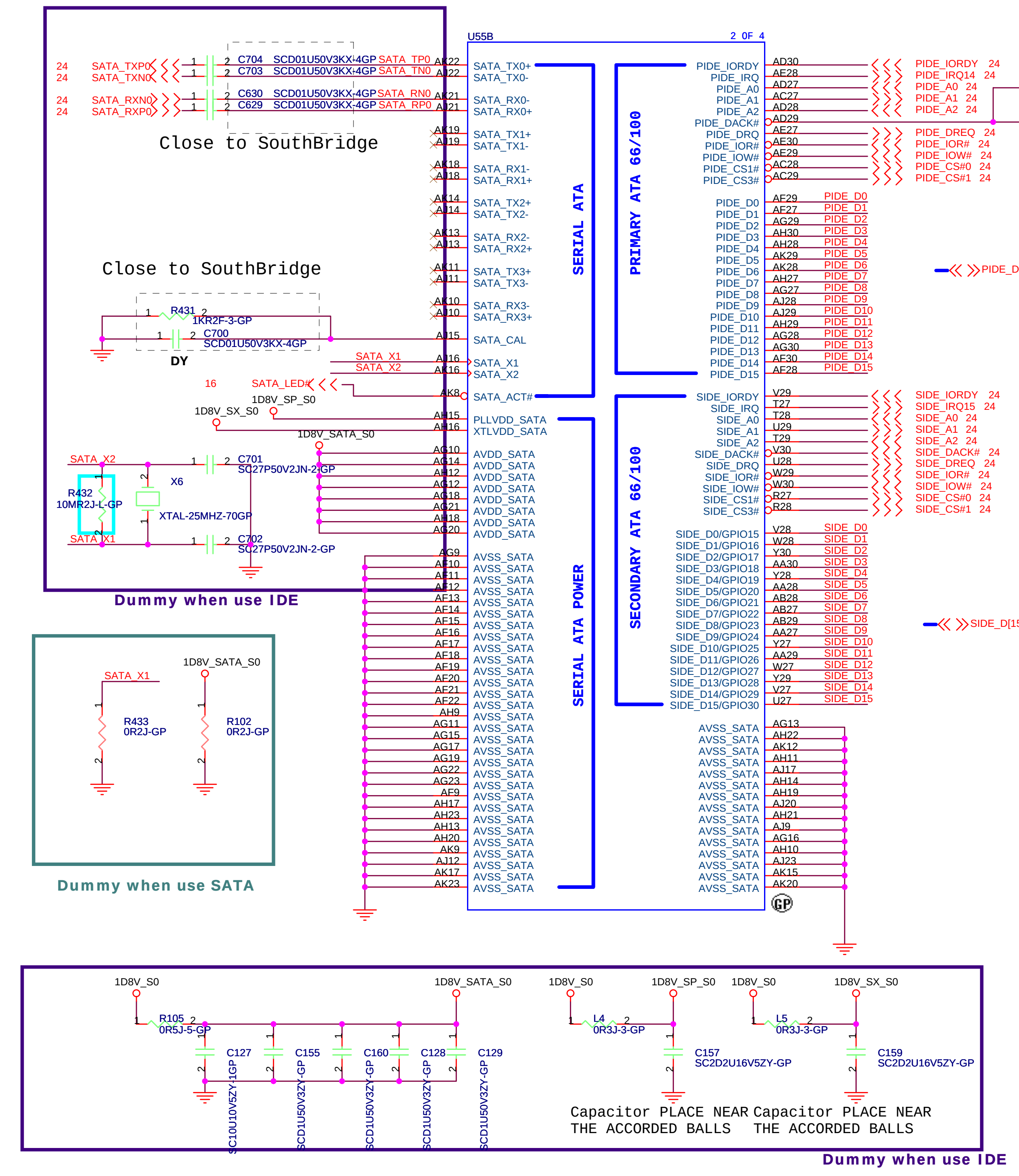


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB450 (1 of 5) PCI, PCIE

Size: A3 | Document Number: Bolsena-E | Rev: SA

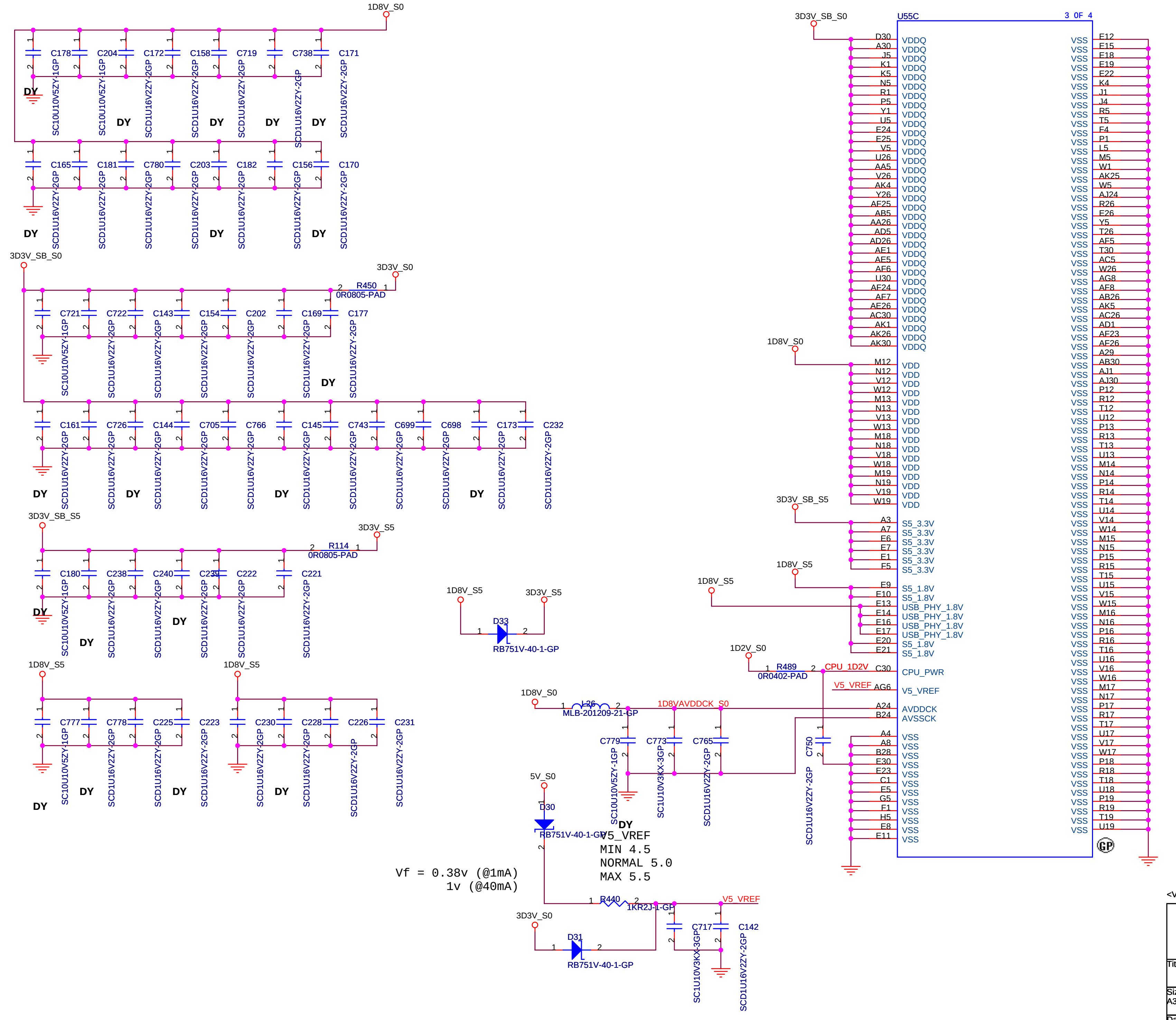
Date: Thursday, October 13, 2005 | Sheet 17 of 58



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

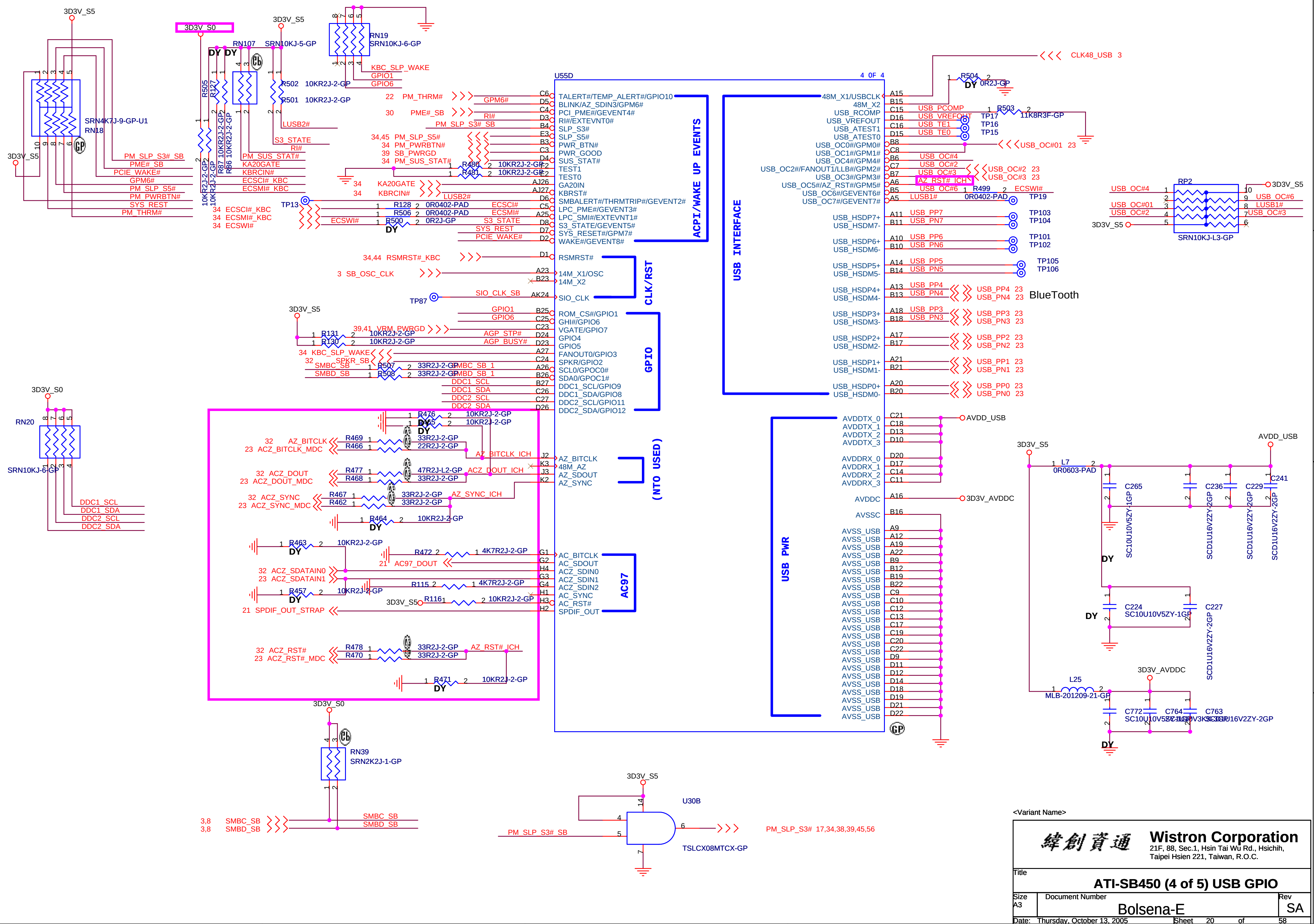
Title	ATI-SB400 (2 of 5) IDE	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 18 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
ATI-SB400 (3 of 5) POWER		
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 19 of 58	

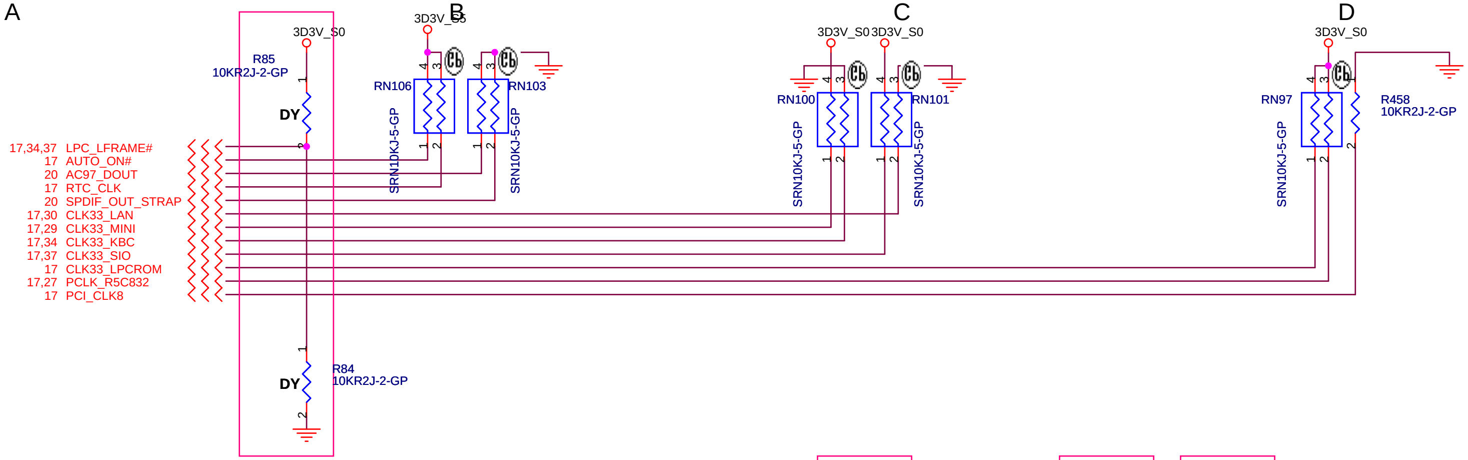


<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

緯創資通

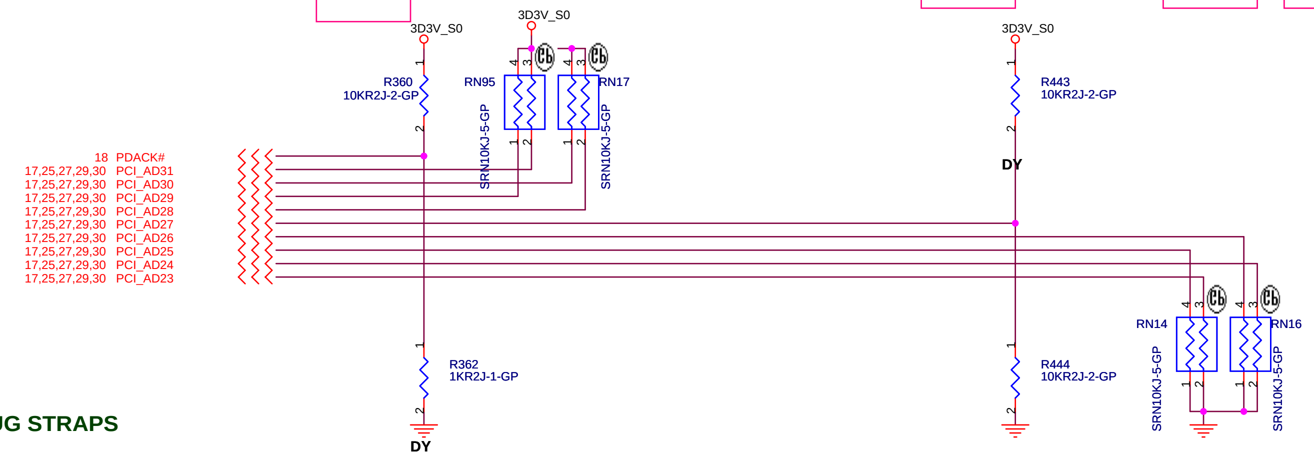
Title		
ATI-SB450 (4 of 5) USB GPIO		
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 20 of 58	



Place these R close to SouthBridge if possible

REQUIRED SYSTEM STRAPS

	LFRAME#	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2 (CLK33_LAN)	PCI_CLK3 (CLK33_MINI)	PCI_CLK4 (CLK33_KBC)	PCI_CLK5 (CLK33_SIO)	PCI_CLK6 (CLK33_LPCROM)	PCI_CLK7 (PCLK_R5C832) PCI_CLK8
STRAP HIGH	Thermal Trip is not enable as default Optional	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ -Crytsal Pad	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48	PCIE_CM_SET HIGH DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	Thermal Trip is enable as default Optional	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ Use External only	PCIE_CM_SET LOW	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

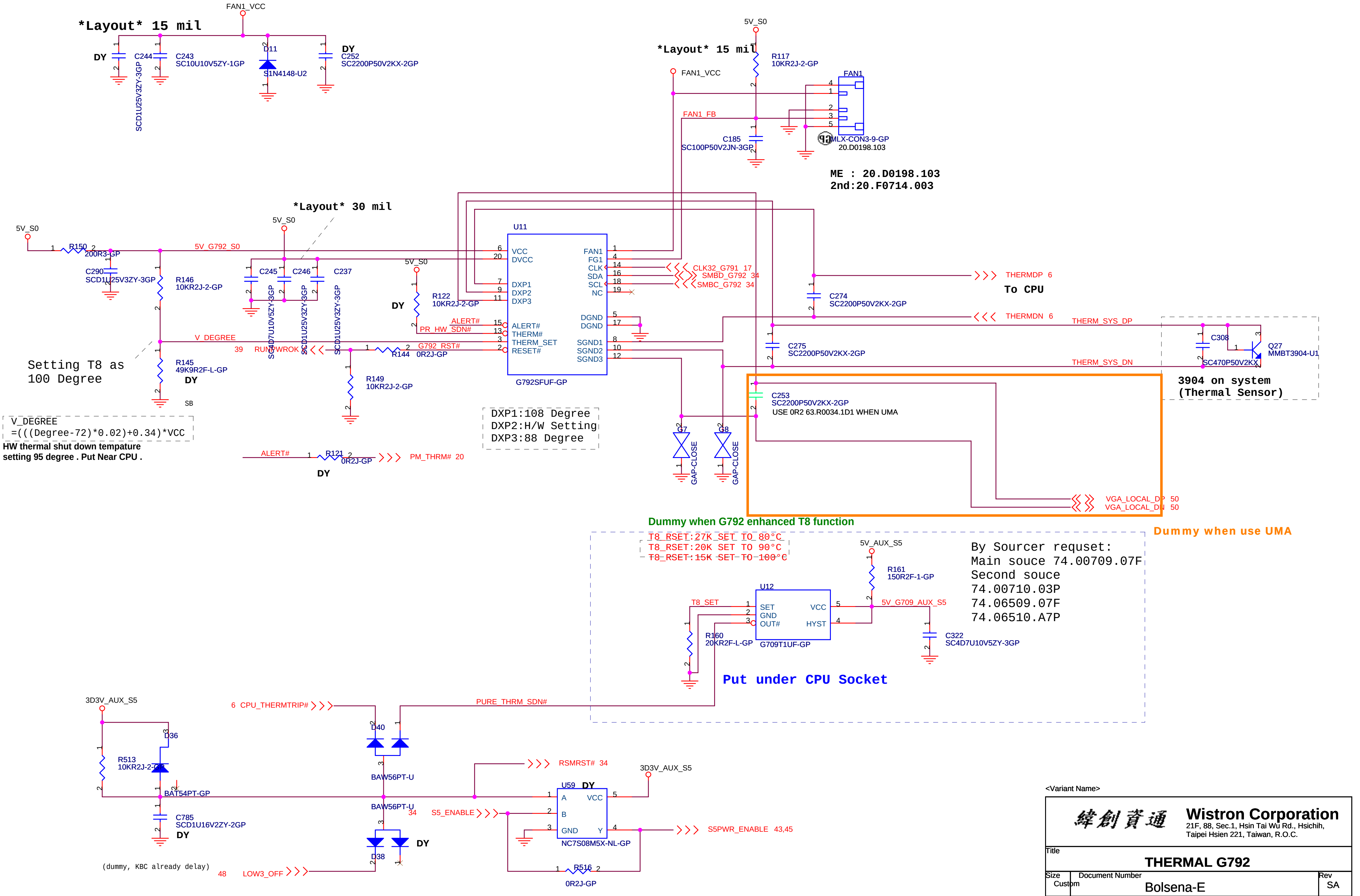
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB400 STRAPPING(5 of 5)**

Size	Document Number	Rev
A3	Bolsena-E	SA

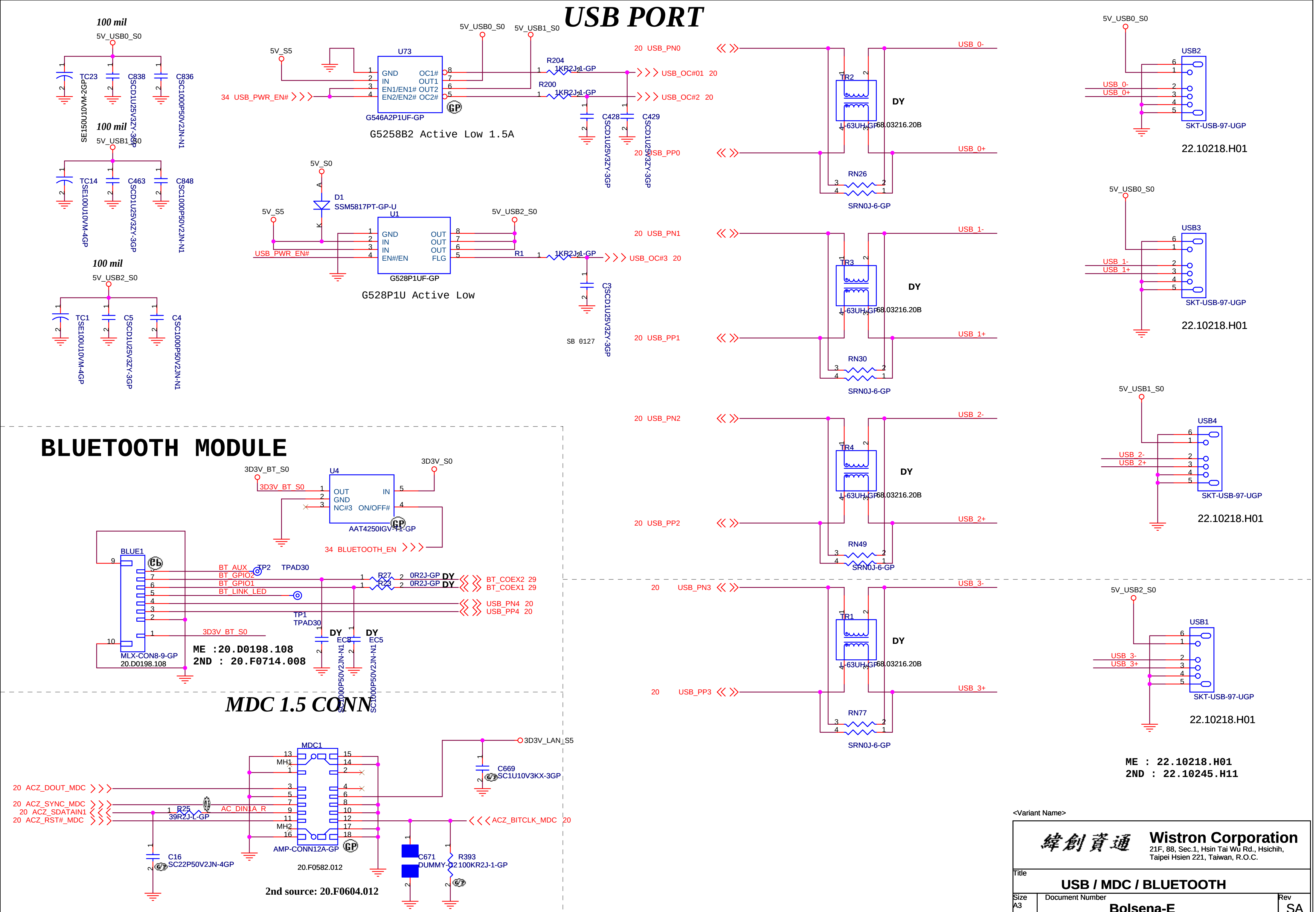
Date: Thursday, October 13, 2005 Sheet 21 of 58



<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

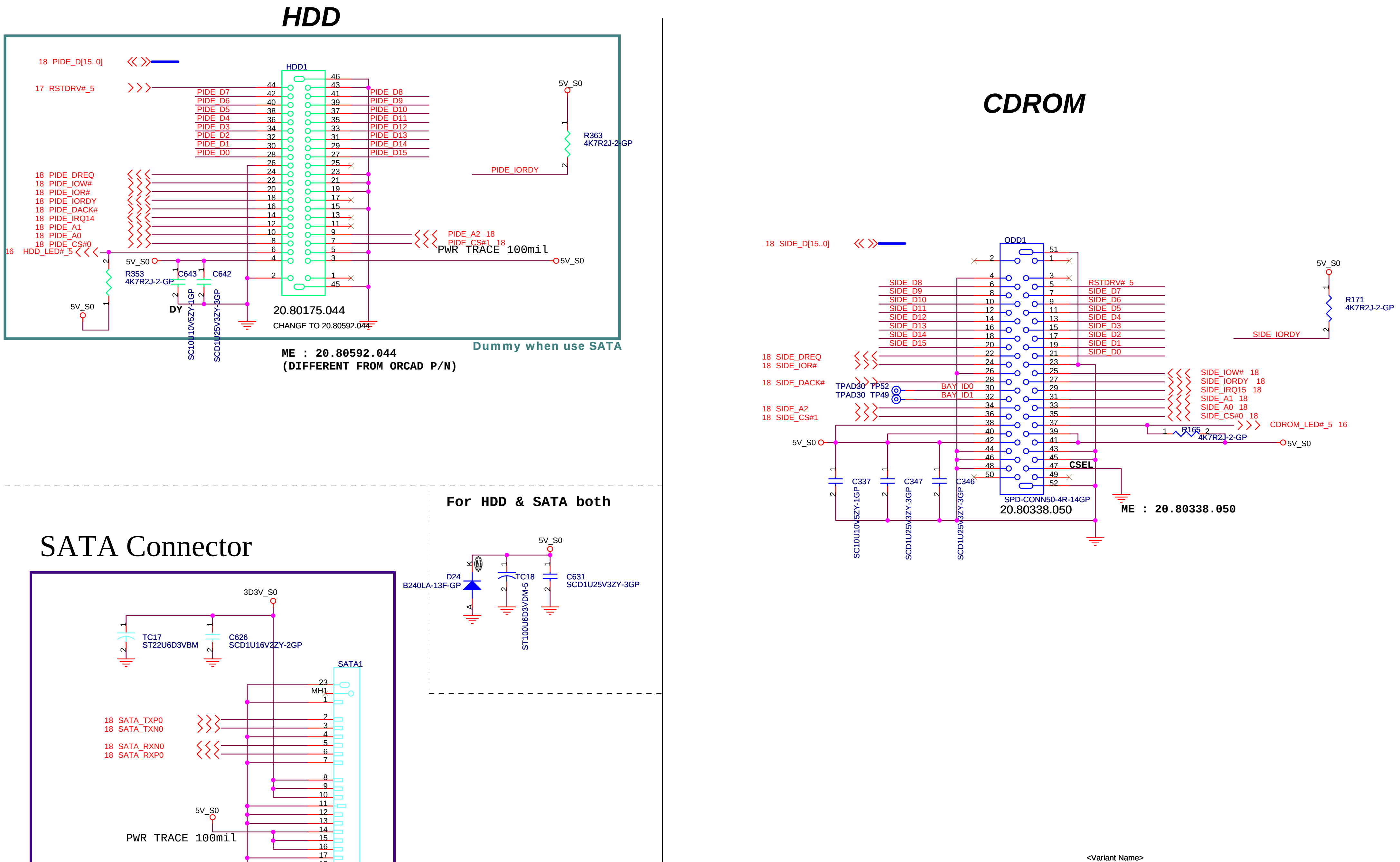
Title		
THERMAL G792		
Size: Custom	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 22 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

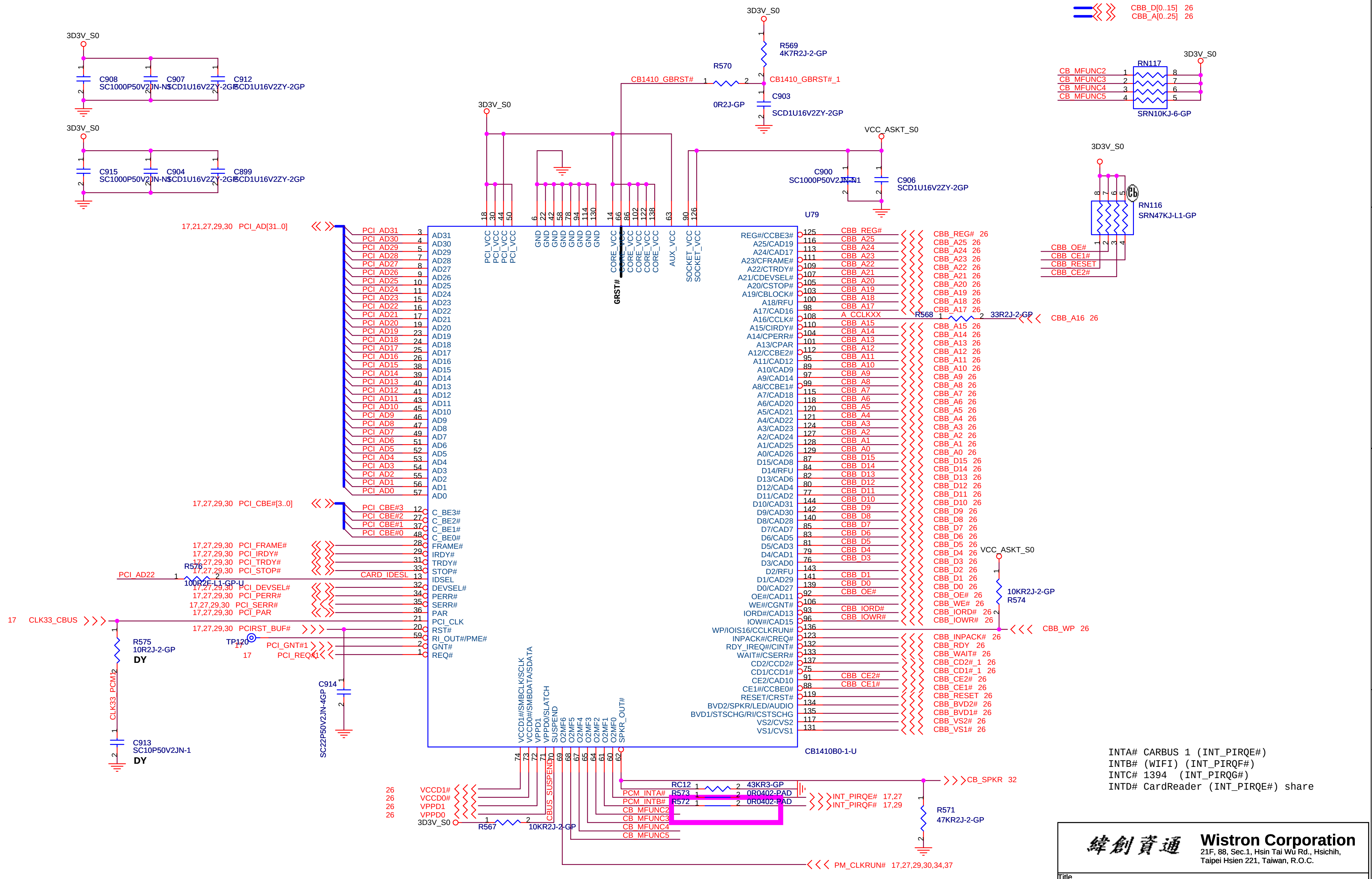
Title	USB / MDC / BLUETOOTH	
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 23 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
HDD / CDROM / SATA		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 24 of 58	




```
INTA# CARBUS 1 (INT_PIRQE#)
INTB# (WIFI) (INT_PIRQF#)
INTC# 1394  (INT_PIRQG#)
INTD# CardReader (INT_PIRQE#) share
```

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CardBus_ENE CB1410**

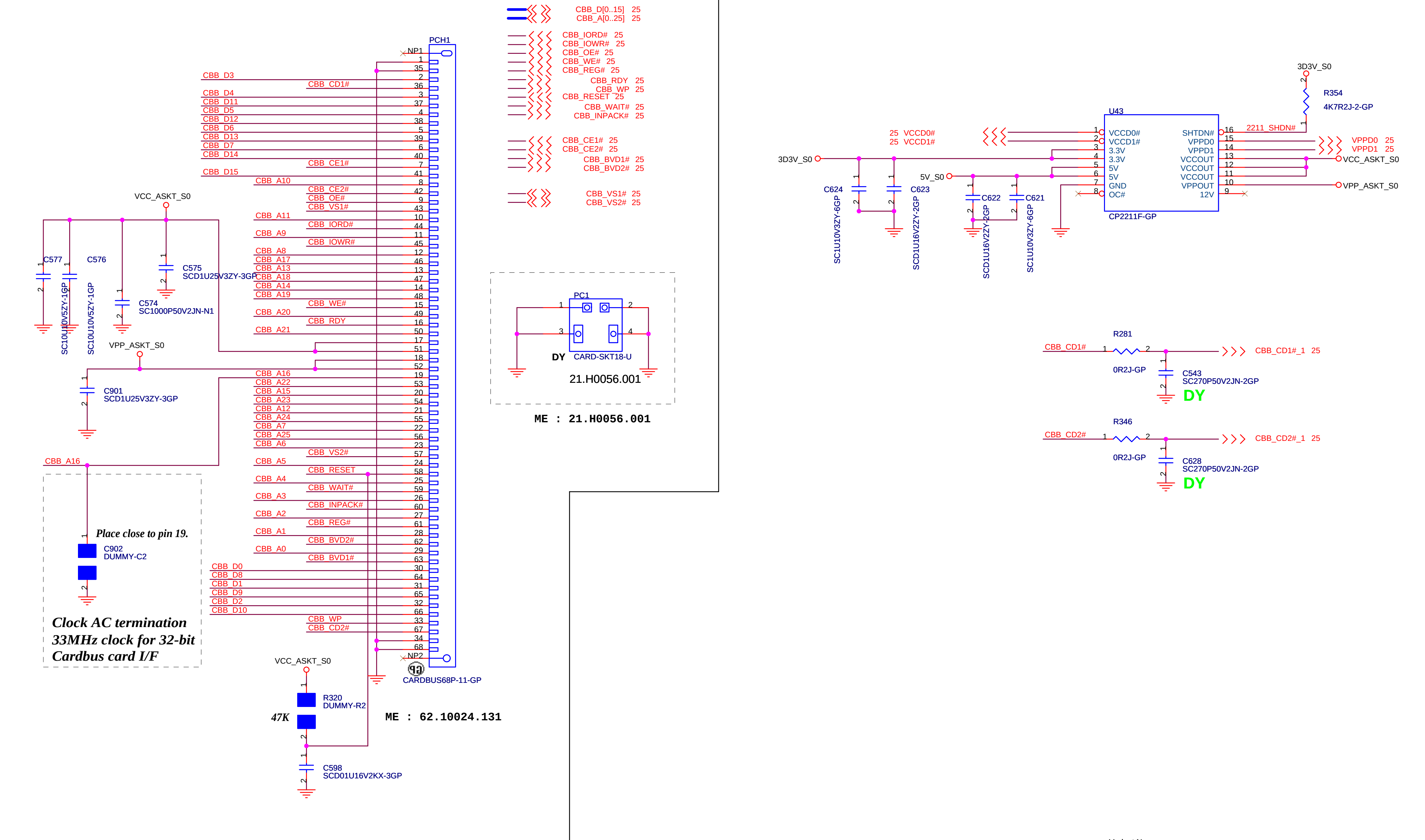
Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 25 of 58

PCMCIA Socket

Cardbus I/F

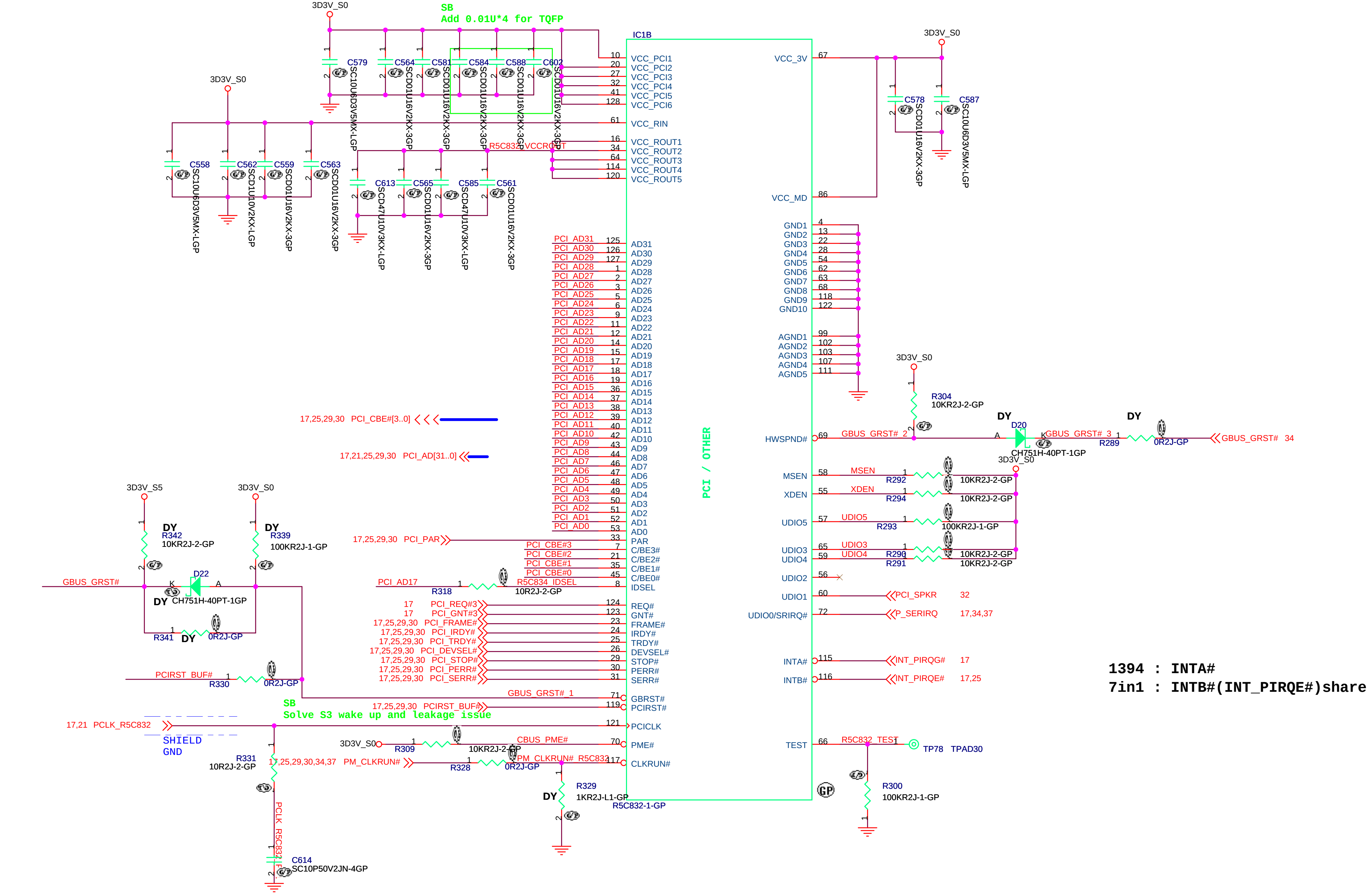
Power switch



<Variant Name>

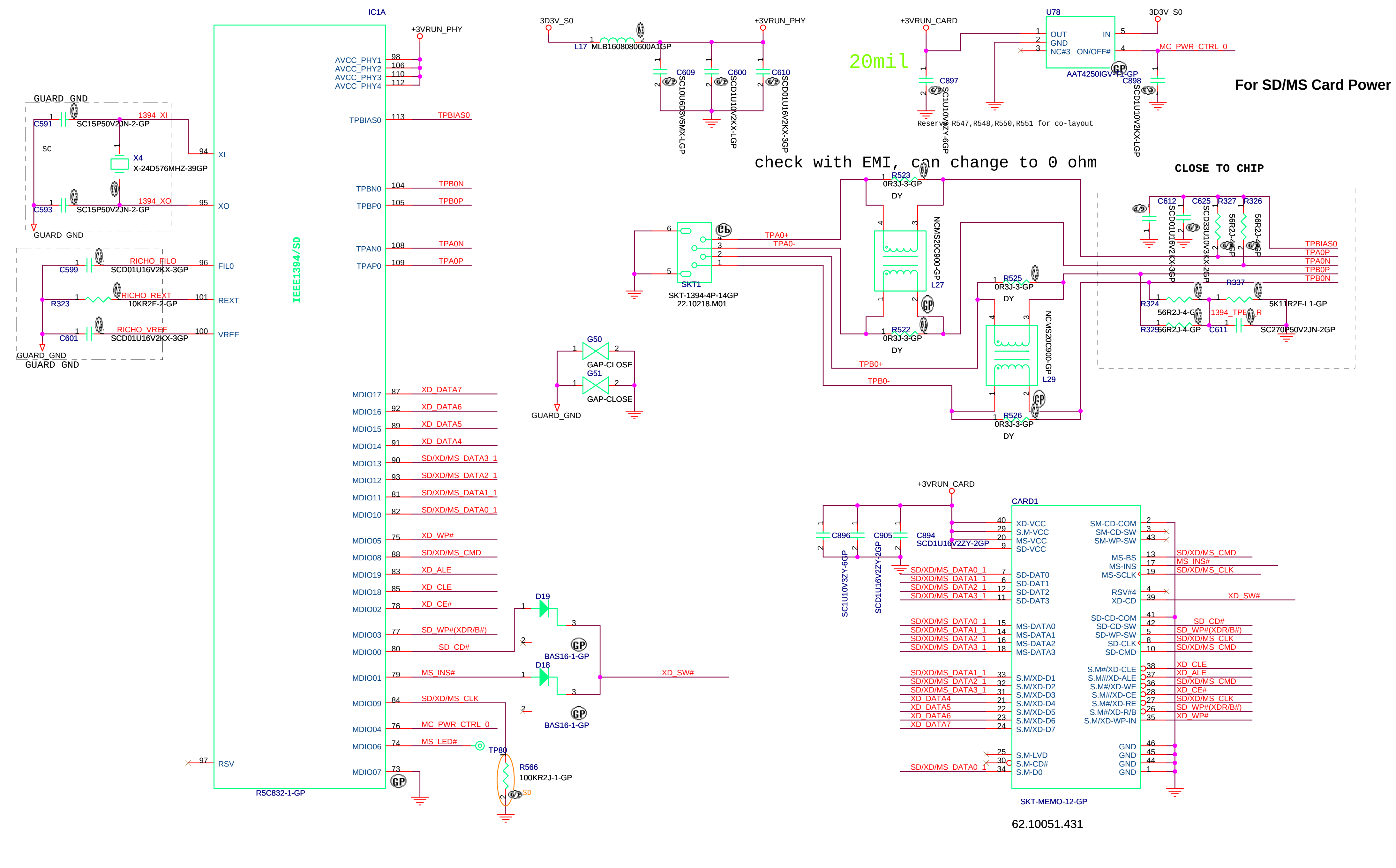
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
PCMCA / 1394 / CARD READER		
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 26 of 58	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

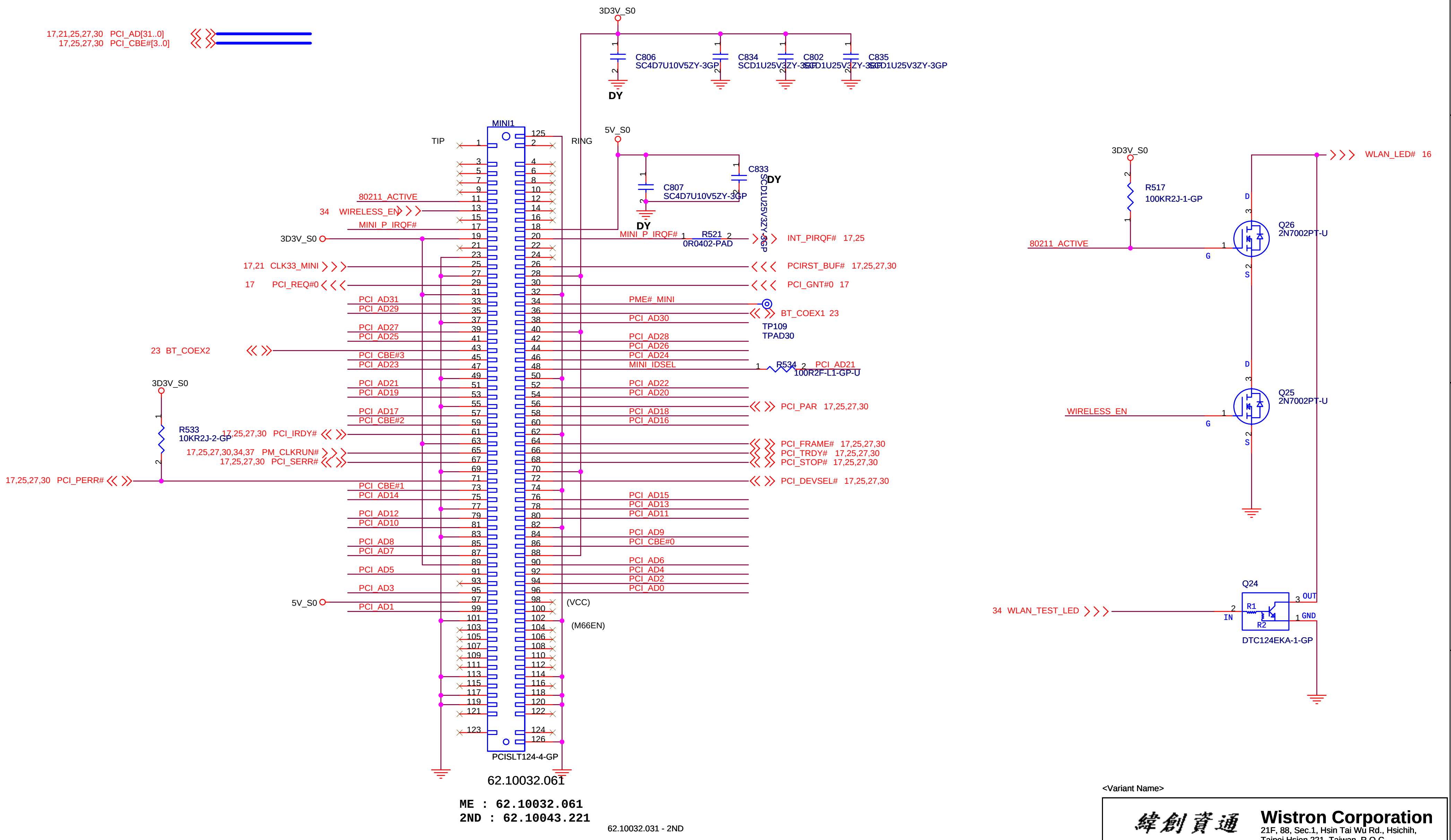
Title		
R5C832_1394_7IN1(2/2)		
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 27 of 58	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	R5C832_1394_7IN1(2/2)	
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 28 of 58	

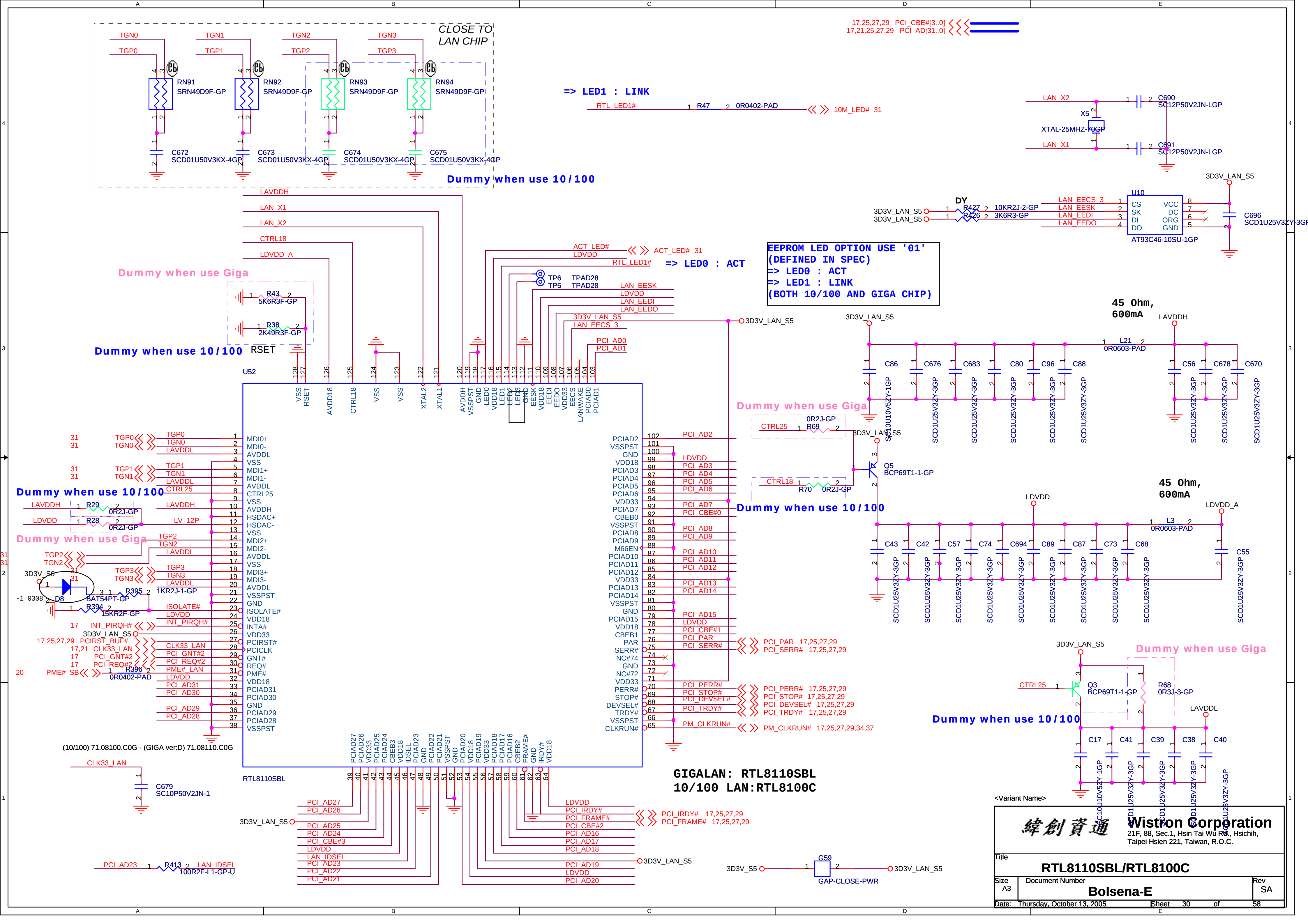
MINI-PCI



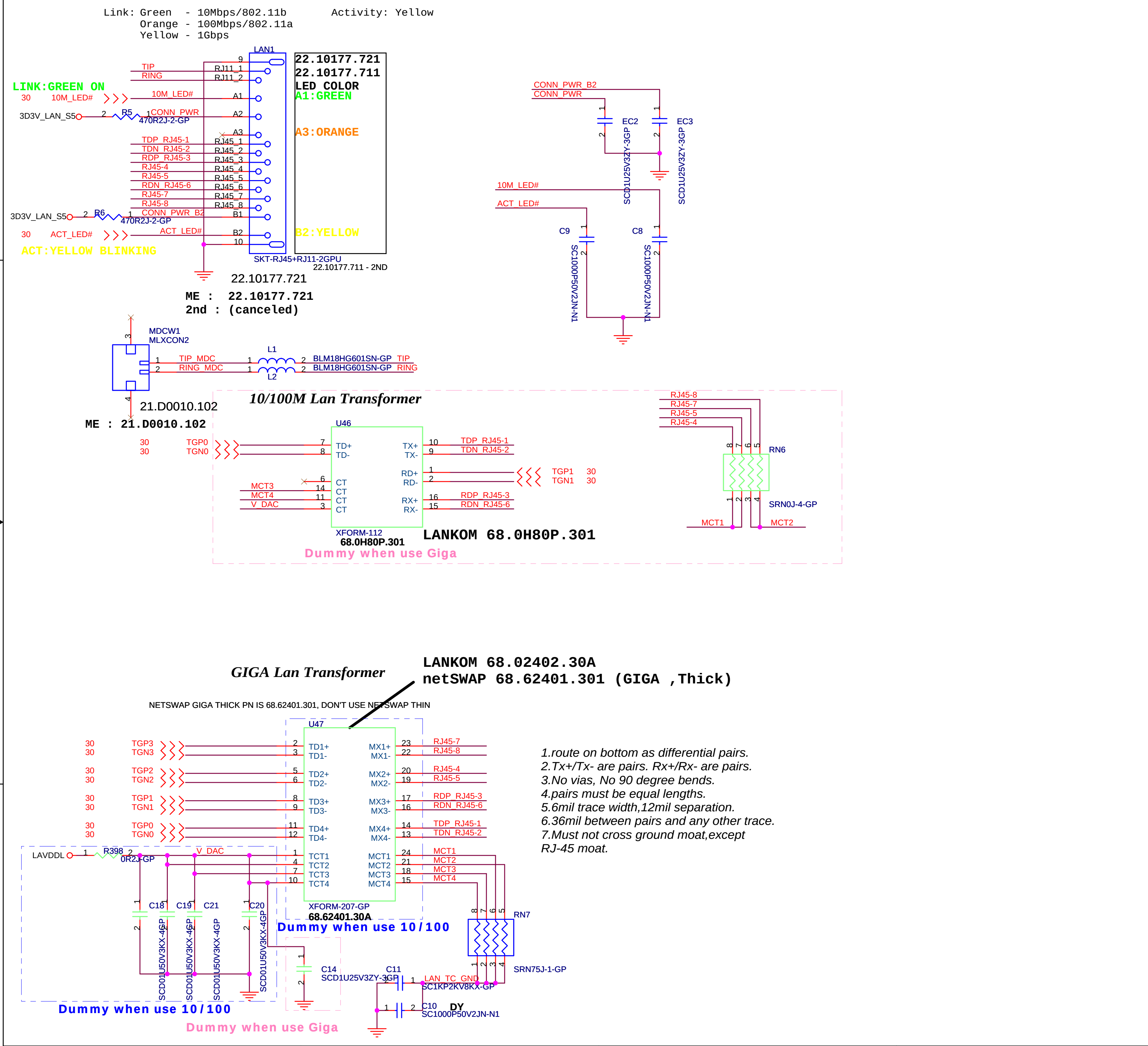
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MINI-PCI		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 29 of 58	

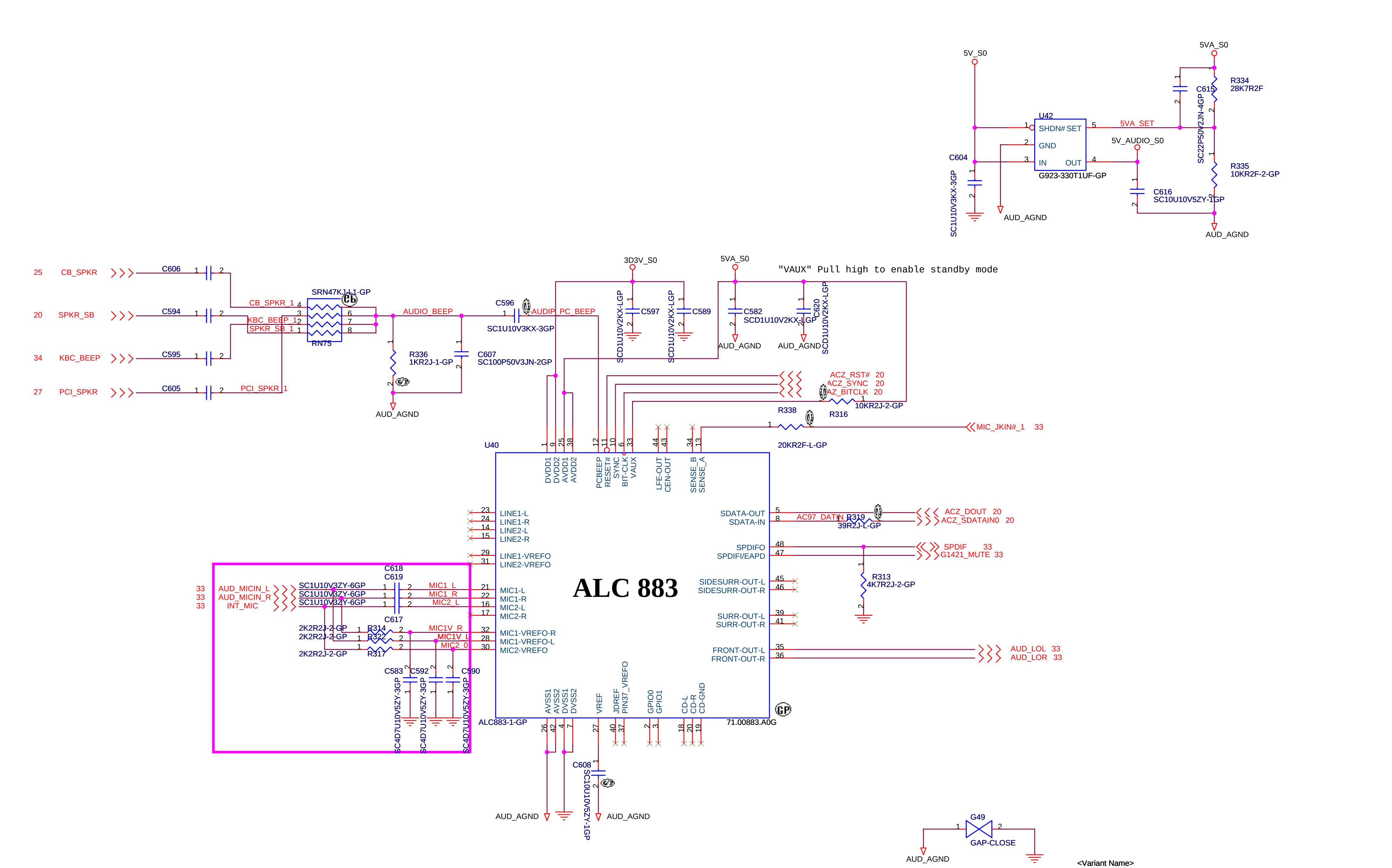


CLOSE TO LAN CHIP
RN91 SRN49D9F-GP
RN92 SRN49D9F-GP
RN93 SRN49D9F-GP
RN94 SRN49D9F-GP
C672 SCD01U50V3KX-4GP
C673 SCD01U50V3KX-4GP
C674 SCD01U50V3KX-4GP
C675 SCD01U50V3KX-4GP
Dummy when use 10/100
17,25,27,29 PCI_CBE#[3..0]
17,21,25,27,29 PCI_AD[31..0]
=> LED1 : LINK
RTL_LED1# R47 0R0402-PAD 10M_LED# 31
LAN_X2 C690 SC12P50V2JN-LGP
X5 XTAL-25MHZ-70GP
LAN_X1 C691 SC12P50V2JN-LGP
3D3V_LAN_S5
DY
R427 10KR2J-2-GP
R426 3K6R3-GP
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
U10 AT93C46-10SU-1GP
C696 SCD1U25V3ZY-3GP
ACT_LED# 31
=> LED0 : ACT
EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)
Dummy when use Giga
R43 5K6R3F-GP
R38 2K49R3F-GP
RSET
TP6 TPAD28
TP5 TPAD28
45 Ohm, 600mA
LAVDDH
L21 0R0603-PAD
C86 C676 C683 C80 C96 C88 C56 C678 C670
U52
RTL8110SBL
Dummy when use Giga
CTRL25 R69 0R2J-GP
Q5 BCP69T1-1-GP
CTRL18 R70 0R2J-GP
Dummy when use 10/100
45 Ohm, 600mA
LDVDD
LDVDD_A
L3 0R0603-PAD
C43 C42 C57 C74 C694 C89 C87 C73 C68 C55
Dummy when use 10/100
R29 0R2J-GP
R28 0R2J-GP
Dummy when use Giga
D8 BAT54PT-GP
R395 1KR2J-1-GP
R394 15KR2F-GP
R396 0R0402-PAD
(10/100) 71.08100.C0G - (GIGA ver:D) 71.08110.C0G
CLK33_LAN
C679 SC10P50V2JN-1
PCI_PAR 17,25,27,29
PCI_SERR# 17,25,27,29
3D3V_LAN_S5
Q3 BCP69T1-1-GP
R68 0R3J-3-GP
Dummy when use Giga
Dummy when use 10/100
LAVDDL
C17 C41 C39 C38 C40
PCI_PERR# 17,25,27,29
PCI_STOP# 17,25,27,29
PCI_DEVSEL# 17,25,27,29
PCI_TRDY# 17,25,27,29
PM_CLKRUN# 17,25,27,29,34,37
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
PCI_IRDY# 17,25,27,29
PCI_FRAME# 17,25,27,29
R413 100R2F-L1-GP-U
G59 GAP-CLOSE-PWR
3D3V_S5
<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8110SBL/RTL8100C
Size A3
Document Number
Bolsena-E
Rev SA
Date: Thursday, October 13, 2005
Sheet 30 of 58



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

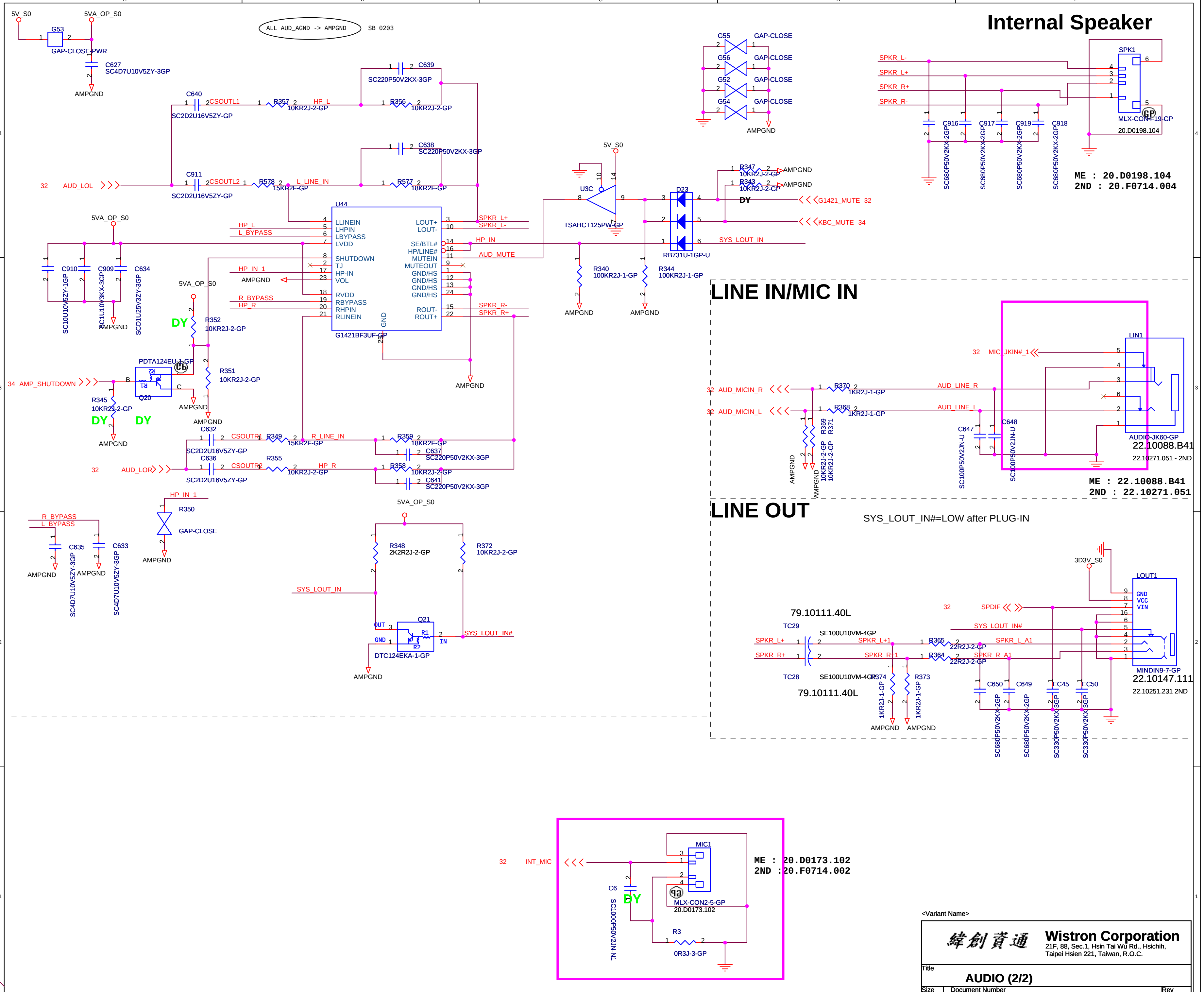
Title	LAN CONN	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 31 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO (1/2) -- CODEC ALC655	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 32 of 58	



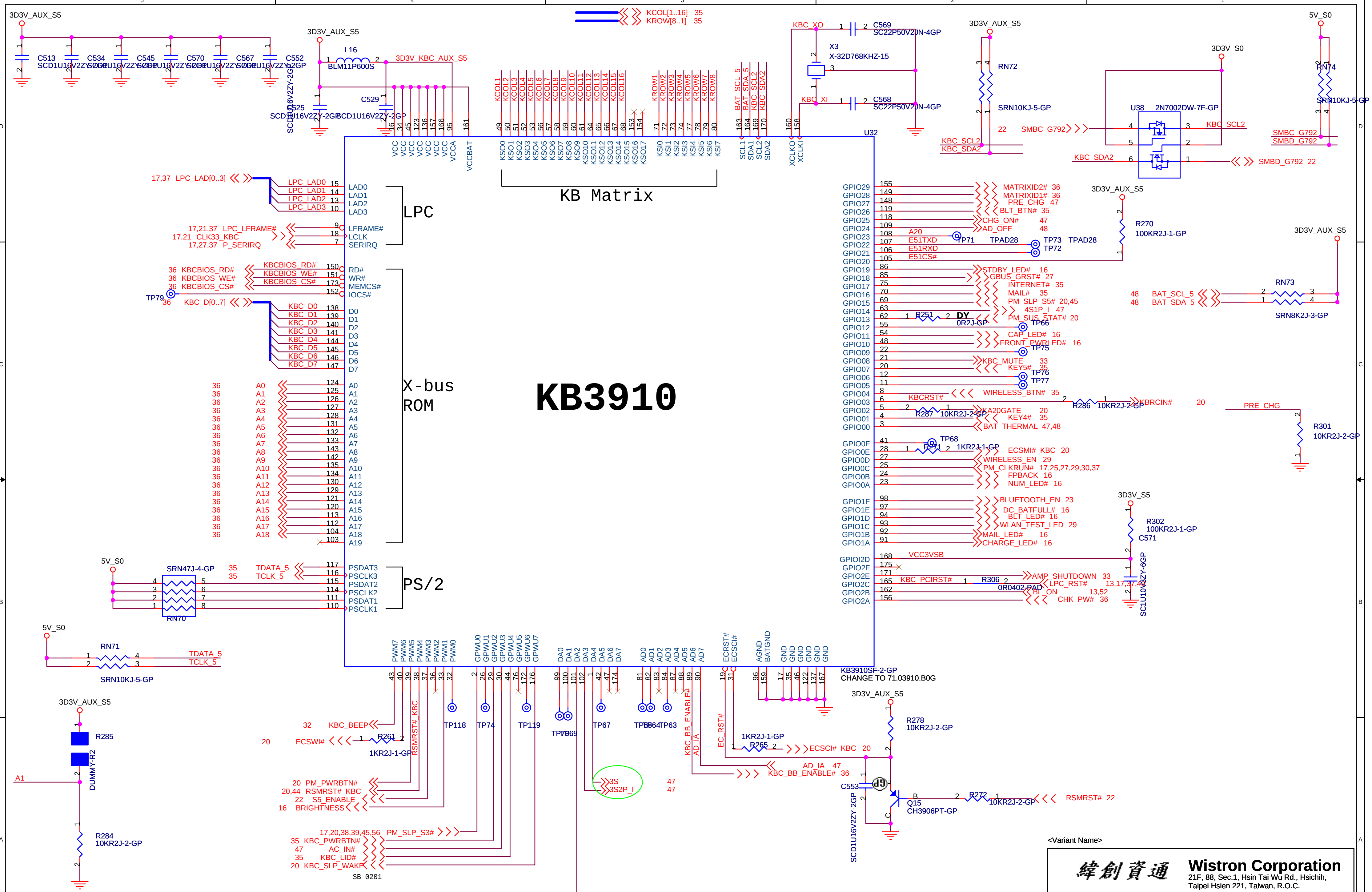
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (2/2)**

Size	Document Number	Rev
Custom	Bolsena-E	SA

Date: Thursday, October 13, 2005 | Sheet 33 of 58

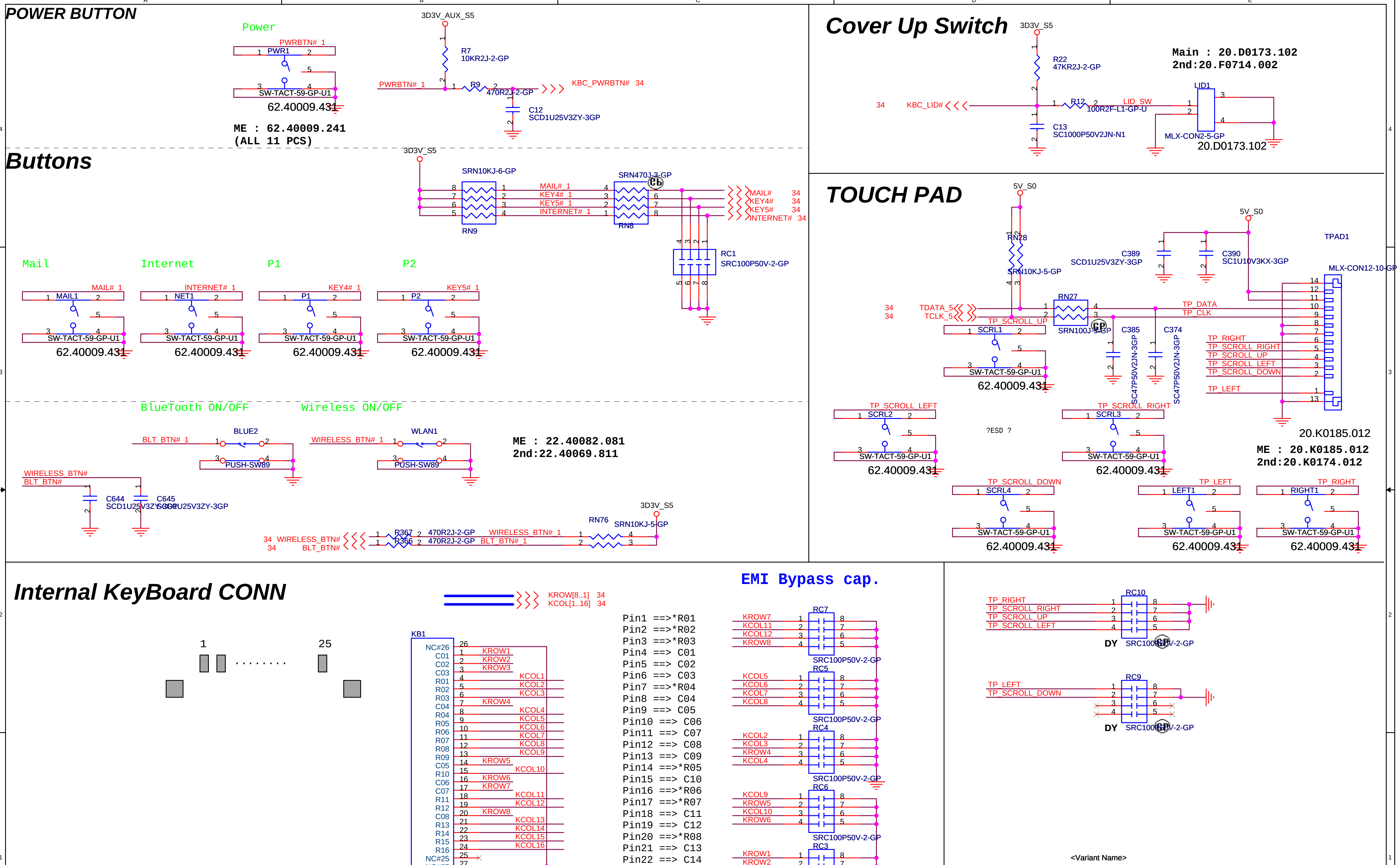


A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPI005 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPI006 for DPLL test mode==>High=Test Mode,Low=Normal operation(Recommended)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
KBC KB3910		
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 34 of 58	



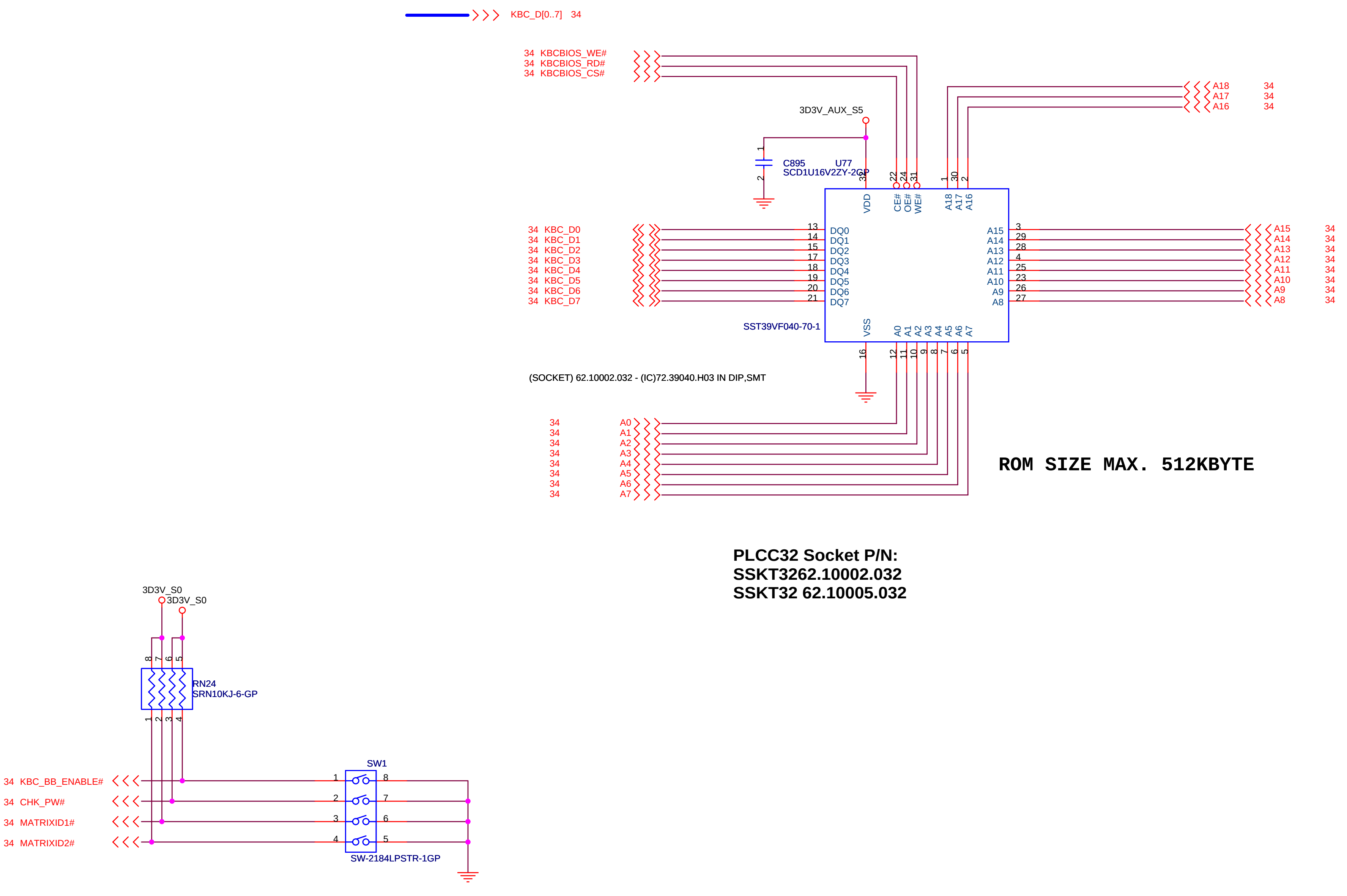
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
BUTTONs / KB / TOUCHPAD

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 | Sheet 35 of 58



ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032

Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

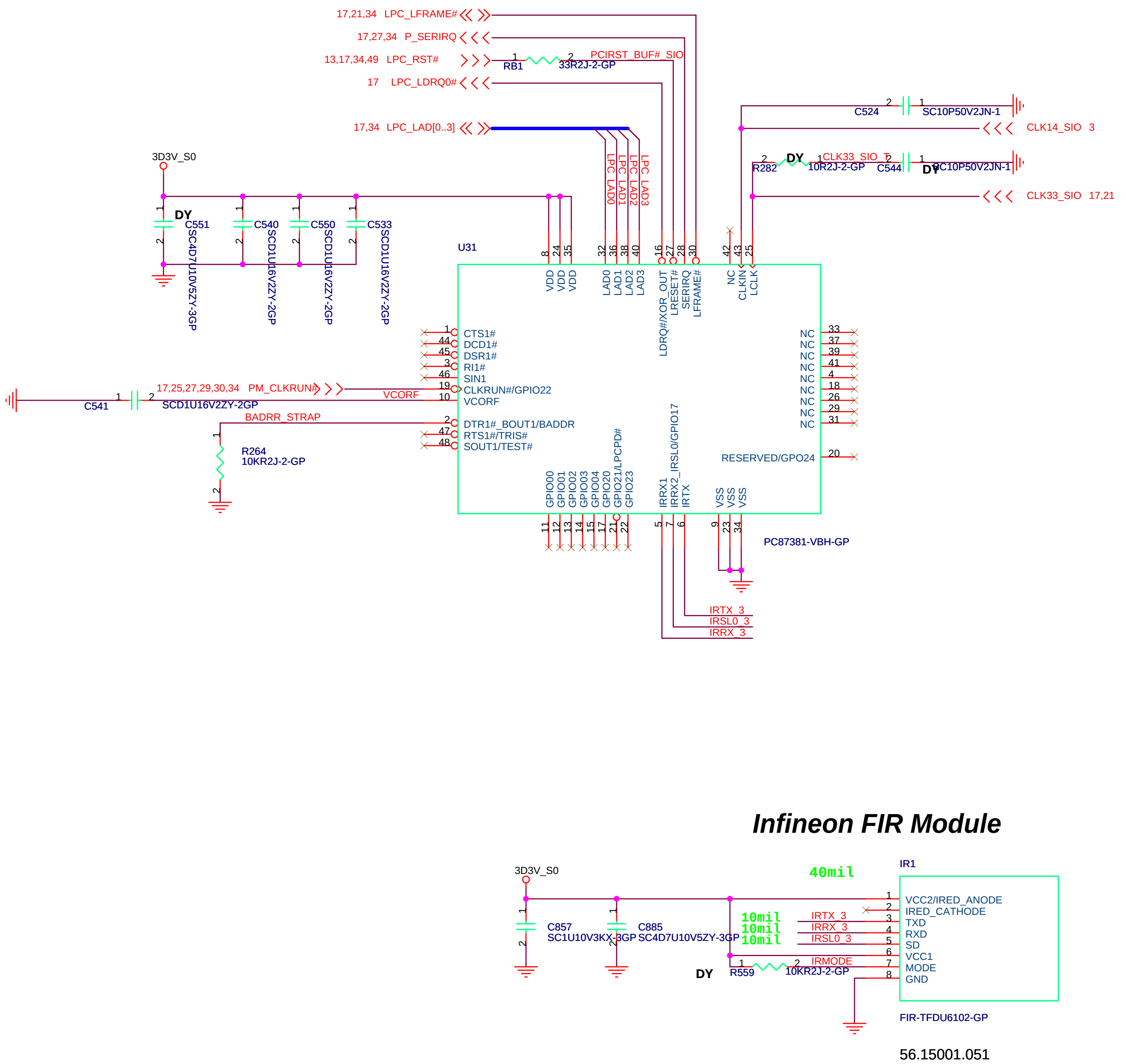
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

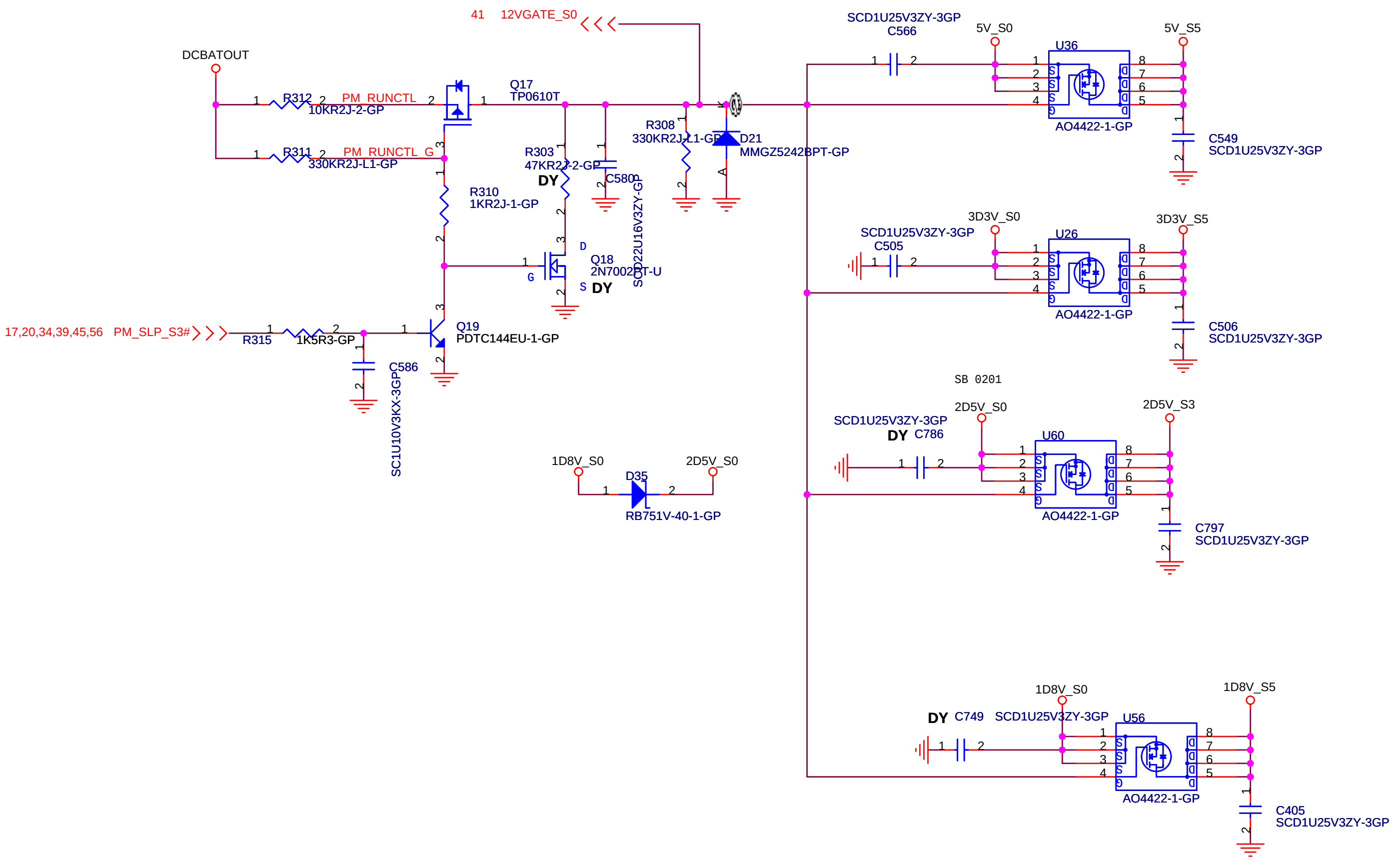
Size: A3 | Document Number: **Bolsena-E** | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 36 of 58



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: **SUPER IO NC87381**		
Size: A3	Document Number: **SNIPE**	Rev: -2
Date: Thursday, October 13, 2005	Sheet 37 of 58	

Run Power



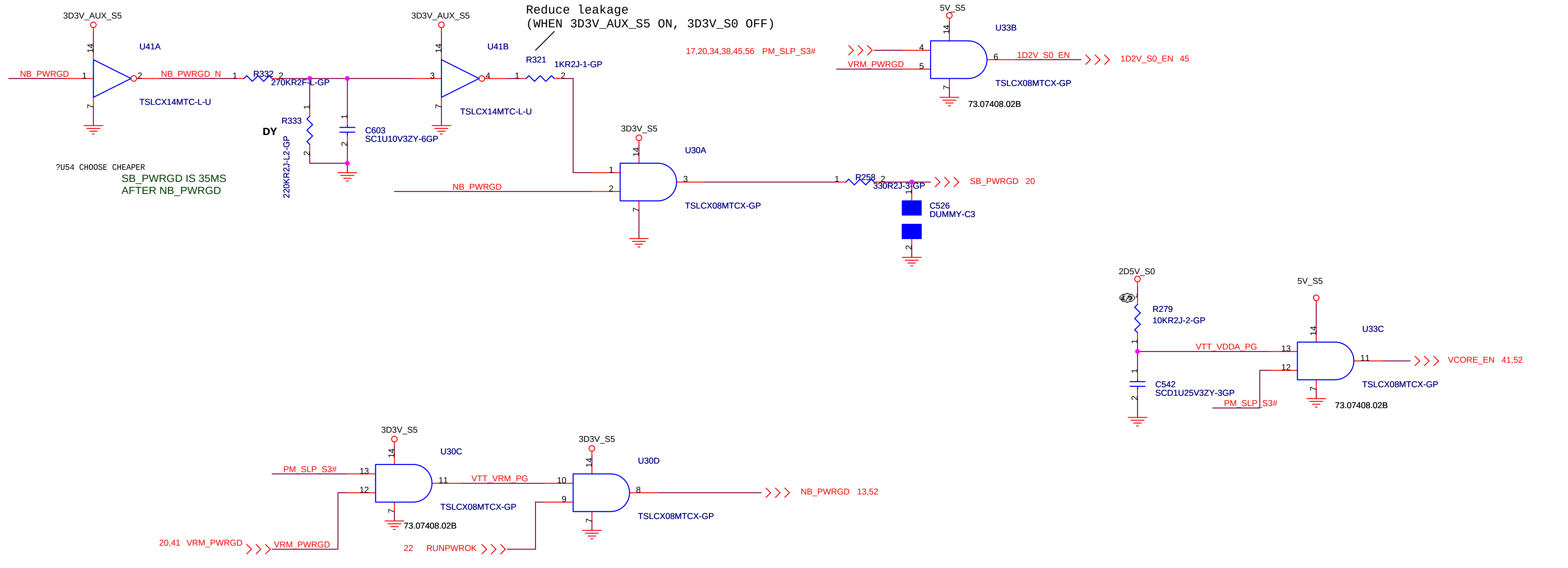
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PWR CTL LOGIC / PWR PLANE**

Size: A3 | Document Number: **Bolsena-E** | Rev: SA

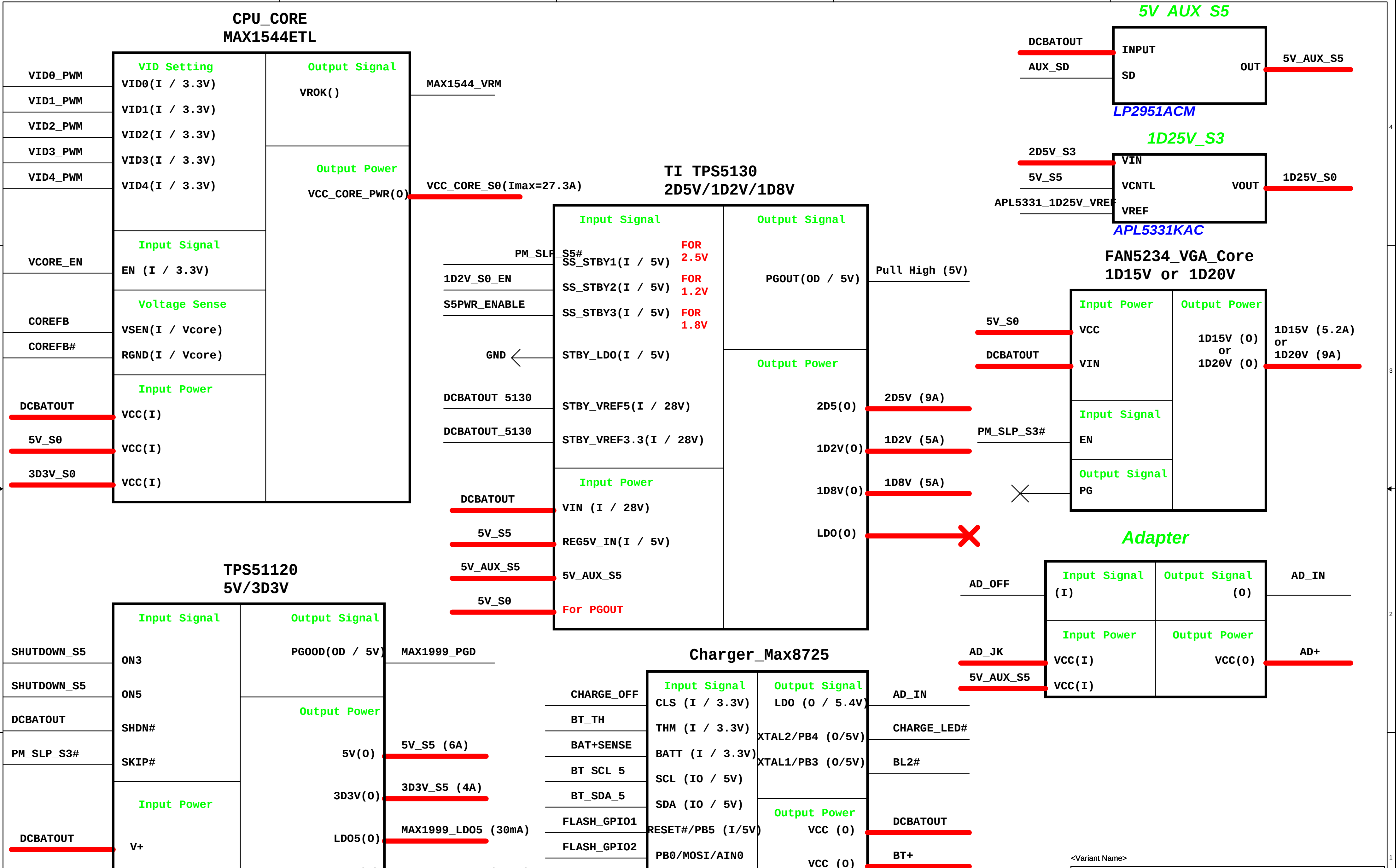
Date: Thursday, October 13, 2005 |



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**POWERGOOD&ENABLES**	
Size: Custom	Document Number: **Bolsena-E**	Rev: SA
Date: Thursday, October 13, 2005	Sheet 39 of 58	



(Power Team)

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
POWER BLOCK DIAGRAM

Size	Document Number	Rev
A3	Bolsena-E	SA

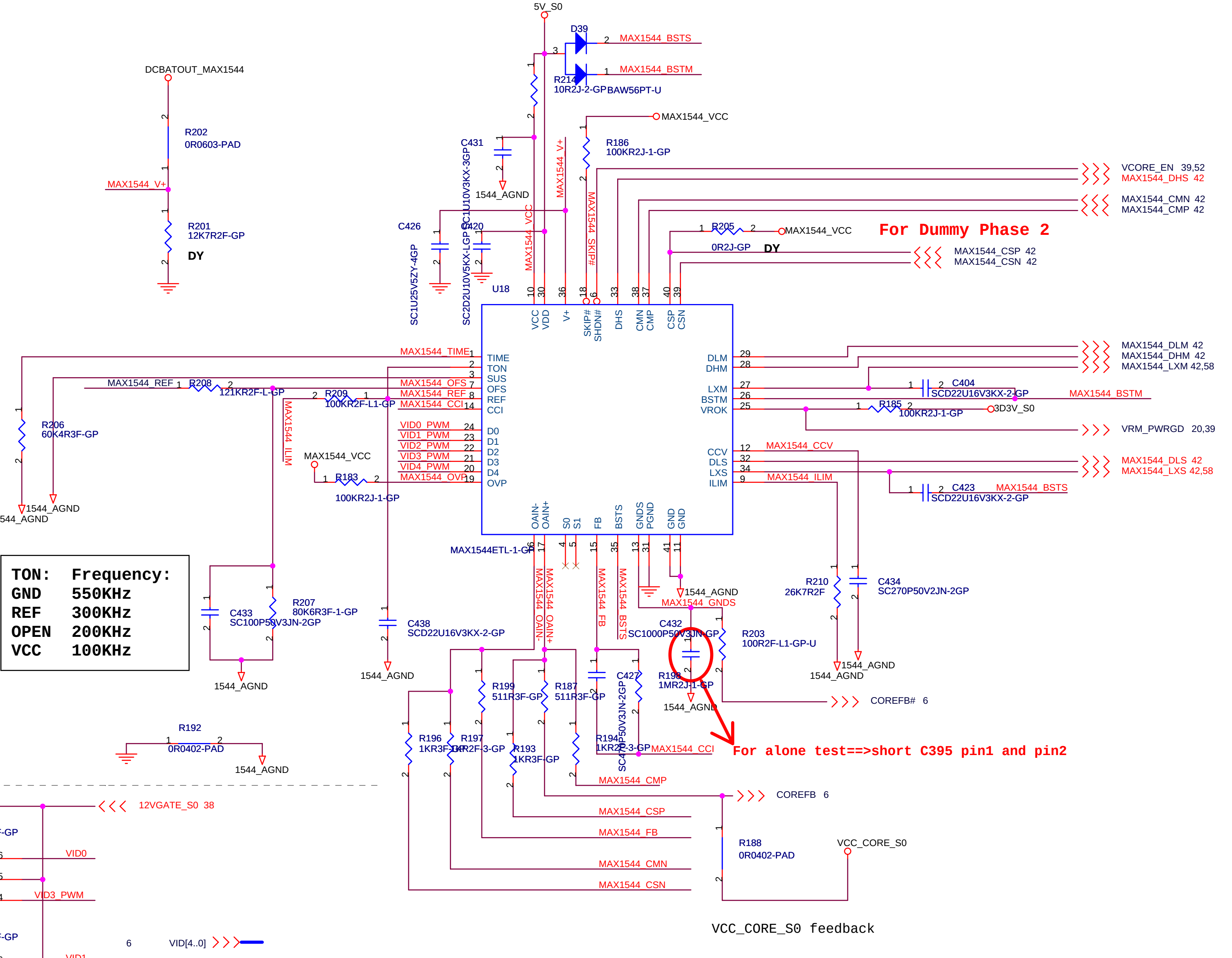
Date: Thursday, October 13, 2005 Sheet 40 of 58

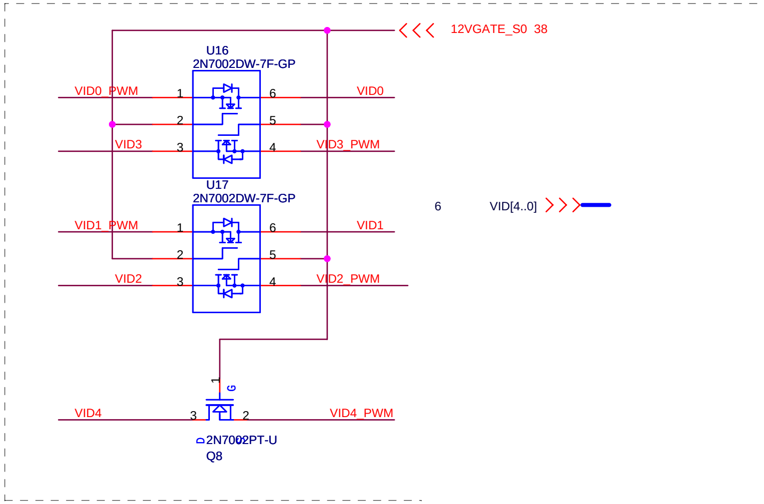
CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)
OCP=40A~45A

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

TON:	Frequency:
GND	550KHz
REF	300KHz
OPEN	200KHz
VCC	100KHz





From KBC

(Power Team)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CPU Vcore 1	
Size A3	Document Number: Bolsena-E	Rev SA
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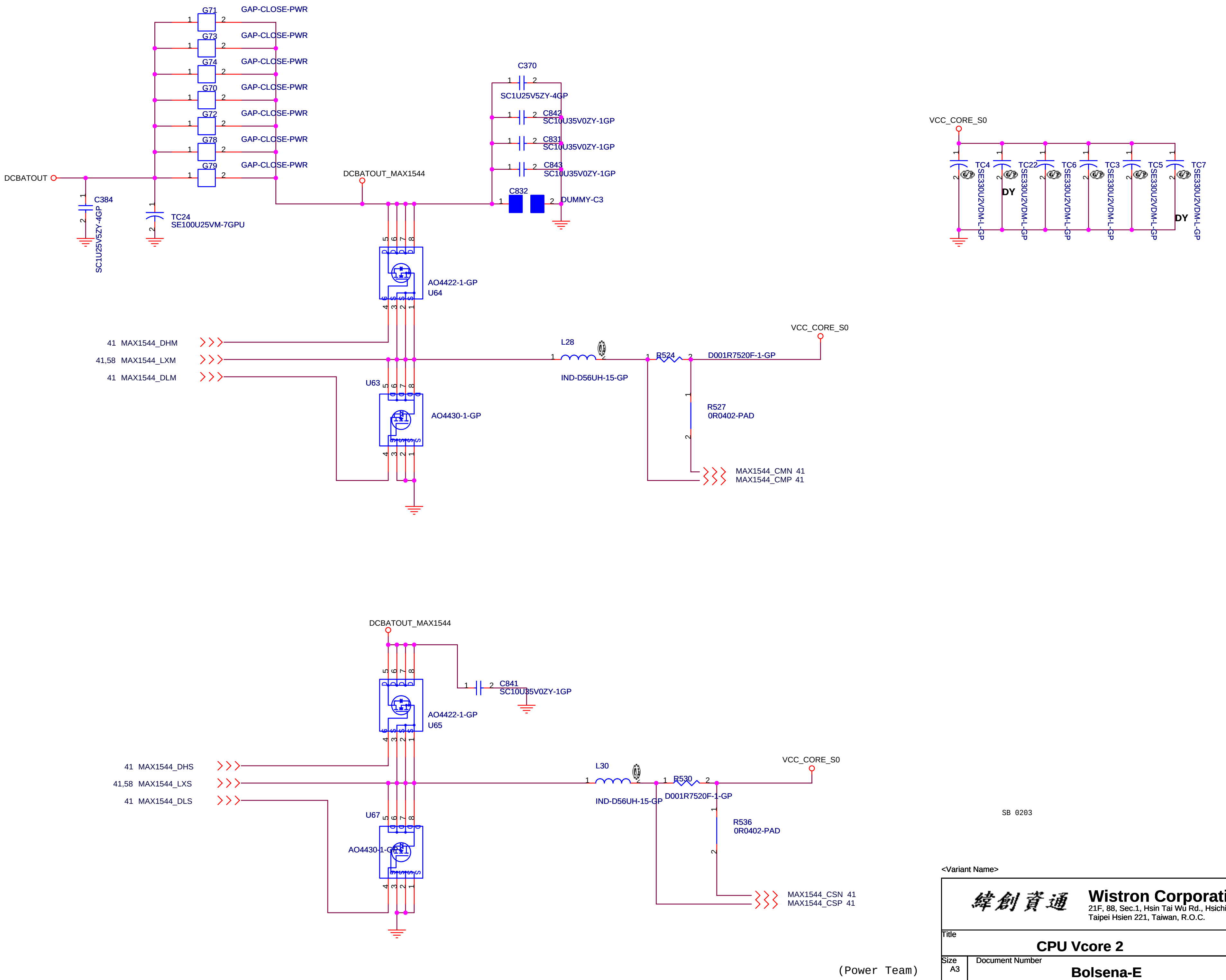
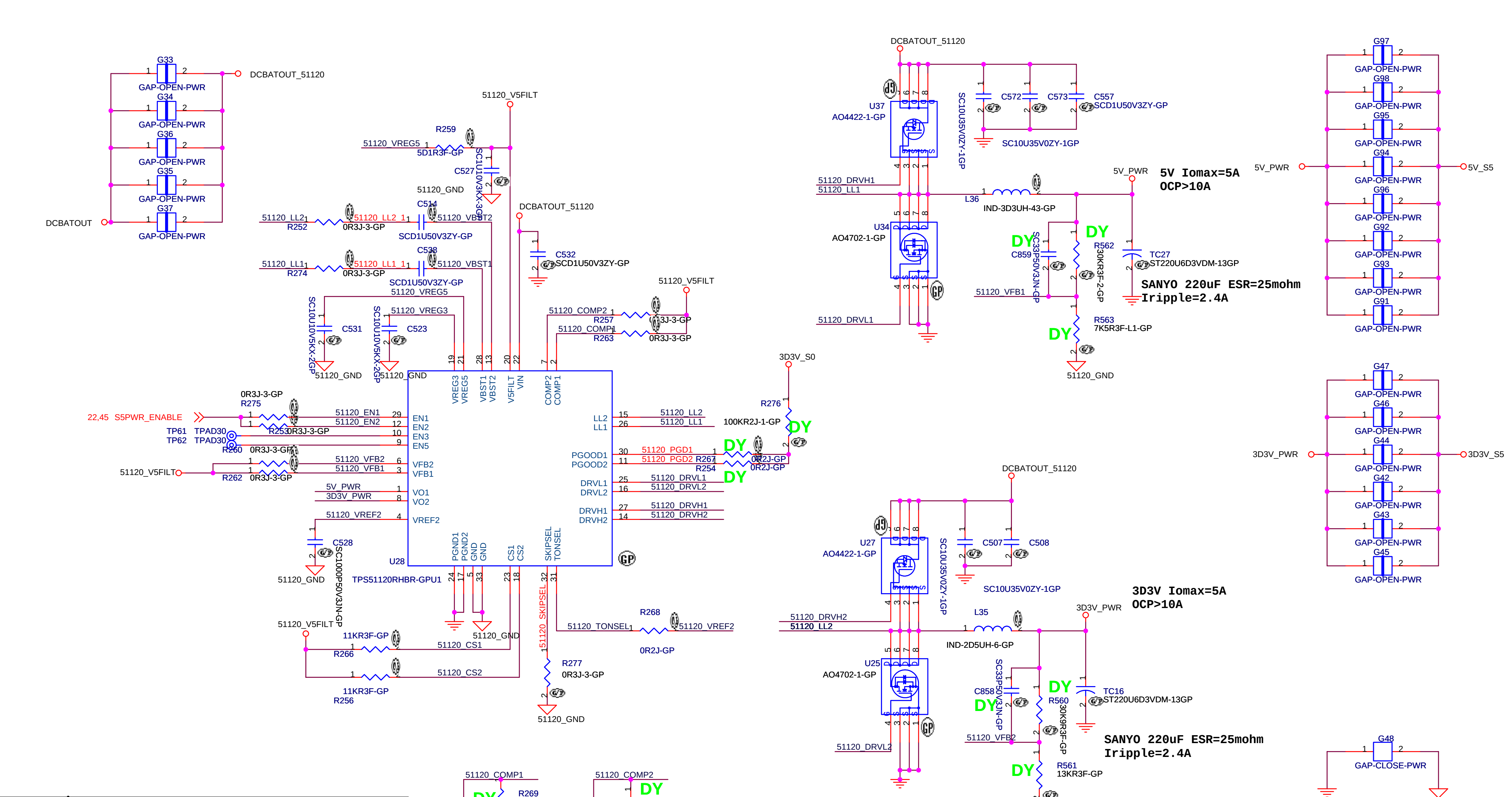


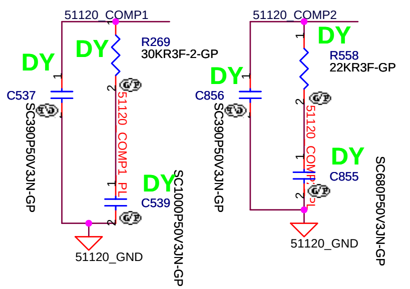
<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title		
CPU Vcore 2		
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 42 of 58	





	GND	VREF2	FLOAT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	220k/CH1 330k/CH2	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Swithchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 on

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.
Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

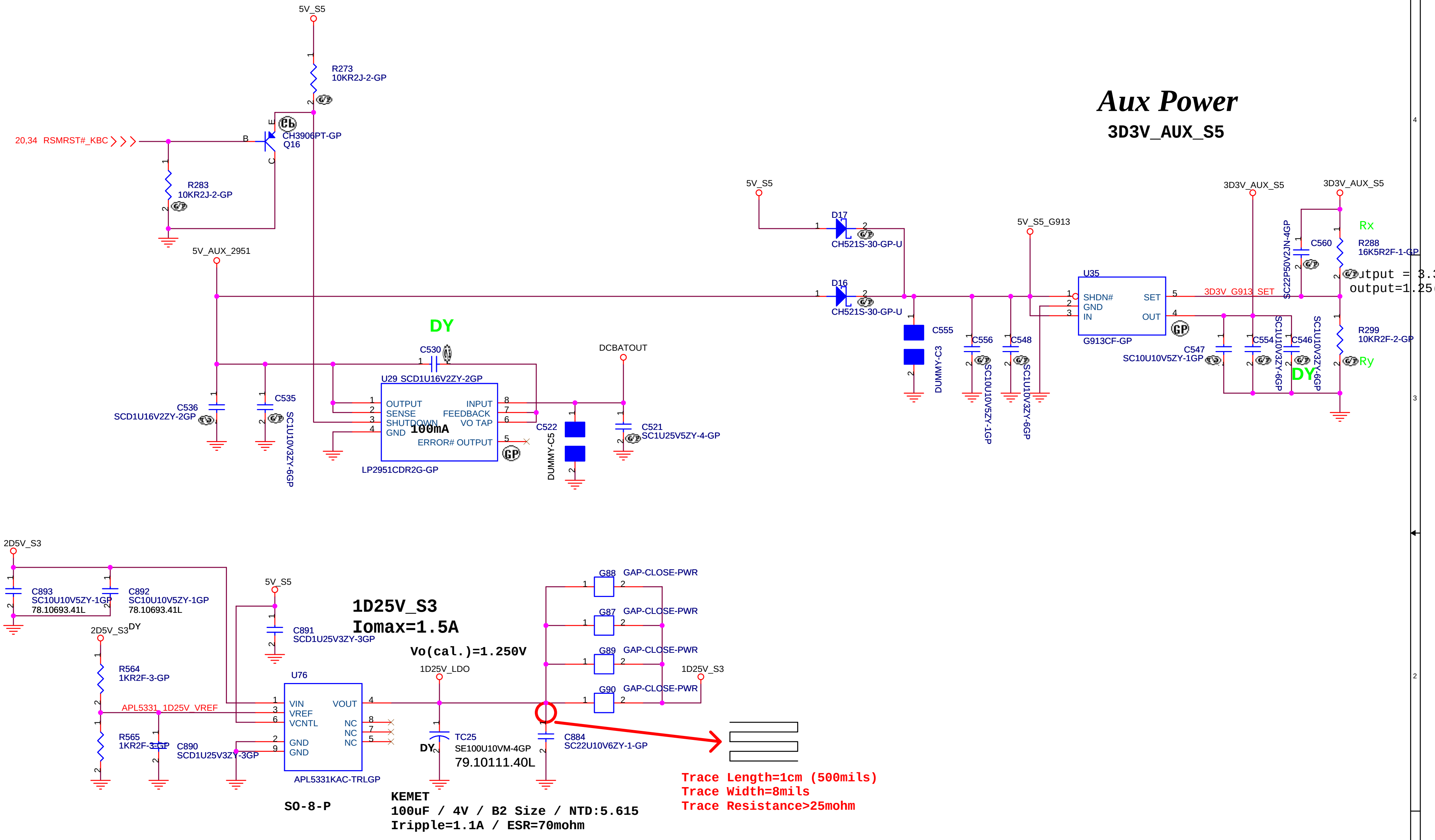
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	TPS51120 / 3D3V / 5V	
Size A3	Document Number Bolsena-E	Rev -1
Date: Thursday, October 13, 2005	Sheet 43 of 58	

Aux Power

3D3V_AUX_S5



(Power Team)

<Variant Name>

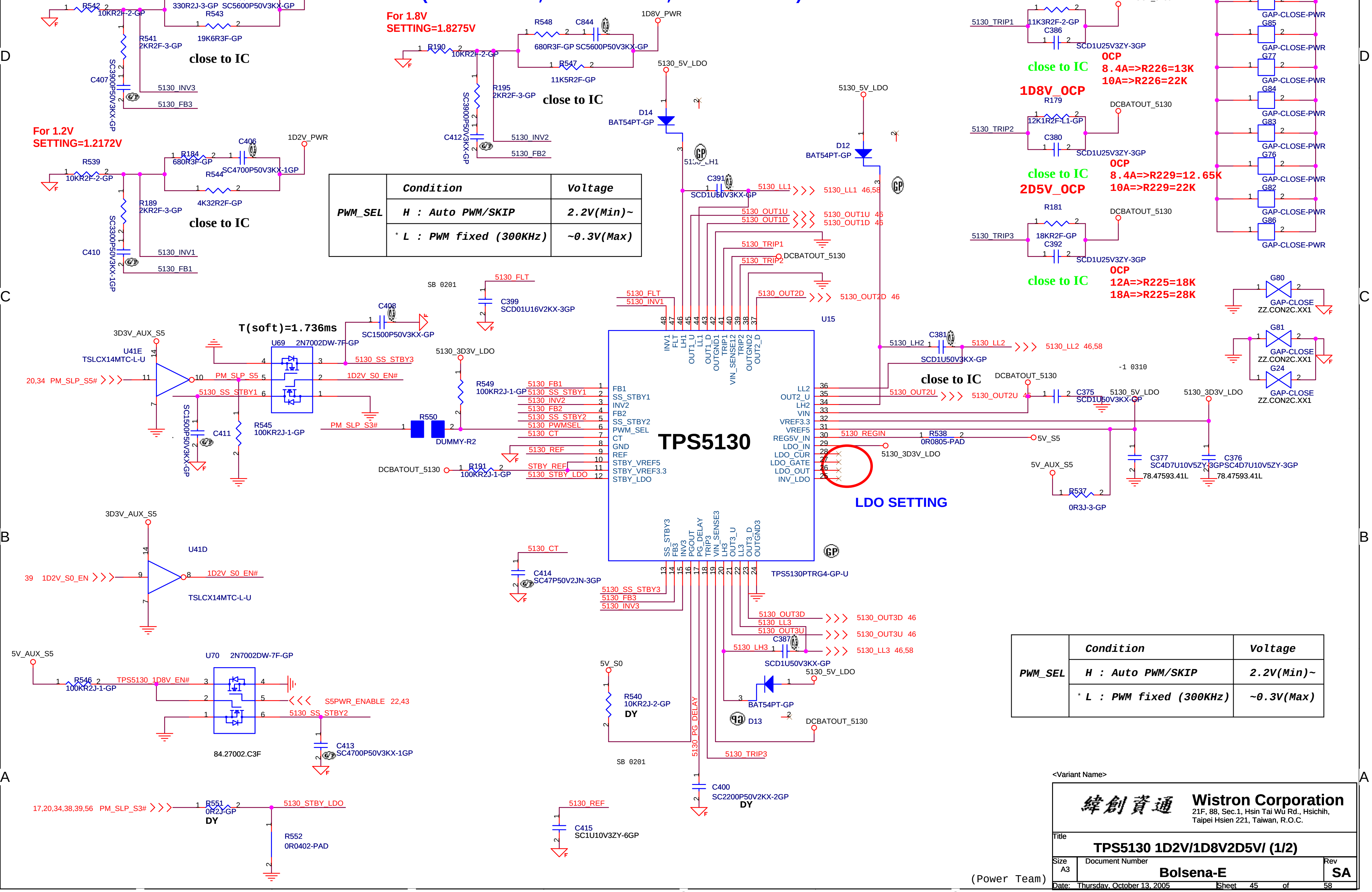
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	1D2V_S3 / 3D3V_AUX		
Size A3	Document Number	Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 44	of	58

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)



PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

(Power Team)

<Variant Name>

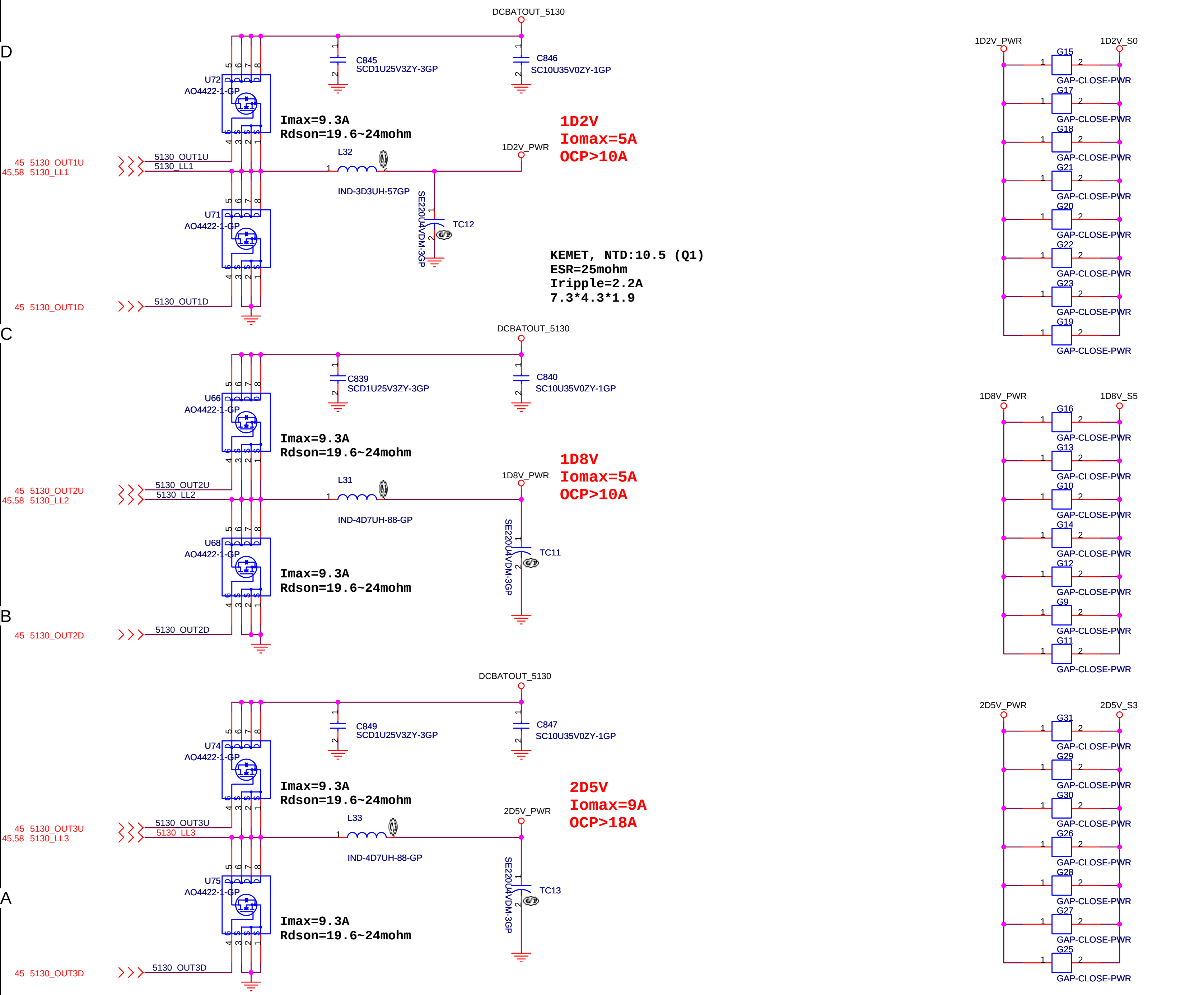
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS5130 1D2V/1D8V2D5V/ (1/2)

Size	Document Number	Rev
A3	Bolsena-E	SA

TI TPS5130 for 2D5V, 1D2V, 1D8V

(1D2V=>CH1 , 1D8V=>CH2 , 2D5V =>CH3)

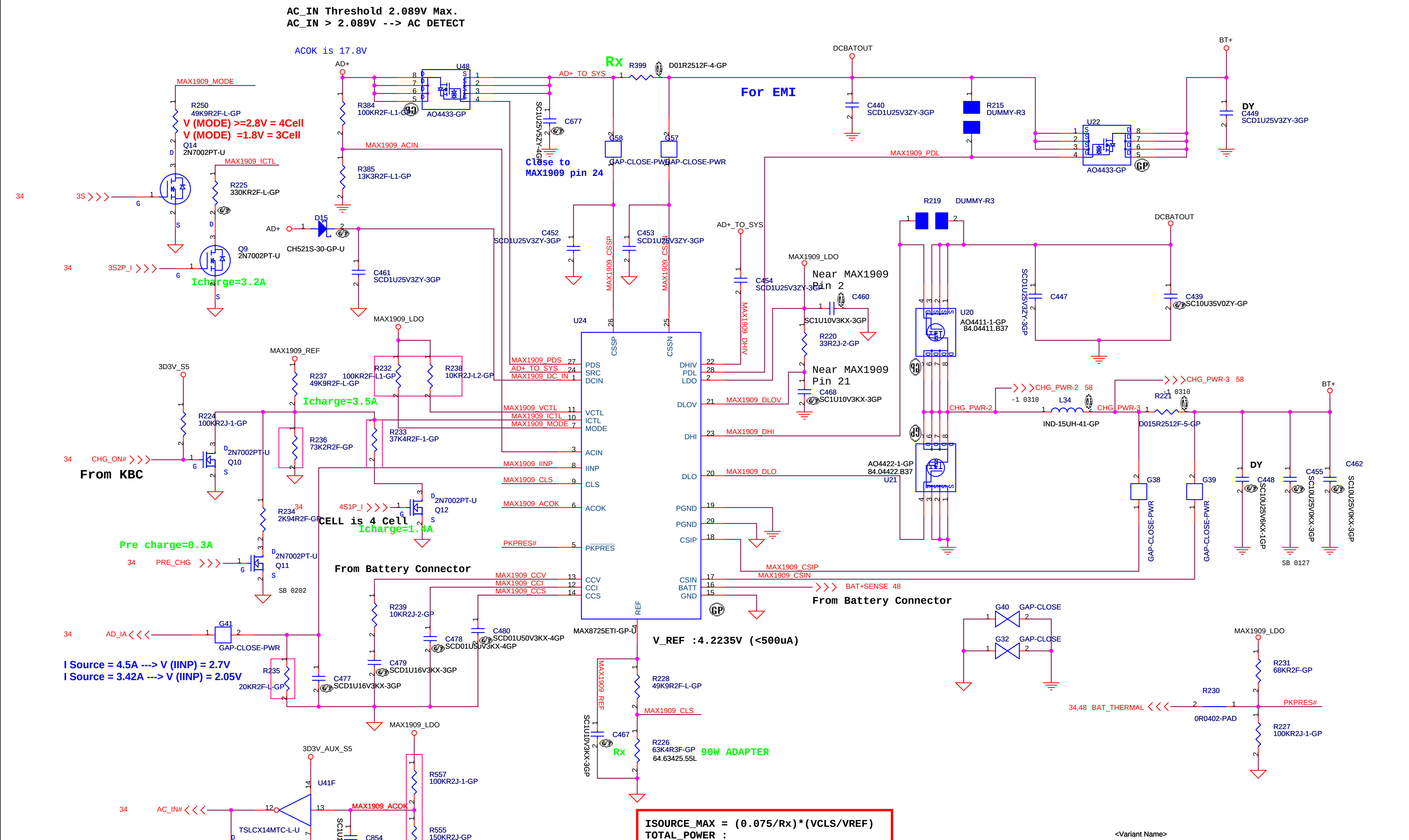


(Power Team)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
TPS5130 1D2V/1D8V2D5V/ (2/2)		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 46 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER MAX8725
Size: Custom	Document Number: Bolsena-E
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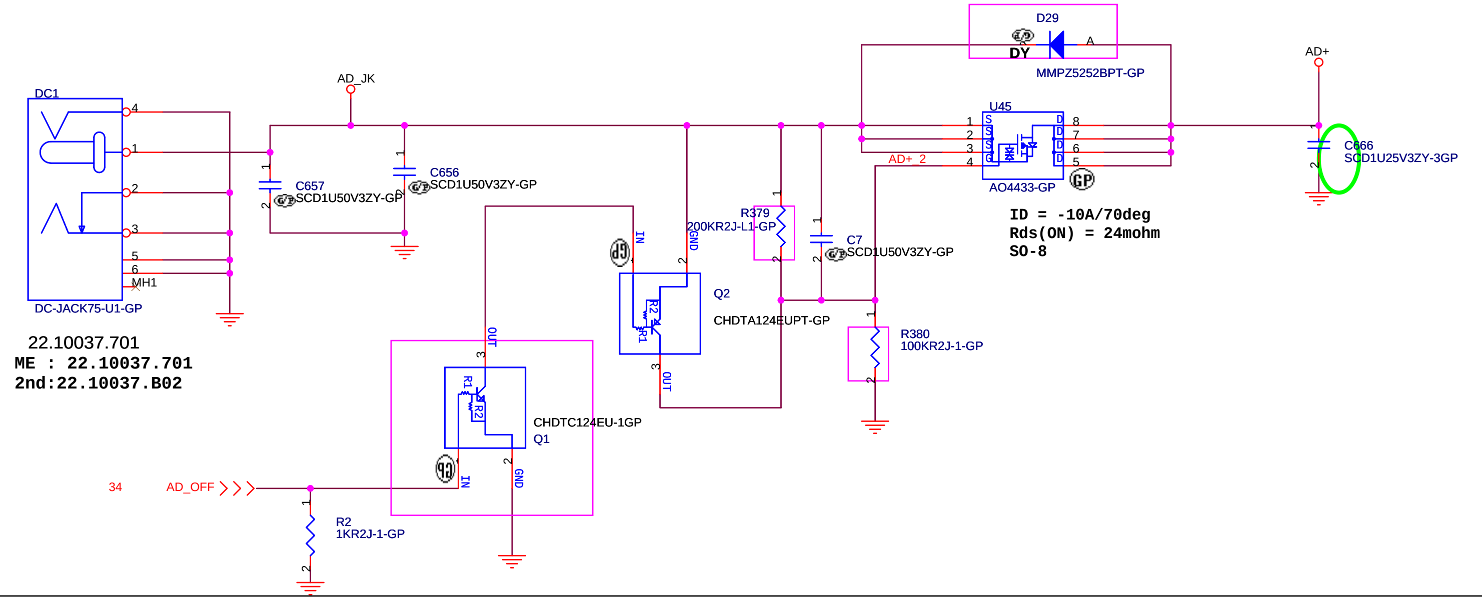
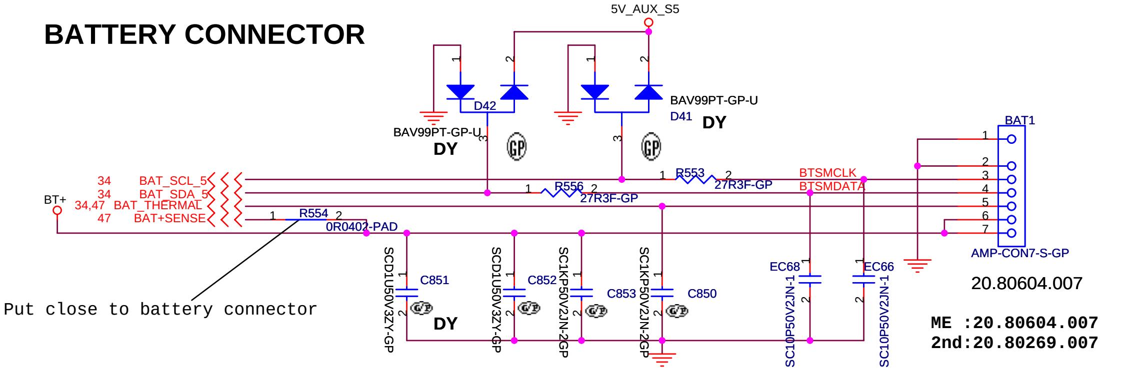
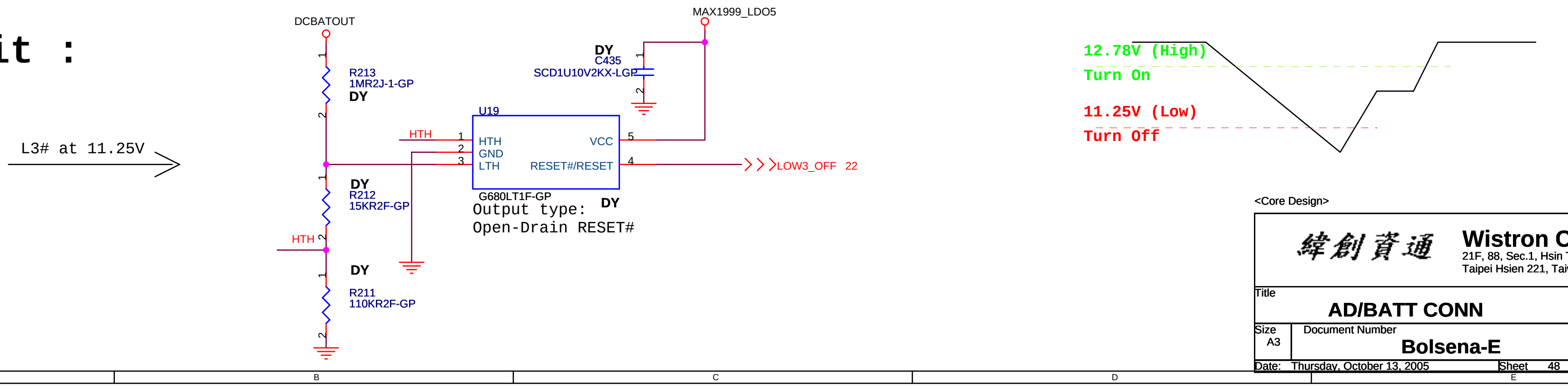
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



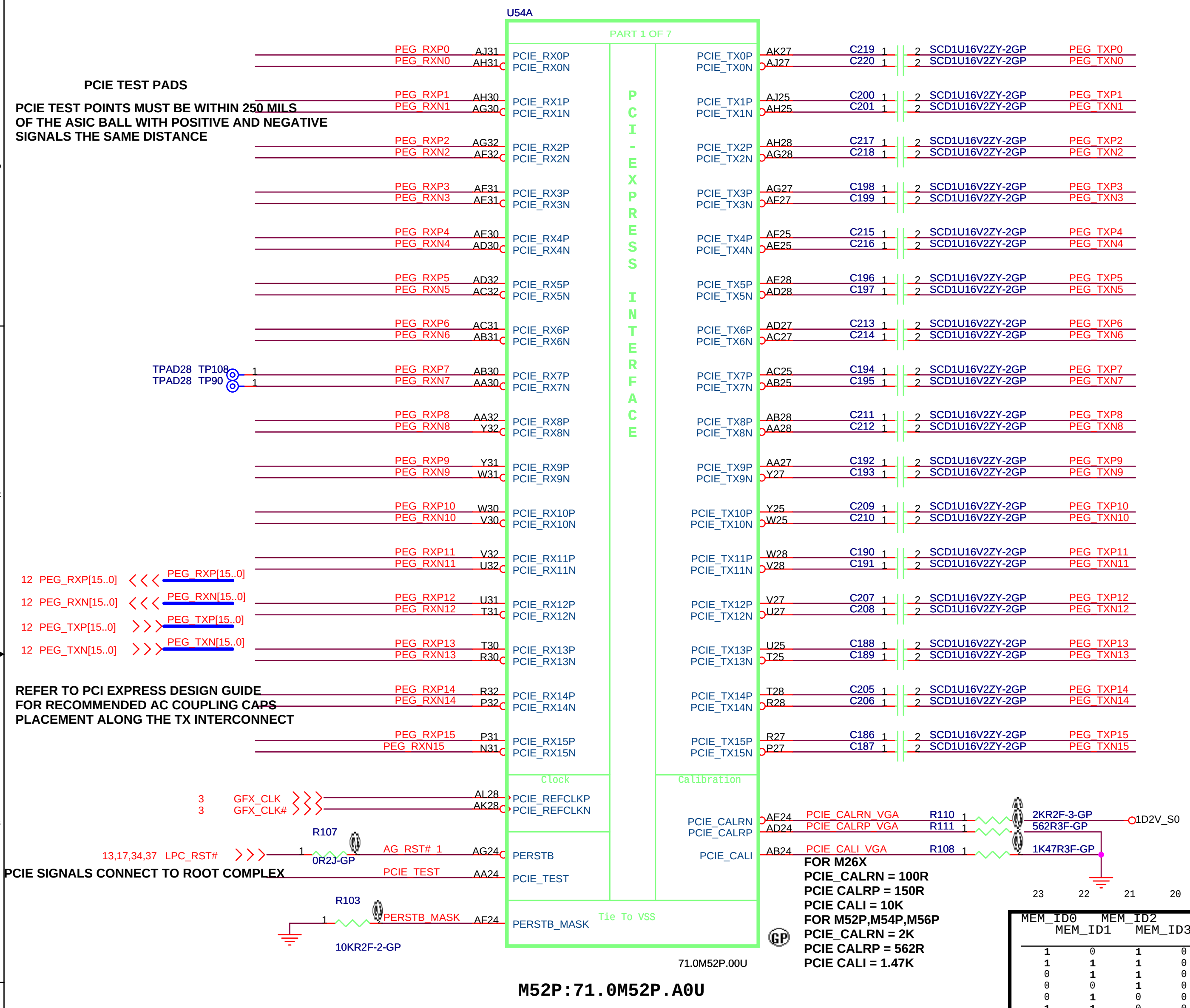
Low3 Circuit :



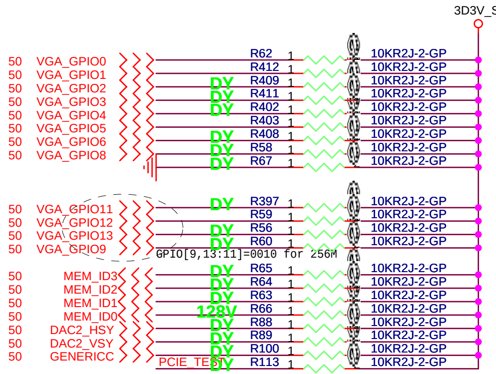
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	AD/BATT CONN	
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 48 of 58	



STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED
STRAP_B_PTX_PWRS_ENB	GPIO0	TRANSMITTER POWER SAVINGS ENABLE - FULL TX OUTPUT SWING	INSTALL 10K RESISTOR
STRAP_B_PTX_DEEMPH_EN	GPIO1	TRANSMITTER DE-EMPHASIS ENABLE DEPENDS ON PCIE CHIPSET BEING USED FOR M26X,M5X INSTALL WITH ATI RS480,RS400,RX480, RC410,RS482 CHIPSETS FOR M26X ONLY DO NOT INSTALL WITH INTEL 915PM CHIPSET	TBD
RSVD	GPIO(3:2)	NO ATI FEATURE ENABLED	DO NOT INSTALL 10K RESISTORS
REVERSE LANES DEBUG ACCESS	GPIO4	NOT REVERSED LANE (M26X) NO DEBUG ACCESS (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTOR
STRAP_FORCE_COMPLIANCE sets the desired PCIE PLL bandwidth for M5x parts.	GPIO5	DO NOT FORCE COMPLIANCE STATE QUICKLY (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	INSTALL 10K RESISTORS
COMMON MODE RANGE RSVD	GPIO6	NORMAL RANGE (M26X) NO ATI FEATURE ENABLED (M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
DEBUG ACCESS FORCE_COMPLIANCE	GPIO8	NO DEBUG ACCESS (M26X) DON'T FORCE COMPLIANCE STATE(M52P,M54P,M56P)	DO NOT INSTALL 10K RESISTORS
ROMIDCFG(3:0)	GPIO[9,13:11]	SERIAL FLASH ROM TYPE (M26X,M52P,M54P,M56P) - SERIAL M25P10 ROM	1011
MEMORY APERTURE SIZE	GPIO[13:11]	IF NO ROM GPIO11(M26X) AND GPIO12,13(M52,M54,M56) SET MEMORY APERTURE SIZE SEE M26X,M54X,M56X DATA BOOK FOR MEMORY,FRAME BUFFER APERATURE SETTINGS	TBD
MEM_TYPE	MEMID (3:0)	MEMORY TYPE AND SPEED SELECT	TBD
RSVD NO STRAP FUNCTION	H2SYNC V2SYNC GENERICC	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	DO NOT INSTALL 10K RESISTORS
RSVD NO STRAP FUNCTION	PCIE_TEST	ATI FEATURE NOT ENABLED (M52P,M54P,M56P) NO STRAP (M26X)	



23 22 21 20

MEM_ID0	MEM_ID1	MEM_ID2	MEM_ID3	MEM	SIZE	VENDOR	CHIPs
1	0	1	0	64M	16M*16	Infineon	x2
1	1	1	0	64M	16M*16	Hynix	x2
0	1	1	0	128M	16M*16	Samsung	x4
0	0	1	0	256M	32M*16	Samsung	x4
0	1	0	0	128M	16M*16	Infineon	x4
1	1	0	0	256M	32M*16	Infineon	x4
1	0	0	0	128M	16M*16	Hynix	x4
0	0	0	0	256M	32M*16	Hynix	x4

```
When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the frame buffer aperture size.
GPIO[13:12] = 00: 128M frame buffer, same as ROM strap 00
GPIO[13:12] = 01: 256M frame buffer, same as ROM strap 01
GPIO[13:12] = 10: 64M frame buffer, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11
```

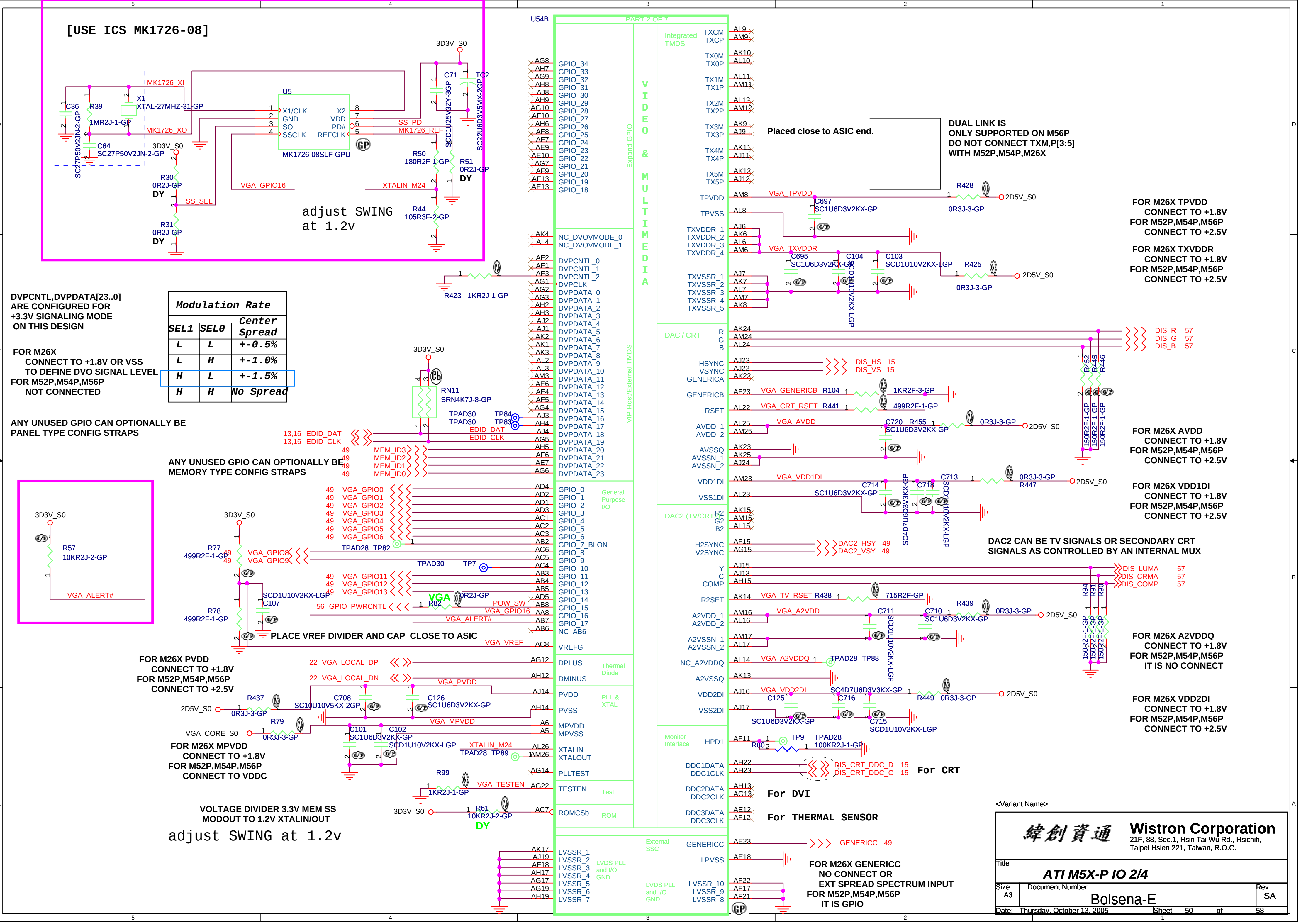
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATI M5X-P PCIE 1/4***

Size: A3 | Document Number: AG1 | Rev: SA

Date: Thursday, October 13, 2005 | Sheet 49 of 58



Modulation Rate

SEL1	SEL0	Center Spread
L	L	+-0.5%
L	H	+-1.0%
H	L	+-1.5%
H	H	No Spread

<Variant Name>

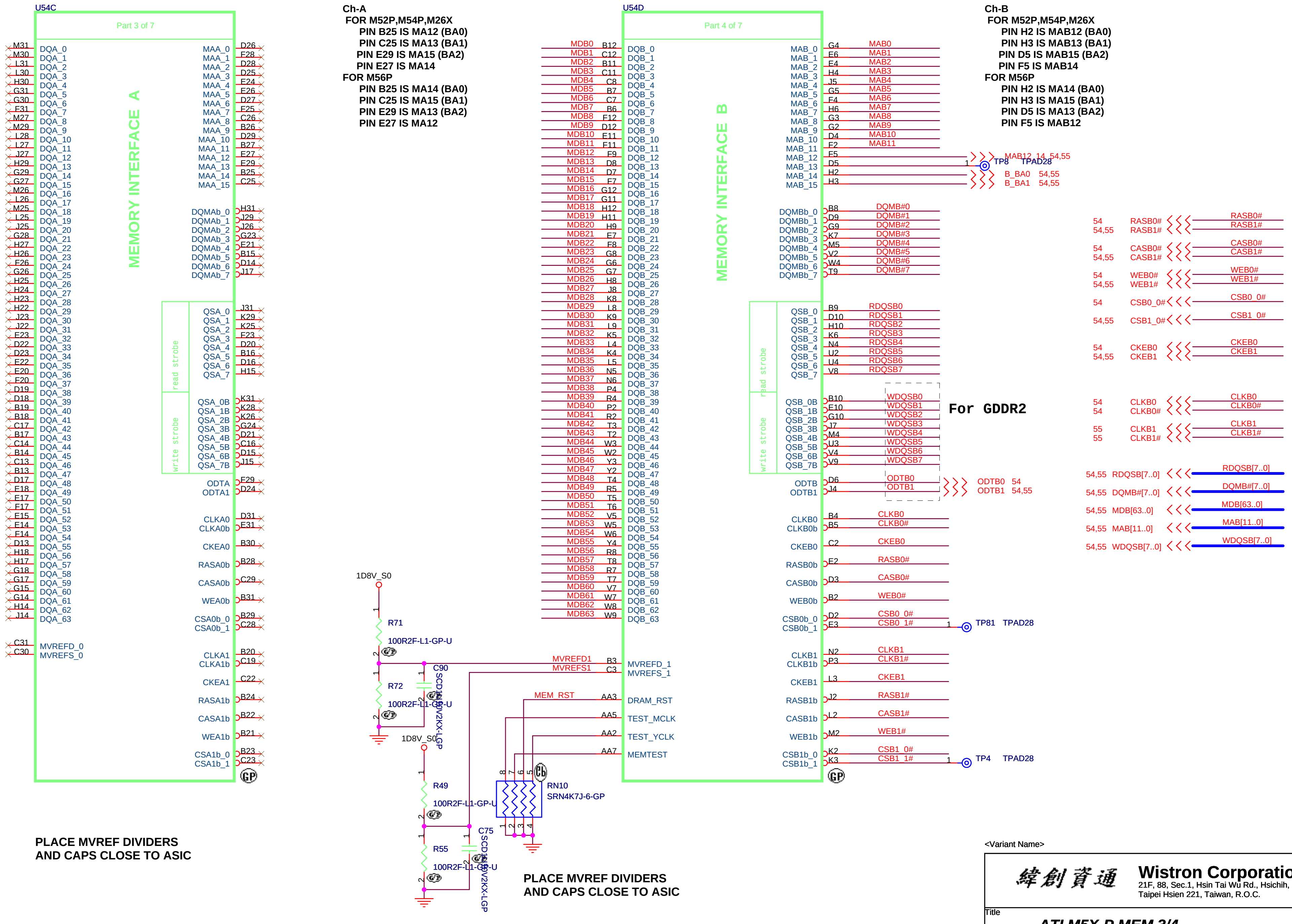
緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI M5X-P IO 2/4**

Size	Document Number	Rev
A3	Bolsena-E	SA

Date: Thursday, October 13, 2005 Sheet 50 of 58

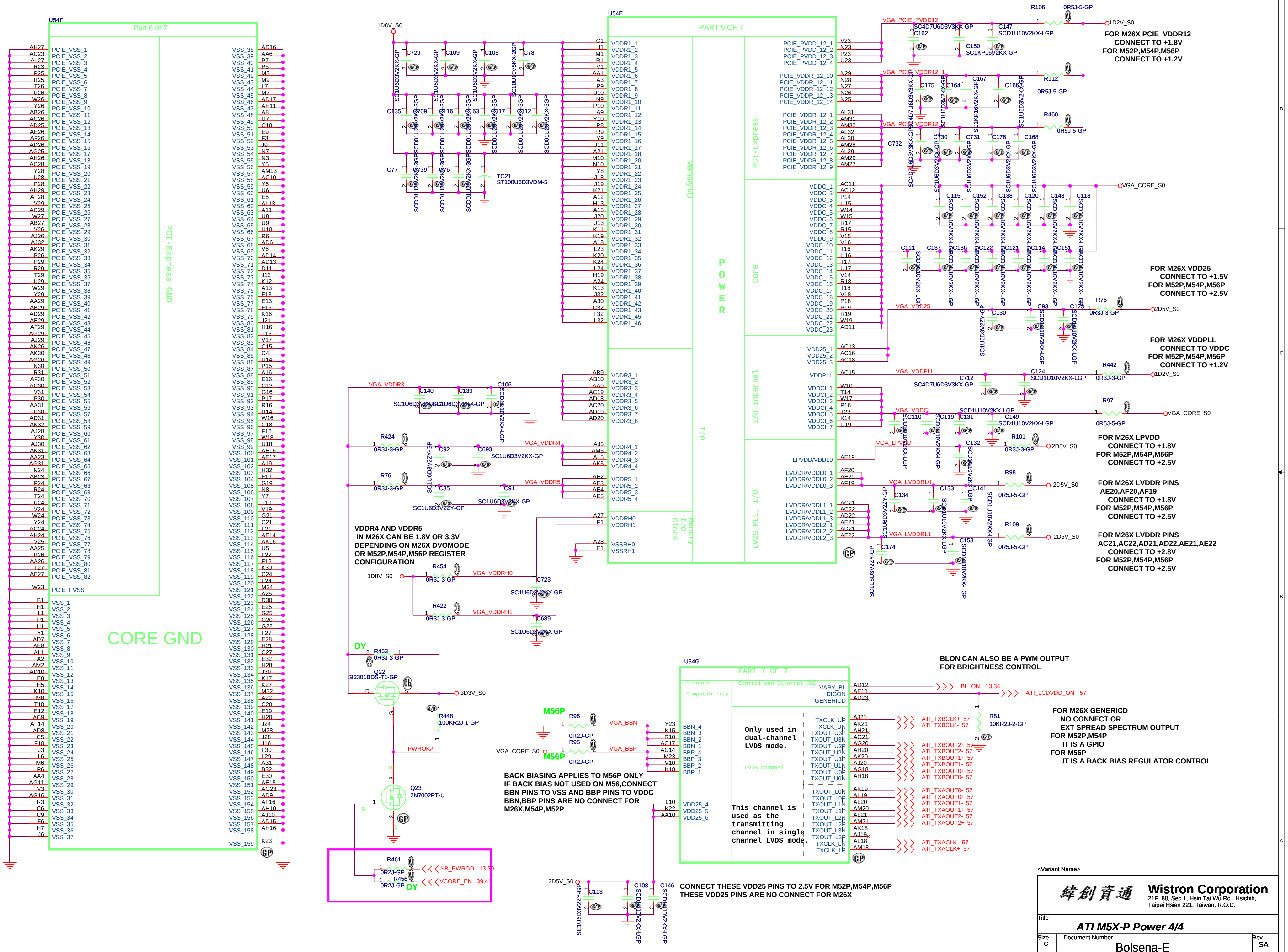


<Variant Name>

緯創資通 **Wistron Corporation**

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	ATI M5X-P MEM 3/4	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 51 of 58	

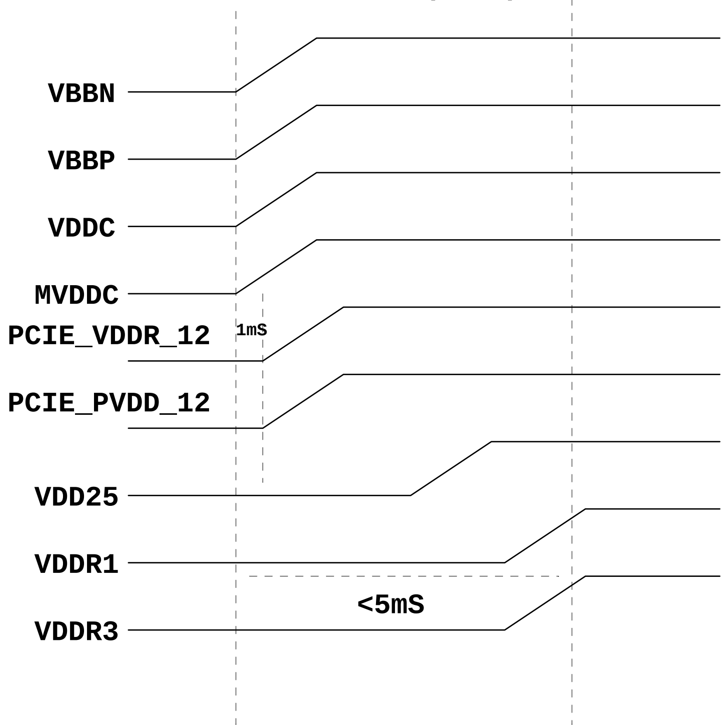


<Variant Name>

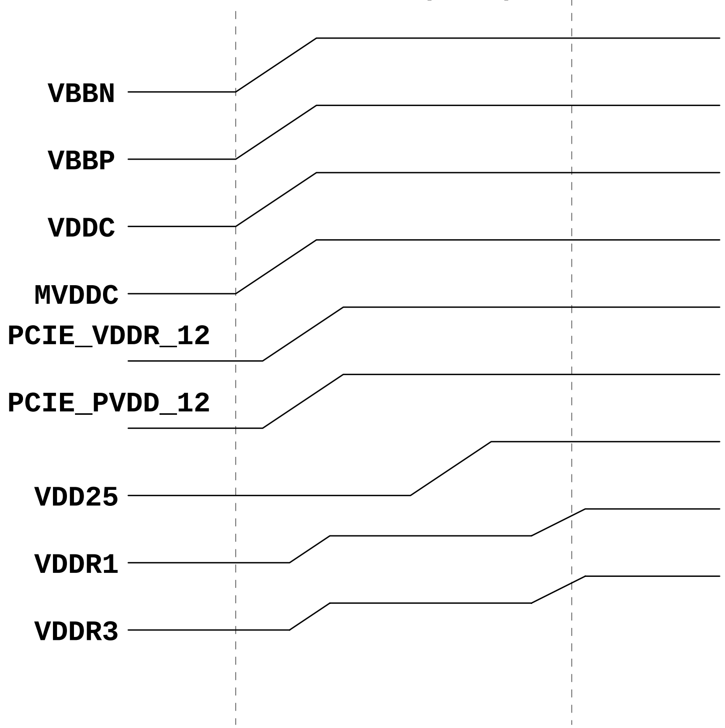
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	ATI M5X-P Power 4/4	
Size: C	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 52 of 58	

Ideal Power Up Sequence



Real Power Up Sequence



RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
For the value, it can be read by the number before R. (R means resistor)
For the tolerance, it can be read from the last letter.
For the rating, we don't show on the symbol name.
For the size, R2=>0402, R3=>0603, R5=>0805,....

General Guidelines:

- BBN and BBP must ramp up before or at the same time as VDDC but not after.
- VDDC and MVDDC must be ramped up first, followed by PCIE_VDDR_12, PCIE_PVDD12, VDD25, VDDR1 and VDDR3 (and other I/O powers).
- All powers must be ramped up within 5ms of each other (from the ramp of VDDC to 90% of VDDR3).
- VDD25 can be ramped with VDDC or VDDR1 but it cannot be ramped later than VDDR1.
- The power down is the opposite of the power on sequence: VDDR3/VDDR1 -> VDD25 ->VDDC/MVDDC/BBN/BBP.

Due to the level shifter design in the memory I/Os, in order to avoid over-stressing the thin oxide transistors when VDDR1 is powered on but VDDC is not, VDDC must ramp up before VDDR1. Similarly, VDDC must ramp up before VDDR3. The level shifter design is a function of the transistor types used in 90nm technology and of the voltage level support. The drawback of ramping up VDDC before the I/O voltages (such as VDDR1 and VDDR3) is that parasitic P/N junctions are forward biased, thus creating a conduction path. These conduction paths will pump up VDDR1 (from the memory IOs) and VDDR3 (from the GPIOs).
The real power up sequence will appear as follows:
Figure 2-2. Real Power Up Sequence
As long as MVDDC ramps up with VDDC, the pump voltage on VDDR1 should be all right since the DRAM spec will not be violated.

CAPACITOR

Symbol name	Value	Tolerance (J: +/-5, K: +/-10, M: +/-20, Z: +80/-20)	Rating (X5R / X7R < 80%, Y5V/Y5U/Z5U < 1/3)	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceremic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance J, K, M, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

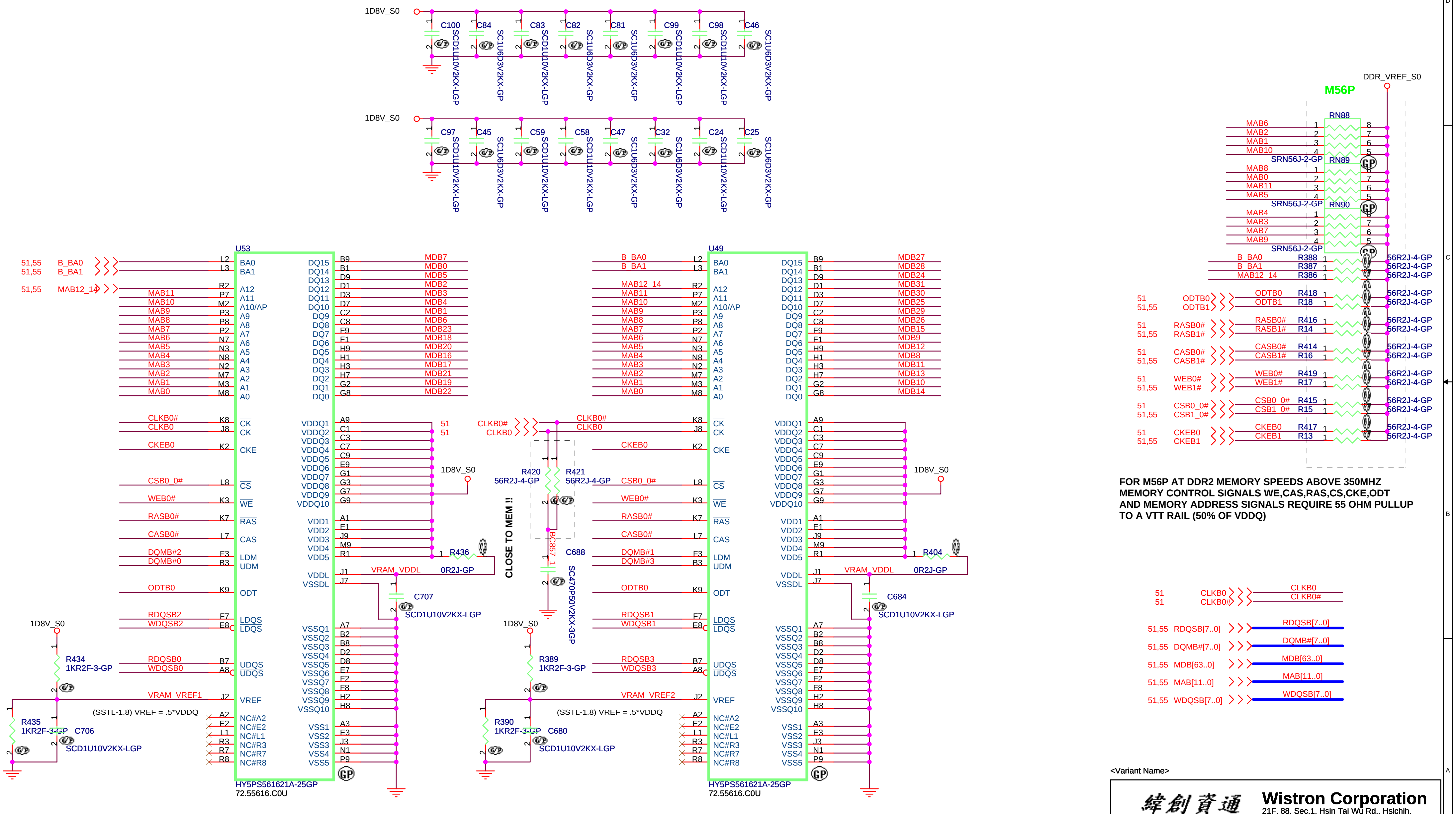
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M5X-P POWER SEQUENCE

Size: A3 | Document Number: Bolsena-E | Rev: SA

CHAN B DDR2 84BGA 32MX16 MEMORY



72.55616.C0U IC VRAM HY5PS561621AFP-25 FBGA(16M*16, 400Mhz)
72.51216.D0U IC VRAM HY5PS121621BFP-25 FBGA(32M*16, 400Mhz)

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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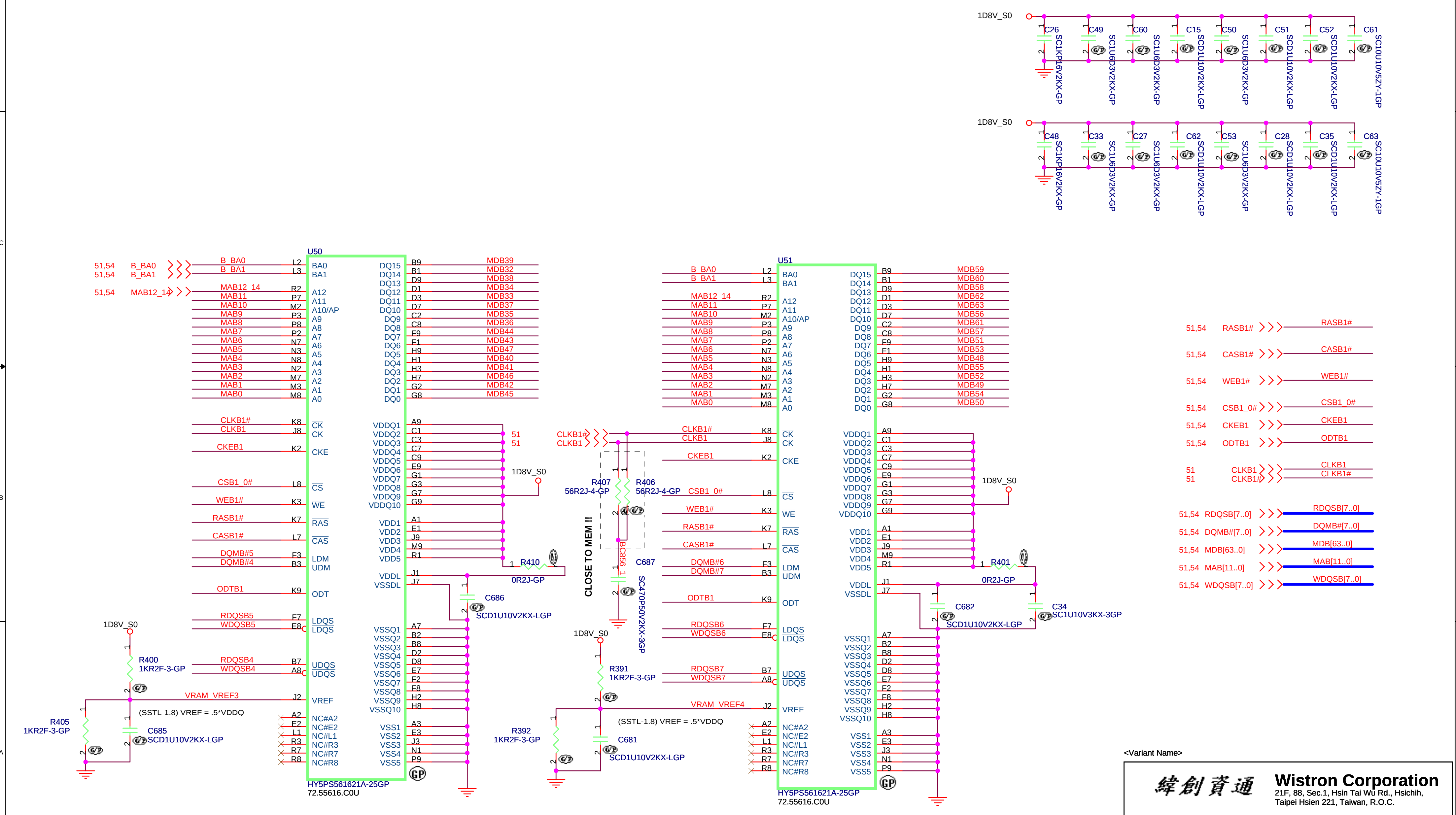
Title: VRAM 1/2		
Size: A3	Document Number: Bolsena-E	Rev: SA
Date: Thursday, October 13, 2005	Sheet 54 of 58	



<Variant Name>

緯創資通 **Wistron Corporation**
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Title		
VRAM 2/2		
Size: A3	Document Number: Bolsena-E	Rev: SA
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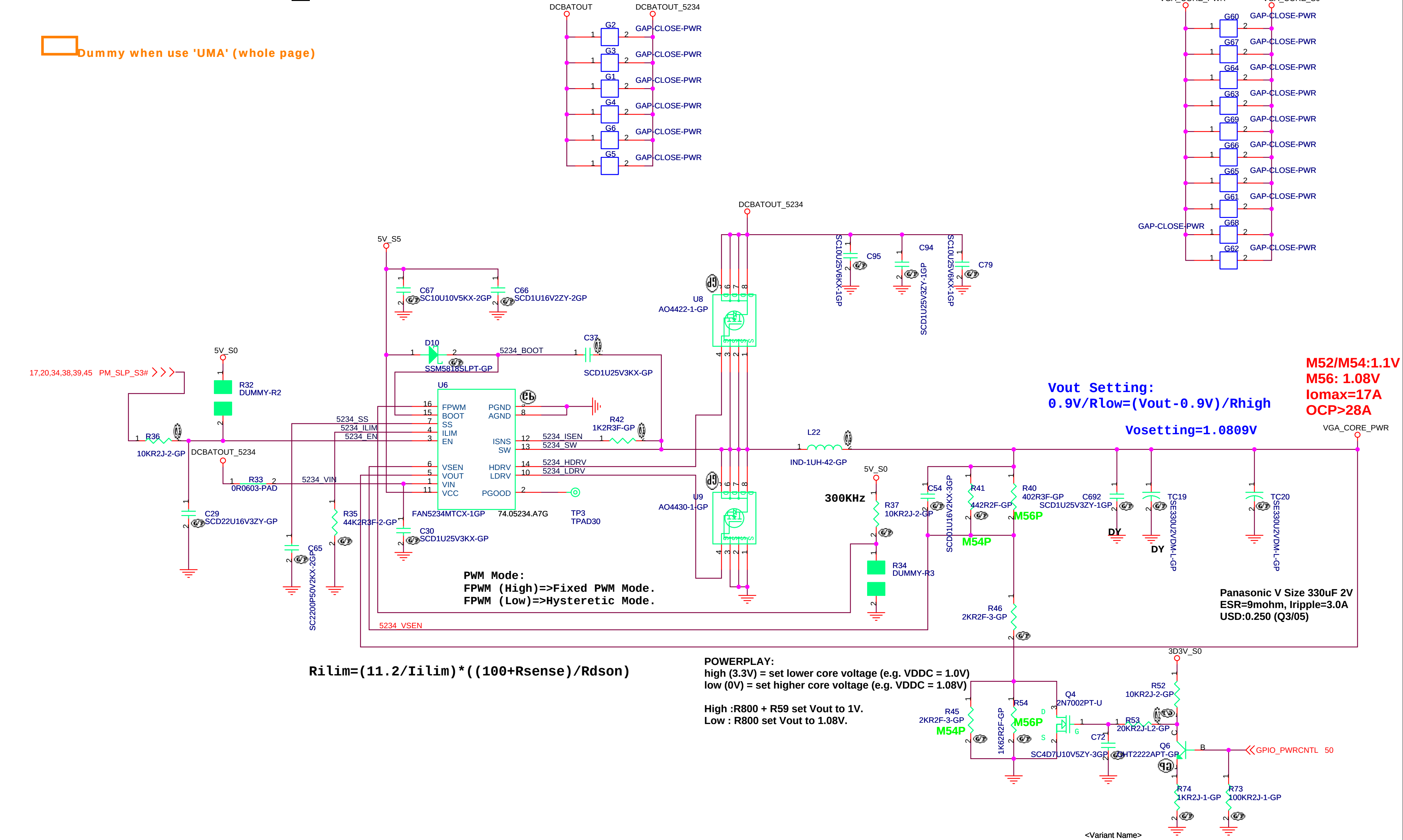
FAN5234 FOR VGA_Core



<Variant Name>

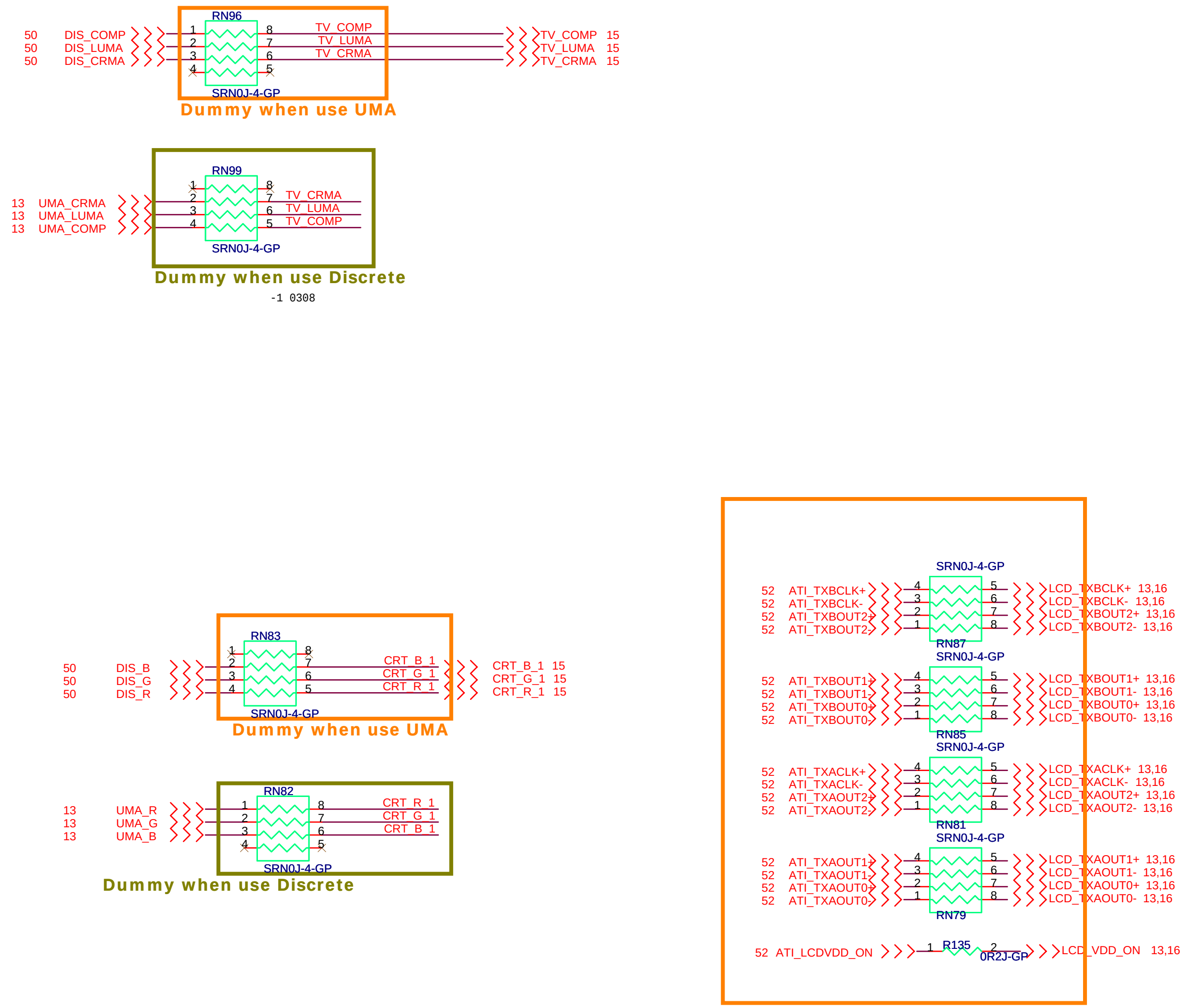
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VGA CORE 1D1V	
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 56 of 58	

(Power Team)

TV SWITCH

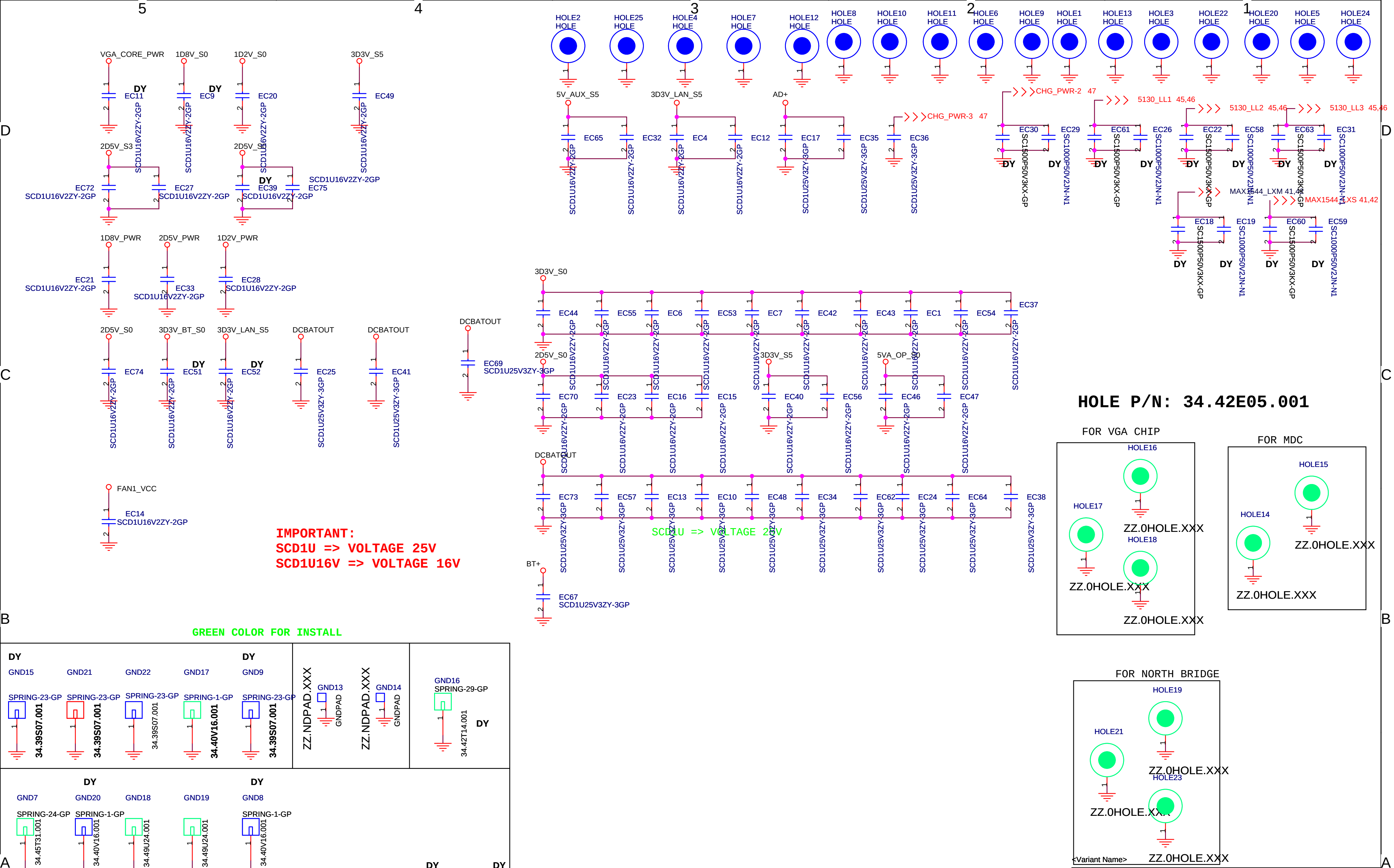
Function	S
A to B0	L
A to B1	H



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	VGA SELECTOR	
Size A3	Document Number: Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 57 of 58	



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI	
Size A3	Document Number Bolsena-E	Rev SA
Date: Thursday, October 13, 2005	Sheet 58 of 58	