Bolsena Block Diagram

91.4C501.001 (04243)

Dummy when use EZ4
Dummy when no EZ4
Dummy when use 10/100
Dummy when use Giga
Dummy when use UMA
Dummy when use Discrete
Dummy when use SATA
Dummy when use IDE

CLK GEN
IDT CV137 3

LEDs 17

AMD CPU
35W/25W
4,5,6,7

DDR 333/400

200-PIN DDR SODIMM
DDR x2
8,9,10

HyperTransport
6.4GB/S 16b/8b

ATI
RS480M
AGTL+ CPU I/F + UMA
11,12,13,14

SVIDEO/COMP
TVOUT 16

LVDS
LCD 17

RGB CRT
CRT 16

PCI Express x16

ATI
M26/M24
50,51,52

Sil1162 15

TMDS
DVI-D
(EZ4 only) 15

VRAM x4
HY5DS573222F
53,54

PCI-Express
x2

PWR SW
TSP2220A
28

PCMCIA
SLOT
Support
TypeII
28

PCMCIA I/F

MS/MSpro
SDIO/MMC/SD
5 in 1
28

1394 4pin
Conn
28

TI
PCI 7411
1* Slot Cardbus
1* 1394
26,27

ATI
SB400
PCI
ACPI 2.0
6xUSB 2.0
6-CH
AC97 2.2
LPC I/F
ATA 133
18,19,20,21,22

PCI Bus / 33MHz

Mini-PCI
802.11a/b/g
31

USB x 4
24

BlueTooth
miniUSB
24

CODEC
ALC655
32

AC97

Line In
MIC In
33

MODEM
MDC Card
24

RJ11
CONN
29

OP AMP
G1421
33

Line Out
33

Int. SPKR
33

RJ45
30

TXFM
30

1000Mb

TXFM
30

10/100Mb

PCI LAN
Realtek
RTL8110SBL
1000/100/10
RTL8100C
100/10
29

LPC Bus / 33MHz

NS SIO
PC87392
37

Thermal
& Fan
G792 23

KBC
KB3910
34

XBUS

FIR
TFDU6102
37

Touch
Pad
35

Int.
KB
35

ISA ROM
36

PIDE

SIDE

SATA
25

HDD
25

DVD/
CD-RW
25

PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

?modify power block

Battery Charger 48

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 44

INPUT	OUTPUT
DCBATOUT	5V_S5, 3D3V_S5

SYSTEM DC/DC 45,46

INPUT	OUTPUT
DCBATOUT	2D5V_S3 1D8V_S5 1D2V_S0

CPU V_CORE 42,43

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 47

INPUT	OUTPUT
2D5V_S3 DCBATOUT	1D25V_S3 5V_AUX_S5

Port Replicator 4 (124 PIN)

AC IN | RJ45-11 | SEARIAL PORT | CRT | PRINTER | PS2 | MIC | LINE IN | LINE OUT | TV OUT | DVI | PCIeX2 | SMBUS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM
Size: A3 | Document Number: Bolsena | Rev: SA
Date: Tuesday, December 28, 2004 | Sheet 1 of 58

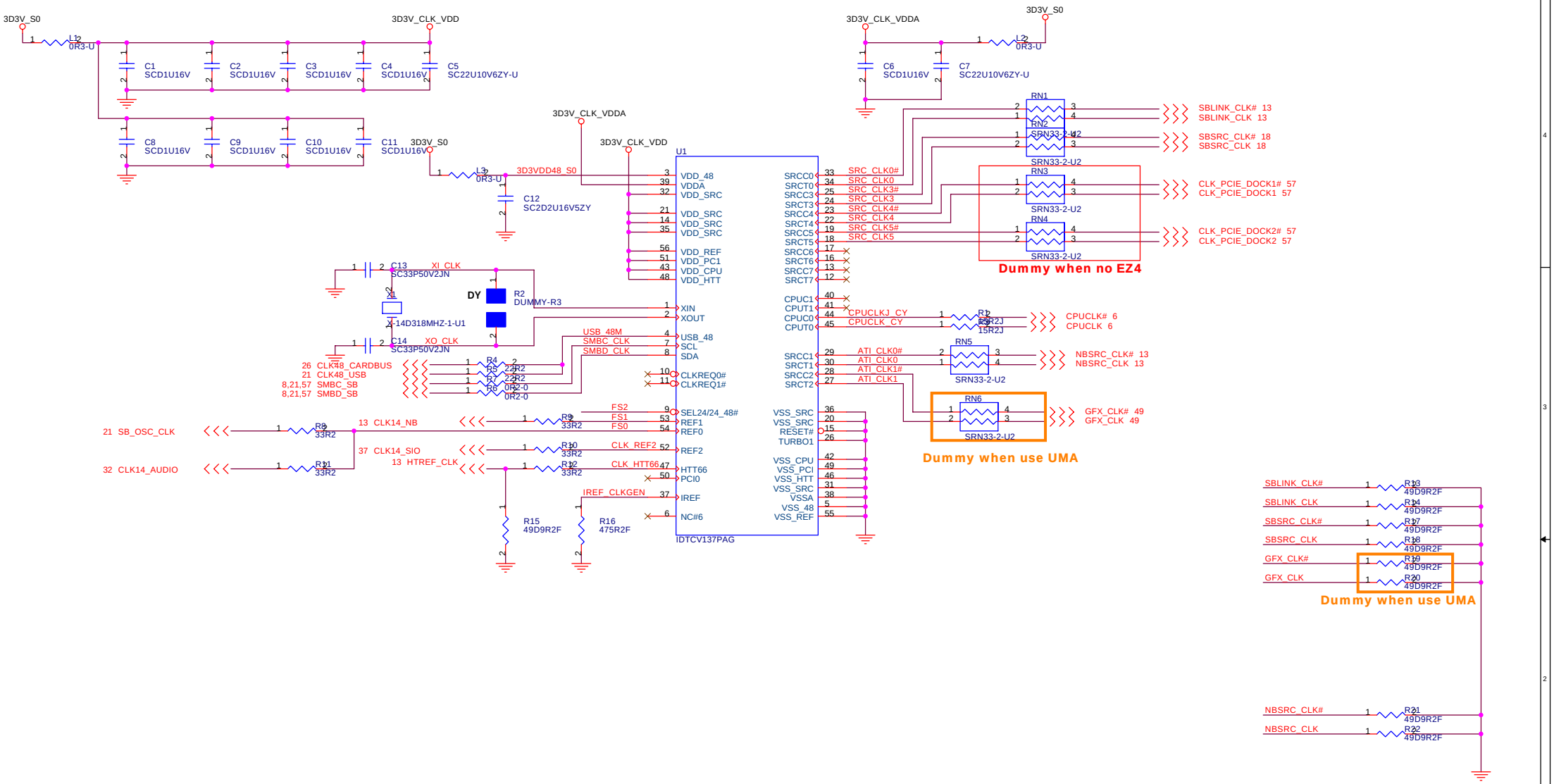
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHANGE HISTORY

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 2 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CLKGEN_IDTCV137**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 3 of 58

1D2V_HT0A_S0

C19 SCD22U16V3ZY
C20 SCD22U16V3ZY
C21 SCD22U16V3ZY
C22 SCD22U16V3ZY

HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power

1D2V_HT0A_S0

U2A

1D2V_HT0B_S0

C23 SC4D7U10V5ZY

LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

11 NB0CADOUT[15..0]
11 NB0CADOUTJ[15..0]

Used SideB Power Plane

CPUCADOUT[15..0] 11
CPUCADOUTJ[15..0] 11

Used SideA Power Plane

		D29	VLDT0_A	VLDT0_B	AH29		
		D27	VLDT0_A	VLDT0_B	AH27		
		D25	VLDT0_A	VLDT0_B	AG28		
		C28	VLDT0_A	VLDT0_B	AG26		
		C26	VLDT0_A	VLDT0_B	AF29		
		B29	VLDT0_A	VLDT0_B	AE28		
		B27	VLDT0_A	VLDT0_B	AE25		
NB0CADOUT15	T25	L0_CADIN_H15		L0_CADOUT_H15	N26	CPUCADOUT15	
NB0CADOUTJ15	R25	L0_CADIN_L15		L0_CADOUT_L15	N27	CPUCADOUTJ15	
NB0CADOUT14	U27	L0_CADIN_H14		L0_CADOUT_H14	L25	CPUCADOUT14	
NB0CADOUTJ14	U26	L0_CADIN_L14		L0_CADOUT_L14	M25	CPUCADOUTJ14	
NB0CADOUT13	V25	L0_CADIN_H13		L0_CADOUT_H13	L26	CPUCADOUT13	
NB0CADOUTJ13	U25	L0_CADIN_L13		L0_CADOUT_L13	L27	CPUCADOUTJ13	
NB0CADOUT12	W27	L0_CADIN_H12		L0_CADOUT_H12	J25	CPUCADOUT12	
NB0CADOUTJ12	W26	L0_CADIN_L12		L0_CADOUT_L12	K25	CPUCADOUTJ12	
NB0CADOUT11	AA27	L0_CADIN_H11		L0_CADOUT_H11	G25	CPUCADOUT11	
NB0CADOUTJ11	AA26	L0_CADIN_L11		L0_CADOUT_L11	H25	CPUCADOUTJ11	
NB0CADOUT10	AB25	L0_CADIN_H10		L0_CADOUT_H10	G26	CPUCADOUT10	
NB0CADOUTJ10	AA25	L0_CADIN_L10		L0_CADOUT_L10	G27	CPUCADOUTJ10	
NB0CADOUT9	AC27	L0_CADIN_H9		L0_CADOUT_H9	E25	CPUCADOUT9	
NB0CADOUTJ9	AC26	L0_CADIN_L9		L0_CADOUT_L9	F25	CPUCADOUTJ9	
NB0CADOUT8	AD25	L0_CADIN_H8		L0_CADOUT_H8	E26	CPUCADOUT8	
NB0CADOUTJ8	AC25	L0_CADIN_L8		L0_CADOUT_L8	E27	CPUCADOUTJ8	
NB0CADOUT7	T27	L0_CADIN_H7		L0_CADOUT_H7	N29	CPUCADOUT7	
NB0CADOUTJ7	T28	L0_CADIN_L7		L0_CADOUT_L7	P29	CPUCADOUTJ7	
NB0CADOUT6	V29	L0_CADIN_H6		L0_CADOUT_H6	M28	CPUCADOUT6	
NB0CADOUTJ6	U29	L0_CADIN_L6		L0_CADOUT_L6	M27	CPUCADOUTJ6	
NB0CADOUT5	V27	L0_CADIN_H5		L0_CADOUT_H5	L29	CPUCADOUT5	
NB0CADOUTJ5	V28	L0_CADIN_L5		L0_CADOUT_L5	M29	CPUCADOUTJ5	
NB0CADOUT4	Y29	L0_CADIN_H4		L0_CADOUT_H4	K28	CPUCADOUT4	
NB0CADOUTJ4	W29	L0_CADIN_L4		L0_CADOUT_L4	K27	CPUCADOUTJ4	
NB0CADOUT3	AB29	L0_CADIN_H3		L0_CADOUT_H3	H28	CPUCADOUT3	
NB0CADOUTJ3	AA29	L0_CADIN_L3		L0_CADOUT_L3	H27	CPUCADOUTJ3	
NB0CADOUT2	AB27	L0_CADIN_H2		L0_CADOUT_H2	G29	CPUCADOUT2	
NB0CADOUTJ2	AB28	L0_CADIN_L2		L0_CADOUT_L2	H29	CPUCADOUTJ2	
NB0CADOUT1	AD29	L0_CADIN_H1		L0_CADOUT_H1	F28	CPUCADOUT1	
NB0CADOUTJ1	AC29	L0_CADIN_L1		L0_CADOUT_L1	F27	CPUCADOUTJ1	
NB0CADOUT0	AD27	L0_CADIN_H0		L0_CADOUT_H0	E29	CPUCADOUT0	
NB0CADOUTJ0	AD28	L0_CADIN_L0		L0_CADOUT_L0	F29	CPUCADOUTJ0	
NB0HTTCLKOUT1	Y25	L0_CLKIN_H1		L0_CLKOUT_H1	J26	CPUHTTCLKOUT1	
NB0HTTCLKOUTJ1	W25	L0_CLKIN_L1		L0_CLKOUT_L1	J27	CPUHTTCLKOUTJ1	
NB0HTTCLKOUT0	Y27	L0_CLKIN_H0		L0_CLKOUT_H0	J29	CPUHTTCLKOUT0	
NB0HTTCLKOUTJ0	Y28	L0_CLKIN_L0		L0_CLKOUT_L0	K29	CPUHTTCLKOUTJ0	
CPUHTTCTLIN1	R27	L0_CTLIN_H1		L0_CTLOUT_H1	N25		
CPUHTTCTLINJ1	R26	L0_CTLIN_L1		L0_CTLOUT_L1	P25		
NB0HTTCTLOUT	T29	L0_CTLIN_H0		L0_CTLOUT_H0	P28	CPUHTTCTLOUT0	
NB0HTTCTLOUTJ	R29	L0_CTLIN_L0		L0_CTLOUT_L0	P27	CPUHTTCTLOUTJ0	

11 NB0HTTCLKOUT1
11 NB0HTTCLKOUTJ1
11 NB0HTTCLKOUT0
11 NB0HTTCLKOUTJ0

CPUHTTCLKOUT1 11
CPUHTTCLKOUTJ1 11
CPUHTTCLKOUT0 11
CPUHTTCLKOUTJ0 11

1D2V_HT0B_S0

R29 49D9R3F
R30 49D9R3F

11 NB0HTTCTLOUT
11 NB0HTTCTLOUTJ

CPUHTTCTLOUT0 11
CPUHTTCTLOUTJ0 11

62.10030.041

BGA754-SKT-U

By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

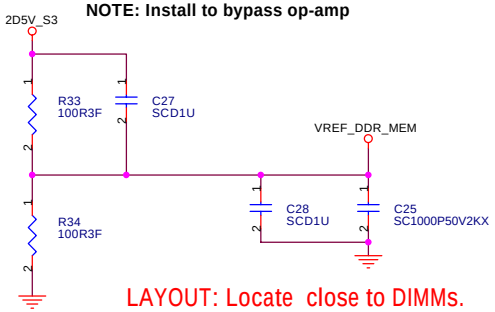
Title: CPU(1/4)_HyperTransport I/F

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 4 of 58

VREF_DDR_MEM

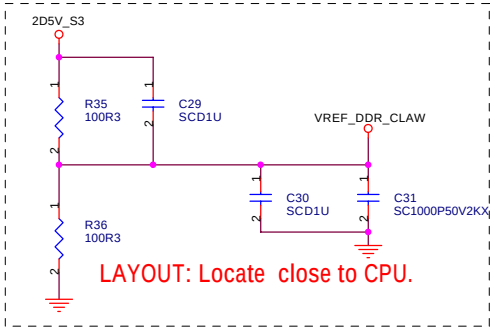
NOTE: Test with passive probes only.
NOTE: Install to bypass op-amp



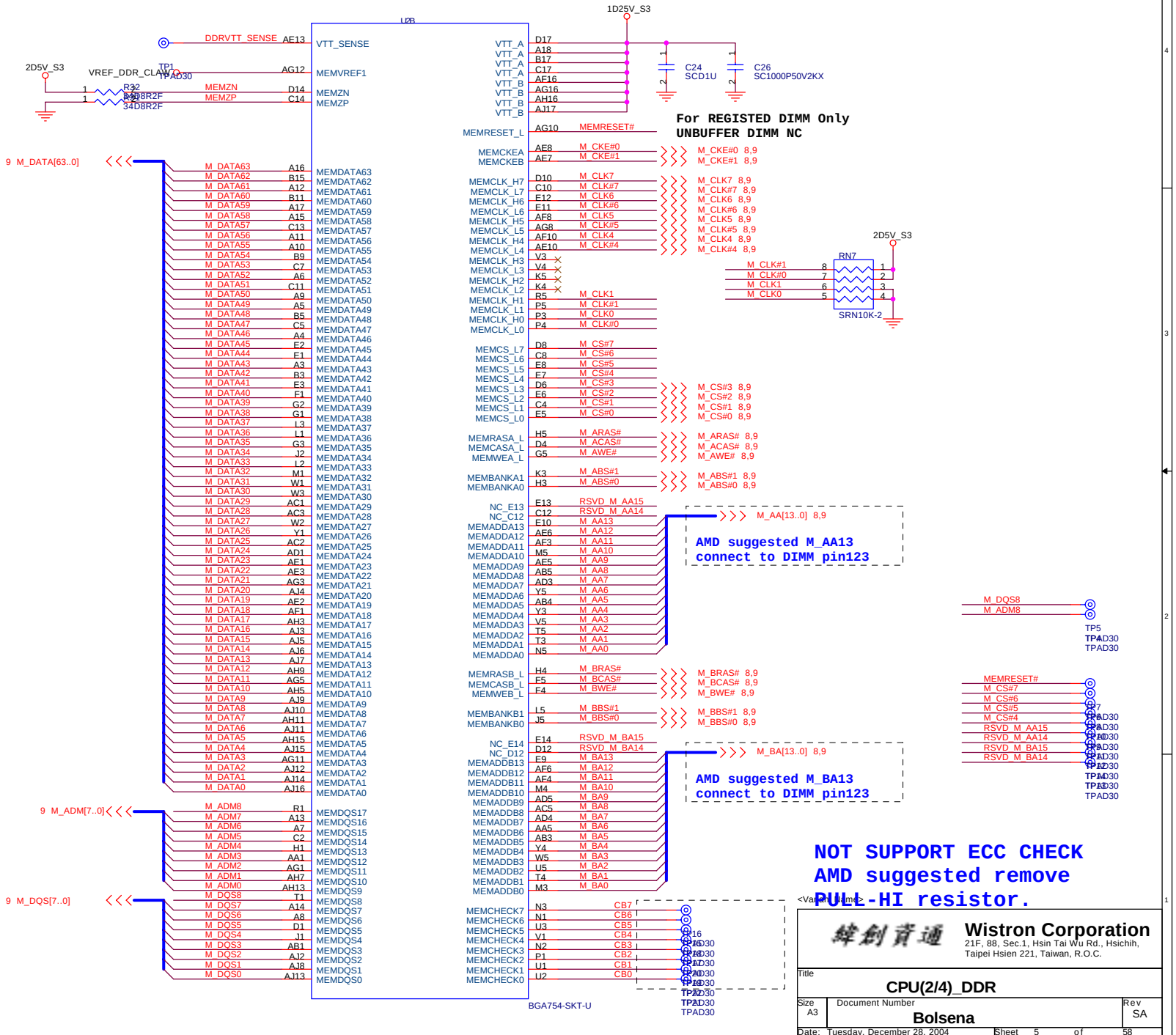
LAYOUT: Locate close to DIMMs.

NOTE: Remove to bypass op-amp

VREF_DDR_CLAW

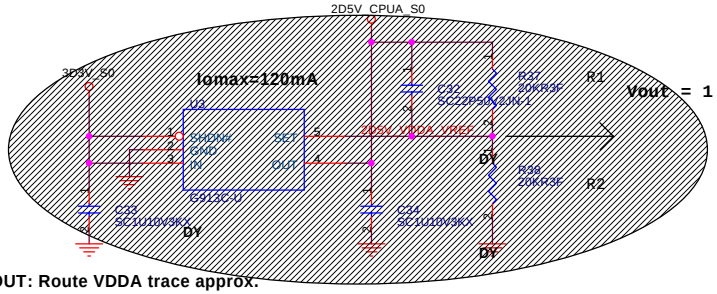


LAYOUT: Locate close to CPU.



Wistron Corporation			
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: CPU(2/4)_DDR			
Size: A3	Document Number: Bolsena	Rev: SA	
Date: Tuesday, December 28, 2004	Sheet 5 of 58		

2D5V_VDDA_S0



2D5V_S0

AMD SUGGEST TO USE 100 ~ 300UH

R39 0R3-U 2D5V_CPUR_S0

C35 SC10U10V5ZY

Change L270H

2D5V_VDDA_S0

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

2D5V_CPUA_S0

R40 0R3-U

R59 0R5J-1

63.R0004.151

TC1 ST100U4VBM-1

DY

C39 SC1U10V5ZY

C36 SC3300P50V2KX

C40 SCD22U16V3ZY

1D2V_HT0B_S0

R44 44D2R3F

R42 44D2R3F

64.44R25.551

C37 SC1000P50V2KX

C41 SC1000P50V2KX

AMD SUGGEST TO USE 2D5V_CPUA_S0

KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

AMD suggest voltege from 2D5V_S0 to 2D5V_S3 differentially impedance 100

2D5V_S3

R46 820R3

3 CPUCLK

C42 SC3900P50V3KX

3 CPUCLK#

C38 SC3900P50V3KX

R45 169R3F

1D25V_S3

2D5V_S0

LDT_RST#

SB_CPUPWRGD

LDT_STP#

R48 680R3

R49 680R3

R50 680R3

2D5V_S0

C44 SCD1U

RN8 SRN680-U

R53 680R3

R54 680R3

DBREQ_J

DBRDY

TCK

TMS

TDI

TRST_L

TDO

DY

2D5V_S3

R57 680R3

CHANGE FROM 1KR3 TO 680R2 FOR AMD CHECK LIST

RN10 SRN680-U

NC_AG17
NC_AJ18
NC_D18

RN11 SRN680-U

NC_B19
NC_C19
NC_D20
NC_C21

Validation Test Points

LAYOUT: Place close to the CPU.

NC_C15
NC_AE23
NC_AF23
NC_AF22
NC_AF21

LDT_RST#
CLKIN
CLKIN#
CORE_SENSE
VDDIOFB
VDDIOFBJ
VDDIOSENSE
NC_AE24
NC_AF24

TPAD30

U2C

BGA754-SKT-U

VDDA1 AH25
VDDA2 AJ25

RESET_L AF20
PWROK AE18
LDTSTOP_L AJ27

L0_REF1 AF27
L0_REF0 AE26

COREFB A23
COREFB# A24
CORE_SENSE B23

VDDIOFB_H AE12
VDDIOFB_L AE12
VDDIO_SENSE AE11

CLKIN_H AJ21
CLKIN_L AH21

NC_AJ23 AJ23
NC_AH23 AH23

NC_AE24 AE24
NC_AF24 AF24

VTT_A C16
VTT_B AG15

DBRDY AH17

NC_C15 C15

TMS E20
TCK E17
TRST_L B21
TDI A21

NC_C18 C18

NC_A19 A19

KEY1 A28
KEY0 AJ28

NC_AE23 AE23
NC_AF23 AF23
NC_AF22 AF22
NC_AF21 AF21

NC_C1 C1
NC_J3 J3
NC_R3 R3
NC_AA2 AA2
NC_D3 D3
NC_AG2 AG2
NC_B18 B18
NC_AH1 AH1
NC_AE21 AE21
NC_C20 C20
NC_AG4 AG4
NC_C6 C6
NC_AG6 AG6
NC_AE9 AE9
NC_AG9 AG9

THERMTRIP_L A20
THERMDA A26
THERMDC A27

VID4 AG13
VID3 AF14
VID2 AG14
VID1 AF15
VID0 AE15

NC_AG18 AG18
NC_AH18 AH18
NC_AG17 AG17
NC_AJ18 AJ18

FBCLKOUT_H AH19
FBCLKOUT_L AJ19

DBREQ_L AE19

NC_D20 D20
NC_C21 C21
NC_D18 D18
NC_C19 C19
NC_B19 B19

TDO A22

NC_AF18 AF18

NC_D22 D22
NC_C22 C22

NC_B13 B13
NC_B7 B7
NC_C3 C3
NC_K1 K1
NC_R2 R2
NC_AA3 AA3
NC_F3 F3
NC_C23 C23
NC_AG7 AG7
NC_AE22 AE22
NC_C24 C24
NC_A25 A25
NC_C9 C9

THERMTRIP#
THERMDP 23
THERMDN 23
VID[4..0] 41

TP23 TPAD30
TP24 TPAD30

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

FBCLKOUT
R47 80D6R3F-U
FBCLKOUTJ

DBREQJ
SUMMY-R3
DY

Connect to VDDIO for AMD suggest.

2D5V_S3

2D5V_S0
3D3V_S5
R55 680R3
R56 10KR2
THERMTRIP#
Q1 MMBT3904-U1
CPU_THERMTRIP# 21,23
NS3
R58 1KR2

THERMTRIP#Level shift to SB400

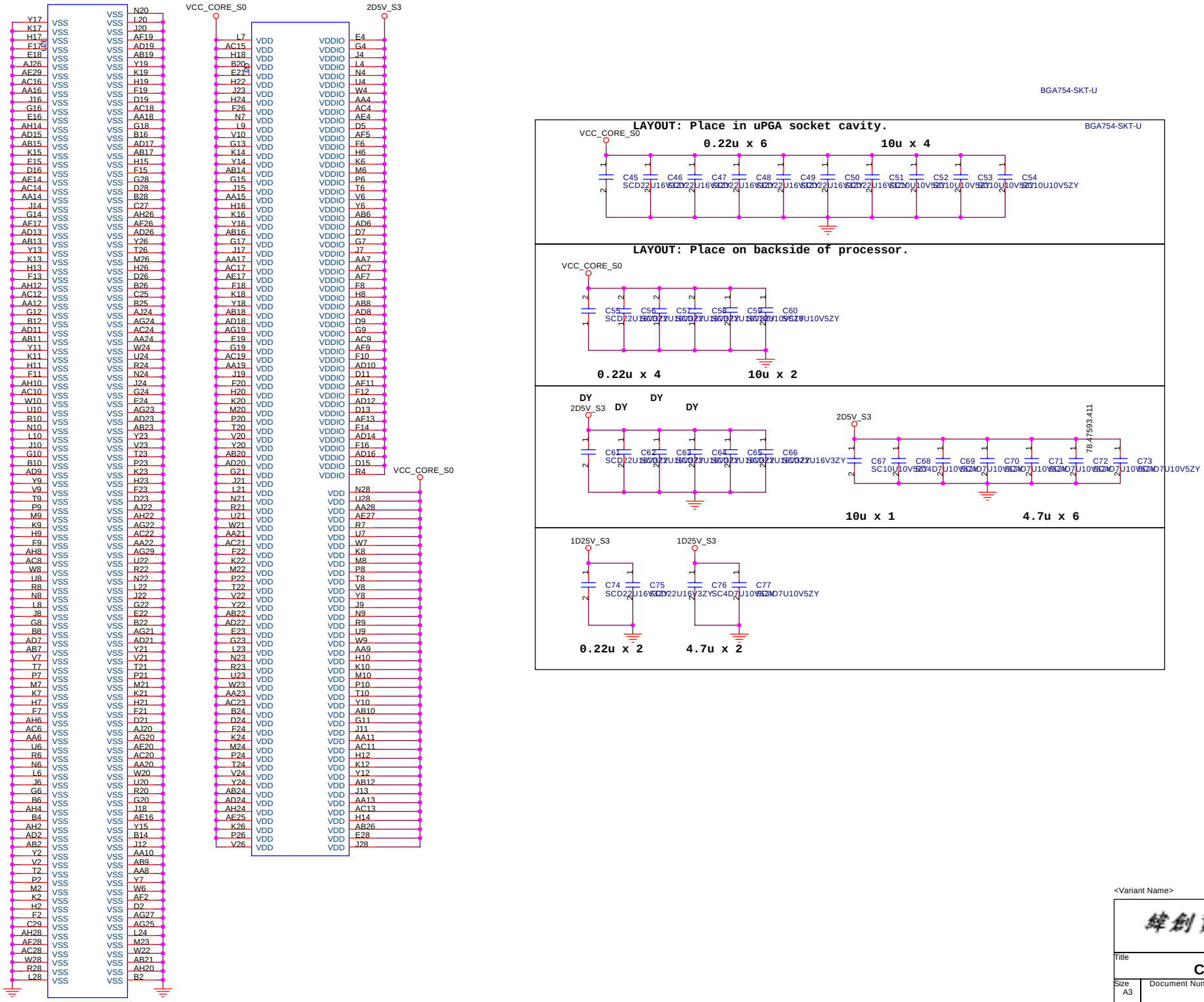
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU(3/4)_Control & Debug

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 6 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU(4/4)_Power**

Size	Document Number	Rev
A3	**Bolsena**	SA

Date: Tuesday, December 28, 2004 Sheet 7 of 58

DDR1

REVERSE TYPE 5.2MM

SKT-SODIMM200-24

62.10017.701

NOT SUPPORT ECC CHECK
AMD suggested pull-low

Layout trace 20 mil

DDR2

REVERSE TYPE 9.2MM

SKT-SODIMM200-6U

62.10017.391

Layout trace 20 mil

?NEED CHANGE LIBRARY

M_ADM_R[7..0] 9
M_DATA_R_[63..0] 9
M_DQS_R[7..0] 9
M_AA[13..0] 5,9
M_ABS#[1..0] 5,9
M_BA[13..0] 5,9
M_BBS#[1..0] 5,9

R563 4K7R2

RN92 SRN10K-2

DDR_CLK#1
DDR_CLK#0
DDR_CLK1
DDR_CLK0

2D5V_S3

DY

AMD CPU

MD63 SMA11 SMA10 SMA0 SMA14 SMA12 MD0

DDR1(Reverse 5.2mm)

DDR2(Reverse 9.2mm)

Pin 199 Pin 1 Pin 200 Pin 2

(Bottom view)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR SO-DIMM SKT**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 8 of 58

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DIMM, < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

SRN10J-3 RN13

M_DATA4	8	9	M_DATA_R_4
M_DATA5	7	10	M_DATA_R_5
M_ADM0	6	11	M_ADM_R0
M_DATA6	5	12	M_DATA_R_6
M_DATA7	4	13	M_DATA_R_7
M_DATA13	3	14	M_DATA_R_13
M_DATA12	2	15	M_DATA_R_12
M_ADM1	1	16	M_ADM_R1

SRN10J-3 RN14

M_DATA32	8	9	M_DATA_R_32
M_DATA33	7	10	M_DATA_R_33
M_DATA36	6	11	M_DATA_R_36
M_DATA37	5	12	M_DATA_R_37
M_DQS4	4	13	M_DQS_R4
M_ADM4	3	14	M_ADM_R4
M_DATA34	2	15	M_DATA_R_34
M_DATA39	1	16	M_DATA_R_39

SRN10J-3 RN18

M_DATA1	8	9	M_DATA_R_1
M_DATA0	7	10	M_DATA_R_0
M_DQS0	6	11	M_DQS_R0
M_DATA2	5	12	M_DATA_R_2
M_DATA3	4	13	M_DATA_R_3
M_DATA8	3	14	M_DATA_R_8
M_DATA9	2	15	M_DATA_R_9
M_DQS1	1	16	M_DQS_R1

SRN10J-3 RN19

M_DATA35	8	9	M_DATA_R_35
M_DATA41	7	10	M_DATA_R_41
M_DATA40	6	11	M_DATA_R_40
M_DQS5	5	12	M_DQS_R5
M_DATA42	4	13	M_DATA_R_42
M_DATA43	3	14	M_DATA_R_43
M_DATA49	2	15	M_DATA_R_49
M_DATA48	1	16	M_DATA_R_48

SRN10J-3 RN24

M_DATA14	8	9	M_DATA_R_14
M_DATA15	7	10	M_DATA_R_15
M_DATA21	6	11	M_DATA_R_21
M_DATA20	5	12	M_DATA_R_20
M_ADM2	4	13	M_ADM_R2
M_DATA23	3	14	M_DATA_R_23
M_DATA22	2	15	M_DATA_R_22
M_DATA25	1	16	M_DATA_R_25

SRN10J-3 RN25

M_DATA38	8	9	M_DATA_R_38
M_DATA45	7	10	M_DATA_R_45
M_DATA44	6	11	M_DATA_R_44
M_ADM5	5	12	M_ADM_R5
M_DATA47	4	13	M_DATA_R_47
M_DATA46	3	14	M_DATA_R_46
M_DATA53	2	15	M_DATA_R_53
M_DATA52	1	16	M_DATA_R_52

SRN10J-3 RN29

M_DATA11	8	9	M_DATA_R_11
M_DATA10	7	10	M_DATA_R_10
M_DATA17	6	11	M_DATA_R_17
M_DATA16	5	12	M_DATA_R_16
M_DQS2	4	13	M_DQS_R2
M_DATA19	3	14	M_DATA_R_19
M_DATA18	2	15	M_DATA_R_18
M_DATA24	1	16	M_DATA_R_24

SRN10J-3 RN30

M_DQS6	8	9	M_DQS_R6
M_DATA50	7	10	M_DATA_R_50
M_DATA51	6	11	M_DATA_R_51
M_DATA56	5	12	M_DATA_R_56
M_DATA57	4	13	M_DATA_R_57
M_DQS7	3	14	M_DQS_R7
M_DATA58	2	15	M_DATA_R_58
M_DATA59	1	16	M_DATA_R_59

SRN10J-3 RN34

M_DATA29	8	9	M_DATA_R_29
M_DATA28	7	10	M_DATA_R_28
M_DQS3	6	11	M_DQS_R3
M_ADM3	5	12	M_ADM_R3
M_DATA26	4	13	M_DATA_R_26
M_DATA27	3	14	M_DATA_R_27
M_DATA30	2	15	M_DATA_R_30
M_DATA31	1	16	M_DATA_R_31

SRN10J-3 RN35

M_ADM6	8	9	M_ADM_R6
M_DATA54	7	10	M_DATA_R_54
M_DATA55	6	11	M_DATA_R_55
M_DATA61	5	12	M_DATA_R_61
M_DATA60	4	13	M_DATA_R_60
M_ADM7	3	14	M_ADM_R7
M_DATA62	2	15	M_DATA_R_62
M_DATA63	1	16	M_DATA_R_63

5,8 M_CKE#0 <<< M_CKE#0

5,8 M_CKE#1 <<< M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

SRN68J-1 RN15

M_ADM_R1	8	9	8	9	M_DATA_R_32
M_DATA_R_13	7	10	7	10	M_DATA_R_33
M_DATA_R_12	6	11	6	11	M_DATA_R_36
M_DATA_R_7	5	12	5	12	M_DATA_R_37
M_DATA_R_6	4	13	4	13	M_ADM_R4
M_ADM_R0	3	14	3	14	M_DQS_R4
M_DATA_R_5	2	15	2	15	M_DATA_R_38
M_DATA_R_4	1	16	1	16	M_DATA_R_39

SRN68J-1 RN16

SRN68J-1 RN20

M_DATA_R_1	8	9	8	9	M_DATA_R_48
M_DATA_R_0	7	10	7	10	M_DATA_R_49
M_DQS_R0	6	11	6	11	M_DATA_R_43
M_DATA_R_2	5	12	5	12	M_DATA_R_42
M_DATA_R_3	4	13	4	13	M_DQS_R5
M_DATA_R_8	3	14	3	14	M_DATA_R_41
M_DATA_R_9	2	15	2	15	M_DATA_R_40
M_DQS_R1	1	16	1	16	M_DATA_R_34

SRN68J-1 RN21

SRN68J-1 RN26

M_DATA_R_25	8	9	8	9	M_DATA_R_35
M_DATA_R_23	7	10	7	10	M_DATA_R_44
M_DATA_R_22	6	11	6	11	M_DATA_R_45
M_ADM_R2	5	12	5	12	M_ADM_R5
M_DATA_R_21	4	13	4	13	M_DATA_R_46
M_DATA_R_20	3	14	3	14	M_DATA_R_47
M_DATA_R_15	2	15	2	15	M_DATA_R_52
M_DATA_R_14	1	16	1	16	M_DATA_R_53

SRN68J-1 RN27

SRN68J-1 RN31

M_DATA_R_11	8	9	8	9	M_DATA_R_59
M_DATA_R_10	7	10	7	10	M_DATA_R_58
M_DATA_R_16	6	11	6	11	M_DQS_R7
M_DATA_R_17	5	12	5	12	M_DATA_R_57
M_DQS_R2	4	13	4	13	M_DATA_R_56
M_DATA_R_19	3	14	3	14	M_DATA_R_51
M_DATA_R_18	2	15	2	15	M_DATA_R_50
M_DATA_R_24	1	16	1	16	M_DQS_R6

SRN68J-1 RN32

SRN68J-1 RN36

M_DATA_R_31	8	9	8	9	M_ADM_R6
M_DATA_R_30	7	10	7	10	M_DATA_R_54
M_DATA_R_26	6	11	6	11	M_DATA_R_55
M_DATA_R_27	5	12	5	12	M_DATA_R_60
M_ADM_R3	4	13	4	13	M_DATA_R_61
M_DQS_R3	3	14	3	14	M_ADM_R7
M_DATA_R_29	2	15	2	15	M_DATA_R_62
M_DATA_R_28	1	16	1	16	M_DATA_R_63

SRN68J-1 RN37

1D25V_S3

SRN47J RN17

M_CKE#0	1	4	
M_CKE#1	2	3	

SRN47J RN22

M_BA12	1	4	
M_AA12	2	3	

SRN47J-1-U RN23

M_AA11	8	9	
M_AA9	7	10	
M_AA7	6	11	
M_AA5	5	12	
M_AA4	4	13	
M_AA8	3	14	
M_AA6	2	15	
M_AA3	1	16	

SRN47J-1-U RN28

M_CS#3	8	9	
M_BCAS#	7	10	
M_BRAS#	6	11	
M_BBS#1	5	12	
M_CS#2	4	13	
M_BA13	3	14	
M_BA0	2	15	
M_BA2	1	16	

SRN47J-1-U RN33

M_AA1	8	9	
M_AA10	7	10	
M_AA2	6	11	
M_AA0	5	12	
M_ABS#1	4	13	
M_ARAS#	3	14	
M_AWE#	2	15	
M_ABS#0	1	16	

SRN47J-1-U RN38

M_BA7	8	9	
M_BA3	7	10	
M_BA6	6	11	
M_BA9	5	12	
M_BA10	4	13	
M_BA1	3	14	
M_BBS#0	2	15	
M_BWE#	1	16	

SRN47-1 RN39

M_BA4	4	5	
M_BA8	3	6	
M_BA11	2	7	
M_BA5	1	8	

SRN47-1 RN40

M_AA13	4	5	
M_CS#0	3	6	
M_ACAS#	2	7	
M_CS#1	1	8	

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8

M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8

M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8

M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

Place it near CPU

R60 121R3F	M_CLK7	M_CLK#7	M_CLK7 5,8	M_CLK#7 5,8
R61 121R3F	M_CLK6	M_CLK#6	M_CLK6 5,8	M_CLK#6 5,8
R62 121R3F	M_CLK5	M_CLK#5	M_CLK5 5,8	M_CLK#5 5,8
R63 121R3F	M_CLK4	M_CLK#4	M_CLK4 5,8	M_CLK#4 5,8

<Variant Name>

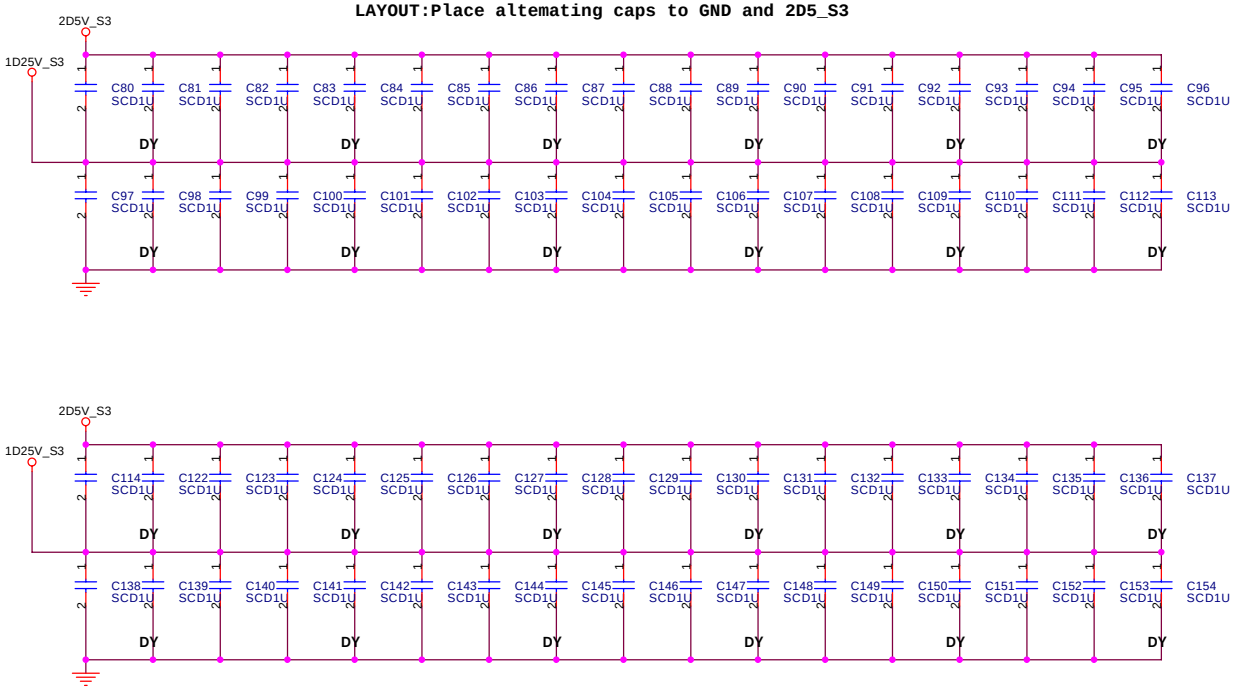
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

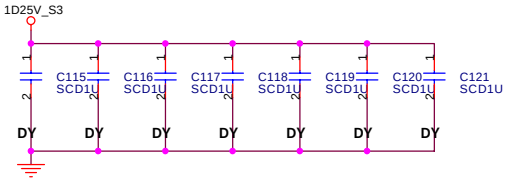
Title: DDR DAMPING & TERMINATION

Size	Document Number	Rev
A3	Bolsena	SA

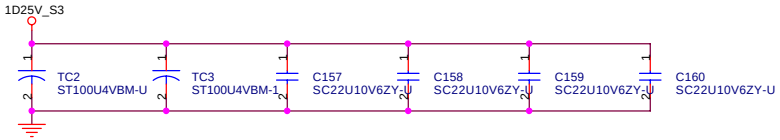
Date: Tuesday, December 28, 2004 Sheet 9 of 58

LAYOUT:Place altemating caps to GND and 2D5_S3

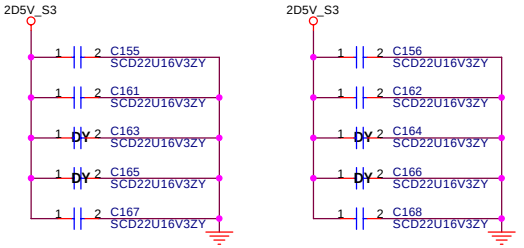




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

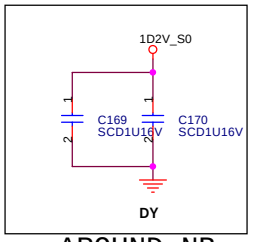
Title: **DDR DECOUPLING**

Size	Document Number	Rev
A3	Bolsena	SA

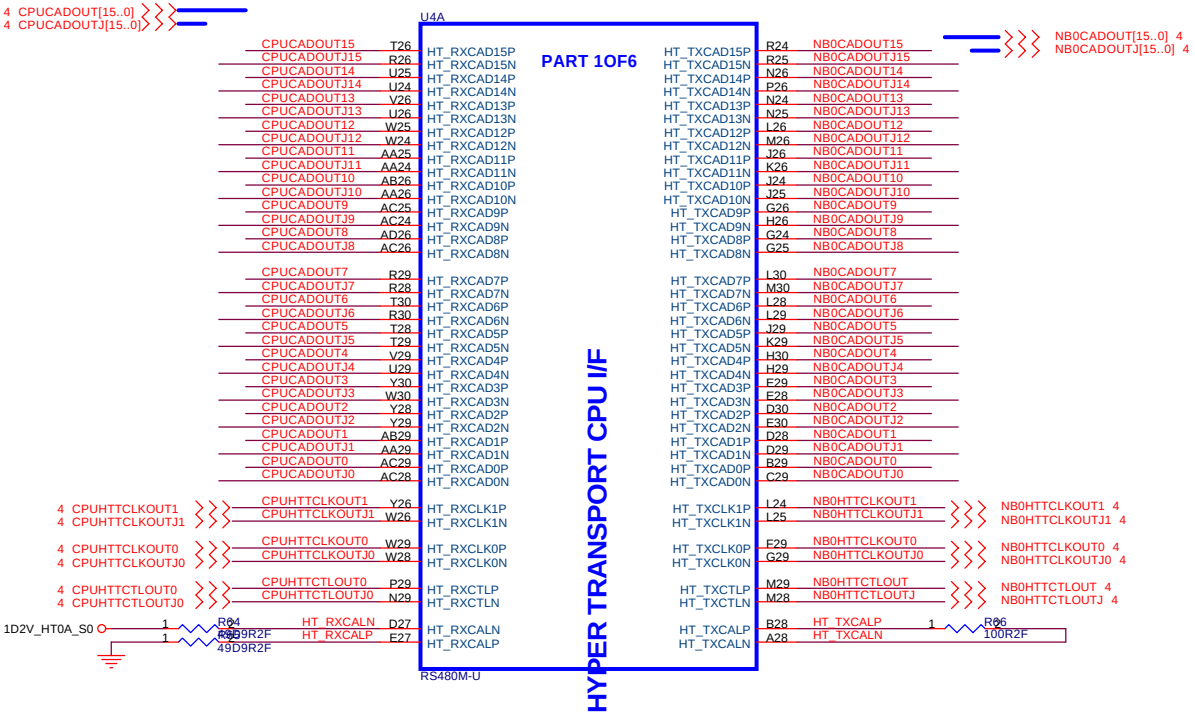
Date: Tuesday, December 28, 2004 Sheet 10 of 58

CLAW HAMMER TO NB

NB TO CLAW HAMMER



AROUND NB



<variant_name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-RS480M (1 of 4) HT

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 11 of 58

?PLACE THESE CAP CLOSE
TO CONNECTOR

49 PEG_TXP[15..0]
49 PEG_TXN[15..0]
49 PEG_RXP[15..0]
49 PEG_RXN[15..0]

U4C
PART 3 OF 6
MEM_A I/F
RS480M-U

U4B
PART 2 OF 6
LANE REVERSE
PCIE I/F TO VIDEO
PCIE I/F TO SLOT
PCIE I/F TO SB
RS480M-U

Dummy when use UMA
Dummy when no EZ4
?NEED STRAP FOR MULTI PIN?

1D8V_S0
15 IDCKP
15 IDCKN
R67 1KR2F
R68 1KR2F
MEM_VREF

Connect MEM_VREF to VDD_MEM/2
PA_RS480F1.PDF

C212 SCD47U16V3ZY
C214 SCD47U16V3ZY
DY
DY

1D8V_S0
MEM_VMODE
MEM_VREF
MPVDD_PLL
L5 0R5J-1
C213 SC1U10V3KX

2D5V_S3
R74 60D4R2F
R75 60D4R2F
DY
DY

DO NOT SUPPORT SIDEPORT MEMORY
DUMMY IT

When disable local frame buffer,
VDD_MEM connect to 2D5V_S3,
MEM_VMODE connect to GND,
MEM_VREF connect to 2D5V_S3,
MPVDD connected to 1D8V

?CHECK THESE PINS

DSG-215-RS480-04.PDF

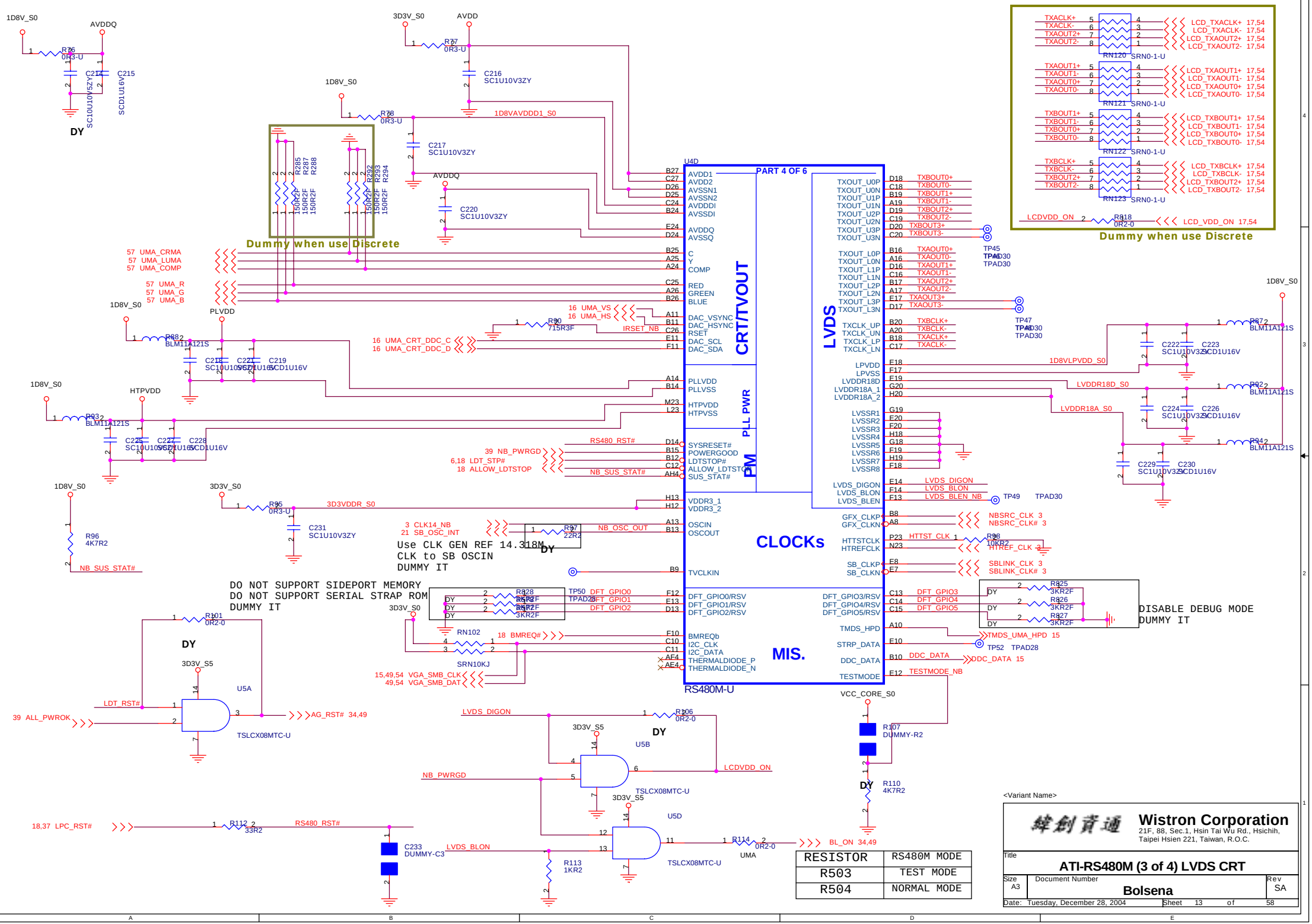
<Variant Name>

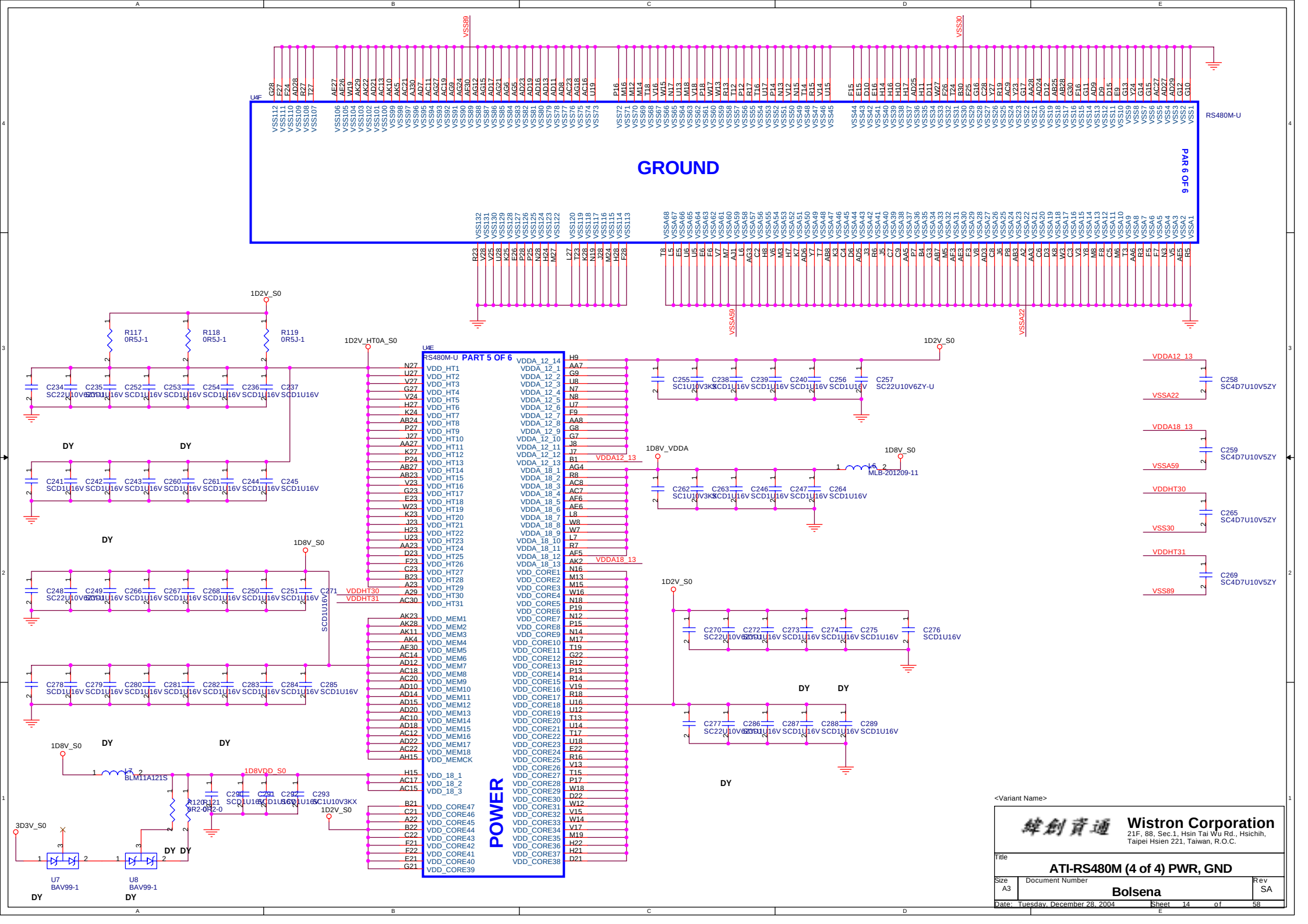
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

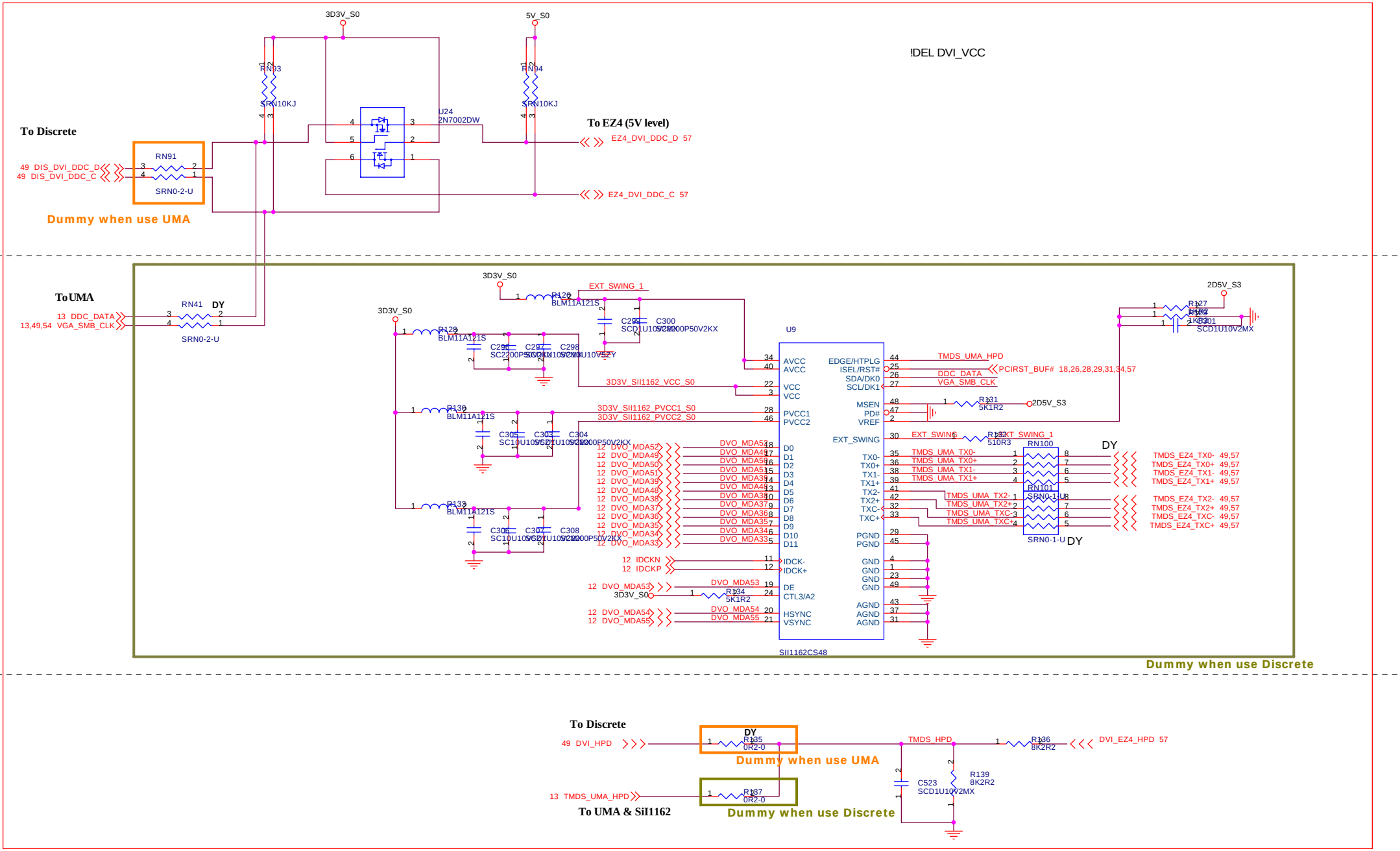
Title: ATI-RS480M (2 of 4) PCIE

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 12 of 58


1D8V_S0
AVDDQ
R26 0R3-U
C214 SC10U10V5ZY
C215 SCD1U16V
DY
3D3V_S0
AVDD
R27 0R3-U
C216 SC1U10V3ZY
1D8V_S0
R28 0R3-U
1D8VAVDDD1_S0
C217 SC1U10V3ZY
AVDDQ
C220 SC1U10V3ZY
R285 150R2F
R287 150R2F
R288 150R2F
R292 150R2F
R293 150R2F
R294 150R2F
Dummy when use Discrete
U4D
PART 4 OF 6
B27 AVDD1
C27 AVDD2
D26 AVSSN1
D25 AVSSN2
C24 AVDDDI
B24 AVSSDI
E24 AVDDQ
D24 AVSSQ
B25 C
A25 Y
A24 COMP
C25 RED
A26 GREEN
B26 BLUE
A11 DAC_VSYNC
B11 DAC_HSYNC
C26 RSET
E11 DAC_SCL
F11 DAC_SDA
CRT/TVOUT
A14 PLLVDD
B14 PLLVSS
M23 HTPVDD
L23 HTPVSS
PLL PWR
D14 SYSRESET#
B15 POWERGOOD
B12 LDTSTOP#
C12 ALLOW_LDTSTOP
AH4 SUS_STAT#
PM
H13 VDDR3_1
H12 VDDR3_2
A13 OSCIN
B13 OSCOUT
B9 TVCLKIN
CLOCKs
F12 DFT_GPIO0/RSV
E13 DFT_GPIO1/RSV
D13 DFT_GPIO2/RSV
F10 BMREQb
C10 I2C_CLK
C11 I2C_DATA
AE4 THERMALDIODE_P
AE4 THERMALDIODE_N
MIS.
RS480M-U
LVDS
D18 TXOUT_U0P
C18 TXOUT_U0N
B19 TXOUT_U1P
A19 TXOUT_U1N
D19 TXOUT_U2P
C19 TXOUT_U2N
D20 TXOUT_U3P
C20 TXOUT_U3N
B16 TXOUT_L0P
A16 TXOUT_L0N
D16 TXOUT_L1P
C16 TXOUT_L1N
B17 TXOUT_L2P
A17 TXOUT_L2N
E17 TXOUT_L3P
D17 TXOUT_L3N
B20 TXCLK_UP
A20 TXCLK_UN
B18 TXCLK_LP
C17 TXCLK_LN
E18 LPVDD
F17 LPVSS
E19 LVDDR18D
G20 LVDDR18A_1
H20 LVDDR18A_2
G19 LVSSR1
E20 LVSSR2
F20 LVSSR3
H18 LVSSR4
G18 LVSSR5
F19 LVSSR6
H19 LVSSR7
F18 LVSSR8
E14 LVDS_DIGON
F14 LVDS_BLON
F13 LVDS_BLEN
B8 GFX_CLKP
A8 GFX_CLKN
P23 HTTSTCLK
N23 HTREFCLK
E8 SB_CLKP
E7 SB_CLKN
C13 DFT_GPIO3/RSV
C14 DFT_GPIO4/RSV
C15 DFT_GPIO5/RSV
A10 TMDS_HPD
E10 STRP_DATA
B10 DDC_DATA
F12 TESTMODE
TXACLK+ TXACLK- TXAOUT2+ TXAOUT2-
RN120 SRN0-1-U
TXAOUT1+ TXAOUT1- TXAOUT0+ TXAOUT0-
RN121 SRN0-1-U
TXBOUT1+ TXBOUT1- TXBOUT0+ TXBOUT0-
RN122 SRN0-1-U
TXBCLK+ TXBCLK- TXBOUT2+ TXBOUT2-
RN123 SRN0-1-U
LCD_TXACLK+ LCD_TXACLK- LCD_TXAOUT2+ LCD_TXAOUT2-
LCD_TXAOUT1+ LCD_TXAOUT1- LCD_TXAOUT0+ LCD_TXAOUT0-
LCD_TXBOUT1+ LCD_TXBOUT1- LCD_TXBOUT0+ LCD_TXBOUT0-
LCD_TXBCLK+ LCD_TXBCLK- LCD_TXBOUT2+ LCD_TXBOUT2-
LCDVDD_ON R118 0R2-0 LCD_VDD_ON
Dummy when use Discrete
TP45 TPAD30
TP46 TPAD30
TP47 TPAD30
TP48 TPAD30
TP49 TPAD30
TP50 TPAD28
TP52 TPAD28
57 UMA_CRMA
57 UMA_LUMA
57 UMA_COMP
57 UMA_R
57 UMA_G
57 UMA_B
16 UMA_VS
16 UMA_HS
IRSET_NB R90 715R3F
16 UMA_CRT_DDC_C
16 UMA_CRT_DDC_D
R882 BLM11A121S
C218 SC10U10V5ZY
C221 SC1U10V3ZY
C219 SCD1U16V
HTPVDD
R932 BLM11A121S
C225 SC10U10V5ZY
C227 SC1U10V3ZY
C228 SCD1U16V
RS480_RST#
39 NB_PWRGD
6,18 LDT_STP#
18 ALLOW_LDTSTOP
NB_SUS_STAT#
R95 0R3-U
3D3VDDR_S0
C231 SC1U10V3ZY
R96 4K7R2
NB_SUS_STAT#
3 CLK14_NB
21 SB_OSC_INT
R97 22R2
NB_OSC_OUT
Use CLK GEN REF 14.318M
CLK to SB OSCIN
DUMMY IT
DY
DO NOT SUPPORT SIDEPORT MEMORY
DO NOT SUPPORT SERIAL STRAP ROM
DUMMY IT
R98 10KR2
HTREF_CLK 3
NBSRC_CLK 3
NBSRC_CLK# 3
SBLINK_CLK 3
SBLINK_CLK# 3
LVDS_DIGON
LVDS_BLON
LVDS_BLEN_NB
HTTST_CLK 1
DFT_GPIO0
DFT_GPIO1
DFT_GPIO2
DFT_GPIO3
DFT_GPIO4
DFT_GPIO5
R825 3KR2F
R826 3KR2F
R827 3KR2F
DISABLE DEBUG MODE
DUMMY IT
TMDS_UMA_HPD 15
DDC_DATA 15
R101 0R2-0
3D3V_S5
U5A
LDT_RST#
39 ALL_PWROK
TSLCX08MTC-U
AG_RST# 34,49
RN102
18 BMREQ#
SRN10KJ
15,49,54 VGA_SMB_CLK
49,54 VGA_SMB_DAT
LVDS_DIGON
R106 0R2-0
U5B
LCDVDD_ON
NB_PWRGD
U5D
VCC_CORE_S0
R107 DUMMY-R2
R110 4K7R2
18,37 LPC_RST#
R112 33R2
C233 DUMMY-C3
R113 1KR2
R114 0R2-0
BL_ON 34,49
UMA
C222 SC1U10V3ZY
C223 SCD1U16V
C224 SC1U10V3ZY
C226 SCD1U16V
C229 SC1U10V3ZY
C230 SCD1U16V
R872 BLM11A121S
R922 BLM11A121S
R942 BLM11A121S
1D8VLPVDD_S0
LVDDR18D_S0
LVDDR18A_S0
RESISTOR
R503
R504
RS480M MODE
TEST MODE
NORMAL MODE
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS480M (3 of 4) LVDS CRT
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 13 of 58


GROUND
PAR 6 OF 6
RS480M-U
PART 5 OF 6
POWER
1D2V_S0
1D8V_S0
1D8V_VDDA
1D2V_HT0A_S0
1D8VDD_S0
3D3V_S0
VDDA12_13
VDDA18_13
VDDHT30
VDDHT31
VSS89
VSS30
VSSA59
VSSA22
U7 BAV99-1
U8 BAV99-1
DY
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATI-RS480M (4 of 4) PWR, GND
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 14 of 58



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<variant_name>

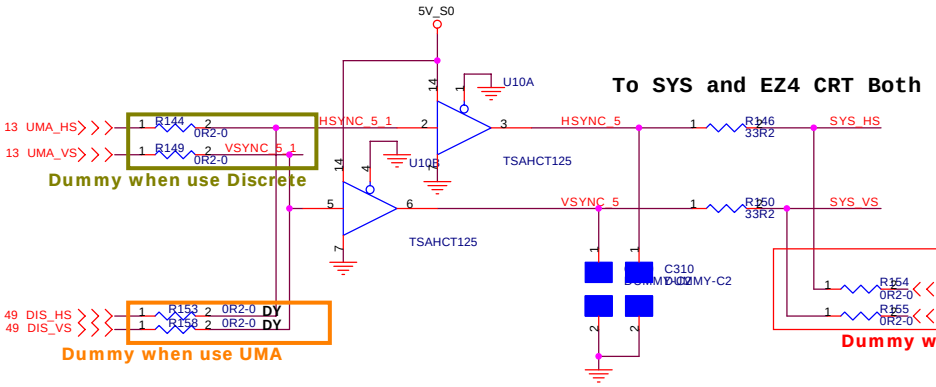
Title: UMA DVI - SiI 1162

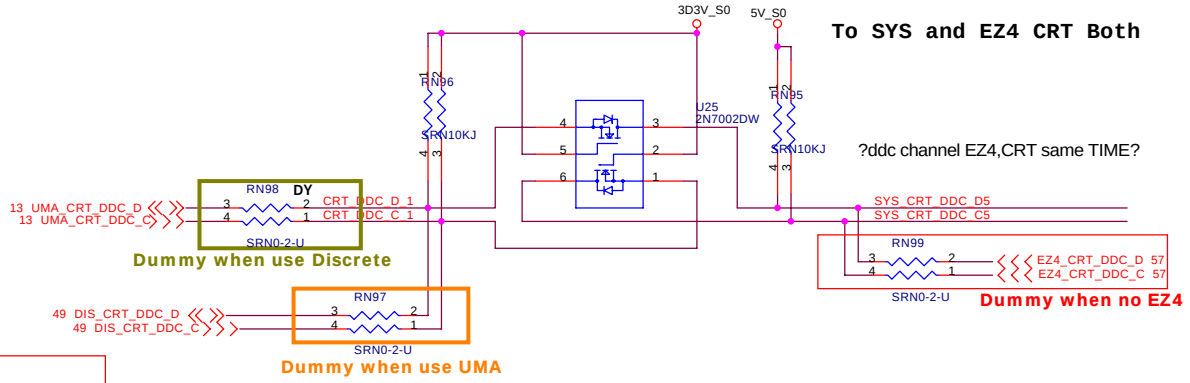
Size: A3 | Document Number: Bolsena | Rev: SA

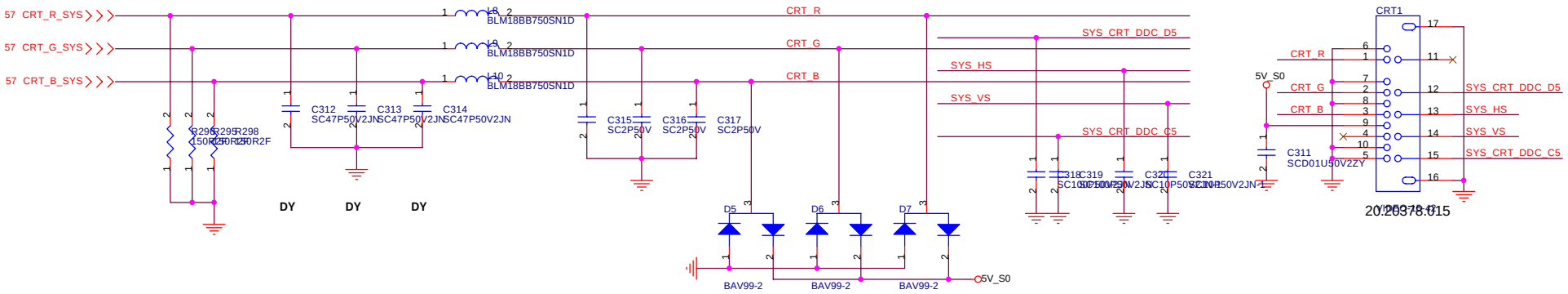
Date: Tuesday, December 28, 2004 | Sheet 15 of 58

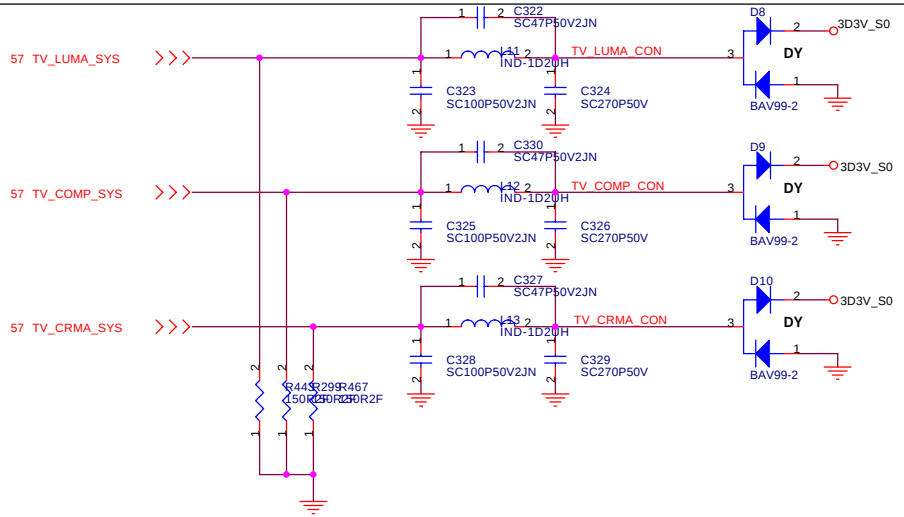
CRT CONN

200mA Rating/Spec 500mA

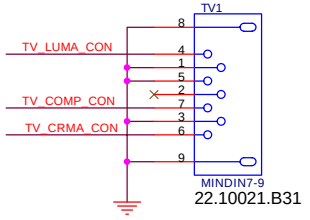


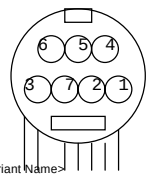






TV CONN





Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CRT / TV

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 16 of 58

LEDs

34 NUM_LED#
34 CAP_LED#
34 MAIL_LED#
34 BLT_LED#
34 WLAN_LED#
34 STDBY_LED#
34 CHARGE_LED#

Dummy when use IDE

19 SATA_LED# — R138 DY 0R2-0

25 HDD_LED#_5 — R140 0R2-0 — D11 BAW56 — MEDIA_LED#

Dummy when use SATA

25 CDROM_LED#_5

RC15 SRC100P50V-U
NUM_LED#
CAP_LED#
MAIL_LED#
MEDIA_LED#

RC16 SRC100P50V-U
WLAN_LED#
STDBY_LED#
PWRLED#
CHARGE_LED#

BLT_LED# — C714 SC100P50V2JN

PWRLED# — Q7 PDTC144EU — 3D3V_S0

3D3V_S0

NUM_LED# — R566 330R2 — D_NUM1 LED-G-31
CAP_LED# — R567 330R2 — D_CAPS1 LED-G-31
MAIL_LED# — R568 330R2 — D_MAIL1 LED-G-31
MEDIA_LED# — R572 330R2 — D_MEDIA1 LED-G-31
WLAN_LED# — R573 330R2 — D_WLAN1 LED-Y-22
BLT_LED# — R565 330R2 — D_BTH1 LED-B-13-U

3D3V_S5

STDBY_LED# — R569 330R2 — D_STDBY1 LED-Y-22
PWRLED# — R570 330R2 — D_PWR1 LED-G-31
CHARGE_LED# — R571 330R2 — D_CHGR1 LED-Y-22

on KB cover

LED	V	V				V	V	V
Button	V	V	V	V	V			
	POWER	E-MAIL	INTERNET	e-BTN	PROGRAM	CAPS	NUM	HDD

Front panel

LED	V	V	V	V
Button	V	V		
	BlutTooth	Wireless	Charger	Power

LCD CONN

LCD CONN

LCDPOWER_S0

C343 SC1U10V2ZU — C344 SC1U10V2ZU — C345 SCD1U

DY DY

LCD1 ETY-CONN40D-1

37 PANEL_ID0
37 PANEL_ID1
37 PANEL_ID2
37 PANEL_ID3

34 FPBACK — R888 10KR2
34 BRIGHTNESS

C716 SC100P50V2JN — C715 SC100P50V2JN

LCD_TXBCLK+ 13,54
LCD_TXBCLK- 13,54
LCD_TXBOUT2+ 13,54
LCD_TXBOUT2- 13,54
LCD_TXBOUT1+ 13,54
LCD_TXBOUT1- 13,54
LCD_TXBOUT0+ 13,54
LCD_TXBOUT0- 13,54
LCD_TXACLK+ 13,54
LCD_TXACLK- 13,54
LCD_TXAOUT2+ 13,54
LCD_TXAOUT2- 13,54
LCD_TXAOUT1+ 13,54
LCD_TXAOUT1- 13,54
LCD_TXAOUT0+ 13,54
LCD_TXAOUT0- 13,54

EVEN CHANNEL
ODD CHANNEL

?add net?

20.F0322.040

LCD POWER

Layout 40 mil

13,54 LCD_VDD_ON — R160 1KR2 — LCDVDD_ON_1

LCDPOWER_S0

U11 AAT4280IGU-3-T1
OUT GND ON/OFF# IN GND IN

C346 SC1U10V3KX — C347 SCD1U — C348 SC1U10V3KX

3D3V_S0

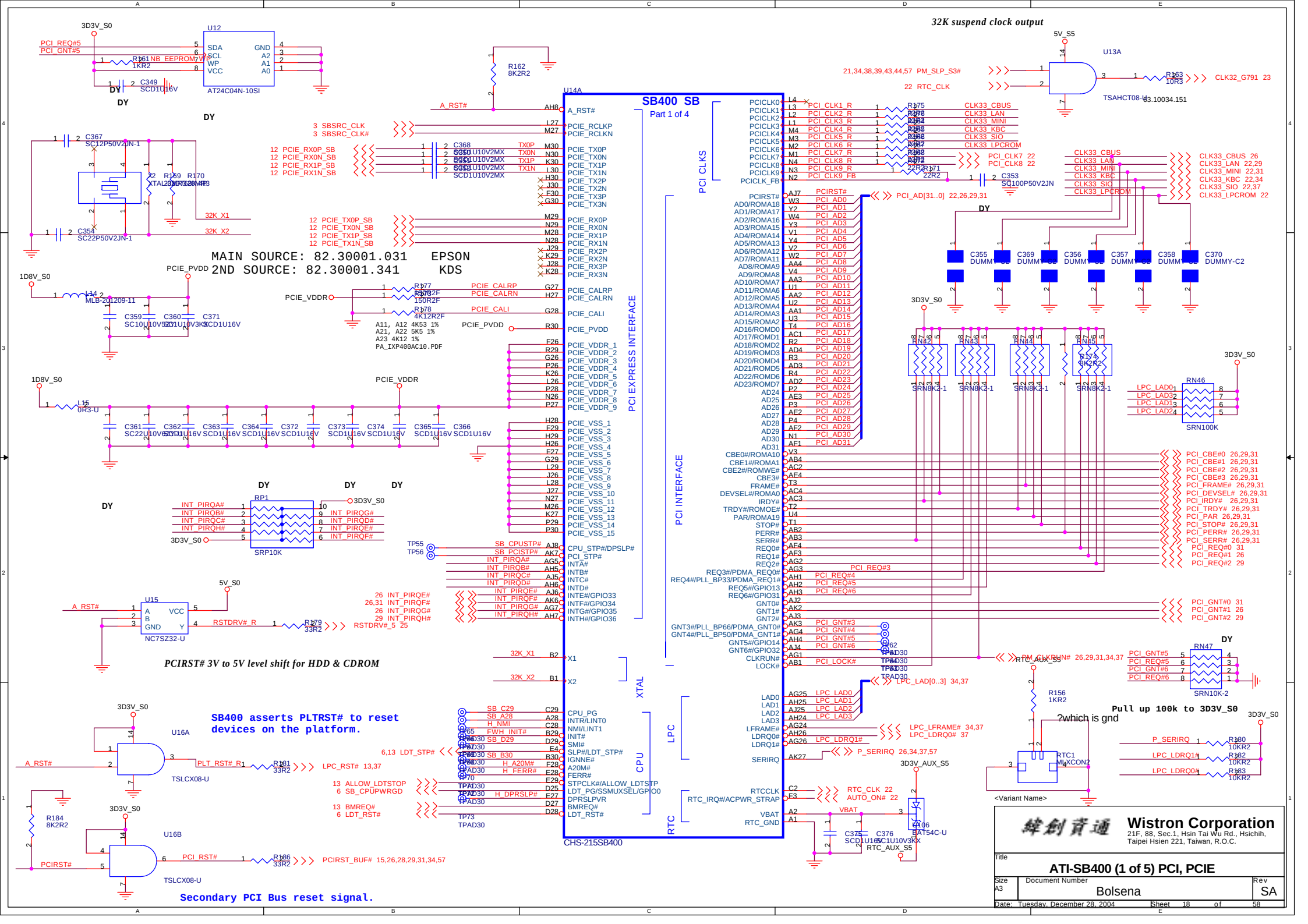
<Variant Name>

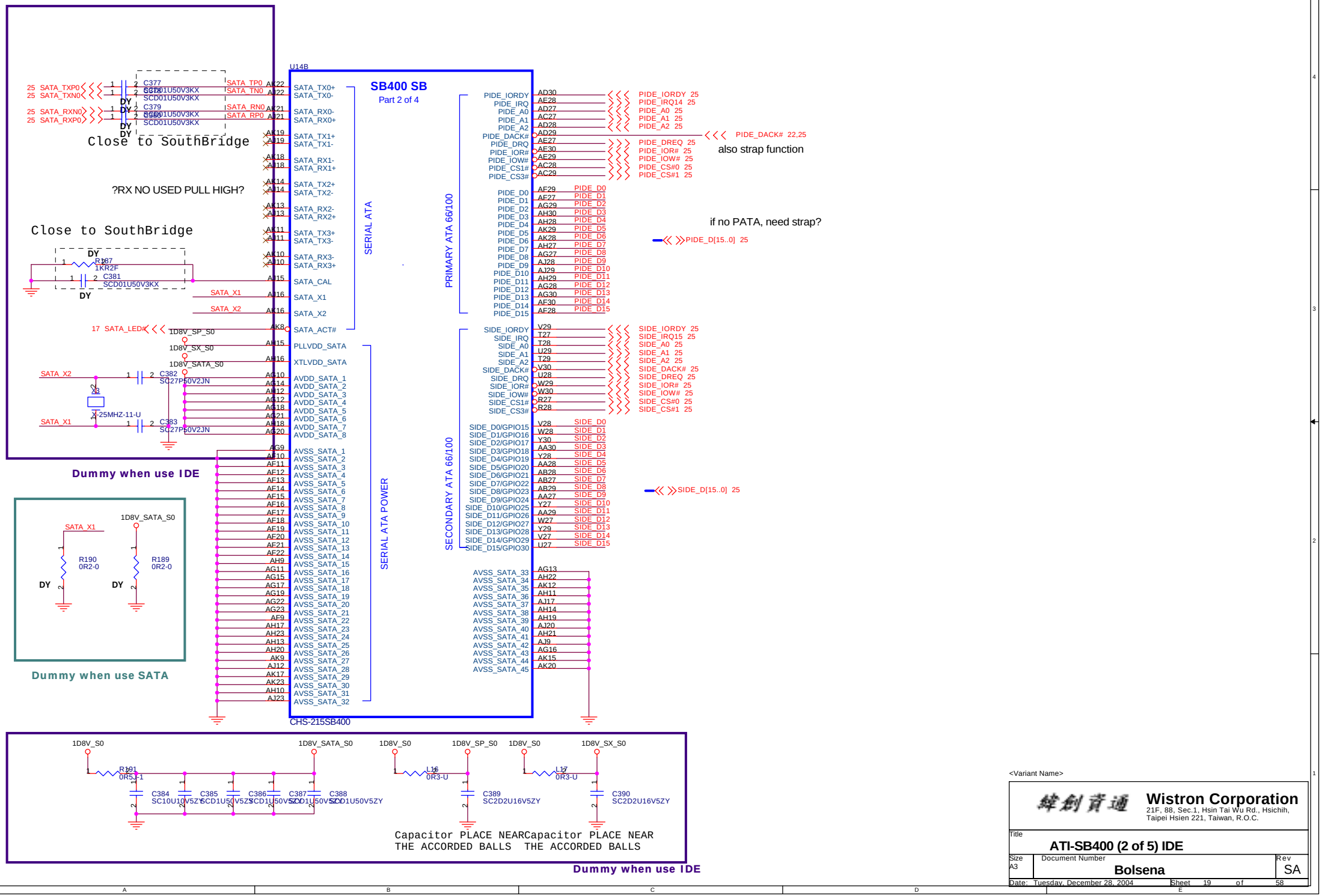
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **INV / LCD / LEDs**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 17 of 58


32K suspend clock output
MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
SB400 SB
Part 1 of 4
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKS
XTAL
LPC
CPU
RTC
CHS-215SB400
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
Pull up 100k to 3D3V_S0
?which is gnd
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
ATI-SB400 (1 of 5) PCI, PCIE
Size A3
Document Number Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 18 of 58



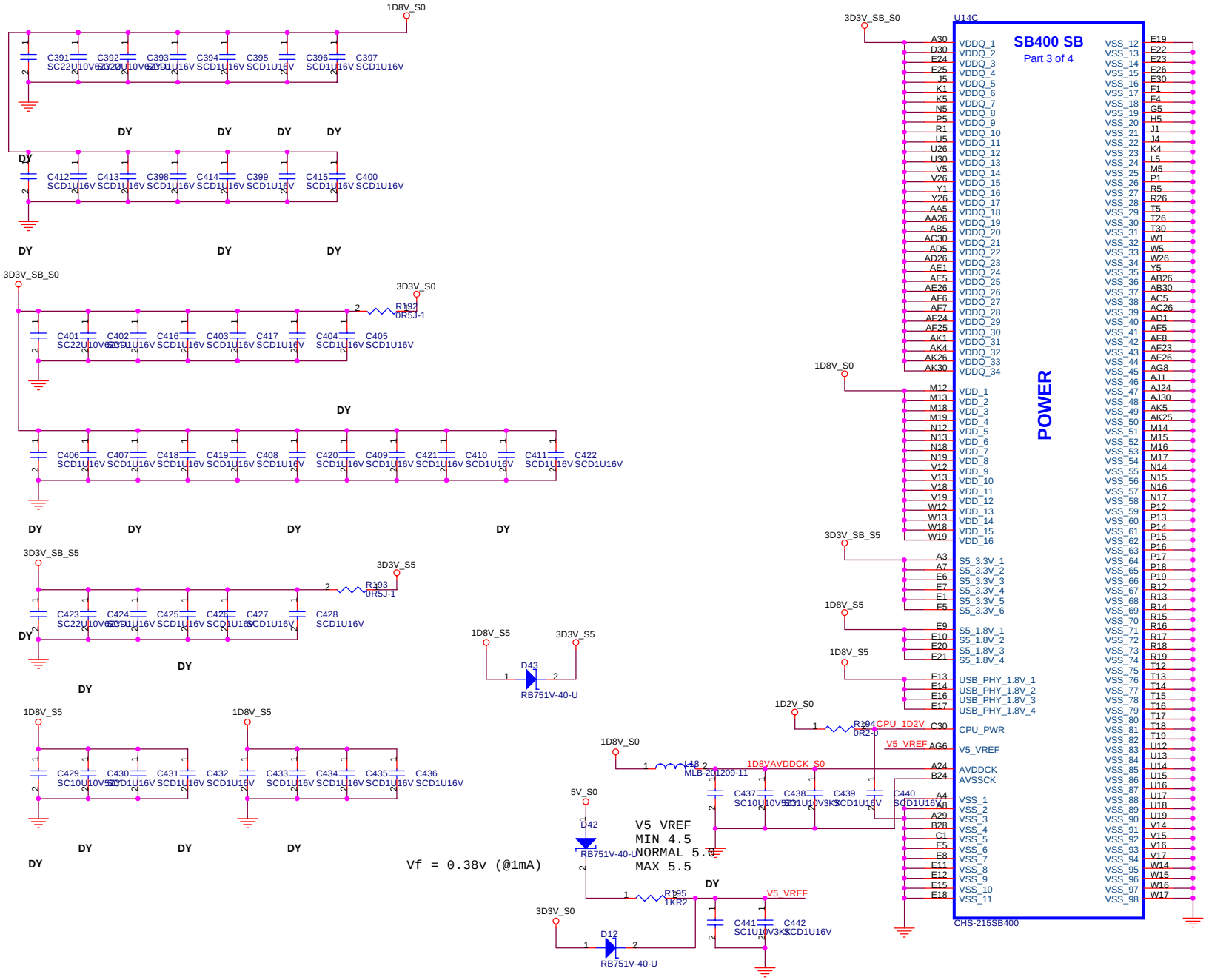
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATI-SB400 (2 of 5) IDE**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 19 of 58



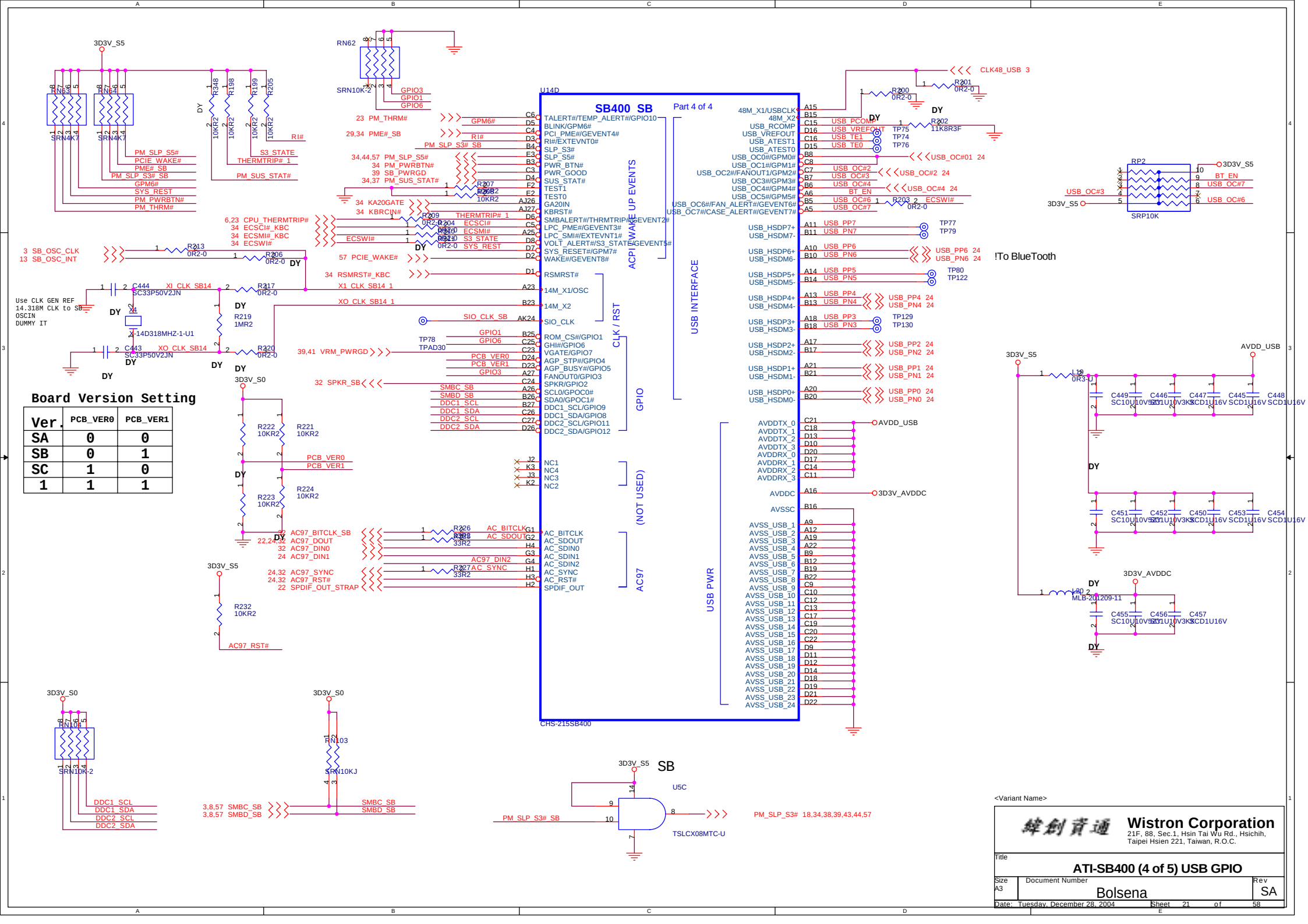
<Variant Name>

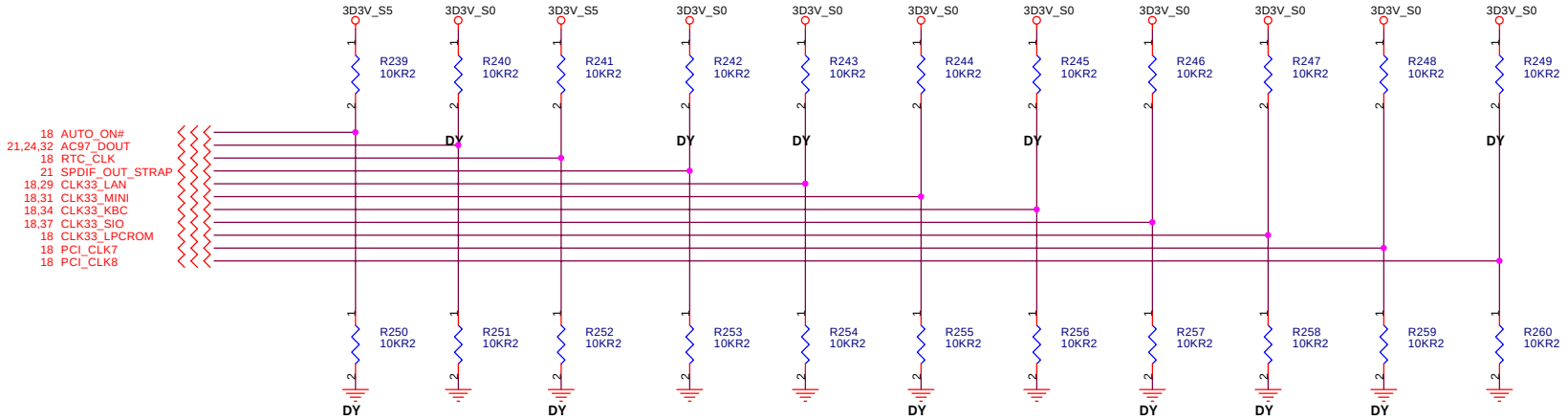
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 (3 of 5) POWER

Size	Document Number	Rev
A3	Bolsena	SA

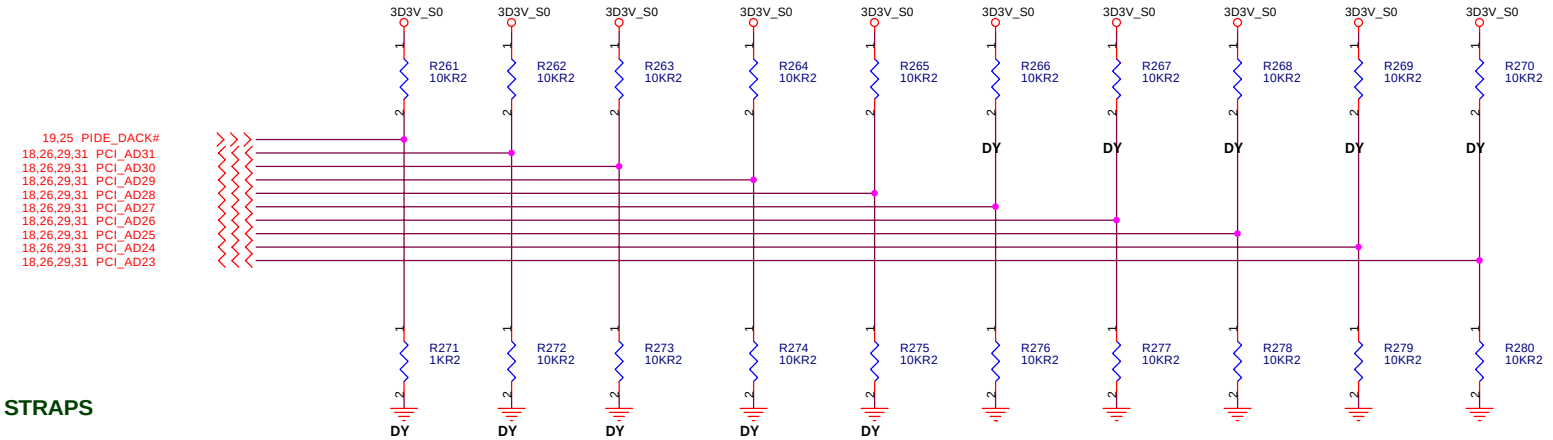
Date: Tuesday, December 28, 2004 Sheet 20 of 58


SB400 SB
Part 4 of 4
U14D
CHS-215SB400
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
(NOT USED)
AC97
USB INTERFACE
USB PWR
Board Version Setting
Ver. PCB_VER0 PCB_VER1
SA 0 0
SB 0 1
SC 1 0
1 1 1
!To BlueTooth
SB
U5C
TSLCX08MTC-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
<Variant Name>
Title
ATI-SB400 (4 of 5) USB GPIO
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 21 of 58



REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48 DEFAULT	14MHZ OSC MODE DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ -Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

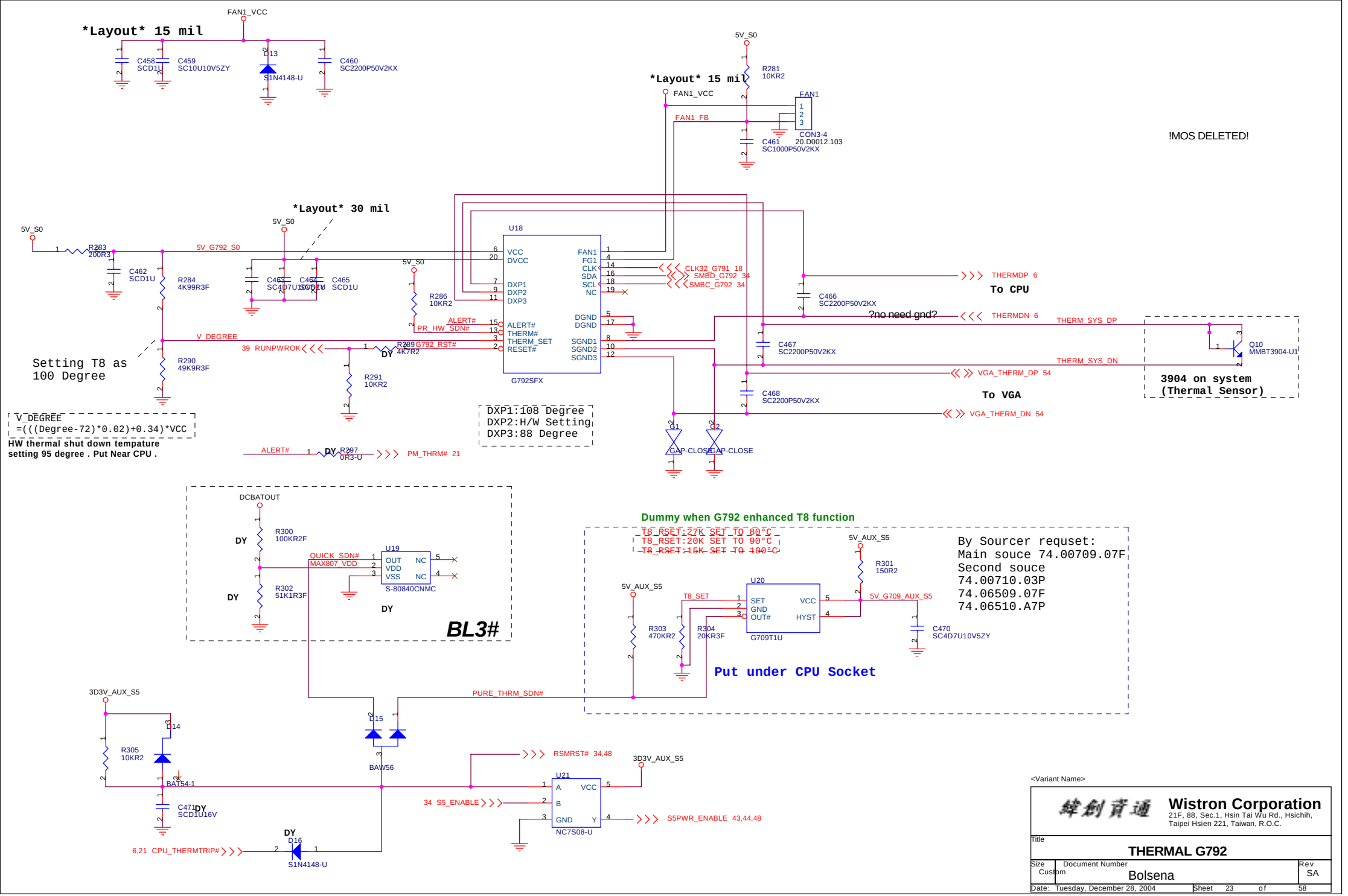
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI-SB400 STRAPPING(5 of 5)

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 22 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **THERMAL G792**

Size	Document Number	Rev
Custom	Bolsena	SA

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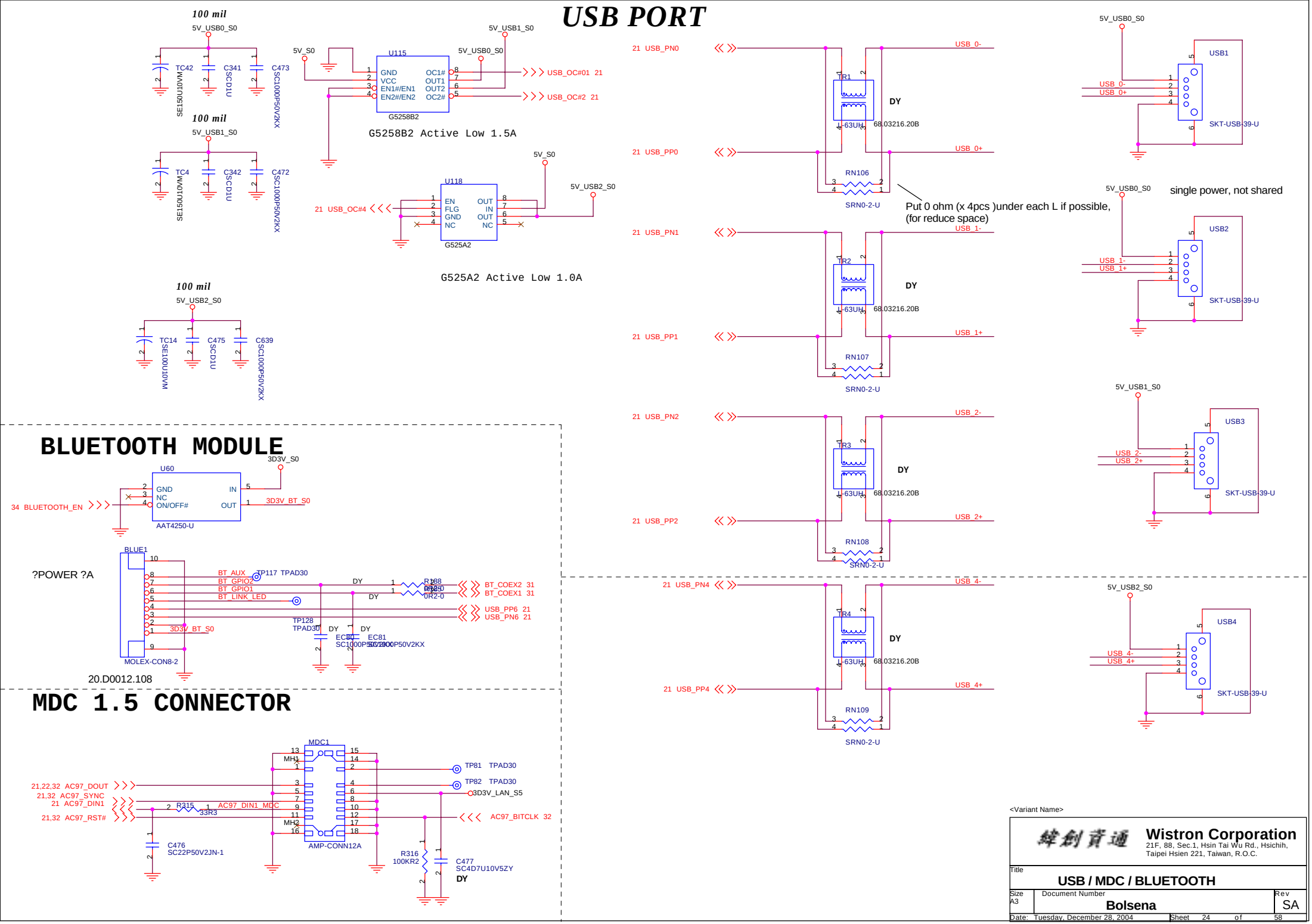
USB PORT



BLUETOOTH MODULE

MDC 1.5 CONNECTOR

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB / MDC / BLUETOOTH**

Size	Document Number	Rev
A3	**Bolsena**	SA

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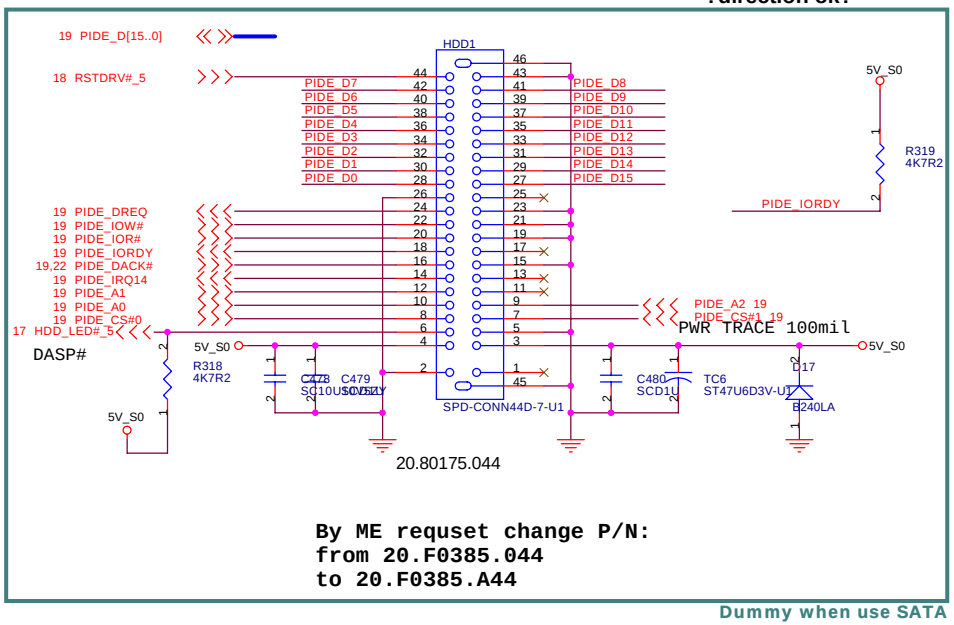
HDD

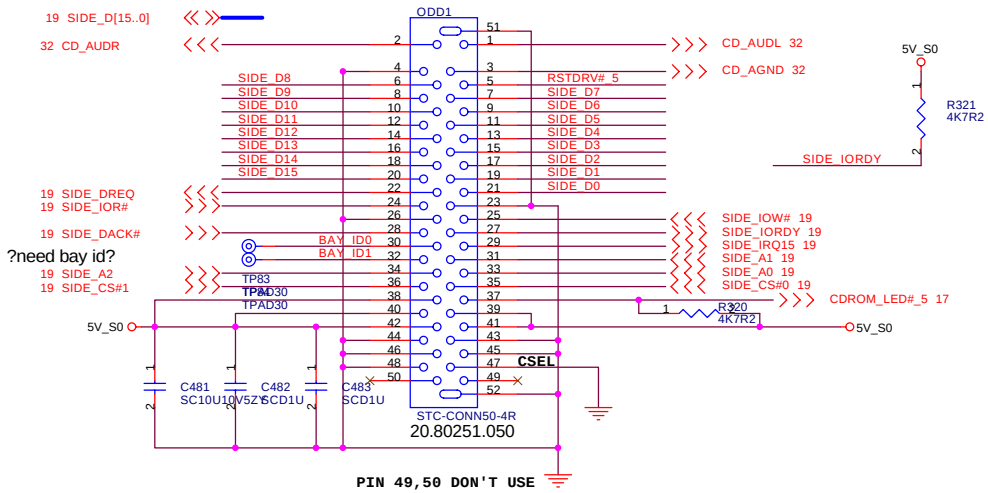
?direction ok?



By ME requset change P/N:
from 20.F0385.044
to 20.F0385.A44

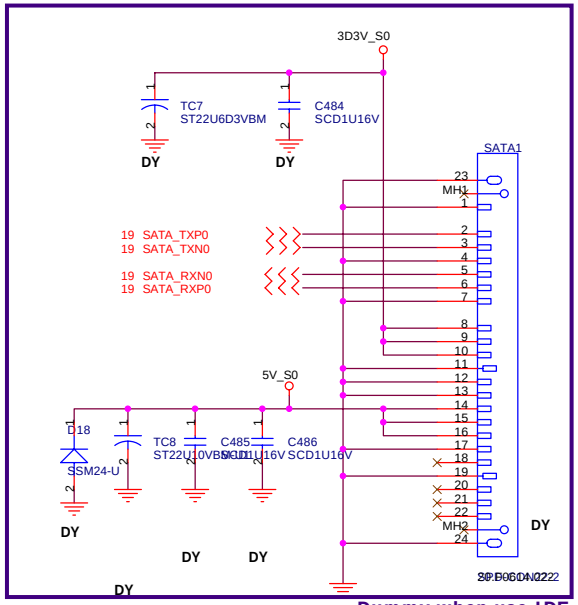
Dummy when use SATA

CDROM



PIN 49,50 DON'T USE

SATA Connector



Dummy when use IDE

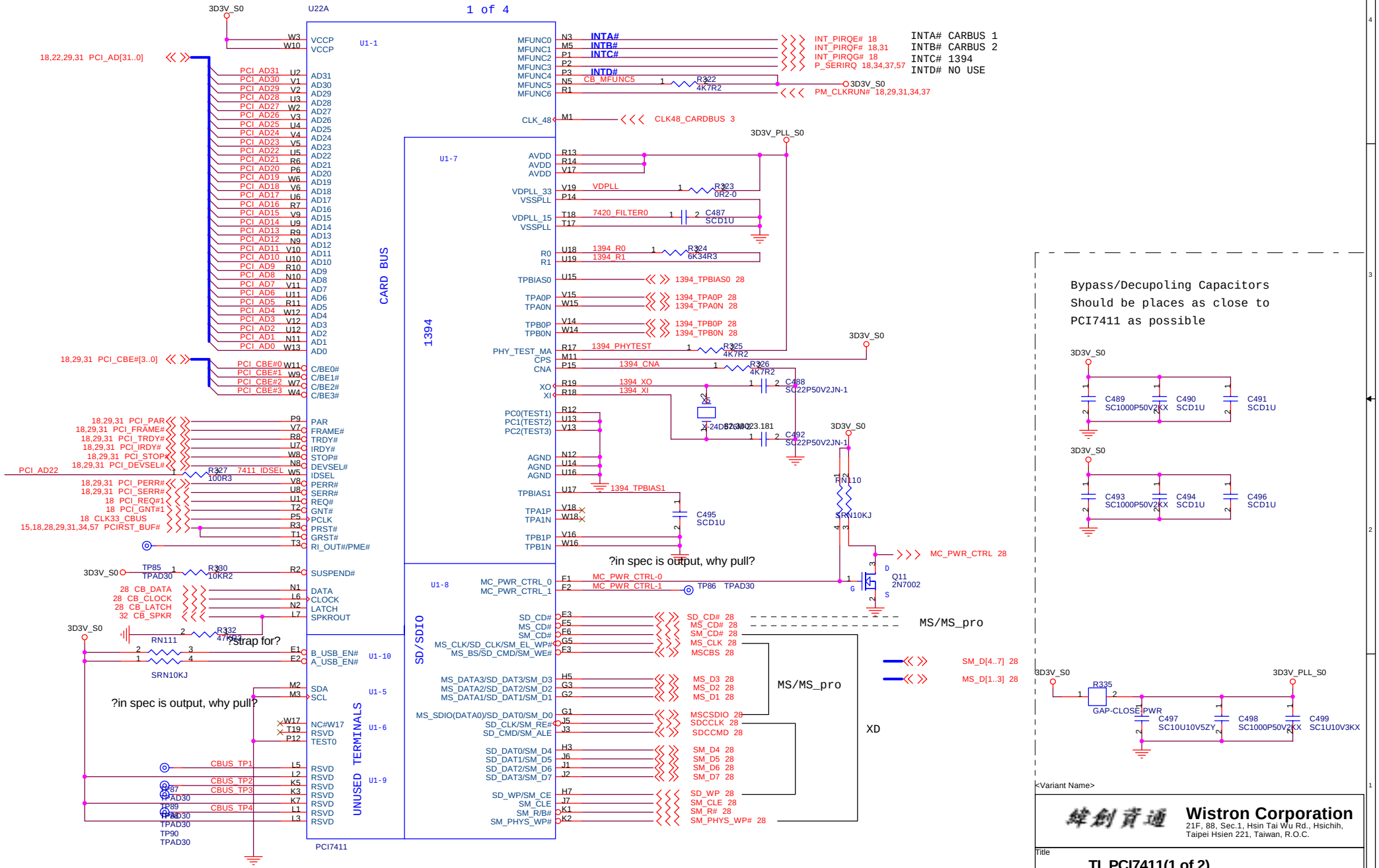
<Variant Name>

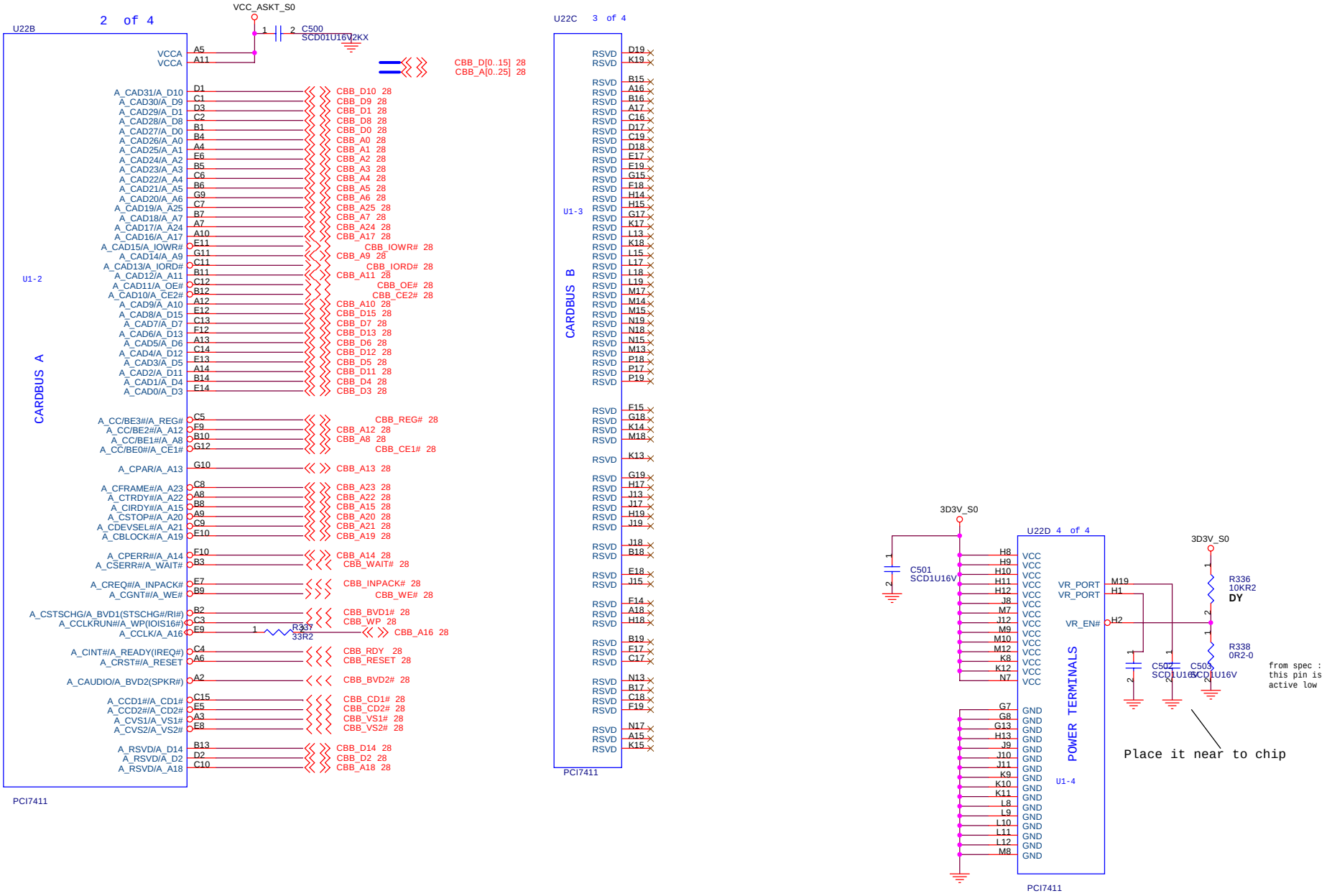
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDD / CDROM / SATA**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 25 of 58


1 of 4
U22A
CARD BUS
1394
SD/SDIO
UNUSED TERMINALS
PCI7411
U1-1
U1-7
U1-8
U1-10
U1-5
U1-6
U1-9
3D3V_S0
3D3V_PLL_S0
18,22,29,31 PCI_AD[31..0]
18,29,31 PCI_CBE#[3..0]
CLK48_CARDBUS 3
PM_CLKRUN# 18,29,31,34,37
INT_PIRQE# 18
INT_PIRQF# 18,31
INT_PIRQG# 18
P_SERIRQ 18,34,37,57
INTA# CARBUS 1
INTB# CARBUS 2
INTC# 1394
INTD# NO USE
Bypass/Decupoling Capacitors
Should be places as close to
PCI7411 as possible
?in spec is output, why pull?
?strap for?
MS/MS_pro
XD
MC_PWR_CTRL 28
SM_D[4..7] 28
SM_D[1..3] 28
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TI_PCI7411(1 of 2)
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 26 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
TI_PCI7411(2 of 2)

Size	Document Number	Rev
A3	**Bolsena**	SA

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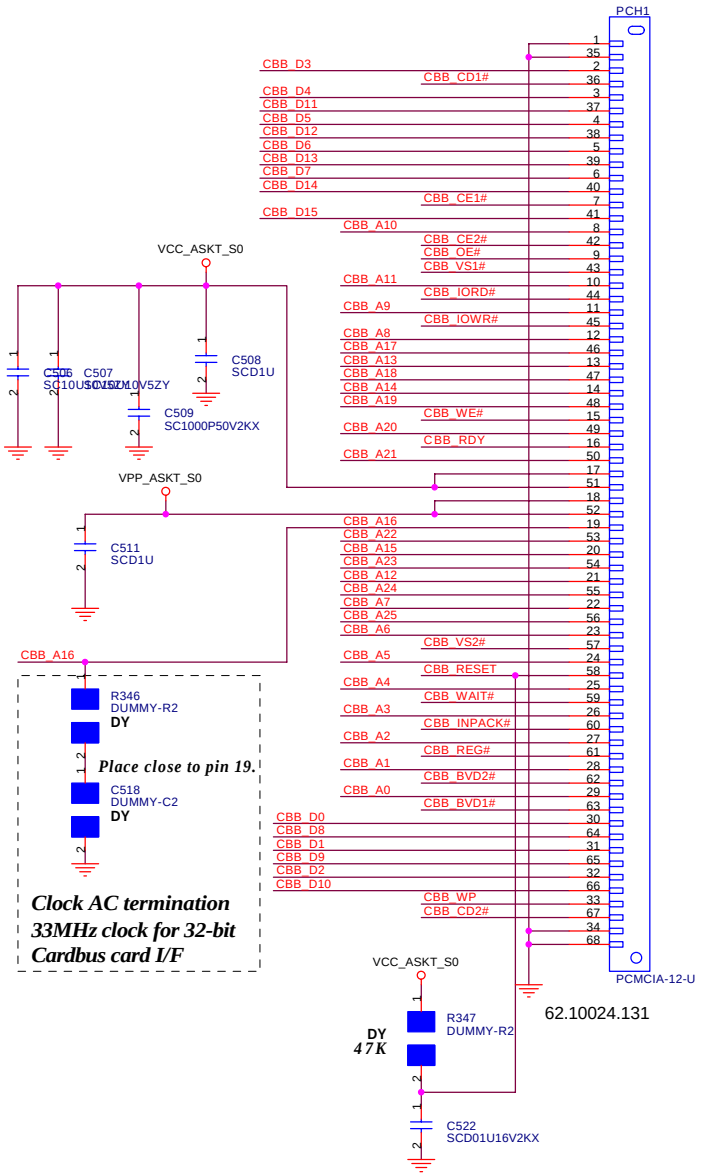
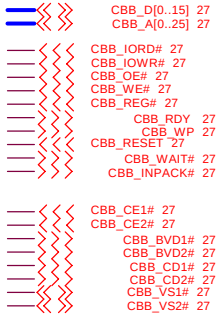
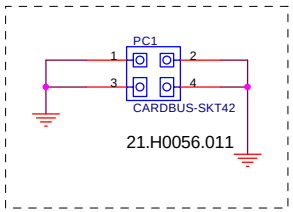
PCMCIA Socket

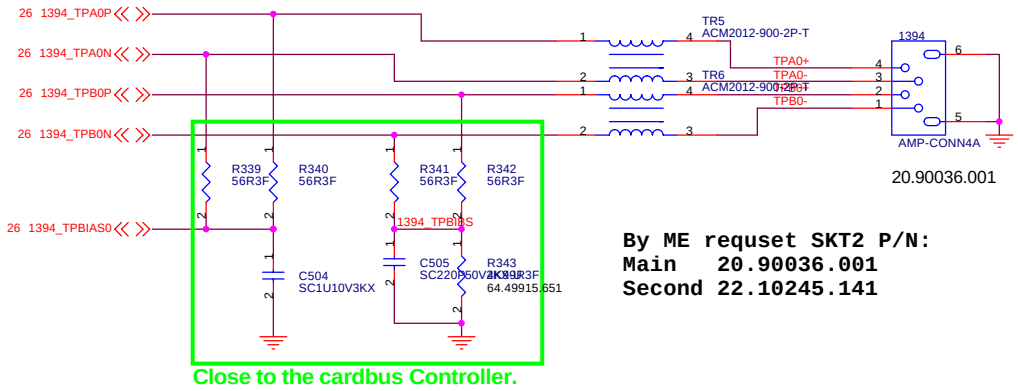


Cardbus I/F



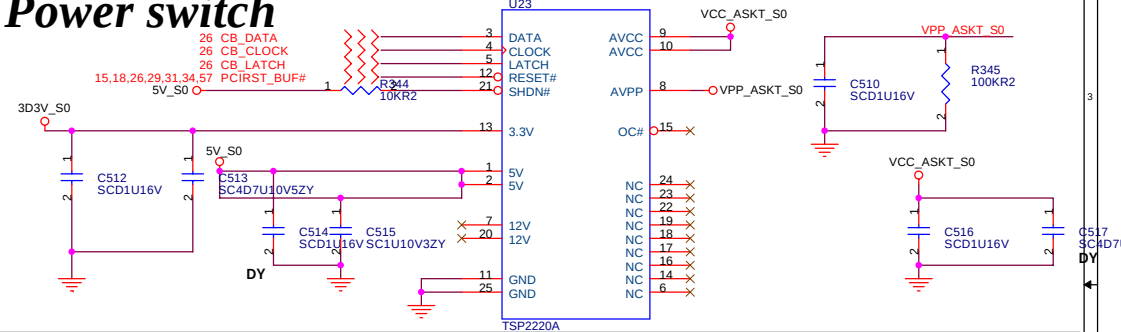


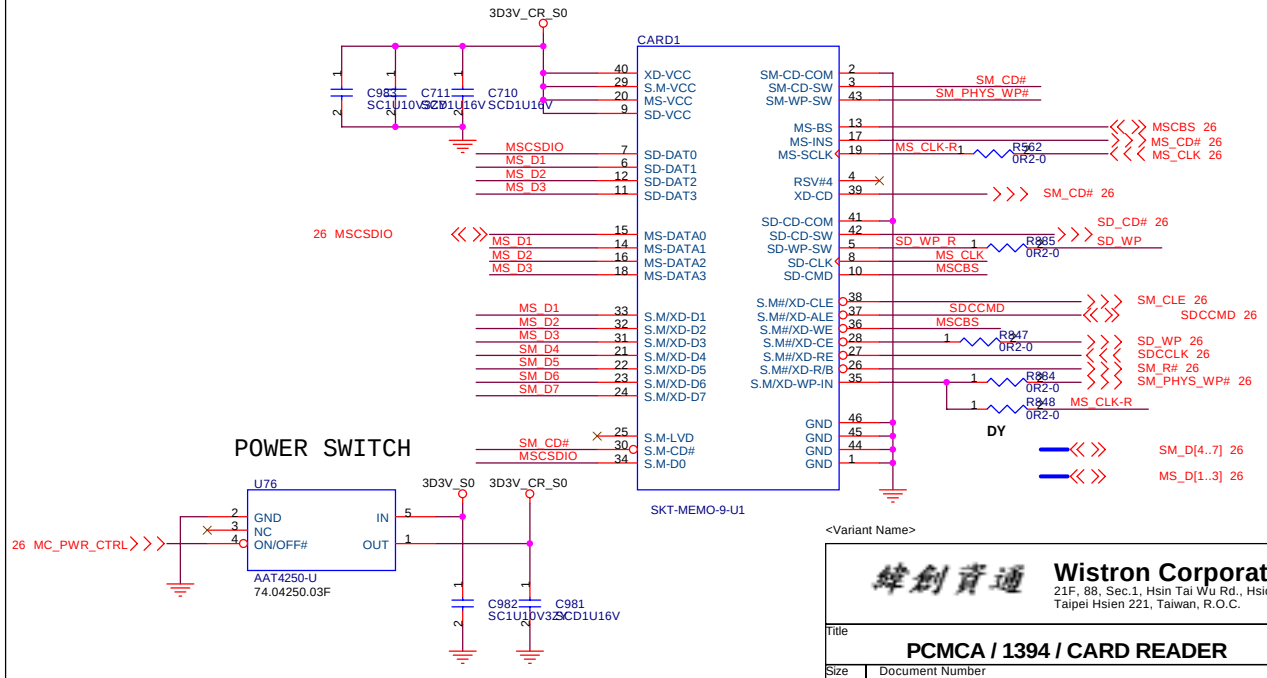
1394 Connector



By ME requset SKT2 P/N:
Main 20.90036.001
Second 22.10245.141

Power switch





<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**PCMCA / 1394 / CARD READER**	
Size A3	Document Number **Bolsena**	Rev SA
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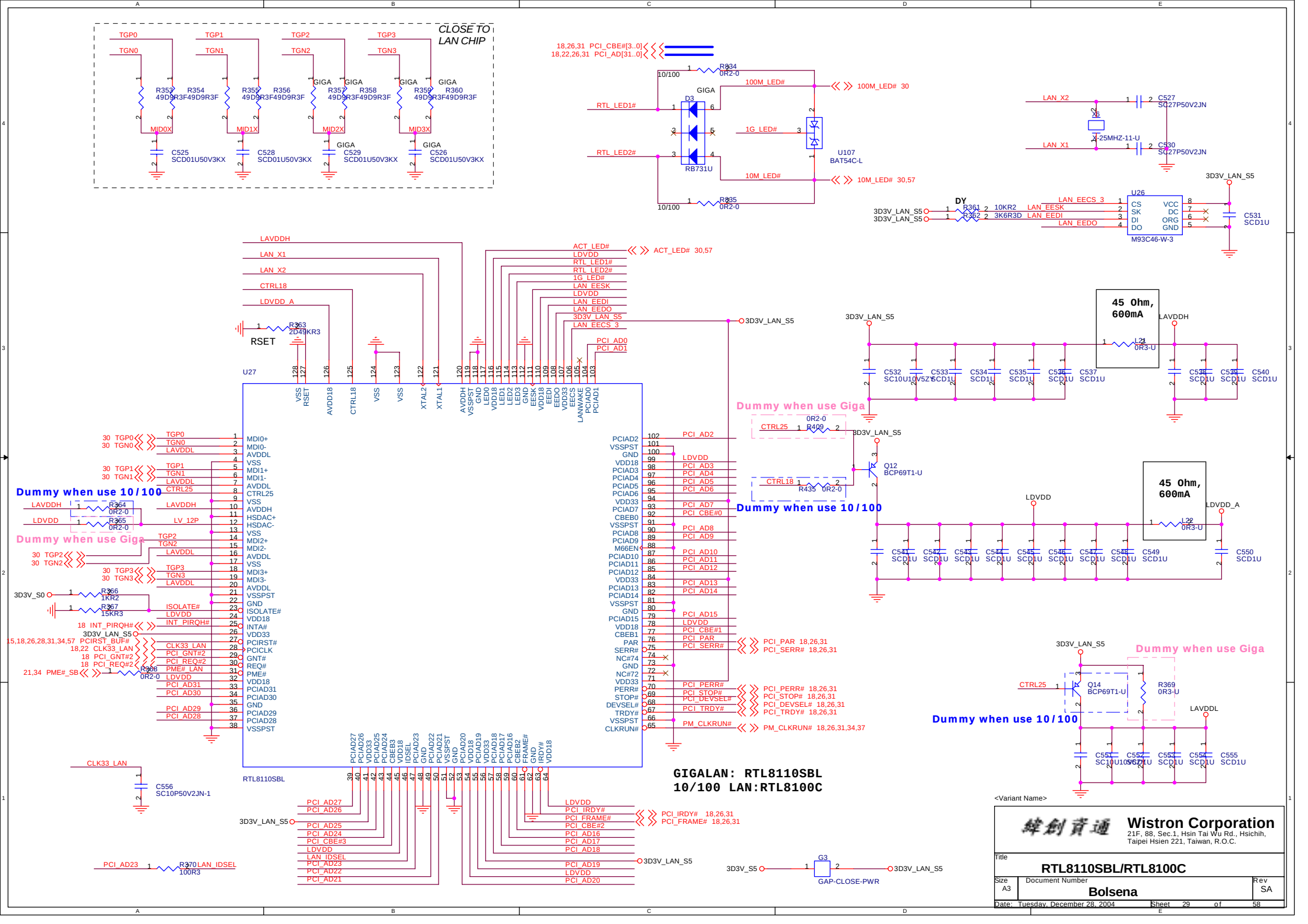

CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
TGP2
TGN2
TGP3
TGN3
R352 49D9R3F
R354 49D9R3F
R355 49D9R3F
R356 49D9R3F
R357 GIGA
R358 GIGA
R359 GIGA
R360 GIGA
MID0X
MID1X
MID2X
MID3X
C525 SCD01U50V3KX
C528 SCD01U50V3KX
C529 GIGA SCD01U50V3KX
C526 GIGA SCD01U50V3KX
18,26,31 PCI_CBE#[3..0]
18,22,26,31 PCI_AD[31..0]
R834 0R2-0
10/100
GIGA
D3
RTL_LED1#
RTL_LED2#
RB731U
100M_LED#
1G_LED#
10M_LED#
U107 BAT54C-L
100M_LED# 30
10M_LED# 30,57
R835 0R2-0
LAN_X2
LAN_X1
X6 25MHZ-11-U
C527 SC27P50V2JN
C530 SC27P50V2JN
3D3V_LAN_S5
DY
R361 10KR2
R362 3K6R3D
LAN_EESK
LAN_EEDI
LAN_EEDO
LAN_EECS_3
U26
CS
SK
DI
DO
VCC
DC
ORG
GND
M93C46-W-3
C531 SCD1U
LAVDDH
LAN_X1
LAN_X2
CTRL18
LDVDD_A
R363 2D49KR3
RSET
U27
ACT_LED#
LDVDD
RTL_LED1#
RTL_LED2#
1G_LED#
LAN_EESK
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
ACT_LED# 30,57
VSS
RSET
AVDD18
CTRL18
XTAL2
XTAL1
AVDDH
VSSPST
LED0
LED1
LED2
LED3
EESK
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1
45 Ohm, 600mA
L21 0R3-U
C532 SC10U10V5ZY
C533 SCD1U
C534 SCD1U
C535 SCD1U
C536 SCD1U
C537 SCD1U
C538 SCD1U
C539 SCD1U
C540 SCD1U
Dummy when use Giga
CTRL25
R409 0R2-0
Q12 BCP69T1-U
CTRL18
R435 0R2-0
Dummy when use 10/100
LDVDD
LDVDD_A
L22 0R3-U
C541 SCD1U
C542 SCD1U
C543 SCD1U
C544 SCD1U
C545 SCD1U
C546 SCD1U
C547 SCD1U
C548 SCD1U
C549 SCD1U
C550 SCD1U
30 TGP0
30 TGN0
TGP0
TGN0
LAVDDL
MDI0+
MDI0-
AVDDL
VSS
MDI1+
MDI1-
AVDDL
CTRL25
30 TGP1
30 TGN1
TGP1
TGN1
LAVDDL
VSS
AVDDH
HSDAC+
HSDAC-
VSS
MDI2+
MDI2-
AVDDL
VSS
MDI3+
MDI3-
AVDDL
VSSPST
GND
ISOLATE#
VDD18
INTA#
VDD33
PCIRST#
PCICLK
GNT#
REQ#
PME#
VDD18
PCIAD31
PCIAD30
GND
PCIAD29
PCIAD28
VSSPST
LAVDDH
LDVDD
R364 0R2-0
R365 0R2-0
LV_12P
30 TGP2
30 TGN2
TGP2
TGN2
30 TGP3
30 TGN3
TGP3
TGN3
3D3V_S0
R366 1KR2
R367 15KR3
ISOLATE#
LDVDD
INT_PIRQH#
18 INT_PIRQH#
3D3V_LAN_S5
15,18,26,28,31,34,57 PCIRST_BUF#
18,22 CLK33_LAN
18 PCI_GNT#2
18 PCI_REQ#2
21,34 PME#_SB
CLK33_LAN
PCI_GNT#2
PCI_REQ#2
PME#_LAN
R368 0R2-0
LDVDD
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
Dummy when use 10/100
Dummy when use Giga
PCIAD2
VSSPST
GND
VDD18
PCIAD3
PCIAD4
PCIAD5
PCIAD6
VDD33
PCIAD7
CBEB0
VSSPST
PCIAD8
PCIAD9
M66EN
PCIAD10
PCIAD11
PCIAD12
VDD33
PCIAD13
PCIAD14
VSSPST
GND
PCIAD15
VDD18
CBEB1
PAR
SERR#
NC#74
GND
NC#72
VDD33
PERR#
STOP#
DEVSEL#
TRDY#
VSSPST
CLKRUN#
PCI_AD2
LDVDD
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_CBE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
LDVDD
PCI_CBE#1
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN#
PCI_PAR 18,26,31
PCI_SERR# 18,26,31
PCI_PERR# 18,26,31
PCI_STOP# 18,26,31
PCI_DEVSEL# 18,26,31
PCI_TRDY# 18,26,31
PM_CLKRUN# 18,26,31,34,37
3D3V_LAN_S5
Dummy when use Giga
CTRL25
Q14 BCP69T1-U
R369 0R3-U
LAVDDL
Dummy when use 10/100
C551 SC10U10V5ZY
C552 SCD1U
C553 SCD1U
C554 SCD1U
C555 SCD1U
CLK33_LAN
C556 SC10P50V2JN-1
RTL8110SBL
PCIAD27
PCIAD26
VDD33
PCIAD25
PCIAD24
CBEB3
VDD18
IDSEL
GND
PCIAD23
PCIAD22
PCIAD21
VSSPST
GND
PCIAD20
VDD18
PCIAD19
VDD33
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAME#
GND
IRDY#
VDD18
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_CBE#3
LDVDD
LAN_IDSEL
PCI_AD23
PCI_AD22
PCI_AD21
PCI_IRDY#
PCI_FRAME#
PCI_CBE#2
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
LDVDD
PCI_AD20
PCI_IRDY# 18,26,31
PCI_FRAME# 18,26,31
PCI_AD23
R370 100R3
LAN_IDSEL
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
3D3V_S5
G3
GAP-CLOSE-PWR
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
RTL8110SBL/RTL8100C
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 29 of 58

Link: Green - 10Mbps/802.11b
Orange - 100Mbps/802.11a
Yellow - 1Gbps

Activity: Yellow

?LED COLOR?

22.10177.721

10/100M Lan Transformer

Dummy when use Giga

By Sourcer requset change P/N:
From 68.H0013.301
To 68.0H80P.301

By Sourcer requset change P/N:
From 68.H5015.301
To 68.02402.30A

GIGA Lan Transformer

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Dummy when use 10/100

For 10/100 Cap. changeto SCD1U

Dummy when use 10/100

Dummy when use Giga

Function	SEL
An to nB1	L
An to nB2	H

LAN switch

Dummy when no EZ4

Dummy when use EZ4

<Variant Name>

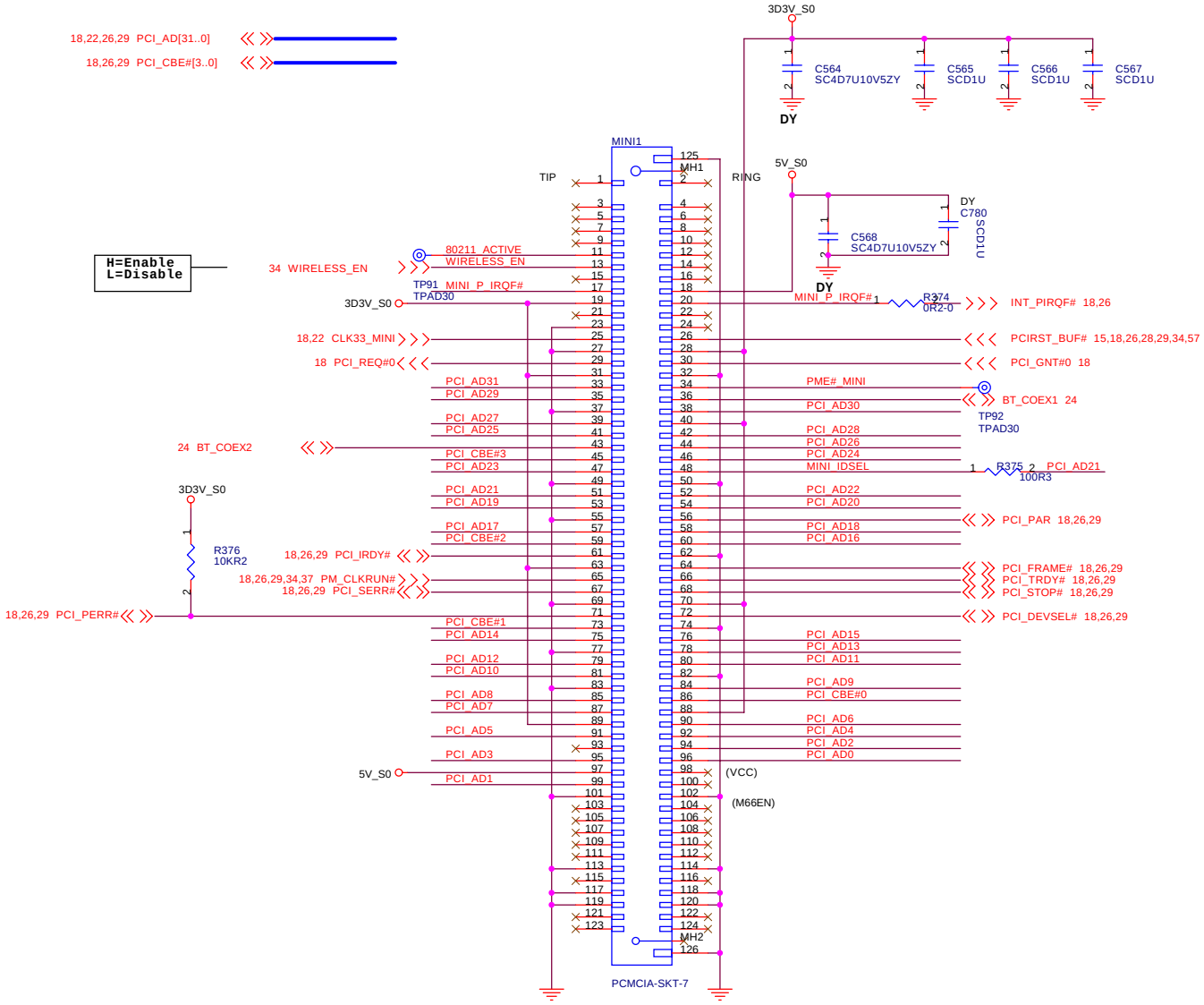
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN CONN

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 30 of 58

MINI-PCI



62.10071.001

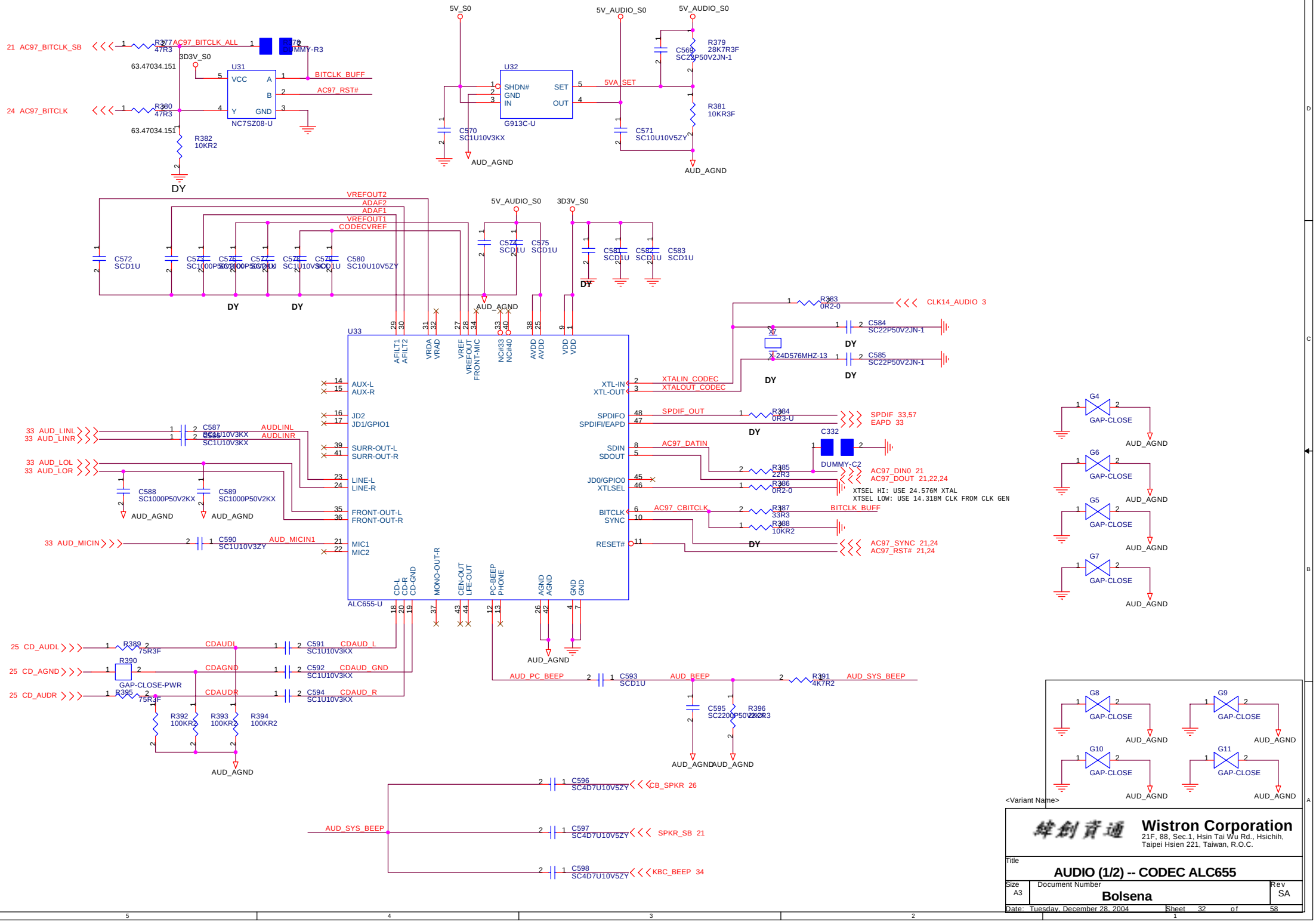
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINI-PCI**

Size	Document Number	Rev
A3	**Bolsena**	SA

Date: Tuesday, December 28, 2004 Sheet 31 of 58


21 AC97_BITCLK_SB
R377 47R3
AC97_BITCLK_ALL
R378 0R0MMY-R3
3D3V_S0
63.47034.151
U31
VCC
A
B
Y
GND
NC7SZ08-U
BITCLK_BUFF
AC97_RST#
24 AC97_BITCLK
R380 47R3
63.47034.151
R382 10KR2
DY
5V_S0
5V_AUDIO_S0
5V_AUDIO_S0
U32
SHDN#
GND
IN
SET
OUT
G913C-U
5VA_SET
C569 SC22P50V2JN-1
R379 28K7R3F
R381 10KR3F
C570 SC1U10V3KX
C571 SC10U10V5ZY
AUD_AGND
AUD_AGND
VREFOUT2
ADAF2
ADAF1
VREFOUT1
CODECVREF
C572 SCD1U
C573 SC1000P50V2KX
C576 SC1000P50V2KX
C577 SC1000P50V2KX
C578 SC1U10V3KX
C579 SCD1U
C580 SC10U10V5ZY
5V_AUDIO_S0
3D3V_S0
C574 SCD1U
C575 SCD1U
C581 SCD1U
C582 SCD1U
C583 SCD1U
DY
DY
DY
AUD_AGND
U33
AFILT1
AFILT2
VRDA
VRAD
VREF
VREFOUT
FRONT-MIC
NC#33
NC#40
AVDD
AVDD
VDD
VDD
AUX-L
AUX-R
JD2
JD1/GPIO1
SURR-OUT-L
SURR-OUT-R
LINE-L
LINE-R
FRONT-OUT-L
FRONT-OUT-R
MIC1
MIC2
CD-L
CD-R
CD-GND
MONO-OUT-R
CEN-OUT
LFE-OUT
PC-BEEP
PHONE
AGND
AGND
GND
GND
ALC655-U
XTL-IN
XTL-OUT
SPDIFO
SPDIFI/EAPD
SDIN
SDOUT
JD0/GPIO0
XTLSEL
BITCLK
SYNC
RESET#
R383 0R2-0
CLK14_AUDIO 3
C584 SC22P50V2JN-1
X1 24D576MHZ-13
C585 SC22P50V2JN-1
DY
DY
DY
XTALIN_CODEC
XTALOUT_CODEC
SPDIF_OUT
R384 0R3-U
SPDIF 33,57
EAPD 33
DY
C332
DUMMY-C2
AC97_DATIN
R385 22R3
R386 0R2-0
AC97_DIN0 21
AC97_DOUT 21,22,24
XTSEL HI: USE 24.576M XTAL
XTSEL LOW: USE 14.318M CLK FROM CLK GEN
AC97_CBITCLK
R387 33R3
R388 10KR2
BITCLK_BUFF
DY
AC97_SYNC 21,24
AC97_RST# 21,24
33 AUD_LINL
33 AUD_LINR
C587 SC1U10V3KX
C586 SC1U10V3KX
AUDLINL
AUDLINR
33 AUD_LOL
33 AUD_LOR
C588 SC1000P50V2KX
C589 SC1000P50V2KX
AUD_AGND
AUD_AGND
33 AUD_MICIN
C590 SC1U10V3ZY
AUD_MICIN1
25 CD_AUDL
25 CD_AGND
25 CD_AUDR
R389 75R3F
R390 GAP-CLOSE-PWR
R395 75R3F
CDAUDL
CDAGND
CDAUDR
C591 SC1U10V3KX
C592 SC1U10V3KX
C594 SC1U10V3KX
CDAUD_L
CDAUD_GND
CDAUD_R
R392 100KR2
R393 100KR2
R394 100KR2
AUD_AGND
AUD_PC_BEEP
C593 SCD1U
AUD_BEEP
R391 4K7R2
AUD_SYS_BEEP
C595 SC2200P50V2KX
R396 22R3
AUD_AGND
AUD_AGND
AUD_SYS_BEEP
C596 SC4D7U10V5ZY
CB_SPKR 26
C597 SC4D7U10V5ZY
SPKR_SB 21
C598 SC4D7U10V5ZY
KBC_BEEP 34
G4 GAP-CLOSE
G5 GAP-CLOSE
G6 GAP-CLOSE
G7 GAP-CLOSE
G8 GAP-CLOSE
G9 GAP-CLOSE
G10 GAP-CLOSE
G11 GAP-CLOSE
AUD_AGND
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO (1/2) -- CODEC ALC655
Size A3
Document Number
Bolsena
Rev SA
Date: Tuesday, December 28, 2004
Sheet 32 of 58

Internal Speaker

?ddck jack in high?low?

Dummy when no EZ4

Dummy when use EZ4

Dummy when no EZ4

By GMT suggest.
Change from
74.01421.01G
to 74.01421.A1G

Additional 12dB gain

LINE IN

MIC_JKIN = Hi after PLUG-IN

Dummy when no EZ4

LINE OUT

SE#_BTL= LOW after PLUG-IN

If R->L 避免 noise
1000P -> 100P

?spdif led on, delete ic?

80.10715.591

Audio VREF Generator

Microphone External Preamp

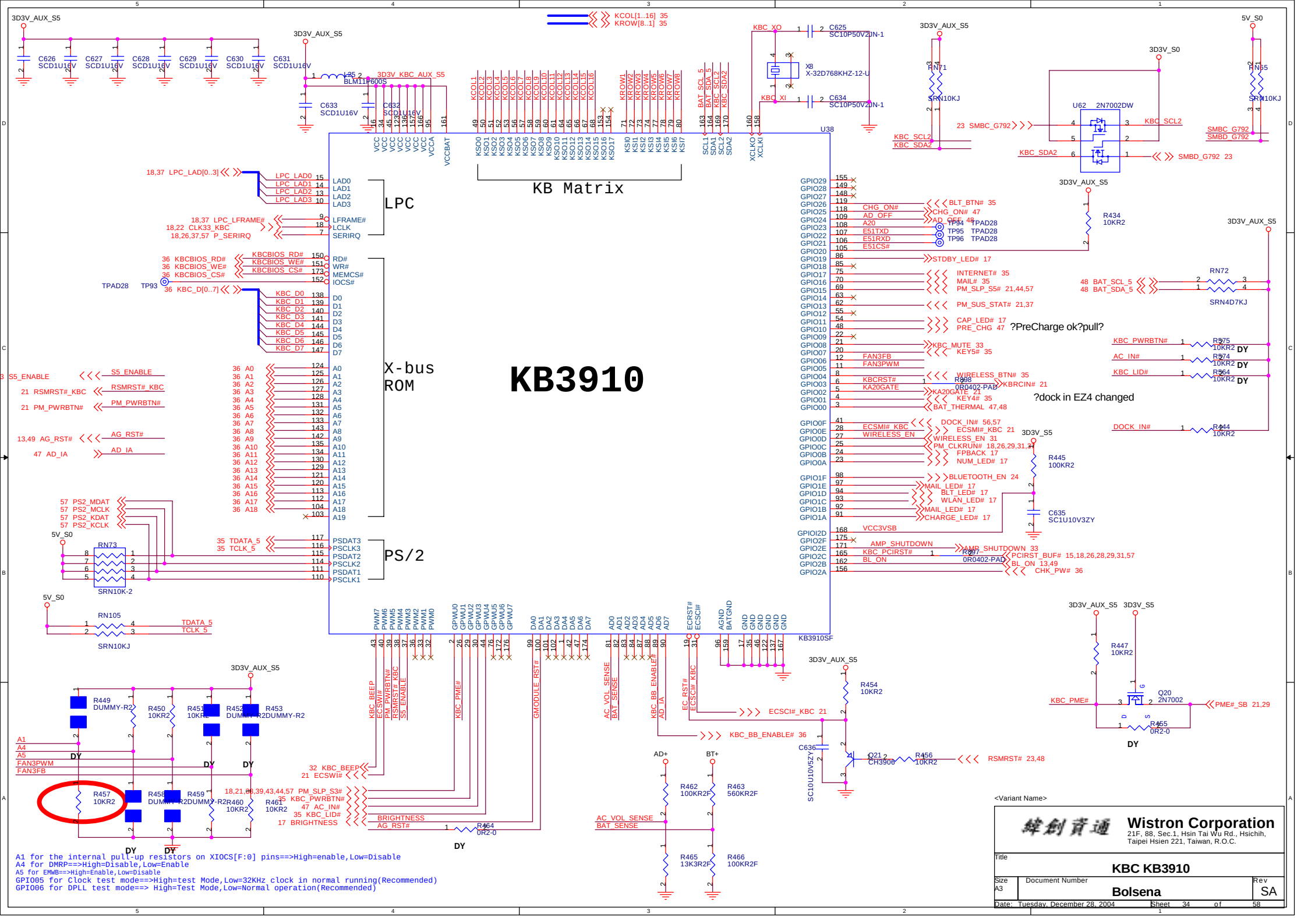
Internal Mic

LOW OFF

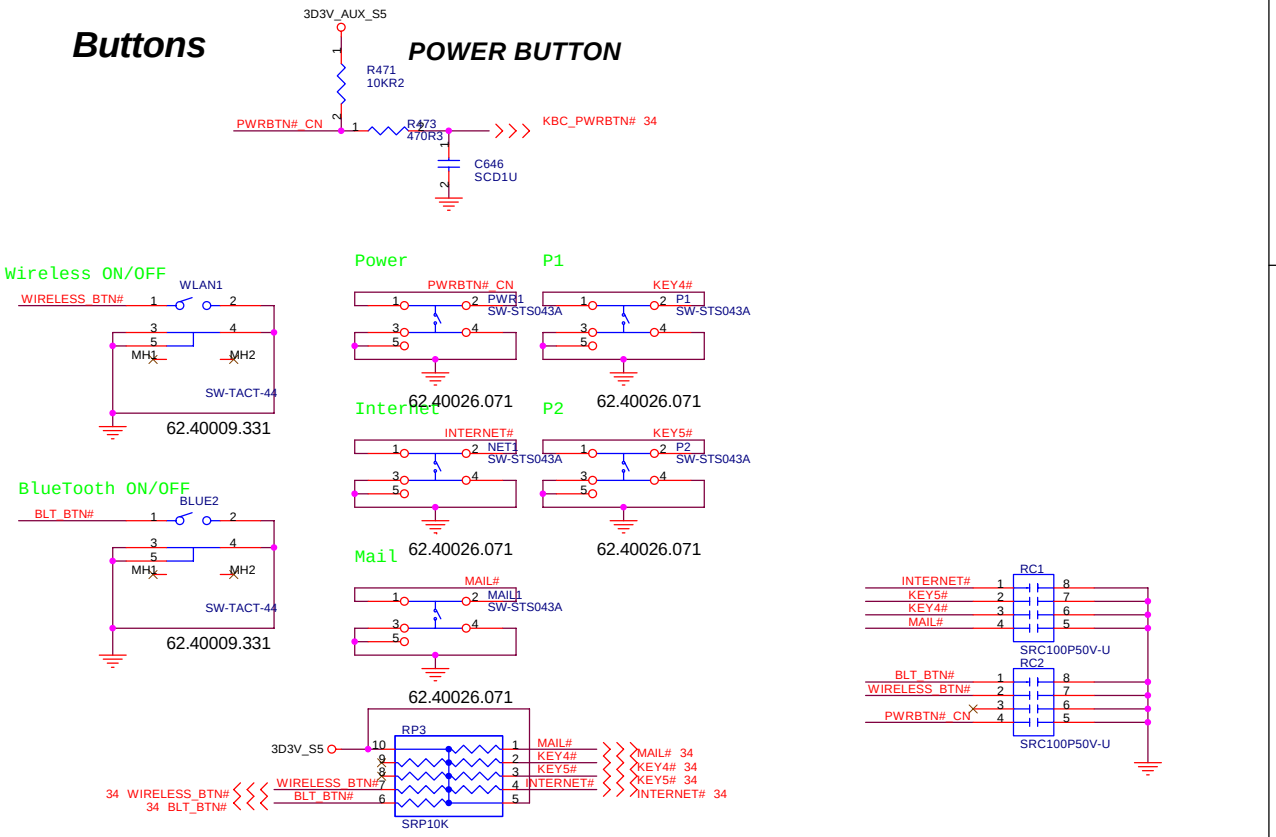
?which is gnd

20.D0012.102

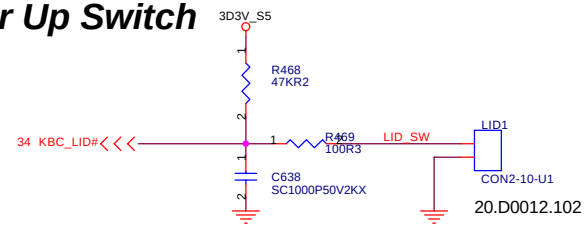
Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO (2/2)		
Size: Custom	Document Number: Bolsena	Rev: SA
Date: Tuesday, December 28, 2004	Sheet 33 of 58	


KB3910
KB Matrix
LPC
X-bus ROM
PS/2
U38
KB3910SF
?PreCharge ok?pull?
?dock in EZ4 changed
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==> High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC KB3910
Bolsena
SA
Tuesday, December 28, 2004
34
58

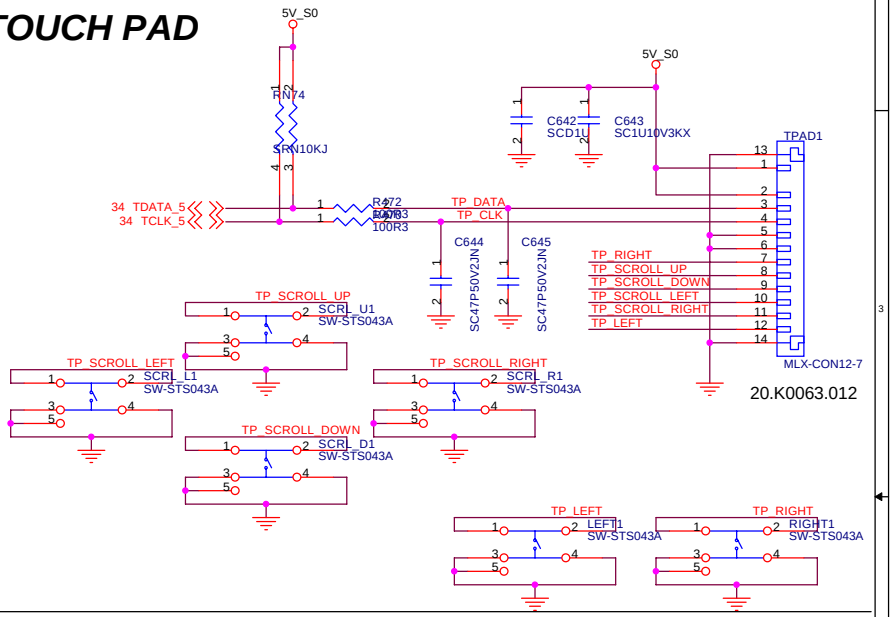
Buttons



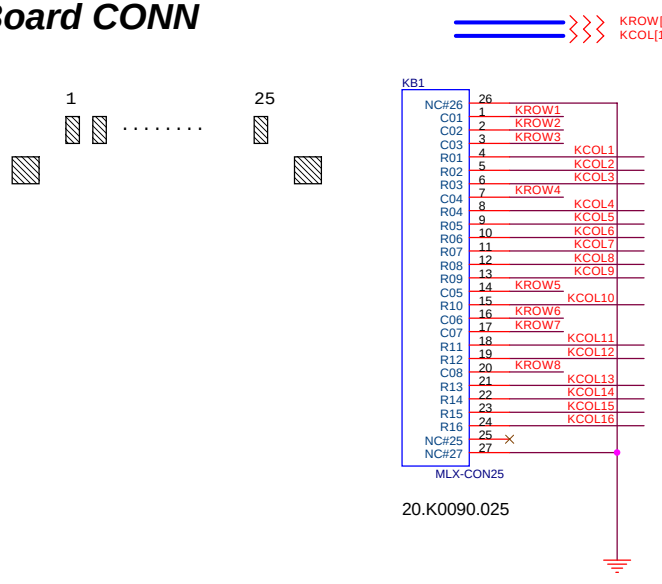
Cover Up Switch



TOUCH PAD

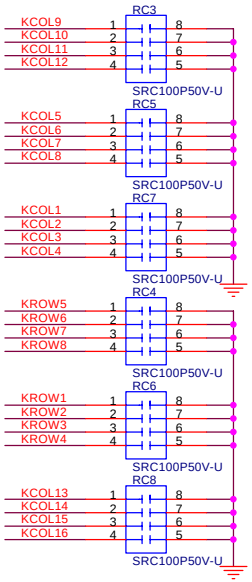


Internal KeyBoard CONN



Pin1 ==>*R01
Pin2 ==>*R02
Pin3 ==>*R03
Pin4 ==> C01
Pin5 ==> C02
Pin6 ==> C03
Pin7 ==>*R04
Pin8 ==> C04
Pin9 ==> C05
Pin10 ==> C06
Pin11 ==> C07
Pin12 ==> C08
Pin13 ==> C09
Pin14 ==>*R05
Pin15 ==> C10
Pin16 ==>*R06
Pin17 ==>*R07
Pin18 ==> C11
Pin19 ==> C12
Pin20 ==>*R08
Pin21 ==> C13
Pin22 ==> C14
Pin23 ==> C15
Pin24 ==> C16
Pin25 ==> NC

EMI Bypass cap.



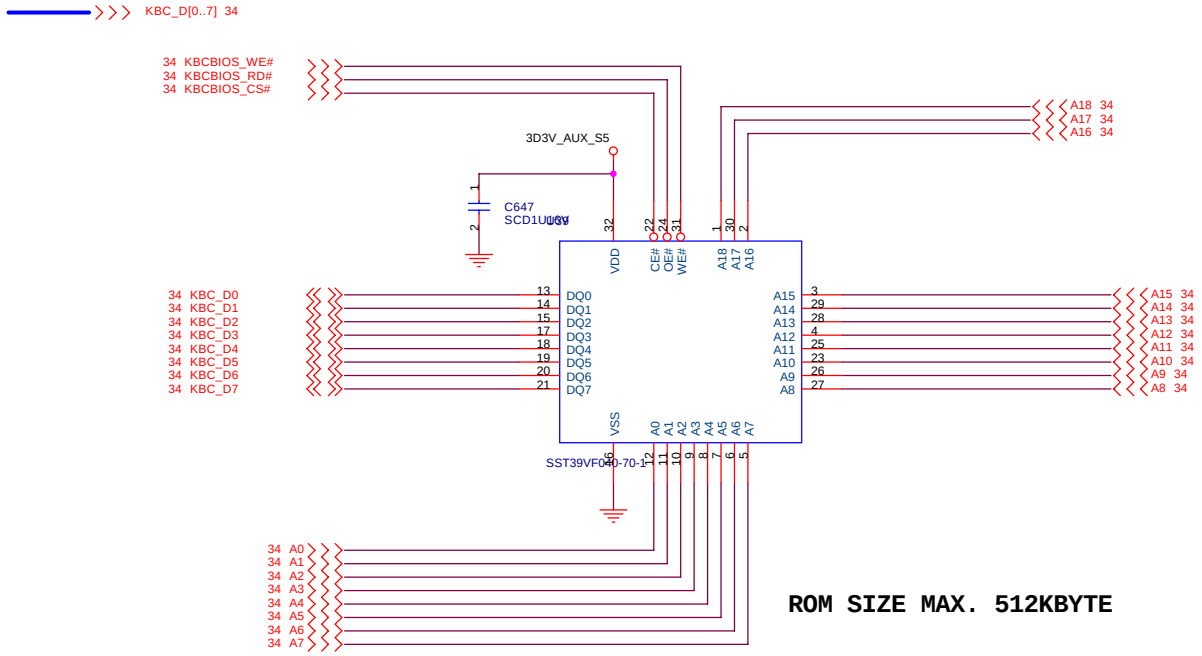
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BUTTONs / KB / TOUCHPAD**

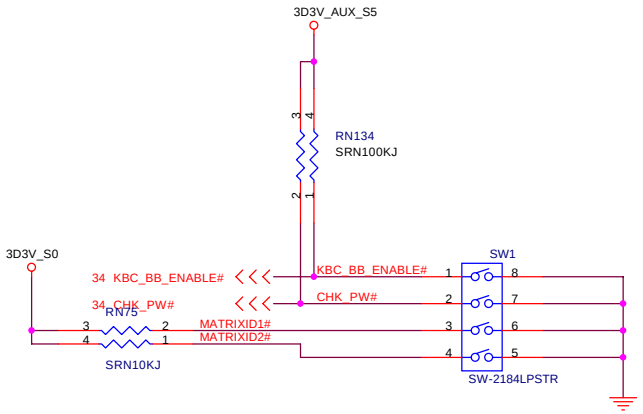
Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 35 of 58



ROM SIZE MAX. 512KBYTE

PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



Keyboard matrix (from vendor)

		US	Jap	Eur	Other
Low Bit	MATRIXID1#	1	1	0	0
High Bit	MATRIXID2#	1	0	1	0

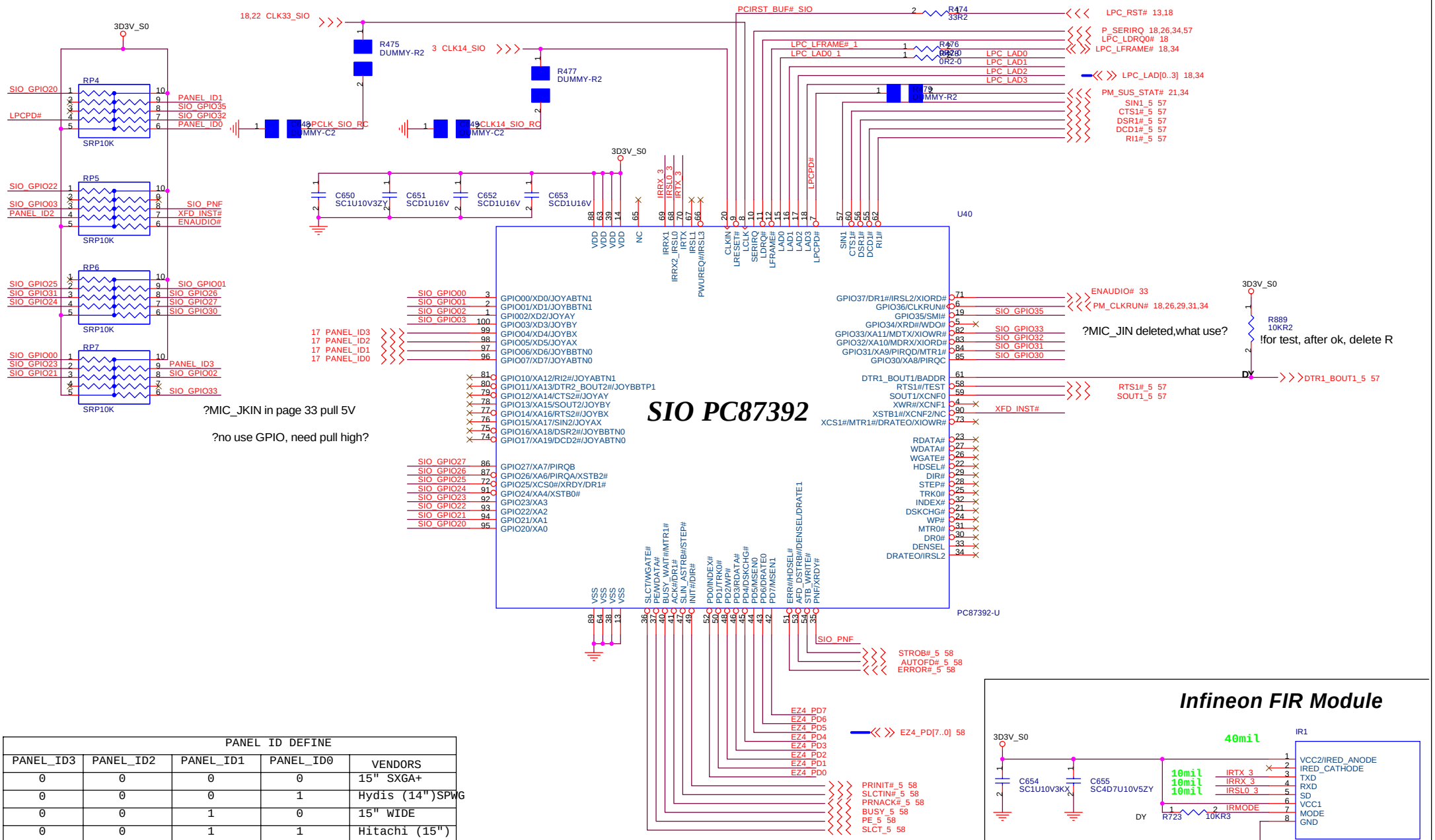
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS ROM**

Size: A3 | Document Number: **Bolsena** | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 36 of 58



PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel

Note : AU (友達),CMO(奇美),** : With Digitizer

<Variant Name>

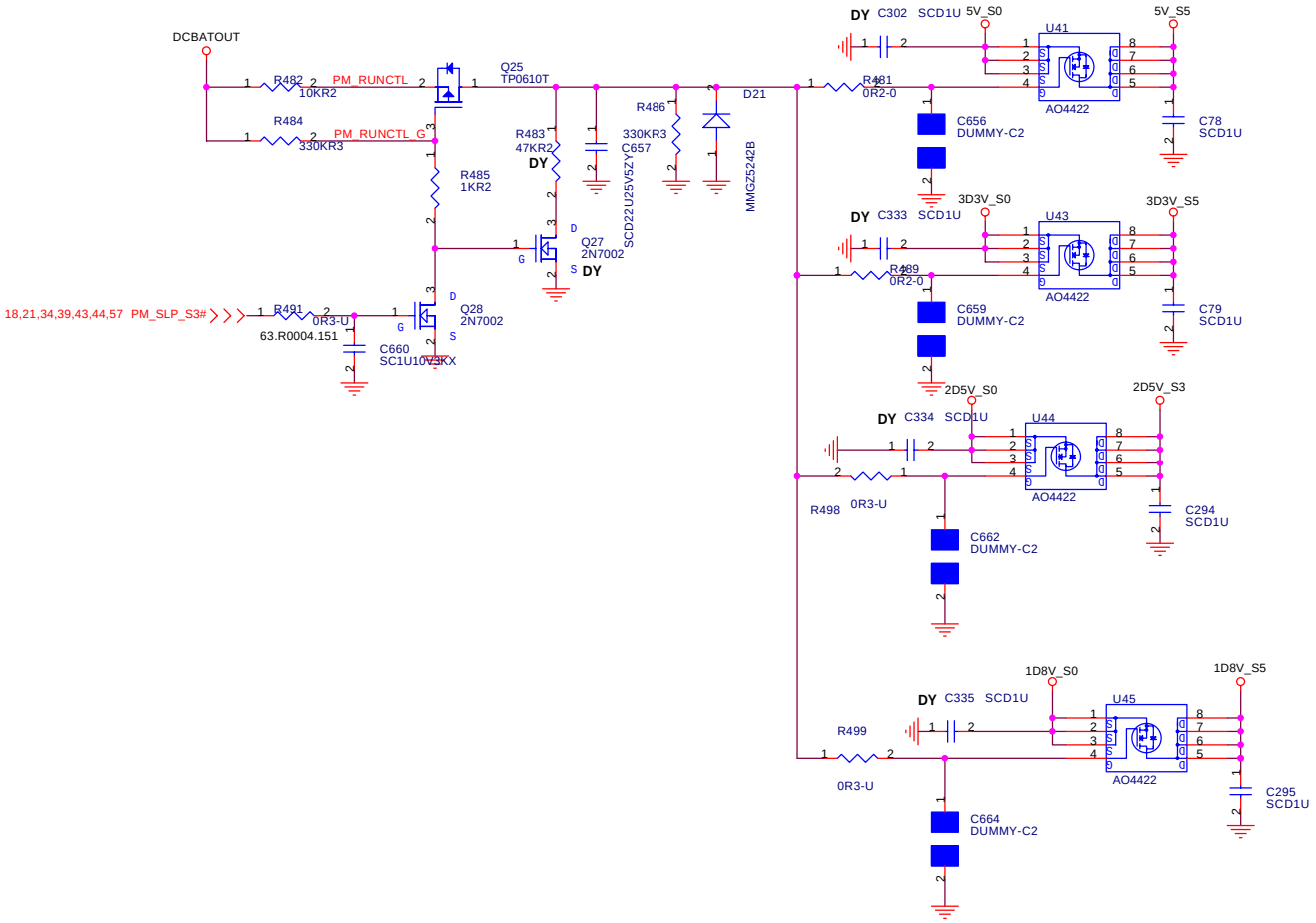
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SUPER IO NC87392

Size: A3 | Document Number: Bolsena | Rev: SA

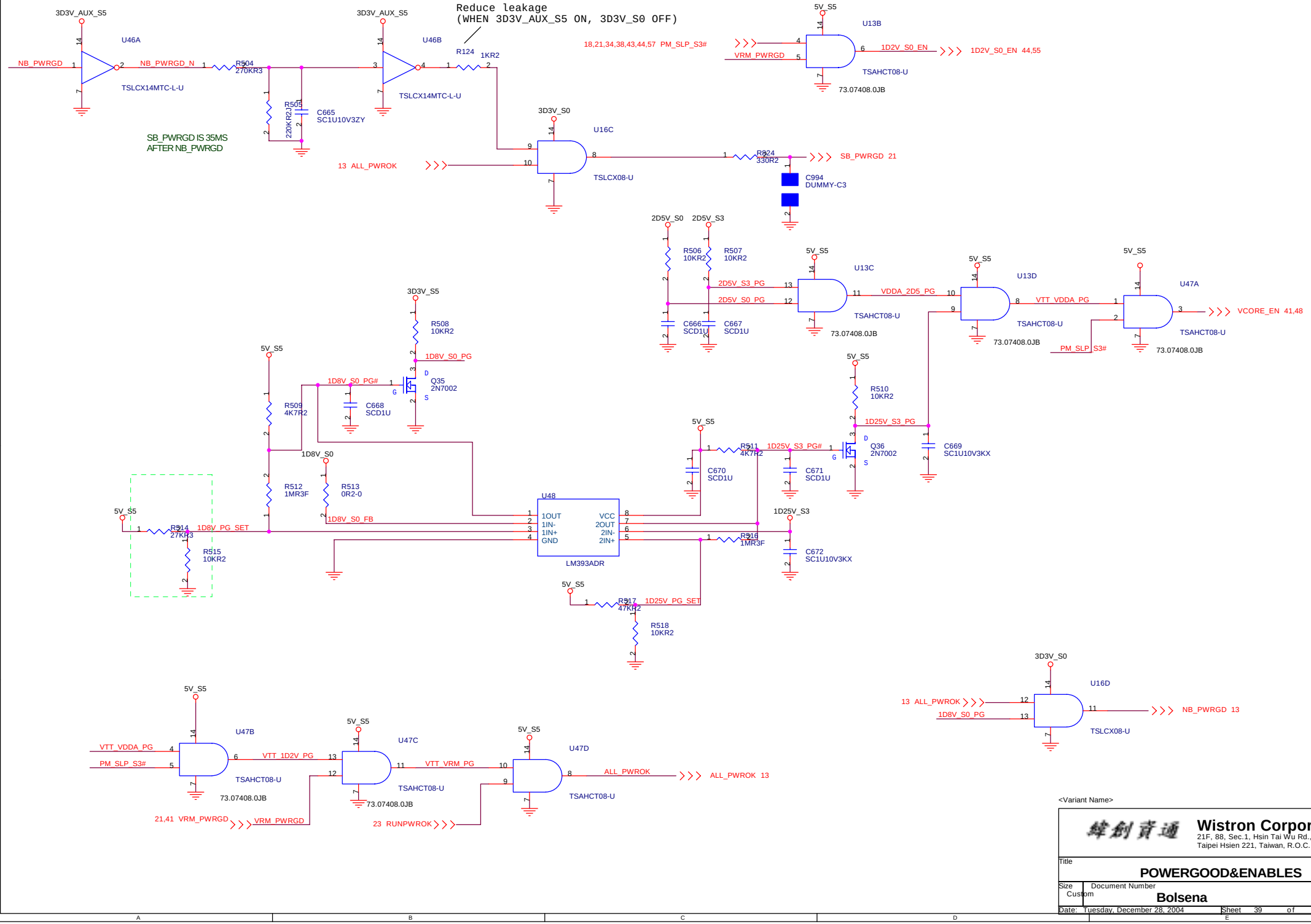
Date: Tuesday, December 28, 2004 | Sheet 37 of 58

Run Power



<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	PWR CTL LOGIC / PWR PLANE
Size A3	Document Number: Bolsena
Rev	SA
Date: Tuesday, December 28, 2004	Sheet 38 of 58



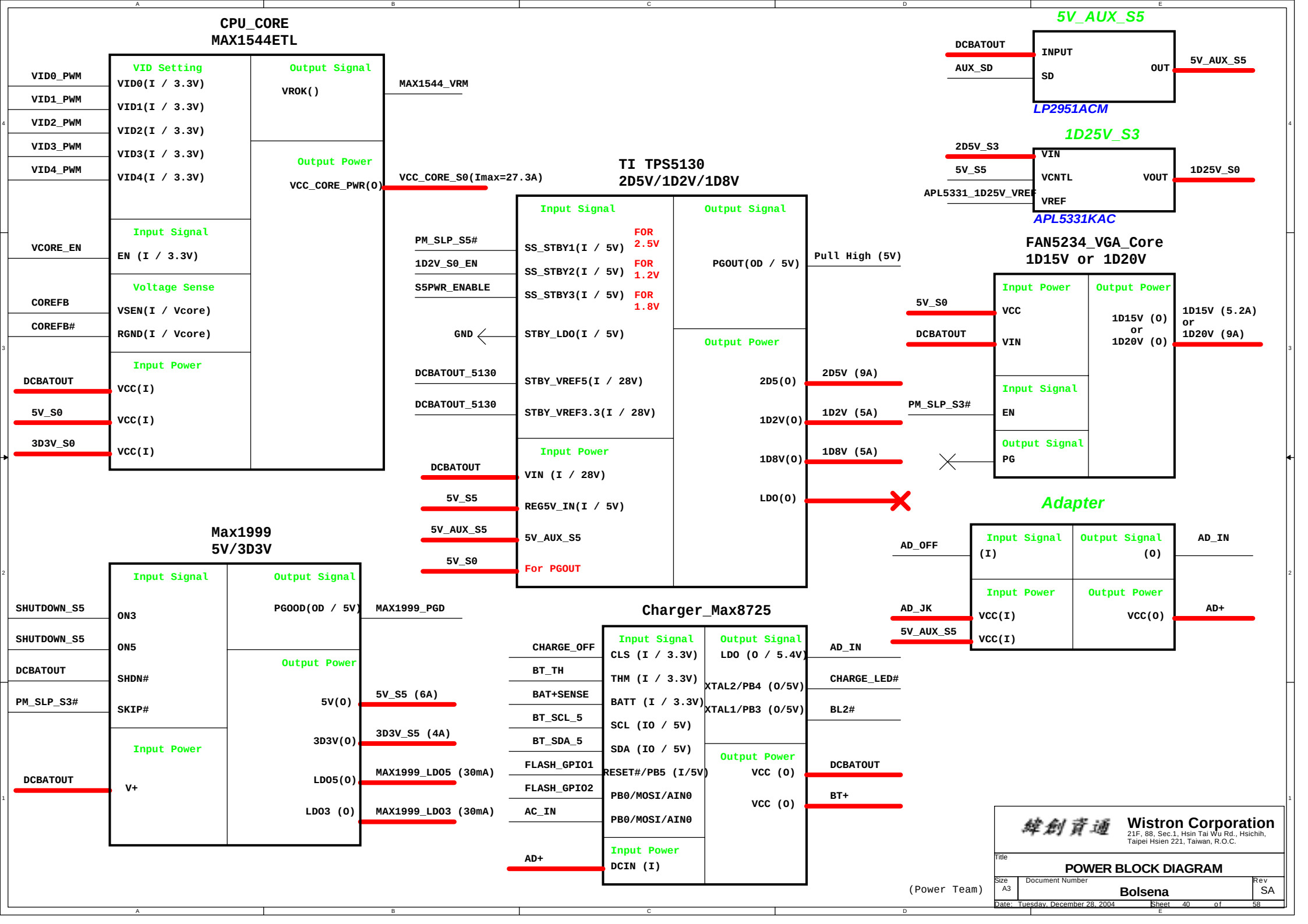
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWERGOOD&ENABLES**

Size: Custom | Document Number: **Bolsena** | Rev: SA

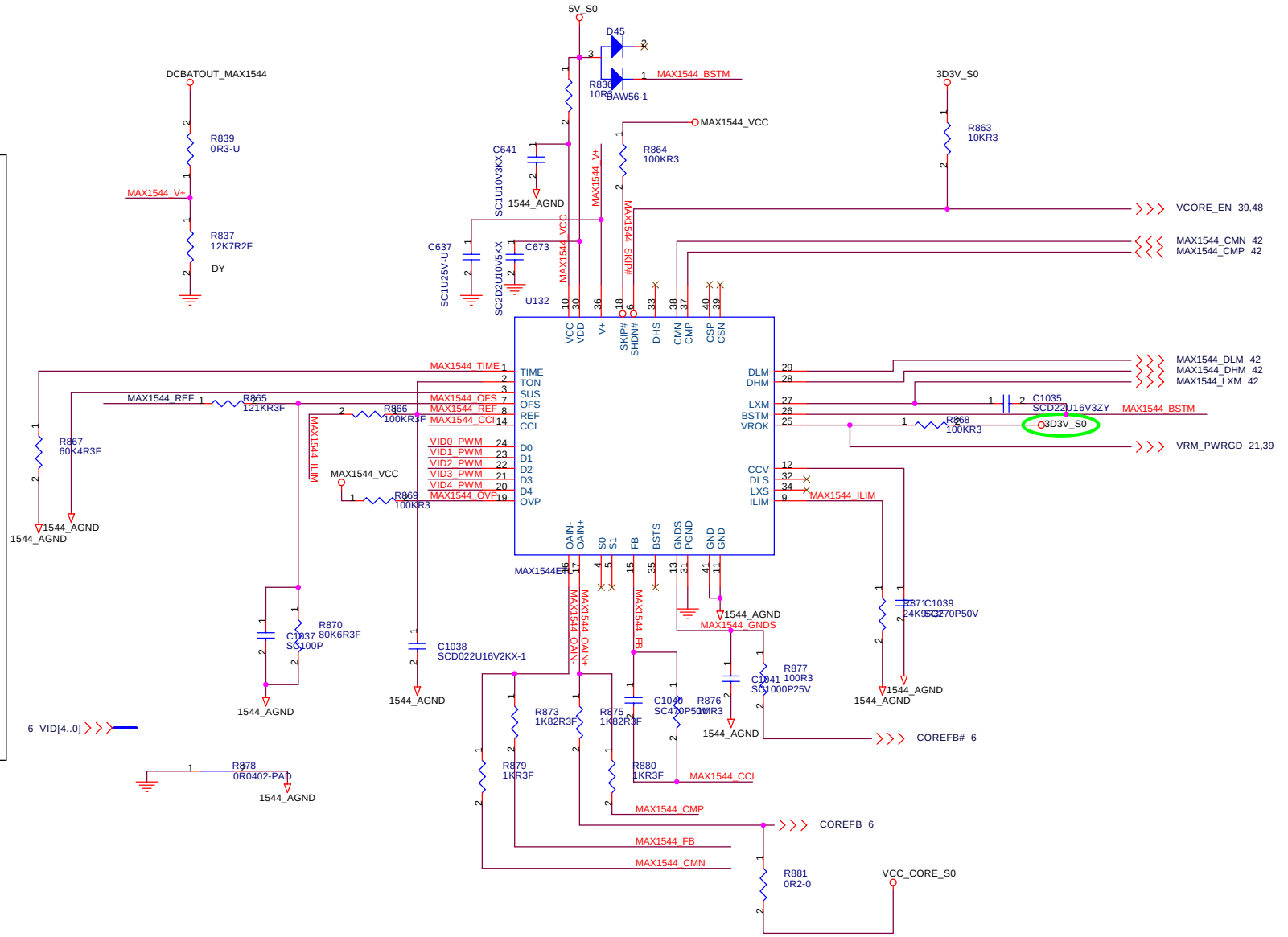
Date: Tuesday, December 28, 2004 | Sheet 39 of 58


CPU_CORE
MAX1544ETL
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Output Signal
VROK()
Output Power
VCC_CORE_PWR(O)
VID0_PWM
VID1_PWM
VID2_PWM
VID3_PWM
VID4_PWM
MAX1544_VRM
VCC_CORE_S0(Imax=27.3A)
Input Signal
EN (I / 3.3V)
VCORE_EN
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
COREFB
COREFB#
Input Power
VCC(I)
VCC(I)
VCC(I)
DCBATOUT
5V_S0
3D3V_S0
TI TPS5130
2D5V/1D2V/1D8V
Input Signal
SS_STBY1(I / 5V) FOR 2.5V
SS_STBY2(I / 5V) FOR 1.2V
SS_STBY3(I / 5V) FOR 1.8V
STBY_LDO(I / 5V)
STBY_VREF5(I / 28V)
STBY_VREF3.3(I / 28V)
Input Power
VIN (I / 28V)
REG5V_IN(I / 5V)
5V_AUX_S5
For PGOUT
Output Signal
PGOUT(OD / 5V)
Output Power
2D5(O)
1D2V(O)
1D8V(O)
LDO(O)
PM_SLP_S5#
1D2V_S0_EN
S5PWR_ENABLE
GND
DCBATOUT_5130
DCBATOUT_5130
DCBATOUT
5V_S5
5V_AUX_S5
5V_S0
Pull High (5V)
2D5V (9A)
1D2V (5A)
1D8V (5A)
5V_AUX_S5
INPUT
SD
OUT
DCBATOUT
AUX_SD
5V_AUX_S5
LP2951ACM
1D25V_S3
VIN
VCNTL
VREF
VOUT
2D5V_S3
5V_S5
APL5331_1D25V_VREF
1D25V_S0
APL5331KAC
FAN5234_VGA_Core
1D15V or 1D20V
Input Power
VCC
VIN
Input Signal
EN
Output Signal
PG
Output Power
1D15V (O)
or
1D20V (O)
5V_S0
DCBATOUT
PM_SLP_S3#
1D15V (5.2A)
or
1D20V (9A)
Adapter
Input Signal
(I)
Output Signal
(O)
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN
AD+
Max1999
5V/3D3V
Input Signal
ON3
ON5
SHDN#
SKIP#
Input Power
V+
Output Signal
PGOOD(OD / 5V)
Output Power
5V(O)
3D3V(O)
LDO5(O)
LDO3 (O)
SHUTDOWN_S5
SHUTDOWN_S5
DCBATOUT
PM_SLP_S3#
DCBATOUT
MAX1999_PGD
5V_S5 (6A)
3D3V_S5 (4A)
MAX1999_LDO5 (30mA)
MAX1999_LDO3 (30mA)
Charger_Max8725
Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0
Input Power
DCIN (I)
Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)
Output Power
VCC (O)
VCC (O)
CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN
AD+
AD_IN
CHARGE_LED#
BL2#
DCBATOUT
BT+
(Power Team)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
POWER BLOCK DIAGRAM
Size
A3
Document Number
Bolsena
Rev
SA
Date: Tuesday, December 28, 2004
Sheet 40 of 58

CPU_VCORE
VID=1.20V
Iomax=27.3A (35W)

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown



VCC_CORE_S0 feedback

<Variant Name>

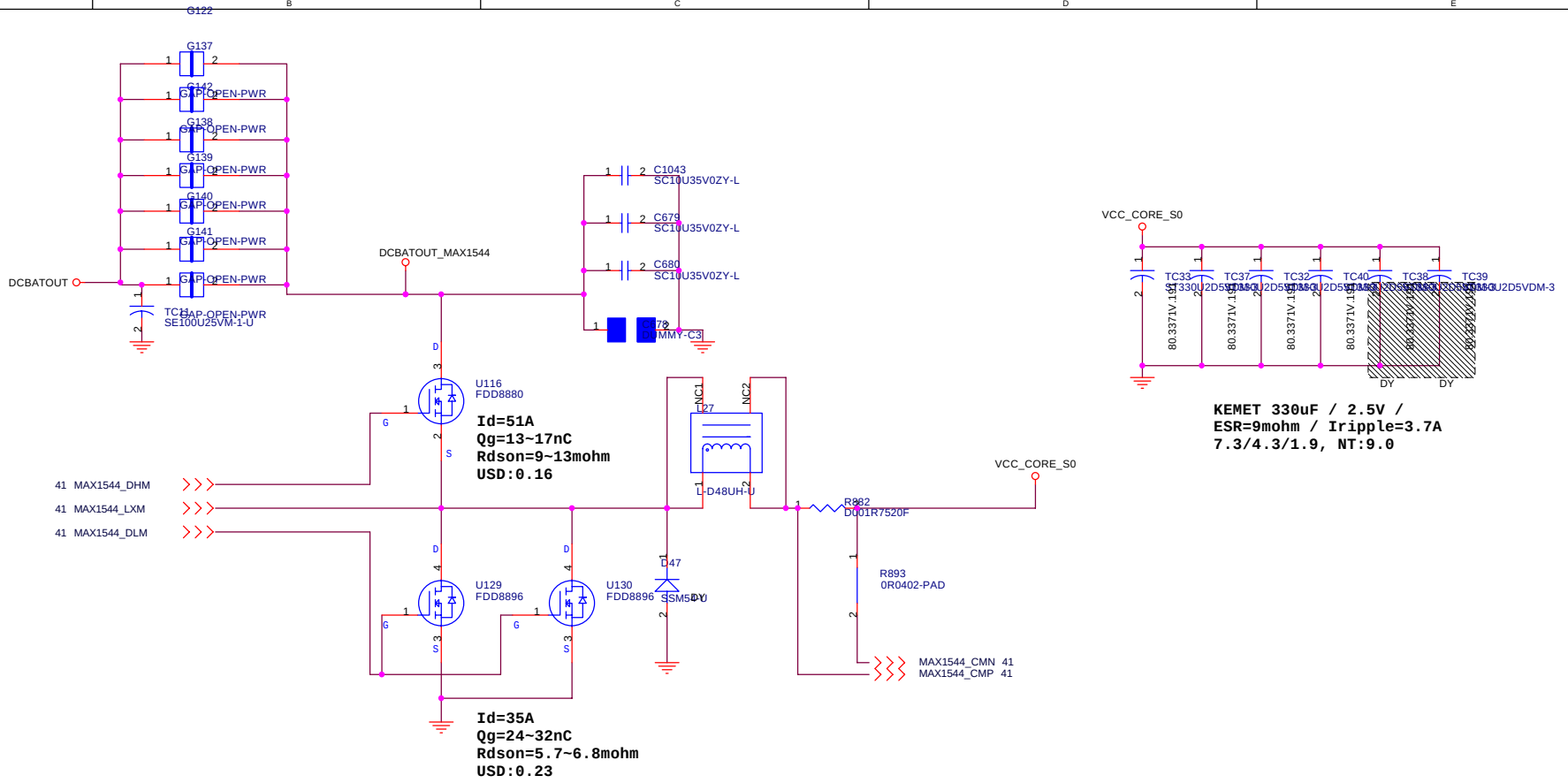
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore 1

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 41 of 58

(Power Team)



<Variant Name>

(Power Team)

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU Vcore 2**

Size: A3 | Document Number: **Bolsena** | Rev: SA

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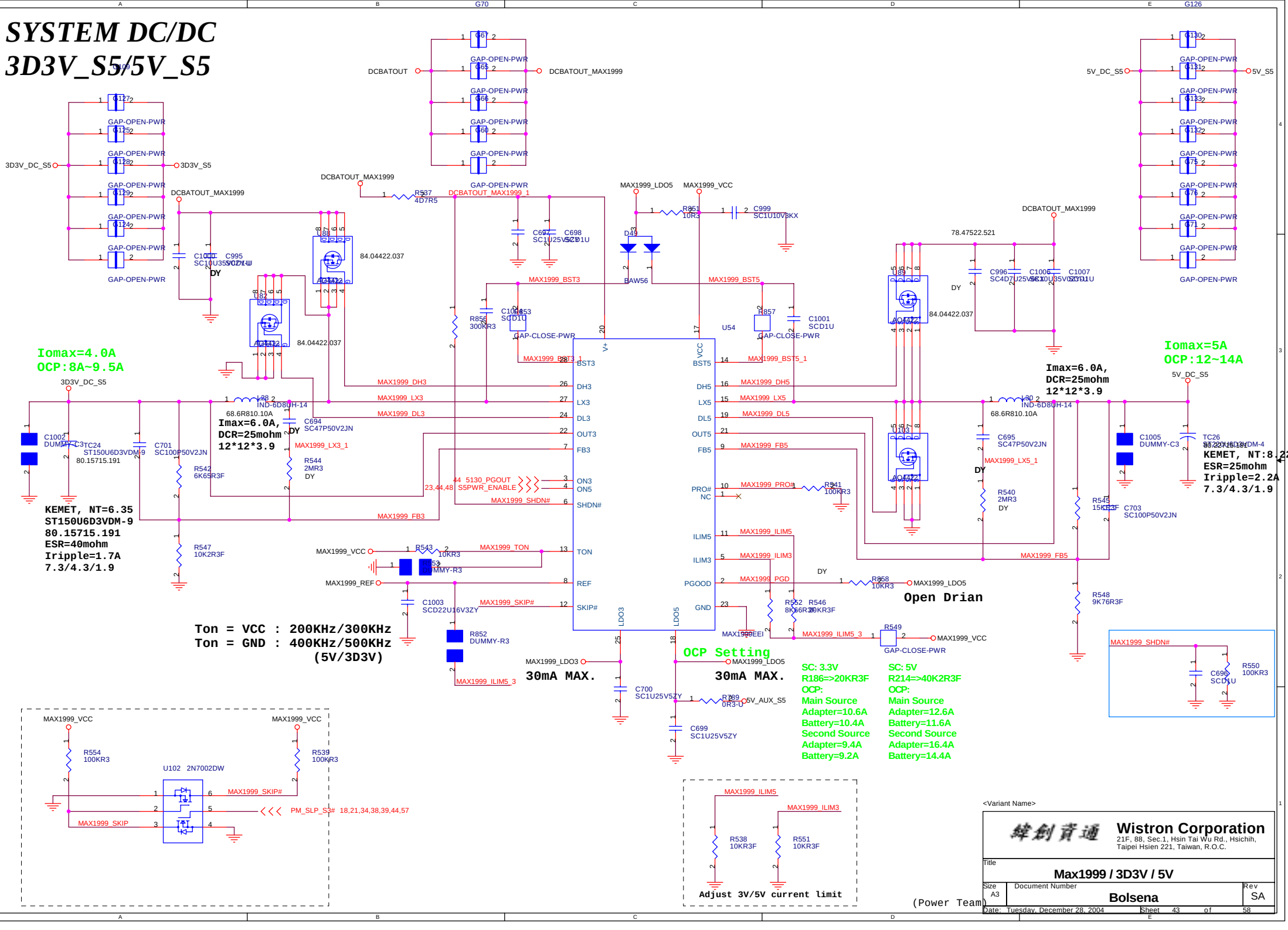
SYSTEM DC/DC
3D3V_S5/5V_S5



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: Max1999 / 3D3V / 5V

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 43 of 58

TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)

For 1.8V
SETTING=1.8275V

For 1.2V
SETTING=1.2172V

For 2.5V
SETTING=2.516V

close to IC

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

T(soft)=1.736ms

TPS5130

LDO SETTING

2D5V_OCP
OCP
12A=>R225=18K
18A=>R225=28K
close to IC

1D2V_OCP
OCP
8.4A=>R226=13K
10A=>R226=22K
close to IC

1D8V_OCP
OCP
8.4A=>R229=12.65K
10A=>R229=22K
close to IC

PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5130 1D2V/1D8V2D5V/ (1/2)**

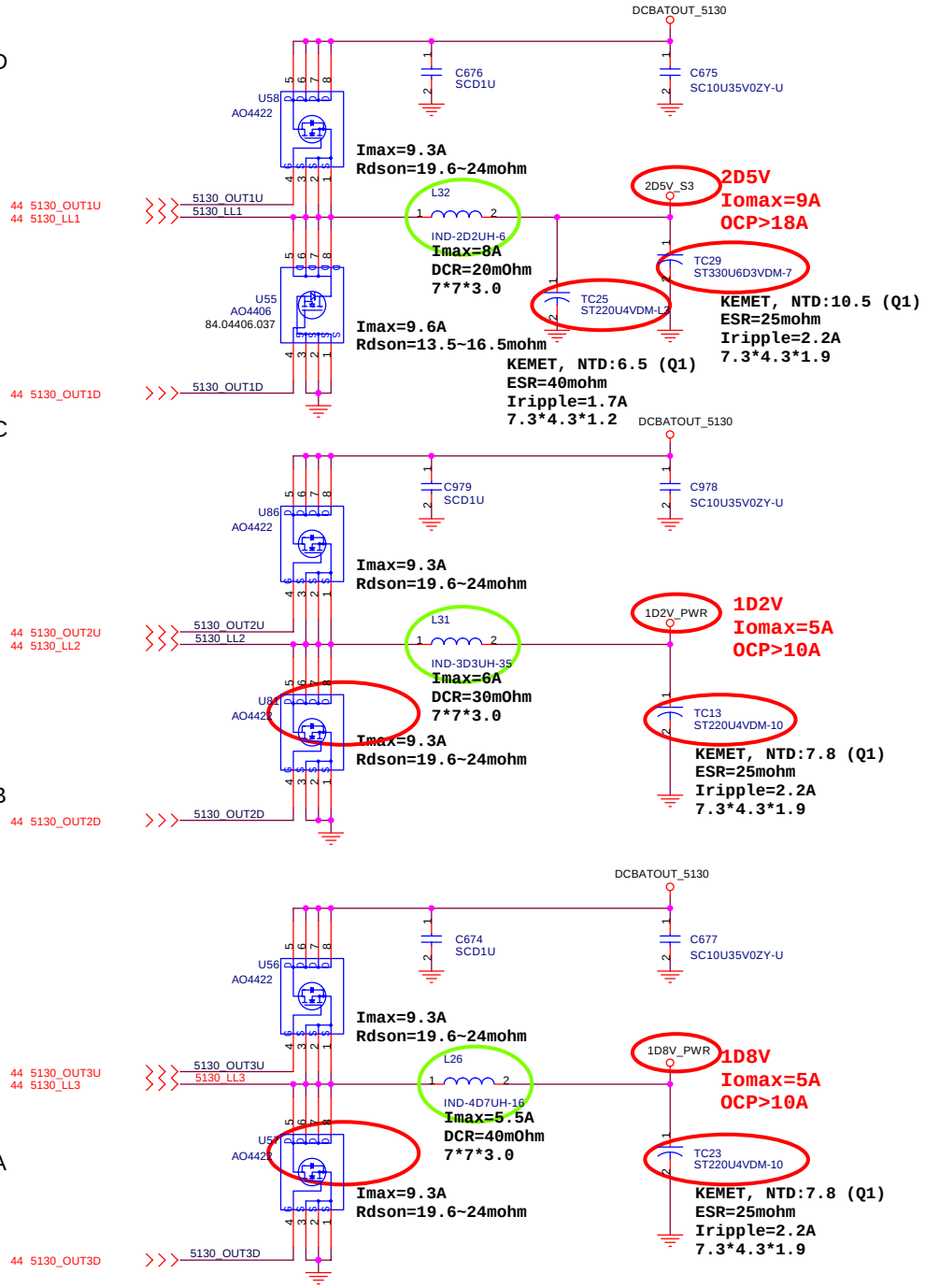
Size: A3 | Document Number: **Bolsena** | Rev: **SA**

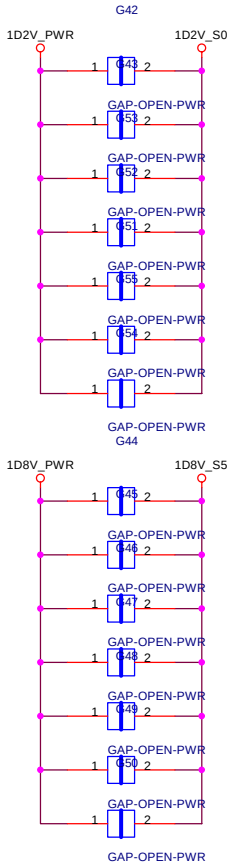
Date: Tuesday, December 28, 2004 | Sheet 44 of 58

(Power Team)

TI TPS5130 for 2D5V, 1D2V, 1D8V

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)





(Power Team)

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS5130 1D2V/1D8V2D5V/ (2/2)**

Size	Document Number	Rev
A3	**Bolsena**	SA

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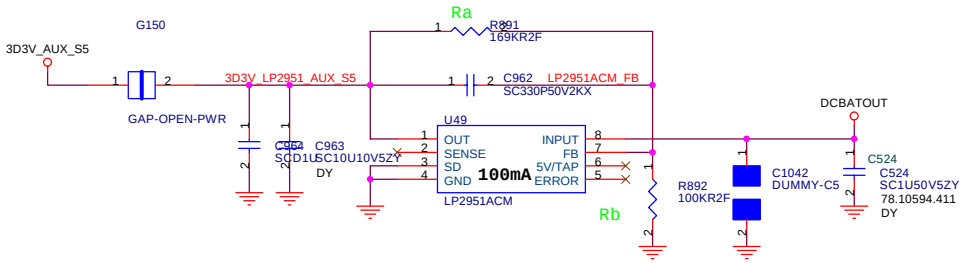
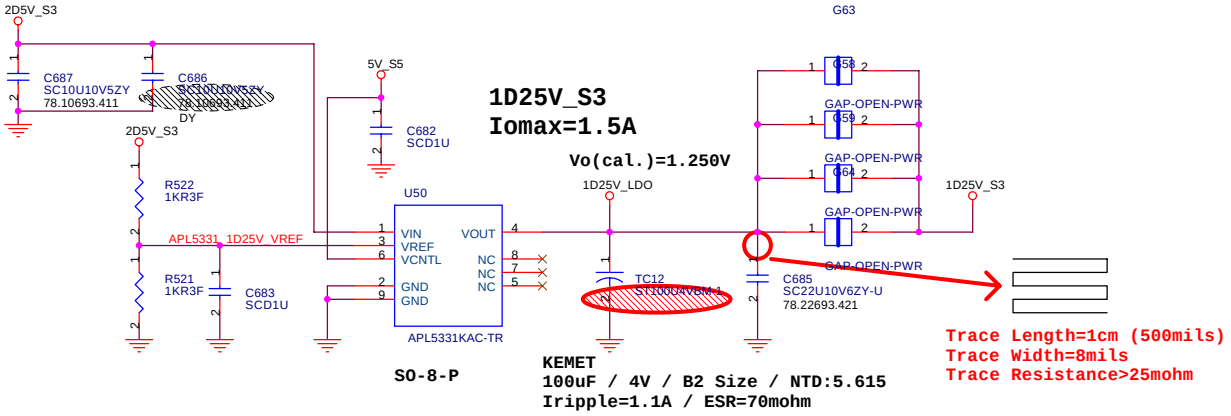
3D3V_AUX_S5



Vout = 1.23 * (Ra / Rb)



SO-8-P

KEMET
100uF / 4V / B2 Size / NTD:5.615
Iripple=1.1A / ESR=70mohm

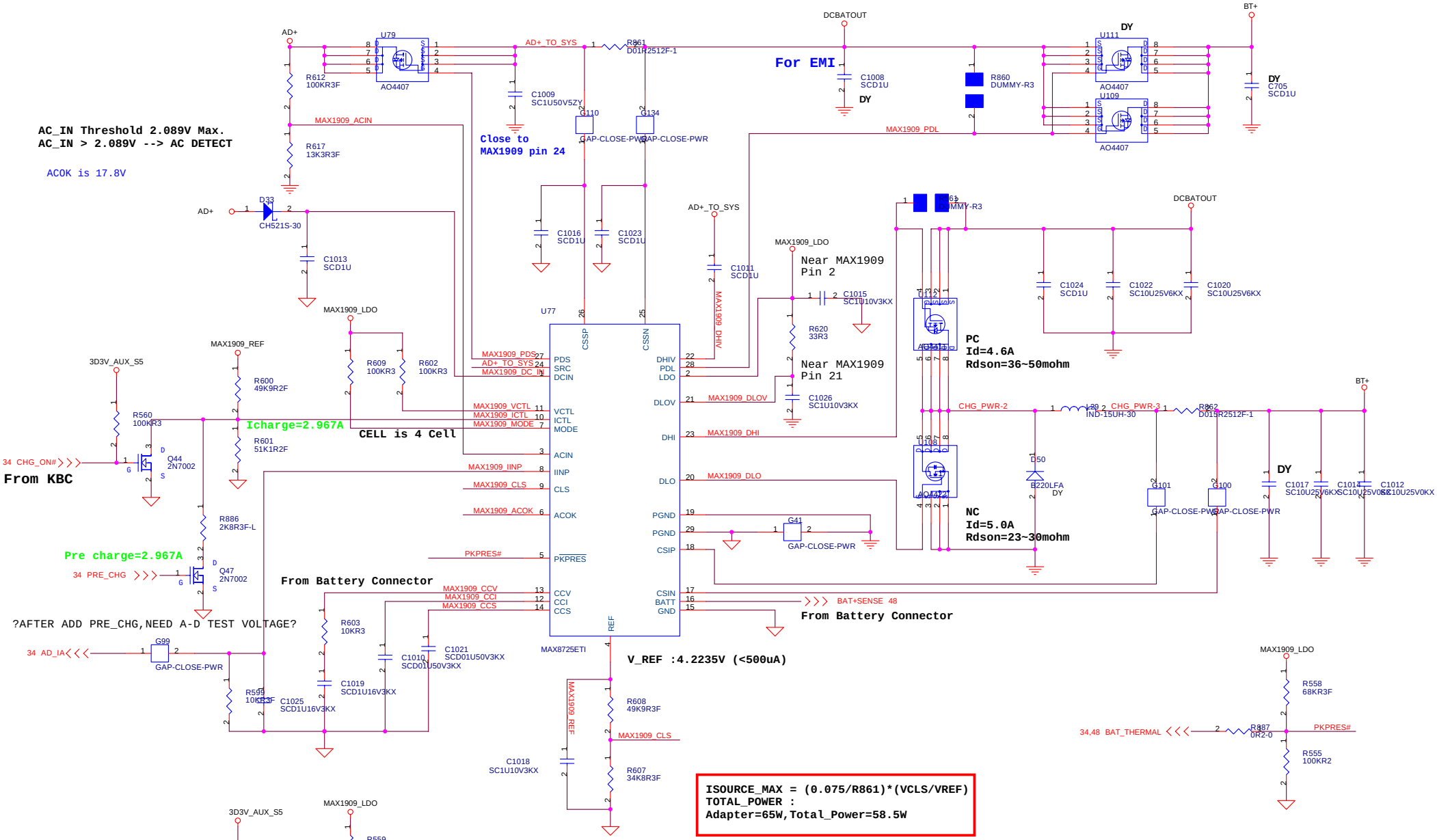
(Power Team)

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: 1D2V_S3 / 3D3V_AUX

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 46 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER MAX8725

Size: Custom | Document Number: Bolsena | Rev: SA

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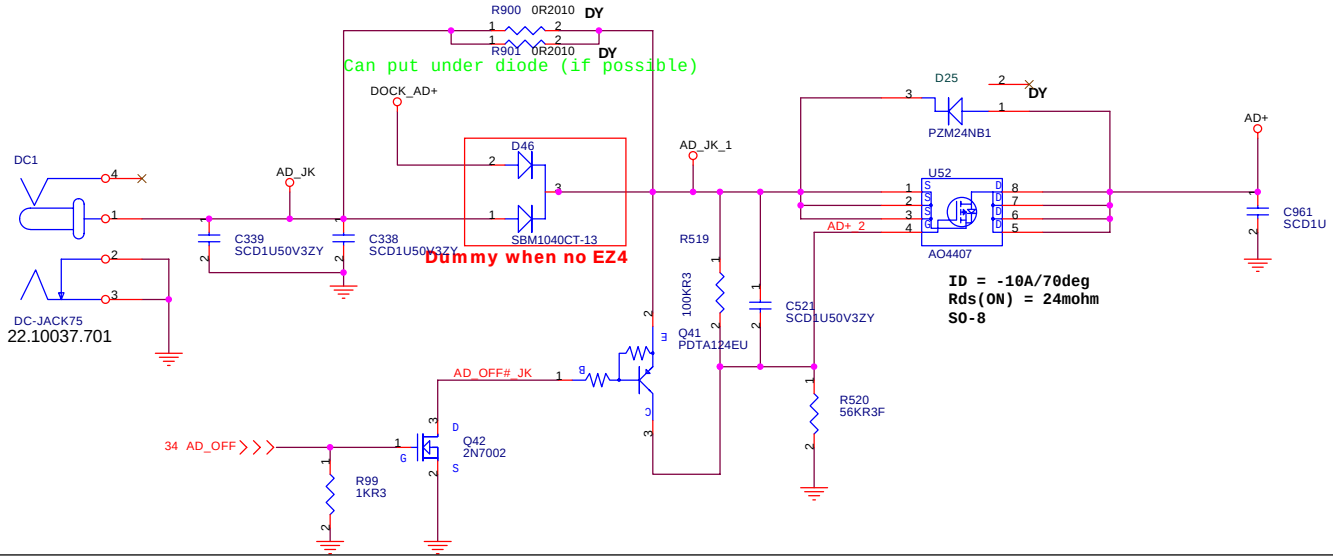
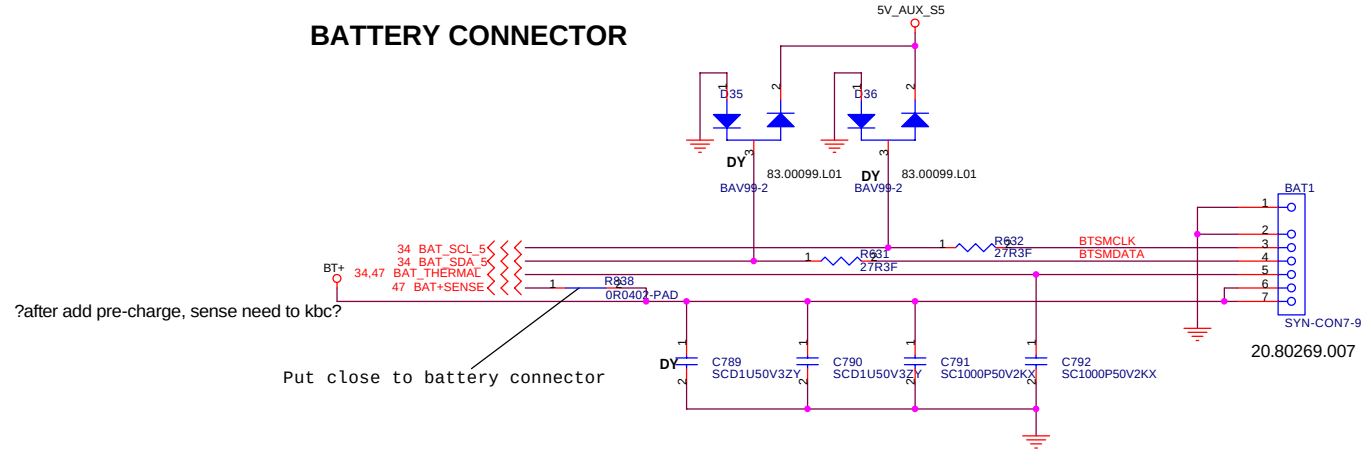
Adaptor in to generate DCBATOUT

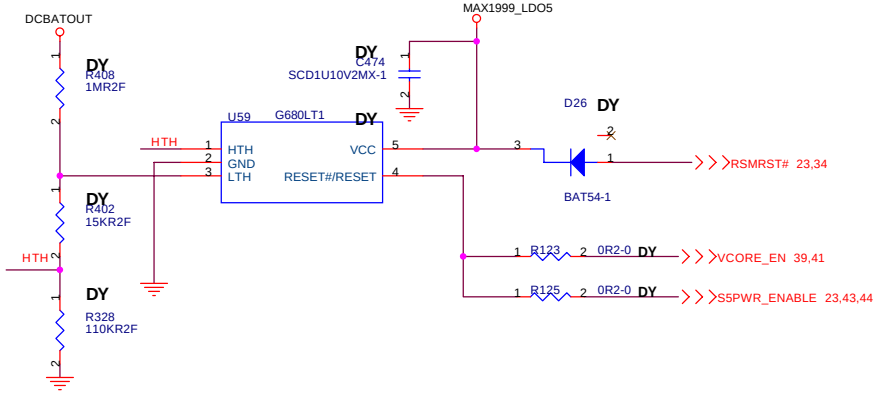


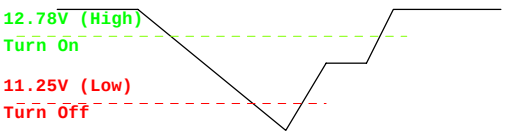
BATTERY CONNECTOR



Low3 Circuit :

L3# at 11.25V





<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	AD/BATT CONN
Size A3	Document Number Bolsena
Rev	SA
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Dummy when use UMA (WHOLE PAGE)

U90

P2779A-08ST
71.02779.00A
ORIGNAL
P2779A-08TT
USE W180-01
GEOMETRY

adjust SWING at 1.2v

U91A

Part 1 of 6

PCI EXPRESS

DVO / EXT TMDS / GPIO

LVDS

TMDS

DAC2

DAC1

CLK $S

THERM

M26-P-1

STRAPS	PIN	DEFAULT
CAL_BG_BACKUP	GPIO0	0
PLL_CAL_FORCE_EN	GPIO1	0
PCIE_MODE(1:0)	GPIO(3:2)	00
CAL_OFF	GPIO4	0
BYPASS_PLL	GPIO5	0
ICOMP	GPIO6	0
DEBUG_ACCESS	GPIO8	0
ROMIDCFG(3:0)	GPIO(9,13:11)	0000
MULTIFUNC(1:0)	LCDDATA(17:16)	00
VIP_DEVICE	LCDDATA(20)	0
DWNGR0	LCDDATA(21) (internal pull-down)	0

MUST TO CHECK

DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPDATA

DVPDATA_0, 1, 2
0 0 0 64MB Hynix
0 0 1 64MB Samsung
0 1 0 64MB X brand
0 1 1 64MB Y brand
1 0 0 128MB Hynix
1 0 1 128MB Samsung
1 1 0 128MB X brand
1 1 1 128MB Y brand

ATI Ref. Datasheets(page 3-32)
DOC.NO.:CHS-216M24-03
GPIO[0..13] are internal pull-down.

M24/M26 POWER PLAY (GPIO_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)

The PERSTB must deplay 4ms from M24 bug.

Place them near to chip

Place Near To EZPORT4

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M26 PCIE LVDS (1/3)

Size: A3 | Document Number: Bolsena | Rev: SA

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Dummy when use UMA (WHOLE PAGE)

M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V

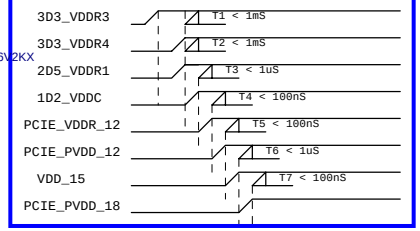
U91D — Part 4 of 6 — M26-P-1

I/O POWER

DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON

DIODE SUPPLIES POWER TO VDDC RAIL WHILE VDDC REGULATOR STABALIZES DURING POWER ON

M22 Power UP Squence



ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED PLACED CLOSE TO THE POWER/GND PINS WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI M26 POWER (2/3)

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 50 of 58

Dummy when use UMA (WHOLE PAGE)

MEMORY CHANNEL A

MEMORY CHANNEL B

M22,24,26P :Not connected

When use M22/24P

PIN	C6	C7
1.8V =	PD	PU
2.5V =	PU	PD

As close to CHIP as possible

When select M24 use 45ohm 1%
When select M26 use 240ohm 1%

When use M26P, pls remove this.

MVDDQ= 1.8v/ 2.5v

VDDR1	MEMVMODE_0	MEMVMODE_1
1.8V	GND	+VDDC_CT
2.5V	+VDDC_CT	GND
2.8V	+VDDC_CT	+VDDC_CT

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

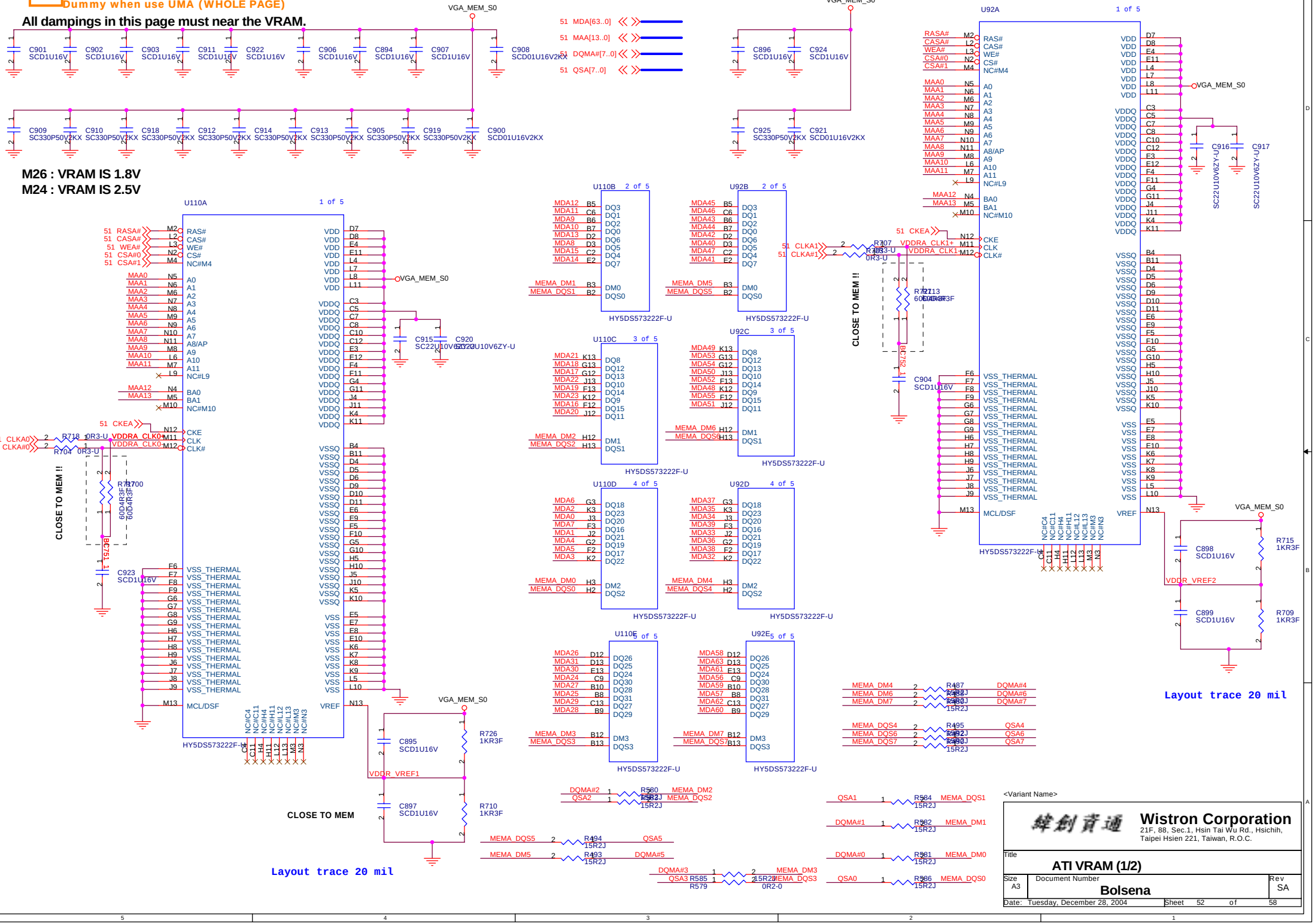
Title: ATI M26 MEM (3/3)

Size: A3 | Document Number: Bolsena | Rev: SA

Date: Tuesday, December 28, 2004 | Sheet 51 of 58

Dummy when use UMA (WHOLE PAGE)

All dampings in this page must near the VRAM.



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATI VRAM (1/2)

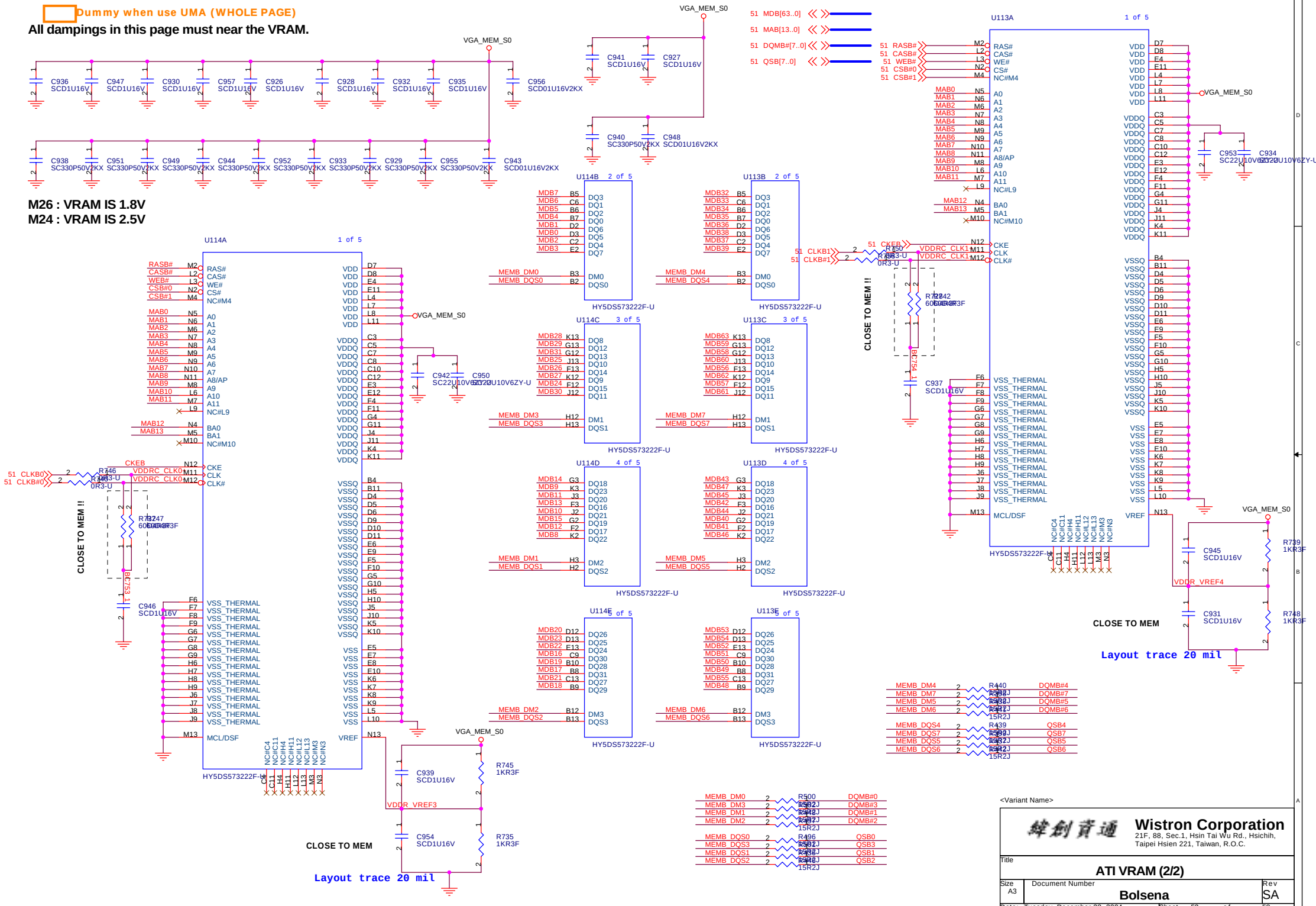
Size	Document Number	Rev
A3	Bolsena	SA

Date: Tuesday, December 28, 2004 Sheet 52 of 58

Dummy when use UMA (WHOLE PAGE)

All dampings in this page must near the VRAM.

M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V



<Variant Name>

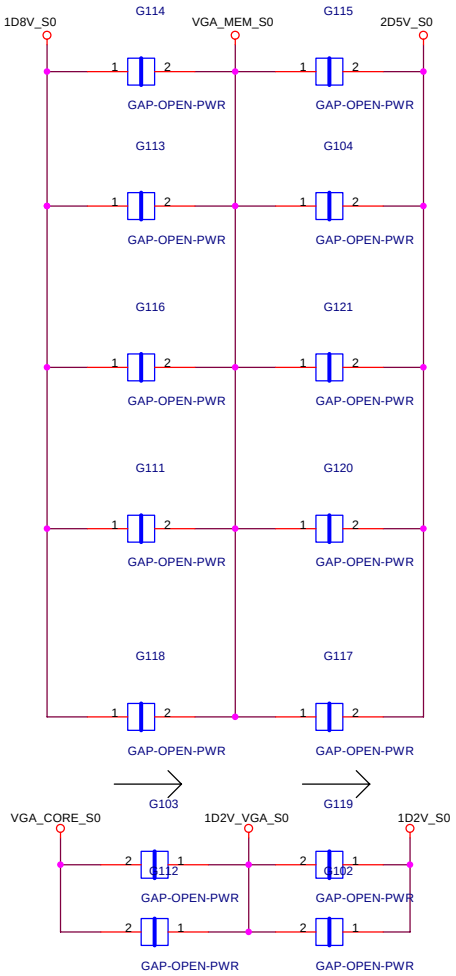
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

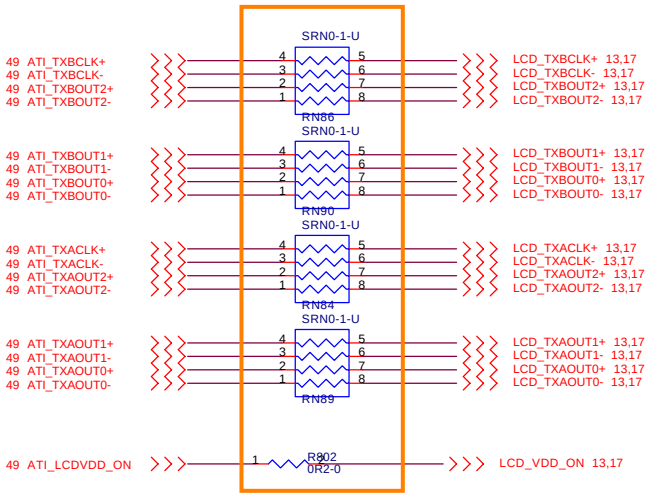
Title: **ATI VRAM (2/2)**

Size	Document Number	Rev
A3	Bolsena	SA

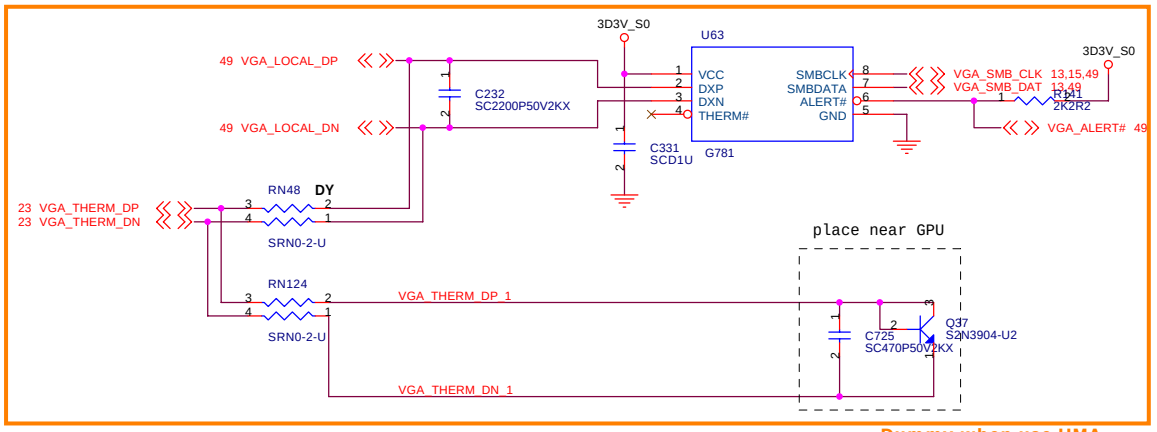
Date: Tuesday, December 28, 2004 Sheet 53 of 58

M26 : VRAM IS 1.8V
M24 : VRAM IS 2.5V ONLY 1.8 'OR' 2.5 SHORT





Dummy when use UMA



Dummy when use UMA

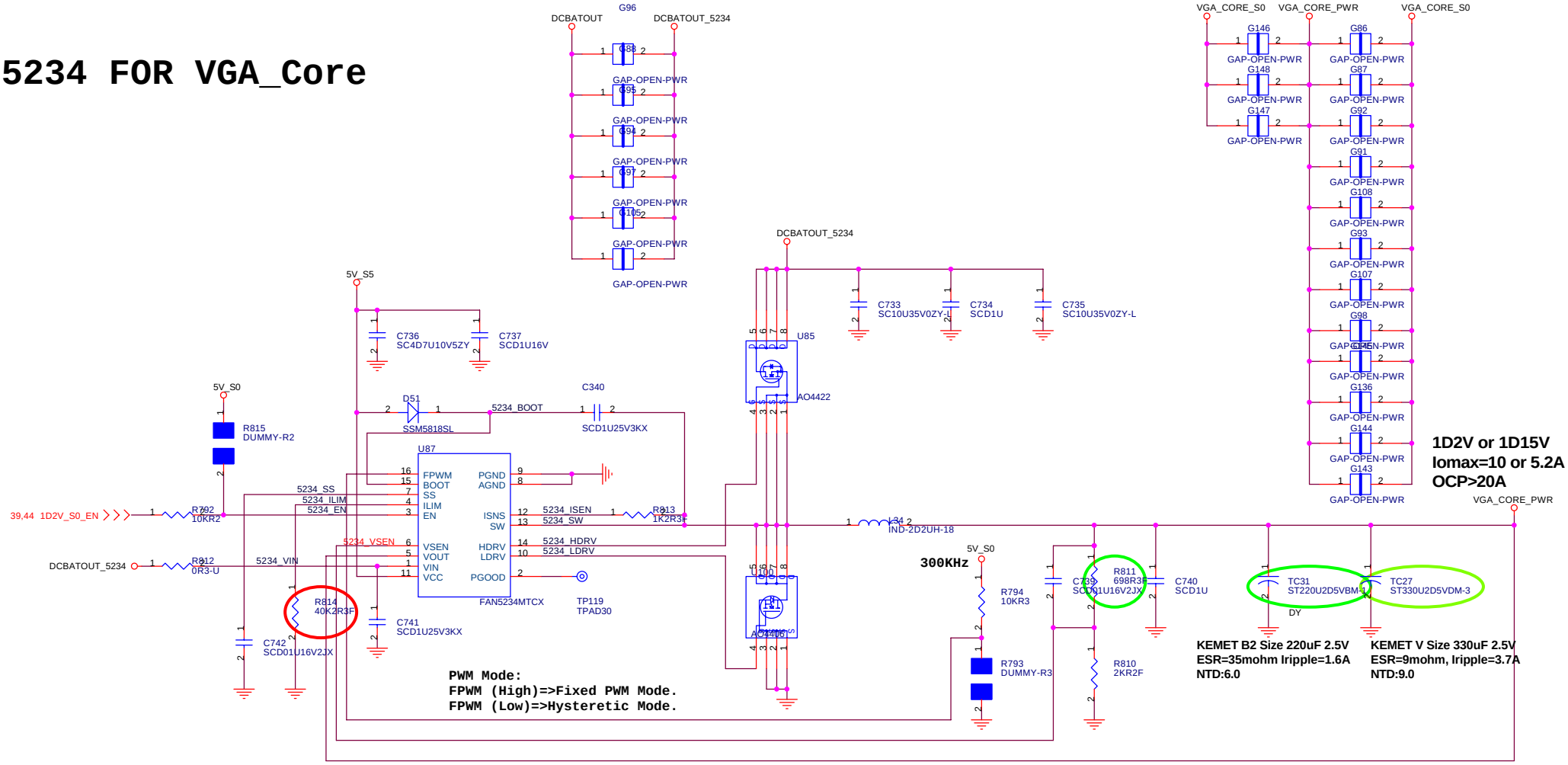
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

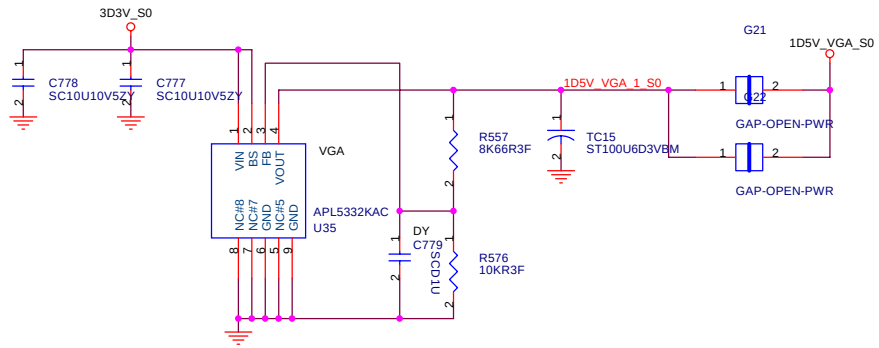
Title: **VGA SELECTOR**

Size	Document Number	Rev
A3	**Bolsena**	SA

Date: Tuesday, December 28, 2004 Sheet 54 of 58

FAN5234 FOR VGA_Core



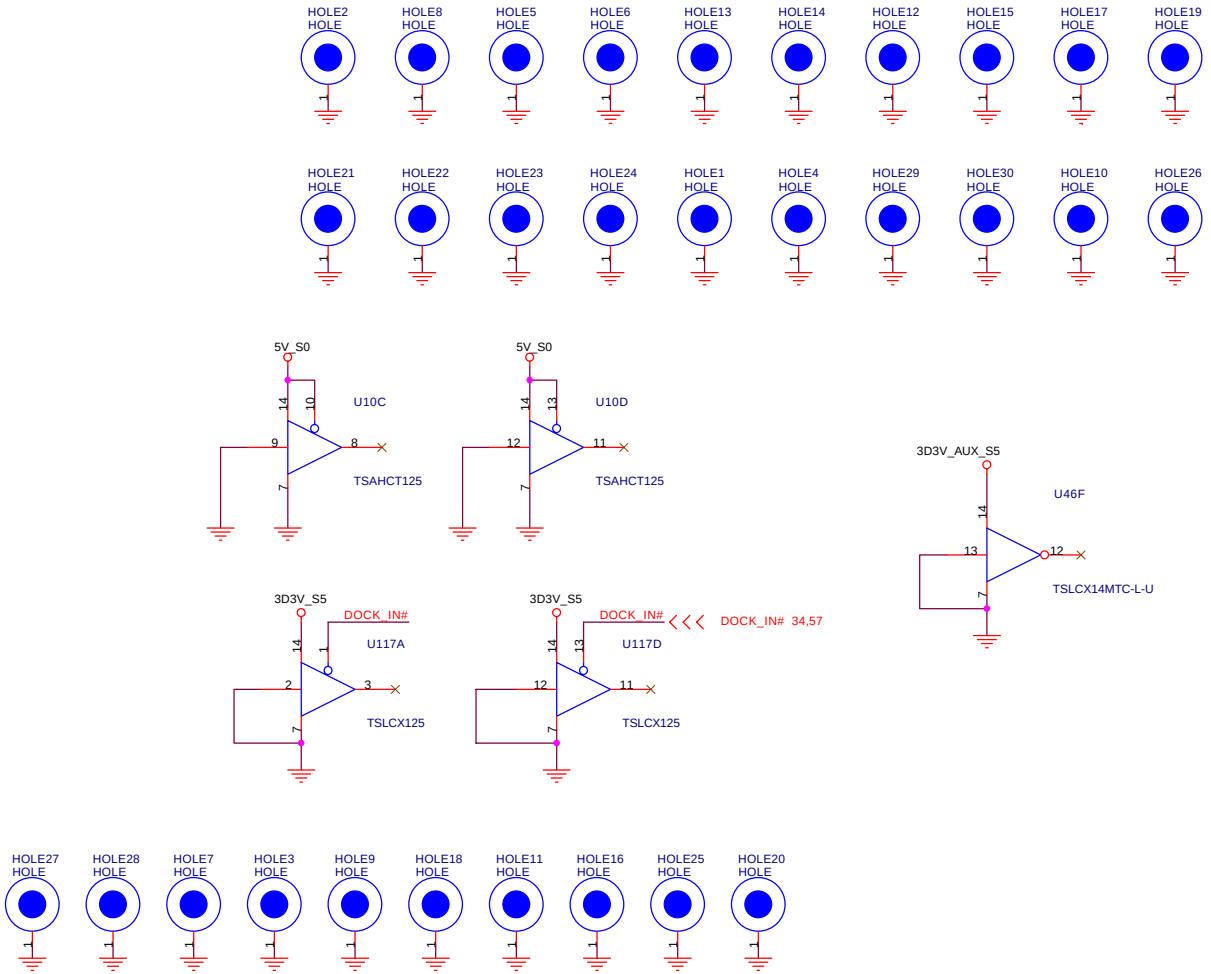


?M24/M26 POWER PLAY (GPIO_PWRCNTL)
high (3.3V) = set lower core voltage (VDDC = 1.0V)
low (0V) = set higher core voltage (VDDC = 1.2V)

(Power Team)

<Variant Name>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VGA CORE 1D2V or 1D0V
Size A3	Document Number: Bolsena
Rev	SA
Date: Tuesday, December 28, 2004	Sheet 55 of 58



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EMI**

Size	Document Number	Rev
A3	**Bolsena**	SA

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?ez4 signal changed

EZ4

FOX-CONN120-8R

PPD[7..0] 58

15,49 TMDS_EZ4_TX1-
15,49 TMDS_EZ4_TX2-
15,49 TMDS_EZ4_TX1+
15,49 TMDS_EZ4_TX2+
15,49 TMDS_EZ4_TX0-
15 DVI_EZ4_HPD
15,49 TMDS_EZ4_TX0+
15 EZ4_DVI_DDC_D
15,49 TMDS_EZ4_TXC+
15 EZ4_DVI_DDC_C
15,49 TMDS_EZ4_TXC-
34,56 DOCK_IN#
33 DOCK_MIC_JKIN#
33 DOCK_LIN_R
33 DOCK_LIN_L
33 DOCK_EXT_MIC_IN
33 SPKR_R_DOCK
33 SPKR_L_DOCK
16 EZ4_HS
16 EZ4_VS
16 EZ4_CRT_DDC_D
12 PCIE_RXP0
16 EZ4_CRT_DDC_C
12 PCIE_RXN0
18,26,34,37 P_SERIRQ
3,8,21 SMBC_SB
12 PCIE_TXP0
12 PCIE_TXN0
3,8,21 SMBD_SB
PE_REQ1#
3 CLK_PCIE_DOCK1
12 PCIE_RXP1
3 CLK_PCIE_DOCK1#
12 PCIE_RXN1

D_TTGP0
D_TTGN0
D_RTGP1
D_TGP2
D_RTGN1
D_TGN2
D_TGP3
10M_LED#
D_TGN3
PSTROB#
PAUTOFD#
DOCK_JACK_IN
PPD0
PERROR#
RI1#_5 37
PPD1
PINIT#
PPD2
PSLCTIN#
PPD3
PPD4
PPD5
PPD6
PPD7
PACK#
PBUSY
PPE
PSLCT
SUSON
MAINON

D_TTGP0 30
ACT_LED# 29,30
D_TTGN0 30
D_RTGP1 30
D_TGP2 30
D_RTGN1 30
D_TGN2 30
D_TGP3 30
10M_LED# 29,30
D_TGN3 30
PSTROB# 58
PAUTOFD# 58
DOCK_JACK_IN 33
SPDIF 32,33
PERROR# 58
DTR1_BOUT1_5 37
PINIT# 58
CTS1#_5 37
SOUT1_5 37
PSLCTIN# 58
RTS1#_5 37
SIN1_5 37
DSR1#_5 37
DCD1#_5 37
PS2_KDAT 34
PACK# 58
PS2_KCLK 34
PBUSY 58
PS2_MDAT 34
PPE 58
PS2_MCLK 34
PSLCT 58
PCIE_WAKE# 21
PCIRST_BUF# 15,18,26,28,29,31,34
CLK_PCIE_DOCK2 3
PCIE_TXP1 12
CLK_PCIE_DOCK2# 3
PCIE_TXN1 12
DOCK_AD+

TV_COMP_DOCK
TV_LUMA_DOCK
TV_CRMA_DOCK
EZ_PWROK
DOCK_ON_2#

R764 1KR2
TP118 TPAD30
TP121 TPAD30
AUD_AGND_EZ4

3D3V_S5
R762 10KR2
U93 NC7SZ08-U
Q46 2N7002
R763 1MR2
DOCK_IN#
DOCK_ON_1 30

Function	LAN
SYSTEM	L
DOCK	H

5V_S0
R761 10KR2
R760 1MR2
Q45 MMBT3904-U1
DOCK_ON_2#

Dummy when no EZ4

TV SWITCH

Function	S
A to B0	L
A to B1	H

5V_S0
C977 SCD1U16V

TV_COMP
TV_LUMA
TV_CRMA

RN112 SRN0-1-U
49 DIS_COMP
49 DIS_LUMA
49 DIS_CRMA
Dummy when use UMA

RN113 SRN0-1-U DY
13 UMA_COMP
13 UMA_LUMA
13 UMA_CRMA
Dummy when use Discrete

DOCK_ON_2#
R791 0R2-0
DOCK_TV_ON#

U96 NC7SB3157P6X-U
U97 NC7SB3157P6X-U
U98 NC7SB3157P6X-U
A B0 VCC GND S B1

TV_COMP_DOCK
TV_LUMA_DOCK
TV_CRMA_DOCK
TV_COMP_SYS 16
TV_LUMA_SYS 16
TV_CRMA_SYS 16
Dummy when no EZ4

RN117 SRN0-1-U DY
Dummy when use EZ4

CRT SWITCH

Function	CRT	TV
SYSTEM	H	H
DOCK	L	L

5V_S0
C959 SCD1U16V

CRT_G_1
CRT_B_1
CRT_R_1

RN114 SRN0-1-U
49 DIS_G
49 DIS_B
49 DIS_R
Dummy when use UMA

RN115 SRN0-1-U DY
13 UMA_G
13 UMA_B
13 UMA_R
Dummy when use Discrete

DOCK_ON_2#
R790 0R2-0
DOCK_CRT_ON#

U95 NC7SB3157P6X-U
U94 NC7SB3157P6X-U
U99 NC7SB3157P6X-U
A B0 VCC GND S B1

CRT_G_DOCK
CRT_B_DOCK
CRT_R_DOCK
CRT_G_SYS 16
CRT_B_SYS 16
CRT_R_SYS 16
Dummy when no EZ4

RN116 SRN0-1-U DY
Dummy when use EZ4

CTS1# 5
SIN1_5
DSR1# 5
DCD1# 5
RTS1# 5
RI1# 5
DTR1_BOUT1_5
SOUT1_5
RC13 RC14
SRC100P50V-U SRC100P50V-U
Dummy when no EZ4

18,21,34,38,39,43,44 PM_SLP_S3#
21,34,44 PM_SLP_S5#
DOCK_IN#
U117C
U117B
MAINON
SUSON
TSLCX125
Dummy when no EZ4

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: EASY PORT4 (1/2)

Size: A3 | Document Number: Bolsena | Rev: SA

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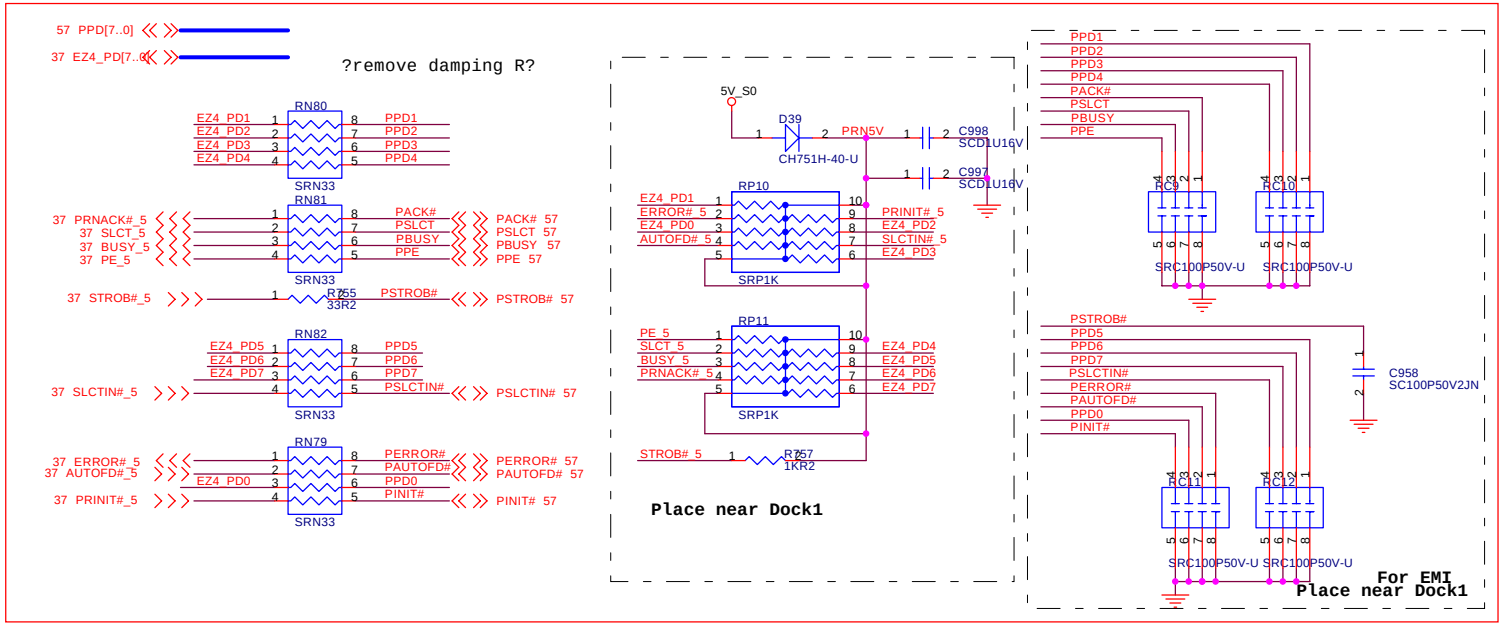
PRINT PORT



Dummy when no EZ4

華創資通 **Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
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