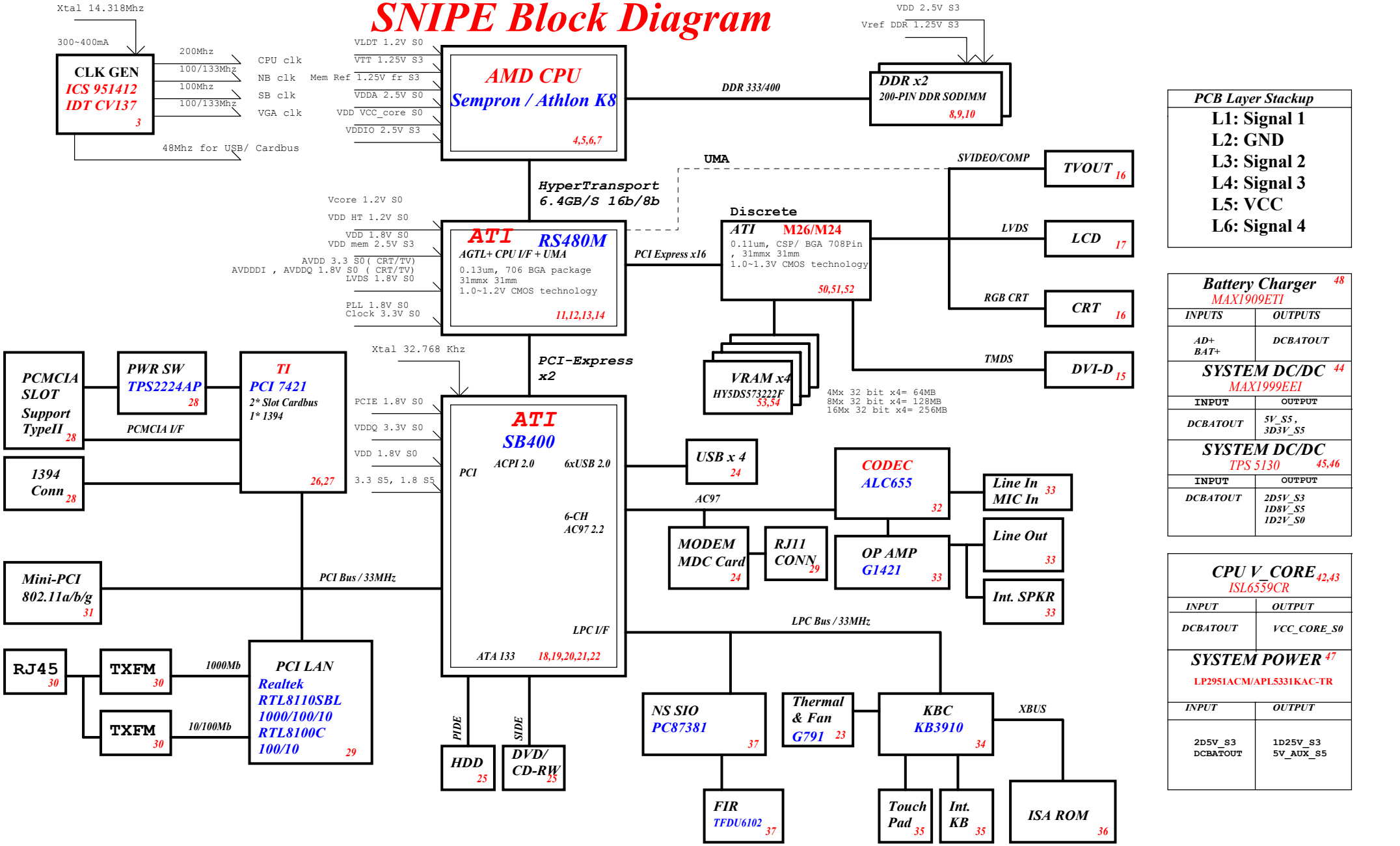
SNIPE Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: GND
L3: Signal 2
L4: Signal 3
L5: VCC
L6: Signal 4

Battery Charger 48
MAX1909ETI

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SYSTEM DC/DC 44
MAX1999EEI

INPUT	OUTPUT
DCBATOUT	5V_S5 , 3D3V_S5

SYSTEM DC/DC
TPS 5130 45,46

INPUT	OUTPUT
DCBATOUT	2D5V_S3 1D8V_S5 1D2V_S0

CPU V_CORE 42,43
ISL6559CR

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM POWER 47
LP2951ACM/APL5331KAC-TR

INPUT	OUTPUT
2D5V_S3 DCBATOUT	1D25V_S3 5V_AUX_S5

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **BLOCK DIAGRAM**

Size	Document Number	Rev
A3	SNIPE	SA

Date: Monday, November 22, 2004 Sheet 1 of 56

SA to SB need to check
1. connect G781 Thermal Alert pin to VGA_GPIO14
2. ene KBC P165 LPCRST# , we suggest pull low avoid leakage
3. Clk to NB need to add Cap. when the trace change layer.
4. check page 9. what is the value of R481,R486, R498 and R499 is 100 ohm or 12 ohm.
5. check page 15, if on discrete mode does the 1D8V_S0 power for lvds should dummy or still contect on power plan.
6. check page 19, can the 0 ohm resistance be dummied on P.19 right hand side?
7. check page 20, R203's voltage on pin 2.
8. page 21. check when the unused USB pin should be pull down or floating.
9. Can R471 change to common value?
10. check giga lan and 10/100 connect. Does them the same or can chose a cheaper one?
11. page 38. 12VGATE_S0 can decreased resistance.
12. Does the 1D5V_VGA_S0 can come from TPS5130?

Schematic change:
R659, change from 0R2 to 10Kr2

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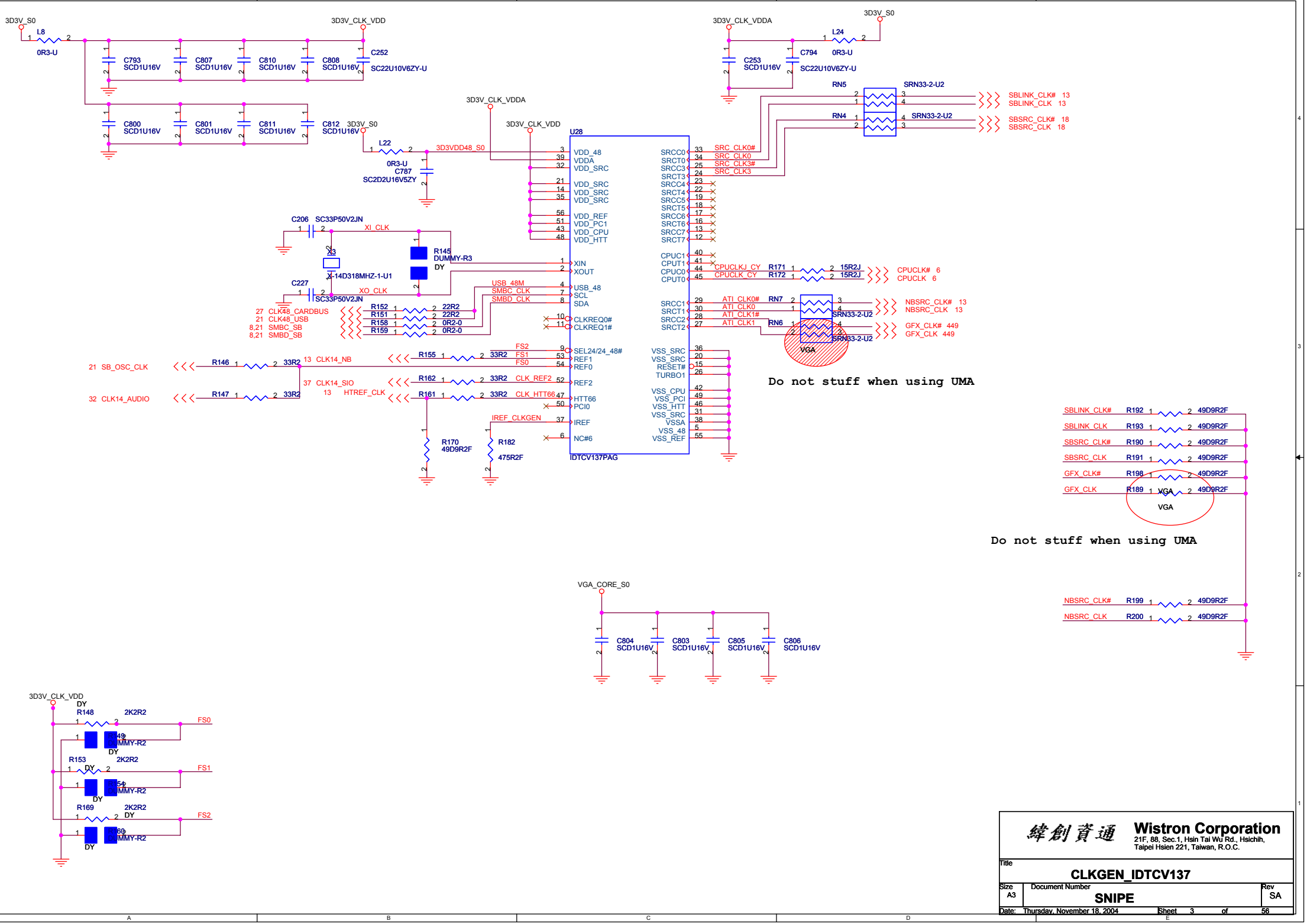
Taipei Hsien 221, Taiwan, R.O.C.

Title	CHANGE HISTORY	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 2 of 56	



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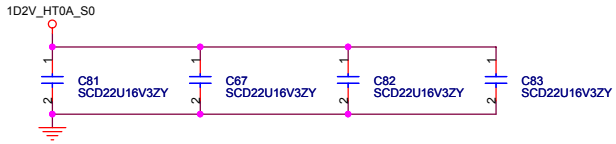
Title	CLKGEN_IDTCV137	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 3 of 56	



HTT for CPU sideA Transmit power and NB sideA Receive power

HTT for CPU sideB Receive power and NB sideA Transmit power

LAYOUT: Place bypass cap on topside of board near HTT power pins that are not connected directly to downstream HTT device, but connected internally to other HTT power pins.

Used SideB Power Plane

Used SideA Power Plane

62.10030.041

BGA754-SKT-U

By ME requset U11 P/N:
Main 62.10030.041
Second 62.10053.191
Third 62.10053.201

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Taipei Hsien 221, Taiwan, R.O.C.

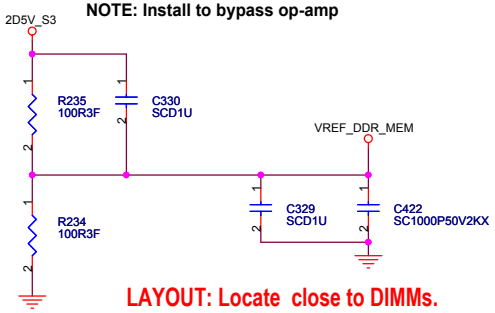
Title: CPU(1/4)_HyperTransport I/F

Size: A3 | Document Number: SNIPE | Rev: SA

Date: Thursday, November 18, 2004 | Sheet 4 of 56

VREF_DDR_MEM

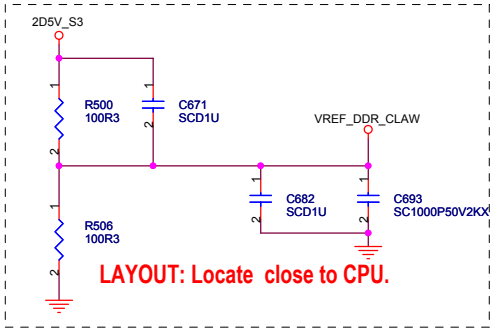
NOTE: Test with passive probes only.
NOTE: Install to bypass op-amp



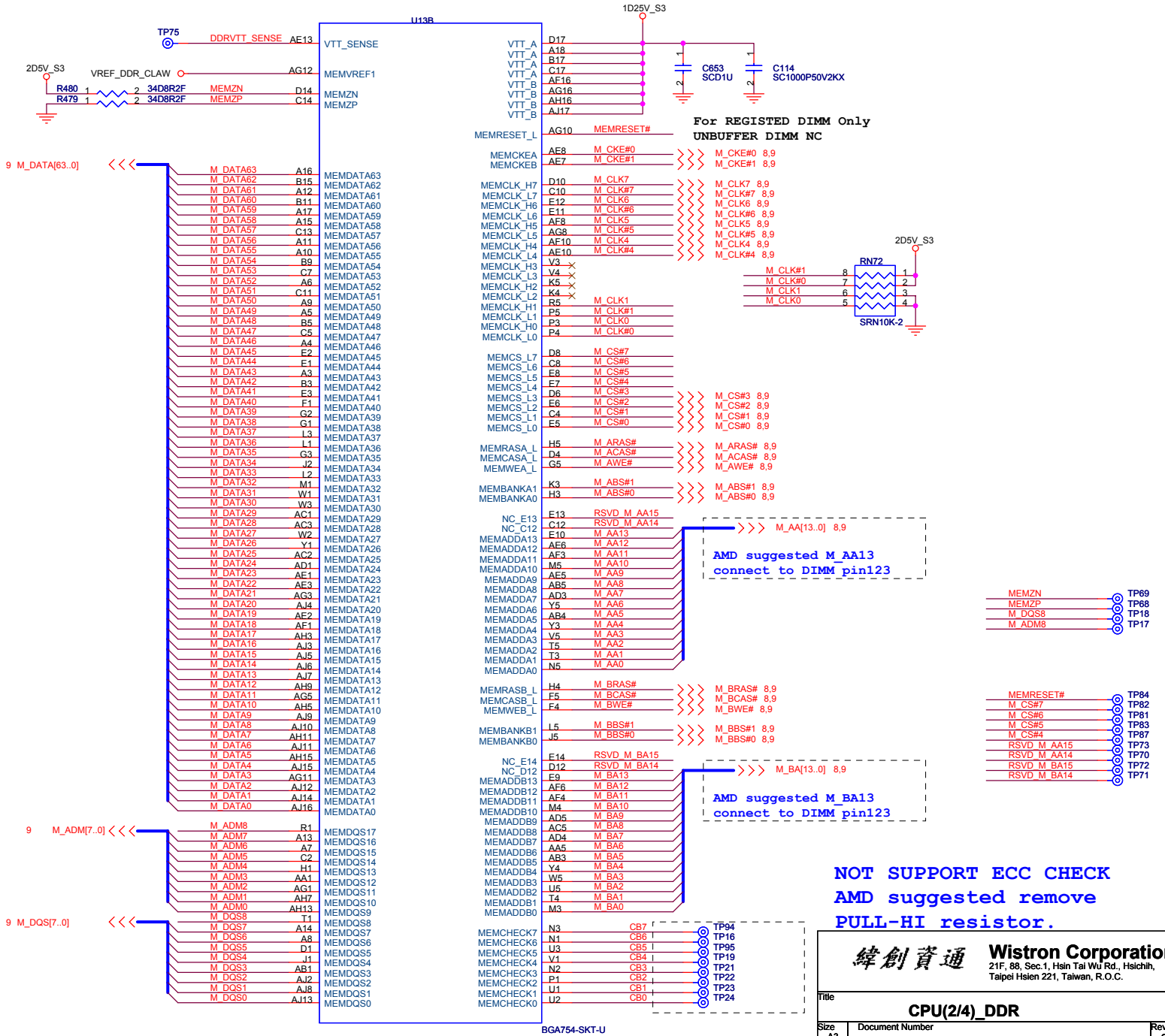
LAYOUT: Locate close to DIMMs.

NOTE: Remove to bypass op-amp

VREF_DDR_CLAW



LAYOUT: Locate close to CPU.



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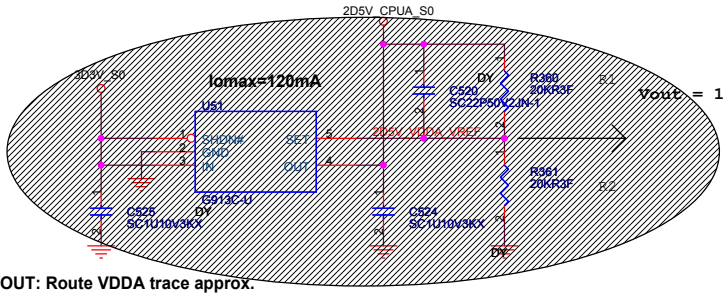
Title: CPU(2/4)_DDR

Size: A3 | Document Number: SNIPE | Rev: SA

Date: Thursday, November 18, 2004 | Sheet 5 of 56

2D5V_VDDA_S0



AMD SUGGEST TO USE 100 ~ 300UH

LAYOUT: Route trace 50 mils wide and 500 to 750 mils long between these caps.

LAYOUT: Route VDDA trace approx. 50 mils wide (use 2x25 mil traces to exit ball field) and 500 mils long.

AMD SUGGEST TO USE 2D5V_CPUA_S0

KEMET,NT:5.7, B2 size
ST100U4VBM-1 (80.10716.321)
Iripple=1.1A,ESR=70mohm

SANYO, NT$:6.1
Iripple=1.1A,ESR=70mohm
3.5/2.8/2.0
77.21071.031

AMD suggest voltege from 2D5V_S0 to 2D5V_S3 differentially impedance 100

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

Connect to VDDIO for AMD suggest.

THERMTRIP#Level shift to SB400

HDT Connectors

Add HDT connector for AMD suggested

CHANGE FROM 1KR3 TO 680R2 FOR AMD
CHECK LIST

Validation Test Points

LAYOUT: Place close to the CPU.

BGA754-SKT-U

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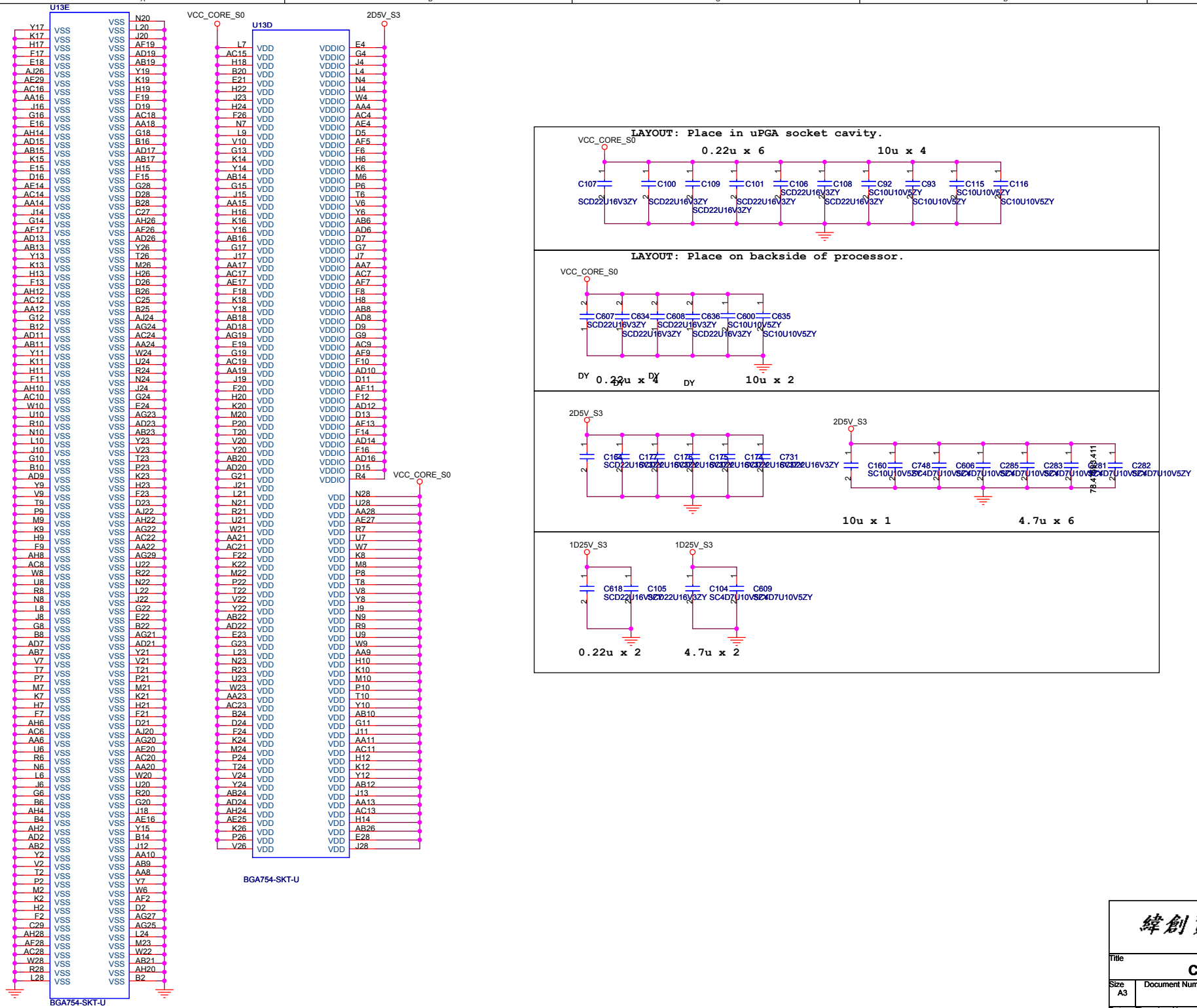
Title: CPU(3/4)_Control & Debug
Size: A3 | Document Number: SNIPE | Rev: SA
Date: Thursday, November 18, 2004 | Sheet 6 of 56



Company	Wistron Corporation
Address	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	CPU(4/4)_Power
Size	A3
Document Number	SNIPE
Rev	SA
Date	Thursday, November 18, 2004
Sheet	7 of 56

DM1

NORMAL TYPE

DDR-SODIMM-N-U1

NOT SUPPORT ECC CHECK
AMD suggested pull-low

Layout trace 20 mil

DM2

REVERSE TYPE

DDR-SODIMM-R-U2

Layout trace 20 mil

By ME requset DM1 P/N:
Main 62.10017.191
Second 62.10017.381

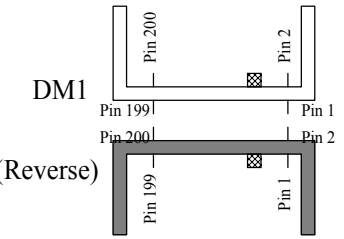
By ME requset DM2 P/N:
Main 62.10017.201
Second 62.10017.371
Third 62.10017.701

DY

AMD K8
ClawHummar

MD63 SMA11 SMA10 SMA0 SMA14 SMA12 MD0

DDR SOCKET PLACEMENT
TOP VIEW PERSPECTIVE DRAWING



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Title	DDR SO-DIMM SKT	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 8 of 56	

SERIES DAMPING

PLACE RNs CLOSE TO FIRST DM (DM1), < 0.75"
STRICT EQUAL LENGTH LIMITATION WITH DQS,
CB PINS

RN21
M_DATA4 1 16 M_DATA_R_4
M_DATA5 2 15 M_DATA_R_5
M_ADM0 3 14 M_ADM_R0
M_DATA6 4 13 M_DATA_R_6
M_DATA7 5 12 M_DATA_R_7
M_DATA13 6 11 M_DATA_R_13
M_DATA12 7 10 M_DATA_R_12
M_ADM1 8 9 M_ADM_R1
SRN10J-3

RN18
M_DATA34 1 16 M_DATA_R_34
M_DATA32 2 15 M_DATA_R_32
M_DQS4 3 14 M_DQS_R4
M_DATA33 4 13 M_DATA_R_33
M_DATA36 5 12 M_DATA_R_36
M_DATA37 6 11 M_DATA_R_37
M_ADM4 7 10 M_ADM_R4
M_DATA39 8 9 M_DATA_R_39
SRN10J-3

RN34
M_DATA1 1 16 M_DATA_R_1
M_DATA0 2 15 M_DATA_R_0
M_DQS0 3 14 M_DQS_R0
M_DATA2 4 13 M_DATA_R_2
M_DATA3 5 12 M_DATA_R_3
M_DATA8 6 11 M_DATA_R_8
M_DATA9 7 10 M_DATA_R_9
M_DQS1 8 9 M_DQS_R1
SRN10J-3

RN28
M_DATA35 1 16 M_DATA_R_35
M_DATA41 2 15 M_DATA_R_41
M_DATA40 3 14 M_DATA_R_40
M_DQS5 4 13 M_DQS_R5
M_DATA42 5 12 M_DATA_R_42
M_DATA43 6 11 M_DATA_R_43
M_DATA49 7 10 M_DATA_R_49
M_DATA48 8 9 M_DATA_R_48
SRN10J-3

RN20
M_DATA14 1 16 M_DATA_R_14
M_DATA15 2 15 M_DATA_R_15
M_DATA21 3 14 M_DATA_R_21
M_DATA20 4 13 M_DATA_R_20
M_ADM2 5 12 M_ADM_R2
M_DATA23 6 11 M_DATA_R_23
M_DATA22 7 10 M_DATA_R_22
M_DATA25 8 9 M_DATA_R_25
SRN10J-3

RN17
M_DATA38 1 16 M_DATA_R_38
M_DATA45 2 15 M_DATA_R_45
M_DATA44 3 14 M_DATA_R_44
M_ADM5 4 13 M_ADM_R5
M_DATA47 5 12 M_DATA_R_47
M_DATA46 6 11 M_DATA_R_46
M_DATA53 7 10 M_DATA_R_53
M_DATA52 8 9 M_DATA_R_52
SRN10J-3

RN33
M_DATA11 1 16 M_DATA_R_11
M_DATA10 2 15 M_DATA_R_10
M_DATA17 3 14 M_DATA_R_17
M_DATA16 4 13 M_DATA_R_16
M_DQS2 5 12 M_DQS_R2
M_DATA19 6 11 M_DATA_R_19
M_DATA18 7 10 M_DATA_R_18
M_DATA24 8 9 M_DATA_R_24
SRN10J-3

RN27
M_DQS6 1 16 M_DQS_R6
M_DATA50 2 15 M_DATA_R_50
M_DATA51 3 14 M_DATA_R_51
M_DATA56 4 13 M_DATA_R_56
M_DATA57 5 12 M_DATA_R_57
M_DQS7 6 11 M_DQS_R7
M_DATA58 7 10 M_DATA_R_58
M_DATA59 8 9 M_DATA_R_59
SRN10J-3

RN19
M_DATA29 1 16 M_DATA_R_29
M_DATA28 2 15 M_DATA_R_28
M_DQS3 3 14 M_DQS_R3
M_ADM3 4 13 M_ADM_R3
M_DATA26 5 12 M_DATA_R_26
M_DATA27 6 11 M_DATA_R_27
M_DATA30 7 10 M_DATA_R_30
M_DATA31 8 9 M_DATA_R_31
SRN10J-3

RN16
M_ADM6 1 16 M_ADM_R6
M_DATA54 2 15 M_DATA_R_54
M_DATA55 3 14 M_DATA_R_55
M_DATA61 4 13 M_DATA_R_61
M_DATA60 5 12 M_DATA_R_60
M_ADM7 6 11 M_ADM_R7
M_DATA62 7 10 M_DATA_R_62
M_DATA63 8 9 M_DATA_R_63
SRN10J-3

5,8 M_CKE#0 M_CKE#0
5,8 M_CKE#1 M_CKE#1

05/10
Remove the damping resistor for AMD suggest.

PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", PLACE RPs CLOSE TO SECOND DM (DM2)
NO EQUAL LENGTH LIMITATION

1D25V_S3

RN44
M_ADM_R1 1 16 M_DATA_R_36
M_DATA_R_13 2 15 M_DATA_R_32
M_DATA_R_12 3 14 M_DATA_R_37
M_DATA_R_6 4 13 M_DATA_R_33
M_DATA_R_7 5 12 M_ADM_R4
M_ADM_R0 6 11 M_DQS_R4
M_DATA_R_5 7 10 M_DATA_R_38
M_DATA_R_4 8 9 M_DATA_R_39
SRN68J-1

RN38
1 16 M_DATA_R_36
2 15 M_DATA_R_32
3 14 M_DATA_R_37
4 13 M_DATA_R_33
5 12 M_ADM_R4
6 11 M_DQS_R4
7 10 M_DATA_R_38
8 9 M_DATA_R_39
SRN68J-1

RN52
M_DATA_R_1 1 16 M_DATA_R_48
M_DATA_R_0 2 15 M_DATA_R_49
M_DQS_R0 3 14 M_DATA_R_43
M_DATA_R_2 4 13 M_DATA_R_42
M_DATA_R_3 5 12 M_DQS_R5
M_DATA_R_8 6 11 M_DATA_R_41
M_DATA_R_9 7 10 M_DATA_R_40
M_DQS_R1 8 9 M_DATA_R_34
SRN68J-1

RN48
1 16 M_DATA_R_48
2 15 M_DATA_R_49
3 14 M_DATA_R_43
4 13 M_DATA_R_42
5 12 M_DQS_R5
6 11 M_DATA_R_41
7 10 M_DATA_R_40
8 9 M_DATA_R_34
SRN68J-1

RN43
M_DATA_R_25 1 16 M_DATA_R_35
M_DATA_R_22 2 15 M_DATA_R_46
M_DATA_R_23 3 14 M_DATA_R_47
M_ADM_R2 4 13 M_ADM_R5
M_DATA_R_20 5 12 M_DATA_R_44
M_DATA_R_21 6 11 M_DATA_R_45
M_DATA_R_14 7 10 M_DATA_R_53
M_DATA_R_15 8 9 M_DATA_R_52
SRN68J-1

RN37
1 16 M_DATA_R_35
2 15 M_DATA_R_46
3 14 M_DATA_R_47
4 13 M_ADM_R5
5 12 M_DATA_R_44
6 11 M_DATA_R_45
7 10 M_DATA_R_53
8 9 M_DATA_R_52
SRN68J-1

RN51
M_DATA_R_11 1 16 M_DATA_R_59
M_DATA_R_10 2 15 M_DATA_R_58
M_DATA_R_16 3 14 M_DQS_R7
M_DATA_R_17 4 13 M_DATA_R_57
M_DQS_R2 5 12 M_DATA_R_56
M_DATA_R_19 6 11 M_DATA_R_51
M_DATA_R_18 7 10 M_DATA_R_50
M_DATA_R_24 8 9 M_DQS_R6
SRN68J-1

RN47
1 16 M_DATA_R_59
2 15 M_DATA_R_58
3 14 M_DQS_R7
4 13 M_DATA_R_57
5 12 M_DATA_R_56
6 11 M_DATA_R_51
7 10 M_DATA_R_50
8 9 M_DQS_R6
SRN68J-1

RN42
M_DATA_R_30 1 16 M_DATA_R_55
M_DATA_R_31 2 15 M_DATA_R_54
M_DATA_R_26 3 14 M_ADM_R6
M_DATA_R_27 4 13 M_DATA_R_60
M_ADM_R3 5 12 M_DATA_R_61
M_DQS_R3 6 11 M_ADM_R7
M_DATA_R_29 7 10 M_DATA_R_63
M_DATA_R_28 8 9 M_DATA_R_62
SRN68J-1

RN36
1 16 M_DATA_R_55
2 15 M_DATA_R_54
3 14 M_ADM_R6
4 13 M_DATA_R_60
5 12 M_DATA_R_61
6 11 M_ADM_R7
7 10 M_DATA_R_63
8 9 M_DATA_R_62
SRN68J-1

1D25V_S3

RN50
M_CKE#1 2 3
M_BA12 1 4
SRN47J

RN32
M_CKE#0 2 3
M_AA12 1 4
SRN47J

RN31
M_AA11 1 16
M_AA9 2 15
M_AA7 3 14
M_AA5 4 13
M_AA4 5 12
M_AA8 6 11
M_AA6 7 10
M_AA3 8 9
SRN47J-1-U

RN39
M_CS#3 1 16
M_BA13 2 15
M_CS#2 3 14
M_BRAS# 4 13
M_BBS#1 5 12
M_BCAS# 6 11
M_BA0 7 10
M_BA2 8 9
SRN47J-1-U

RN30
M_AA1 1 16
M_AA10 2 15
M_AA2 3 14
M_AA0 4 13
M_ABS#1 5 12
M_ARAS# 6 11
M_AWE# 7 10
M_ABS#0 8 9
SRN47J-1-U

RN49
M_BA7 1 16
M_BA3 2 15
M_BA6 3 14
M_BA9 4 13
M_BA10 5 12
M_BA1 6 11
M_BBS#0 7 10
M_BWE# 8 9
SRN47J-1-U

RN40
M_BA5 1 8
M_BA8 2 7
M_BA11 3 6
M_BA4 4 5
SRN47-1

RN29
M_AA13 1 8
M_CS#0 2 7
M_CS#1 3 6
M_ACAS# 4 5
SRN47-1

M_ADM_R[7..0] 8
M_ADM[7..0] 5
M_DATA[63..0] 5
M_DATA_R_[63..0] 8
M_DQS[7..0] 5
M_DQS_R[7..0] 8
M_AA[13..0] 5,8
M_ABS#[1..0] 5,8
M_BA[13..0] 5,8
M_BBS#[1..0] 5,8
M_AWE# 5,8
M_ACAS# 5,8
M_ARAS# 5,8
M_BWE# 5,8
M_BCAS# 5,8
M_BRAS# 5,8
M_CS#0 5,8
M_CS#1 5,8
M_CS#2 5,8
M_CS#3 5,8

Place it near CPU

1 R498 121R3F M_CLK7 M_CLK#7 M_CLK7 5,8 M_CLK#7 5,8
1 R481 121R3F M_CLK6 M_CLK#6 M_CLK6 5,8 M_CLK#6 5,8
1 R499 121R3F M_CLK5 M_CLK#5 M_CLK5 5,8 M_CLK#5 5,8
1 R486 121R3F M_CLK4 M_CLK#4 M_CLK4 5,8 M_CLK#4 5,8

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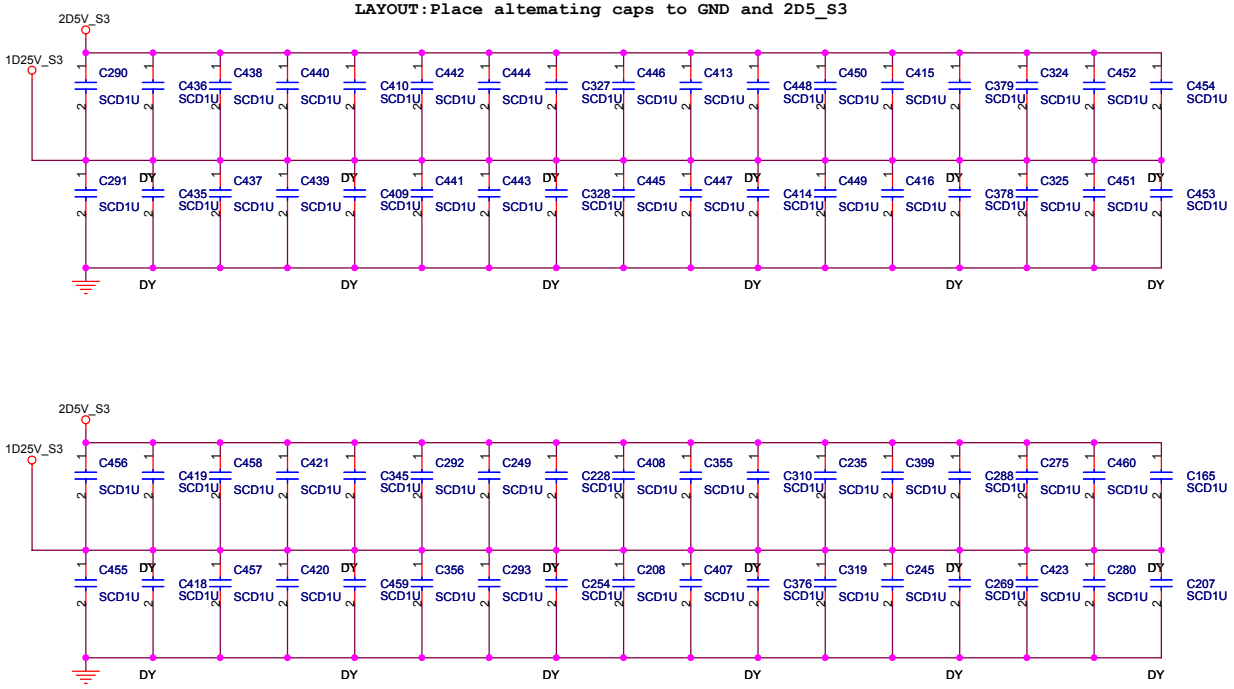
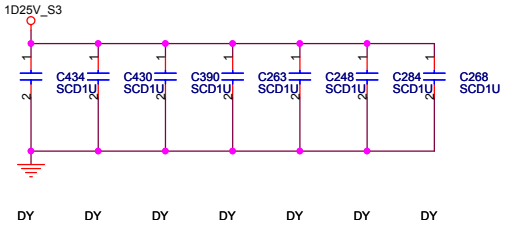
Taipei Hsien 221, Taiwan, R.O.C.

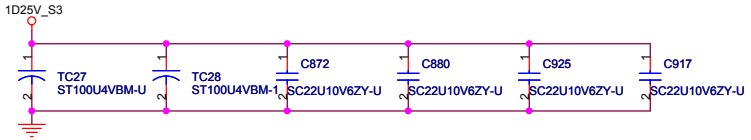
Title: DDR DAMPING & TERMINATION
Size: A3 | Document Number: SNIPE | Rev: SA
Date: Thursday, November 18, 2004 | Sheet 9 of 56

LAYOUT:Place altemating caps to GND and 2D5_S3

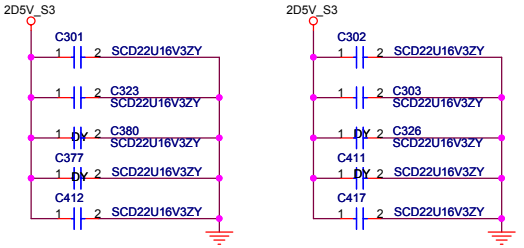




LAYOUT:Place at end of the DIMMs



LAYOUT:Place close to Power Pin of DDR socket.



0.22u x 10

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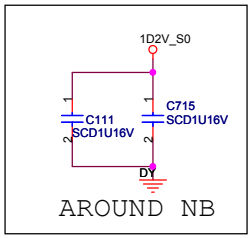
Title: **DDR DECOUPLING**

Size	Document Number	Rev
A3	SNIPE	SA

Date: Thursday, November 18, 2004 Sheet 10 of 56

CLAW HAMMER TO NB

NB TO CLAW HAMMER



緯創資通 **Wistron Corporation**
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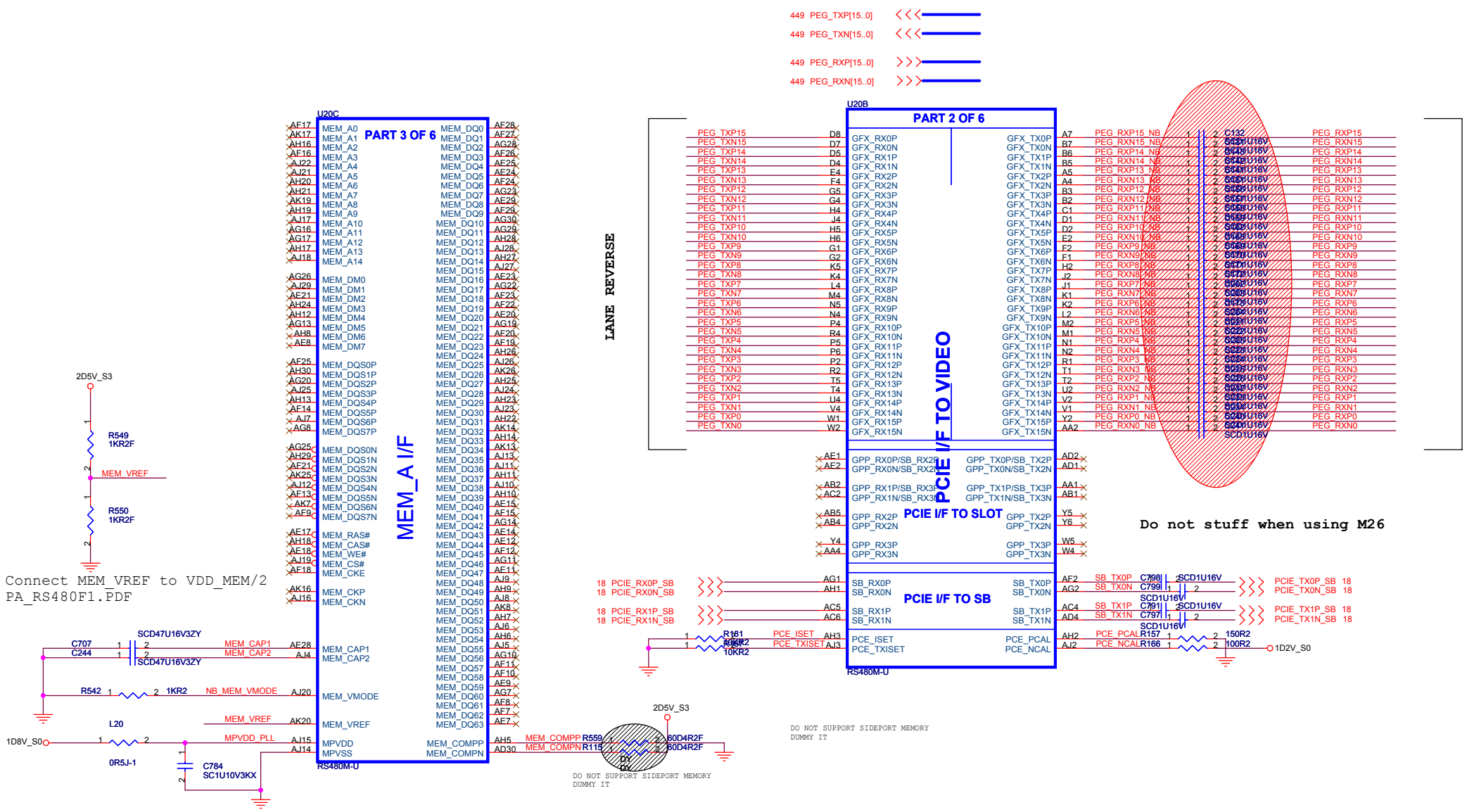
Taipei Hsien 221, Taiwan, R.O.C.

Title	NB-RS480M_HT	
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 11 of 56	



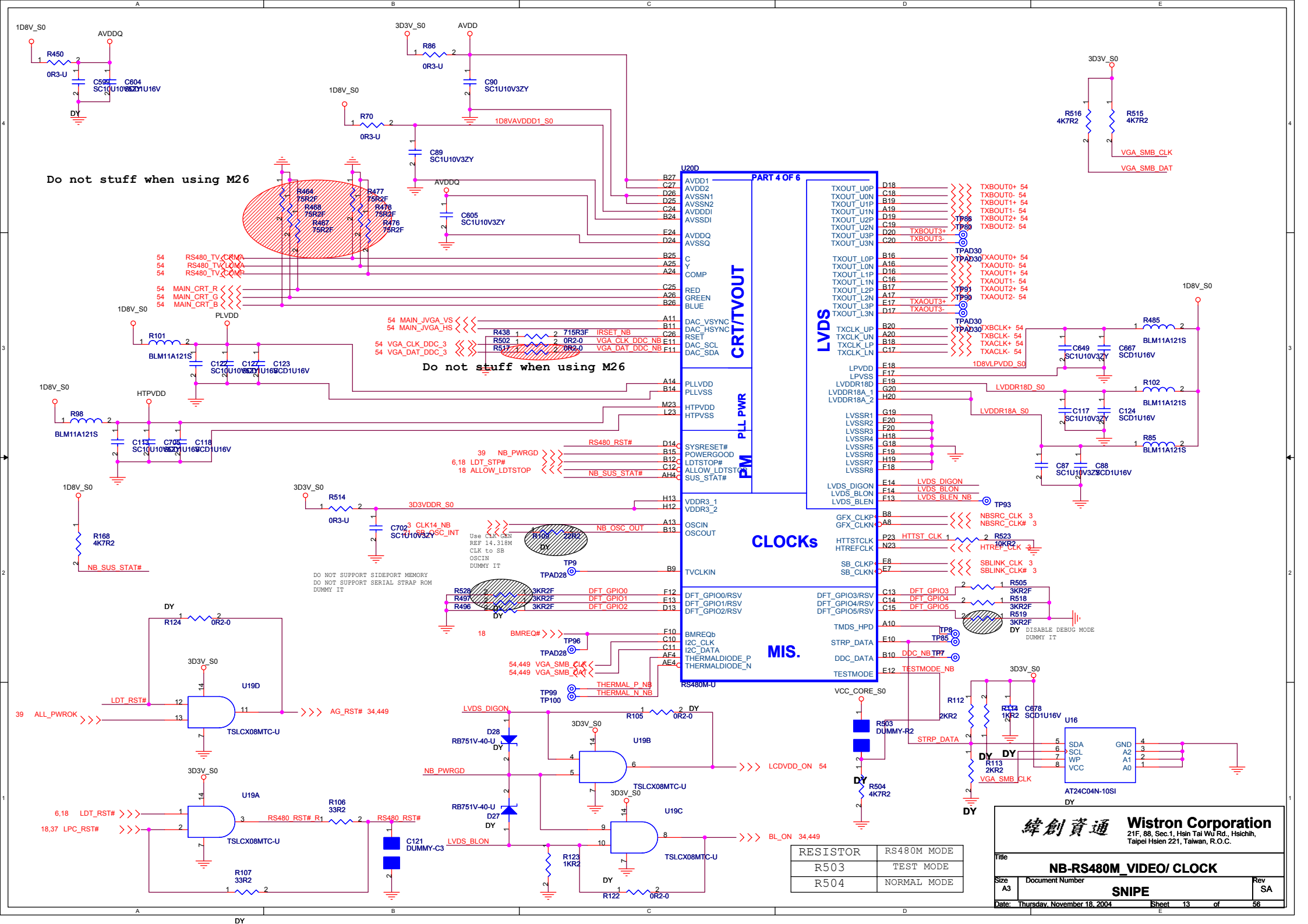
When disable local frame buffer, VDD_MEM connect to 2D5V_S3, MEM_VMODE connect to GND, MEM_VREF connect to 2D5V_S3, MPVDD connected to 1D8V
DSG-215-RS480-04.PDF

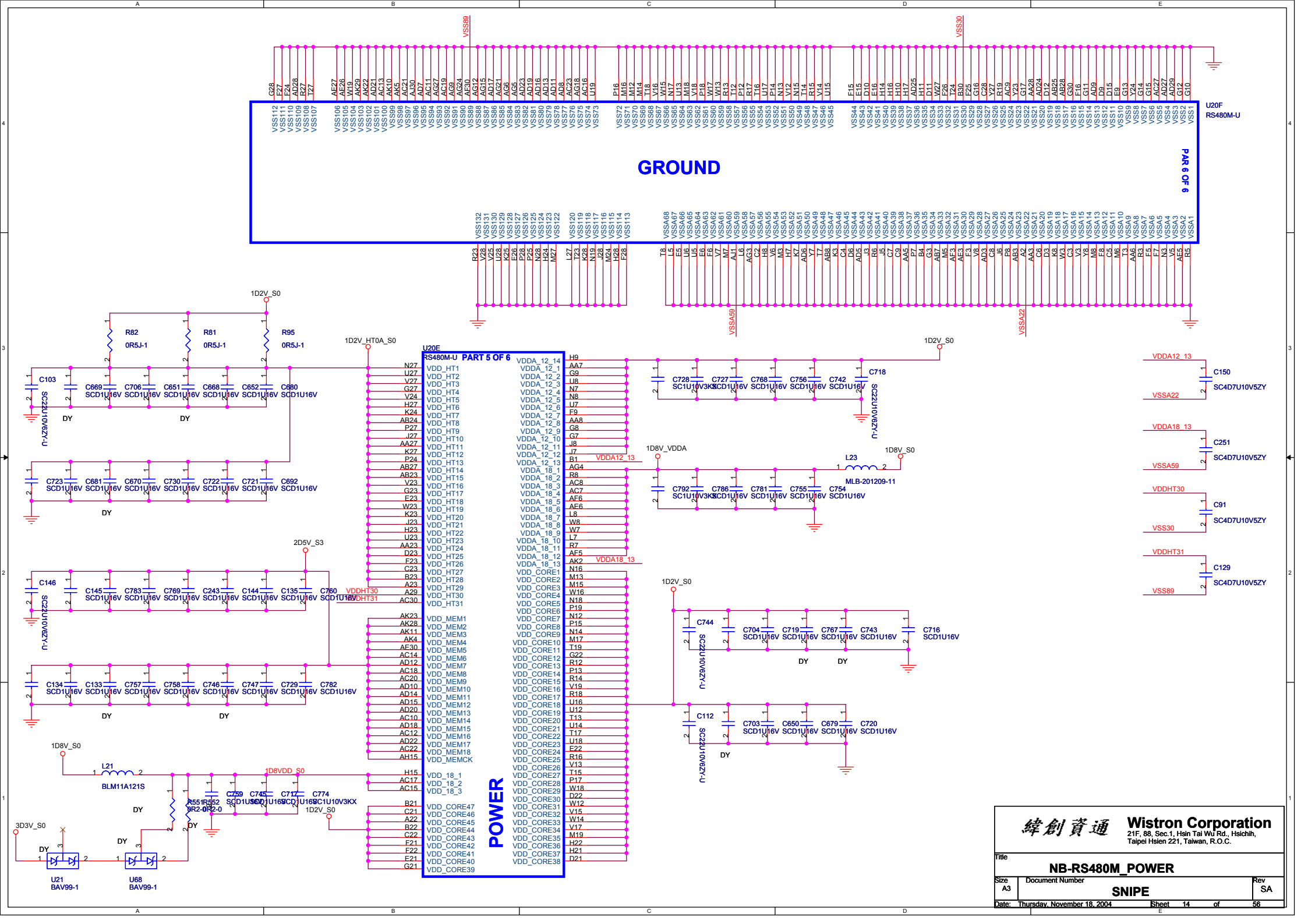
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: NB-RS480M_MEM/PCIE_LINK I/F

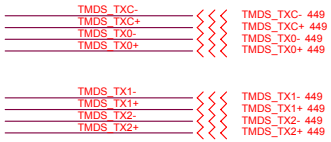
Size	Document Number	Rev
A3	SNIPE	SA

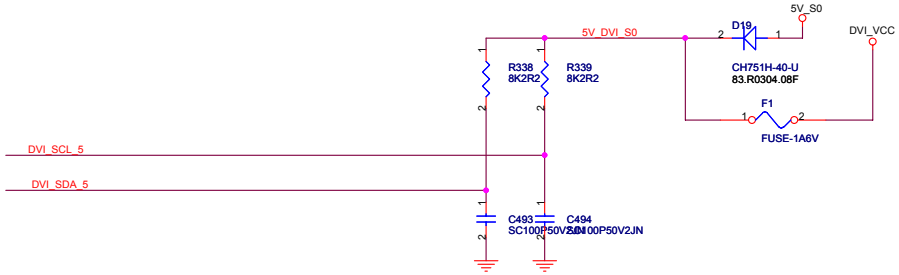
Date: Thursday, November 18, 2004 Sheet 12 of 56


Do not stuff when using M26
Do not stuff when using M26
U20D
PART 4 OF 6
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
RS480M-U
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C
Y
COMP
RED
GREEN
BLUE
DAC_VSYNC
DAC_HSYNC
RSET
DAC_SCL
DAC_SDA
PLLVDD
PLLVSS
HTPVDD
HTPVSS
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
SUS_STAT#
VDDR3_1
VDDR3_2
OSCIN
OSCOUT
TVCLKIN
DFT_GPIO0/RSV
DFT_GPIO1/RSV
DFT_GPIO2/RSV
DFT_GPIO3/RSV
DFT_GPIO4/RSV
DFT_GPIO5/RSV
BMREQb
I2C_CLK
I2C_DATA
THERMALDIODE_P
THERMALDIODE_N
TMDS_HPD
STRP_DATA
DDC_DATA
TESTMODE
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
GFX_CLKP
GFX_CLKN
HTTSTCLK
HTREFCLK
SB_CLKP
SB_CLKN
LVDDR18D
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LPVDD
LPVSS
1D8V_S0
3D3V_S0
AVDDQ
AVDD
PLVDD
HTPVDD
1D8VAVDDD1_S0
3D3VDDR_S0
LVDDR18D_S0
LVDDR18A_S0
1D8VLPVDD_S0
VCC_CORE_S0
R450 0R3-U
R86 0R3-U
R70 0R3-U
C90 SC1U10V3ZY
C89 SC1U10V3ZY
C605 SC1U10V3ZY
C590 SC1U10V3ZY
C604 SCD1U16V
R464 75R2F
R468 75R2F
R467 75R2F
R477 75R2F
R478 75R2F
R476 75R2F
R438 715R3F IRSET_NB
R502 0R2-0 VGA_CLK_DDC_NB
R517 0R2-0 VGA_DAT_DDC_NB
R101 BLM11A121S
C122 SC10U10V3ZY
C127 SCD1U16V
C123 SCD1U16V
R98 BLM11A121S
C113 SC10U10V3ZY
C705 SCD1U16V
C118 SCD1U16V
R514 0R3-U
C702 SC1U10V3ZY
R168 4K7R2
R124 0R2-0
R528 3KR2F
R497 3KR2F
R496 3KR2F
R105 0R2-0
R106 33R2
R107 33R2
R123 1KR2
R122 0R2-0
C121 DUMMY-C3
D28 RB751V-40-U
D27 RB751V-40-U
R516 4K7R2
R515 4K7R2
R503 DUMMY-R2
R504 4K7R2
R112 2KR2
R114 1KR2
C678 SCD1U16V
R113 2KR2
R485 BLM11A121S
R102 BLM11A121S
R85 BLM11A121S
C649 SC1U10V3ZY
C667 SCD1U16V
C117 SC1U10V3ZY
C124 SCD1U16V
C87 SC1U10V3ZY
C88 SCD1U16V
R505 3KR2F
R518 3KR2F
R519 3KR2F
R523 10KR2
U19A TSLCX08MTC-U
U19B TSLCX08MTC-U
U19C TSLCX08MTC-U
U19D TSLCX08MTC-U
U16 AT24C04N-10SI
TP93
TP96
TP99
TP100
TP85
TP86
TP87
TP88
TP89
TP90
TP91
TP9
TP8
TP7
TPAD28
TPAD30
DY
RESISTOR | RS480M MODE
R503 | TEST MODE
R504 | NORMAL MODE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
NB-RS480M_VIDEO/ CLOCK
Size A3
Document Number SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 13 of 56

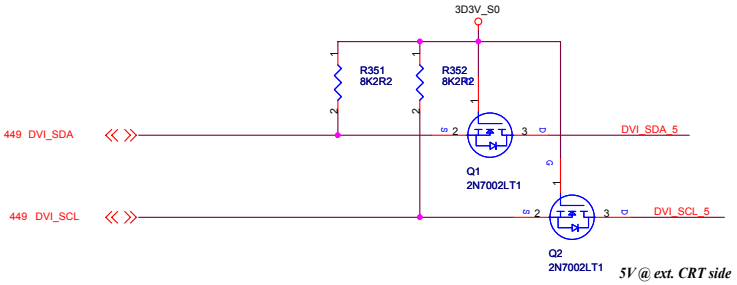


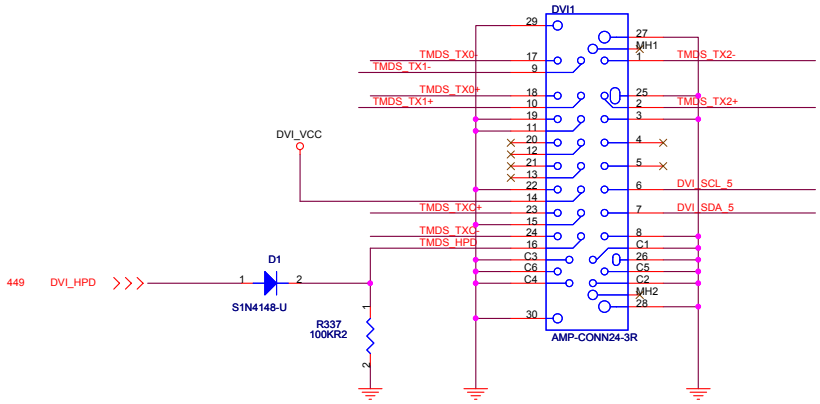
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: NB-RS480M_POWER	
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 14 of 56	





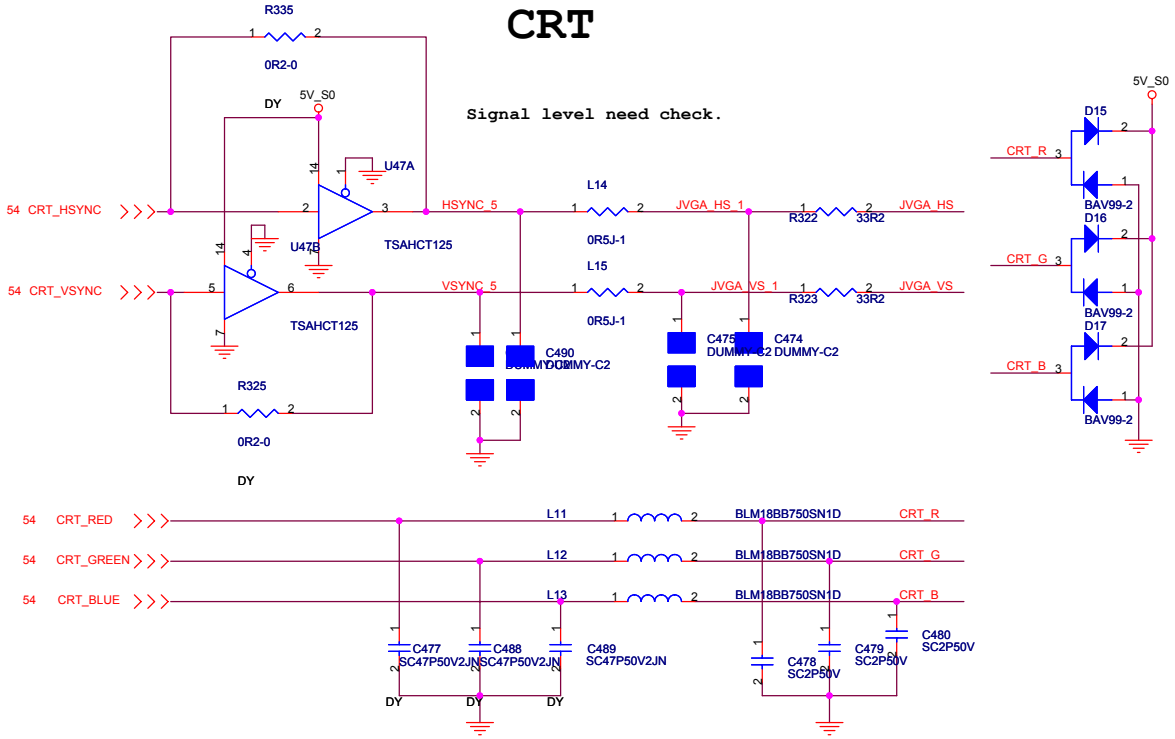
Do not stuff when using UMA





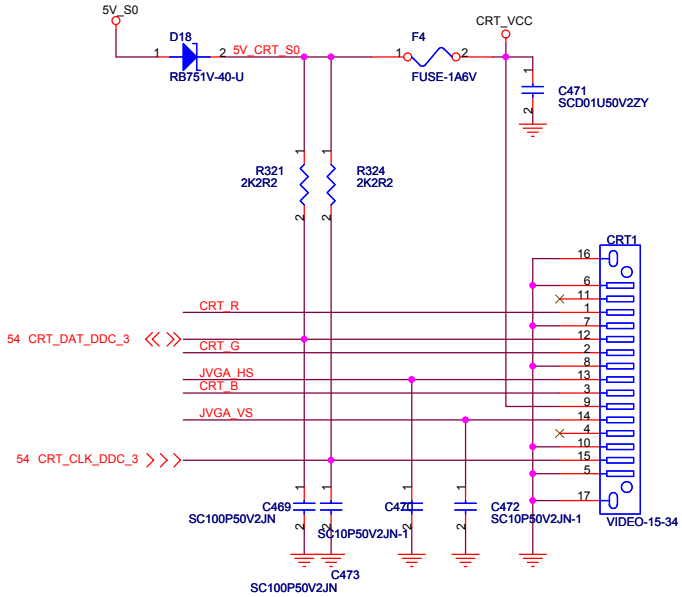
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DVI CONNECTOR		
Size: Custom	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 15 of 56	

CRT



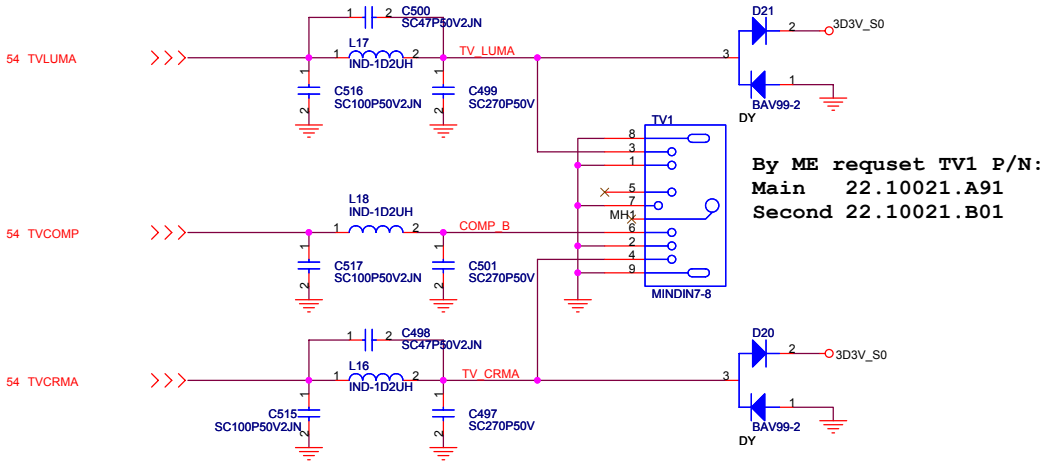
CRT CONN

200mA Rating/Spec 500mA

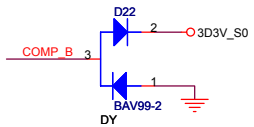


By ME requset CRT1 P/N:
Main 20.B0026.A15
Second 20.B0034.015

TV CONN

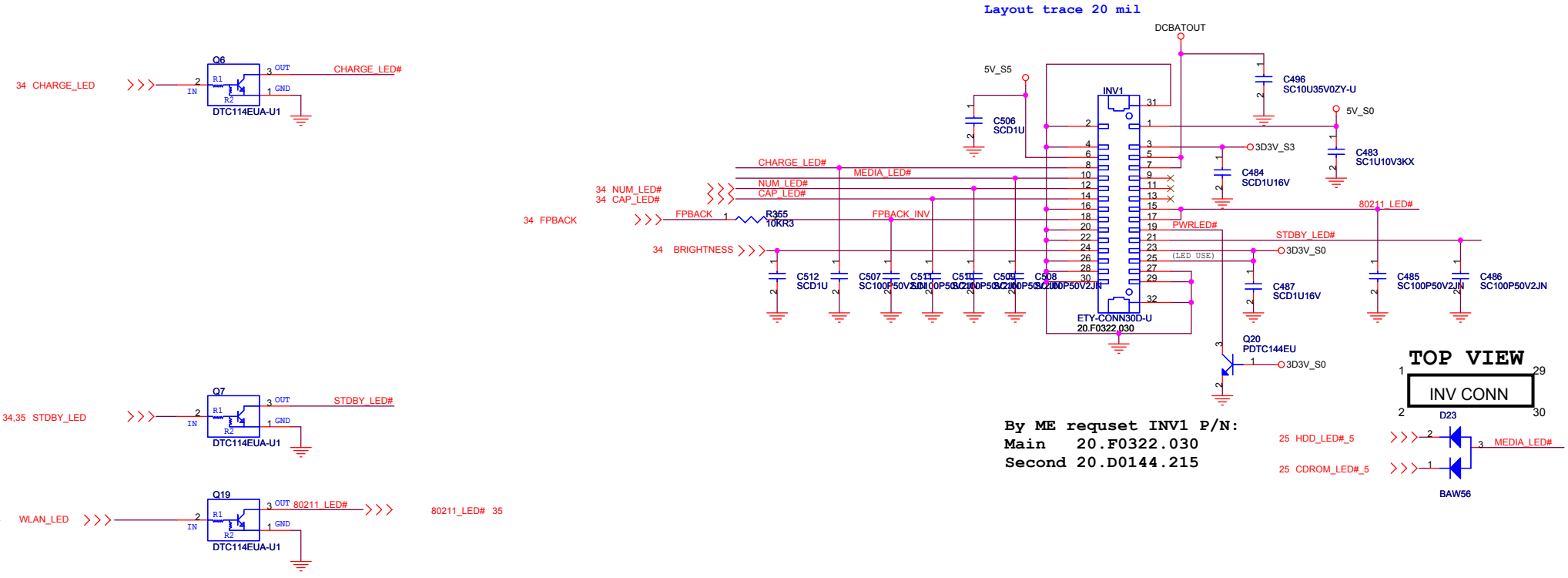


By ME requset TV1 P/N:
Main 22.10021.A91
Second 22.10021.B01

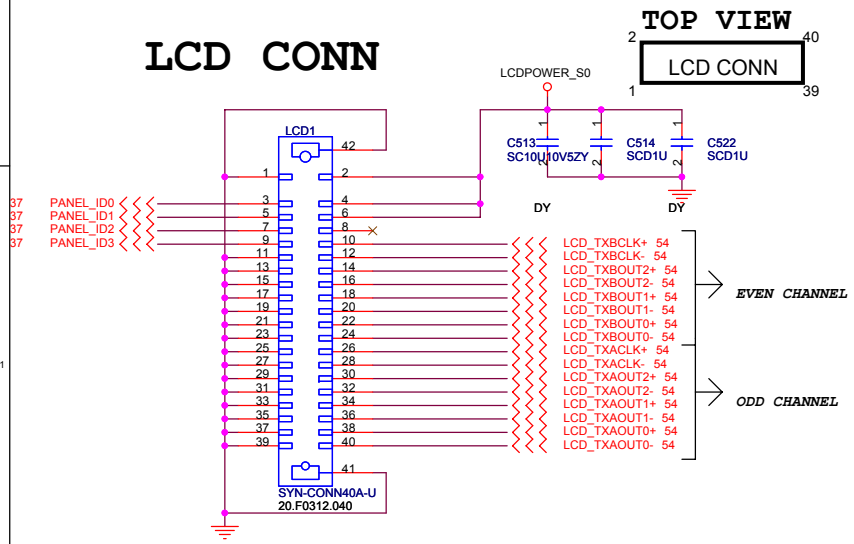


緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CRT / TV		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 16 of 56	

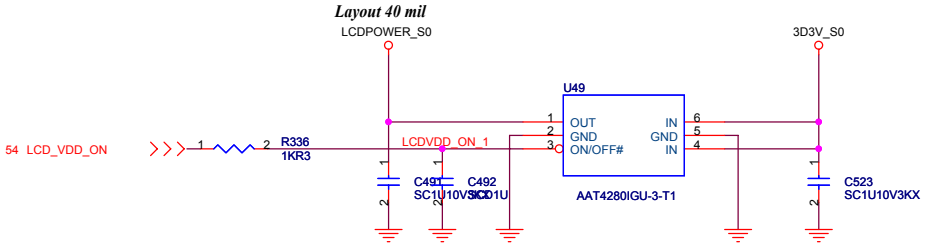
INVERTER/LED



LCD CONN

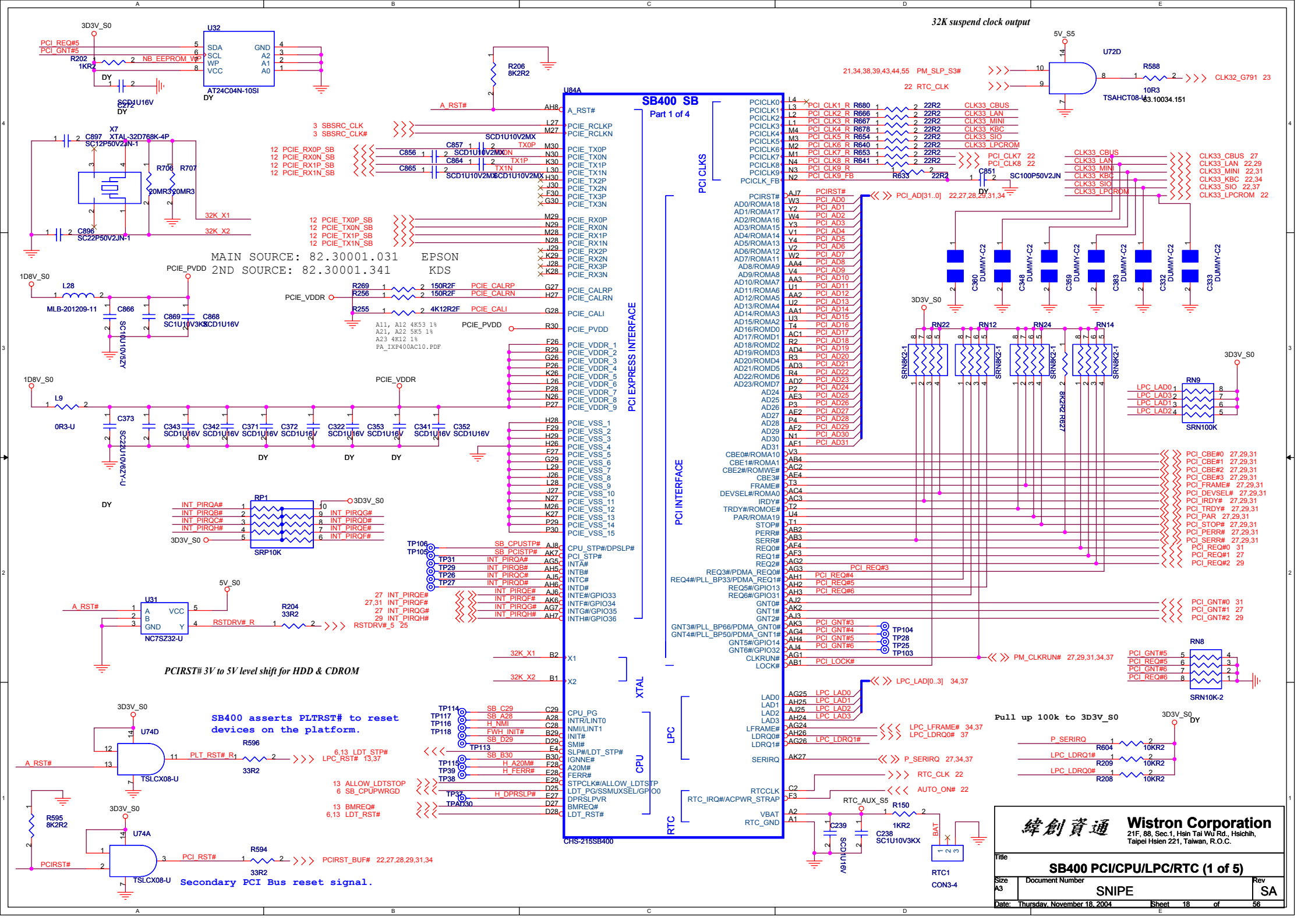


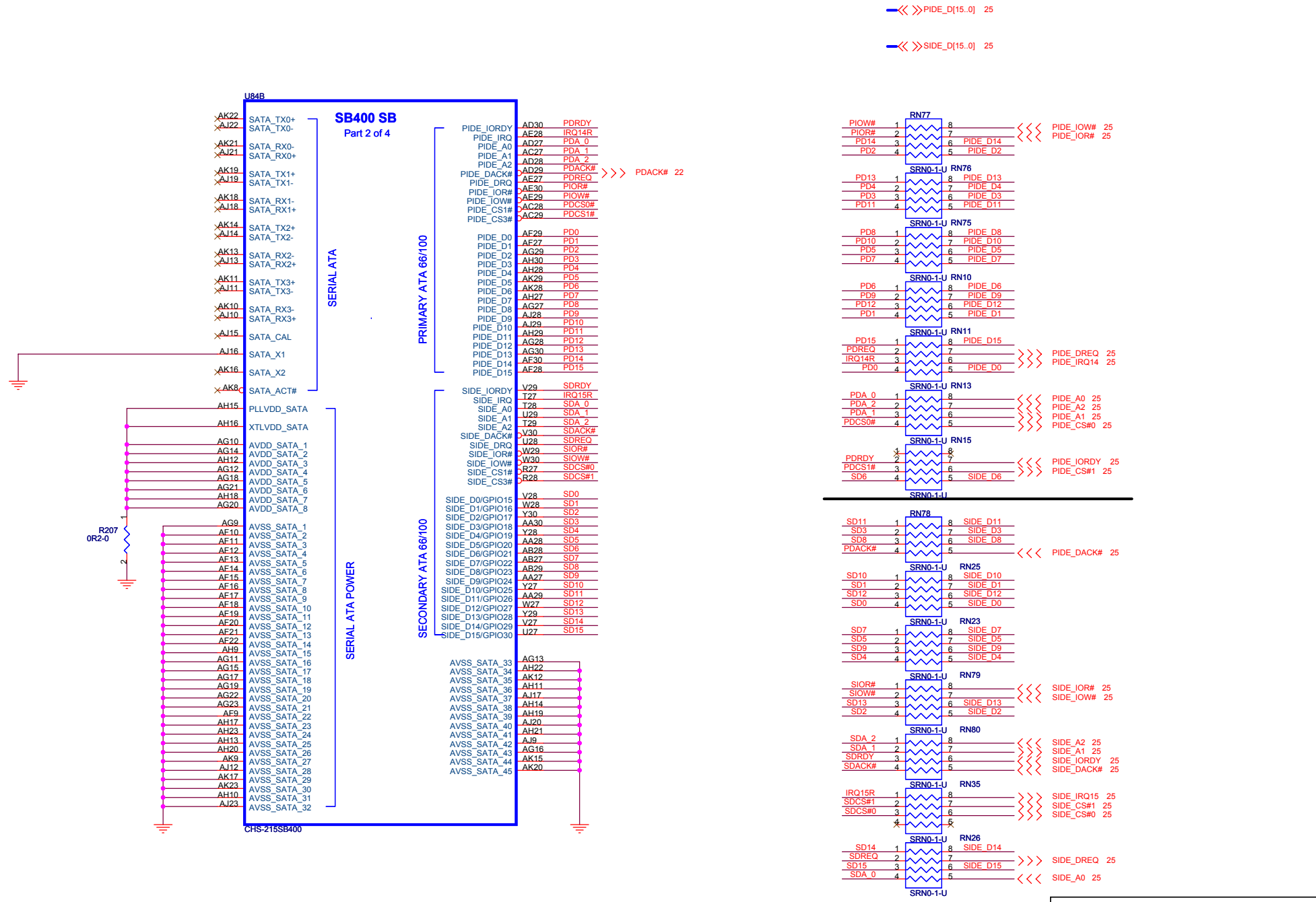
LCD POWER

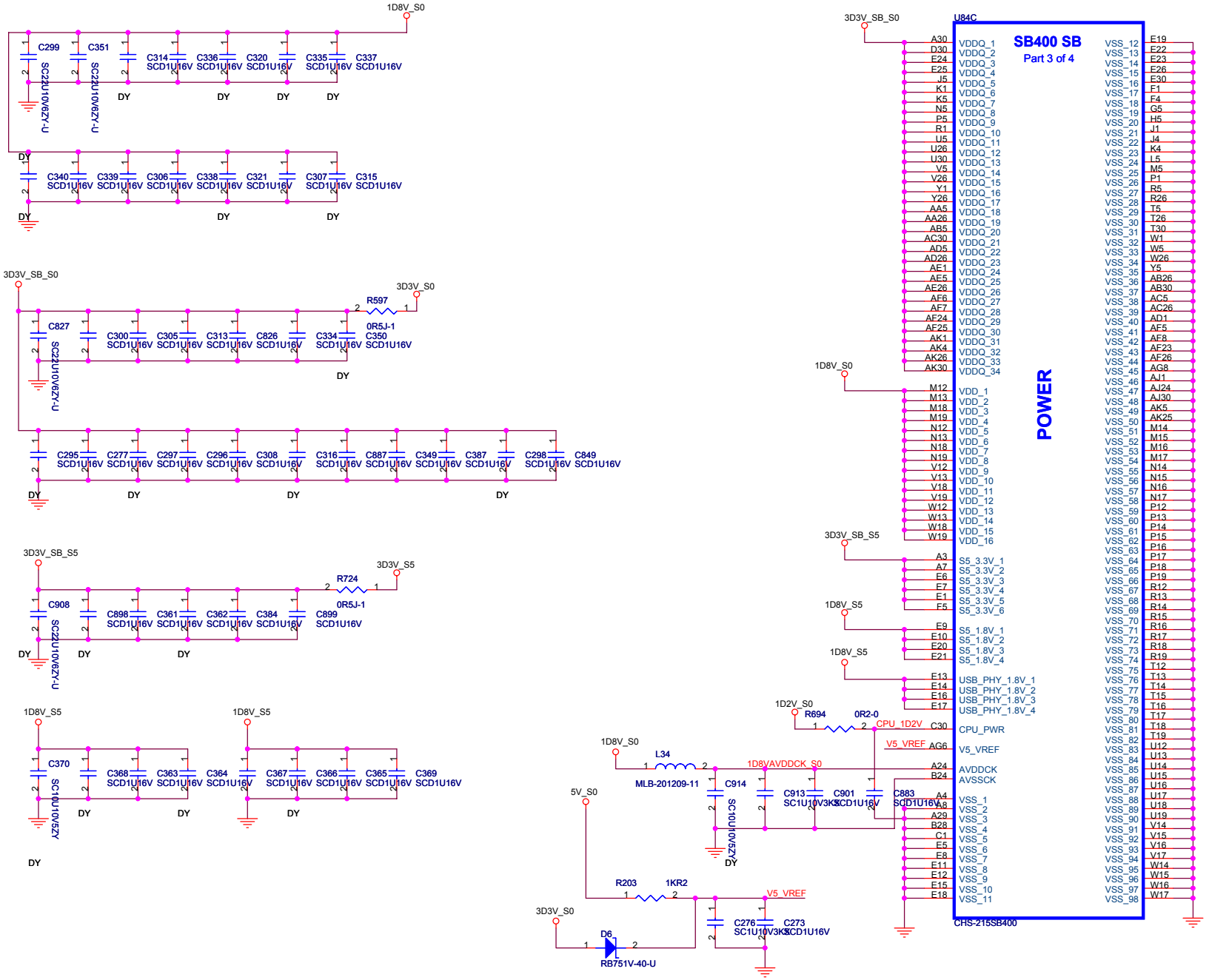


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INV / LCD	
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 17 of 56	

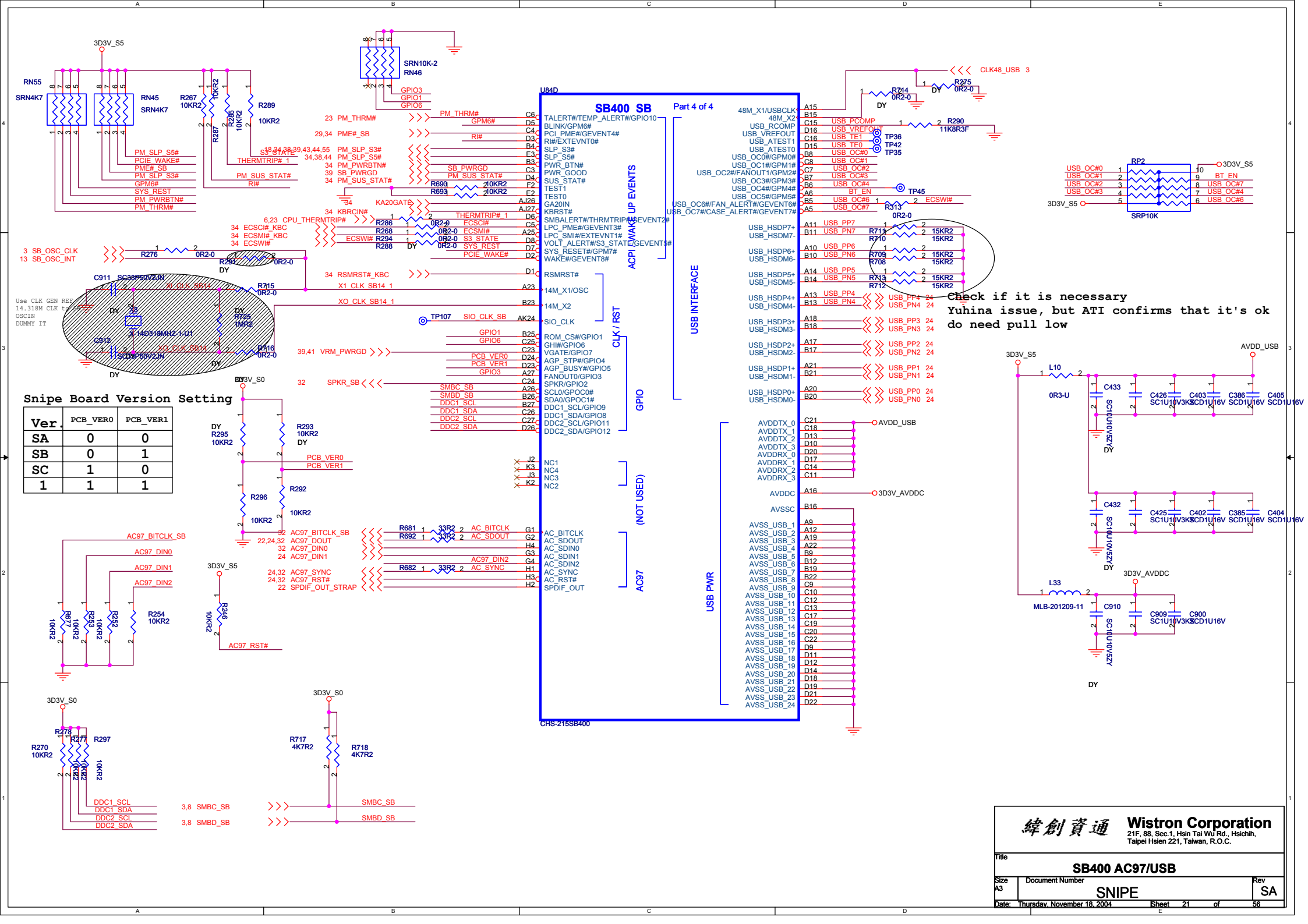

32K suspend clock output
SB400 SB
Part 1 of 4
U84A
MAIN SOURCE: 82.30001.031 EPSON
2ND SOURCE: 82.30001.341 KDS
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
XTAL
LPC
CPU
RTC
CHS-215SB400
PCIRST# 3V to 5V level shift for HDD & CDROM
SB400 asserts PLTRST# to reset devices on the platform.
Secondary PCI Bus reset signal.
Pull up 100k to 3D3V_S0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
SB400 PCI/CPU/LPC/RTC (1 of 5)
Size A3
Document Number SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 18 of 56

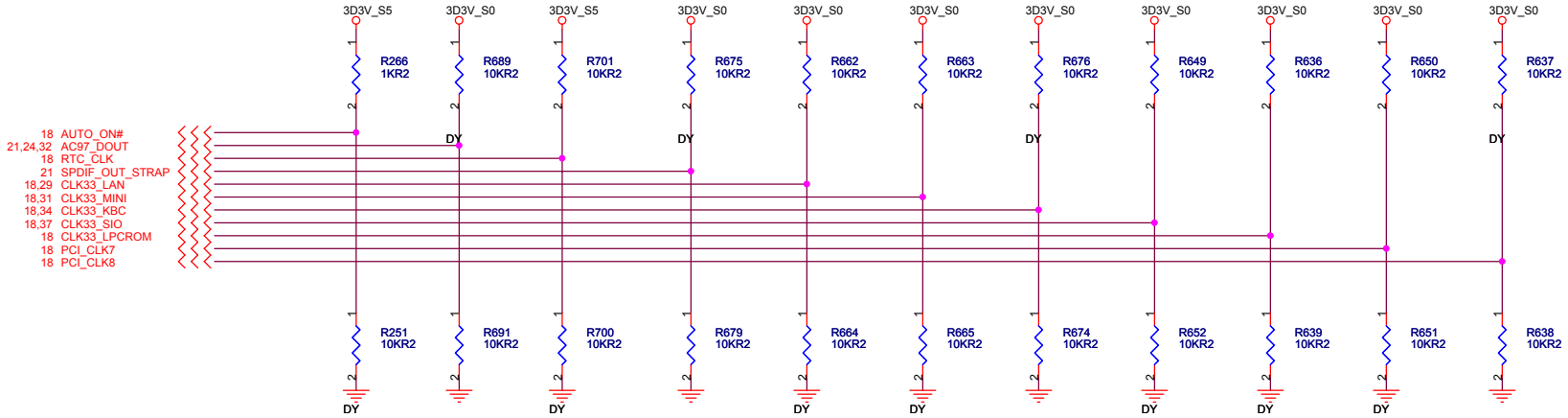

PIDE_D[15..0] 25
SIDE_D[15..0] 25
U84B
SB400 SB
Part 2 of 4
SERIAL ATA
SERIAL ATA POWER
PRIMARY ATA 66/100
SECONDARY ATA 66/100
SATA_TX0+
SATA_TX0-
SATA_RX0-
SATA_RX0+
SATA_TX1+
SATA_TX1-
SATA_RX1-
SATA_RX1+
SATA_TX2+
SATA_TX2-
SATA_RX2-
SATA_RX2+
SATA_TX3+
SATA_TX3-
SATA_RX3-
SATA_RX3+
SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#
PLLVDD_SATA
XTLVDD_SATA
AVDD_SATA_1
AVDD_SATA_2
AVDD_SATA_3
AVDD_SATA_4
AVDD_SATA_5
AVDD_SATA_6
AVDD_SATA_7
AVDD_SATA_8
AVSS_SATA_1
AVSS_SATA_2
AVSS_SATA_3
AVSS_SATA_4
AVSS_SATA_5
AVSS_SATA_6
AVSS_SATA_7
AVSS_SATA_8
AVSS_SATA_9
AVSS_SATA_10
AVSS_SATA_11
AVSS_SATA_12
AVSS_SATA_13
AVSS_SATA_14
AVSS_SATA_15
AVSS_SATA_16
AVSS_SATA_17
AVSS_SATA_18
AVSS_SATA_19
AVSS_SATA_20
AVSS_SATA_21
AVSS_SATA_22
AVSS_SATA_23
AVSS_SATA_24
AVSS_SATA_25
AVSS_SATA_26
AVSS_SATA_27
AVSS_SATA_28
AVSS_SATA_29
AVSS_SATA_30
AVSS_SATA_31
AVSS_SATA_32
CHS-215SB400
R207
0R2-0
PIDE_IORDY
PIDE_IRQ
PIDE_A0
PIDE_A1
PIDE_A2
PIDE_DACK#
PIDE_DRQ
PIDE_IOR#
PIDE_IOW#
PIDE_CS1#
PIDE_CS3#
PIDE_D0
PIDE_D1
PIDE_D2
PIDE_D3
PIDE_D4
PIDE_D5
PIDE_D6
PIDE_D7
PIDE_D8
PIDE_D9
PIDE_D10
PIDE_D11
PIDE_D12
PIDE_D13
PIDE_D14
PIDE_D15
PDACK# 22
SIDE_IORDY
SIDE_IRQ
SIDE_A0
SIDE_A1
SIDE_A2
SIDE_DACK#
SIDE_DRQ
SIDE_IOR#
SIDE_IOW#
SIDE_CS1#
SIDE_CS3#
SIDE_D0/GPIO15
SIDE_D1/GPIO16
SIDE_D2/GPIO17
SIDE_D3/GPIO18
SIDE_D4/GPIO19
SIDE_D5/GPIO20
SIDE_D6/GPIO21
SIDE_D7/GPIO22
SIDE_D8/GPIO23
SIDE_D9/GPIO24
SIDE_D10/GPIO25
SIDE_D11/GPIO26
SIDE_D12/GPIO27
SIDE_D13/GPIO28
SIDE_D14/GPIO29
SIDE_D15/GPIO30
AVSS_SATA_33
AVSS_SATA_34
AVSS_SATA_35
AVSS_SATA_36
AVSS_SATA_37
AVSS_SATA_38
AVSS_SATA_39
AVSS_SATA_40
AVSS_SATA_41
AVSS_SATA_42
AVSS_SATA_43
AVSS_SATA_44
AVSS_SATA_45
RN77
RN76
RN75
RN10
RN11
RN13
RN15
RN78
RN25
RN23
RN79
RN80
RN35
RN26
SRN0-1-U
PIOW# PIOR# PD14 PD2
PD13 PD4 PD3 PD11
PD8 PD10 PD5 PD7
PD6 PD9 PD12 PD1
PD15 PDREQ IRQ14R PD0
PDA_0 PDA_2 PDA_1 PDCS0#
PDRDY PDCS1# SD6
SD11 SD3 SD8 PDACK#
SD10 SD1 SD12 SD0
SD7 SD5 SD9 SD4
SIOR# SIOW# SD13 SD2
SDA_2 SDA_1 SDRDY SDACK#
IRQ15R SDCS#1 SDCS#0
SD14 SDREQ SD15 SDA_0
PIDE_IOW# 25
PIDE_IOR# 25
PIDE_D14
PIDE_D2
PIDE_D13
PIDE_D4
PIDE_D3
PIDE_D11
PIDE_D8
PIDE_D10
PIDE_D5
PIDE_D7
PIDE_D6
PIDE_D9
PIDE_D12
PIDE_D1
PIDE_DREQ 25
PIDE_IRQ14 25
PIDE_D0
PIDE_D15
PIDE_A0 25
PIDE_A2 25
PIDE_A1 25
PIDE_CS#0 25
PIDE_IORDY 25
PIDE_CS#1 25
PIDE_D6
SIDE_D11
SIDE_D3
SIDE_D8
PIDE_DACK# 25
SIDE_D10
SIDE_D1
SIDE_D12
SIDE_D0
SIDE_D7
SIDE_D5
SIDE_D9
SIDE_D4
SIDE_IOR# 25
SIDE_IOW# 25
SIDE_D13
SIDE_D2
SIDE_A2 25
SIDE_A1 25
SIDE_IORDY 25
SIDE_DACK# 25
SIDE_IRQ15 25
SIDE_CS#1 25
SIDE_CS#0 25
SIDE_D14
SIDE_D15
SIDE_DREQ 25
SIDE_A0 25
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
SB400 ACPI/GPIO/SATA/IDE (2 of 5)
Size
A3
Document Number
SNIPE
Rev
SA
Date: Thursday, November 18, 2004
Sheet 19 of 56



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

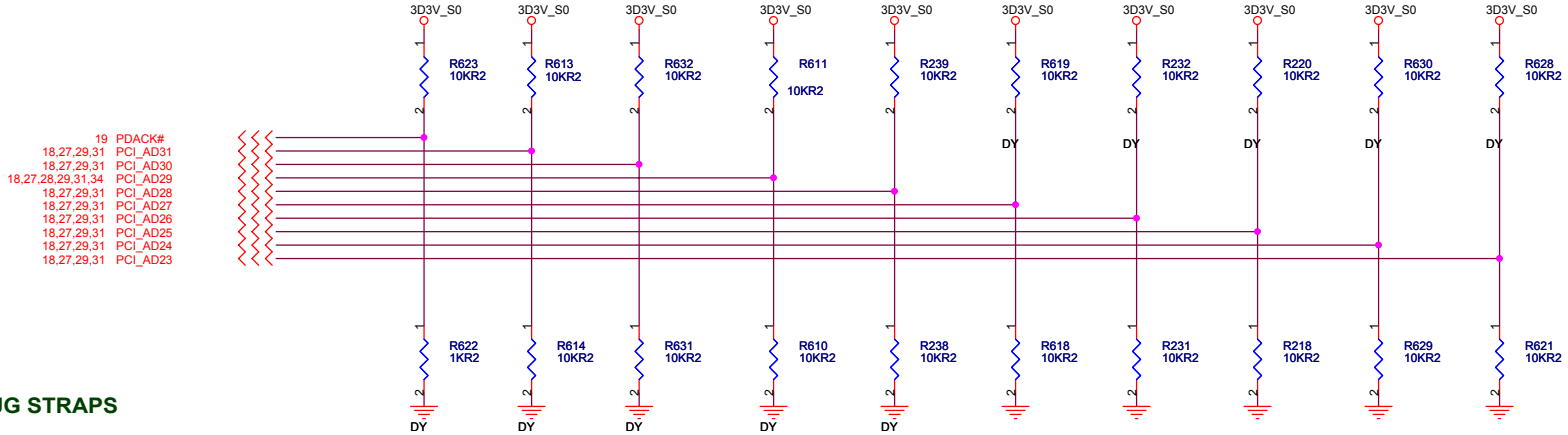
Title: SB400 POWER/DECOUPLING		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 20 of 56	


SB400 SB
Part 4 of 4
U84D
CHS-215SB400
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
(NOT USED)
AC97
USB INTERFACE
USB PWR
Snipe Board Version Setting
Ver. PCB_VER0 PCB_VER1
SA 0 0
SB 0 1
SC 1 0
1 1 1
Check if it is necessary
Yuhina issue, but ATI confirms that it's ok
do need pull low
Use CLK GEN REF 14.318M CLK to SB OSCIN
DUMMY IT
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
SB400 AC97/USB
Size A3
Document Number SNIPE
Rev SA
Date: Thursday, November 18, 2004
Sheet 21 of 56



REQUIRED SYSTEM STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7 PCI_CLK8
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	48MHZ-Clock Input Buffer DEFAULT	USB PHY PWRDOWN DISABLE DEFAULT	USB INT PLL48 DEFAULT	14MHZ OSC MODE DEFAULT	CPU I/F=K8 DEFAULT	ROM TYPE H,H=PCI (X Bus) ROM H,L=LPC ROM I
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTENNAL RTC (NOT SUPPORTED W/IT8712)	SIO 48MHz DEFAULT	48MHZ -Crytsal Pad	USB PHY PWRDOWN ENABLE	USB EXT. 48MHZ	14MHZ XTAL MODE	CPU I/F=P4	L,H=LPC ROM II L,L=Firmware Hub ROM



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
STRAP HIGH	USE LONG RESET DEFAULT	RESERVED	RESERVED	RESERVED	RESERVED	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	RESERVED
STRAP LOW	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	

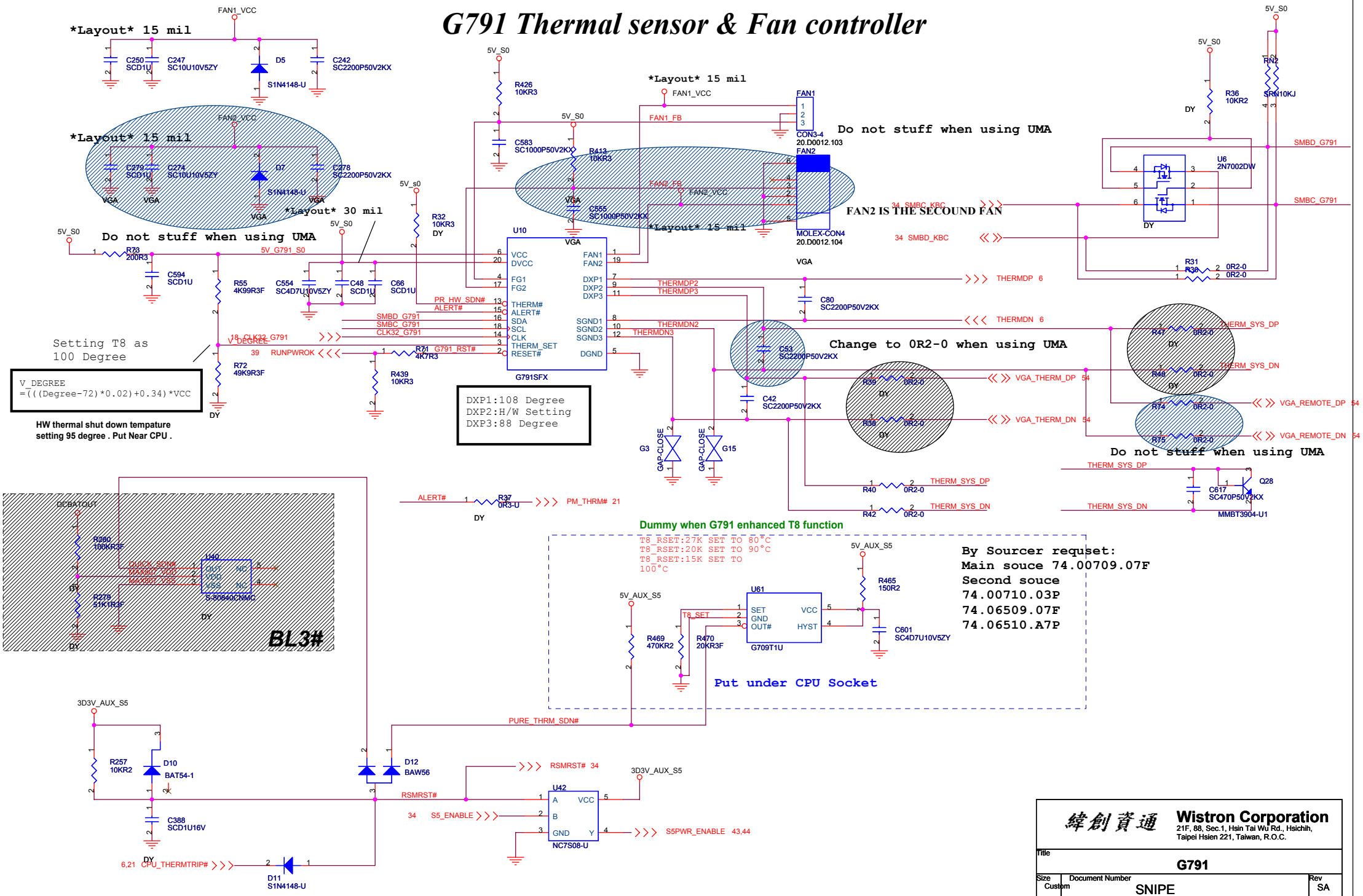
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB400 STRAPPING PIN

Size: A3 | Document Number: SNIPE | Rev: SA

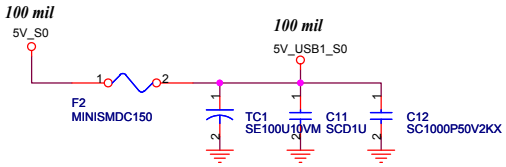
Date: Thursday, November 18, 2004 | Sheet 22 of 56

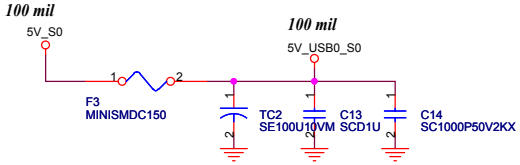
G791 Thermal sensor & Fan controller



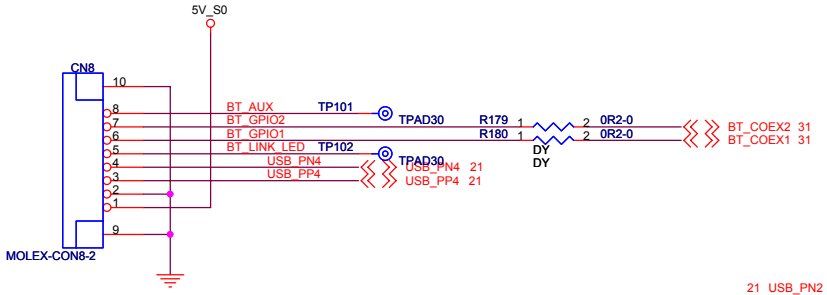
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	G791
Size: Custom	Document Number: SNIPE — Rev: SA
Date: Thursday, November 18, 2004	Sheet 23 of 56

USB PORT

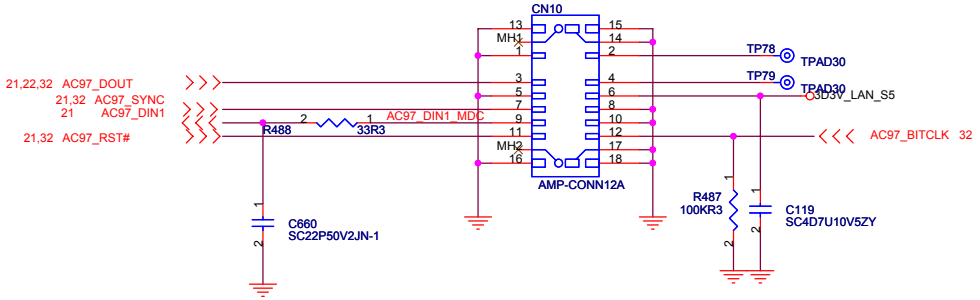


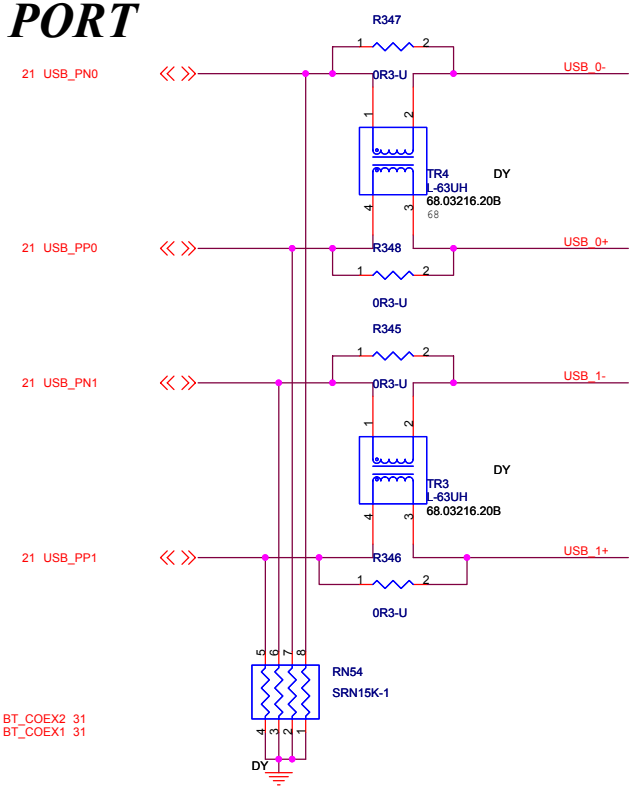


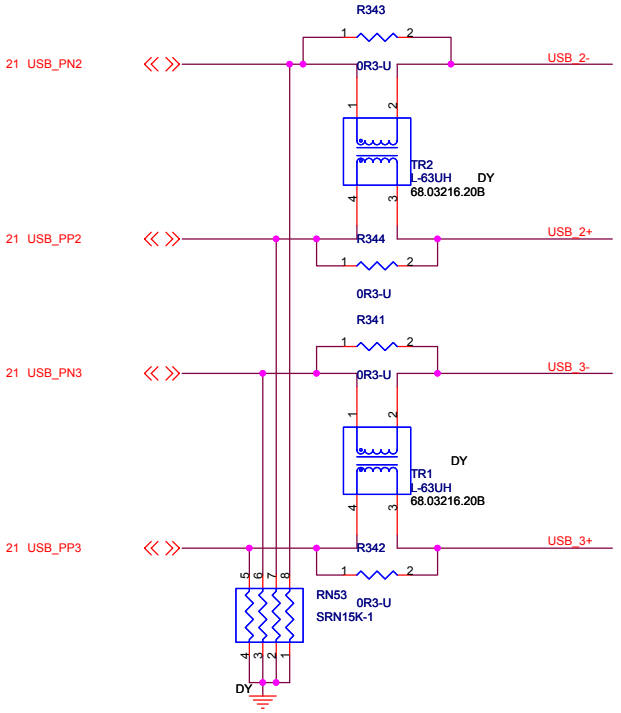
BLUETOOTH MODULE CONNECTOR

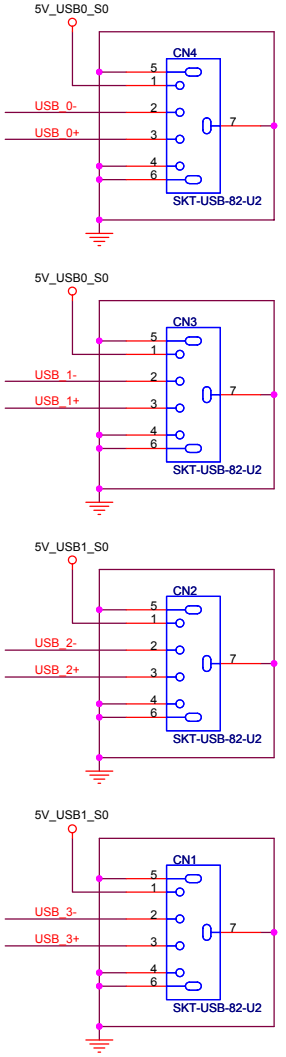


MDC 1.5 CONNECTOR









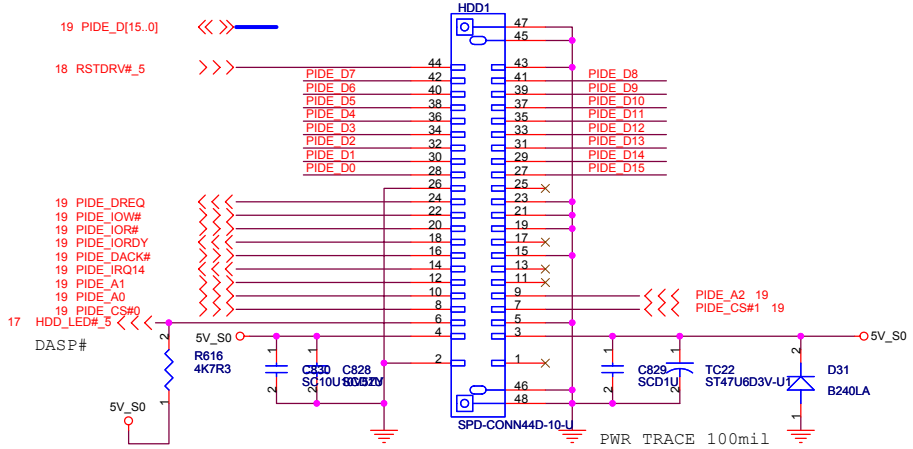
By Sourcer requset change P/N:
From 22.10218.701
To 22.10218.F51

By ME requset P/N:
Main 22.10218.F51
Second 22.10218.F41

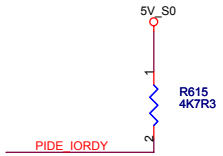
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB and MDC		
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 24 of 56	

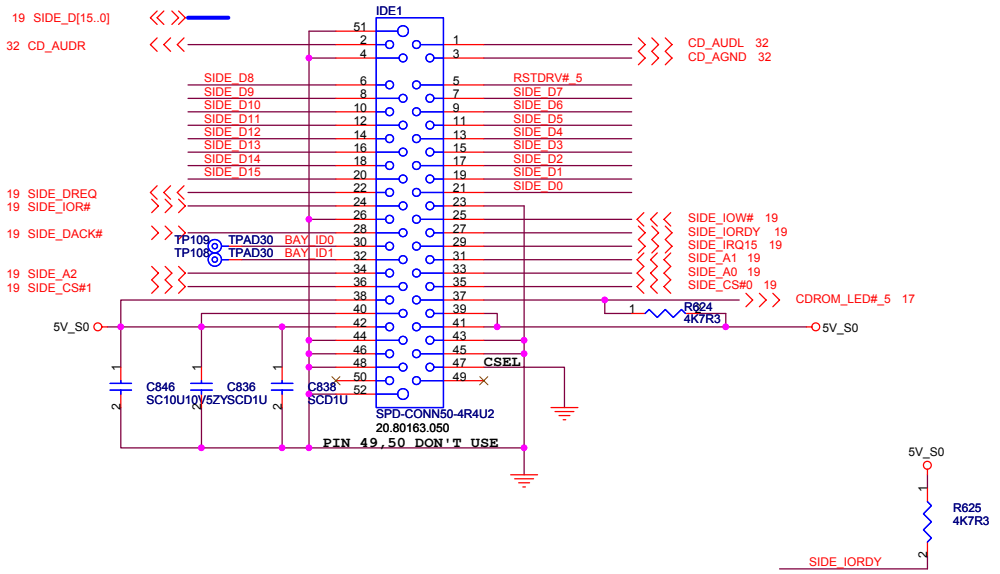
HDD



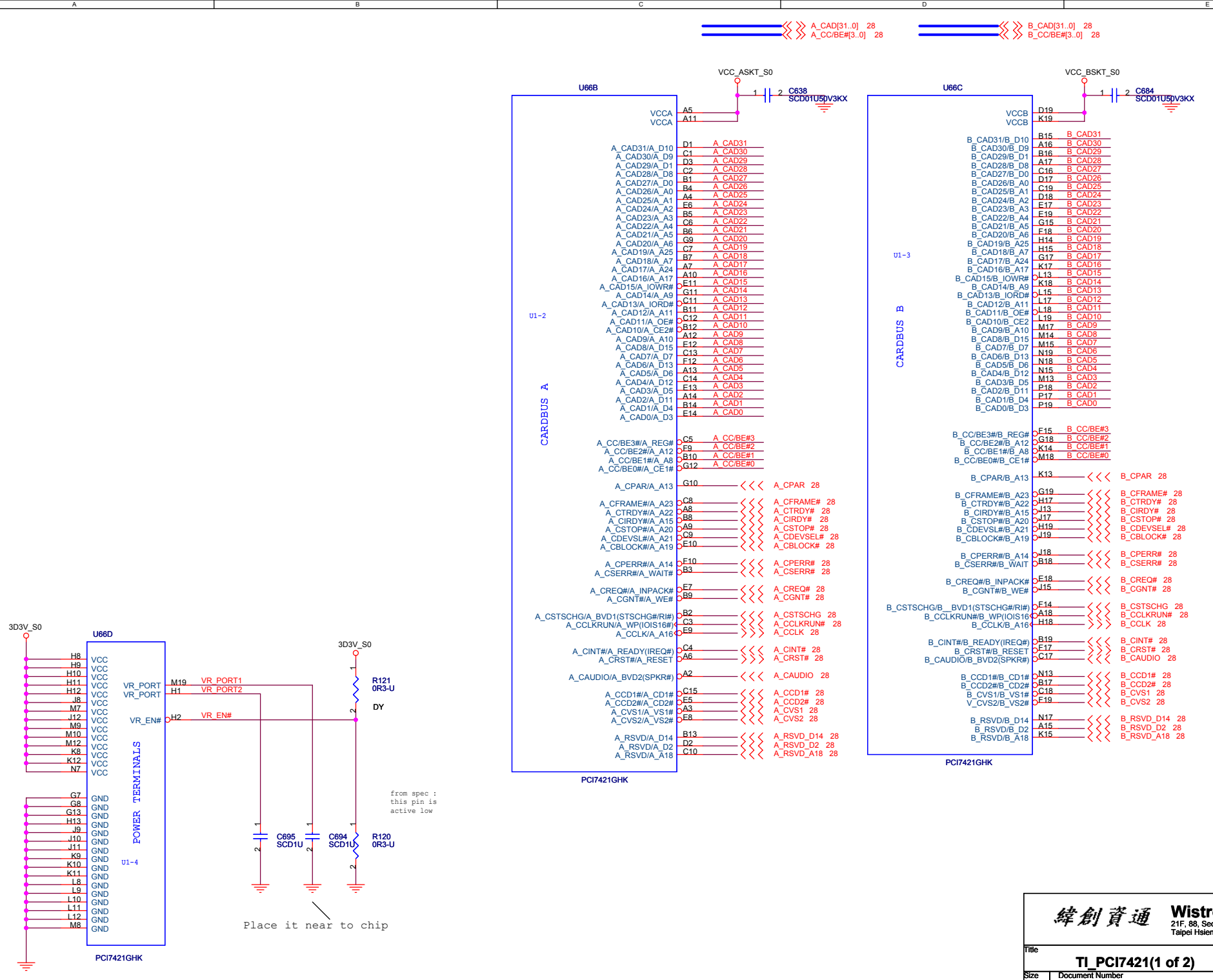
By ME requset change P/N:
from 20.F0385.044
to 20.F0385.A44



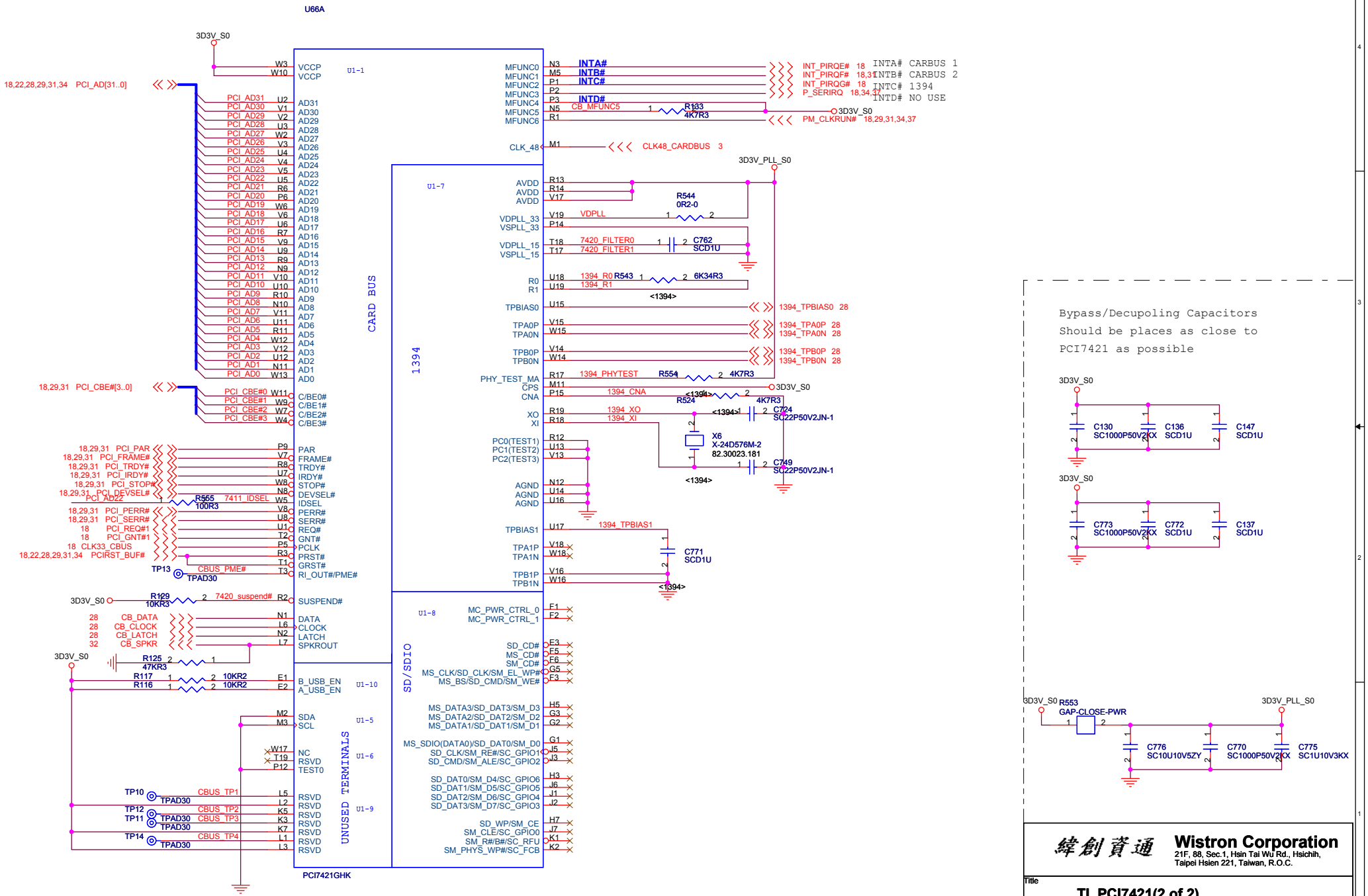
CDROM



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDD / CDROM**	
Size A3	Document Number **SNIPE**	Rev SA
Date: Thursday, November 18, 2004	Sheet 25 of 56	



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: TI_PCI7421(1 of 2)	
Size: A3	Document Number: SNIPE
Rev: SA	
Date: Thursday, November 18, 2004	Sheet 26 of 56



Title	TI_PCI7421(2 of 2)
Size	A3
Document Number	SNIPE
Rev	SA
Date:	Thursday, November 18, 2004
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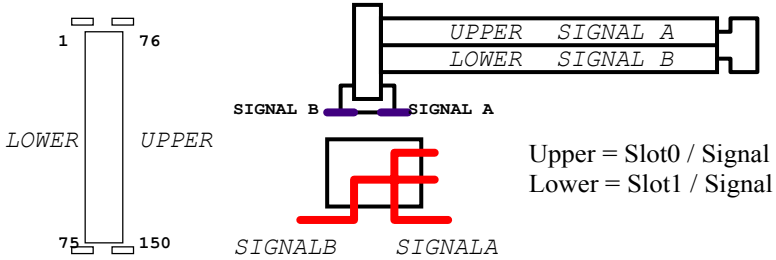
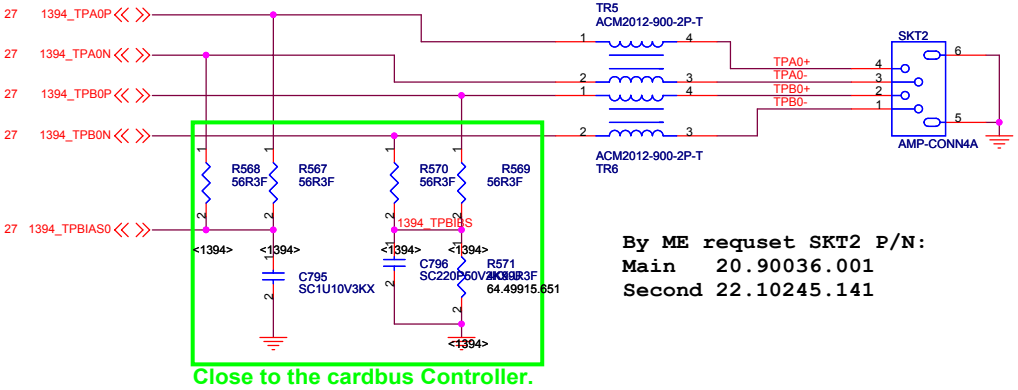
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

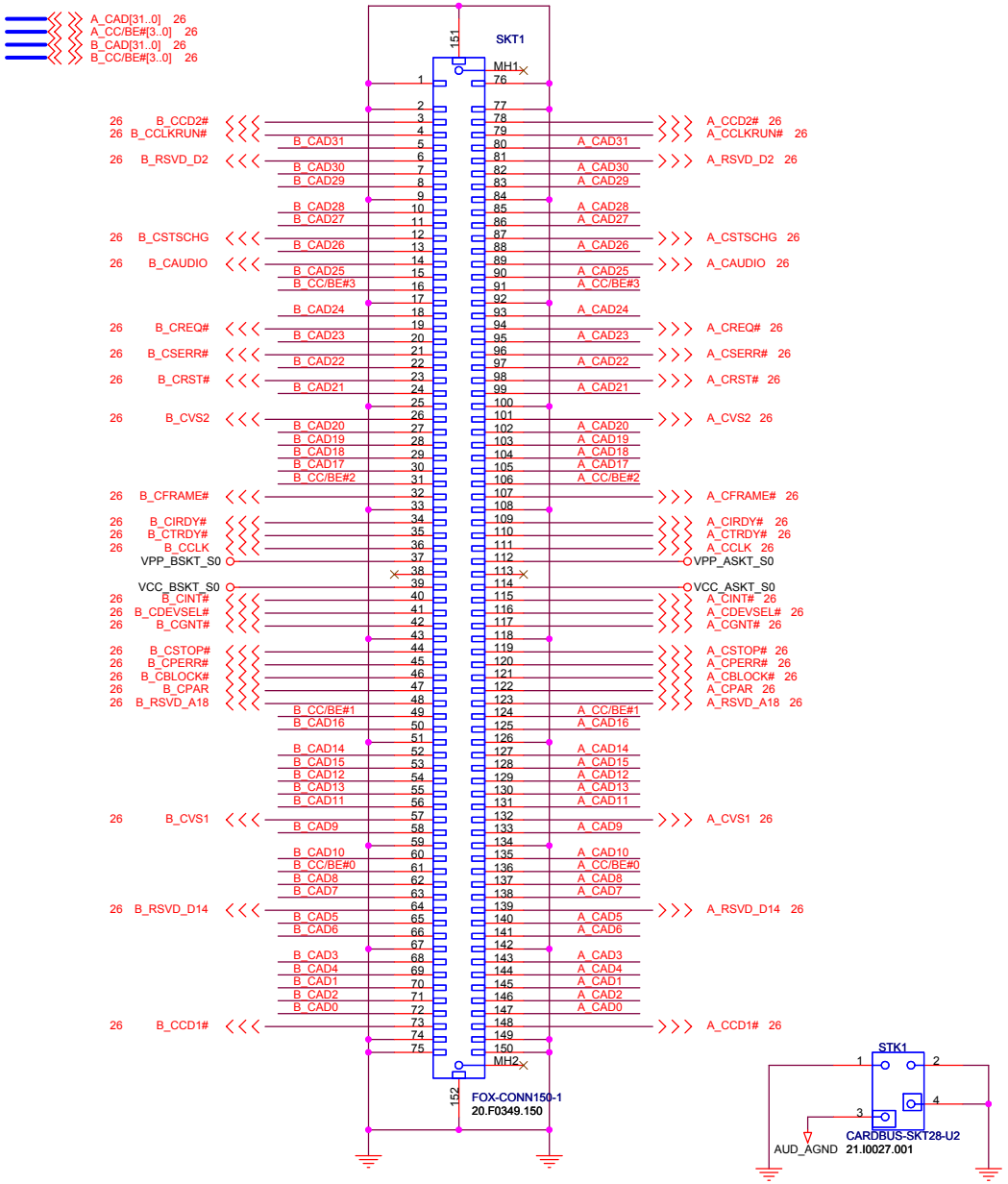


Upper = Slot0 / Signal A = Conn B
Lower = Slot1 / Signal B = Conn A

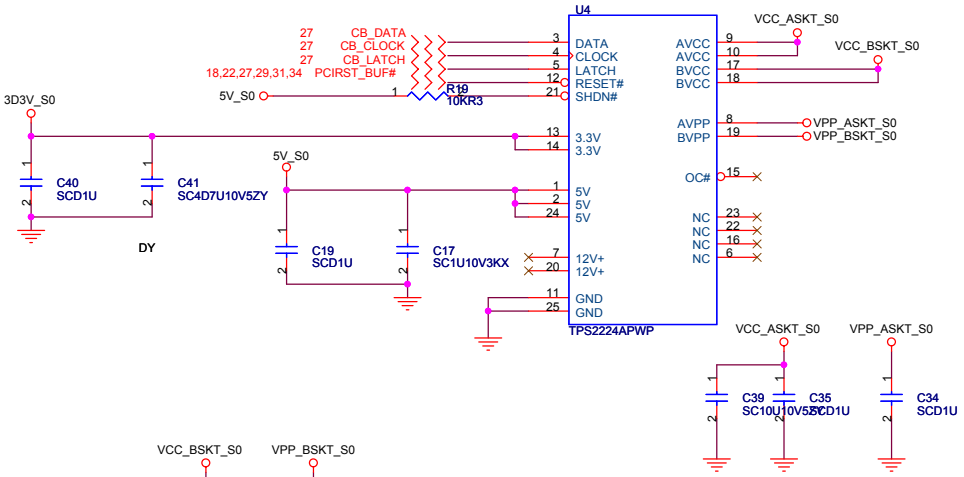
1394 Connector



By ME requset SKT2 P/N:
Main 20.90036.001
Second 22.10245.141



Power switch



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PCMCA SLOT_1394 CONN
Size: A3 | Document Number: SNIPE | Rev: SA
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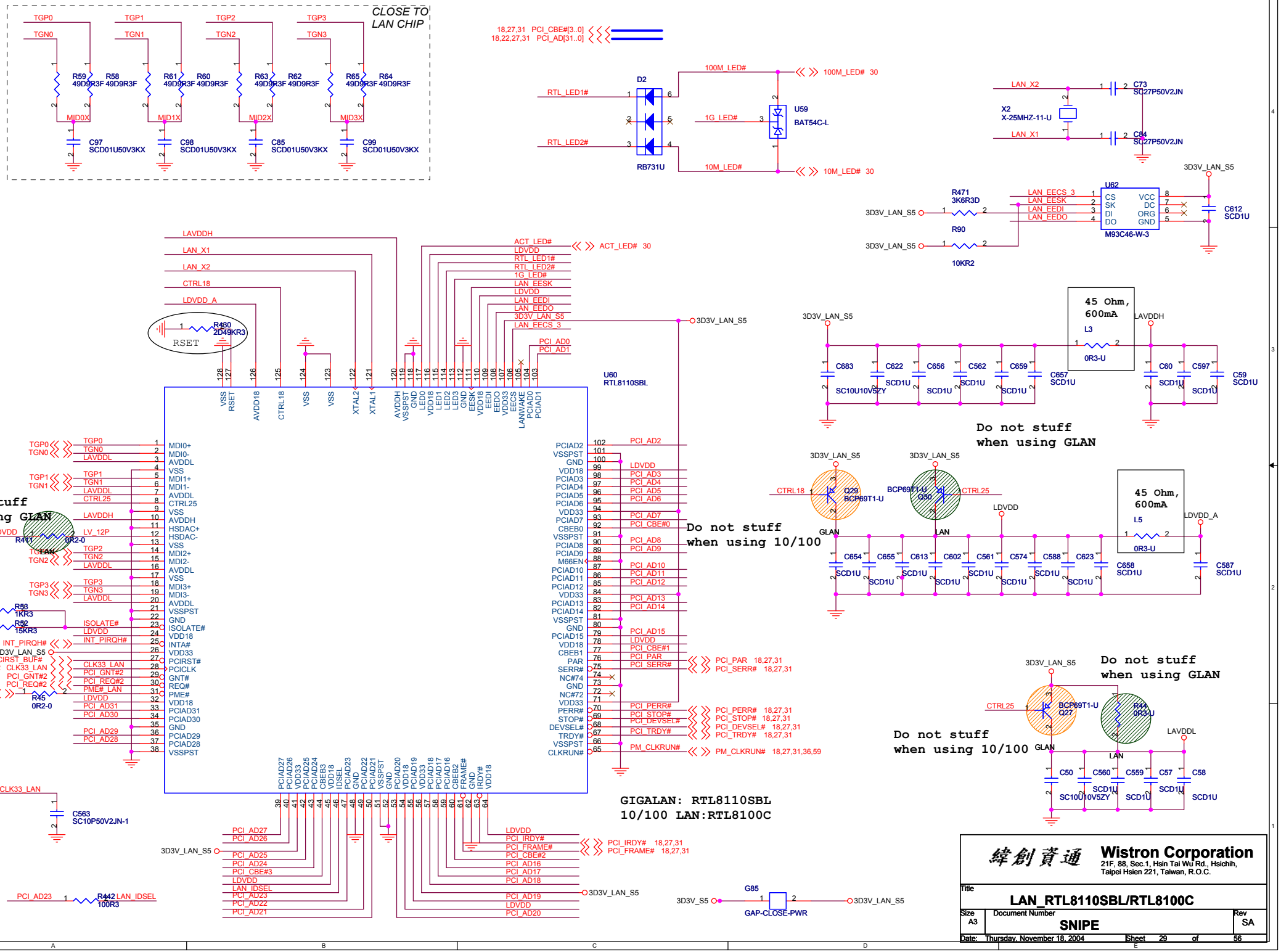
CLOSE TO LAN CHIP
TGP0
TGN0
TGP1
TGN1
TGP2
TGN2
TGP3
TGN3
R59 49D9R3F
R58 49D9R3F
R61 49D9R3F
R60 49D9R3F
R63 49D9R3F
R62 49D9R3F
R65 49D9R3F
R64 49D9R3F
MID0X
MID1X
MID2X
MID3X
C97 SCD01U50V3KX
C98 SCD01U50V3KX
C85 SCD01U50V3KX
C99 SCD01U50V3KX
18,27,31 PCI_CBE#[3..0]
18,22,27,31 PCI_AD[31..0]
D2
RTL_LED1#
RTL_LED2#
100M_LED#
1G_LED#
10M_LED#
RB731U
U59
BAT54C-L
100M_LED# 30
10M_LED# 30
LAN_X2
LAN_X1
X2
X-25MHZ-11-U
C73 SC27P50V2JN
C84 SC27P50V2JN
3D3V_LAN_S5
R471 3K6R3D
R90
10KR2
LAN_EECS_3
LAN_EESK
LAN_EEDI
LAN_EEDO
U62
CS
SK
DI
DO
VCC
DC
ORG
GND
M93C46-W-3
C612 SCD01U
LAVDDH
LAN_X1
LAN_X2
CTRL18
LDVDD_A
R430 2D49KR3
RSET
ACT_LED#
LDVDD
RTL_LED1#
RTL_LED2#
1G_LED#
LAN_EESK
LAN_EEDI
LAN_EEDO
3D3V_LAN_S5
LAN_EECS_3
PCI_AD0
PCI_AD1
ACT_LED# 30
U60
RTL8110SBL
VSS
RSET
AVDD18
CTRL18
XTAL2
XTAL1
AVDDH
VSSPST
GND
LED0
VDD18
LED1
LED2
LED3
EESK
EEDI
EEDO
VDD33
EECS
LANWAKE
PCIAD0
PCIAD1
MDI0+
MDI0-
MDI1+
MDI1-
CTRL25
HSDAC+
HSDAC-
MDI2+
MDI2-
MDI3+
MDI3-
ISOLATE#
INTA#
VDD33
PCIRST#
PCICLK
GNT#
REQ#
PME#
PCIAD31
PCIAD30
PCIAD29
PCIAD28
PCIAD2
PCIAD3
PCIAD4
PCIAD5
PCIAD6
PCIAD7
CBEB0
M66EN
PCIAD10
PCIAD11
PCIAD12
PCIAD13
PCIAD14
PCIAD15
CBEB1
PAR
SERR#
NC#74
NC#72
PERR#
STOP#
DEVSEL#
TRDY#
CLKRUN#
PCI_AD2
PCI_AD3
PCI_AD4
PCI_AD5
PCI_AD6
PCI_AD7
PCI_CBE#0
PCI_AD8
PCI_AD9
PCI_AD10
PCI_AD11
PCI_AD12
PCI_AD13
PCI_AD14
PCI_AD15
PCI_CBE#1
PCI_PAR
PCI_SERR#
PCI_PERR#
PCI_STOP#
PCI_DEVSEL#
PCI_TRDY#
PM_CLKRUN#
PCI_PAR 18,27,31
PCI_SERR# 18,27,31
PCI_PERR# 18,27,31
PCI_STOP# 18,27,31
PCI_DEVSEL# 18,27,31
PCI_TRDY# 18,27,31
PM_CLKRUN# 18,27,31,36,59
Do not stuff when using 10/100
Do not stuff when using GLAN
LV_12P
R411 0R2-0
LAN
TGP0
TGN0
TGP1
TGN1
TGP2
TGN2
TGP3
TGN3
LAVDDL
CTRL25
LAVDDH
3D3V_S0
R53 1KR3
R52 15KR3
INT_PIRQH#
3D3V_LAN_S5
18,27,28,31,59 PCIRST_BUF#
18,22 CLK33_LAN
18 PCI_GNT#2
18 PCI_REQ#2
21,59 PME#_SB
R45 0R2-0
LDVDD
PCI_AD31
PCI_AD30
PCI_AD29
PCI_AD28
CLK33_LAN
C563 SC10P50V2JN-1
PCI_AD23
R442 100R3
LAN_IDSEL
PCIAD27
PCIAD26
PCIAD25
PCIAD24
CBEB3
PCIAD23
PCIAD22
PCIAD21
PCIAD20
PCIAD19
PCIAD18
PCIAD17
PCIAD16
CBEB2
FRAME#
IRDY#
PCI_AD27
PCI_AD26
PCI_AD25
PCI_AD24
PCI_CBE#3
PCI_AD23
PCI_AD22
PCI_AD21
PCI_IRDY# 18,27,31
PCI_FRAME# 18,27,31
PCI_IRDY#
PCI_FRAME#
PCI_CBE#2
PCI_AD16
PCI_AD17
PCI_AD18
PCI_AD19
PCI_AD20
GIGALAN: RTL8110SBL
10/100 LAN:RTL8100C
G85
GAP-CLOSE-PWR
3D3V_S5
45 Ohm, 600mA
L3
0R3-U
C683 SC10U10V5ZY
C622 SCD1U
C656 SCD1U
C562 SCD1U
C659 SCD1U
C657 SCD1U
C60 SCD1U
C597 SCD1U
C59 SCD1U
Do not stuff when using GLAN
CTRL18
CTRL25
Q29 BCP69T1-U
Q30 BCP69T1-U
GLAN
LAN
LDVDD
LDVDD_A
45 Ohm, 600mA
L5
0R3-U
C654 SCD1U
C655 SCD1U
C613 SCD1U
C602 SCD1U
C561 SCD1U
C574 SCD1U
C588 SCD1U
C623 SCD1U
C658 SCD1U
C587 SCD1U
Do not stuff when using 10/100
Do not stuff when using GLAN
Q27 BCP69T1-U
R44 0R3-U
C50 SC10U10V5ZY
C560 SCD1U
C559 SCD1U
C57 SCD1U
C58 SCD1U
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LAN_RTL8110SBL/RTL8100C
Size A3
Document Number SNIPE
Rev SA
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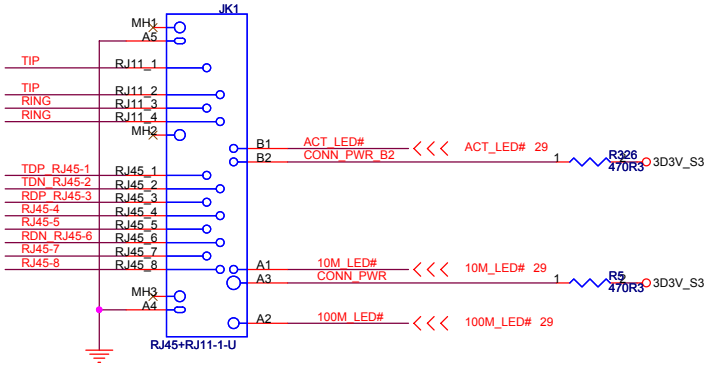
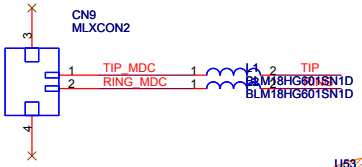
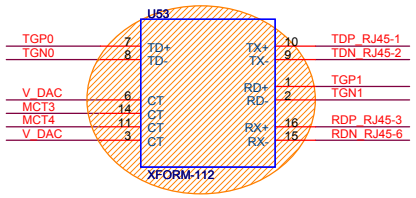
Link: Green - 10Mbps/802.11b Activity: Yellow
Orange - 100Mbps/802.11a
Yellow - 1Gbps



By ME requset for
10/100 LAN change P/N:
From 22.10177.621
To 22.10177.731
By ME requset for
GigaLAN JK1 P/N:
Main 22.10177.601
Second 22.10245.771
By ME requset change P/N:
From 20.D0121.102
To 21.D0010.102



Do not stuff
when using GLAN



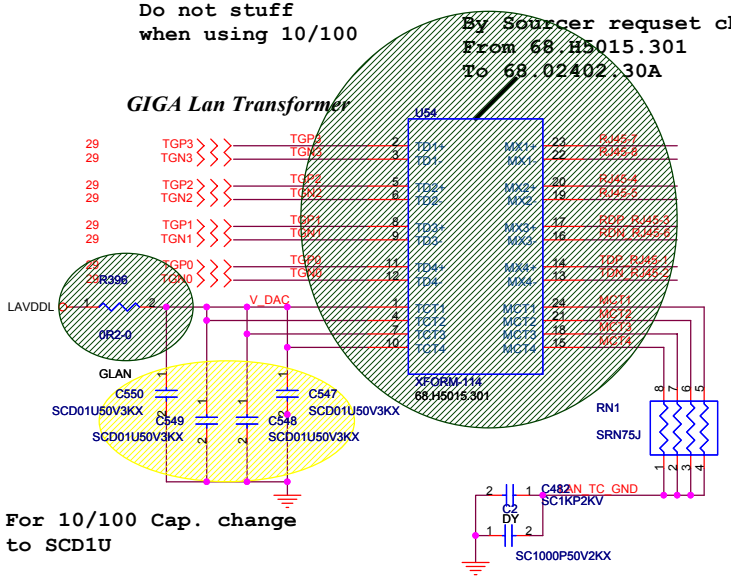
10/100M Lan Transformer

By Sourcer requset change P/N:
From 68.H0013.301
To 68.0H80P.301

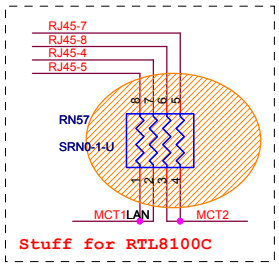
Do not stuff
when using 10/100

By Sourcer requset change P/N:
From 68.H5015.301
To 68.02402.30A

GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



Do not stuff
when using GLAN

For 10/100 Cap. change
to SCD1U

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN_CONN 10/100/1000
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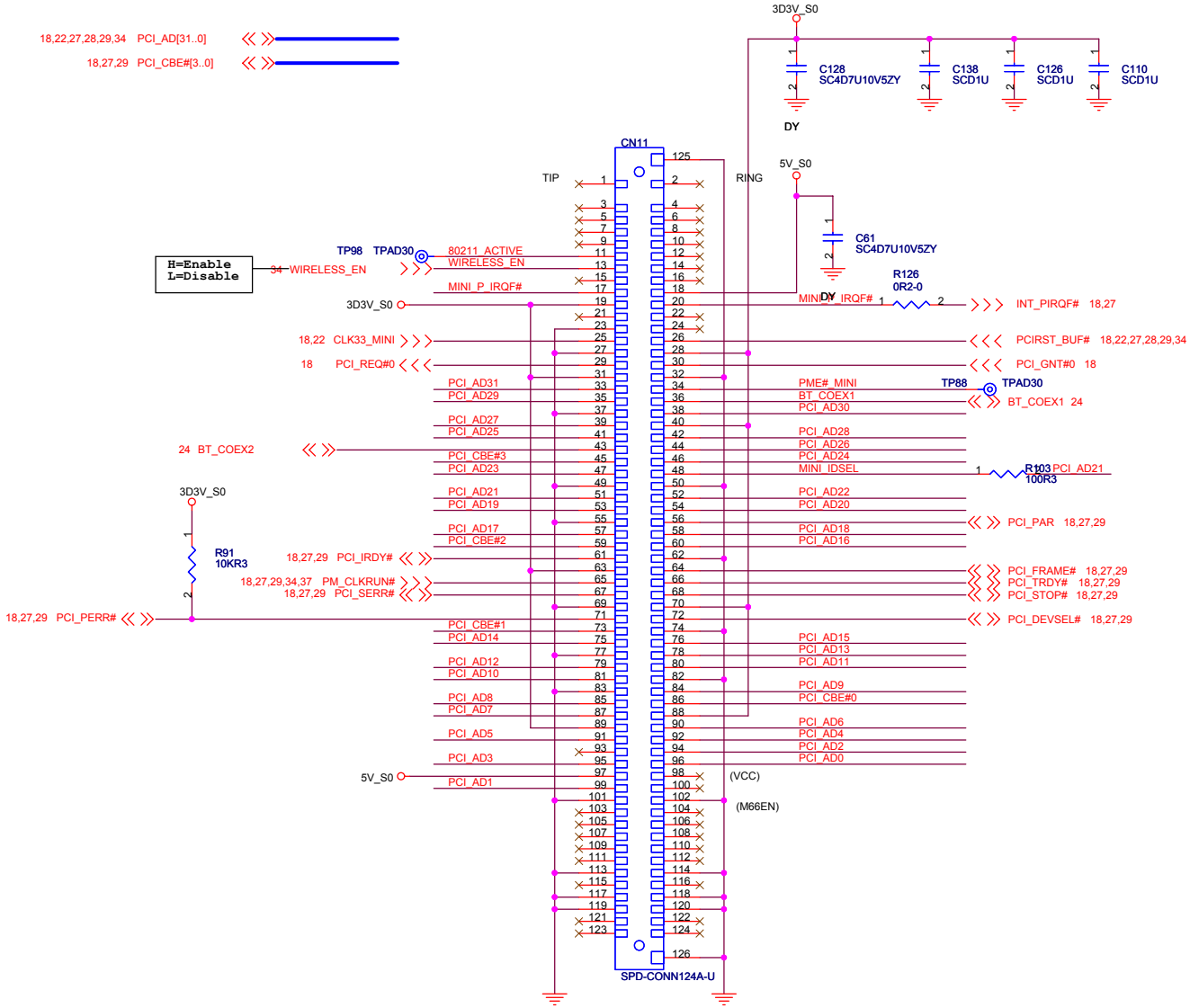
MINI-PCI



緯創資通 Wistron Corporation
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Title	MINI-PCI	
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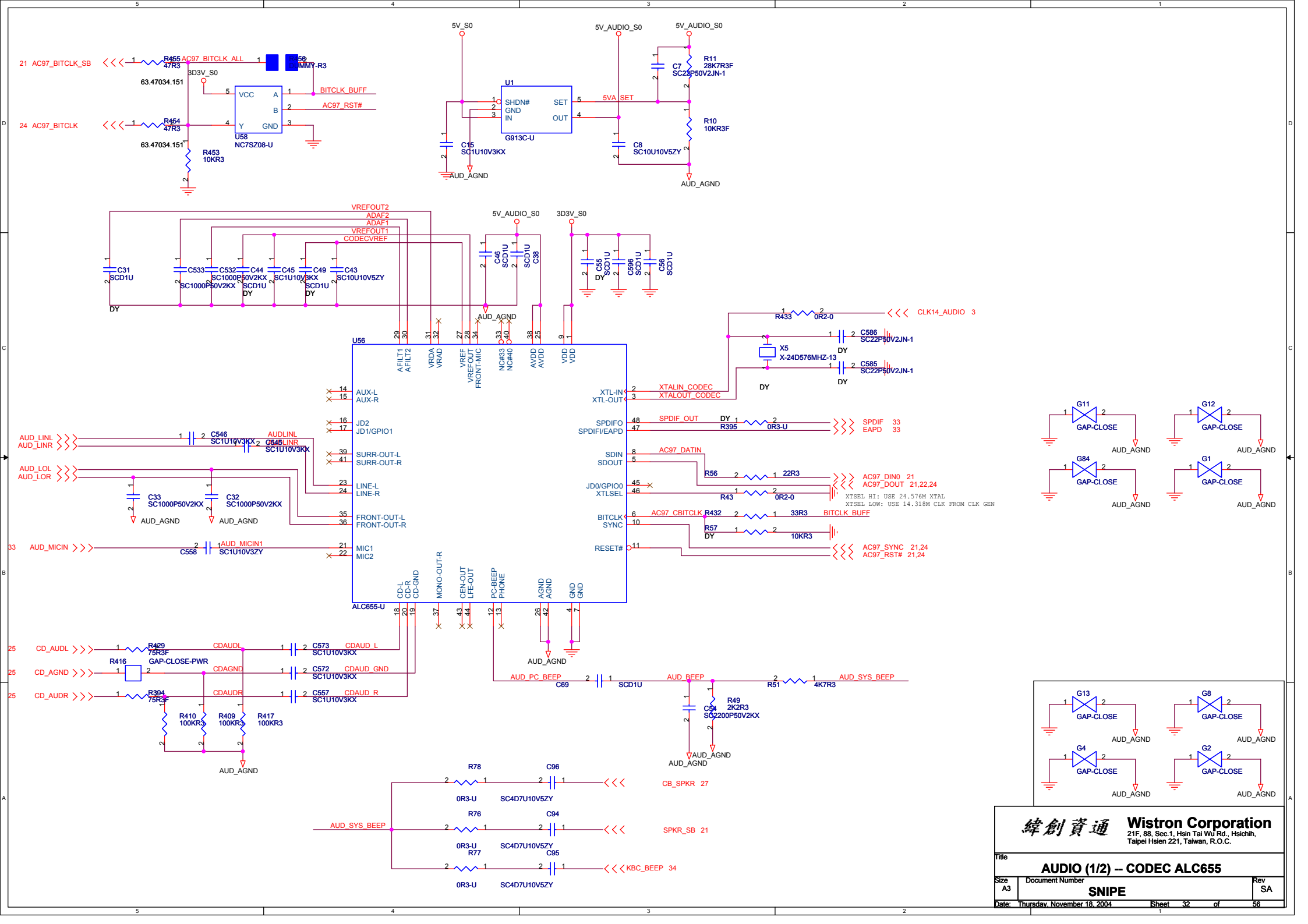

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO (1/2) -- CODEC ALC655**

Size	Document Number	Rev
A3	SNIPE	SA

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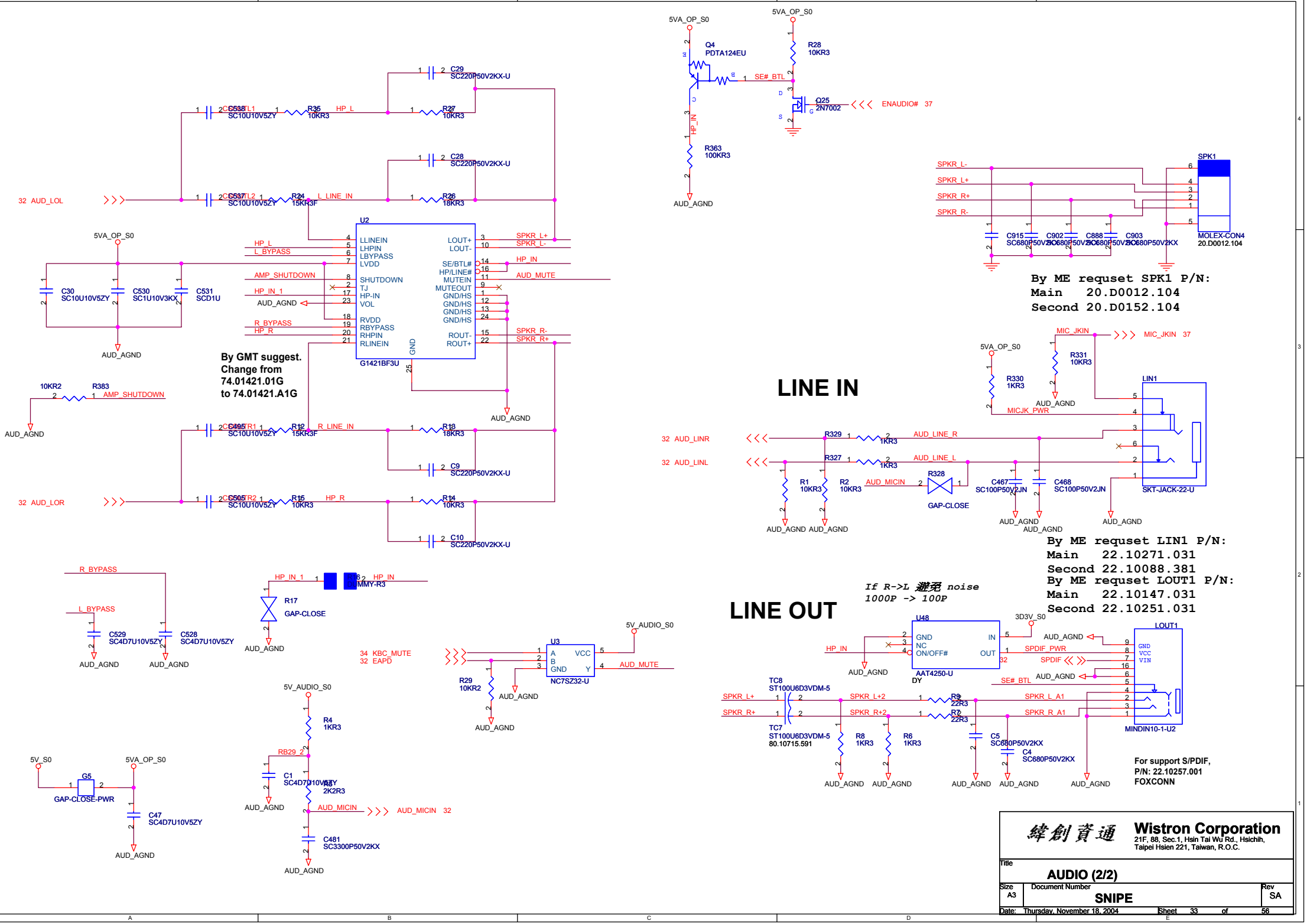
U2
G1421BF3U
LLINEIN
LHPIN
LBYPASS
LVDD
SHUTDOWN
TJ
HP-IN
VOL
RVDD
RBYPASS
RHPIN
RLINEIN
GND
LOUT+
LOUT-
SE/BTL#
HP/LINE#
MUTEIN
MUTEOUT
GND/HS
GND/HS
GND/HS
GND/HS
ROUT-
ROUT+
By GMT suggest.
Change from
74.01421.01G
to 74.01421.A1G
LINE IN
LINE OUT
By ME requset SPK1 P/N:
Main 20.D0012.104
Second 20.D0152.104
By ME requset LIN1 P/N:
Main 22.10271.031
Second 22.10088.381
By ME requset LOUT1 P/N:
Main 22.10147.031
Second 22.10251.031
If R->L 避免 noise
1000P -> 100P
For support S/PDIF,
P/N: 22.10257.001
FOXCONN
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
AUDIO (2/2)
SNIPE
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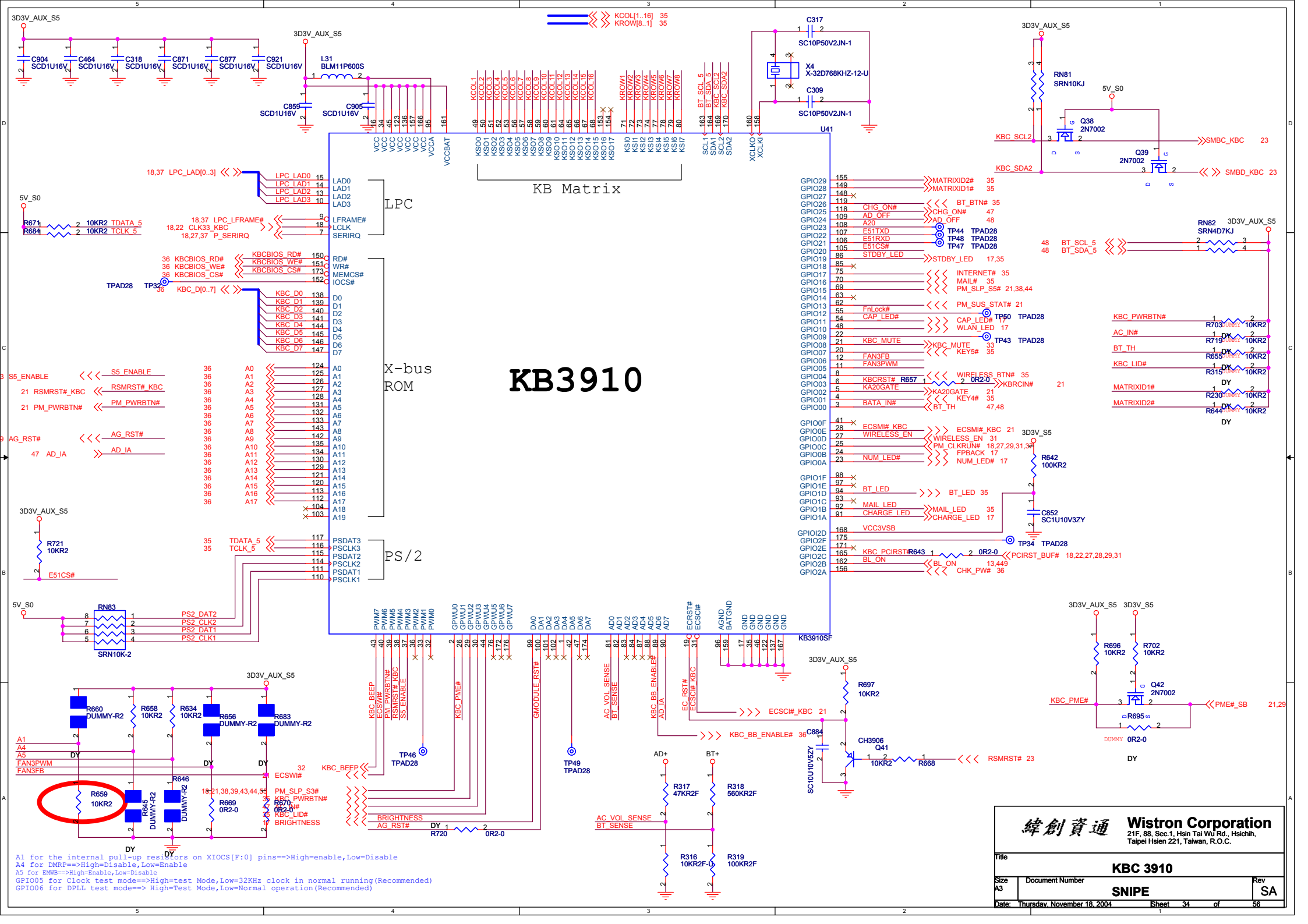
KB3910
KB Matrix
LPC
X-bus ROM
PS/2
KB3910SF
U41
3D3V_AUX_S5
5V_S0
KCOL[1..16] 35
KROW[8..1] 35
C317
SC10P50V2JN-1
X4
X-32D768KHZ-12-U
C309
SC10P50V2JN-1
L31
BLM11P600S
RN81
SRN10KJ
Q38
2N7002
Q39
2N7002
KBC_SCL2
KBC_SDA2
SMBC_KBC 23
SMBD_KBC 23
RN82
SRN4D7KJ
BT_SCL_5 48
BT_SDA_5 48
KBC_PWRBTN#
AC_IN#
BT_TH
KBC_LID#
MATRIXID1#
MATRIXID2#
R703 10KR2
R719 10KR2
R655 10KR2
R315 10KR2
R230 10KR2
R644 10KR2
R642 100KR2
C852 SC1U10V3ZY
R643 0R2-0
PCIRST_BUF# 18,22,27,28,29,31
RN83
SRN10K-2
PS2_DAT2
PS2_CLK2
PS2_DAT1
PS2_CLK1
R721 10KR2
E51CS#
R660 DUMMY-R2
R658 10KR2
R634 10KR2
R656 DUMMY-R2
R683 DUMMY-R2
R659 10KR2
R645 DUMMY-R2
R646
R669 0R2-0
R670 0R2-0
R720 0R2-0
R697 10KR2
C884
CH3906
Q41
R668 10KR2
RSMRST# 23
R696 10KR2
R702 10KR2
Q42
2N7002
R695
0R2-0
PME#_SB 21,29
R317 47KR2F
R318 560KR2F
R316 10KR2F-L
R319 100KR2F
A1 for the internal pull-up resistors on XIOCS[F:0] pins==>High=enable,Low=Disable
A4 for DMRP==>High=Disable,Low=Enable
A5 for EMWB==>High=Enable,Low=Disable
GPIO05 for Clock test mode==>High=test Mode,Low=32KHz clock in normal running(Recommended)
GPIO06 for DPLL test mode==> High=Test Mode,Low=Normal operation(Recommended)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC 3910
Size A3
Document Number
SNIPE
Rev SA
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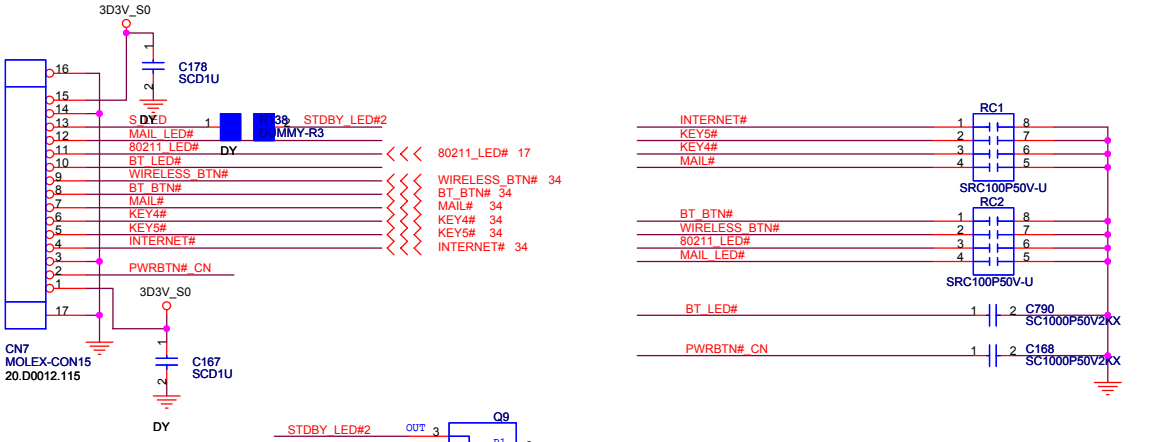
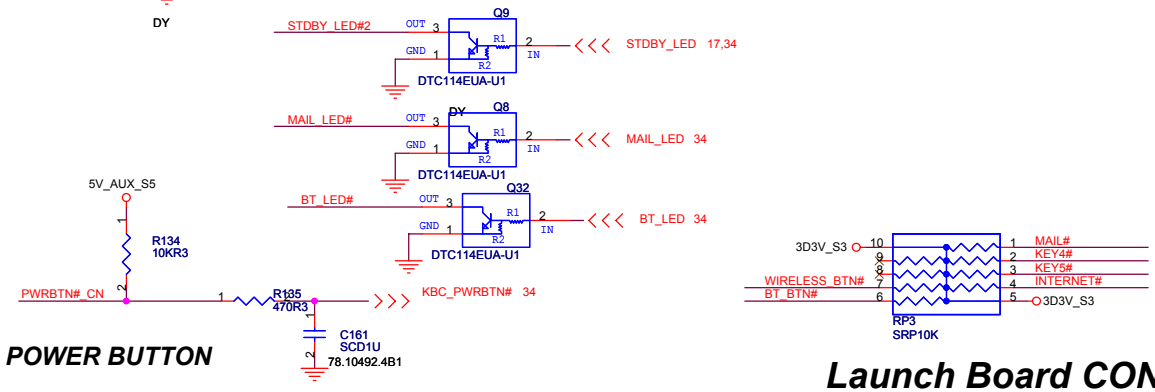
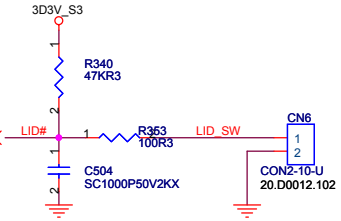


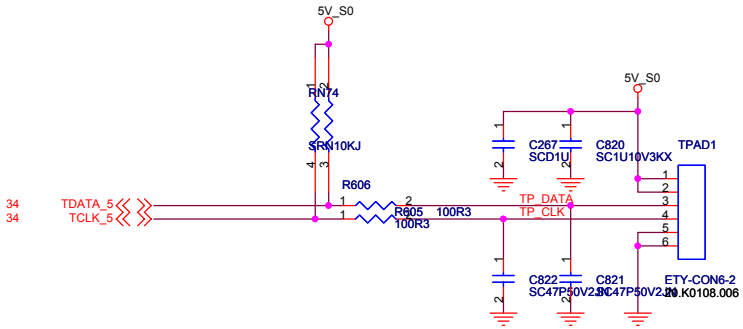


POWER BUTTON

Launch Board CONN

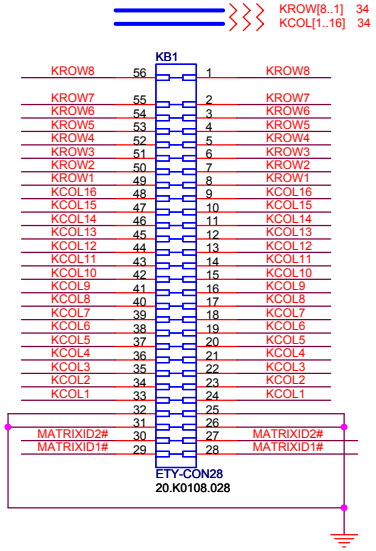


Cover Up Switch



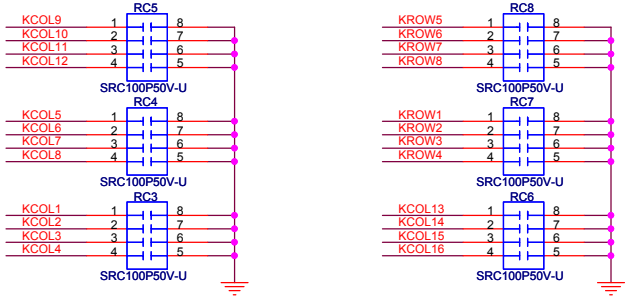
TOUCH PAD

Internal KeyBoard CONN



Keyboard matrix	(from vendor)			
	US	Jap	Eur	Other
Low Bit MATRIXID1#	1	1	0	0
High Bit MATRIXID2#	1	0	1	0

EMI Bypass cap.



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: LAUNCH / TOUCHPAD / KB CONN

Size: A3 | Document Number: SNIPE | Rev: SA

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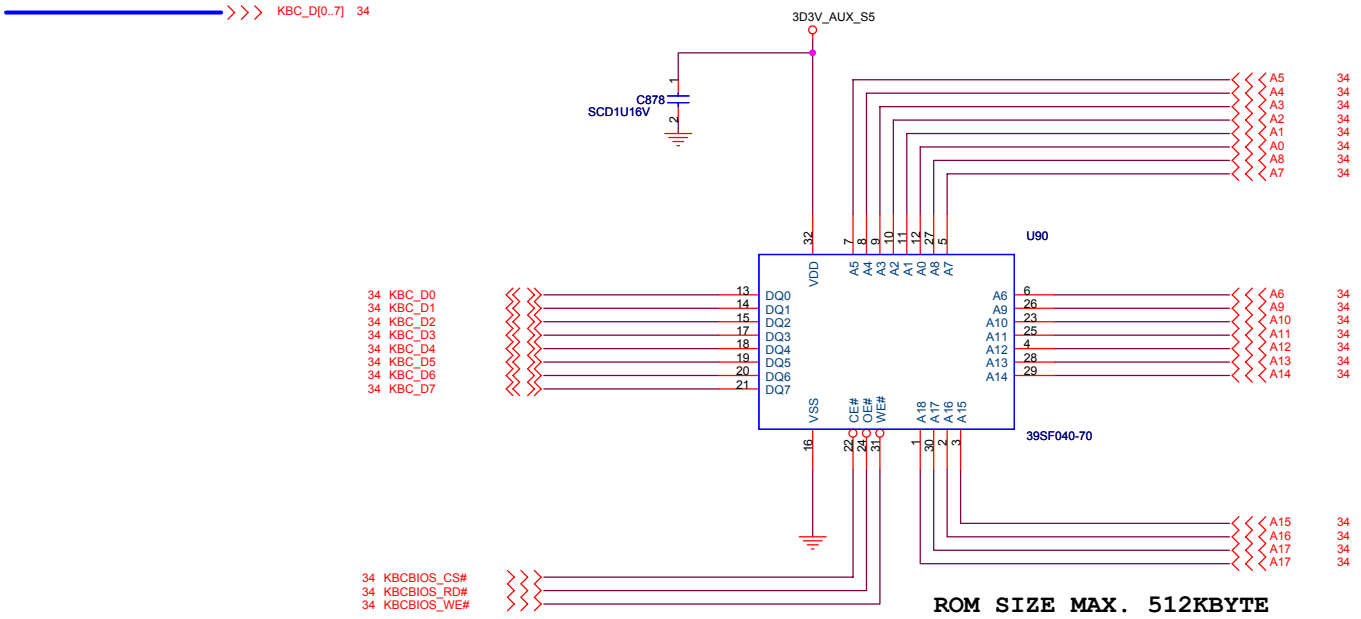
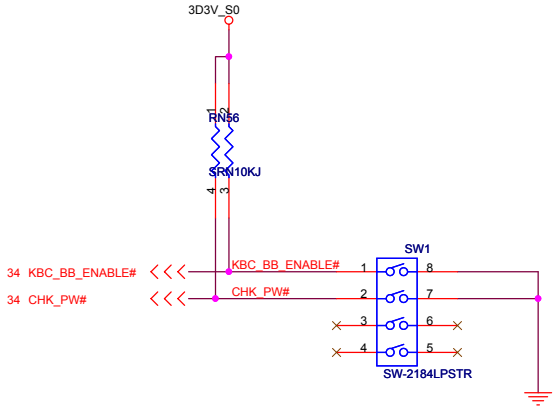


PLCC32 Socket P/N:
SSKT3262.10002.032
SSKT32 62.10005.032



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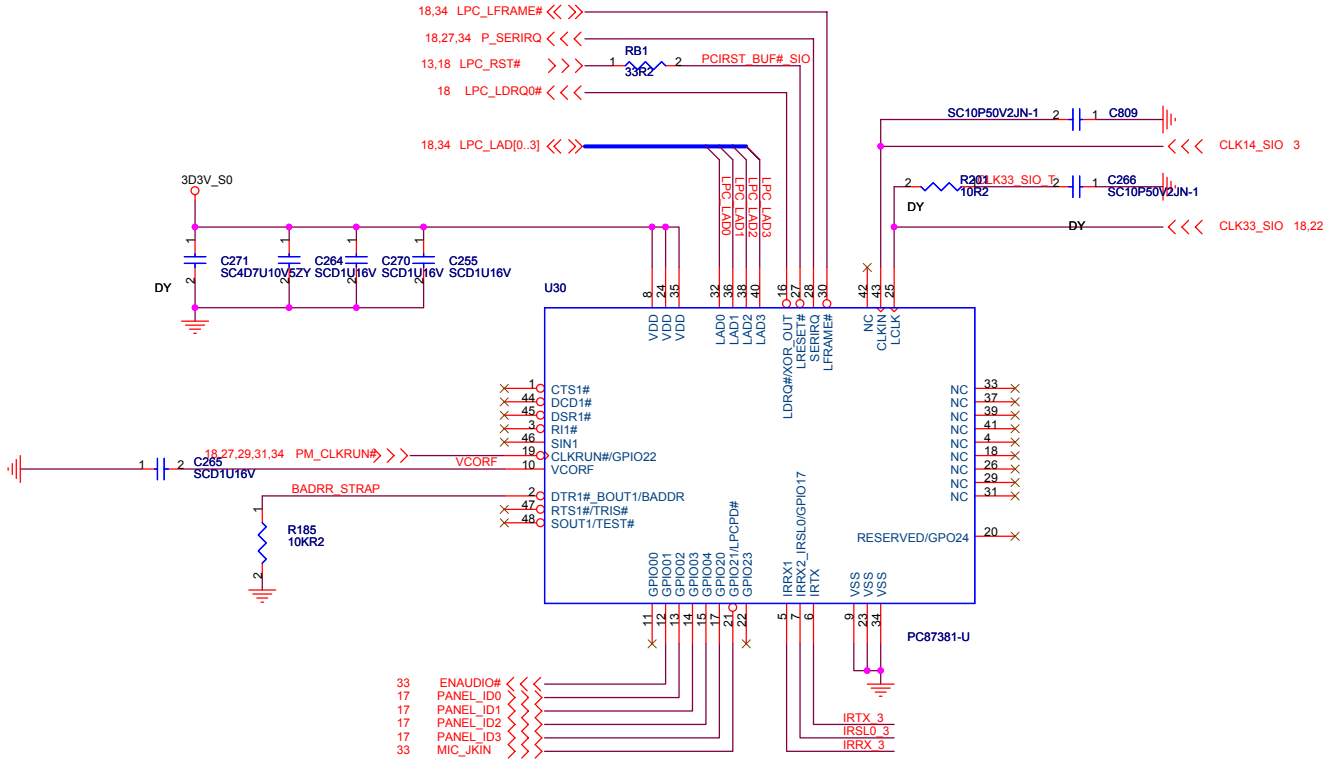
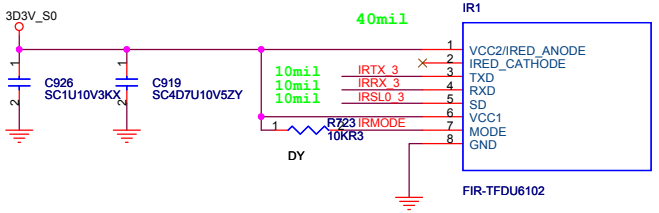
Title: **BIOS ROM**		
Size: A3	Document Number: **SNIPE**	Rev: SA
Date: Thursday, November 18, 2004	Sheet 36 of 56	



Infineon FIR Module



PANEL ID DEFINE				
PANEL_ID3	PANEL_ID2	PANEL_ID1	PANEL_ID0	VENDORS
0	0	0	0	15" SXGA+
0	0	0	1	Hydis (14")SPWG
0	0	1	0	15" WIDE
0	0	1	1	Hitachi (15")
0	0	1	1	AU (15")
0	0	1	1	CMO(15")
0	1	0	0	CMO(14")
0	1	0	1	AU (14")
0	1	1	0	AU (14")**
0	1	1	1	No Panel

Note : AU (友達),CMO(奇美),** : With Digitizer

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Title: **SUPER IO NC87381**

Size	Document Number	Rev
A3	SNIPE	SA

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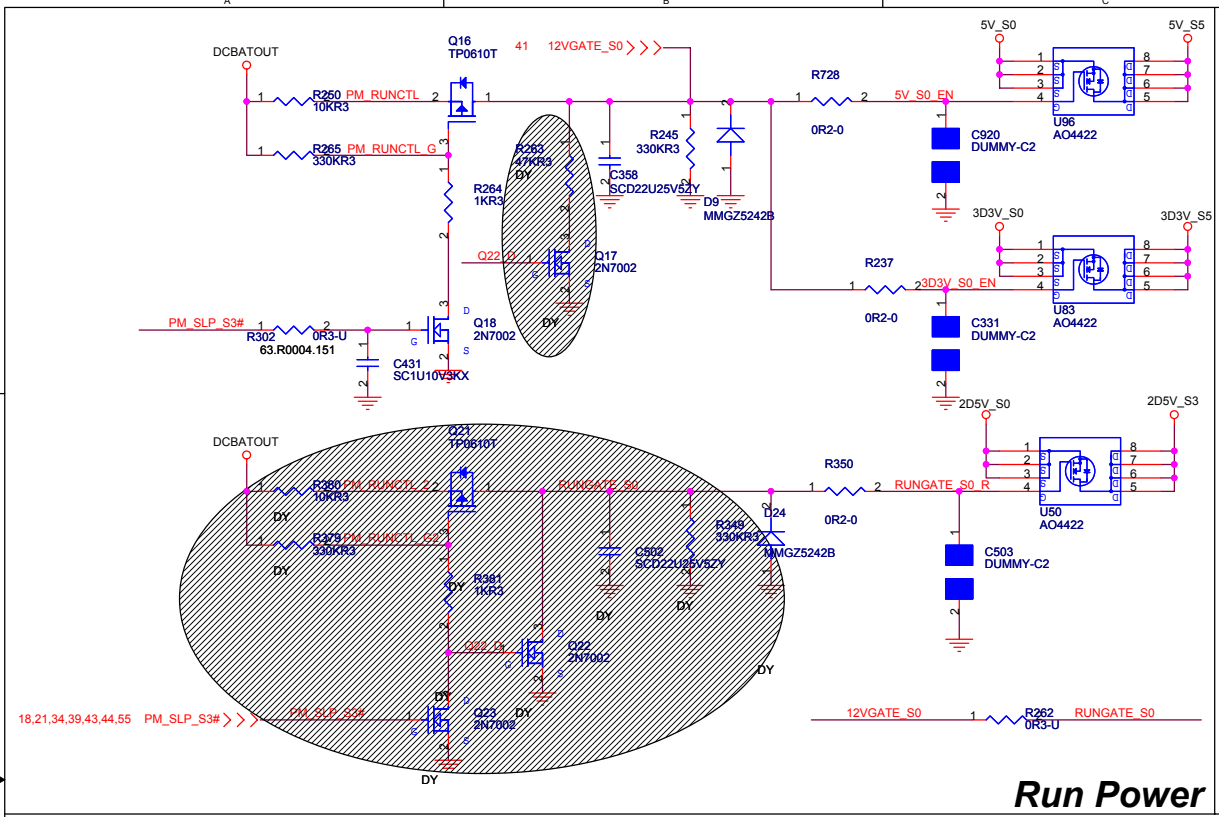

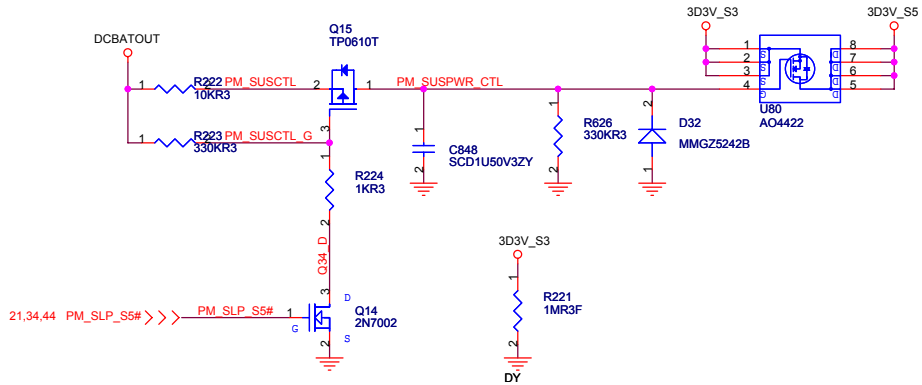

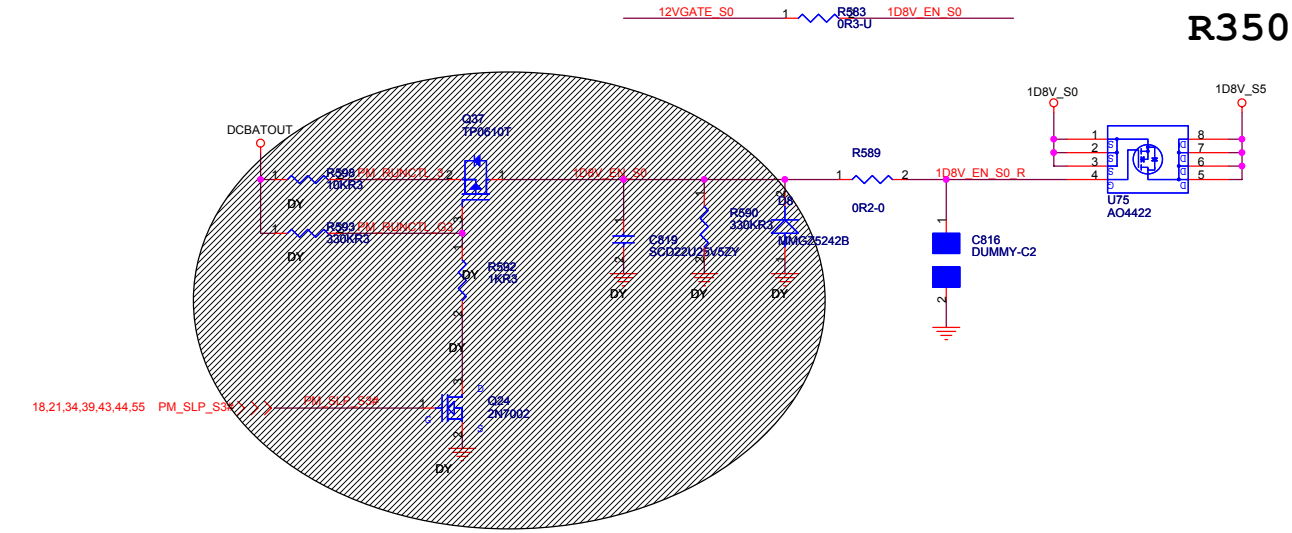

R350 & R589 WILL BE REMOVED ON VER SB

Power On Logic

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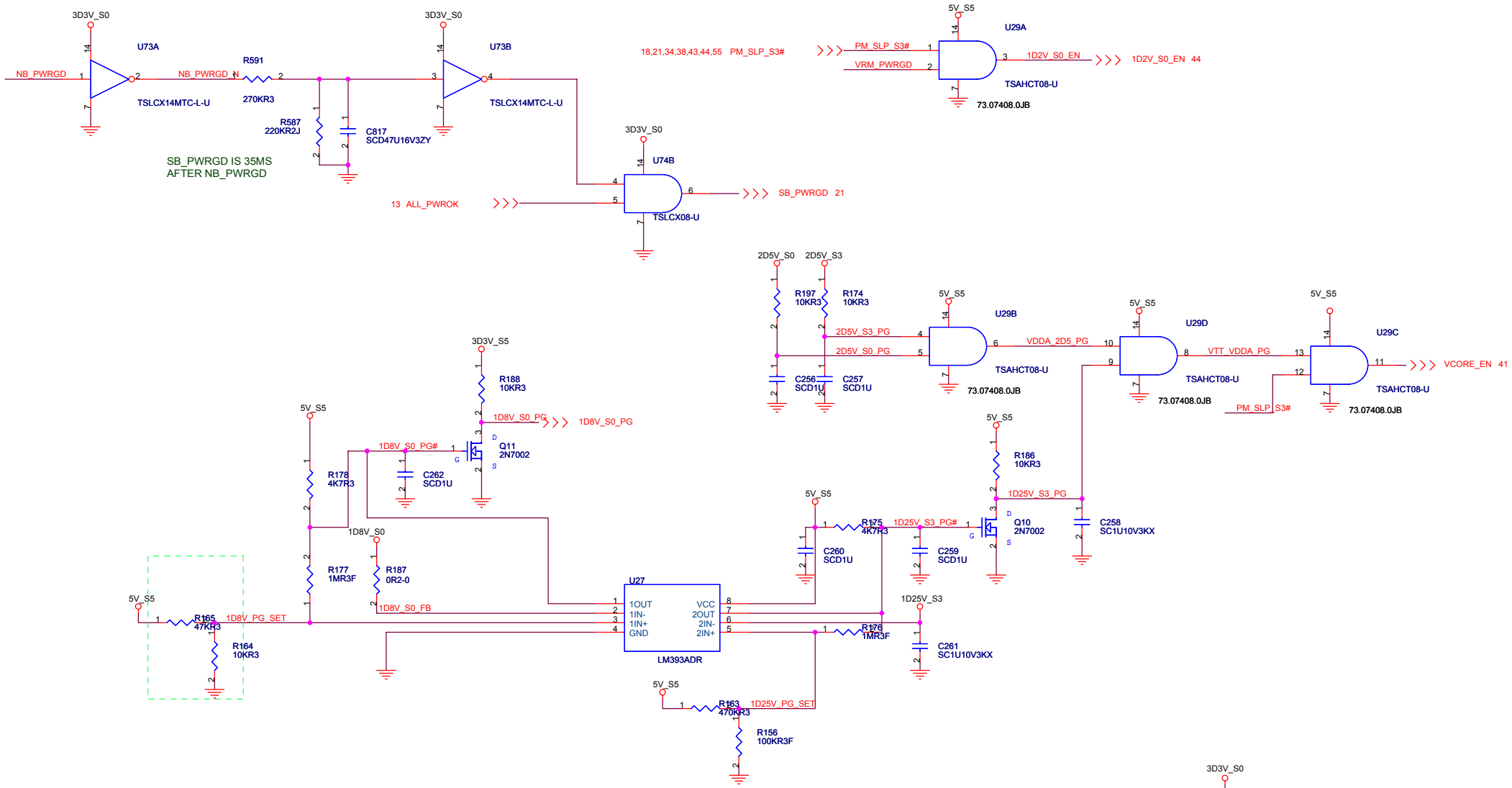
Taipei Hsien 221, Taiwan, R.O.C.

Title	PWR CTL LOGIC / PWR PLANE	
Size A3	Document Number SNIPE	Rev SA
Date: Thursday, November 18, 2004	Sheet 38 of 56	



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Taipei Hsien 221, Taiwan, R.O.C.

Title: **POWERGOOD&ENABLES**

Size	Document Number	Rev
Custom	SNIPE	SA

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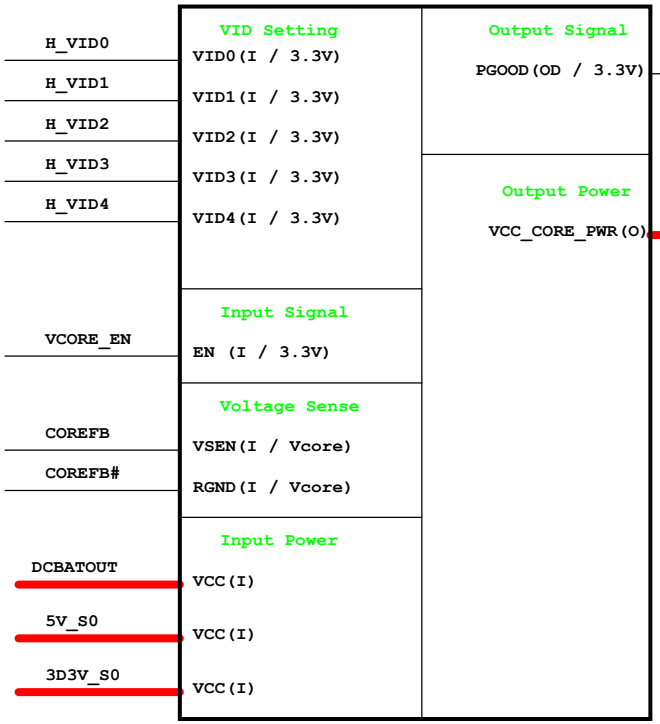
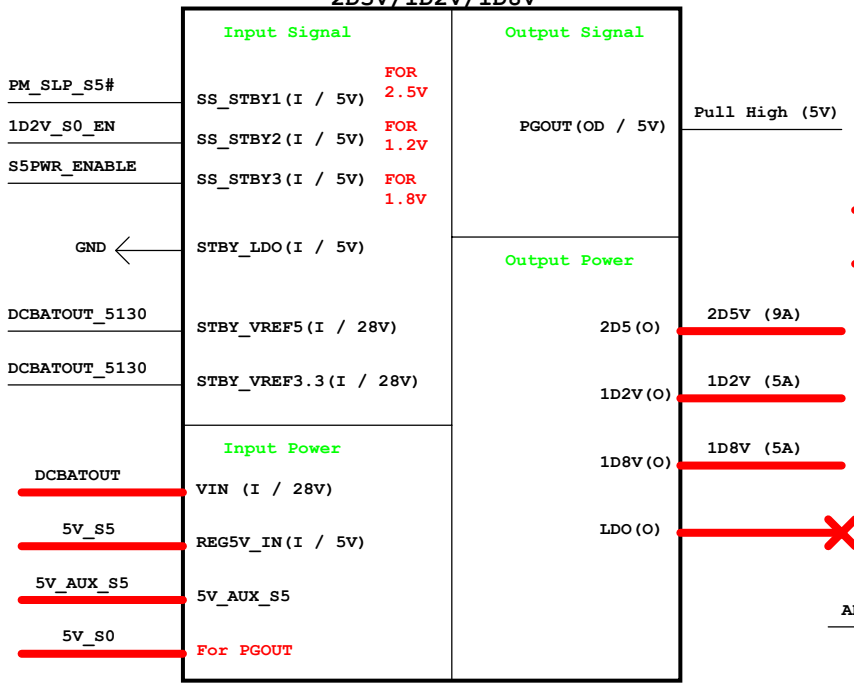
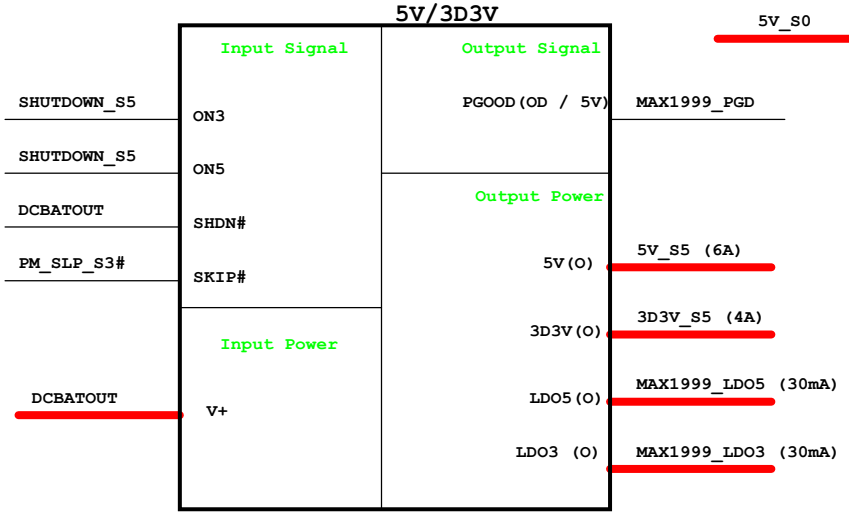
CPU_CORE
Intersil 6559CR + ISL6207CB*3 (Dummy *1)



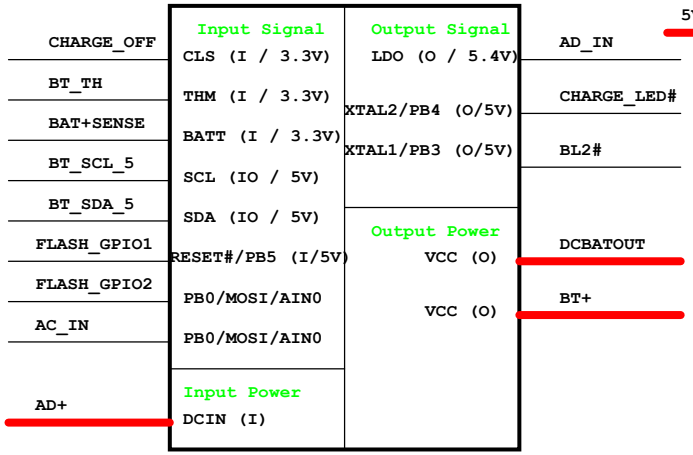
TI TPS5130
2D5V/1D2V/1D8V



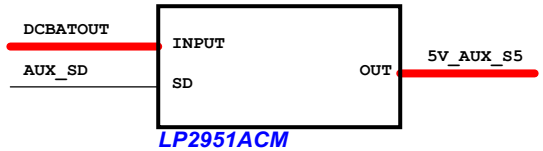
Max1999
5V/3D3V



Charger_Max1909

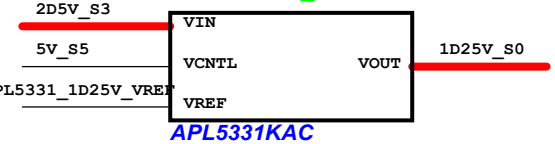


5V_AUX_S5



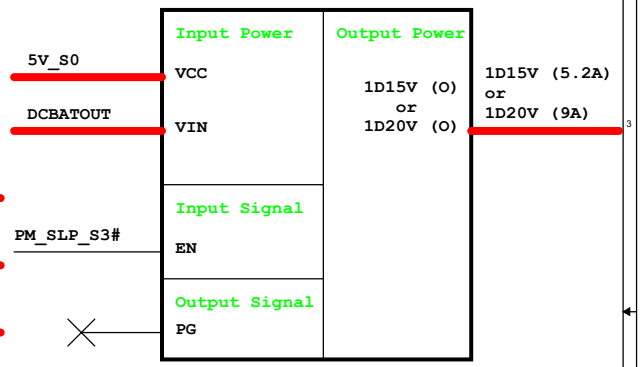
LP2951ACM

1D25V_S3

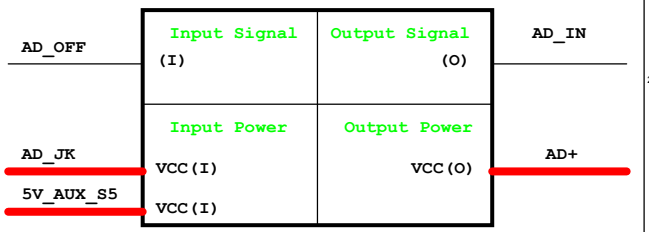


APL5331KAC

FAN5234_VGA_Core
1D15V or 1D20V



Adapter



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Title: **Power Block Diagram**

Size	Document Number	Rev
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Vcore_CPU=1.500V
Iomax=52.9A
Vcore_CPU=1.400V
Iomax=42.7A

Vdrop is over spec under max loading

R value large, then offset small.
=> 3K or 4.99K?
Now=>Offset value is over 0.05V
If without offset =>R158=0ohm

Gain value large, then bandwidth large!
=> 2.74K or 3.65K

PLACE IN THE BACK OF CPU

Remote Sense Tie to CPU

SB

53A*1.5=79.5A (OCP),=>79.5A/2Phase=39.75A/Phase
90uA*Rsense=39.75A*(6.5m/2)*1.4
=>Rsense=2.0K

C216/C201/C140 Can not stuff!

Rt=10^[11.09-1.13log(fs)]
Rt=107K,=>fs=230KHz
But real freq.=270KHz

Follow MOSFET rise time spec.

DCR=1.3mohm+-10% / Imax=40A / Panasonic / ETQP2H0R7BF / 0.48uH / 13.4*13.3*4.9

Power-PAK
Id=7A
Qg=10~15nC
Rdson=13~16.5mohm

Power-PAK
Id=13A
Qg=32~50nC
Rdson=4~4.8mohm

BSC059N03S-U (84.59N03.037)
BSC042N03S-U (84.42N03.037)
2'nd Source:
H/S:SI7392DP (84.07392.037)
L/S:SI7636DP (84.07636.037)

Main Source:
KEMET 2D5V/ 330uF / ESR=9mohm / Iripple=3.7A / ST330U2D5VDM-3
80.3371V.191/ 7.3*4.3*1.9 / NT$:9.5
2'nd Source:
Panasonic 2V/ 330uF / ESR=9mohm / Iripple=3.0A/ SE330U2VDM-2
79.33719.20A/ 7.3*4.3*1.9 / NT$:10.0

Panasonic 25V / E1 Cap.
8.5*6.5mm / SMD
ESR=0.26ohm, Iripple=0.3A
FX Serial

Follow MOSFET rise time spec.
=> Mount 0ohm first.

SB Version:
Change U4 from ISL6209CB (74.06209.071)
to ISL6207CB-U (74.06207.071)

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	DAC
0	0	0	0	0	1.550
0	0	0	0	1	1.525
0	0	0	1	0	1.500
0	0	0	1	1	1.475
0	0	1	0	0	1.450
0	0	1	0	1	1.425
0	0	1	1	0	1.400
0	0	1	1	1	1.375
0	1	0	0	0	1.350
0	1	0	0	1	1.325
0	1	0	1	0	1.300
0	1	0	1	1	1.275
0	1	1	0	0	1.250
0	1	1	0	1	1.225
0	1	1	1	0	1.200
0	1	1	1	1	1.175
1	0	0	0	0	1.150
1	0	0	0	1	1.125
1	0	0	1	0	1.100
1	0	0	1	1	1.075
1	0	1	0	0	1.050
1	0	1	0	1	1.025
1	0	1	1	0	1.000
1	0	1	1	1	0.975
1	1	0	0	0	0.950
1	1	0	0	1	0.925
1	1	0	1	0	0.900
1	1	0	1	1	0.875
1	1	1	0	0	0.850
1	1	1	0	1	0.825
1	1	1	1	0	0.800
1	1	1	1	1	Shutdown

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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power_1

Size: A2 | Document Number: SNIPE | Rev: SA

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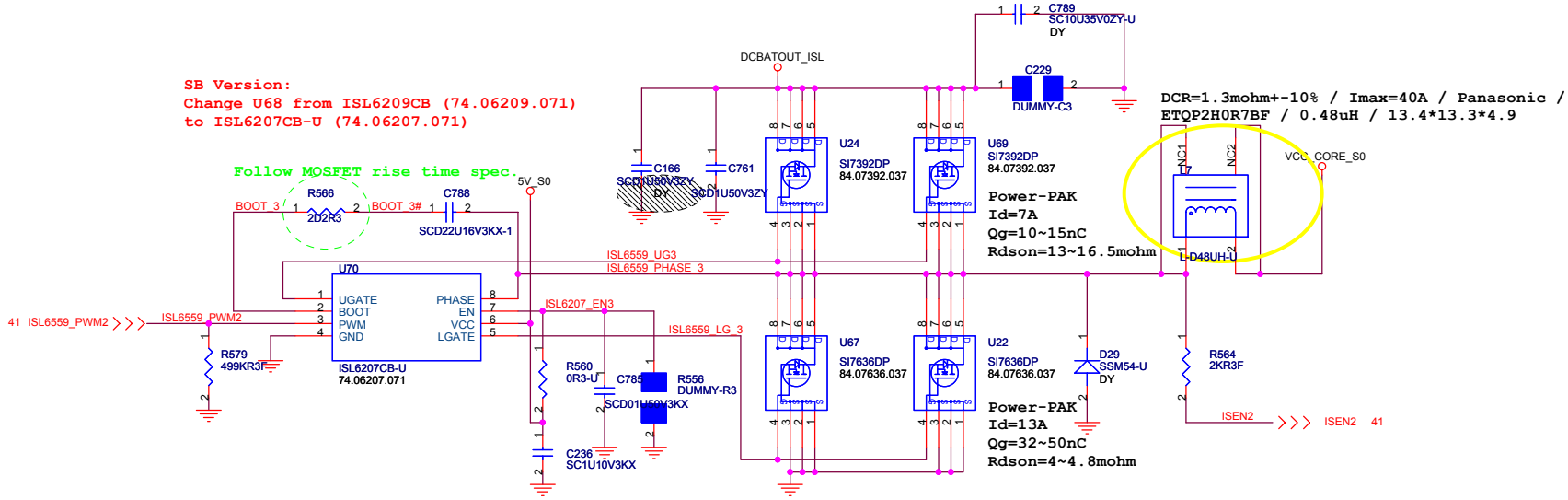

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**CPU Vcore Power_2**	
Size: A3	Document Number: **SNIPE**	Rev: SA
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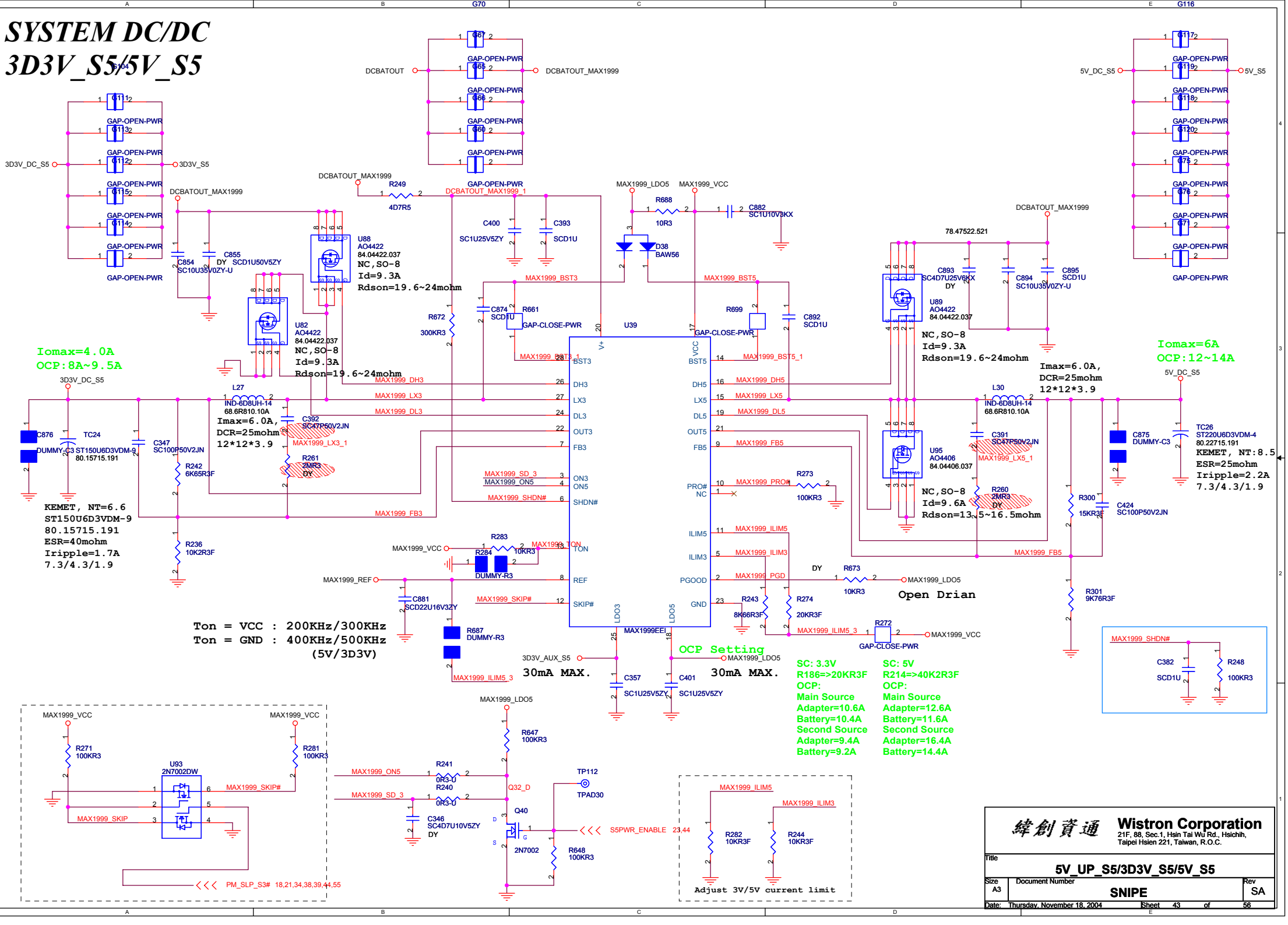
SYSTEM DC/DC
3D3V_S5/5V_S5



緯創資通	**Wistron Corporation**
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title	5V_UP_S5/3D3V_S5/5V_S5	
Size A3	Document Number SNIPE	Rev SA
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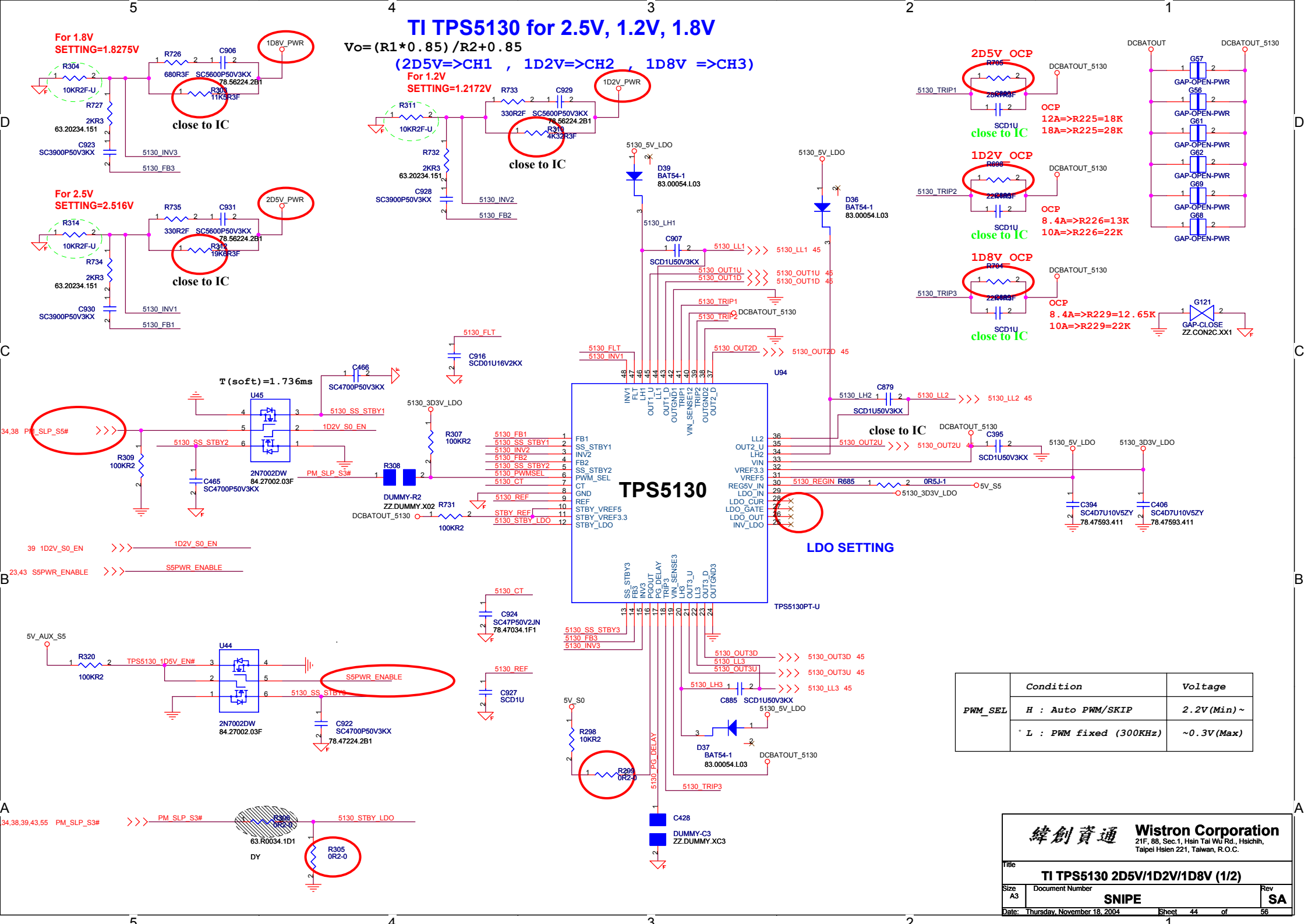
TI TPS5130 for 2.5V, 1.2V, 1.8V

Vo=(R1*0.85)/R2+0.85

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)



PWM_SEL	Condition	Voltage
	H : Auto PWM/SKIP	2.2V(Min)~
	* L : PWM fixed (300KHz)	~0.3V(Max)

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

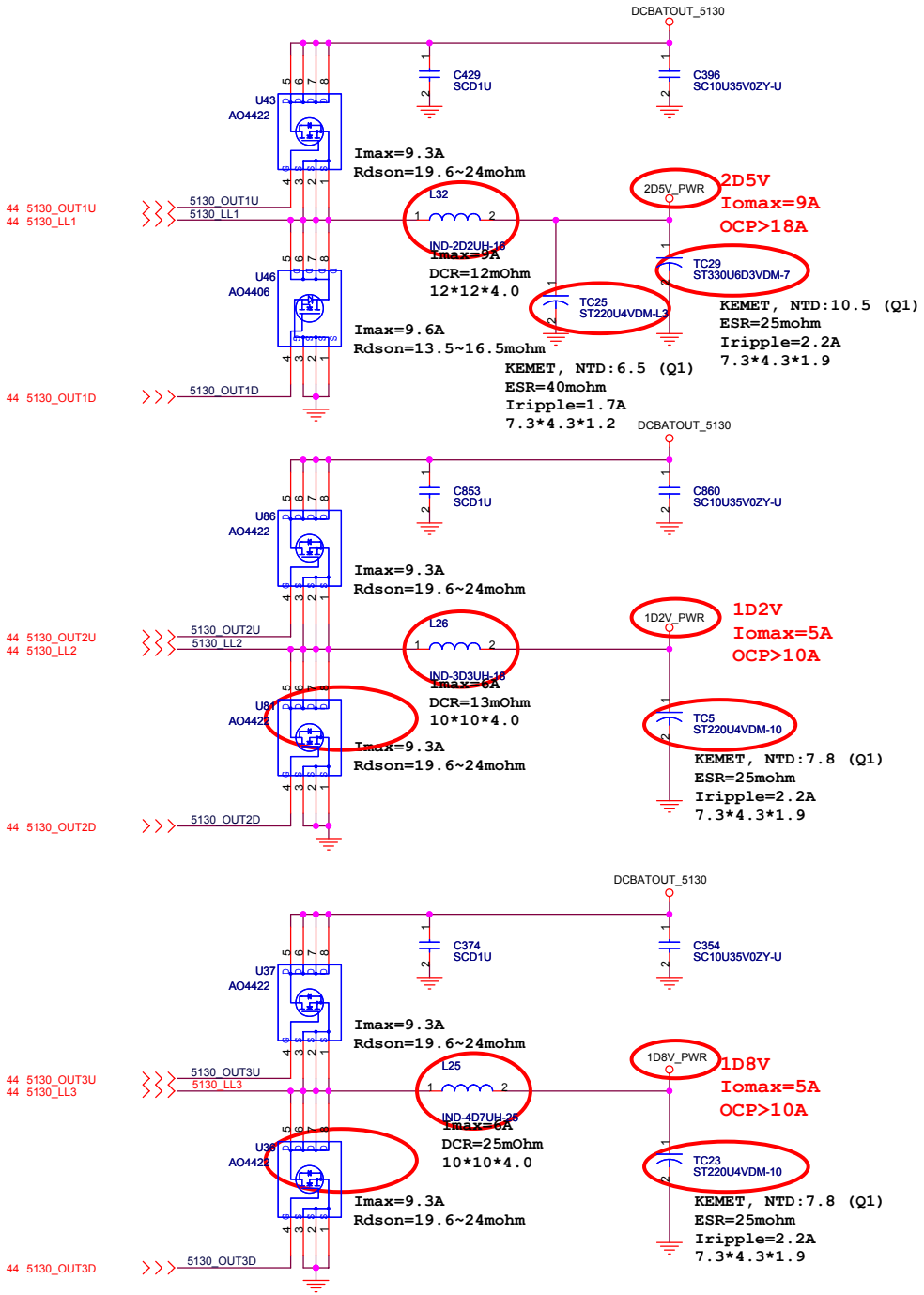
Title: TI TPS5130 2D5V/1D2V/1D8V (1/2)

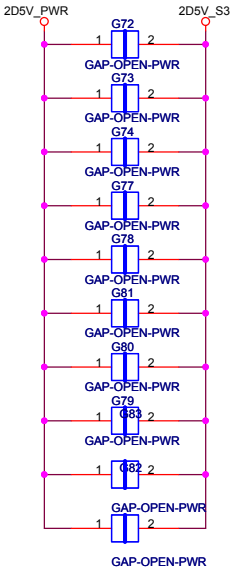
Size: A3 | Document Number: SNIPE | Rev: SA

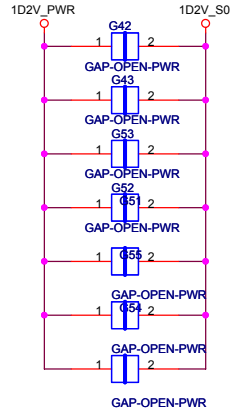
Date: Thursday, November 18, 2004 | Sheet 44 of 56

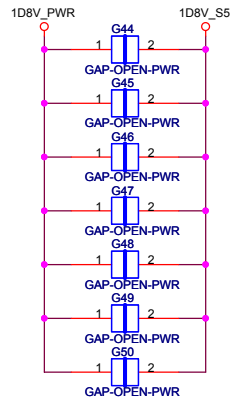
TI TPS5130 for 2D5V, 1D2V, 1D8V

(2D5V=>CH1 , 1D2V=>CH2 , 1D8V =>CH3)









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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **TI TPS5130 2D5V/1D2V/1D8V (2/2)**

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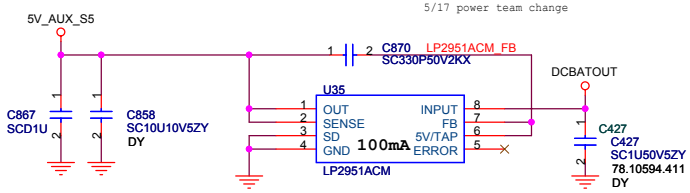
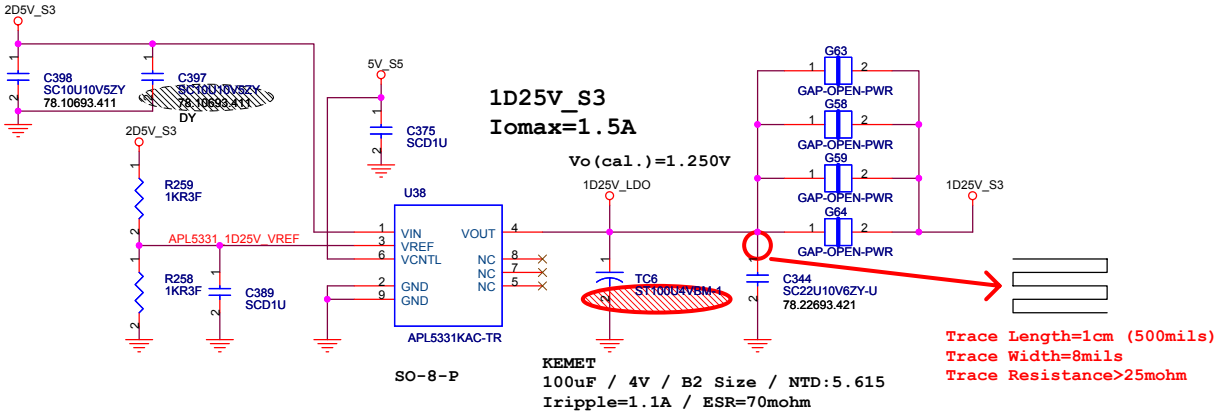
5V_AUX_S5

5/17 power team change





緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D2V_LDO/5V_AUX		
Size: A3	Document Number: SNIPE	Rev: SA
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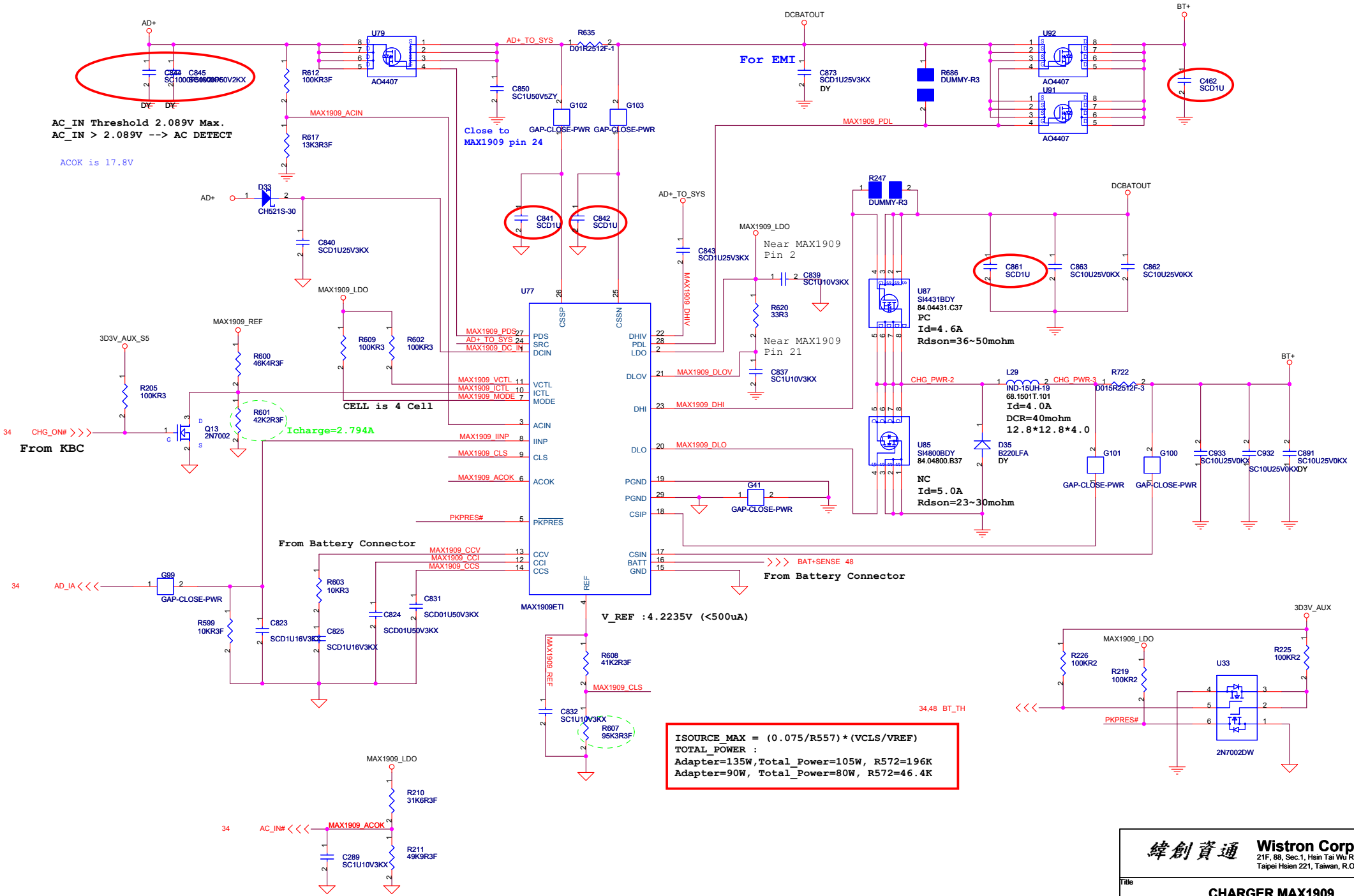

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Taipei Hsien 221, Taiwan, R.O.C.

Title	CHARGER MAX1909		
Size: Custom	Document Number: SNIPE		Rev: SA
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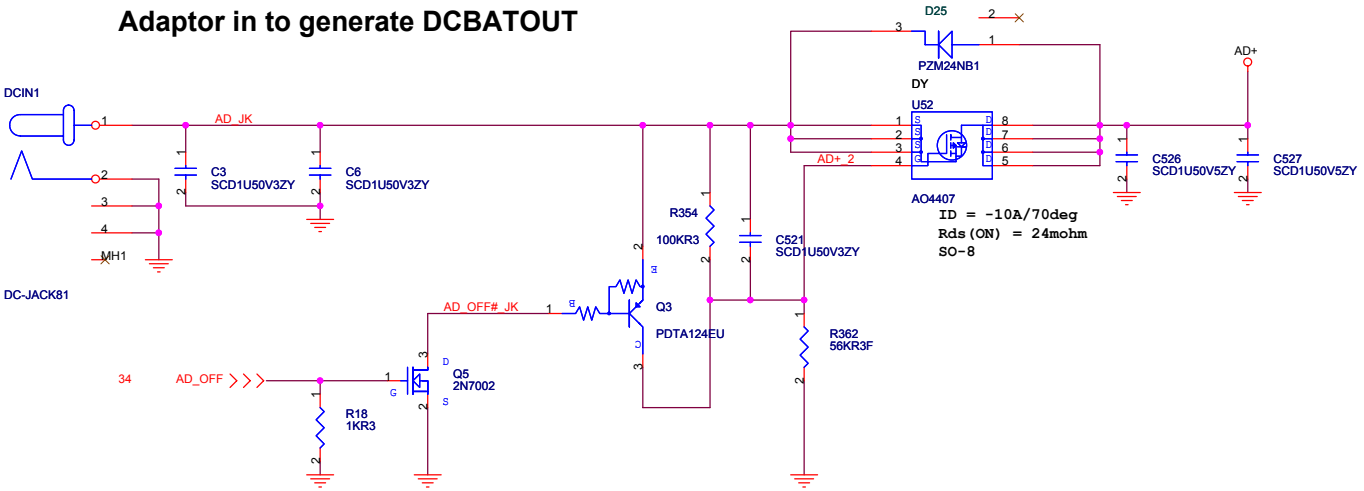
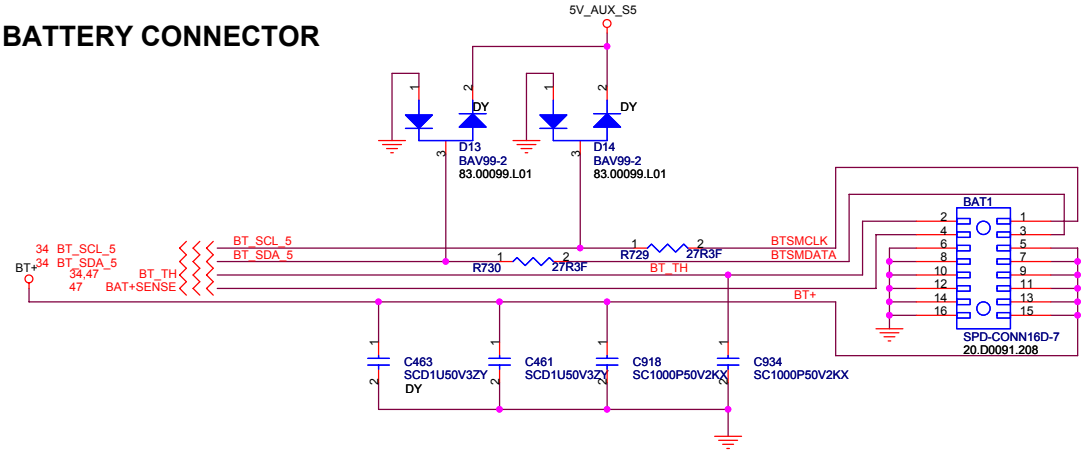
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: DC/DC (1/2) -- 5V / 3.3V / 2.5V		
Size: A3	Document Number: SNIPE	Rev: SA
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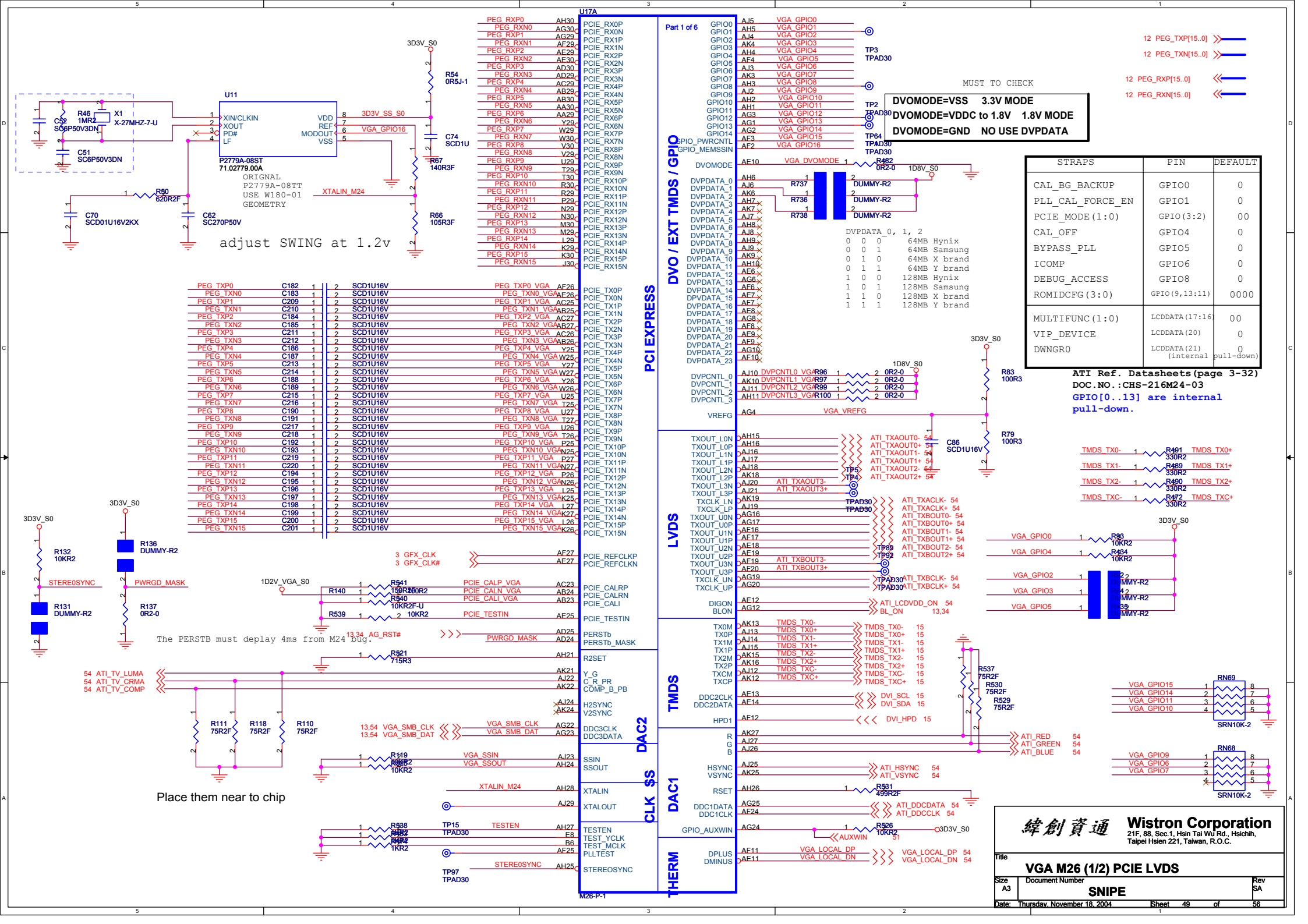
U17A
Part 1 of 6
PCI EXPRESS
DVO / EXT TMDS / GPIO
LVDS
TMDS
DAC2
DAC1
CLK $S
THERM
M26-P-1
U11
P2779A-08ST
71.02779.00A
ORIGNAL
P2779A-08TT
USE W180-01
GEOMETRY
adjust SWING at 1.2v
Place them near to chip
The PERSTB must deplay 4ms from M24 bug.
MUST TO CHECK
DVOMODE=VSS 3.3V MODE
DVOMODE=VDDC to 1.8V 1.8V MODE
DVOMODE=GND NO USE DVPDATA
STRAPS
PIN
DEFAULT
CAL_BG_BACKUP GPIO0 0
PLL_CAL_FORCE_EN GPIO1 0
PCIE_MODE(1:0) GPIO(3:2) 00
CAL_OFF GPIO4 0
BYPASS_PLL GPIO5 0
ICOMP GPIO6 0
DEBUG_ACCESS GPIO8 0
ROMIDCFG(3:0) GPIO(9,13:11) 0000
MULTIFUNC(1:0) LCDDATA(17:16) 00
VIP_DEVICE LCDDATA(20) 0
DWNGR0 LCDDATA(21) 0
(internal pull-down)
ATI Ref. Datasheets(page 3-32)
DOC.NO.:CHS-216M24-03
GPIO[0..13] are internal pull-down.
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Title
VGA M26 (1/2) PCIE LVDS
Size A3
Document Number SNIPE
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Date: Thursday, November 18, 2004
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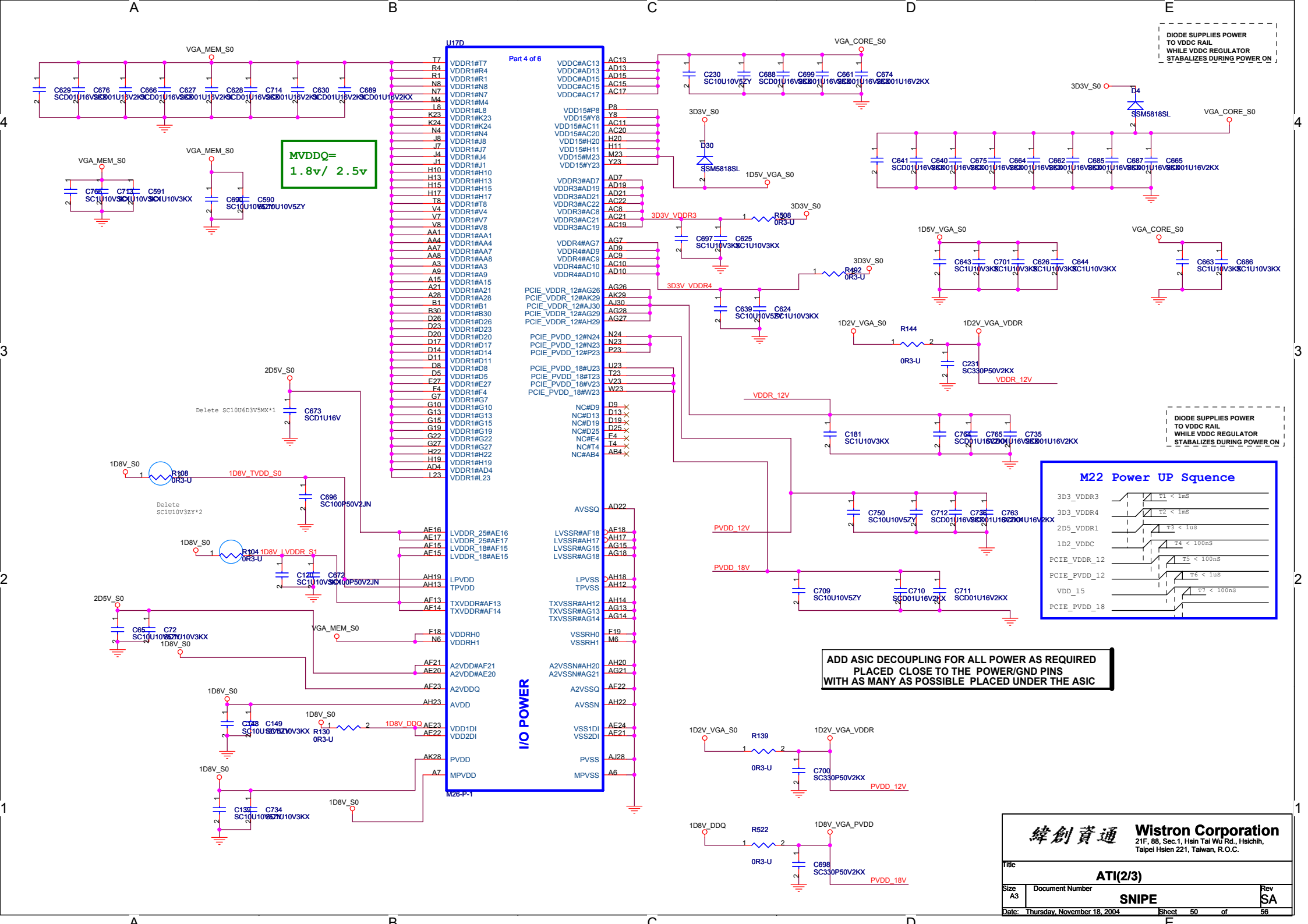
U17D
Part 4 of 6
I/O POWER
M26-P-1
MVDDQ=
1.8v/ 2.5v
DIODE SUPPLIES POWER
TO VDDC RAIL
WHILE VDDC REGULATOR
STABALIZES DURING POWER ON
M22 Power UP Squence
3D3_VDDR3
3D3_VDDR4
2D5_VDDR1
1D2_VDDC
PCIE_VDDR_12
PCIE_PVDD_12
VDD_15
PCIE_PVDD_18
T1 < 1mS
T2 < 1mS
T3 < 1uS
T4 < 100nS
T5 < 100nS
T6 < 1uS
T7 < 100nS
ADD ASIC DECOUPLING FOR ALL POWER AS REQUIRED
PLACED CLOSE TO THE POWER/GND PINS
WITH AS MANY AS POSSIBLE PLACED UNDER THE ASIC
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Title
ATI(2/3)
Size A3
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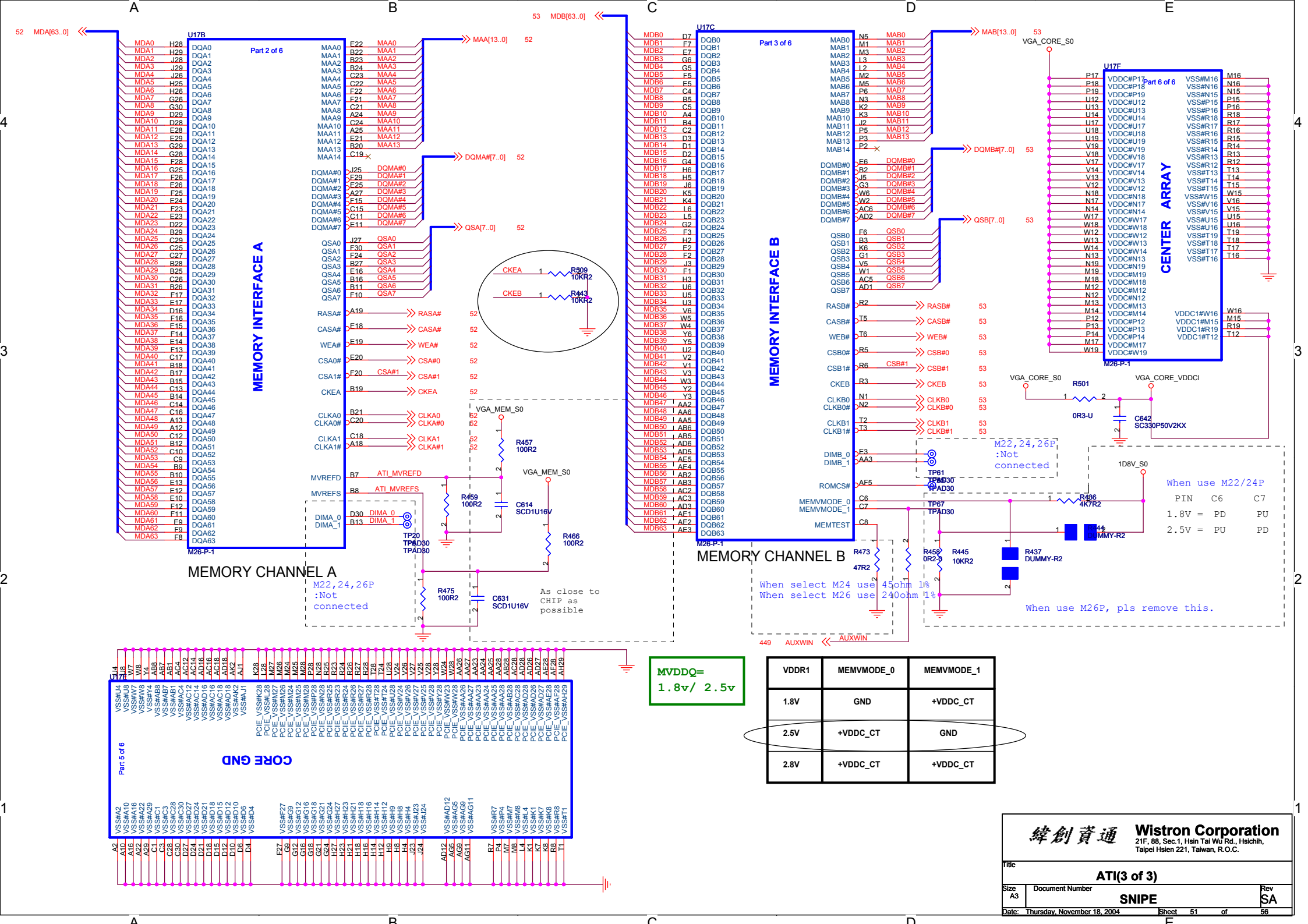
MEMORY INTERFACE A
MEMORY CHANNEL A
MEMORY INTERFACE B
MEMORY CHANNEL B
CENTER ARRAY
CORE GND
M22,24,26P :Not connected
When use M22/24P
PIN C6 C7
1.8V = PD PU
2.5V = PU PD
When use M26P, pls remove this.
When select M24 use 45ohm 1%
When select M26 use 240ohm 1%
As close to CHIP as possible
MVDDQ= 1.8v/ 2.5v
VDDR1 MEMVMODE_0 MEMVMODE_1
1.8V GND +VDDC_CT
2.5V +VDDC_CT GND
2.8V +VDDC_CT +VDDC_CT
Wistron Corporation
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ATI(3 of 3)
SNIPE
Thursday, November 18, 2004
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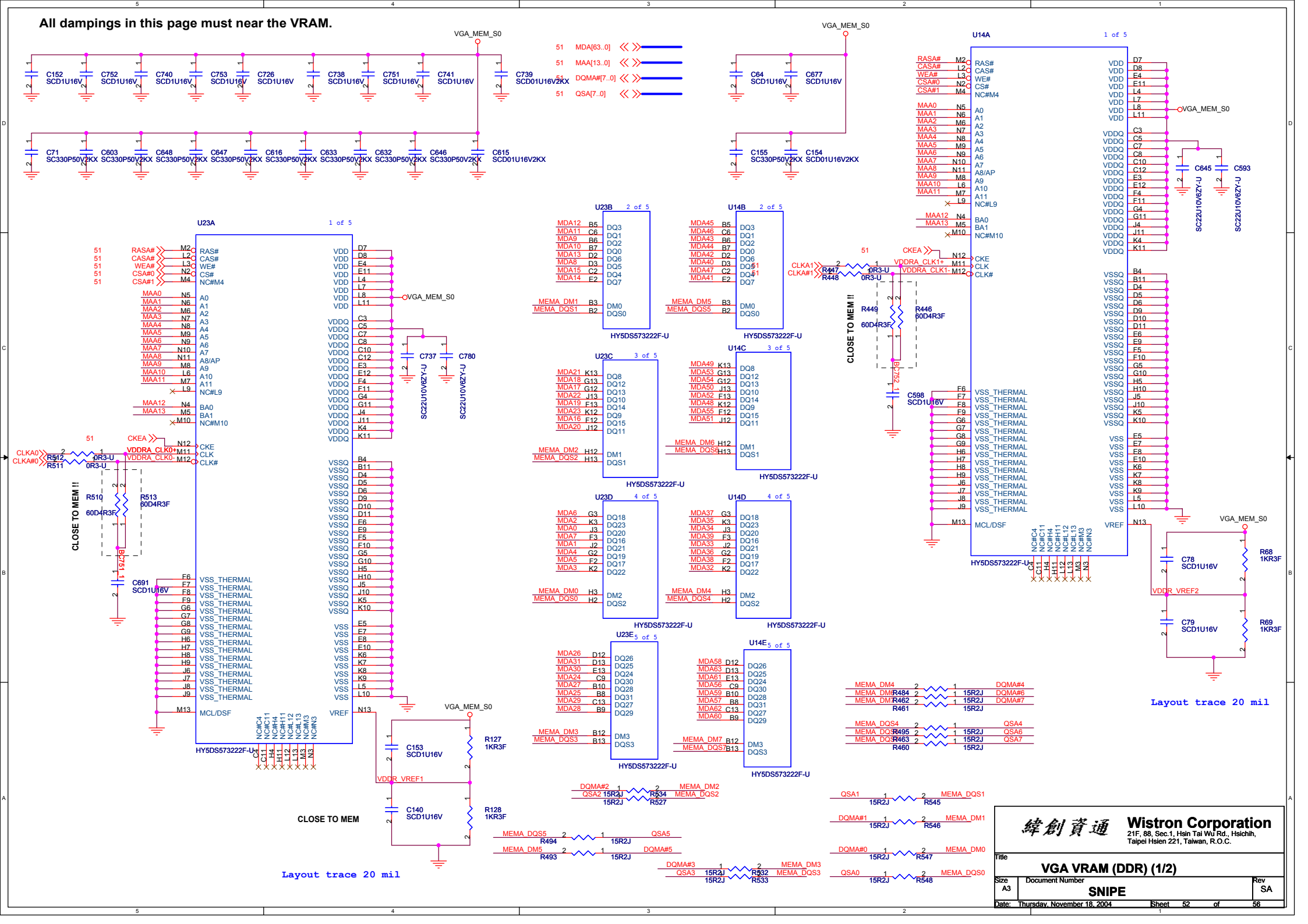
All dampings in this page must near the VRAM.



Wistron Corporation	緯創資通
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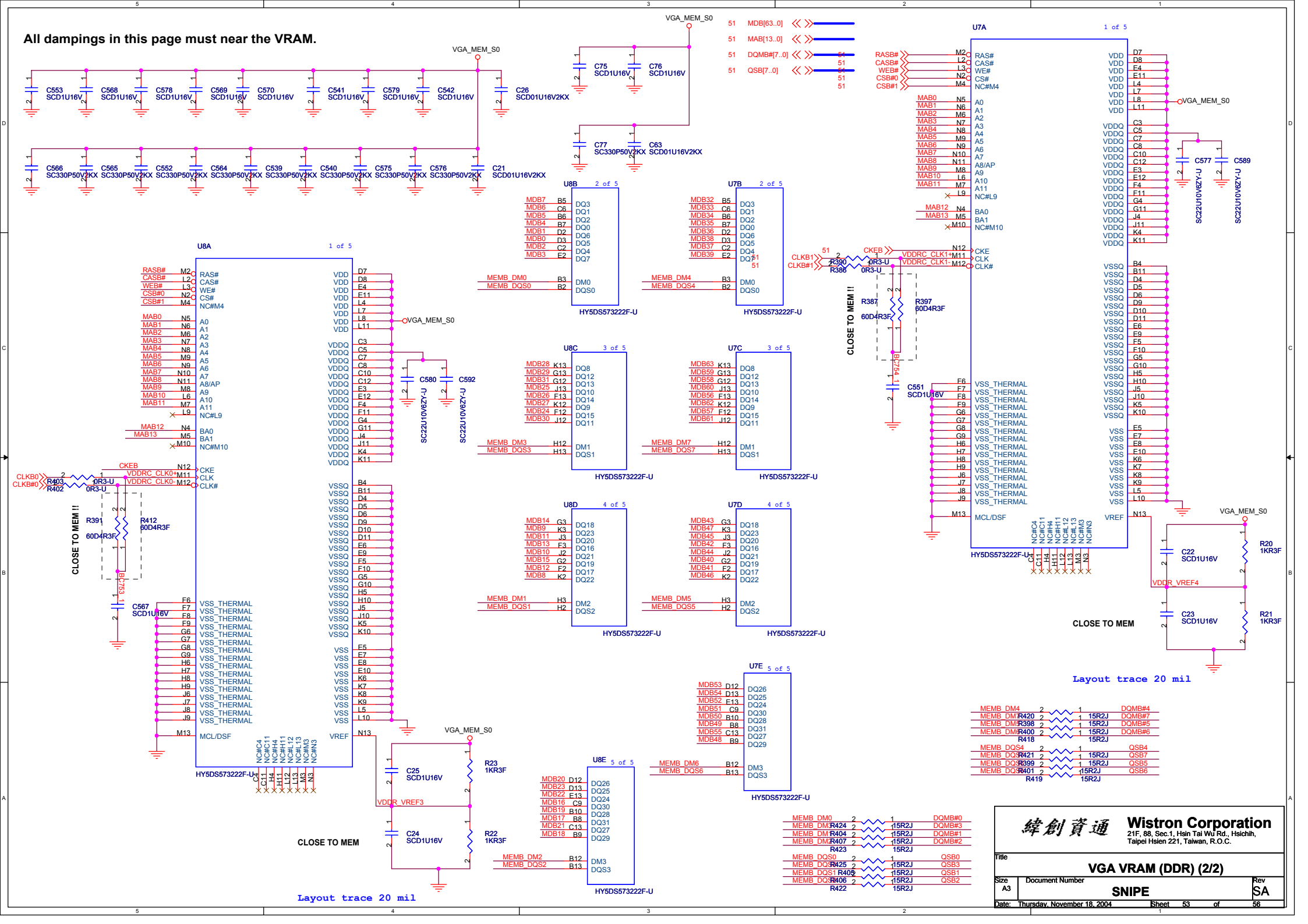
Title: VGA VRAM (DDR) (1/2)	
Size: A3	Document Number: SNIPE	Rev: SA
Date: Thursday, November 18, 2004	Sheet 52 of 56	

All dampings in this page must near the VRAM.



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	VGA VRAM (DDR) (2/2)
Size A3	Document Number SNIPE
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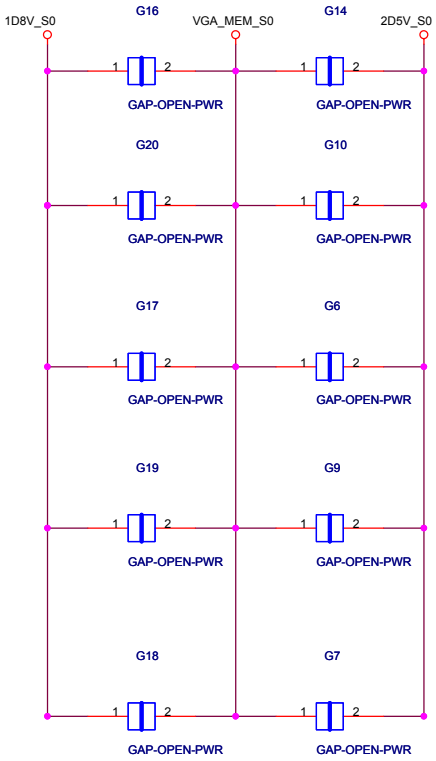
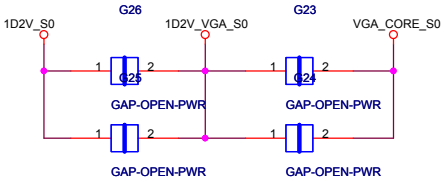
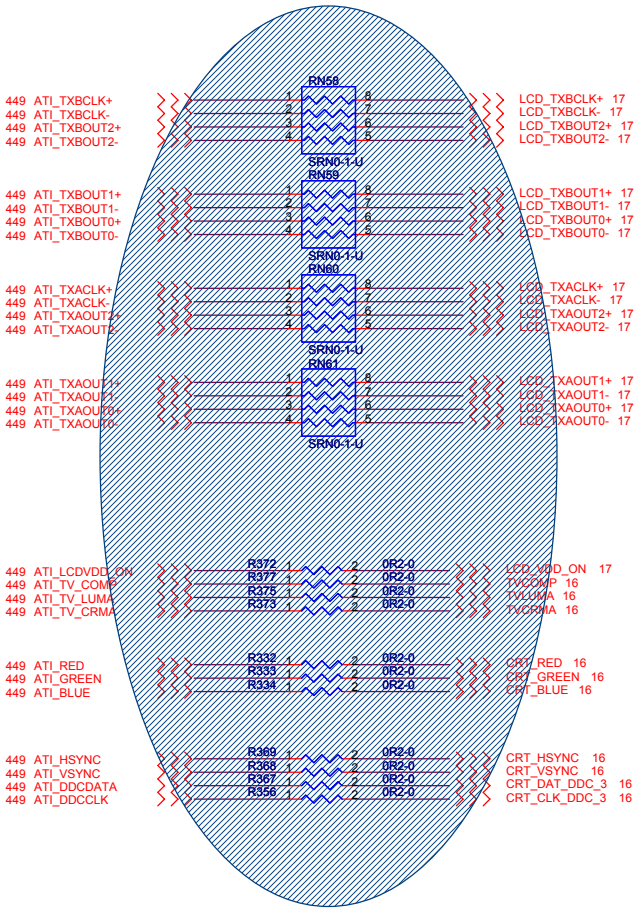
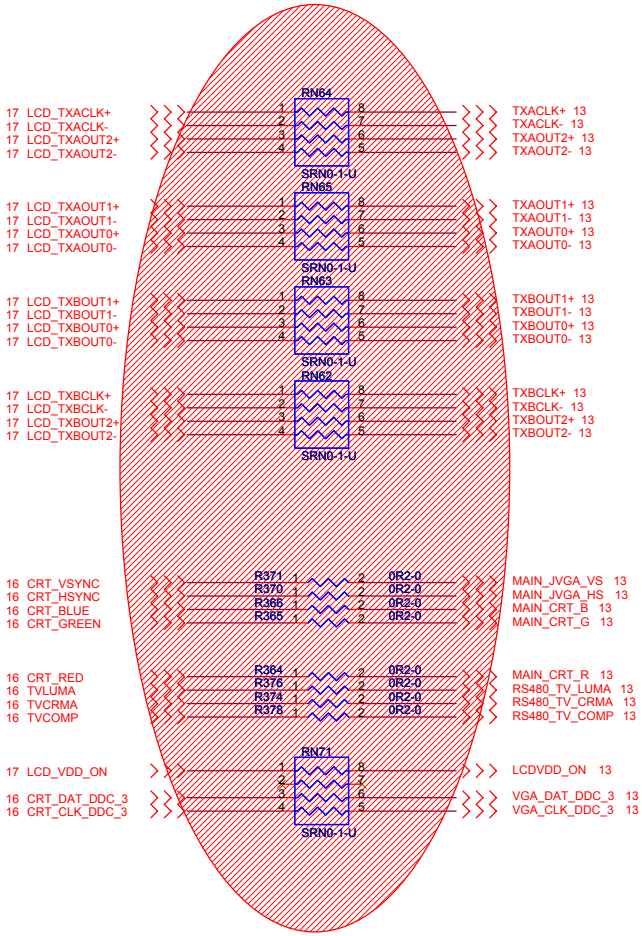
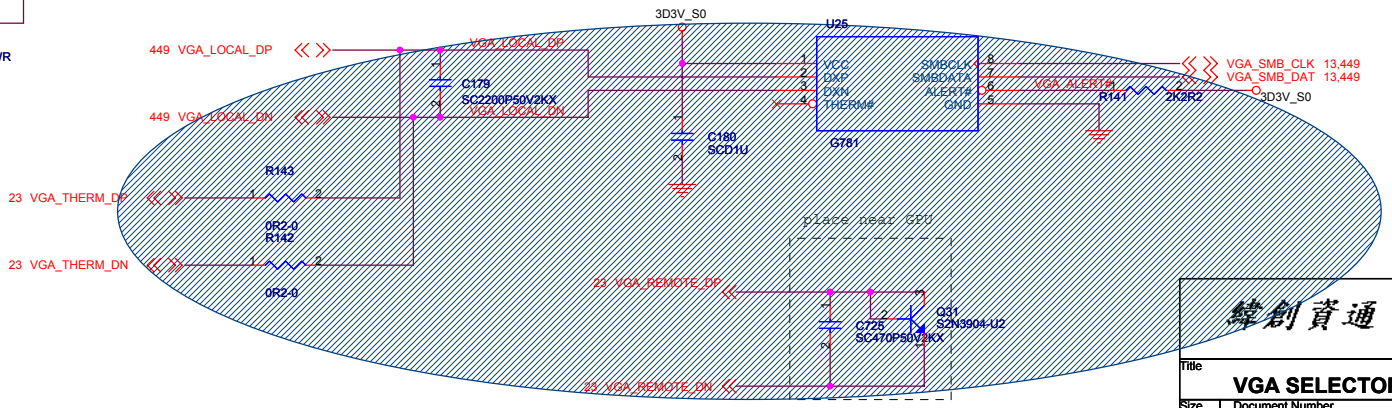
Date: Thursday, November 18, 2004	Sheet 53 of 56











緯創資通 Wistron Corporation
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Title: **VGA SELECTOR**

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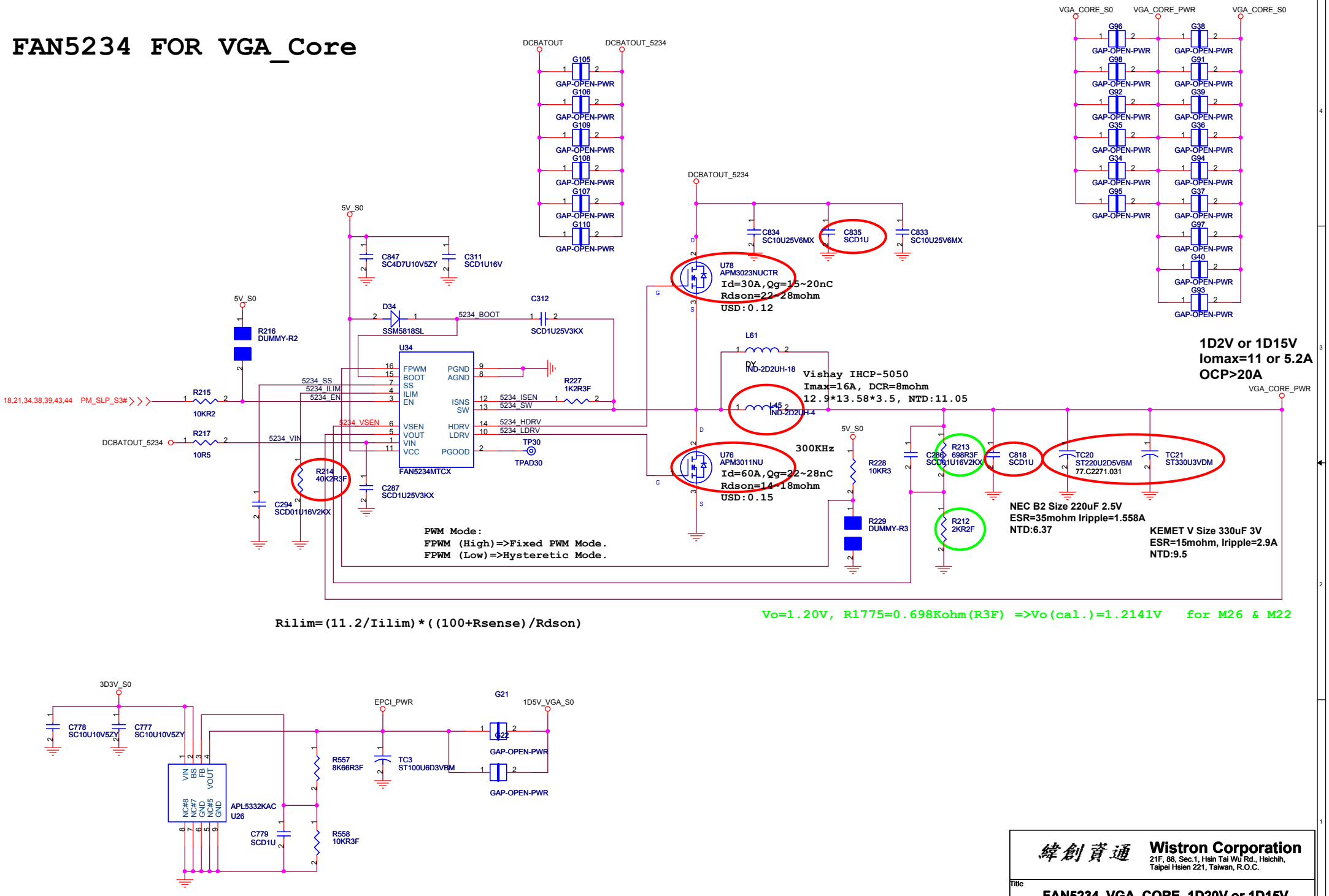
FAN5234 FOR VGA_Core



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**FAN5234_VGA_CORE_1D20V or 1D15V**	
Size: A3	Document Number: **SNIPE**	Rev: SA
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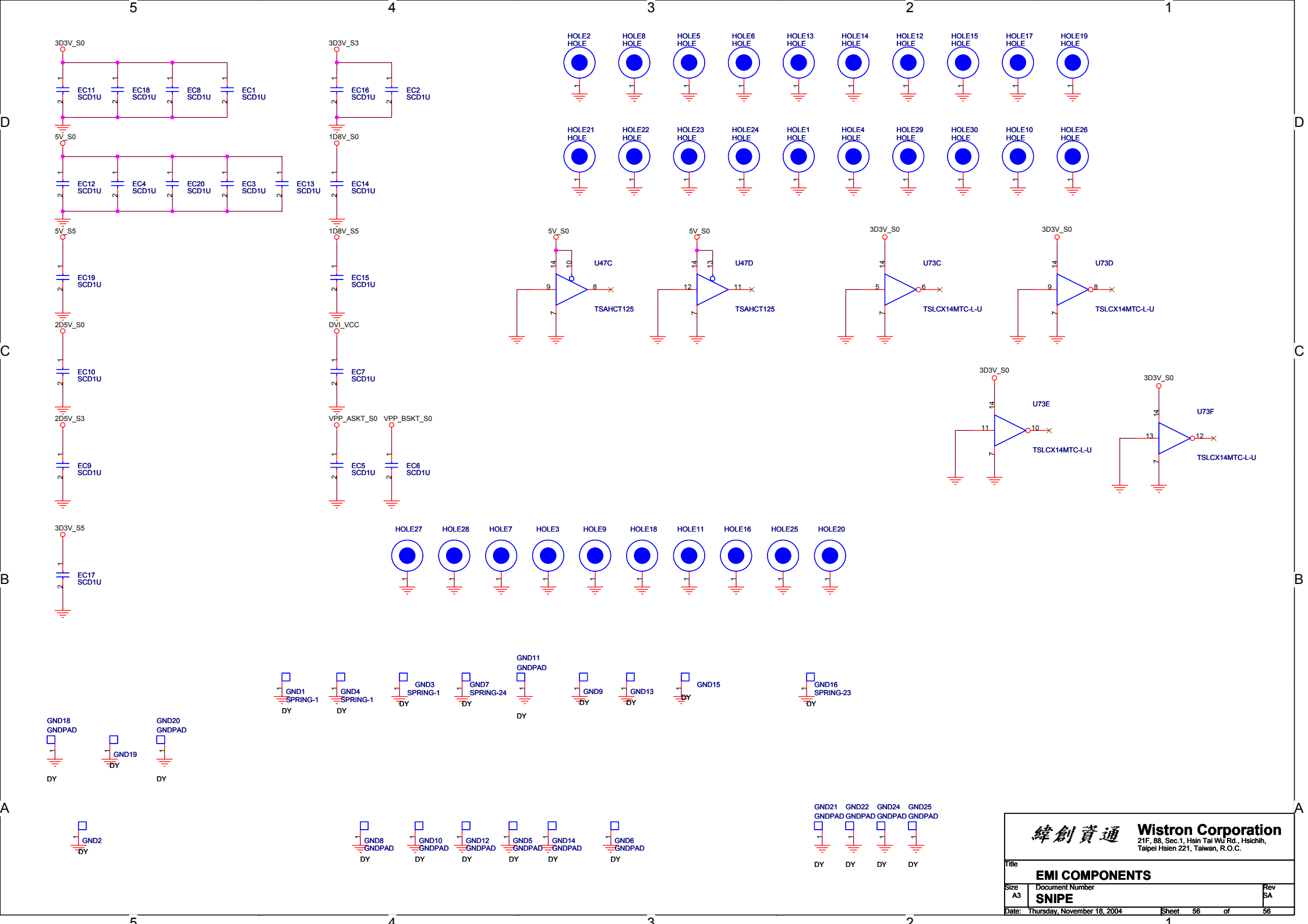

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Title: **EMI COMPONENTS**

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