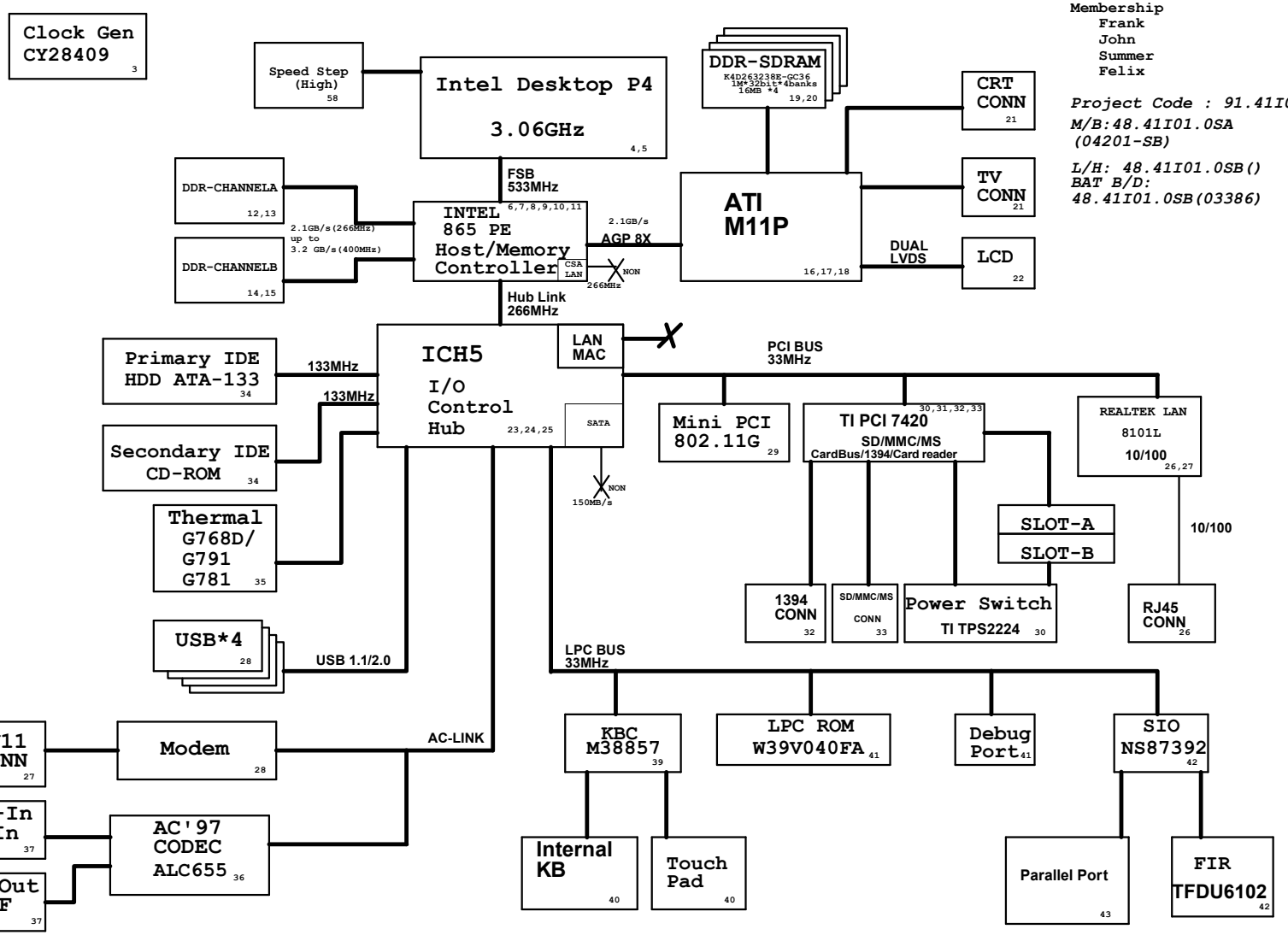
2003/01/07

Membership
Frank
John
Summer
Felix

Project Code : 91.41I01.001
M/B:48.41I01.0SA (04201-SB)
L/H: 48.41I01.0SB()
BAT B/D: 48.41I01.0SB(03386)



POWER BOARD

SYSTEM DC/DC

MAX1999 49

INPUT	OUTPUT
DCBATOUT	5V_S5
MAX1999_LDO5	3D3V_S5 +5V_UP_S5

CHARGER

Tiny12 / MAX1645 51

INPUT	OUTPUT
AD+ or BT+	DCBATOUT
AD+	BT+

SYSTEM DC/DC

MAX1999 / FDS9412 /TPS5130 / APL5308-18A 18

INPUT	OUTPUT
1D5V_S5	1D5V_S0 1D5V_AGP_S0 1D8V_S0
3D3V_S0	
2D5V_S3	2D5V_S0
3D3V_S5	3D3V_S3 3D3V_S0 3D3V_LAN_S5
5V_S5	5V_S3 5V_S0
DCBATOUT	2D5V_S3 1D5V_S5 NVVDD_AGP_S0

DDR & VDDR DC/DC

TPS5130 P.47/ APL5331 P.55/

INPUT	OUTPUT
DCBATOUT	DDR_VDD = 2D5V_S3
2D5V_S3	DDR_VTT = 1D25V_S0

CPU VCC_CORE DC/DC

DESKTOP CPU

Controller-ISL6247 P.44 / Drive-ISL6207 * 3 (3 Phase)

INPUT	OUTPUT
DCBATOUT	VCC_CORE
RANGE	RANGE
9V~20V	1.1Vcore~1.85Vcore
V_VID	V_AGTL+ BUS
1D2V_VID(Northwood only) VCC_CORE	VCC_CORE

(NORTHWOOD) CPU only

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: Block diagram
Size: Custom | Document Number: YuhinaME | Rev: SB
Date: Wednesday, January 07, 2004 | Sheet 1 of 58

PCI device TABLE

DEVICE	IDSEL	PCI IRQ	REQ# / GNT#	DEVICE NO.	BUS	FUNC
Mini-PCI	AD22	P_IRQC#	REQ3#/GNT3#	6	2	0
LAN REL8101L	AD21	P_IRQD#	REQ4#/GNT4#	5	2	0
CARDBUS / 1394	AD20	P_IRQE# / P_IRQF#, P_IRQG# / P_IRQH#	REQ1#/GNT1#	4	2	0
AGP(VGA)		P_IRQA#	AGP_REQ# / AGP_GNT#			
HUB I/F to PCI bridge	AD14			30	0	0
PCI to LPC bridge	AD15			31	0	0
IDE Controller	AD15			31	0	1
SMBUS	AD15			31	0	3
AC'97 Audio controller	AD15			31	0	5
AC'97 Modem controller	AD15			31	0	6
USB UHCI Controller#1	AD13			29	0	0
USB UHCI Controller#2	AD13			29	0	1
USB UHCI Controller#3	AD13			29	0	2
USB 2.0 EHCI Controller	AD13			29	0	7
SATA Controller (reserve)	AD15			31	0	2

3,4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44,47,50,53,54,56,57,58 3D3V_S0

32 1394_AVDD

33 3D3V_CARD_S0

30,31 A_SKT_VCC_S0

30 A_SKT_VPP

30 B_SKT_VPP

30,31 B_SKT_VCC_S0

25,47,49,52,53,55 5V_S5

22,51,52,53,57 +5V_UP_S5

35,38,47,50,53,57 5V_AUX_S5

49,53 MAX1999_LDO5

28 5V_USB1_S0

28 5V_USB3_S0

21,22,24,25,28,29,30,34,35,36,37,39,40,41,42,43,44,45,46,53,56,57,58 5V_S0

35 5V_G768_S0

36,37 5V_AUDIO_S0

37 MIC_VREF_S0

37 5VA_OP_S0

51,52,57 BT+

50,51,57 AD+

47,48 DCBATOUT1

44,45,46,57 DCBATOUT_ISL

10,22,35,45,47,49,51,53,57 DCBATOUT

18,48,57 1D2V_S0

4,44 1D2V_VID

7,8,12,14,55 DDR_VREF

12,13,55,57 1D25V_S0_A

14,15,55 1D25V_S0_B

6,10 VTT_GMCH

4,5,6,24,25,35,41,44,45,46,54 VCC_CORE

25,48,53 1D5V_S5

9,10,11,16,18,23,25,53,57 1D5V_S0

26 2D5V_LAN_S5

7,10,12,14,48,53,55,57 2D5V_S3

8,10 V_SMYRCOMP

8,10 V_SMYRCOMPVO

17,18,19,20,53 2D5V_S0

24 VCC_RTC_S5

24,25 RTC_AUX_S5

24 ICH_VBIAS

4,22,23,24,25,28,29,35,39,49,50,53,56,57 3D3V_S5

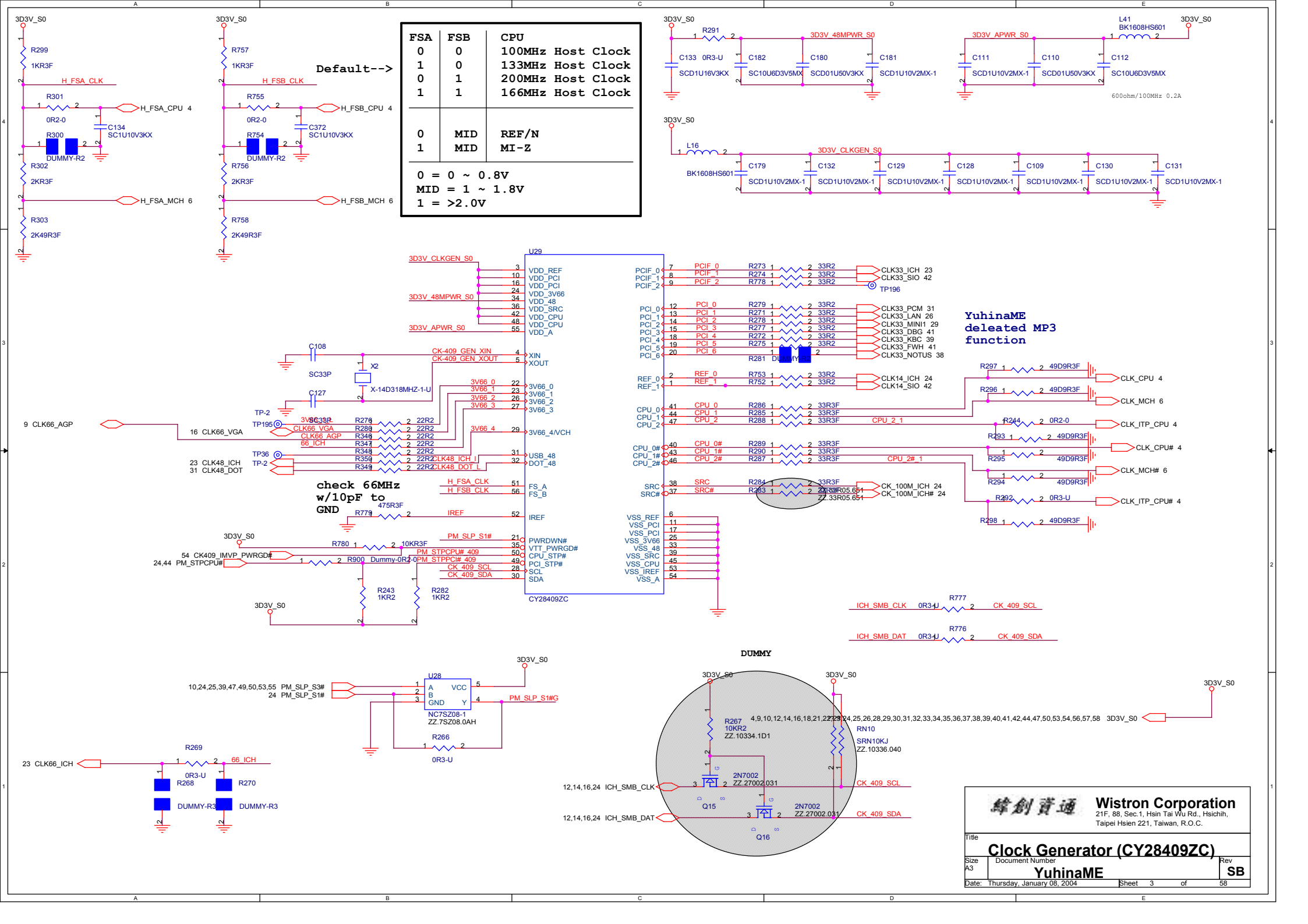
26,27,53 3D3V_LAN_S5

22,28,29,38,39,53,57 3D3V_S3

29 3D3V_BT_S0

22 LCDPOWER_S0

鋒創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**PCI device table**		
Size A3	Document Number **YuhinaME**		Rev **SB**
Date: Thursday, January 08, 2004	Sheet 2 of 58		


3D3V_S0
R299
1KR3F
H_FSA_CLK
R301
H_FSA_CPU 4
0R2-0
C134
SC1U10V3KX
R300
DUMMY-R2
R302
2KR3F
H_FSA_MCH 6
R303
2K49R3F
R757
1KR3F
H_FSB_CLK
R755
H_FSB_CPU 4
0R2-0
C372
SC1U10V3KX
R754
DUMMY-R2
R756
2KR3F
H_FSB_MCH 6
R758
2K49R3F
Default-->
FSA FSB CPU
0 0 100MHz Host Clock
1 0 133MHz Host Clock
0 1 200MHz Host Clock
1 1 166MHz Host Clock
0 MID REF/N
1 MID MI-Z
0 = 0 ~ 0.8V
MID = 1 ~ 1.8V
1 = >2.0V
R291
3D3V_48MPWR_S0
C133 0R3-U
C182
C180
C181
SCD1U16V3KX
SC10U6D3V5MX
SCD01U50V3KX
SCD1U10V2MX-1
3D3V_APWR_S0
L41
BK1608HS601
C111
C110
C112
SCD01U50V3KX
SC10U6D3V5MX
600ohm/100MHz 0.2A
L16
BK1608HS601
3D3V_CLKGEN_S0
C179
C132
C129
C128
C109
C130
C131
SCD1U10V2MX-1
U29
CY28409ZC
VDD_REF
VDD_PCI
VDD_PCI
VDD_3V66
VDD_48
VDD_SRC
VDD_CPU
VDD_CPU
VDD_A
XIN
XOUT
3V66_0
3V66_1
3V66_2
3V66_3
3V66_4/VCH
USB_48
DOT_48
FS_A
FS_B
IREF
PWRDWN#
VTT_PWRGD#
CPU_STP#
PCI_STP#
SCL
SDA
PCIF_0
PCIF_1
PCIF_2
PCI_0
PCI_1
PCI_2
PCI_3
PCI_4
PCI_5
PCI_6
REF_0
REF_1
CPU_0
CPU_1
CPU_2
CPU_0#
CPU_1#
CPU_2#
SRC
SRC#
VSS_REF
VSS_PCI
VSS_PCI
VSS_3V66
VSS_48
VSS_SRC
VSS_CPU
VSS_IREF
VSS_A
CLK33_ICH 23
CLK33_SIO 42
TP196
CLK33_PCM 31
CLK33_LAN 26
CLK33_MINI1 29
CLK33_DBG 41
CLK33_KBC 39
CLK33_FWH 41
CLK33_NOTUS 38
CLK14_ICH 24
CLK14_SIO 42
CK_100M_ICH 24
CK_100M_ICH# 24
CK-409_GEN_XIN
CK-409_GEN_XOUT
X2
X-14D318MHZ-1-U
SC33P
C108
C127
TP-2
TP195
TP36
CLK66_VGA
CLK66_AGP
66_ICH
CLK48_ICH_L
CLK48_DOT_L
9 CLK66_AGP
16 CLK66_VGA
23 CLK48_ICH
31 CLK48_DOT
check 66MHz w/10pF to GND
475R3F
R779
PM_SLP_S1#
R780 10KR3F
54 CK409_IMVP_PWRGD#
24,44 PM_STPCPU#
R900 Dummy-0R2-0
PM_STPCPU# 409
PM_STPPCI# 409
CK_409_SCL
CK_409_SDA
R243 1KR2
R282 1KR2
R297 49D9R3F
R296 49D9R3F
R244 0R2-0
R293 49D9R3F
R295 49D9R3F
R294 49D9R3F
R292 0R3-U
R298 49D9R3F
CLK_CPU 4
CLK_MCH 6
CLK_ITP_CPU 4
CLK_CPU# 4
CLK_MCH# 6
CLK_ITP_CPU# 4
CPU_2_1
CPU_2#_1
YuhinaME
deleated MP3
function
ICH_SMB_CLK
ICH_SMB_DAT
R777
R776
U28
NC7SZ08-1
ZZ.7SZ08.0AH
10,24,25,39,47,49,50,53,55 PM_SLP_S3#
24 PM_SLP_S1#
PM_SLP_S1#G
R266 0R3-U
R269
23 CLK66_ICH
66_ICH
R268 0R3-U
R270
DUMMY-R3
DUMMY
R267 10KR2
ZZ.10334.1D1
RN10
SRN10KJ
ZZ.10336.040
4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44,47,50,53,54,56,57,58
2N7002
ZZ.27002.031
Q15
Q16
12,14,16,24 ICH_SMB_CLK
12,14,16,24 ICH_SMB_DAT
CK_409_SCL
CK_409_SDA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator (CY28409ZC)
Size A3
Document Number
YuhinaME
Rev SB
Date: Thursday, January 08, 2004
Sheet 3 of 58

BSEL1	BSEL0	FSB
L	H	133Mhz

U15C

1D2V_VID TRACE WIDTH NEED 12MILS

L:RATED I = 60mA
C:ESR < 0.3 OHM,
ESL < 5nH, +/-
20% TOLERANT

THERMDP&THERMDN靠拢它

PZ47803-U1
62.10053.051
BGA478-1-U1

U15D

CPU SKT P/N :
62.10053.061 AMP
62.10055.011
FOXCONN

PZ47803-U1
62.10053.051 BGA478-1-U1

CHECK

RESERVED FOR ITP

K2P-SC

< 3" from CPU

CHECK MOUNT OR UN-MOUNT

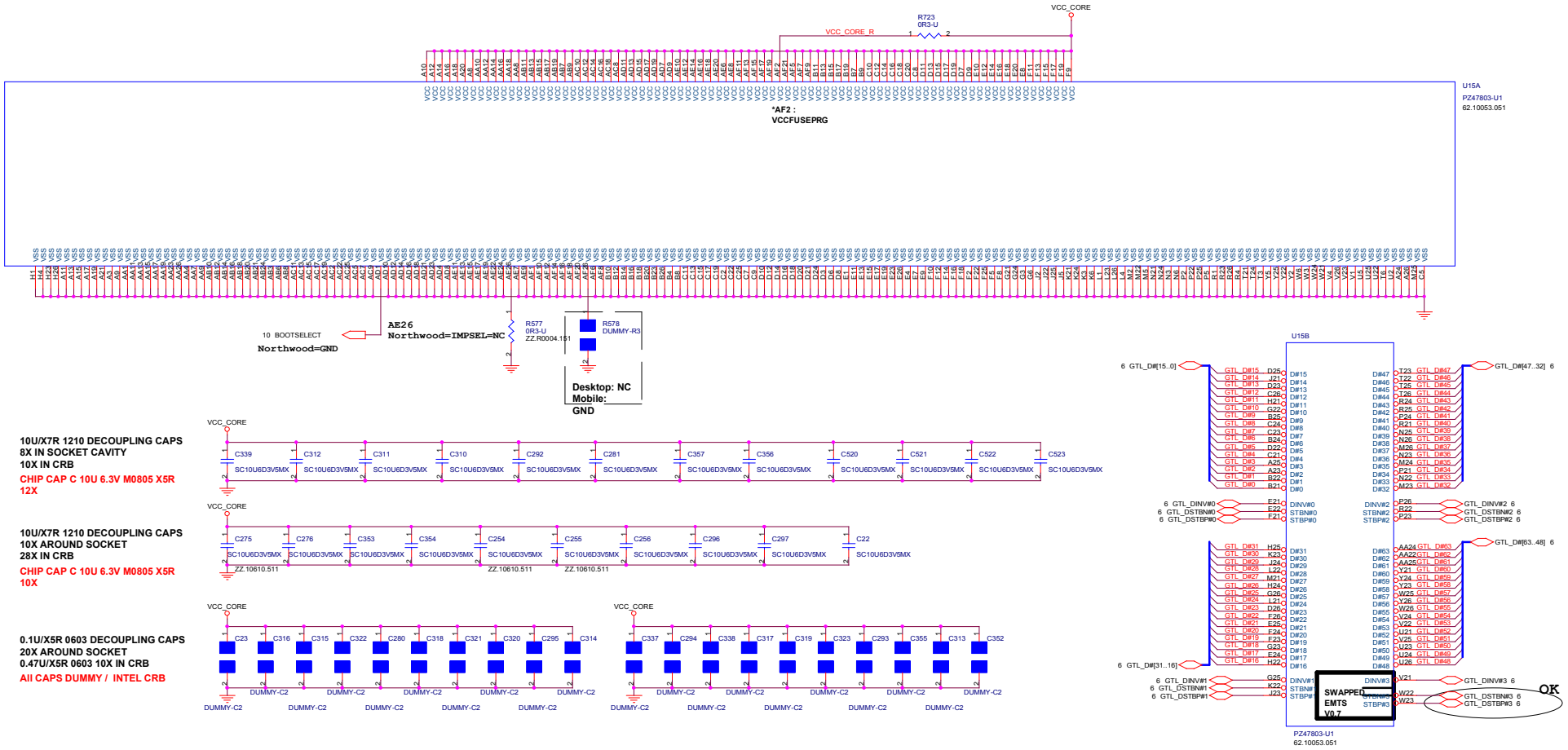
PULL TO 3.3V OR VCC_CORE??
Northwood EMTS rev0.5 P52

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU-Pentium4(1/2)

Size: A3 | Document Number: YuhinaME | Rev: SB

Date: Thursday, January 08, 2004 | Sheet 4 of 58

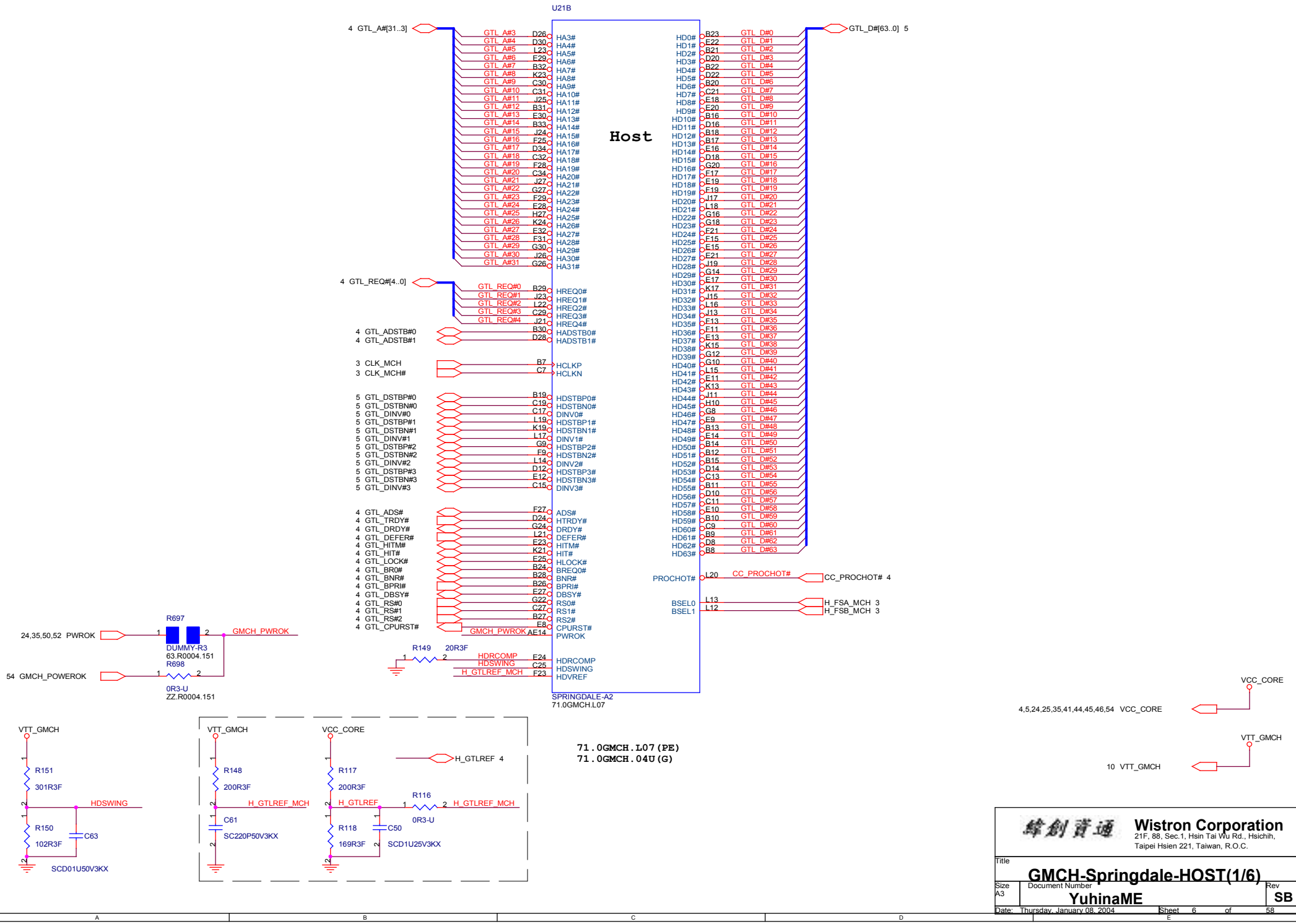


CHANGE NOTES			
CHANGE SC10U10V-U	P/N:78.10613.2A1	(1210)	(X7R)
	P/N:78.10620.221	(1206)	(X7R)
	P/N:78.10610.521	(1206)	(X5R)

VCC_CORE

4,6,24,25,35,41,44,45,46,54 VCC_CORE

緯創資通	Wistron Corporation	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU-Pentium4(2/2)	
Size A2	Document Number K2P-ATI	Rev SB
Date: Thursday, January 08, 2004	Sheet 5 of 58	


U21B
Host
4 GTL_A#[31..3]
GTL_A#3 D26 HA3#
GTL_A#4 D30 HA4#
GTL_A#5 L23 HA5#
GTL_A#6 E29 HA6#
GTL_A#7 B32 HA7#
GTL_A#8 K23 HA8#
GTL_A#9 C30 HA9#
GTL_A#10 C31 HA10#
GTL_A#11 J25 HA11#
GTL_A#12 B31 HA12#
GTL_A#13 E30 HA13#
GTL_A#14 B33 HA14#
GTL_A#15 J24 HA15#
GTL_A#16 F25 HA16#
GTL_A#17 D34 HA17#
GTL_A#18 C32 HA18#
GTL_A#19 F28 HA19#
GTL_A#20 C34 HA20#
GTL_A#21 J27 HA21#
GTL_A#22 G27 HA22#
GTL_A#23 F29 HA23#
GTL_A#24 E28 HA24#
GTL_A#25 H27 HA25#
GTL_A#26 K24 HA26#
GTL_A#27 E32 HA27#
GTL_A#28 E31 HA28#
GTL_A#29 G30 HA29#
GTL_A#30 J26 HA30#
GTL_A#31 G26 HA31#
4 GTL_REQ#[4..0]
GTL_REQ#0 B29 HREQ0#
GTL_REQ#1 J23 HREQ1#
GTL_REQ#2 L22 HREQ2#
GTL_REQ#3 C29 HREQ3#
GTL_REQ#4 J21 HREQ4#
4 GTL_ADSTB#0 B30 HADSTB0#
4 GTL_ADSTB#1 D28 HADSTB1#
3 CLK_MCH B7 HCLKP
3 CLK_MCH# C7 HCLKN
5 GTL_DSTBP#0 B19 HDSTBP0#
5 GTL_DSTBN#0 C19 HDSTBN0#
5 GTL_DINV#0 C17 DINV0#
5 GTL_DSTBP#1 L19 HDSTBP1#
5 GTL_DSTBN#1 K19 HDSTBN1#
5 GTL_DINV#1 L17 DINV1#
5 GTL_DSTBP#2 G9 HDSTBP2#
5 GTL_DSTBN#2 F9 HDSTBN2#
5 GTL_DINV#2 L14 DINV2#
5 GTL_DSTBP#3 D12 HDSTBP3#
5 GTL_DSTBN#3 E12 HDSTBN3#
5 GTL_DINV#3 C15 DINV3#
4 GTL_ADS# F27 ADS#
4 GTL_TRDY# D24 HTRDY#
4 GTL_DRDY# G24 DRDY#
4 GTL_DEFER# L21 DEFER#
4 GTL_HITM# E23 HITM#
4 GTL_HIT# K21 HIT#
4 GTL_LOCK# E25 HLOCK#
4 GTL_BR0# B24 BREQ0#
4 GTL_BNR# B28 BNR#
4 GTL_BPRI# B26 BPRI#
4 GTL_DBSY# E27 DBSY#
4 GTL_RS#0 G22 RS0#
4 GTL_RS#1 C27 RS1#
4 GTL_RS#2 B27 RS2#
4 GTL_CPURST# E8 CPURST#
GMCH_PWROK AE14 PWROK
R149 20R3F
HDRCOMP E24 HDRCOMP
HDSWING C25 HDSWING
H_GTLREF_MCH F23 HDVREF
SPRINGDALE-A2
71.0GMCH.L07
HD0# B23 GTL_D#0
HD1# E22 GTL_D#1
HD2# B21 GTL_D#2
HD3# D20 GTL_D#3
HD4# B22 GTL_D#4
HD5# D22 GTL_D#5
HD6# B20 GTL_D#6
HD7# C21 GTL_D#7
HD8# E18 GTL_D#8
HD9# E20 GTL_D#9
HD10# B16 GTL_D#10
HD11# D16 GTL_D#11
HD12# B18 GTL_D#12
HD13# B17 GTL_D#13
HD14# E16 GTL_D#14
HD15# D18 GTL_D#15
HD16# G20 GTL_D#16
HD17# F17 GTL_D#17
HD18# E19 GTL_D#18
HD19# F19 GTL_D#19
HD20# J17 GTL_D#20
HD21# L18 GTL_D#21
HD22# G16 GTL_D#22
HD23# G18 GTL_D#23
HD24# F21 GTL_D#24
HD25# E15 GTL_D#25
HD26# E15 GTL_D#26
HD27# E21 GTL_D#27
HD28# J19 GTL_D#28
HD29# G14 GTL_D#29
HD30# E17 GTL_D#30
HD31# K17 GTL_D#31
HD32# J15 GTL_D#32
HD33# L16 GTL_D#33
HD34# J13 GTL_D#34
HD35# F13 GTL_D#35
HD36# F11 GTL_D#36
HD37# E13 GTL_D#37
HD38# K15 GTL_D#38
HD39# G12 GTL_D#39
HD40# G10 GTL_D#40
HD41# L15 GTL_D#41
HD42# E11 GTL_D#42
HD43# K13 GTL_D#43
HD44# J11 GTL_D#44
HD45# H10 GTL_D#45
HD46# G8 GTL_D#46
HD47# E9 GTL_D#47
HD48# B13 GTL_D#48
HD49# E14 GTL_D#49
HD50# B14 GTL_D#50
HD51# B12 GTL_D#51
HD52# B15 GTL_D#52
HD53# D14 GTL_D#53
HD54# C13 GTL_D#54
HD55# B11 GTL_D#55
HD56# D10 GTL_D#56
HD57# C11 GTL_D#57
HD58# E10 GTL_D#58
HD59# B10 GTL_D#59
HD60# C9 GTL_D#60
HD61# B9 GTL_D#61
HD62# D8 GTL_D#62
HD63# B8 GTL_D#63
GTL_D#[63..0] 5
PROCHOT# L20 CC_PROCHOT#
CC_PROCHOT# 4
BSEL0 L13 H_FSA_MCH 3
BSEL1 L12 H_FSB_MCH 3
R697
24,35,50,52 PWROK
DUMMY-R3
63.R0004.151
GMCH_PWROK
R698
54 GMCH_POWEROK
0R3-U
ZZ.R0004.151
VTT_GMCH
R151
301R3F
HDSWING
R150
102R3F
C63
SCD01U50V3KX
VTT_GMCH
R148
200R3F
H_GTLREF_MCH
C61
SC220P50V3KX
VCC_CORE
H_GTLREF 4
R117
200R3F
H_GTLREF
R116
0R3-U
H_GTLREF_MCH
R118
169R3F
C50
SCD1U25V3KX
71.0GMCH.L07(PE)
71.0GMCH.04U(G)
VCC_CORE
4,5,24,25,35,41,44,45,46,54 VCC_CORE
VTT_GMCH
10 VTT_GMCH
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH-Springdale-HOST(1/6)
Size A3
Document Number
YuhinaME
Rev SB
Date: Thursday, January 08, 2004
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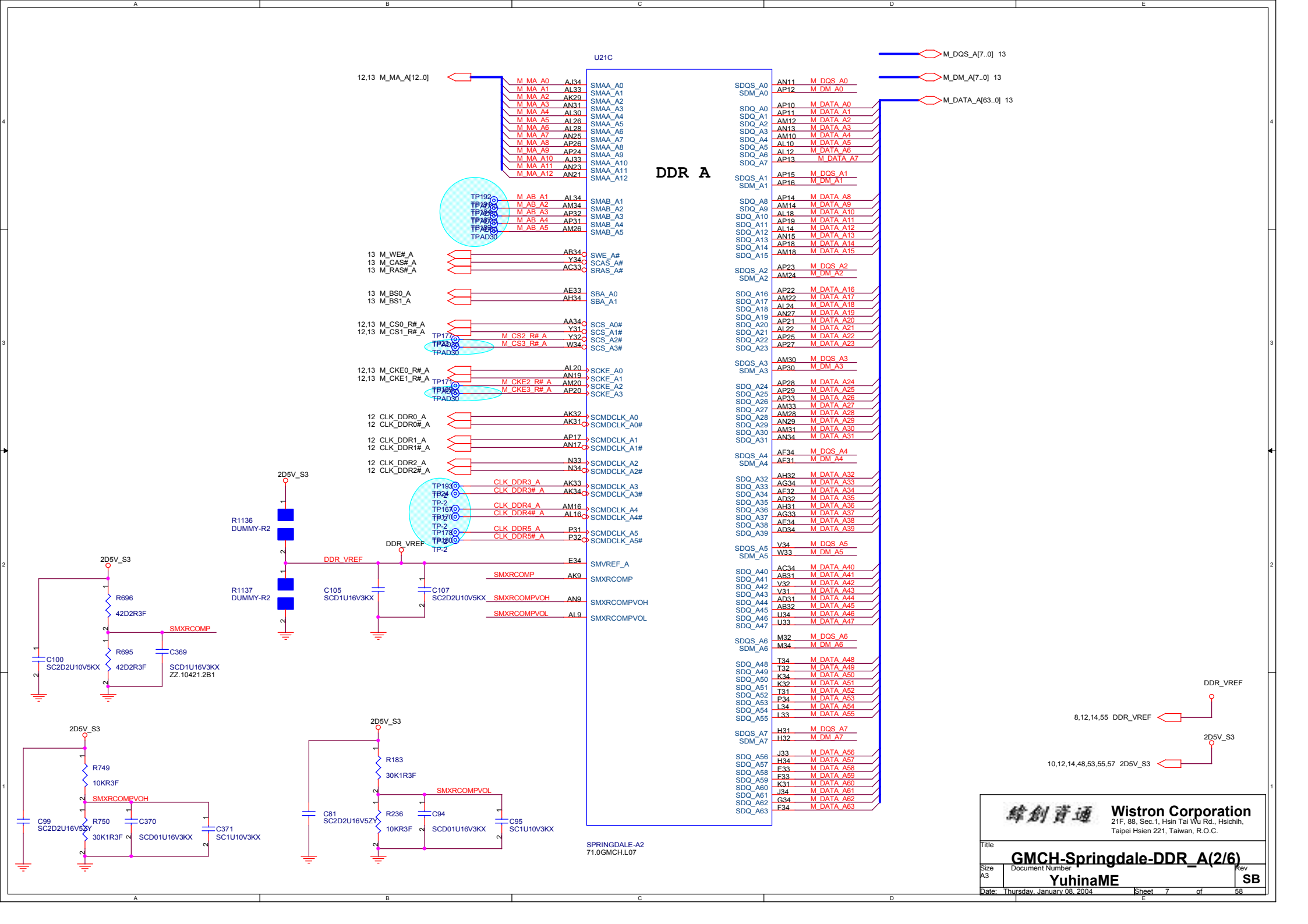
U21C
DDR A
SPRINGDALE-A2
71.0GMCH.L07
M_DQS_A[7..0] 13
M_DM_A[7..0] 13
M_DATA_A[63..0] 13
12,13 M_MA_A[12..0]
13 M_WE#_A
13 M_CAS#_A
13 M_RAS#_A
13 M_BS0_A
13 M_BS1_A
12,13 M_CS0_R#_A
12,13 M_CS1_R#_A
12,13 M_CKE0_R#_A
12,13 M_CKE1_R#_A
12 CLK_DDR0_A
12 CLK_DDR0#_A
12 CLK_DDR1_A
12 CLK_DDR1#_A
12 CLK_DDR2_A
12 CLK_DDR2#_A
2D5V_S3
R1136
DUMMY-R2
R1137
DUMMY-R2
DDR_VREF
C105
SCD1U16V3KX
C107
SC2D2U10V5KX
SMXRCOMP
SMXRCOMPVOH
SMXRCOMPVOL
R696
42D2R3F
R695
42D2R3F
C100
SC2D2U10V5KX
C369
SCD1U16V3KX
ZZ.10421.2B1
R749
10KR3F
C99
SC2D2U16V5ZY
R750
30K1R3F
C370
SCD01U16V3KX
C371
SC1U10V3KX
R183
30K1R3F
C81
SC2D2U16V5ZY
R236
10KR3F
C94
SCD01U16V3KX
C95
SC1U10V3KX
8,12,14,55 DDR_VREF
10,12,14,48,53,55,57 2D5V_S3
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH-Springdale-DDR_A(2/6)
Size A3
Document Number
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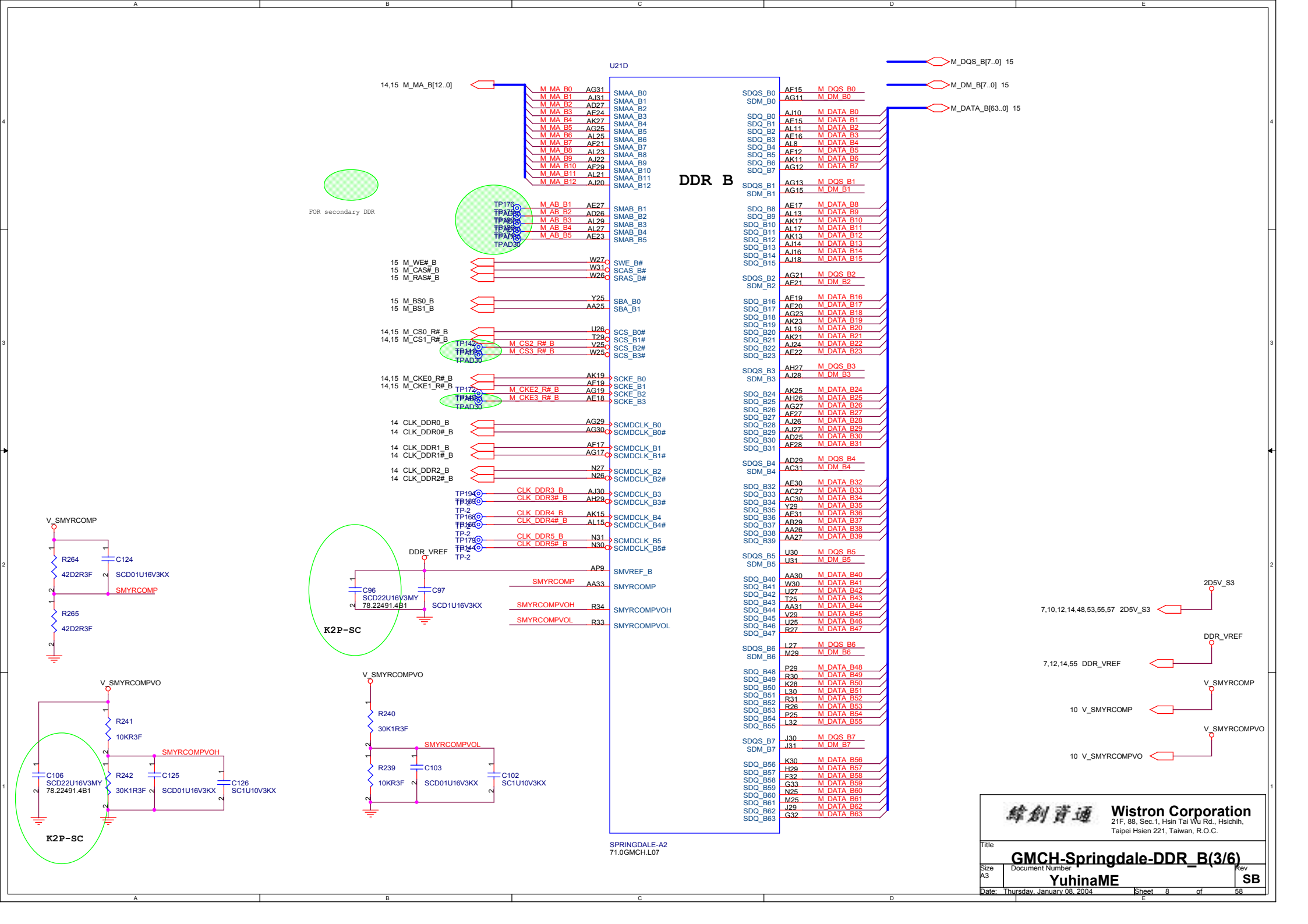
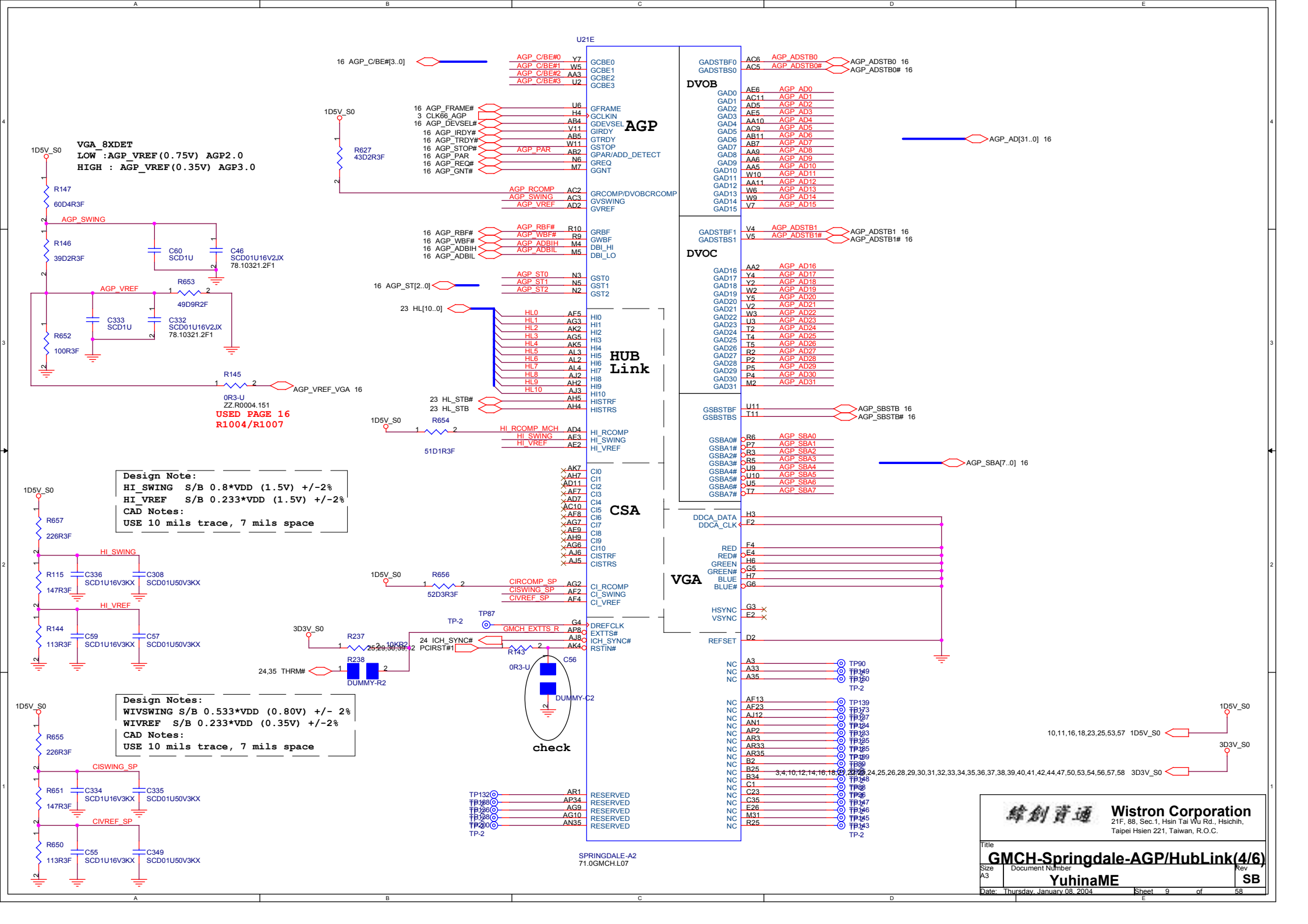
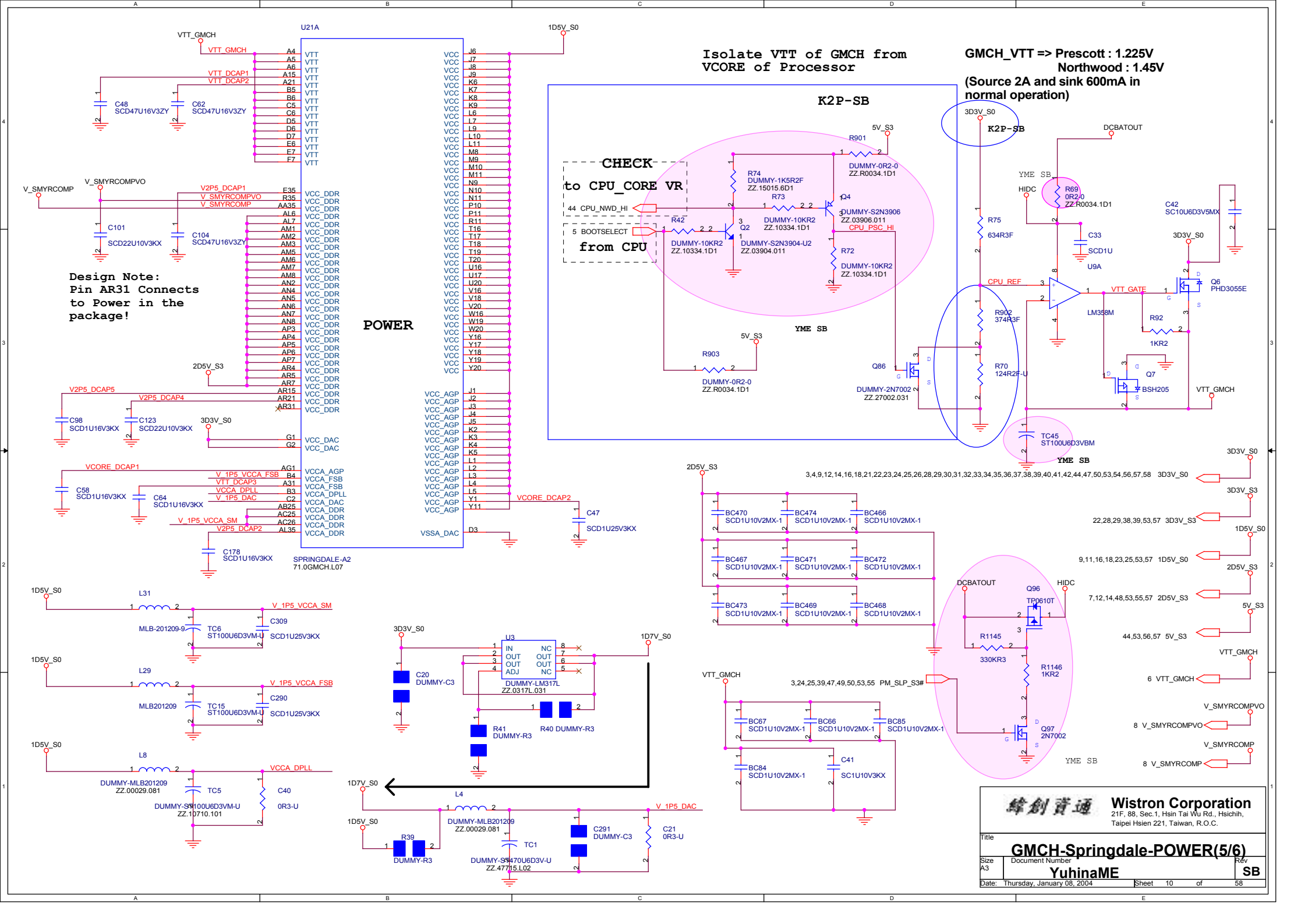
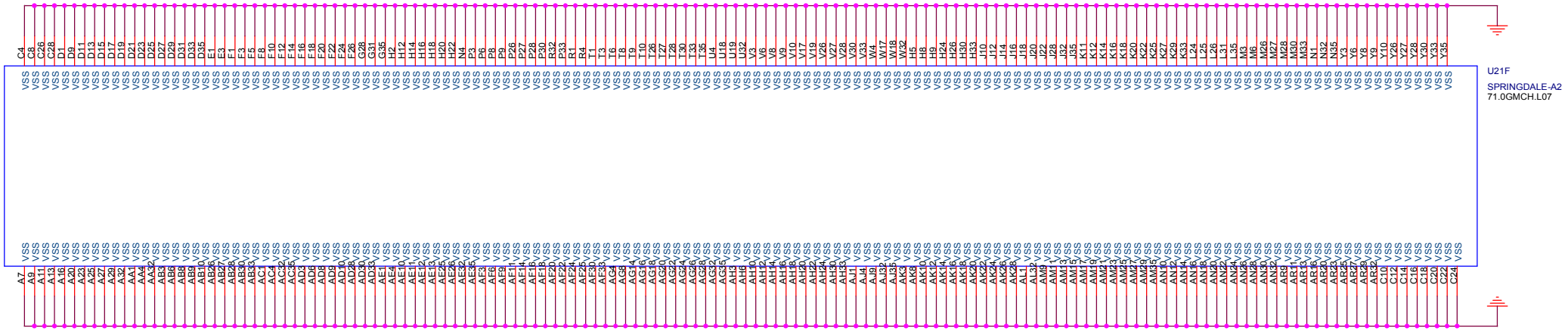
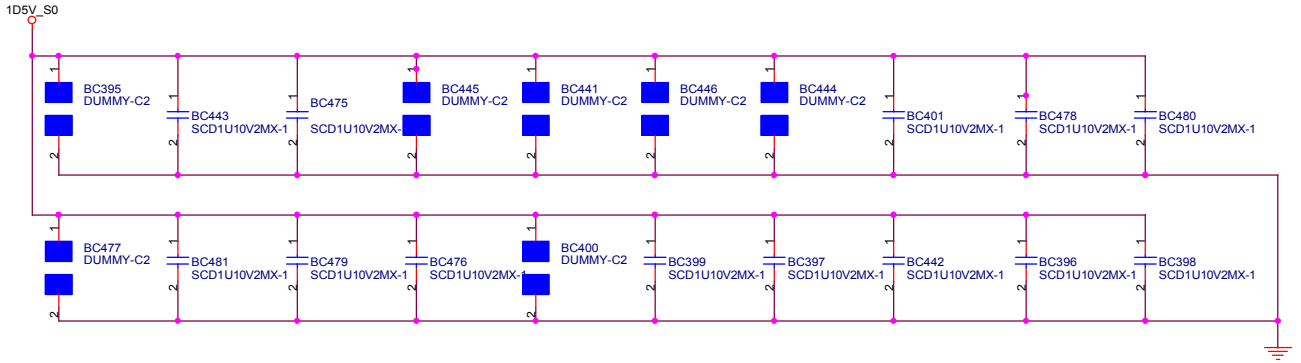
Date: Thursday, January 08, 2004
Sheet 7 of 58


U21D
DDR B
SPRINGDALE-A2
71.0GMCH.L07
FOR secondary DDR
K2P-SC
K2P-SC
V_SMYRCOMP
V_SMYRCOMPVO
V_SMYRCOMPVO
DDR_VREF
M_DQS_B[7..0] 15
M_DM_B[7..0] 15
M_DATA_B[63..0] 15
2D5V_S3
7,10,12,14,48,53,55,57 2D5V_S3
DDR_VREF
7,12,14,55 DDR_VREF
V_SMYRCOMP
10 V_SMYRCOMP
V_SMYRCOMPVO
10 V_SMYRCOMPVO
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH-Springdale-DDR_B(3/6)
Size A3
Document Number
YuhinaME
Rev SB
Date: Thursday, January 08, 2004
Sheet 8 of 58


U21E
AGP
HUB Link
CSA
VGA
DVOB
DVOC
SPRINGDALE-A2
71.0GMCH.L07
VGA_8XDET
LOW :AGP_VREF(0.75V) AGP2.0
HIGH : AGP_VREF(0.35V) AGP3.0
USED PAGE 16
R1004/R1007
Design Note:
HI_SWING S/B 0.8*VDD (1.5V) +/-2%
HI_VREF S/B 0.233*VDD (1.5V) +/-2%
CAD Notes:
USE 10 mils trace, 7 mils space
Design Notes:
WIVSWING S/B 0.533*VDD (0.80V) +/- 2%
WIVREF S/B 0.233*VDD (0.35V) +/-2%
CAD Notes:
USE 10 mils trace, 7 mils space
check
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
GMCH-Springdale-AGP/HubLink(4/6)
Size A3
Document Number YuhinaME
Rev SB
Date: Thursday, January 08, 2004
Sheet 9 of 58


U21A
POWER
SPRINGDALE-A2
71.0GMCH.L07
Design Note:
Pin AR31 Connects
to Power in the
package!
Isolate VTT of GMCH from
VCORE of Processor
GMCH_VTT => Prescott : 1.225V
Northwood : 1.45V
(Source 2A and sink 600mA in
normal operation)
K2P-SB
CHECK
to CPU_CORE VR
from CPU
YME SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
GMCH-Springdale-POWER(5/6)
YuhinaME
SB
Thursday, January 08, 2004
Sheet 10 of 58



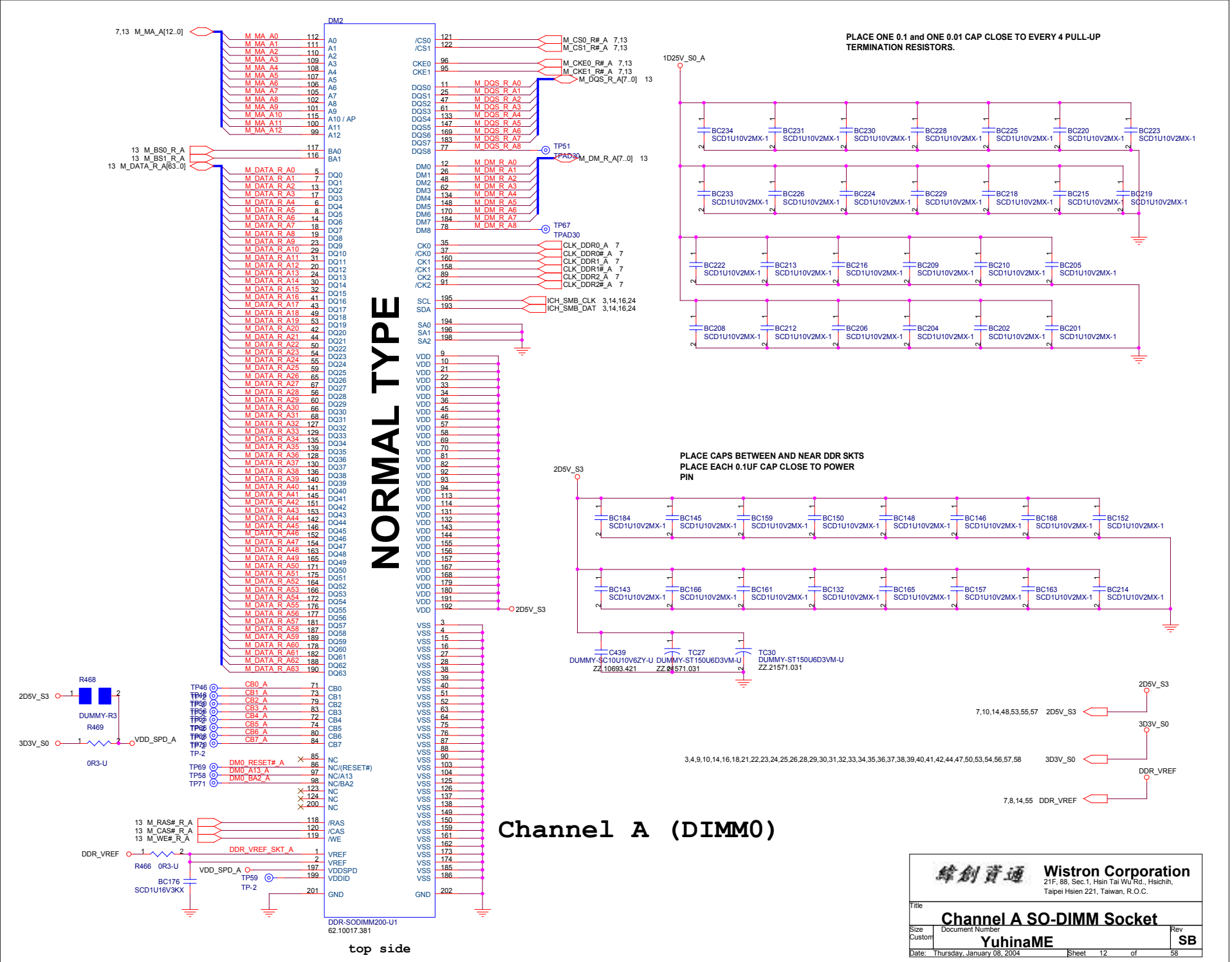


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: GMCH-Springdale-GND Power(6/6)

Size: A3 | Document Number: YuhinaME | Rev: SB

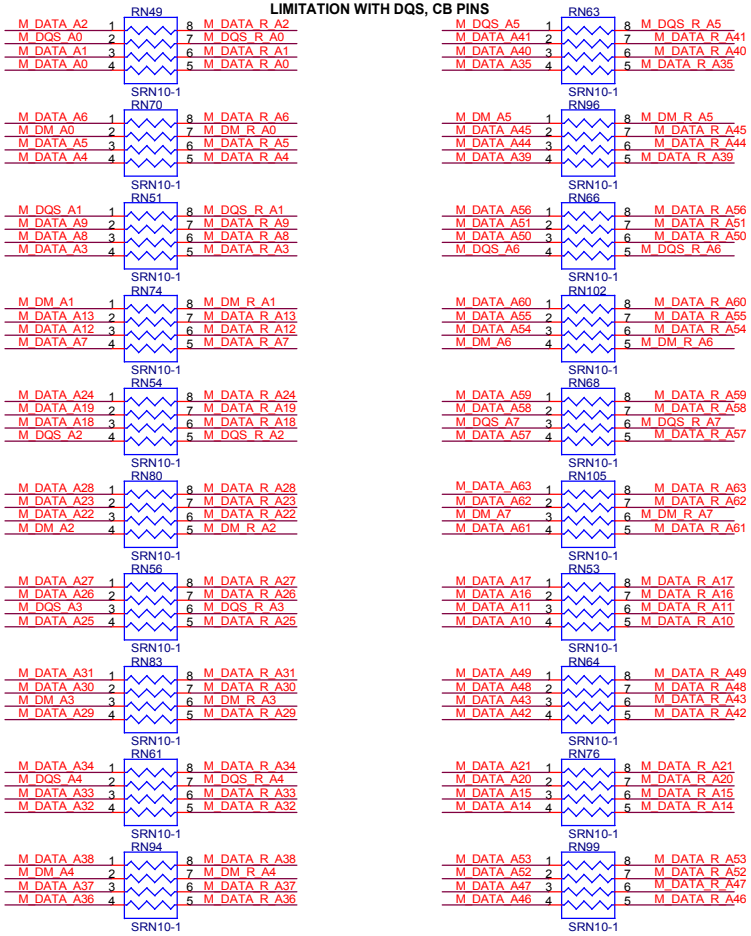
Date: Thursday, January 08, 2004 | Sheet 11 of 58



Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Channel A SO-DIMM Socket
Size: Custom	Document Number: YuhinaME
Rev	SB
Date: Thursday, January 08, 2004	Sheet 12 of 58

SERIES DAMPING

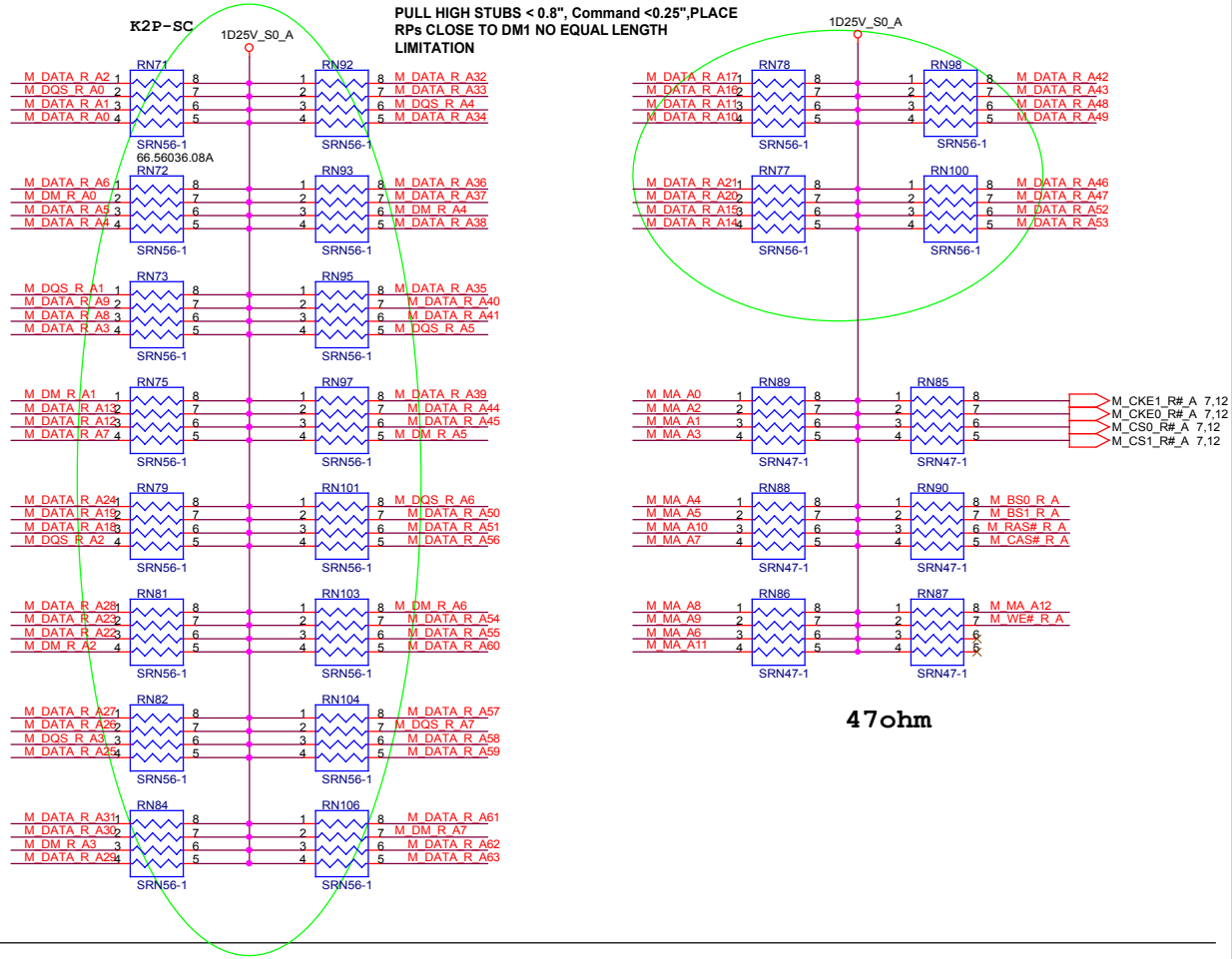
PLACE RNs CLOSE TO DM0, < 0.75"
STRICT EQUAL LENGTH
LIMITATION WITH DQS, CB PINS



PARALLEL TERMINATION

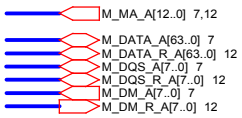
PULL HIGH STUBS < 0.8", Command <0.25",PLACE
RPs CLOSE TO DM1 NO EQUAL LENGTH
LIMITATION

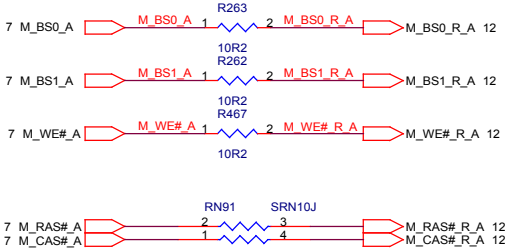
K2P-SC

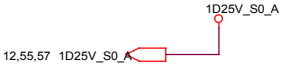


47ohm

Control signals use Topology 2







Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Channel A SO-DIMM TERMINATION

Size	Document Number	Rev
A3	YuhinaME	SB

Date: Thursday, January 08, 2004 Sheet 13 of 58

PLACE ONE 0.1 and ONE 0.01 CAP CLOSE TO EVERY 4
PULL-UP TERMINATION RESISTORS

PLACE CAPS BETWEEN AND NEAR DDR SKTS
PLACE EACH 0.1UF CAP CLOSE TO POWER
PIN

REVERSE TYPE

bot side

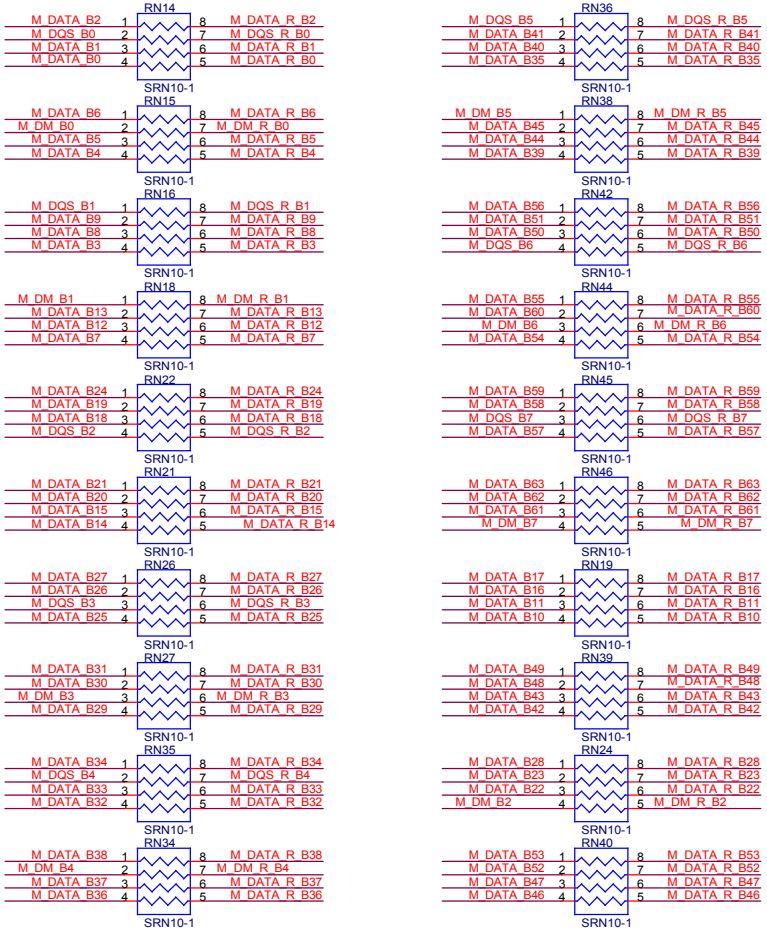
Channel B (DIMM0)

JAE-CONN200A-U
62.10017.371

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	Channel B SO-DIMM Socket
Size: Custom	Document Number: YuhinaME
Rev	SB
Date: Thursday, January 08, 2004	Sheet 14 of 58

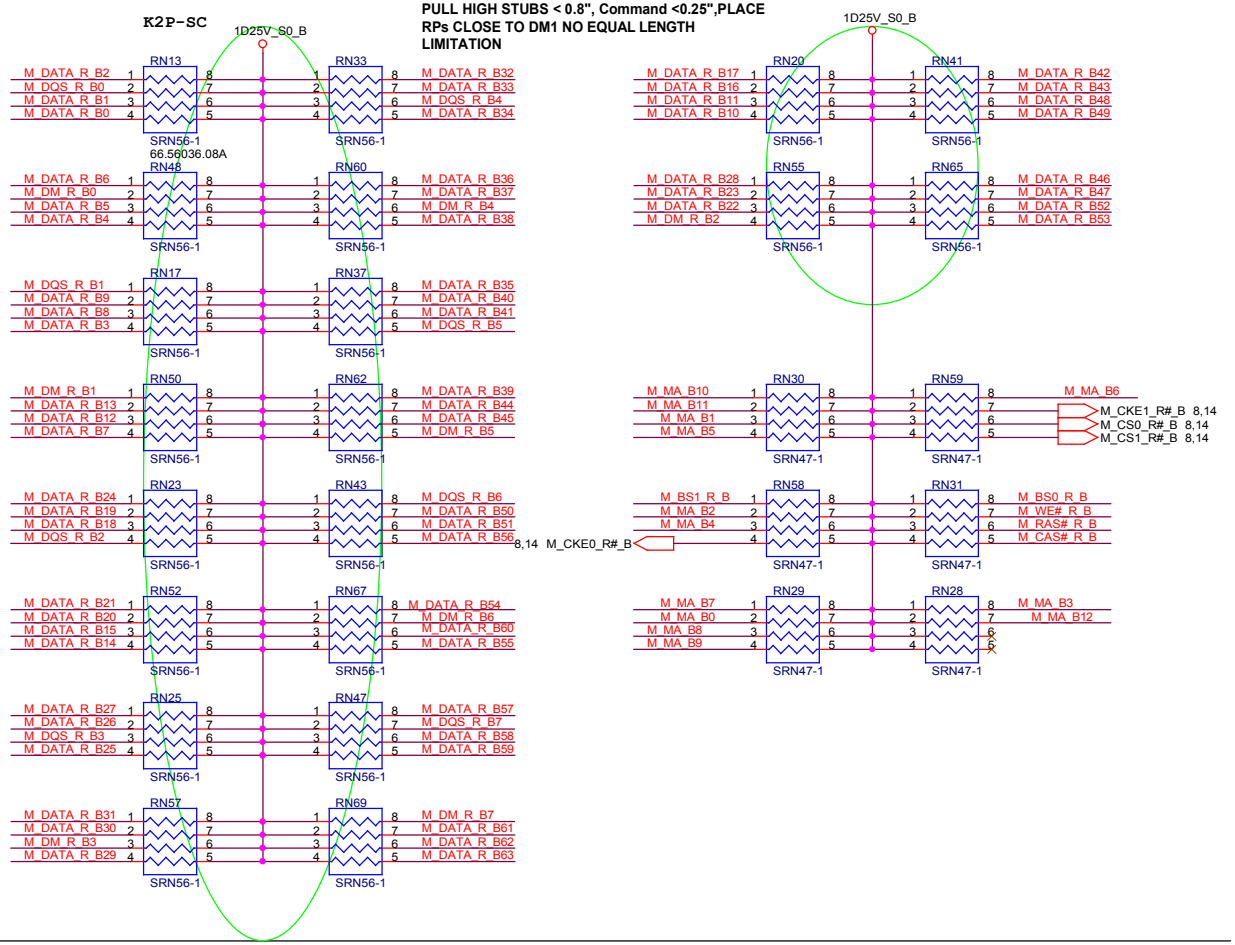
SERIES DAMPING

PLACE RNs CLOSE TO DM0, < 0.75"
STRICT EQUAL LENGTH
LIMITATION WITH DQS, CB PINS

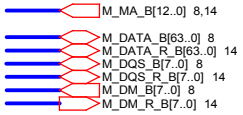


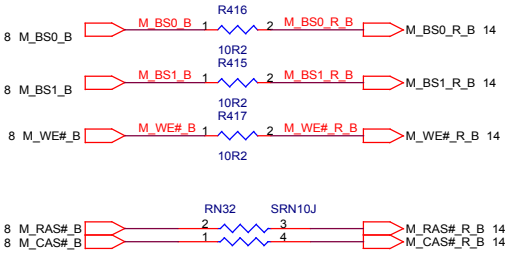
PARALLEL TERMINATION

PULL HIGH STUBS < 0.8", Command <0.25",PLACE
RPs CLOSE TO DM1 NO EQUAL LENGTH
LIMITATION



Control signals use Topology 2





Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Channel B SO-DIMM TERMINATION		
Size: A3	Document Number: YuhinaME	Rev: SB
Date: Thursday, January 08, 2004	Sheet 15 of 58	

Memory clocks Spread Spectrum support via the GPIO16 pin.

NEAR NB-MCH

1.5V x (0.715/(2.32+0.715)) = 0.3534V

Place this cap close to chip

YME SB

VRAM	DET1	DET0
32M	0	0
64M	0	1
128M	1	0

+-0.25/0.24%
C38=0.1uF,C37=270pF,R147=620ohm(+-0.5%)

Set AGP_VREF_VGA to 0.35V for AGP 3.0

Set AGP_VREF_VGA to 0.35V for AGP 3.0

Set AGP_VREF_VGA to VDDP/2 for AGP 2.0

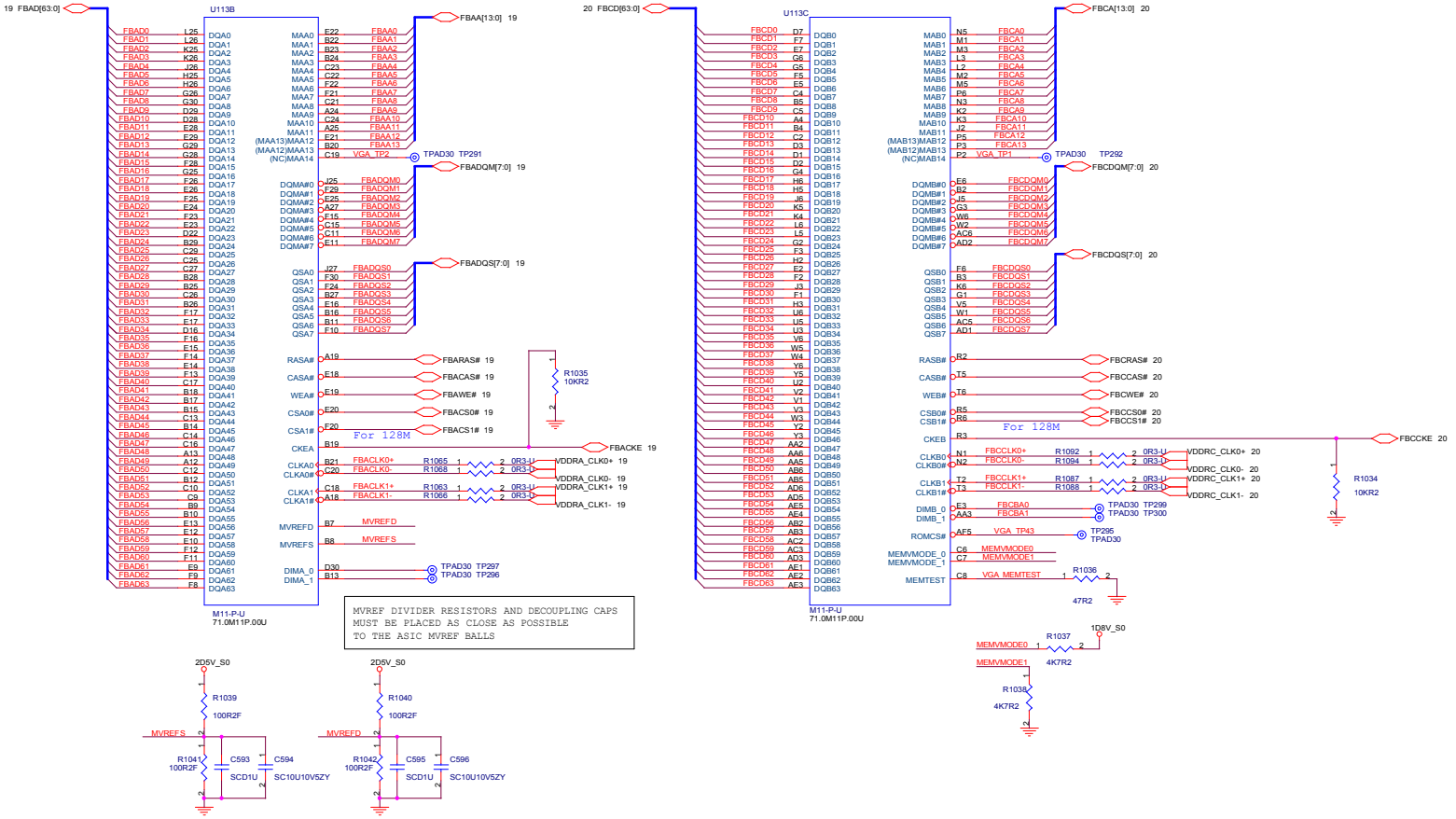
PULL DOWN FOR 8X
PULL UP FOR 4X

For AGP8X

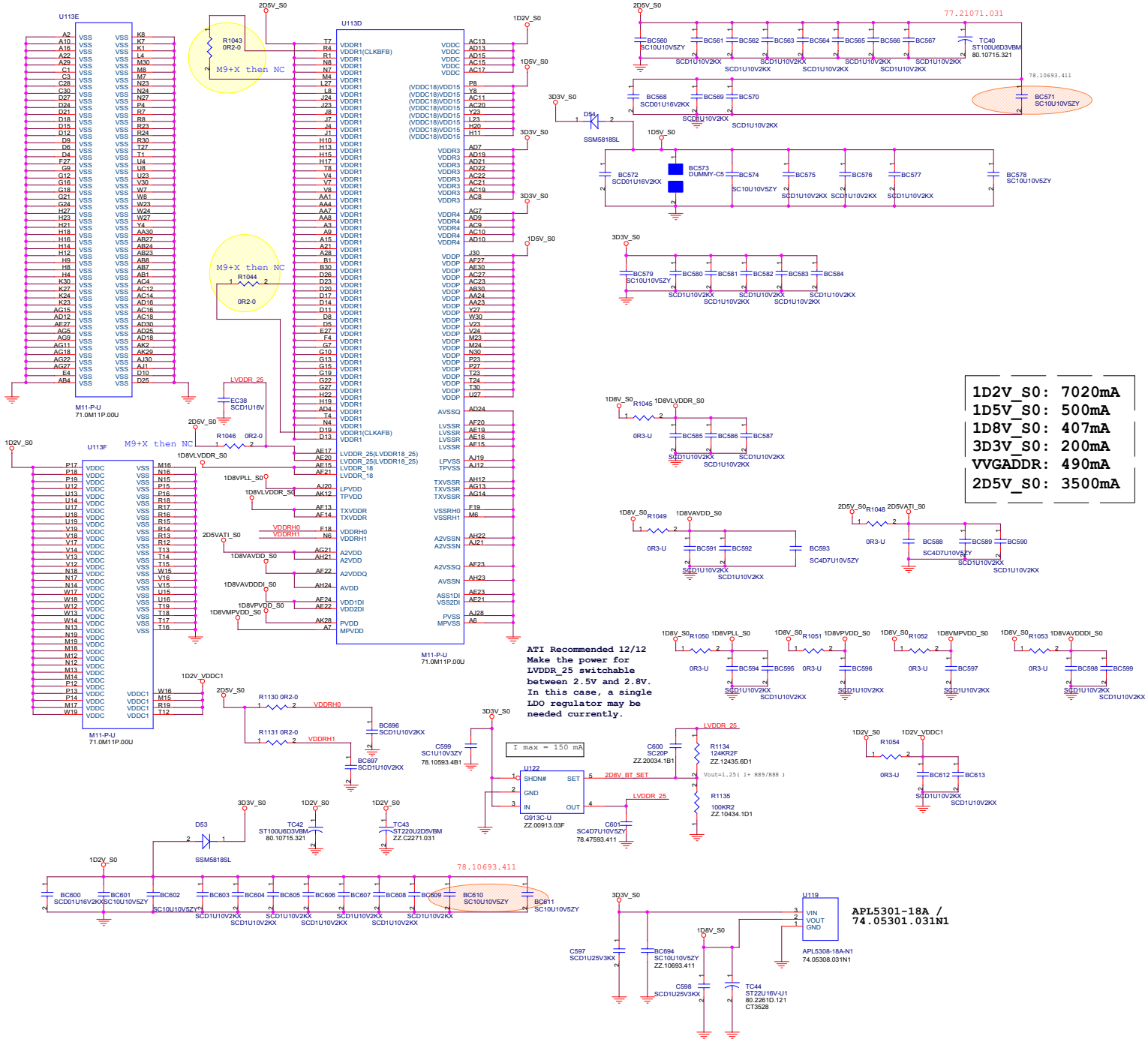
Don't forget to add 4.7 pull-ups (to 3.3V) on I2C pair.

Title	VGA(1/3) ATI M11-P HOST
Size	A3
Document Number	YuhinaME
Rev	SB
Date	Thursday, January 08, 2004
Sheet	16 of 58

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.



華創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VGA(2/3) ATI M11-P MEM***	
Size A2	Document Number YuhinaME	Rev **SB**
Date: Thursday, January 08, 2004	Sheet 17 of 58	


1D2V_S0: 7020mA
1D5V_S0: 500mA
1D8V_S0: 407mA
3D3V_S0: 200mA
VVGADDR: 490mA
2D5V_S0: 3500mA
ATI Recommended 12/12
Make the power for
LVDDR_25 switchable
between 2.5V and 2.8V.
In this case, a single
LDO regulator may be
needed currently.
APL5301-18A /
74.05301.031N1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VGA(3/3) ATI M11-P POWER
YuhinaME
SB
Thursday, January 08, 2004
Sheet 18 of 58

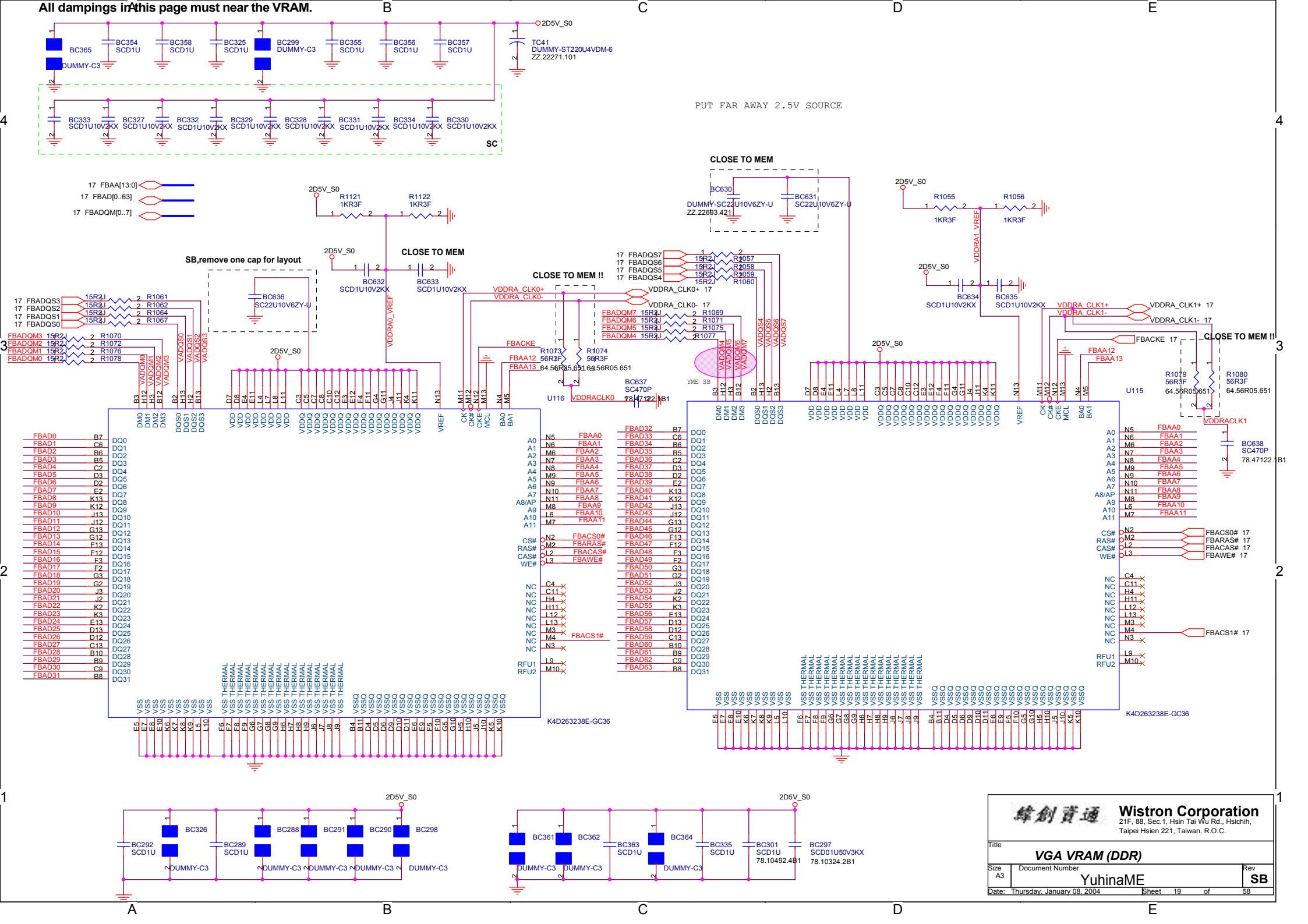
All dampings in this page must near the VRAM.

PUT FAR AWAY 2.5V SOURCE

SB,remove one cap for layout

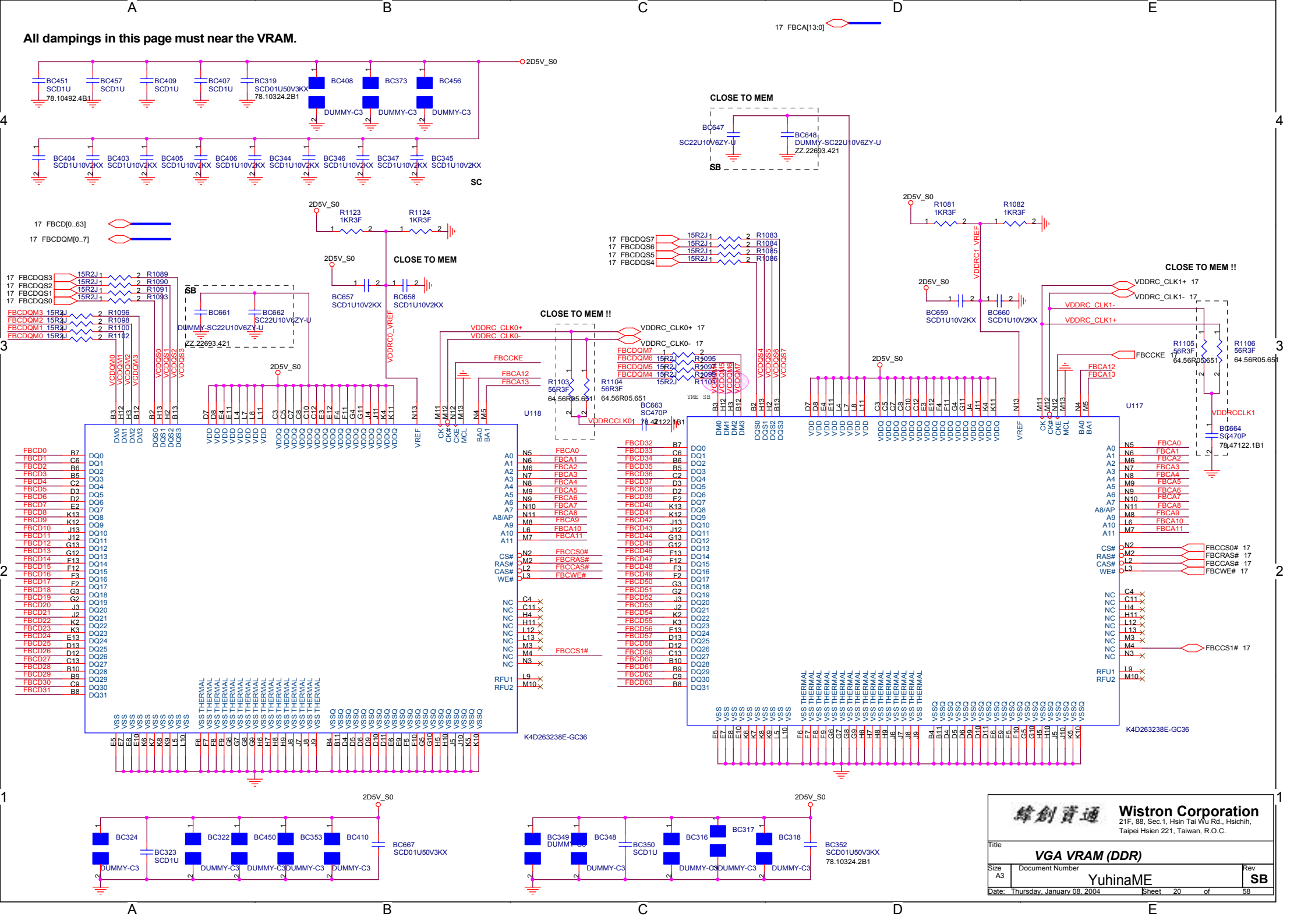
CLOSE TO MEM

CLOSE TO MEM !!



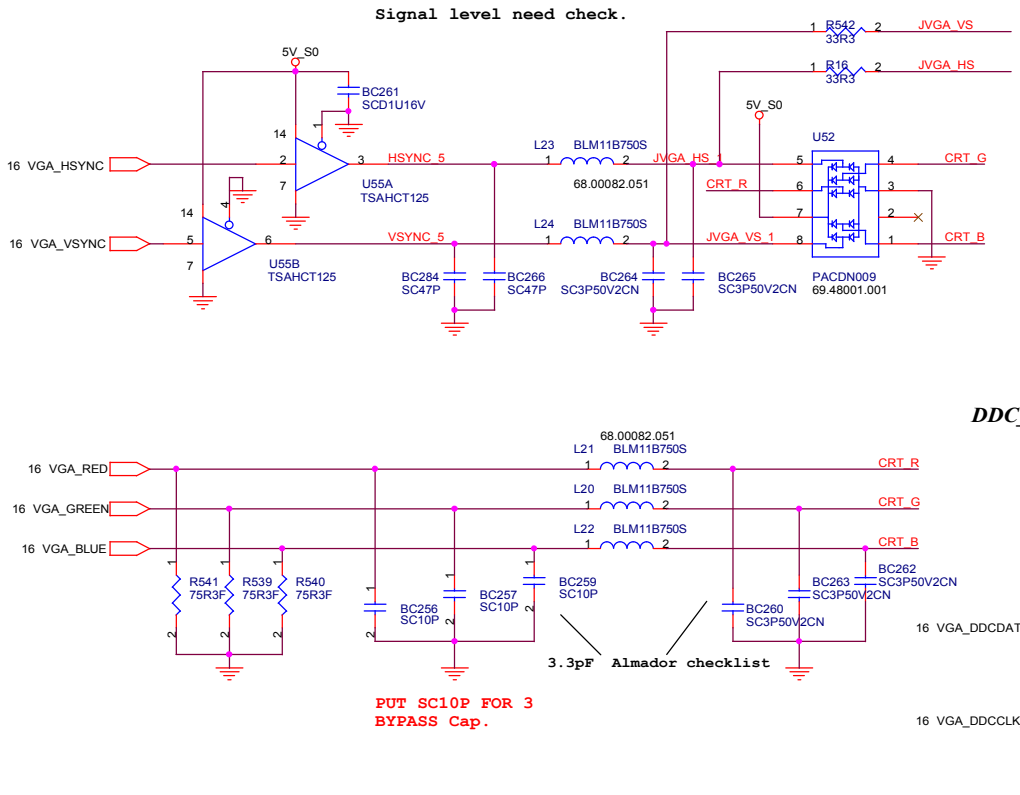
Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VGA VRAM (DDR)
Size A3	Document Number YuhinaME
Rev	SB
Date: Thursday, January 08, 2004	Sheet 19 of 58

All dampings in this page must near the VRAM.

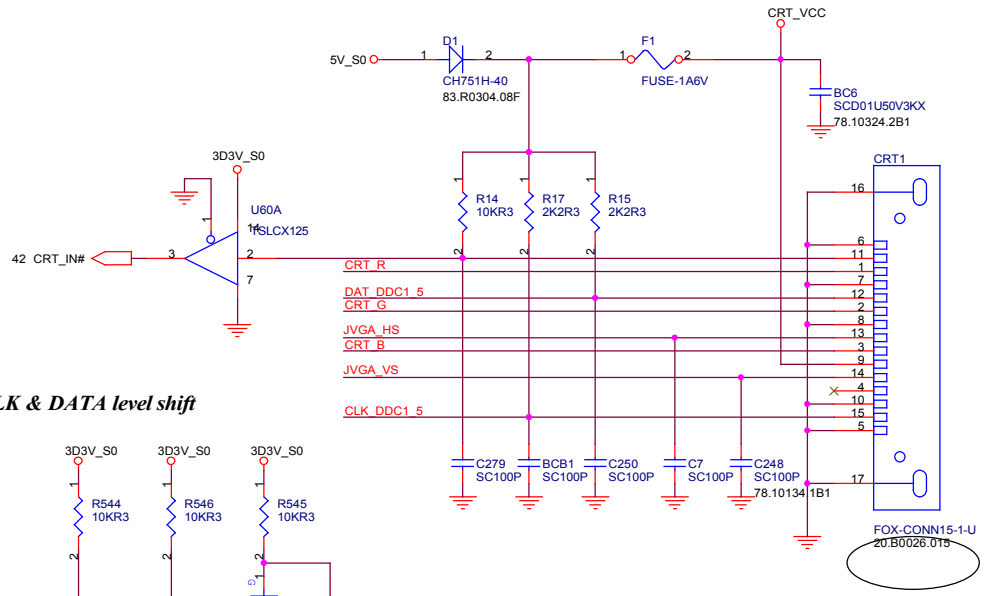


Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	VGA VRAM (DDR)
Size A3	Document Number YuhinaME
Rev	SB
Date: Thursday, January 08, 2004	Sheet 20 of 58

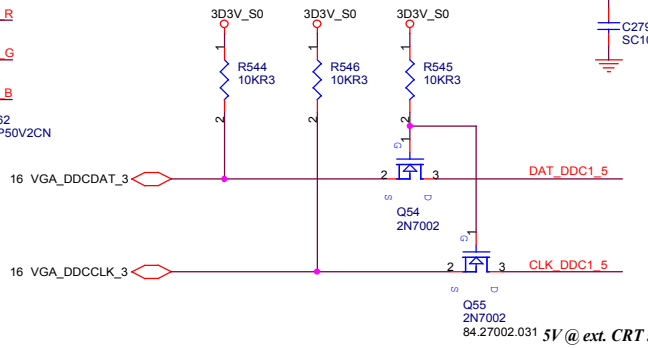
CRT



CRT CONN

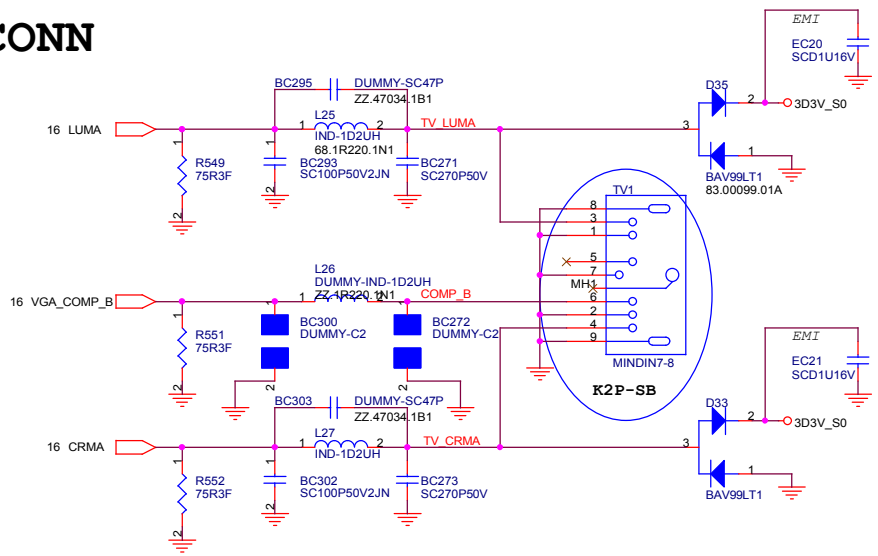


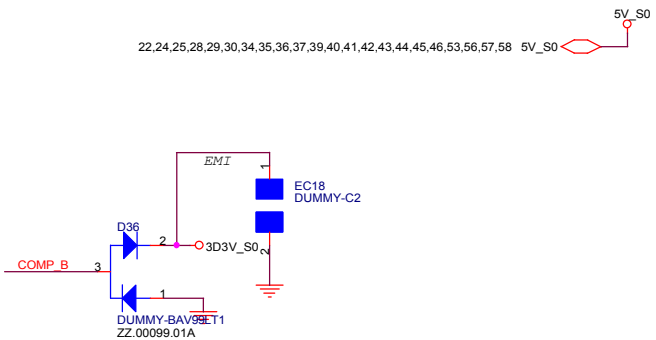
DDC_CLK & DATA level shift



5V @ ext. CRT side

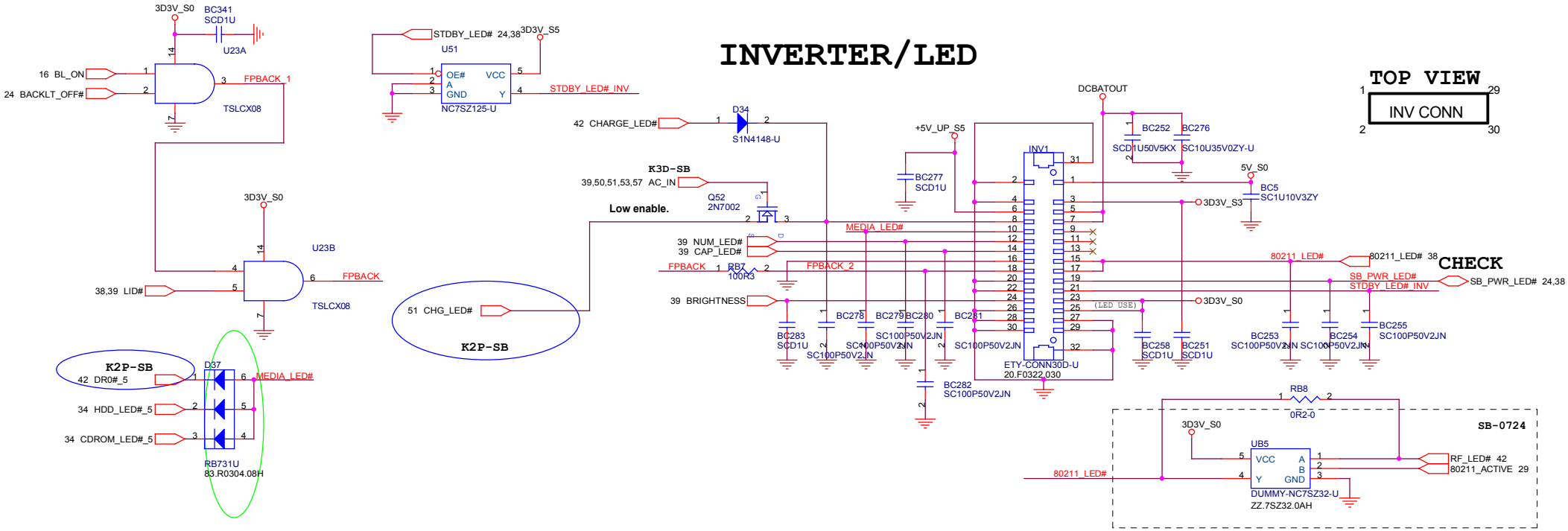
TV CONN



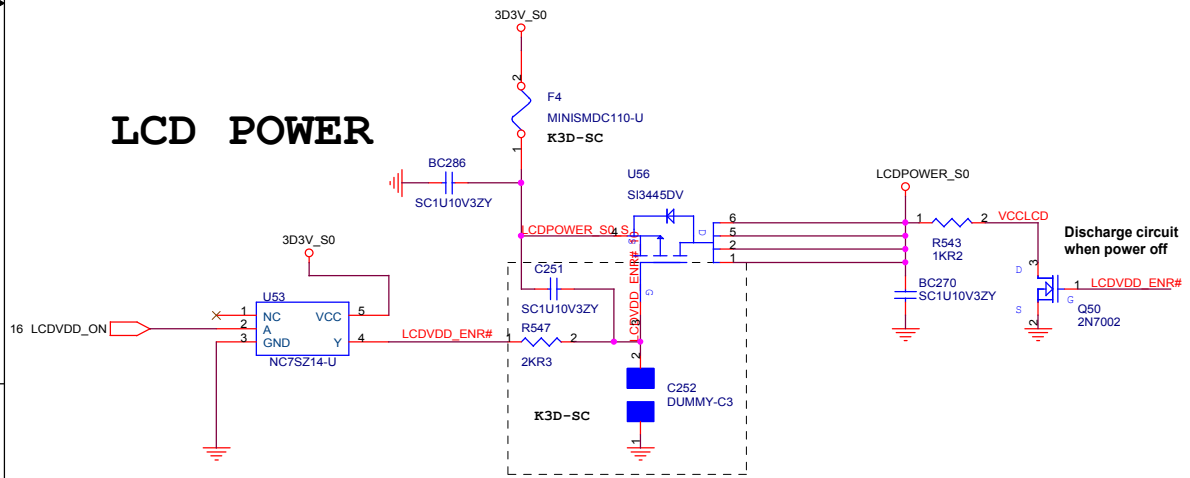


Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *CRT / TV*		
Size: A3	Document Number: YuhinaME	Rev: SB
Date: Thursday, January 08, 2004	Sheet 21 of 58	

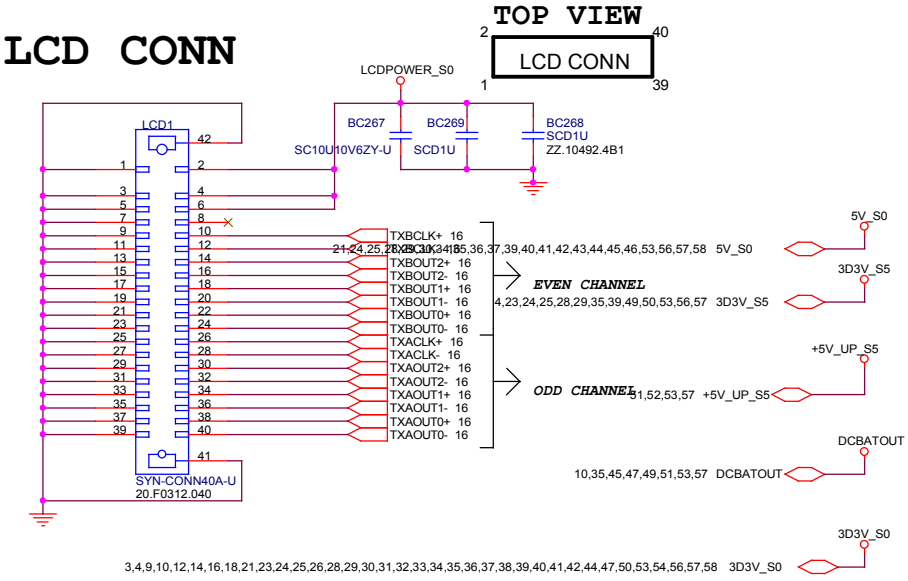
INVERTER/LED



LCD POWER

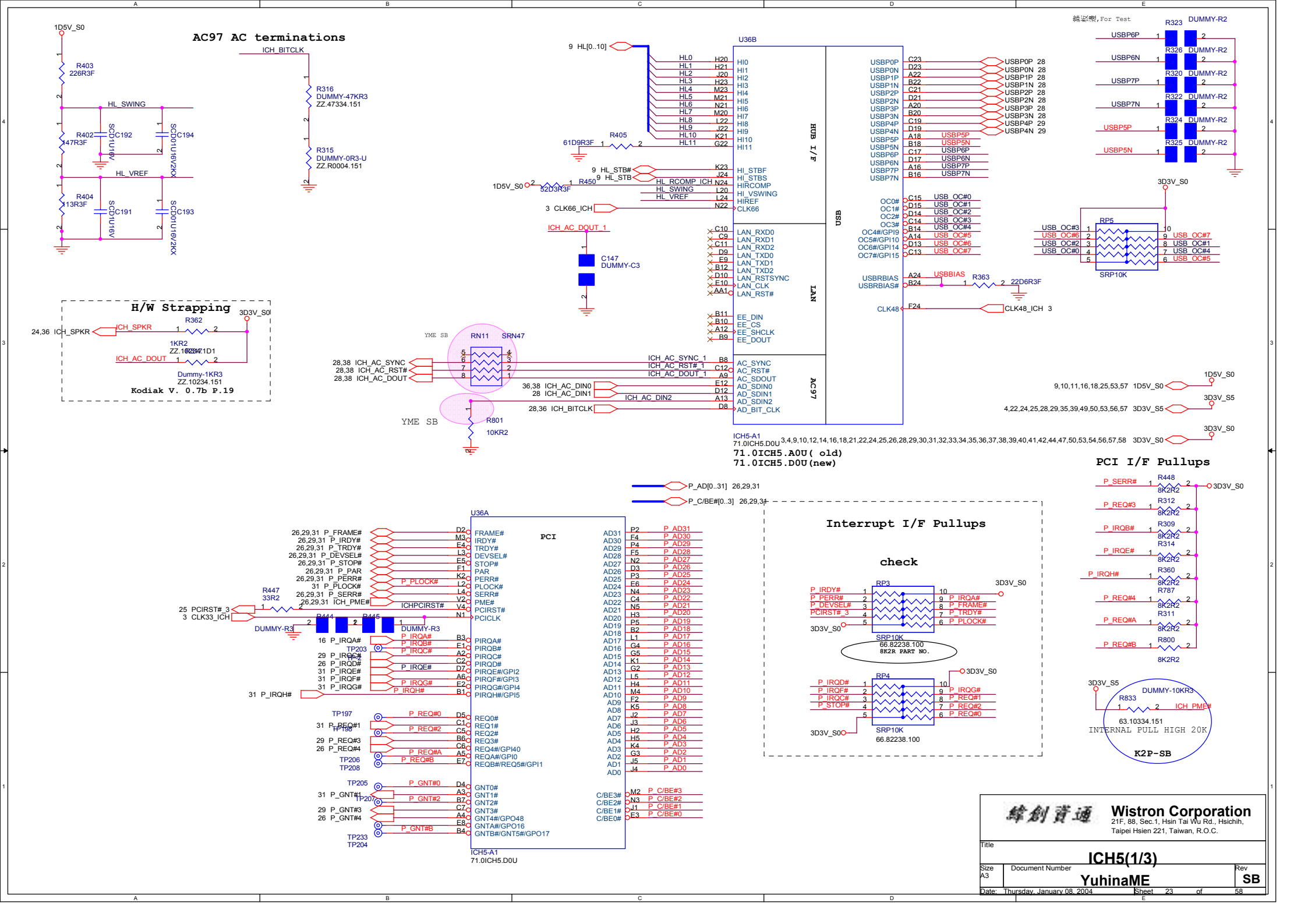


LCD CONN

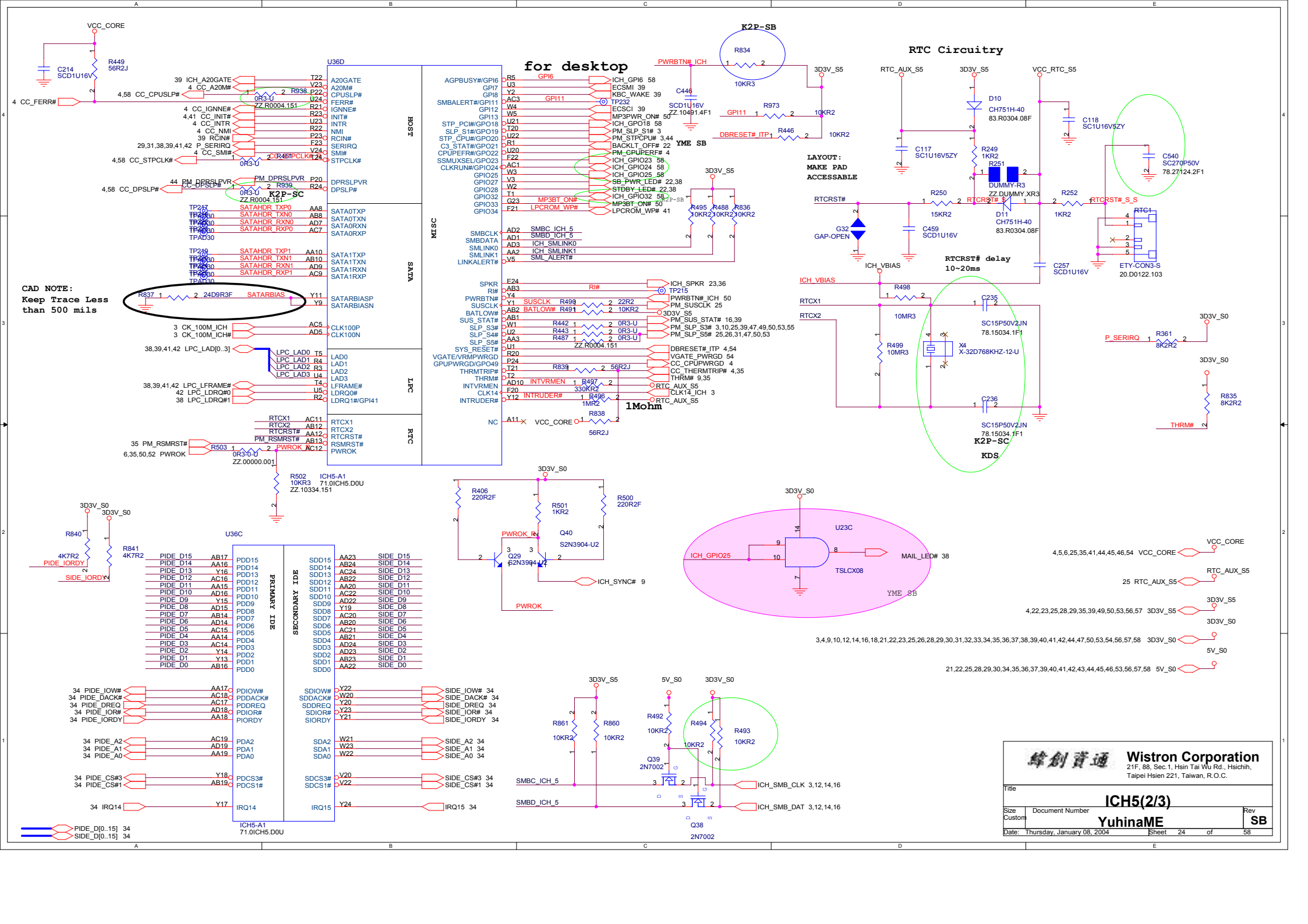


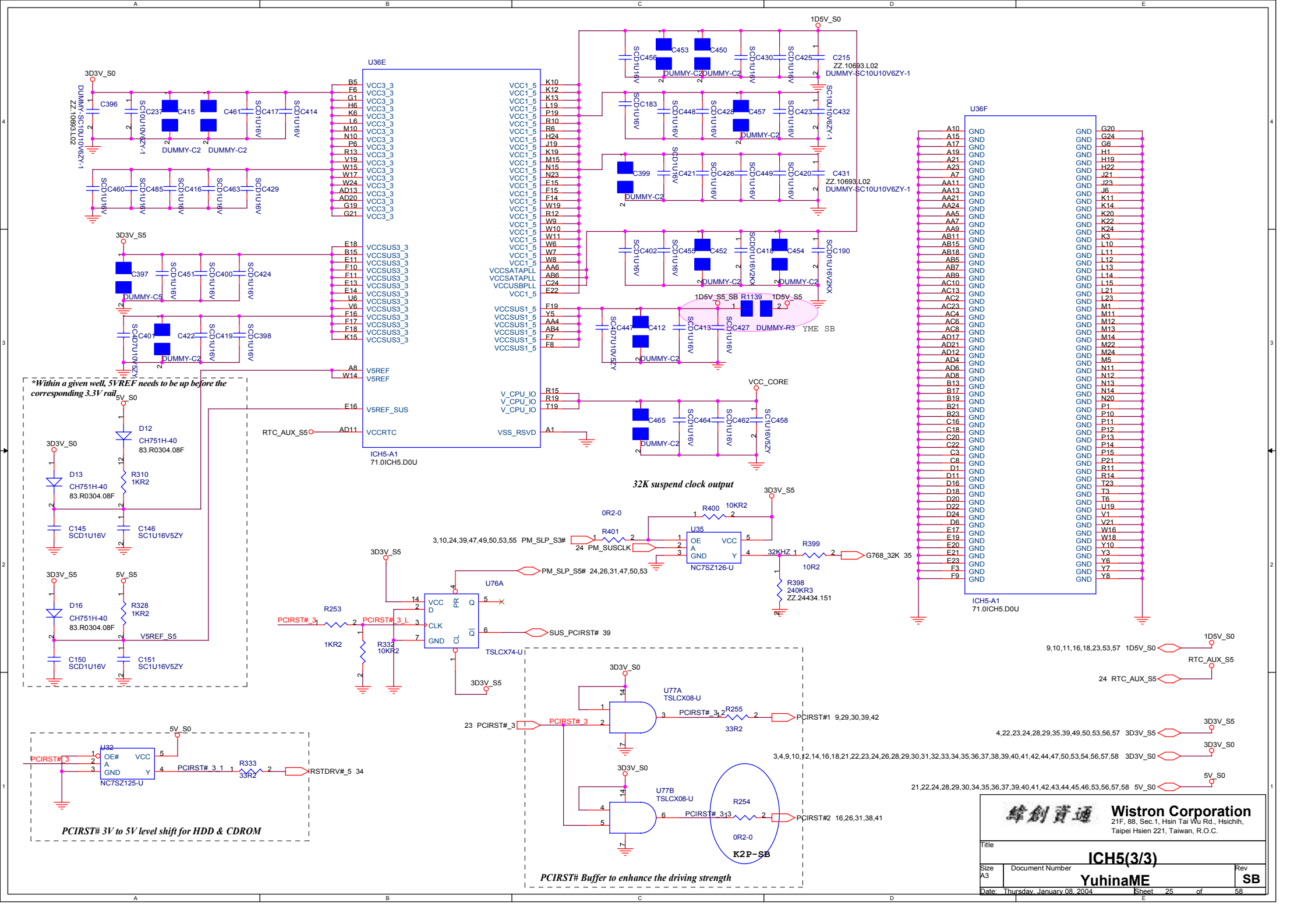
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INV / LCD	
Size A3	Document Number YuhinaME	Rev SB
Date: Thursday, January 08, 2004	Sheet 22 of 58	



Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	ICH5(1/3)	
Size A3	Document Number YuhinaME	Rev SB
Date: Thursday, January 08, 2004	Sheet 23 of 58	


for desktop
RTC Circuitry
CAD NOTE:
Keep Trace Less
than 500 mils
LAYOUT:
MAKE PAD
ACCESSABLE
RTCRST# delay
10~20ms
1Mohm
K2P-SB
K2P-SC
YME_SB
KDS
U36D
U36C
HOST
SATA
LPC
RTC
MISC
PRIMARY IDE
SECONDARY IDE
ICH5-A1
71.0ICH5.D0U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH5(2/3)
Size
Custom
Document Number
YuhinaME
Rev
SB
Date: Thursday, January 08, 2004
Sheet 24 of 58


U36E
ICH5-A1
71.0ICH5.D0U
U36F
ICH5-A1
71.0ICH5.D0U
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
32K suspend clock output
PCIRST# 3V to 5V level shift for HDD & CDROM
PCIRST# Buffer to enhance the driving strength
NC7SZ126-U
NC7SZ125-U
TSLCX74-U
TSLCX08-U
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ICH5(3/3)
Size A3
Document Number
YuhinaME
Rev SB
Date: Thursday, January 08, 2004
Sheet 25 of 58

The components of this region are reserved for future use. Please reserve the component space and pads in your layout for future extension.

100ohm @100MHz

L10 L-D1UH
L12 L-D1UH
L11 L-D1UH

BC72 SCD1U16V
BC75 SCD1U16V
BC372 SCD1U16V

3D3V_LAN_S5
2D5V_LAN_S5
LAN_VDD4
LAN_VDD1
LAN_VDD2
LAN_VDD3

R609 0R5
BC340 SC10U10V6ZY-U

3D3V_S0
R85 1KR2
D7 S1N4148-U
ISOB
R87
R86 15KR2
R84 DUMMY-25KR3
DUMMY-0R3-U
24,25,31,47,50,53 PM_SLP_S5#

K2P-SB
Q10 DTC124EUA-U1 ZZ.00124.A1K
22 K
PME# LAN
ICH_PME# 23,29,31

U63 RTL8101L 71.08101.00G
R98 DUMMY-R2 63.R0034.1D1

VDD VDD25 AVDD AVDDC AVDDL
PMEB/PME# ISOLATEB/ISOLATE# LWAKE
AUX/EEDI EESK EEDO EECS
EEDI EESK EEDO EECS_3

23,29,31 P_AD[31..0]
P_AD31 P_AD30 P_AD29 P_AD28 P_AD27 P_AD26 P_AD25 P_AD24 P_AD23 P_AD22 P_AD21 P_AD20 P_AD19 P_AD18 P_AD17 P_AD16 P_AD15 P_AD14 P_AD13 P_AD12 P_AD11 P_AD10 P_AD9 P_AD8 P_AD7 P_AD6 P_AD5 P_AD4 P_AD3 P_AD2 P_AD1 P_AD0
AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

LED2 LED1 LED0
LAN_LINK10# LAN_LINK100# LAN_ACTLED#
TP80
LAN_LINK100# 27
LAN_ACTLED# 27
GREEN
YELLOW

TXD- TXD+
TDN TDP
TDN 27
TDP 27

RXIN- RXIN+
RDN RDP
RDN 27
RDP 27

X1 X2
LAN_X1 LAN_X2

AC_RSTB AC_SYNC AC_DOUT AC_DIN AC_BCK INTBB GPIO0 GPIO1 RTT3 RTSET VCTRL CLKRUNB ROMCS/OEB NC
R122 10KR2
3D3V_S0
R99 5K6R2
TP3
LAN_RTSET
R607 10KR2

(Out) 3D3V_LAN_S5
C52 DUMMY-SCD1U16V

23,29,31 P_C/BE#[3..0]
P_C/BE#0 P_C/BE#1 P_C/BE#2 P_C/BE#3
C/BE0 C/BE1 C/BE2 C/BE3
CLK DEVSELB FRAMEB GNTB REQB IDSEL INTAB IRDYB TRDYB PAR PERRB SERRB STOPB RSTB
DGND AGND

R101 DUMMY-R3
D6 DUMMY-BAT54
R83 DUMMY-4K7R3

T=22ms
BC62 DUMMY-SC4D7U10V5ZY ZZ.47593.411
YME SB

3 CLK33_LAN
23,29,31 P_DEVSEL#
23,29,31 P_FRAME#
23 P_GNT#4
23 P_REQ#4
PCIRST#2 16,25,31,38,41
P_STOP# 23,29,31
P_SERR# 23,29,31
P_PERR# 23,29,31
P_PAR 23,29,31
P_TRDY# 23,29,31
P_IRDY# 23,29,31

23 P_IRQD#
R100 0R2-0
LAN_INTA#
R161 10R2
P_AD21
LAN_IDSEL

Check need bead or not

3D3V_LAN_S5
BC74 SCD1U16V
BC89 SCD1U16V
BC87 SCD1U16V
BC88 SCD1U16V
BC73 SCD1U16V
BC70 SCD1U16V

2D5V_LAN_S5
BC71 SCD1U16V
BC369 SCD1U16V
BC90 SCD1U16V

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

Close to RTL8139BL Pin60,Pin61
LAN_X1
LAN_X2
R610 DUMMY-R2
X5 X-25MHZ-11
BC370 SC27P50V2JN
BC371 SC27P50V2JN

3D3V_LAN_S5
R557 5K6R2
EECS_3
EESK
EEDI
EEDO
U14 M93C46-W-3
CS SK DI DO VCC DC ORG GND
BC315 SCD1U16V

main source: 72.93C46.K01
Second source:72.93C46.D01(ATMEL)

27,53 3D3V_LAN_S5
3D3V_S0
3,4,9,10,12,14,16,18,21,22,23,24,25,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44,47,50,53,54,56,57,58 3D3V_S0

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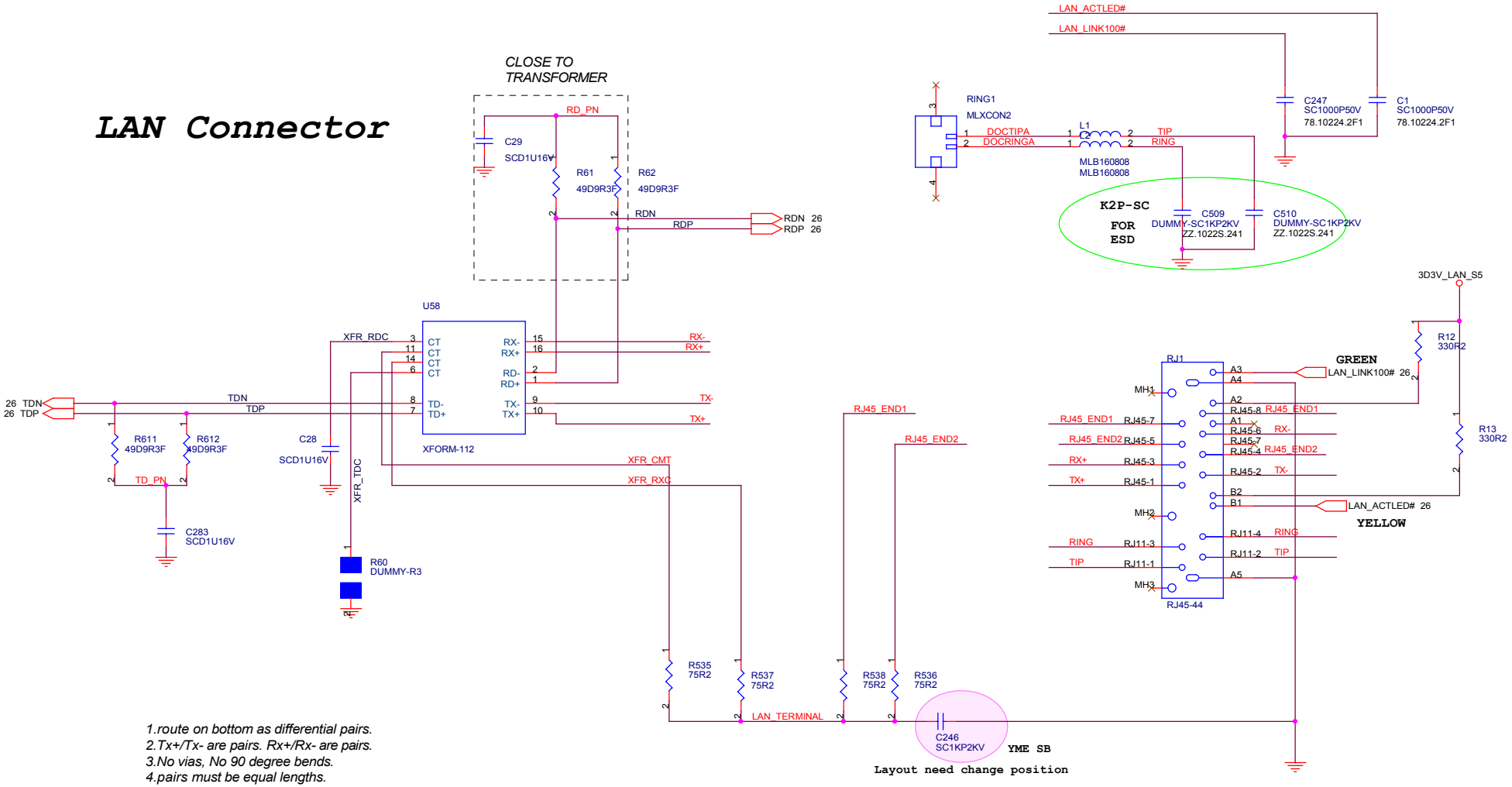
Title: LAN RTL8101L
Size: A3
Document Number: YuhinaME
Rev: SB
Date: Thursday, January 08, 2004
Sheet 26 of 58

LAN Connector



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

Green LED---Speed100:ON/Speed10:OFF
Yellow LED---Link:ON,TX/RX:Flash

26,53 3D3V_LAN_S5

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAN Connector		
Size: A3	Document Number: YuhinaME	Rev: SB
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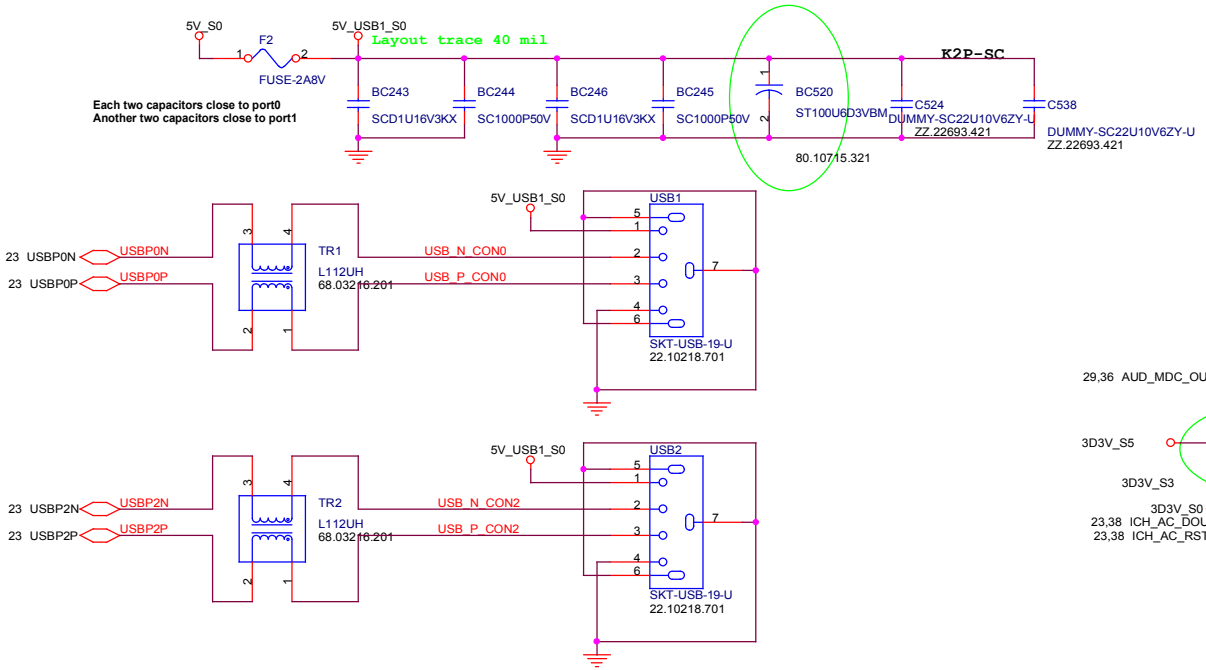
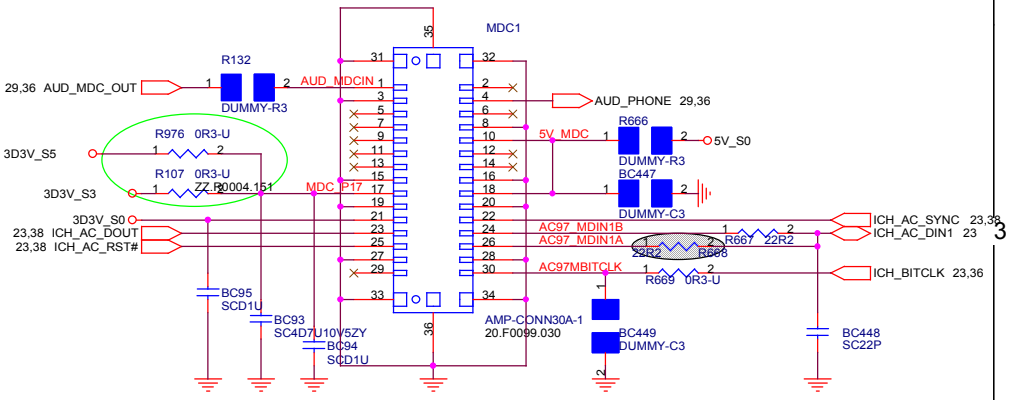
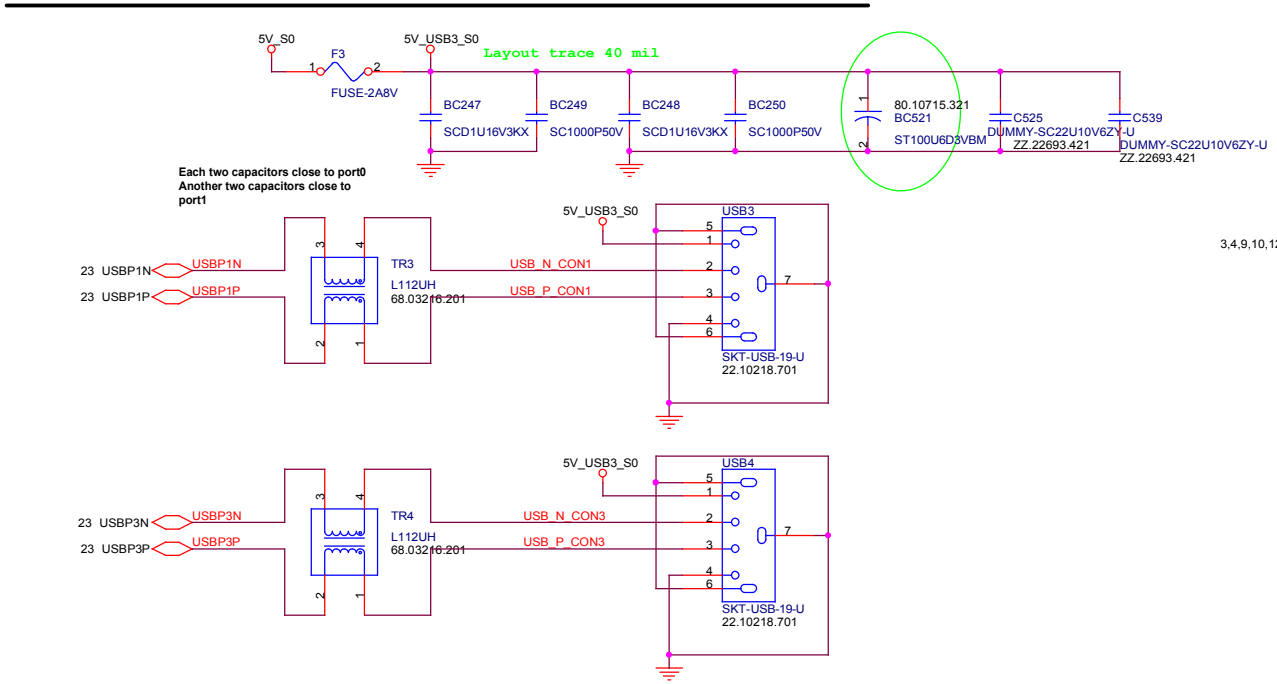
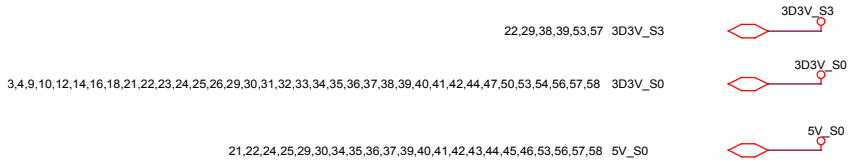
USB CONN









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Title: ***MDC / USB PORT***

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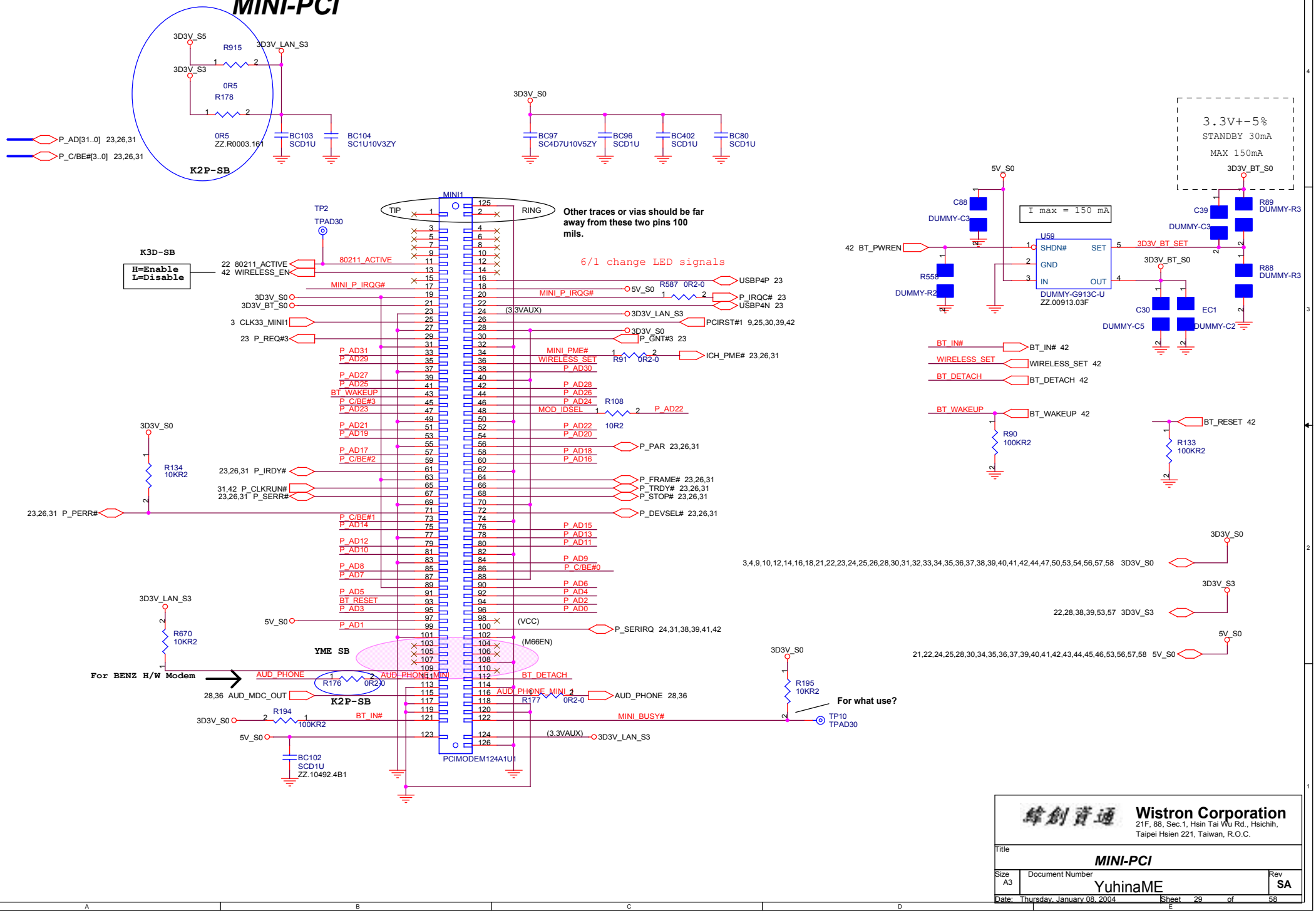
MINI-PCI



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI-PCI		
Size: A3	Document Number: YuhinaME	Rev: SA
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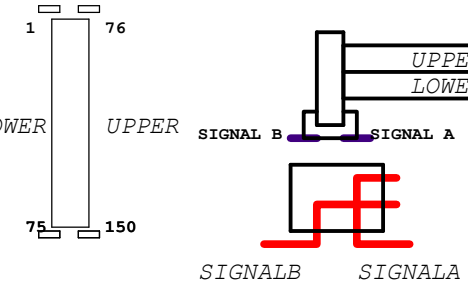
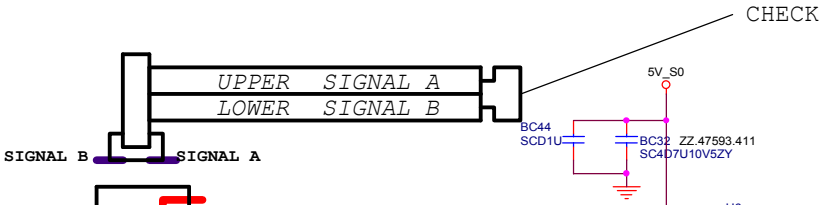
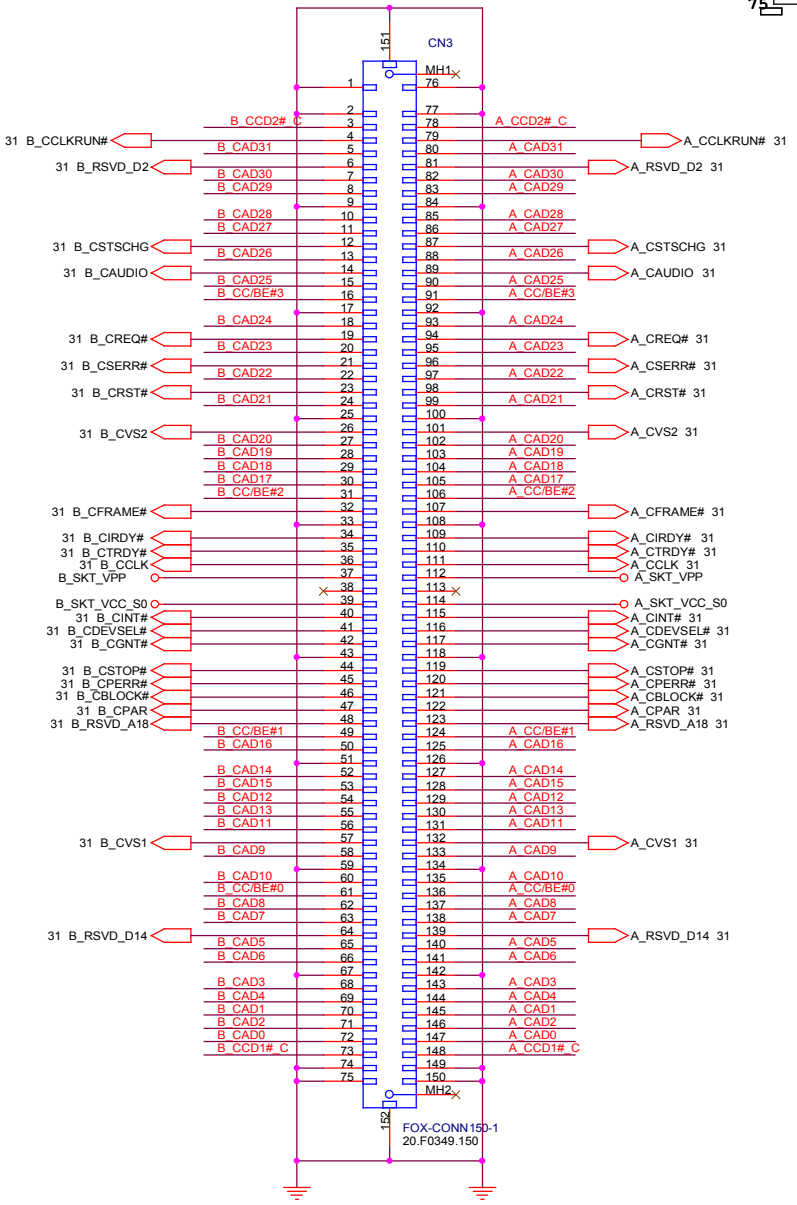
A_CC/BE#[3..0] 31
B_CC/BE#[3..0] 31
A_CAD[31..0] 31
B_CAD[31..0] 31

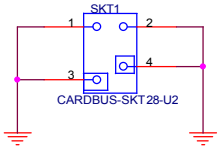
UPPER = SLOT 0 / SIGNAL A

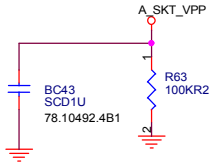
LOWER=SLOT 1/ SIGNAL B

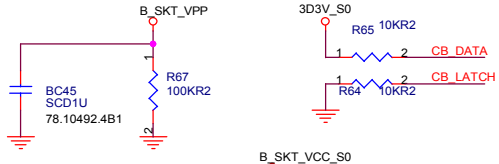


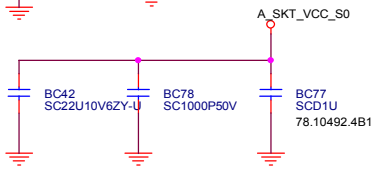


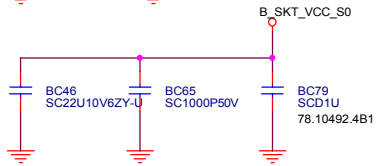


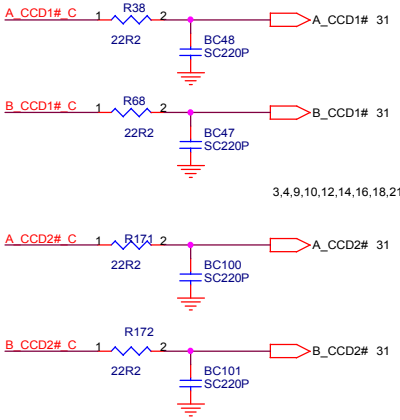


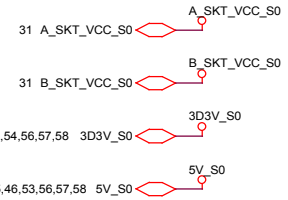












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Title: ***CARDBUS CONN / PWR SW***

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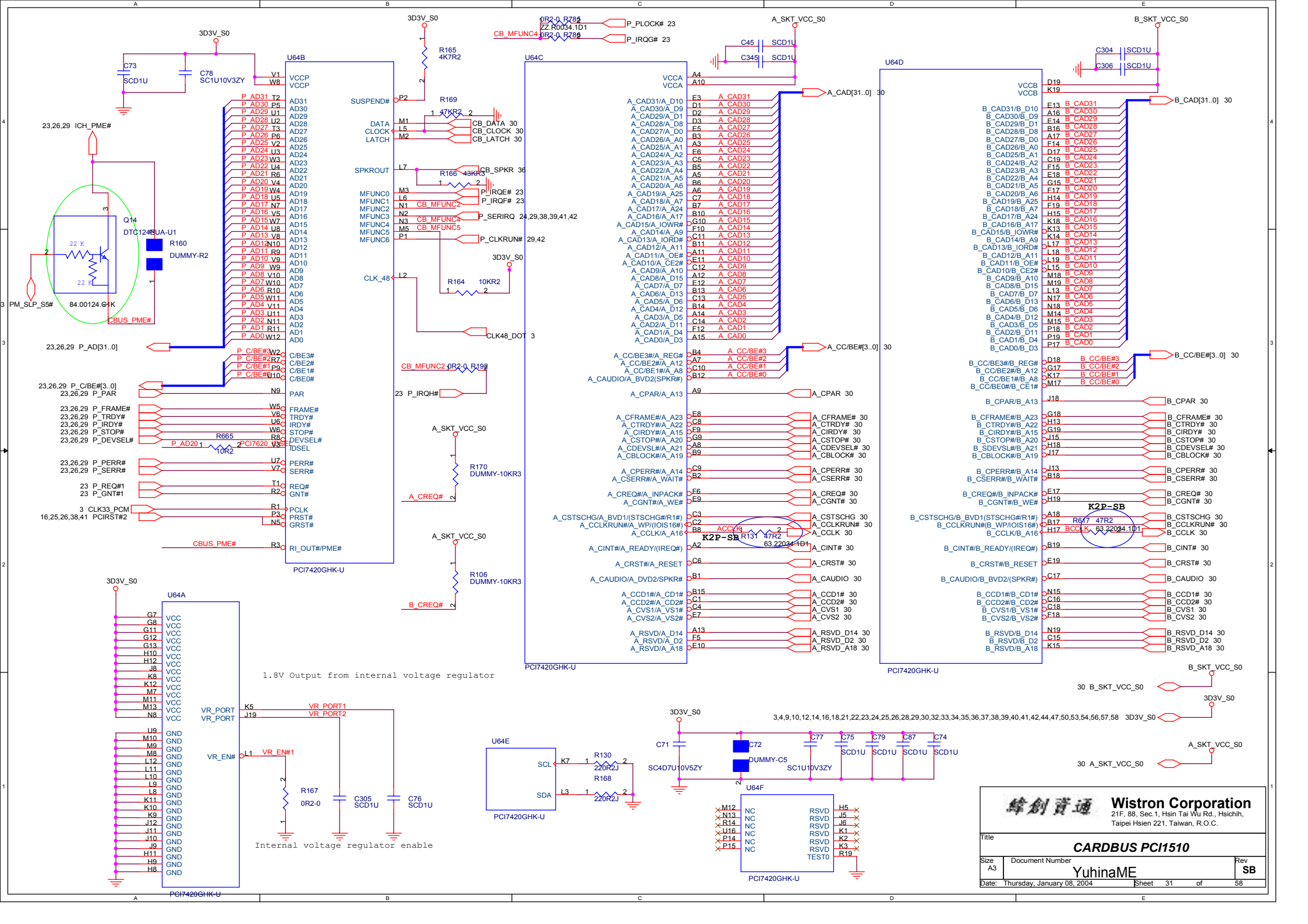
U64B
PCI7420GHK-U
U64C
PCI7420GHK-U
U64D
PCI7420GHK-U
U64A
PCI7420GHK-U
U64E
PCI7420GHK-U
U64F
PCI7420GHK-U
3D3V_S0
A_SKT_VCC_S0
B_SKT_VCC_S0
C73 SCD1U
C78 SC1U10V3ZY
Q14 DTC124EUA-U1
R160 DUMMY-R2
84.00124.G1K
CBUS_PME#
23,26,29 ICH_PME#
3 PM_SLP_S5#
23,26,29 P_AD[31..0]
23,26,29 P_C/BE#[3..0]
23,26,29 P_PAR
23,26,29 P_FRAME#
23,26,29 P_TRDY#
23,26,29 P_IRDY#
23,26,29 P_STOP#
23,26,29 P_DEVSEL#
P_AD20
R665 10R2
PCI7620_VSE
23,26,29 P_PERR#
23,26,29 P_SERR#
23 P_REQ#1
23 P_GNT#1
3 CLK33_PCM
16,25,26,38,41 PCIRST#2
CBUS_PME#
SUSPEND#
DATA
CLOCK
LATCH
CB_DATA 30
CB_CLOCK 30
CB_LATCH 30
SPKROUT
R166 43KR3
CB_SPKR 36
MFUNC0
MFUNC1
MFUNC2
MFUNC3
MFUNC4
MFUNC5
MFUNC6
CB_MFUNC2
CB_MFUNC4
CB_MFUNC5
P_IRQE# 23
P_IRQF# 23
P_SERIRQ 24,29,38,39,41,42
P_CLKRUN# 29,42
CLK_48
R164 10KR2
CLK48_DOT 3
R165 4K7R2
R169 47KR2
CB_MFUNC2 0R2-0 R192
23 P_IRQH#
R170 DUMMY-10KR3
A_CREQ#
R106 DUMMY-10KR3
B_CREQ#
0R2-0 R785 ZZ.R0034.1D1
CB_MFUNC4 0R2-0 R786
P_PLOCK# 23
P_IRQG# 23
C45 SCD1U
C345 SCD1U
A_CAD[31..0] 30
A_CC/BE#[3..0] 30
A_CPAR 30
A_CFRAME# 30
A_CTRDY# 30
A_CIRDY# 30
A_CSTOP# 30
A_CDEVSEL# 30
A_CBLOCK# 30
A_CPERR# 30
A_CSERR# 30
A_CREQ# 30
A_CGNT# 30
A_CSTSCHG 30
A_CCLKRUN# 30
A_CCLK 30
A_CINT# 30
A_CRST# 30
A_CAUDIO 30
A_CCD1# 30
A_CCD2# 30
A_CVS1 30
A_CVS2 30
A_RSVD_D14 30
A_RSVD_D2 30
A_RSVD_A18 30
ACCLK1 R131 47R2 63.22034.1D1
K2P-SB
C304 SCD1U
C306 SCD1U
B_CAD[31..0] 30
B_CC/BE#[3..0] 30
B_CPAR 30
B_CFRAME# 30
B_CTRDY# 30
B_CIRDY# 30
B_CSTOP# 30
B_CDEVSEL# 30
B_CBLOCK# 30
B_CPERR# 30
B_CSERR# 30
B_CREQ# 30
B_CGNT# 30
B_CSTSCHG 30
B_CCLKRUN# 30
B_CCLK 30
B_CINT# 30
B_CRST# 30
B_CAUDIO 30
B_CCD1# 30
B_CCD2# 30
B_CVS1 30
B_CVS2 30
B_RSVD_D14 30
B_RSVD_D2 30
B_RSVD_A18 30
R617 47R2
BCCLK 63.22034.1D1
30 B_SKT_VCC_S0
30 A_SKT_VCC_S0
3,4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,32,33,34,35,36,37,38,39,40,41,42,44,47,50,53,54,56,57,58 3D3V_S0
C71 SC4D7U10V5ZY
C72 DUMMY-C5
C77 SC1U10V3ZY
C75 C79 C87 C74 SCD1U
1.8V Output from internal voltage regulator
VR_PORT
VR_EN#
VR_PORT1
VR_PORT2
VR_EN#1
R167 0R2-0
C305 SCD1U
C76 SCD1U
Internal voltage regulator enable
SCL
SDA
R130 220R2J
R168 220R2J
NC
RSVD
TEST0
R19
Wistron Corporation
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Title
CARDBUS PCI1510
Size A3
Document Number
YuhinaME
Rev SB
Date: Thursday, January 08, 2004
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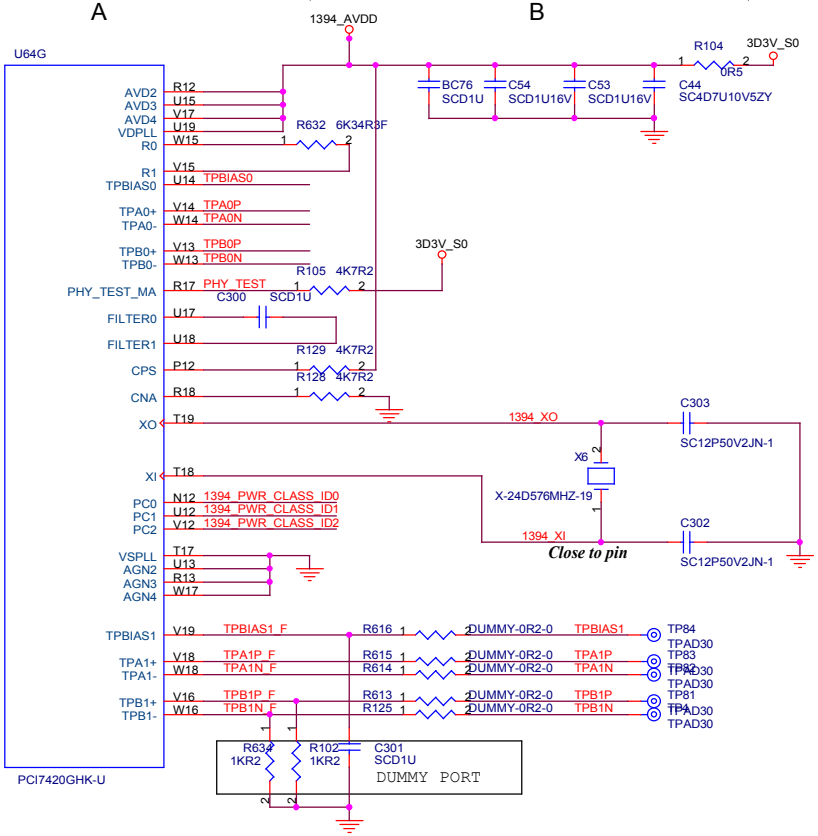

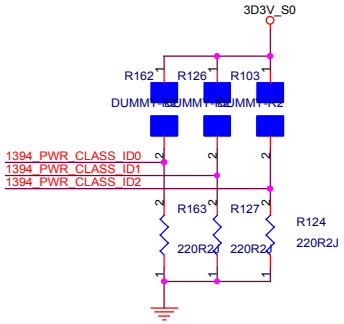

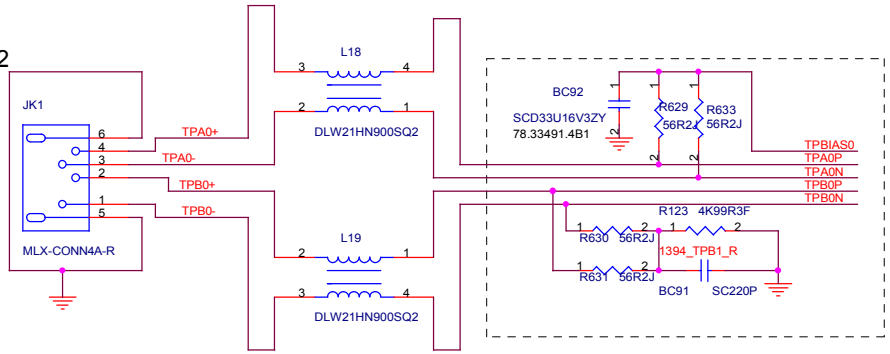

3,4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,31,33,34,35,36,37,38,39,40,41,42,44,47,50,53,54,56,57,58 3D3V_S0

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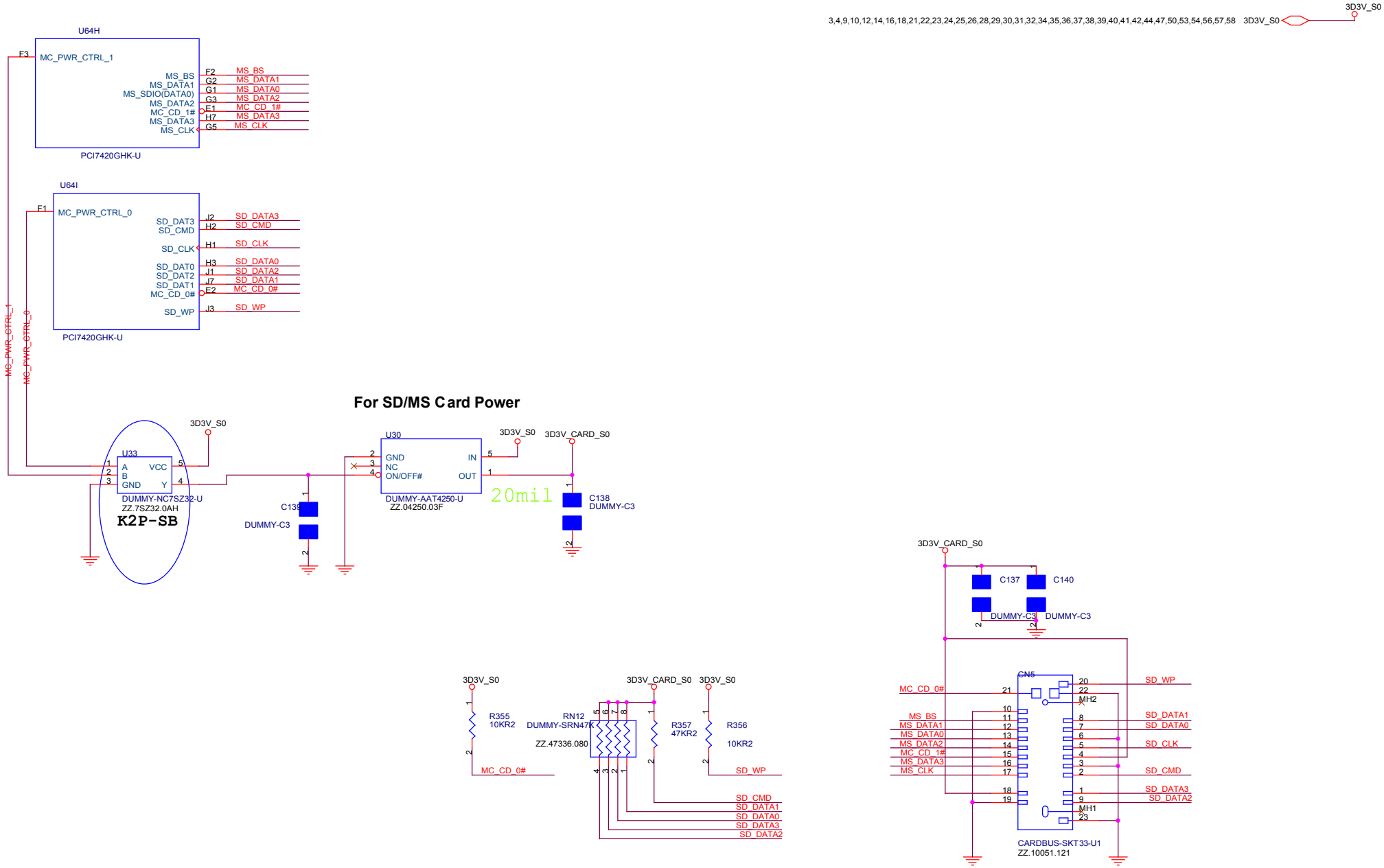
Title: *IEE1394-PHY_FW802C*

Size: A3 | Document Number: YuhinaME | Rev: SB

Date: Thursday, January 08, 2004 | Sheet 32 of 58



Wistron Corporation
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Title: **SD/MS READER**

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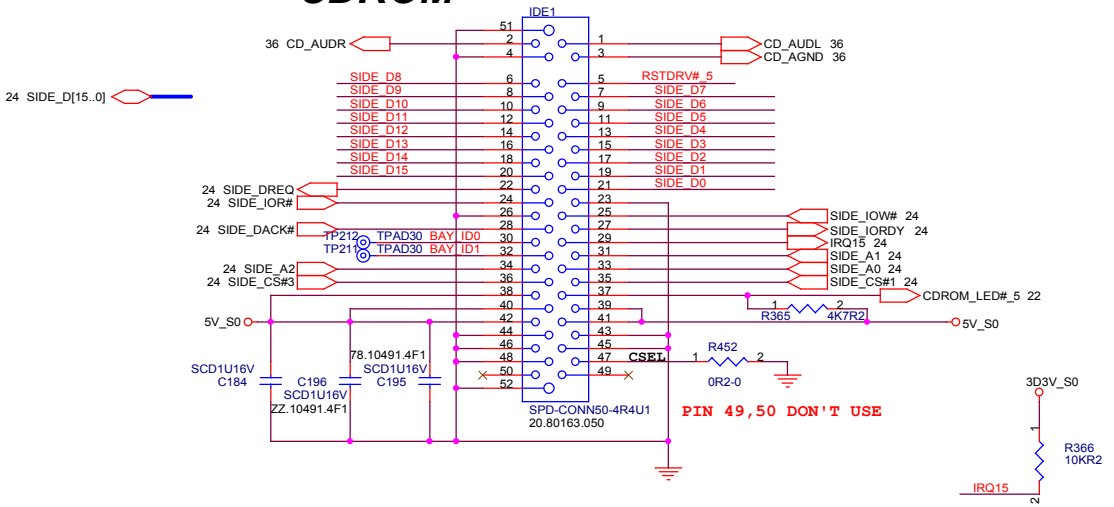
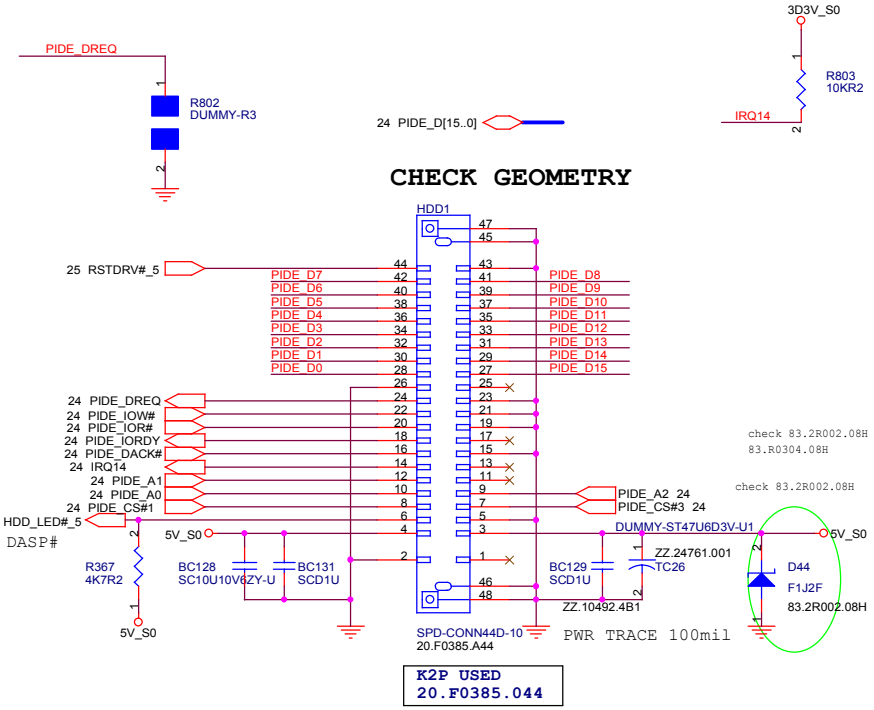
CDROM



21,22,24,25,28,29,30,35,36,37,39,40,41,42,43,44,45,46,53,56,57,58 5V_S0

HDD



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Title: HDD / CDROM		
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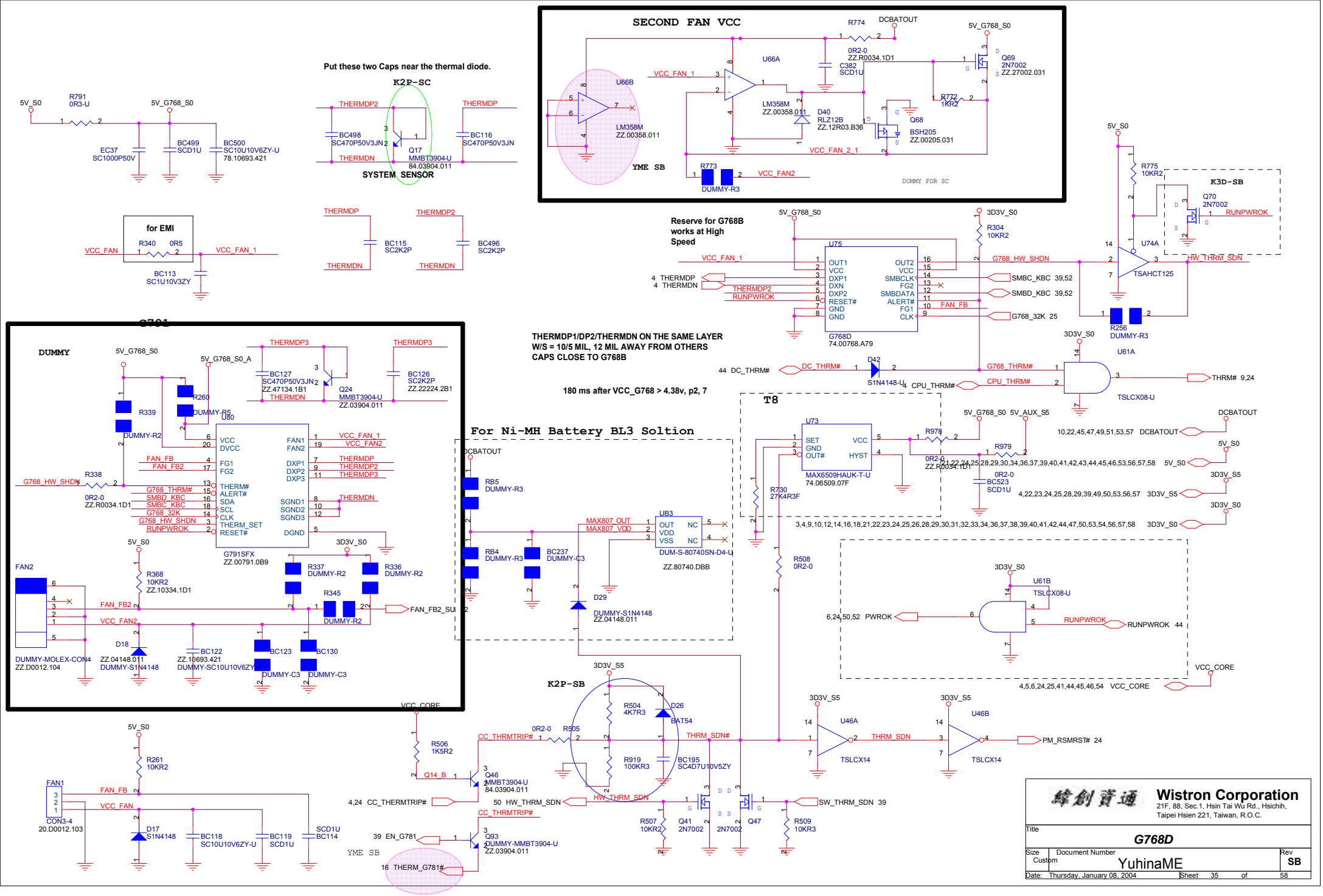
SECOND FAN VCC
Put these two Caps near the thermal diode.
K2P-SC
SYSTEM SENSOR
for EMI
G701
DUMMY
THERMDP1/DP2/THERMDN ON THE SAME LAYER
W/S = 10/5 MIL, 12 MIL AWAY FROM OTHERS
CAPS CLOSE TO G768B
Reserve for G768B
works at High
Speed
180 ms after VCC_G768 > 4.38v, p2, 7
For Ni-MH Battery BL3 Soltion
T8
K2P-SB
K3D-SB
YME SB
DUMMY FOR SC
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.
Title
G768D
Size
Custom
Document Number
YuhinaME
Rev
SB
Date: Thursday, January 08, 2004
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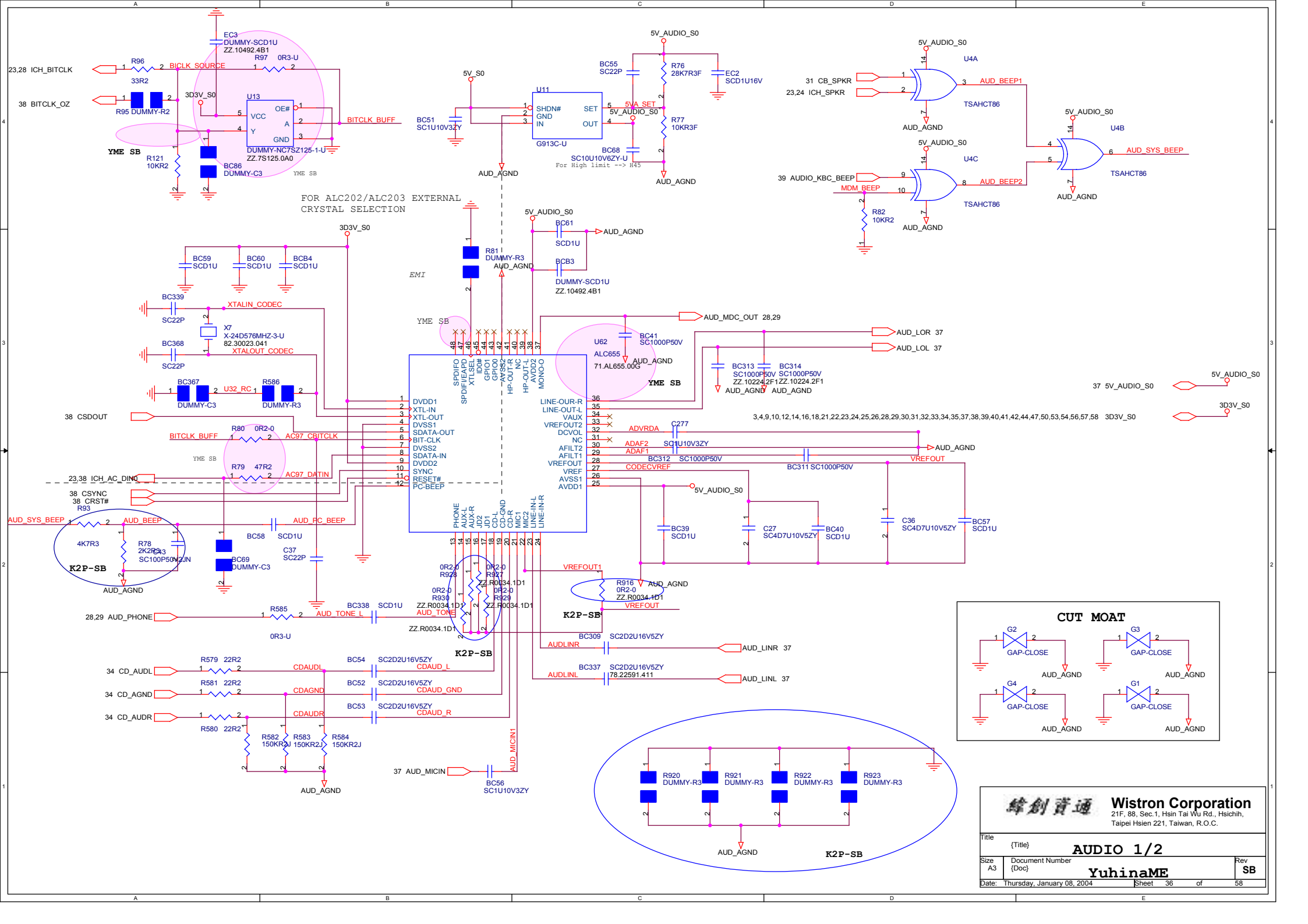
FOR ALC202/ALC203 EXTERNAL CRYSTAL SELECTION
EMI
YME SB
K2P-SB
CUT MOAT
G2 GAP-CLOSE
G3 GAP-CLOSE
G4 GAP-CLOSE
G1 GAP-CLOSE
U13
U11
U62
U4A
U4B
U4C
ALC655
71.AL655.00G
G913C-U
TSAHCT86
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title {Title}
AUDIO 1/2
Size A3
Document Number {Doc}
YuhinaME
Rev SB
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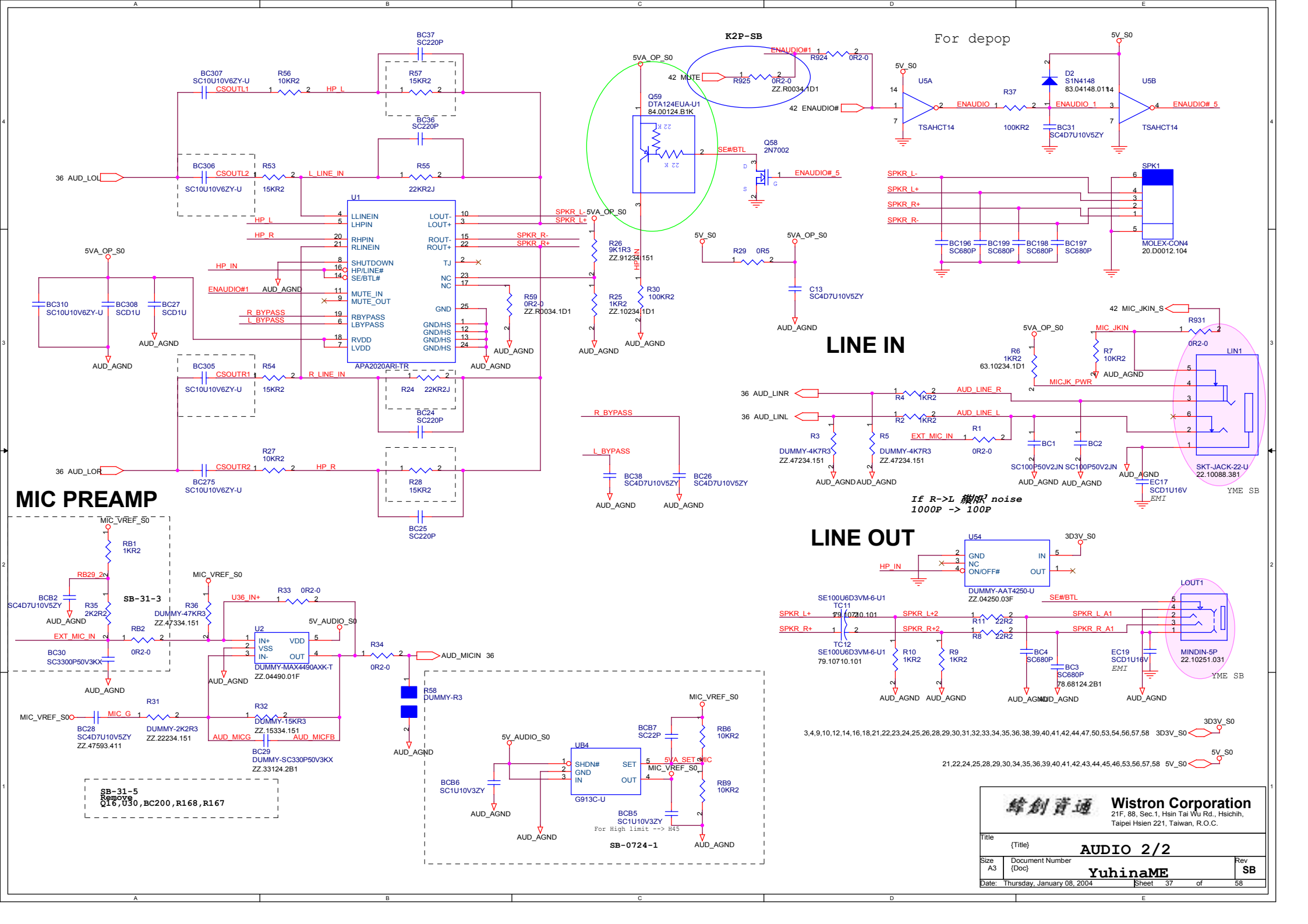
K2P-SB
For depop
LINE IN
LINE OUT
MIC PREAMP
U1
APA2020ARI-TR
U2
DUMMY-MAX4490AXK-T
ZZ.04490.01F
U4
G913C-U
U54
DUMMY-AAT4250-U
ZZ.04250.03F
U5A
U5B
TSAHCT14
Q59
DTA124EUA-U1
84.00124.B1K
Q58
2N7002
D2
S1N4148
83.04148.011
SPK1
MOLEX-CON4
20.D0012.104
SKT-JACK-22-U
22.10088.381
MINDIN-5P
22.10251.031
SB-31-3
SB-31-5
Remove
Q16,U30,BC200,R168,R167
SB-0724-1
If R->L 雜訊 noise
1000P -> 100P
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
{Title}
AUDIO 2/2
Size
A3
Document Number
{Doc}
YuhinaME
Rev
SB
Date: Thursday, January 08, 2004
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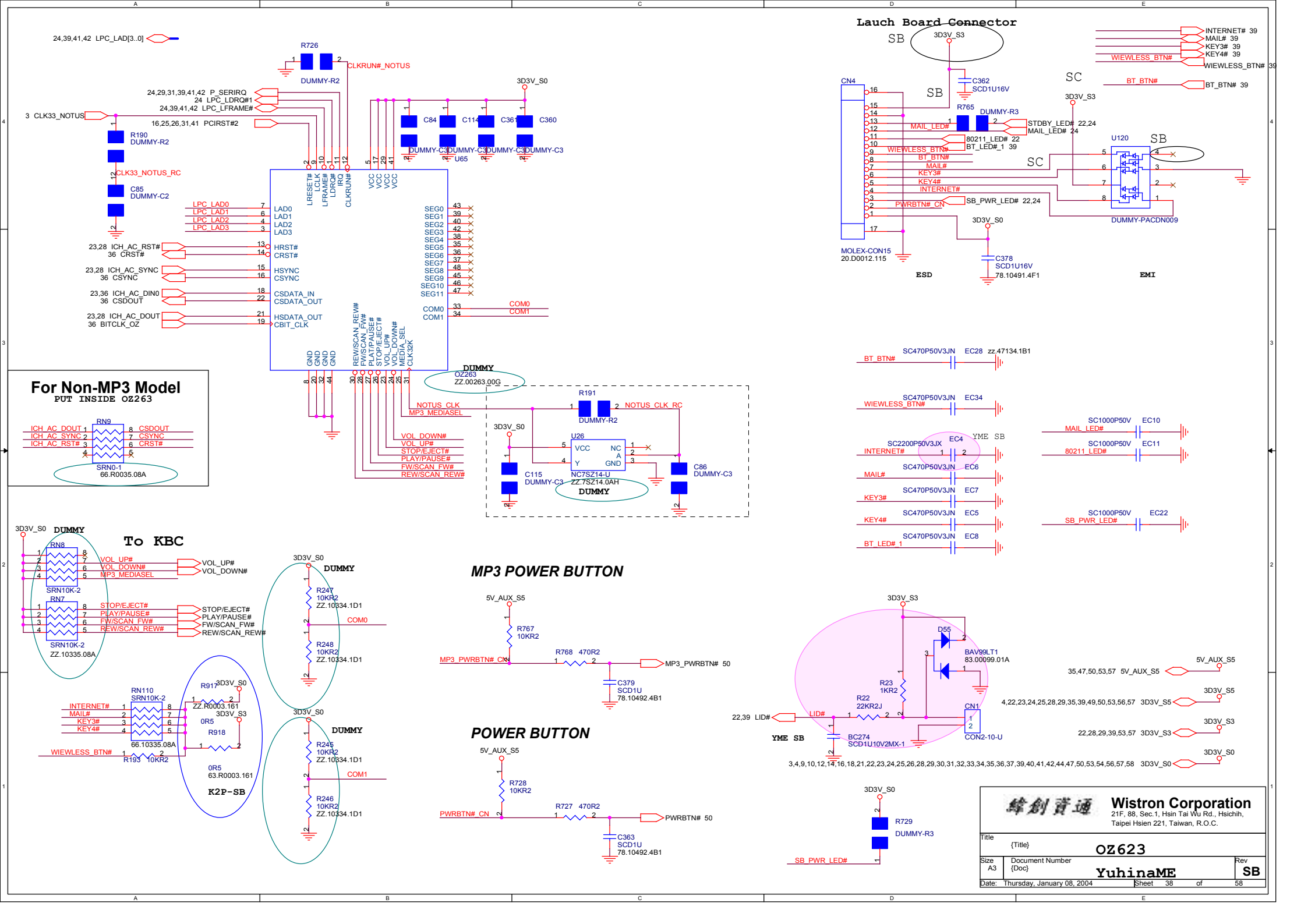
24,39,41,42 LPC_LAD[3..0]
R726
DUMMY-R2
CLKRUN#_NOTUS
24,29,31,39,41,42 P_SERIRQ
24 LPC_LDRQ#1
24,39,41,42 LPC_LFRAME#
3 CLK33_NOTUS
16,25,26,31,41 PCIRST#2
R190
DUMMY-R2
CLK33_NOTUS_RC
C85
DUMMY-C2
3D3V_S0
C84
C114
C361
C360
DUMMY-C3
U65
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LAD0
LAD1
LAD2
LAD3
LRESET#
LCLK
LFRAME#
LDRQ#
IRQ
CLKRUN#
VCC
SEG0
SEG1
SEG2
SEG3
SEG4
SEG5
SEG6
SEG7
SEG8
SEG9
SEG10
SEG11
COM0
COM1
23,28 ICH_AC_RST#
36 CRST#
HRST#
CRST#
23,28 ICH_AC_SYNC
36 CSYNC
HSYNC
CSYNC
23,36 ICH_AC_DIN0
36 CSDOUT
CSDATA_IN
CSDATA_OUT
23,28 ICH_AC_DOUT
36 BITCLK_OZ
HSDATA_OUT
CBIT_CLK
GND
REW/SCAN_REW#
FW/SCAN_FW#
PLAY/PAUSE#
STOP/EJECT#
VOL_UP#
VOL_DOWN#
MEDIA_SEL
CLK32K
DUMMY
OZ263
ZZ.00263.00G
NOTUS_CLK
MP3_MEDIASEL
R191
NOTUS_CLK_RC
U26
NC7SZ14-U
ZZ.7SZ14.0AH
C115
C86
VOL_DOWN#
STOP/EJECT#
PLAY/PAUSE#
FW/SCAN_FW#
REW/SCAN_REW#
For Non-MP3 Model
PUT INSIDE OZ263
RN9
ICH_AC_DOUT
ICH_AC_SYNC
ICH_AC_RST#
CSDOUT
CSYNC
CRST#
SRN0-1
66.R0035.08A
To KBC
RN8
VOL_UP#
VOL_DOWN#
MP3_MEDIASEL
SRN10K-2
RN7
STOP/EJECT#
PLAY/PAUSE#
FW/SCAN_FW#
REW/SCAN_REW#
ZZ.10335.08A
R247
10KR2
ZZ.10334.1D1
COM0
R248
10KR2
ZZ.10334.1D1
R245
10KR2
ZZ.10334.1D1
COM1
R246
10KR2
ZZ.10334.1D1
RN110
SRN10K-2
INTERNET#
MAIL#
KEY3#
KEY4#
66.10335.08A
WIEWLESS_BTN#
R193 10KR2
R917
ZZ.R0003.161
R918
0R5
0R5
63.R0003.161
K2P-SB
MP3 POWER BUTTON
5V_AUX_S5
R767
10KR2
MP3_PWRBTN# CN
R768 470R2
MP3_PWRBTN# 50
C379
SCD1U
78.10492.4B1
POWER BUTTON
PWRBTN# CN
R728
10KR2
R727 470R2
PWRBTN# 50
C363
SCD1U
78.10492.4B1
Lauch Board Connector
SB
SC
CN4
MOLEX-CON15
20.D0012.115
C362
SCD1U16V
R765
DUMMY-R3
MAIL_LED#
STDBY_LED# 22,24
MAIL_LED# 24
80211_LED# 22
BT_LED#_1 39
WIEWLESS_BTN#
BT_BTN#
MAIL#
KEY3#
KEY4#
INTERNET#
PWRBTN# CN
SB_PWR_LED# 22,24
C378
SCD1U16V
78.10491.4F1
ESD
EMI
U120
DUMMY-PACDN009
INTERNET# 39
MAIL# 39
KEY3# 39
KEY4# 39
WIEWLESS_BTN# 39
BT_BTN# 39
SC470P50V3JN
EC28 zz.47134.1B1
EC34
EC4
YME SB
SC2200P50V3JX
EC6
EC7
EC5
EC8
SC1000P50V
EC10
EC11
EC22
MAIL_LED#
80211_LED#
SB_PWR_LED#
D55
BAV99LT1
83.00099.01A
R23
1KR2
R22
22KR2J
LID#
22,39 LID#
BC274
SCD1U10V2MX-1
CN1
CON2-10-U
3,4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,31,32,33,34,35,36,37,39,40,41,42,44,47,50,53,54,56,57,58 3D3V_S0
35,47,50,53,57 5V_AUX_S5
4,22,23,24,25,28,29,35,39,49,50,53,56,57 3D3V_S5
22,28,29,39,53,57 3D3V_S3
R729
DUMMY-R3
SB_PWR_LED#
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
{Title}
OZ623
Size
A3
Document Number
{Doc}
YuhinaME
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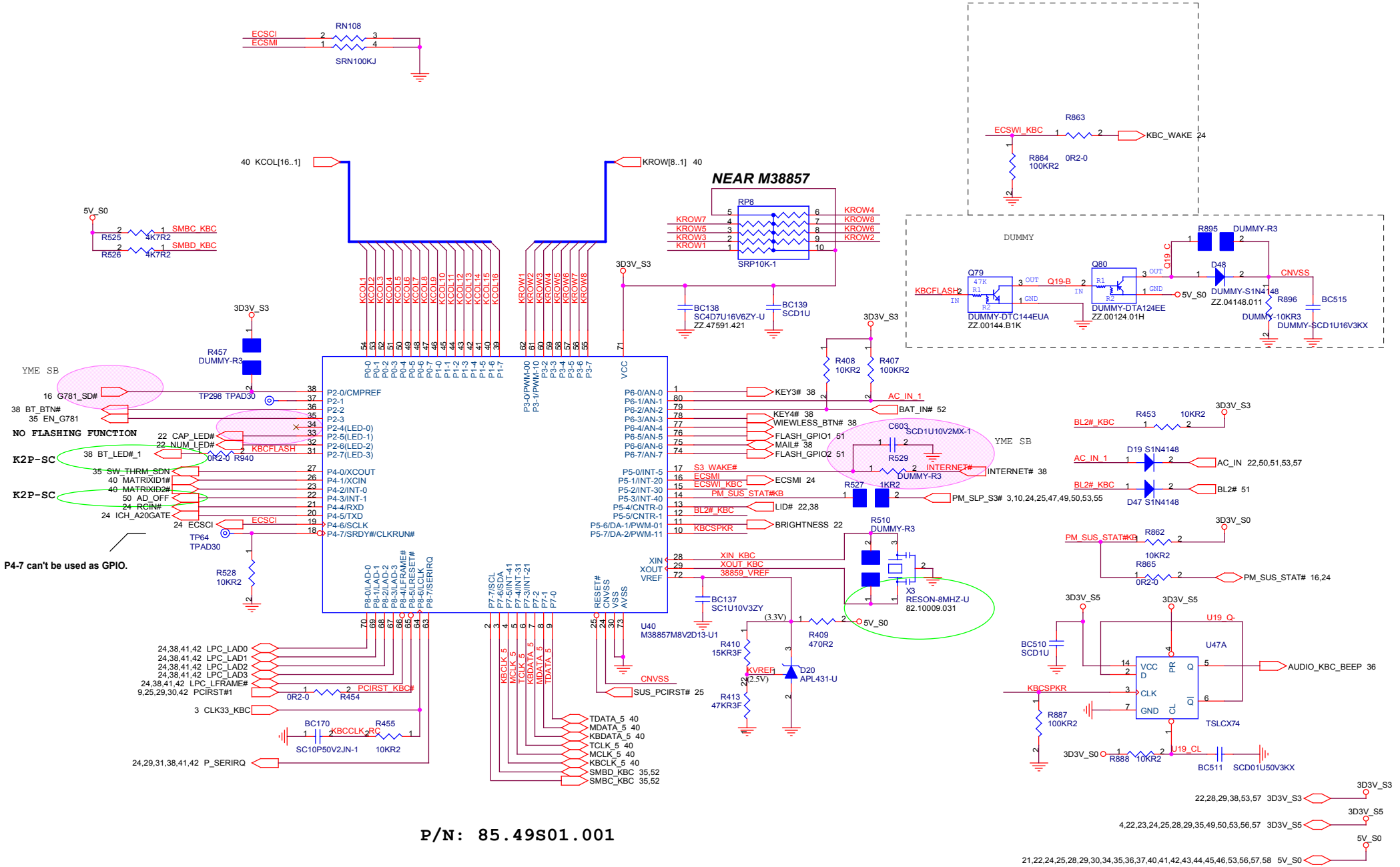
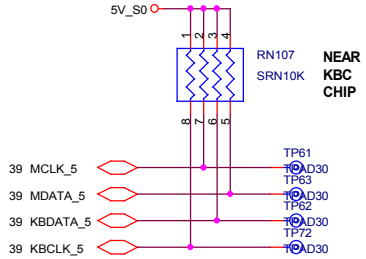
Date: Thursday, January 08, 2004
Sheet 38 of 58



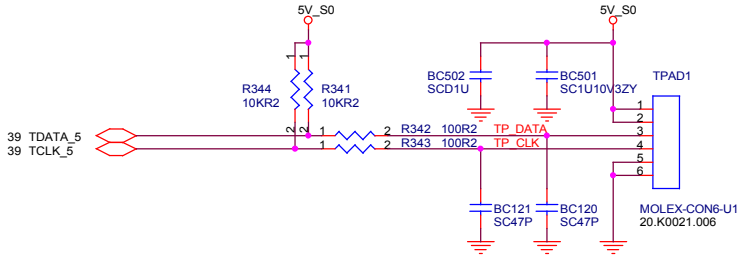
P/N: 85.49S01.001

Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: KBC M38857		
Size: A3	Document Number: YuhinaME	Rev: SB
Date: Thursday, January 08, 2004	Sheet 39 of 58	

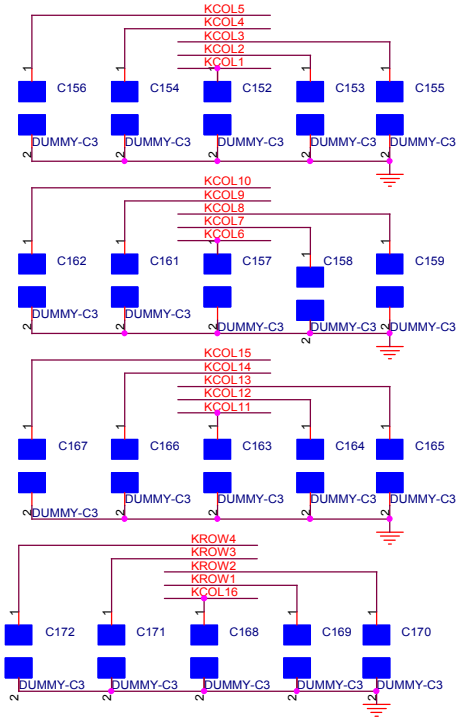
PS/2 CONN

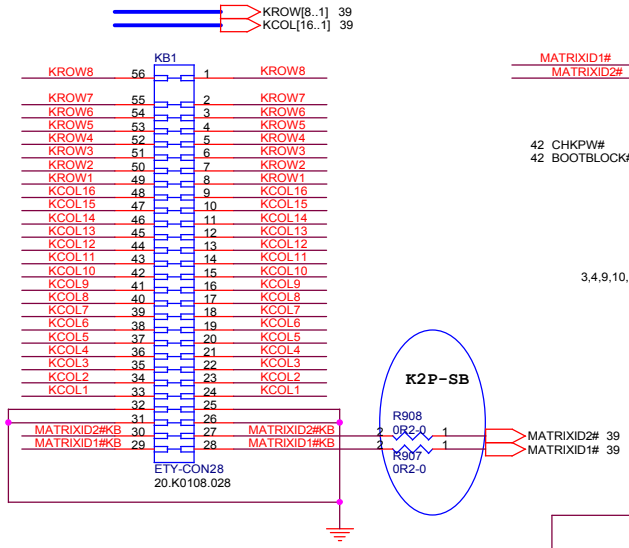


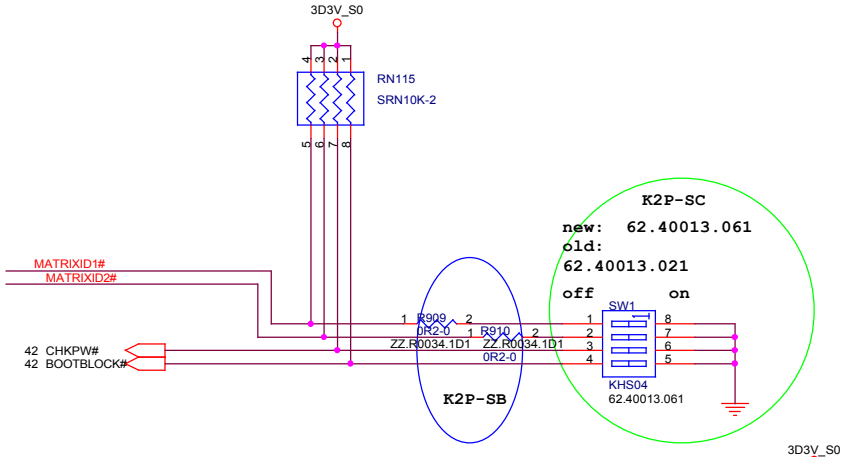
TOUCH PAD

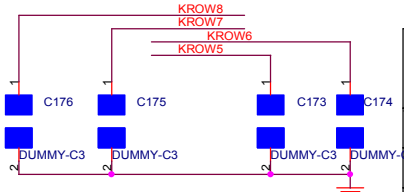


Internal KeyBoard CONN









		US	Jap	Eur
Low Bit	MATRIXID1#	1	1	0
High Bit	MATRIXID2#	1	0	0

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Title: PS2 / TOUCHPAD / KB CONN

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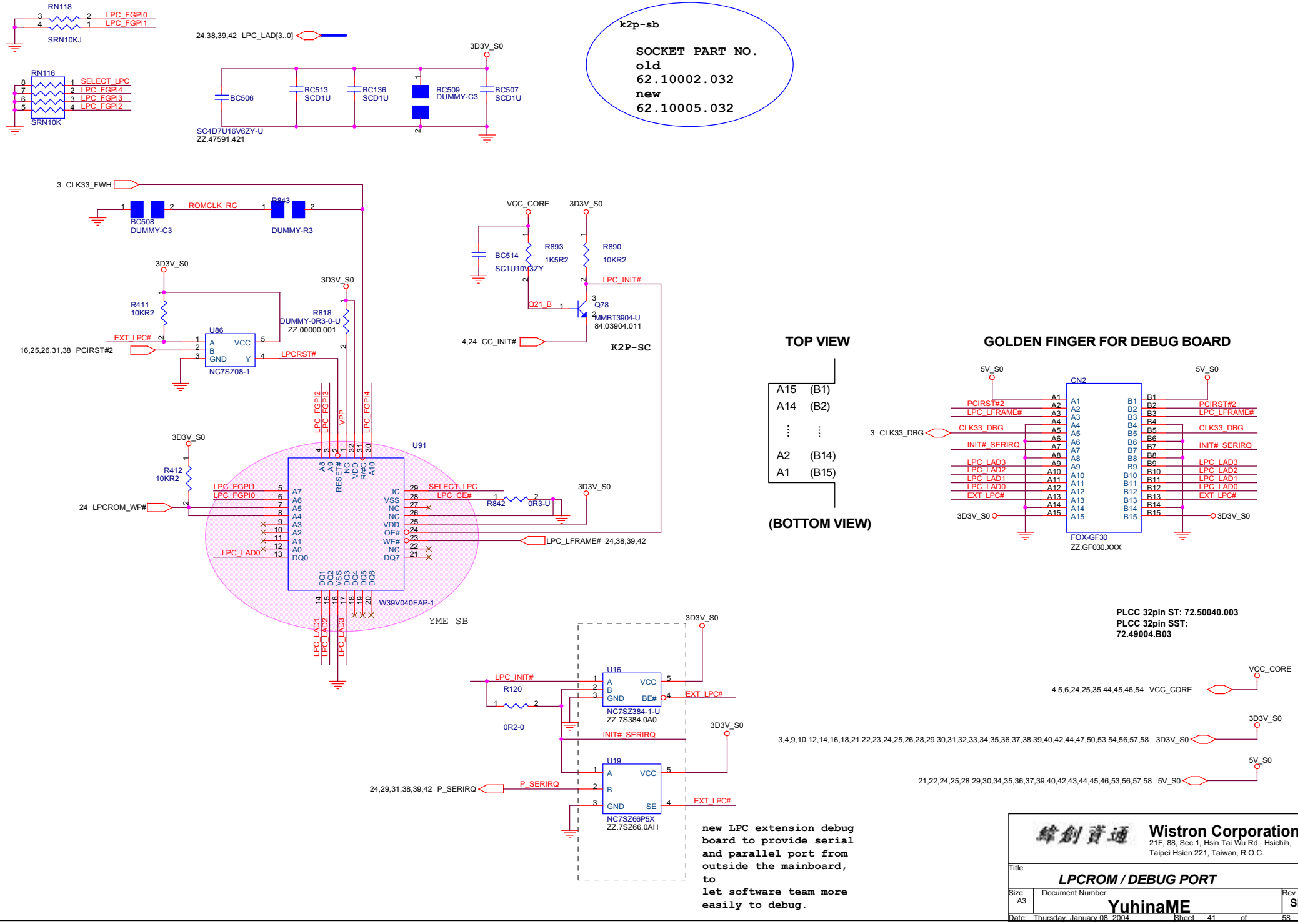
RN118
LPC_FGPI0
LPC_FGPI1
SRN10KJ
RN116
SELECT_LPC
LPC_FGPI4
LPC_FGPI3
LPC_FGPI2
SRN10K
24,38,39,42 LPC_LAD[3..0]
3D3V_S0
BC506
BC513
SCD1U
BC136
SCD1U
BC509
DUMMY-C3
BC507
SCD1U
SC4D7U16V6ZY-U
ZZ.47591.421
k2p-sb
SOCKET PART NO.
old
62.10002.032
new
62.10005.032
3 CLK33_FWH
ROMCLK_RC
BC508
DUMMY-C3
R843
DUMMY-R3
VCC_CORE
3D3V_S0
BC514
SC1U10V3ZY
R893
1K5R2
R890
10KR2
LPC_INIT#
Q21_B
Q78
MMBT3904-U
84.03904.011
4,24 CC_INIT#
K2P-SC
R411
10KR2
R818
DUMMY-0R3-0-U
ZZ.00000.001
EXT_LPC#
16,25,26,31,38 PCIRST#2
U86
NC7SZ08-1
LPCRST#
LPC_FGPI2
LPC_FGPI3
VPP
LPC_FGPI4
U91
R412
10KR2
24 LPCROM_WP#
LPC_FGPI1
LPC_FGPI0
LPC_LAD0
SELECT_LPC
LPC_CE#
R842
0R3-U
LPC_LFRAME# 24,38,39,42
W39V040FAP-1
YME SB
LPC_LAD1
LPC_LAD2
LPC_LAD3
TOP VIEW
A15 (B1)
A14 (B2)
A2 (B14)
A1 (B15)
(BOTTOM VIEW)
GOLDEN FINGER FOR DEBUG BOARD
5V_S0
CN2
PCIRST#2
LPC_LFRAME#
3 CLK33_DBG
CLK33_DBG
INIT#_SERIRQ
LPC_LAD3
LPC_LAD2
LPC_LAD1
LPC_LAD0
EXT_LPC#
FOX-GF30
ZZ.GF030.XXX
PLCC 32pin ST: 72.50040.003
PLCC 32pin SST:
72.49004.B03
U16
LPC_INIT#
R120
0R2-0
NC7SZ384-1-U
ZZ.7SZ384.0A0
EXT_LPC#
INIT#_SERIRQ
U19
24,29,31,38,39,42 P_SERIRQ
P_SERIRQ
NC7SZ66P5X
ZZ.7SZ66.0AH
new LPC extension debug board to provide serial and parallel port from outside the mainboard, to let software team more easily to debug.
4,5,6,24,25,35,44,45,46,54 VCC_CORE
3,4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,31,32,33,34,35,36,37,38,39,40,42,44,47,50,53,54,56,57,58
21,22,24,25,28,29,30,34,35,36,37,39,40,42,43,44,45,46,53,56,57,58
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Title
LPCROM / DEBUG PORT
Size A3
Document Number
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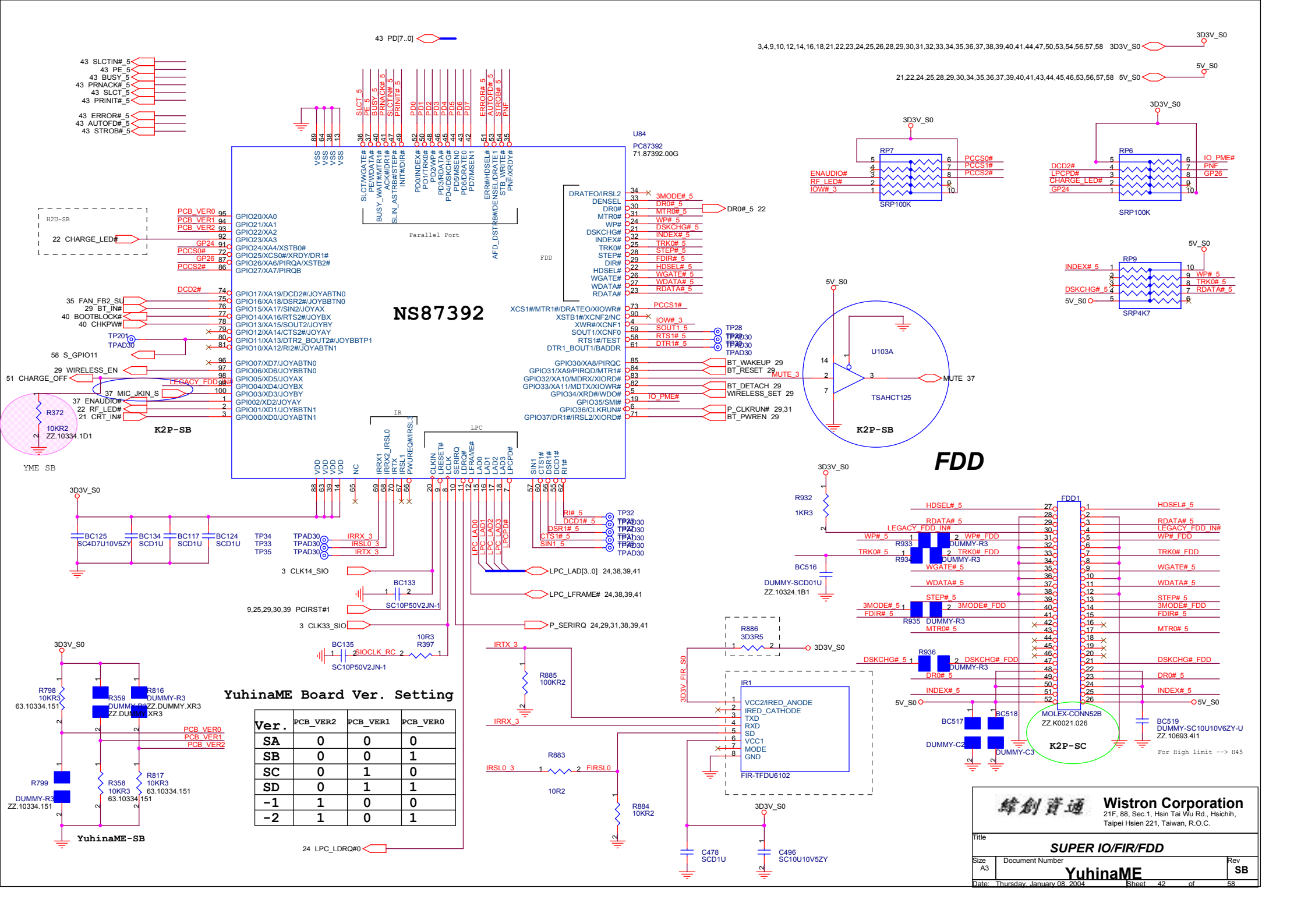
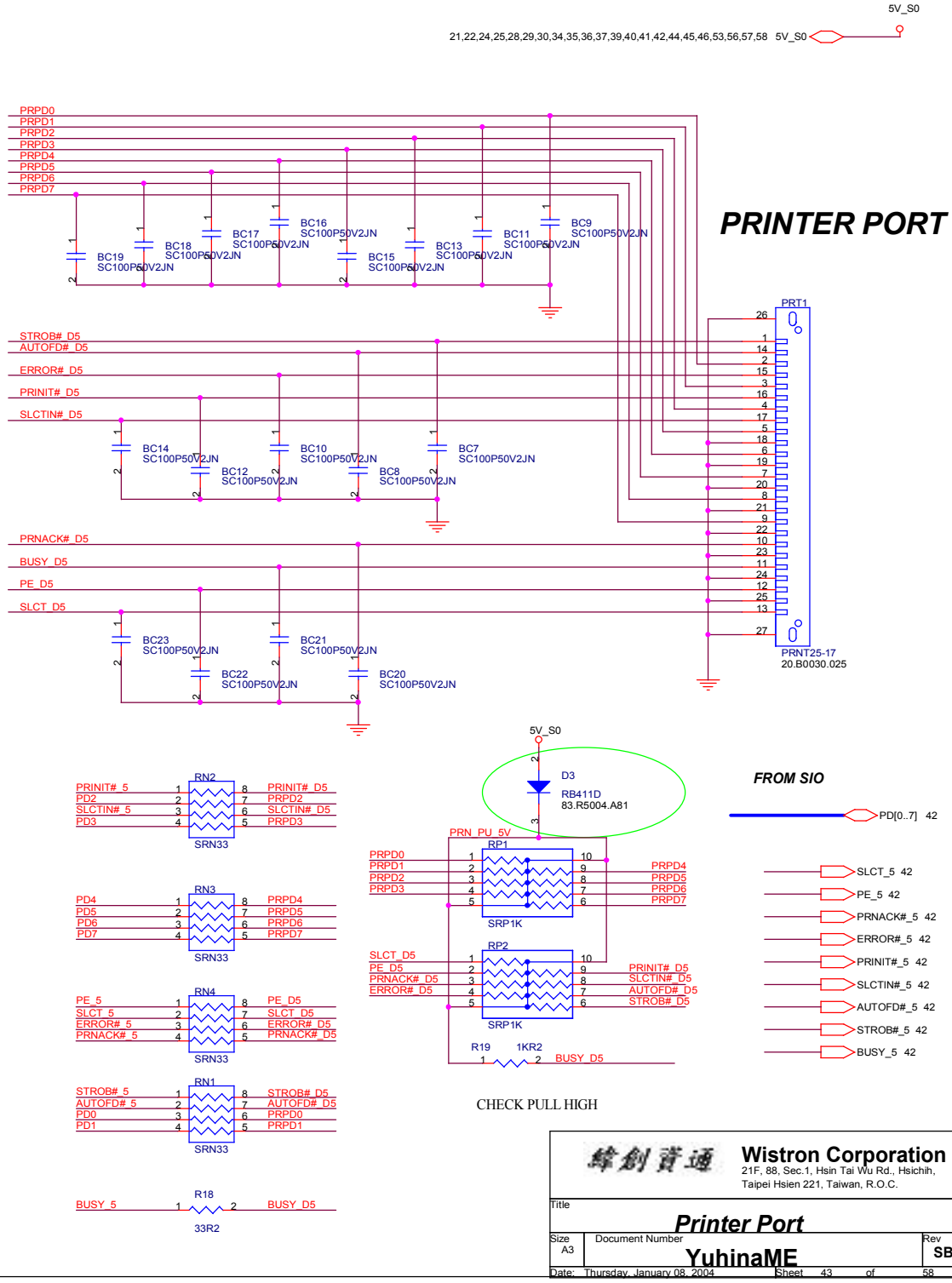


YuhinaME Board Ver. Setting

Ver.	PCB_VER2	PCB_VER1	PCB_VER0
SA	0	0	0
SB	0	0	1
SC	0	1	0
SD	0	1	1
-1	1	0	0
-2	1	0	1


5V_S0
21,22,24,25,28,29,30,34,35,36,37,39,40,41,42,44,45,46,53,56,57,58 5V_S0
PRINTER PORT
PRPD0
PRPD1
PRPD2
PRPD3
PRPD4
PRPD5
PRPD6
PRPD7
BC19 SC100P50V2JN
BC18 SC100P50V2JN
BC17 SC100P50V2JN
BC16 SC100P50V2JN
BC15 SC100P50V2JN
BC13 SC100P50V2JN
BC11 SC100P50V2JN
BC9 SC100P50V2JN
PRT1
STROB# D5
AUTOFD# D5
ERROR# D5
PRINIT# D5
SLCTIN# D5
BC14 SC100P50V2JN
BC12 SC100P50V2JN
BC10 SC100P50V2JN
BC8 SC100P50V2JN
BC7 SC100P50V2JN
PRNACK# D5
BUSY D5
PE D5
SLCT D5
BC23 SC100P50V2JN
BC22 SC100P50V2JN
BC21 SC100P50V2JN
BC20 SC100P50V2JN
PRNT25-17
20.B0030.025
RN2
PRINIT# 5
PD2
SLCTIN# 5
PD3
PRINIT# D5
PRPD2
SLCTIN# D5
PRPD3
SRN33
RN3
PD4
PD5
PD6
PD7
PRPD4
PRPD5
PRPD6
PRPD7
SRN33
RN4
PE 5
SLCT 5
ERROR# 5
PRNACK# 5
PE D5
SLCT D5
ERROR# D5
PRNACK# D5
SRN33
RN1
STROB# 5
AUTOFD# 5
PD0
PD1
STROB# D5
AUTOFD# D5
PRPD0
PRPD1
SRN33
R18
BUSY 5
BUSY D5
33R2
5V_S0
D3
RB411D
83.R5004.A81
PRN_PU_5V
RP1
PRPD0
PRPD1
PRPD2
PRPD3
PRPD4
PRPD5
PRPD6
PRPD7
SRP1K
RP2
SLCT D5
PE D5
PRNACK# D5
ERROR# D5
PRINIT# D5
SLCTIN# D5
AUTOFD# D5
STROB# D5
SRP1K
R19 1KR2
BUSY D5
FROM SIO
PD[0..7] 42
SLCT_5 42
PE_5 42
PRNACK#_5 42
ERROR#_5 42
PRINIT#_5 42
SLCTIN#_5 42
AUTOFD#_5 42
STROB#_5 42
BUSY_5 42
CHECK PULL HIGH
Wistron Corporation
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CPU_Vcore IMVP5_FMS1 (1/2)

for Desktop CPU

FOR NORTHWOOD ONLY

PLACE IN THE BACK OF CPU

300mA SUPPORT

VNTC trip point = 0.5V

Vramp=1/9*Vin

PWM4 Dummy
Deep Offset = 1.7%

Soft Start = 2mSec.

Tie to CPU side

Connect with CAP.

N=2.34K*39.5uA=96mV(Spec.=99mV)
P=(11.3K/2.43K)*48.7uA=97mV(Spec.=80A*1.3m=104mV)

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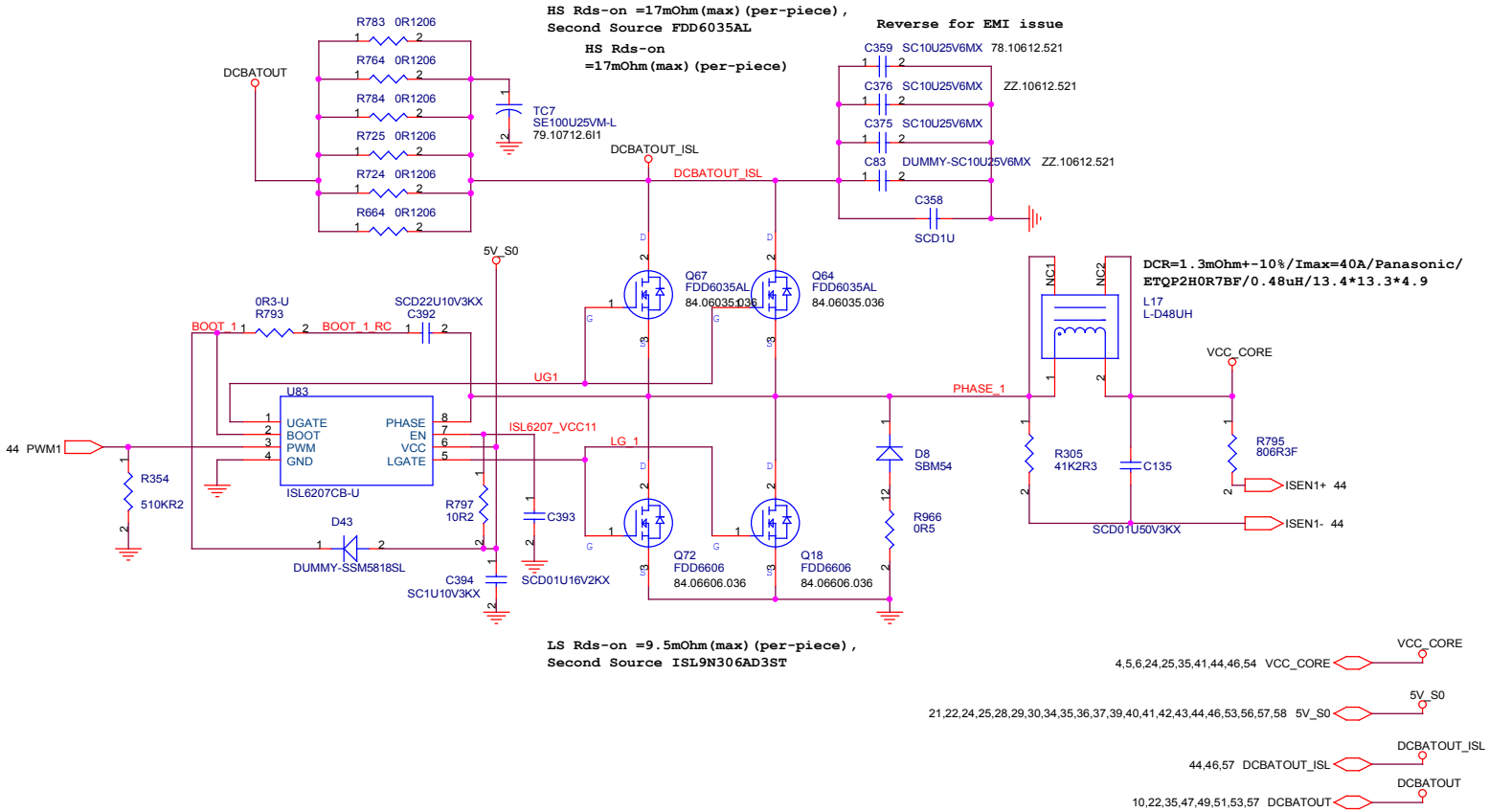
Title	CPU_Vcore IMVP5_FMS1 (1/2)
Size A3	Document Number YuhinaME Rev SB
Date: Thursday, January 08, 2004	Sheet 44 of 58

Voltage Identication Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
X	1	1	1	1	1	OFF
0	0	1	0	1	0	0.8375
1	0	1	0	0	1	0.8500
0	0	1	0	0	1	0.8625
1	0	1	0	0	0	0.8750
0	0	1	0	0	0	0.8875
1	0	0	1	1	1	0.9000
0	0	0	1	1	1	0.9125
1	0	0	1	1	0	0.9250
0	0	0	1	1	0	0.9375
1	0	0	1	0	1	0.9500
0	0	0	1	0	1	0.9625
1	0	0	1	0	0	0.9750
0	0	0	1	0	0	0.9875
1	0	0	0	1	1	1.0000
0	0	0	0	1	1	1.0125
1	0	0	0	1	0	1.0250
0	0	0	0	1	0	1.0375
1	0	0	0	0	1	1.0500
0	0	0	0	0	1	1.0625
1	0	0	0	0	0	1.0750
0	0	0	0	0	0	1.0875
1	1	1	1	1	0	1.1000
0	1	1	1	1	0	1.1125
1	1	1	1	0	1	1.1250
0	1	1	1	0	1	1.1375
1	1	1	1	0	0	1.1500
0	1	1	1	0	0	1.1625
1	1	1	0	1	1	1.1750
0	1	1	0	1	1	1.1875
1	1	1	0	1	0	1.2000
0	1	1	0	1	0	1.2125
1	1	1	0	0	1	1.2250
0	1	1	1	1	1	1.2375
1	1	1	0	0	0	1.2500
0	1	1	0	0	0	1.2625
1	1	0	1	1	1	1.2750
0	1	0	1	1	1	1.2875
1	1	0	1	1	0	1.3000
0	1	0	1	1	0	1.3125
1	1	0	1	0	1	1.3250
0	1	0	1	0	1	1.3375
1	1	0	1	0	0	1.3500
0	1	0	1	0	0	1.3625
1	1	0	0	1	1	1.3750
0	1	0	0	1	1	1.3875
1	1	0	0	1	0	1.4000
0	1	0	0	1	0	1.4125
1	1	0	0	0	1	1.4250
0	1	0	0	0	1	1.4375
1	1	0	0	0	0	1.4500
0	1	0	0	0	0	1.4625
1	0	1	1	1	1	1.4750

Voltage Identication Codes

VID5	VID4	VID3	VID2	VID1	VID0	VDAC
0	0	1	1	1	1	1.4875
1	0	1	1	1	0	1.5000
0	0	1	1	1	0	1.5125
1	0	1	1	0	1	1.5250
0	0	1	1	0	1	1.5375
1	0	1	1	0	0	1.5500
0	0	1	1	0	0	1.5625
1	0	1	0	1	1	1.5750
0	0	1	0	1	1	1.5875
1	0	1	0	1	0	1.6000



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Title: CPU_Vcore IMVP5_FMS1 (2/3)

Size: A3 | Document Number: YuhinaME | Rev: SB

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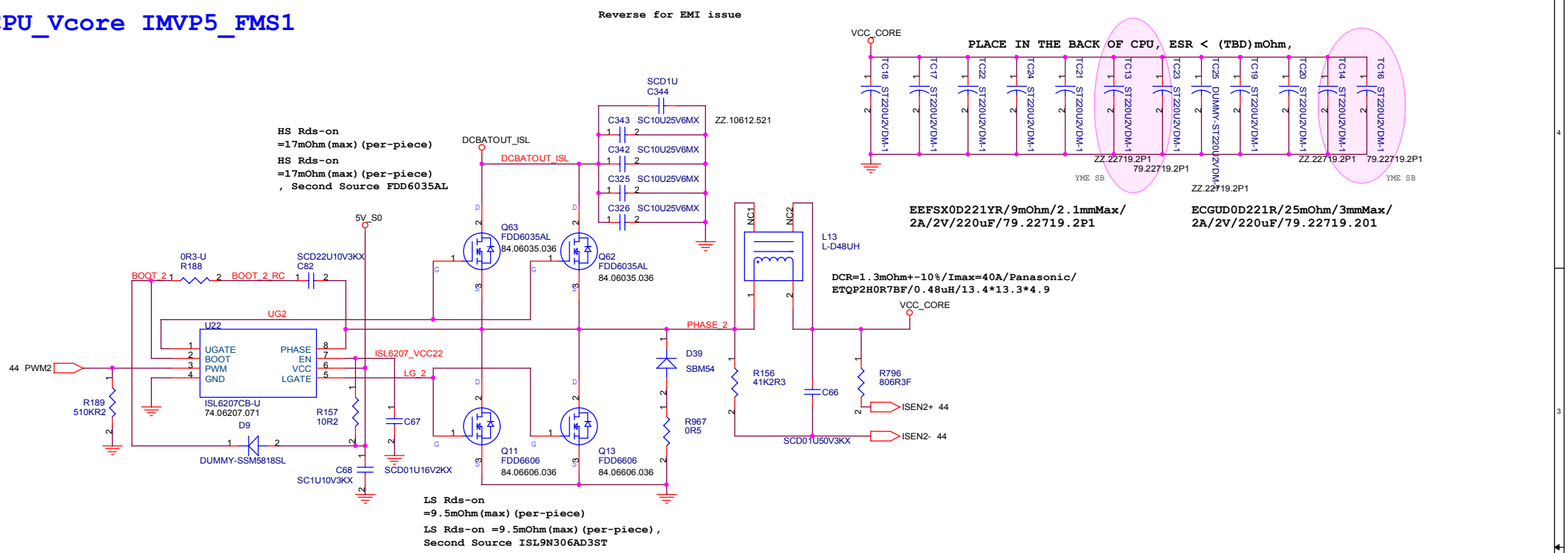
CPU_Vcore IMVP5_FMS1



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Title: CPU_Vcore IMVP5_FMS1 (3/3)

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TI TPS5130 for 3.3V, 5V, 2.5V and 1.8V
3.3V_CH2, 5V_CH3, 2.5V_CH1,
Freq.:CT= 47pF / 300KHz

close to IC

OCP1
R848 10K7R3F
OCP_TRIP1
C471
SCD1U50V3ZY
DCBATOUT1
K2P-SA(7K87R3F
OCP=13.95A)

OCP2
R847
OCP_TRIP2
9K09R3F
C470
SCD1U50V3ZY
DCBATOUT1
K2P-SA(6K81R3F
OCP=6.07A)

close to IC

OCP3
R844
OCP_TRIP3
14K7R3F
C466
SCD1U50V3ZY
DCBATOUT1
K2P-SA(10K7R3F
OCP=9.97A)
K2P-SB

R897 0R1206
R898 0R1206
R937 0R1206
DCBATOUT1
DCBATOUT

R(cl)=Rds(on)*(Itrip +Iripple)/(13*10^ -6)
Itrip=OCP

2.5V
1.5V
1.26V

5130_5V_LDO
D21 BAT54-1
5130_5V_LDO_LL2
R462 0R3-U
D27 BAT54-1
5130_5V_LDO_LL1
R464 0R3-U
C493 SCD1U16V
5130_FLT
5130_INV1
48 5130_OUT1_D
48 5130_LL1
48 5130_OUT1_U
48 5130_LH1
48 5130_INV1

AUTO PWM/SKIP
R514 0R2-0
R511 DUMMY-R2

K2P-SC
5V_AUX_S5
5V_S5
R942 10KR2
R530 10KR2 ZZ.10334.1D1
R515 10KR2 ZZ.10334.1D1
Q84 2N7002
Q81 2N7002
2.5V

TPS5130
FB1
SS_STBY1
INV2
FB2
SS_STBY2
PWM_SEL
CT
GND
REF
STBY_VREF5
STBY_VREF3.3
STBY_LDO
INV1
FLT
LH1
OUT1_U
LL1
OUT1_D
OUTGND1
TRIP1
VIN_SENSE12
TRIP2
OUTGND2
OUT2_D
LL2
OUT2_U
LH2
VIN
VREF3.3
VREF5
REG5V_IN
LDO_IN
LDO_CUR
LDO_GATE
LDO_OUT
INV_LDO

U92
5130_OUT2_D 48
5130_LL2 48
5130_OUT2_U 48
5130_LH2 48
DCBATOUT1
5130_3D3V_LDO
5130_5V_LDO
C434 SC1U10V3ZY
C197 SC10U06V5MX
C433 SC10U10V5ZY
close to IC
K2P-SB
5130_REGIN
R458 0R5
R460 0R3-U
R459 10KR2
5V_S5
3D3V_S0
5130_LDOCUR
5130_LDOGATE
5130_LDOOUT
TP45 TPAD30
TP44 TPAD30
LDO_INV

5130_FB1
5130_INV2
5130_FB2
SS_STBY2
5130_PWM_SEL
5130_CT
R874 100KR2 STBY_VREF5
R873 100KR2 STBY_VREF3
STBY_LDO
R872 0R2-0
R871 100KR2
C239 SC4700P50V3KX
C491 SC4700P50V3KX
5130_REF
C489 SC1U10V3XX
SC4700P50V2JN

C468 SC1U10V3ZY
R846 10KR2

24,25,26,31,50,53 PM_SLP_S5#

K2P-SC
5V_AUX_S5
5V_S5
R943 10KR2
R869 10KR2 ZZ.10334.1D1
R845 10KR2 ZZ.10334.1D1
SS_STBY3
Q83 2N7002
C487 SC4700P50V3KX
1.2V
3,10,24,25,39,49,50,53,55 PM_SLP_S3#
Q82 2N7002

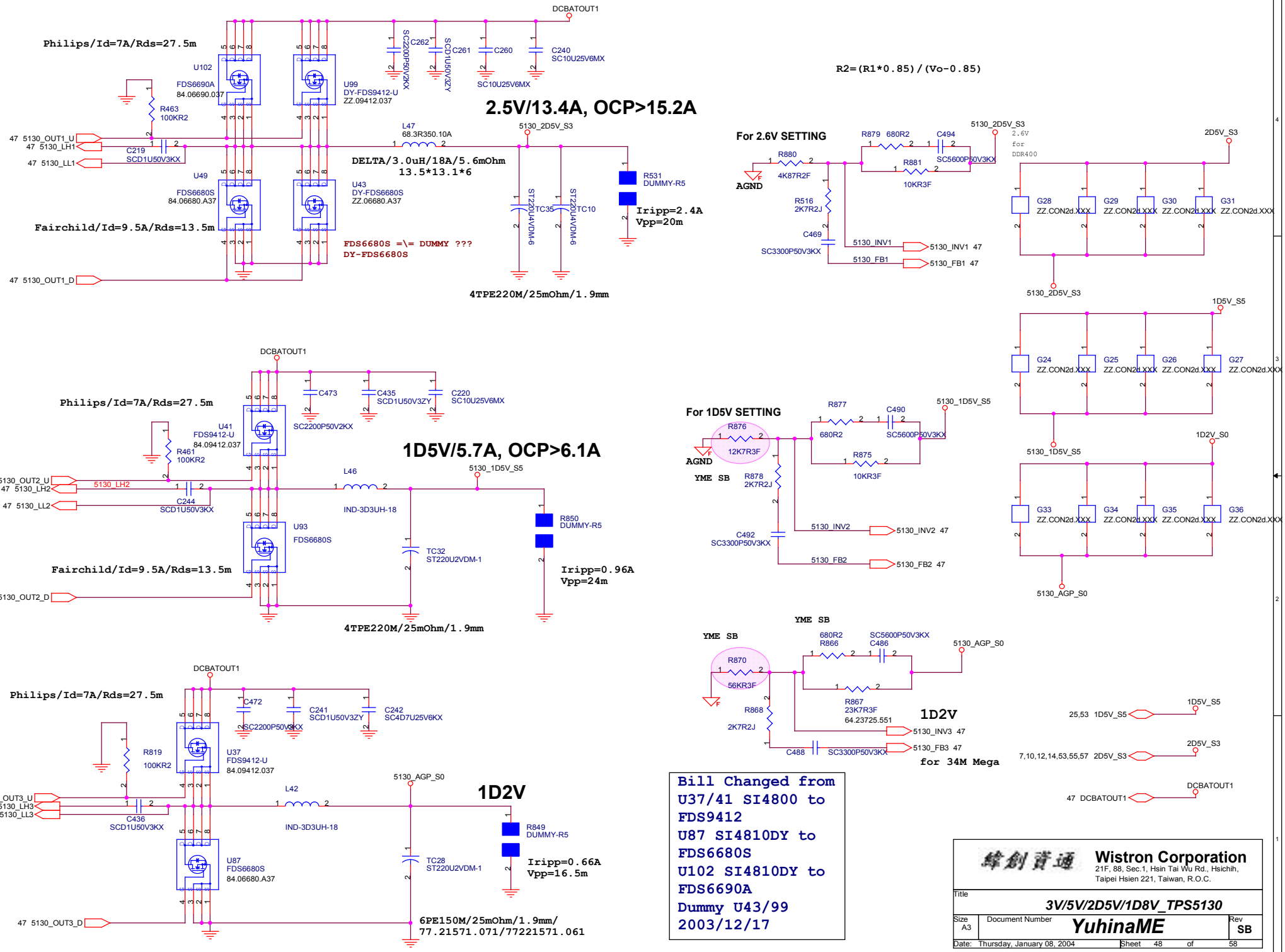
SS_STBY3
FB3
INV3
PGOUT
PG_DELAY
TRIP3
VIN_SENSE3
LH3
OUT3_U
LL3
OUT3_D
OUTGND3
TPS5130PT-U
5130_PGDELAY
5130_OUT3_D 48
5130_LL3 48
5130_OUT3_U 48
5130_LH3 48
48 5130_FB3
48 5130_INV3
C467 SCD01U16V2KX
R456 0R3-U
5130_5V_LDO_LL3
D24 BAT54-1
5130_5V_LDO
OCP_TRIP3
DCBATOUT1

G43 GAP-CLOSE
G42 GAP-CLOSE

Q95 2N7002
YME SB
5V_S5
R512 10KR2 ZZ.10334.1D1
1.5V
SS_STBY2
49,50 SHUTDOWN_S5
Q42 2N7002 ZZ.27002.031
C258 SC4700P50V3KX
R513 100KR2 ZZ.10434.1D1

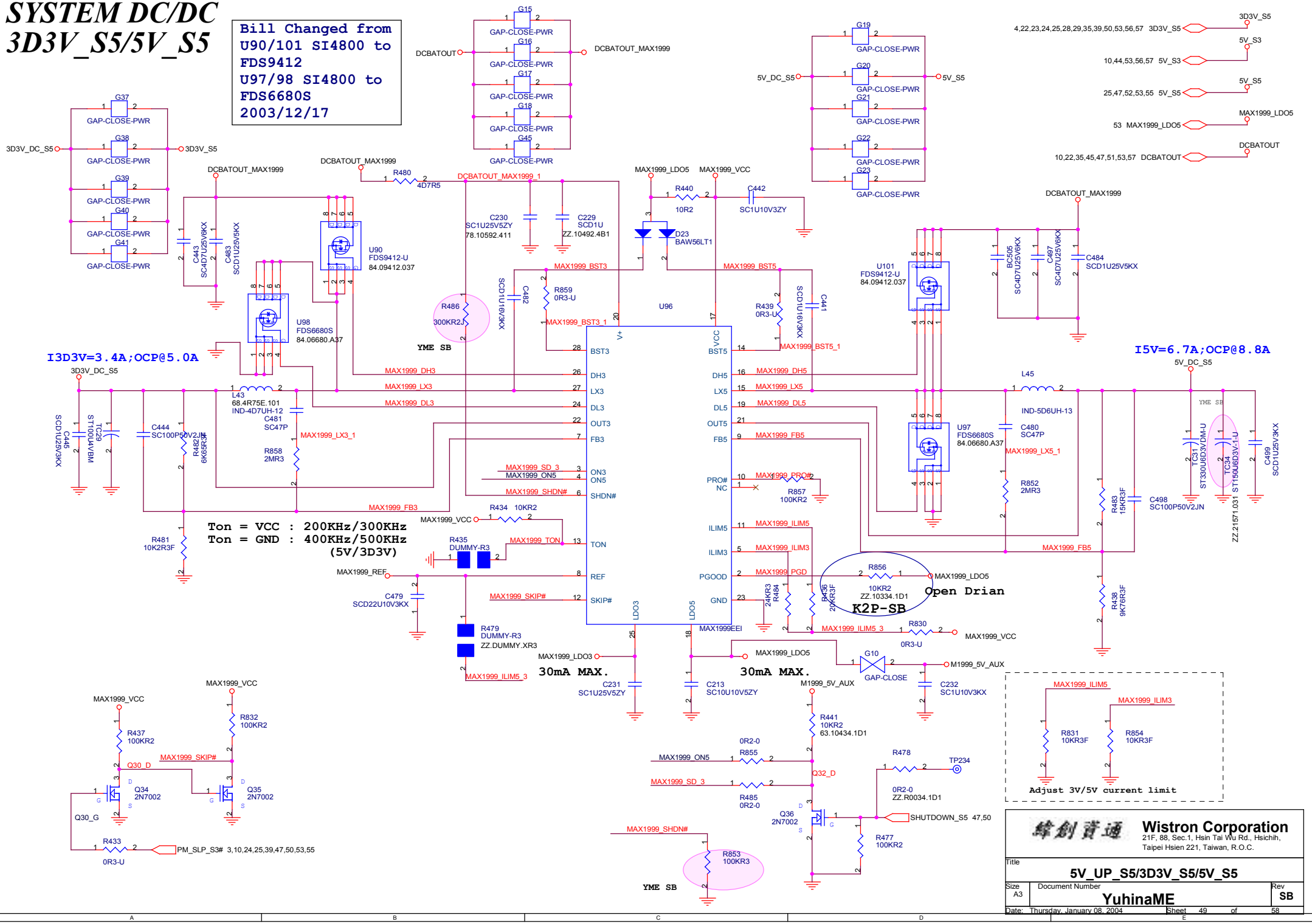
7,10,12,14,48,53,55,57 2D5V_S3
2D5V_S3
48 DCBATOUT1
DCBATOUT1
10,22,35,45,49,51,53,57 DCBATOUT
DCBATOUT

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 3V/5V/2D5V/1D8V_TPS5130		
Size: A3	Document Number: YuhinaME	Rev: SB
Date: Thursday, January 08, 2004	Sheet 47 of 58	


Philips/Id=7A/Rds=27.5m
Fairchild/Id=9.5A/Rds=13.5m
2.5V/13.4A, OCP>15.2A
DELTA/3.0uH/18A/5.6mOhm
13.5*13.1*6
FDS6680S =\= DUMMY ???
DY-FDS6680S
Iripp=2.4A
Vpp=20m
4TPE220M/25mOhm/1.9mm
R2=(R1*0.85)/(Vo-0.85)
For 2.6V SETTING
1D5V/5.7A, OCP>6.1A
Iripp=0.96A
Vpp=24m
For 1D5V SETTING
YME SB
1D2V
Iripp=0.66A
Vpp=16.5m
6PE150M/25mOhm/1.9mm/
77.21571.071/77221571.061
for 34M Mega
Bill Changed from
U37/41 SI4800 to
FDS9412
U87 SI4810DY to
FDS6680S
U102 SI4810DY to
FDS6690A
Dummy U43/99
2003/12/17
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
3V/5V/2D5V/1D8V_TPS5130
YuhinaME
Date: Thursday, January 08, 2004
Sheet 48 of 58

SYSTEM DC/DC 3D3V_S5/5V_S5

Bill Changed from
U90/101 SI4800 to
FDS9412
U97/98 SI4800 to
FDS6680S
2003/12/17



Bill Changed from
U57 SI4425DY to AO4407
2003/12/17

DCIN1
Layout trace 200 mil
AD_JACK+
L3
0R1206
63.R0032.111
LB1 0R1206
C12
SCD1U50V3KX 63.R0032.111
78.10424.2B1
DC-JACK74-U
ZZ.10134.1F1
SC100P50V2JN
Layout trace 200 mil
ADJACK
BC34
BC33
SCD1U
U57
AO4407
84.04407.037
AD+
D4
MMBZ5246BLT
83.16R03.A31
D45_RPO
R47
0R3-U
R52
100KR2
BC35
SC1U50V5ZY
C26
SCD1U50V3KX
Q20_L
R50
475R3F
AD_SWITCH
R51
56KR3
C11
SC1U16V5ZY
78.10591.411
R20
100KR2
R21
56KR3
5V_AUX_S5
AC_IN 22,39,51,53,57
Q18_G
Q51
2N7002
Q56
DTC124EUA-U1
84.00124.C1K
22 K
22 K
AD_OFF#
R555
10KR2
AD_OFF_1
39 AD_OFF
R556
100KR2
BC304
SCD01U16V2JX
78.10321.2F1
Q57
2N7002
Q3
DTA124EUA-U1
84.00124.B1K
K2P USED
22.10037.501
Change from KBC GPIO43 to SIS963
GPIO13.

3D3V_S5
4,22,23,24,25,28,29,35,39,49,53,56,57 3D3V_S5
3D3V_S0
3,4,9,10,12,14,16,18,21,22,23,24,25,26,28,29,30,31,32,33,34,35,36,37,38,39,40,41,42,44,47,53,54,56,57,58 3D3V_S0
5V_AUX_S5
35,38,47,53,57 5V_AUX_S5

PWR_CTL Logic BY Hardware

5V_AUX_S5
R789 22KR2J
MP3_PR
U70A
TSAHCT74
ZZ.07474.0JB
C380
SCD1U
MP3_PWRBTN#_1
U71C
TSAHCT14
MP3_PWRBTN#
C148
SCD1U
ZZ.10492.4B1
3D3V_S5
R319
10KR2
DUMMY-R2
R318
MP3_U55_Q
24 MP3PWR_ON#
D14
RB751V-40-U
ZZ.R2004.08F
R321
1KR2
ZZ.10234.1D1
K3D-SB
MP3_D
Q27_D
MP3_CL#
Q20
2N7002
ZZ.27002.031

5V_AUX_S5
R790
22KR2J
ZZ.22334.1D1
BC497
SCD1U16V
ZZ.10491.4F1
Q73
2N7002
ZZ.27002.031
HI_PAUSE
U69
NC7ST08-U
ZZ.7ST08.0BG
DL_ALL_PG
U71E
TSAHCT14
MP3_SLP_S3
MP3_SLP_S3_1
R771
10KR2
U71D
TSAHCT14
PM_SLP_S3# 3,10,24,25,39,47,49,53,55
BC495
SC1U10V3ZY
ZZ.10593.4B1

PWRBTN_3
R770 47KR2
PWRBTN_2
BC493
SC1U10V3ZY
K3D-SB
U71B
TSAHCT14
24 PWRBTN#_ICH
D41
S1N4148-U
PM_PWRBTN#_1
U72A
TSAHCT32
U70B
TSAHCT74
U50_PR
R769
10KR2
PWRBTN_74
PM_SLP_S5#
PM_SLP_S5# 24,25,26,31,47,53
U71A
TSAHCT14
PWRBTN#
PWRBTN# 38
52,53 SYS_S0_G
R330
0R2-0
ZZ.R0034.1D1
6,24,35,52 PWROK
R329
DUMMY-R2
K2P-SB
R331
10KR2
ZZ.10334.1D1
12VGATE_30
Q21
2N7002
MP3BT_ON#
MP3BT_ON# 24
MP3_PWRBTN# 38
U31
NC7SZ125-U
ZZ.7S125.0AH
D15
S1N4148-U
ZZ.04148.011
U58_Y
U71F
TSAHCT14
47,49 SHUTDOWN_S5
SHUTDOWN_S5
RB3
DUMMY-R3
SD#_S5
SD_S5
SD_S5_P
AC_IN
U72B
TSAHCT32
73.07432.0JB
3D3V_S0
R313
10KR2
Q26_G
Q19
2N7002
U50_CL
R788
22KR2J
BC494
SCD1U
HW_THRM_SDN 35
U72C
TSAHCT32
73.07432.0JB

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: PWR CTL LOGIC / ADT / DC CONN
Size: A3
Document Number: YuhinaME
Rev: SB
Date: Thursday, January 08, 2004
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CHARGER CIRCUIT

old:64.11515.651

imax_set LOW: Vcls=1.1983V
Pmax=(1.1982/0.2)*20V=119.82W

Rating 4.9A

SB

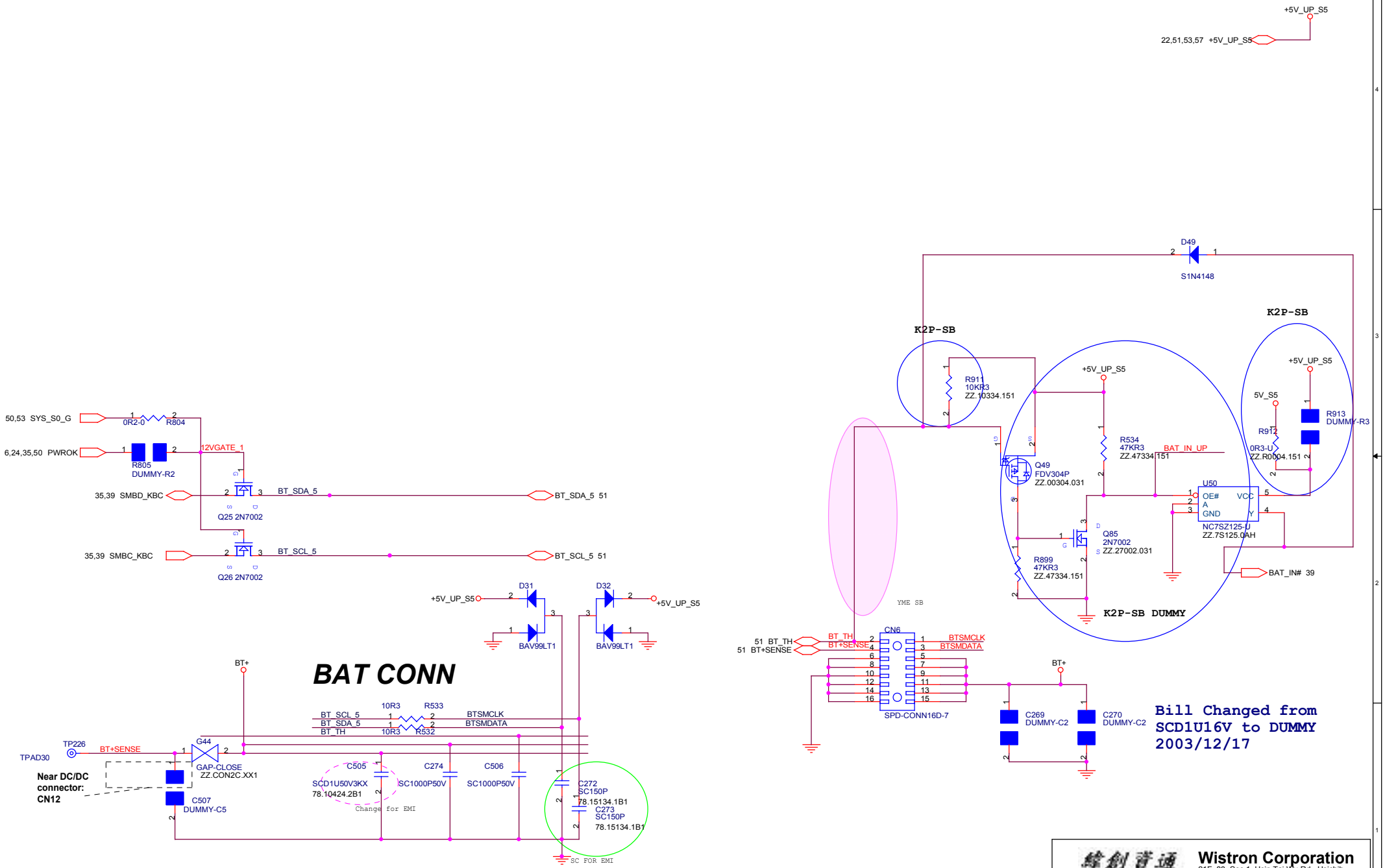
IF IMAX_SET
LOW->120W,HI->98W

K2P-SB

0x12

Bill Changed from
U94/95 SI4892DY to
FDS6674
U45/46/100
SI4425DY to AO4407
2003/12/17

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	*Battery Charger Max1645*
Size A3	Document Number: YuhinaME
Rev	SB
Date: Thursday, January 08, 2004	Sheet 51 of 58


+5V_UP_S5
22,51,53,57 +5V_UP_S5
D49
S1N4148
K2P-SB
K2P-SB
50,53 SYS_S0_G
6,24,35,50 PWROK
0R2-0
R804
R805
DUMMY-R2
12VGATE_1
35,39 SMBD_KBC
35,39 SMBC_KBC
BT_SDA_5
BT_SCL_5
Q25 2N7002
Q26 2N7002
BT_SDA_5 51
BT_SCL_5 51
R911
10KR3
ZZ.10334.151
Q49
FDV304P
ZZ.00304.031
R534
47KR3
ZZ.47334.151
BAT_IN_UP
U50
OE#
A
GND
VCC
Y
NC7SZ125-U
ZZ.7S125.0AH
Q85
2N7002
ZZ.27002.031
R899
47KR3
ZZ.47334.151
K2P-SB DUMMY
5V_S5
R913
DUMMY-R3
R912
0R3-U
ZZ.R0004.151
BAT_IN# 39
YME SB
51 BT_TH
51 BT+SENSE
CN6
BTSMCLK
BTSMDATA
SPD-CONN16D-7
C269
DUMMY-C2
C270
DUMMY-C2
D31
D32
BAV99LT1
BAV99LT1
BAT CONN
BT+
TP226
TPAD30
BT+SENSE
G44
GAP-CLOSE
ZZ.CON2C.XX1
Near DC/DC
connector:
CN12
C507
DUMMY-C5
10R3
R533
10R3
R532
BT_SCL_5
BT_SDA_5
BT_TH
BTSMCLK
BTSMDATA
C505
SCD1U50V3KX
78.10424.2B1
Change for EMI
C274
SC1000P50V
C506
SC1000P50V
C272
SC150P
78.15134.1B1
C273
SC150P
78.15134.1B1
SC FOR EMI
Bill Changed from
SCD1U16V to DUMMY
2003/12/17
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Micro-P Tiny 12
Size
A3
Document Number
YuhinaME
Rev
SB
Date: Thursday, January 08, 2004
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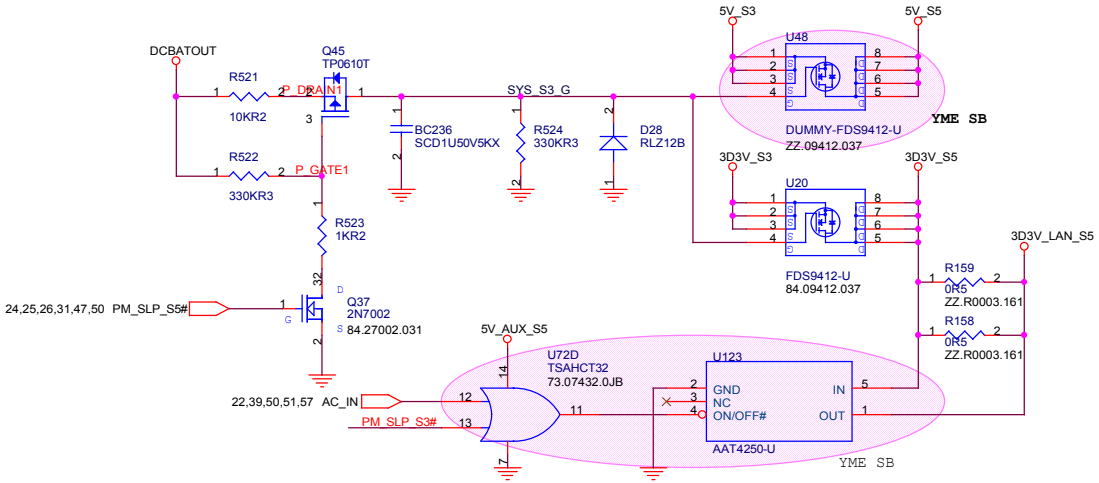
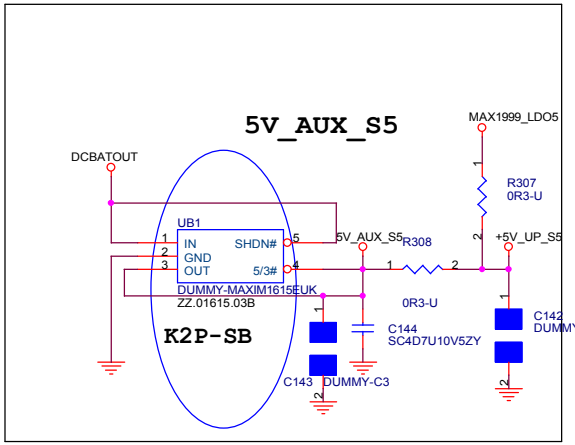
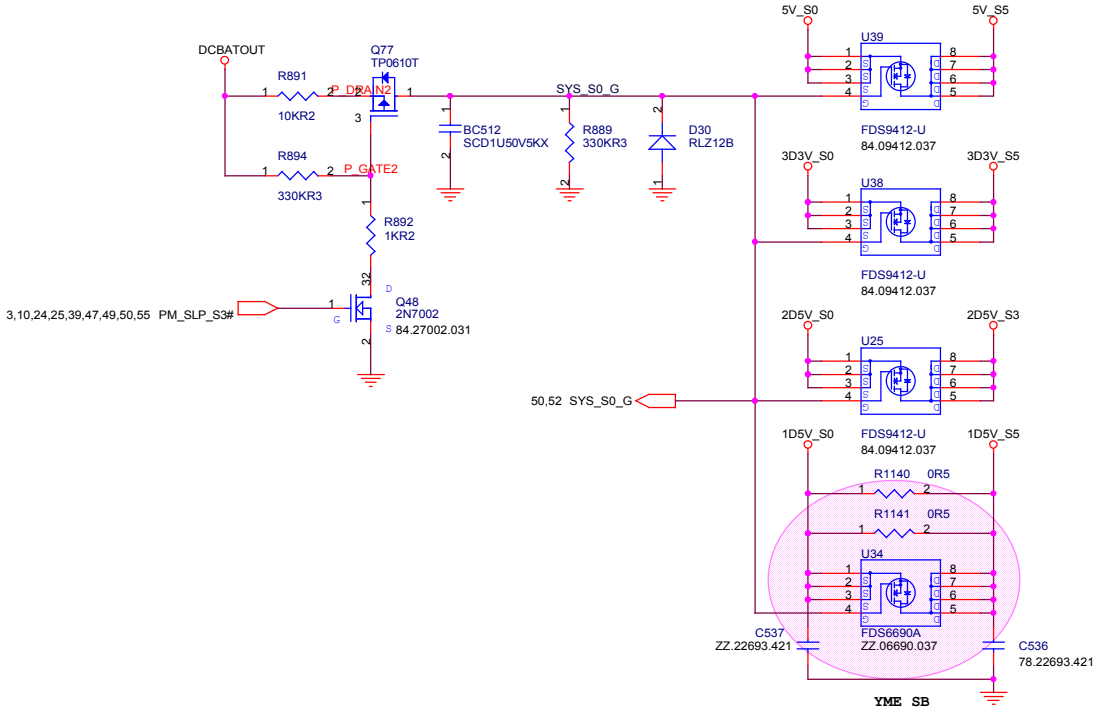
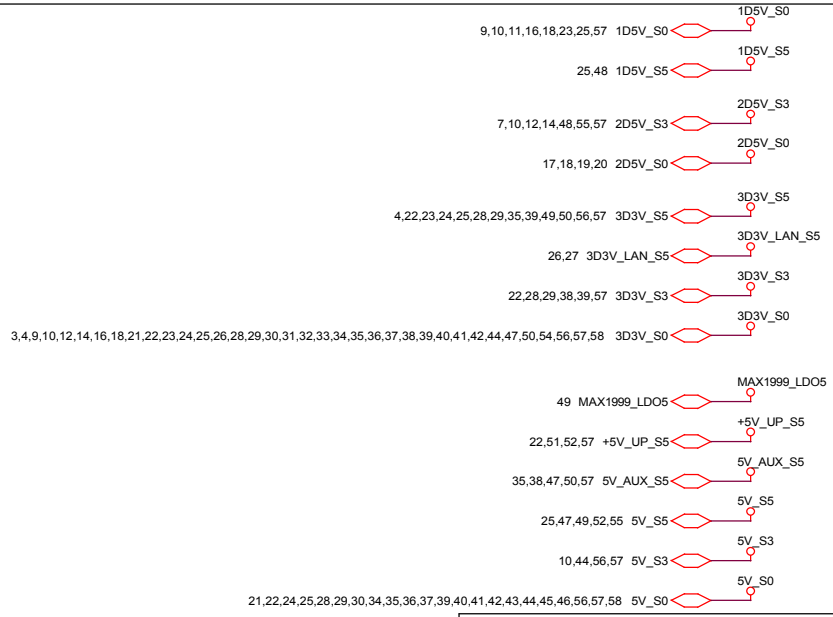
K2P-SB

Bill Changed from Philips
SI4800
84.04800.A37
2003/12/17









Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **3D3V_S3/5V_S3/1D5V_S0/2D5V_S0/3D3V_S0/5V_S0/5V_AUX_S5**

Size: A3 | Document Number: **YuhinaME** | Rev: SB

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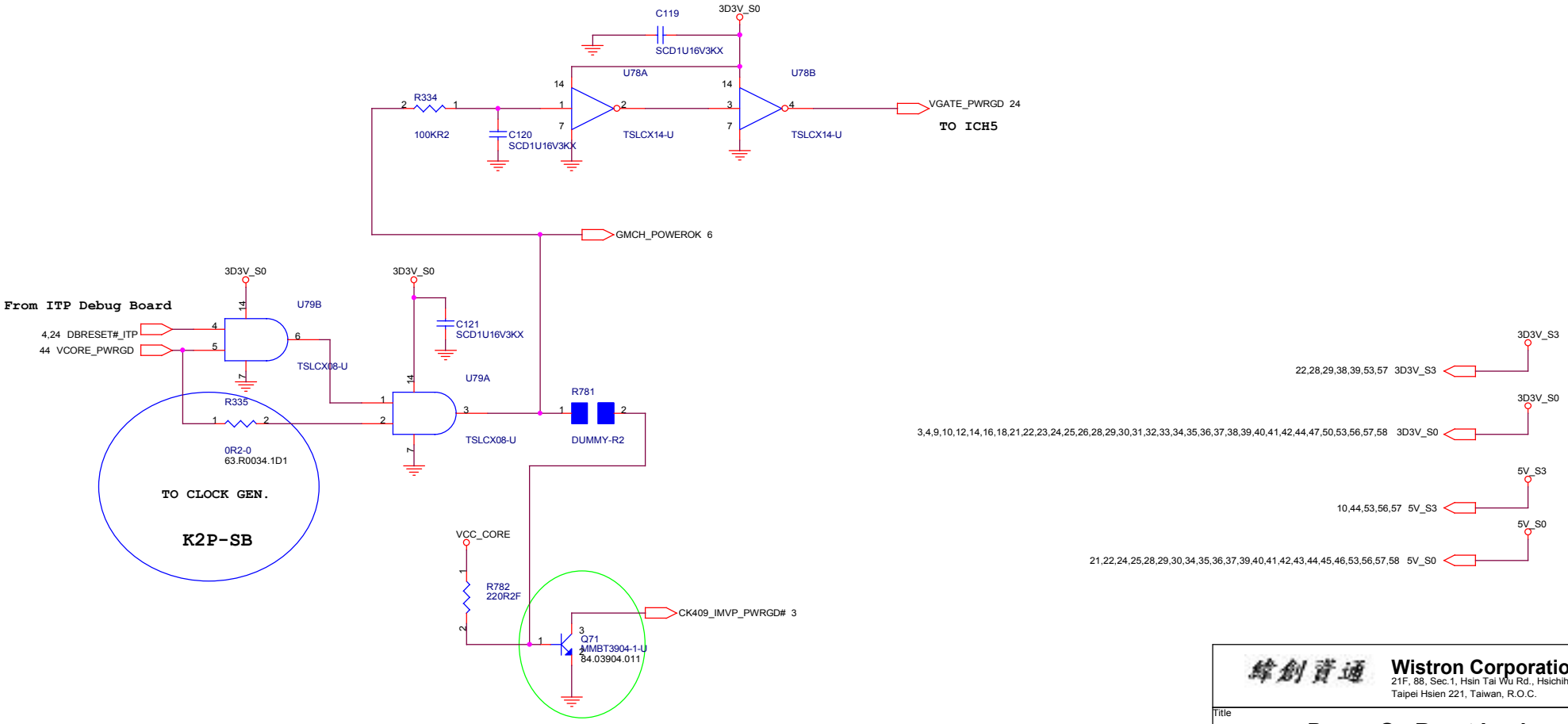
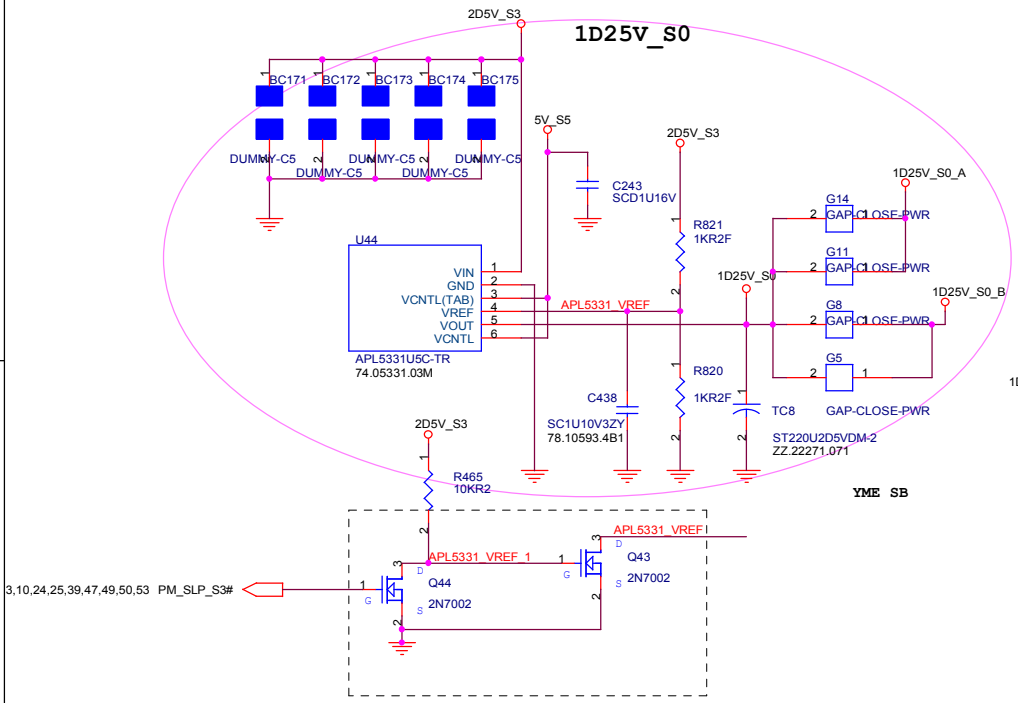
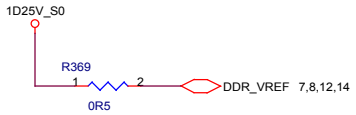
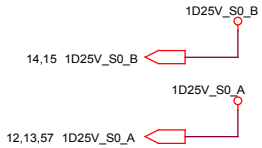


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Power On Reset Logic**	
Size A3	Document Number **YuhinaME**	Rev **SB**
Date: Thursday, January 08, 2004	Sheet 54 of 58	

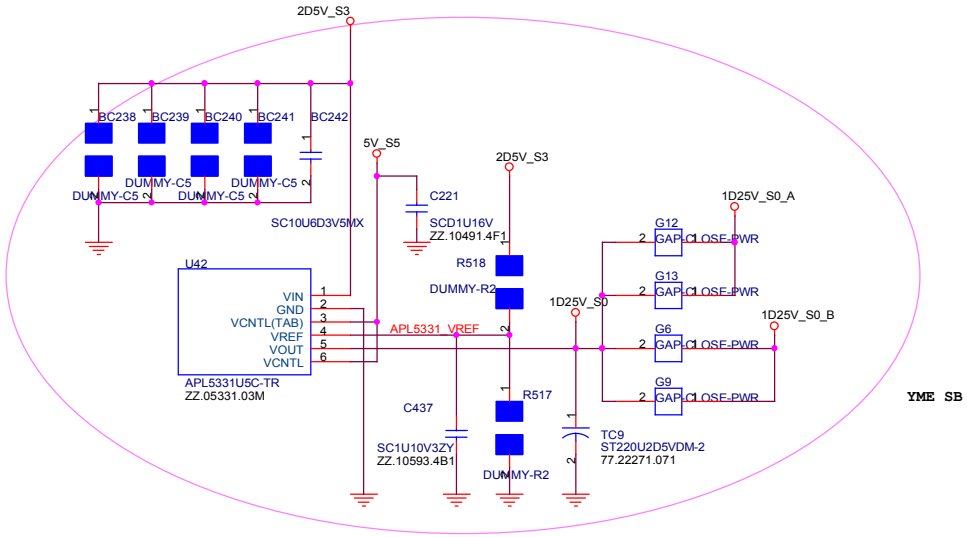




Target adding division resistors from 2D5V_S3



DUMMY



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: APL5331-1D25V_S3		
Size: A3	Document Number: YuhinaME	Rev: SB
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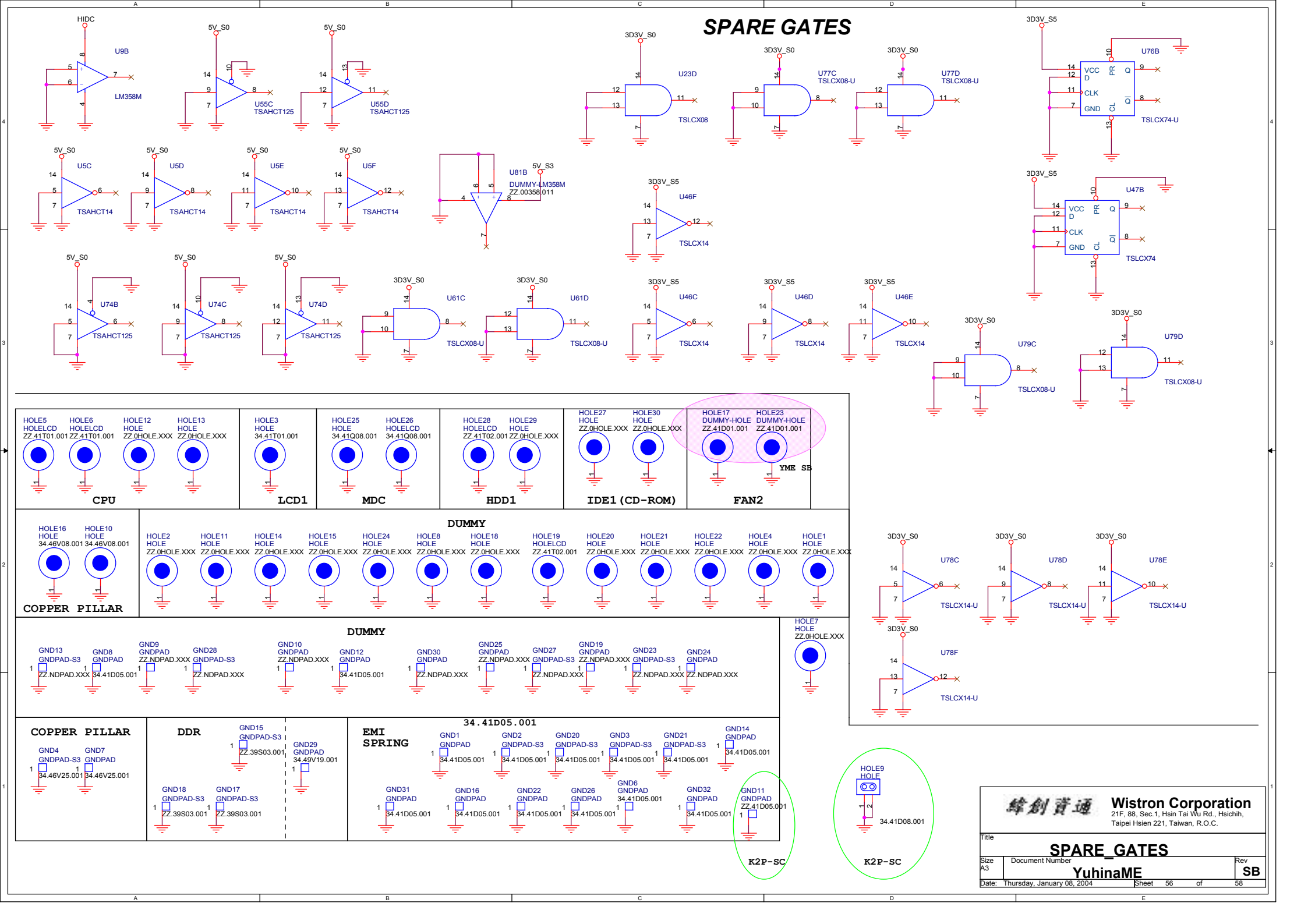
SPARE GATES



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: SPARE_GATES

Size: A3 | Document Number: YuhinaME | Rev: SB

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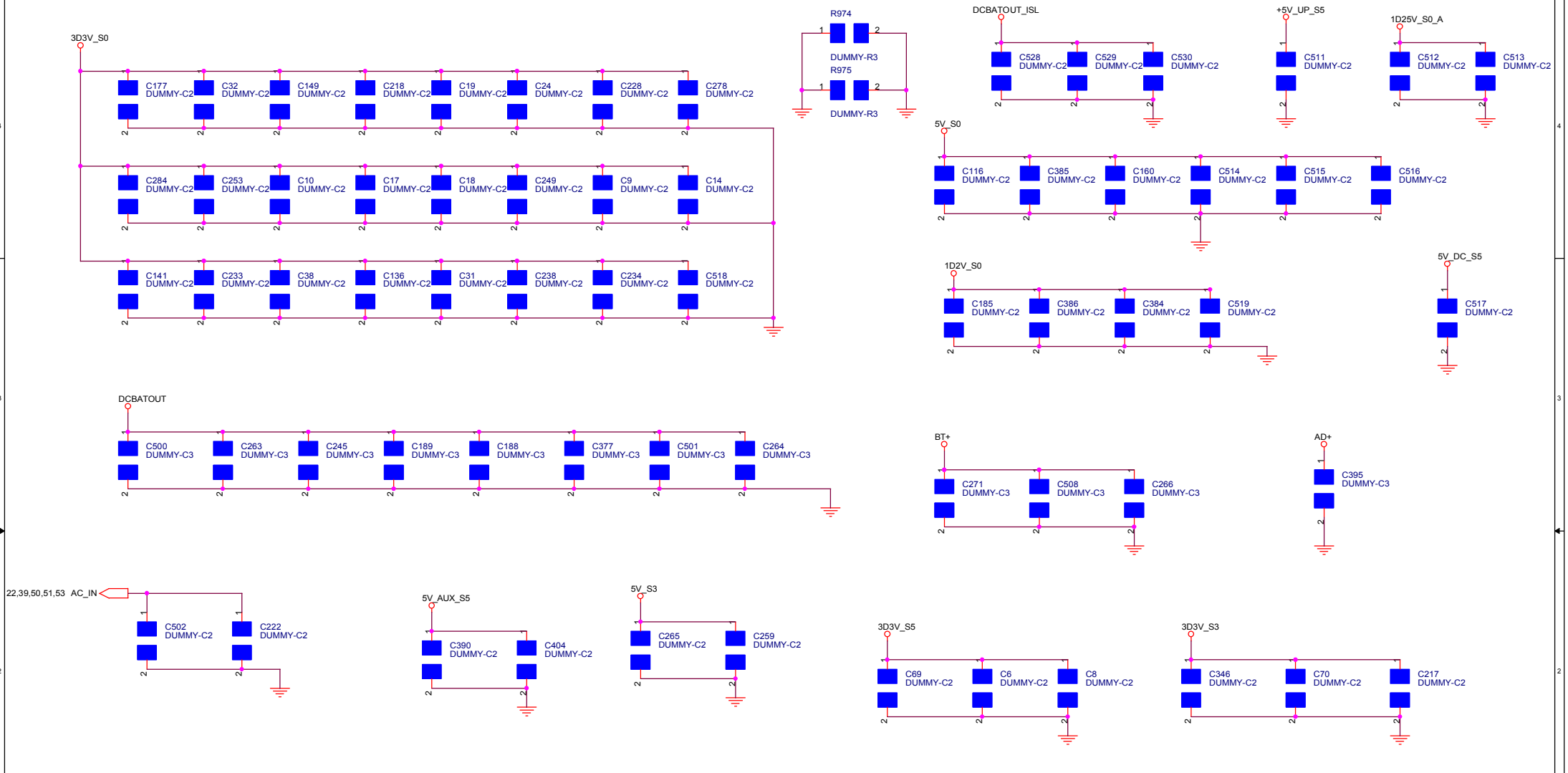
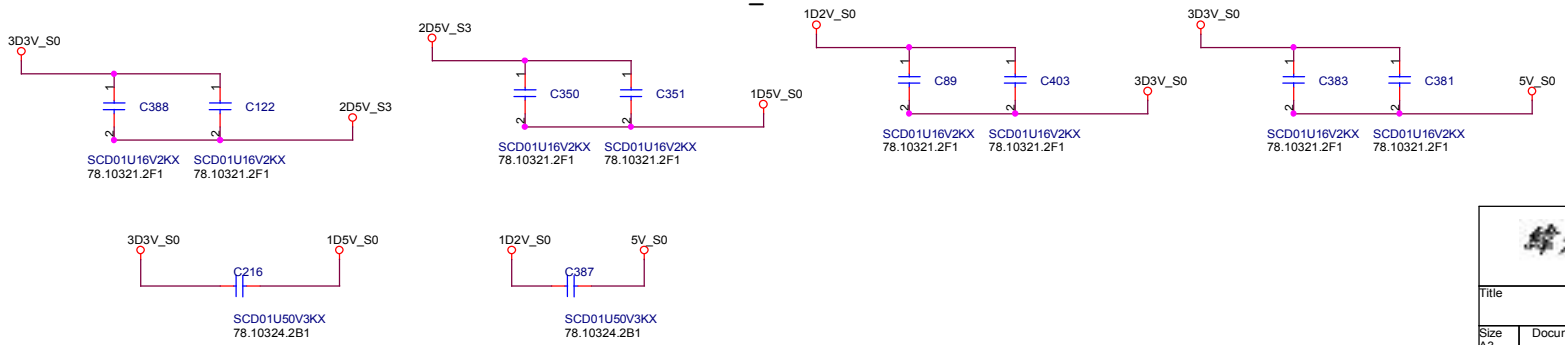


K2P_SB



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Bypass CapacitorS**	
Size A3	Document Number **YuhinaME**	Rev **SB**
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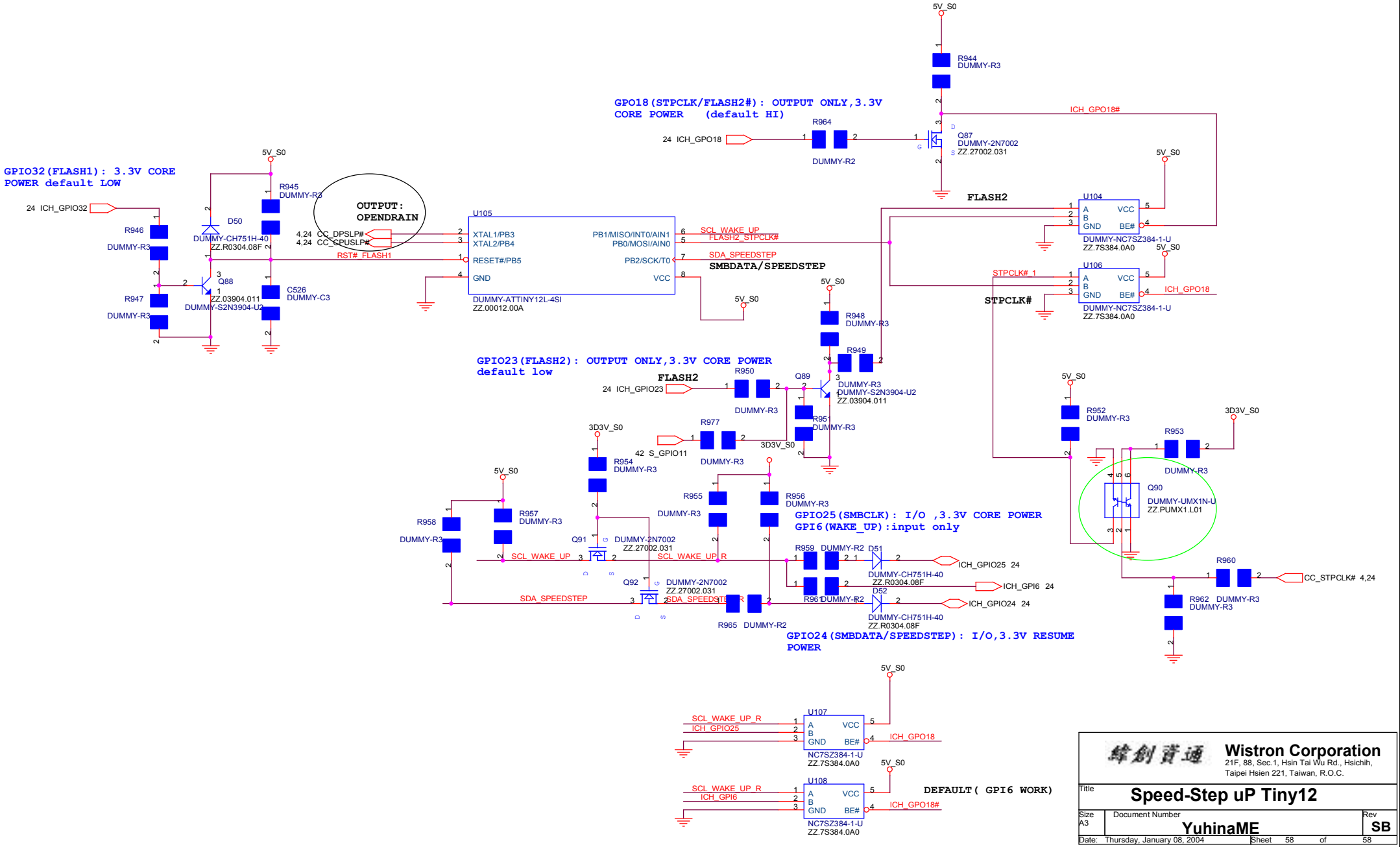
K2P-SC SPEED STEP FUNCTION

GPIO22(GHI#): OUTPUT ONLY(OPEN DRAIN),3.3V CORE POWER



Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: Speed-Step uP Tiny12		
Size: A3	Document Number: YuhinaME	Rev: SB
Date: Thursday, January 08, 2004	Sheet 58 of 58	