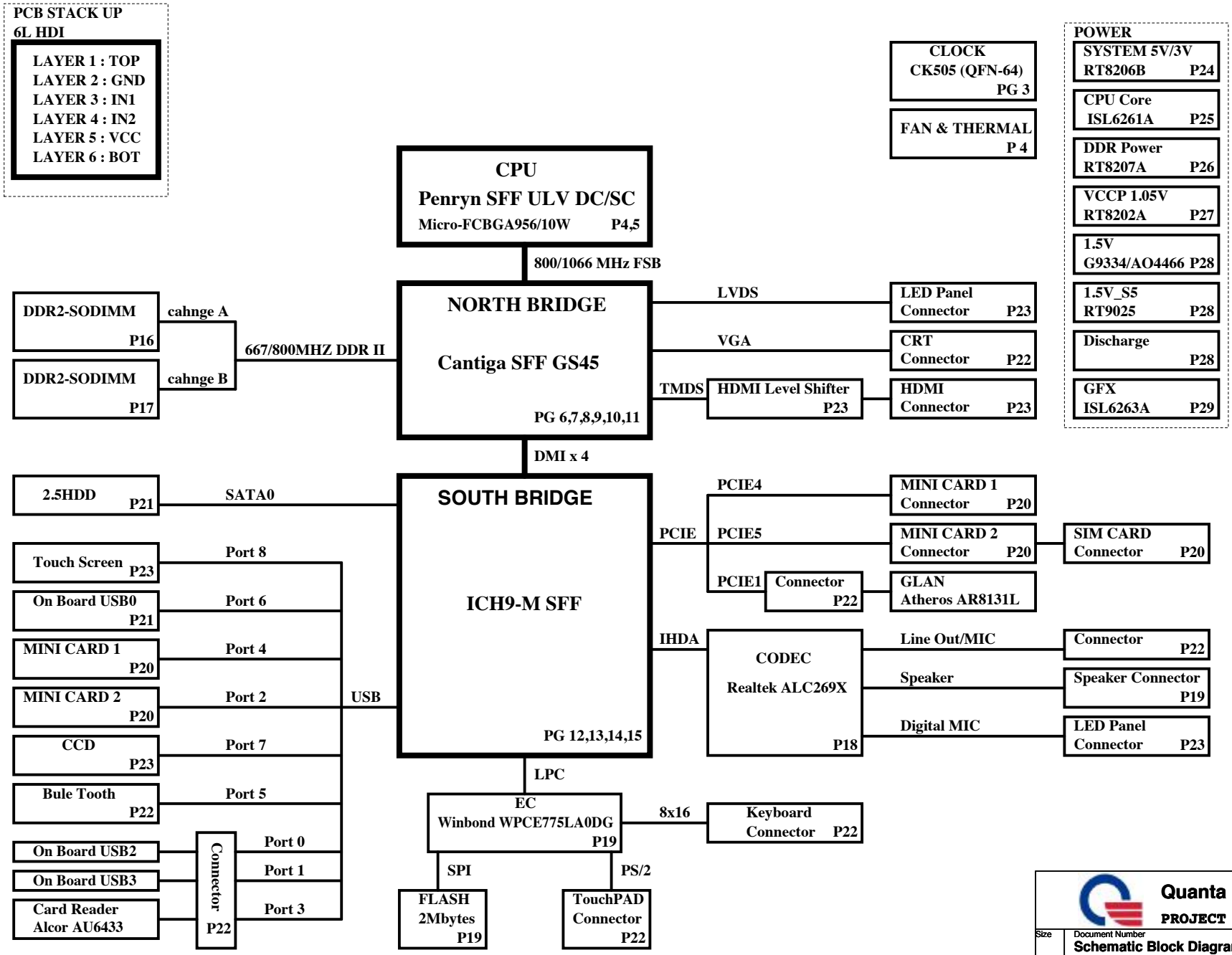
ZE8 BLOCK DIAGRAM



Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	Schematic Block Diagram	1A

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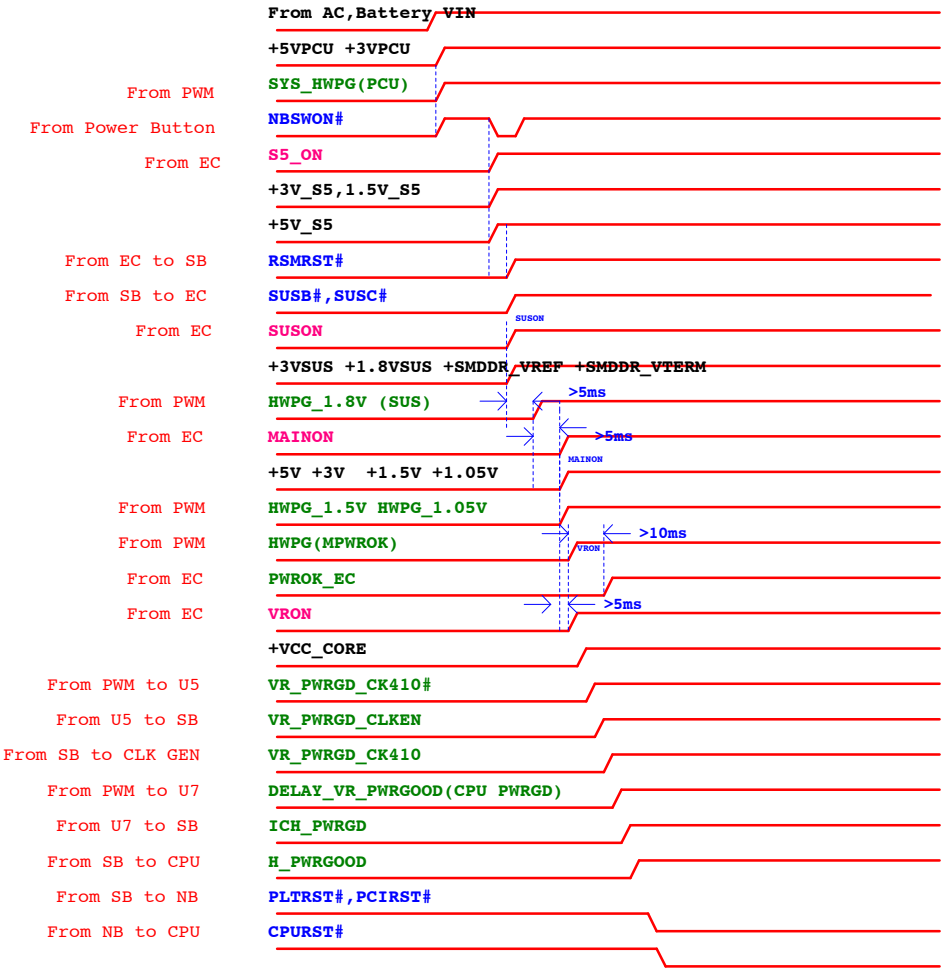
ZE8 Power On Sequence



BOM naming rule

Items	Function	Name	Description
1	With HDMI	HD@	
2	Without HDMI	NHD@	
3	3G Module	3G@	
4			
5			
6			

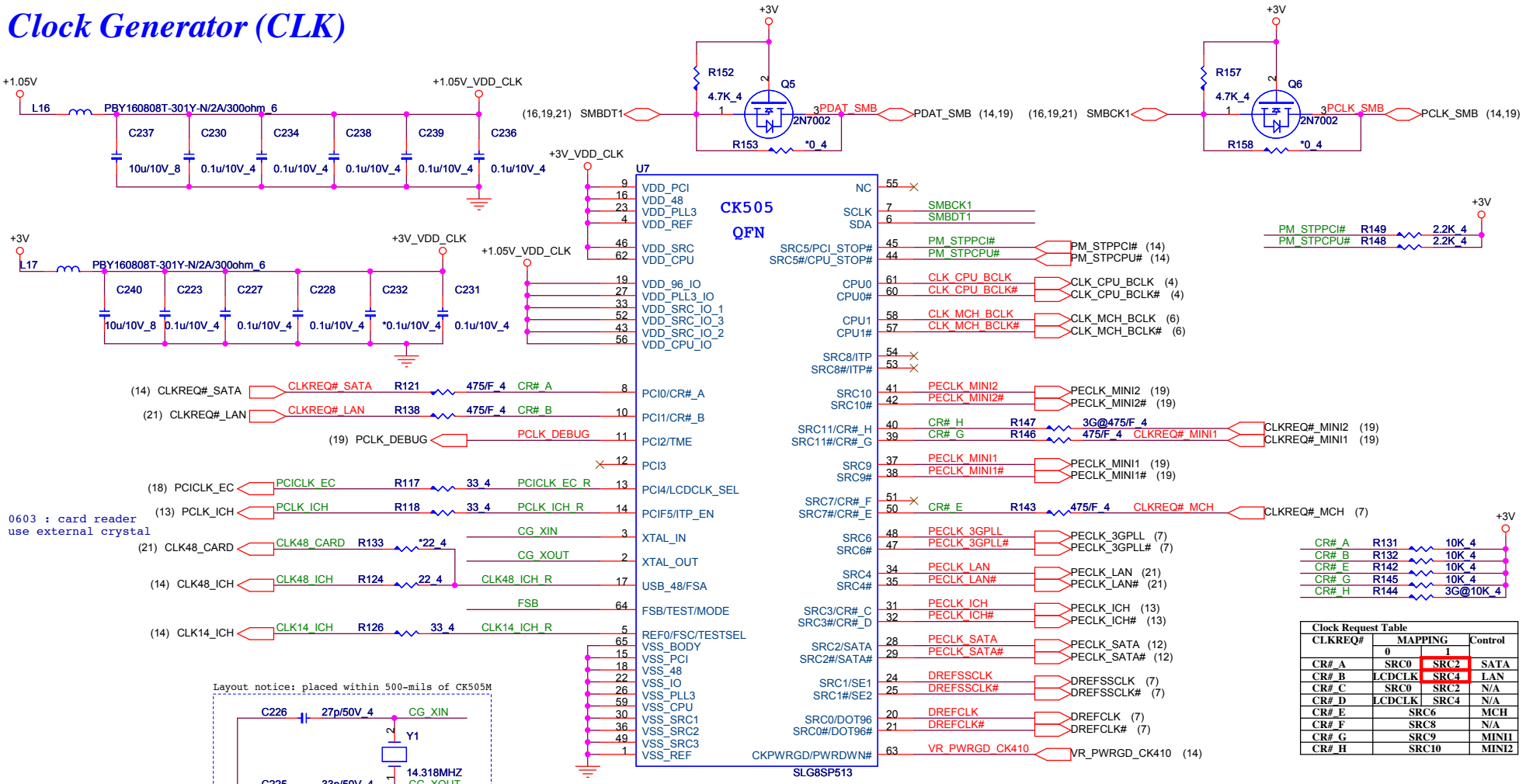
ICH9M SFF SMBUS Table

	CLK GEN	RAM	Mini Card (WLAN/WMAX)	Mini Card (3G)	G sensor
(SMB_DATA) / (SMB_CLK) (+3V_S5)	V	V	V	V	V
Power Plane	+3V	+3V	+3V	+3VSUS	+3V
MOS CKT	Stuff	Stuff	Stuff	Stuff	Stuff

EC SMBUS Table

	Battery	CPU thermal Sensor	EC EEPROM
EC775 SDATA1/SCLK1(+3VPCU)	V		
EC775 SDATA2/SCLK2(+3V)		V	
EC775 SDATA3/SCLK3(+3VPCU)			V
Power Plane	+3VPCU	+3V	+3VPCU
MOS CKT	X	X	X

Clock Generator (CLK)



Clock Request Table			
CLKREQ#	MAPPING 0	MAPPING 1	Control
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MCH
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MINI2

	SLG8SP513VTR (AL8SP513000)	ICS9LPRS365 (ALPRS365000)	PULL HIGH	PULL DOWN
Pin 11	PCI2/TME	PCI2/TME	NO OVERCLOCKING (default)	NORMAL RUN
Pin 13	PCI4/ 27_Select	PCI_4/ SEL_LCDCLK#	PIN 24/25 IS 27MHz	PIN 24/25 IS SRC/DOT (default)
Pin 14	PCIF-5/ITP_EN	PCIF-5/ITP_EN	PIN 53/54 IS CPUITP	PIN 53/54 IS SRC8 (default)

<MAIN> : SLG8SP513VTR(AL8SP513000)
<SECOND> : ICS9LPRS365BKLFT(ALPRS365000)

FSC	FSB	FSA	CPU (MHz)	SRC (MHz)	PCI (MHz)	REF (MHz)	DOT96 (MHz)	USB (MHz)
0	0	0	266.6	100.0	33.3	14.318	96.0	48.0
0	0	1	133.3	100.0	33.3	14.318	96.0	48.0
0	1	0	200.0	100.0	33.3	14.318	96.0	48.0
0	1	1	166.6	100.0	33.3	14.318	96.0	48.0
1	0	0	333.3	100.0	33.3	14.318	96.0	48.0
1	0	1	100.0	100.0	33.3	14.318	96.0	48.0
1	1	0	400.0	100.0	33.3	14.318	96.0	48.0
1	1	1	Reserved					

ITP_EN	Pin 53/54
0	SRC_8/SRC_8#
1	ITP/ITP#

LCDCLK_SEL	Pin 20/21	Pin 24/25
0	DOT_96/DOT96#	LCDCLK/LCDCLK#
1	SRC_0/SRC_0#	27M/27M_SS

Quanta Computer Inc.
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Size	Document Number	Rev
	CLOCK GENERATOR CK505	1A
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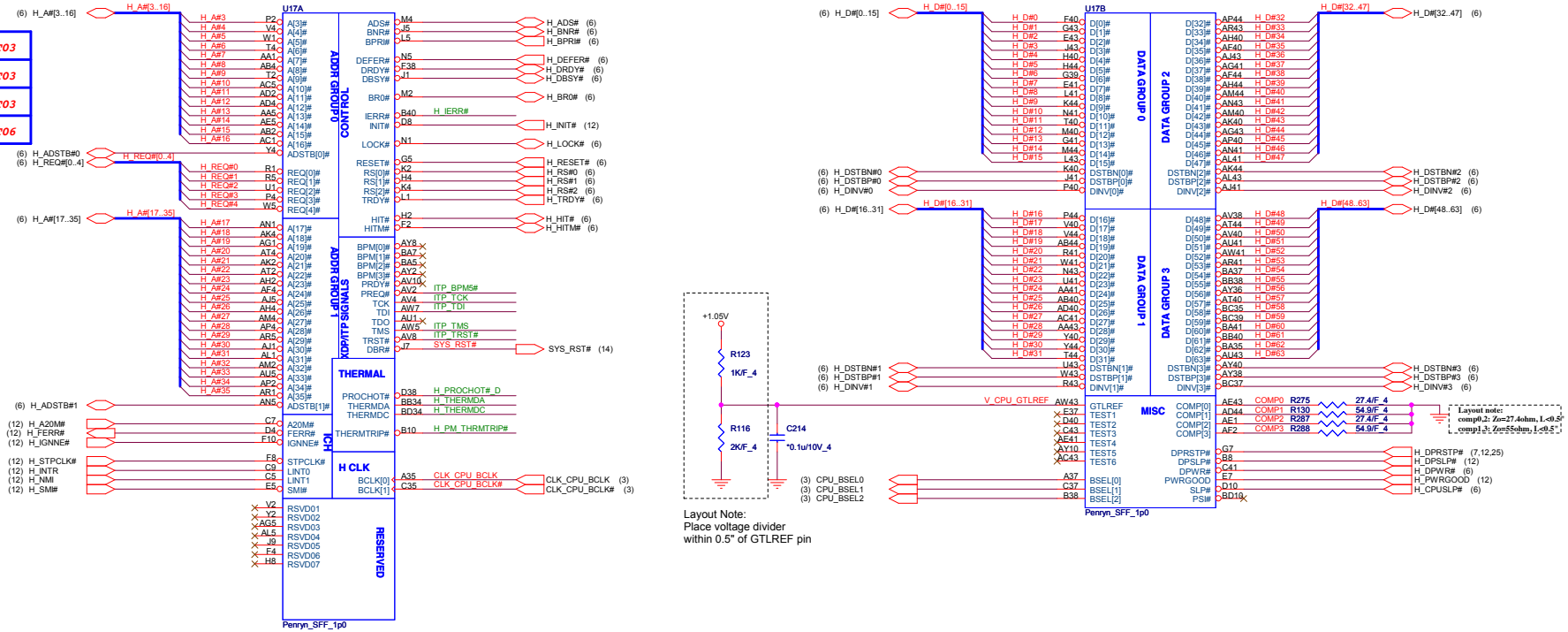
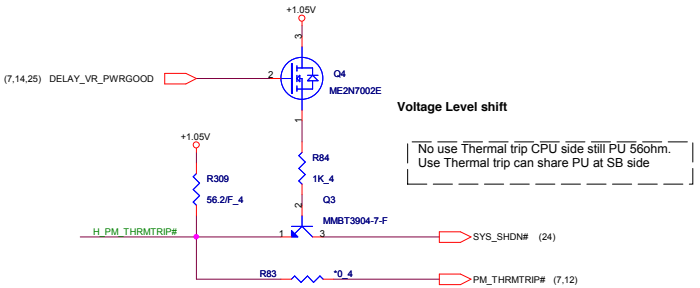
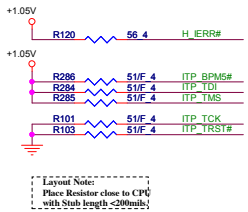
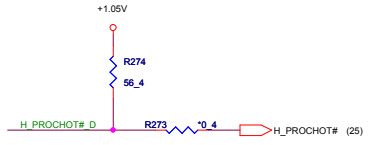
Penryn SFF - Host Bus (CPU)

Celeron 743	AJSLGEVVT03
SU2300	AJSLGYWVT03
SU4100	AJSLGS4VT03
SU7300	AJSLGYVVT06

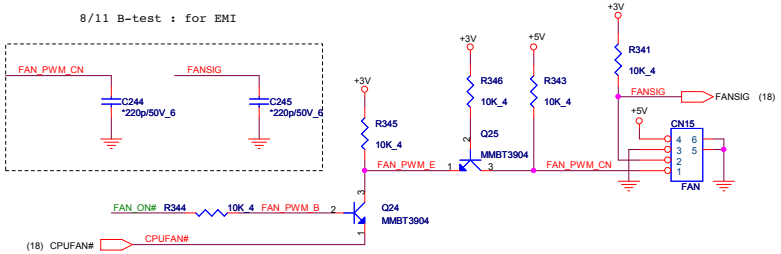




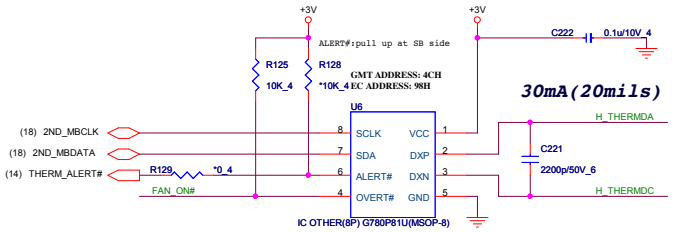




CPU FAN CTRL(THM)



CPU Thermal Monitor(THM)



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Size	Document Number	Rev
	Penryn SFF (Host Bus)/FAN/Thermal	1A

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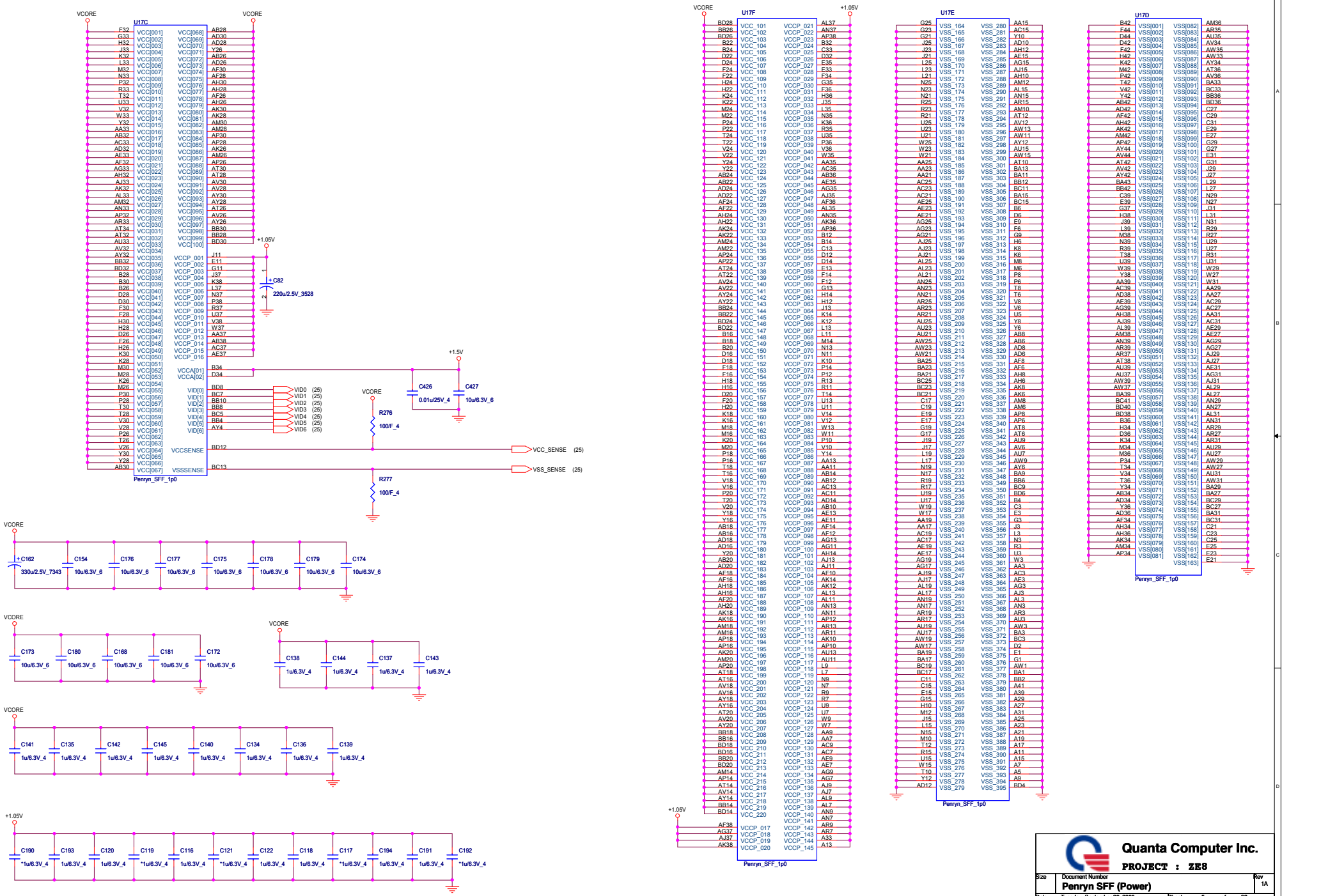
Penryn SFF - Power (CPU)



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PROJECT : ZE8

Size	Document Number	Rev
	Penryn SFF (Power)	1A

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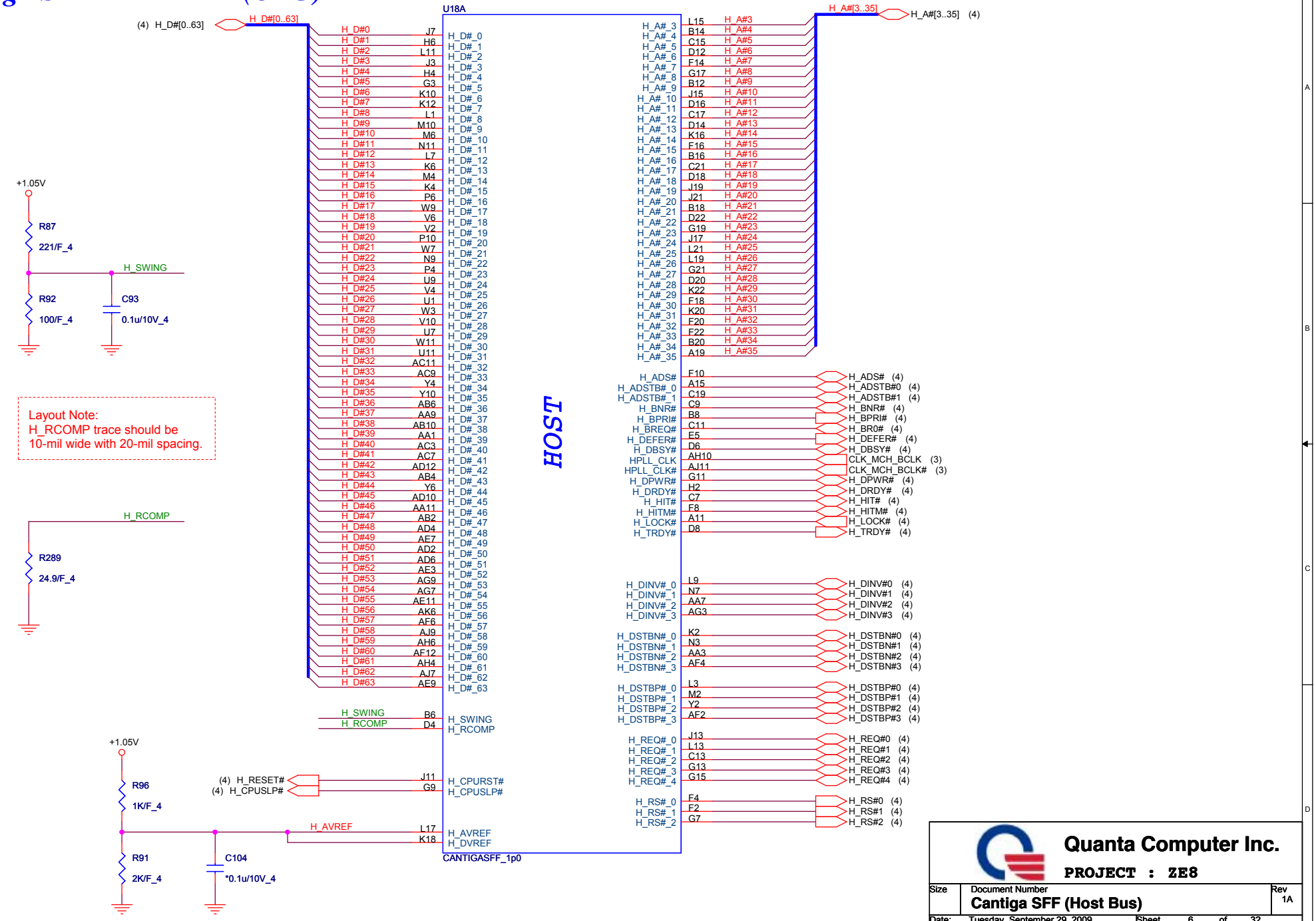
Cantiga SFF - Host Bus (CLG)



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PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (Host Bus)	1A

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Cantiga SFF - DMI/VGA (CLG)

Intel GS40/GS45 Strapping Signals and Configuration		
Pin Name	Strap Description	Configuration
CFG2:0	FSB Frequency	000 = FSB1066 010 = FSB800 011 = FSB667 Other = Reserved
CFG4:3	Reserved	
CFG5	DMI x2 Select	1 = DMI x 4 0 = DMI x2
CFG6	ITPM Host Interface	1 = ITPM disabled 0 = ITPM enabled
CFG7	Intel Management Engine Crypto Strap	1 = Intel Management Engine Crypto TLS cipher suite with confidentiality 0 = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
CFG8	Reserved	
CFG9	PCIE Graphics Lane	1 = Normal operation : Lane Numbered in Order 0 = Reverse Lanes
CFG10	PCIE Loopback enable	1 = Disabled 0 = Enabled
CFG11	Reserved	
CFG12	ALLZ	1 = Disabled 0 = ALLZ mode enabled
CFG13	XOR	1 = Disabled 0 = XOR mode enabled
CFG14	Reserved	
CFG15	Reserved	
CFG16	FSB Dynamic ODT	1 = Dynamic ODT enabled 0 = Dynamic ODT disabled
CFG17	Reserved	
CFG18	Reserved	
CFG19	DMI Lane Reversal	1 = Reverse Lanes 0 = Normal operation : Lane Numbered in Order
CFG20	Digital DisplayPort (SDVO/DP/iHDMI) Concurrent with PCIE	1 = Digital DisplayPort (SDVO/DP/iHDMI) and PCIE are operating simultaneously via the PEG port 0 = Digital DisplayPort (SDVO/DP/iHDMI) or PCIE are operational
SDVO_CTRLDATA	SDVO Present	1 = SDVO/IHDMI/DP interface enabled 0 = No SDVO/IHDMI/DP interface disabled
L_DDC_DATA	Local Flat Panel (LFP) Present	1 = LFP Card Present; PCIE disabled 0 = LFP Disable
DDPC_CTRLDATA	Digital Display Present	1 = Digital display (iHDMI/DP) device present 0 = Digital display (iHDMI/DP) interface absent

- The recommended pull-up resistor value is 4.02 k Ω ±1%
- The recommended pull-down resistor value is 2.21 k Ω ±1%.

U18B

RSVD / CONTROL/COMPENSATION

DDR CLK / CONTROL / COMPENSATION

CLK

DMI

CFG

VID

GRAPHICS

PM

ME

NC

MISC

HDA

CANTIGASFF_1p0

SM_VREF=0.5*VCC_SM

SM_PWROK only for DDR3.(DDR2 PD only)

SM_DRAMRST# only for DDR3.(DDR2:NC)

U18C

PCI-EXPRESS GRAPHICS

DMI

VGA

CANTIGASFF_1p0

Layout notice: Place the resistor within 500 mils (1.27 mm) of the (G)MCH.

HDMI Port B

DDR3 PWROK

At 11/19 change U21 power supply from +3VSUS to +3V_S5

U21 TC7SH08FU

DDR3 VREF

(20mils)

(15mils)

+SMDDR_VREF_NB.Default use voltage divider for poor layout cause +SMDDR_VREF not meet spec.And Intel circuit PU/PD is 1K,But Check list PU/PD is 10K.

<Checklist ver0.8>
If TSATN# is not used, then it must be terminated with a 56-Ω pull-up resistor to VCCP.

DDR3 RCOMP

DDR3 RCOMP_VOH/VOL

CRT setting

R84:
~~if the total motherboard route length is less than 12",~~
the recommended reference resistor value is 1 K Ω ±1%
For longer route lengths between 12" - 15.3",
the recommended reference resistor value is 976 Ω ±1%

LVDS setting

(7/7) intel check list 360543 rev 2.0 CLKREQ# need to 10K pull high to 3.3V

Quanta Computer Inc.
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Size	Document Number	Rev
	Cantiga SFF (DMI/VGA)	1A
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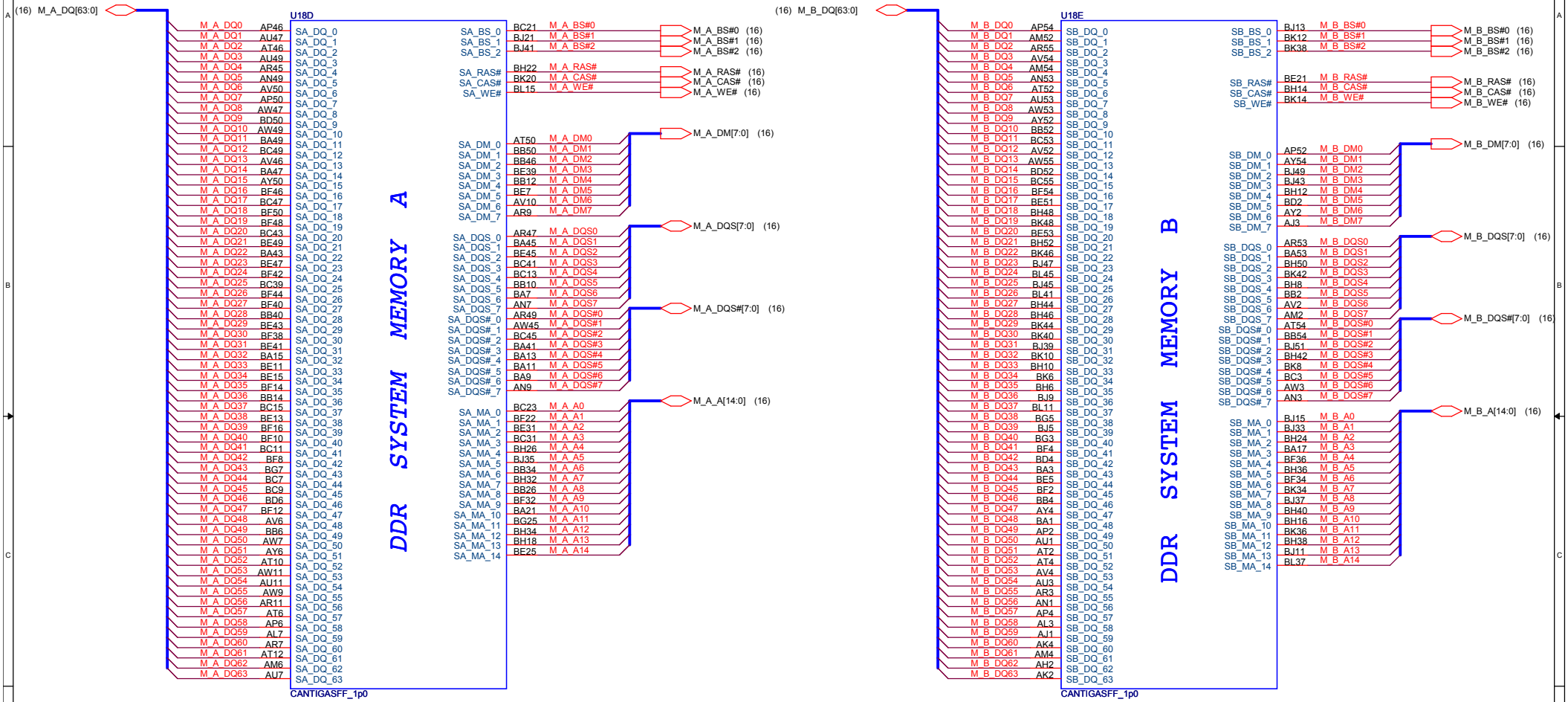
Cantiga SFF - DDRII (CLG)



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PROJECT : ZE8

Size	Document Number	Rev
	Cantiga SFF (DDRII)	1A
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Cantiga SFF - VCC/NCTF (CLG)

Ivcc internal VGA 2.4A
(Shape or 140mils)

VCC_SM(+1.5V_SUS)
DDR3(800M) : 3162.5mA
DDR3(1067M) : 4140mA

UMA 9.6A(GM45)
(Plane or shape)

VCC 2200mA

U18F

VCC CORE

POWER

VCC NCTF

CANTIGASFF_1p0

VCC_SM :3000mA

U18G

VCC SM

POWER

VCC GFX NCTF

VCC GFX

VCC_AXG 7700mA

VCC SM LF

CANTIGASFF_1p0

Differential routing

(29) GFX_VCCSENSE
(29) GFX_VSSSENSE

R108 10/F_4
R107 10/F_4

1. Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially
2. VCC_AXG_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AXG_SENSE PD with 10ohm for Intel suggest

R64 *0_8
R65 *0_8
R183 *0_8

Celeron 723,743 not support graphics render standby mode,
so add R64 , R65, del GFX power (Page 29)
SU type cpu support it, so del R64, R65 and add GFX power (Page 29)

9/28: add R183 for voltage low issue

C203 0.1u/10V_4
C182 0.22u/10V_4
C201 0.22u/10V_4
C156 *10u/6.3V_8
C83 *220u/2.5V_3528

Layout Note:
Inside GMCH cavity.

C200 0.1u/10V_4
C215 10u/6.3V_8
C211 10u/6.3V_8
C212 *10u/6.3V_8

C133 0.47u/6.3V_4
C127 *1u/16V_6
C128 10u/6.3V_6
C115 10u/6.3V_8
C124 0.1u/10V_4
C132 0.1u/10V_4

C108 *220u/2.5V_3528
C107 220u/2.5V_3528

Close to GMCH

Layout Note:
370 mils from edge.

6/13 : add for EMI

C246 *220p/50V_6
C247 *220p/50V_6

10mil

C163 0.1u/10V_4
C205 0.1u/10V_4
C204 0.22u/10V_4
C207 0.22u/10V_4
C218 0.47u/6.3V_4
C210 1u/10V_6
C197 1u/10V_6

C217 0.1u/10V_4
C216 0.1u/10V_4
C213 0.1u/10V_4
C209 0.1u/10V_4
C424 0.1u/10V_4
C206 0.1u/10V_4

Quanta Computer Inc.
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Size	Document Number	Rev
	Cantiga SFF (VCC/NCTF)	1A
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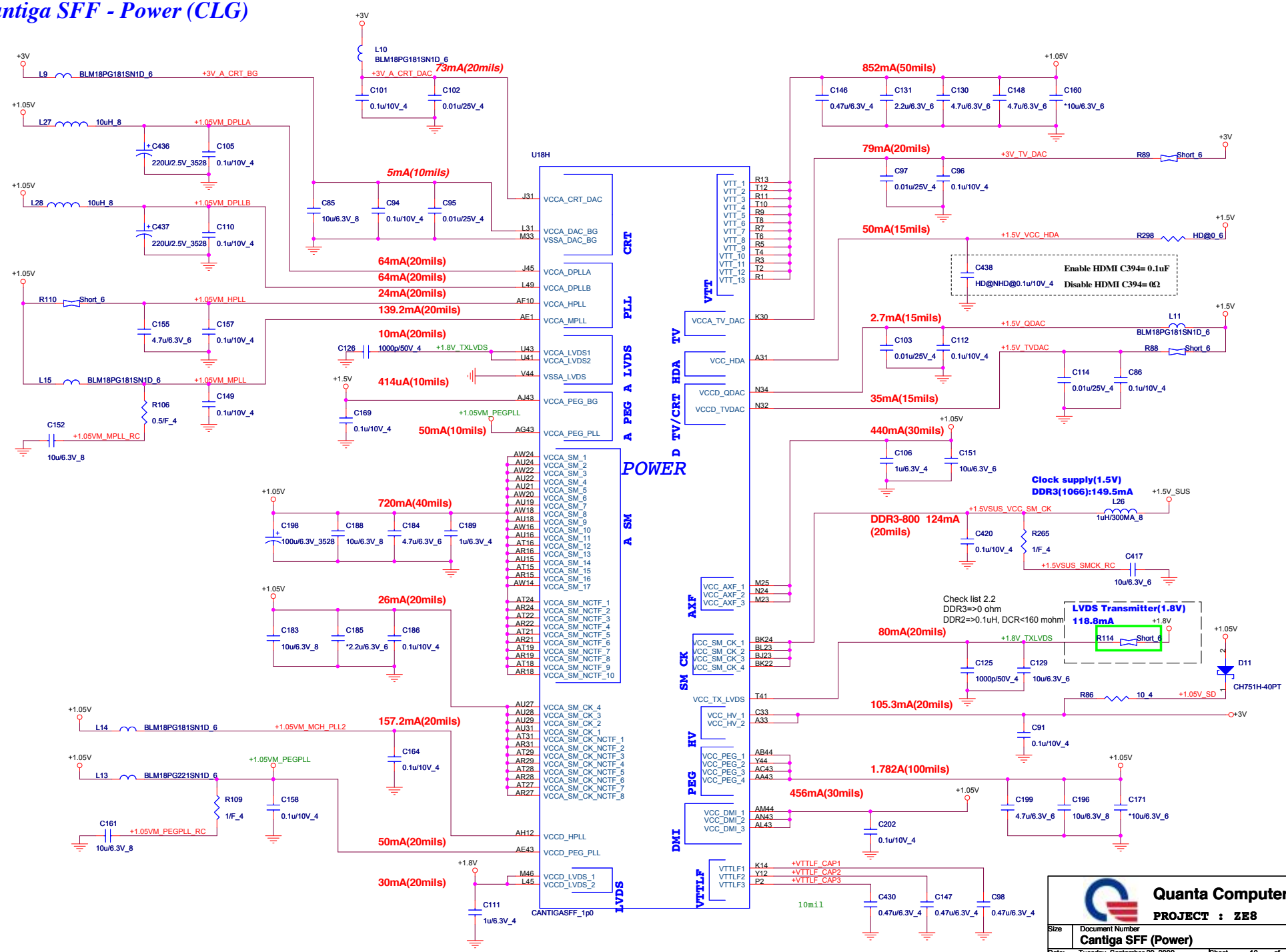
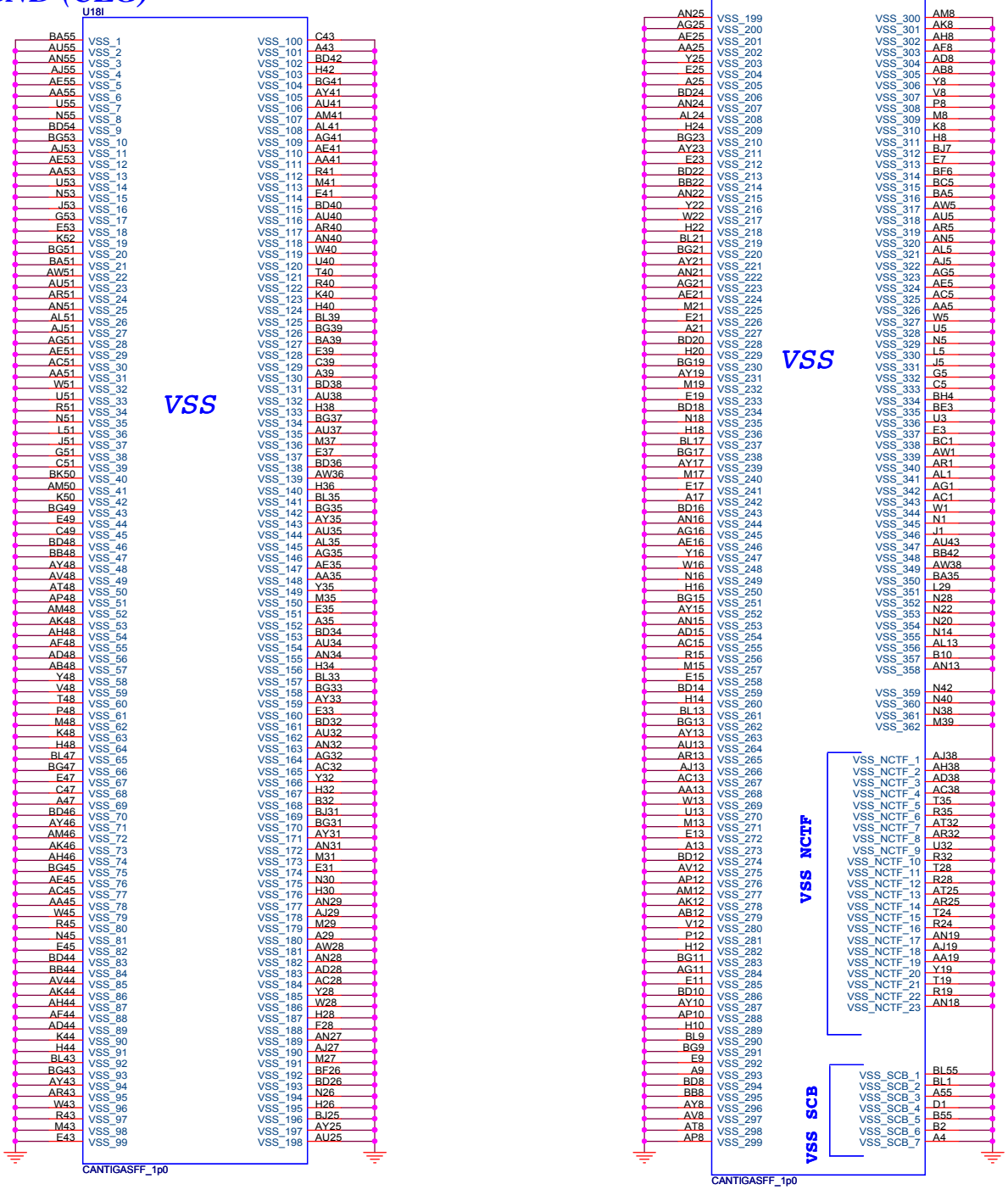
Cantiga SFF - Power (CLG)



Cantiga SFF - GND (CLG)



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Size	Document Number	Rev
	Cantiga SFF (GND)	1A
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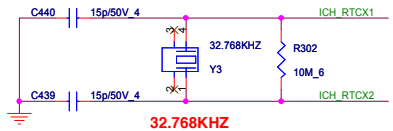
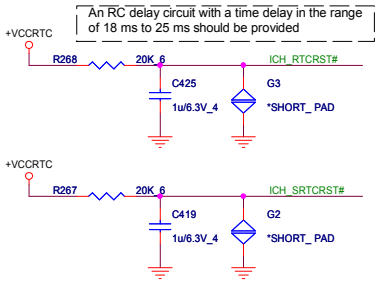
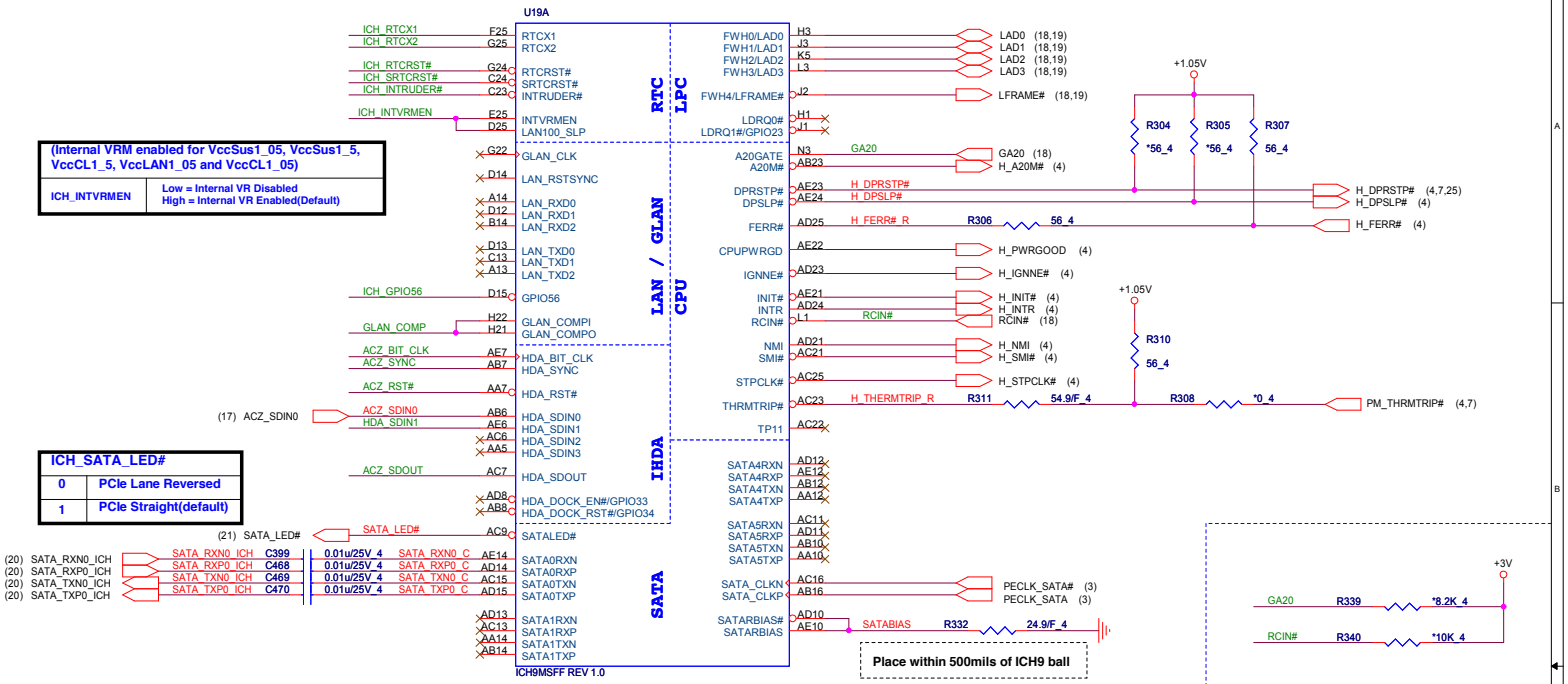
RTC CRYSTAL



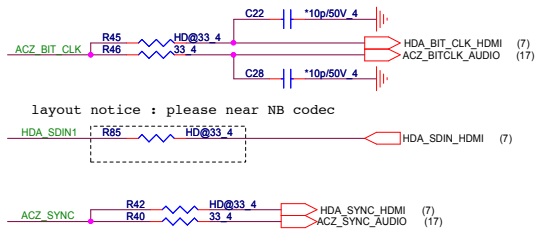
RESET JUMP

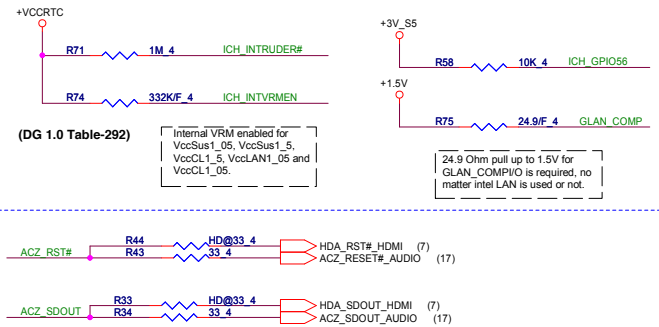


ICH9M SFF - Host,SATA,HDA (CLG)

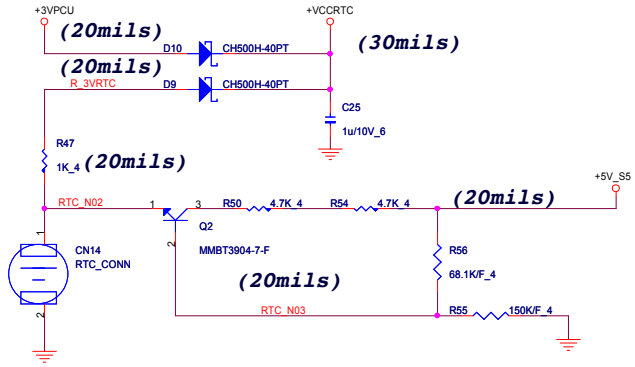


HD Audio Interface





RTC BATTERY (RTC)



South Bridge Strap Pin (1/3)				
Pin Name	**Strap description**	**Sampled**	**Configuration**	**PU/PD**
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU	
	XOR Chain Entrance	PWROK	ICH_TP3 = 0, HDA_SDOUT = 0: RSVD ICH_TP3 = 0, HDA_SDOUT = 1: Enter XOR Chain ICH_TP3 = 1, HDA_SDOUT = 0: Normal opration(Default) ICH_TP3 = 1, HDA_SDOUT = 1: Set PCIE port config bit 1	(14) ICH_TP3 — ICH_TP3 — R316 — *1K_4
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK		HDA_IO_ICH — R37 *1K_4 ACZ_SDOUT; R36 *1K_4 ACZ_SYNC intel design guide: pull high 3.3k

Quanta Computer Inc.
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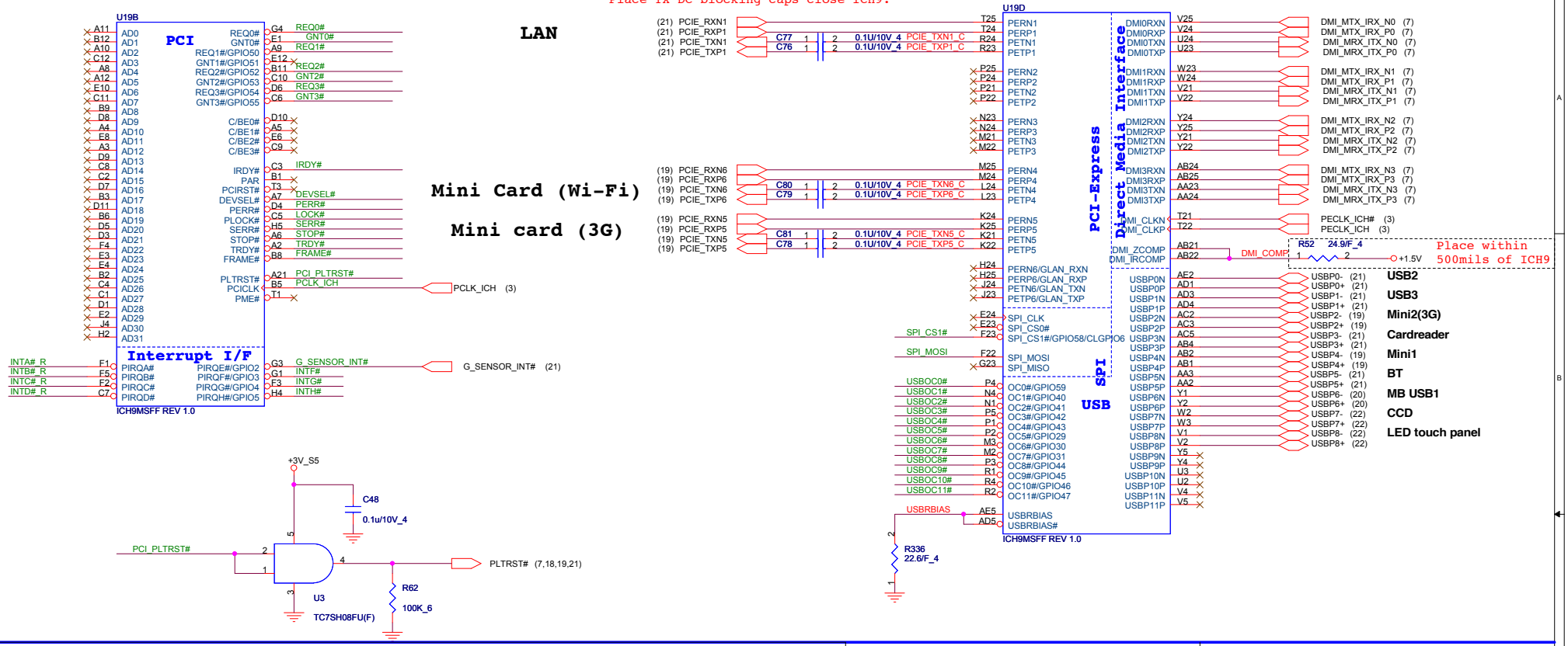
Size | Document Number: ICH9M SFF (Host/SATA/HDA) | Rev: 1A
Date: Tuesday, September 29, 2009 | Sheet 12 of 32

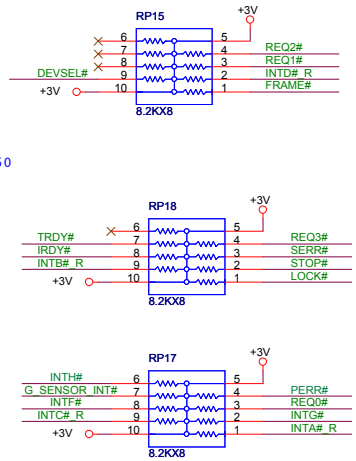
ICH9M SFF - USB/PCIE/DMI (CLG)



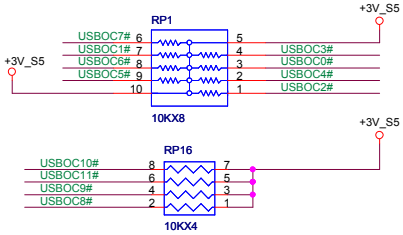
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0	
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default	GNT2# — T20
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default	8/28 : add pull high resister R160 in GNT3# pin for no video issue.
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	T3 — GNT3# — R160 10K_4 — +3V
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI — T18
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0 / SPI_CS#1 / Boot Location 0 / 1 / SPI(Default) 1 / 0 / PCI	GNT0# — T21
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK		SPI_CS1# — T19

PCI PULL-UP



USBOC# PULL-UP



Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	ICH9M SFF (USB/PCIE/DMI)	1A

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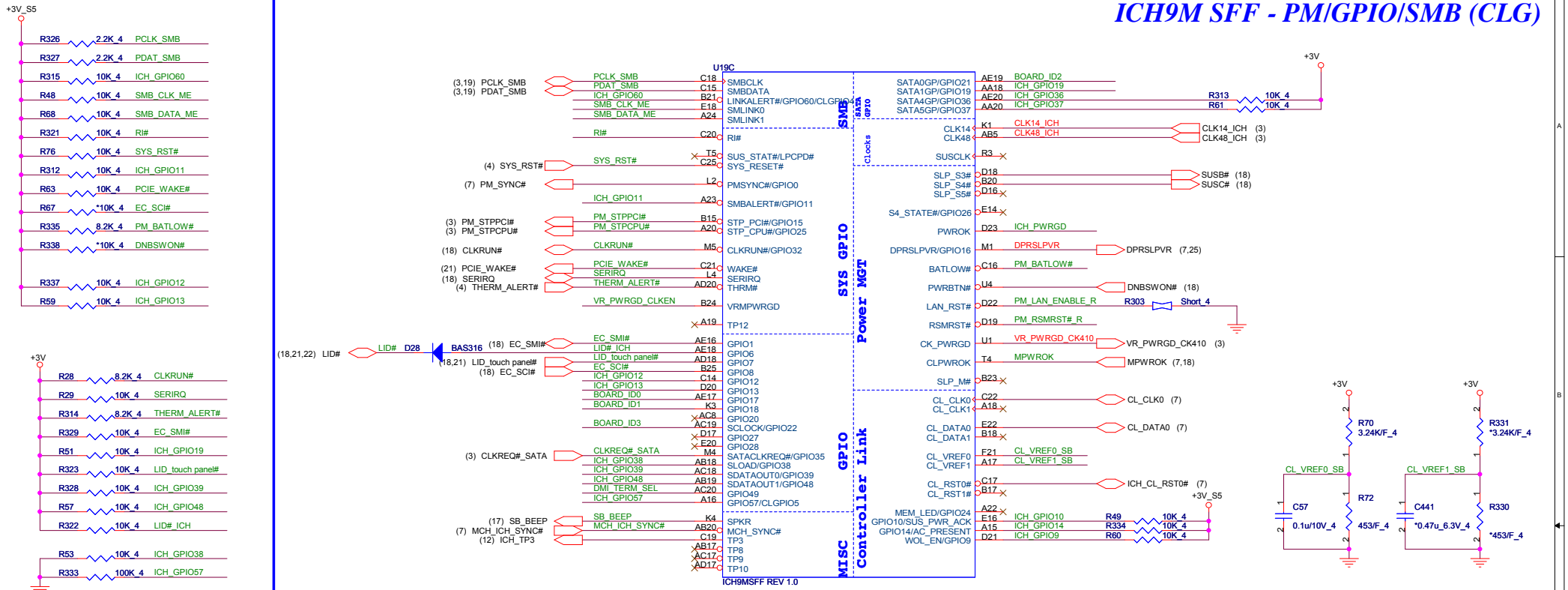
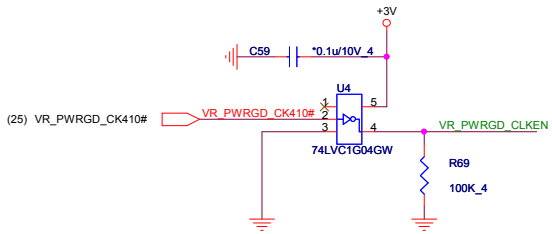
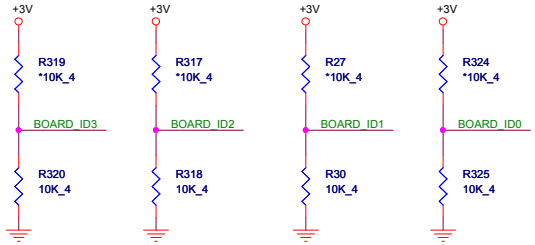
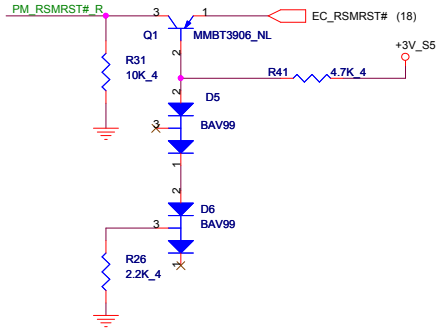
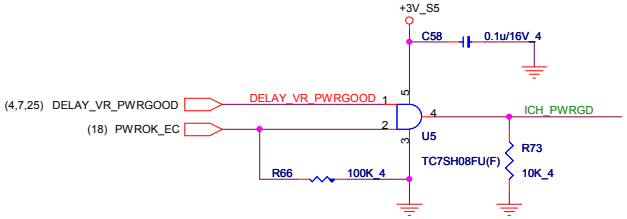
ICH9M SFF - PM/GPIO/SMB (CLG)









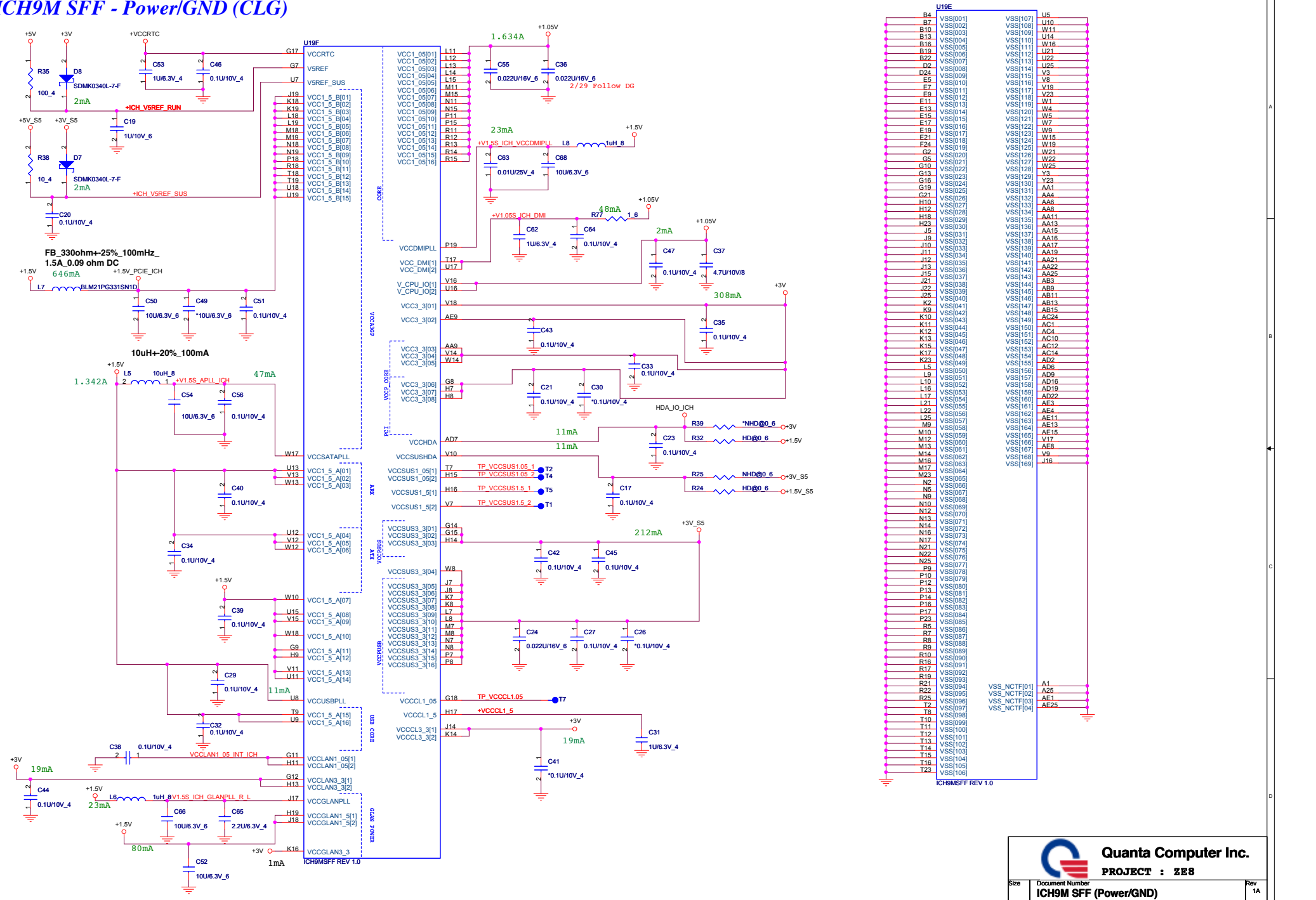


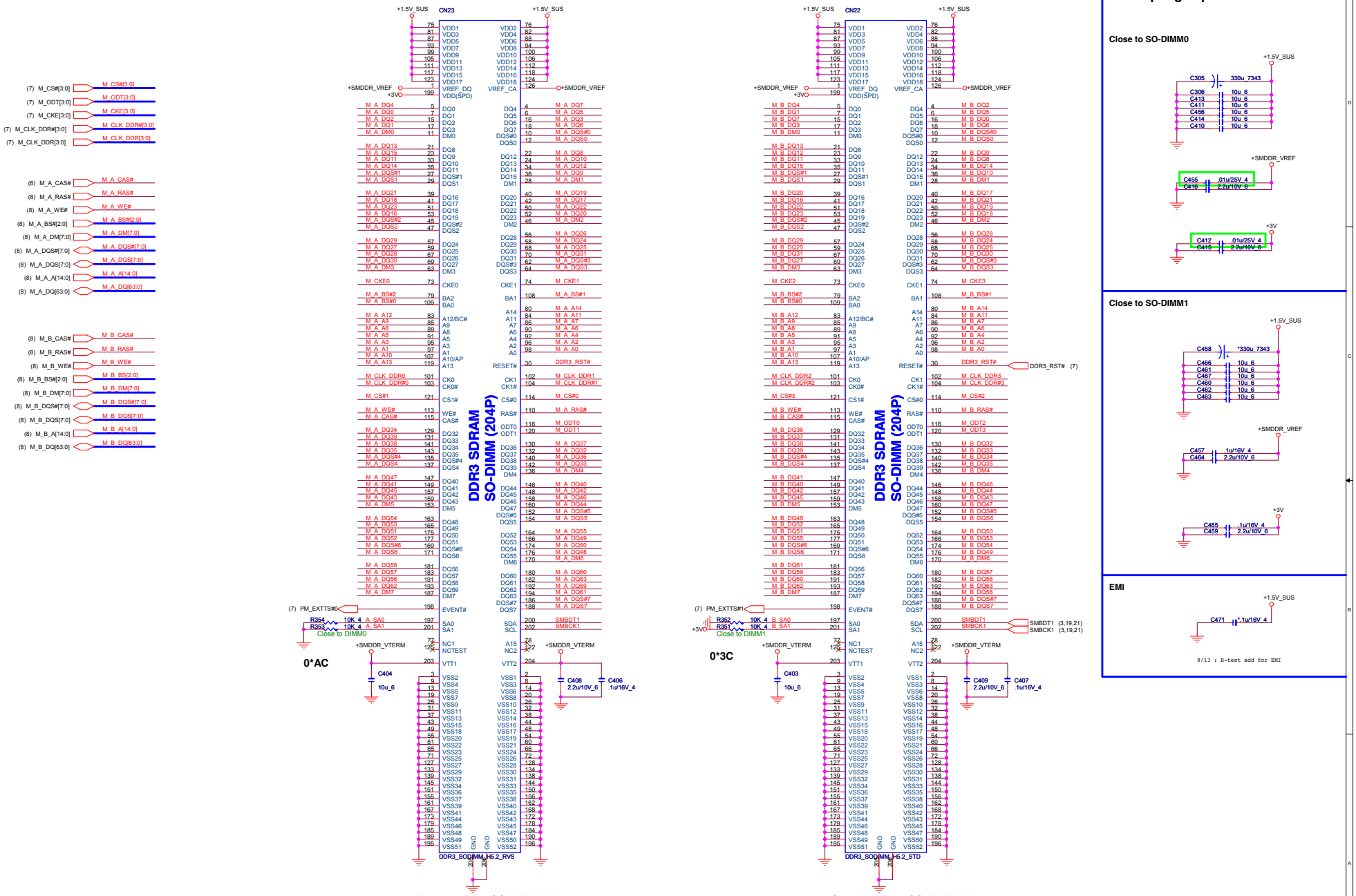
South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
PCBEEP	No Reboot	PWROK	0 = Default 1 = No Reboot mode	
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL — T6

Quanta Computer Inc.	PROJECT : ZE8		
Size	Document Number: ICH9M SFF (PM/GPIO/SMB)		Rev 1A
Date: Tuesday, September 29, 2009	Sheet 14 of 32		

ICH9M SFF - Power/GND (CLG)




(7) M_CS#[3:0]
M_CS#[3:0]
(7) M_ODT[3:0]
M_ODT[3:0]
(7) M_CKE[3:0]
M_CKE[3:0]
(7) M_CLK_DDR#[3:0]
M_CLK_DDR#[3:0]
(7) M_CLK_DDR[3:0]
M_CLK_DDR[3:0]
(8) M_A_CAS#
M_A_CAS#
(8) M_A_RAS#
M_A_RAS#
(8) M_A_WE#
M_A_WE#
(8) M_A_BS#[2:0]
M_A_BS#[2:0]
(8) M_A_DM[7:0]
M_A_DM[7:0]
(8) M_A_DQS#[7:0]
M_A_DQS#[7:0]
(8) M_A_DQS[7:0]
M_A_DQS[7:0]
(8) M_A_A[14:0]
M_A_A[14:0]
(8) M_A_DQ[63:0]
M_A_DQ[63:0]
(8) M_B_CAS#
M_B_CAS#
(8) M_B_RAS#
M_B_RAS#
(8) M_B_WE#
M_B_WE#
(8) M_B_BS#[2:0]
M_B_BS#[2:0]
(8) M_B_DM[7:0]
M_B_DM[7:0]
(8) M_B_DQS#[7:0]
M_B_DQS#[7:0]
(8) M_B_DQS[7:0]
M_B_DQS[7:0]
(8) M_B_A[14:0]
M_B_A[14:0]
(8) M_B_DQ[63:0]
M_B_DQ[63:0]
CN23
DDR3 SDRAM SO-DIMM (204P)
DDR3_SODIMM_H5.2_RVS
+1.5V_SUS
+SMDDR_VREF
+3V
+SMDDR_VTERM
(7) PM_EXTTS#0
R354 10K_4 A_SA0
R353 10K_4 A_SA1
Close to DIMM0
0*AC
C404 10u_6
C408 2.2u/10V_6
C406 .1u/16V_4
Reverse Type SO-DIMM0 ,H=5.2mm
SMbus address A0
CN22
DDR3_SODIMM_H5.2_STD
(7) PM_EXTTS#1
R352 10K_4 B_SA0
R351 10K_4 B_SA1
Close to DIMM1
0*3C
C403 10u_6
C409 2.2u/10V_6
C407 .1u/16V_4
Standard Type SO-DIMM1,H=5.2
SMbus address A2
Decoupling capacitor
Close to SO-DIMM0
C305 330u_7343
C306 10u_6
C413 10u_6
C411 10u_6
C456 10u_6
C414 10u_6
C410 10u_6
C455 .01u/25V_4
C416 2.2u/10V_6
C412 .01u/25V_4
C415 2.2u/10V_6
Close to SO-DIMM1
C458 *330u_7343
C466 10u_6
C461 10u_6
C467 10u_6
C460 10u_6
C462 10u_6
C463 10u_6
C457 .1u/16V_4
C464 2.2u/10V_6
C465 .1u/16V_4
C459 2.2u/10V_6
EMI
C471 *.1u/16V_4
8/13 : B-test add for EMI
Quanta Computer Inc.
PROJECT : ZE8
Size
Document Number
DDRIII SO-DIMM
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1A
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Codec ALC269X (ADO)

B-test 8/11: for EMI

SPDIF_OUT — C243 *680p/50V_6; +5VA — C363 0.1U/10V_4

HPOUT-R → HPOUT-R (21)
HPOUT-L → HPOUT-L (21)
MIC1-VREFO-R
MIC1-VREFO-L
Place next to pin 27

ADOGND
C358 2.2U/6.3V_6
C352 2.2U/6.3V_6
C359 *10U/6.3V/6
C353 0.1U/10V/4
C348 0.1U/10V_4
C347 *10U/6.3V_6
Place next to pin 25

U11 (ALC269)

36	CBP	37	AVSS2
35	CBN	38	AVDD2
34	CPVEE	39	PVDD1
33	HP-OUT-R	40	SPK-L+
32	HP-OUT-L	41	SPK-L-
31	CPVREF	42	PVSS1
30	MIC1-VREFO-R	43	PVSS2
29	MIC2VREFO	44	SPK-R-
28	MIC1-VREFO-L	45	SPK-R+
27	VREF	46	PVDD2
26	AVSS1	47	SPDIFO2/EAPD
25	AVDD1	48	SPDIFO
58	GND	49	PGND
57	GND	50	GND
56	GND	51	GND
55	GND	52	GND
54	GND	1	DVDD1
53	GND	2	GPIO0/DMIC-DATA
24	LINE1-R	3	GPIO1/DMIC-CLK
23	LINE1-L	4	PD#
22	MIC1-R	5	SDATA-OUT
21	MIC1-L	6	BIT-CLK
20	MONO-OUT	7	DVSS2
19	JDREF	8	SDATA-IN
18	Sense-B	9	DVDD-IO
17	MIC2-R	10	SYNC
16	MIC2-L	11	RESET#
15	LINE2-R	12	PCBEEP
14	LINE2-L		
13	Sense A		

Spilt by DGND

+5VA — C350 10U/6.3V_6 — C349 0.1U/10V_4 — ADOGND
Place next to pin 38

+5V — L_SPK+ — L_SPK- — R_SPK- — R_SPK+ — +5V

(Vista Premium Version)

MIC1_R1 — MIC1_L1

R226 20K/F_4 → ADOGND

SENSEA — R209 39.2K/F/4 → LINEOUT_JD# (21)
R221 20K/F/4 → MIC1_JD# (21)

Placement near Audio Codec

(21) SPDIF_OUT → SPDIF_OUT

ALC269

DIGITAL
1.6Vrms

ANALOG

+5V — C342 0.1U/10V_4 — C334 10U/6.3V_6
Place next to pin 39

+3V — C325 0.1U/10V_4 — C327 10U/6.3V_6
Place next to pin 1

+5V — C332 0.1U/10V_4 — C335 *10U/6.3V_6
Place next to pin 46

(22) DMIC_DAT
(22) DMIC_CLK

PD#
0V : Power down Class D SPK amplifer
3.3V : Power up Class D SPK amplifer

PCBEEP — C324 1u/10V_6 — BEEP_1 — R198 47K_4 → SB_BEEP (14)
C316 100p/50V_6 — R203 2K_4

SDIN2

+AZA_VDD

BOM notice: just can stuff one in BOM
R192 *NHD@0_6 → +3V
R189 HD@0_6 → +1.5V

C315 0.1U/10V/4 — C323 10U/6.3V_6
Place next to pin 9

ACZ_RESET#_AUDIO → ACZ_RESET#_AUDIO (12)
ACZ_SYNC_AUDIO (12)
R196 22_4 — C322 10P/50V_4 → ACZ_SDIN0 (12)
ACZ_SDOUT_AUDIO (12)
R195 Short_4 → ACZ_BITCLK_AUDIO (12)
C321 *10P/50V_4

Speaker (AMP)

R_SPK+ — R242 Short_6 — R_SPK+_1
C357 *0.22U/25V/6
C365 *1u/6.3V_4
C356 *0.22U/25V/6
R_SPK- — R241 Short_6 — R_SPK-_1
L_SPK- — R240 Short_6 — L_SPK-_1
CN8 (1, 2, 35, 46) Speak CNN
C355 *0.22U/25V/6
C364 *1u/6.3V_4
C354 *0.22U/25V/6
L_SPK+ — R239 Short_6 — L_SPK+_1

MIC1-VREFO-R
MIC1-VREFO-L
R238 4.7K/F_4
R237 4.7K/F_4
MIC1_L1 — C338 4.7U/6.3V/6 — R234 1K/F_4 → MIC1_L2 (21)
MIC1_R1 — C341 4.7U/6.3V/6 — R233 1K/F_4 → MIC1_R2 (21)

stitching caps for Audio signals
+3VPCU — C345 0.1U/10V_4 — +3V
+3VPCU — C385 0.1U/10V_4 — +3V

+3V — R202 *HD@100K_4 — PD# — *NHD@BAS316 D24 ACZ_RESET#_AUDIO
*BAS316 D25 EAPD#
*BAS316 D23 AMP_MUTE# → AMP_MUTE# (18)
R199 Short_4

+3V — R188 *HD@100K_4 — Q15 *HD@2N7002E
ACZ_RESET#_AUDIO — Q14 *HD@DTC144EU

Power (ADO)

Demodulation Filter
Place close to Codec

+5V — C373 *0.1U/10V/4
L25 TI201209U220/8
U15 *MAX8863SEUK+T (IN, GND, SHDN, OUT, SET)
+5VA
R245 *29.4K/F/4
R246 *10K/F/4 → ADOGND
C366 *10U/10V/3216 → ADOGND

R259 Short_6
R248 *0_6
R250 *0_6
R243 *0_6
R254 Short_6
C377 *1000p/50V_4
C387 *1000p/50V_4
R247 *0_6
→ ADOGND

Quanta Computer Inc.
PROJECT : ZE8

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	Codec ALC269X	1A
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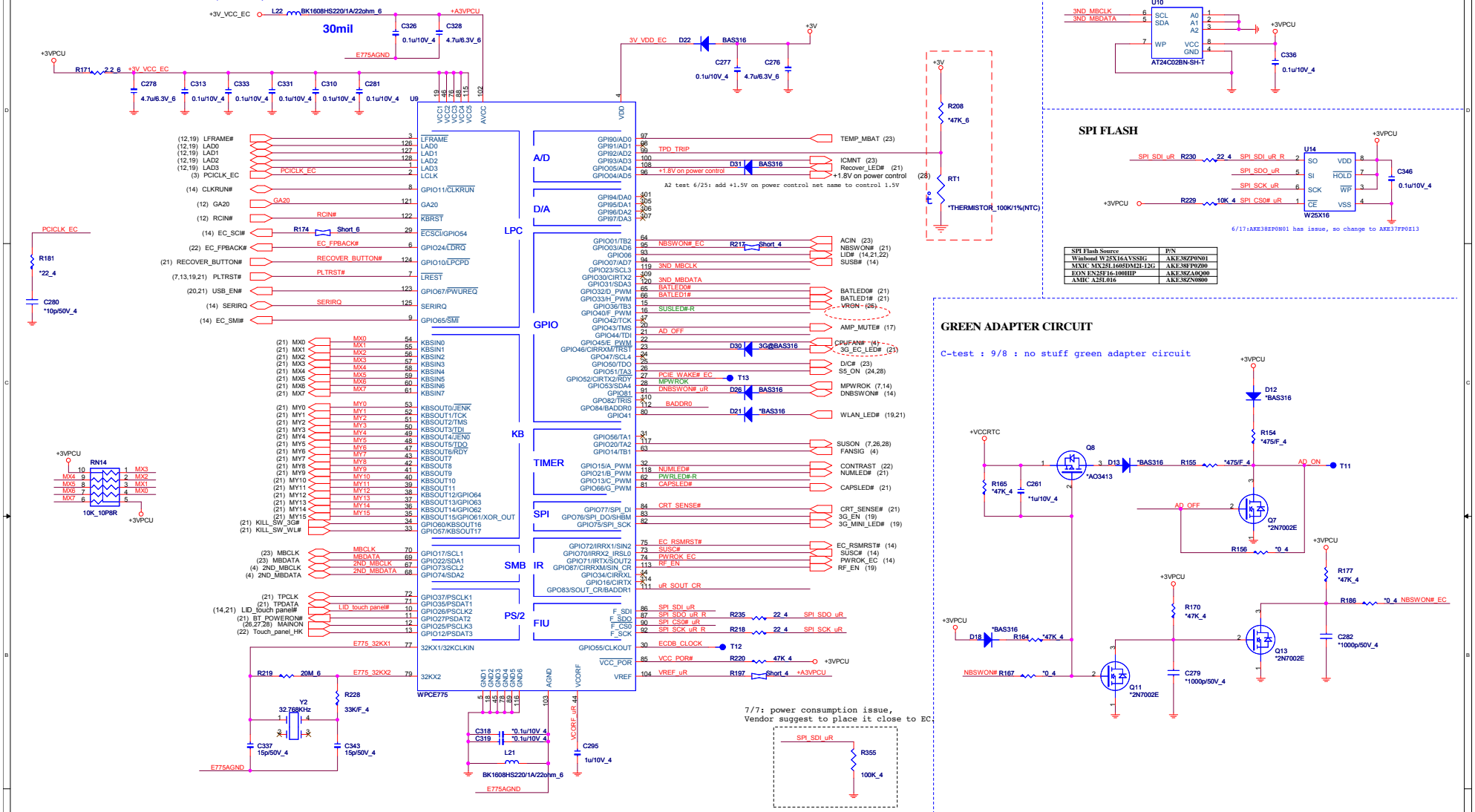
EC WPCE775LA0DG (KBC)



ACER ID

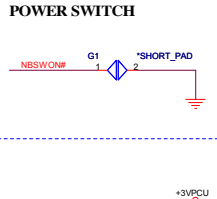
SPI FLASH

SPI Flash Source	P/N
Winbond W25X16AVSSIG	AKE38ZP0N01
MXIC MX25L1605DM2I-12G	AKE38FP0Z00
EON EN25F16-100HIP	AKE38ZA0Q00
AMIC A25L016	AKE38ZN0B00

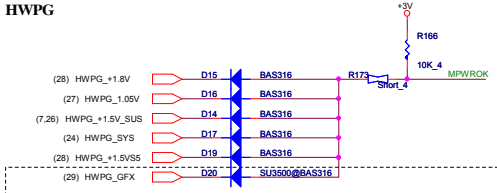
GREEN ADAPTER CIRCUIT

C-test : 9/8 : no stuff green adapter circuit

POWER SWITCH



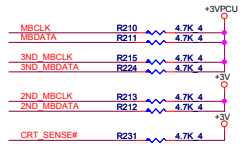
HWPG



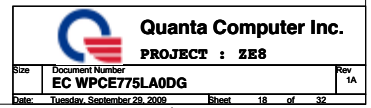
I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

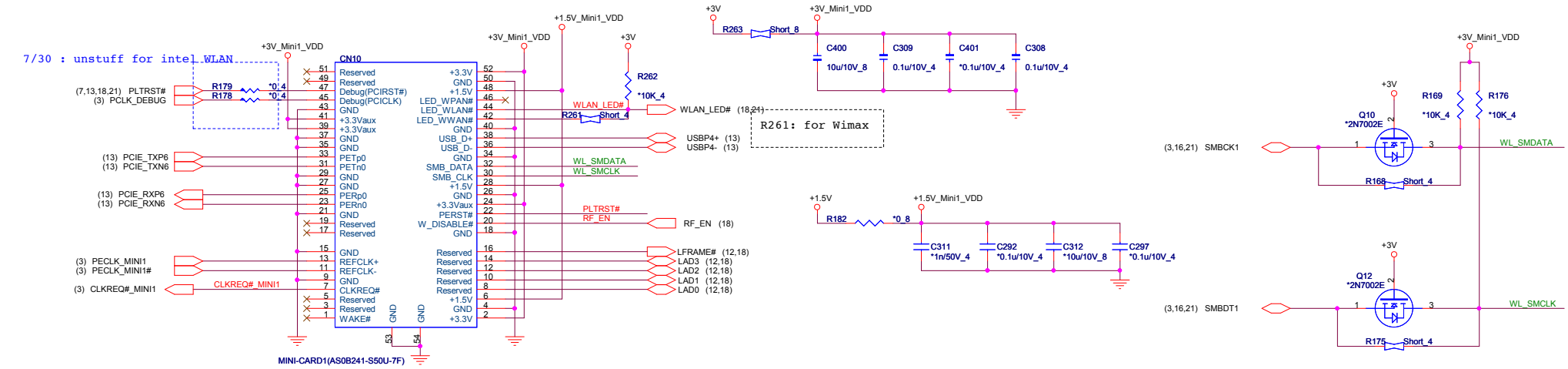
SM BUS PU



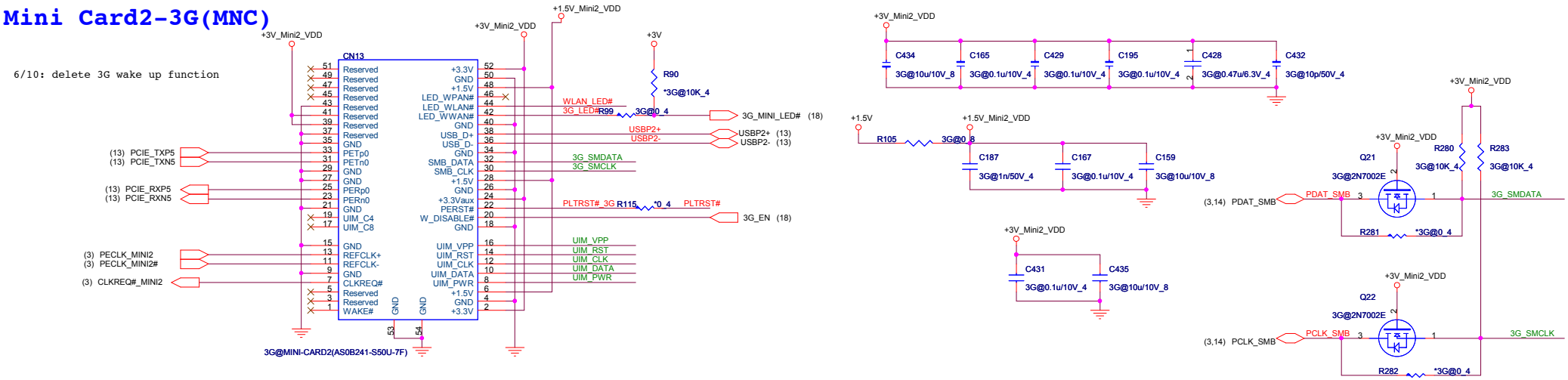
INTERNAL KEYBOARD STRIP SET

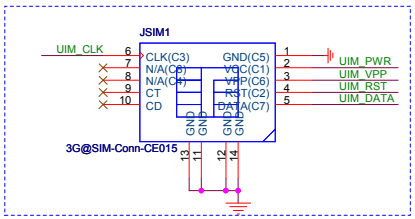


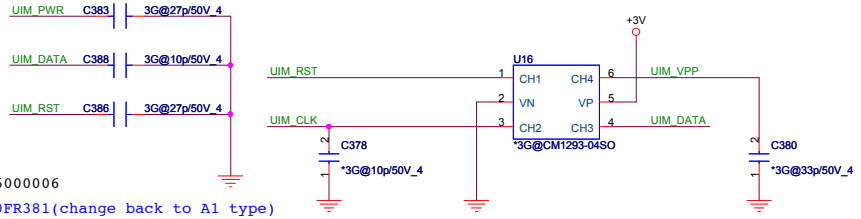
Mini Card1-WLAN/WMAX(MNC)

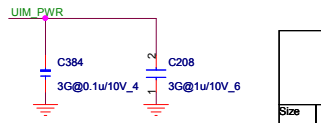


Mini Card2-3G(MNC)









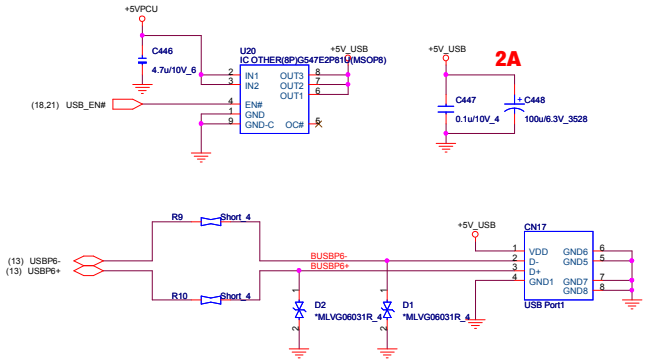
6/23 A2 test : change PN to DG006000005 or DG006000006

9/2 C test : change PN and footprint to DFHS10FR381(change back to A1 type)

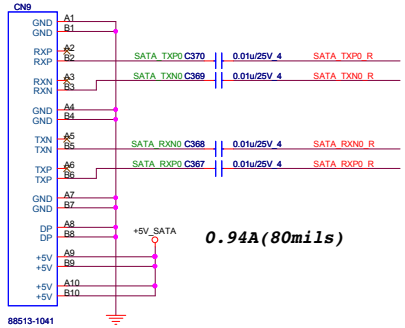
Layout : C431 and C252 place near JSIM2

Quanta Computer Inc.		
PROJECT : ZE8		
Size	Document Number: MINI PCIE (WLAN/WMAX/3G)	Rev: 1A
Date: Tuesday, September 29, 2009	Sheet 19 of 32	

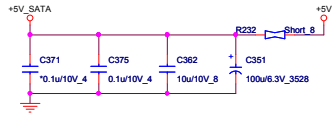
MB USB (USB)



2.5" SATA HDD(HDD)



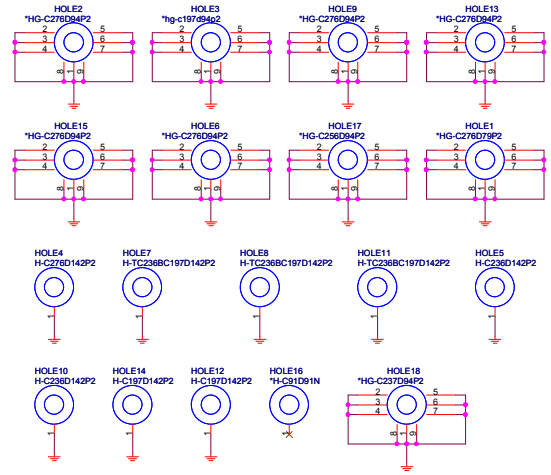
0.94A(80mils)



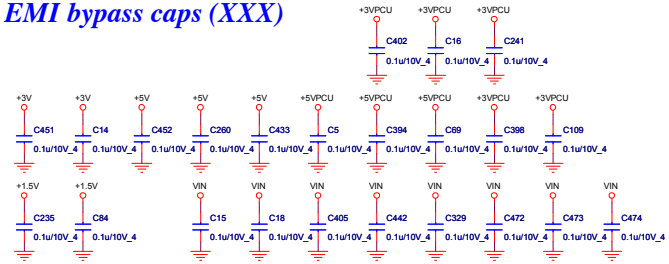
SATA ESD(EMC)

8/5 : because of the space is not enough, so, del SATA ESD U12 and C363.

HOLE (EXC)

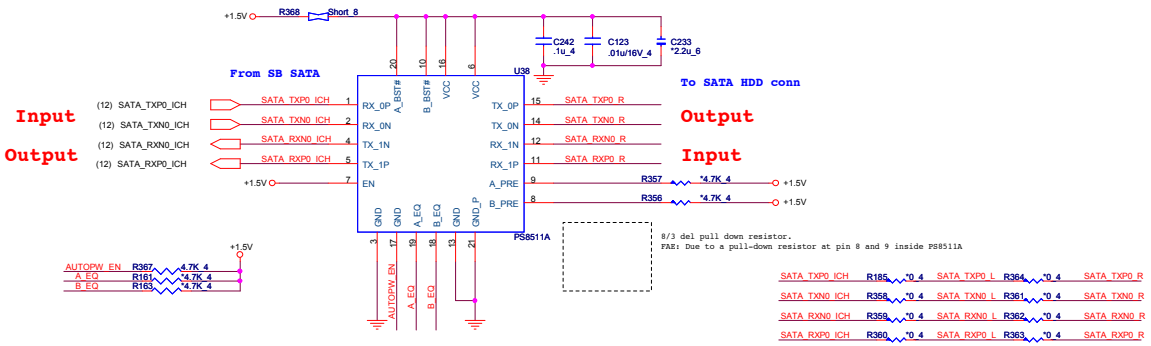


EMI bypass caps (XXX)



PAD

SATA RE-DRIVER IC(XXX)



8/3 del pull down resistor.
FAE: Due to a pull-down resistor at pin 8 and 9 inside PS8511A

PARADE : PS8511A

PIN 18,19	Input Equalization setting: Internal pull down ~150Kohm A_EQ/B_EQ = LOW: For short and medium length PCB traces (default) A_EQ/B_EQ = HIGH: For long length PCB traces
PIN 8,9	Output Pre-emphasis Setting: Internal pull down ~150Kohm A_PRE/B_PRE = LOW, Pre-emphasis disabled (default) A_PRE/B_PRE = HIGH, Pre-emphasis enabled
PIN 10,20	Output Level Boost setting: Internal pull up~150Kohm A_BST#/B_BST# = HIGH, SATAi/m output level 400~700mVpp A_BST#/B_BST# = LOW, SATAx output level 800~1200mVpp (default--SATA internal)
PIN 17	Automatic Power Saving Enable: Internal pull down~150Kohm AUTOPW_EN = HIGH, automatic power saving enable (default) AUTOPW_EN = LOW, automatic power saving disable

PARADE : PS8511A

EN	A_PRE	B_PRE	CH-0	CH-1
0	X	X	Standby	Standby
1	0	0	0dB	0dB
1	1	0	Pre-emphasis (3.5dB)	0dB
1	0	1	0dB	Pre-emphasis (3.5dB)
1	1	1	Pre-emphasis (3.5dB)	Pre-emphasis (3.5dB)

Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	USB/HDD/HOLE	1A

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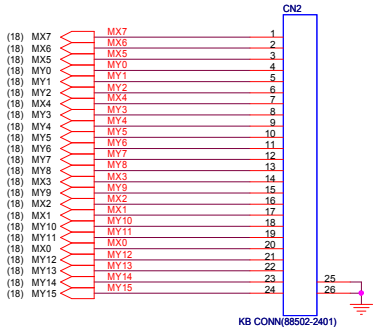
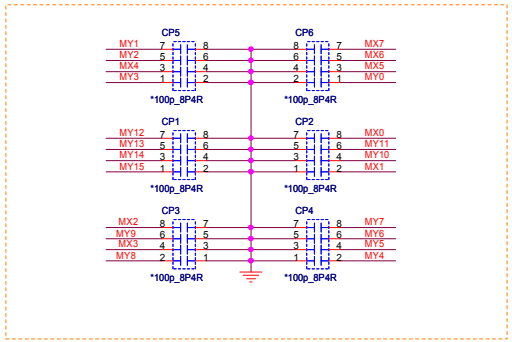
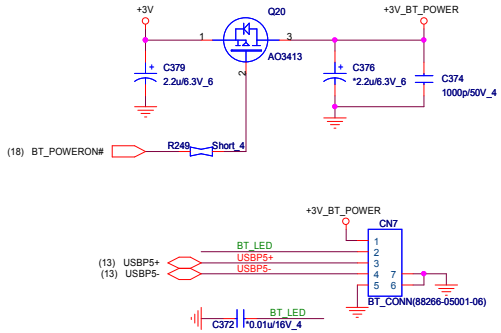
Keyboard(KBC)



For EMI Reserve Caps for debug

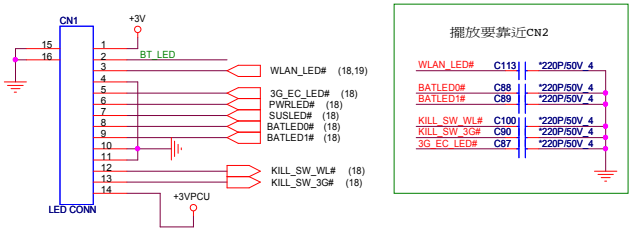


BuleTooth (BTM)

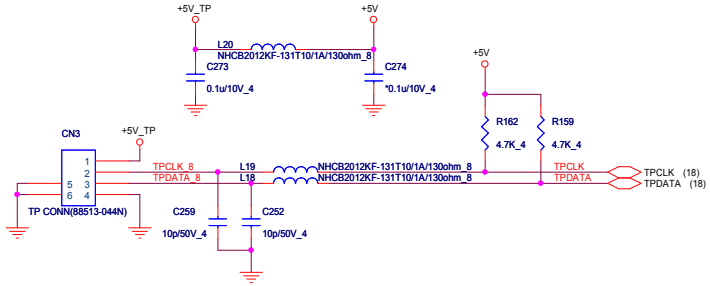


Be careful that bluetooth module PIN 2 is GND and PIN 5 is BT_LED.

LED D/B (UIF)



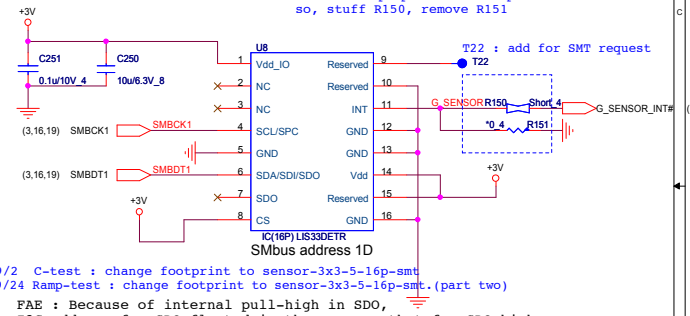
Touch Pad D/B (TPD)



G SENSOR(GSR)

A0 test : have free fall function, stuff R329, if not, stuff R327 just can stuff one of them

6/23 A2 test : per Acer request, use interrupt pin to detect panel status so, stuff R150, remove R151



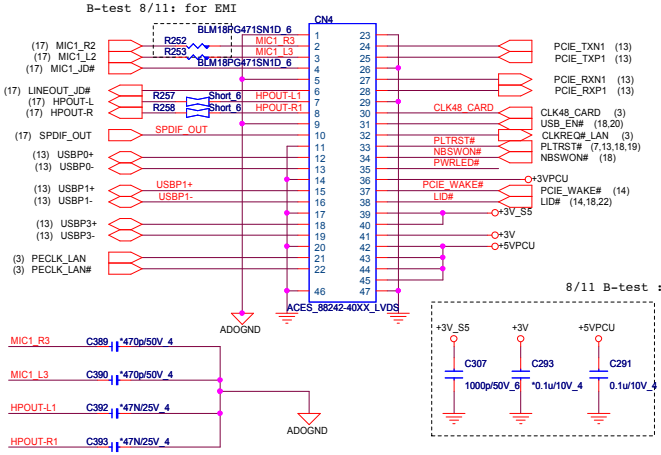
9/2 C-test : change footprint to sensor-3x3-5-16p-smt

9/24 Ramp-test : change footprint to sensor-3x3-5-16p-smt.(part two)

FAE : Because of internal pull-high in SDO, I2C address for SDO floated is the same as that for SDO high

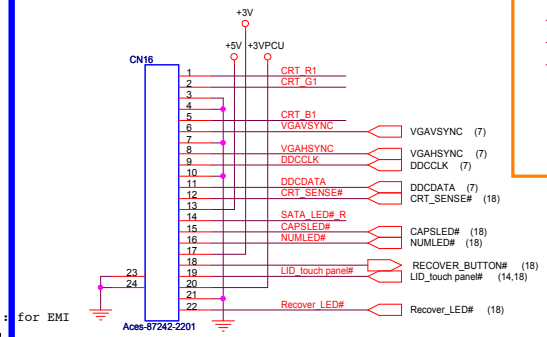
Card Reader/USB DB CONNECTER(MMC)/Power Connector

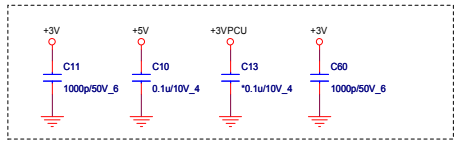
B-test 8/11: for EMI

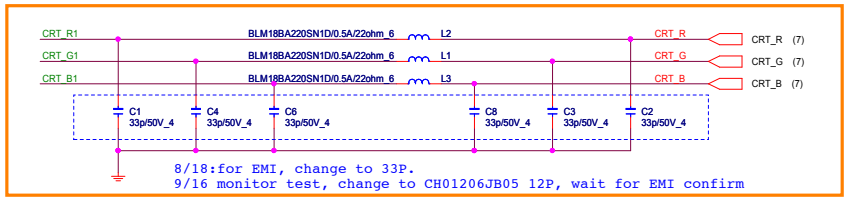


8/11 B-test : for EMI

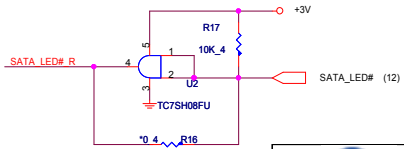
CRT D/B (CRT)

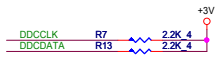






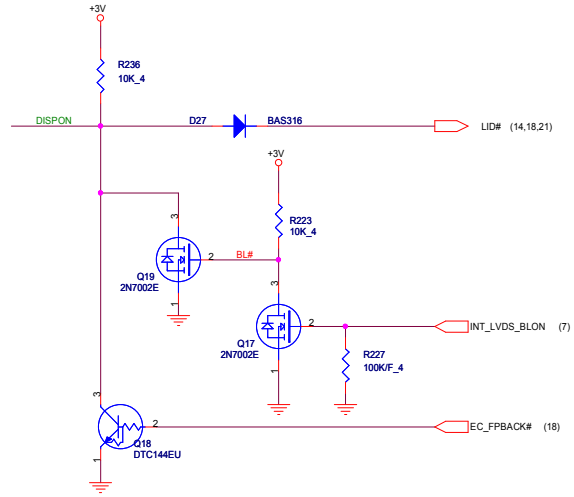
For EMI





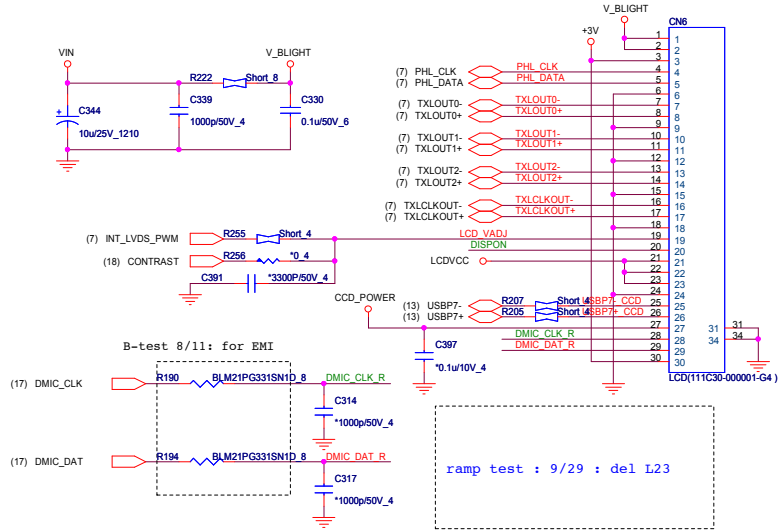
Quanta Computer Inc.			
PROJECT : ZE8			
Size	Document Number		Rev
	KB/BT/PR/TP/LAN/LED/CR Connects		1A
Date: Tuesday, September 29, 2009	Sheet 21	of 32	

Backlight Control(LDS)

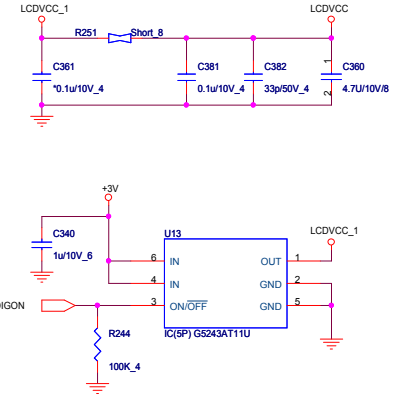


LED Panel(LDS)

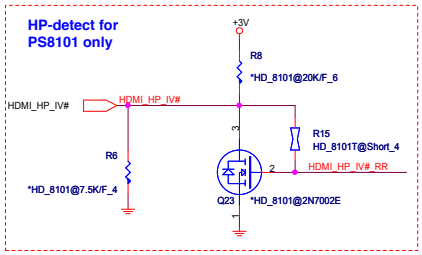
C test: 8/31: exchange V_BLIGHT and LCDVCC pin define



LED Panel POWER SWITCH(LDS)

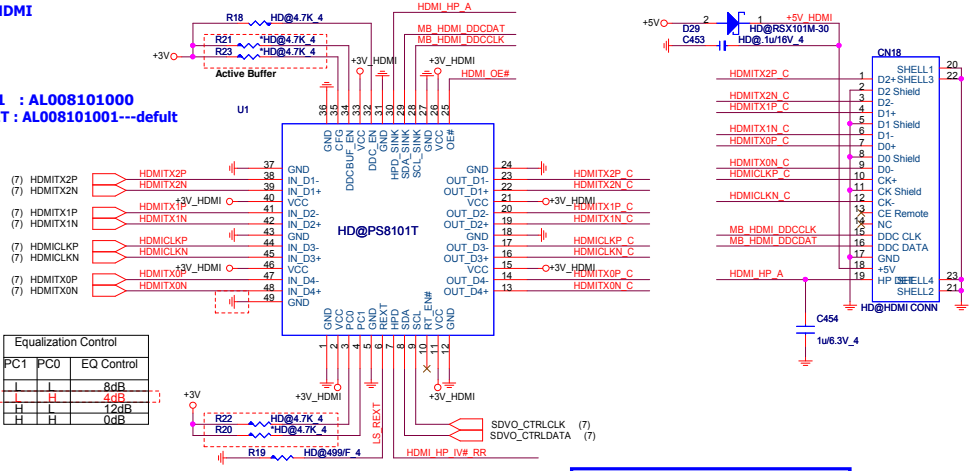


HDMI(HDM)



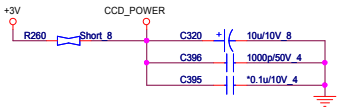
HDMI

PS8101 : AL008101000
PS8101T : AL008101001---defult

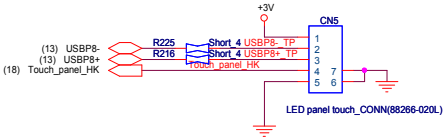


Equalization Control		
PC1	PC0	EQ Control
L	L	8dB
L	H	4dB
H	L	12dB
H	H	0dB

Camera(CCD)

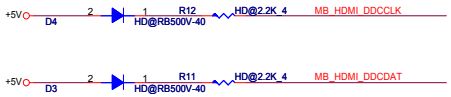


LED touch Panel connector (LDS)



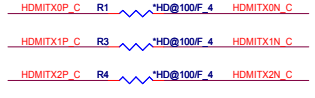
ramp test : 9/29 : del L24

SDVO I2C Control

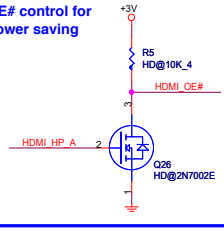


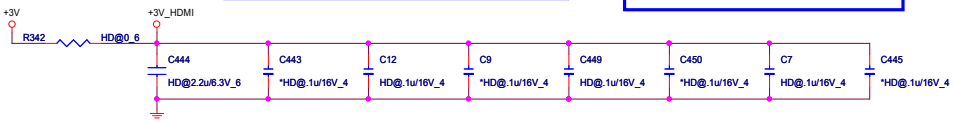
	PS8101 AL008101000	PS8101T AL008101001
pin 7	HPD	HPD#
pin 34	DDCBUF_EN	CFG0
pin 35	CFG	CFG1

FOR EMI



OE# control for power saving





Quanta Computer Inc.
PROJECT : ZE8

Size	Document Number	Rev
	LED Panel/CCD/HDMI	1A
Date: Tuesday, September 29, 2009	Sheet 22 of 32	

Charger(DCD)

DC-IN JACK

PJ2 — POWER_JACK dcjk-2dc3003-001211-5p

PA1 — PL10 HI0805R800R-10/5A/80ohm_8 — VA

PC150 0.1u/50V_6 | PC4 *0.1u/50V_6 | PC148 2200p/50V_6

PD1 1N4148WS

PD10 SX34

PD9 CYSMAJ20

PC6 0.1u/50V_6 | PC145 0.1u/50V_6

0.01_3720 PR5 — R1

PC12 0.1u/50V_6 | PR6 220K/F_6 | PR10 220K/F_6

PQ1 IMD2AT108

PQ36 AO4427 — C-STAGE change source

PC147 *0.1u/50V_6 | PC146 2200p/50V_6

PQ4 AO4427 — C-STAGE change source

PR57 33K_6 | PR59 10K_6 | PC162 1000p/50V_4

(18) D/C# — PQ5 2N7002K

+3VPCU — PR168 100K/F_6 — (18) ACIN

PR45 10/F_6 | PR43 10/F_6 | PC47 0.1u/50V_6 | PR20 4.7_6 | PC43 1u/16V_6 | PC25 1u/16V_6

PC58 2200p/50V_6 | PC57 *0.1u/50V_6 | PC56 10u/25V_1206

PD8 RB500V-40

PC30 0.1u/50V_6

(18) MBDATA | (18) MBCLK

PU5 CM1293A-04SO — MBCLK | +3VPCU | MBDATA | TEMP_MBAT

Add ESD diode base on EC FAE suggestion

PC31 0.1u/50V_6

PR23 49.9/F_6 | PR164 82.5K/F_6 | PR48 22K/F_6

PU2 ISL88731A

NC | GND | GND | GND | GND | CSSP | CSSN | VCC | VDDP

VDDSMB | SDA | SCL | ACOK | DCIN | ACIN | VREF | ICOMP | NC | VCOMP

BOOT | UGATE | PHASE | LGATE | PGND | CSOP | CSON | NC | VBF | GND

PR40 2.7_6 | PC34 0.1u/50V_8

PQ3 AO4932

PL6 6.8uH/4.5A_7X7X3 | PR58 0.01_3720

PR56 2.2/F_6 | PC55 2200p/50V_6

PC130 2200p/50V_6 | PC62 10u/25V_1206 | PC80 10u/25V_1206 | PC131 0.01u/50V_6 | PC163 1000p/50V_4

PR180 10/F_6 | PC27 0.1u/50V_6 | PR179 10/F_6 | PR172 *Short_4 | PR16 100_4

PR47 2.21K/F_6 | PC49 0.01u/50V_6 | PC52 *1u/16V_6 | PC51 0.01u/50V_6 | PC50 *0.01u/50V_6

ICMNT (18) — PC44 3300p/50V_4

PR65 *Short_6 | PC67 100p/50V_6

C114F3-108A1-L_Batt_Conn — PJ1 — MBAT+

PR63 *0_6 | PD5 RB500V-40

PL1 HI0805R800R-10/5A/80ohm_8 | PL4 HI0805R800R-10/5A/80ohm_8 — BAT-V

TEMP_MBAT (18)

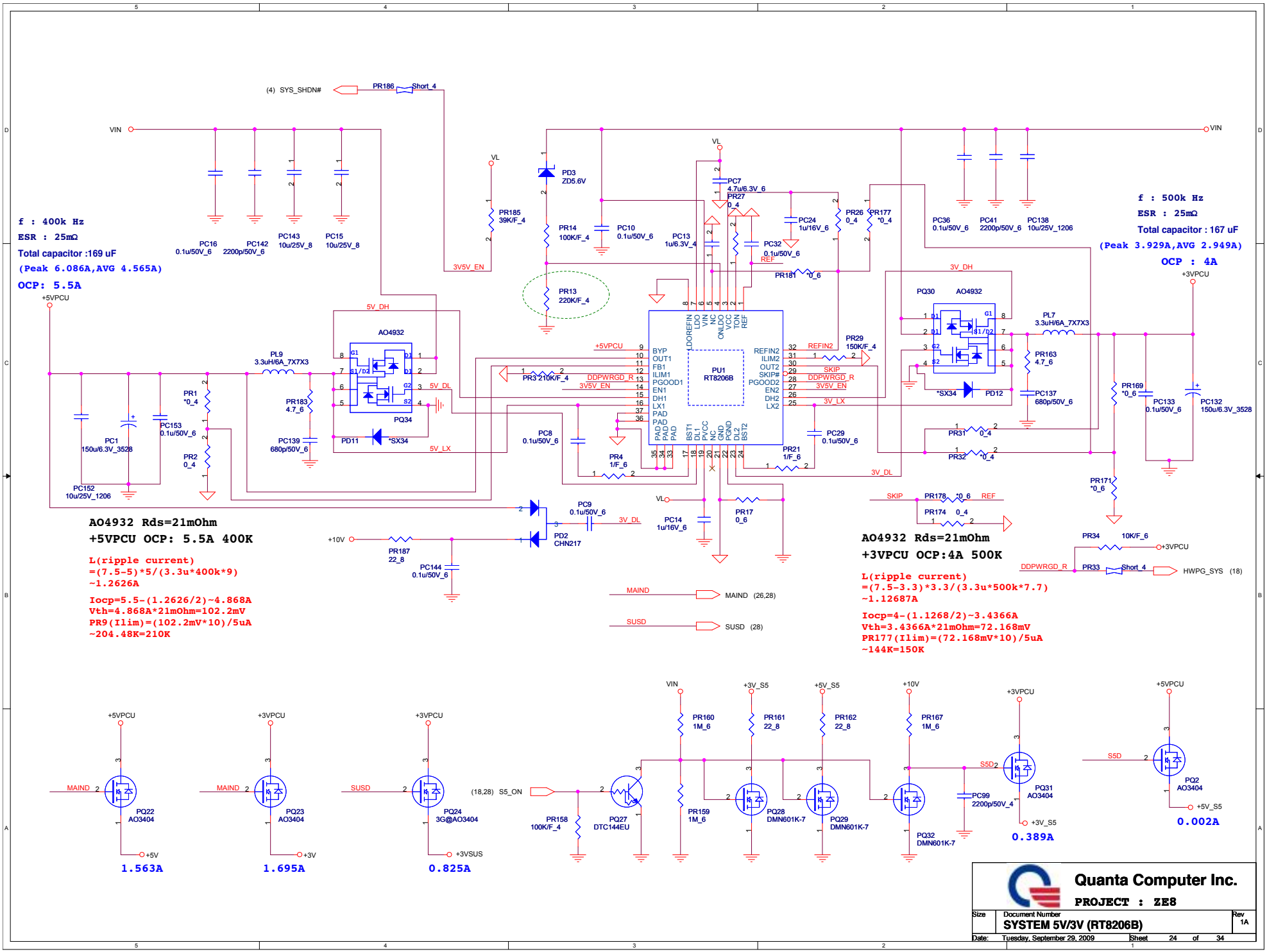
PR147 100K/F_6

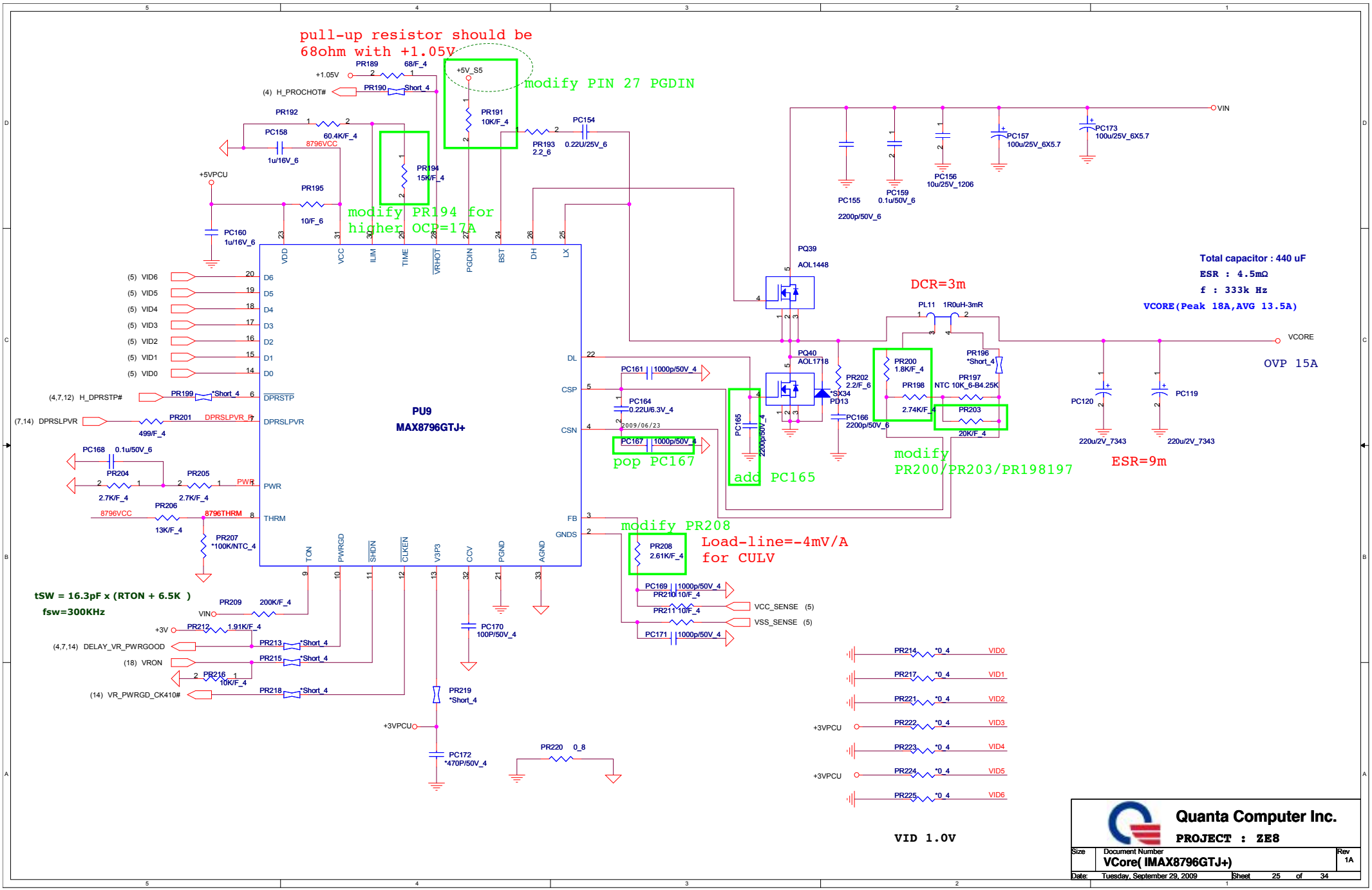
PC127 47p/50V_6 | PC121 0.1u/50V_6 | PC63 47p/50V_6

PR152 100_4 | PR150 100_4 — MBCLK | MBDATA

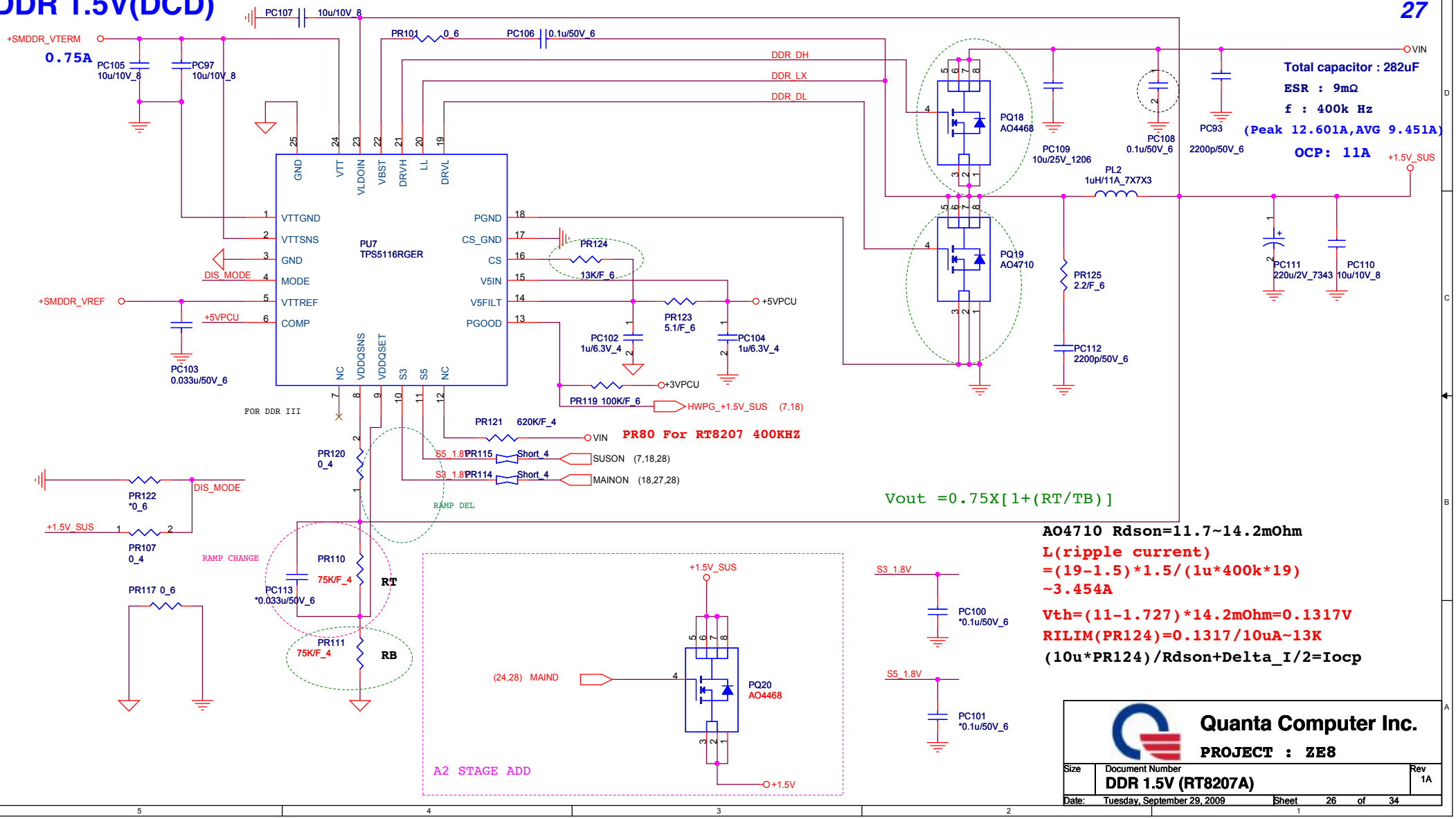
PR148 *100K/F_6 | PC122 0.01u/16V_4

Quanta Computer Inc.		
PROJECT : ZE8		
Size	Document Number: CHARGER (ISL88731)	Rev: 1A
Date: Tuesday, September 29, 2009	Sheet 23 of 34	

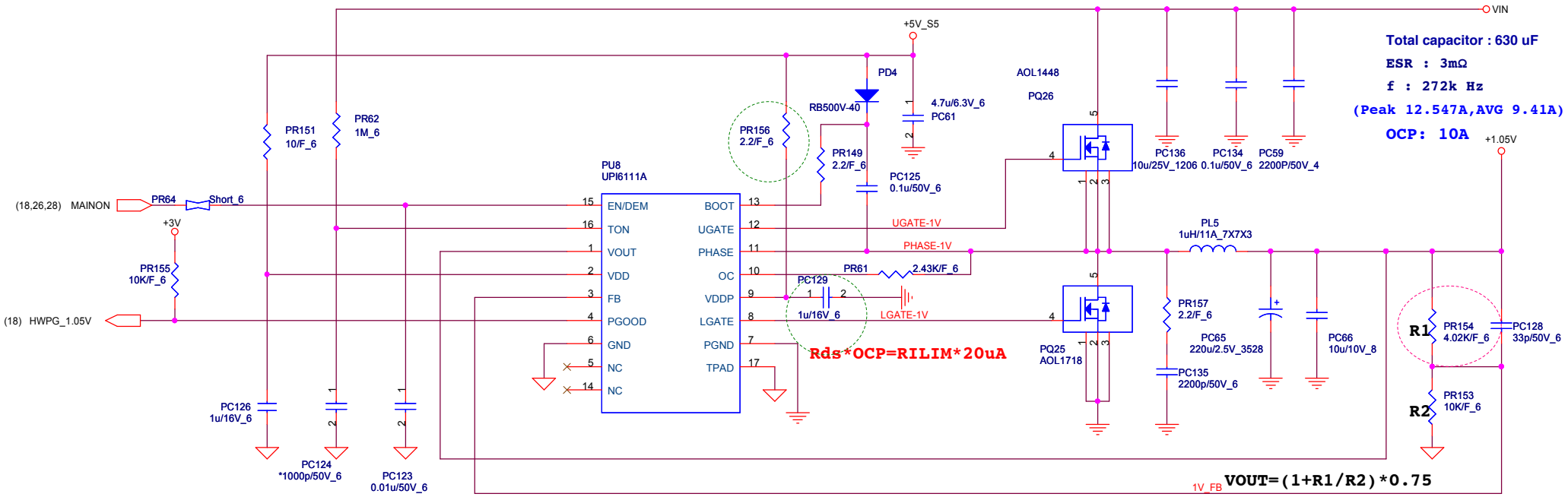

f : 400k Hz
ESR : 25mΩ
Total capacitor :169 uF
(Peak 6.086A,AVG 4.565A)
OCP: 5.5A
f : 500k Hz
ESR : 25mΩ
Total capacitor : 167 uF
(Peak 3.929A,AVG 2.949A)
OCP : 4A
AO4932 Rds=21mOhm
+5VPCU OCP: 5.5A 400K
L(ripple current)
=(7.5-5)*5/(3.3u*400k*9)
~1.2626A
Iocp=5.5-(1.2626/2)~4.868A
Vth=4.868A*21mOhm=102.2mV
PR9(Ilim)=(102.2mV*10)/5uA
~204.48K=210K
AO4932 Rds=21mOhm
+3VPCU OCP:4A 500K
L(ripple current)
=(7.5-3.3)*3.3/(3.3u*500k*7.7)
~1.12687A
Iocp=4-(1.1268/2)~3.4366A
Vth=3.4366A*21mOhm=72.168mV
PR177(Ilim)=(72.168mV*10)/5uA
~144K=150K
1.563A
1.695A
0.825A
0.389A
0.002A
Quanta Computer Inc.
PROJECT : ZE8
SYSTEM 5V/3V (RT8206B)
Tuesday, September 29, 2009


pull-up resistor should be
68ohm with +1.05V
modify PIN 27 PGDIN
modify PR194 for
higher OCP=17A
PU9
MAX8796GTJ+
PQ39
AOL1448
PQ40
AOL1718
DCR=3m
Total capacitor : 440 uF
ESR : 4.5mΩ
f : 333k Hz
VCORE(Peak 18A,AVG 13.5A)
OVP 15A
ESR=9m
pop PC167
add PC165
modify
PR200/PR203/PR198197
modify PR208
Load-line=-4mV/A
for CULV
tSW = 16.3pF x (RTON + 6.5K)
fsw=300KHz
VID 1.0V
Quanta Computer Inc.
PROJECT : ZE8
VCore(IMAX8796GTJ+)
Tuesday, September 29, 2009

DDR 1.5V(DCD)



Quanta Computer Inc.		
PROJECT : ZE8		
Size	Document Number: DDR 1.5V (RT8207A)	Rev: 1A
Date: Tuesday, September 29, 2009	Sheet 26 of 34	



TON=3.85p*RTON*Vout/(Vin-0.5)

Frequency=Vout/(Vin*TON)

TON=3.85p*1M*1/(Vin-0.5)

Frequency=1/(0.0036767)=272K

AOL1718 Rdson=4.6mOhm

OCP=10-0.8A

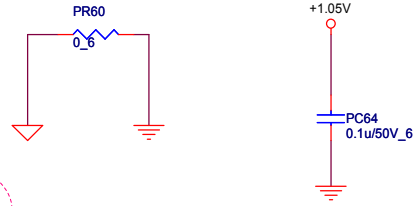
L(ripple current)
=(19-1.05)*1.05/(1u*272k*19)
~3.646A

4.6m*10=RILIM*20uA

RILIM(PR61)=2.3K--- 2.43K

RAMP CHANGE

	743 CPU	Other CPU
PR154	4.22K (CS24223F917)	4.02K (CS24023F928)



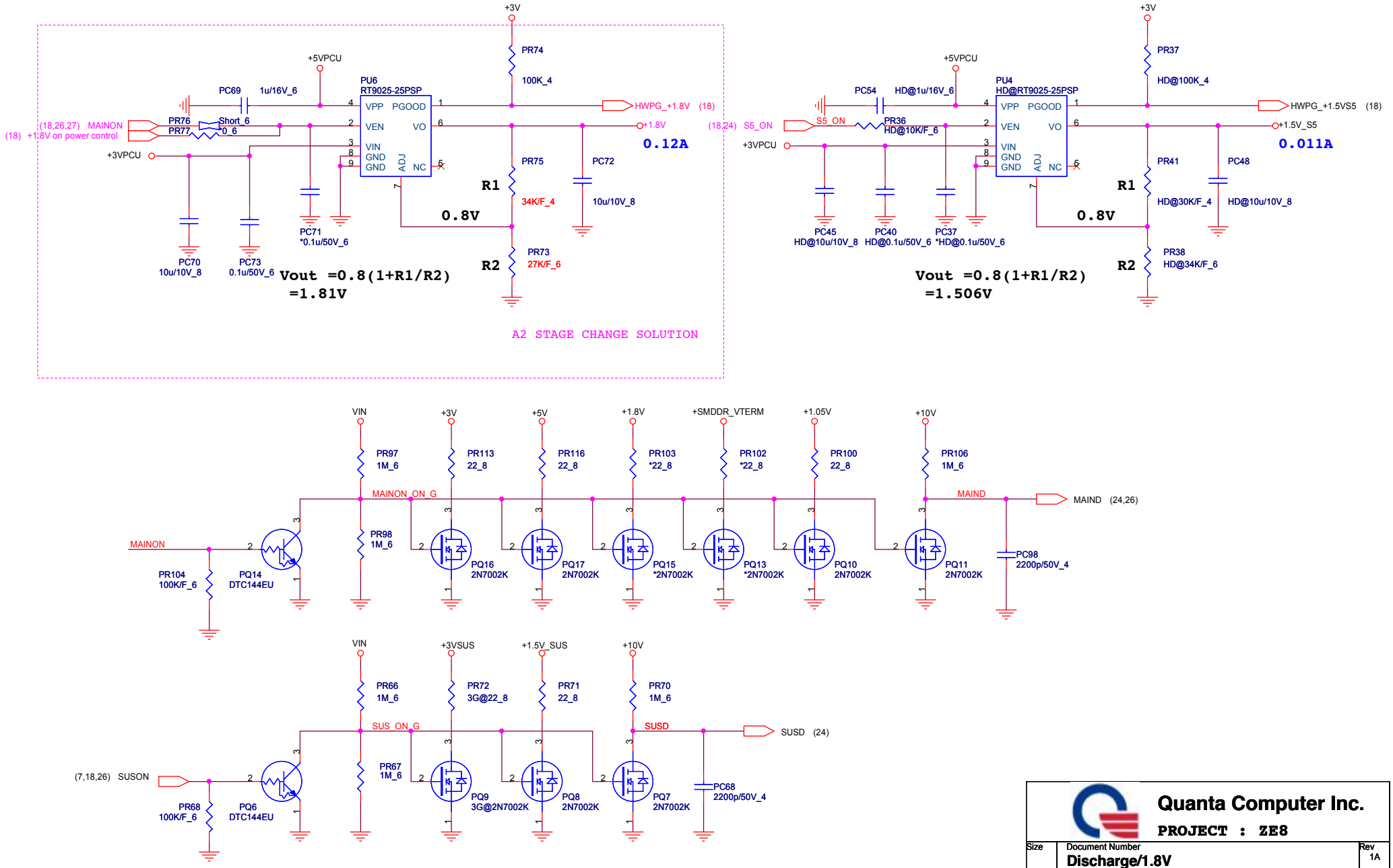
Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	VCCP 1.05V (RT8202A)	1A

Date: Tuesday, September 29, 2009 Sheet 27 of 34

Discharger/1.8V(DCD)

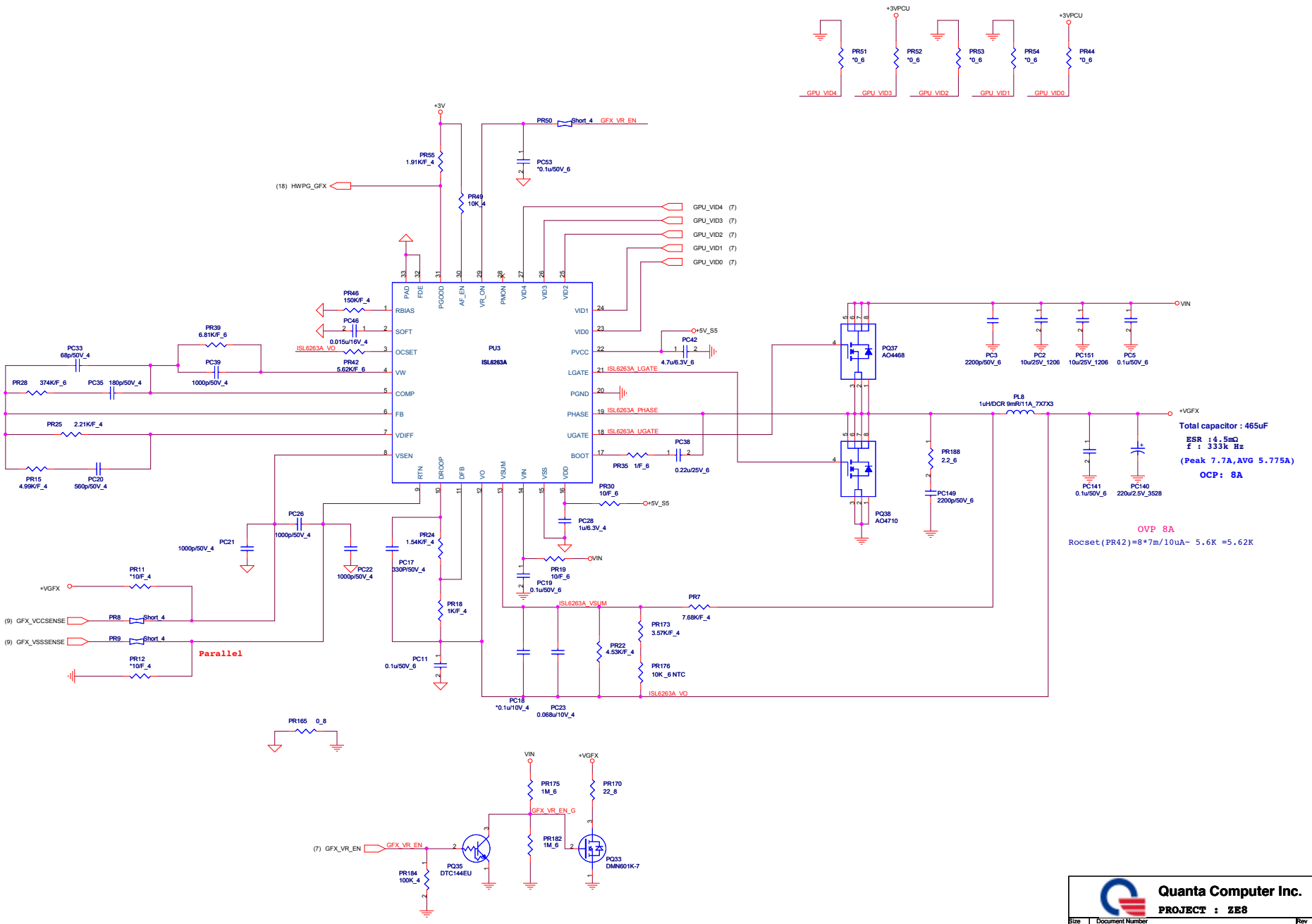


Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	Discharge/1.8V	1A

Date: Tuesday, September 29, 2009 Sheet 28 of 34

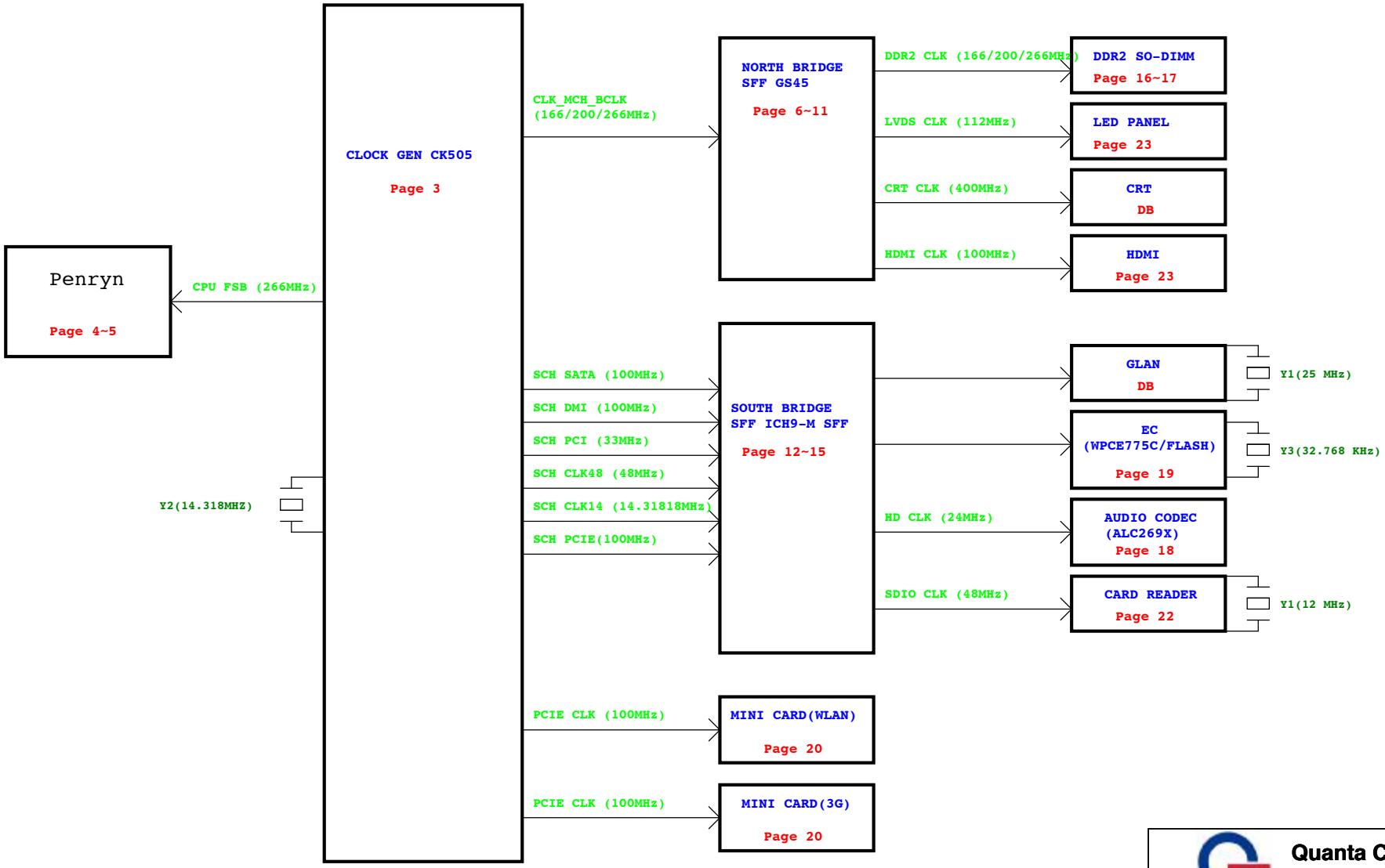


Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	1.05V_GFX	1A

Date: Tuesday, September 29, 2009 Sheet 29 of 34

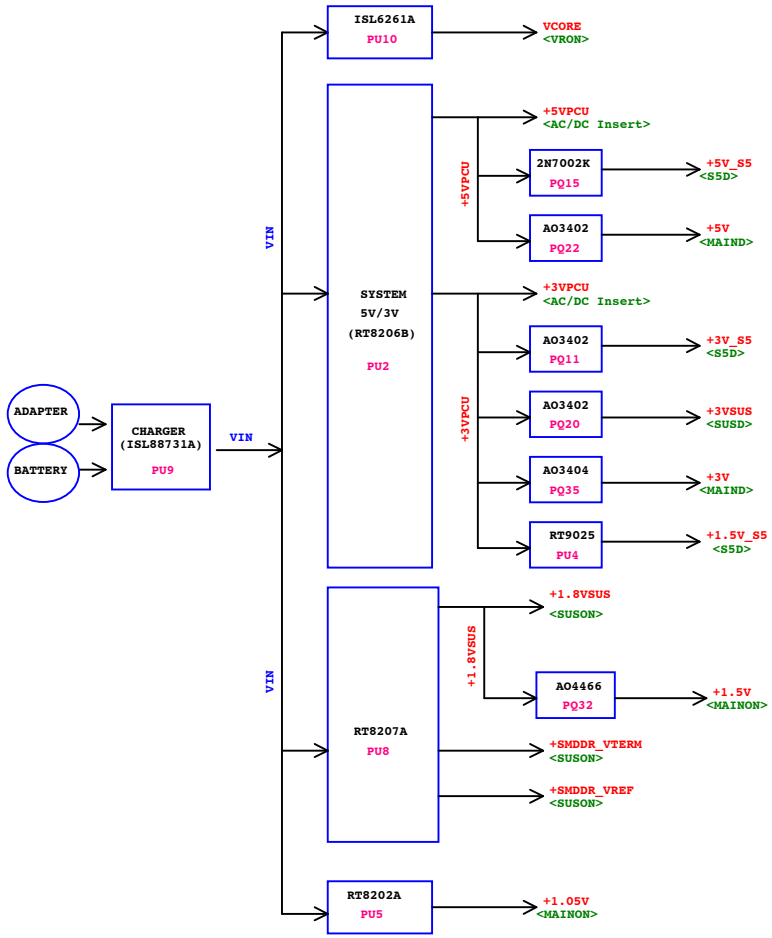


Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	Clock Distribution Diagram	1A

Date: Tuesday, September 29, 2009 Sheet 30 of 34



POWER	Distribution
VCORE	CPU
+5VPCU	RTC, USB Connecter
+5V_S5	ICH9M Power
+5V	ICH9M Power, CRT, Audio Codec, SATA HDD, Touch Pad ,HDMI
+3VPCU	RTC, LED Power, CRT, EC, ID , SPI Flash , Green Adapter
+3V_S5	ICH9M Power, CR
+3VSUS	3G
+3V	CLK_GEN Power, Thermal Sensor Power, NB Power, SB, DDRII Power, Audio Codec, LCD Power, WLAN/WMAX, 3G, Card Reader, BT, EC, LED, CRT, CAMERA
+1.5V_S5	ICH9M Power
+1.8VSUS	NB Power, DDRII SO-DIMM
+1.5V	CPU, NB, SB, AUDIO Codec, WLAN/WMAX, 3G
+SMDDR_VTERM	DDRII SO-DIMM
+SMDDR_VREF	DDRII SO-DIMM
+1.05V	CLK_GEN, CPU, NB, SB

Quanta Computer Inc.
PROJECT : ZE8
Size | Document Number: Power Tree | Rev: 1A
Date: Tuesday, September 29, 2009 | Sheet 31 of 34

CK505 Clock Setting Table

Differential CPU Clock

Pin Name	Pin	Net Name	Description
CPU_0	61	CLK_CPU_BCLK	
CPU_0#	60	CLK_CPU_BCLK#	Differential CPU clock
CPU_1	58	CLK_MCH_BCLK	
CPU_1#	57	CLK_MCH_BCLK#	Differential NB GS45 clock

PCI Express Clock

Pin Name	Pin	Net Name	Description
SRC0/DOT96	20	DREFCLK	
SRC0#/DOT96#	21	DREFCLK#	96MHz DOT clock for NB GS45
LCDCLK/27M	24	DREFSSCLK	
LCDCLK#/27M_SS	25	DREFSSCLK#	Clock output for NB GS45 graphic contoller
SRC2	28	PECLK_SATA	
SRC2#	29	PECLK_SATA#	Differential Serial Reference Clock for SB ICH9M SATA
SRC3/CR#_C	31	PECLK_ICH	
SRC3#/CR#_D	32	PECLK_ICH#	Differential Serial Reference Clock for SB ICH9M
SRC4	34	PECLK_LAN	
SRC4#	35	PECLK_LAN#	Differential Serial Reference Clock for on board LAN
SRC6	48	PECLK_MINI2	
SRC6#	47	PECLK_MINI2#	Differential Serial Reference Clock for Mini Card 2
SRC7/CR#_F	51		No use
SRC7#/CR#_E	50	CLKREQ#_MINI2	Clock Request for Mini Card 2 (SRC6)
SRC8/CPU_ITP	54		
SRC8#/CPU_ITP#	53		No use
SRC9	37	PECLK_MINI1	
SRC9#	38	PECLK_MINI1#	Differential Serial Reference Clock for MINI CARD 1
SRC10	41	PECLK_3GPLL	
SRC10#	42	PECLK_3GPLL#	Differential Serial Reference Clock for NB GS45
SRC11/CR#_H	40	CLKREQ#_MCH	Clock Request for NB GS45 (SRC10)
SRC11#/CR#_G	39	CLKREQ#_MINI1	Clock Request for Mini Card 1 (SRC9)

PCI Clock

Pin Name	Pin	Net Name	Description
PCI0/CR#_A	8	CLKREQ#_SATA	Clock Request for SATA (SRC2)
PCI1/CR#_B	10	CLKREQ#_LAN	Clock Request for on board LAN (SRC4)
PCI2	11	PCLK_DEBUG	PCI clock for debug card
PCI3	12		No use
PCI4	13	PCLK_EC	PCI clock for EC
PCI5	14	PCLK_ICH	PCI clock for SB ICH9M

Other Clock

Pin Name	Pin	Net Name	Description
USB_48	17	CLK48_ICH	48MHz for SB ICH9M
		CLK48_CARD	48MHz for USB Card Reader
REF	5	CLK14_ICH	14.318MHz for SB ICH9M

Clock Request Table

CLKREQ#	MAPPING		Control
	0	1	
CR#_A	SRC0	SRC2	SATA
CR#_B	LCDCLK	SRC4	LAN
CR#_C	SRC0	SRC2	N/A
CR#_D	LCDCLK	SRC4	N/A
CR#_E	SRC6		MINI2
CR#_F	SRC8		N/A
CR#_G	SRC9		MINI1
CR#_H	SRC10		MCH

Quanta Computer Inc.

PROJECT : ZE8

Size	Document Number	Rev
	Schematic Setting	1A
Date: Tuesday, September 29, 2009	Sheet 32 of 34	

Model	REV	DATE	CHANGE LIST	NOTE
ZE8	A1A		PAGE23 :move LED touch Panel hall sensor to LAN DB	ECN Release
			PAGE20 : reserve R179 , R183 for 3G wake up function	
			PAGE5 : Del C128,C173,C149,C171,C130,C131,C133,C169,C181,C177,C132,C175,C140,C138,C185,C154,C135,C92,C184,C106,C117,C156,C186,C153 for placeing C386 in CPU BGA TOP side	
			PAGE18 :change U14 footprint to qfn48-7x7-5-58p-0_9h	
			PAGE23 :change CN18 PN to DFHD19MR053	
			PAGE23 :Add L28 and L29 for CCD and Touch screen USB signals	
			PAGE23 :change CN18 footprint to hdmi-100042mr019m21hzr-19p-v	
			PAGE23 :change CN19 footprint to 85204-0500x-5p-l	
			PAGE23 :add 5V power trace to CN19 for touch screen IC	
			PAGE19 :FAE suggest that add R352 for VCC latch up	
			PAGE19 : FAE suggest that change C347 and C350 value from 15p to 6.8p	
			PAGE10 : add stitching caps C149,C153 and C154 for DMI signals	
			PAGE14 : add stitching caps C156,C169 and C171 for DMI signals	
			PAGE20 : add C431 for SIM Card to filter power noise.	
			PAGE20 : change U10 PN from AL001293003 to AL001293000	
			PAGE21 : reserve ESD protection U11 for SATA signals.	
			PAGE23 : del +5V signal of CN19	
			PAGE18 : add stitching caps C432,C438 for Audio signals	
			PAGE21 : del hole 19	
			PAGE22 : reserve C439, C440,C445,C446,C447,C448 for EMI	
			PAGE23 : reserve C106 for EMI	
			PAGE 19, 20 : del R179, R183 and 3G wake up signals of 3G wake up function	
			PAGE19 : add D30 for WLAN_LED# connect from WALN connector to EC	
			PAGE19 : add 3G_EC_LED# signal from EC to LED connector CN2	
			PAGE19 : change R233 to D31 for leakage issue.	
			PAGE22 : del C426 due to don't need 3G_MINI_LED# singal from 3G connector to LED connector CN2	
			PAGE21 : add EMI bypass caps	
			PAGE23 : HDMICLKP swap to HDMITX0P,HDMICLKN swap to HDMITX0N,HDMICLKP_C swap to HDMITX0P_C,HDMICLKN_C swap to HDMITX0N_C	
			6/13 : PAGE10 : change C63 and C208 value from 220u to 10u.	
			6/15 : PAGE18 : due to layout, add 9 GND pin for U14	
			6/15 : PAGE19 and 23 : add Touch_panel_HK signal for hot key on touch panel	
			6/16 : PAGE 23 : change R14 to C454 of CN18 for HDMI detect issue	
			6/18 : PAGE 23 : change CN5 PN to DFHD05MRD98	
			6/18 : PAGE 19 : change U14 PN to AKE38ZA0Q00	
	B1A		6/22 : PAGE 21 : change CN17_PN to DFHS04FR269	
			6/22 : PAGE 24 : change PJ1_PN to DFHD08MR085	
			6/23 : PAGE 22 : Per Acer request, use interrupt pin of G-sensor to detect panel status ,so , stuff R150, remove R151	
			6/25 : PAGE 19 : EC add +1.5V on power control net name to control 1.5V	
			6/25 : PAGE 22 : connect G-sensor interrupt signal to SB PIRQE#	
			6/26 : PAGE 26 : change V-core solution to Maxim IC	
			6/26 : PAGE 24 : add PD20 in TEMP_MBAT signal	
			6/29 : PAGE 9 : change C212 from 330U to 10U for placement issue	
			6/30 : PAGE 16 : change DDR2 to DDR3	
			7/2 : PAGE 14 : LID_touch panel# change from GPIO19 to GPIO7 (SCI)	
			7/2 : PAGE 16 : change DDR3 connector footprint to H=5.2mm	
			7/6 : PAGE 18,21 : add RECOVER_BUTTON# signal in EC and CRT DB	
			7/7 : PAGE 18,21 : add RECOVER_LED# signal in EC and CRT DB	
			7/7 : PAGE 24 : add PD11 and PD12	
			7/7 : PAGE 25 : add PD13	
			7/7 : PAGE 20 : add nut on Hole 7, Hole 8 and Hole 11	
			7/7 : PAGE 18 : add R355 for power consumption issue,Vendor suggest to place it close to EC.	
			7/8 : PAGE 18 : add D30 for current leakage issue of 3G_EC_LED# signal.	
			7/9 : PAGE 18 : add D31 to prevent current leakage of Recover_LED# signal.	
			7/10 : PAGE 19 : change the direction of Q21 and Q22 to prevent the current leakage	
			7/10 : PAGE 3 : follow vendor suggestion to change C226 from 33p to 27p.	
			7/13 : PAGE 18 : follow vendor suggestion to change C337 and C343 from 6.8p to 15p.	

Model	REV	DATE	CHANGE LIST	NOTE
ZE8	C1A		7/23 : PAGE 20 : change CN17 footprint to usb-04wl4b-4p-r-v	ECN Release
			7/23 : PAGE 20 : add U38 re-driver IC for SATA connector	
			7/29 : PAGE 19 : change JSIM1 pin define to solve SIM card not detect issue	
			7/31 : PAGE 20 : add parade solution of SATA re-driver IC	
			8/4 : PAGE 20 : change footprint of U38 to qfn20-4x4-5-21p-ps8511b	
			8/6 : because of DMI reference to GND, so, del C60 C67 C61 C150 C166 C153 CAPS	
			8/6 : PAGE 20 : change Hole 18 footprint HG-C237D94P2, Hole 16 to H-C91D91N	
			8/10 : PAGE 19 : change JSIM1 PN to DFHS06FS017 and change footprint to simcard-sim-06lj3g-10p	
			8/11 : add C244 C245=220pF, add C243 =680pF,change C11= 1000pF,add C60=1000pF,change C307= 1000pF,add C363=0.1uF,change C10= 0.1uF, R113 change to BLM18BA750SN1 ferrite bead,R252, R253 = ferrite bead (BLM18PG471SN1),R190, R194 = BLM21PG331SN1 for EMI	
			8/12 : change JSIM1 back to A2-test P/N and footprint.	
			8/13 : add C246,C247=220pF, add C471=0.1uF for EMI	
			8/28 : page13 : add pull high resister R160 in GNT3# pin for no video issue.	
			8/31 : page 22 : exchange V_BLIGHT and LCDVCC pin define	
			9/2 : page 19 : change PN and footprint of JSIM1 back to A1 type.	
			9/2 : page 21 : change G-Sensor footprint to sensor-3x3-5-16p-smt for SMT solder issue.	
			9/8 : page 23 : change battery connector footprint to bat-btj-08fg0b-8p-l-v for SMT issue.	
			9/8 : change R141,R303,R199,R259,R254,R174,R201,R172,R173,R217,R261,R168,R175,R249,R150,R15 to short pad	
	C3A		9/28 : change PU2 footprint from QFN28-5X5-5-33P to qfn28-5x5-5-33p-nb4	

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