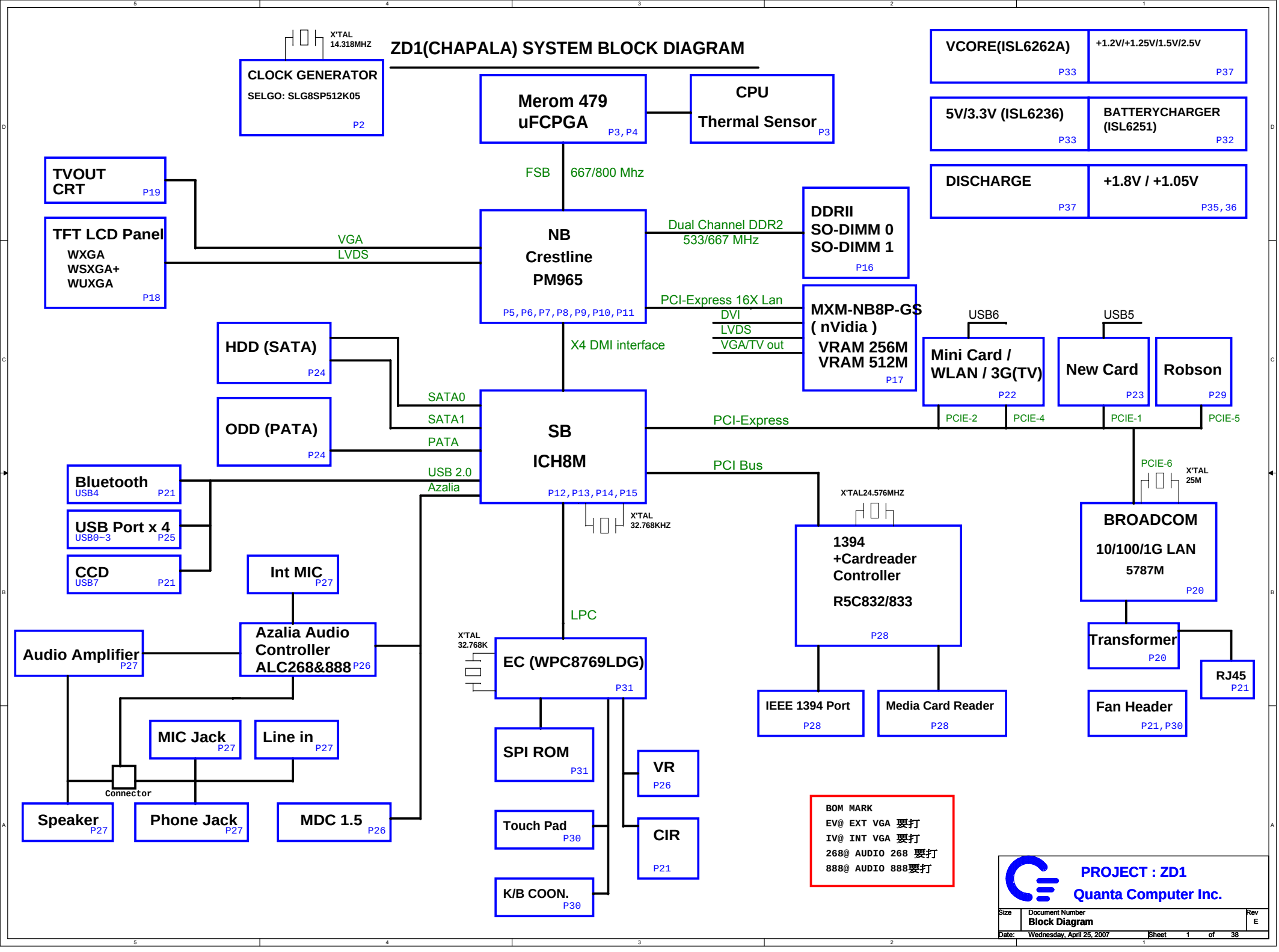
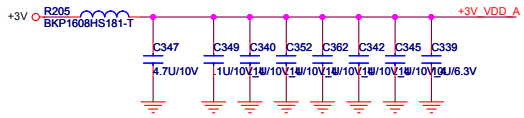
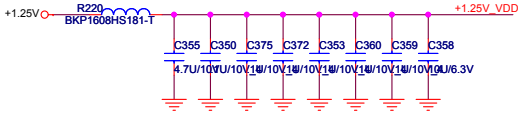
ZD1(CHAPALA) SYSTEM BLOCK DIAGRAM

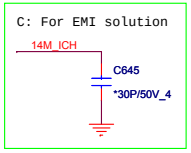


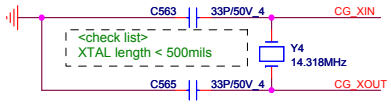
Clock Generator

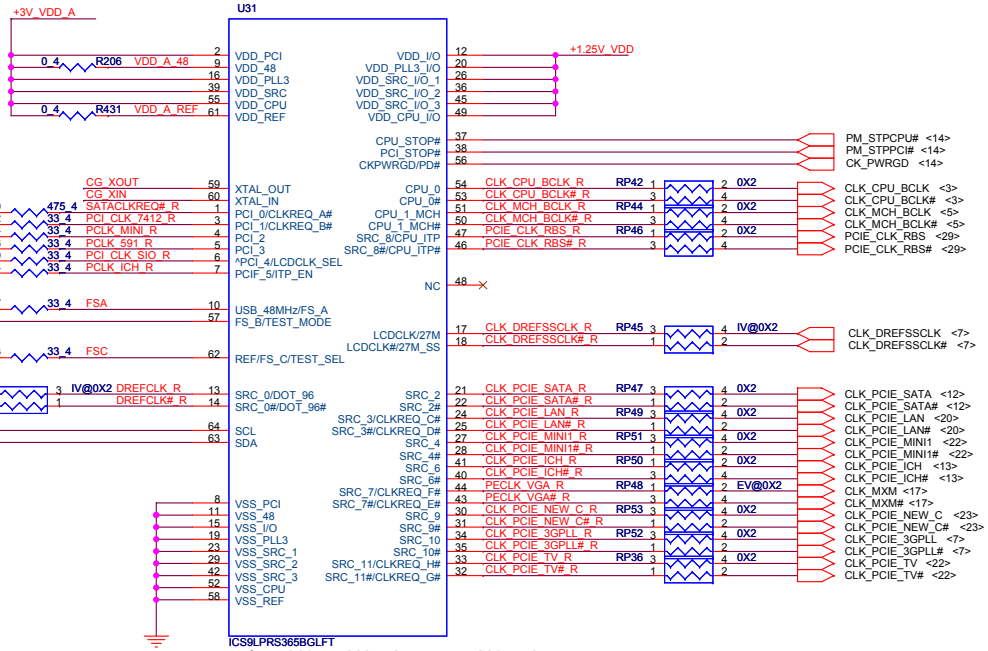
Change list:
B-test
1.Change U31 P/N to ALPRS365K13 (ICS)





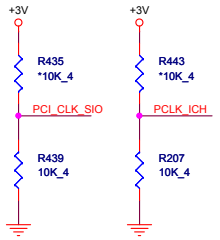




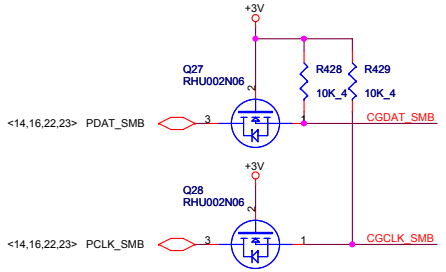


ICS9LPRS365BGLFT

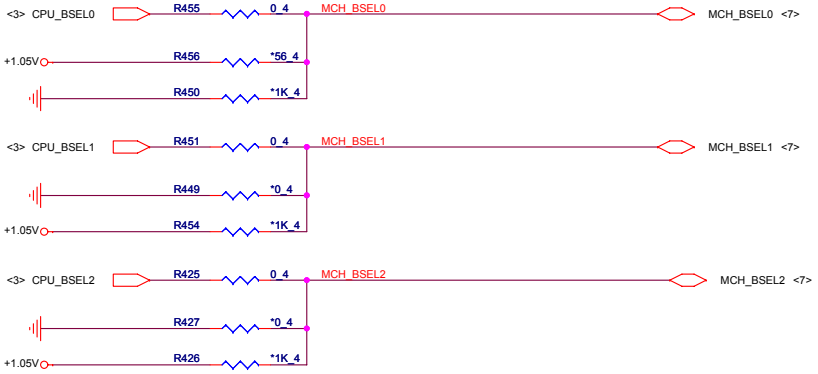
Main: ICS9LPRS365BGLFT:ALPRS365K13
SLG8SP512T: AL8SP512K05



Clock Gen I2C



CPU Clock select



BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	CLOCK GENERATOR CK505 W/REGULATOR	E
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CPU(HOST)

U22A

<5> H_A#[16:3]
H_A#3 J4
H_A#4 L5
H_A#5 L4
H_A#6 K5
H_A#7 M3
H_A#8 N2
H_A#9 J1
H_A#10 N3
H_A#11 P5
H_A#12 P2
H_A#13 L2
H_A#14 P4
H_A#15 P1
H_A#16 R1
ADDR GROUP 0
A[3]#
A[4]#
A[5]#
A[6]#
A[7]#
A[8]#
A[9]#
A[10]#
A[11]#
A[12]#
A[13]#
A[14]#
A[15]#
A[16]#
ADSTB[0]#

<5> H_ADSTB0#
<5> H_REQ#[4:0]
H_REQ#0 K3
H_REQ#1 H2
H_REQ#2 K2
H_REQ#3 J3
H_REQ#4 L1
REQ[0]#
REQ[1]#
REQ[2]#
REQ[3]#
REQ[4]#

<5> H_A#[35:17]
H_A#17 Y2
H_A#18 U5
H_A#19 R3
H_A#20 W6
H_A#21 U4
H_A#22 Y5
H_A#23 U1
H_A#24 R4
H_A#25 T5
H_A#26 T3
H_A#27 W2
H_A#28 W5
H_A#29 Y4
H_A#30 U2
H_A#31 V4
H_A#32 W3
H_A#33 AA4
H_A#34 AB2
H_A#35 AA3
ADDR GROUP 1
A[17]#
A[18]#
A[19]#
A[20]#
A[21]#
A[22]#
A[23]#
A[24]#
A[25]#
A[26]#
A[27]#
A[28]#
A[29]#
A[30]#
A[31]#
A[32]#
A[33]#
A[34]#
A[35]#
ADSTB[1]#

<5> H_ADSTB1#
V1

<12> H_A20M#
<12> H_FERR#
<12> H_IGNNE#
A6 A20M#
A5 FERR#
C4 IGNNE#

<12> H_STPCLK#
R350 0_4 H_STPCLK_R#
D5 STPCLK#
<12> H_INTR
<12> H_NMI
<12> H_SMI#
C6 LINT0
B4 LINT1
A3 SMI#

M4 RSVD[01]
N5 RSVD[02]
T2 RSVD[03]
V3 RSVD[04]
B2 RSVD[05]
C3 RSVD[06]
D2 RSVD[07]
D22 RSVD[08]
D3 RSVD[09]
F6 RSVD[10]
RESERVED

CONTROL
ADS# H1 → H_ADS# <5>
BNR# E2 → H_BNR# <5>
BPRI# G5 → H_BPRI# <5>
DEFER# H5 → H_DEFER# <5>
DRDY# F21 → H_DRDY# <5>
DBSY# E1 → H_DBSY# <5>
BR0# F1 → H_BREQ#0 <5>
IERR# D20 H_IERR# R79 56.2/F_4 +1.05V
INIT# B3 → H_INIT# <12>
LOCK# H4 → H_LOCK# <5>
RESET# C1 → H_CPURST# <5>
RS[0]# F3 → H_RS#0 <5>
RS[1]# F4 → H_RS#1 <5>
RS[2]# G3 → H_RS#2 <5>
TRDY# G2 → H_TRDY# <5>
HIT# G6 → H_HIT# <5>
HITM# F4 → H_HITM# <5>

XDP/ITP SIGNALS
BPM[0]# AD4 XDP_BPM#0 T8
BPM[1]# AD3 XDP_BPM#1 T2
BPM[2]# AD1 XDP_BPM#2 T3
BPM[3]# AC4 XDP_BPM#3 T6
PRDY# AC2 XDP_BPM#4 T4
PREQ# AC1 XDP_BPM#5 T5
TCK AC5 XDP_TCK
TDI AA6 XDP_TDI
TDO AB3 XDP_TDO
TMS AB5 XDP_TMS
TRST# AB6 XDP_TRST#
DBR# C20 XDP_DBRESET# R358 0_4 SYS_RST# <14>

THERMAL
PROCHOT# D21 H_PROCHOT_R# R355 56.2/F_4 +1.05V R82 *2.2K_4 H_PROCHOT# <34>
THERMDA A24 H_THERMDA
THERMDC B25 H_THERMDC
THERMTRIP# C7 PM_THRMTRIP#

<check list>
Default PU 56ohm if no use.
Serial R NC, If connect to power side PU 68ohm. Serial R 2.2K

H CLK
BCLK[0] A22 CLK_CPU_BCLK <2>
BCLK[1] A21 CLK_CPU_BCLK# <2>

Merom Ball-out Rev 1a

CPU Thermal monitor

+3V
Q25 RHU002N06
<31,32> MBCLK
Q26 RHU002N06
<31,32> MBDATA
R360 10K_4
R361 10K_4
R357 200
LM86VCC
C517 .1U/10V_4
U24
SCLK VCC
SDA DXP
ALERT# DXN
OVERT# GND
MAX6657
ADDRESS: 98H
H_THERMDA
C518 2200P/50V_4
H_THERMDC
<14,17> THERM_ALERT#
R362 *0_4
+3V R363 *10K_4 CPUFAN#_ON
<30> CPUFAN#_ON

<check list>
Layout Note:Routing 10:10 mils and away from noise source with ground gard

Thermal Trip

+1.05V
Q3 FDV301N
<7,14,34> DELAY_VR_PWRGOOD
R55 *10K_4
D4 *BAS316
C39 *1U
R56 56.2/F_4
Q4 MMBT3904
PM_THRMTRIP#
SYS_SHDN# <33>
PM_THRMTRIP# <7,12>

<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

PU/PD (ITP700)

+1.05V
XDP_TMS R44 39/F_4
XDP_TDI R42 150/F_4
XDP_BPM#5 R47 *54.9/F_4
XDP_TDO R45 54.9/F_4
XDP_TCK R54 27/F_4
XDP_TRST# R46 680/F_4

U22B

<5> H_D#[15:0]
H_D#0 E22
H_D#1 F24
H_D#2 F26
H_D#3 G22
H_D#4 F23
H_D#5 G25
H_D#6 E25
H_D#7 E23
H_D#8 K24
H_D#9 G24
H_D#10 J24
H_D#11 J23
H_D#12 H22
H_D#13 F26
H_D#14 K22
H_D#15 H23
D[0]#
D[1]#
D[2]#
D[3]#
D[4]#
D[5]#
D[6]#
D[7]#
D[8]#
D[9]#
D[10]#
D[11]#
D[12]#
D[13]#
D[14]#
D[15]#
DATA GRP 0

<5> H_DSTBN#0
<5> H_DSTBP#0
<5> H_DINV#0
DSTBN[0]#
DSTBP[0]#
DINV[0]#

<5> H_D#[31:16]
H_D#16 N22
H_D#17 K25
H_D#18 P26
H_D#19 R23
H_D#20 L23
H_D#21 M24
H_D#22 L22
H_D#23 M23
H_D#24 P25
H_D#25 P23
H_D#26 P22
H_D#27 T24
H_D#28 R24
H_D#29 L25
H_D#30 T25
H_D#31 N25
D[16]#
D[17]#
D[18]#
D[19]#
D[20]#
D[21]#
D[22]#
D[23]#
D[24]#
D[25]#
D[26]#
D[27]#
D[28]#
D[29]#
D[30]#
D[31]#
DATA GRP 1

<5> H_DSTBN#1
<5> H_DSTBP#1
<5> H_DINV#1
DSTBN[1]#
DSTBP[1]#
DINV[1]#

D[32]# Y22 H_D#32
D[33]# AB24 H_D#33
D[34]# V24 H_D#34
D[35]# V26 H_D#35
D[36]# V23 H_D#36
D[37]# T22 H_D#37
D[38]# U25 H_D#38
D[39]# U23 H_D#39
D[40]# Y25 H_D#40
D[41]# W22 H_D#41
D[42]# Y23 H_D#42
D[43]# W24 H_D#43
D[44]# W25 H_D#44
D[45]# AA23 H_D#45
D[46]# AA24 H_D#46
D[47]# AB25 H_D#47
DATA GRP 2

DSTBN[2]# Y26 → H_DSTBN#2 <5>
DSTBP[2]# AA26 → H_DSTBP#2 <5>
DINV[2]# U22 → H_DINV#2 <5>
H_D#[47:32] <5>

D[48]# AE24 H_D#48
D[49]# AD24 H_D#49
D[50]# AA21 H_D#50
D[51]# AB22 H_D#51
D[52]# AB21 H_D#52
D[53]# AC26 H_D#53
D[54]# AD20 H_D#54
D[55]# AE22 H_D#55
D[56]# AF23 H_D#56
D[57]# AC25 H_D#57
D[58]# AE21 H_D#58
D[59]# AD21 H_D#59
D[60]# AC22 H_D#60
D[61]# AD23 H_D#61
D[62]# AF22 H_D#62
D[63]# AC23 H_D#63
DATA GRP 3

DSTBN[3]# AE25 → H_DSTBN#3 <5>
DSTBP[3]# AF24 → H_DSTBP#3 <5>
DINV[3]# AC20 → H_DINV#3 <5>
H_D#[63:48] <5>

<Check list & CRB>
Layout note: Z=55 ohm
H_GTLREF<0.5"

<Check list & CRB>
Layout note: L<0.5"
COMP0/2 Z=27.4ohm
COMP1/3 Z=54.9

<CRB & Design guide>
Layout Note:Connect from SB and daisy chain to CPU CORE VR.Not use T connect.(SB/VR/CPU/NB)

+1.05V
R365 1K/F_4
R364 2K/F
H_GTLREF AD26
R101 *1K_4 CPU_TEST1 C23
R369 *1K_4 CPU_TEST2 D25
CPU_TEST3 C24
CPU_TEST4 AF26
CPU_TEST5 AF1
CPU_TEST6 A26
T10
T74
T7
T73
GTLREF
TEST1
TEST2
TEST3
TEST4
TEST5
TEST6
MISC

COMP[0] R26 COMP0 R367 27.4/F
COMP[1] U26 COMP1 R366 54.9/F_4
COMP[2] AA1 COMP2 R48 27.4/F
COMP[3] Y1 COMP3 R43 54.9/F_4
DPRSTP# E5 → ICH_DPRSTP# <7,12,34>
DPSLP# B5 → H_DPSLP# <12>
DPWR# D24 → H_DPWR# <5>
PWRGOOD D6 → H_PWRGD <12>
SLP# D7 → H_CPUSLP# <5>
PSI# AF6 → PSI# <34>

<2> CPU_BSEL0 B22
<2> CPU_BSEL1 B23
<2> CPU_BSEL2 C21
BSEL[0]
BSEL[1]
BSEL[2]

Merom Ball-out Rev 1a

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	CPU(1 of 2)/FAN/Thermal	E
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CPU(Power)

VCC_CORE

C43 C46 C49 C55 C59 C69 C84 C94 C102 C56
10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8

C60 C42 C47 C53 C58 C63 C80 C90 C99 C51
10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8

C93 C97 C91 C44 C83 C70
10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8

C86 C77 C61 C57 C52 C48
10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8 10U/6.3V_8
10U/6.3V_8
<Part Number>
<Description>

DESIGN GUIDE
CHANGE FROM 22UF *20 TO 10UF *32

+C40 330U/2.5V_7
+C41 330U_7
+C100 330U/2.5V_7

<Check list>
Option1:330U*6(ESR=1.5m ohm aggregate , ESL=0.8nH/6) and 22U*20(ESR=3mohm typ/20 , ESL=0.6nH/20)
Option2:330U*6(ESR=1.5m ohm aggregate , ESL=1.8nH/6) and 22U*32(ESR=3mohm typ/32 , ESL=0.6nH/32)

U22C

A7	VCC[001]	VCC[068]	AB20	
A9	VCC[002]	VCC[069]	AB7	
A10	VCC[003]	VCC[070]	AC7	
A12	VCC[004]	VCC[071]	AC9	
A13	VCC[005]	VCC[072]	AC12	
A15	VCC[006]	VCC[073]	AC13	
A17	VCC[007]	VCC[074]	AC15	
A18	VCC[008]	VCC[075]	AC17	
A20	VCC[009]	VCC[076]	AC18	
B7	VCC[010]	VCC[077]	AD7	
B9	VCC[011]	VCC[078]	AD9	
B10	VCC[012]	VCC[079]	AD10	
B12	VCC[013]	VCC[080]	AD12	
B14	VCC[014]	VCC[081]	AD14	
B15	VCC[015]	VCC[082]	AD15	
B17	VCC[016]	VCC[083]	AD17	
B18	VCC[017]	VCC[084]	AD18	
B20	VCC[018]	VCC[085]	AE9	
C9	VCC[019]	VCC[086]	AE10	
C10	VCC[020]	VCC[087]	AE12	
C12	VCC[021]	VCC[088]	AE13	
C13	VCC[022]	VCC[089]	AE15	
C15	VCC[023]	VCC[090]	AE17	
C17	VCC[024]	VCC[091]	AE18	
C18	VCC[025]	VCC[092]	AE20	
D9	VCC[026]	VCC[093]	AF9	
D10	VCC[027]	VCC[094]	AF10	
D12	VCC[028]	VCC[095]	AF12	
D14	VCC[029]	VCC[096]	AF14	
D15	VCC[030]	VCC[097]	AF15	
D17	VCC[031]	VCC[098]	AF17	
D18	VCC[032]	VCC[099]	AF18	
E7	VCC[033]	VCC[100]	AF20	
E9	VCC[034]			
E10	VCC[035]	VCCP[01]	G21	
E12	VCC[036]	VCCP[02]	V6	
E13	VCC[037]	VCCP[03]	J6	
E15	VCC[038]	VCCP[04]	K6	
E17	VCC[039]	VCCP[05]	M6	
E18	VCC[040]	VCCP[06]	J21	
E20	VCC[041]	VCCP[07]	K21	
F7	VCC[042]	VCCP[08]	M21	
F9	VCC[043]	VCCP[09]	N21	
F10	VCC[044]	VCCP[10]	N6	
F12	VCC[045]	VCCP[11]	R21	
F14	VCC[046]	VCCP[12]	R6	
F15	VCC[047]	VCCP[13]	T21	
F17	VCC[048]	VCCP[14]	T6	
F18	VCC[049]	VCCP[15]	V21	
F20	VCC[050]	VCCP[16]	W21	
AA7	VCC[051]			
AA9	VCC[052]	VCCA[01]	B26	+VCCA_PROC
AA10	VCC[053]	VCCA[02]	C26	
AA12	VCC[054]			
AA13	VCC[055]	VID[0]	AD6	H_VID0 <34>
AA15	VCC[056]	VID[1]	AF5	H_VID1 <34>
AA17	VCC[057]	VID[2]	AE5	H_VID2 <34>
AA18	VCC[058]	VID[3]	AF4	H_VID3 <34>
AA20	VCC[059]	VID[4]	AE3	H_VID4 <34>
AB9	VCC[060]	VID[5]	AF3	H_VID5 <34>
AC10	VCC[061]	VID[6]	AE2	H_VID6 <34>
AB10	VCC[062]			
AB12	VCC[063]			
AB14	VCC[064]	VCCSENSE	AF7	VCCSENSE <34>
AB15	VCC[065]			
AB17	VCC[066]			
AB18	VCC[067]	VSSSENSE	AE7	VSSSENSE <34>

Merom Ball-out Rev 1a

0C Delete R75,R63 0104

<REV.NO. 0.5/REF.NO.19343>
Ivcc Max 52A
Ivccp Max 6A(VCCP supply before Vcc stable)
Max 2A(VCCP supply after Vcc stable)
Ivcca Max 130mA

+1.05V
C76 C45 C75 C81 C89 C82
.1U/16V .1U/16V .1U/16V .1U/16V .1U/16V .1U/16V

+1.05V
C54 330U/2.5V_7
<Check list>
ESR=12m ohm

<CRB>
.01U near to B26 ball
+1.5V
R368 0

VCC_CORE
C520 .01U/16V_4
C130 10U/10V_8
R62 100/F
R58 100/F

<Demo board>
Routing 27.4ohm with 50mils spacing
PU/PD near to CPU 1"

U22D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AF2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AF25

Merom Ball-out Rev 1a

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Quanta Computer Inc.

Size	Document Number	Rev
	CPU(2 of 2)	E
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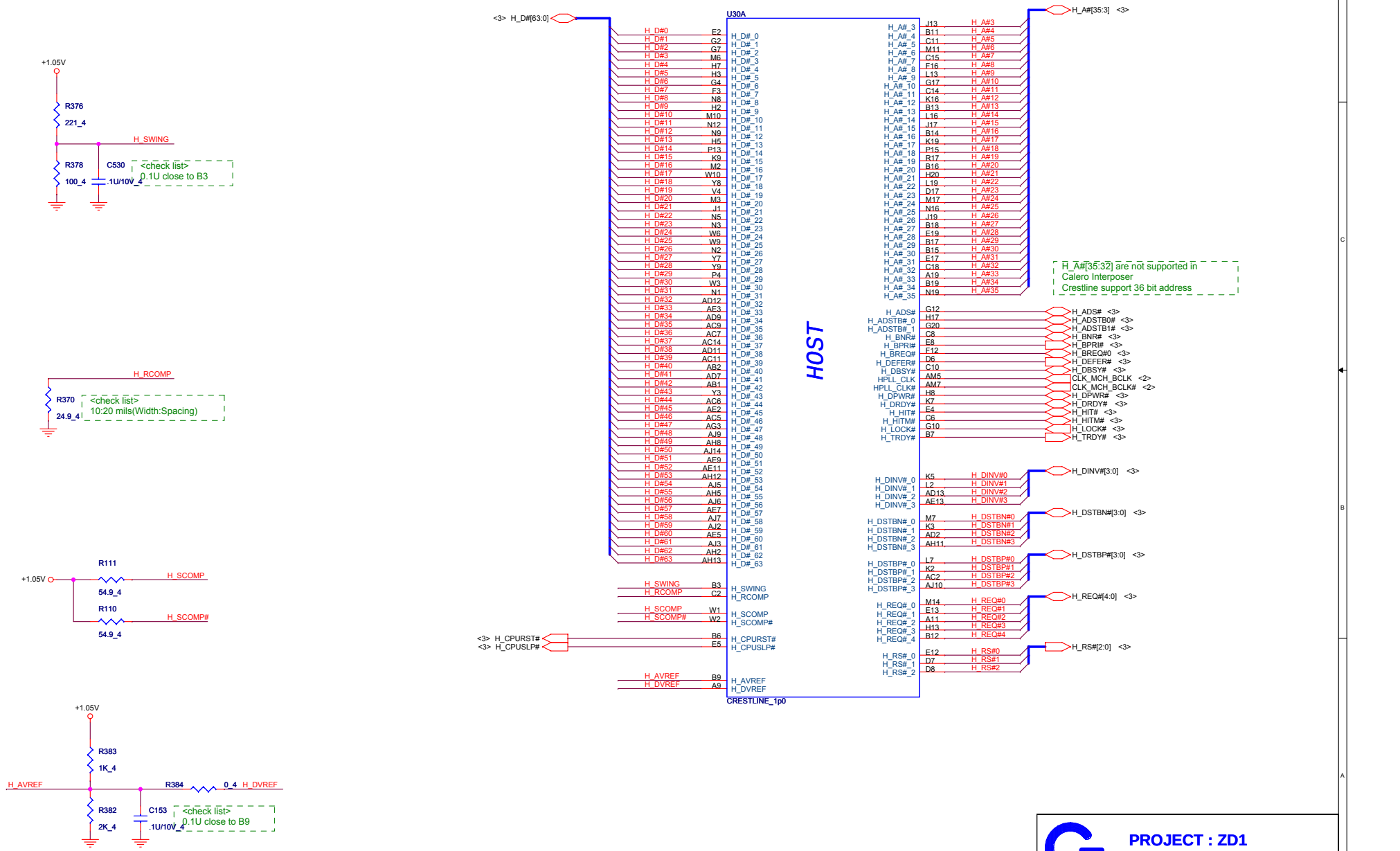
NB(HOST)



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH HOST(1/7)	E

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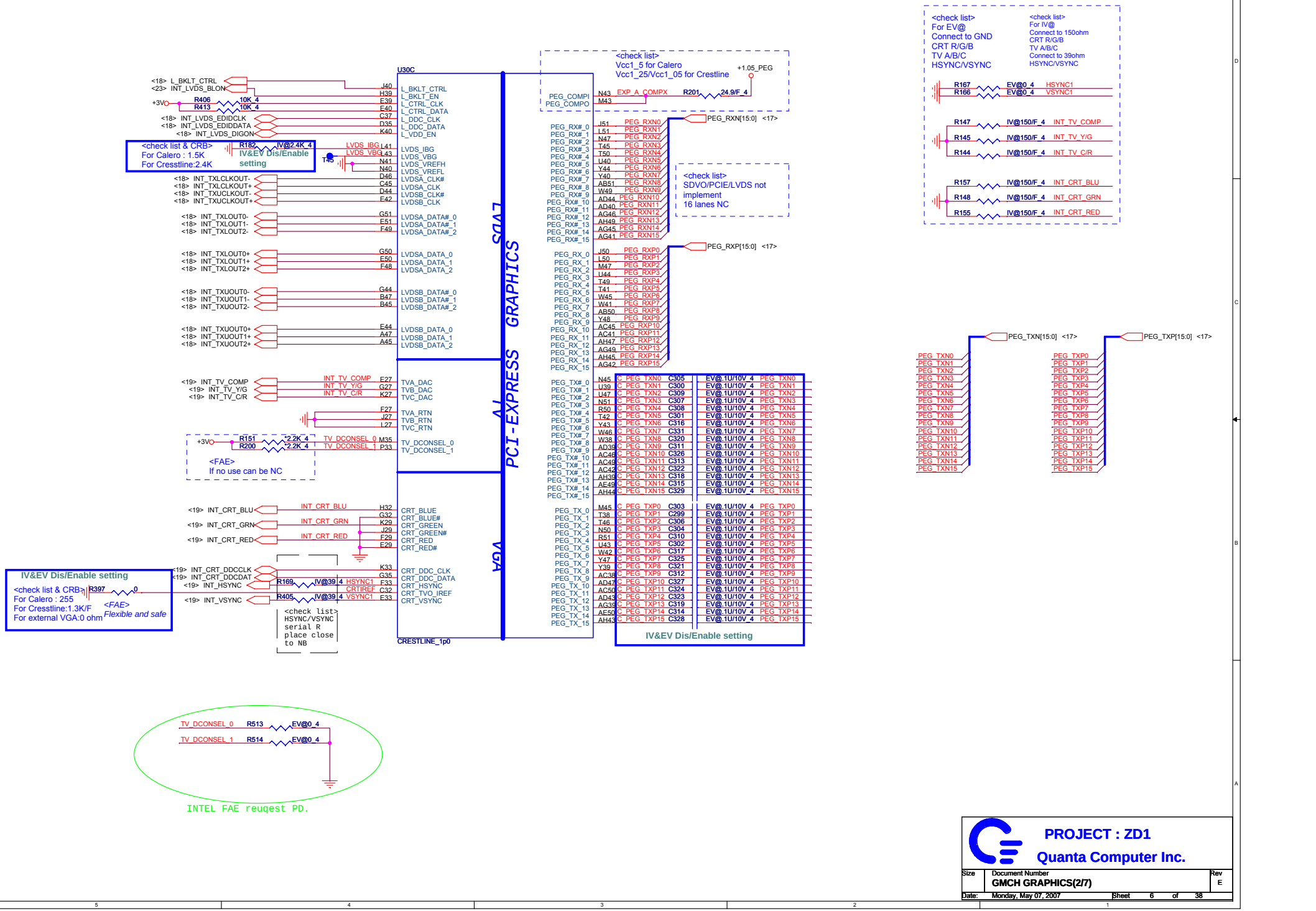

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Quanta Computer Inc.			
Size	Document Number		Rev
	GMCH GRAPHICS(2/7)		E
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Strapping table

All strap are sampled with respect to the leading edge of the GMCH power ok signal
CFG[17:3] have internal pull-up
CFG[18:19] have internal pull-down
Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reserved Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Clock gating disable 01 = ALL-Z Mode Enable 10 = XOR Mode Enable 11 = Normal Cperation (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation 1 = Reverse Lanes (Default)
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present

INTEL CRB
CRESSTLINE SHOULD USE 20OHM

<check list & CRB>
R Value select
For Calero : 80.6ohm
For Cresstline:20ohm
But check list use 80.6ohm

M_RCOMP# — R387 20/F_4 — <FAE> 80.6ohm — R388 20/F_4 — +1.8VSUS
M_RCOMP

INTEL CRB
ADD 0.1UF
C165 .1U/10V_4

U30B

RSVD
P36 RSVD1
P37 RSVD2
R35 RSVD3
N35 RSVD4
AR12 RSVD5
AR13 RSVD6
AM12 RSVD7
AN13 RSVD8
J12 RSVD9
AR37 RSVD10
AM36 RSVD11
AL36 RSVD12
AM37 RSVD13
D20 RSVD14

H10 RSVD20
B51 RSVD21
BJ20 RSVD22
BK22 RSVD23
BF19 RSVD24
BH20 RSVD25
BK18 RSVD26
BJ18 RSVD27
BF23 RSVD28
BG23 RSVD29
BC23 RSVD30
BD24 RSVD31

BH39 RSVD32
AW20 RSVD33
BK20 RSVD34
C48 RSVD35
D47 RSVD36
B44 RSVD37
C44 RSVD38
A35 RSVD39
B37 RSVD40
B36 RSVD41
B34 RSVD42
C34 RSVD43

DDR MUXING
SM_CK_0 AV29 M_CLK0 <16>
SM_CK_1 BB23 M_CLK1 <16>
SM_CK_3 BA25 M_CLK2 <16>
SM_CK_4 AV23 M_CLK3 <16>
SM_CK#_0 AW30 M_CLK#0 <16>
SM_CK#_1 BA23 M_CLK#1 <16>
SM_CK#_3 AW25 M_CLK#2 <16>
SM_CK#_4 AW23 M_CLK#3 <16>
SM_CKE_0 BE29 M_CKE0 <16>
SM_CKE_1 AY32 M_CKE1 <16>
SM_CKE_3 BD39 M_CKE2 <16>
SM_CKE_4 BG37 M_CKE3 <16>
SM_CS#_0 BG20 M_CS#0 <16>
SM_CS#_1 BK16 M_CS#1 <16>
SM_CS#_2 BG16 M_CS#2 <16>
SM_CS#_3 BE13 M_CS#3 <16>
SM_ODT_0 BH18 M_ODT0 <16>
SM_ODT_1 BJ15 M_ODT1 <16>
SM_ODT_2 BJ14 M_ODT2 <16>
SM_ODT_3 BE16 M_ODT3 <16>
SM_RCOMP BL15 M_RCOMP
SM_RCOMP# BK14 M_RCOMP#
SM_RCOMP_VOH BK31 SM_RCOMP_VOH
SM_RCOMP_VOL BL31 SM_RCOMP_VOL
SM_VREF_0 AR49 +SM_VREF_MCH
SM_VREF_1 AW4

CLK
DPLL_REF_CLK B42 CLK_DREFCLK CLK_DREFCLK <2>
DPLL_REF_CLK# C42 CLK_DREFCLK# CLK_DREFCLK# <2>
DPLL_REF_SSCLK H48 CLK_DREFSSCLK CLK_DREFSSCLK <2>
DPLL_REF_SSCLK# H47 CLK_DREFSSCLK# CLK_DREFSSCLK# <2>
PEG_CLK K44 CLK_PCIE_3GPLL CLK_PCIE_3GPLL <2>
PEG_CLK# K45 CLK_PCIE_3GPLL# CLK_PCIE_3GPLL# <2>

DMI
DMI_RXN_0 AN47 DMI_TXN0
DMI_RXN_1 AJ38 DMI_TXN1
DMI_RXN_2 AN42 DMI_TXN2
DMI_RXN_3 AN46 DMI_TXN3
DMI_TXN[3:0] <13>
DMI_RXP_0 AM47 DMI_TXP0
DMI_RXP_1 AJ39 DMI_TXP1
DMI_RXP_2 AN41 DMI_TXP2
DMI_RXP_3 AN45 DMI_TXP3
DMI_TXP[3:0] <13>
DMI_TXN_0 AJ46 DMI_RXN0
DMI_TXN_1 AJ41 DMI_RXN1
DMI_TXN_2 AM40 DMI_RXN2
DMI_TXN_3 AM44 DMI_RXN3
DMI_RXN[3:0] <13>
DMI_TXP_0 AJ47 DMI_RXP0
DMI_TXP_1 AJ42 DMI_RXP1
DMI_TXP_2 AM39 DMI_RXP2
DMI_TXP_3 AM43 DMI_RXP3
DMI_RXP[3:0] <13>

CFG
<2> MCH_BSEL0 P27 CFG_0
<2> MCH_BSEL1 N27 CFG_1
<2> MCH_BSEL2 N24 CFG_2
CFG_3
CFG_4
CFG_5
CFG_6
CFG_7
CFG_8
CFG_9
CFG_10
CFG_11
CFG_12
CFG_13
CFG_14
CFG_15
CFG_16
CFG_17
CFG_18
CFG_19
CFG_20
T30 MCH_CFG_3 C21
T75 MCH_CFG_4 C23
MCH_CFG_5 F23
T34 MCH_CFG_6 N23
T24 MCH_CFG_7 G23
T29 MCH_CFG_8 J20
MCH_CFG_9 C20
T37 MCH_CFG_10 R24
T28 MCH_CFG_11 L23
MCH_CFG_12 J23
MCH_CFG_13 E23
MCH_CFG_14 E20
T25 MCH_CFG_15 K23
T27 MCH_CFG_16 M20
T32 MCH_CFG_17 M24
T40 MCH_CFG_18 L32
MCH_CFG_19 N33
MCH_CFG_20 L35

GRAPHICS VID
GFX_VID_0 E35 MCH_GFX_VID_0 T41
GFX_VID_1 A39 MCH_GFX_VID_1 T42
GFX_VID_2 C38 MCH_GFX_VID_2 T43
GFX_VID_3 B39 MCH_GFX_VID_3 T44
GFX_VR_EN E36 R183 *0_4 SUSB# <14,31>

PM
<14> PM_BMBUSY# R184 0_4 PM_BMBUSY#_R G41 PM_BM_BUSY#
<3,12,34> ICH_DPRSTP# R177 0_4 ICH_DPRSTP#_R L39 PM_DPRSTP#
<16> PM_EXTTS#0 R401 0_4 PM_EXTTS#0_R L36 PM_EXT_TS#_0
<16> PM_EXTTS#1 R150 0_4 PM_EXTTS#1_R J36 PM_EXT_TS#_1
<3,14,34> DELAY_VR_PWRGOOD AW49 PWROK
<13> PLTRST#_NB R140 100_4 RST_IN#_MCH AV20 RSTIN#
<3,12> PM_THRMTRIP# R130 *0_4 PM_THRMTRIP#_GMCH N20 THERMTRIP#
<14,34> PM_DPRSLPVR R407 0_4 PM_DPRSLPVR_GMCH G36 DPRSLPVR

ME
CL_CLK AM49 CL_CLK0 <14>
CL_DATA AK50 CL_DATA0 <14>
CL_PWROK AT43 MPWROK <14,31>
CL_RST# AN49 CL_RST#0 <14>
CL_VREF AM50 +1.25V_CL_VREF

MISC
NC_1 BJ51
NC_2 BK51
NC_3 BK50
NC_4 BL50
NC_5 BL49
NC_6 BL3
NC_7 BL2
NC_8 BK1
NC_9 BJ1
NC_10 E1
NC_11 A5
NC_12 C51
NC_13 B50
NC_14 A50
NC_15 A49
NC_16 BK2
SDVO_CTRL_CLK H35
SDVO_CTRL_DATA K36
CLK_REQ# G39 CLK_MCH_OE#
ICH_SYNC# G40 MCH_ICH_SYNC# <14>
TEST_1 A37 GMCH_TEST1 R178 0_4
TEST_2 R32 GMCH_TEST2 R168 20K_4

CRESTLINE_1p0

+3V
R170 10K_4 CLK_MCH_OE#
R395 10K_4 PM_EXTTS#0
R149 10K_4 PM_EXTTS#1

MCH_CFG_5 R138 *4.02K/F_4
MCH_CFG_9 R127 *4.02K/F_4
MCH_CFG_12 R139 *4.02K/F_4
MCH_CFG_13 R137 *4.02K/F_4
MCH_CFG_16 R129 *4.02K/F_4

+3V
MCH_CFG_19 R171 *4.02K/F_4
MCH_CFG_20 R174 *4.02K/F_4

+1.25V
R422 1K/F_4
C559 .1U/10V_4
R420 392/F

+SMDDR_VREF
+1.8VSUS
R416 *1K/F_4
R417 BK1608LL121
+SM_VREF_MCH
R418 *1K/F_4
C295 .1U/10V_4
C143 1U/10V_4

+1.8VSUS R154 1K/F_4 SM_RCOMP_VOH
R165 3.01K/F_4 C241 .01U/16V_4 C232 2.2U/6.3V
SM_RCOMP_VOL
R163 1K/F_4 C250 .01U/16V_4 C233 2.2U/6.3V

+1.25V
CLK_DREFCLK R409 *4.7K_4
CLK_DREFCLK# R529 EV@0_4
R531 EV@0_4
CLK_DREFSSCLK R411 *4.7K_4
CLK_DREFSSCLK# R532 EV@0_4
R533 EV@0_4
DC Delete R410 and R408 0110

INTEL FAE suggest PD for external graphics

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Quanta Computer Inc.

Size	Document Number	Rev
	GMCH (STRAPPING/OTHER 3/7)	E
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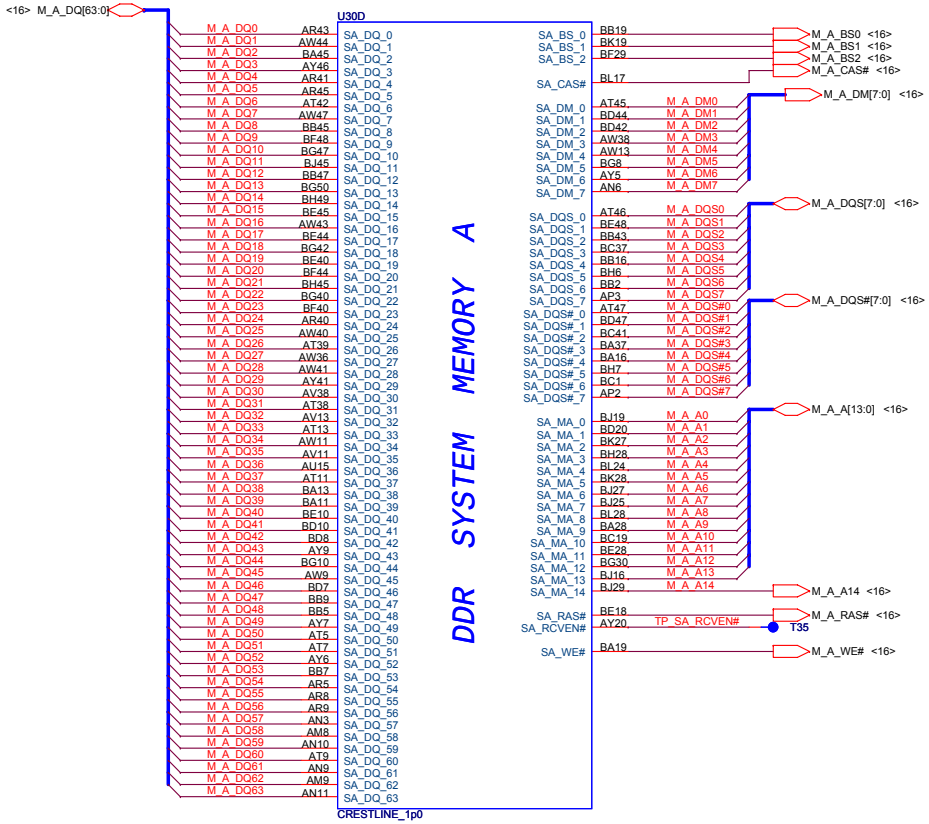
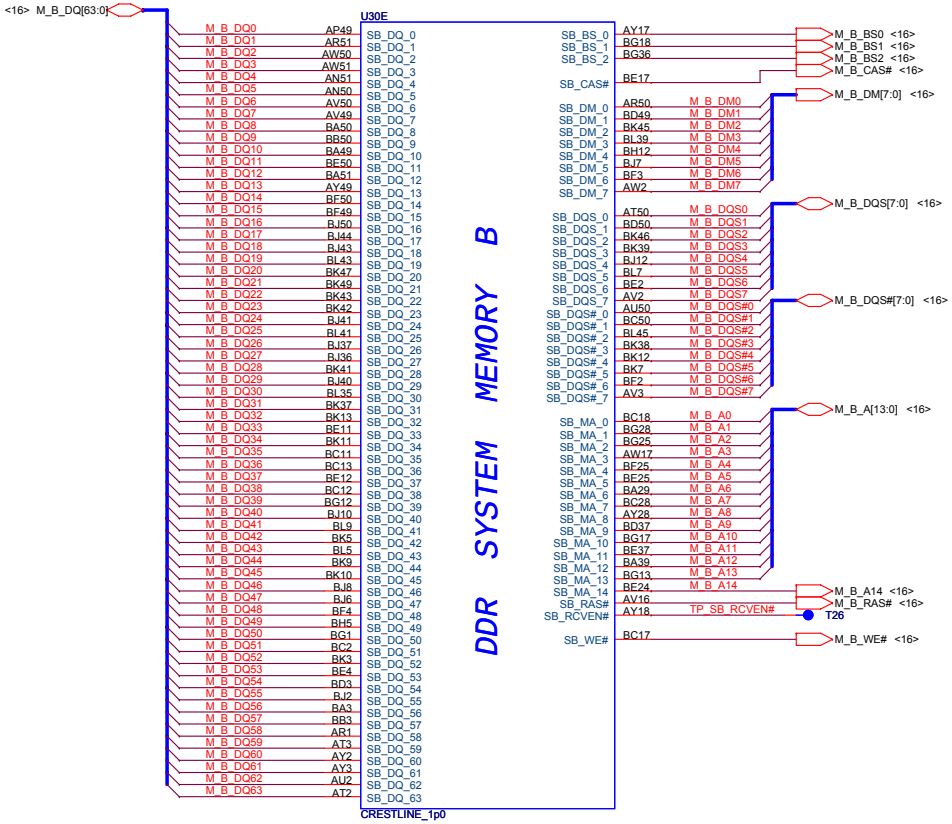
NB(Memory controller)





PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH DDR(4/7)	E
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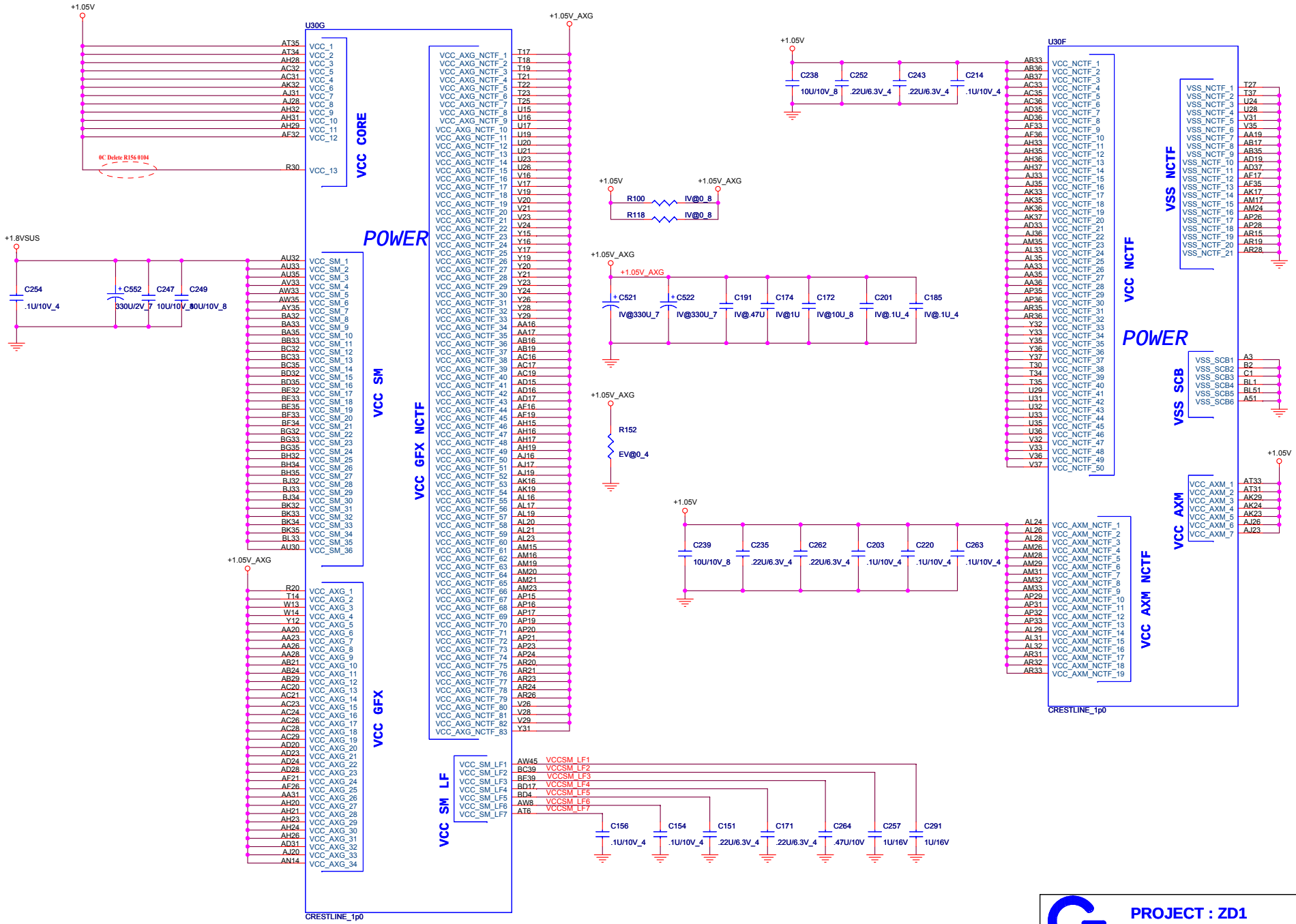
NB(Power-1)



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	GMCH Power-1(5/7)	E
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NB(Power-2)

CRT/TV Disable/Enable guideline

External VGA with EV@part, Internal VGA with IV@ part

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

External VGA with EV@part,Internal VGA with IV@ part

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V

EXTERNAL / INTERNAL

<FAE>
INT VGA disable
VCCSYNC connect to GND

IV&EV Dis/Enable setting

CRB RECOMMEND
180OHM@100MHz
Rdc= 0.09OHM (max)

IV&EV Dis/Enable setting

<FAE>
INT VGA disable
VCCD_TVDAC still +1.5V

Change to
100 ohm Resistor

Use site for filter cap with Gfx enabled CS

IV&EV Dis/Enable setting

<FAE>
VCC_RXR_DMI and VCC_PEG connect to+1.05V

<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

CRESTLINE_1p0

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Quanta Computer Inc.

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	GMCH Power-2(6/7)	E

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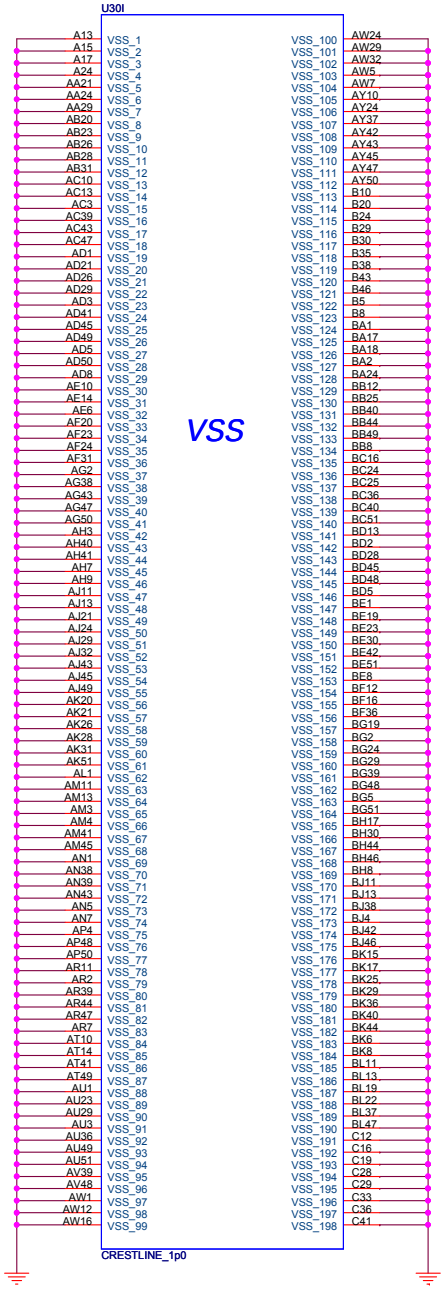
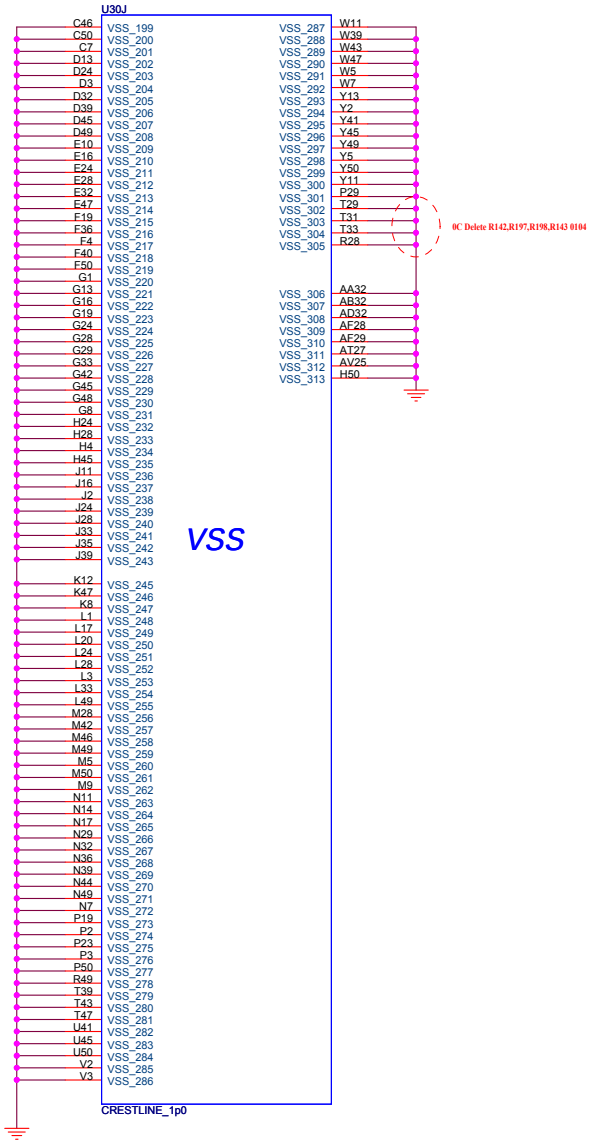
NB(Power-3)





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	GMCH Power-3(7/7)	E
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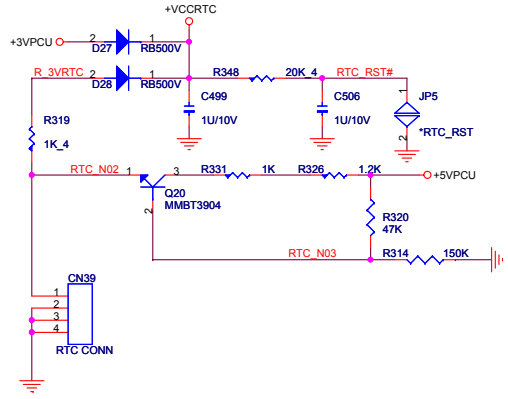
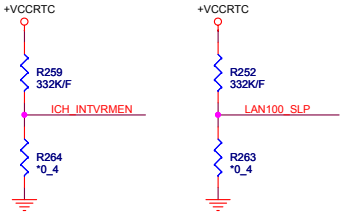
RTC

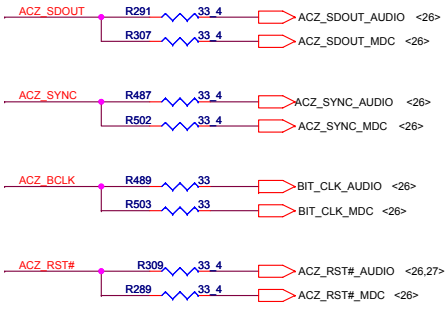


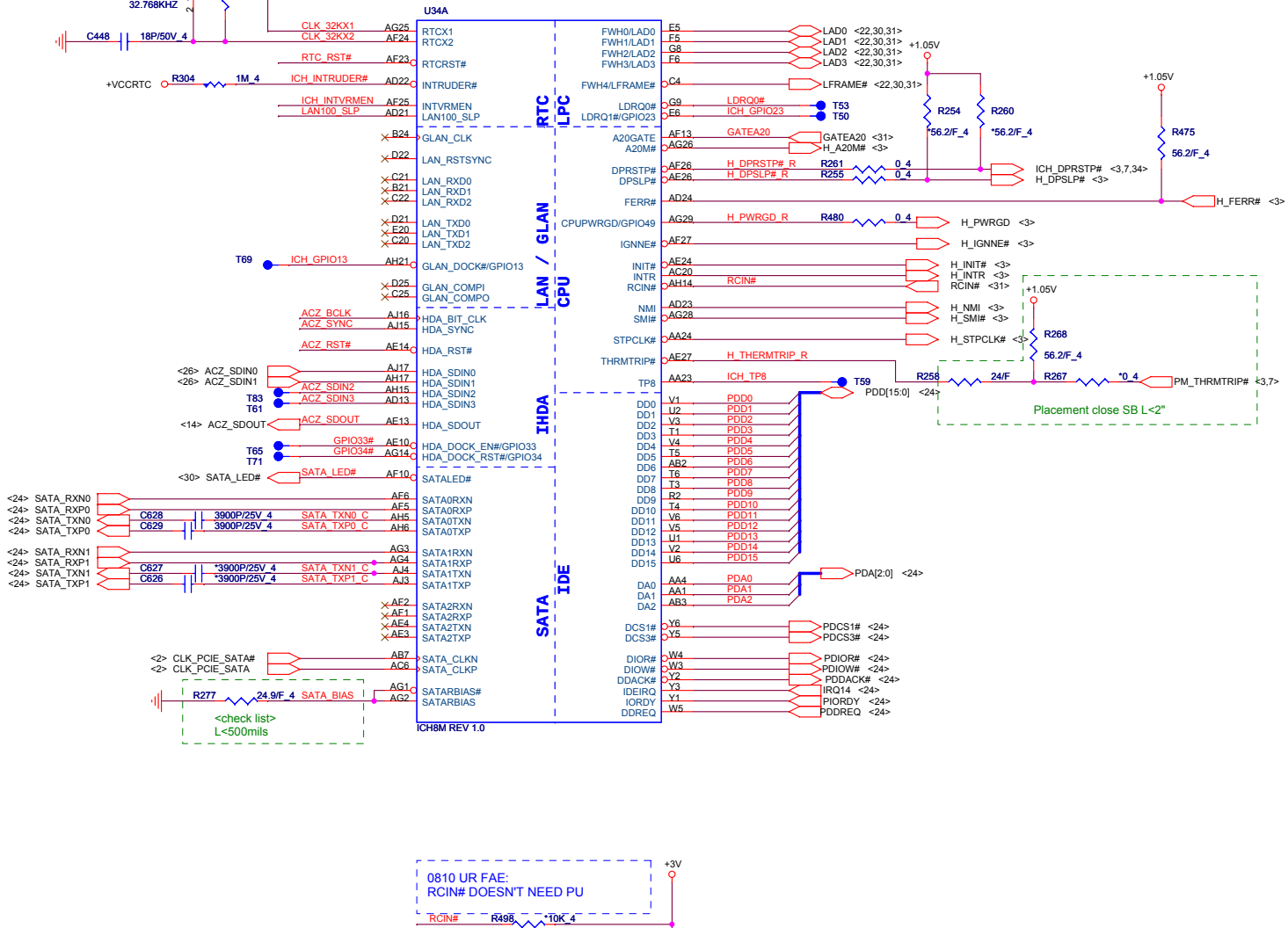
SB Strap

INTVRMEN	Low = Internal VR disable High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



HDA





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	ICH8M HOST(1/4)		E
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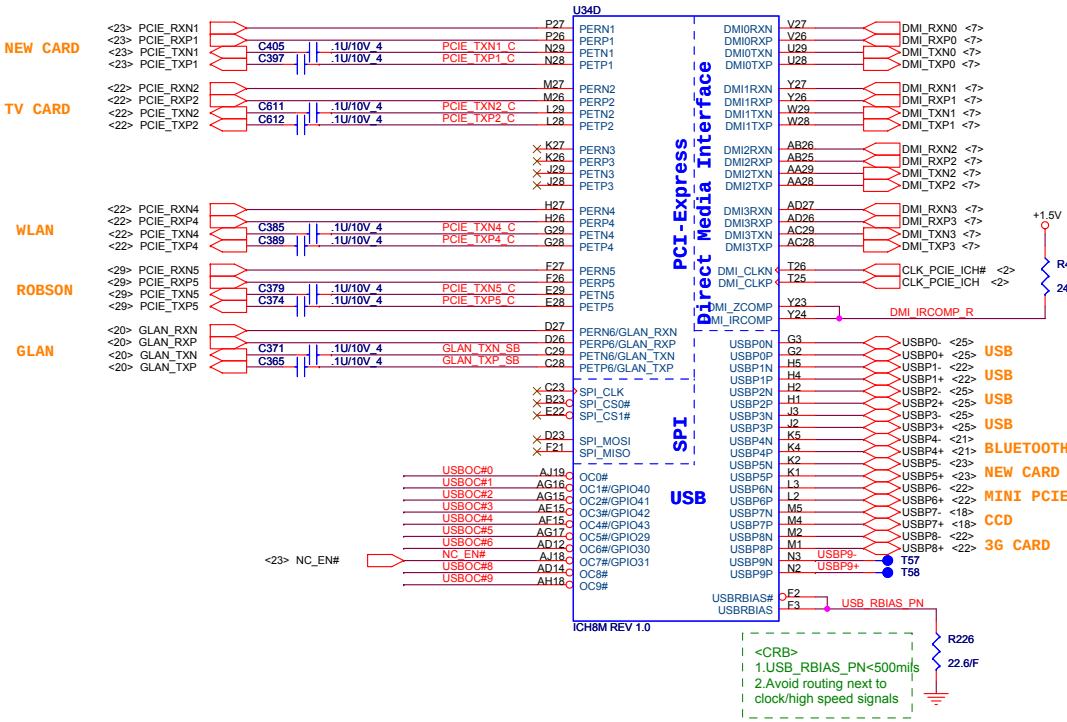
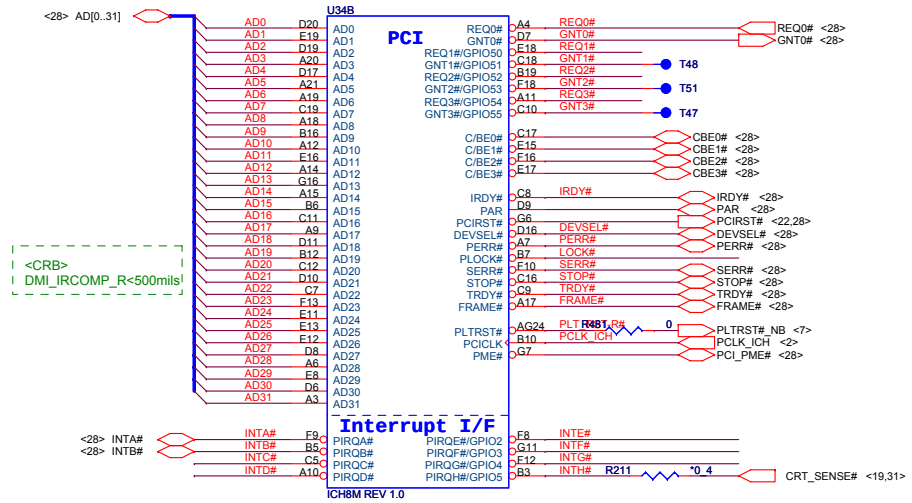
SB-PCIE/USB/DMI

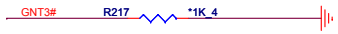


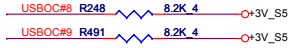
SB-PCI

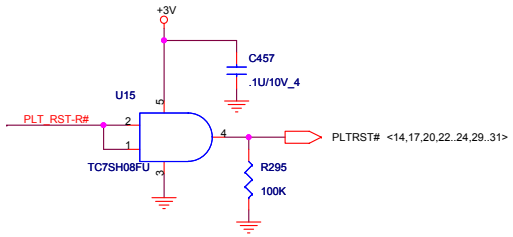


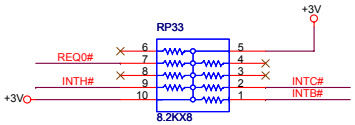
A16 SWAP Override strap

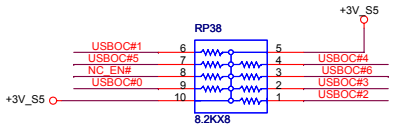
PCI_GNT#3	Low = A16 swap override enabled High = Default

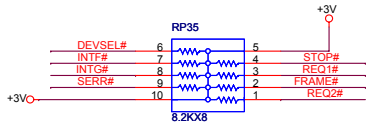


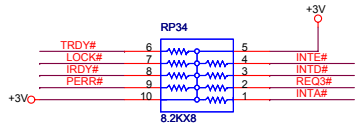












PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M PCIE\PCI\USB(2/4)	E

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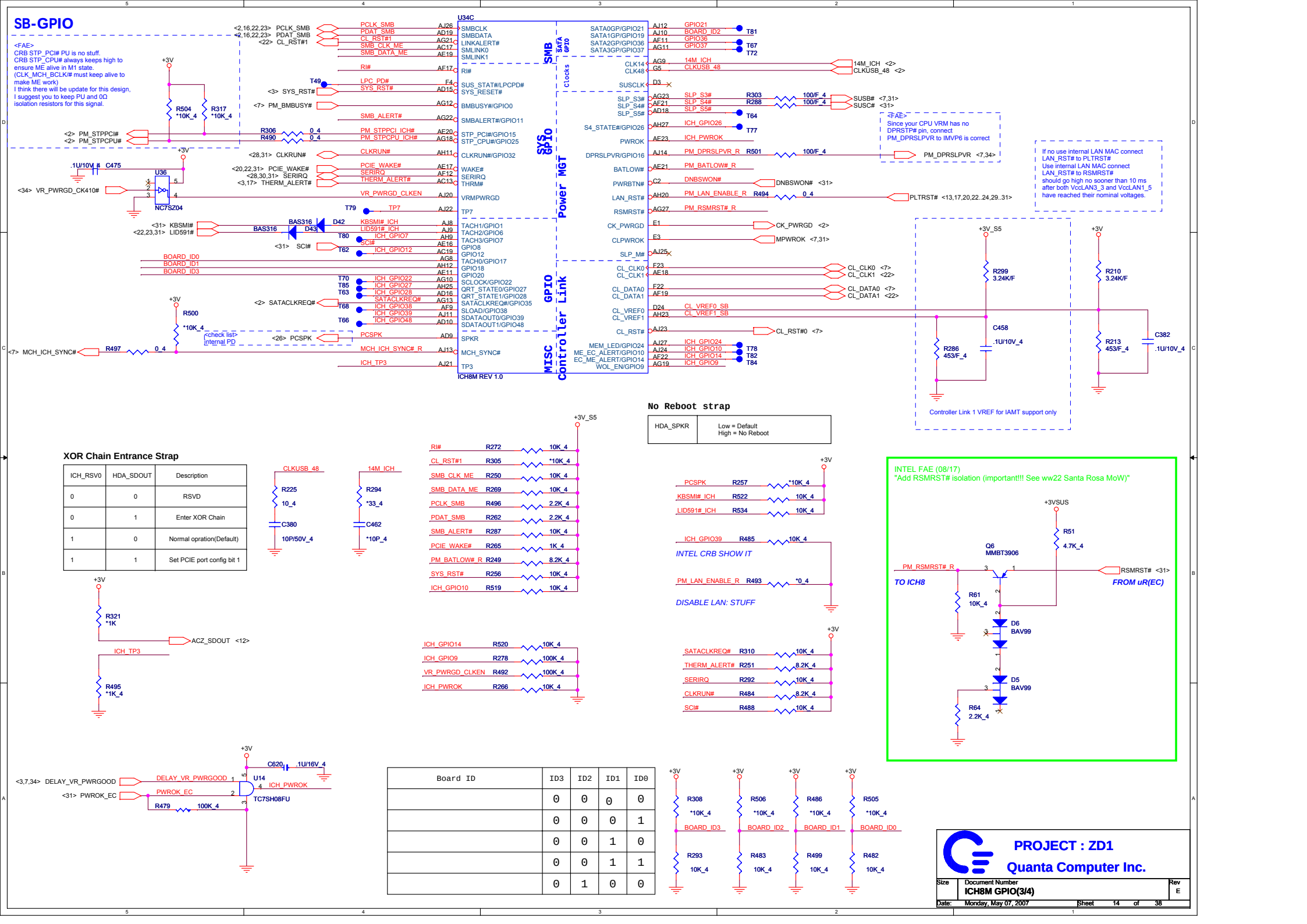
SB-GPIO



No Reboot strap

HDA_SPKR	Low = Default High = No Reboot

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

Board ID	ID3	ID2	ID1	ID0
	0	0	0	0
	0	0	0	1
	0	0	1	0
	0	0	1	1
	0	1	0	0

PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	ICH8M GPIO(3/4)	E
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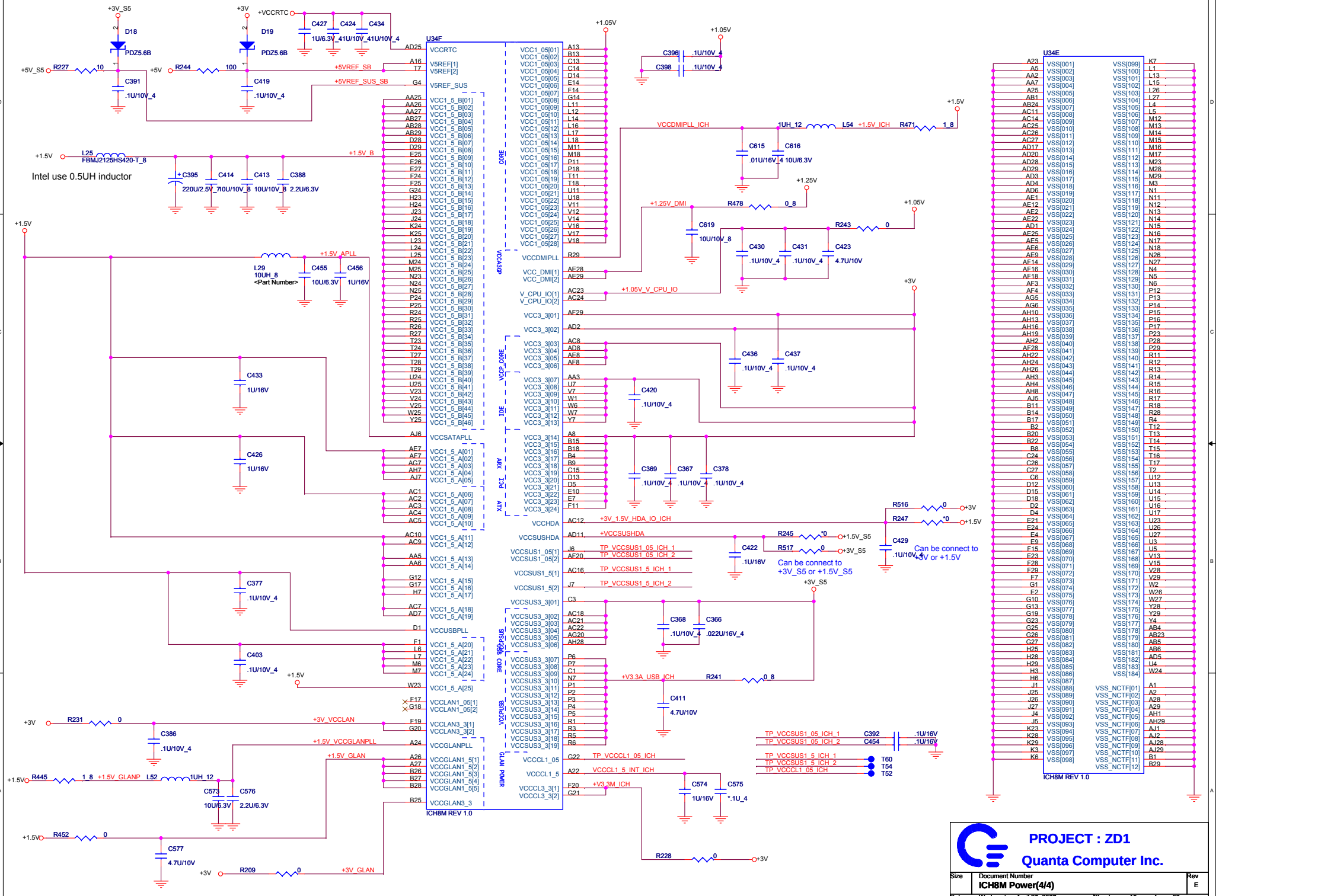
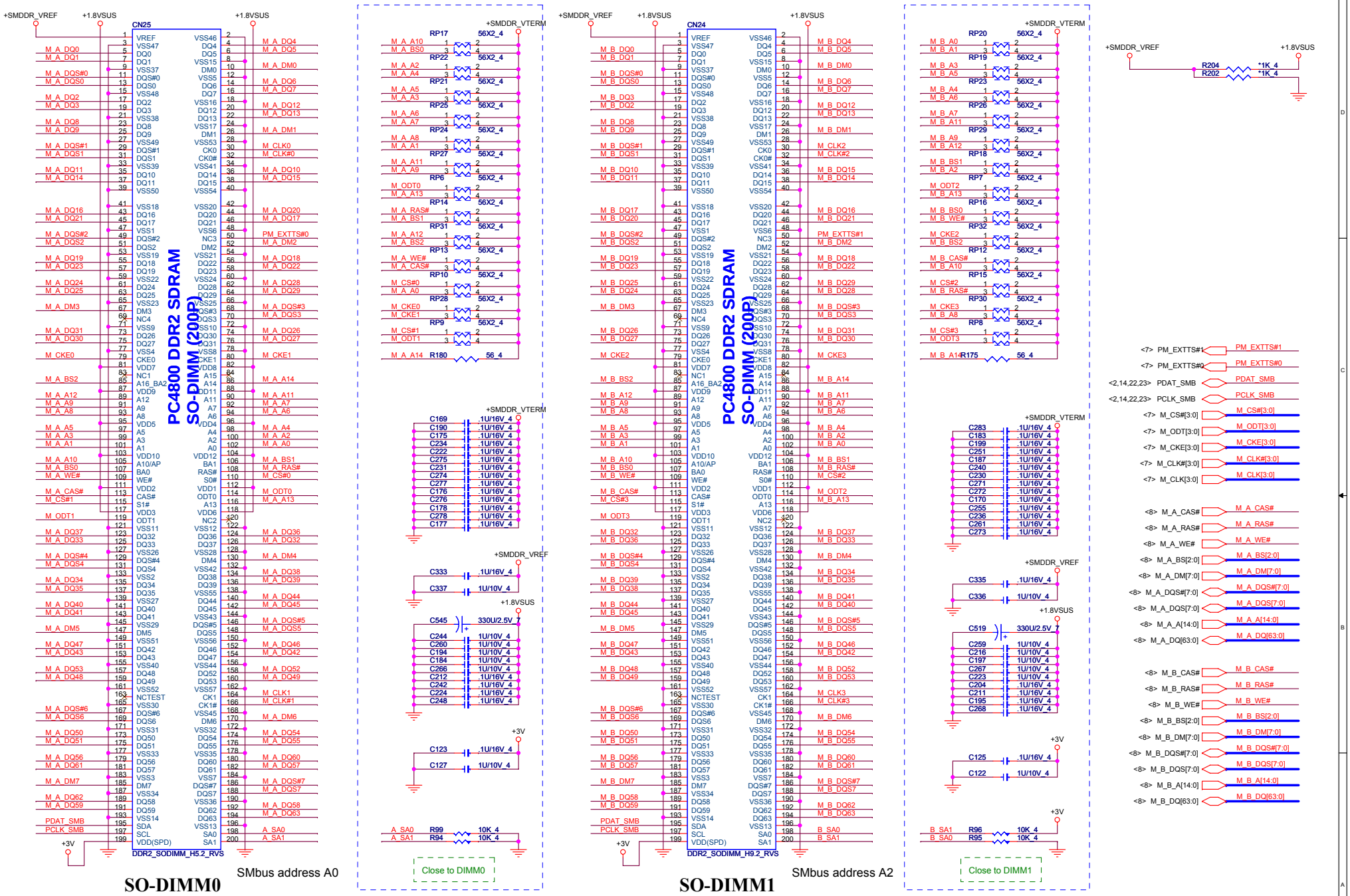

U34F
ICH8M REV 1.0
U34E
ICH8M REV 1.0
Intel use 0.5UH inductor
PROJECT : ZD1
Quanta Computer Inc.
Size
Document Number
ICH8M Power(4/4)
Rev
E
Date: Wednesday, April 25, 2007
Sheet 15 of 38


CN25
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM_H5.2_RVS
+SMDDR_VREF
+1.8VSUS
+3V
+SMDDR_VTERM
SO-DIMM0
SMbus address A0
Close to DIMM0
CN24
PC4800 DDR2 SDRAM
SO-DIMM (200P)
DDR2_SODIMM_H9.2_RVS
SO-DIMM1
SMbus address A2
Close to DIMM1
PROJECT : ZD1
Quanta Computer Inc.
DDRII SO-DIMM
Monday, May 07, 2007
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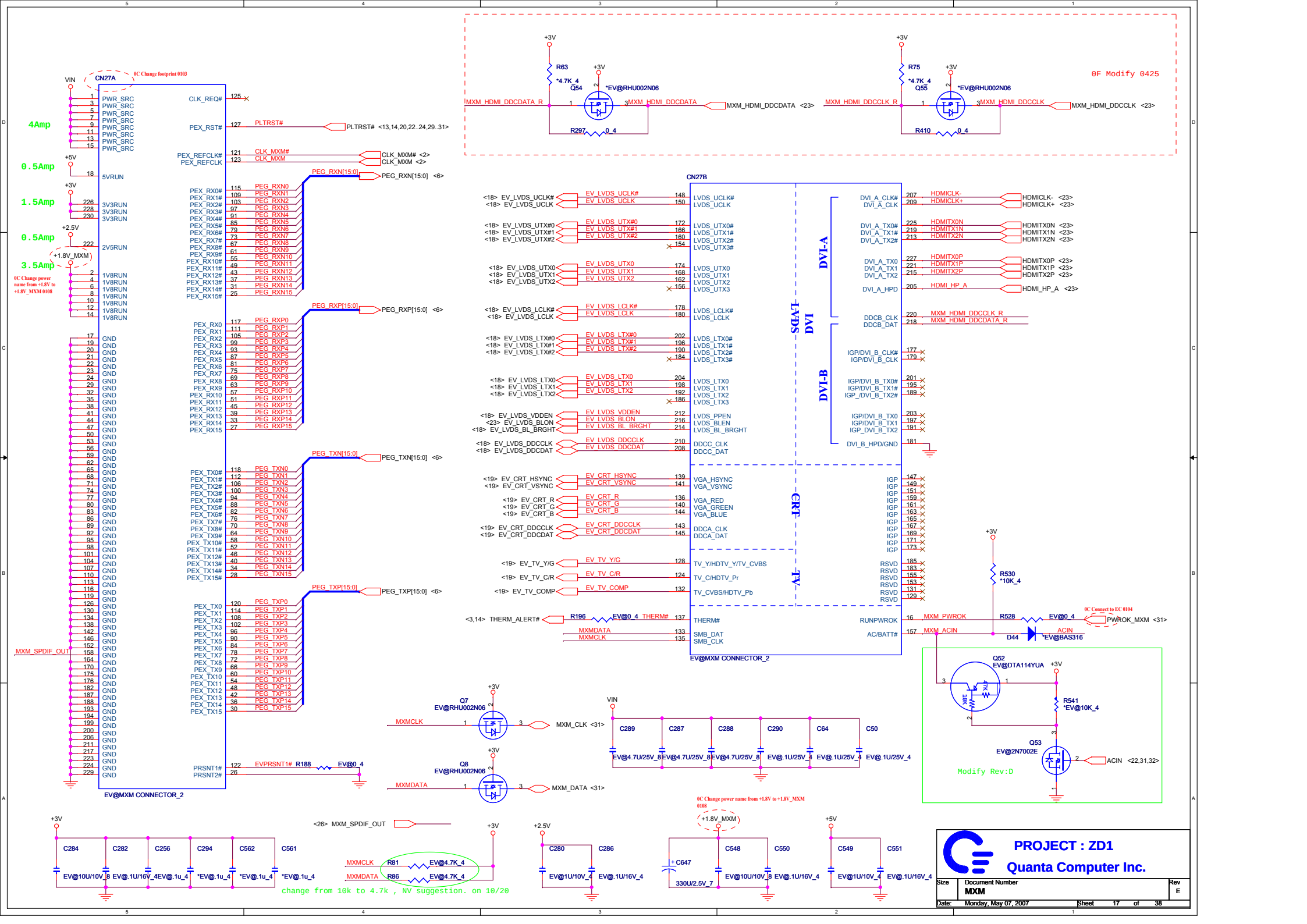
CN27A
0C Change footprint 0103
EV@MXM CONNECTOR_2
CN27B
EV@MXM CONNECTOR_2
LVDS
DVI
DVI-A
DVI-B
CRT
TV
0F Modify 0425
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
0C Change power name from +1.8V to +1.8V_MXM 0108
Modify Rev:D
change from 10k to 4.7k , NV suggestion. on 10/20
PROJECT : ZD1
Quanta Computer Inc.
Size
Document Number
MXM
Rev
E
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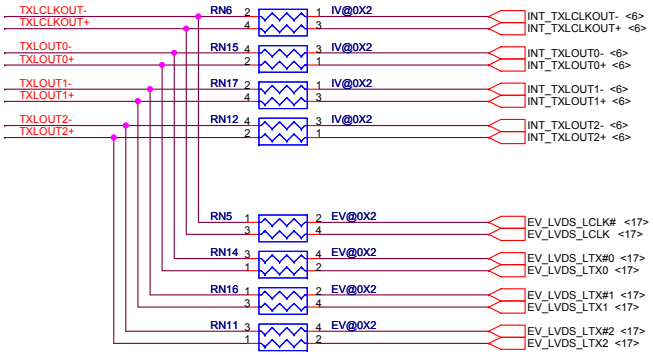
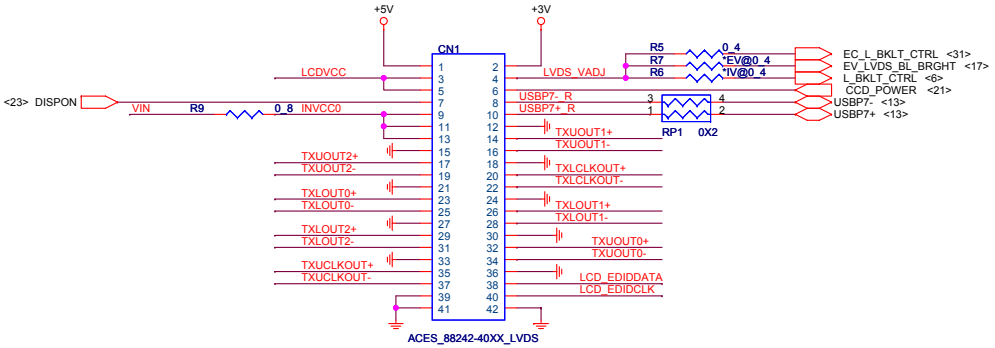
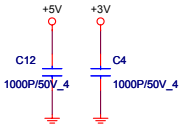
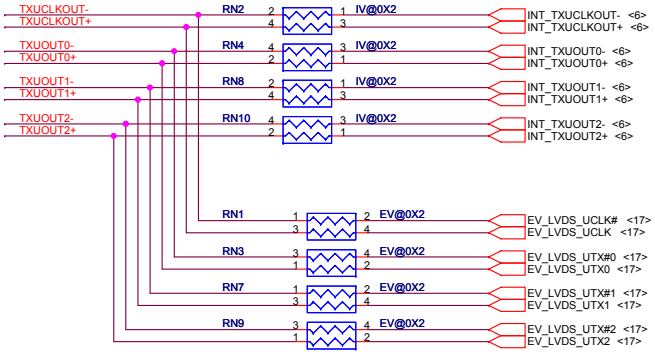
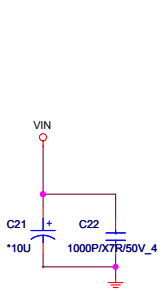
LVDS

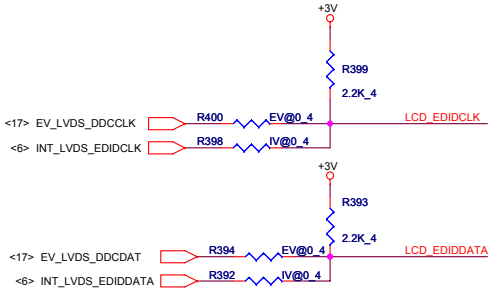


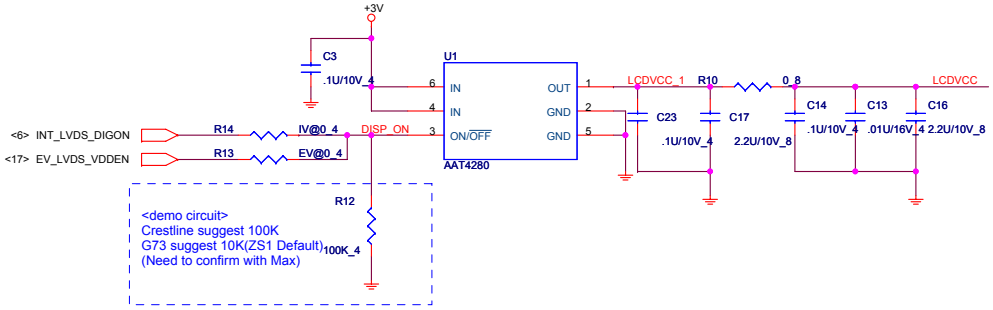












PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	LVDS	E
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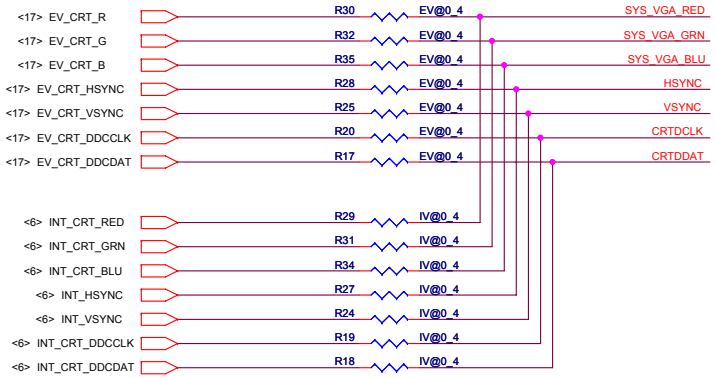
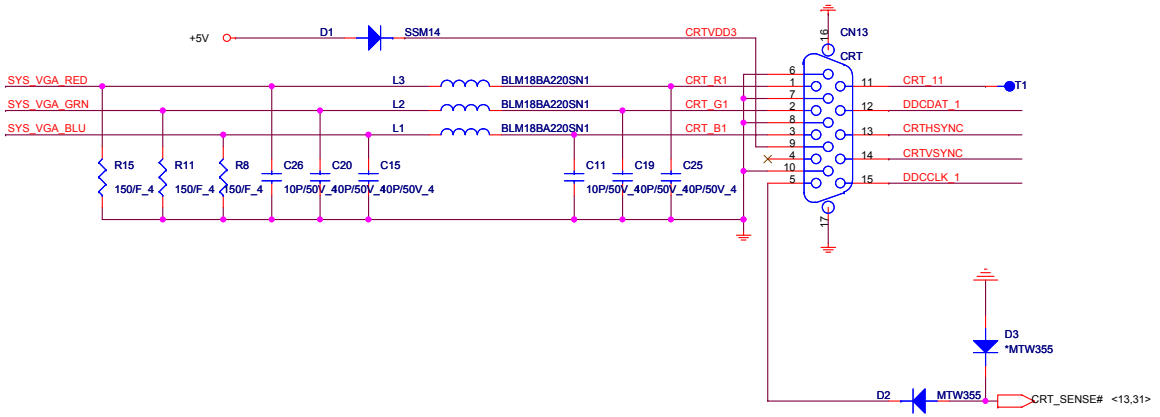
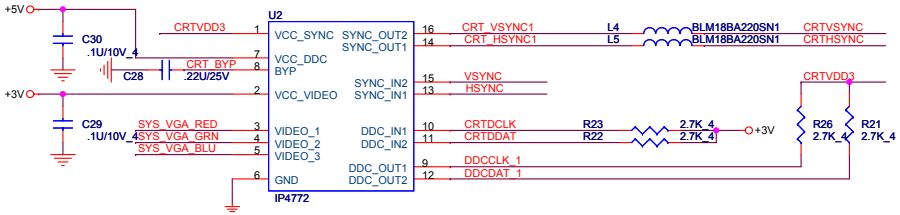
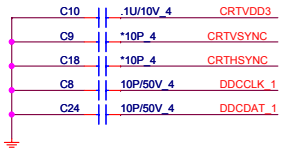
CRT Select



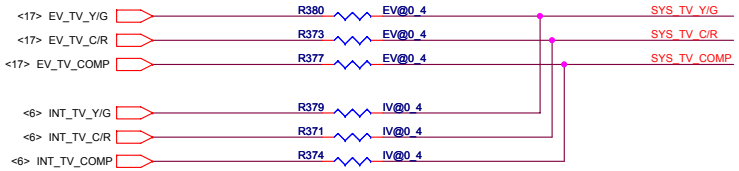
CRT CONNECTOR AND ESD

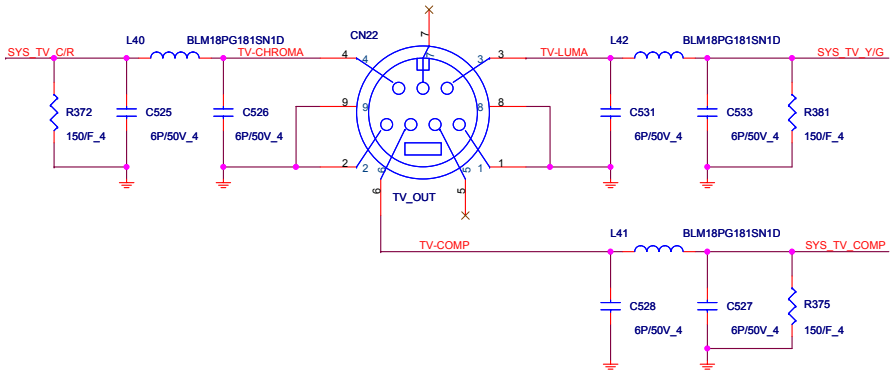


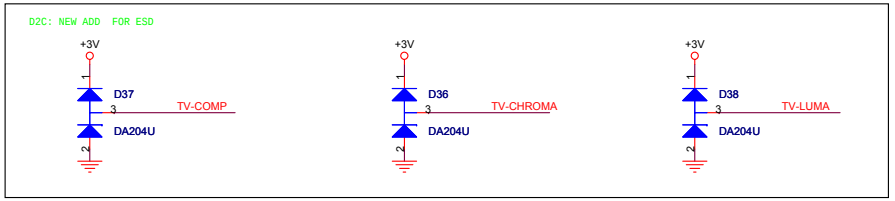




TV Out (SVHS) MiniDIN 7-pin







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Quanta Computer Inc.

Size	Document Number	Rev
	CRT/TVOUT	E
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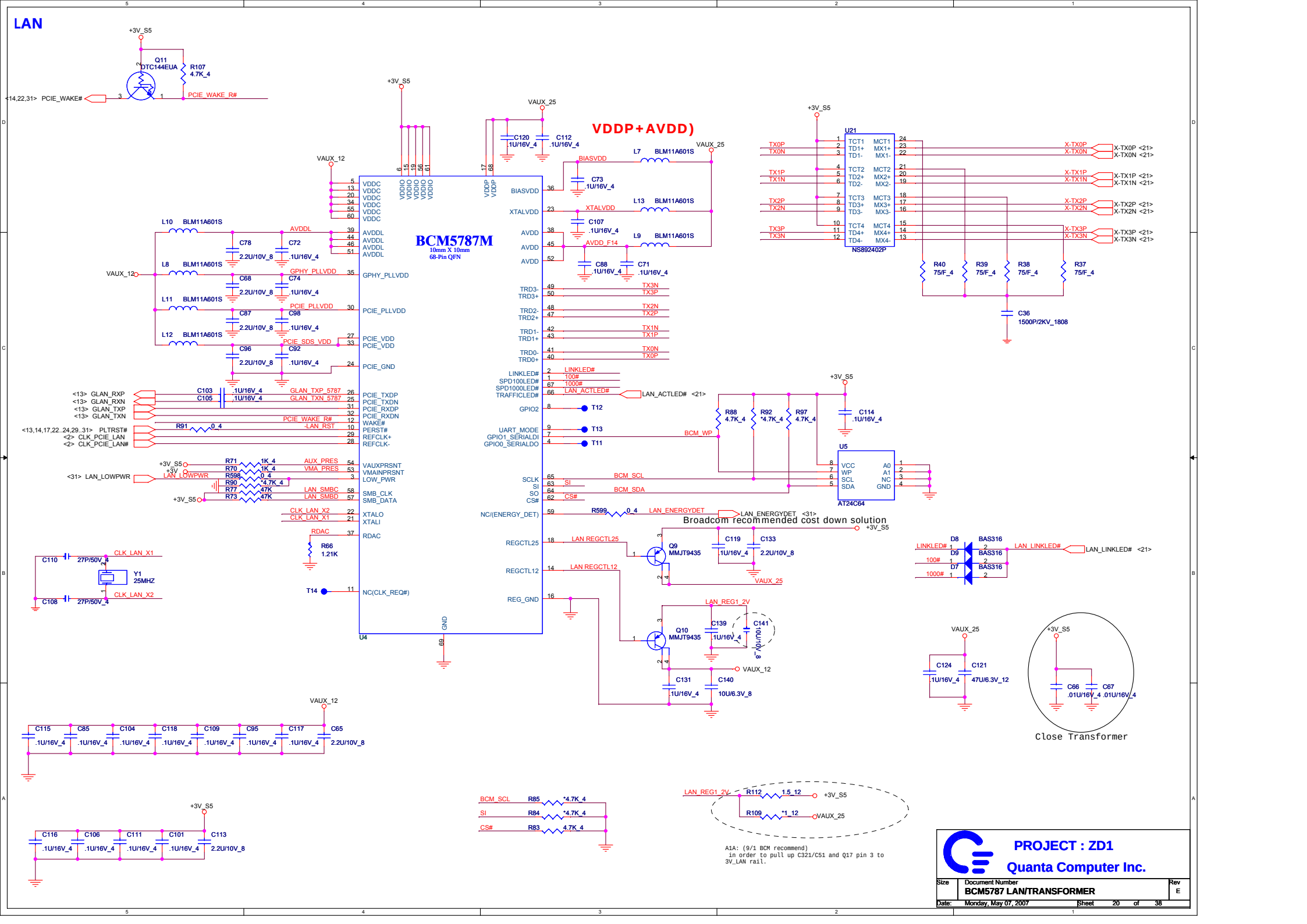
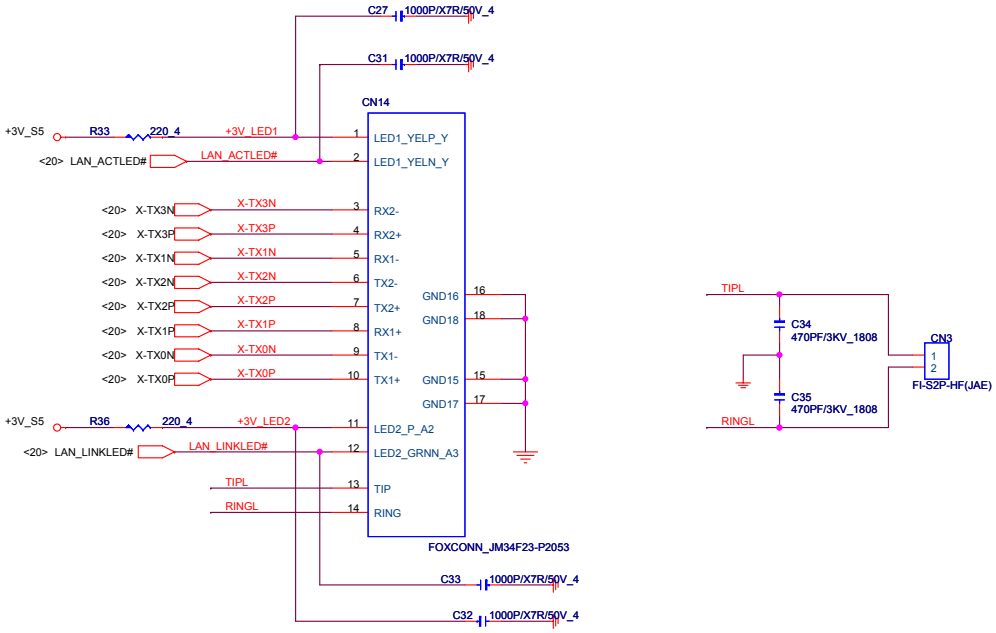
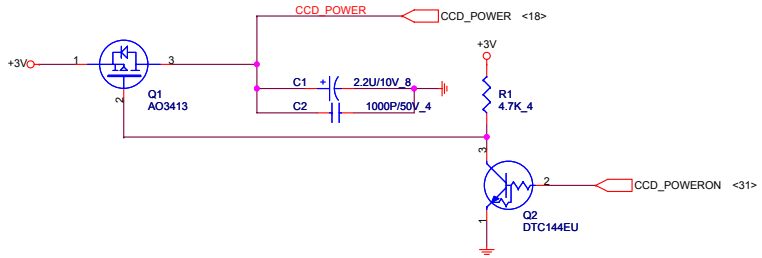
LAN


BCM5787M
10mm X 10mm
68-Pin QFN
U4
VDDP+AVDD)
Broadcom recommended cost down solution
Close Transformer
U21
NS892402P
U5
AT24C64
Q11
DTC144EUA
Q9
MMJT9435
Q10
MMJT9435
Y1
25MHZ
PROJECT : ZD1
Quanta Computer Inc.
BCM5787 LAN/TRANSFORMER
Monday, May 07, 2007
A1A: (9/1 BCM recommend)
in order to pull up C321/C51 and Q17 pin 3 to
3V_LAN rail.

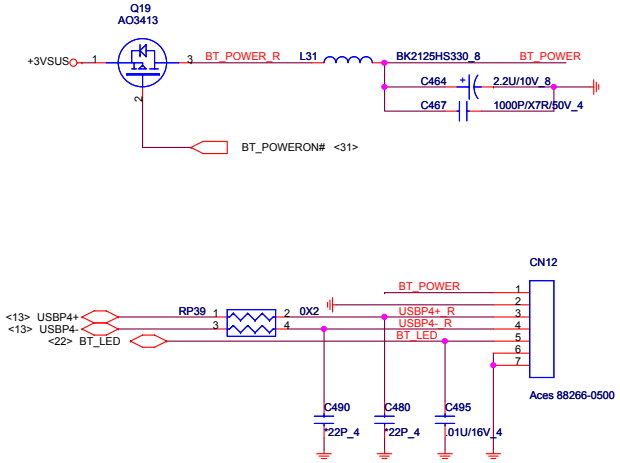
RJ45-11



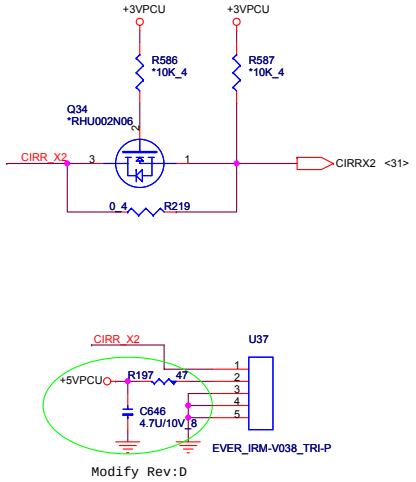
CAMERA MODULE CONNECTOR



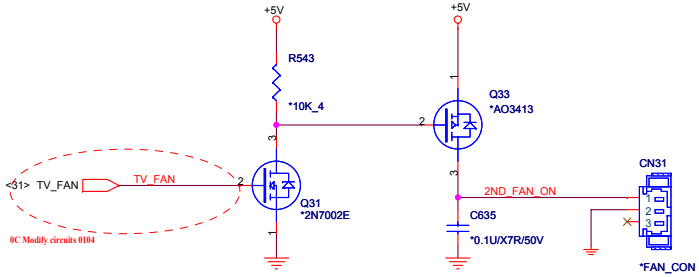
BLUETOOTH MODULE CONNECTOR

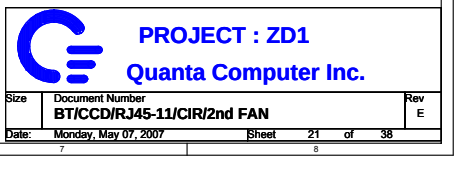


CIR

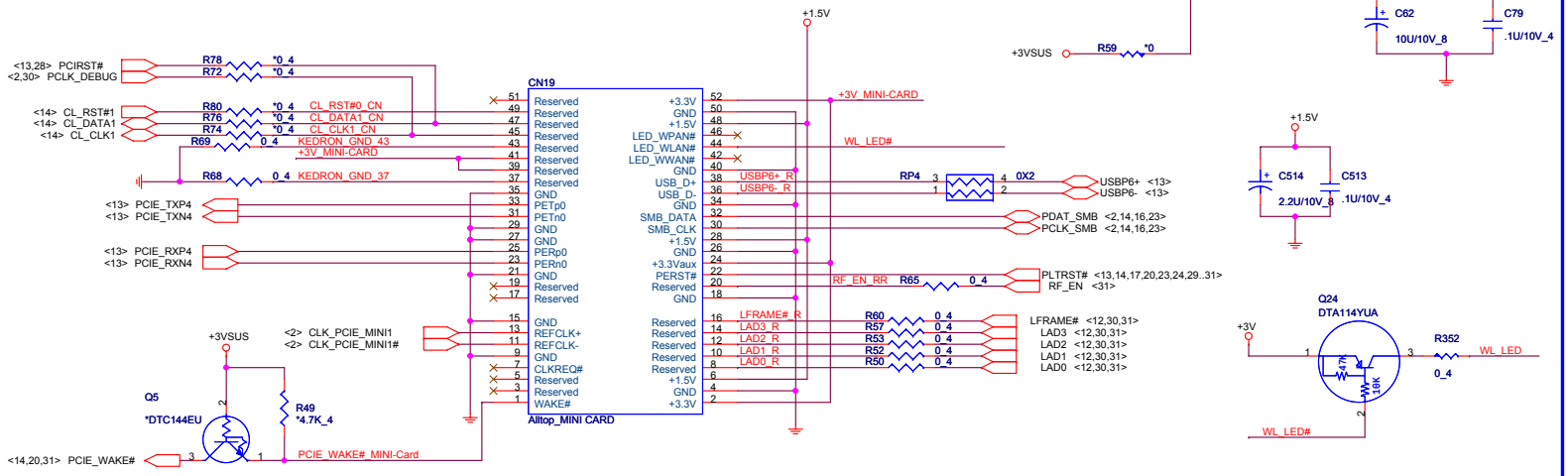


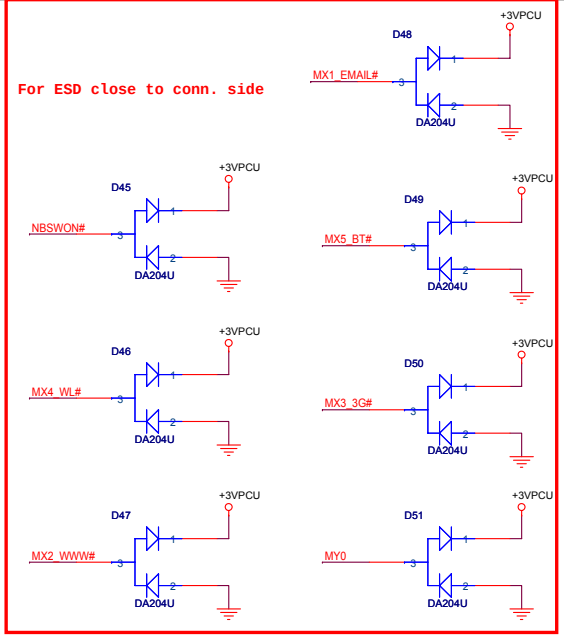
2nd FAN



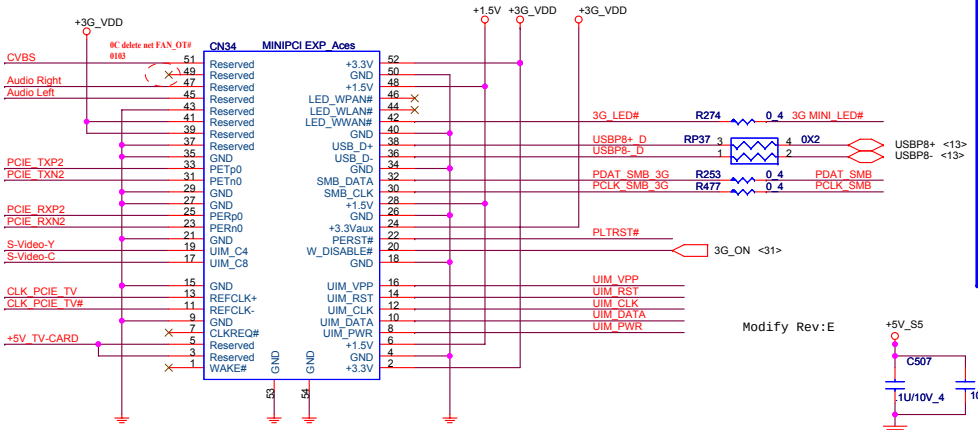


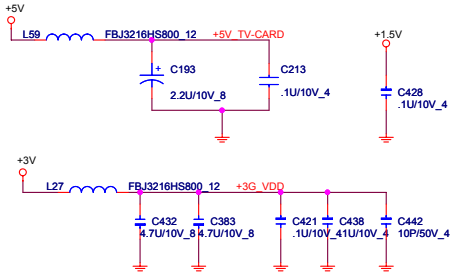
MINI-Card

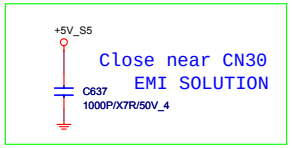


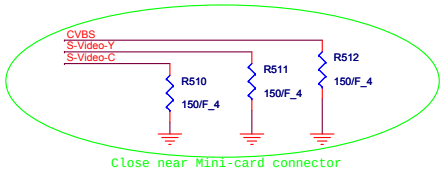


3G/TV MINI CARD

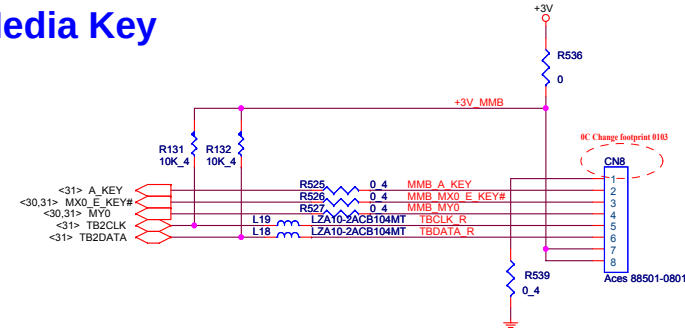


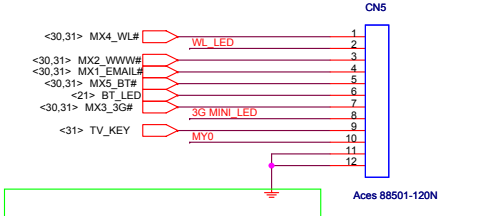


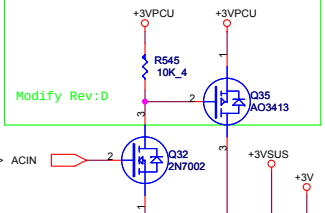


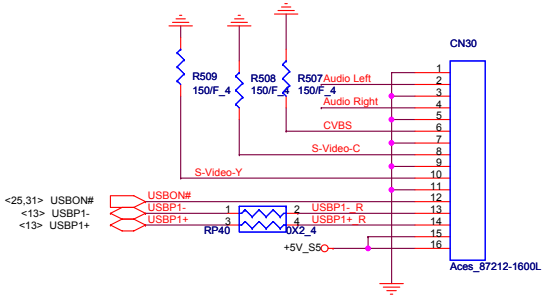


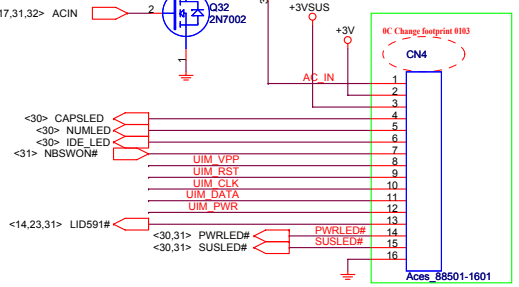
Media Key

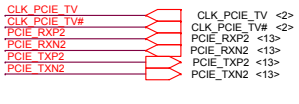












	PROJECT : ZD1		
	Quanta Computer Inc.		
Size	Document Number		Rev
	MINI PCI-E card/3G/TV/Media Key		E
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New card

CN9

<13> PCIE_TXP1
<13> PCIE_TXN1
<13> PCIE_RXP1
<13> PCIE_RXN1
<2> CLK_PCIE_NEW_C
<2> CLK_PCIE_NEW_C#
<13> NC_EN#
C381
C376
PERP3
PERN3
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
<13> USBP5+
<13> USBP5-
R441 0_4 USBP5+_R
R442 0_4 USBP5-_R

GND5 GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND6 GND27 GND28

*Aces_NEW CARD

CN44

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30 GND27 GND28

*Taitwun_NEW CARD

CN43

PCIE_TXP1
PCIE_TXN1
PERP3
PERN3
CLK_PCIE_NEW_C
CLK_PCIE_NEW_C#
NC_EN#
+NEW_3V
PERST#
+NEW_3VAUX
+NEW_1.5V
NEW_SMDATA
NEW_SMCLK
USBP5+_R
USBP5-_R

GND1 PETp0 PETn0 GND2 PERp0 PERn0 GND3 REFCLK+ REFCLK- CPPE# CLKREQ# +3.3V1 +3.3V2 PERST# +3.3VAUX WAKE# +1.5V1 +1.5V2 SMB_DATA SMB_CLK RESERVED1 RESERVED2 CPUSB# USB_D+ USB_D- GND4 GND29 GND30 GND27 GND28

FOX_EXPCARD

NEW CARD'S POWER SWITCH

U33
QFN-TPS2231RGP

+3V
+3V_S5
+1.5V
PLTRST#_NEW

3.3VIN 3.3VOUT AUXIN AUXOUT 1.5VIN 1.5VOUT *SYSRST# *SHDN# *RCLKEN NC GND GNDPAD *STBY# *CPPE# *CPUSB# PERST# OC#

+NEW_3V 1.3A
+NEW_3VAUX 275mA
+NEW_1.5V 650mA
NC_EN#
PERST#

REV:B MODIFY

0C Connect to NC_EN# 0103

TI : AL002231001
RICOH : AL005538001
GMT : AL000577008

<13,14,17,20,22,24,29..31> PLTRST#
Q37 2N7002
PLTRST#_NEW

REV:B MODIFY

+3V_S5: C599 .1U/10V_4
+3V: C581 .1U/10V_4, C582 .1U/10V_4
+1.5V: C598 .1U/10V_4, C597 .1U/10V_4
+NEW_3VAUX: C351 .1U/10V_4
+NEW_3V: C579 2.2U/10V_8, C354 .1U/10V_4, C357 .1U/10V_4
+NEW_1.5V: C348 2.2U/10V_8, C344 .1U/10V_4

+NEW_3V
Q30 2N7002E
RP41 10KX2_4
<2,14,16,22> PDAT_SMB
NEW_SMDATA

+NEW_3V
Q29 2N7002E
<2,14,16,22> PCLK_SMB
NEW_SMCLK

LID SWITCH

+3V
R194 100K_4
<18> DISPON
DISPON
D11 BAS316
LID591# <14,22,31>

D10 BAS316
R190 IV@0_4
R189 EV@0_4
INT_LVDS_BLON <6>
EV_LVDS_BLON <17>
R192 *1K_4

R191 100K_4
<demo circuit>
Crestline suggest 100K
G73 suggest 10K(ZS1 Default)
(Need confirm with Max)

Q12 DTC144EU
EC_FPBACK# <31>

HDMI

+5V
D35 BAS316
D34 BAS316
NV suggestion near HDMI connector
R354 2K_4
R353 2K_4
<17> MXM_HDMI_DDCCLK
L39 220R_100MHZ
HDMI_DDCCLK
C515 *.1U_4
<17> MXM_HDMI_DDCDATA
L38 220R_100MHZ
HDMI_DDCDATA
C516 *.1U_4

+5V
C632 .1U/16V_4
C631 .1U/16V_4
C633 .1U/16V_4

CN21
0C Change footprint 0103

<17> HDMITX2P
<17> HDMITX2N
<17> HDMITX1P
<17> HDMITX1N
<17> HDMITX0P
<17> HDMITX0N
<17> HDMICLK+
<17> HDMICLK-
HDMI_DDCCLK
HDMI_DDCDATA
<17> HDMI_HP_A
R359 EV@10K_4
R602 1K_4
HP_DET
R356 EV@10K_4

SHELL1 D2+ D2 Shield D2- D1+ D1 Shield D1- D0+ D0 Shield D0- CK+ CK Shield CK- CE Remote NC DDC CLK DDC DATA GND +5V HP DET SHELL2 GND GND

HDMI CON

HDMI monitor default have PU to 5V.So ZY3 PD for level change.And serial R for current limited

U26 *RClamp0514M_AG
HDMITX0P HDMITX0N HDMI_HP_A VCC GND

U27 *RClamp0514M_AG
HDMITX2P HDMITX2N HDMITX1P HDMITX1N VCC GND

U25 *RClamp0514M_AG
HDMICLK+ HDMICLK- HDMI_DDCCLK HDMI_DDCDATA VCC GND

PROJECT : ZD1
Quanta Computer Inc.

Size	Document Number	Rev
	NEW CARD/HDMI/LID	E
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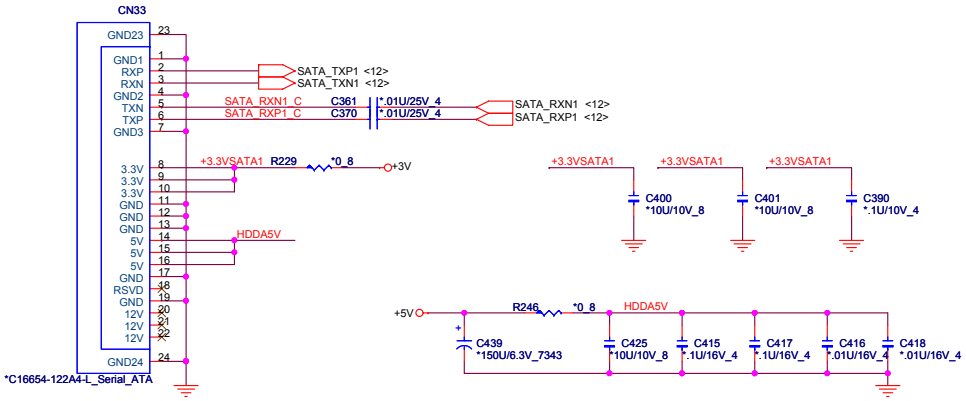
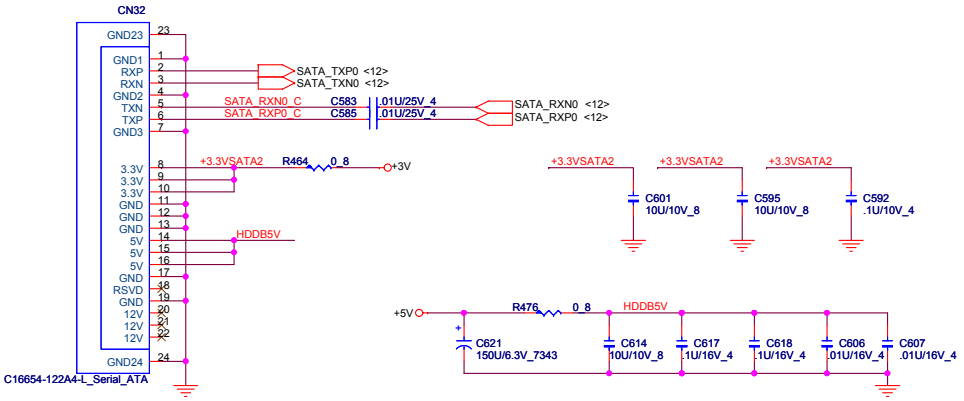
SATA HDD1

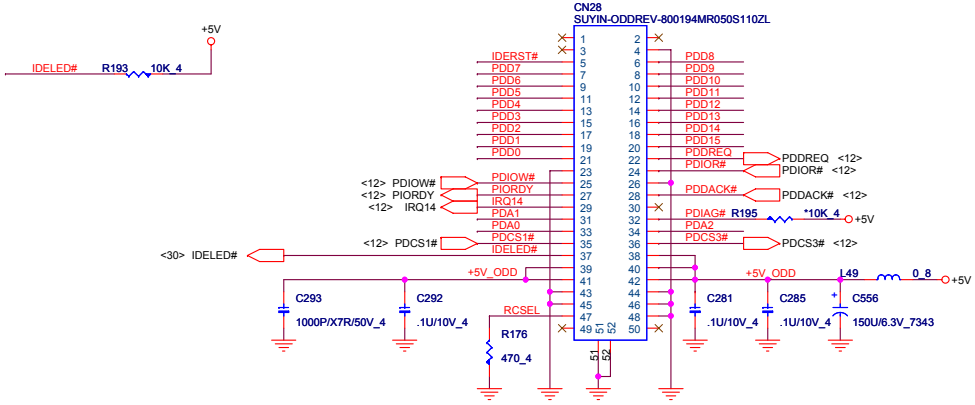


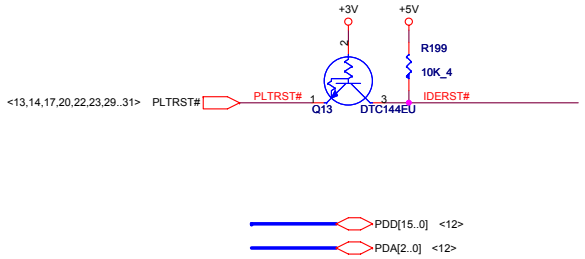
SATA HDD2

Main



ODD (PATA)





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Quanta Computer Inc.

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	SATA-HDD & PATA-ODD	E
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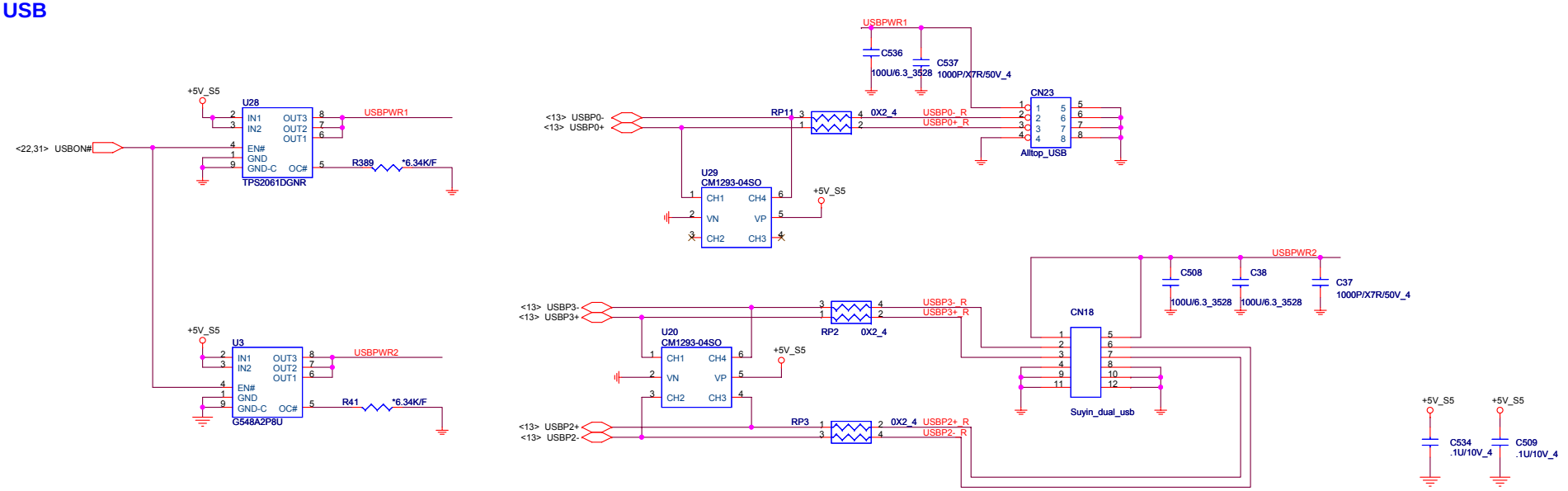
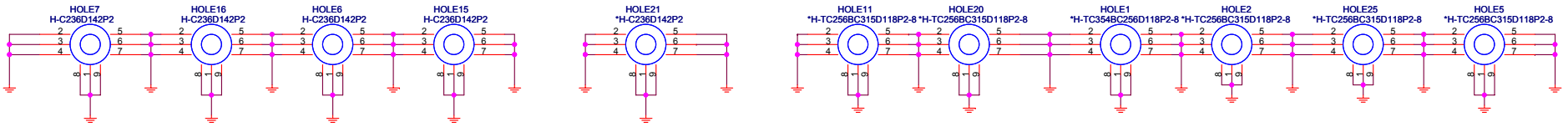
USB

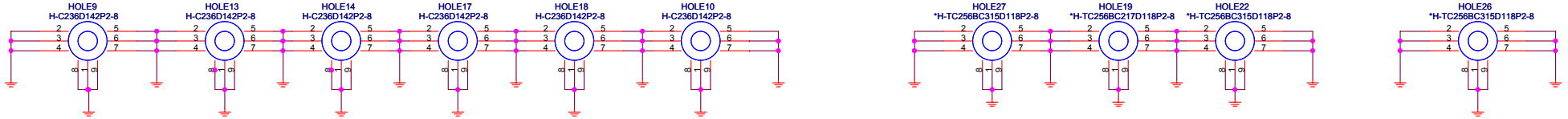


HOLES

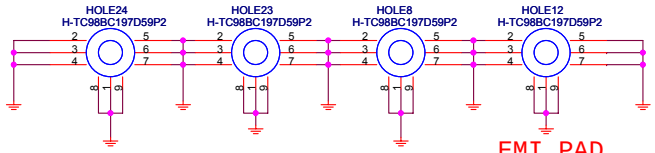
CPU NUT



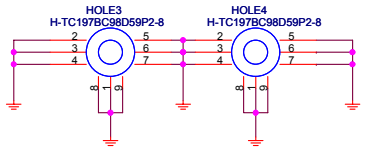
MXM NUT



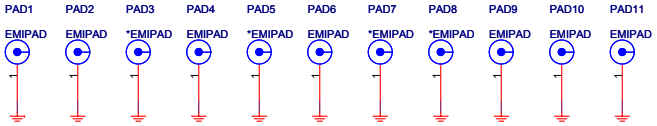
MINI CARD NUT

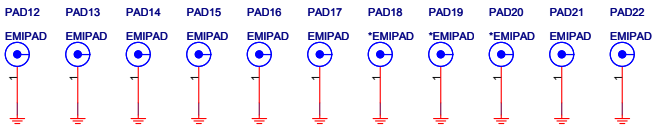


MDC NUT



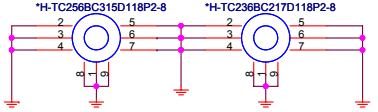
EMI PAD





Footprint error: PAD15 , PAD4 ,PAD16:
emipad97x87

Modify Rev:E



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Quanta Computer Inc.

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	USB/HOLE	E
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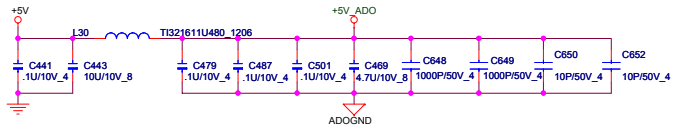
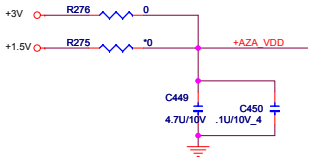
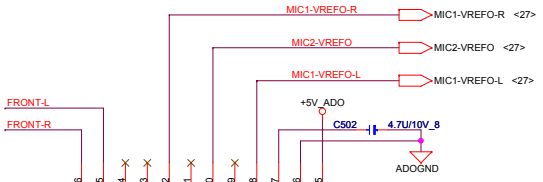
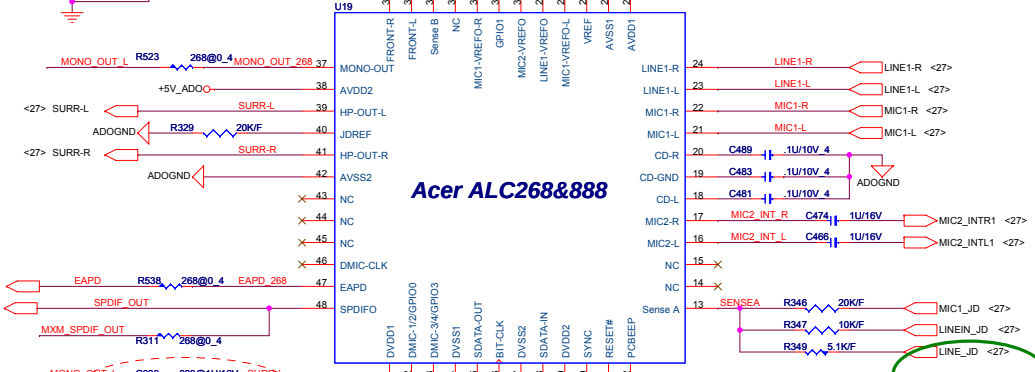
CODEC(ALC268)

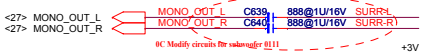




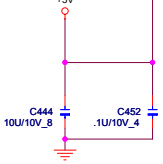


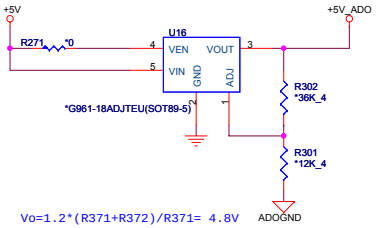


Acer ALC268&888

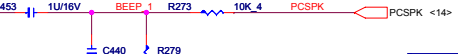


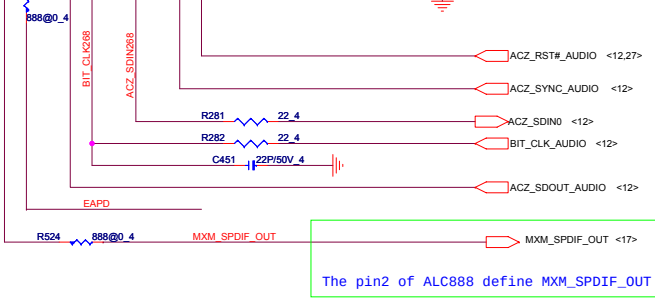
Tied at one point only
under the codec or
near the codec





Vo=1.2*(R371+R372)/R371= 4.8V

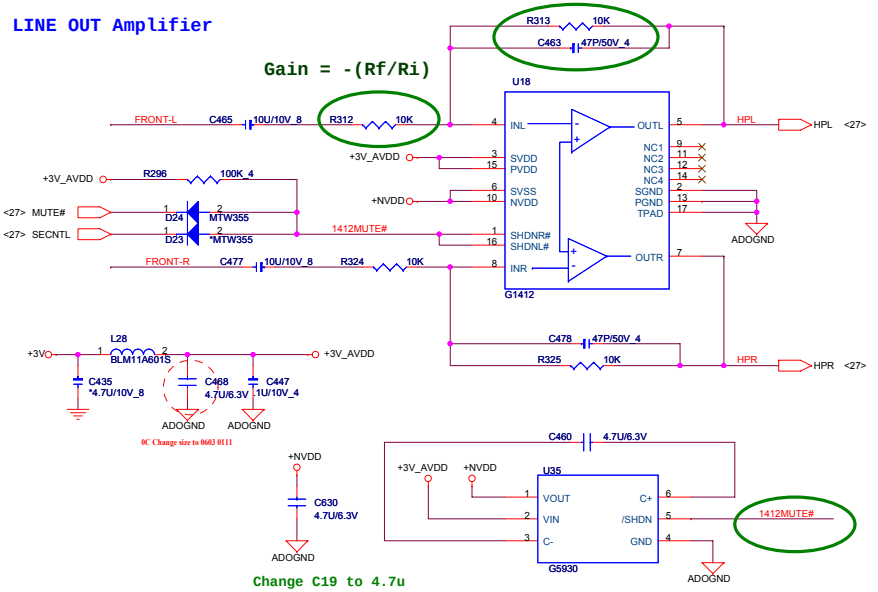




The pin2 of ALC888 define MXM_SPDIF_OUT

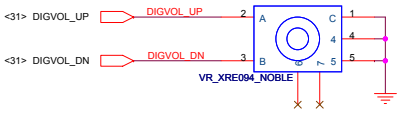
LINE OUT Amplifier

Gain = -(Rf/Ri)

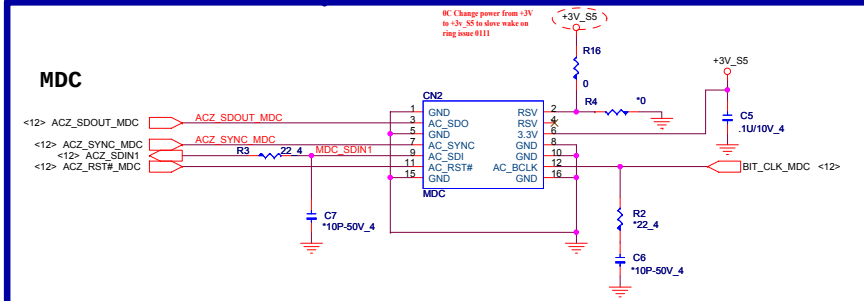


Change C19 to 4.7u

VR



MDC



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Quanta Computer Inc.

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	REALTEK ALC268&888/MDC/VR	E
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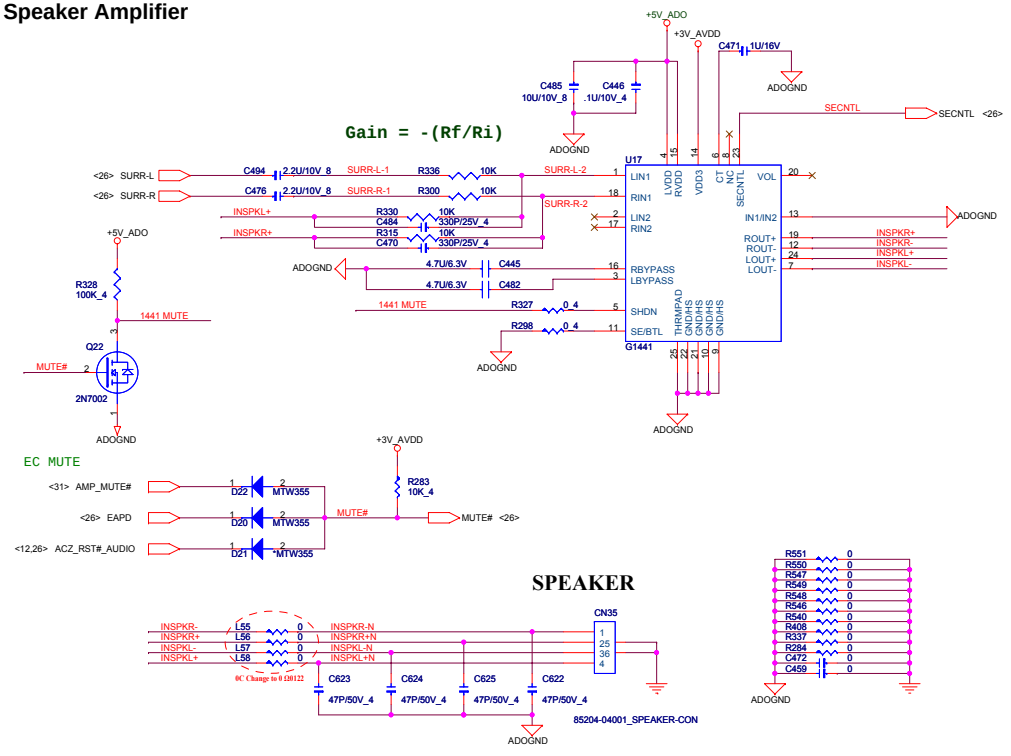
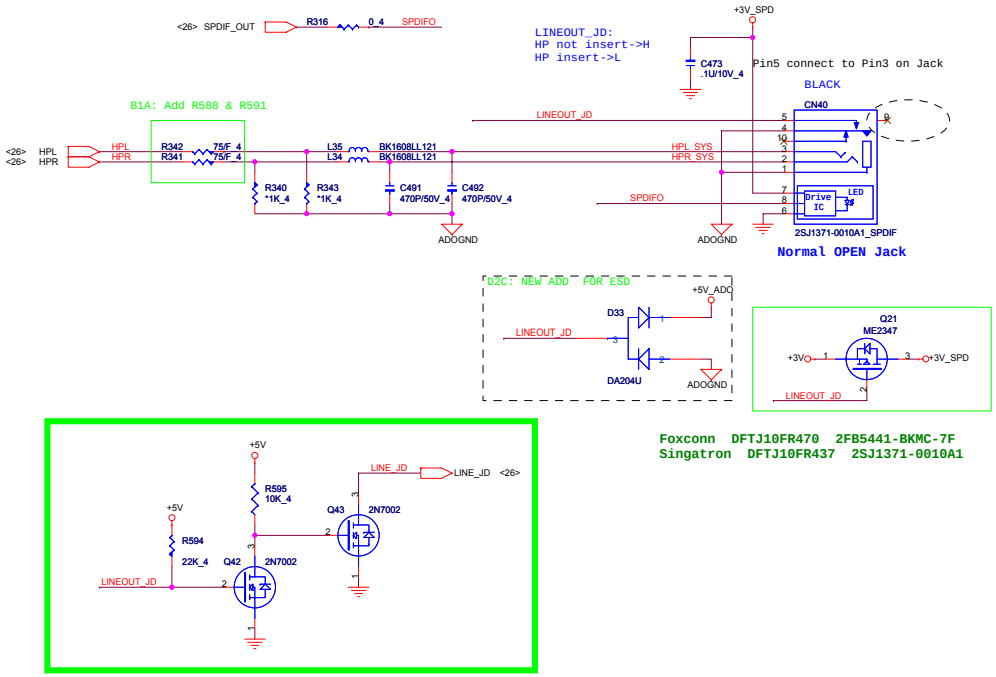
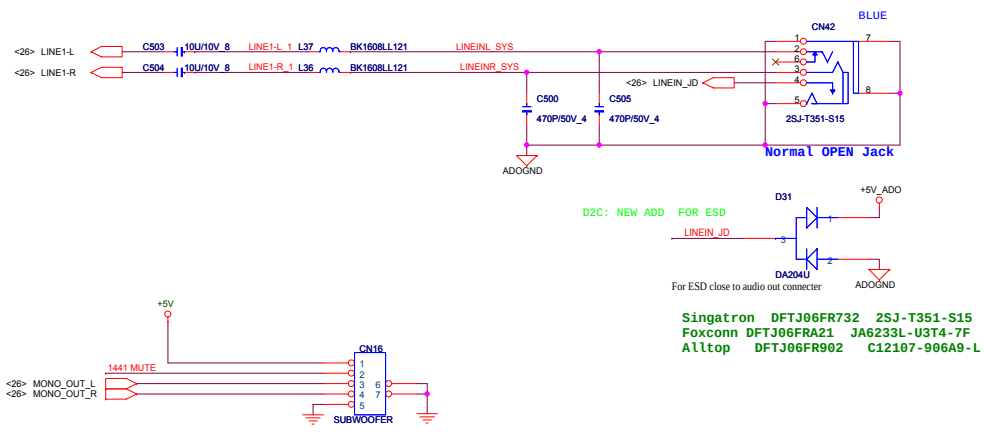
Speaker Amplifier



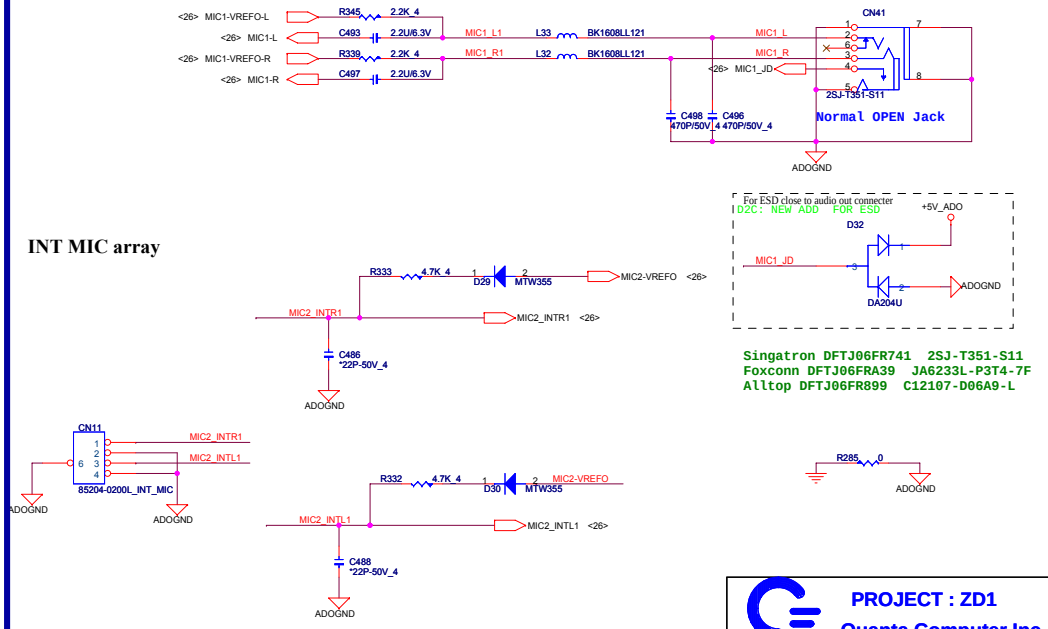
SYSTEM LINE OUT/SPDIF



SYSTEM LINE IN/SUBWOOFER



MIC



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Quanta Computer Inc.

Size	Document Number	Rev
	AMP /AUDIO JACK CONN	E
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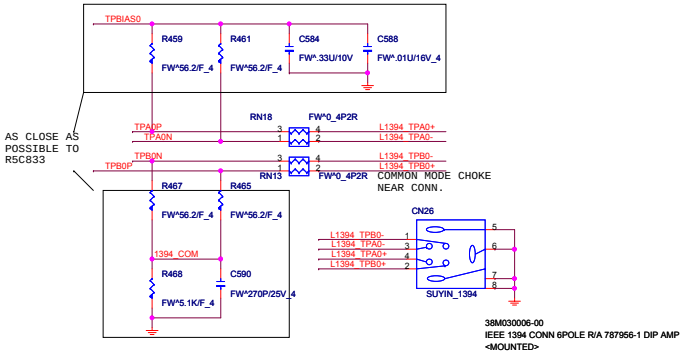
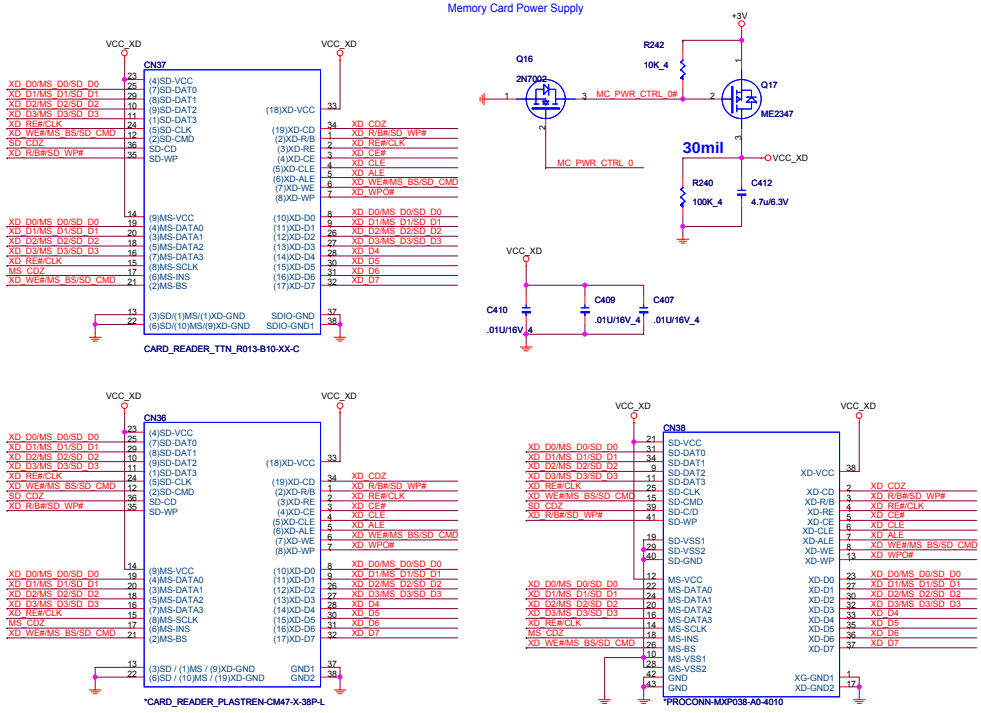
R5C832 : AJ5C8320H26
R5C833 : AJ5C8330H05

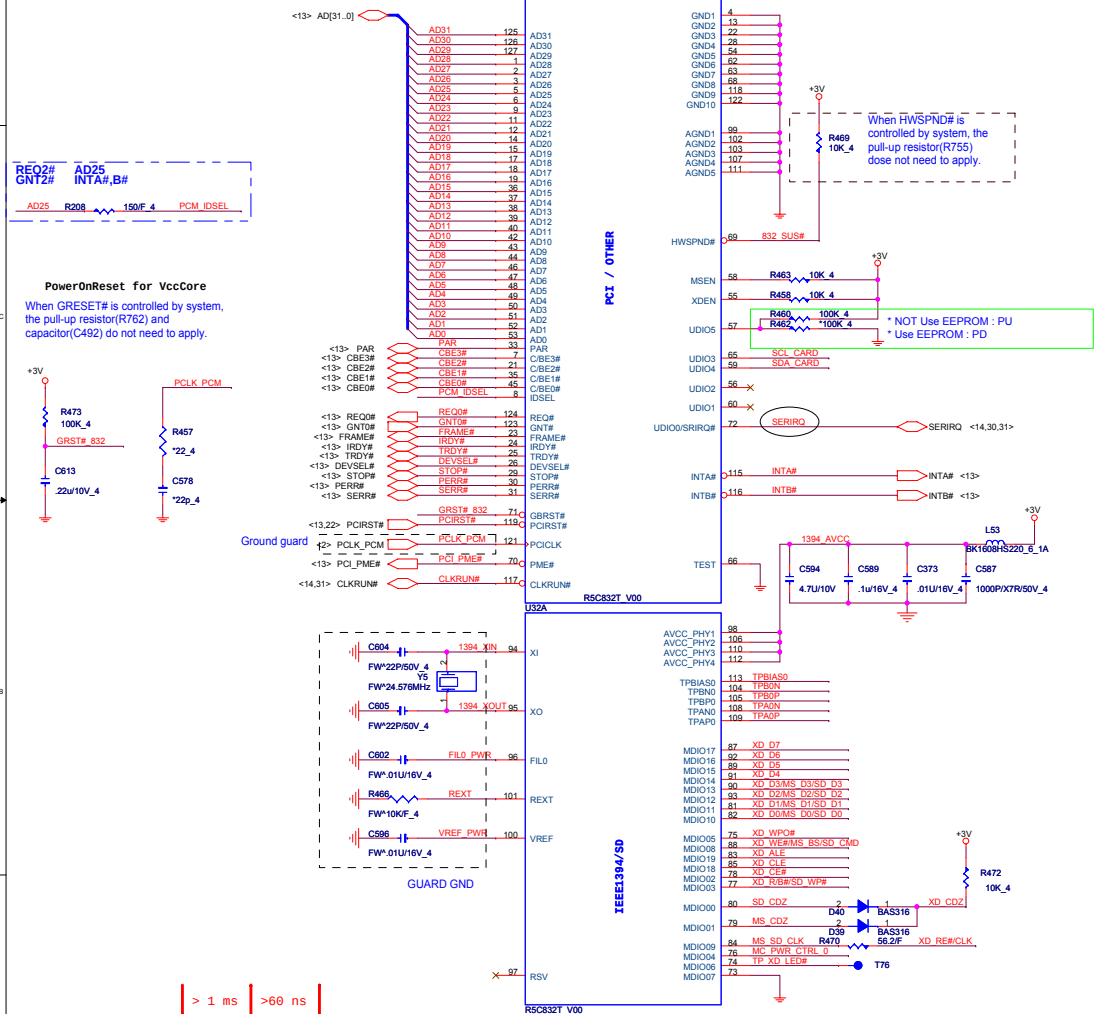
1394



5 IN 1 CARD READER

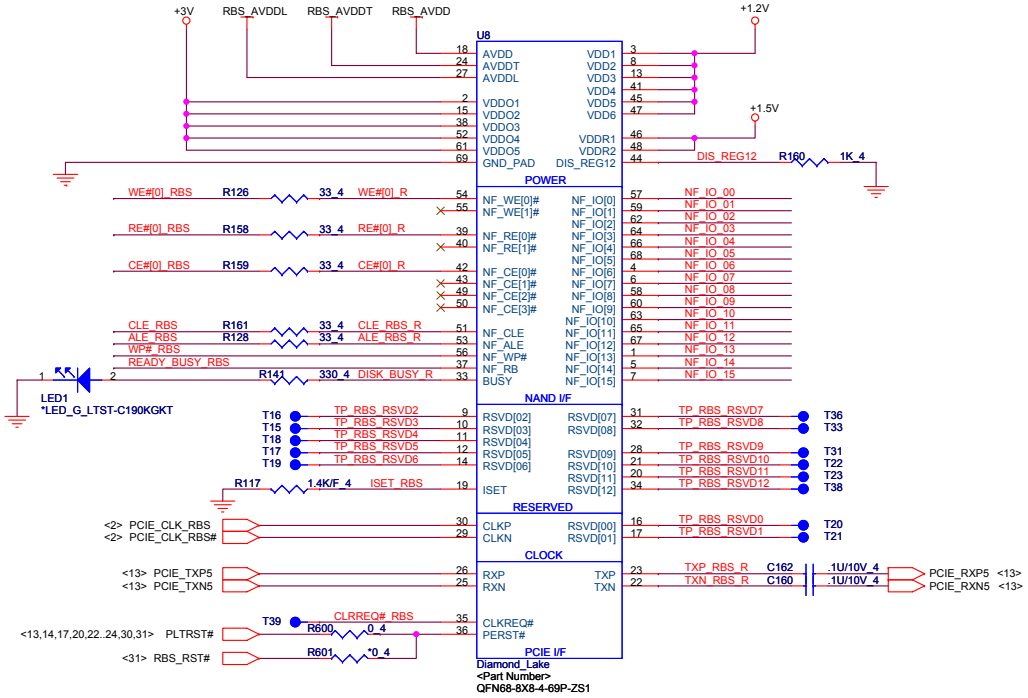


PCI / OTHER

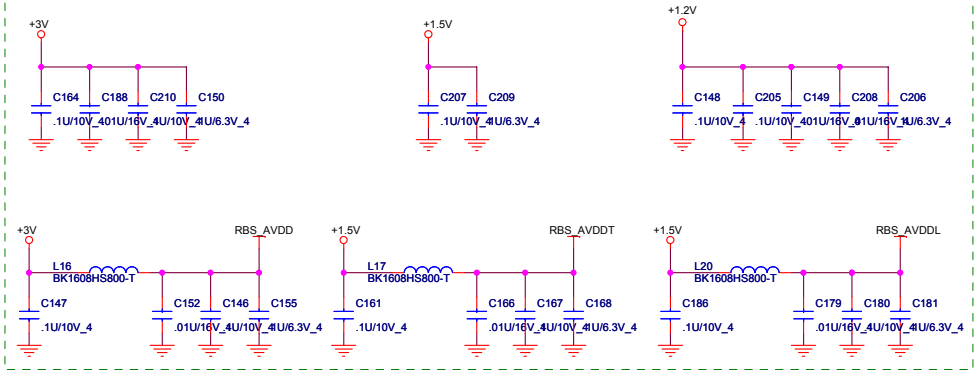


ROBSON

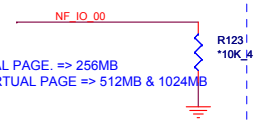
DIAMOND-LAKE ASIC



PLACE AS CLOSE AS POSSIBLE TO DIAMOND-LAKE ASIC.

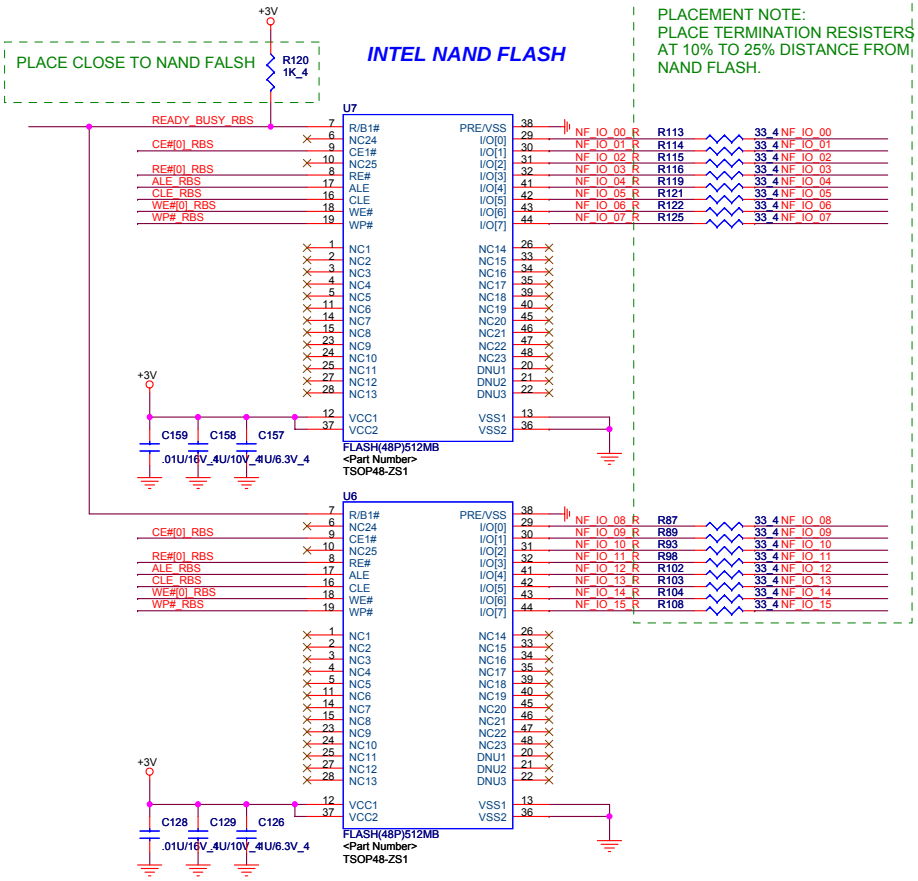


STUFF: INDICATES A 2KB VIRTUAL PAGE. => 256MB
DESTUFF: INDIACTESS A 4KB VIRTUAL PAGE => 512MB & 1024MB



PLACE CLOSE TO NAND FALSH

INTEL NAND FLASH



PLACEMENT NOTE:
PLACE TERMINATION RESISTERS AT 10% TO 25% DISTANCE FROM NAND FLASH.

LAYOUT NOTE:
ANY VIA ADDED BENEATH THE NAND FLASH NEEDS TO HAVE A SOLDERMASK ON IT.

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	ROBSON	E
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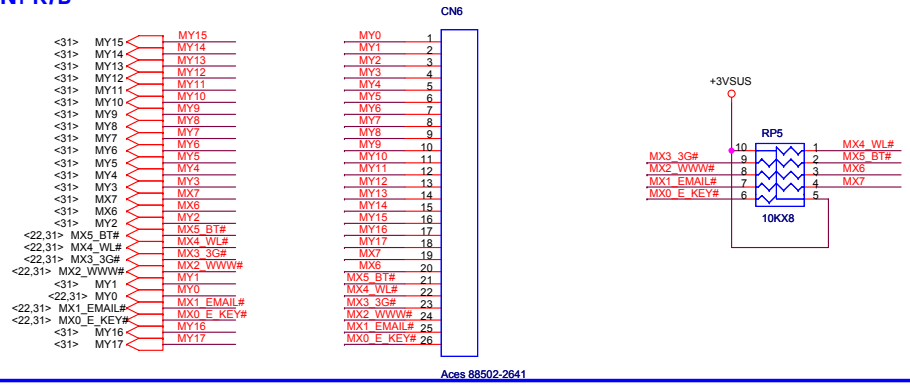
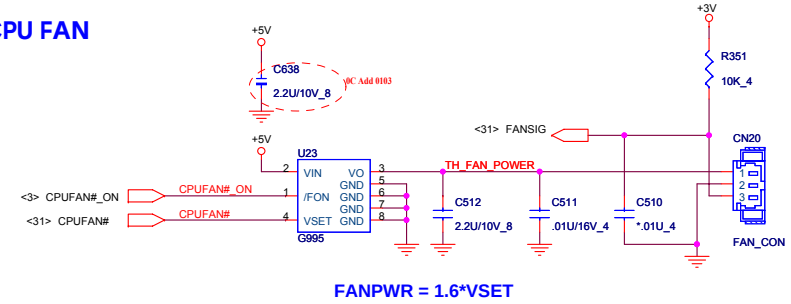
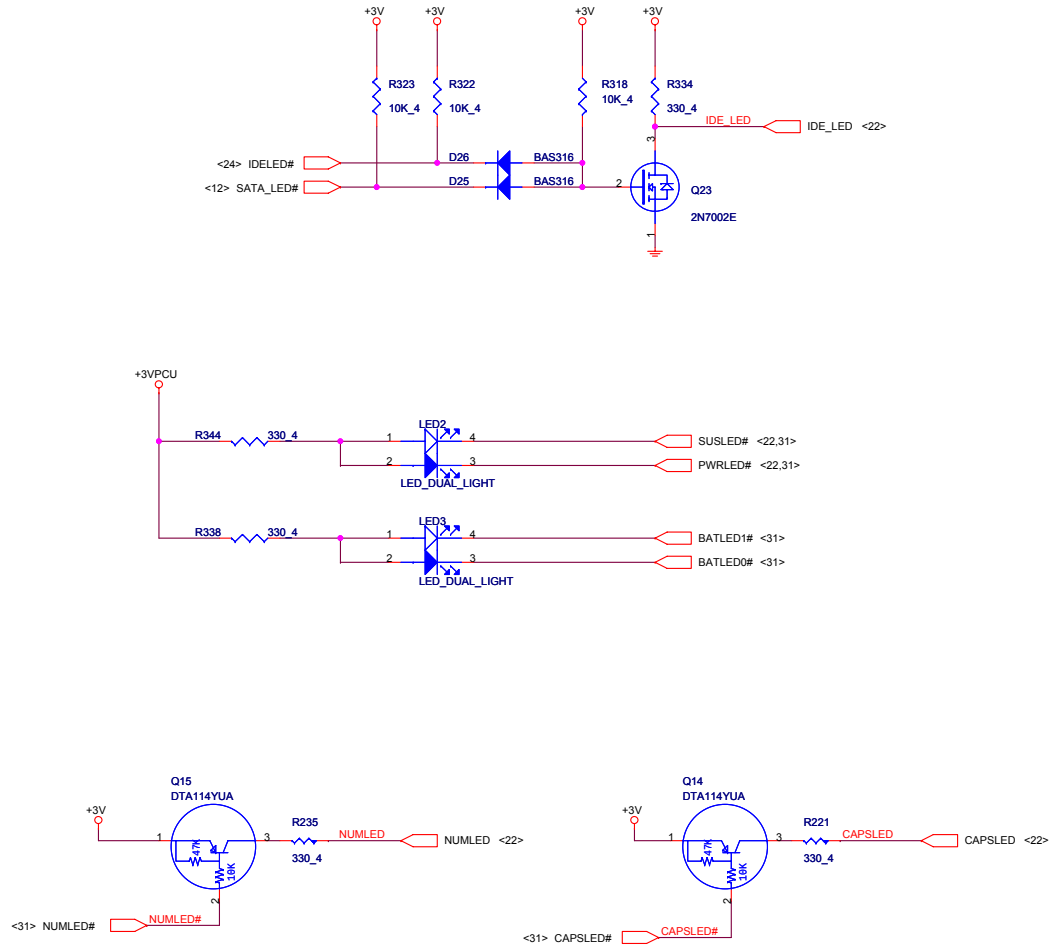
INT K/B



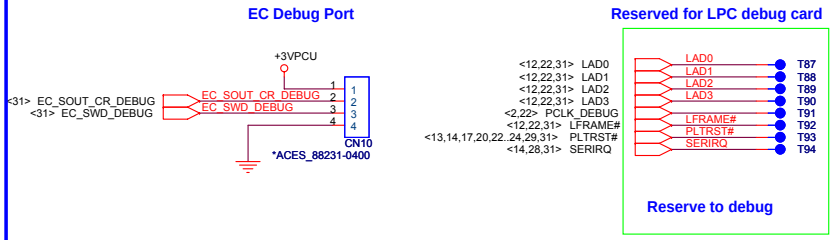
CPU FAN



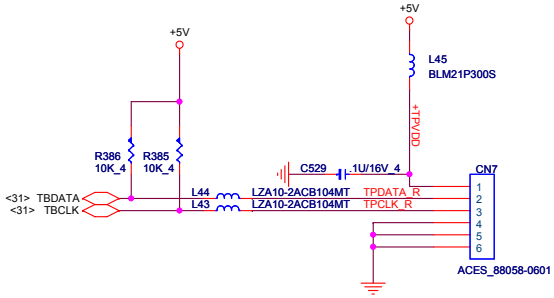
LED



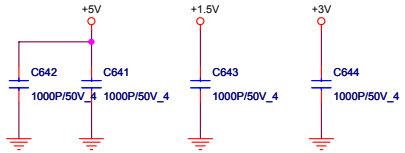
DEBUG PORT



T/P



EMI solution



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	FAN,LED,KB,DEBUG PORT,TP	E
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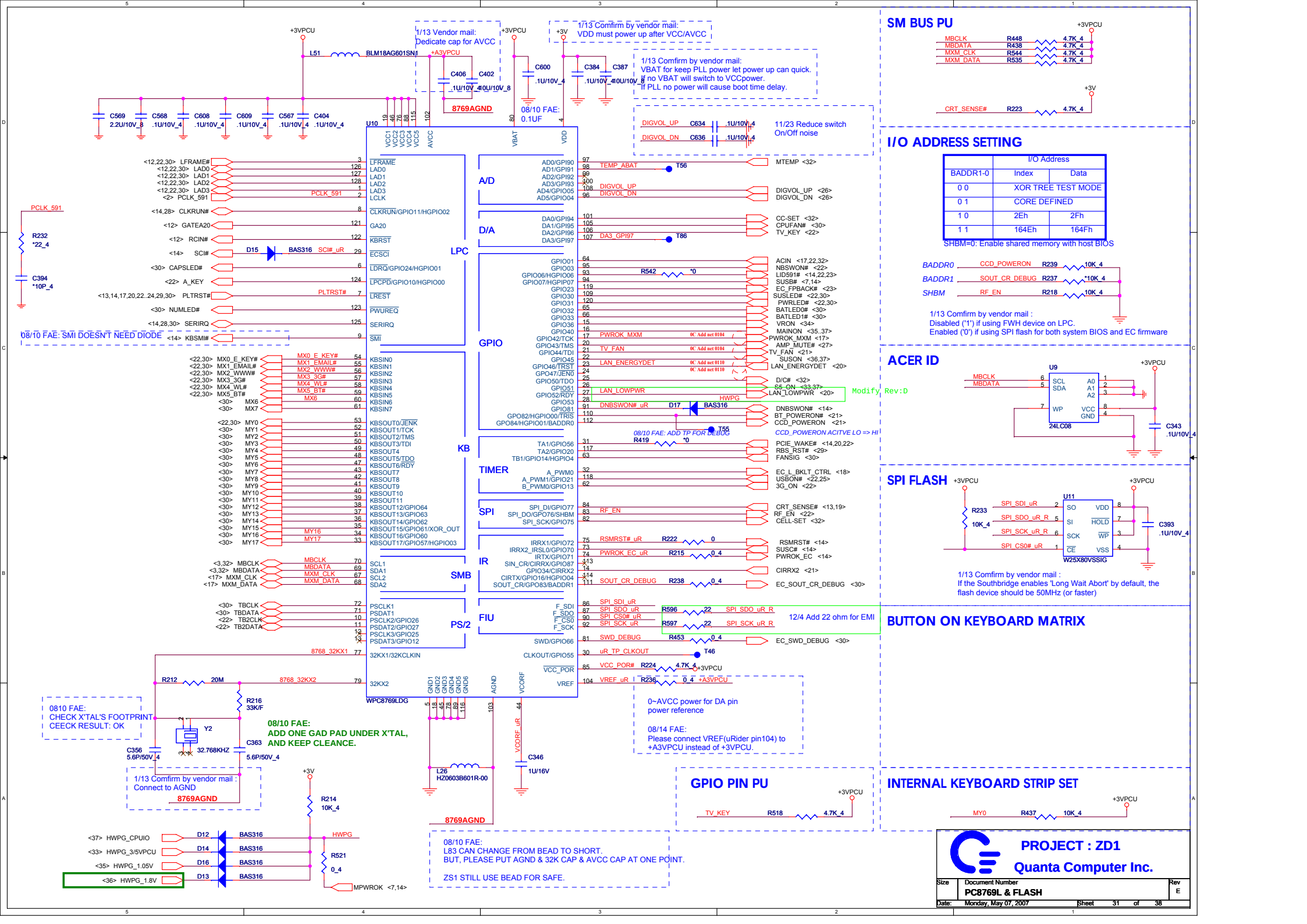
1/13 Vendor mail:
Dedicate cap for AVCC
1/13 Comfirm by vendor mail:
VDD must power up after VCC/AVCC
1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.
08/10 FAE:
0.1UF
11/23 Reduce switch
On/Off noise
08/10 FAE: SMI DOESN'T NEED DIODE
08/10 FAE: ADD TP FOR DEBUG
Modify Rev:D
CCD_POWERON ACITVE LO => HI
0~AVCC power for DA pin
power reference
08/14 FAE:
Please connect VREF(uRider pin104) to
+A3VPCU instead of +3VPCU.
12/4 Add 22 ohm for EMI
0810 FAE:
CHECK X'TAL'S FOOTPRINT
CEECK RESULT: OK
08/10 FAE:
ADD ONE GAD PAD UNDER X'TAL,
AND KEEP CLEANCE.
1/13 Comfirm by vendor mail :
Connect to AGND
08/10 FAE:
L83 CAN CHANGE FROM BEAD TO SHORT.
BUT, PLEASE PUT AGND & 32K CAP & AVCC CAP AT ONE POINT.
ZS1 STILL USE BEAD FOR SAFE.
SM BUS PU
I/O ADDRESS SETTING
I/O Address
BADDR1-0
Index
Data
0 0
XOR TREE TEST MODE
0 1
CORE DEFINED
1 0
2Eh
2Fh
1 1
164Eh
164Fh
SHBM=0: Enable shared memory with host BIOS
1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware
ACER ID
SPI FLASH
1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the
flash device should be 50MHz (or faster)
BUTTON ON KEYBOARD MATRIX
GPIO PIN PU
INTERNAL KEYBOARD STRIP SET
PROJECT : ZD1
Quanta Computer Inc.
PC8769L & FLASH
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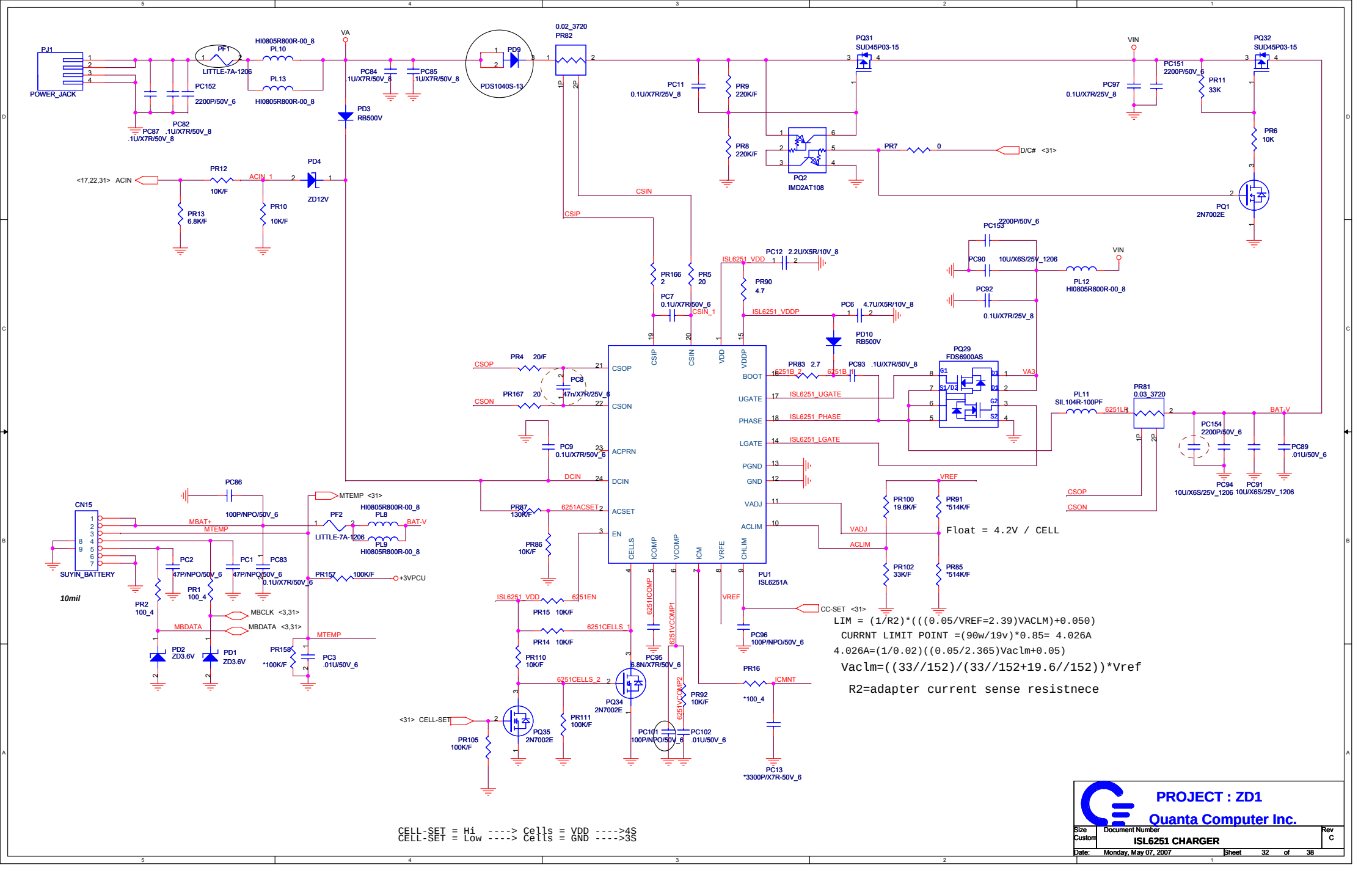
PJ1
POWER_JACK
PF1
LITTLE-7A-1206
HI0805R800R-00_8
PL10
PL13
PC152
2200P/50V_6
PC87 .1U/X7R/50V_8
PC82 .1U/X7R/50V_8
VA
PC84 .1U/X7R/50V_8
PC85 .1U/X7R/50V_8
PD3
RB500V
PD9
PDS1040S-13
0.02_3720
PR82
PC11
0.1U/X7R/25V_8
PR9
220K/F
PR8
220K/F
PQ31
SUD45P03-15
PQ2
IMD2AT108
PR7
0
D/C# <31>
VIN
PC97
0.1U/X7R/25V_8
PC151
2200P/50V_6
PR11
33K
PQ32
SUD45P03-15
PR6
10K
PQ1
2N7002E
<17,22,31> ACIN
PR12
10K/F
ACIN_1
PD4
ZD12V
PR13
6.8K/F
PR10
10K/F
CSIN
CSIP
PR166
2
PR5
20
PC7
0.1U/X7R/50V_6
CSIN_1
ISL6251_VDD
PC12 2.2U/X5R/10V_8
PR90
4.7
ISL6251_VDDP
PC6 4.7U/X5R/10V_8
PD10
RB500V
PC153
2200P/50V_6
PC90
10U/X6S/25V_1206
PC92
0.1U/X7R/25V_8
VIN
PL12
HI0805R800R-00_8
CSOP
PR4 20/F
PC8
47n/X7R/25V_6
CSON
PR167 20
PC9
0.1U/X7R/50V_6
DCIN
PR87
130K/F
6251ACSET
PR86
10K/F
CSIP
CSIN
VDD
VDDP
CSOP
CSON
ACPRN
DCIN
ACSET
EN
BOOT
UGATE
PHASE
LGATE
PGND
GND
VADJ
ACLIM
CELLS
ICOMP
VCOMP
ICM
VRFE
CHLIM
PU1
ISL6251A
PR83 2.7
PC93 .1U/X7R/50_8
6251B_2
6251B_1
PQ29
FDS6900AS
VA3
ISL6251_UGATE
ISL6251_PHASE
ISL6251_LGATE
PL11
SIL104R-100PF
6251LR
PR81
0.03_3720
BAT-V
PC154
2200P/50V_6
PC94
10U/X6S/25V_1206
PC91
10U/X6S/25V_1206
PC89
.01U/50V_6
VREF
PR100
19.6K/F
PR91
*514K/F
VADJ
ACLIM
PR102
33K/F
PR85
*514K/F
Float = 4.2V / CELL
CC-SET <31>
PC96
100P/NPO/50V_6
PC86
100P/NPO/50V_6
MTEMP <31>
CN15
SUYIN_BATTERY
MBAT+
MTEMP
PF2
LITTLE-7A-1206
HI0805R800R-00_8
PL8
PL9
HI0805R800R-00_8
BAT-V
10mil
PC2
47P/NPO/50V_6
PC1
47P/NPO/50V_6
PC83
0.1U/X7R/50V_6
PR157
100K/F
+3VPCU
PR1
100_4
PR2
100_4
MBCLK <3,31>
MBDATA
MBDATA <3,31>
MTEMP
PD2
ZD3.6V
PD1
ZD3.6V
PR158
*100K/F
PC3
.01U/50V_6
ISL6251_VDD
6251EN
PR15 10K/F
6251CELLS_1
PR14 10K/F
PR110
10K/F
6251CELLS_2
6251ICOMP
PC95
6.8N/X7R/50V_6
6251VCOMP1
6251VCOMP2
PR92
10K/F
PQ34
2N7002E
PR111
100K/F
PC101
100P/NPO/50V_6
PC102
.01U/50V_6
PR16
ICMNT
*100_4
PC13
*3300P/X7R-50V_6
<31> CELL-SET
PR105
100K/F
PQ35
2N7002E
LIM = (1/R2)*(((0.05/VREF=2.39)VACLM)+0.050)
CURRNT LIMIT POINT =(90w/19v)*0.85= 4.026A
4.026A=(1/0.02)((0.05/2.365)Vaclm+0.05)
Vaclm=((33//152)/(33//152+19.6//152))*Vref
R2=adapter current sense resistnece
CELL-SET = Hi ----> Cells = VDD ----->4S
CELL-SET = Low ----> Cells = GND ----->3S
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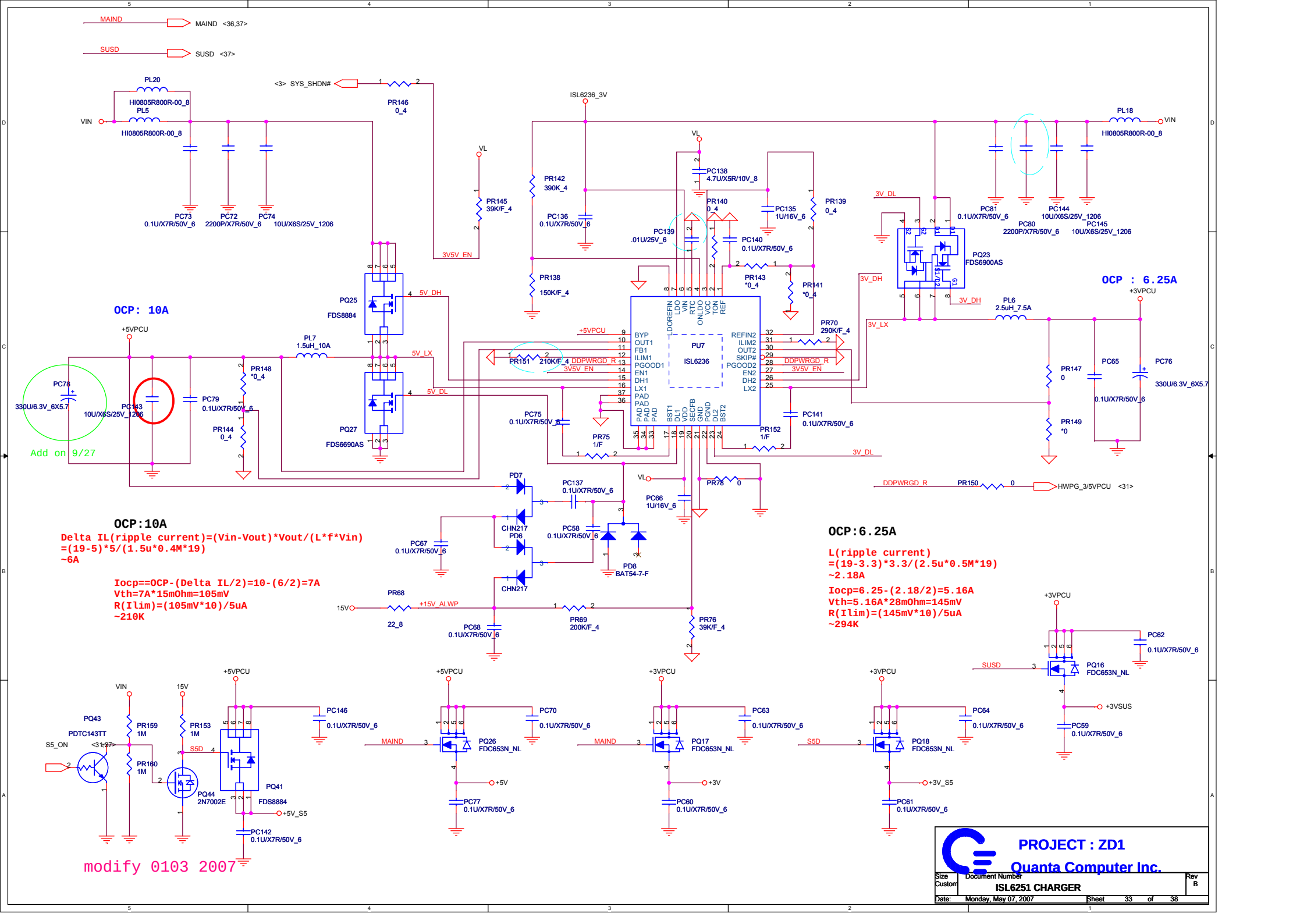
MAIND
MAIND <36,37>
SUSD
SUSD <37>
PL20
HI0805R800R-00_8
PL5
HI0805R800R-00_8
VIN
<3> SYS_SHDN#
PR146
0_4
ISL6236_3V
VL
PR145
39K/F_4
3V5V_EN
PR142
390K_4
PC136
0.1U/X7R/50V_6
PC138
4.7U/X5R/10V_8
PR140
0_4
PC135
1U/16V_6
PR139
0_4
PC139
.01U/25V_6
PC140
0.1U/X7R/50V_6
PR143
*0_4
PR141
*0_4
PR138
150K/F_4
PC73
0.1U/X7R/50V_6
PC72
2200P/X7R/50V_6
PC74
10U/X6S/25V_1206
PL18
HI0805R800R-00_8
PC81
0.1U/X7R/50V_6
PC80
2200P/X7R/50V_6
PC144
10U/X6S/25V_1206
PC145
10U/X6S/25V_1206
3V_DL
PQ23
FDS6900AS
3V_DH
OCP : 6.25A
+3VPCU
PL6
2.5uH_7.5A
3V_LX
PR70
290K/F_4
OCP: 10A
+5VPCU
PL7
1.5uH_10A
PQ25
FDS8884
5V_DH
5V_LX
5V_DL
PQ27
FDS6690AS
PR148
*0_4
PR144
0_4
PC78
330U/6.3V_6X5.7
PC143
10U/X6S/25V_1206
PC79
0.1U/X7R/50V_6
Add on 9/27
PR151
210K/F_4
DDPWRGD_R
3V5V_EN
PU7
ISL6236
DDREFIN
LDO
VIN
RTO
ONLLO
VCC
TON
REF
BYP
OUT1
FB1
ILIM1
PGOOD1
EN1
DH1
LX1
PAD
PAD
PAD
PAD
BST1
DL1
VDD
SFB
SGND
PGND
DL2
BST2
REFIN2
ILIM2
OUT2
SKIP#
PGOOD2
EN2
DH2
LX2
PR147
0
PC65
0.1U/X7R/50V_6
PC76
330U/6.3V_6X5.7
PR149
*0
PC75
0.1U/X7R/50V_6
PR75
1/F
PR152
1/F
PC141
0.1U/X7R/50V_6
PD7
PC137
0.1U/X7R/50V_6
PC66
1U/16V_6
PR78
0
PD6
CHN217
PC58
0.1U/X7R/50V_6
PD8
BAT54-7-F
PC67
0.1U/X7R/50V_6
PR68
22_8
15V
+15V_ALWP
PC68
0.1U/X7R/50V_6
PR69
200K/F_4
PR76
39K/F_4
DDPWRGD_R
PR150
0
HWPG_3/5VPCU <31>
OCP:10A
Delta IL(ripple current)=(Vin-Vout)*Vout/(L*f*Vin)
=(19-5)*5/(1.5u*0.4M*19)
~6A
Iocp==OCP-(Delta IL/2)=10-(6/2)=7A
Vth=7A*15mOhm=105mV
R(Ilim)=(105mV*10)/5uA
~210K
OCP:6.25A
L(ripple current)
=(19-3.3)*3.3/(2.5u*0.5M*19)
~2.18A
Iocp=6.25-(2.18/2)=5.16A
Vth=5.16A*28mOhm=145mV
R(Ilim)=(145mV*10)/5uA
~294K
PQ43
PDTC143TT
S5_ON
<31,37>
PR159
1M
PR160
1M
PR153
1M
S5D
PQ44
2N7002E
PQ41
FDS8884
+5V_S5
PC146
0.1U/X7R/50V_6
PC142
0.1U/X7R/50V_6
PQ26
FDC653N_NL
PC70
0.1U/X7R/50V_6
+5V
PC77
0.1U/X7R/50V_6
PQ17
FDC653N_NL
PC63
0.1U/X7R/50V_6
+3V
PC60
0.1U/X7R/50V_6
PQ18
FDC653N_NL
PC64
0.1U/X7R/50V_6
+3V_S5
PC61
0.1U/X7R/50V_6
PQ16
FDC653N_NL
PC62
0.1U/X7R/50V_6
+3VSUS
PC59
0.1U/X7R/50V_6
modify 0103 2007
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Quanta Computer Inc.
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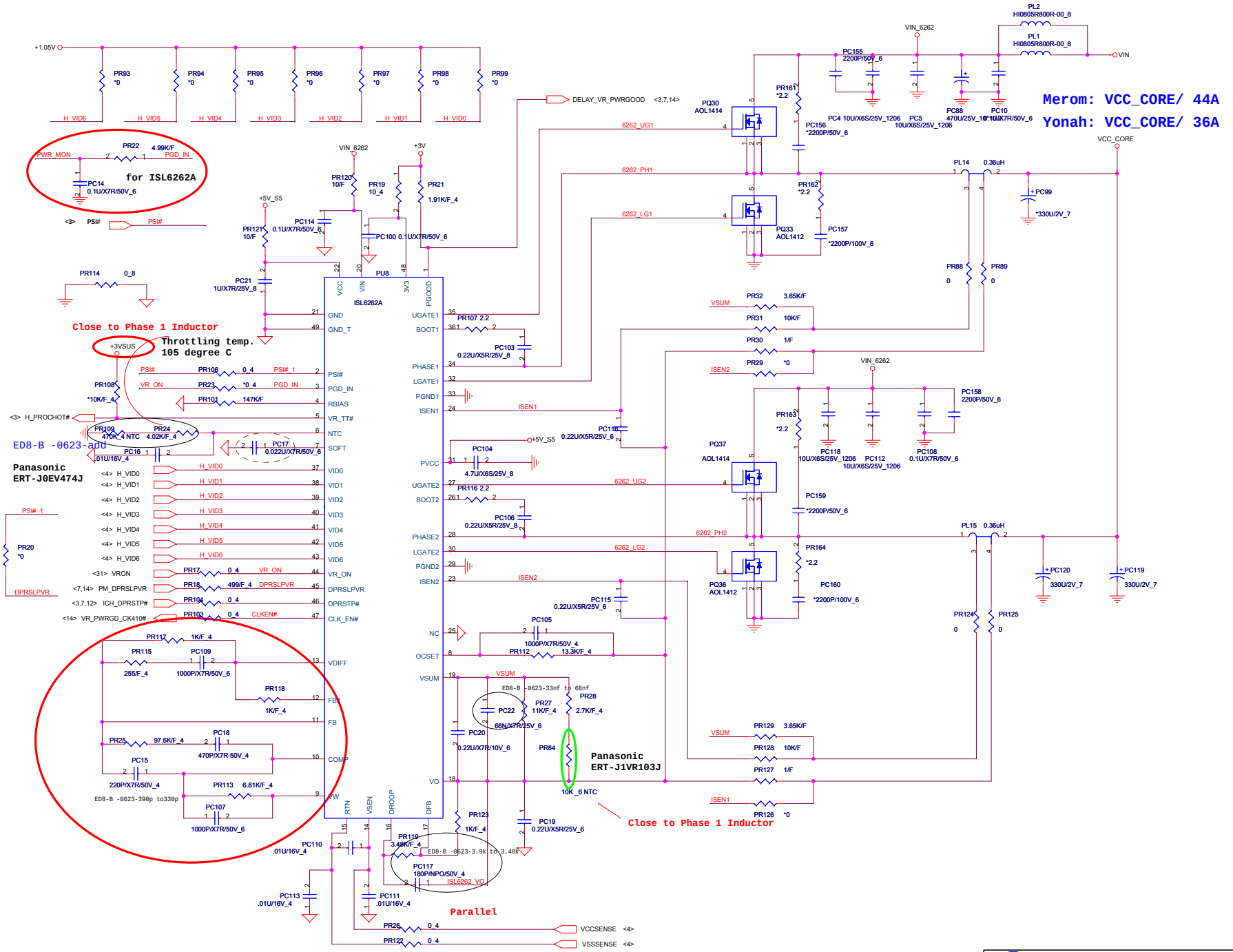
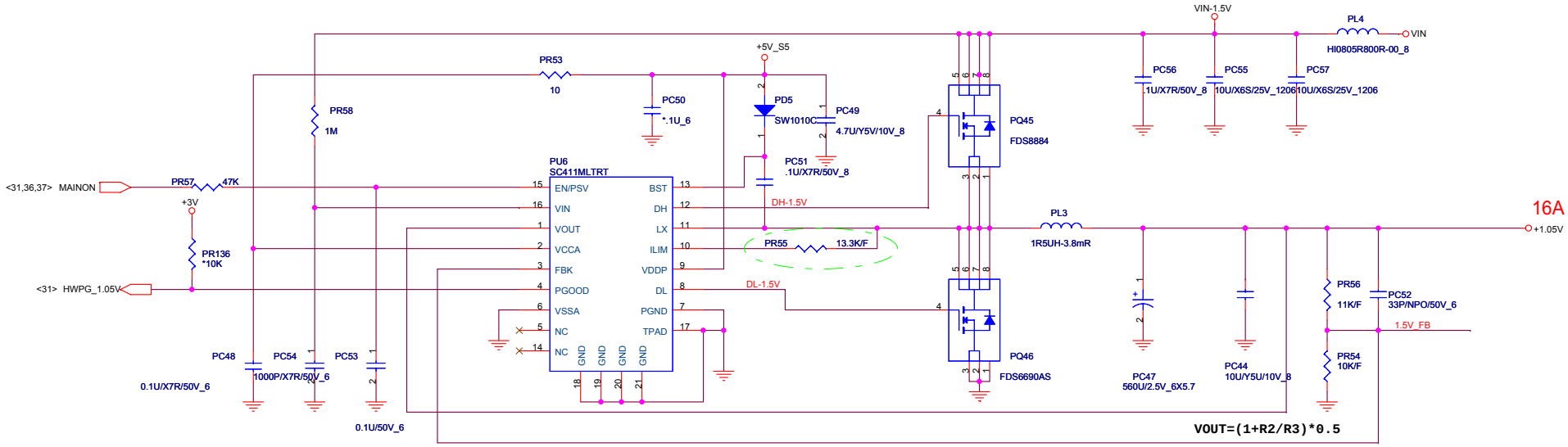

Merom: VCC_CORE/ 44A
Yonah: VCC_CORE/ 36A
for ISL6262A
Close to Phase 1 Inductor
Throttling temp.
105 degree C
ED8-B -0623-add
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Close to Phase 1 Inductor
Parallel
ISL6262A
VCC_CORE
VIN
PROJECT : ZD1
Quanta Computer Inc.
CPU CORE(ISL6262)
Monday, May 07, 2007



Rdson*Iocp=PR55*10u Rdson=15m ohm

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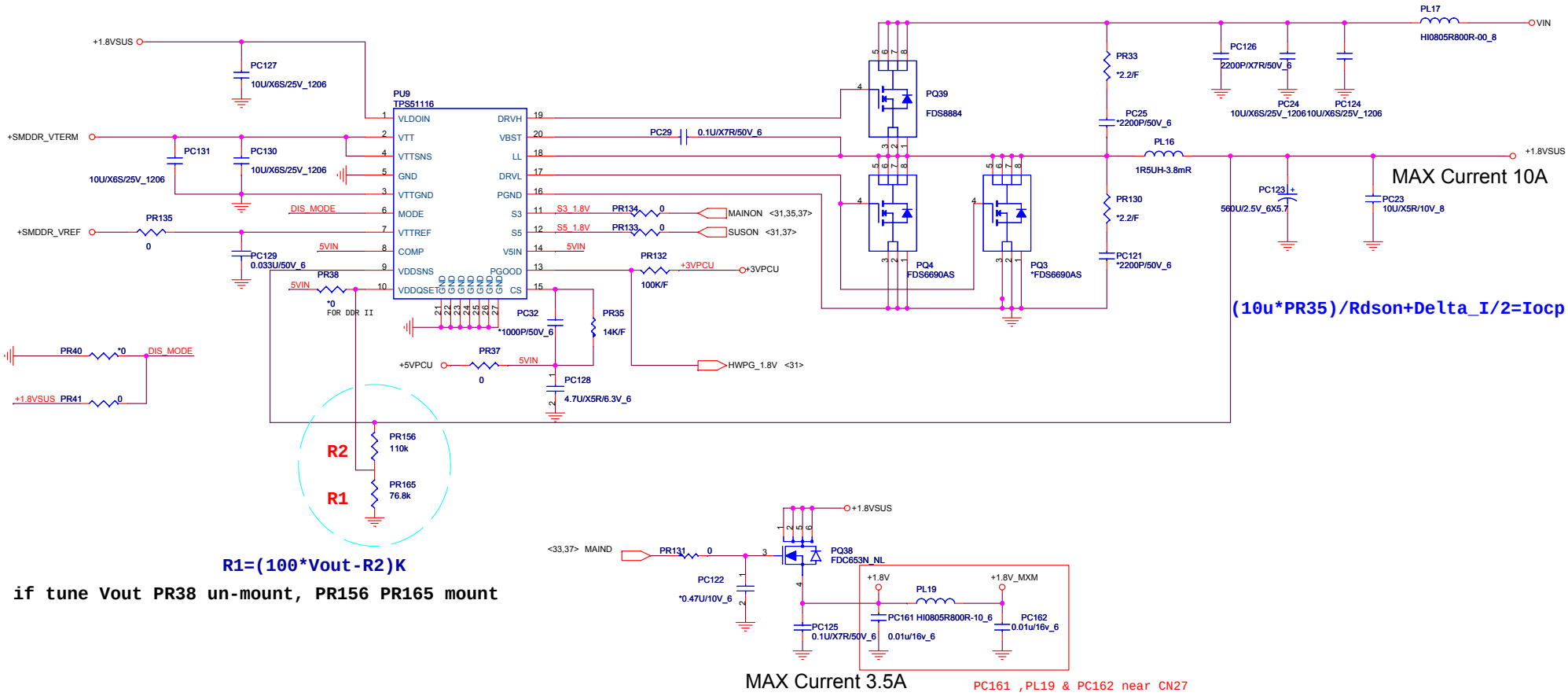

PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	DDR 1.8V(TPS51116)	B
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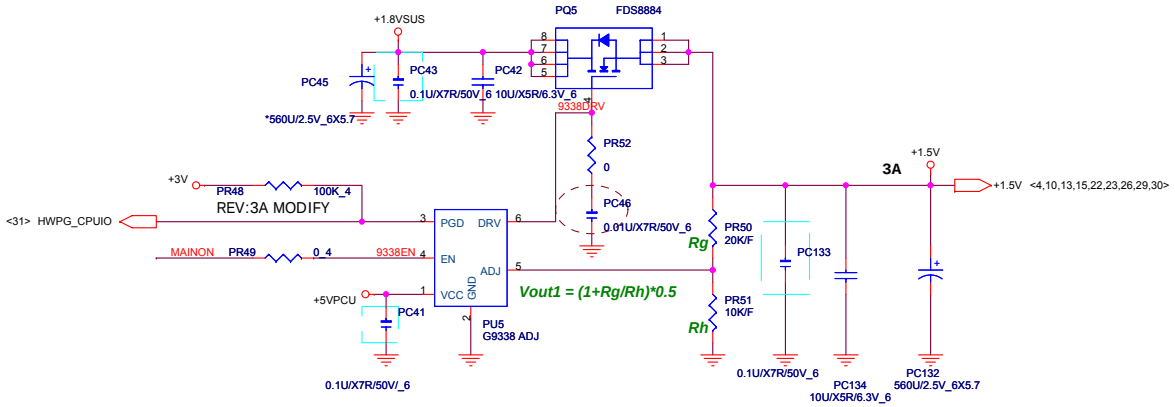
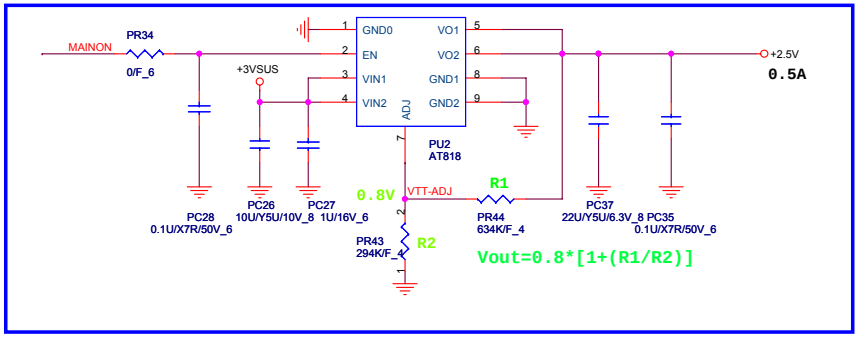
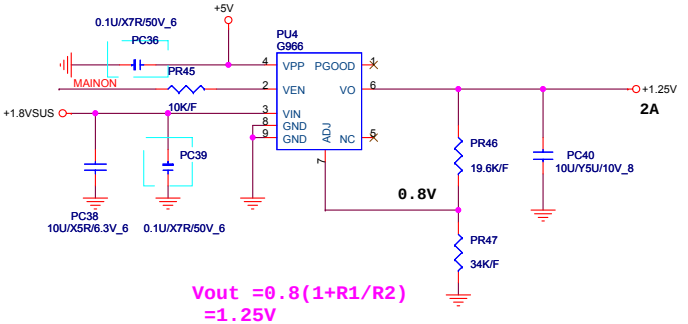
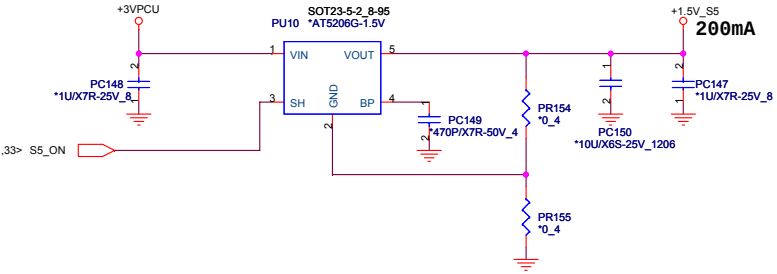
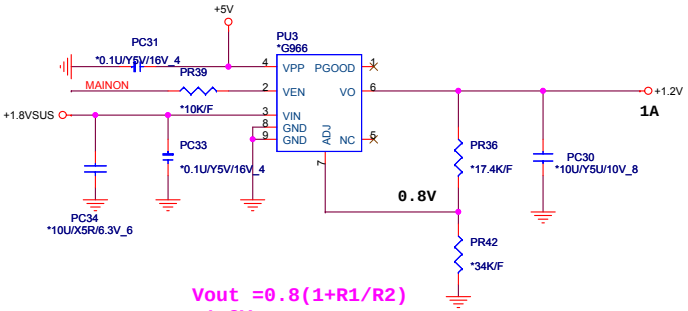
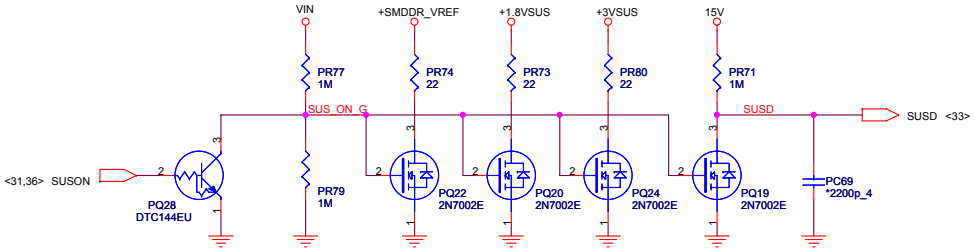




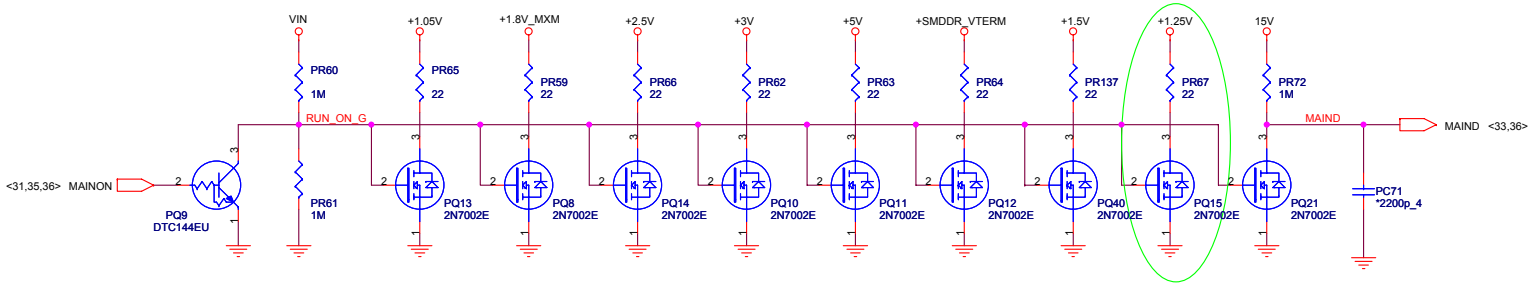








Add by power on 10/19



PROJECT : ZD1

Quanta Computer Inc.

Size	Document Number	Rev
	Discharge (1.5V/2.5V)	C
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CHANGE LIST

Model	REV	
ZD1 MB	1A	FIRST RELEASED: E200610-3793 (PCB: DA0ZD1MB6A0)
	2A	Page10 : Depop R153 & pop L23 for system can not boot Page14 : U36 package didn't math footprint, change P/N. Page26 : Remove R275, install R276; remove R4, install R16; Change R245, R247 power source from +1.5V_S5/+1.5V to +3V_S5/+3V , Follow customer request modem change support to +3VSUS. Page22 : MMB(CN8) PIN define error. Page22 : TV card change support to +1.5V. Page18 : Install R5, depop R7,: Follow customer request use EC to control backlight ON/OFF function. Page14 : GPIO10: Reserve PU, 10K +> It is GPO and OD; GPIO14: Reserve PD, 10K => It is GPI as AC present and active high; Page6 : TV_DCONSEL[0:1], UMA =>NC, External VGA tie to GND. Page31 : 2nd FAN change design Page23 : New card power SW (location: U33) change same as ZO1 Page31 : add 2 capacity 0.1uF(C634,C636) in DIGVOL_UP / DIGVOL_DN pins Page26 : Co-layout ALC268 and 888S Page28 : SD card can not be detected , U32(ES2) sample will fix this issue. Page28 : MMC card can not be detected , U32(ES2) sample will fix this issue. Page14 : The CLPWROK pin of ICH8 connect with HWPG signal Page22 : change CN7 pin definition for T/P no function. Page24 : change CN8 pin definition MMB no function. Page14 : The signal of KBSMI#_ICH add diode , and it PU to +3V_S5 The signal of LID591#_ICH add diode , and it PU to +3V_S5 for ICH8 electric leakage issue. Page26 : Change subwoofer from 4pin to 5pin connector.
	2B	Page 2 : Add C645 for EMI solution Page31 : Follow customer request 2nd FAN is controlled by EC Page19 : Floating CN13.16 & CN13.17 ,CN14.15 & CN14.16 for ESD test Page07 : DPLL_REF_CLK, DPLL_REF_CLK#, DPLL_REF_SSCLK and DPLL_REF_SSCLK#. To GND Page36 : Add PI filter to reduce the power ripple of +1.8V. Page16 : Modify SMbus address A2 , The signal of B_SA1 need to PU and B_SA0 need to PD Page26 : add 2 capacity 1uF(C639,C640) for subwoofer Page30 : add capacity 2.2uF(C638)
	2C	Page17 : Adding (Q52 & R541 & Q53) extra circuitry to prevent power leakage from system into MXM Page21 : Change power of CIR from +3VPCU and +5VPCU. Page31 : AEC pin24 is multi function pin, when EC power up, pin17 will change to JTAG/TCK function not GPIO. So,need to change from pin24 (GPIO47) to pin27 (GPIO52). Page22: Power/B connector add two LED control signal and change to 16 pin from 14-pin for meet ACER LED spec . Page22: Q35 change to AO3413 form DTA114 for increase LED driving power. Page23: BL_ON pull up resistor from 10kohm to 100Khom(R194).+3V pull up will cause power on leakage on BL_ON signal due to our VGA have 10kohm pull low.
	2D	Page19 : Connect CRT of CN13.16 & 17 to GND for ESD Page17 : Add capacity 330uF(C647) & Remove R541 Page22 & 25: Combine USB/B (CN17) and TV/B(CN30) connector, Connector change to 16 pin. and +5_S5 from 1pin to 2pin. Page25 : Connect HOLE 28 & 29 to GND for ESD Page32~37 : Update power circuit Page37 : Remove 1.2V circuit Page26 : Add 1000pF and 10pF total 4 PCS Location: C648 , C649, C650, C652 (between +5V_ADOand AGND). Page22 : CN8.8 remove +5V & R540 & connect to +3V (K) Page27 : Modify and ADD. AGND bridge (R337,R284,C459 and C472 = 0 Ohm). Page34 : Remove PR161, PR163, PC156, PC159 Page22 : Add D45~D51 for ESD Page28 : Change CN36.37 & 38 ,CN37.37 & 38 ,CN38.42 & 43 from ADOGND and GND.
	3A	Page32 : PD9 Change footprint Page25 : Add EMI Spring Page27 : Add GND & AGND bridge (R546,R540,R408) Page22 : Modify pin define (TV/B(CN30) connector)
	F	Page23 & 17 : HDMI circuits modify: Add level-shifter for MXM_HDMI_DDCCLK and MXM_HDMI_DDCDATA.(Location: Q54 ,Q55 , R75, R63, R297, R410 & R602) .

MODEL	ZY3 FROM	ZY3 To
	X	1A
	X	1A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	1A	2A
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2A	2B
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A
	2B	3A

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Quanta Computer Inc.

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DOC NO.	PROJECT MODEL :	ZD1	APPROVED BY:		DATE:	2007/ 2/15
	PART NUMBER:		DRAWING BY:		REVISON:	3A