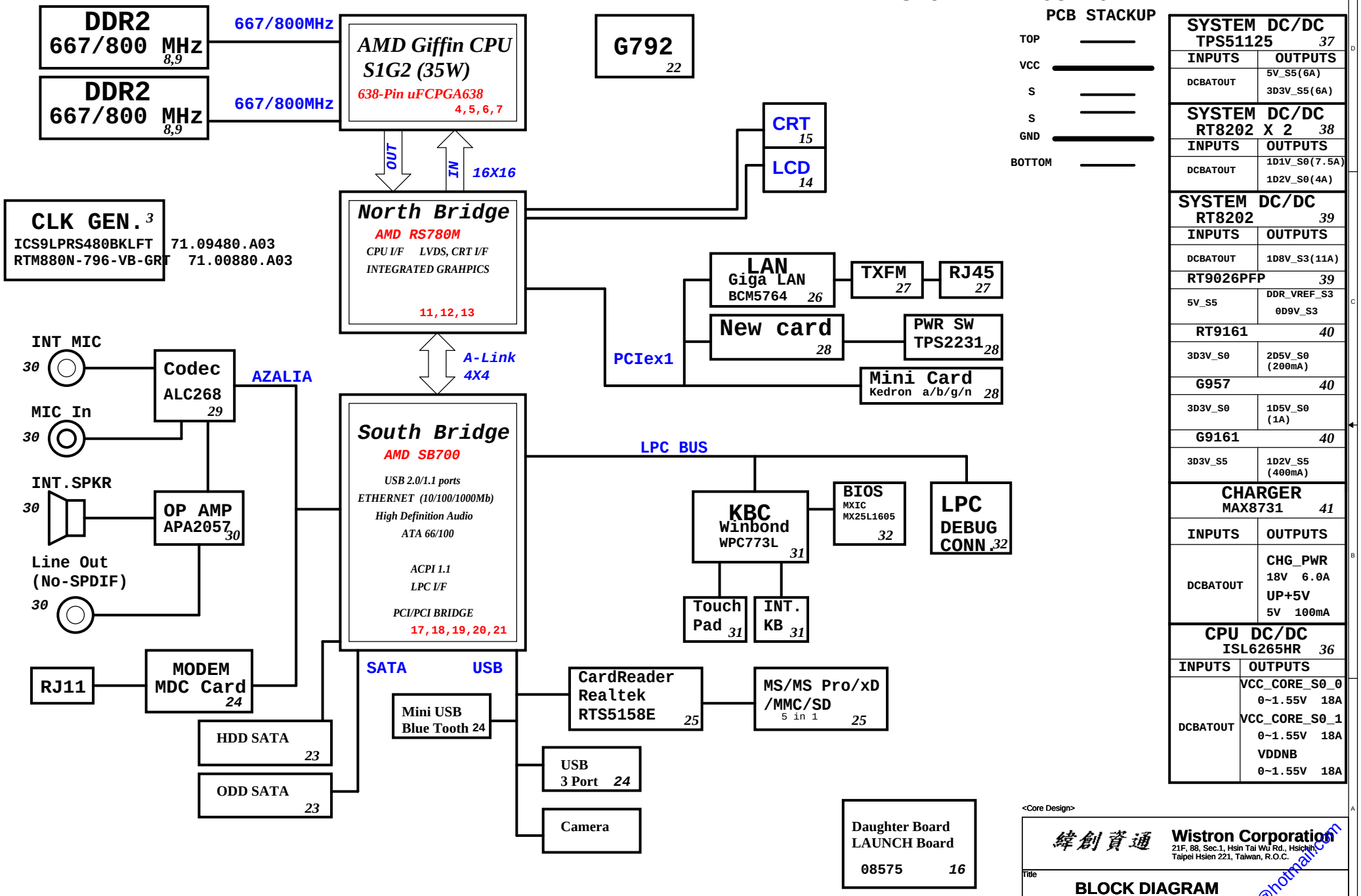
Cathedral Peak 2A Block Diagram

Project code: 91.4K901.001
PCB P/N : 48.4K901.001
REVISION : 08220- -1



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 37	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC RT8202 X 2 38	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8202 39	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)

RT9026PFP 39	
5V_S5	DDR_VREF_S3 0D9V_S3

RT9161 40	
3D3V_S0	2D5V_S0 (200mA)

G957 40	
3D3V_S0	1D5V_S0 (1A)

G9161 40	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 41	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 36	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	Cathedral Peak 2A	-1

Date: Friday, August 22, 2008 Sheet of 43

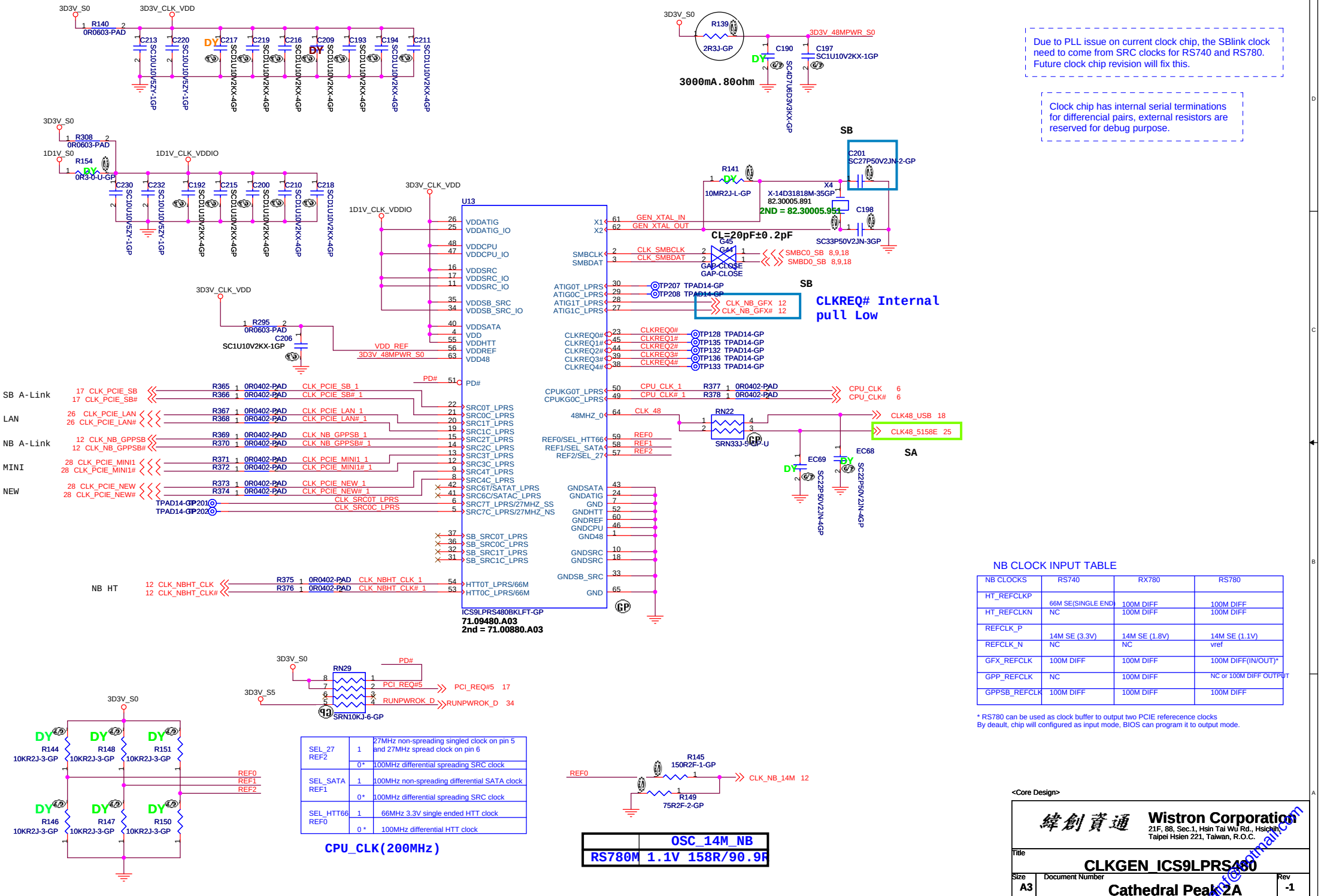
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HISTORY**

Size	Document Number	Rev
A3	Cathedral Peak 2A	-1

Date: Friday, August 22, 2008 Sheet 2 of 43



Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.

Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.

SEL_27 REF2	1	27MHz non-spreading singled clock on pin 5 and 27MHz spread clock on pin 6
	0*	100MHz differential spreading SRC clock
SEL_SATA REF1	1	100MHz non-spreading differential SATA clock
	0*	100MHz differential spreading SRC clock
SEL_HTT66 REF0	1	66MHz 3.3V single ended HTT clock
	0*	100MHz differential HTT clock

CPU_CLK(200MHz)

	OSC_14M_NB
RS780M 1.1V 158R/90.9R	

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE referecence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

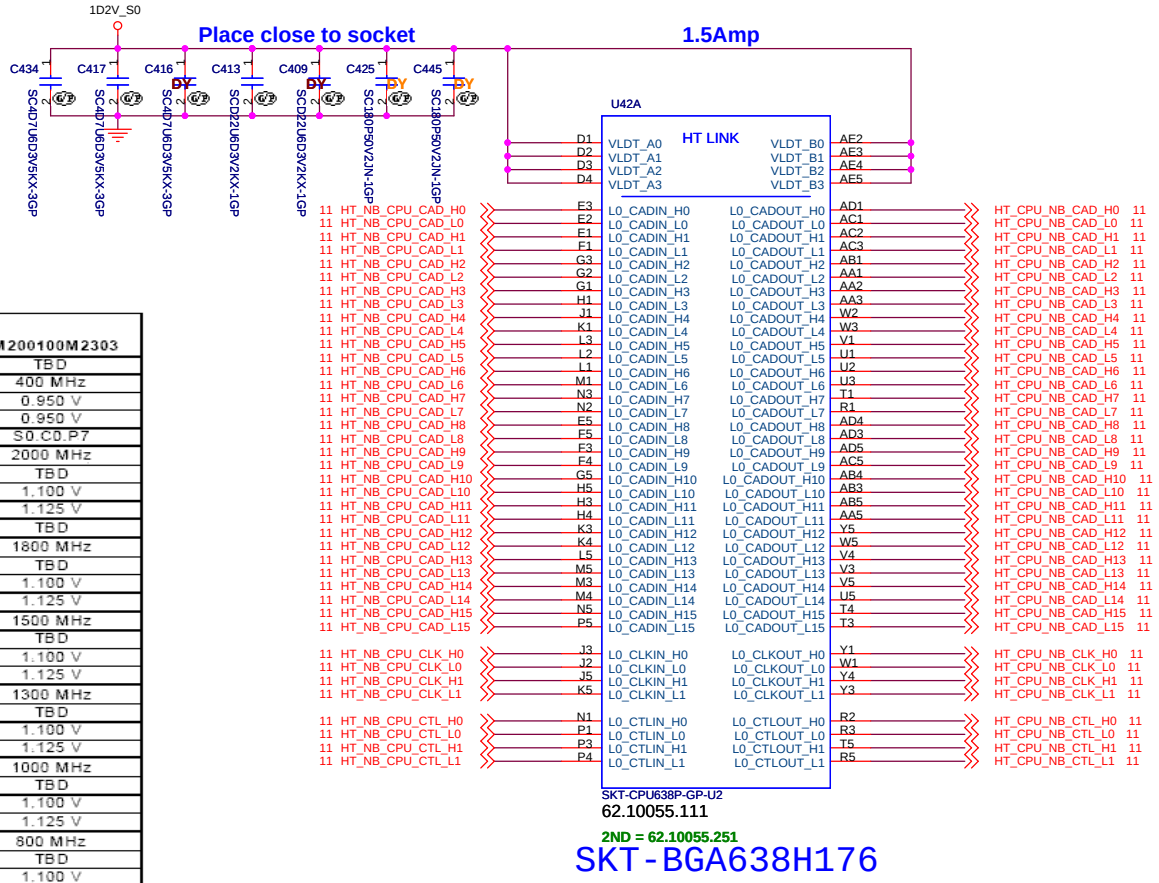
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet of 43



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

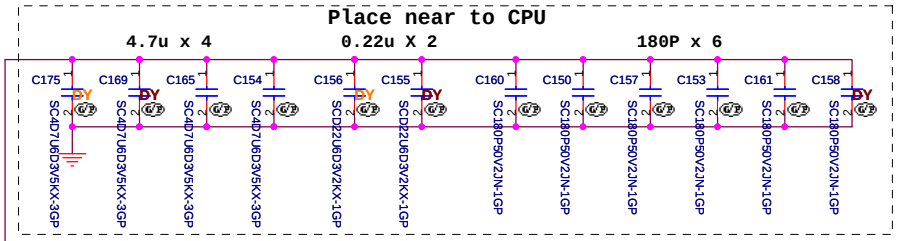
<Core Design>

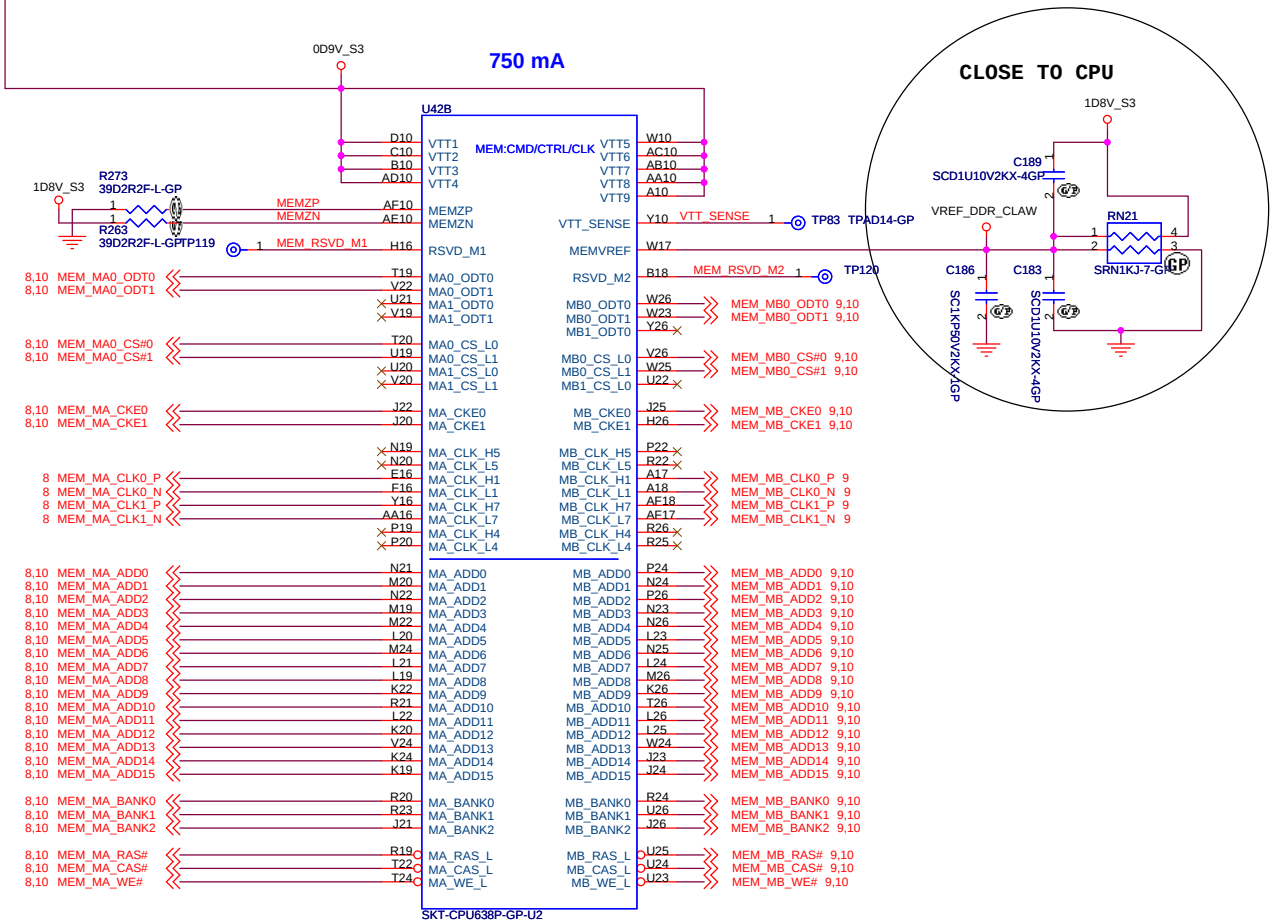
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

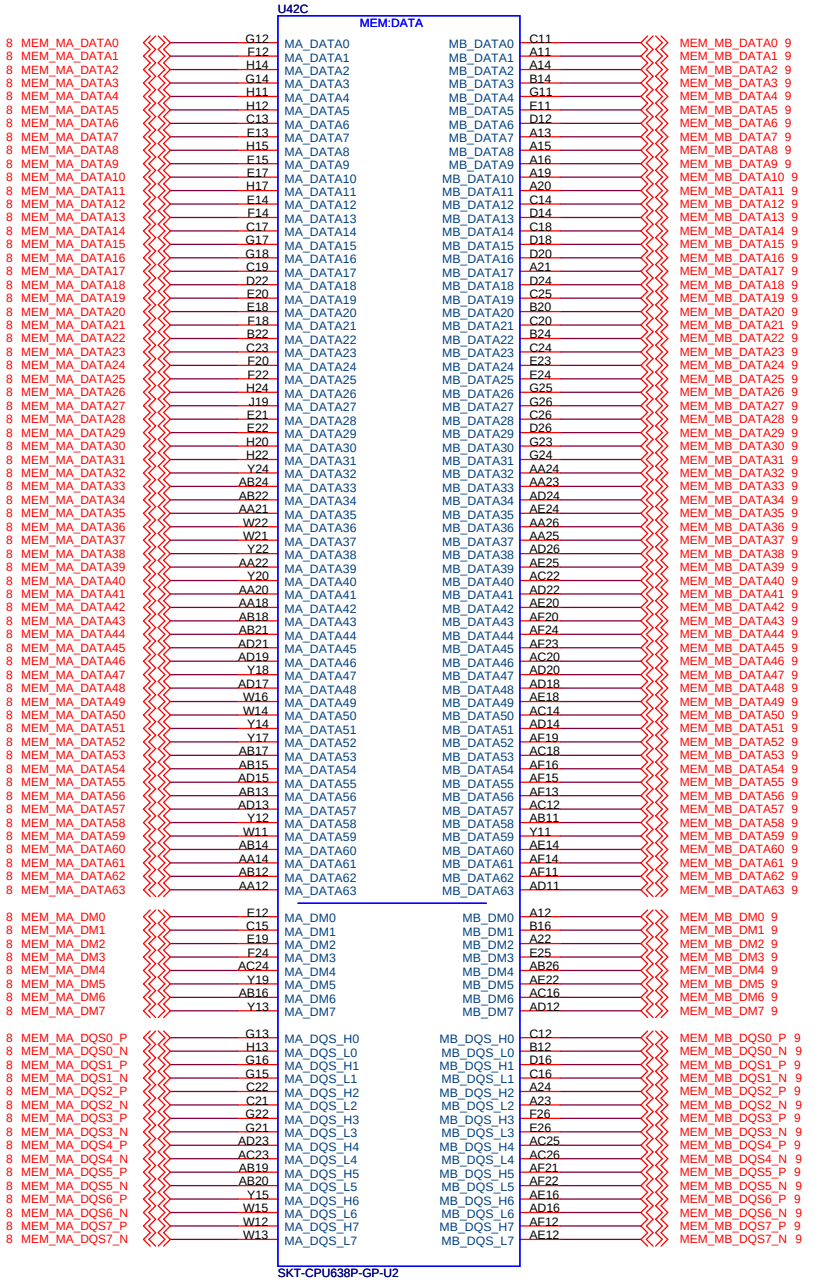
Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 4 of 43







<Core Design>

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	CPU_DDR_(2/4)	
Size: A3	Document Number: Cathedral Peak 2A	Rev: -1
Date: Friday, August 22, 2008	Sheet of 43	

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

SA

Near CPU PIN

CPU exceeds to 125℃

SKT-CPU638P-GP-U2

HDT Connectors

HDT1
SMC-CONN26A-FP

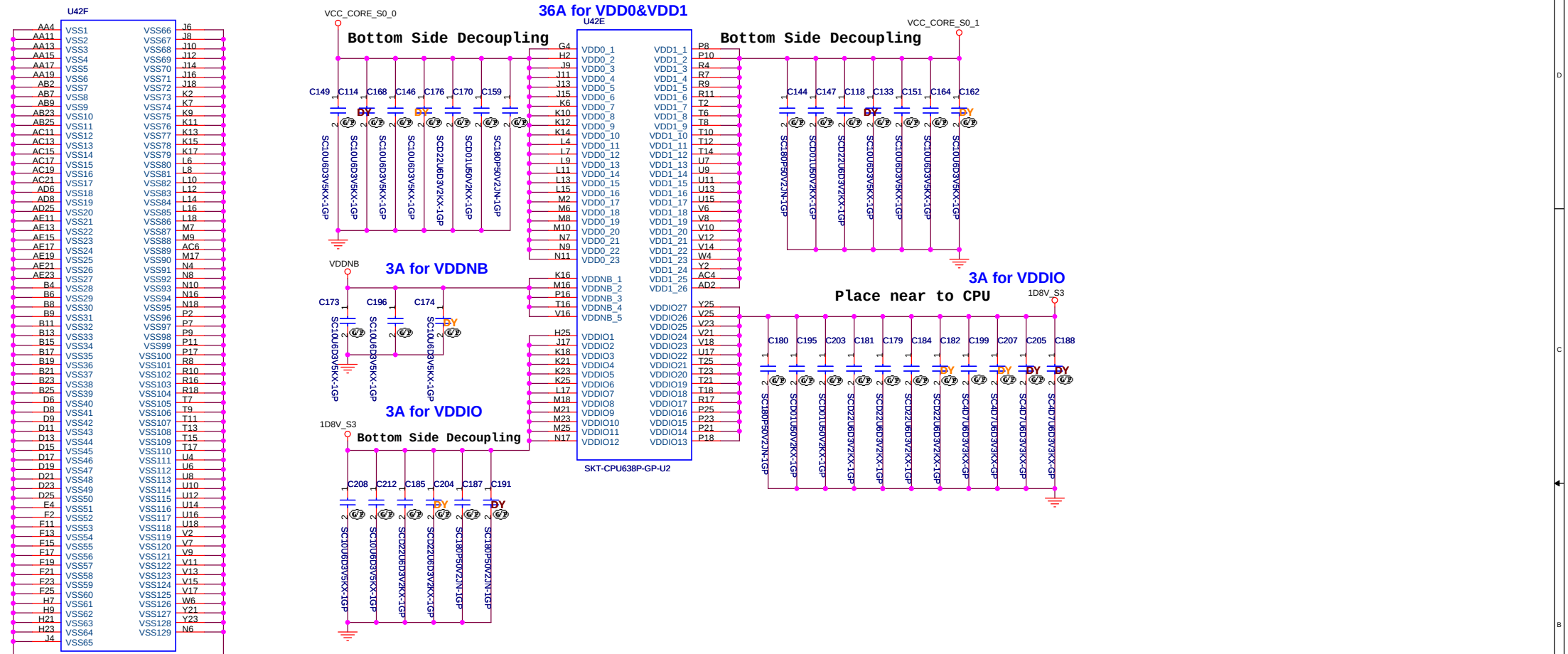
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 6 of 43



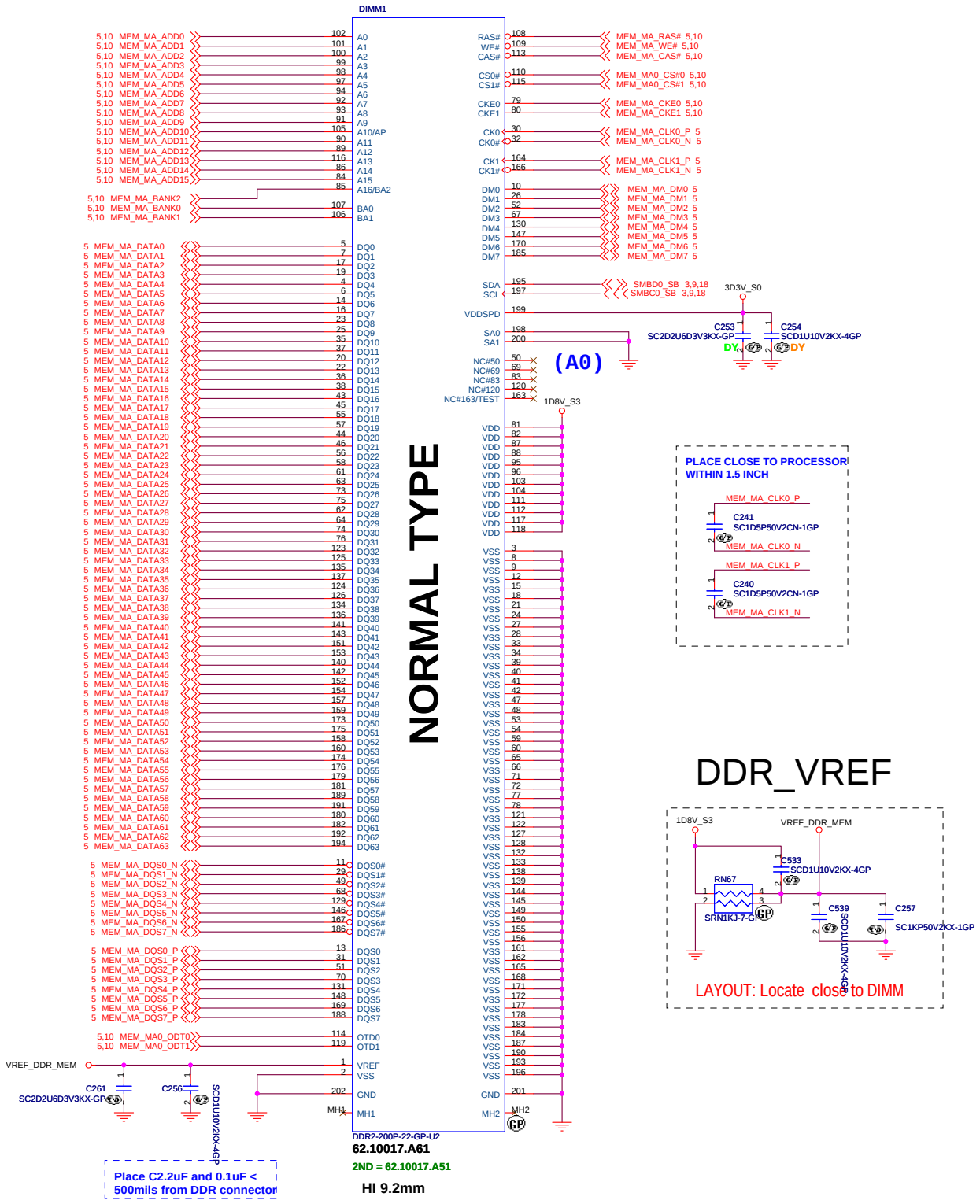
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet of 43



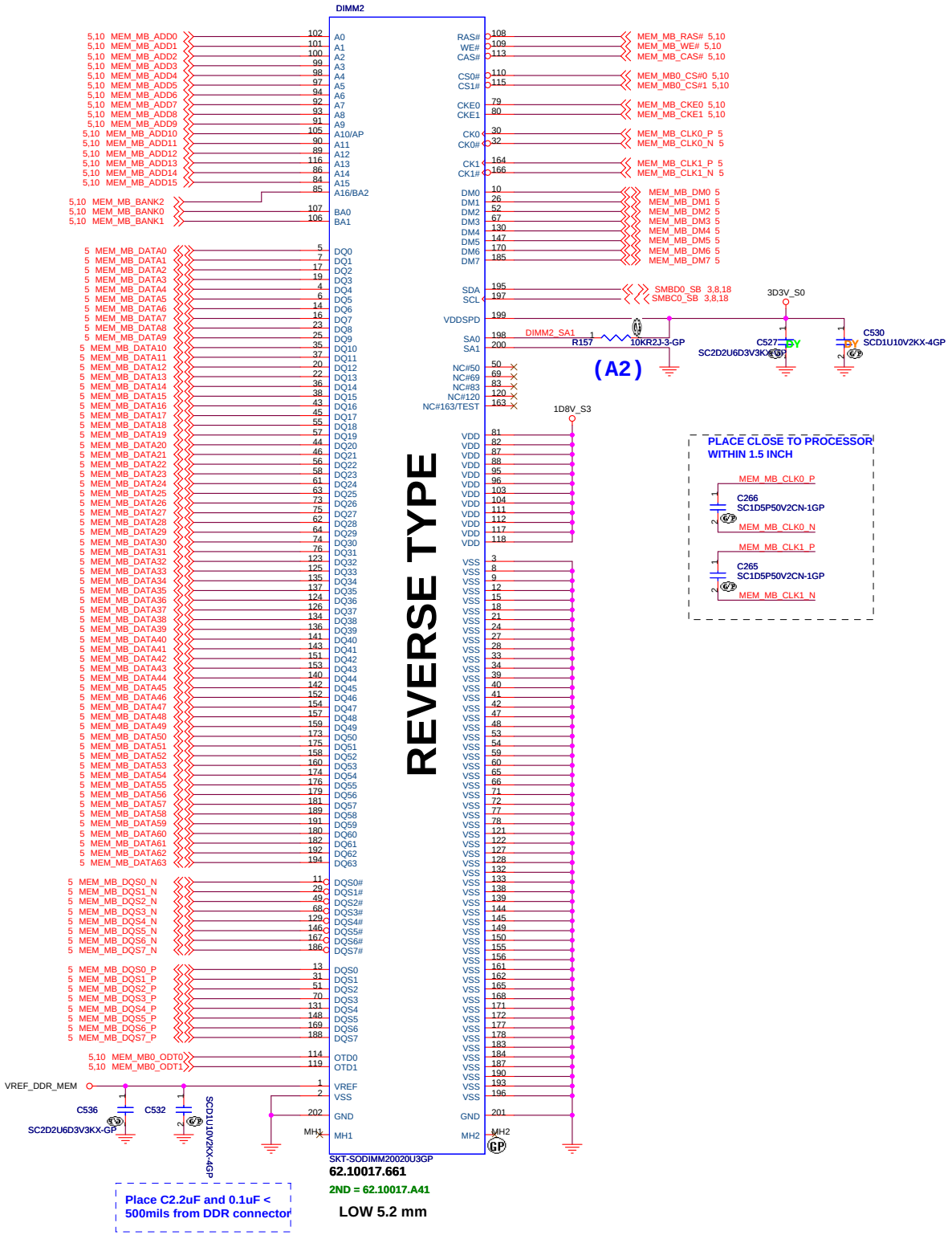
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size	Document Number	Rev
Custom	Cathedral Peak 2A	-1

Date: Friday, August 22, 2008 Sheet 8 of 43



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

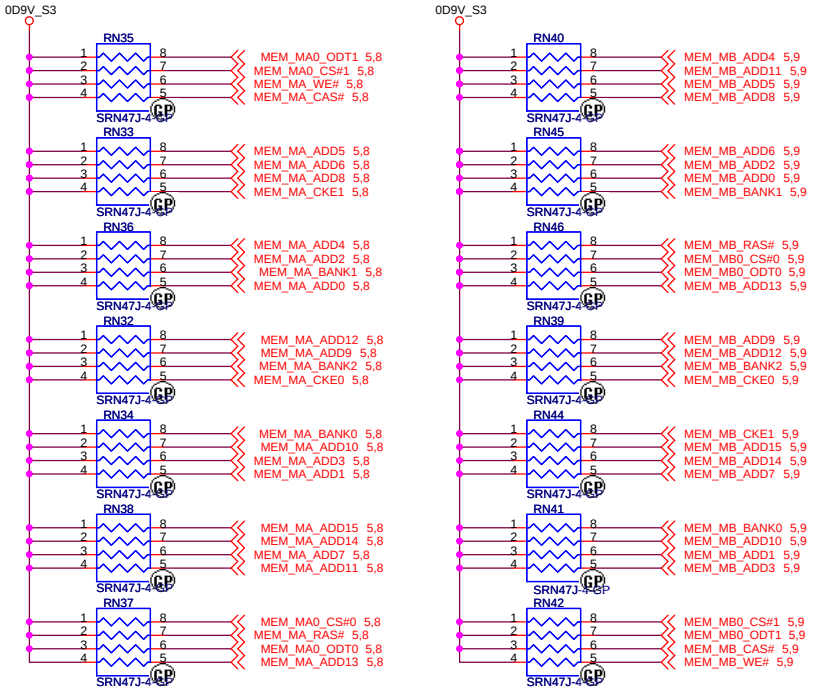
Title: DDR SO-DIMM SKT 2

Size: Custom | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 9 of 43

PARALLEL TERMINATION

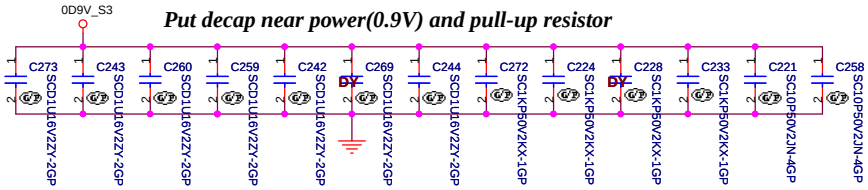
Put decap near power(0.9V) and pull-up resistor



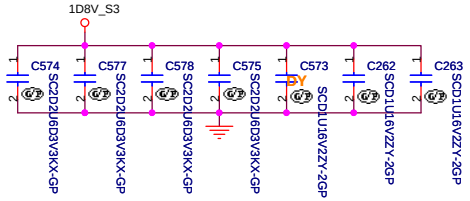
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

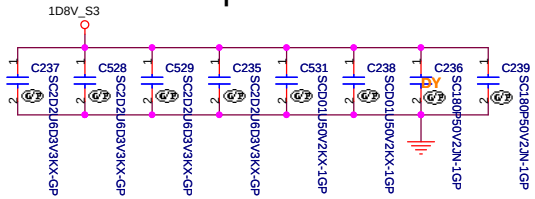


Place these Caps near DM1



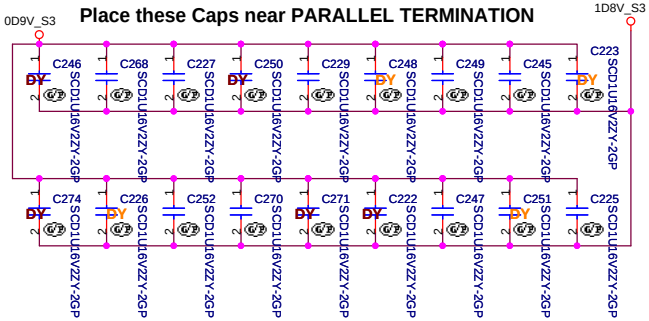
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



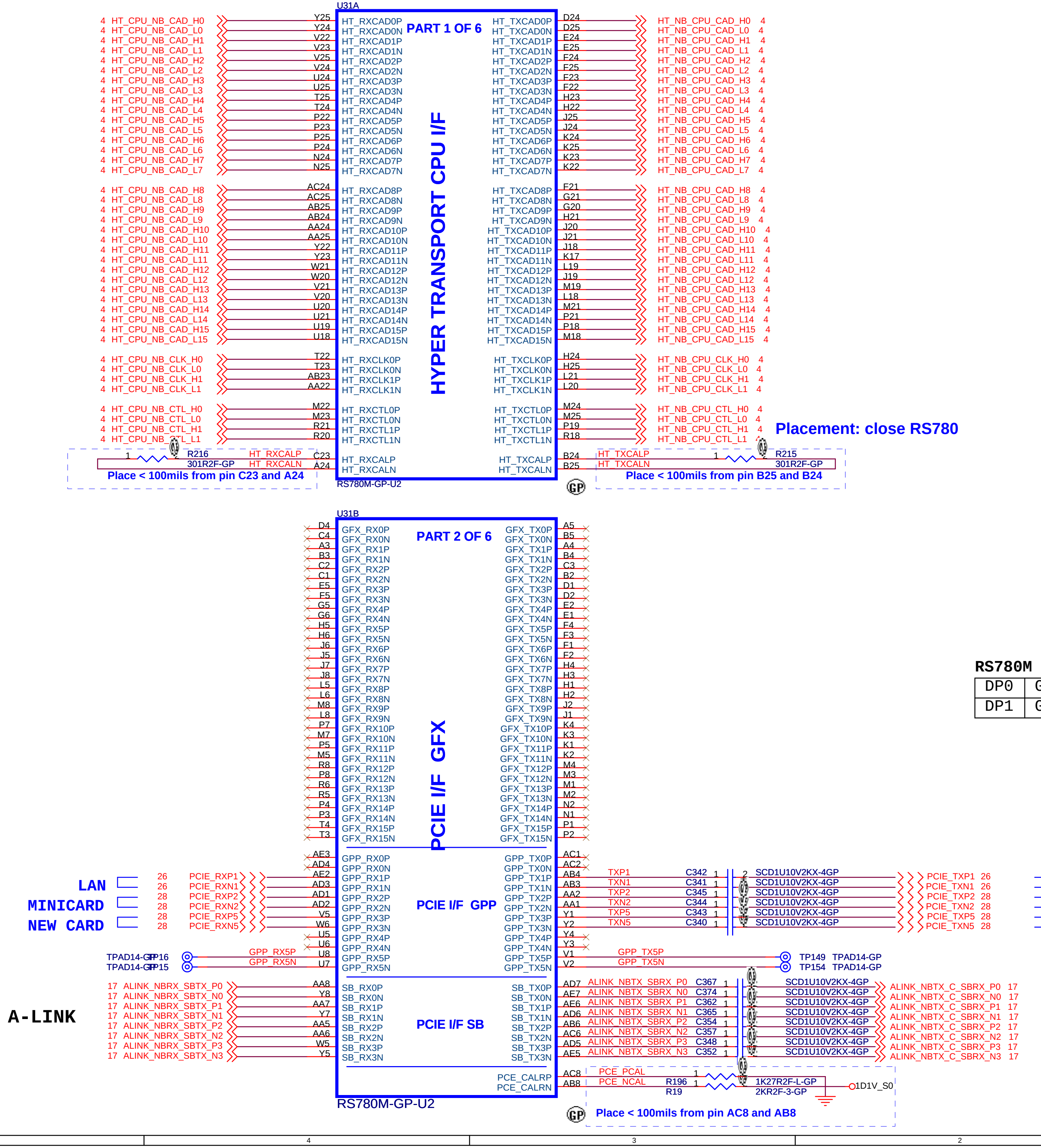
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDR_DAMPING & TERMINATION**

Size	Document Number	Rev
A3	Cathedral Peak 2A	-1

Date: Friday, August 22, 2008 Sheet 10 of 43



RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **ATi-RS780M_HT LINK&PCIe(1/3)**

Size: A3 | Document Number: **Cathedral Peak 2A** | Rev: -1

Date: Friday, August 22, 2008 | Sheet 11 of 43

STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)

*1 :Disable 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

*1 :Disable 0 : Enable

SUS_STAT#

Selects Loading of STRAPS From EEPROM

*1 : Bypass the loading of EEPROM straps and use Hardware Default Values

0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

Close to NB ball

ENABLE External CLK GEN

	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

RS780M-GP-U2

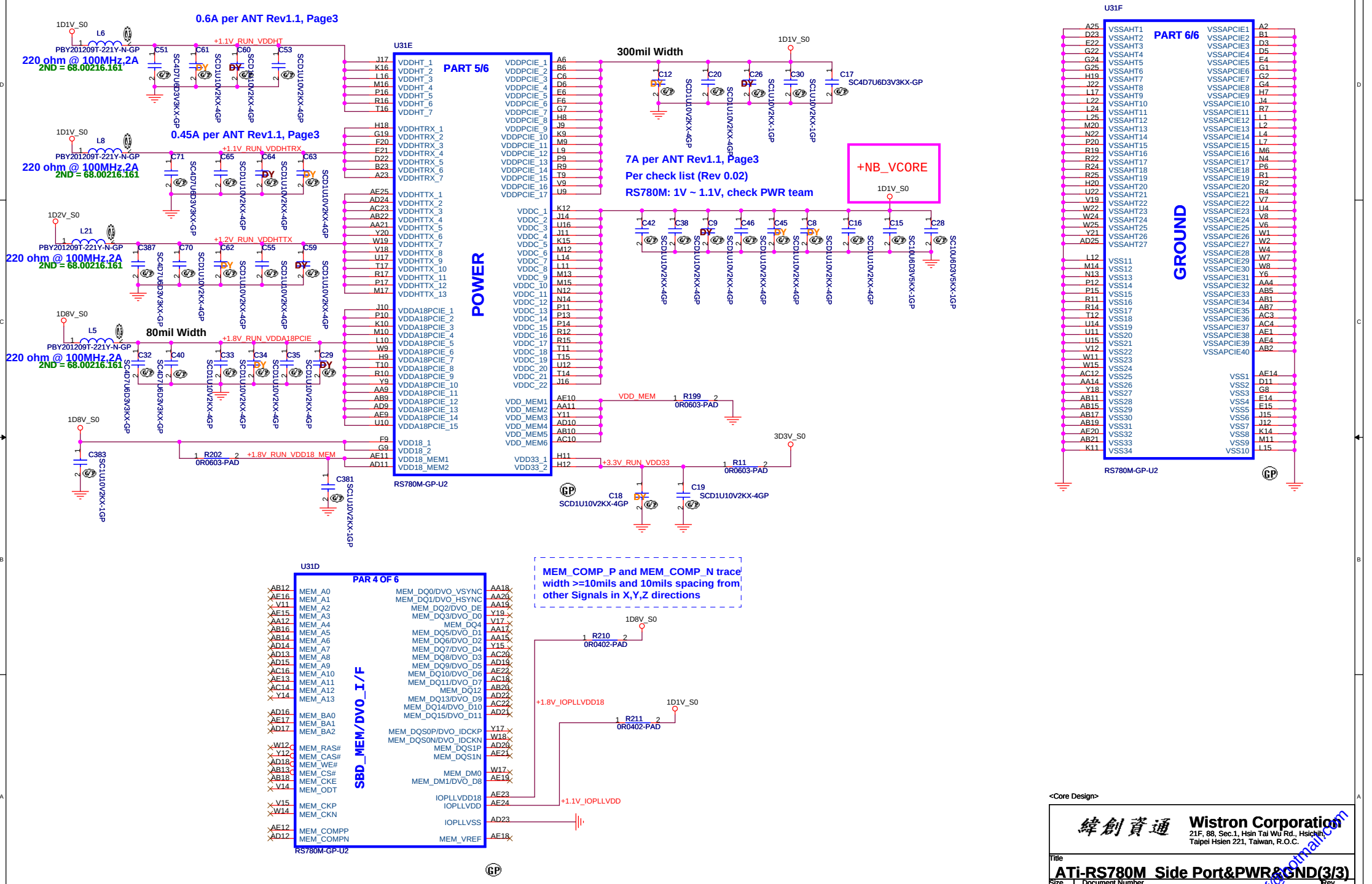
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

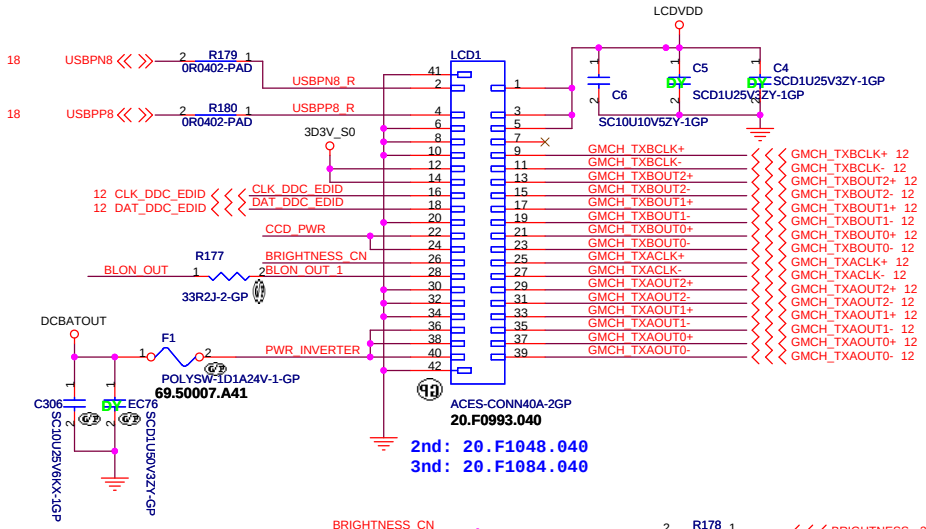
Title: ATi-RS780M LVDS&CRT (2/3)

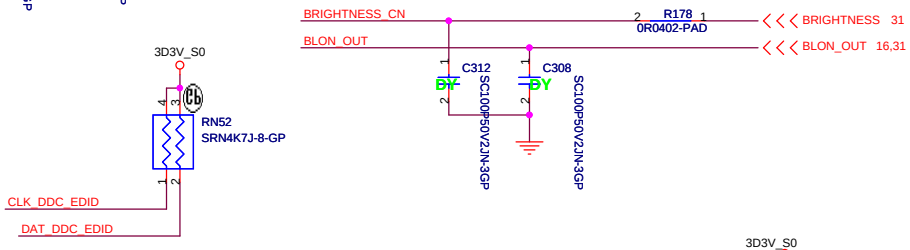
Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

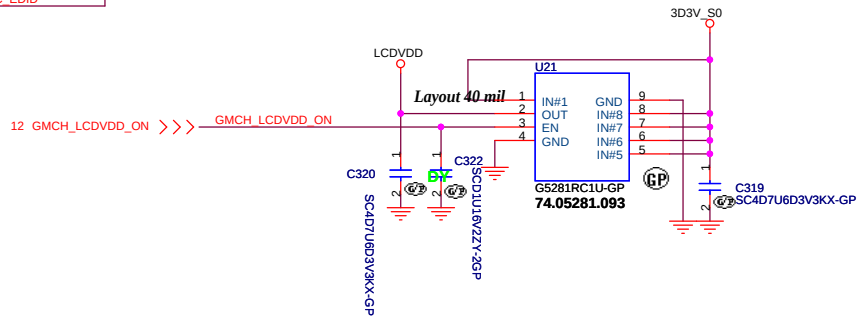
Date: Friday, August 22, 2008 | Sheet 12 of 43

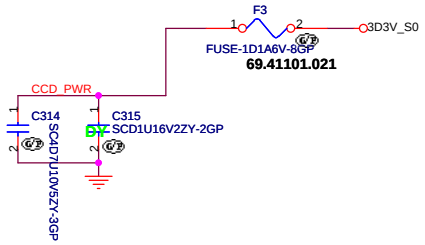

0.6A per ANT Rev1.1, Page3
220 ohm @ 100MHz,2A
2ND = 68.00216.161
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
U31E
PART 5/6
POWER
RS780M-GP-U2
U31F
PART 6/6
GROUND
U31D
PAR 4 OF 6
SBD_MEM/DVO_I/F
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_Side Port&PWR&GND(3/3)
Size A3
Document Number
Cathedral Peak 2A
Rev -1
Date: Friday, August 22, 2008
Sheet 13 of 43

LCD/INVERTER/CCD CONN





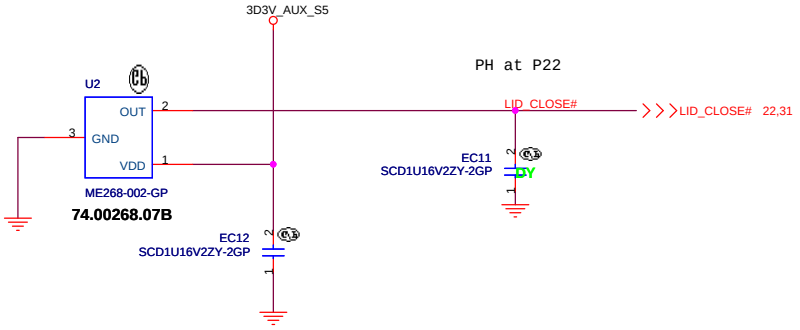




Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch



74.00268.A7B

74.00268.C7B

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

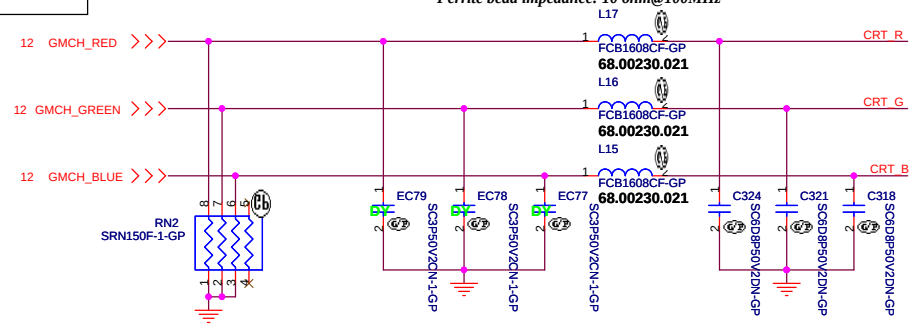
Title: LCD CONN

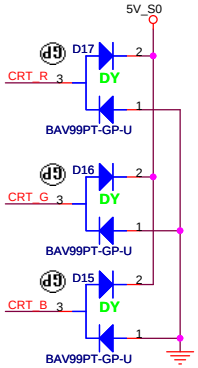
Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 14 of 43

Layout Note:
Place these resistors close to the CRT-out connector

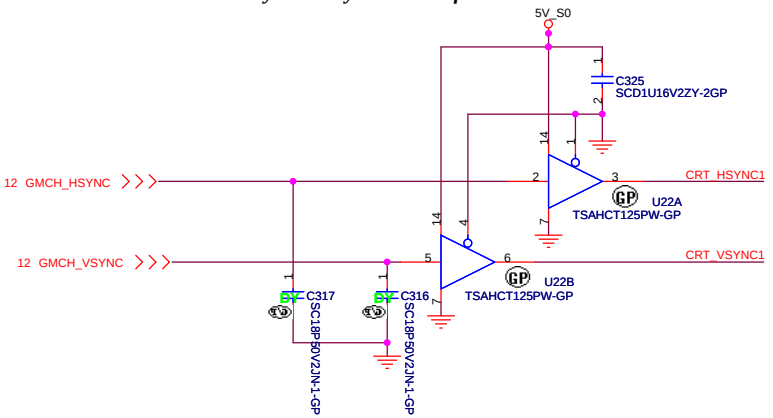
Ferrite bead impedance: 10 ohm@100MHz



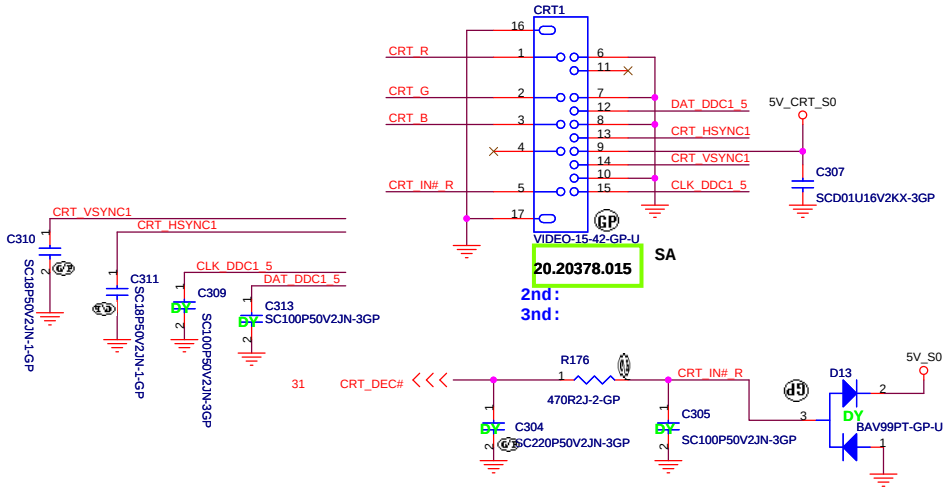


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

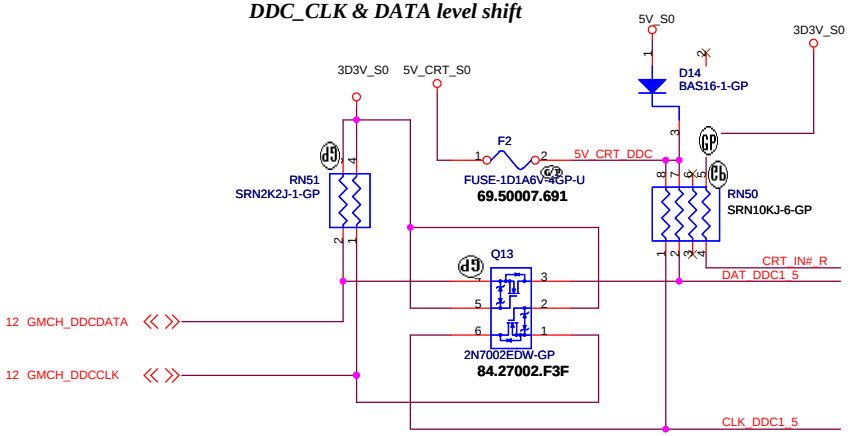
Hsync & Vsync level shift



CRT I/F & CONNECTOR



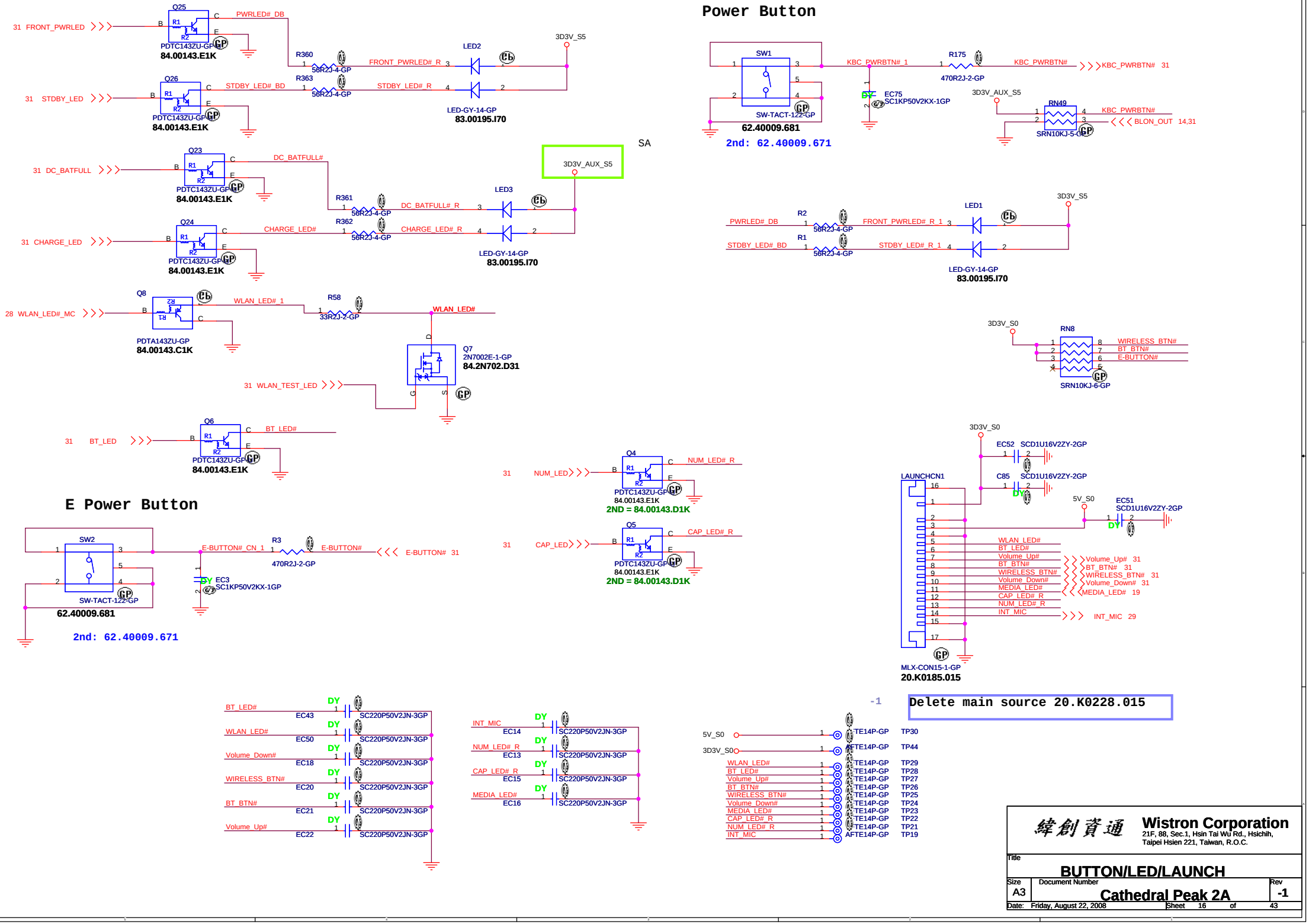
DDC_CLK & DATA level shift

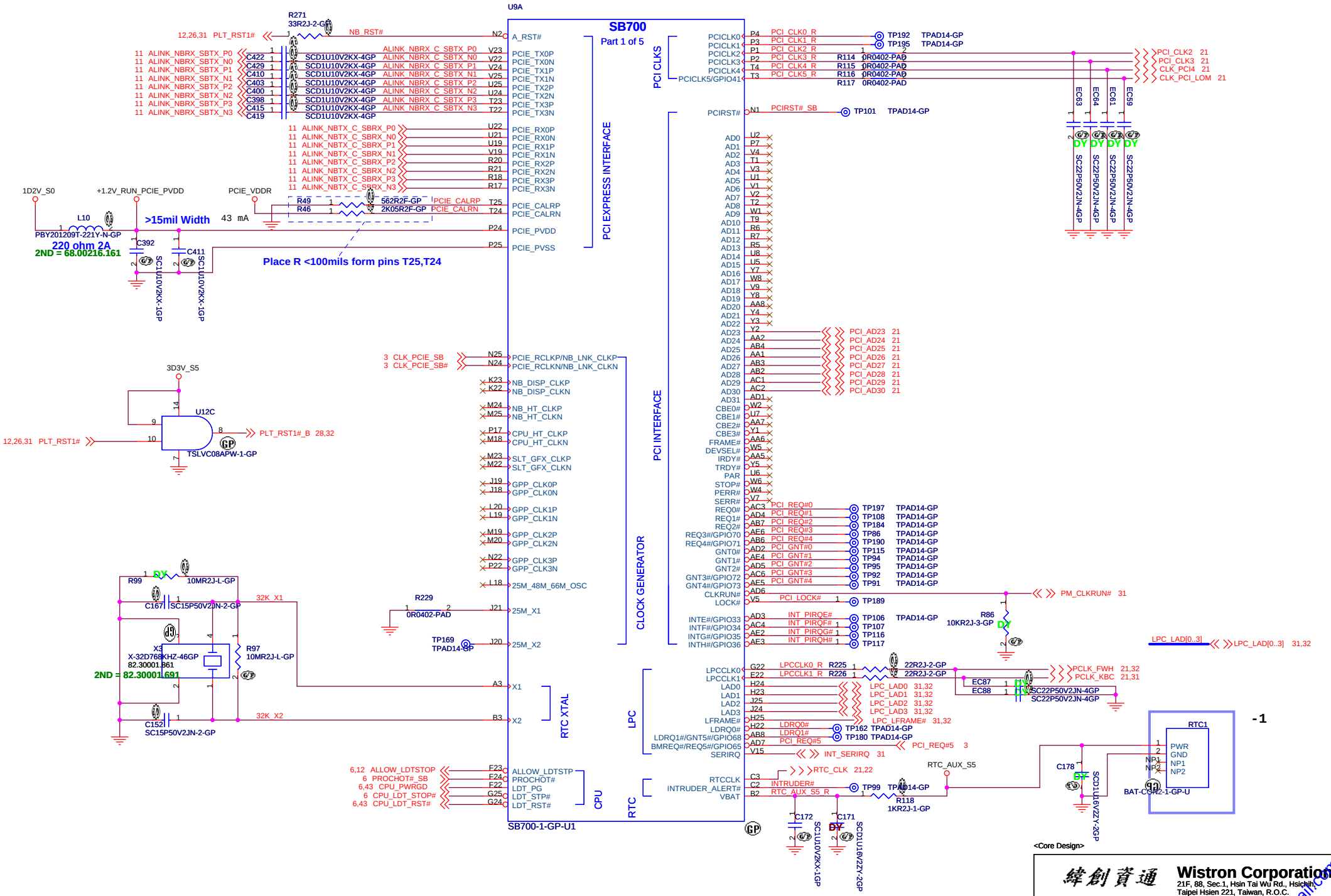


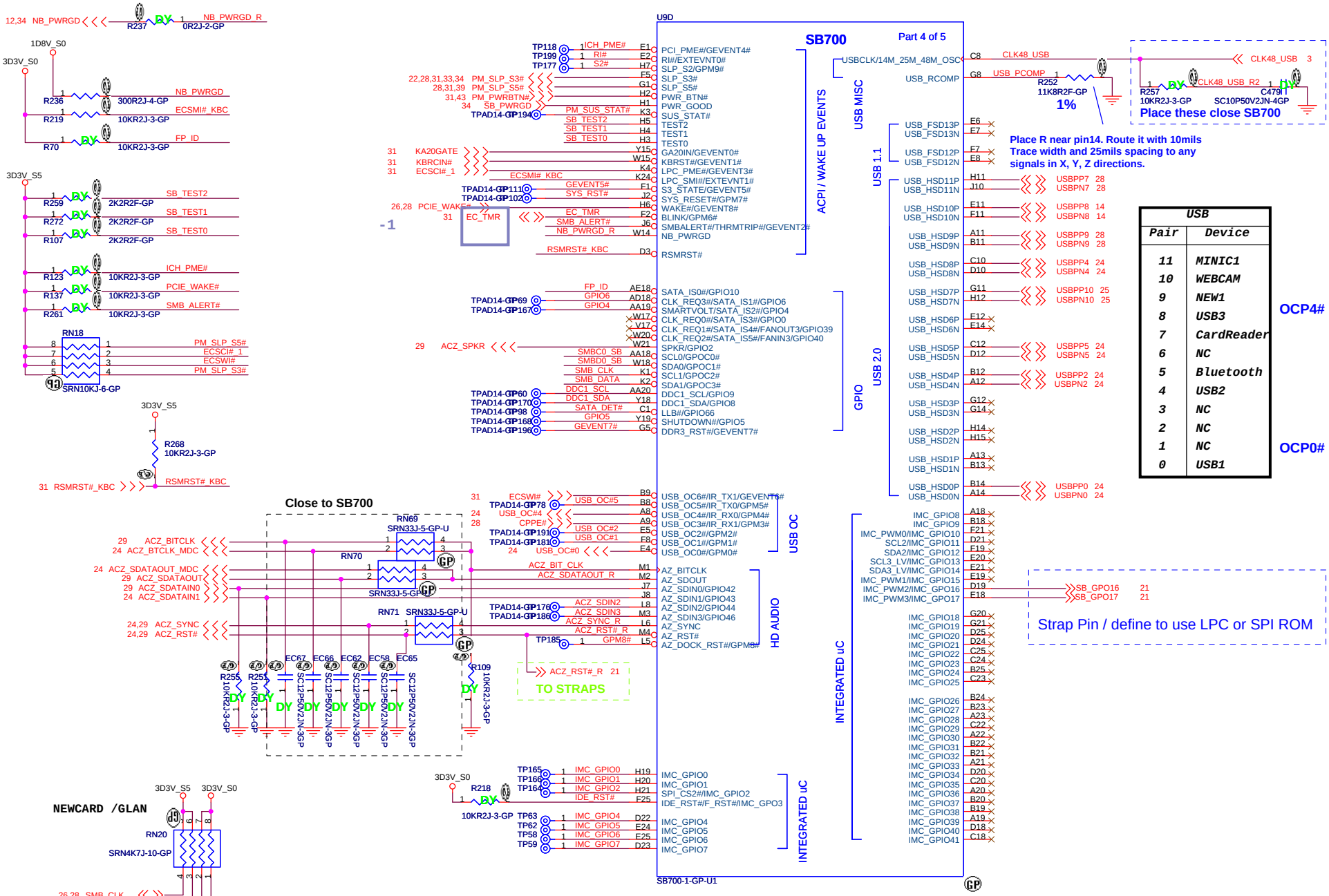
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	CRT Connector	
Size	Document Number: Cathedral Peak 2A	Rev: -1
Date: Friday, August 22, 2008	Sheet 15 of 43	


Power Button
E Power Button
SA
Delete main source 20.K0228.015
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
BUTTON/LED/LAUNCH
Cathedral Peak 2A
Size A3
Rev -1
Date: Friday, August 22, 2008
Sheet 16 of 43


U9A
SB700
Part 1 of 5
SB700-1-GP-U1
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
R271
33R2J-2-GP
NB_RST#
PLT_RST1#
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBRX_C_SBRX_P0
ALINK_NBRX_C_SBRX_N0
ALINK_NBRX_C_SBRX_P1
ALINK_NBRX_C_SBRX_N1
ALINK_NBRX_C_SBRX_P2
ALINK_NBRX_C_SBRX_N2
ALINK_NBRX_C_SBRX_P3
ALINK_NBRX_C_SBRX_N3
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L10
PBY201209T-221Y-N-GP
220 ohm 2A
2ND = 68.00216.161
>15mil Width
43 mA
R49
562R2F-GP
R46
2K05R2F-GP
PCIE_CALRP
PCIE_CALRN
Place R <100mils form pins T25,T24
C392
C411
SC1U10V2KX-1GP
3D3V_S5
U12C
TSLVC08APW-1-GP
PLT_RST1#_B 28,32
3 CLK_PCIE_SB
3 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
R99
10MR2J-L-GP
C167
SC15P50V2JN-2-GP
X3
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
R97
10MR2J-L-GP
C152
32K_X1
32K_X2
R229
0R0402-PAD
TP169
TPAD14-GP
ALLOW_LDTSTP
PROCHOT#_SB
CPU_PWRGD
CPU_LDT_STOP#
CPU_LDT_RST#
LDT_PG
LDT_STP#
LDT_RST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
R114 0R0402-PAD
R115 0R0402-PAD
R116 0R0402-PAD
R117 0R0402-PAD
TP192 TPAD14-GP
TP195 TPAD14-GP
PCI_CLK2 21
PCI_CLK3 21
CLK_PCI4 21
CLK_PCI_LOM 21
EC63
EC64
EC61
EC59
DY
SC22P50V2JN-4GP
PCIRST#
PCIRST# SB
TP101 TPAD14-GP
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
PCI_AD23 21
PCI_AD24 21
PCI_AD25 21
PCI_AD26 21
PCI_AD27 21
PCI_AD28 21
PCI_AD29 21
PCI_AD30 21
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_LOCK#
TP197 TPAD14-GP
TP108 TPAD14-GP
TP184 TPAD14-GP
TP86 TPAD14-GP
TP190 TPAD14-GP
TP115 TPAD14-GP
TP94 TPAD14-GP
TP95 TPAD14-GP
TP92 TPAD14-GP
TP91 TPAD14-GP
TP189
PM_CLKRUN# 31
R86
10KR2J-3-GP
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
TP106 TPAD14-GP
TP107
TP116
TP117
LPC_LAD[0..3]
LPC_LAD[0..3] 31,32
LPCCLK0
LPCCLK1
LPCCLK0_R R225
LPCCLK1_R R226
22R2J-2-GP
PCLK_FWH 21,32
PCLK_KBC 21,31
EC87
EC88
LAD0
LAD1
LAD2
LAD3
LFRAME#
LPC_LAD0 31,32
LPC_LAD1 31,32
LPC_LAD2 31,32
LPC_LAD3 31,32
LPC_LFRAME# 31,32
LDRQ0#
LDRQ1#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
TP162 TPAD14-GP
TP180 TPAD14-GP
PCI_REQ#5
PCI_REQ#5 3
INT_SERIRQ 31
RTCCLK
INTRUDER_ALERT#
VBAT
RTC_CLK 21,22
INTRUDER#
RTC_AUX_S5_R
TP99 TPAD14-GP
R118
1KR2J-1-GP
RTC_AUX_S5
C172
C171
SC1U10V2KX-1GP
SCD1U16V2ZY-2GP
C178
SCD1U16V2ZY-2GP
RTC1
PWR
GND
NP1
NP2
BAT-CON2-1-GP-U
-1
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size
A3
Document Number
Cathedral Peak 2A
Rev
-1
Date: Friday, August 22, 2008
Sheet 33 of 43



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_USB&GPIO_(2/5)

Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 18 of 43

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD
SATA ODD

C300 SCD01U50V2KX-1GP
C299 SCD01U50V2KX-1GP
C460 SCD01U50V2KX-1GP
C465 SCD01U50V2KX-1GP
C571 SCD01U50V2KX-1GP
C567 SCD01U50V2KX-1GP
C461 SCD01U50V2KX-1GP
C457 SCD01U50V2KX-1GP

SATA_TXP0 SATA_TXN0 SATA_RXN0 SATA_RXP0 SATA_TXP1 SATA_TXN1 SATA_RXN1 SATA_RXP1

SATA_TXP0_C SATA_TXN0_C SATA_RXN0_C SATA_RXP0_C SATA_TXP1_C SATA_TXN1_C SATA_RXN1_C SATA_RXP1_C

U9B

SB700
Part 2 of 5

SATA_TX0P SATA_TX0N SATA_RX0N SATA_RX0P SATA_TX1P SATA_TX1N SATA_RX1N SATA_RX1P SATA_TX2P SATA_TX2N SATA_RX2N SATA_RX2P SATA_TX3P SATA_TX3N SATA_RX3N SATA_RX3P SATA_TX4P SATA_TX4N SATA_RX4N SATA_RX4P SATA_TX5P SATA_TX5N SATA_RX5N SATA_RX5P SATA_CAL SATA_X1 SATA_X2 SATA_ACT#/GPIO67 PLLVDD_SATA XTLVDD_SATA

SERIAL ATA

IDE_IORDY IDE_IRQ IDE_A0 IDE_A1 IDE_A2 IDE_DACK# IDE_DRQ IDE_IOR# IDE_IOW# IDE_CS1# IDE_CS3#
IDE_D0/GPIO15 IDE_D1/GPIO16 IDE_D2/GPIO17 IDE_D3/GPIO18 IDE_D4/GPIO19 IDE_D5/GPIO20 IDE_D6/GPIO21 IDE_D7/GPIO22 IDE_D8/GPIO23 IDE_D9/GPIO24 IDE_D10/GPIO25 IDE_D11/GPIO26 IDE_D12/GPIO27 IDE_D13/GPIO28 IDE_D14/GPIO29 IDE_D15/GPIO30

PCB_VER0 PCB_VER1 PCB_VER2
CLK_ID_0 CLK_ID_1

ATA 66/100/133

SPI_DI/GPIO12 SPI_DO/GPIO11 SPI_CLK/GPIO47 SPI_HOLD#/GPIO31 SPI_CS#/GPIO32
LAN_RST#/GPIO13 ROM_RST#/GPIO14

SB_SPI_MISO SPI_MOSI_R ICH_SPICLK SB_SPI_HOLD ICH_SPICS0#
LAN_RST# ROM_RST#

TP187 TPAD14-GP TP109 TPAD14-GP TP110 TPAD14-GP TP200 TPAD14-GP TP96 TPAD14-GP
TP171 TPAD14-GP TP97 TPAD14-GP

SPI ROM

FANOUT0/GPIO3 FANOUT1/GPIO48 FANOUT2/GPIO49 FANIN0/GPIO50 FANIN1/GPIO51 FANIN2/GPIO52 TEMP_COMM TEMPIN0/GPIO61 TEMPIN1/GPIO62 TEMPIN2/GPIO63 TEMPIN3/TALERT#/GPIO64 VIN0/GPIO53 VIN1/GPIO54 VIN2/GPIO55 VIN3/GPIO56 VIN4/GPIO57 VIN5/GPIO58 VIN6/GPIO59 VIN7/GPIO60

ALERT# 22
PSW_CLR#

HW MONITOR

AVDD AVSS

SB700-1-GP-U1

SB

C134 SC12P50V2JN-3GP
X2 XTAL-25MHZ-102-GP 82.30020.851
2ND = 82.30020.791
R83 10MR2J-L-GP
C148 SC15P50V2JN-2-GP
R243 1KR2F-3-GP
SATA_X2_R
R79 300R2J-4-GP
16 MEDIA_LED#
93 mA

Very Close to SB700

1D2V_S0 PLLVDD_SATA >15mil Width
R250 0R0603-PAD
C463 SC1U10V2KX-1GP
C464 DY SCD1U10V2KX-4GP

3D3V_S0 XTLVDD_SATA >15mil Width
R239 0R0603-PAD
C454 SC1U10V2KX-1GP

3D3V_S0
RN16 SRN10KJ-6-GP
MEDIA_LED# PSW_CLR# ALERT#

AVDD_HWM >15mil Width
R260 0R0603-PAD
3D3V_S5
C480 SCD1U10V2KX-4GP
C141 DY SC2D2U6D3V3KX-GP
Layout connect to Cap then GND

3D3V_S0
R60 10KR2J-3-GP DY
R55 10KR2J-3-GP DY
R52 10KR2J-3-GP
R59 10KR2J-3-GP
R54 10KR2J-3-GP
R51 10KR2J-3-GP DY
PCB_VER2 PCB_VER1 PCB_VER0

PlanarID
(2,1,0)
SA: 0,0,0
SB: 0,0,1
-1: 0,1,0
-2: 0,1,1

Dummy CKG select
-1

3D3V_S0
R67 10KR2J-3-GP RTM
R63 10KR2J-3-GP SEG
R66 10KR2J-3-GP ICS+SEG
R62 10KR2J-3-GP ICS+RTM
CLK_ID_1 CLK_ID_0

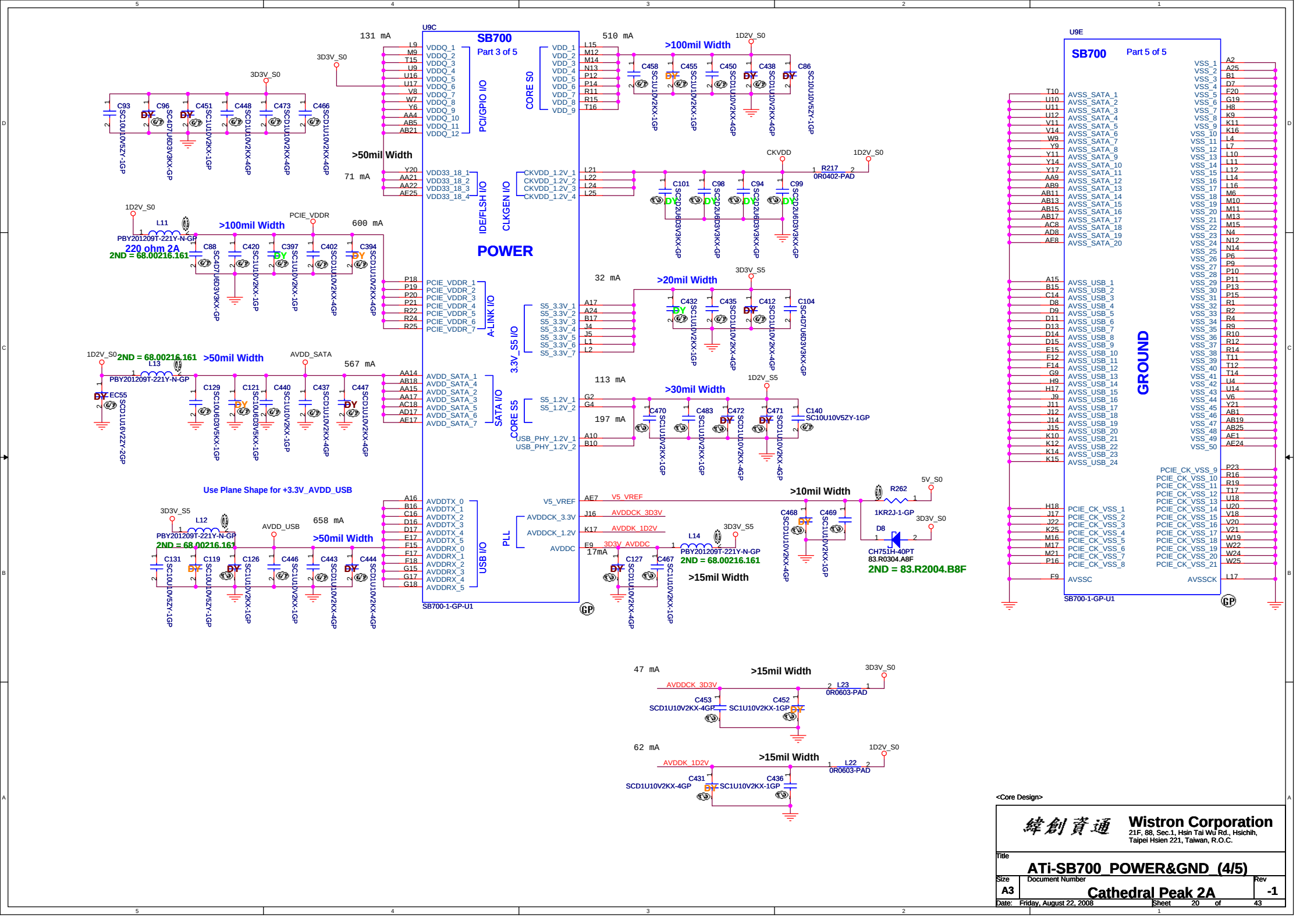
CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

PSW_CLR#
G10
GAP-OPEN

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_SATA-IDE_(3/5)
Size: A3
Document Number: Cathedral Peak2A
Rev: -1
Date: Friday, August 22, 2008
Sheet 19 of 43


SB700
Part 3 of 5
U9C
131 mA
3D3V_S0
>50mil Width
71 mA
PCI/GPIO I/O
CORE S0
IDE/FLSH I/O
CLKGEN I/O
POWER
510 mA
>100mil Width
1D2V_S0
CKVDD
R217
0R0402-PAD
PCIE_VDDR
600 mA
220 ohm 2A
2ND = 68.00216.161
A-LINK I/O
32 mA
>20mil Width
3D3V_S5
3.3V_S5 I/O
113 mA
>30mil Width
1D2V_S5
197 mA
SATA I/O
CORE S5
AVDD_SATA
567 mA
>50mil Width
Use Plane Shape for +3.3V_AVDD_USB
AVDD_USB
658 mA
USB I/O
PLL
V5_VREF
AVDDCK_3D3V
AVDDCK_1.2V
AVDDC
AVDDK_1D2V
17mA
>15mil Width
>10mil Width
5V_S0
1KR2J-1-GP
CH751H-40PT
83.R0304.A8F
2ND = 83.R2004.B8F
SB700-1-GP-U1
47 mA
62 mA
L23
0R0603-PAD
L22
0R0603-PAD
U9E
SB700
Part 5 of 5
GROUND
AVSS_SATA_1
AVSS_USB_1
PCIE_CK_VSS_1
AVSSC
AVSSCK
VSS_1
SB700-1-GP-U1
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_POWER&GND_(4/5)
Size
A3
Document Number
Cathedral Peak 2A
Rev
-1
Date: Friday, August 22, 2008
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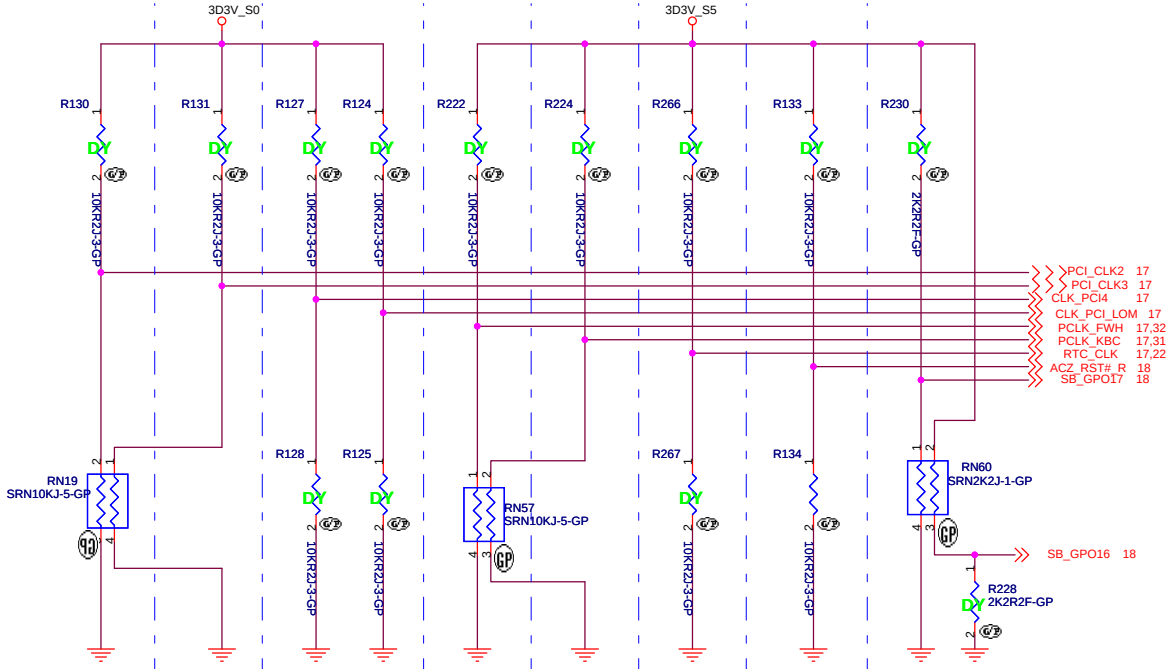
REQUIRED STRAPS

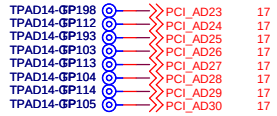
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

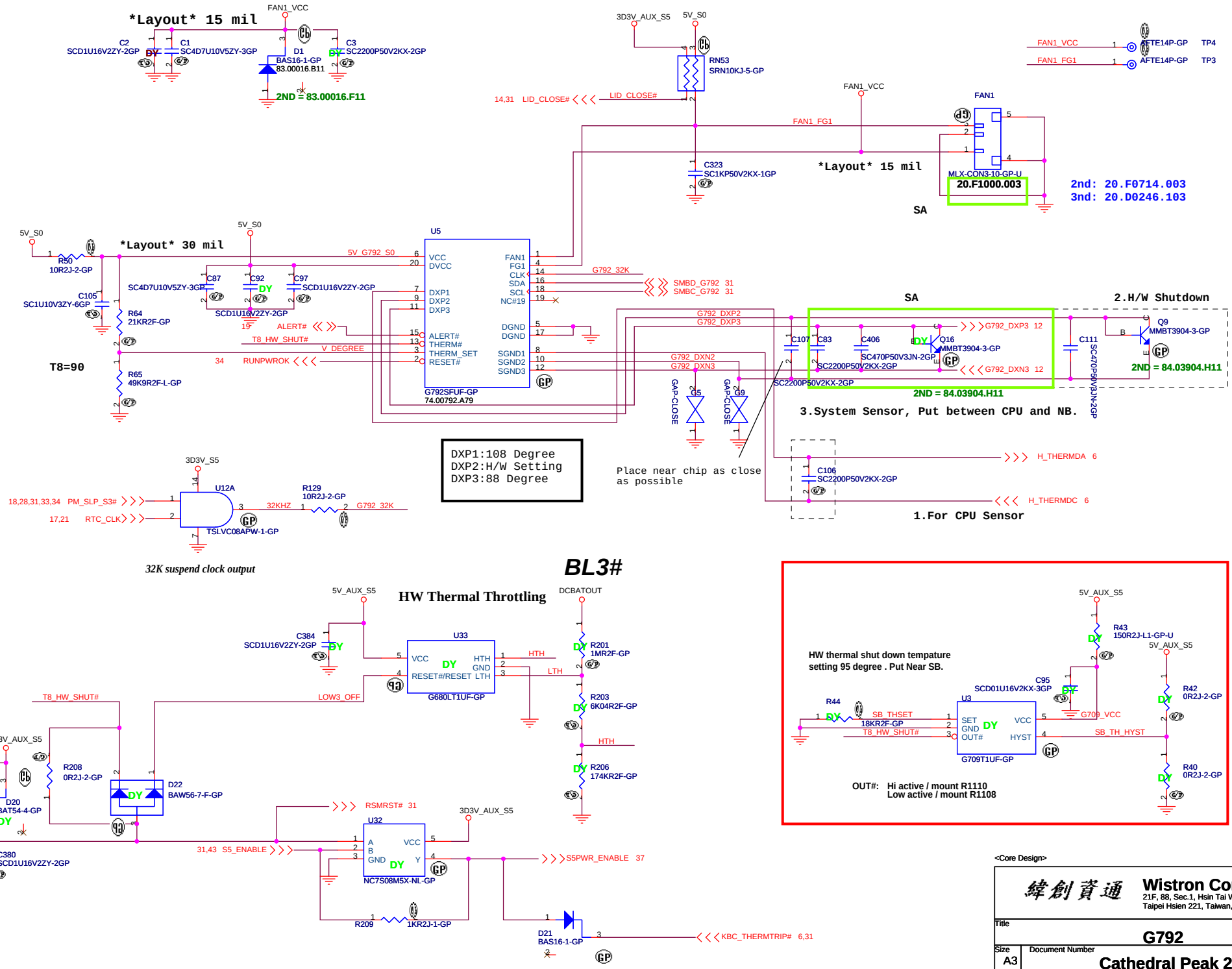
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 21 of 43



<Core Design>

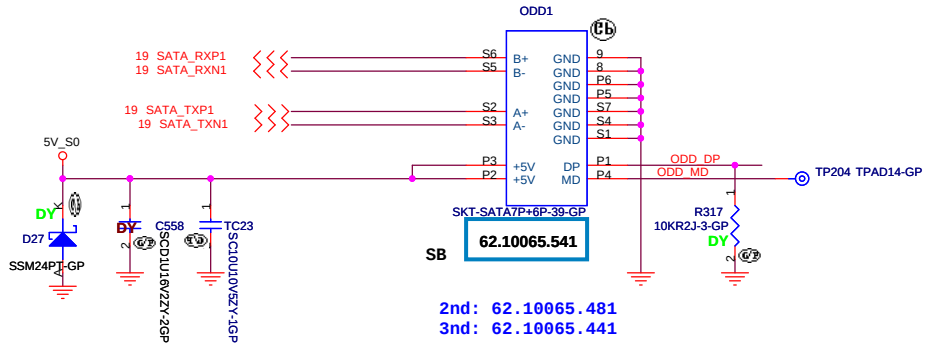
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

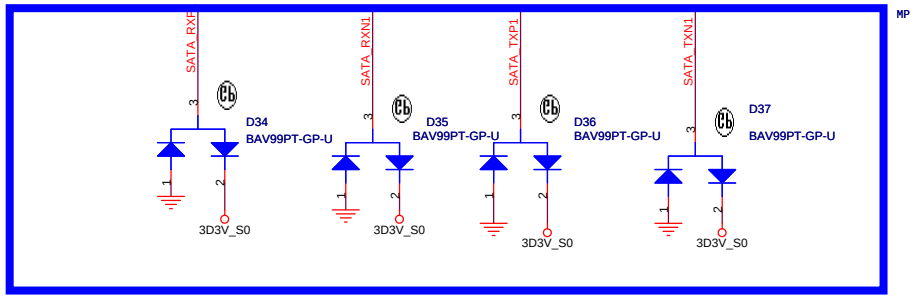
Title: **G792**

Size	Document Number	Rev
A3	**Cathedral Peak 2A**	-1

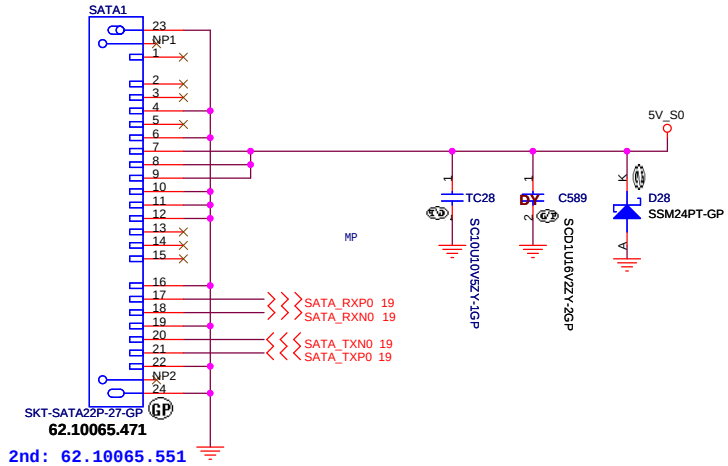
Date: Friday, August 22, 2008 Sheet 22 of 43

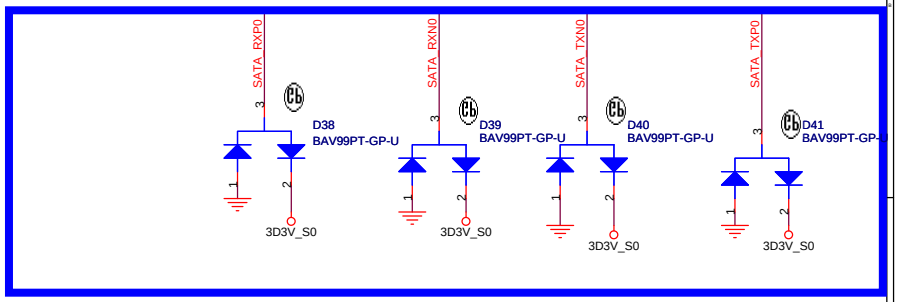
SATA ODD Connector





SATA Connector





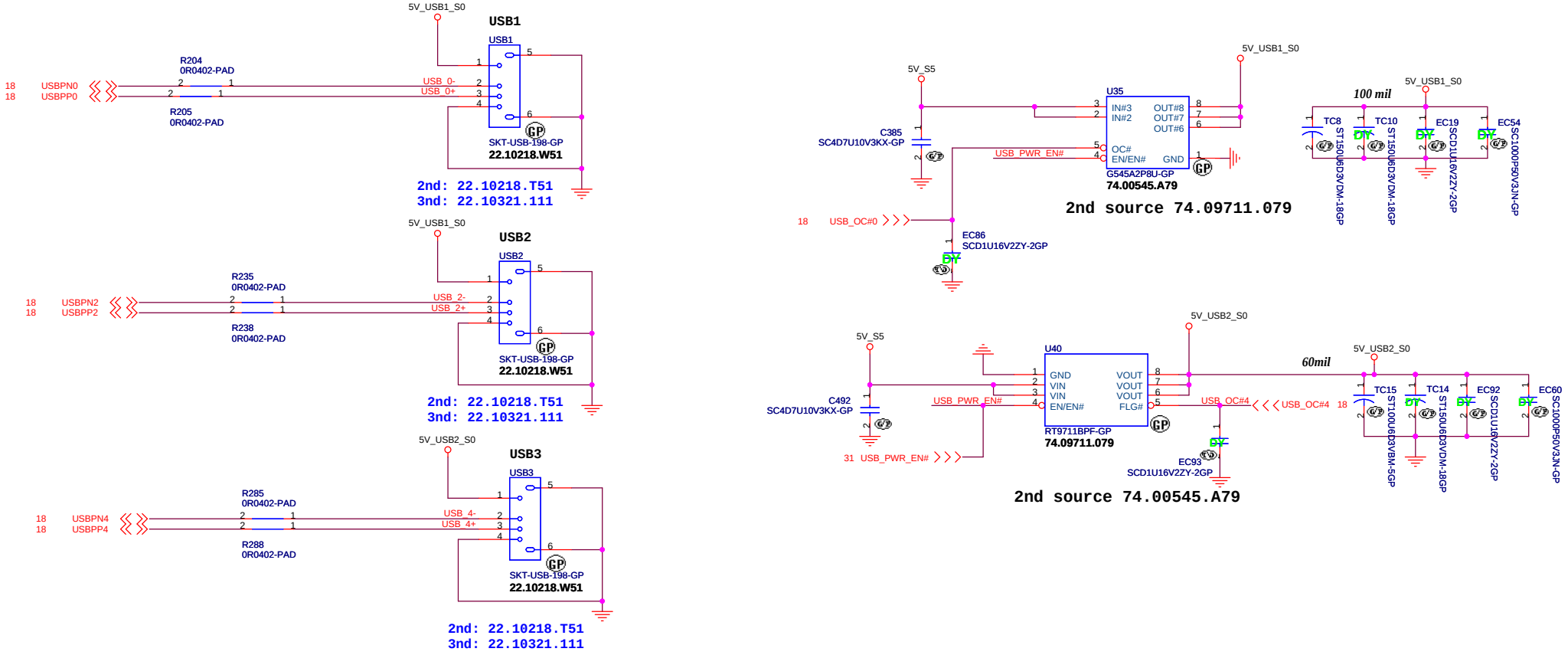
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HDD & CDROM

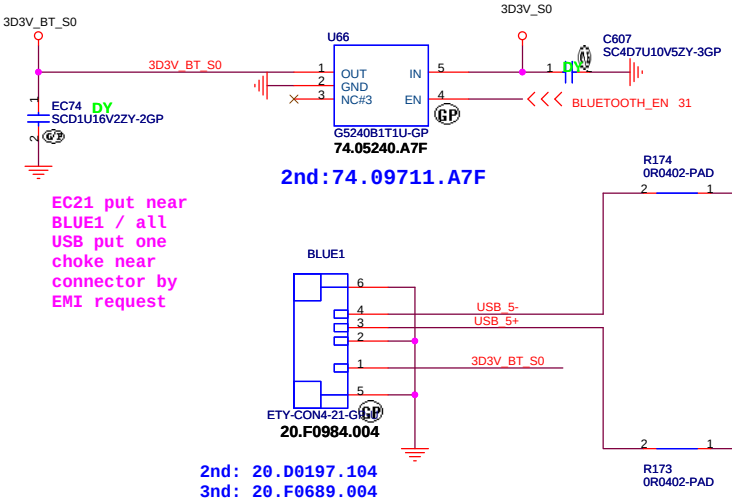
Size | Document Number: Cathedral Peak 2A | Rev: -1

Date: Friday, August 22, 2008 | Sheet 23 of 43

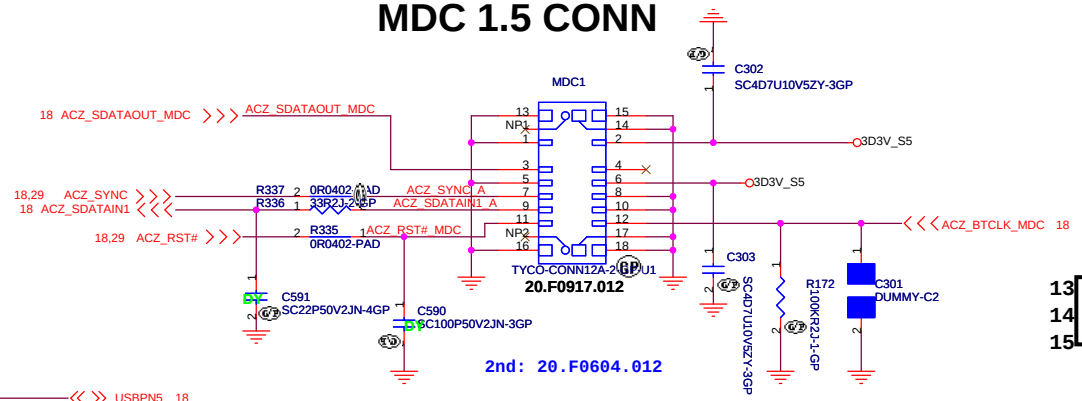


BLUETOOTH MODULE

1.5A / High Active Voltage 2V

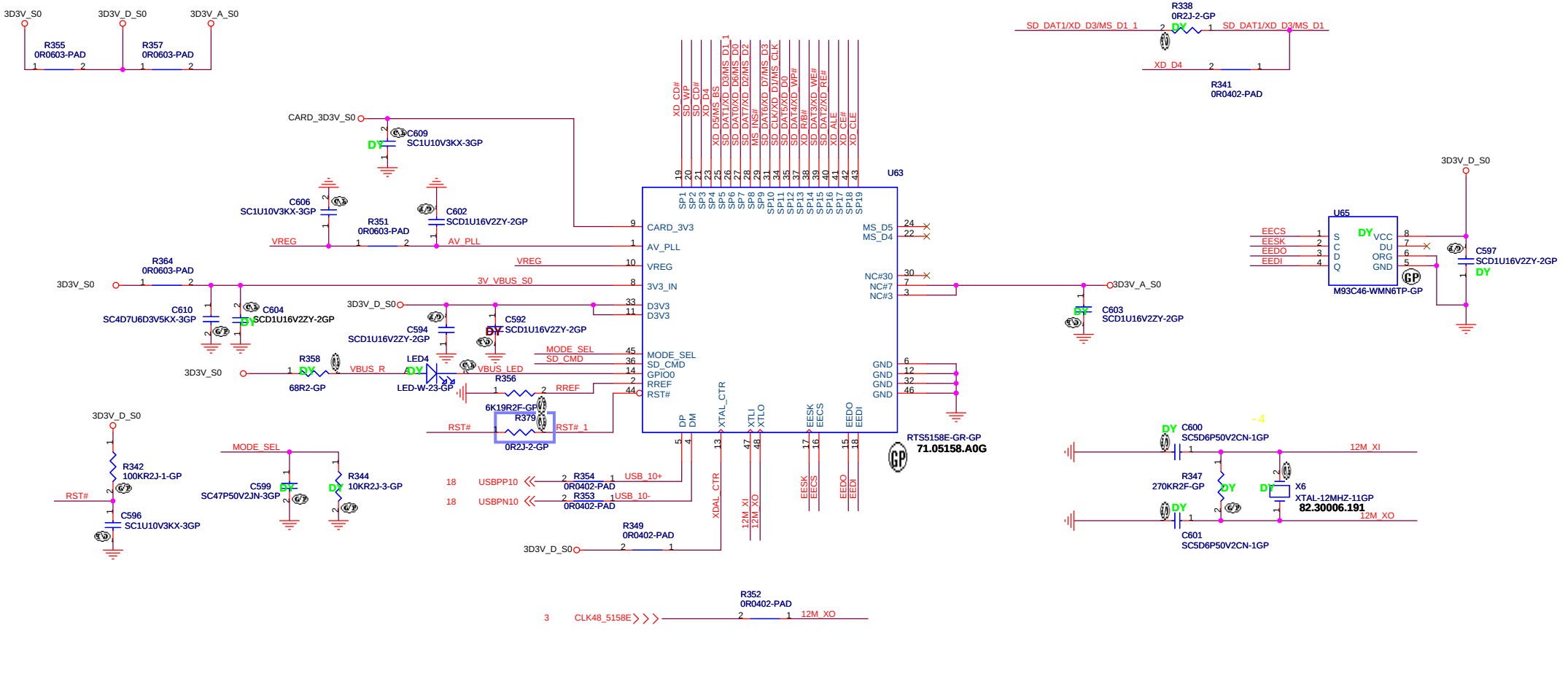


MDC 1.5 CONN

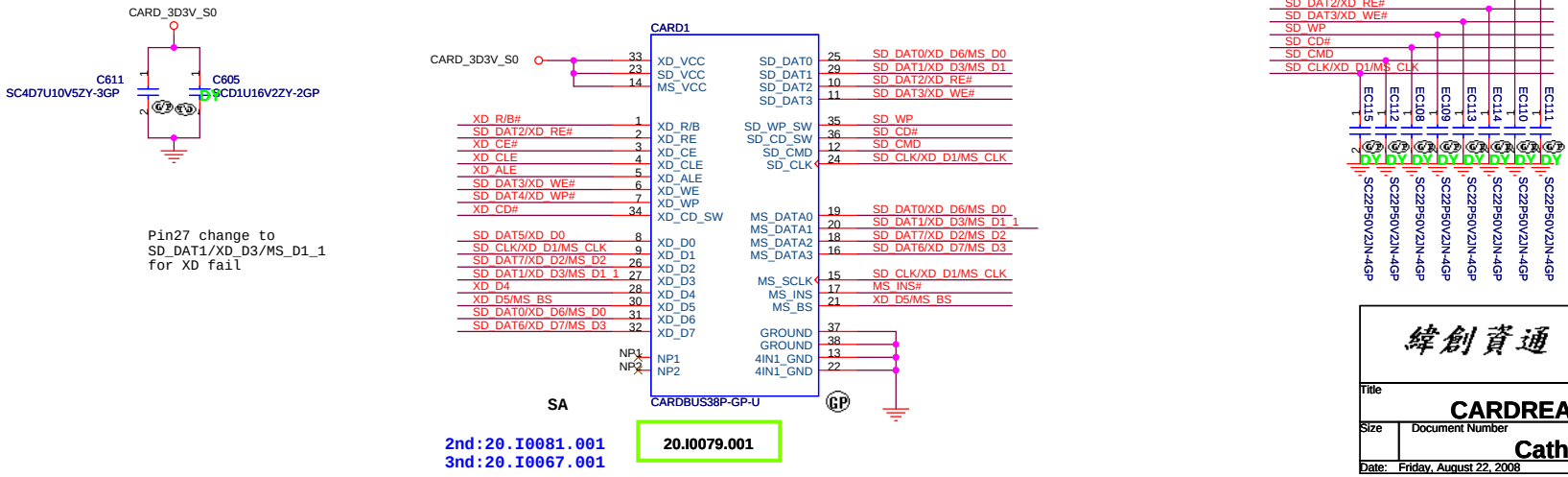


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	USB/BLUETOOTH/MDC	
Size	Document Number: Cathedral Peak 2A	Rev: -1
Date: Friday, August 22, 2008	Sheet 24 of 43	

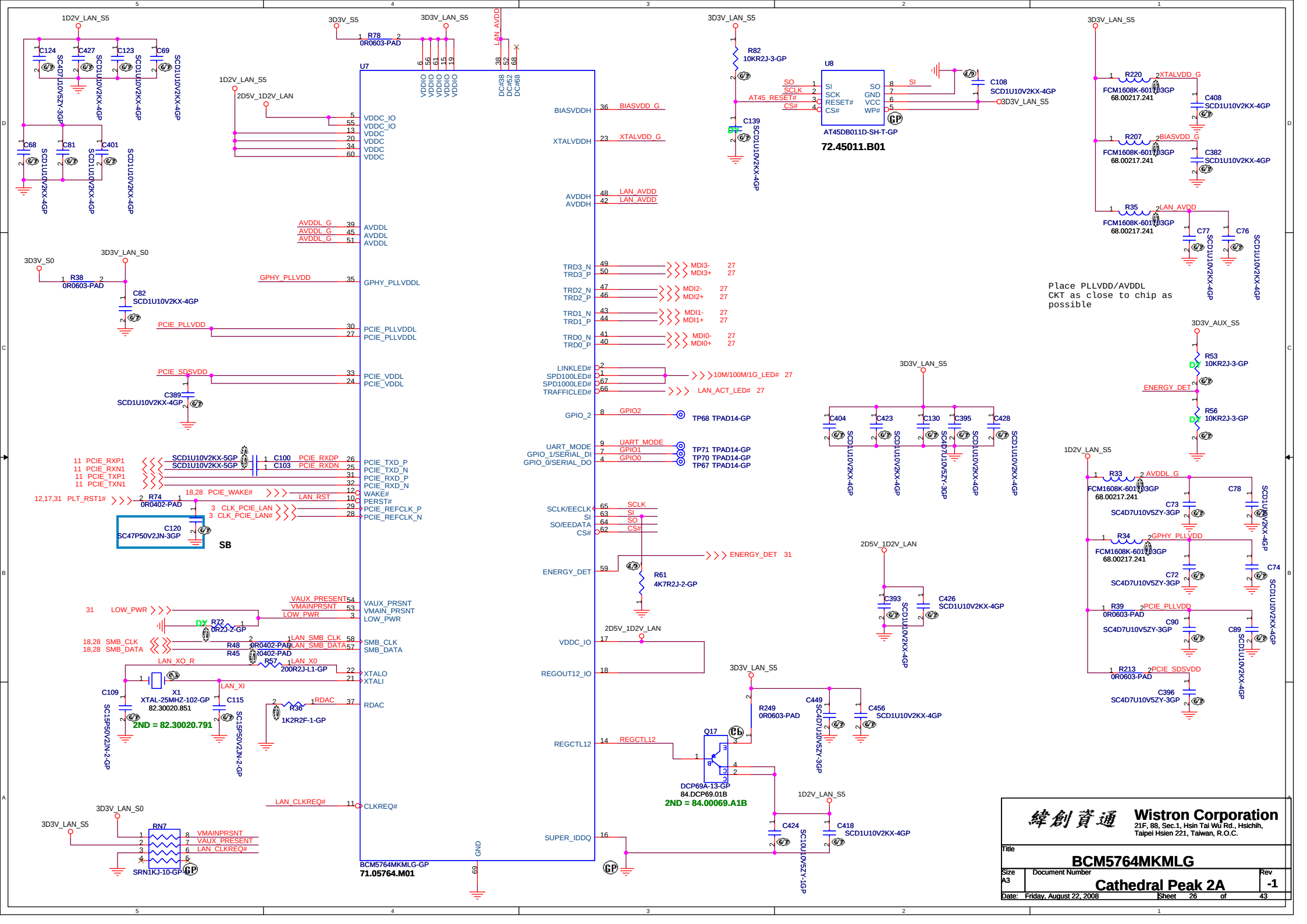


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



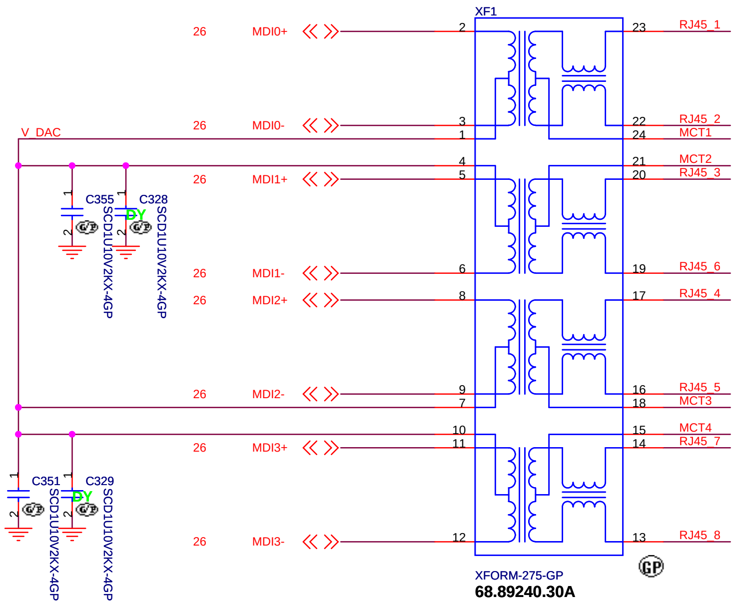
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

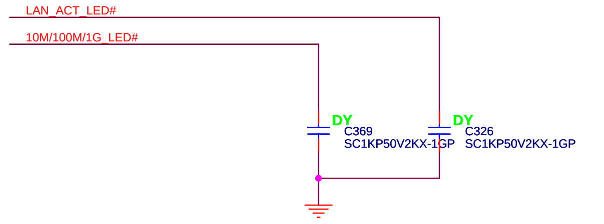
Title	CARDREADER- RTS5158E	
Size	Document Number: Cathedral Peak 2A	Rev: -1
Date: Friday, August 22, 2008	Sheet 25 of 43	


U7
BCM5764MKMLG-GP
71.05764.M01
Place PLLVDD/AVDDL
CKT as close to chip as
possible
U8
AT45DB011D-SH-T-GP
72.45011.B01
X1
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
Q17
DCP69A-13-GP
84.DCP69.01B
2ND = 84.00069.A1B
SB
RN7
SRN1KJ-10-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
BCM5764MKMLG
Size
A3
Document Number
Cathedral Peak 2A
Rev
-1
Date: Friday, August 22, 2008
Sheet 26 of 43

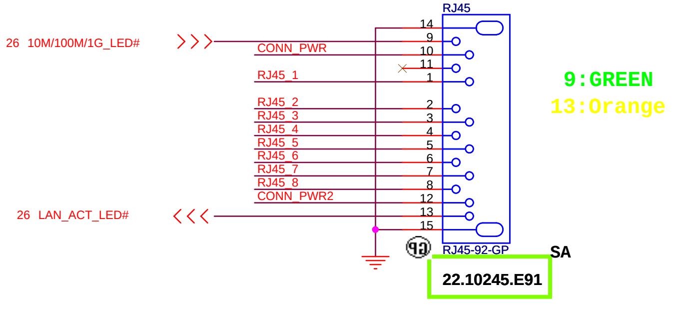
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.





LAN Connector

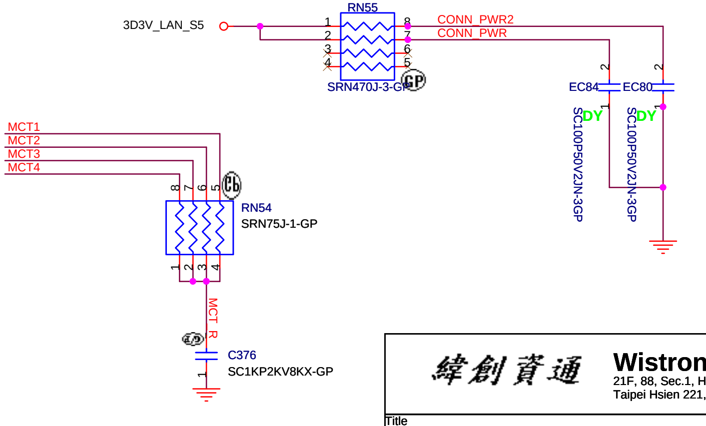


2nd:

LAN Link: Green(9), behavior is the same for 10/100/1000 bits

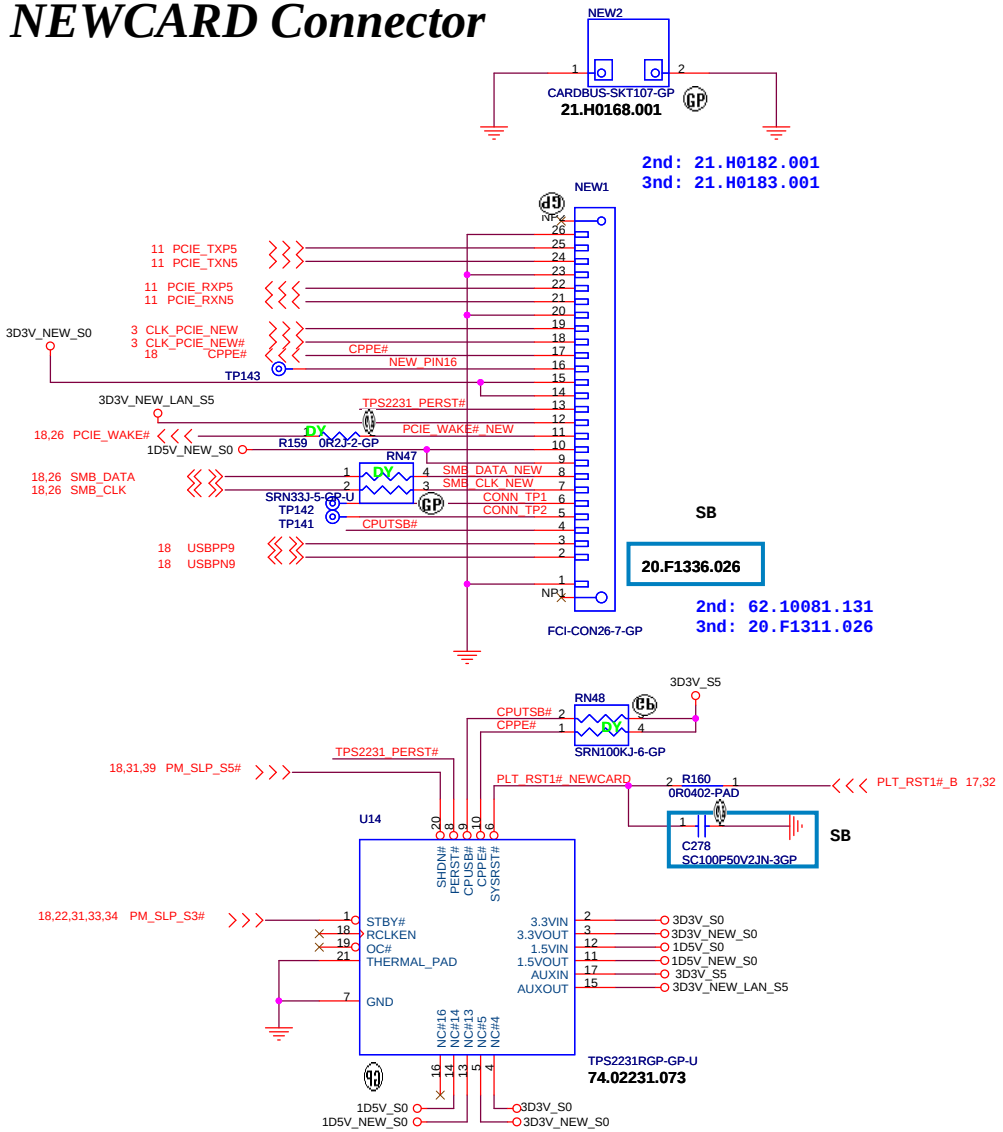
LAN Data: Yellow(13), when LAN is transfering data.

DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers

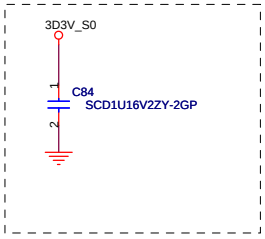


緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	**LAN CONN**		
Size A3	Document Number **Cathedral Peak 2A**		Rev -1
Date: Friday, August 22, 2008		Sheet of	43

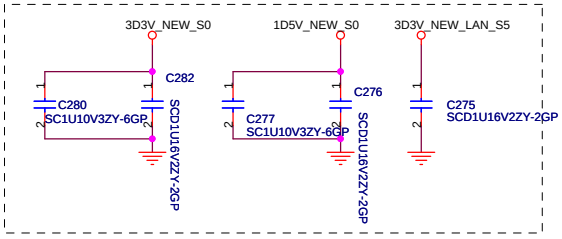
NEWCARD Connector



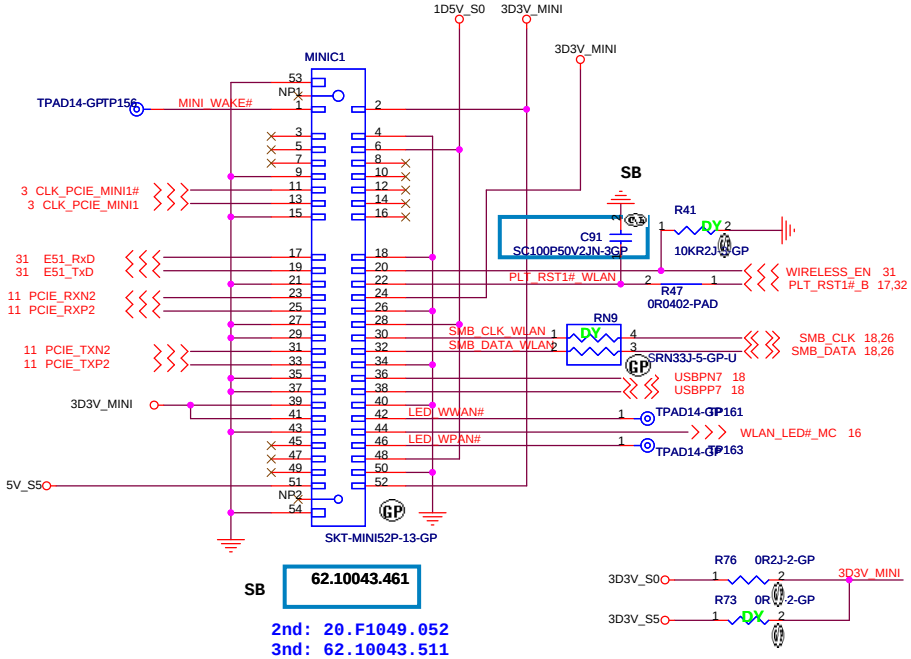
Place them Near to Chip



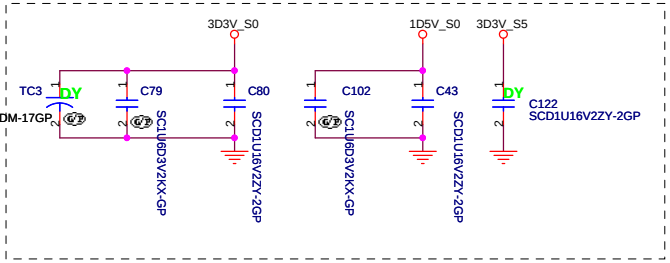
Place them Near to Connector



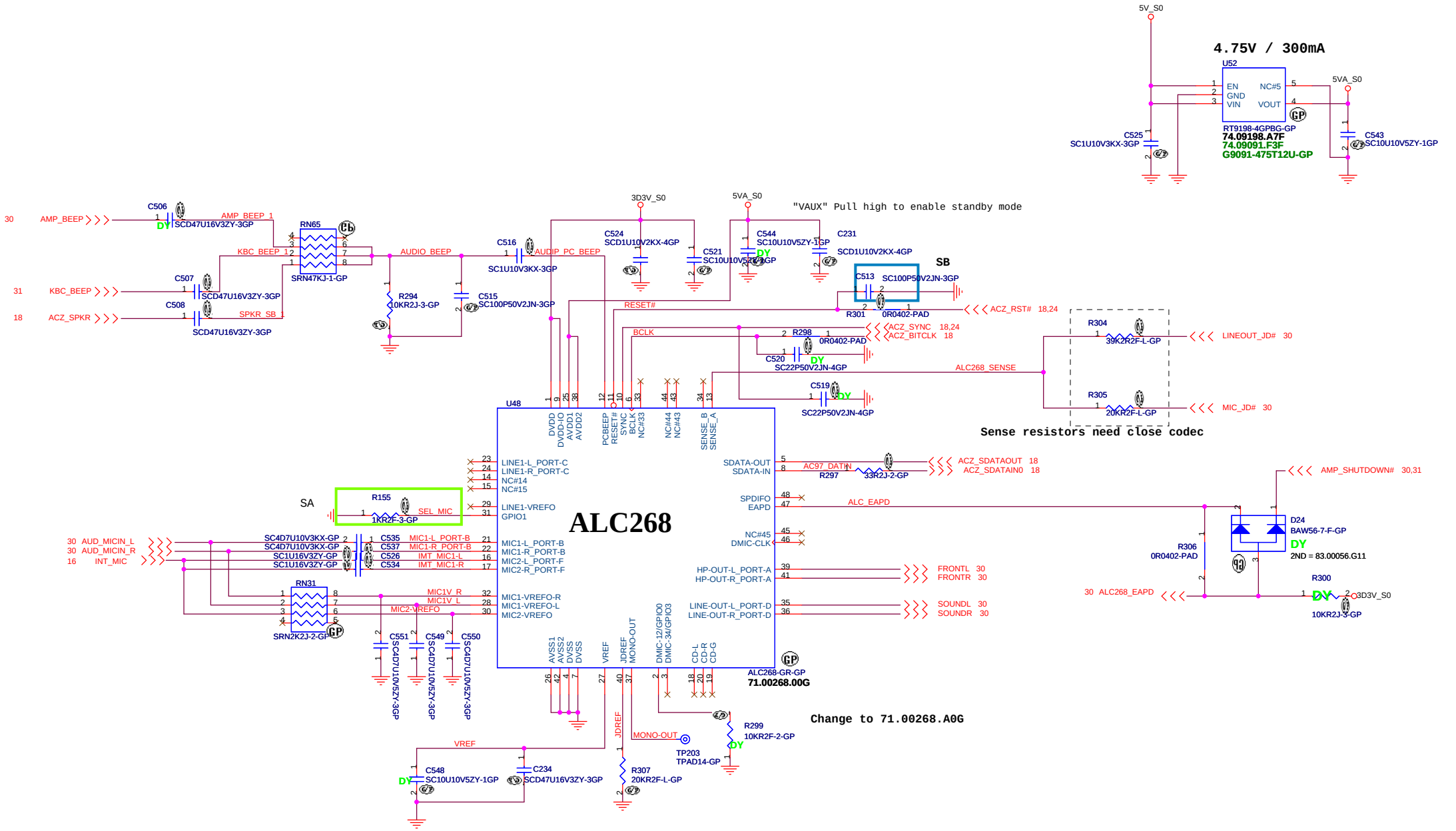
Mini Card Connector(WLAN)



Place near MINIC1



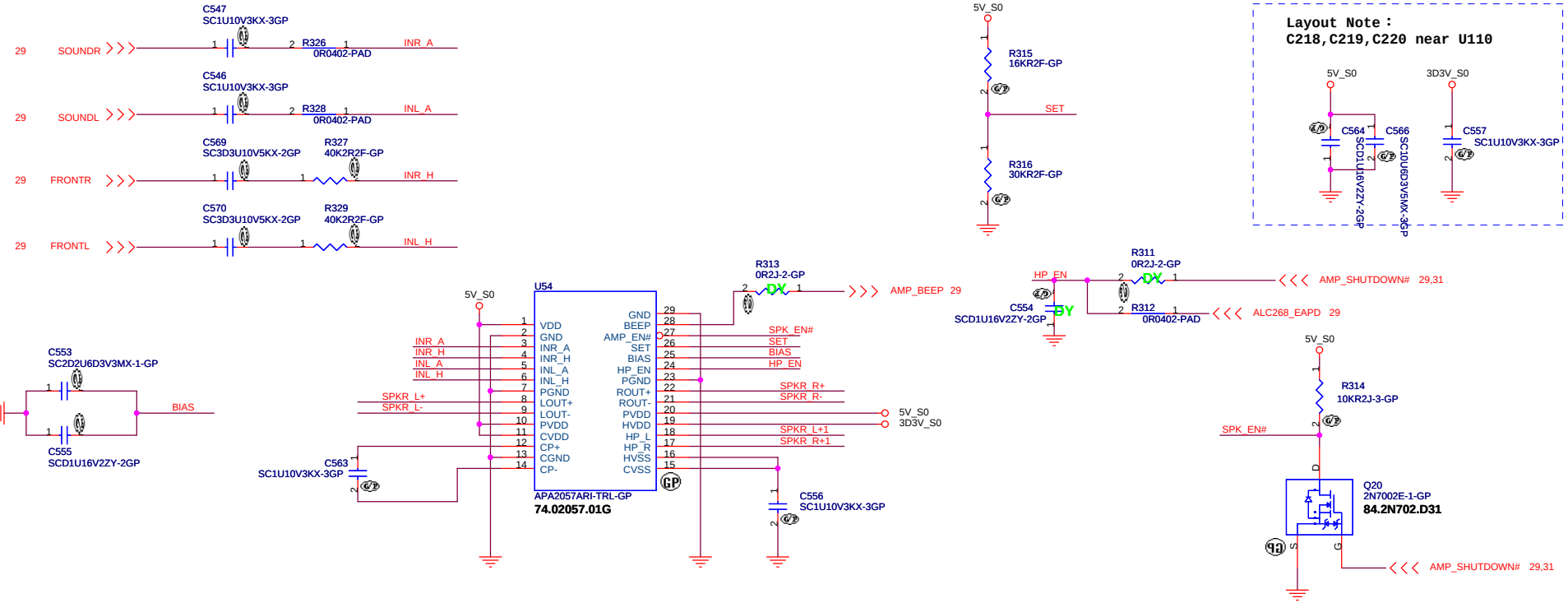
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: NEW CARD/MINI CARD		
Size	Document Number: Cathedral Peak 2A	Rev: -1
Date: Friday, August 22, 2008	Sheet 28 of 43	



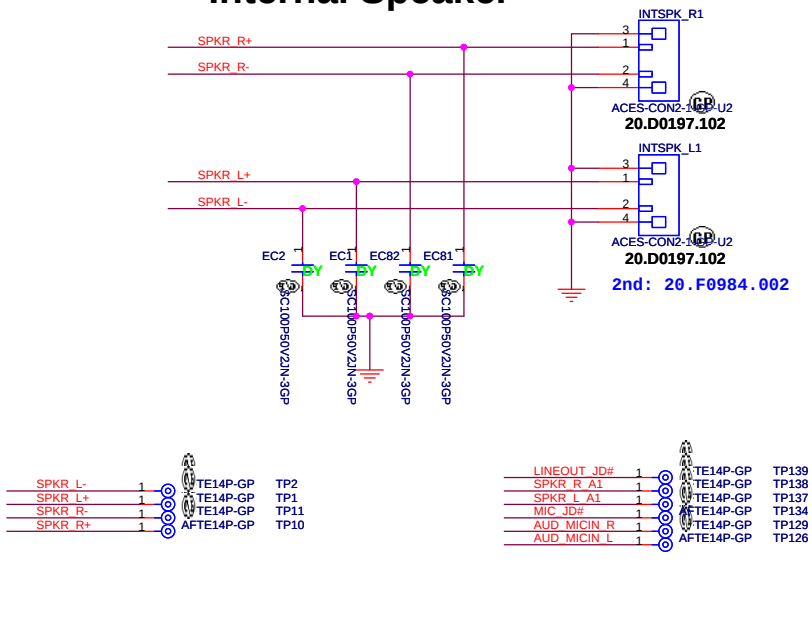
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Azalia codec ALC268**	
Size A3	Document Number **Cathedral Peak 2A**	Rev -1
Date: Friday, August 22, 2008	Sheet 29 of 43	

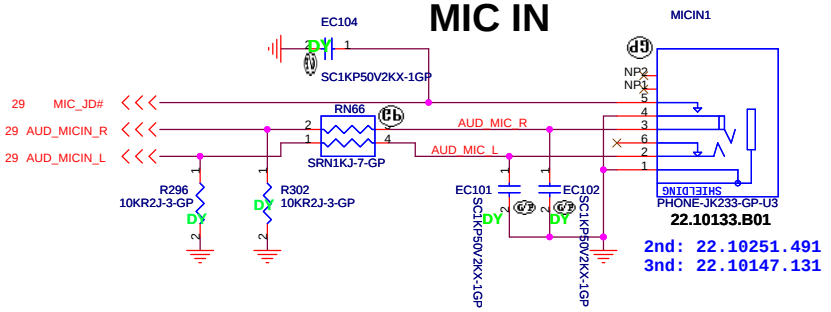
AUDIO OP AMPLIFIER



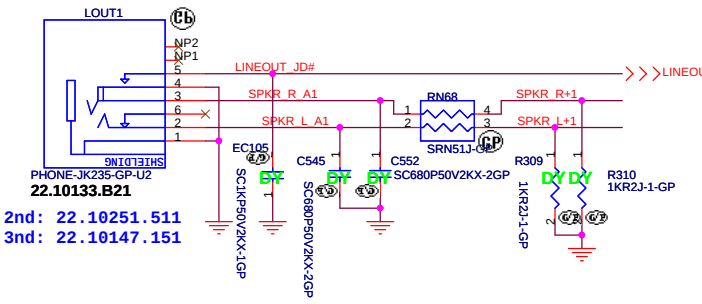
Internal Speaker



MIC IN

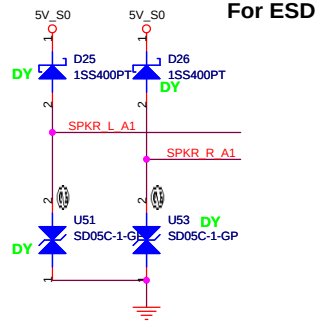


LINE OUT

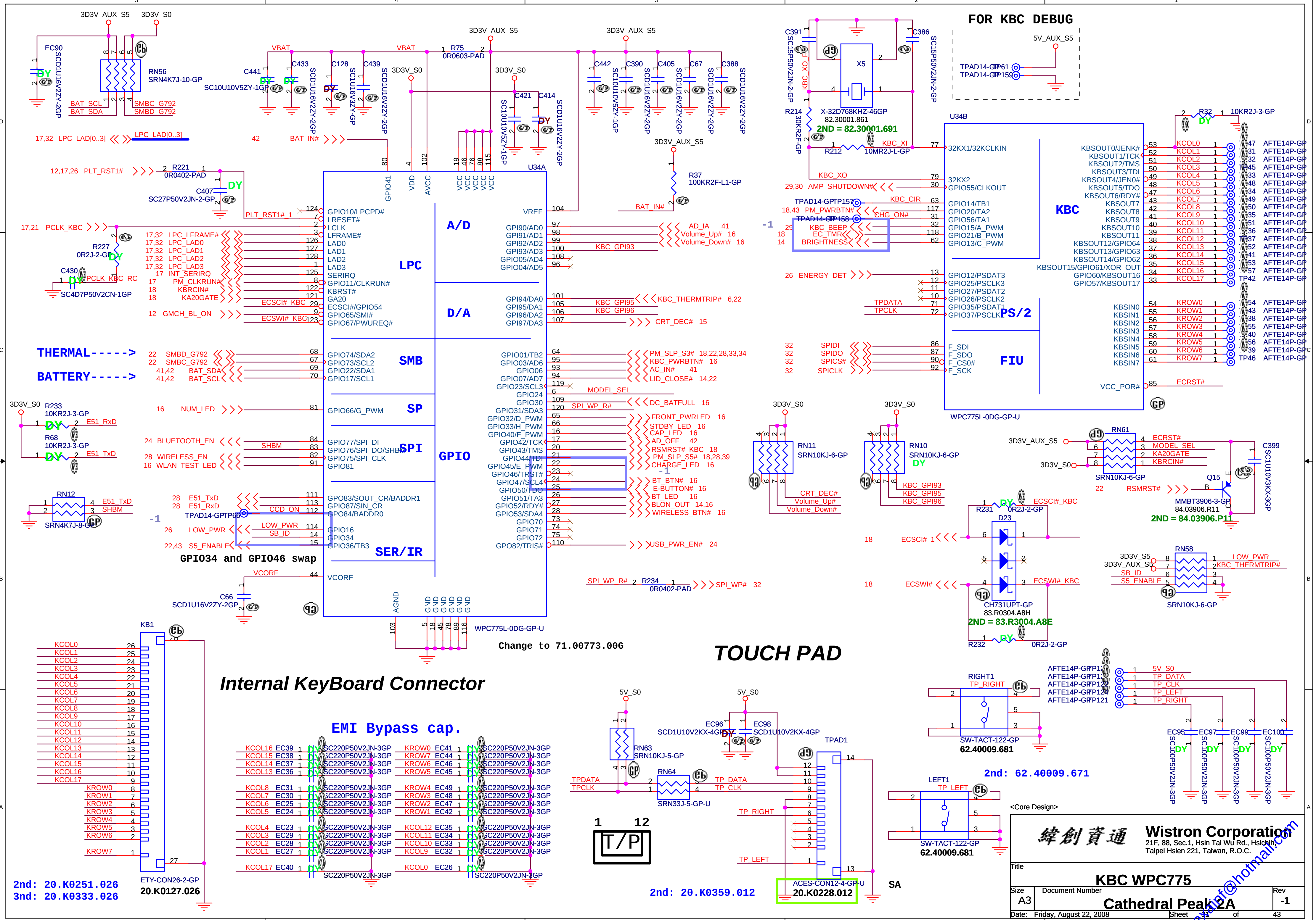


Analog Int. Mic

remove to LED Board



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AUDIO AMP AND JACK**	
Size	Document Number **Dolomites**	Rev **-1**
Date: Friday, August 22, 2008	Sheet 30 of 43	



FOR KBC DEBUG
THERMAL----->
BATTERY----->
KBC
PS/2
FIU
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
U34A
U34B
WPC775L-0DG-GP-U
GPIO34 and GPIO46 swap
Change to 71.00773.00G
Internal KeyBoard Connector
EMI Bypass cap.
TOUCH PAD
KB1
ETY-CON26-2-GP
20.K0127.026
2nd: 20.K0251.026
3rd: 20.K0333.026
TPAD1
ACES-CON12-4-GP-U
20.K0228.012
2nd: 20.K0359.012
SW-TACT-122-GP
62.40009.681
2nd: 62.40009.671
X-32D768KHZ-46GP
82.30001.861
2ND = 82.30001.691
CH731UPT-GP
83.R0304.A8H
2ND = 83.R3004.A8E
MMBT3906-3-GP
84.03906.R11
2ND = 84.03906.P11
T/P
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC WPC775
Size A3
Document Number
Cathedral Peak 2A
Rev -1
Date: Friday, August 22, 2008
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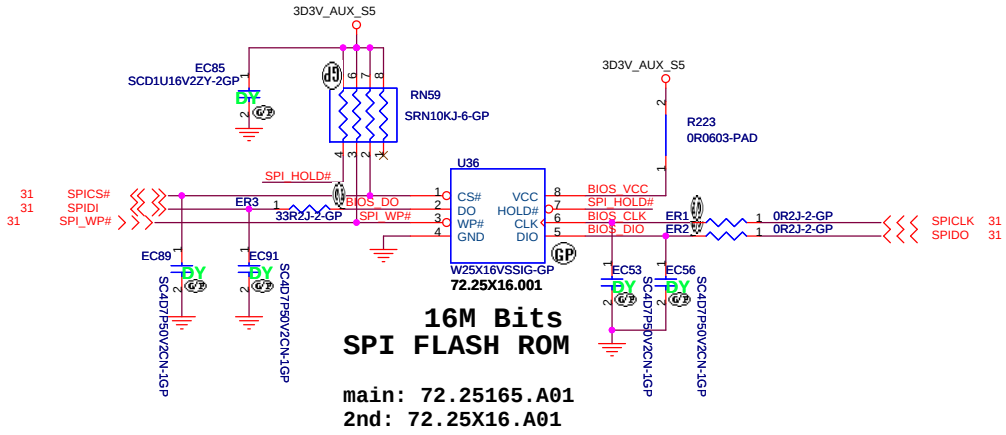

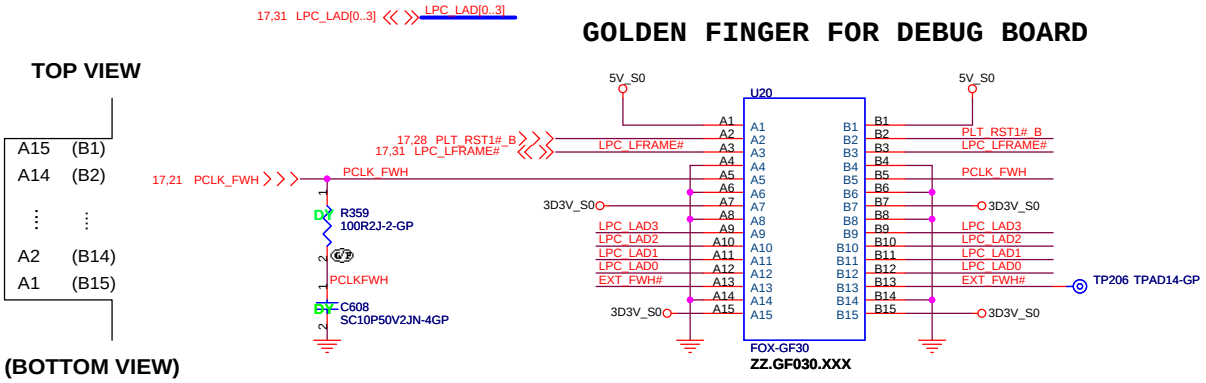

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BIOS**

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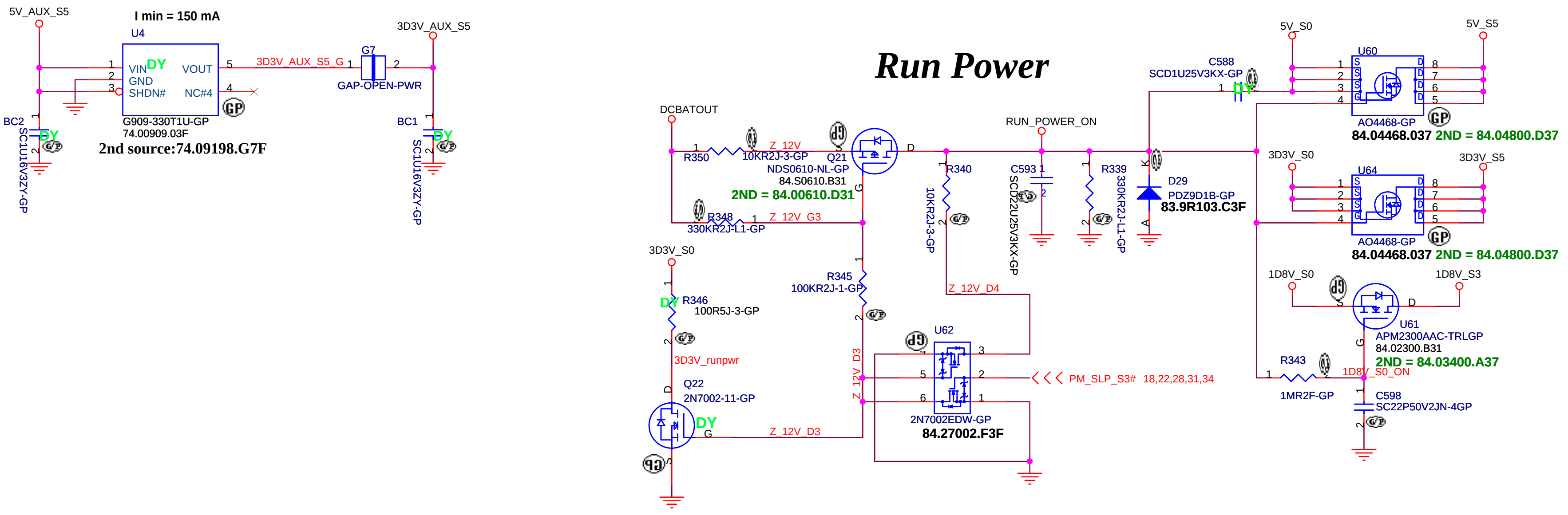
Aux Power 3D3V_AUX_S5



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN AND AUX POWER**

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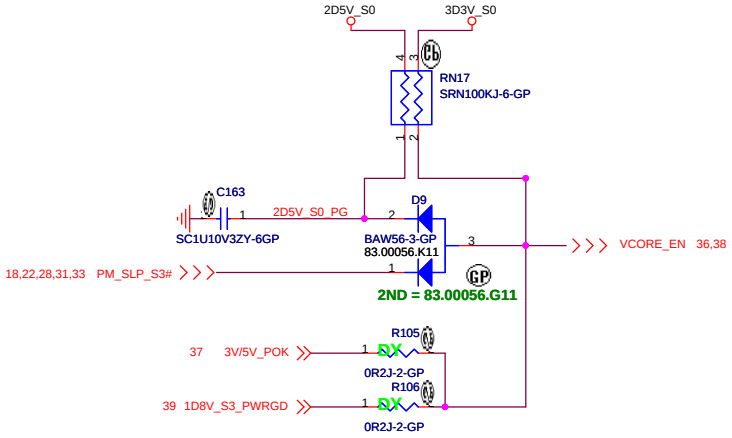
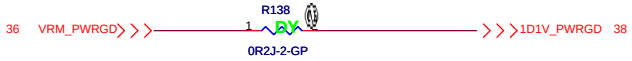
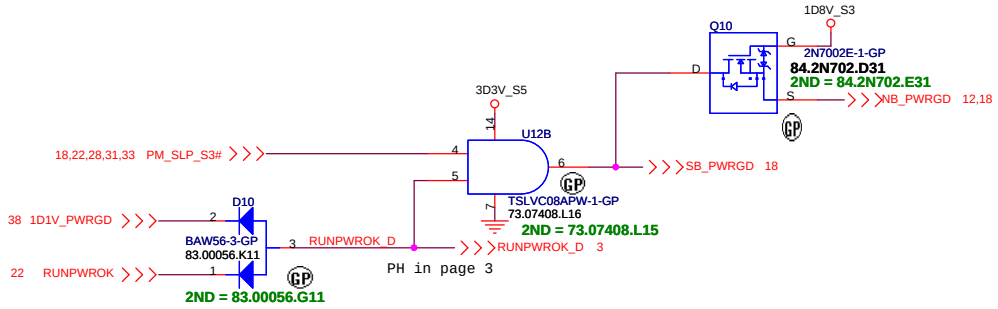
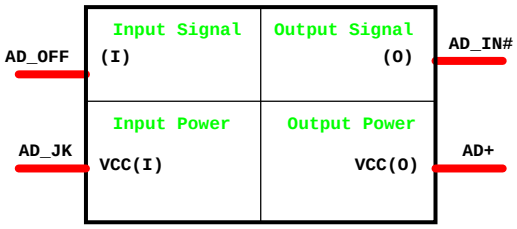


P/H @ 1D8V_S3 PAGE

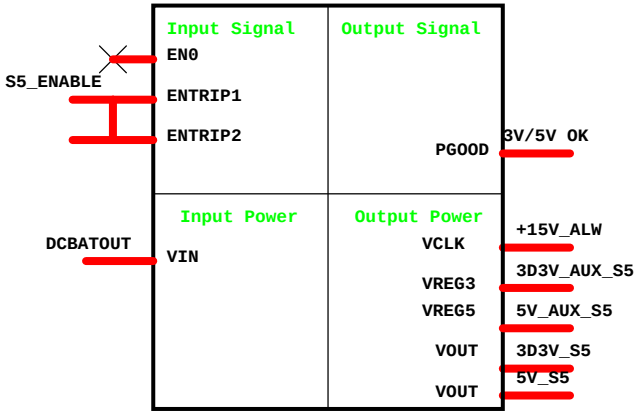




Adapter



DCDC 5V/3D3V(TPS51125)



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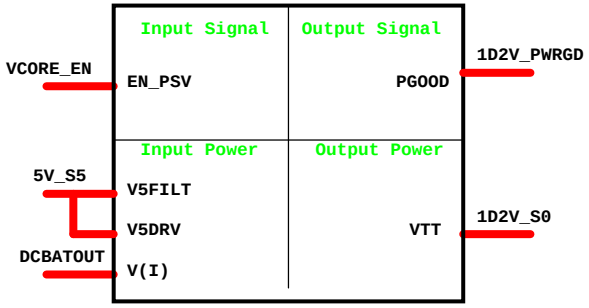
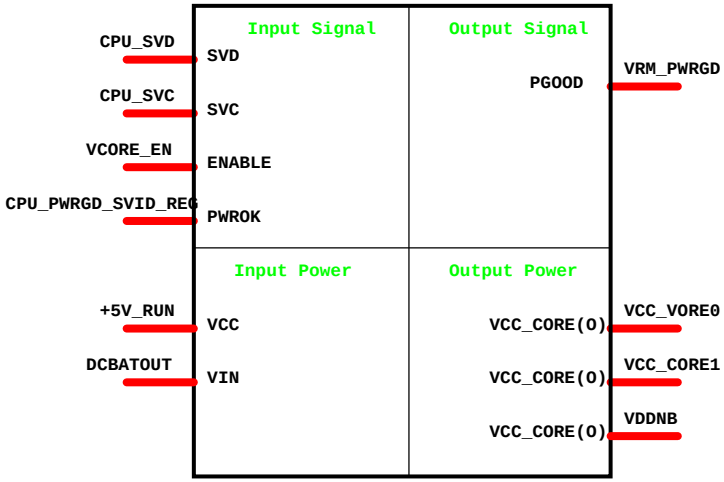


CPU_CORE
ISL6265HRTZ



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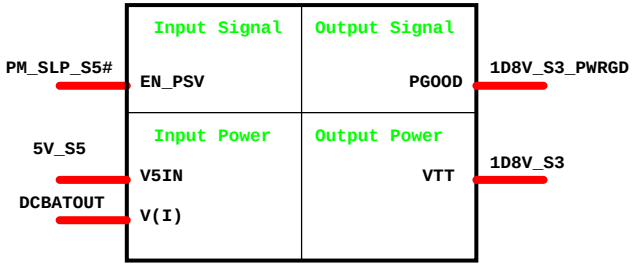
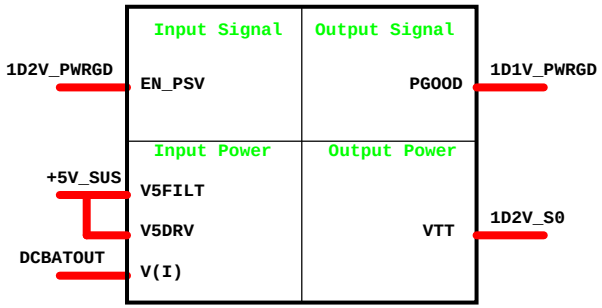
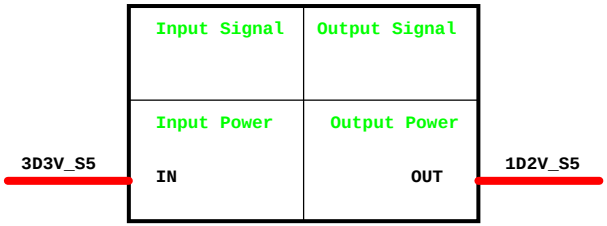


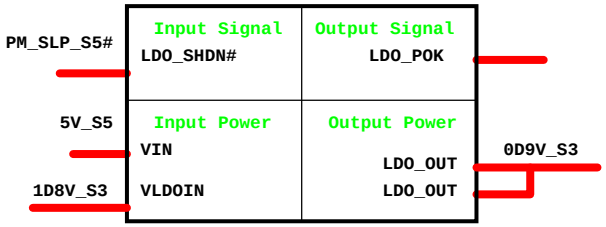
DCDC 1D1V(RT8202)



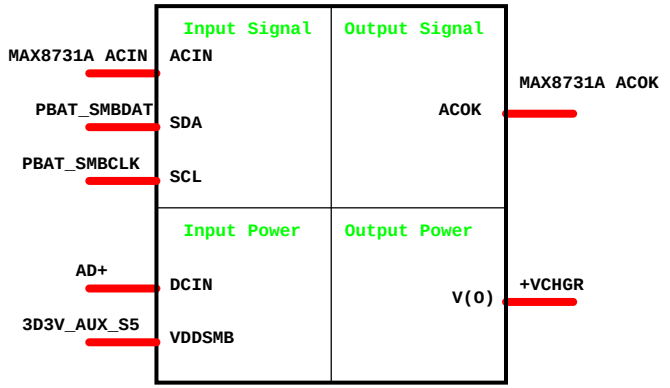
1D2V LDO G9161



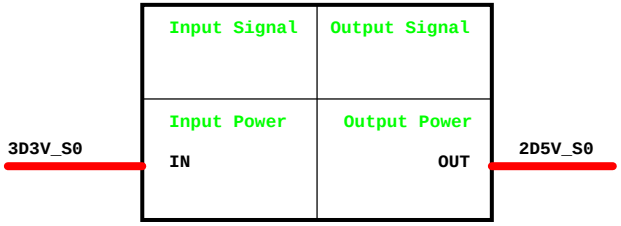
0D9V LDO RT9026



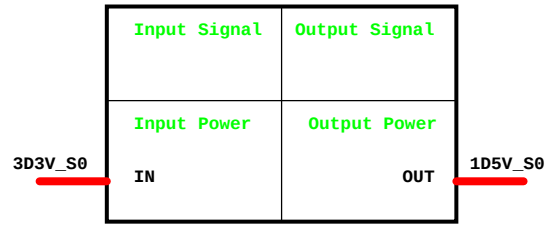
CHARGER MAX8731



2D5V LDO R9161



1D5V LDO G9571



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	Cathedral Peak 2A	-1

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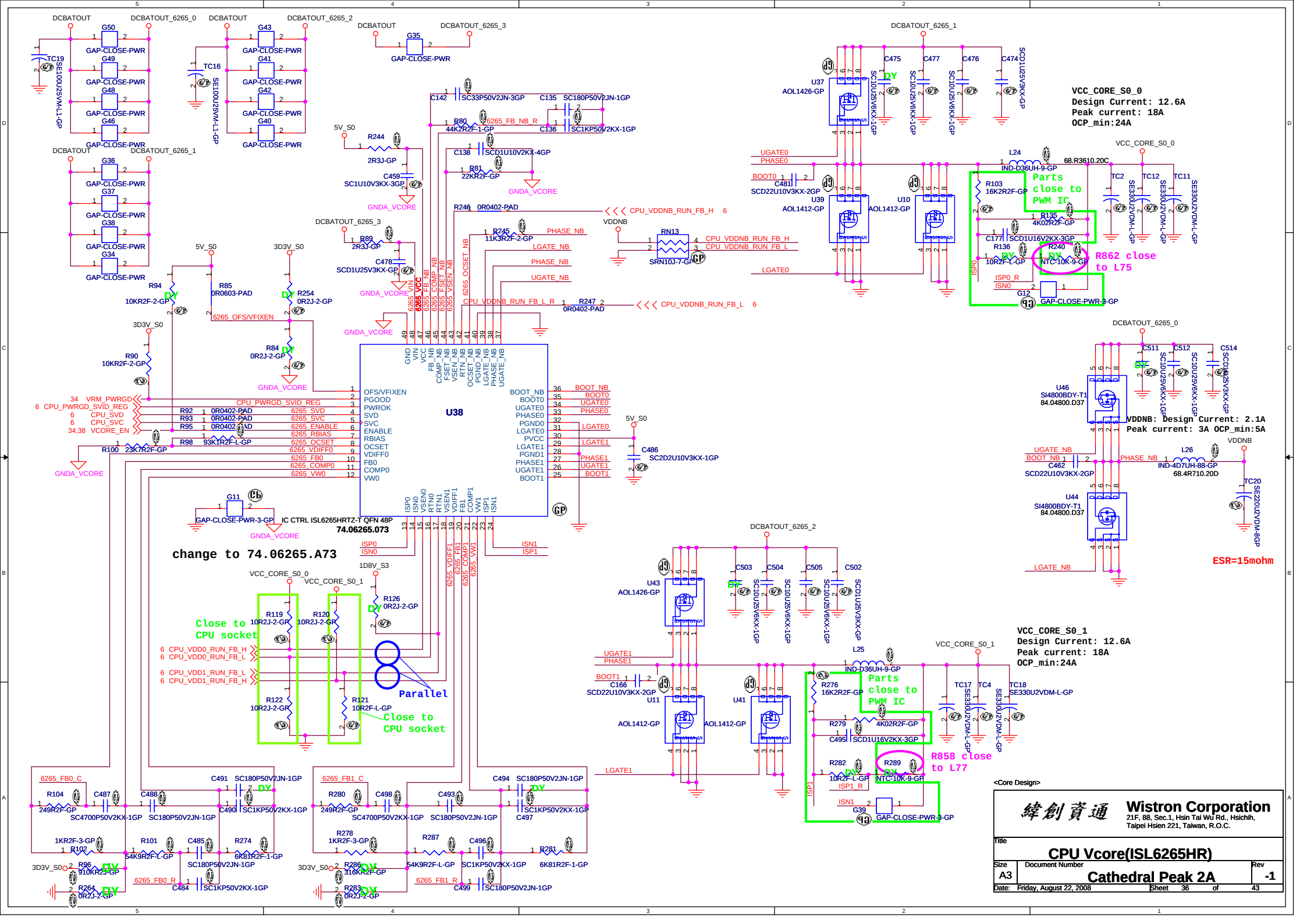
U38
IC CTRL ISL6265HRTZ-T QFN 48P
74.06265.073
change to 74.06265.A73
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
ESR=15mohm
R862 close to L75
R858 close to L77
Parts close to PWM IC
Close to CPU socket
Parallel
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
Cathedral Peak 2A
A3
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Friday, August 22, 2008
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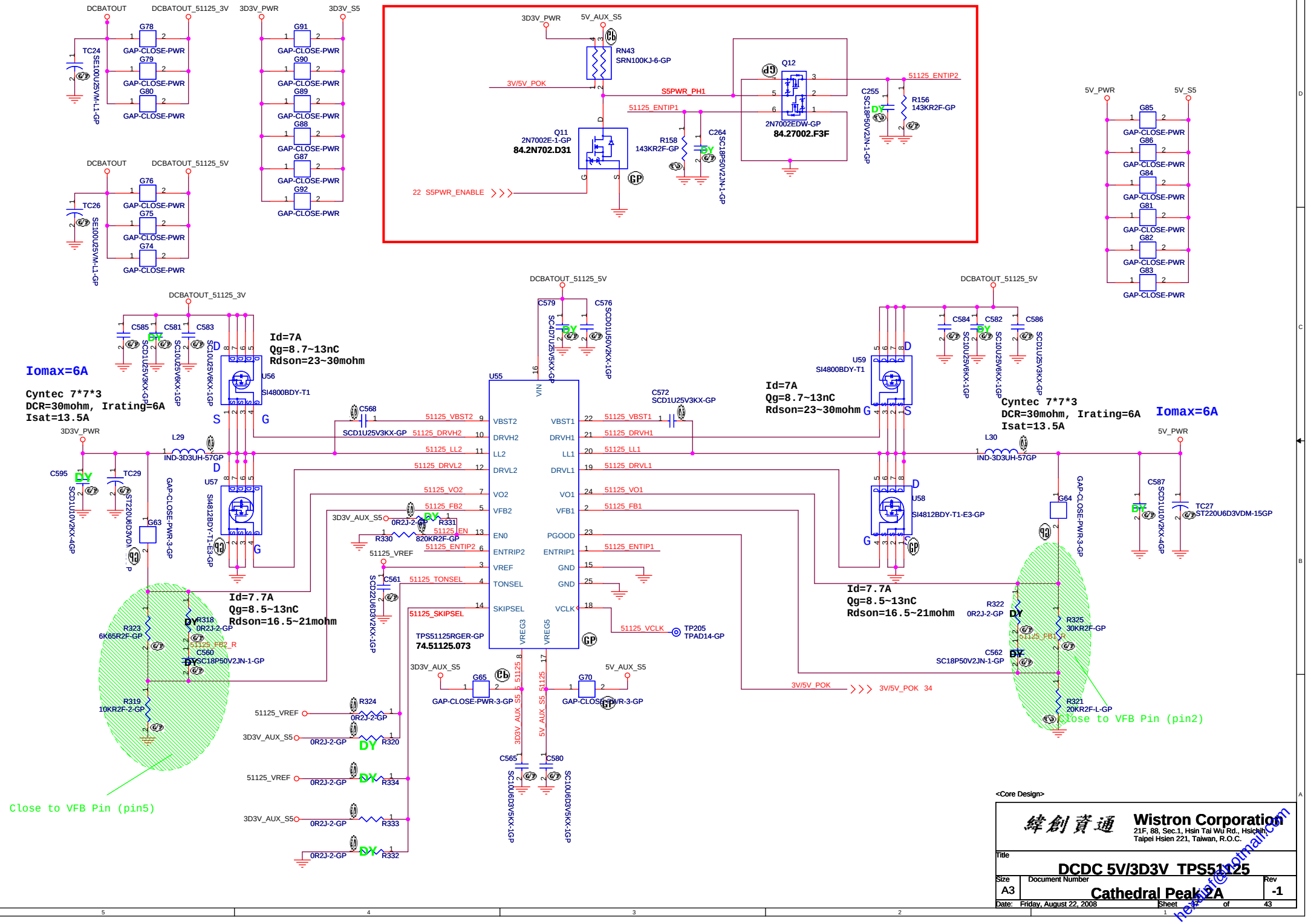
DCBATOUT
DCBATOUT_51125_3V
3D3V_PWR
3D3V_S5
DCBATOUT_51125_5V
5V_AUX_S5
5V_PWR
5V_S5
3V/5V_POK
S5PWR_PH1
51125_ENTIP1
51125_ENTIP2
22 S5PWR_ENABLE
Q11
2N7002E-1-GP
84.2N702.D31
Q12
2N7002EDW-GP
84.27002.F3F
RN43
SRN100KJ-6-GP
Iomax=6A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
U55
TPS51125RGER-GP
74.51125.073
U56
SI4800BDY-T1
U57
SI4812BDY-T1-E3-GP
U58
U59
L29
IND-3D3UH-57GP
L30
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_VREF
51125_TONSEL
51125_SKIPSEL
51125_VCLK
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
TP205
TPAD14-GP
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC 5V/3D3V TPS51125
Size
A3
Document Number
Cathedral Peak 2A
Rev
-1
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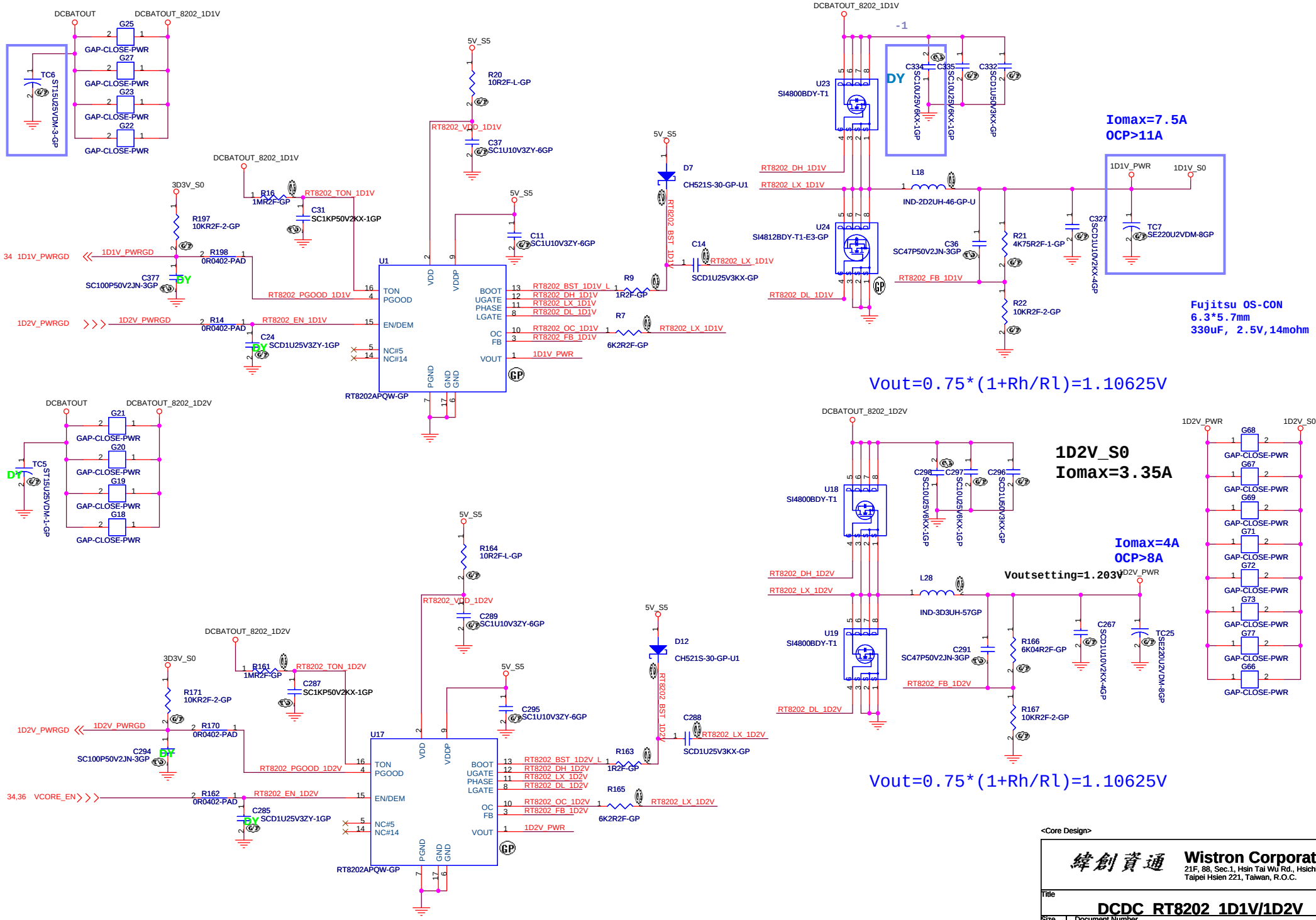
DCBATOUT
DCBATOUT_8202_1D1V
-1
TC6
ST15U25VDM-3-GP
G25
G27
G23
G22
GAP-CLOSE-PWR
5V_S5
R20
10R2F-L-GP
RT8202_VDD_1D1V
C37
SC1U10V3ZY-6GP
3D3V_S0
R16
1MR2F-GP
RT8202_TON_1D1V
C31
SC1KP50V2KX-1GP
R197
10KR2F-2-GP
34 1D1V_PWRGD
1D1V_PWRGD
R198
0R0402-PAD
C377
SC100P50V2JN-3GP
DY
RT8202_PGOOD_1D1V
1D2V_PWRGD
R14
0R0402-PAD
C24
SCD1U25V3ZY-1GP
U1
TON
PGOOD
EN/DEM
NC#5
NC#14
VDD
VDDP
BOOT
UGATE
PHASE
LGATE
OC
FB
VOUT
PGND
GND
RT8202_BST_1D1V_L
RT8202_DH_1D1V
RT8202_LX_1D1V
RT8202_DL_1D1V
RT8202_OC_1D1V
RT8202_FB_1D1V
1D1V_PWR
RT8202APQW-GP
C11
SC1U10V3ZY-6GP
D7
CH521S-30-GP-U1
RT8202_BST_1D1V
C14
RT8202_LX_1D1V
SCD1U25V3KX-GP
R9
1R2F-GP
R7
6K2R2F-GP
RT8202_LX_1D1V
U23
SI4800BDY-T1
U24
SI4812BDY-T1-E3-GP
C334
C335
C332
SC10U25V6KX-1GP
SC10U25V6KX-1GP
SCD1U50V3KX-GP
L18
IND-2D2UH-46-GP-U
C36
SC47P50V2JN-3GP
R21
4K75R2F-1-GP
C327
SCD1U10V2KX-4GP
R22
10KR2F-2-GP
1D1V_PWR
1D1V_S0
TC7
SE220U2VDM-8GP
Iomax=7.5A
OCP>11A
Fujitsu OS-CON
6.3*5.7mm
330uF, 2.5V,14mohm
Vout=0.75*(1+Rh/Rl)=1.10625V
DCBATOUT
DCBATOUT_8202_1D2V
TC5
ST15U25VDM-1-GP
G21
G20
G19
G18
R164
10R2F-L-GP
RT8202_VDD_1D2V
C289
SC1U10V3ZY-6GP
R161
1MR2F-GP
RT8202_TON_1D2V
C287
SC1KP50V2KX-1GP
R171
10KR2F-2-GP
1D2V_PWRGD
R170
0R0402-PAD
C294
SC100P50V2JN-3GP
RT8202_PGOOD_1D2V
34,36 VCORE_EN
R162
0R0402-PAD
C285
SCD1U25V3ZY-1GP
U17
RT8202_BST_1D2V_L
RT8202_DH_1D2V
RT8202_LX_1D2V
RT8202_DL_1D2V
RT8202_OC_1D2V
RT8202_FB_1D2V
1D2V_PWR
RT8202APQW-GP
C295
SC1U10V3ZY-6GP
D12
CH521S-30-GP-U1
RT8202_BST_1D2V
C288
RT8202_LX_1D2V
SCD1U25V3KX-GP
R163
1R2F-GP
R165
6K2R2F-GP
RT8202_LX_1D2V
U18
SI4800BDY-T1
U19
SI4800BDY-T1
C298
C297
C296
SC10U25V6KX-1GP
SC10U25V6KX-1GP
SCD1U50V3KX-GP
L28
IND-3D3UH-57GP
Voutsetting=1.203V
C291
SC47P50V2JN-3GP
R166
6K04R2F-GP
C267
SCD1U10V2KX-4GP
R167
10KR2F-2-GP
1D2V_PWR
1D2V_S0
TC25
SE220U2VDM-8GP
G68
G67
G69
G71
G72
G73
G77
G66
1D2V_S0
Iomax=3.35A
Iomax=4A
OCP>8A
Vout=0.75*(1+Rh/Rl)=1.10625V
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
DCDC_RT8202_1D1V/1D2V
Size
A3
Document Number
Cathedral Peak 2A
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-1
Date: Friday, August 22, 2008
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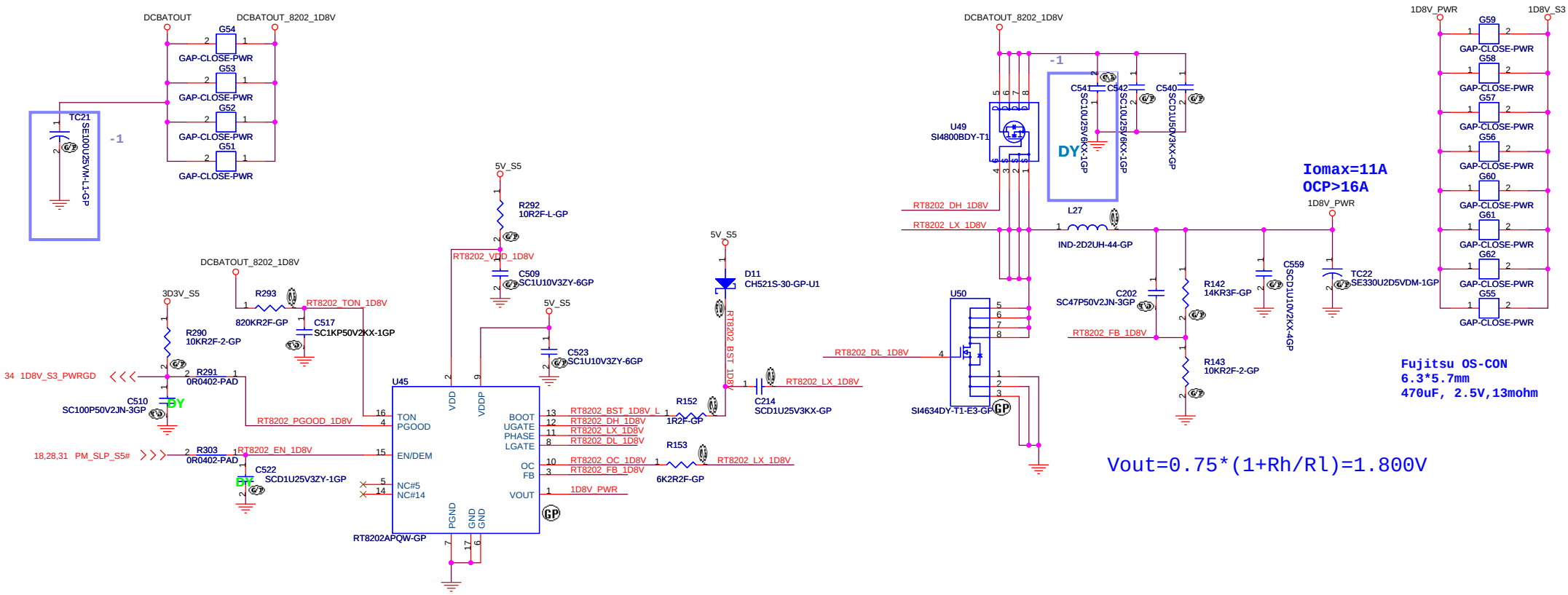
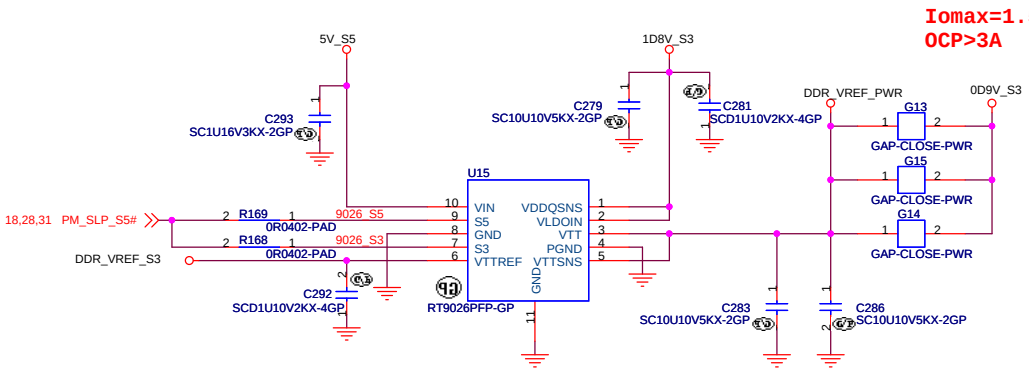


DDR_0.9V



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC_1D8V_RT8202/LDO_0D9V

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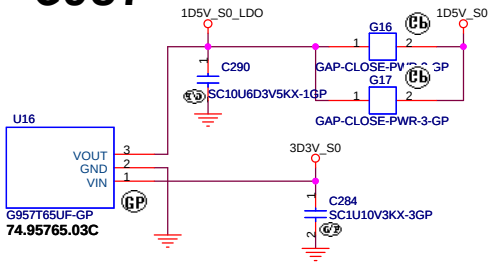
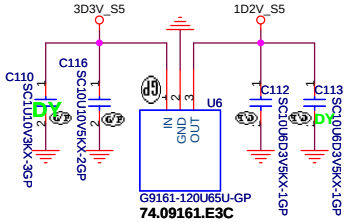
G957

1D5V_S0
Iomax=1A



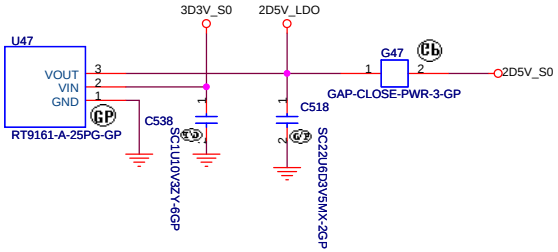
For MINI Card.NEW Card power SW

1D2V_S5
Iomax=400mA



Place near to SB700

2D5V
Iomax=0.2A



Place near to CPU

<Core Design>

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Title: **LDO 2D5V/1D5V/1D2V_S5**

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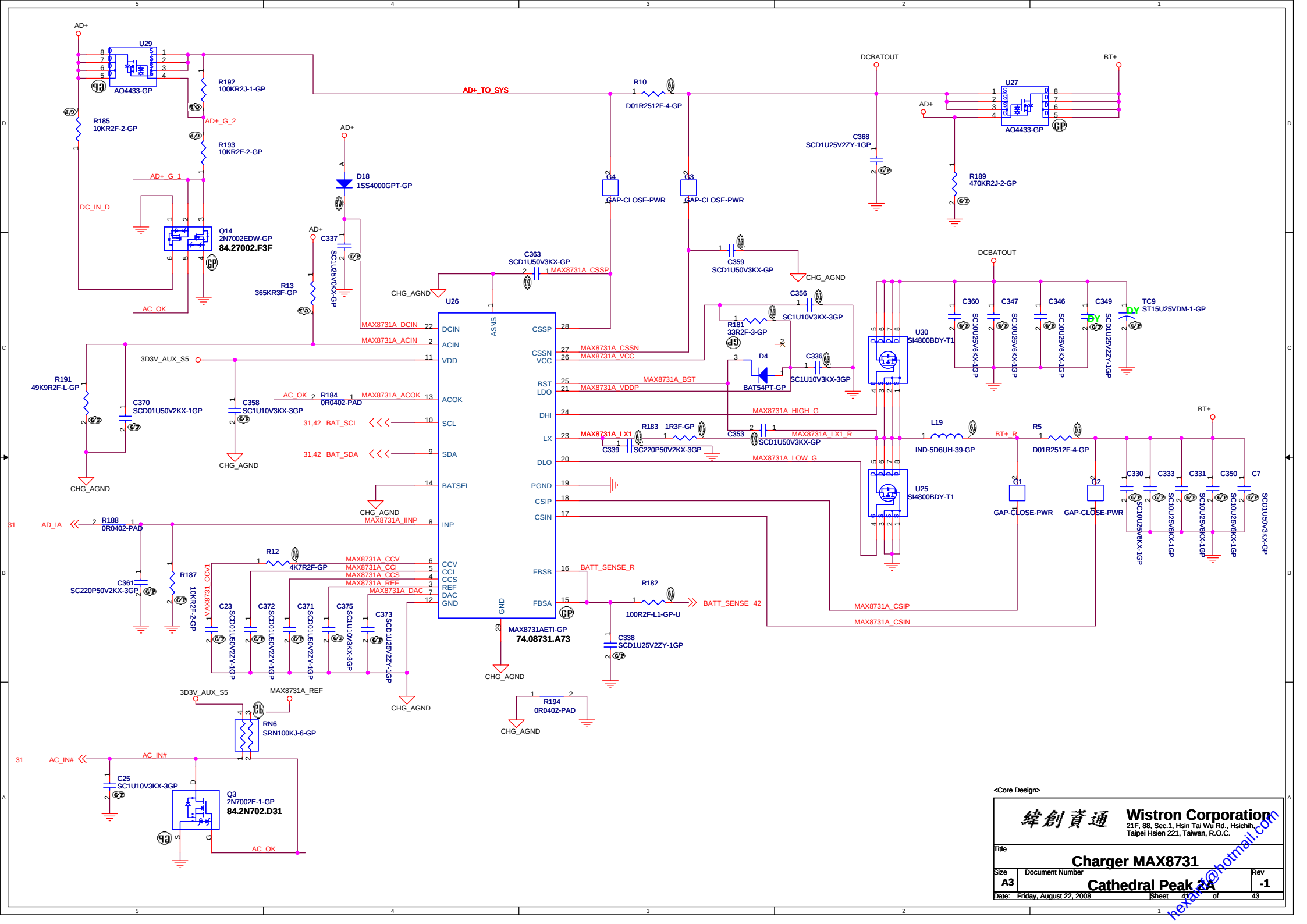

<Core Design>

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Title: Charger MAX8731

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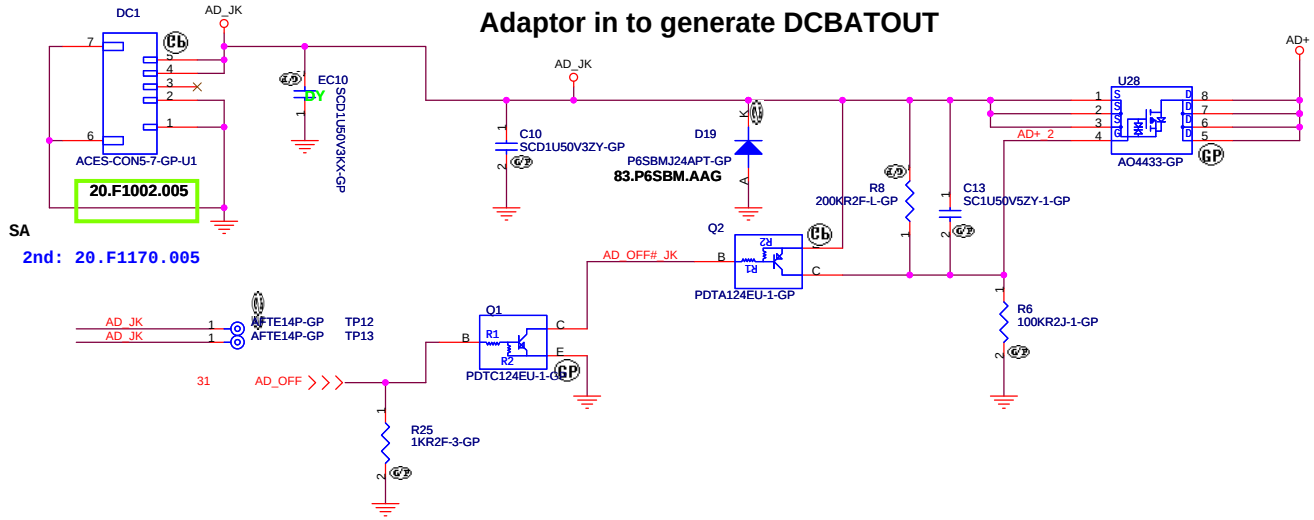
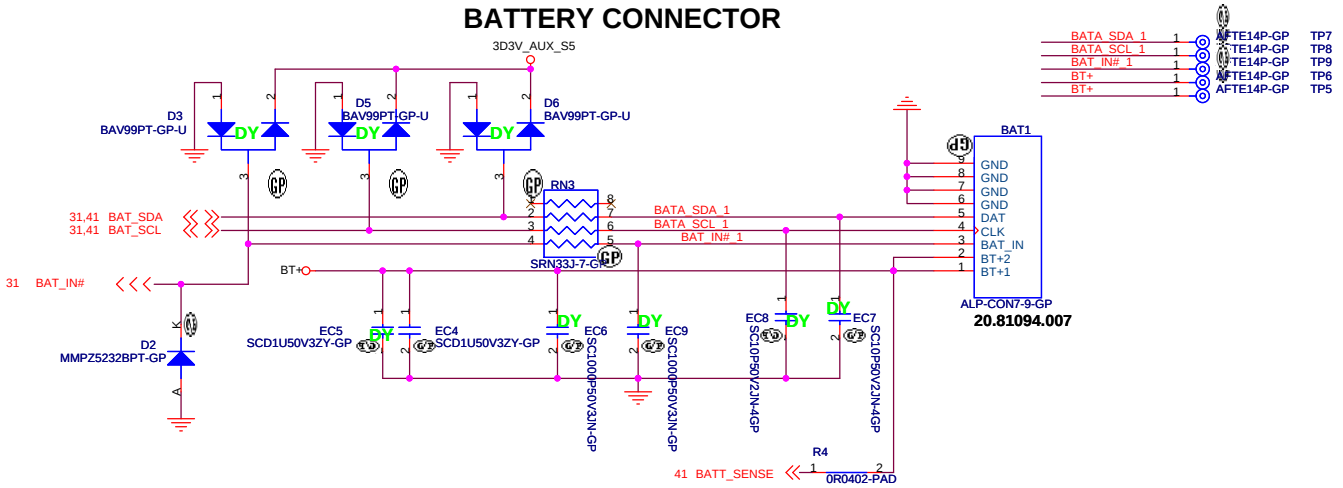
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Title	**AD/BATT CONN**	
Size	Document Number: **Cathedral Peak 2A**	Rev: -1
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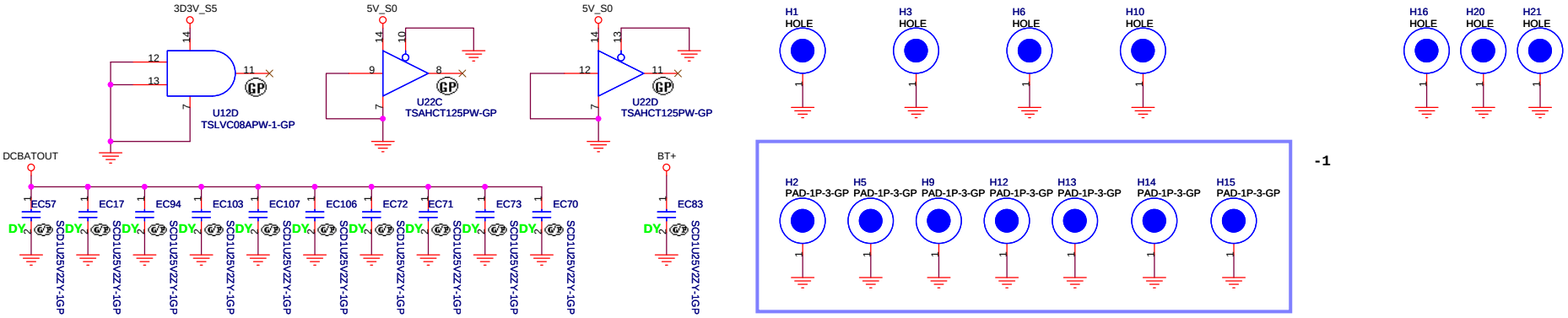
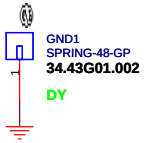


TOP

BOTTOM



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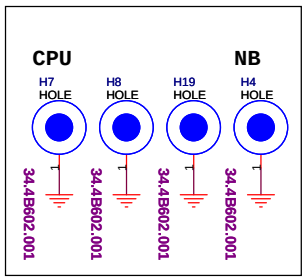

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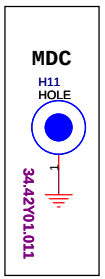

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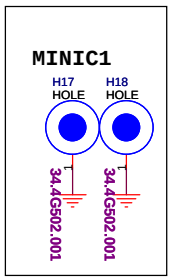

SA SB -1

Check test point

3D3V_S0	TP140	TPAD14-GP	
3D3V_AUX_S5	TP148	TPAD14-GP	
3D3V_S5	TP145	TPAD14-GP	
5V_S5	TP127	TPAD14-GP	
18,31 PM_PWRBTN#	TP65	TPAD14-GP	
6,17 CPU_PWRGD	TP188	TPAD14-GP	
22,31 S5_ENABLE	TP160	TPAD14-GP	
6,17 CPU_LDT_RST#	TP77	TPAD14-GP	

Test Point放在Dimm Door打開可量測處

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Taipei Hsien 221, Taiwan, R.O.C.

Title	EMI/Spring/Boss	
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