Compal Confidential

NCQD0 M/B Schematics Document

Intel Arrandale/Clarksfield Processor with DDRIII + Ibex Peak-M

2009-08-10

REV:1.0

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Issued Date	2009/08/10	Deciphered Date	2010/08/10	Title: SCHEMATICS,MB A5511
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Model Name : NCQD0
File Name : LA5511P

Fan Control
page 43

Clock Generator
IDT: 9LRS3199AKLFT
SILEGO: SLG8SP587
133/120/100/96/14.318MHZ to PCH
48MHZ to CardReader
page 12

ATI
M96/M92XT
page 23,24,25,26,27,28,29

PEG(DIS) 100MHz PCI-E 2.0x16 5GT/s PER LANE
133MHz

Intel
Auburndale / Clarksfield
(UMA/DIS) (DIS)
Processor
rPGA988A
page 4,5,6,7,8,9

Memory BUS(DDRIII)
Dual Channel
1.5V DDRIII 800/1066/1333
6.4G/8.5G/10.6G
100M/133M/166M(CFD)

204pin DDRIII-SO-DIMM X2
BANK 0, 1, 2, 3
page 10,11

LVDS(DIS)
LVDS Conn.
page 30

HDMI(DIS)
CRT(DIS)

HDMI Conn.
page 32

HDMI SW
& Level shift
page 32

CRT SW.
page 31

CRT Conn.
page 31

LVDS SW
page 30

FDI x8
(UMA)
100MHz
2.7GT/s

DMI x4
100MHz
1GB/s x4

USB conn x2
USB port 0,1
USB port 8 HS USB
USB Port 2 (eSATA)
page 37

Bluetooth
Conn
USB port 10
page 36

CMOS Camera
USB port 3
page 30

USBx14
3.3V 48MHz

LVDS(UMA)
CRT(UMA)
HDMI(UMA)

Intel
Ibex Peak-M
PCH
page 13,14,15,16,17
18,19,20,21

HD Audio 3.3V 24MHz

PCI-Express x 8 (ABD PCIE1 2.5GT/S CKD PCIE1/2 2.5/5GT/S) 100MHz

SATA x 6 (GEN1 1.5GT/S ,GEN2 3GT/S) 100MHz

SPI

HDA Codec
ALC669X
page 41

port 5
CardReader
JMB380
page 33

port 3
NEW CARD
page 36

port 2,4
MINI Card x2
WLAN, TV
page 33

port 1
LAN(GbE)
BCM57780
page 34

SPI ROM x2
page 13

port 0
SATA HDD
Conn.
page 33

port 1
SATA ODD
Conn.
page 33

port 4
eSATA
Conn.
page 37

Audio AMP
TPA6017
page 42

1394
Conn.

5 in 1 socket

Sub-board
LS-5511P Switch/B page 39
LS-5011P Cap Sensor/B page 39
LS-5512P MEADIA/B page39
LS-5014P Volumn/B page 39
LS-5513P USB/B page 37
LS-5015P FP/B page39
LS-5514P Card Reader/B page 33
LS-5515P TP BTN/B page 39
LS-5516P PWR SAVING/B page 39

RJ45
page 35

LPC BUS
33MHz

Daul CH NAND interface

Braidwoood
page 22

Int. Speaker
page 41

Phone Jack x 3
+SubWoofer
page 42

ENE KB926
page 38

Touch Pad
page 39

Int.KBD
page 39

EC I/O Buffer
page 39

BIOS ROM
page 39

RTC CKT.
page 36

Power On/Off CKT.
page 40

DC/DC Interface CKT.
page 44,45

Power Circuit DC/DC
page 46~58

PCH XDP
page 21

CPU XDP
133MHz
page 5

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Voltage Rails

Power Plane	Description	S1	S3	S5	DGPU (UMA)	DGPU (DIS)
VIN	Adapter power supply (19V)	N/A	N/A	N/A		
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A		
+CPU_CORE	Core voltage for CPU	ON	ON	OFF		
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF		
+1.05VS	1.05V switched power rail for PCH	ON	OFF	OFF		
+1.1VS_VTT	1.1V switched power rail (1.05 for AUB CPU)	ON	OFF	OFF		
+1.5V	1.5V power rail for DDRIII	ON	ON	OFF		
+1.5VS	1.5V switched power rail	ON	OFF	OFF		
+1.8VS	1.8V switched power rail	ON	OFF	OFF		
+3VALW	3.3V always on power rail	ON	ON	ON*		
+3V	3.3V power rail for PCH	ON	ON	ON		
+3V_LAN	3.3V power rail for LAN	ON	ON	ON*		
+3VS	3.3V switched power rail	ON	OFF	OFF		
+5VALW	5V always on power rail	ON	ON	ON*		
+5VS	5V switched power rail	ON	OFF	OFF		
+5V	5V power rail for PCH	ON	ON	ON		
+VSB	VSB always on power rail	ON	ON	ON*		
+RTCVCC	RTC power	ON	ON	ON		
+5VSDGPU	5V power rail for GPU				OFF	ON
+1.5VSDGPU	1.5V power rail for VRAM				OFF	ON
+1.8VSDGPU	1.8V switched power rail for GPU				OFF	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address

Ibex SM Bus address

Device	Address
Clock Generator (9LRS3199AKLFT, SLG8SP587)	1101 0010b
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb
ISL90727 ISL90728	0101 1100b 0111 1100b

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
* 0	0.1
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
UMA	UMA@
UMA Only	UMAO@
DIS Only	DIS@
DGPU	VGA@
Braidwood	NV@
M96	M96@
Broadway	MAD@
Switchable Graphics	SG@

BOM Config
Switchable Graphics (M96)SKU: UMA@/SG@/VGA@
UMA only SKU: UMA@/UMAO@
DIS ONLY (M96): DIS@/VGA@

USB Port Table

USB 2.0	USB 1.1	Port	4 External USB Port
EHCI1	UHCI0	0	USB Conn.
		1	USB/B
	UHCI1	2	eSATA USB
		3	CMOS Camera
	UHCI2	4	Mini Card 1
		5	Mini Card 2
	UHCI3	6	
		7	
EHCI2	UHCI4	8	USB Conn.
		9	
	UHCI5	10	Blue Tooth
		11	Finger Print
	UHCI6	12	NewCard
		13	

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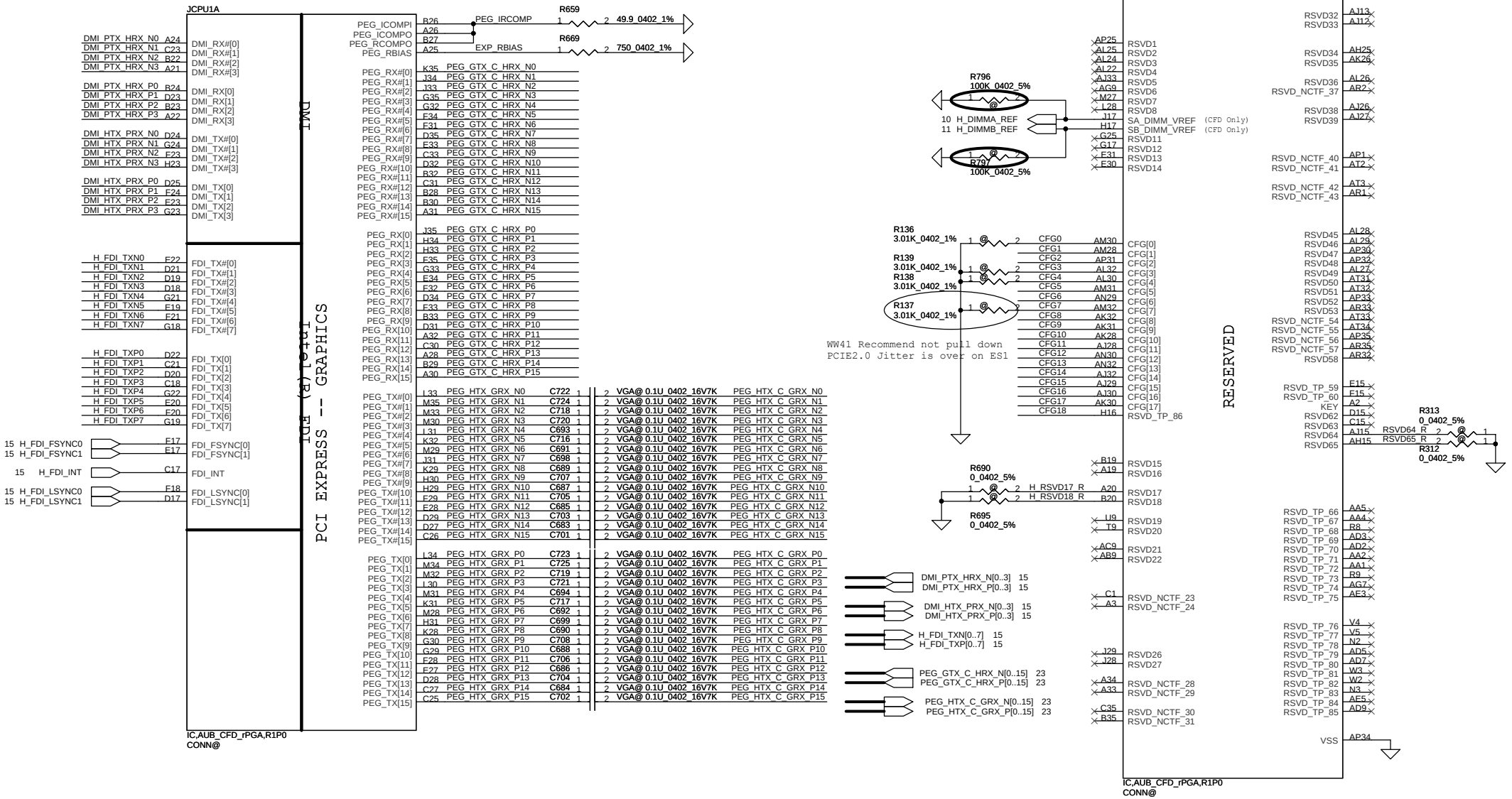

eDP Signals MAPPING

eDP Singal	PEG Singals	Lane Reversal
eDP_TX0	PEG_HTX_C_GRX_P15	PEG_HTX_C_GRX_P0
eDP_TX#0	PEG_HTX_C_GRX_N15	PEG_HTX_C_GRX_N0
eDP_TX1	PEG_HTX_C_GRX_P14	PEG_HTX_C_GRX_P1
eDP_TX#1	PEG_HTX_C_GRX_N14	PEG_HTX_C_GRX_N1
eDP_TX2	PEG_HTX_C_GRX_P13	PEG_HTX_C_GRX_P2
eDP_TX#2	PEG_HTX_C_GRX_N13	PEG_HTX_C_GRX_N2
eDP_TX3	PEG_HTX_C_GRX_P12	PEG_HTX_C_GRX_P3
eDP_TX#3	PEG_HTX_C_GRX_N12	PEG_HTX_C_GRX_N3
eDP_AUX	PEG_GTX_C_HRX_P13	PEG_GTX_C_HRX_P2
eDP_AUX#	PEG_GTX_C_HRX_N13	PEG_GTX_C_HRX_N2
eDP_HPD#	PEG_GTX_C_HRX_P12	PEG_GTX_C_HRX_P3

CFG0 - PCI-Express Configuration Select

*1:Single PEG
0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal

*1 :Normal Operation
0 :Lane Numbers Reversed
15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence

*1:Disabled; No Physical Display Port attached to Embedded Display Port
0:Enabled; An external Display Port device is connected to the Embedded Display Port

*:Default

H_FDI_FSYNC0 R711 1 DIS@ 2 1K_0402_5%
H_FDI_FSYNC1 R705 1 DIS@ 2 1K_0402_5%
H_FDI_INT R699 1 DIS@ 2 1K_0402_5%
H_FDI_LSYNC0 R710 1 DIS@ 2 1K_0402_5%
H_FDI_LSYNC1 R697 1 DIS@ 2 1K_0402_5%
CheckList0.8 1.22
Auburndale Graphics Disable

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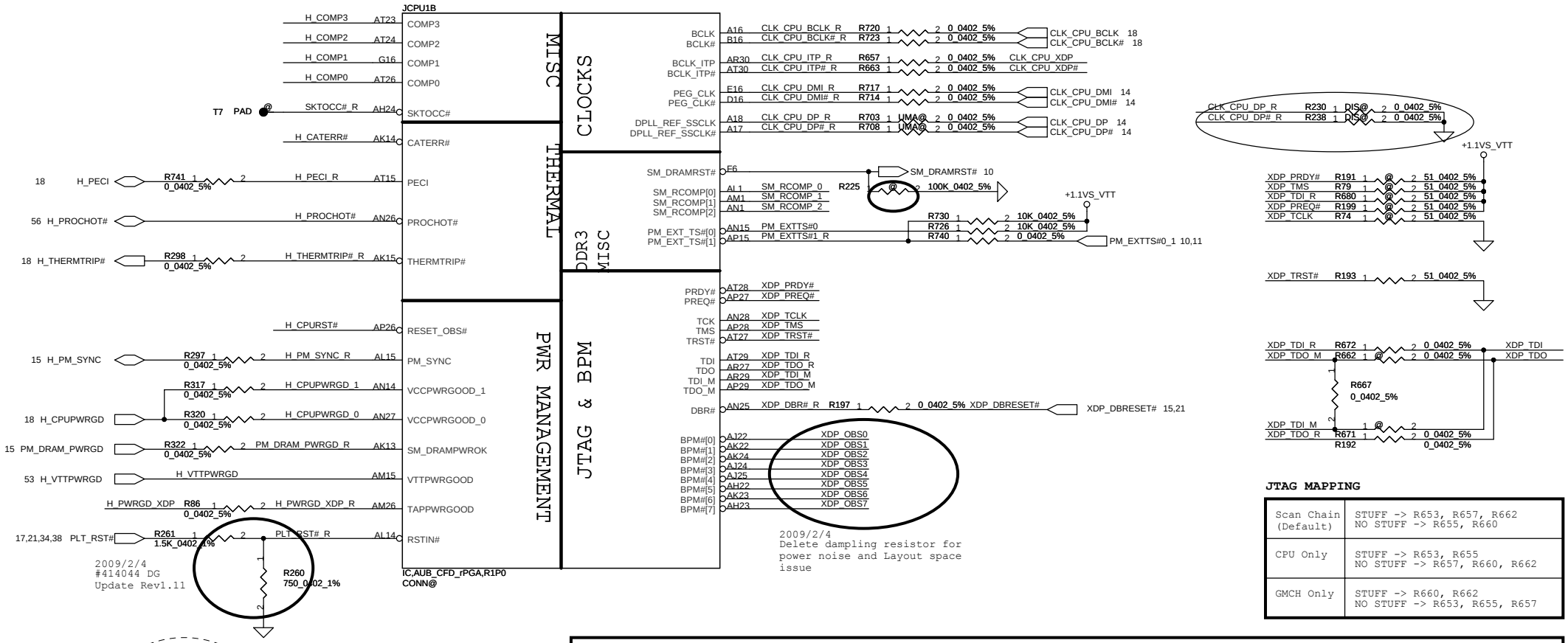
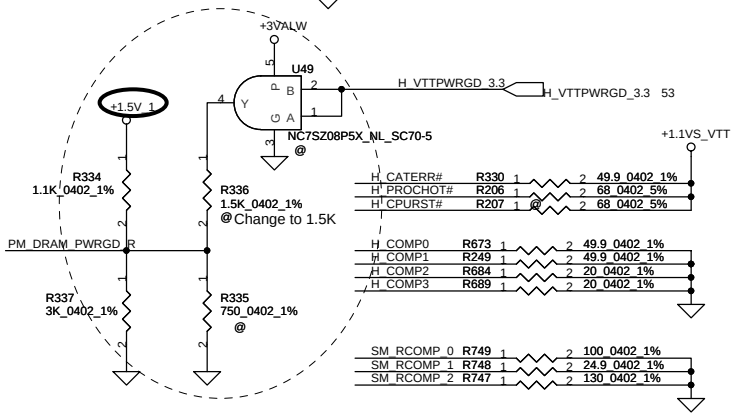


JTAG MAPPING

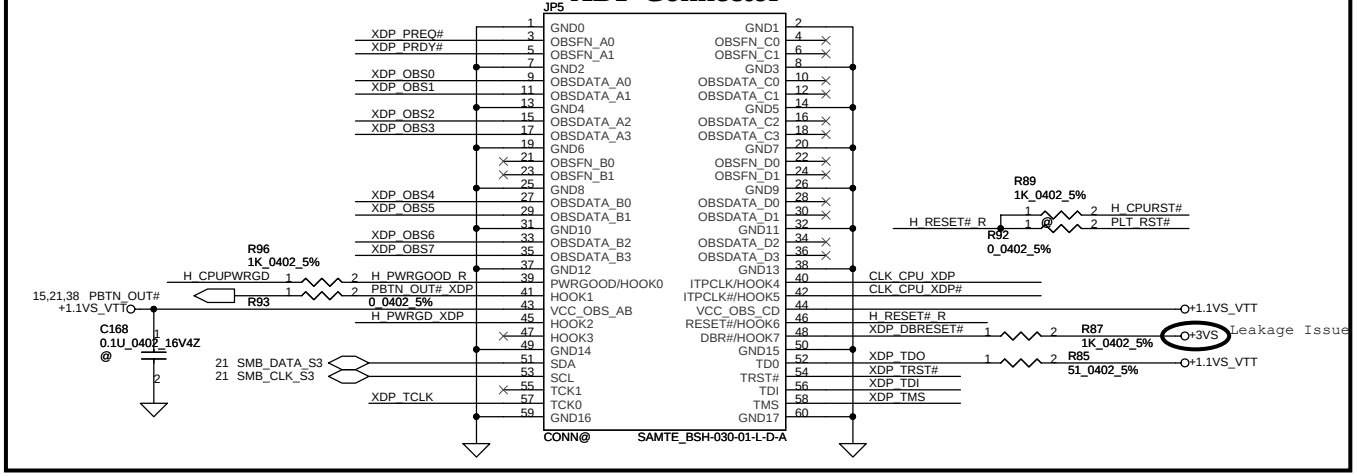
Scan Chain (Default)	STUFF -> R653, R657, R662 NO STUFF -> R655, R660
CPU Only	STUFF -> R653, R655 NO STUFF -> R657, R660, R662
GMCH Only	STUFF -> R660, R662 NO STUFF -> R653, R655, R657



When implement S3 power reduction not to pop R337 pop U49,R336,R335,R334...

2009/4/13
Intel Suggestion by Desige guide V1.52

XDP Connector



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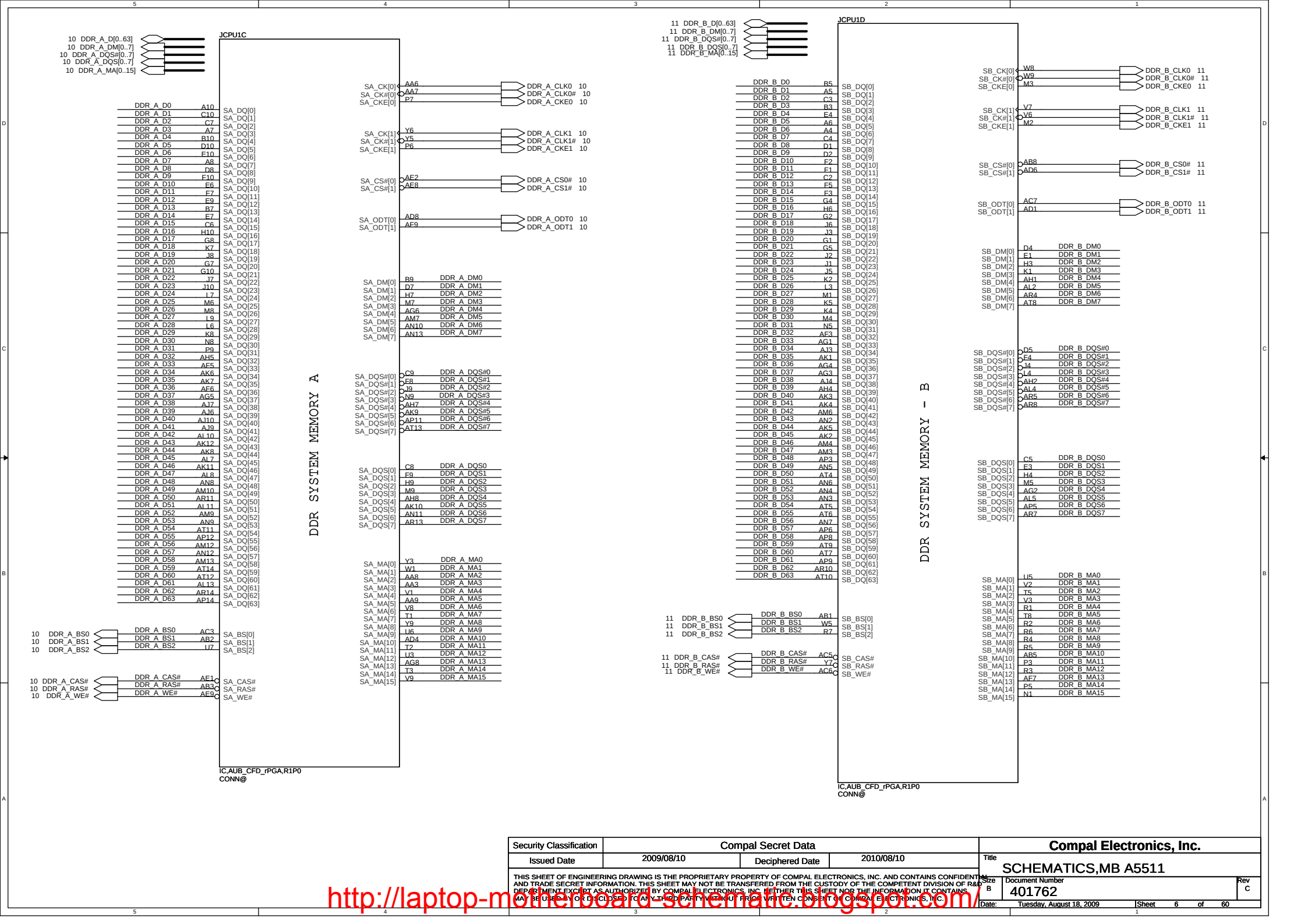

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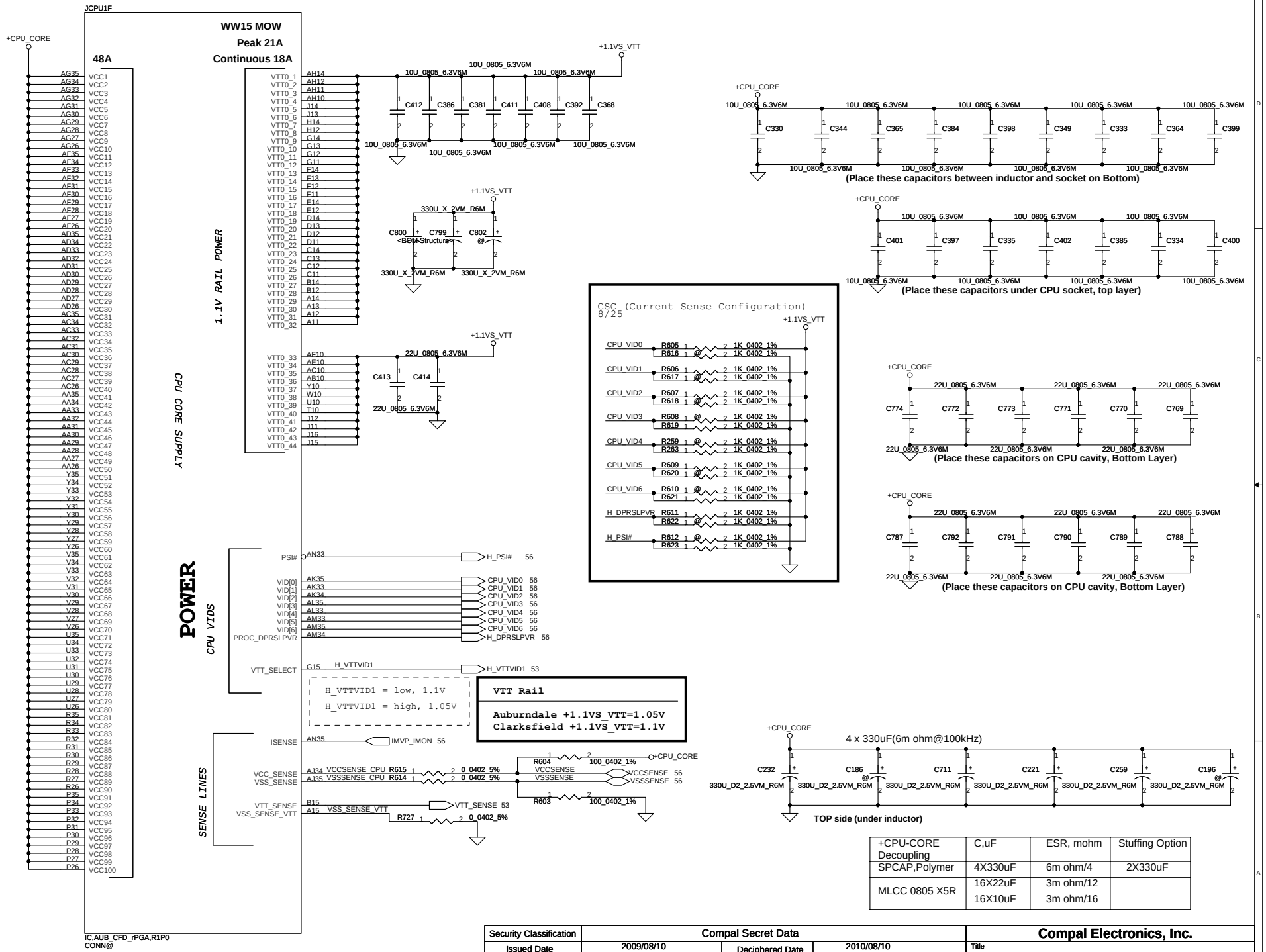

+CPU-CORE Decoupling	C,uF	ESR, mohm	Stuffing Option
SPCAP,Polymer	4X330uF	6m ohm/4	2X330uF
MLCC 0805 X5R	16X22uF 16X10uF	3m ohm/12 3m ohm/16	

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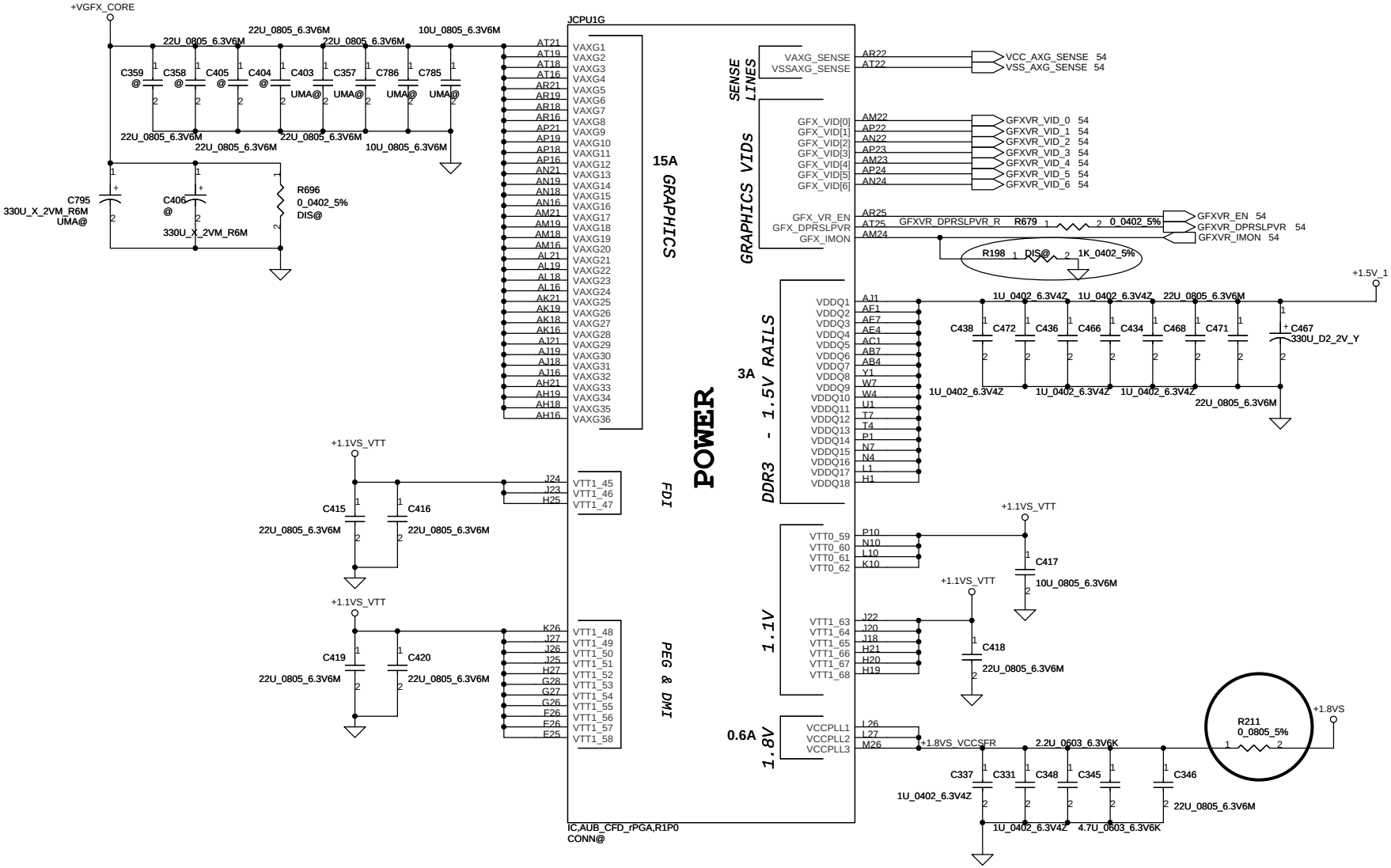

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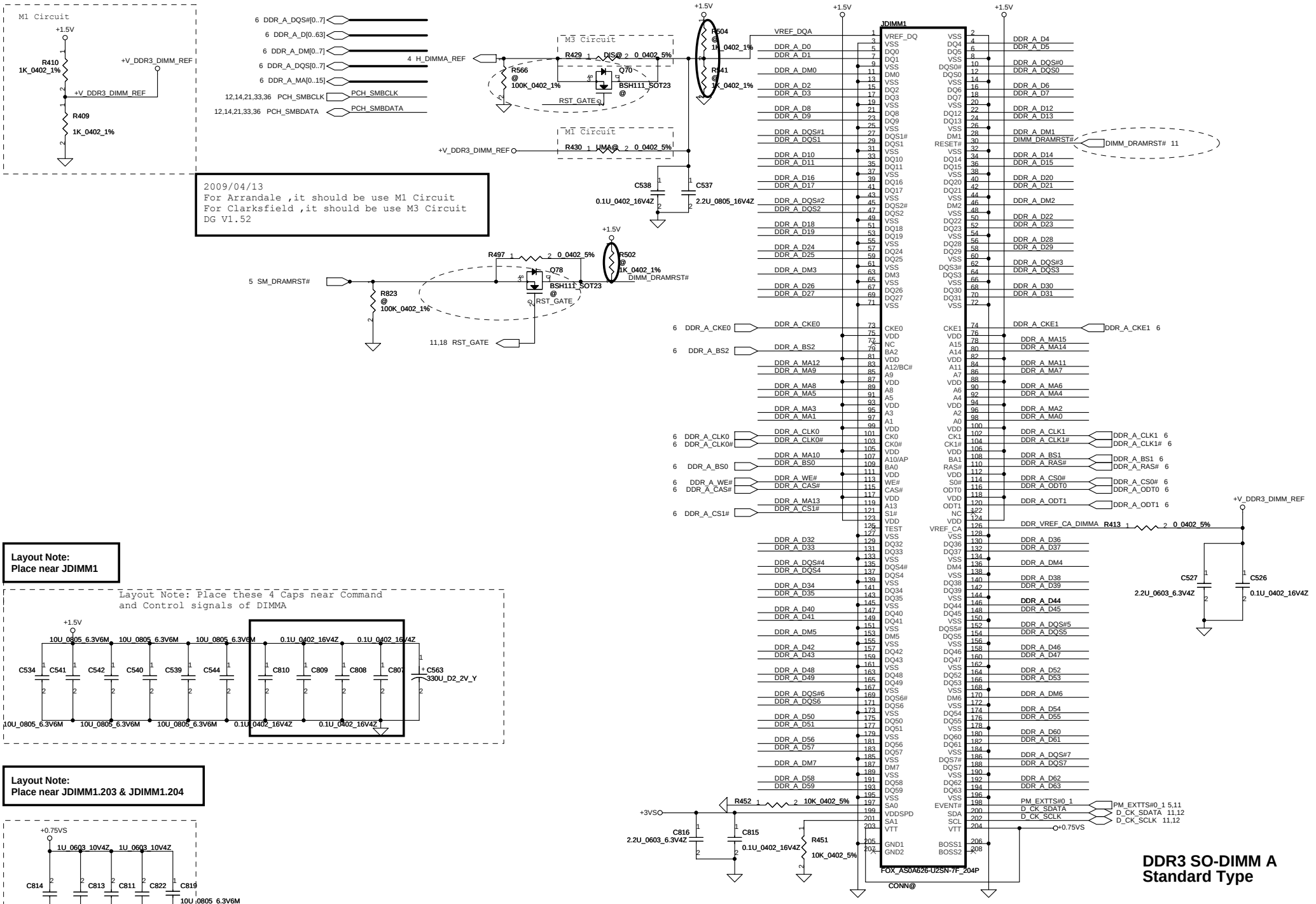

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2008/9/8 #400755
Calpella Clarksfield
DDR3 SO-DIMM
VREFDQ Platform
Design Guide Change Details

6 DDR_B_DQS#[0..7]
6 DDR_B_D[0..63]
6 DDR_B_DM[0..7]
6 DDR_B_DQS[0..7]
6 DDR_B_MA[0..15]
12,14,21,33,36 PCH_SMBCLK — PCH_SMBCLK
12,14,21,33,36 PCH_SMBDATA — PCH_SMBDATA

4 H_DIMMB_REF
R824 @ 100K_0402_1%
M3 Circuit
R445 1 2 0_0402_5%
DIS@ Q77 BSH111_SOT23 @
RST_GATE
10,18 RST_GATE
R546 @ 1K_0402_1%
R550 @ 1K_0402_1%
+1.5V

M1 Circuit
UMA@
+V_DDR3_DIMM_REF
R446 1 2 0_0402_5%

2009/04/13
For Arrandale ,it should be use M1 Circuit
For Clarksfield ,it should be use M3 Circuit
DG V1.52

C553 2.2U_0805_16V4Z
C554 0.1U_0402_16V4Z

JDIMM2

VREF_DQ	1	2	VSS		
VSS	3	4	DQ4	DDR_B_D4	
DQ0	DDR_B_D0	5	6	DQ5	DDR_B_D5
DQ1	DDR_B_D1	7	8	VSS	
VSS	9	10	DQS0#	DDR_B_DQS#0	
DM0	DDR_B_DM0	11	12	DQS0	DDR_B_DQS0
VSS	13	14	VSS		
DQ2	DDR_B_D2	15	16	DQ6	DDR_B_D6
DQ3	DDR_B_D3	17	18	DQ7	DDR_B_D7
VSS	19	20	VSS		
DQ8	DDR_B_D8	21	22	DQ12	DDR_B_D12
DQ9	DDR_B_D9	23	24	DQ13	DDR_B_D13
VSS	25	26	VSS		
DQS1#	DDR_B_DQS#1	27	28	DM1	DDR_B_DM1
DQS1	DDR_B_DQS1	29	30	RESET#	DIMM_DRAMRST# — DIMM_DRAMRST# 10
VSS	31	32	VSS		
DQ10	DDR_B_D10	33	34	DQ14	DDR_B_D14
DQ11	DDR_B_D11	35	36	DQ15	DDR_B_D15
VSS	37	38	VSS		
DQ16	DDR_B_D16	39	40	DQ20	DDR_B_D20
DQ17	DDR_B_D17	41	42	DQ21	DDR_B_D21
VSS	43	44	VSS		
DQS2#	DDR_B_DQS#2	45	46	DM2	DDR_B_DM2
DQS2	DDR_B_DQS2	47	48	VSS	
VSS	49	50	DQ22	DDR_B_D22	
DQ18	DDR_B_D18	51	52	DQ23	DDR_B_D23
DQ19	DDR_B_D19	53	54	VSS	
VSS	55	56	DQ28	DDR_B_D28	
DQ24	DDR_B_D24	57	58	DQ29	DDR_B_D29
DQ25	DDR_B_D25	59	60	VSS	
VSS	61	62	DQS3#	DDR_B_DQS#3	
DM3	DDR_B_DM3	63	64	DQS3	DDR_B_DQS3
VSS	65	66	VSS		
DQ26	DDR_B_D26	67	68	DQ30	DDR_B_D30
DQ27	DDR_B_D27	69	70	DQ31	DDR_B_D31
VSS	71	72	VSS		
CKE0	6 DDR_B_CKE0 — DDR_B_CKE0	73	74	CKE1	DDR_B_CKE1 — DDR_B_CKE1 6
VDD	75	76	VDD		
NC	77	78	A15	DDR_B_MA15	
BA2	6 DDR_B_BS2 — DDR_B_BS2	79	80	A14	DDR_B_MA14
VDD	81	82	VDD		
A12/BC#	DDR_B_MA12	83	84	A11	DDR_B_MA11
A9	DDR_B_MA9	85	86	A7	DDR_B_MA7
VDD	87	88	VDD		
A8	DDR_B_MA8	89	90	A6	DDR_B_MA6
A5	DDR_B_MA5	91	92	A4	DDR_B_MA4
VDD	93	94	VDD		
A3	DDR_B_MA3	95	96	A2	DDR_B_MA2
A1	DDR_B_MA1	97	98	A0	DDR_B_MA0
VDD	99	100	VDD		
CK0	6 DDR_B_CLK0 — DDR_B_CLK0	101	102	CK1	DDR_B_CLK1 — DDR_B_CLK1 6
CK0#	6 DDR_B_CLK0# — DDR_B_CLK0#	103	104	CK1#	DDR_B_CLK1# — DDR_B_CLK1# 6
VDD	105	106	VDD		
A10/AP	DDR_B_MA10	107	108	BA1	DDR_B_BS1 — DDR_B_BS1 6
BA0	DDR_B_BS0 — 6 DDR_B_BS0	109	110	RAS#	DDR_B_RAS# — DDR_B_RAS# 6
VDD	111	112	VDD		
WE#	DDR_B_WE# — 6 DDR_B_WE#	113	114	S0#	DDR_B_CS0# — DDR_B_CS0# 6
CAS#	DDR_B_CAS# — 6 DDR_B_CAS#	115	116	ODT0	DDR_B_ODT0 — DDR_B_ODT0 6
VDD	117	118	VDD		
A13	DDR_B_MA13	119	120	ODT1	DDR_B_ODT1 — DDR_B_ODT1 6
S1#	DDR_B_CS1# — 6 DDR_B_CS1#	121	122	NC	
VDD	123	124	VDD		
TEST	125	126	VREF_CA	DDR_VREF_CA_DIMMB	R442 1 2 0_0402_5% — +V_DDR3_DIMM_REF
VSS	127	128	VSS		
DQ32	DDR_B_D32	129	130	DQ36	DDR_B_D36
DQ33	DDR_B_D33	131	132	DQ37	DDR_B_D37
VSS	133	134	VSS		
DQS4#	DDR_B_DQS#4	135	136	DM4	DDR_B_DM4
DQS4	DDR_B_DQS4	137	138	VSS	
VSS	139	140	DQ38	DDR_B_D38	
DQ34	DDR_B_D34	141	142	DQ39	DDR_B_D39
DQ35	DDR_B_D35	143	144	VSS	
VSS	145	146	DQ44	DDR_B_D44	
DQ40	DDR_B_D40	147	148	DQ45	DDR_B_D45
DQ41	DDR_B_D41	149	150	VSS	
VSS	151	152	DQS5#	DDR_B_DQS#5	
DM5	DDR_B_DM5	153	154	DQS5	DDR_B_DQS5
VSS	155	156	VSS		
DQ42	DDR_B_D42	157	158	DQ46	DDR_B_D46
DQ43	DDR_B_D43	159	160	DQ47	DDR_B_D47
VSS	161	162	VSS		
DQ48	DDR_B_D48	163	164	DQ52	DDR_B_D52
DQ49	DDR_B_D49	165	166	DQ53	DDR_B_D53
VSS	167	168	VSS		
DQS6#	DDR_B_DQS#6	169	170	DM6	DDR_B_DM6
DQS6	DDR_B_DQS6	171	172	VSS	
VSS	173	174	DQ54	DDR_B_D54	
DQ50	DDR_B_D50	175	176	DQ55	DDR_B_D55
DQ51	DDR_B_D51	177	178	VSS	
VSS	179	180	DQ60	DDR_B_D60	
DQ56	DDR_B_D56	181	182	DQ61	DDR_B_D61
DQ57	DDR_B_D57	183	184	VSS	
VSS	185	186	DQS7#	DDR_B_DQS#7	
DM7	DDR_B_DM7	187	188	DQS7	DDR_B_DQS7
VSS	189	190	VSS		
DQ58	DDR_B_D58	191	192	DQ62	DDR_B_D62
DQ59	DDR_B_D59	193	194	DQ63	DDR_B_D63
VSS	195	196	VSS		
SA0	197	198	EVENT#	PM_EXTTS#0_1 — PM_EXTTS#0_1 5,10	
VDDSPD	199	200	SDA	D_CK_SDATA — D_CK_SDATA 10,12	
SA1	201	202	SCL	D_CK_SCLK — D_CK_SCLK 10,12	
VTT	203	204	VTT	+0.75VS	
GND1	205	206	BOSS1		
GND2	207	208	BOSS2		

R773 1 2 10K_0402_5%
+3VSO
R453 1 2 10K_0402_5%
C569 2.2U_0603_6.3V4Z
C568 0.1U_0402_16V4Z

TYCO_2-2013310-1_204P
CONN@

Layout Note: Place near JDIMM2

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

+1.5V
C839 10U_0805_6.3V6M
C860 10U_0805_6.3V6M
C852
C862 10U_0805_6.3V6M
C845 0.1U_0402_16V4Z
C856 0.1U_0402_16V4Z
C844
C843
C842
C841
C855 330U_D2_2V_Y

Layout Note: Place near JDIMM2.203 & JDIMM2.204

+0.75VS
C825 1U_0603_10V4Z
C827
C837
C836
C838 10U_0805_6.3V6M

C552 2.2U_0603_6.3V4Z
C551 0.1U_0402_16V4Z

DDR3 SO-DIMM B Standard Type

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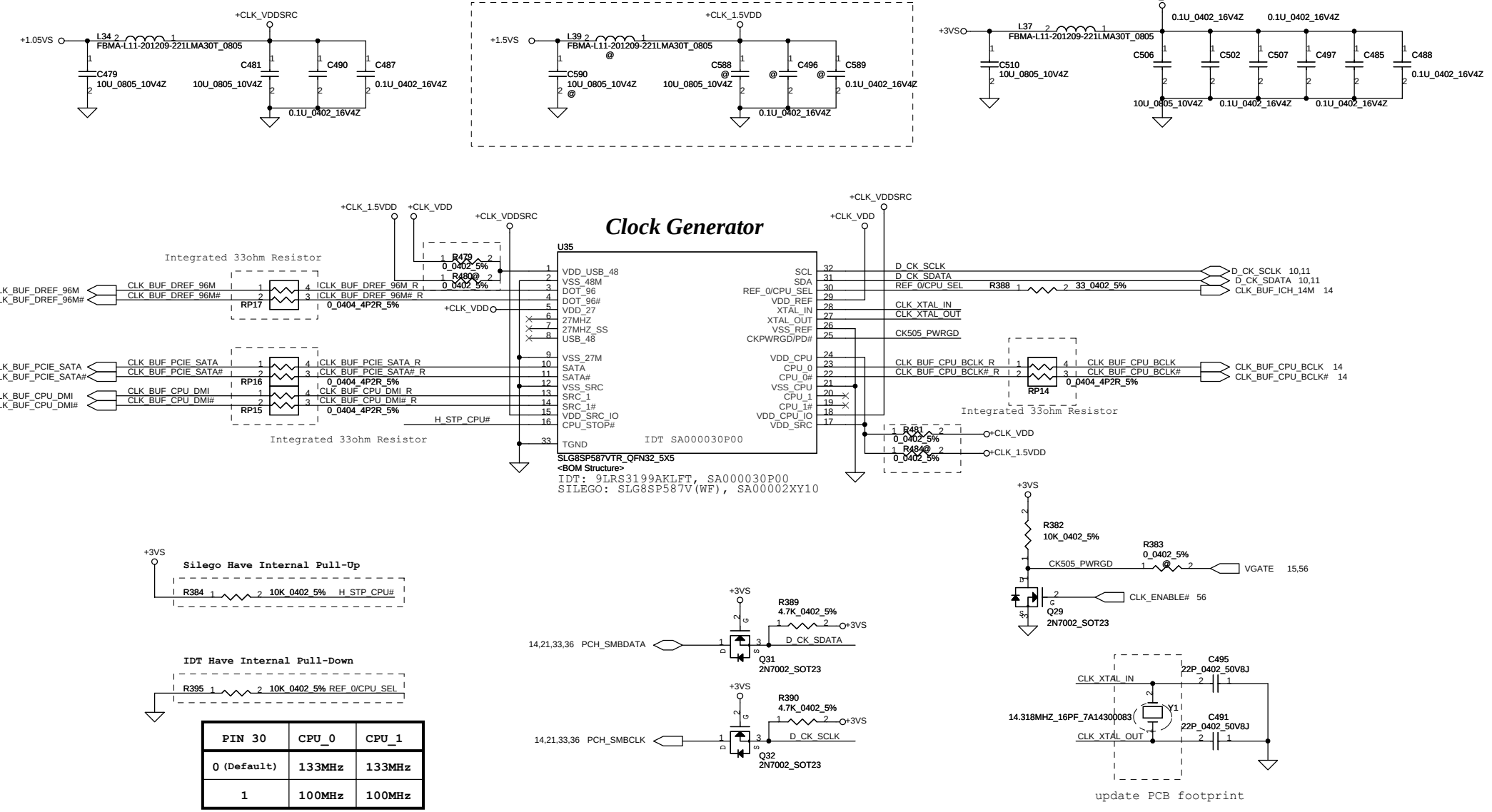

PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz

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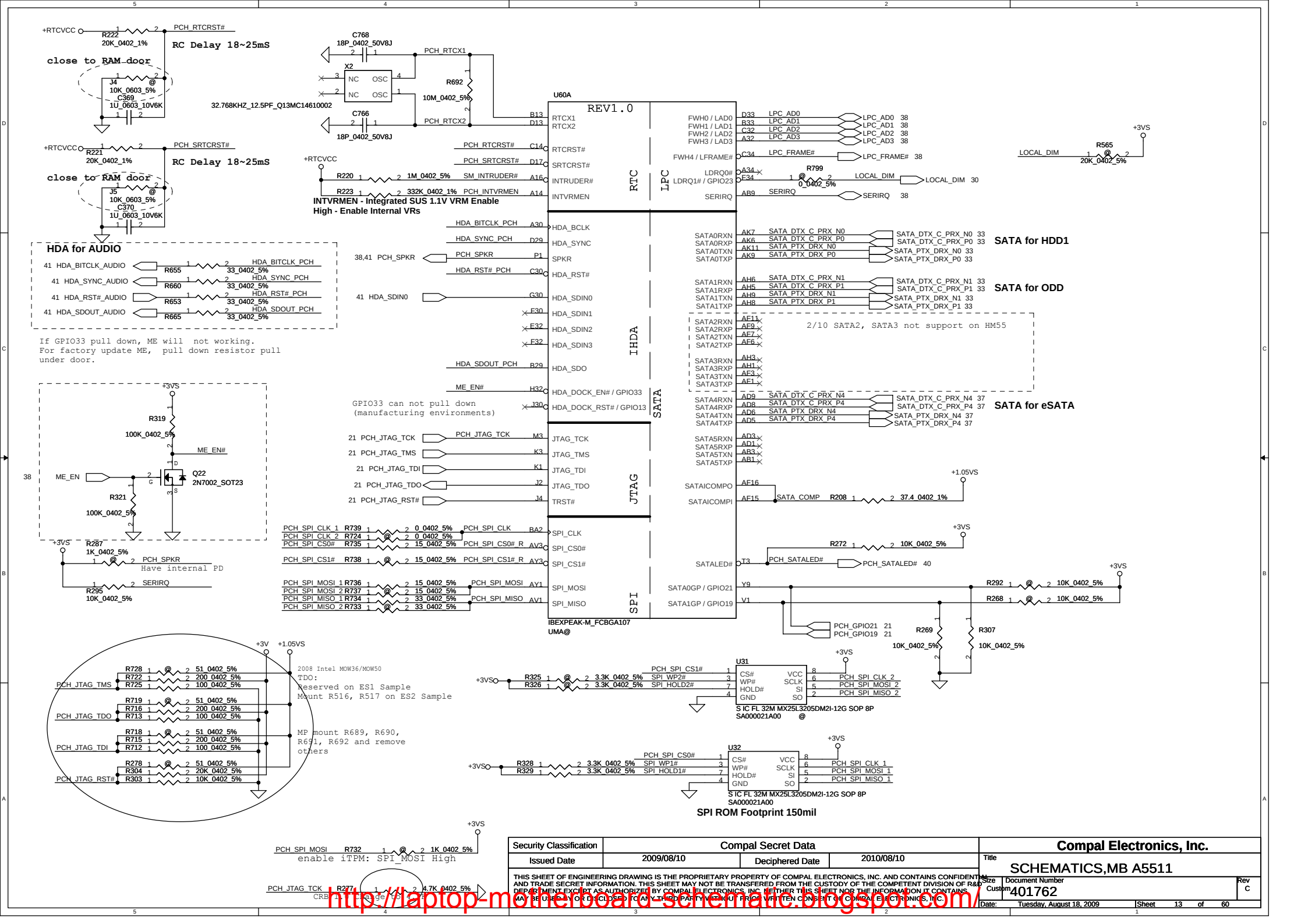

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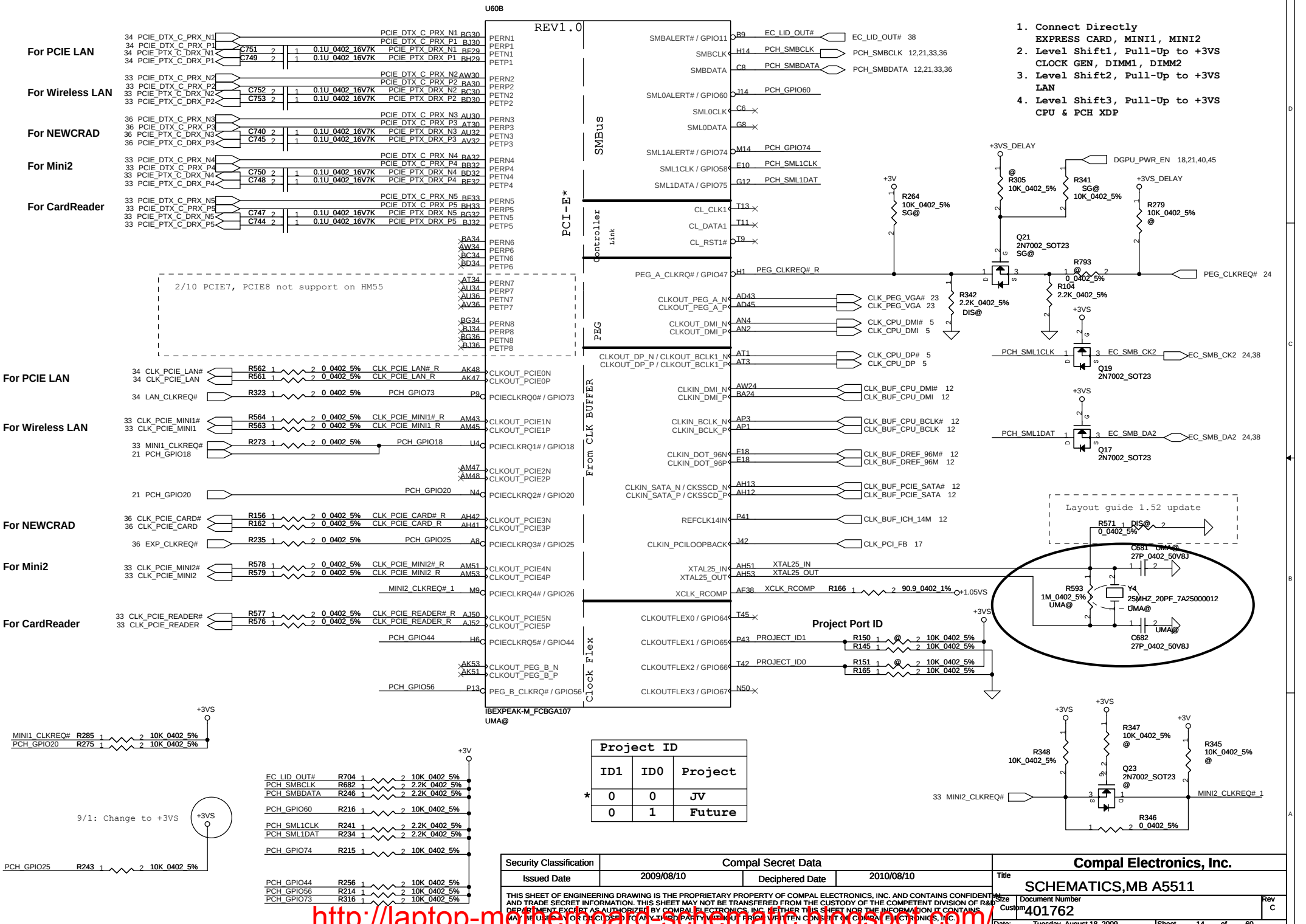

4 DMI_HTX_PRX_N[0..3] DMI_HTX_PRX_N[0..3]
4 DMI_HTX_PRX_P[0..3] DMI_HTX_PRX_P[0..3]
4 DMI_PTX_HRX_N[0..3] DMI_PTX_HRX_N[0..3]
4 DMI_PTX_HRX_P[0..3] DMI_PTX_HRX_P[0..3]

4 H_FDI_TXN[0..7] H_FDI_TXN[0..7]
4 H_FDI_TXP[0..7] H_FDI_TXP[0..7]

U60C

REV1.0

DMI_HTX_PRX_N0 BC24 DMI0RXN
DMI_HTX_PRX_N1 BJ22 DMI1RXN
DMI_HTX_PRX_N2 AW20 DMI2RXN
DMI_HTX_PRX_N3 BJ20 DMI3RXN
DMI_HTX_PRX_P0 BD24 DMI0RXP
DMI_HTX_PRX_P1 BG22 DMI1RXP
DMI_HTX_PRX_P2 BA20 DMI2RXP
DMI_HTX_PRX_P3 BG20 DMI3RXP
DMI_PTX_HRX_N0 BE22 DMI0TXN
DMI_PTX_HRX_N1 BE21 DMI1TXN
DMI_PTX_HRX_N2 BD20 DMI2TXN
DMI_PTX_HRX_N3 BE18 DMI3TXN
DMI_PTX_HRX_P0 BD22 DMI0TXP
DMI_PTX_HRX_P1 BH21 DMI1TXP
DMI_PTX_HRX_P2 BC20 DMI2TXP
DMI_PTX_HRX_P3 BD18 DMI3TXP
BH25 DMI_ZCOMP
DMI_COMP BF25 DMI_IRCOMP

DMI

FDI_RXN0 BA18 H_FDI_TXN0
FDI_RXN1 BH17 H_FDI_TXN1
FDI_RXN2 BD16 H_FDI_TXN2
FDI_RXN3 BJ16 H_FDI_TXN3
FDI_RXN4 BA16 H_FDI_TXN4
FDI_RXN5 BE14 H_FDI_TXN5
FDI_RXN6 BA14 H_FDI_TXN6
FDI_RXN7 BC12 H_FDI_TXN7
FDI_RXP0 BB18 H_FDI_TXP0
FDI_RXP1 BF17 H_FDI_TXP1
FDI_RXP2 BC16 H_FDI_TXP2
FDI_RXP3 BG16 H_FDI_TXP3
FDI_RXP4 AW16 H_FDI_TXP4
FDI_RXP5 BD14 H_FDI_TXP5
FDI_RXP6 BB14 H_FDI_TXP6
FDI_RXP7 BD12 H_FDI_TXP7
FDI_INT BJ14 H_FDI_INT 4
FDI_FSYNC0 BF13 H_FDI_FSYNC0 4
FDI_FSYNC1 BH13 H_FDI_FSYNC1 4
FDI_LSYNC0 BJ12 H_FDI_LSYNC0 4
FDI_LSYNC1 BG14 H_FDI_LSYNC1 4

+3VS
R283 1 2 8.2K_0402_5% PM_CLKRUN#
R309 1 @ 2 10K_0402_5% XDP_DBRESET#

+3V
R276 1 2 10K_0402_5% SUS_PWR_ACK
R709 1 2 8.2K_0402_5% PCH_GPIO72
R195 1 2 10K_0402_5% EC_SWI#
R245 1 2 1K_0402_5% PCH_PCIE_WAKE#
R252 1 @ 2 10K_0402_5% PM_SLP_LAN#

+1.05VS
R656 49.9_0402_1% <BOM Structure>

5,21 XDP_DBRESET# XDP_DBRESET# T6 SYS_RESET#
SYS_PWROK R289 0_0402_5% SYS_PWROK_R M6 SYS_PWROK
VGATE R288 @ 0_0402_5%
SYS_PWROK B17 PWROK
R301 ME_PWROK 0_0402_5% K5 MEPWROK
LAN_RST# A10 LAN_RST#
5 PM_DRAM_PWRGD D9 DRAMPWROK
PCH_RSMRST# C16 RSMRST#
38 SUS_PWR_ACK SUS_PWR_ACK M1 SUS_PWR_DN_ACK / GPIO30
10/2 Intel suggestion change to 10K
5,21,38 PBTN_OUT# PBTN_OUT# P5 PWRBTN#
+3V R315 100K_0402_5%
24,38 ACIN_BUF D17 CH751H-40PT_SOD323-2 PCH_ACIN P7 ACPRESENT / GPIO31
PCH_GPIO72 A6 BATLOW# / GPIO72
38 EC_SWI# EC_SWI# F14 RI#

System Power Management

WAKE# J12 PCH_PCIE_WAKE# PCH_PCIE_WAKE# 33,34,36
CLKRUN# / GPIO32 Y1 PM_CLKRUN# PM_CLKRUN# 38
SUS_STAT# / GPIO61 P8 PCH_GPIO61 @ PAD T8
SUSCLK / GPIO62 F3 PCH_GPIO62 @ PAD T10
SLP_S5# / GPIO63 F4 PM_SLP_S5# 38
SLP_S4# H7 PM_SLP_S4# 38
SLP_S3# P12 PM_SLP_S3# 38
SLP_M# K8 PM_SLP_M# @ PAD T9
TP23 N2 PM_SLP_DSW# @ PAD T19
PMSYNCH BJ10 H_PM_SYNC 5
SLP_LAN# / GPIO29 F6 PM_SLP_LAN#

IBEXPEAK-M_FCBGA107
UMA@

+3VS
21 SYS_PWROK SYS_PWROK 4 U27 NC7SZ08P5X_NL_SC70-5
EC_PWROK EC_PWROK 38
VGATE VGATE 12,56

SYS_PWROK R296 10K_0402_5%
EC_PWROK R311 10K_0402_5%
LAN_RST# R698 10K_0402_5%

No used Integrated LAN,
connecting LAN_RST# to GND

R676 @ 0_0402_5%
Q63 MMBT3906_SOT23-3
PCH_RSMRST# EC_RSMRST# 38
R681 10K_0402_5%
R194 4.7K_0402_5% +3V
D14A BAV99DW-7_SOT363
D14B BAV99DW-7_SOT363
R204 2.2K_0402_5%

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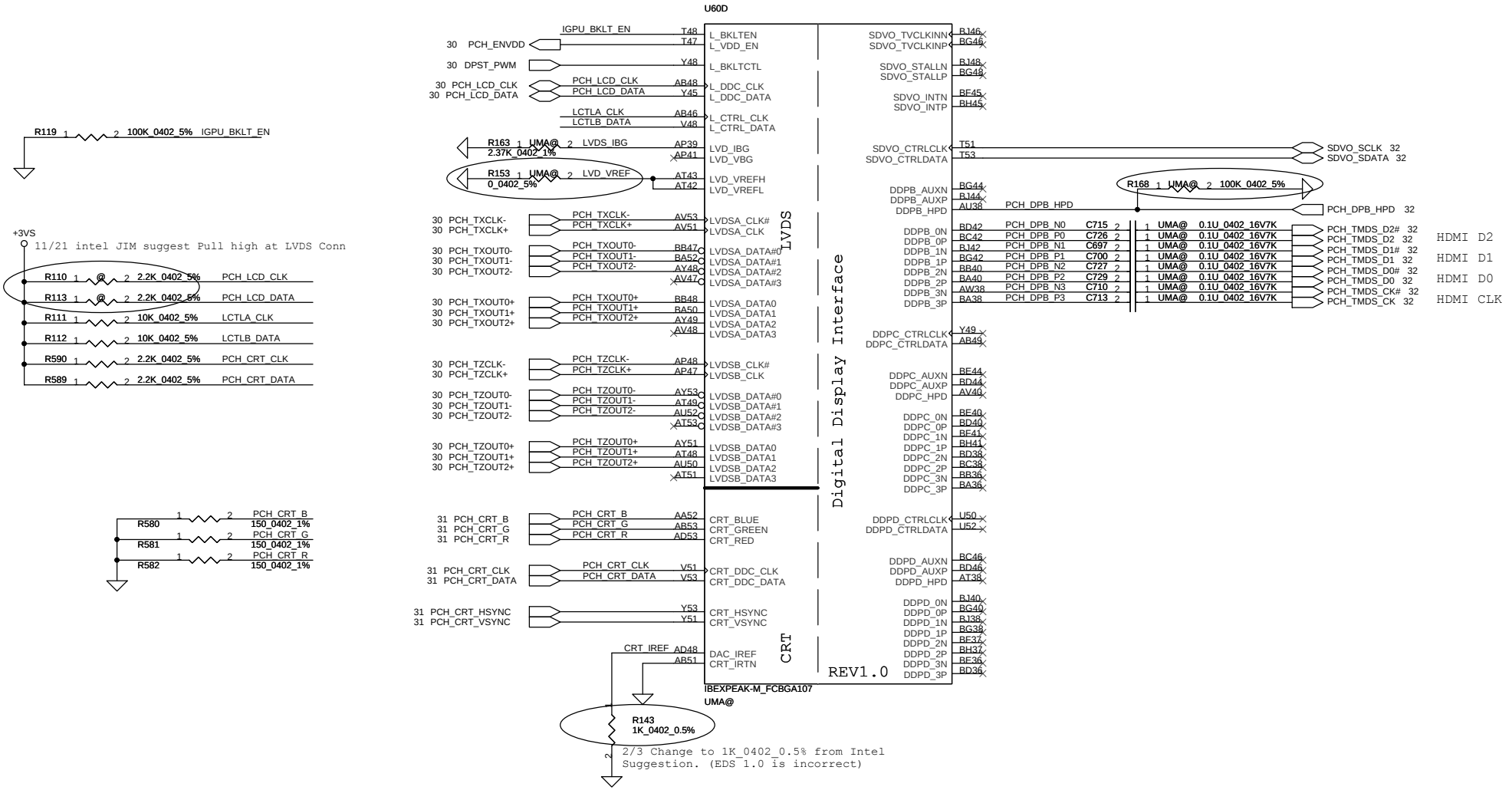

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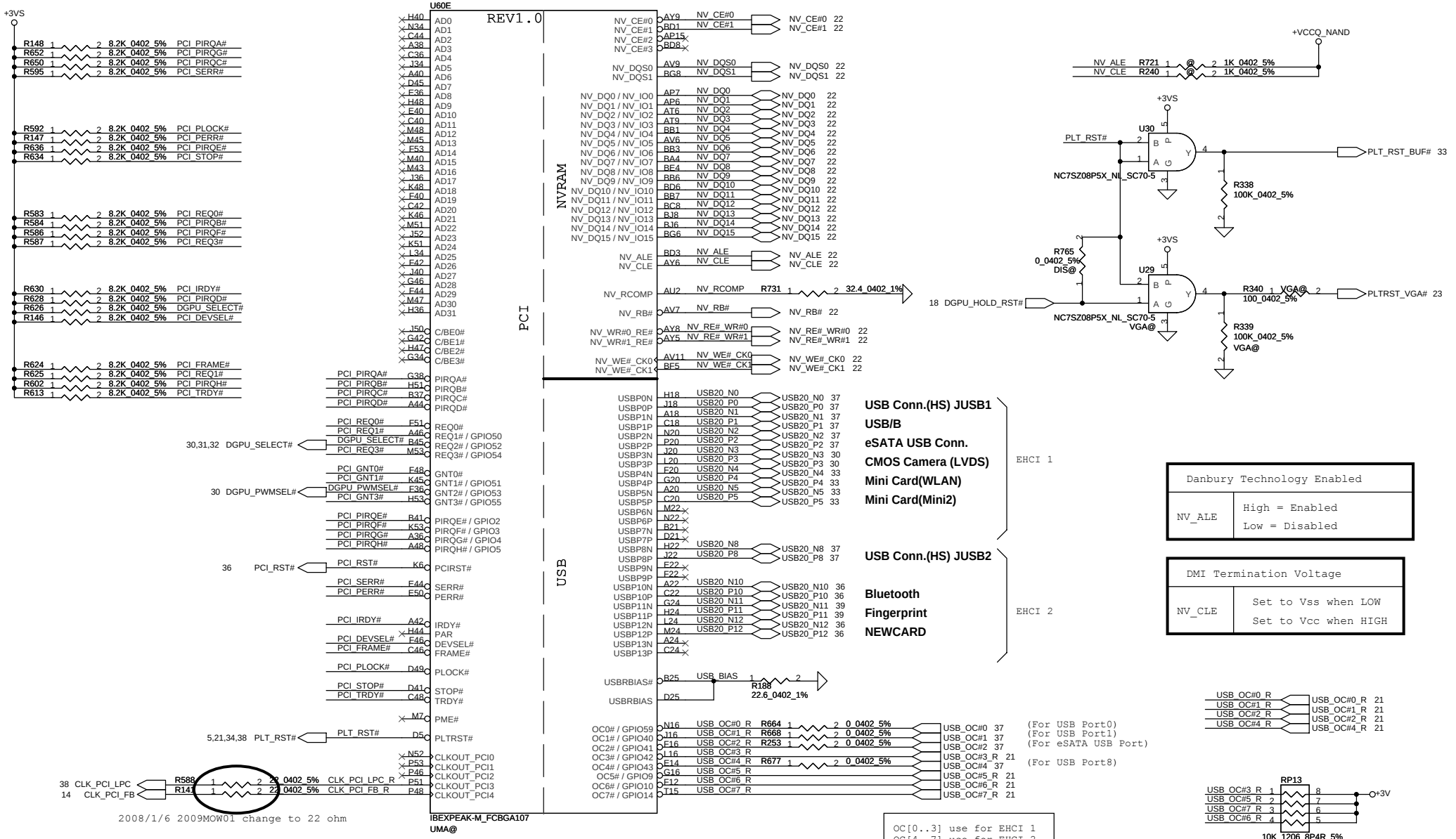

Danbury Technology Enabled	
NV_ALE	High = Enabled Low = Disabled

DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH

Boot BIOS Strap		
PCI_GNT#0	PCI_GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
* 1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap High = Default

PCI_GNT0# R123 1K_0402_5% Have internal PU
PCI_GNT1# R149 1K_0402_5% Have internal PU
PCI_GNT3# R585 1K_0402_5% Have internal PU

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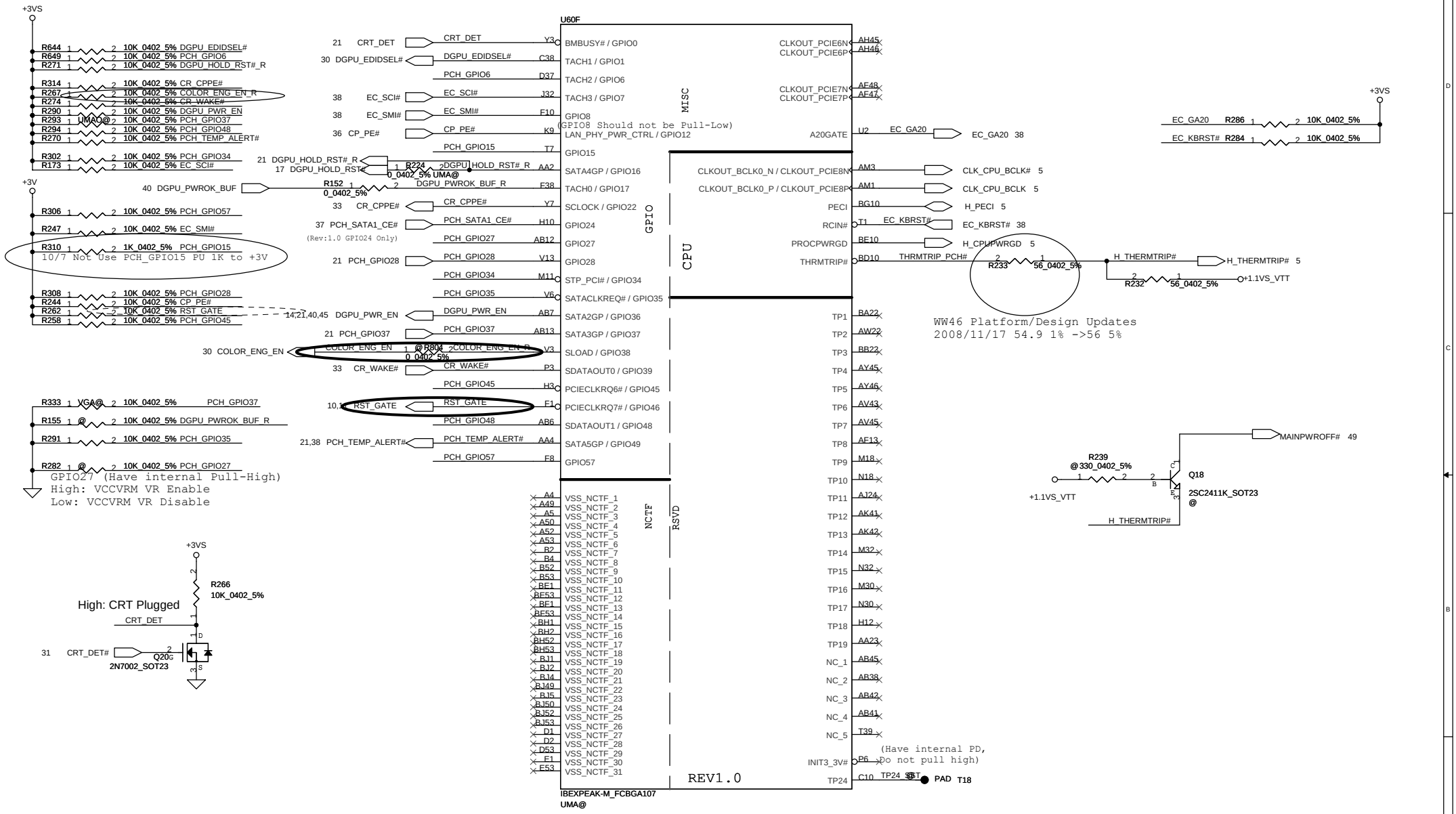

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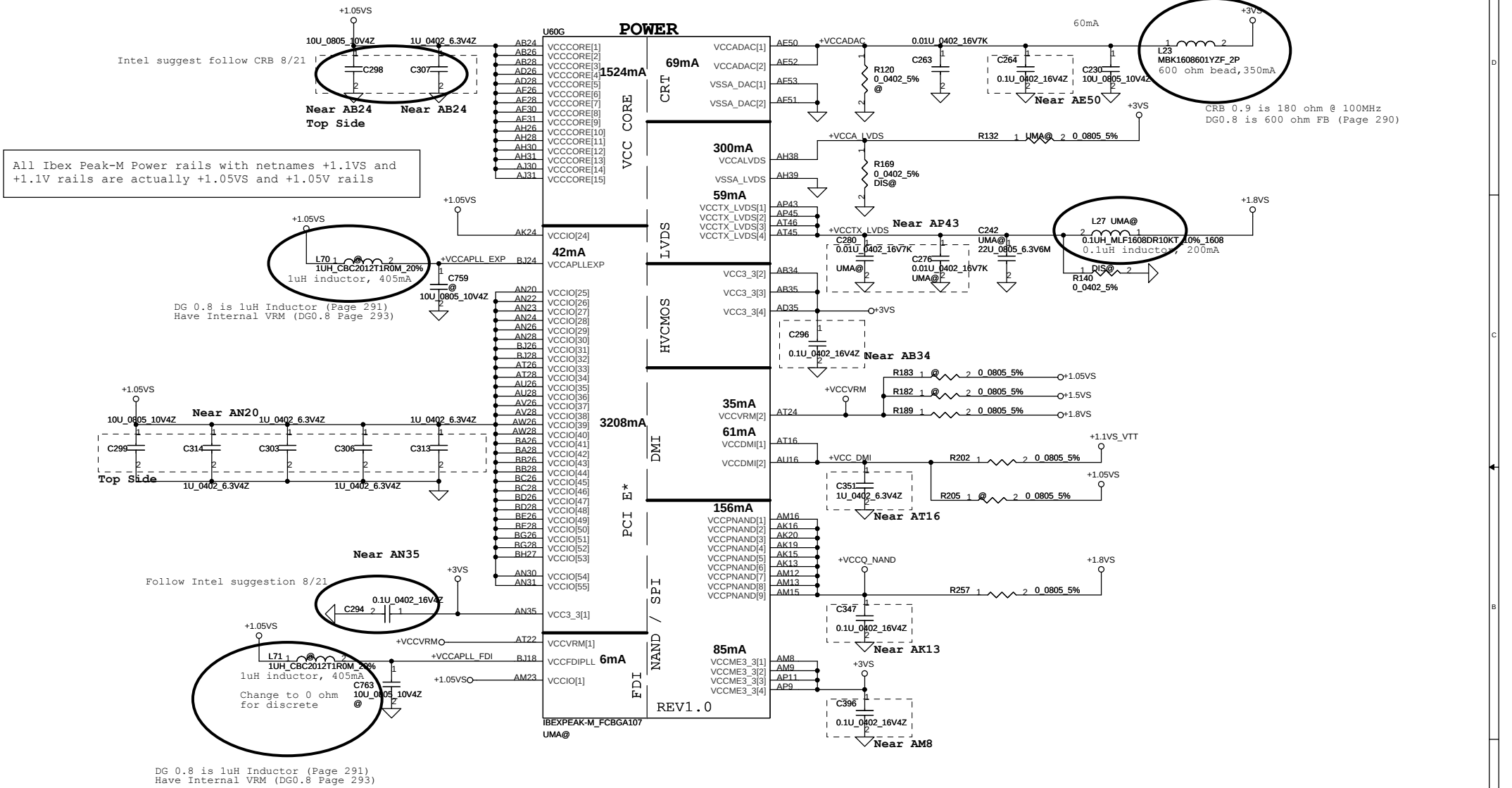

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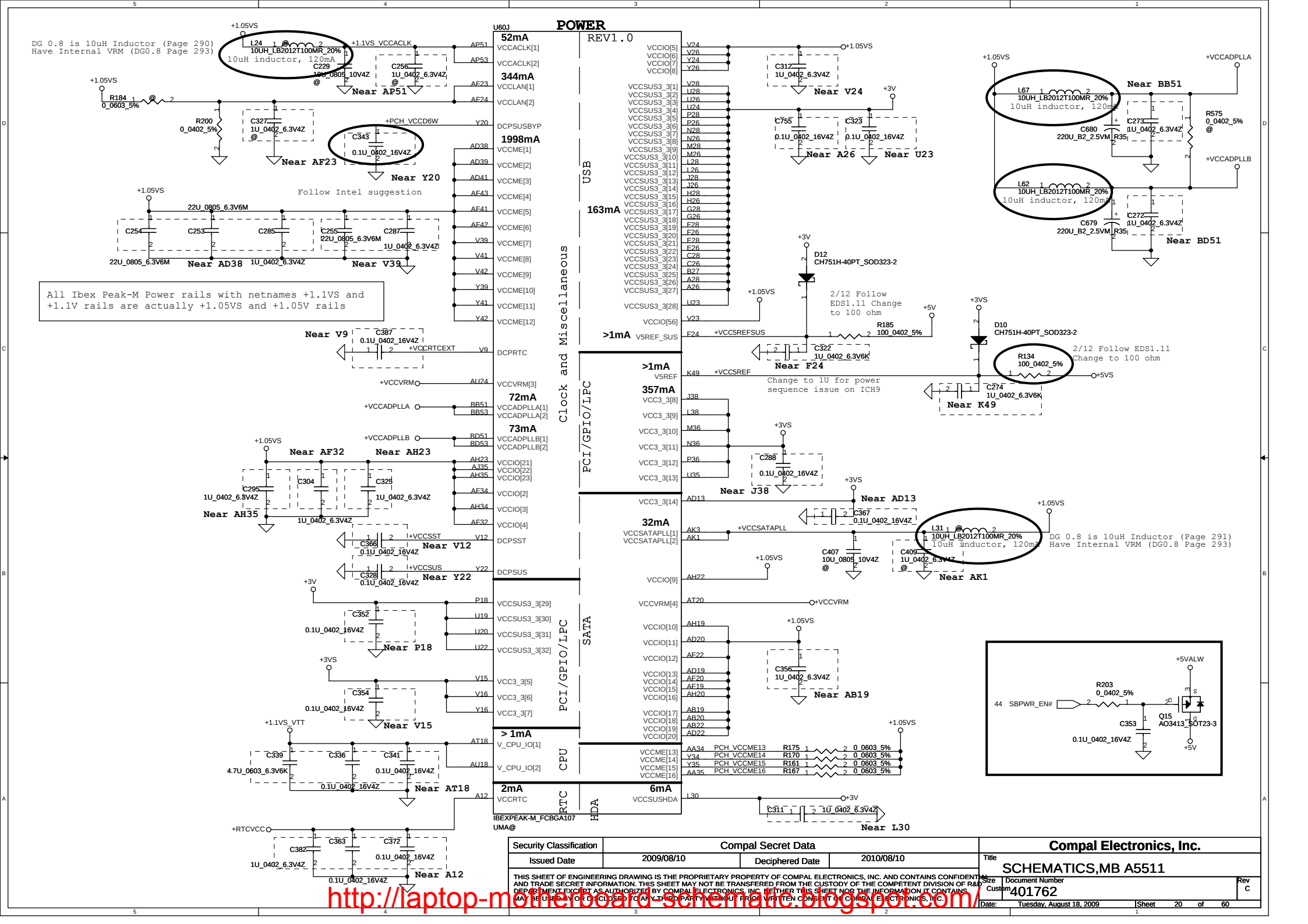
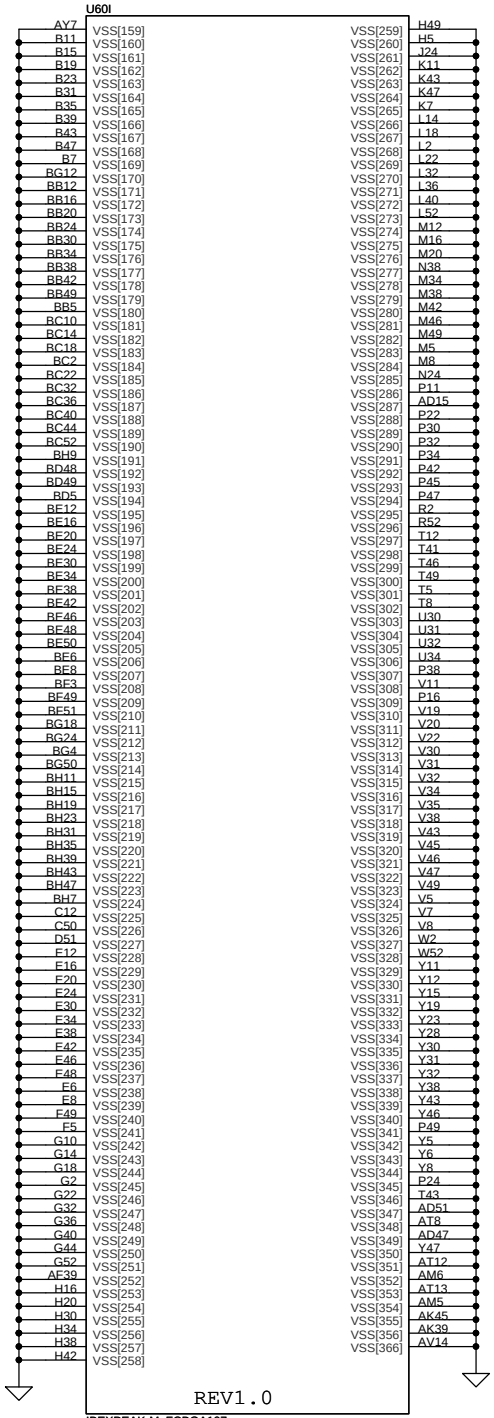
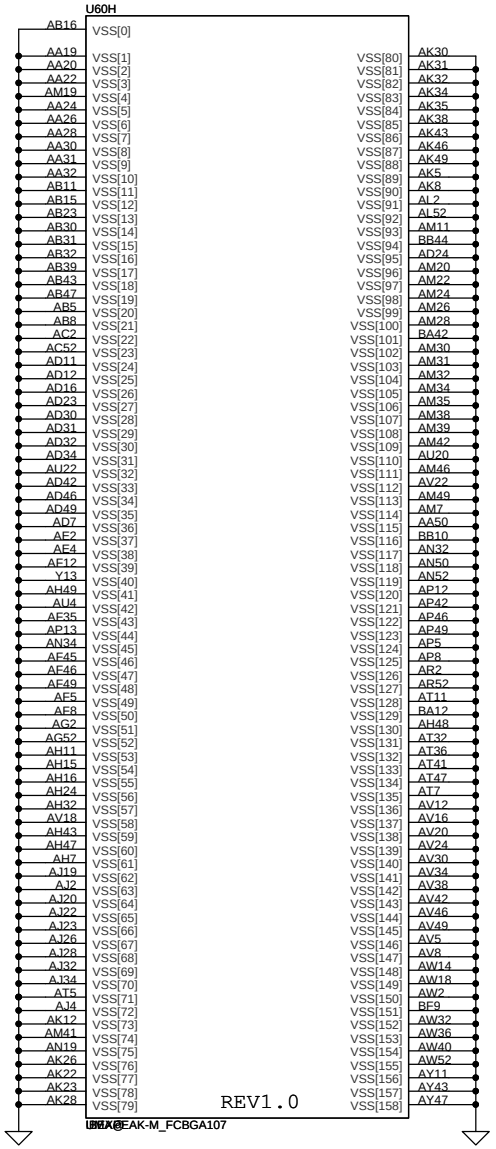
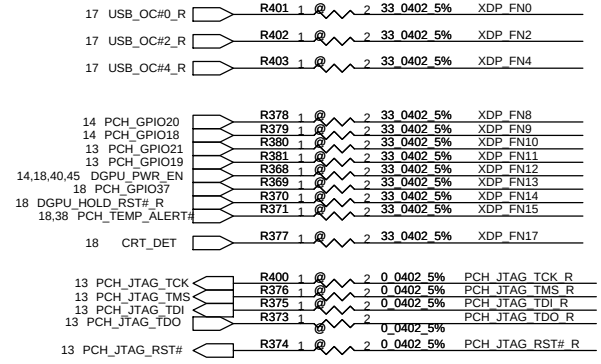
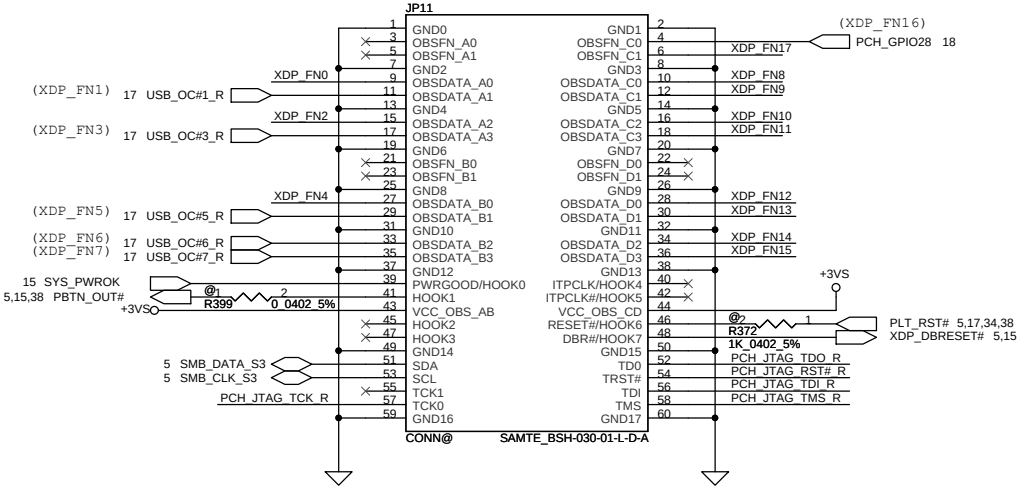


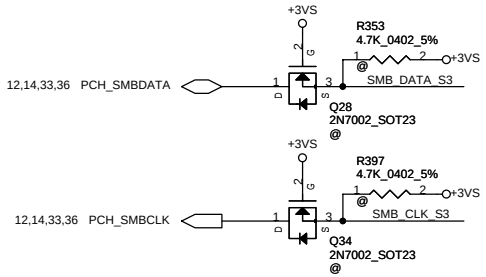
PCH XDP Port











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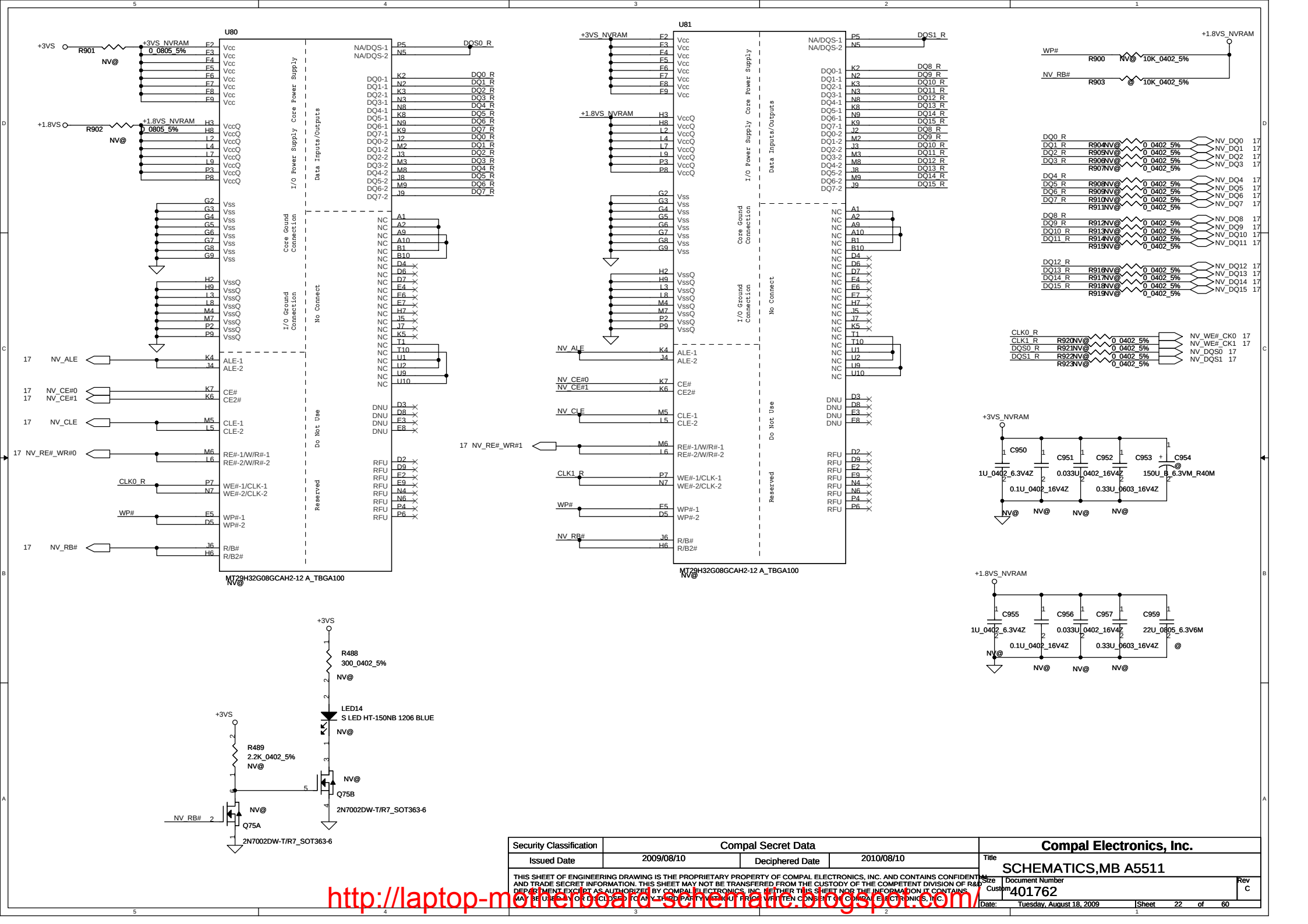

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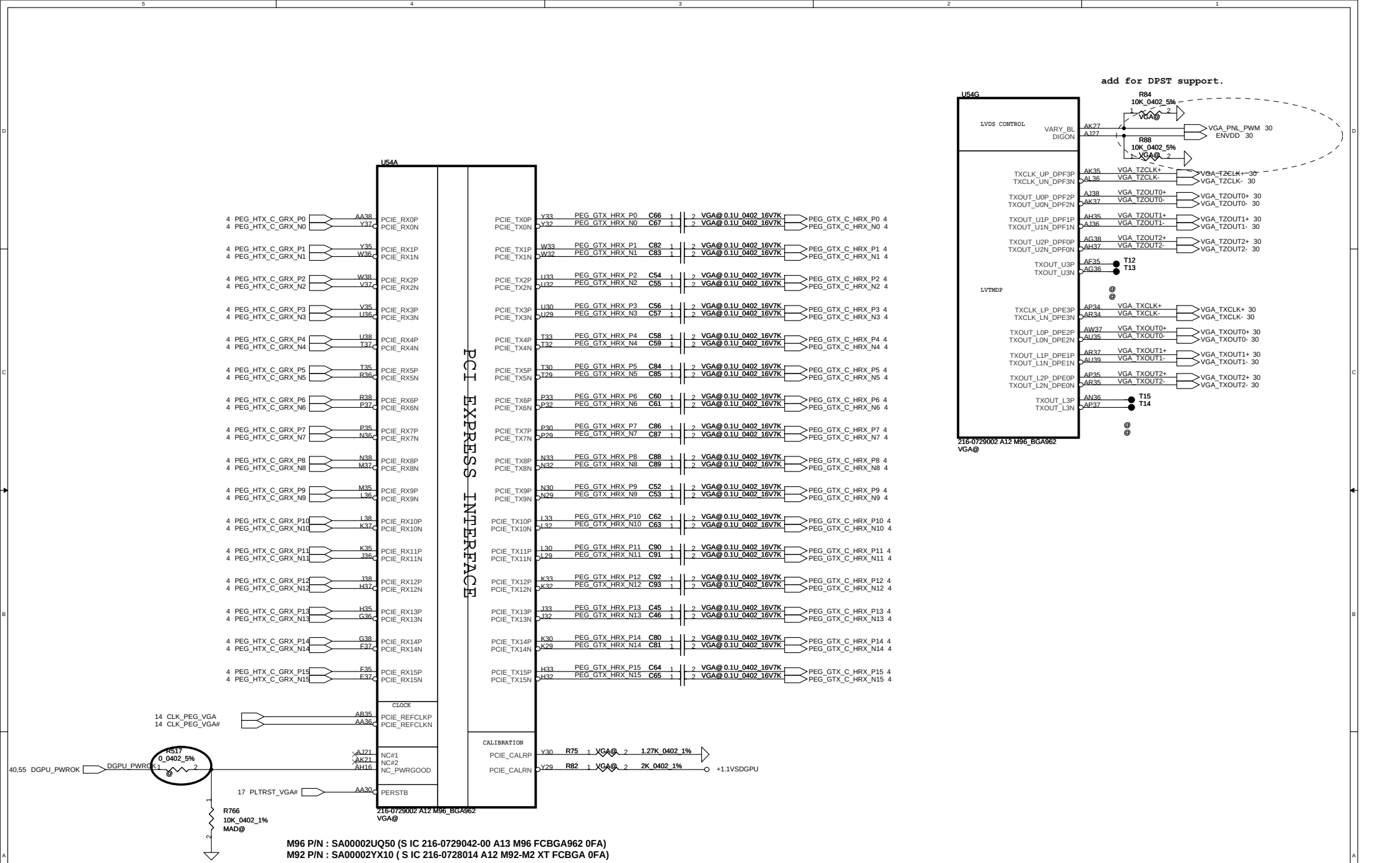

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Strap Name		Pin Straps description	Default
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	0
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	0
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
STRAP_BIF _CLK_PM_EN	GPIO22	Enable CLKREQ# Power Management 0: CLKREQ# power management capability is disabled 1: CLKREQ# power management capability is enabled	0
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
CCBYPASS	GENERICC		0
SMS_EN_HARD	H2SYNC		0
VIP_DEVICE _STRAP_DIS	V2SYNC	If VIP_DEVICE_STRAP_EN is set to ?? then this pin is used to sense whether a VIP slave device is connected to the VIP Host interface. If VIP_DEVICE_STRAP_EN is set to ?? then this pin is not used as a strap at all (i.e. its value during reset is unimportant), and it can be used as a regular GPIO	0

Location / VRAM	VRAM_ID3	VRAM_ID2	VRAM_ID1	VRAM_ID0
Samsung	O	O	O	O
HYNIX	1	O	O	O

External VGA Thermal Sensor

PWR Sequence

VGA_CORE (VDDC)
+1.8VS
+3VS_DELAY

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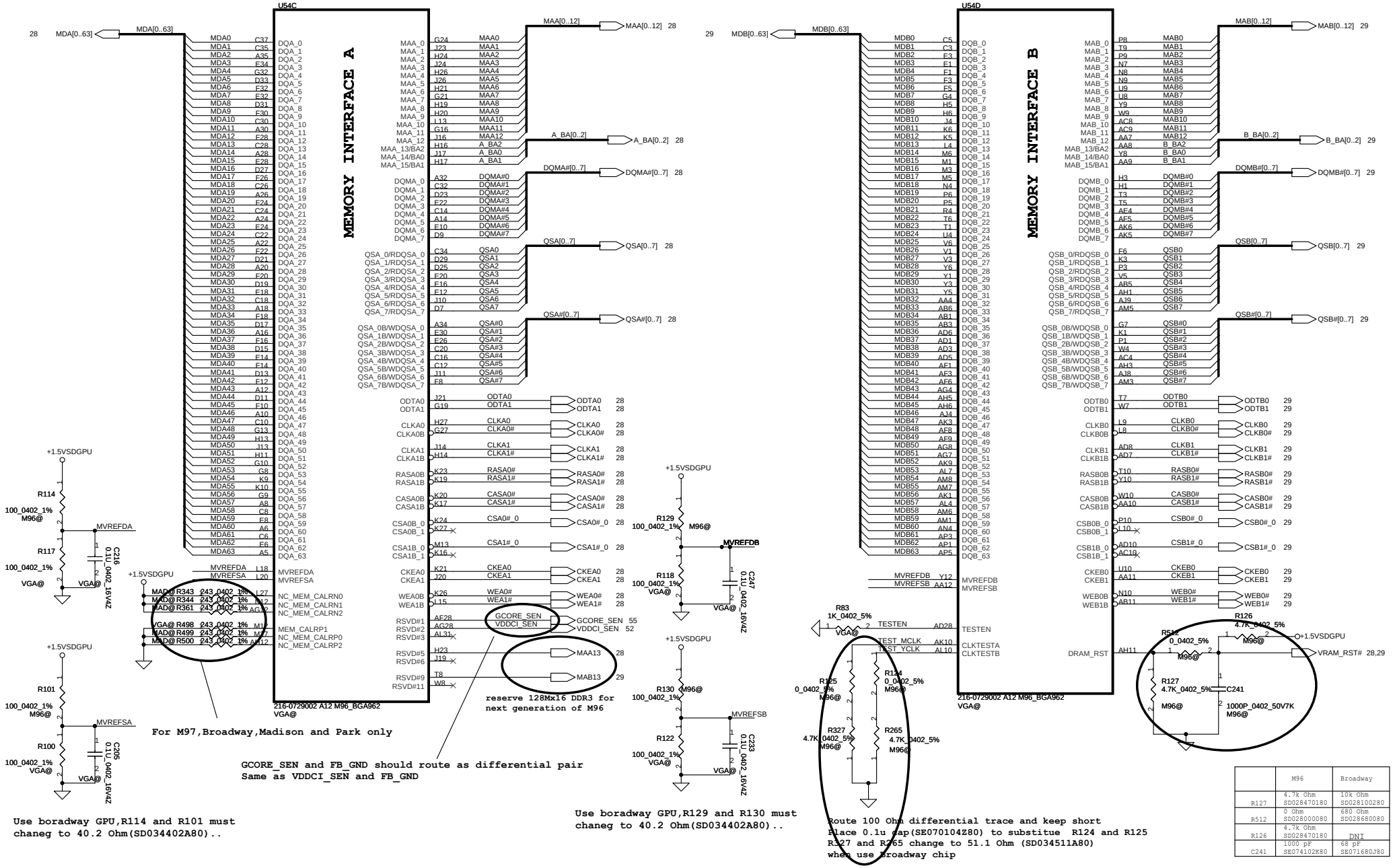

	M96	Broadway
R127	4.7k Ohm SD028470180	10k Ohm SD028100280
R512	0 Ohm SD028000080	680 Ohm SD028680080
R126	4.7k Ohm SD028470180	DNI
C241	1000 pF SE074102K80	68 pF SE071680J80

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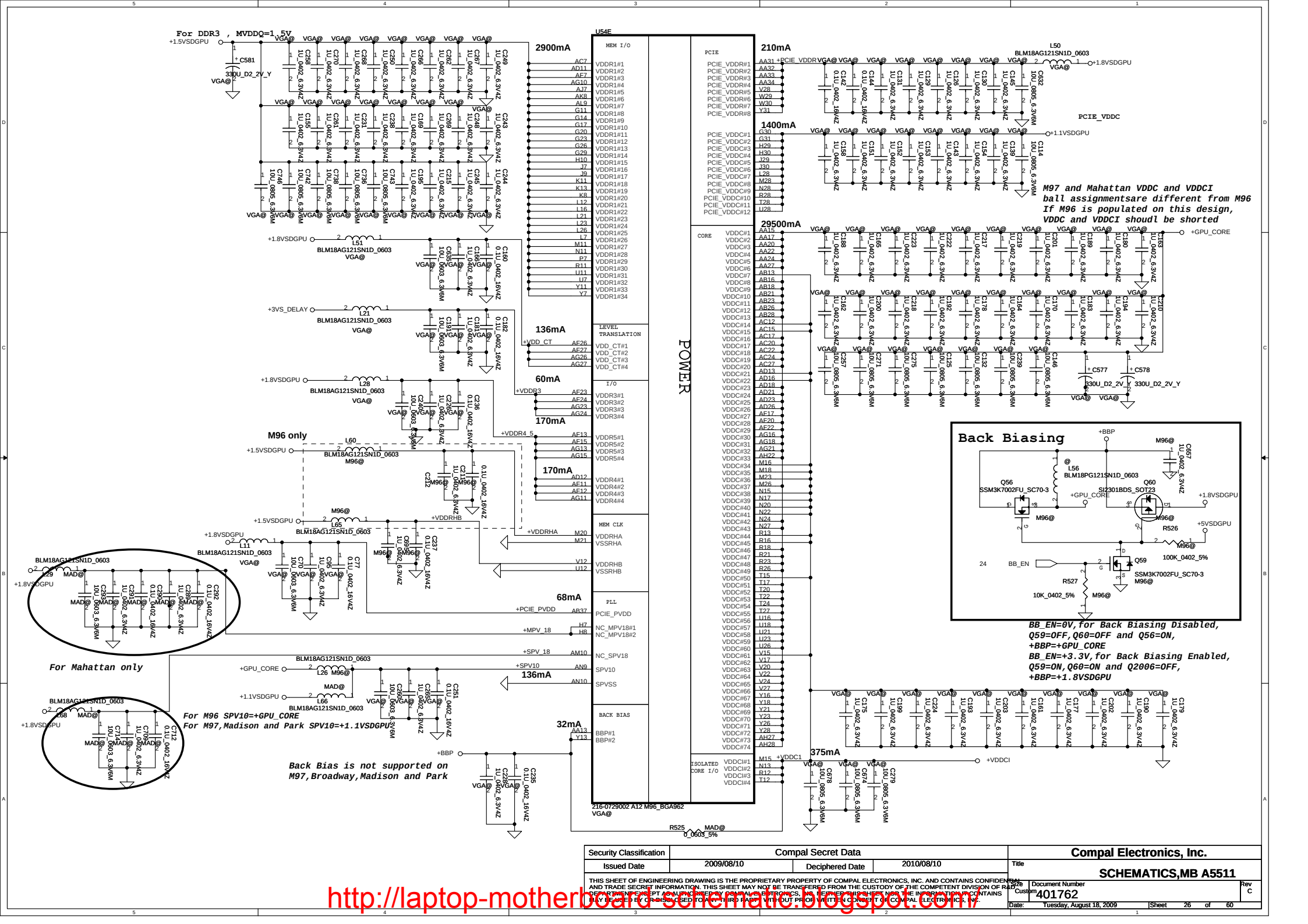

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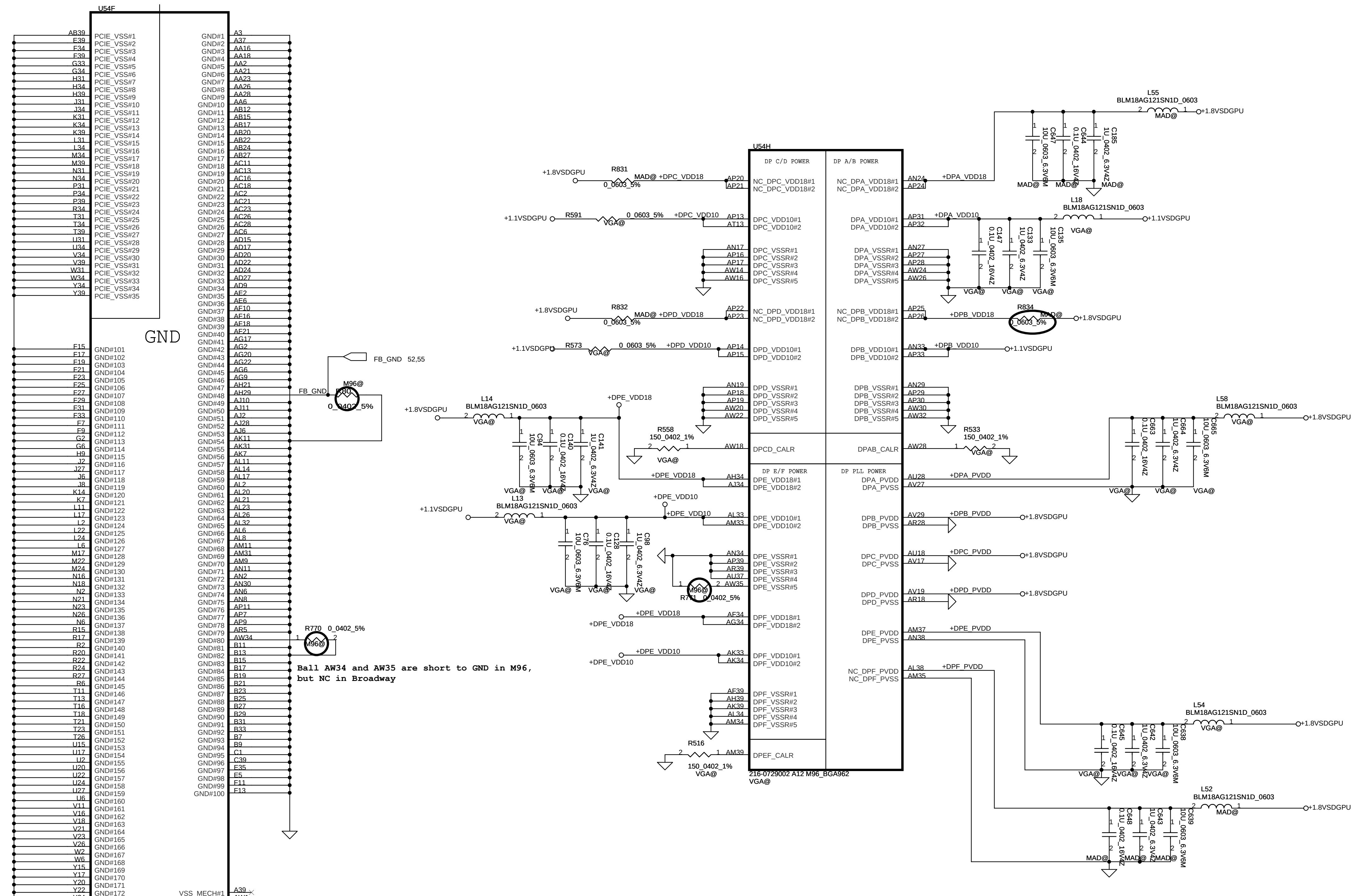

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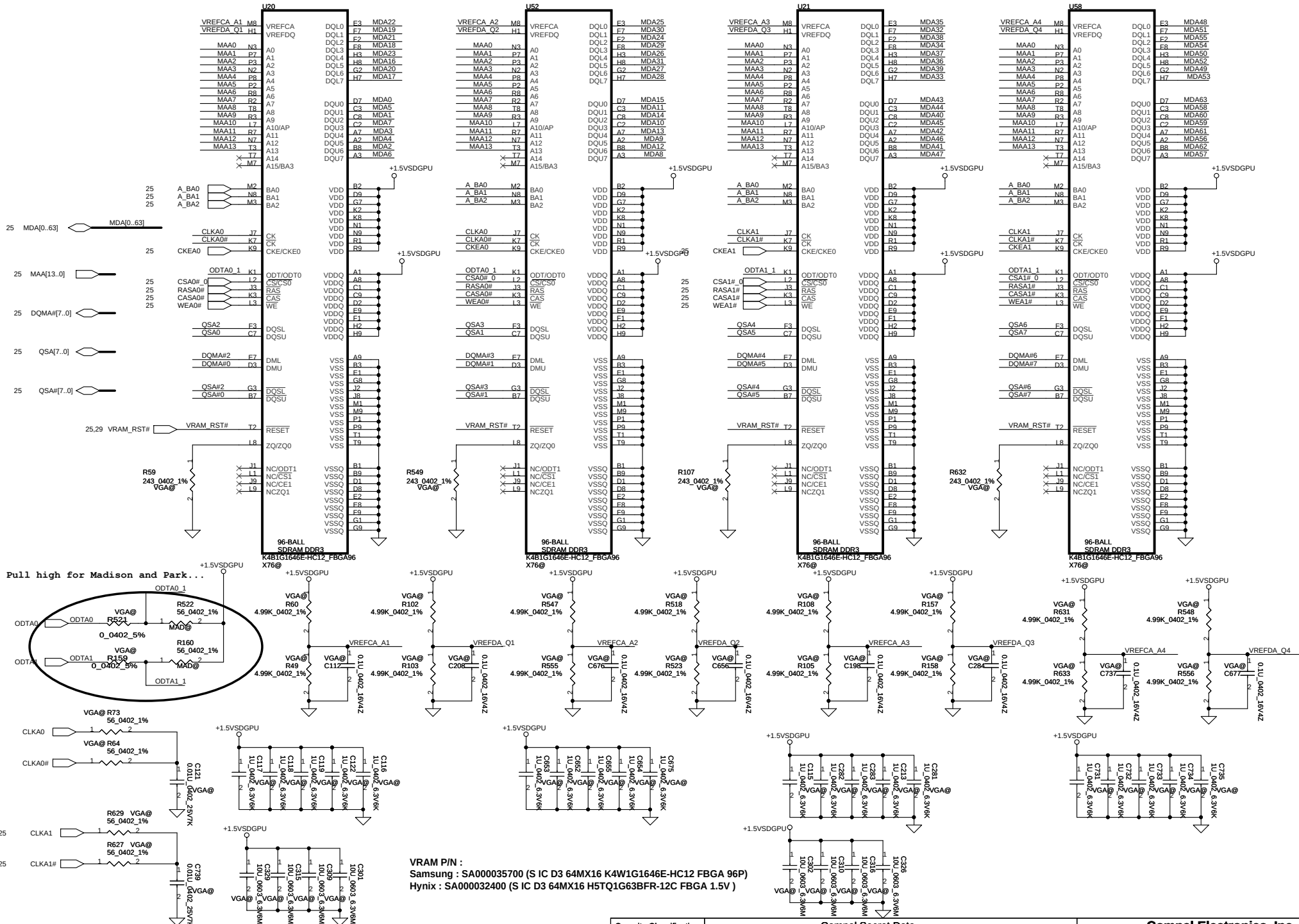

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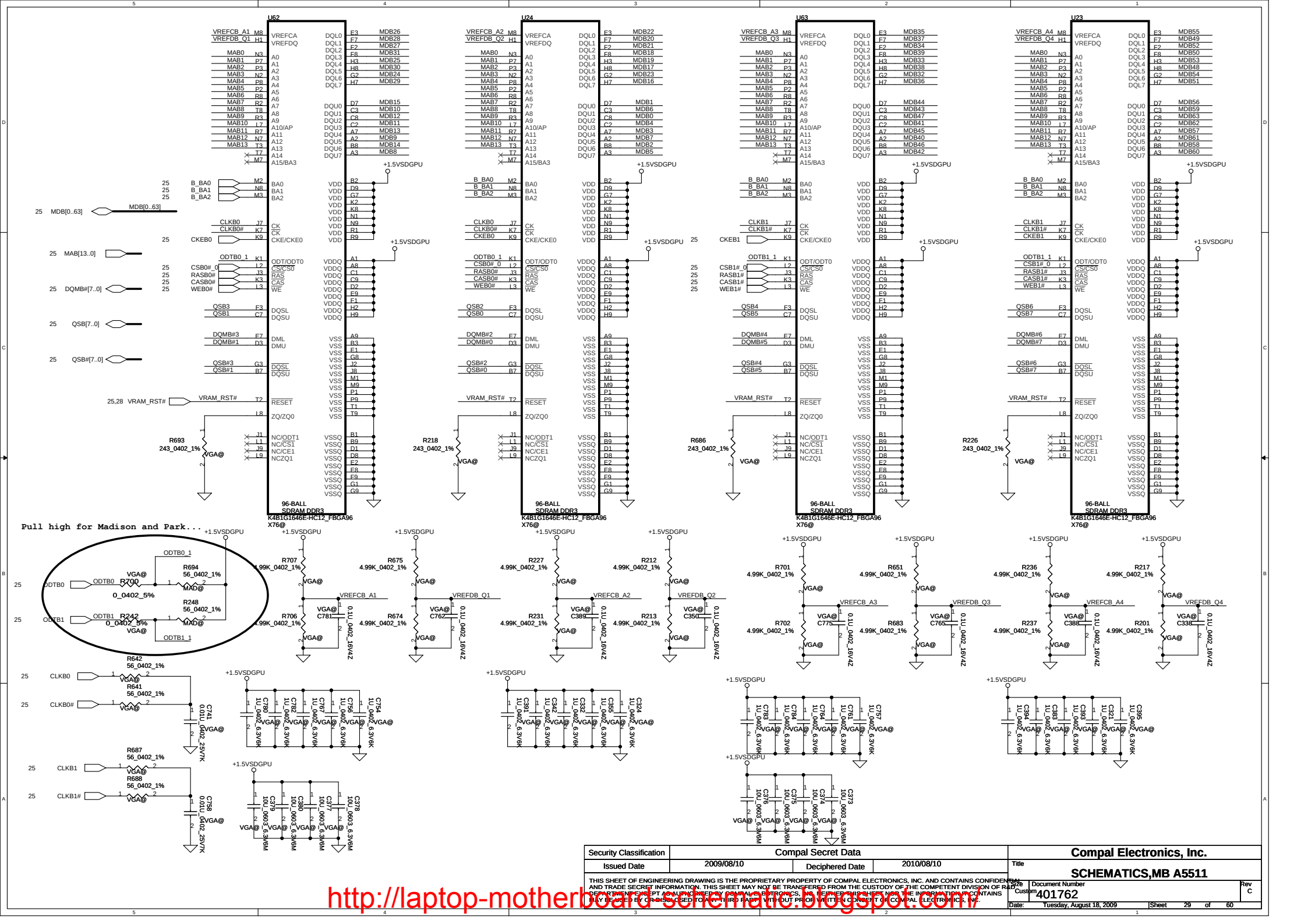

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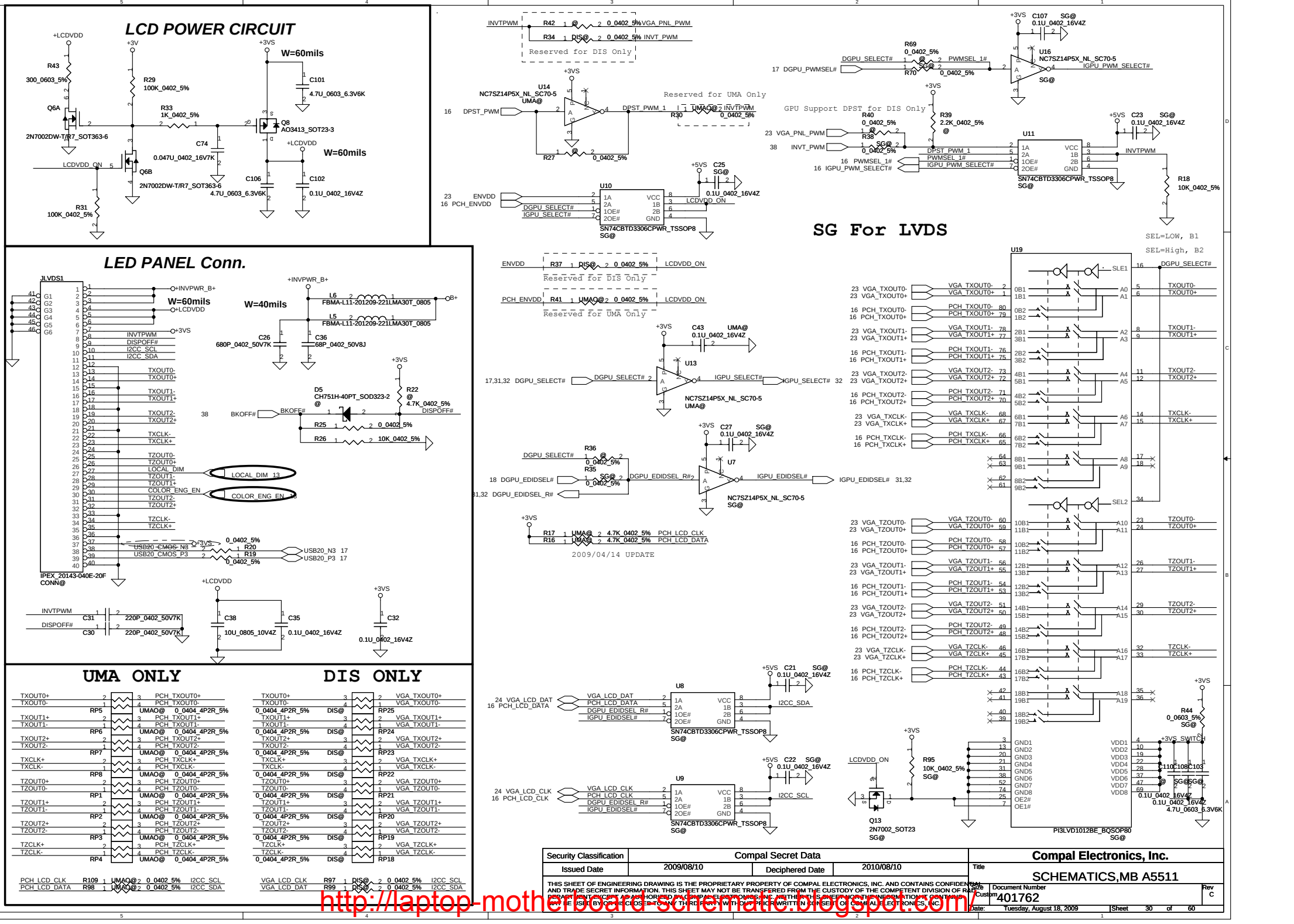
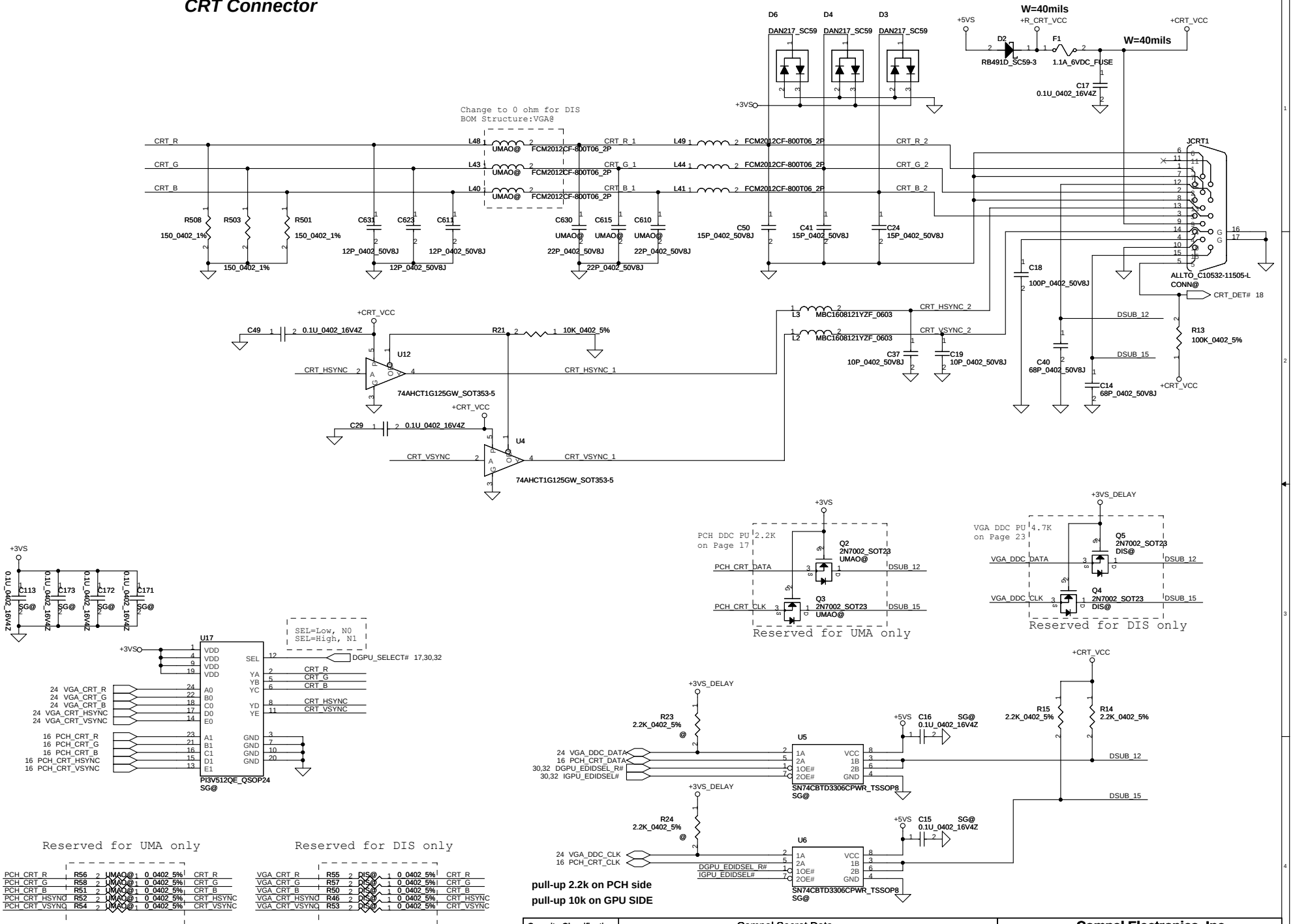


CRT Connector



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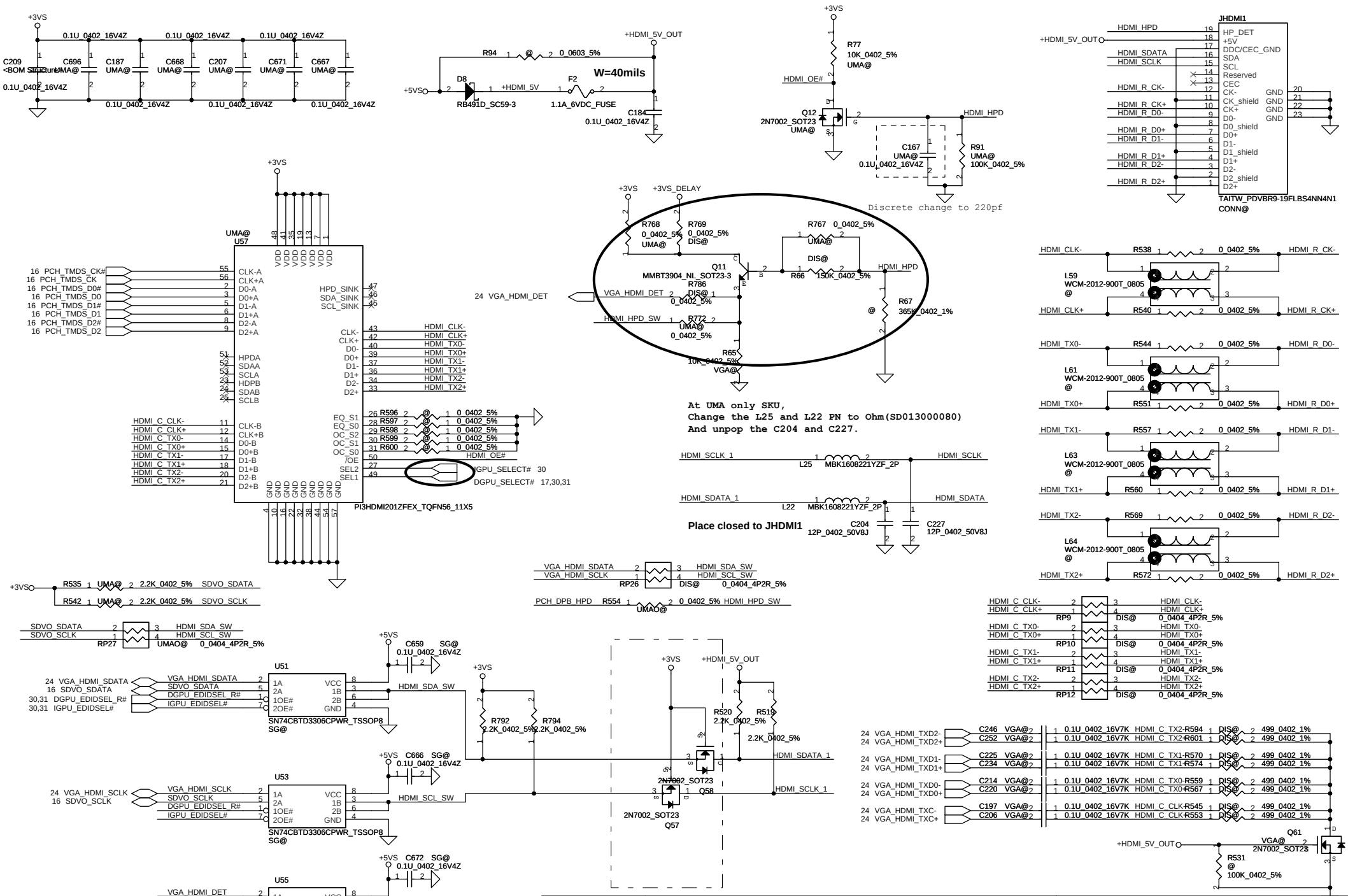

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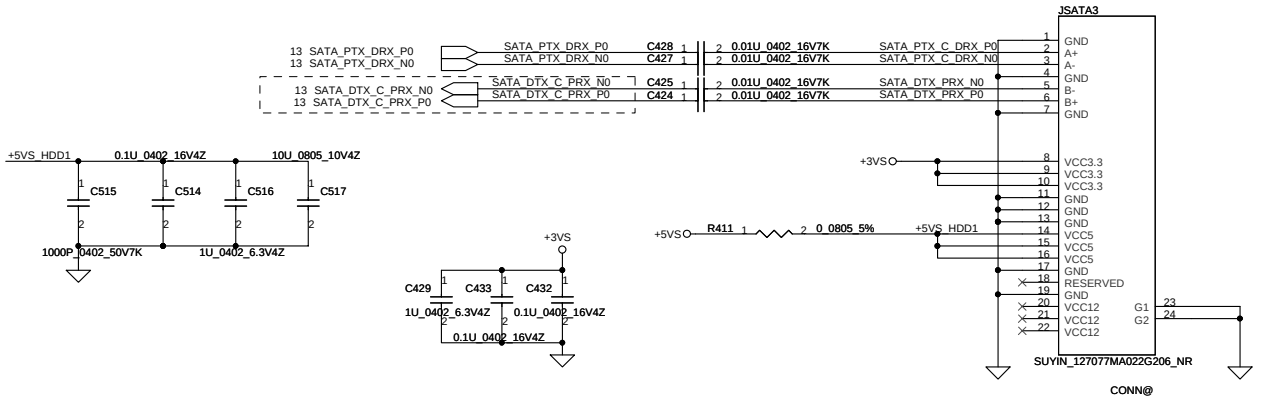
SATA HDD1 Conn.

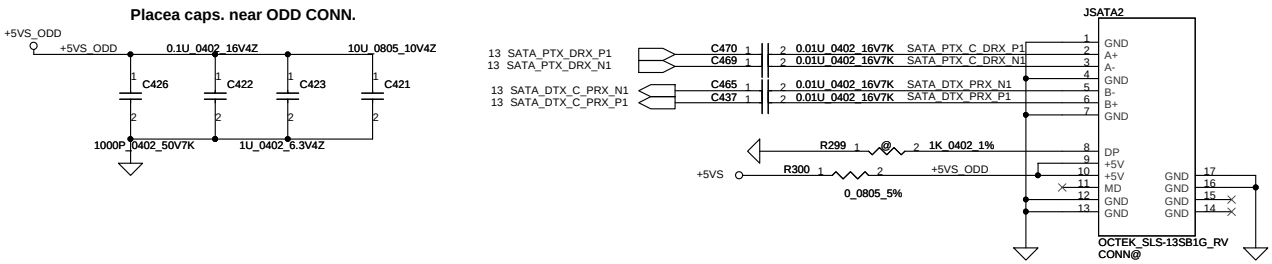
CL 4.0 mm



SATA ODD Conn.

CL 6.0 mm

Placea caps. near ODD CONN.



Card Reader & MINI CARD x2(WLAN & TV)

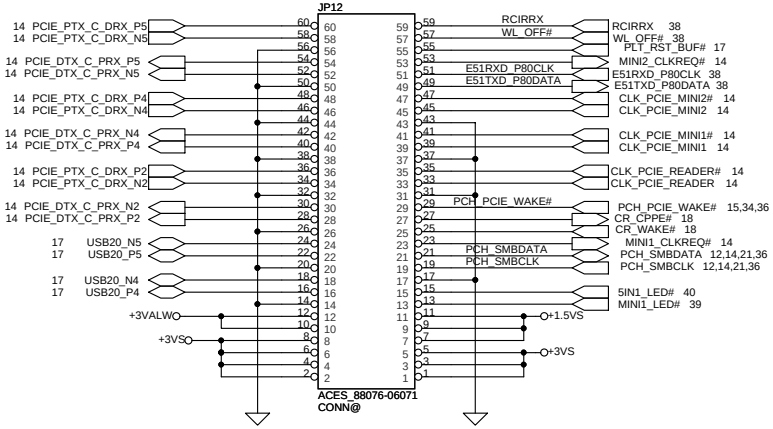
Card Reader

TV

WLAN

TV

WLAN



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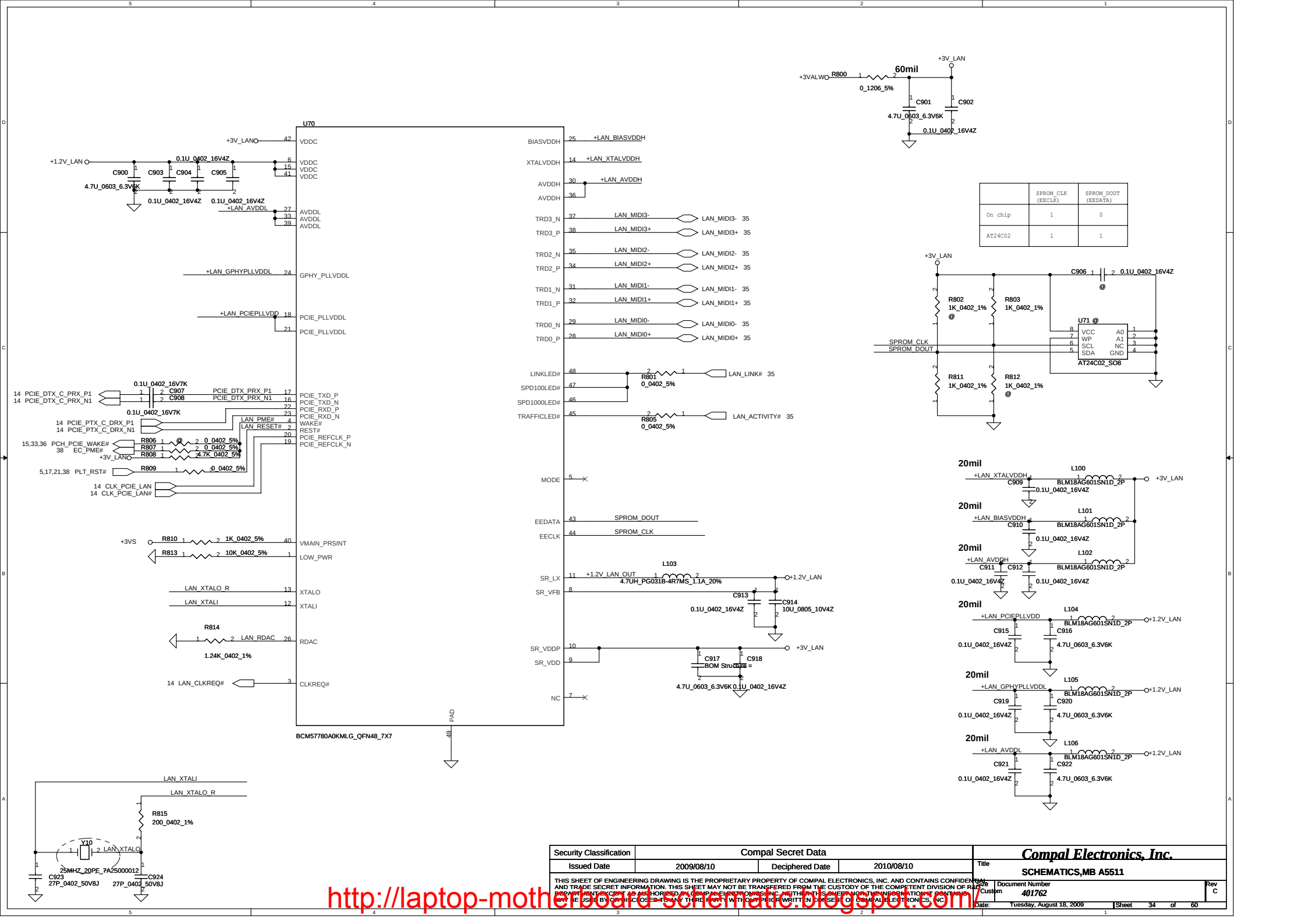

	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

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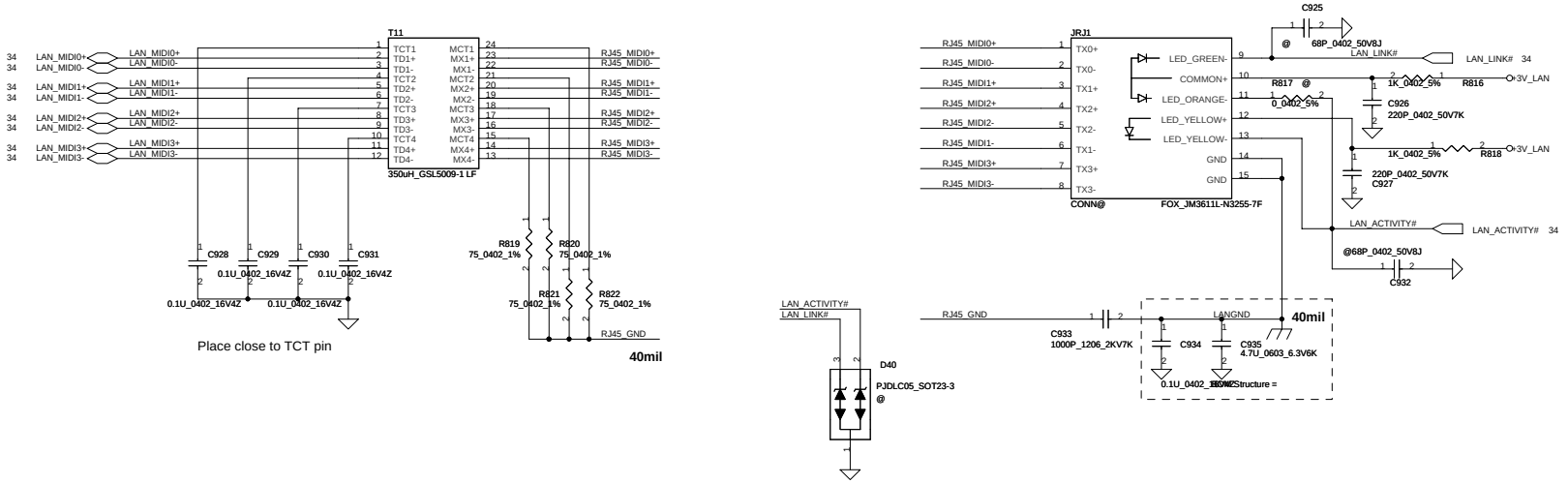
LAN Connector



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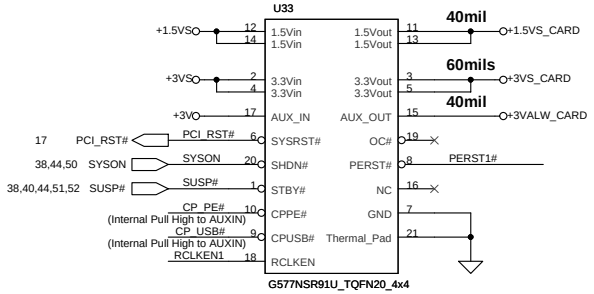
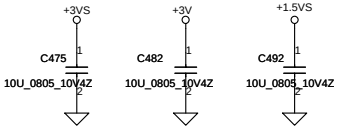
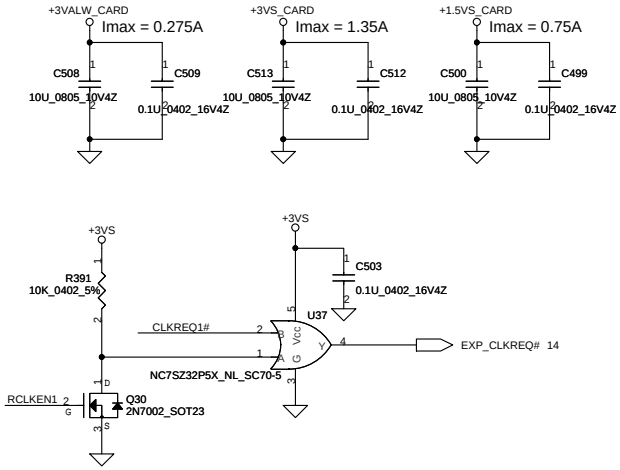
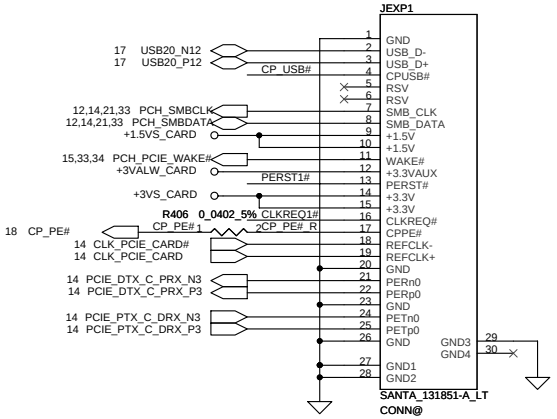
New Card Power Switch



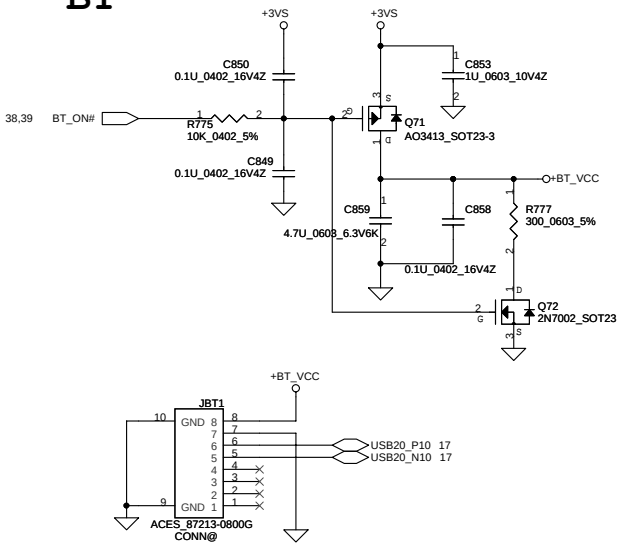




New Card Socket (Left/TOP)

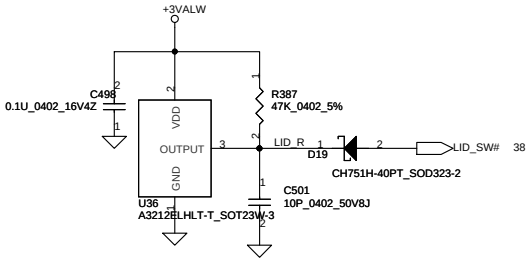


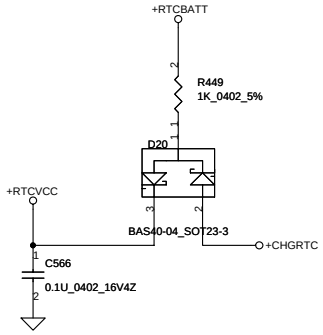
BT



Lid Switch

(Hall Effect Switch)





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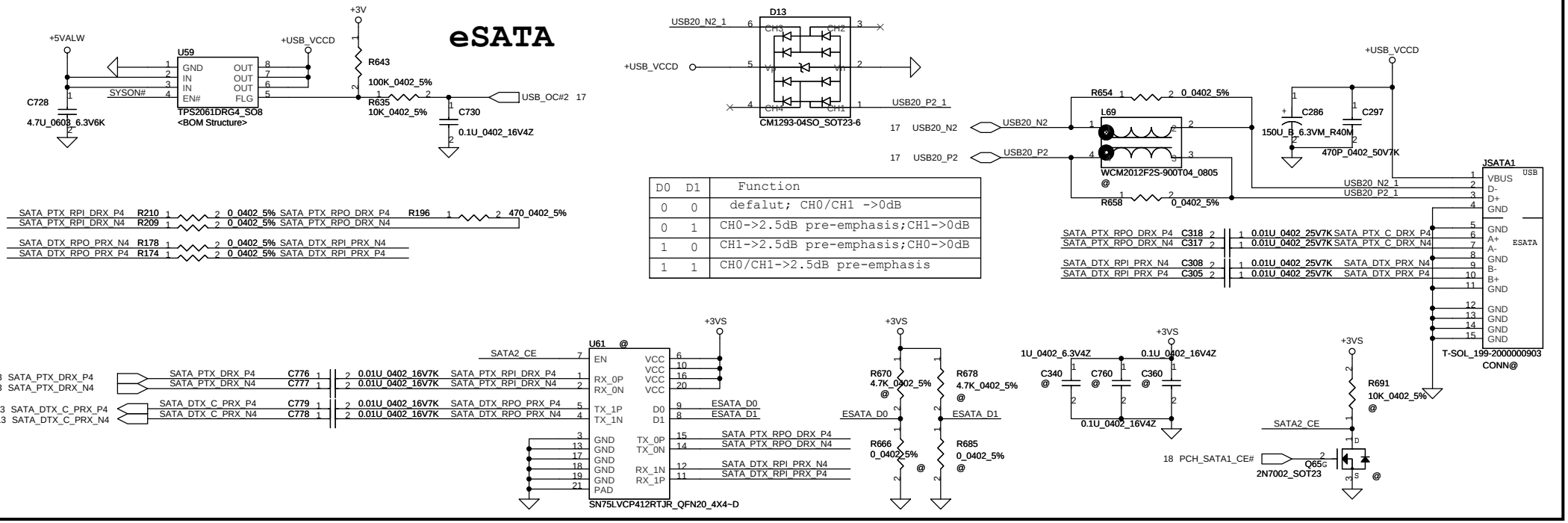
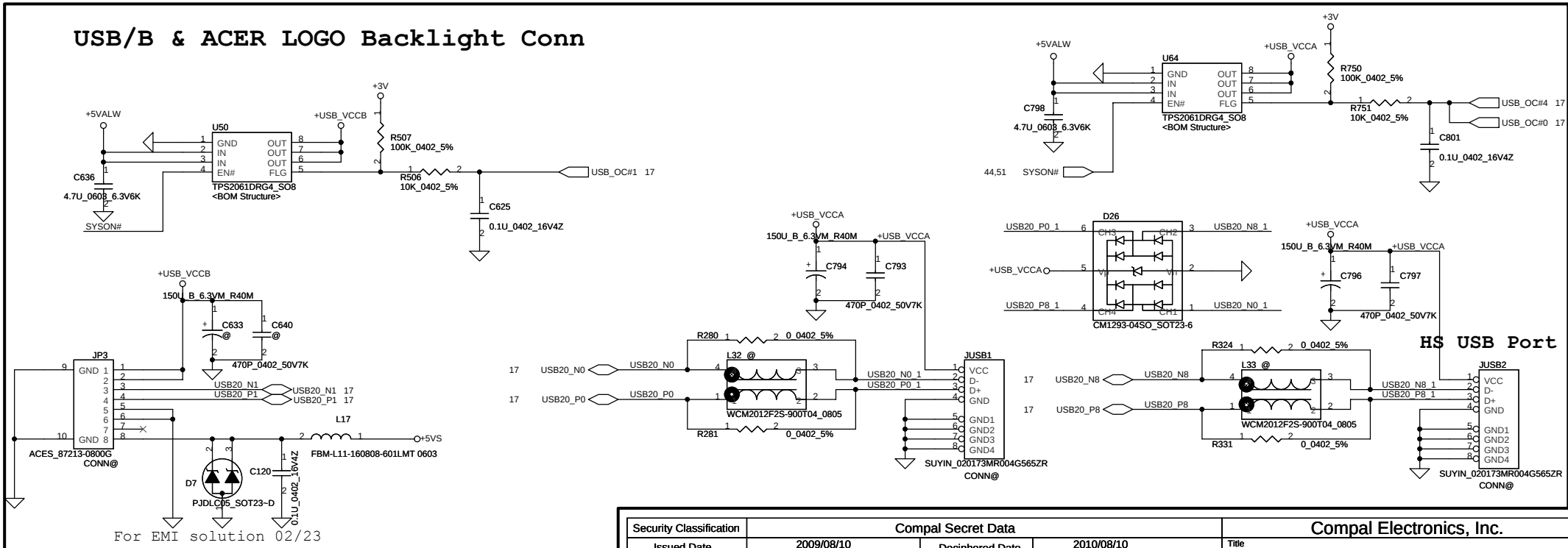
eSATA



D0	D1	Function
0	0	defalut; CH0/CH1 ->0dB
0	1	CH0->2.5dB pre-emphasis;CH1->0dB
1	0	CH1->2.5dB pre-emphasis;CH0->0dB
1	1	CH0/CH1->2.5dB pre-emphasis

USB/B & ACER LOGO Backlight Conn



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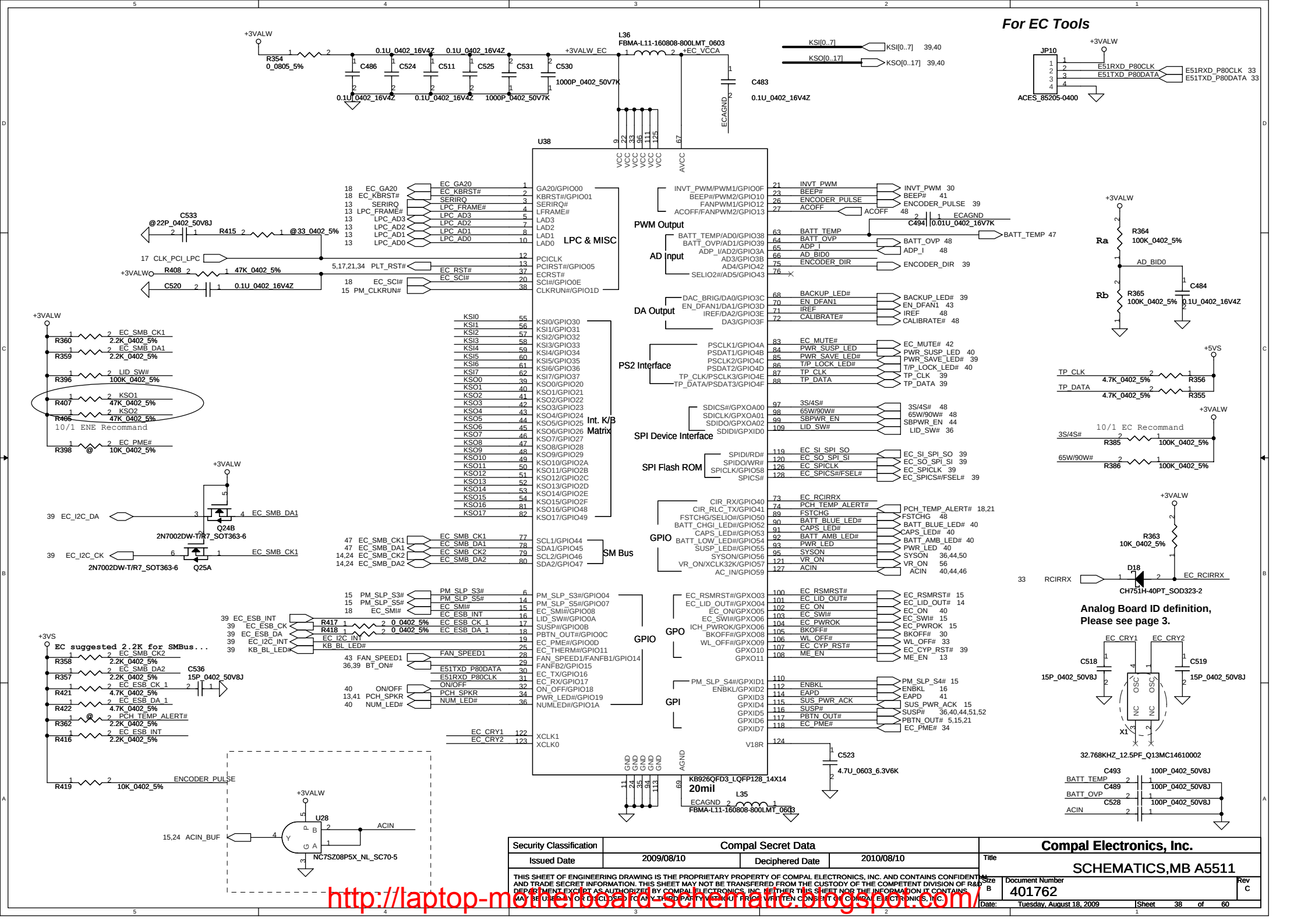

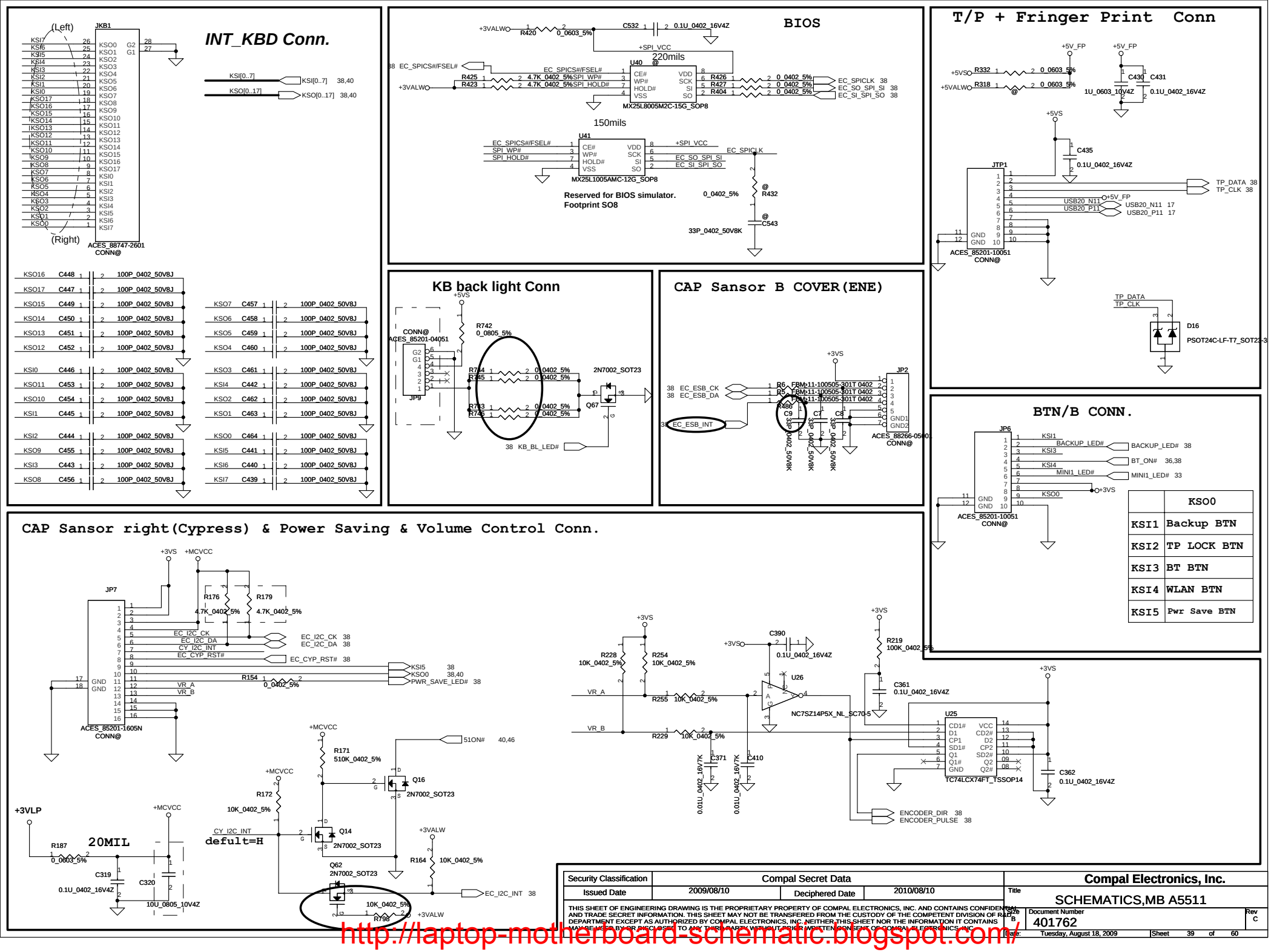

	KSO0
KSI1	Backup BTN
KSI2	TP LOCK BTN
KSI3	BT BTN
KSI4	WLAN BTN
KSI5	Pwr Save BTN

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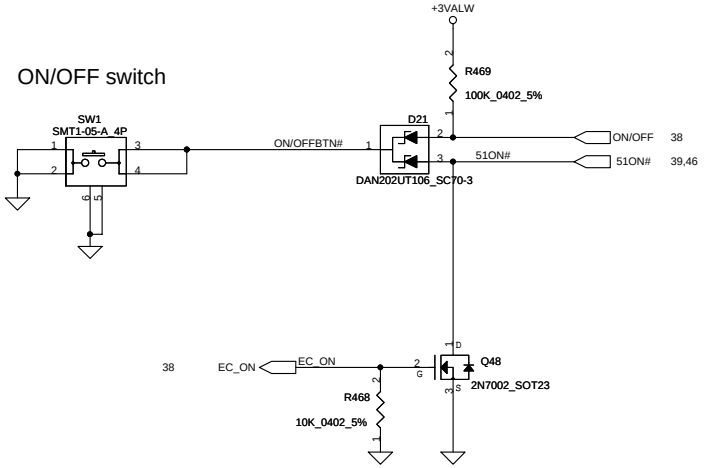
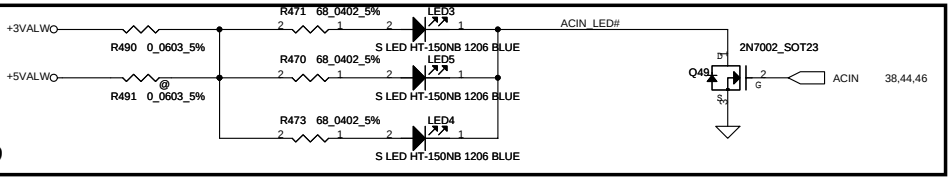
Power Button

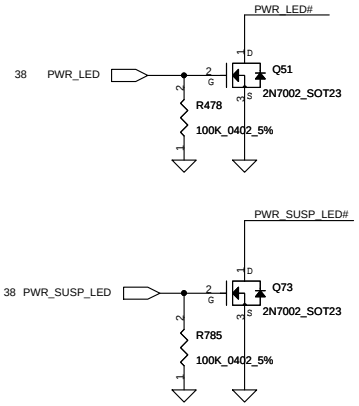
ON/OFF switch

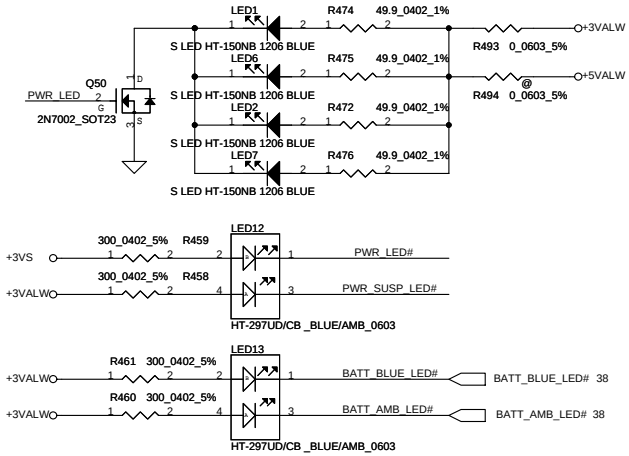


AC_IN LED

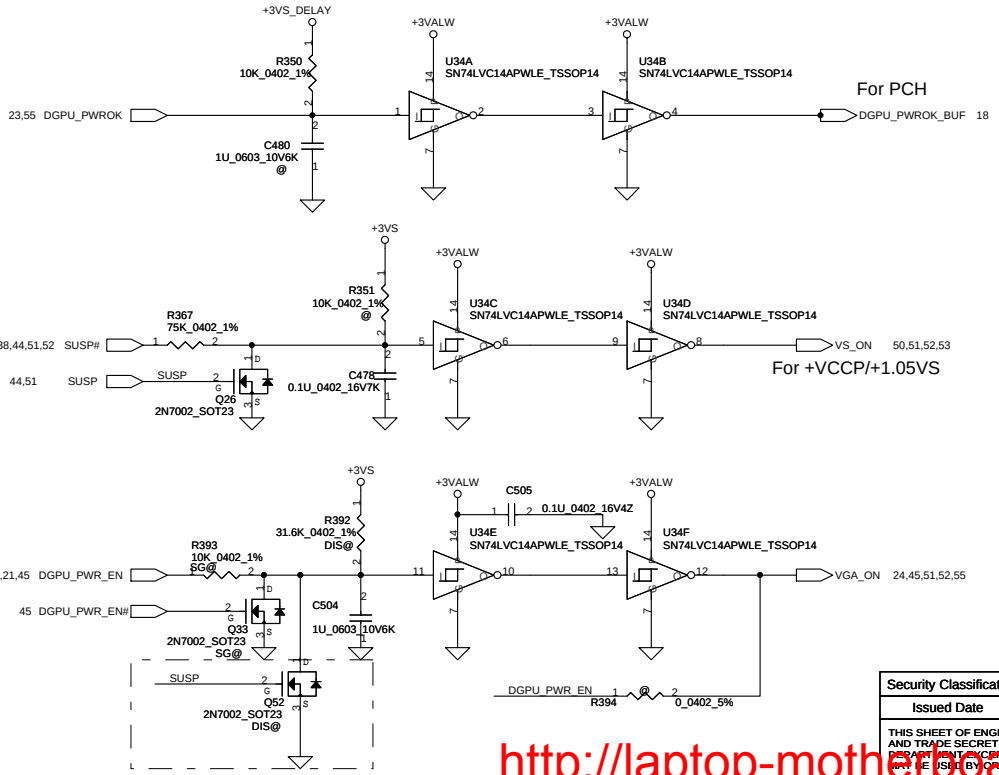


POWER LED

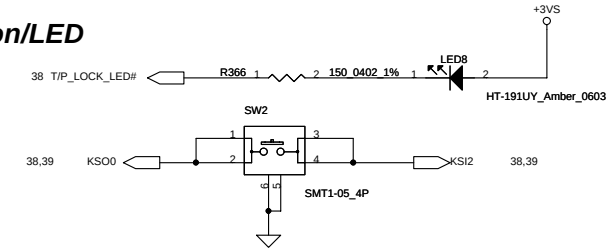




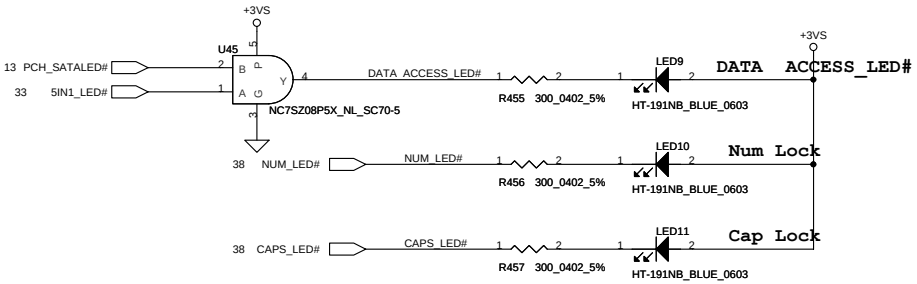
Power ON Circuit



T/P Lock Button/LED



Meadia/Num/Cap LED



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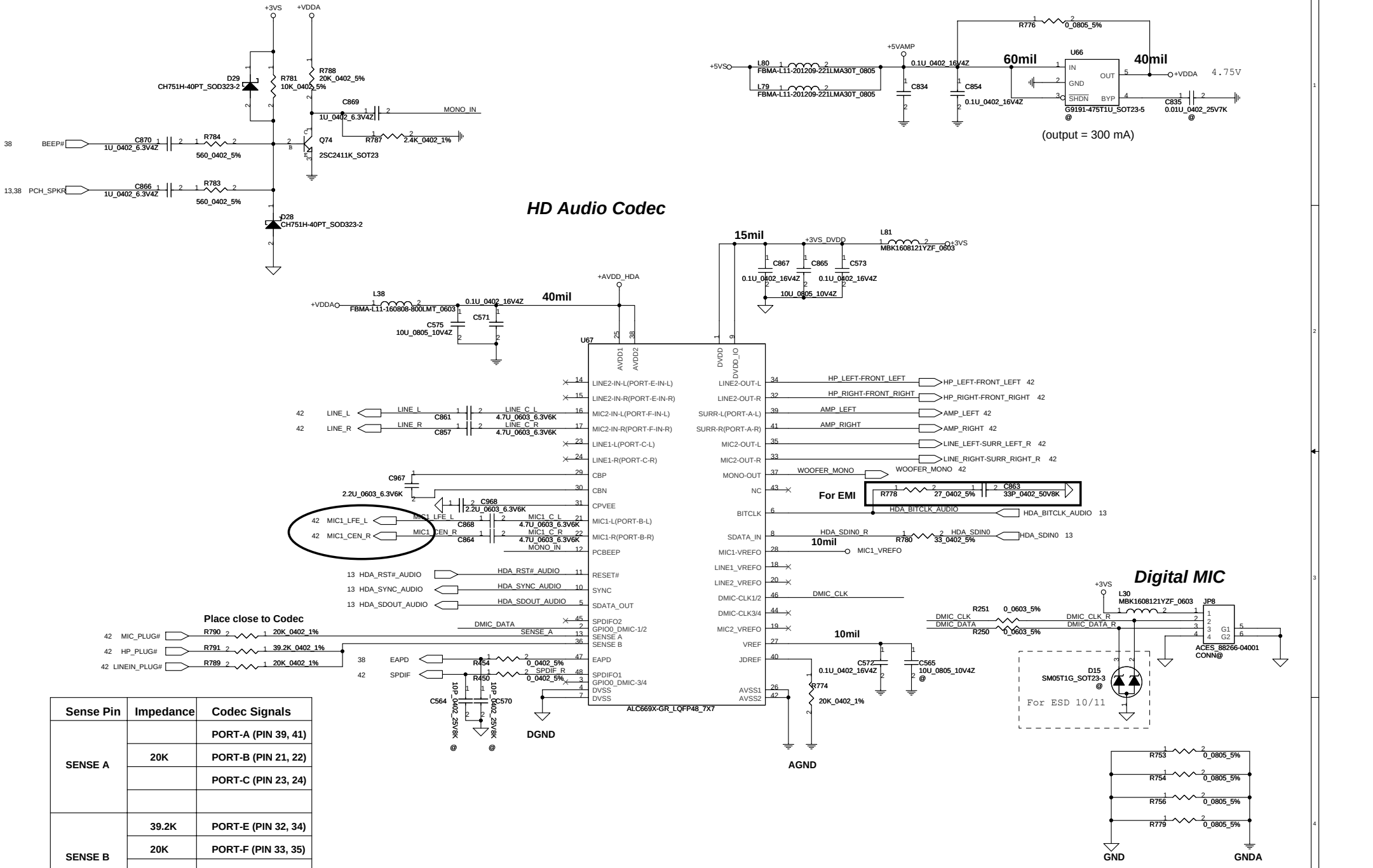

Sense Pin	Impedance	Codec Signals
SENSE A		PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
		PORT-C (PIN 23, 24)
SENSE B	39.2K	PORT-E (PIN 32, 34)
	20K	PORT-F (PIN 33, 35)
		PORT-H (PIN 37)

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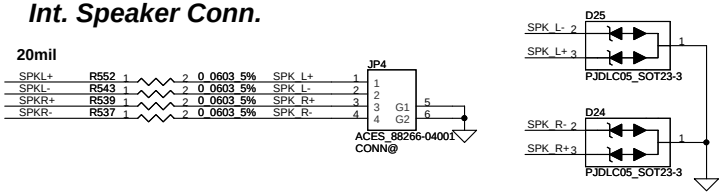
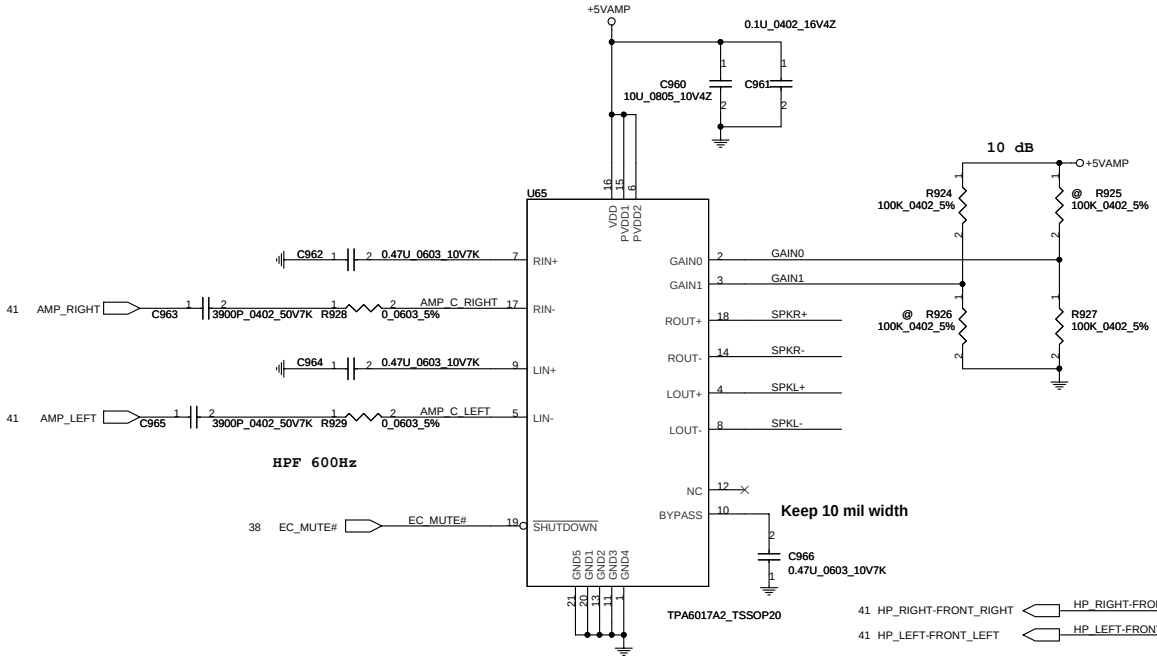
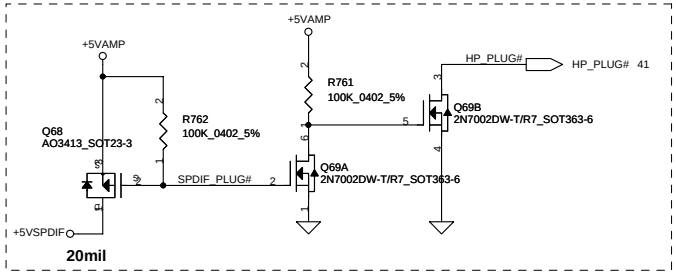
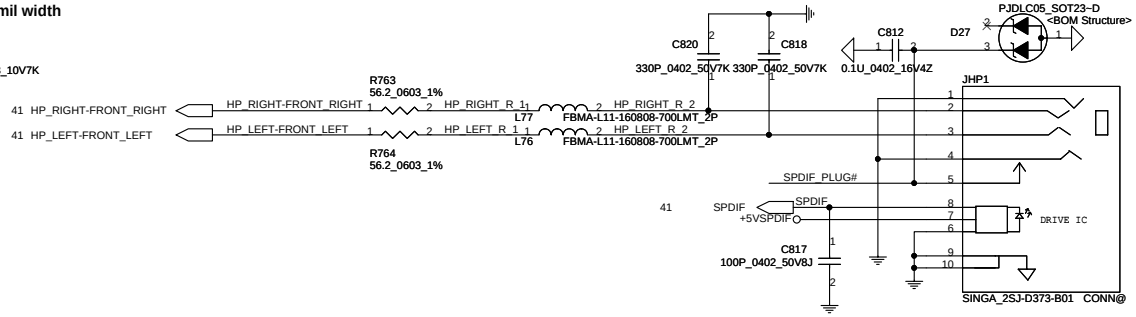
Int. Speaker Conn.



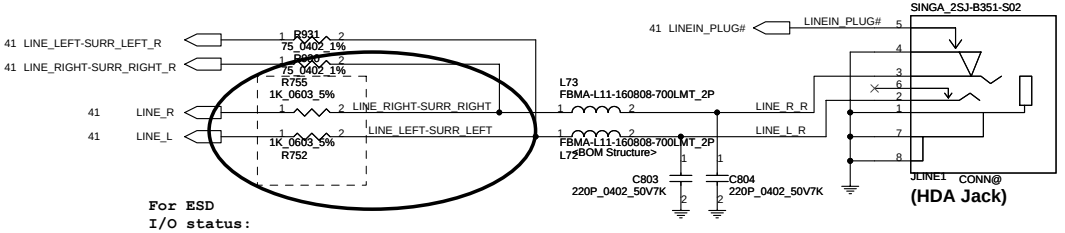


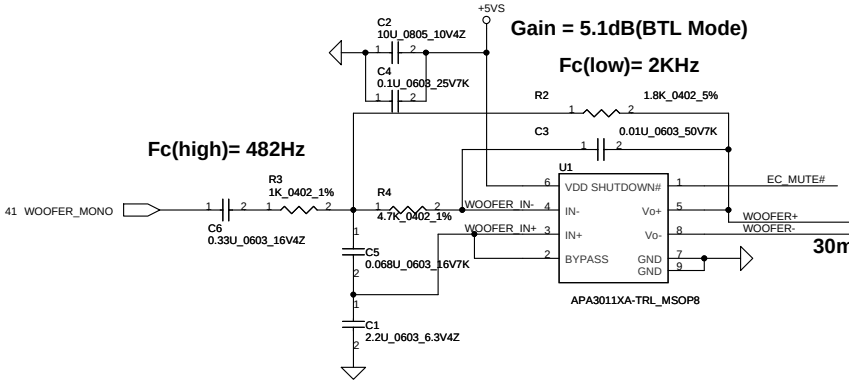


S/PDIF Out JACK
LINE Out/Headphone Out



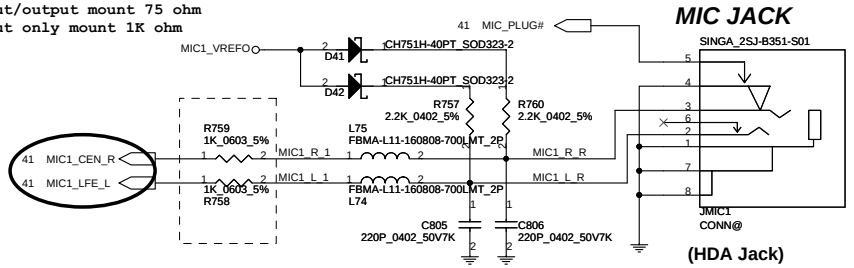
LINE-IN JACK





For ESD
I/O status:
a. input/output mount 75 ohm
b. input only mount 1K ohm

MIC JACK



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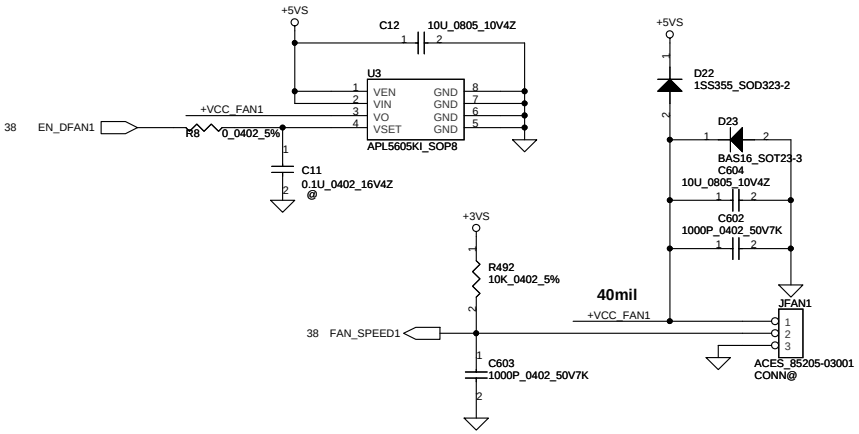
FAN1 Conn



H19 H_3P0 · H7 H_3P0 · H1 H_3P0 · H8 H_3P0 · H24 H_3P0 · H23 H_3P0 · H15 H_3P0 · H18 H_3P0 · H25 H_3P0

H22 H_3P7 · H21 H_3P7

H10 H_6P6 · H5 H_2P8 · H9 H_2P6N

H26 H_3P1X2P6N · H20 H_3P1X2P6N

H4 H_3P2 · H3 H_3P2 · H2 H_3P2

H12 H_4P2 · H13 H_4P2 · H17 H_4P2 · H16 H_4P2

H11 H_4P0 · H14 H_4P0 · H6 H_4P0

FD3 FIDUCIAL_C40M80 · FD1 FIDUCIAL_C40M80 · FD4 FIDUCIAL_C40M80 · FD2 FIDUCIAL_C40M80

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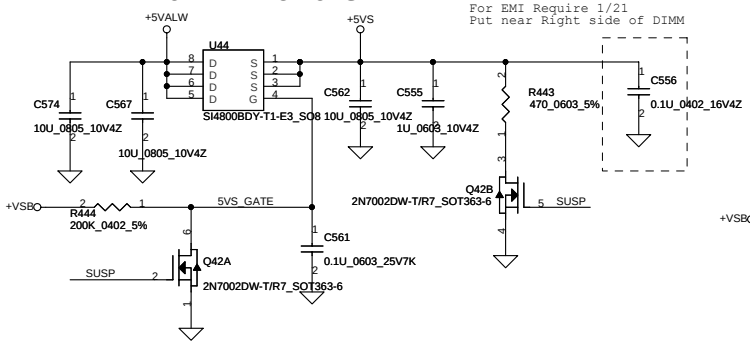
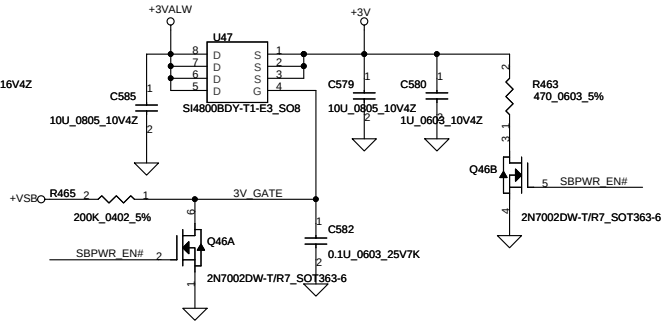
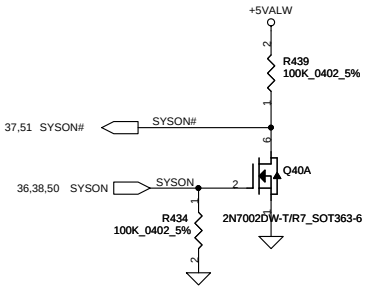
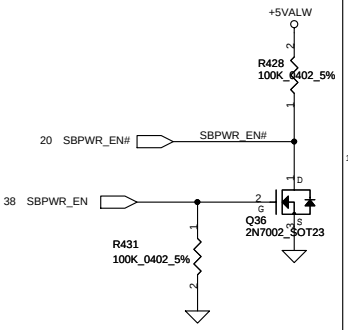
+5VALW TO +5VS



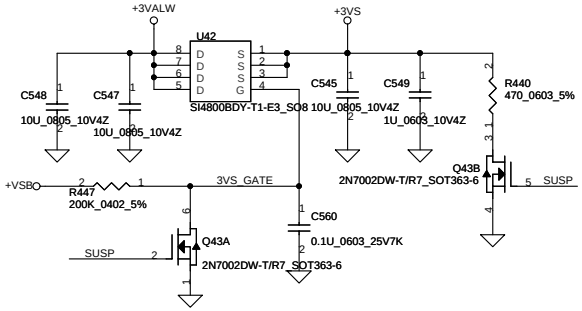
+3VALW TO +3V(PCH AUX Power)

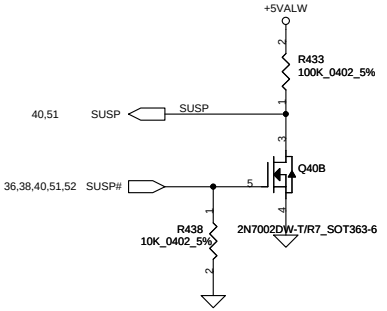






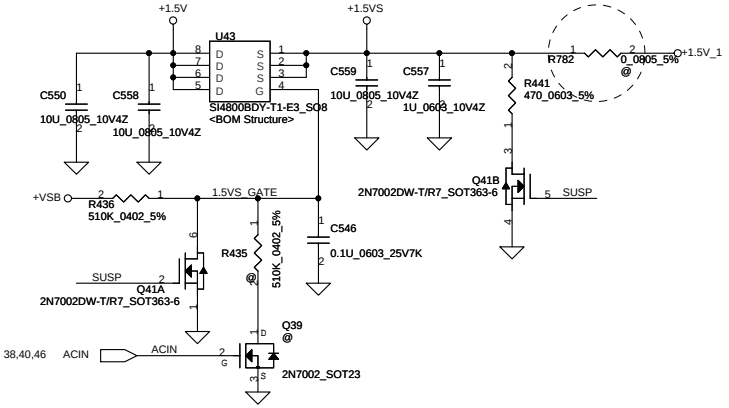
+3VALW TO +3VS

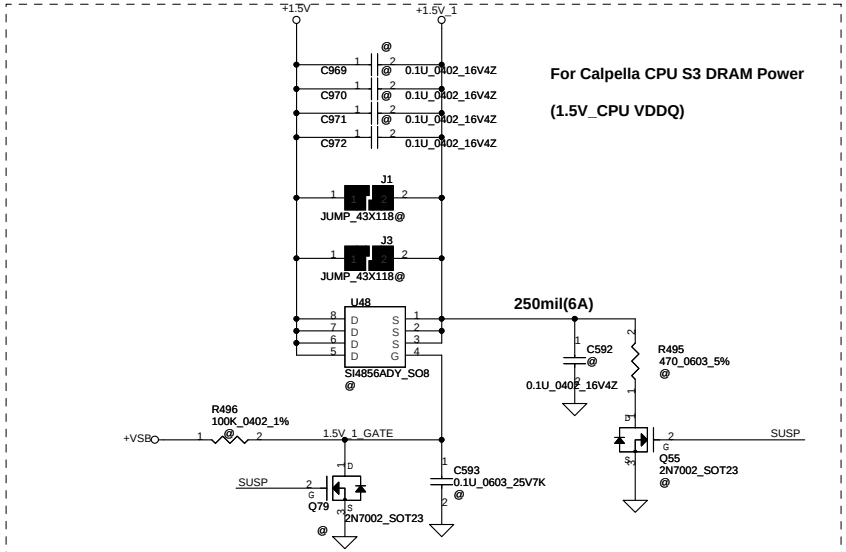


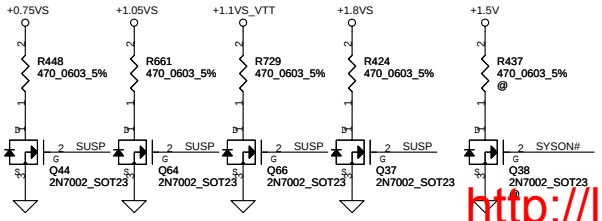


+1.5V to +1.5VS

Optional, if +1.5VS can combine with +1.5V_1







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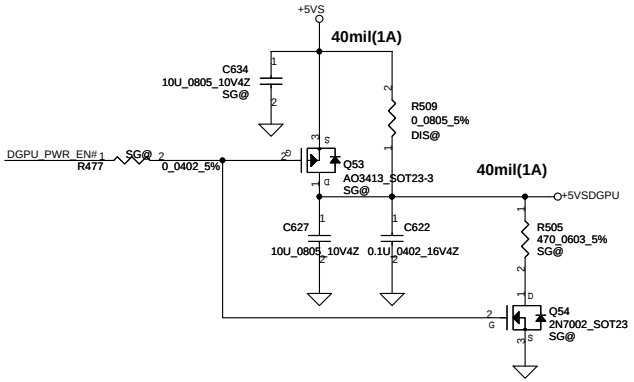
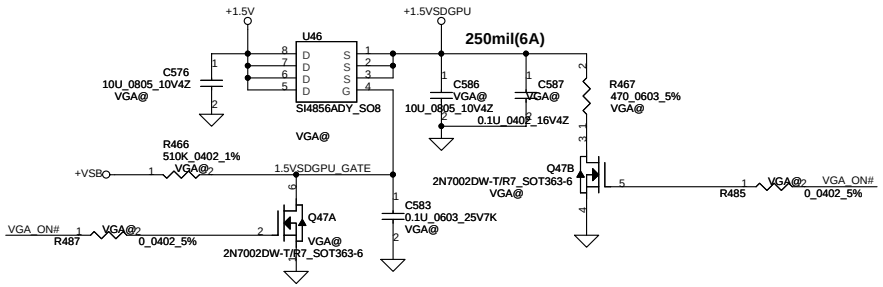
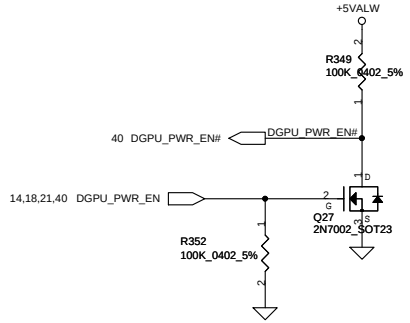
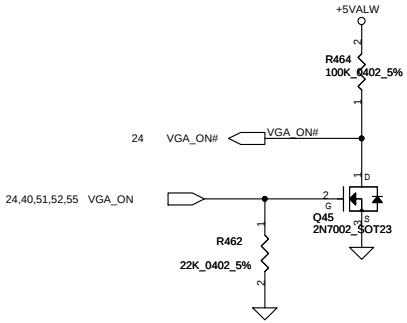
+5VS to +5VSDGPU



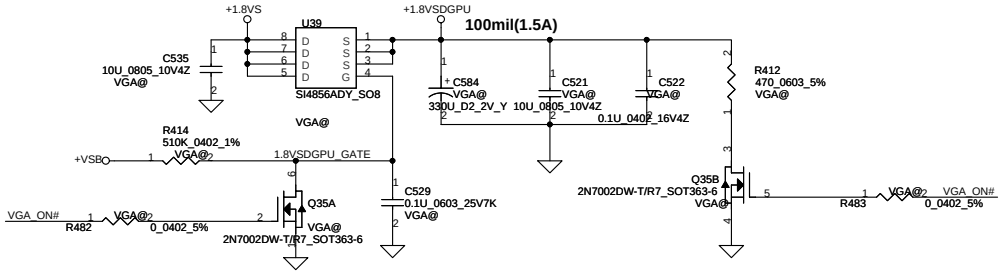
+1.5V to +1.5VSDGPU Transfer







+1.8VS to +1.8VSDGPU Transfer



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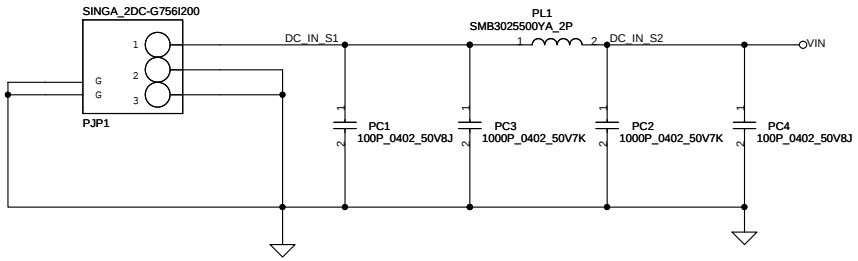
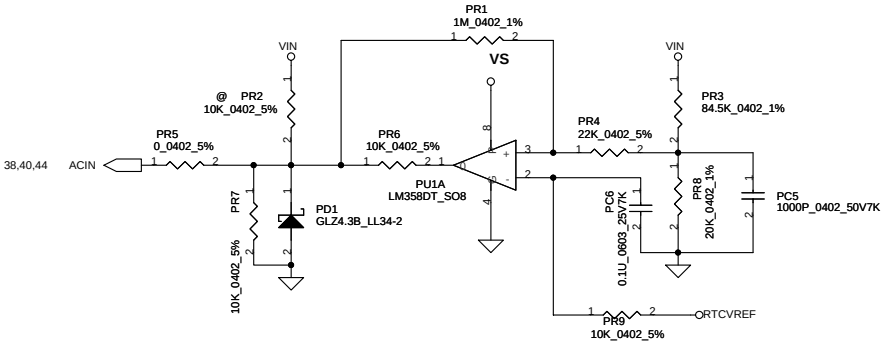
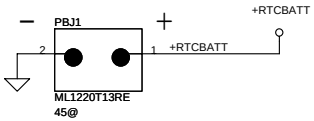
DC231000N00 藍色 For DIS
DC231000P00 黃色 For UMA
Footpront
SINGA_2DC-S756B200_3P

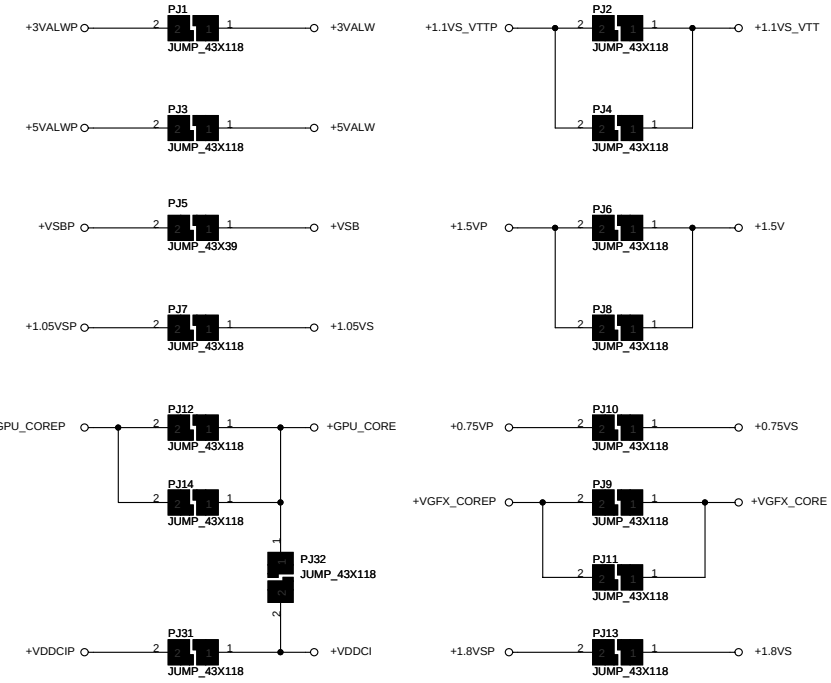


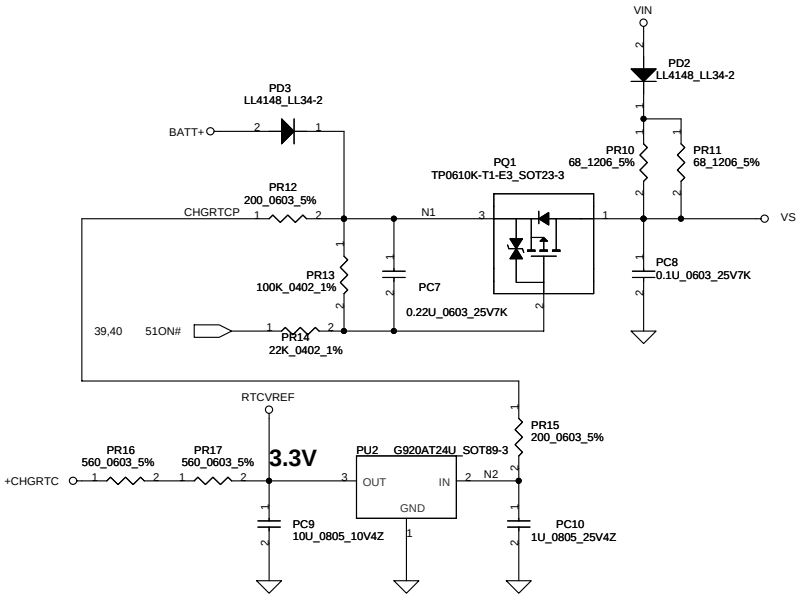




Vin Detector

	Min.	Typ	Max.
H-->L	17.208V	17.212V	17.217V
L-->H	17.879V	17.894V	17.909V





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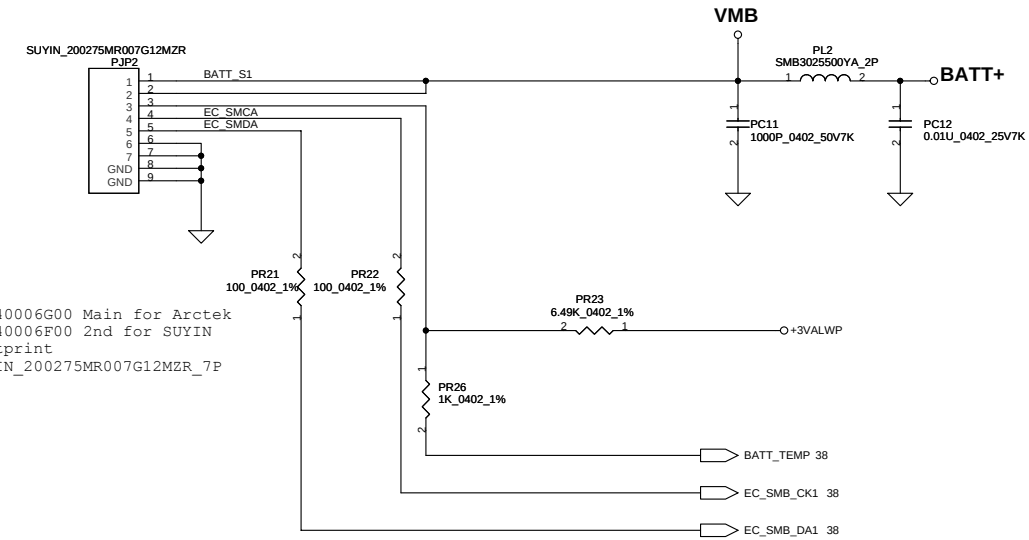
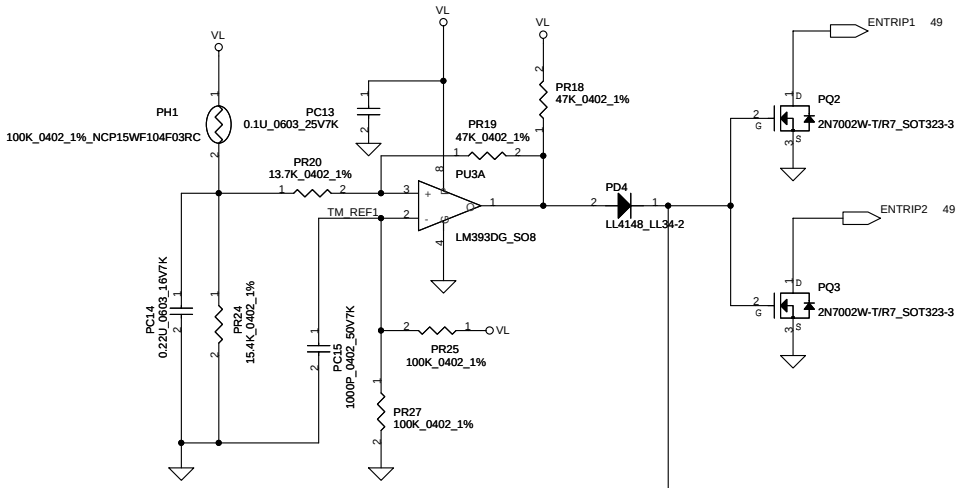
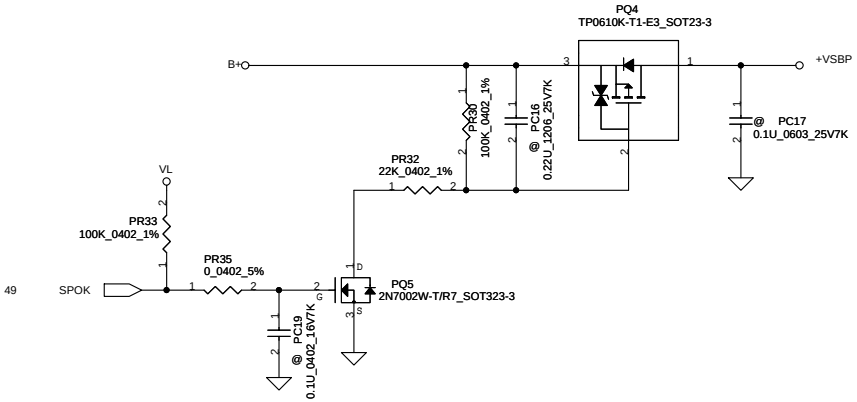
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C

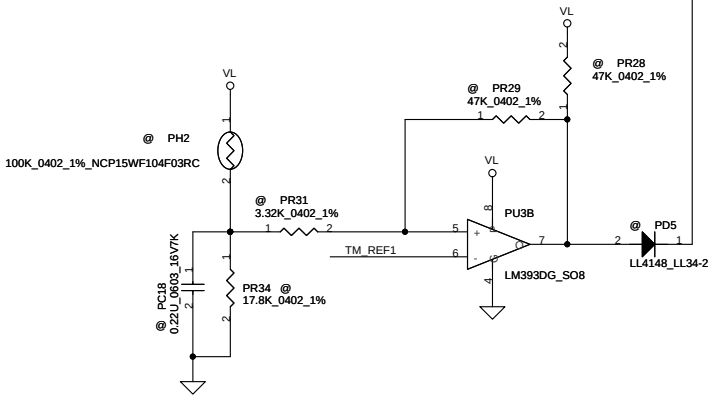


DC040006G00 Main for Arctek
DC040006F00 2nd for SUYIN
Footprint
SUYIN_200275MR007G12MZR_7P



PH2 near main Battery CONN :
BAT. thermal protection at 76 degree C
Recovery at 56 degree C





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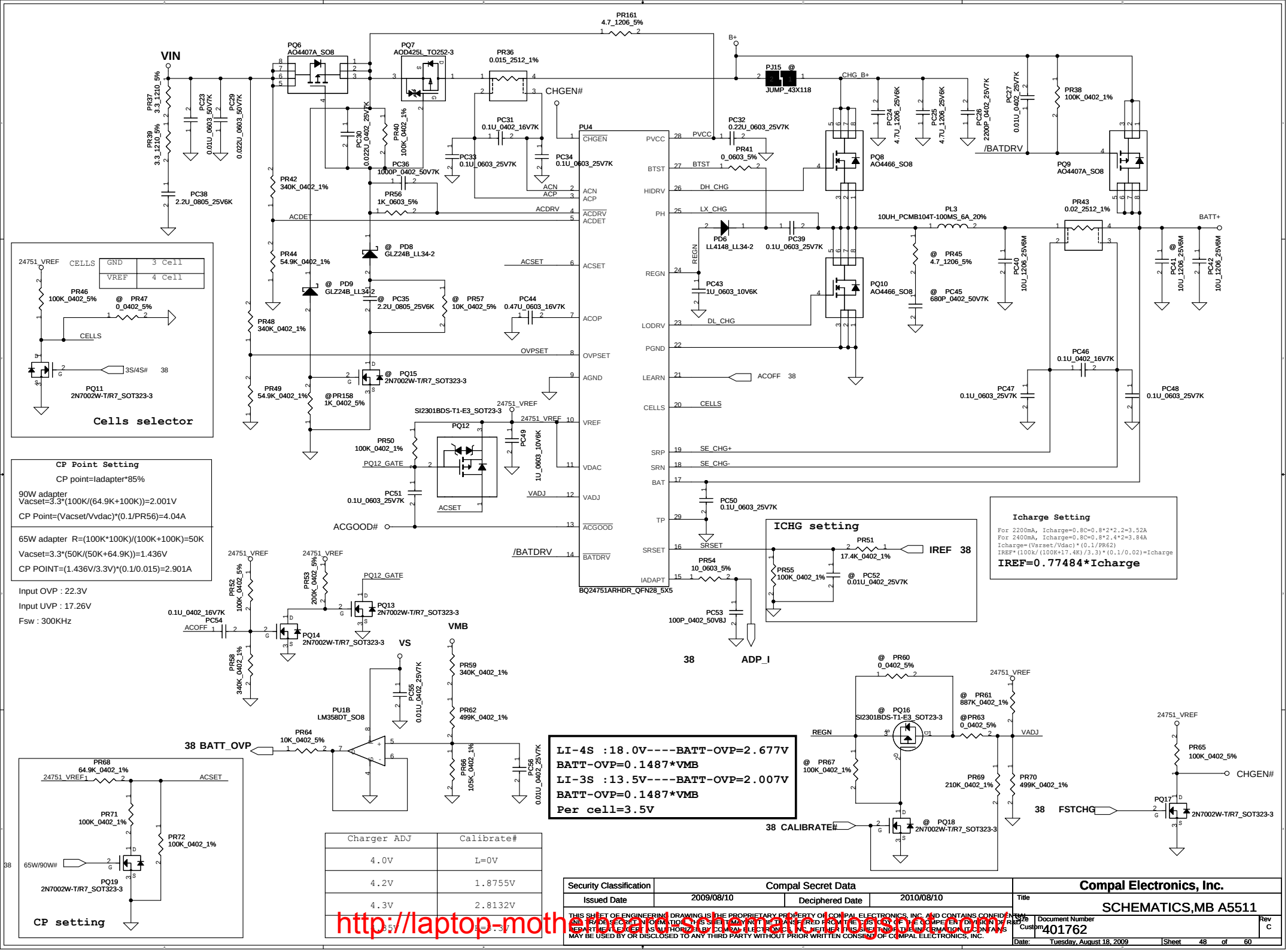

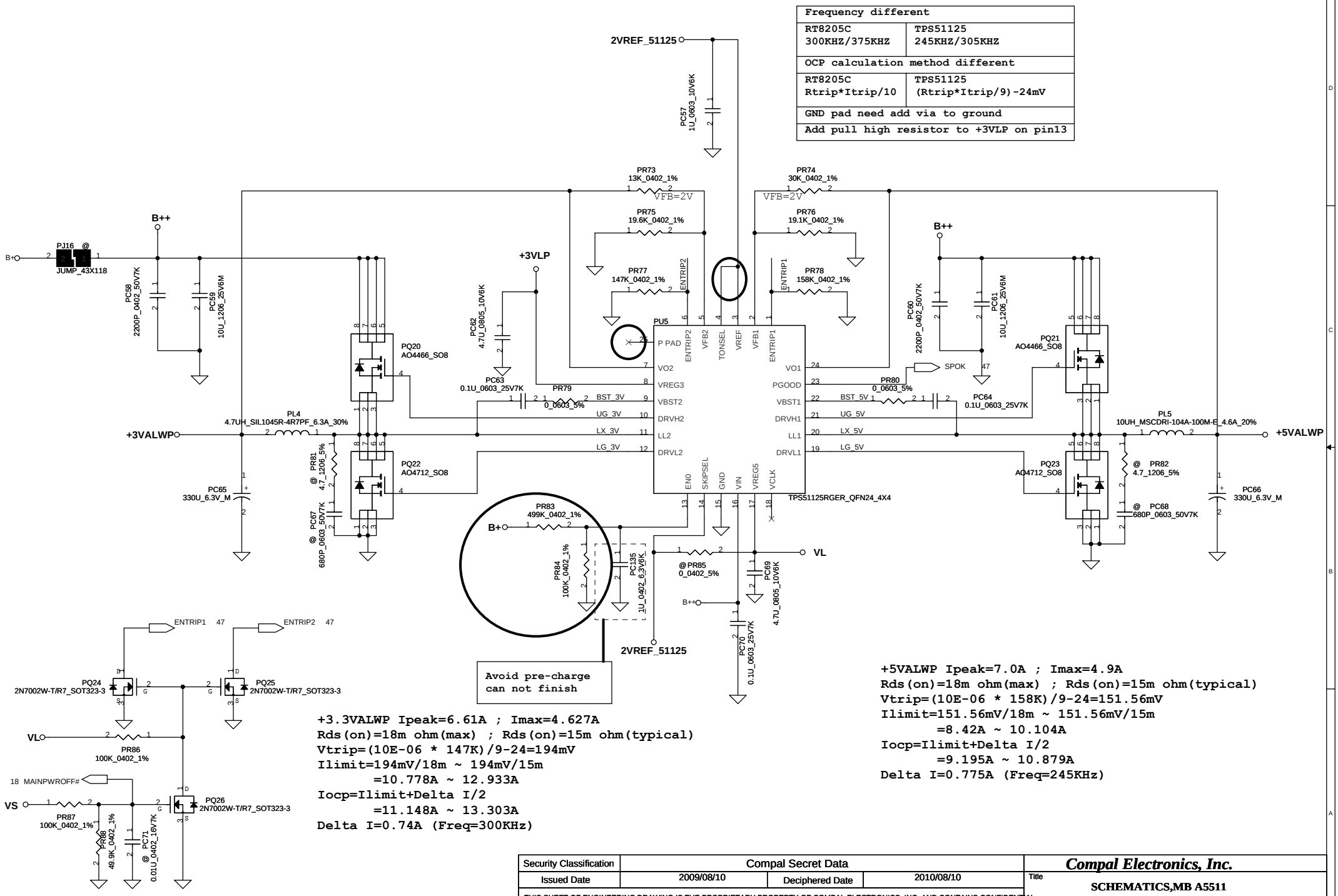

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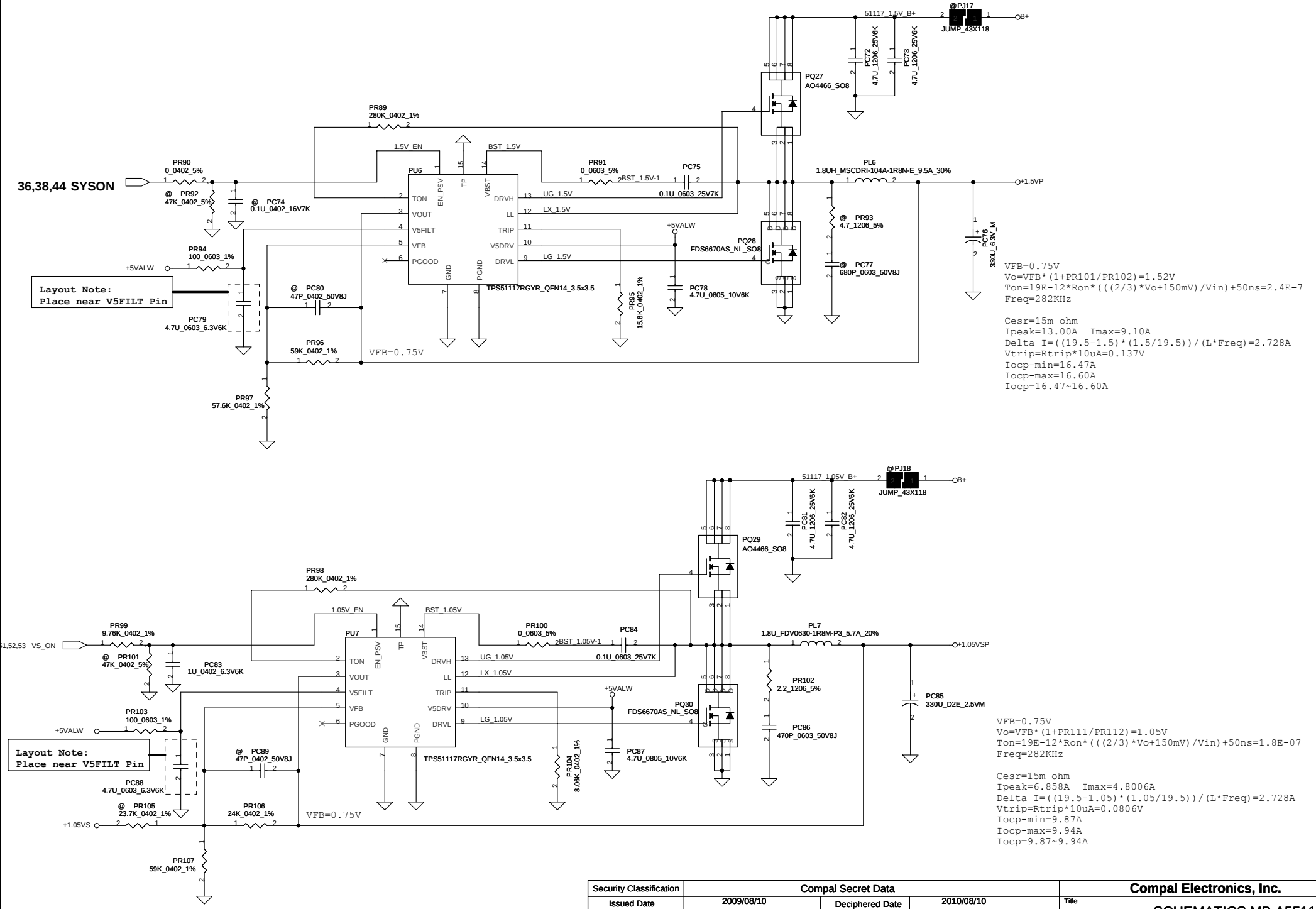

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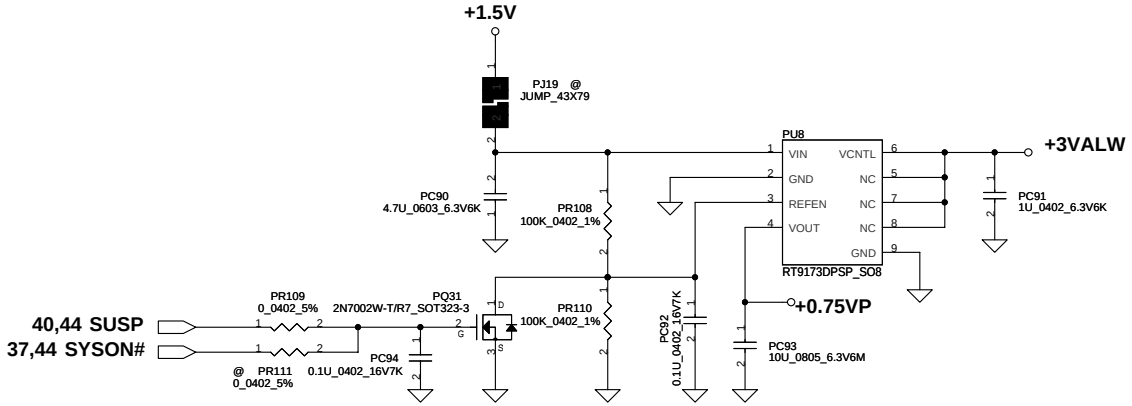
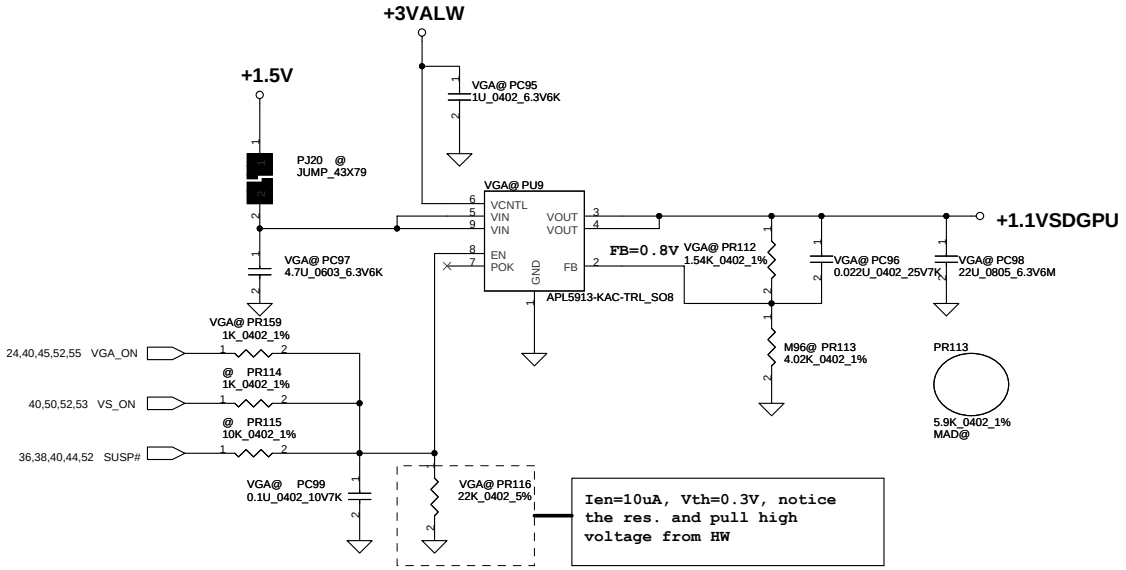


For AMD NEW VGA (Braidway)
Output= 1.0V (PR113= 5.9K SD034590180)



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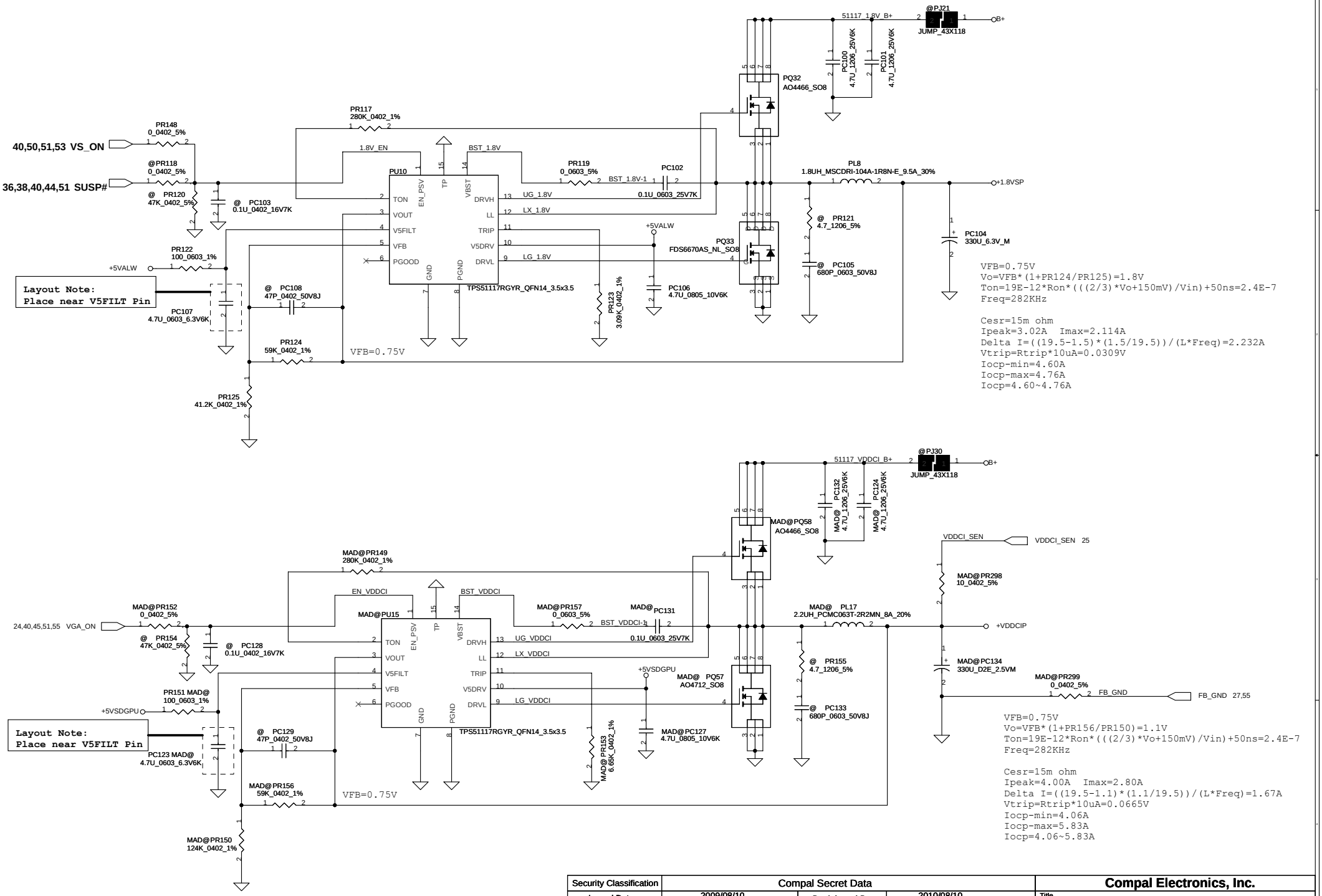

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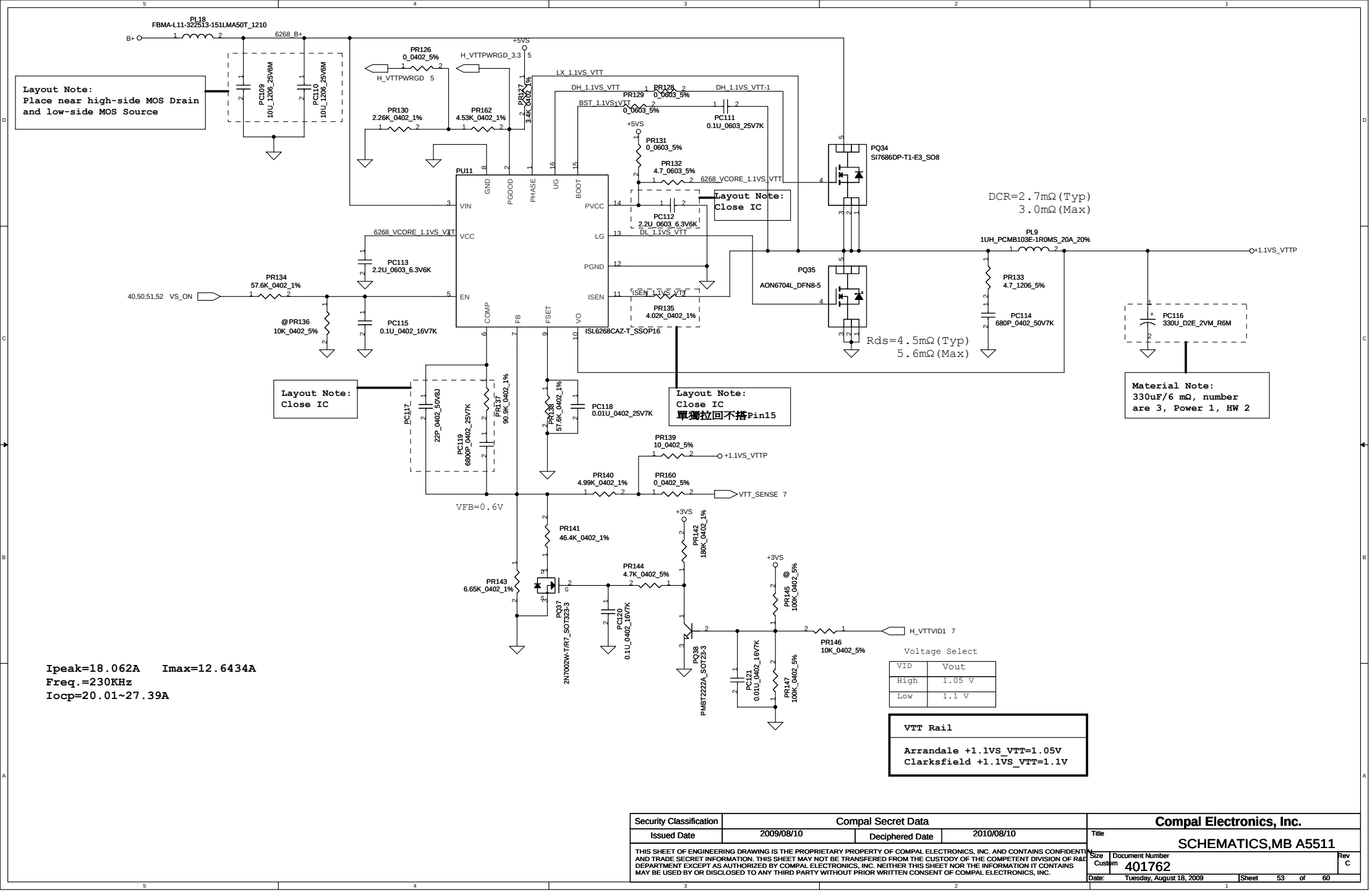

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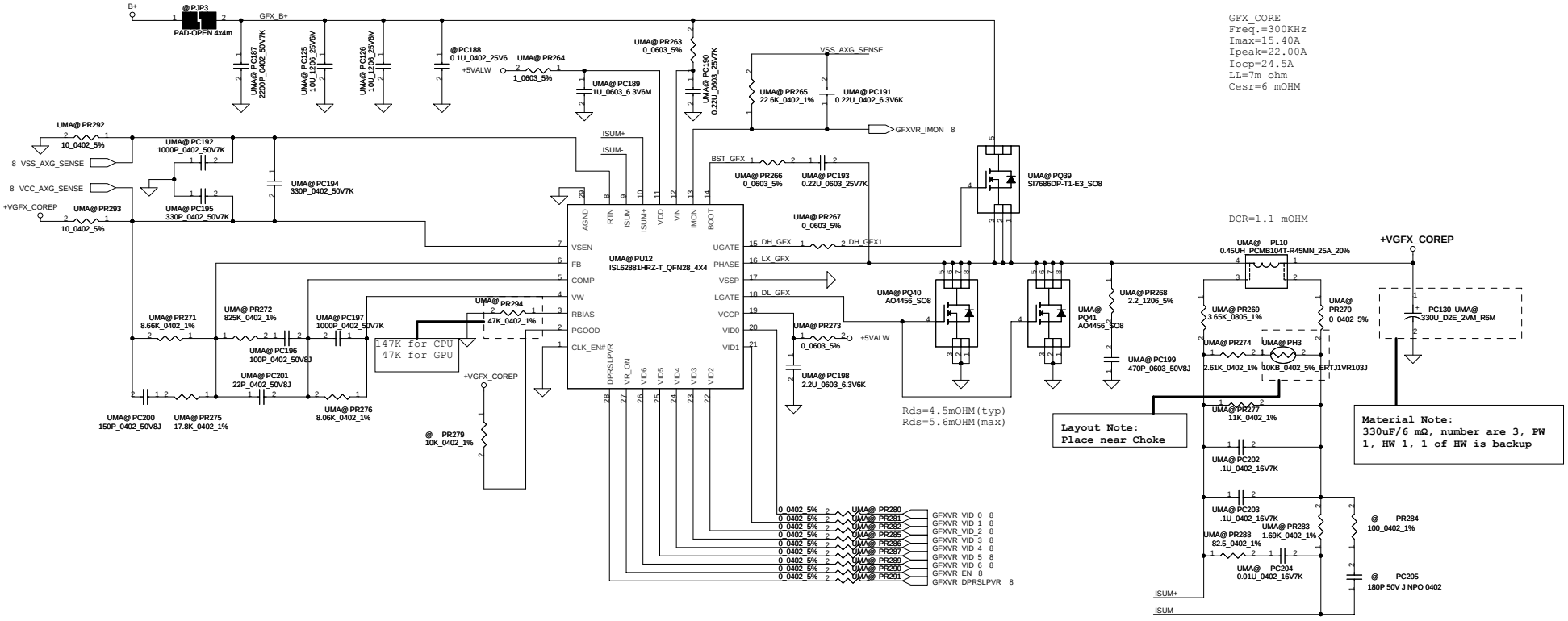

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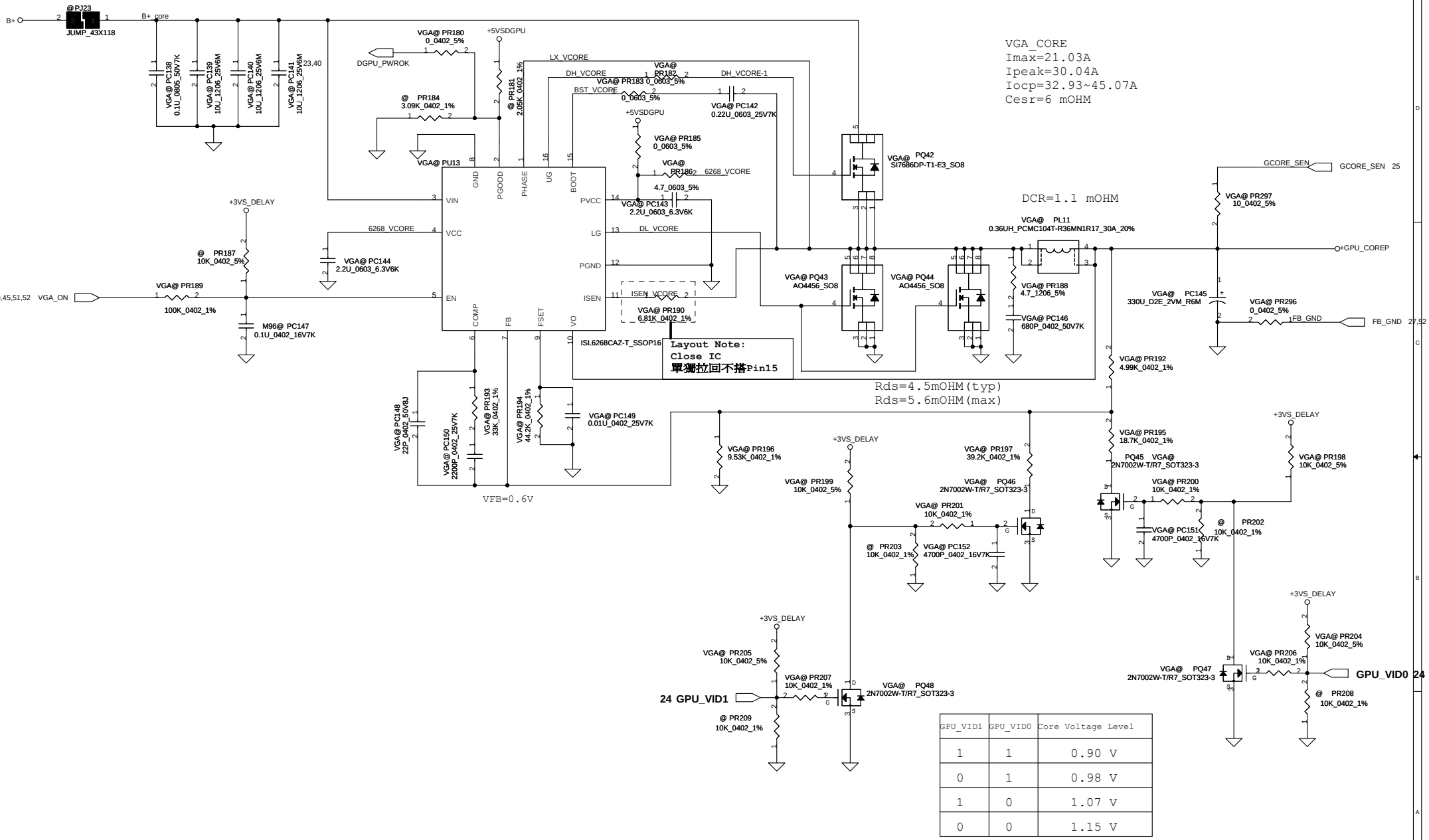

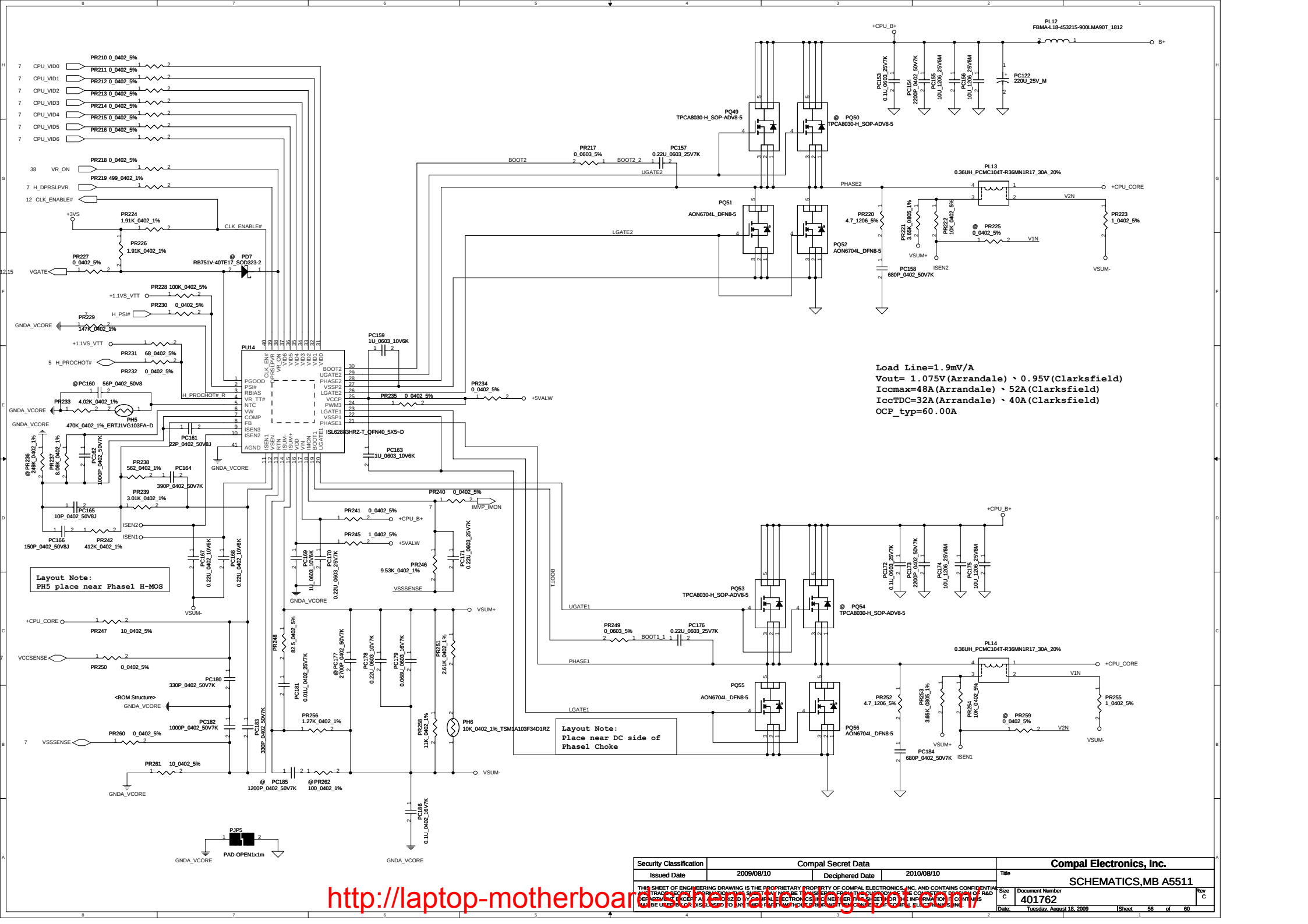

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Version change list (P.I.R. List)

for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	BQ24751A has very low rate crack	Add BQ24751A voltage clamp protection but disable first	0.1	47	Change PR56 from 150 to 0(SD013000080) Disable PD8、PD9、PR57、PR158、PC35、PQ15 Change PQ7 to power pack	2009/05/07	EVT
2	Optimize by control IC vendor suggestion	Optimize by control IC vendor suggestion	0.1	56	Disable PR236、PC177、PC185、PR262 Change PR239 from 2.26K to 2.61K(SD000009M80) Change PC179 from 0.47U to 0.047U(SE026473K80)	2009/05/11	EVT
3					Change PR256 from 1K to 1.21K(SD000004C00) Delete PR243、PR244、PR257		
4	Optimize by control IC vendor suggestion	Optimize by control IC vendor suggestion	0.1	54	Change PR271 from 10.2K to 8.66K(SD034866180) Change PC203 from 0.068U to 0.1U(SE076104KM8)	2009/05/11	EVT
5					Change PR283 from 3.01K to 1.69K(SD00000JB80) Disable PR284、PC205		
6	Tune OCP from 15.81A to 18.62A(min) & optimize compensation by control IC vendor suggestion	Tune OCP from 15.81A to 18.62A(min) & optimize compensation by control IC vendor suggestion	0.1	53	Change PR135 from 1.96K to 2.37K(SD034237180) Change PR137 from 49.9K to 90.9K(SD034909280)	2009/05/11	EVT
7	Tune VDDCI output voltage to 1.1V by HW request	Tune VDDCI output voltage to 1.1V by HW request	0.1	52	Change PR156 from 27.4K to 124K(SD034590280)	2009/05/13	EVT
8	SH16118AM00 is non lead-free part, SH16118AM10 is	SH16118AM00 is non lead-free part, SH16118AM10 is	0.1	50	Change PL7 from SH16118AM00 to SH16118AM10	2009/05/13	EVT
9	Co-lay will cause DRC, but reserve the space	Co-lay will cause DRC, but reserve the space	0.1	56	Delete PL15、PL16	2009/05/14	EVT
10	There is not enough space	Choke change size from 10x10 to 7x7	0.2	52	Change PL17 from SH000007E80 to SH000006I80	2009/05/27	EVT2
11	Tune sequence by HW request and prevent enable abnormally	Tune sequence by HW request and prevent enable abnormally	0.2	51	Change EN net from DGPU_PWR_EN# to VGA_ON Change PR116 from 47K to 22K(SD028220280)	2009/05/27	EVT2
12	Power ON while no CPU will burn out	Power ON while no CPU will burn out	0.2	53	Change Feedback from +1.1VS_VTT to +1.1VS_VTTP	2009/05/27	EVT2
13	PQ7 has very low rate crack	Change PQ7 package to TO-253 DPAK	0.2	48	Change PQ7 from AO4407 to AOD425(SB00000K800)	2009/05/27	EVT2
14	HW request	Don't need this signal	0.2	54	Delete net GFX_CORE_PWRGD	2009/06/01	EVT2
15	Optimize by control IC vendor suggestion	Optimize by control IC vendor suggestion	0.2	56	Change PR226 from 10K to 1.91K(SD000009O80) Change PR256 from 1.21K to 1.1K(SD034110180)	2009/06/01	EVT2
16	To avoid pre-charge can not finish	To avoid pre-charge can not finish	0.2	49	Add PC135 as 1U	2009/06/02	EVT2
17	To avoid 2nd source RT8209B can no power on	To avoid 2nd source RT8209B can no power on	0.2		Change PR94、PR103、PR122、PR151 from 300 to 100(SD034100080) Change PC79、PC88、PC107、PC123 from 1U to 4.7U(SE107475K80)	2009/06/02	EVT2
18	Switch delay time can't over 1mS and OCP has risk	Tune switch delay time to 1mS and OCP to 32.93A(min)	0.2	55	Change PR190 from 3.9K to 6.81K(SD034681180) Change PC151、PC152 from 0.1U to 0.22U(SE095224K00) Change PR197 from 68.1K to 60.4K(SD034604280)	2009/06/02	EVT2 06/29 change back PC151、PC152
19	Tune OCP from 18.62A to 20.01A(min)	Tune OCP from 18.62A to 20.01A(min)	0.2	53	Change PR135 from 2.37K to 4.02K(SD034402180)	2009/06/02	EVT2
20	Sense from VTTP and CPU both	Sense from VTTP and CPU both	0.2	53	Change PR139 to +1.1VS_VTTP Add PR160 to VTT_SENSE	2009/06/03	EVT2
21	Tune OCP to 16.47A(min) & ripple noise	Tune OCP to 16.47A(min) & ripple noise	0.2	50	Change PR95 from 13.7K to 15.8K(SD034158280) Add PC136	2009/06/08	EVT2 06/22 Delete PC136
22	Tune Output Voltage to 1.15V(max) for batter performance by HW request	Tune Output Voltage to 1.15V(max) for batter performance by HW request	0.3	55	Change PR196 from 9.76K to 7.32K(SD034732180) Change PR297 from 0 to 10(SD028100A80)	2009/06/17	EVT3
23	Tune CPU transient	Tune CPU transient	0.3	56	Change PC179 from 47nF to 68nF(SE026683K80)	2009/06/17	EVT3

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Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
24	BQ24751A has very low rate crack	Enable BQ24751A voltage clamp protection	0.3	48	Enable PD8、PD9、PC35、PQ15、PR57、PR158 Change PR56 from 0 to 150(SD014150080)	2009/06/25	EVT3
25	To prevent +3VALW/+5VALW can't boot up when VREG3 and VREG5 capacitor has big different	To prevent +3VALW/+5VALW can't boot up when VREG3 and VREG5 capacitor has big different	0.3	49	Change PC57 from 0.22U to 1U(SE080105K80)	2009/06/25	EVT3
26	Cost Down	Cost Down	0.4		Change PL5 from Molding to Coil(SH000008N80) Change PL8 from Modling to Coil 1.8uH(SH000008U80)	2009/07/02	PVT
27	Dividing equally GPU output voltage from 0.9V to 1.15V by HW request	Dividing equally GPU output voltage from 0.9V to 1.15V by HW request	0.4	55	Change PR195 from 31.6KΩ to 18.7KΩ(SD034187280) Change PR196 from 7.32KΩ to 9.53KΩ(SD034953180) Change PR197 from 60.4KΩ to 39.2KΩ(SD034392280)	2009/07/03	PVT
28	BQ24751A has very low rate crack	To prevent PVCC has spike voltage	0.4	48	Change PC32 from 0.1U to 0.22U(SE000005Z80) Add PR161 as 4.7Ω(SD001470B80) Change PR56 from 150Ω to 1KΩ(SD013100180) ~~Add PC36 as 1000pF(SE074102K80)~~ Change PC30 from 0.01uF to 0.022uF(SE075223K80) Disable PD8、PD9、PQ15、PC35、PR57、PR158	2009/07/09	PVT
29	To avoid false trigger of current imbalance protection if ISEN caps have wider tolerance	To avoid false trigger of current imbalance protection if ISEN caps have wider tolerance	0.4	56	Change PC167、PC168 AGND net to VSUM-	2009/07/09	PVT
30	Tune VID delay time to about 470uS	To false avoid trigle of OVP/UVP, the normal switch time is 220uS	0.4	55	Change PC151、PC152 from 0.1U to ~~0.047U(SE076473K80)~~ 4.7n(SE076472K80)	2009/07/09	PVT Change 2009/07/10
31	Cut in EMI solution	Cut in EMI solution	0.4		Change PJ22 jump to PL18 bead(SM010016410) Enable PR133、PR188、PR220、PR252、PC114、PC146、PC153、PC158、PC172、PC184	2009/07/10	PVT
32	Cost Down	Cost Down	0.4	53	Change PQ35 from AO4456 to AO6704L(SB000001900) Delete PQ36	2009/07/10	PVT
33	Vendor production phase out	Vendor production phase out	0.4		Change PC116、PC130、PC145 from SGA00002380 to SGA00002U00	2009/07/10	PVT
34	Adjust OCP from ~52A to ~60A	Adjust OCP from ~52A to ~60A	0.4	56	Change PR239 from 2.61K to 3.01K(SD034301180) Change PR246 from 8.25K to 9.53K(SD034953180) Change PR256 from 1.1K to 1.27K(SD034127180)	2009/07/21	PVT
35	Cost Down	Cost Down	0.5	56	Change PH6 from 0603 to 0402(SL200000W00) Change PH1、PH2 from 0603 to 0402(SL200000V00) Change PH3 from 0603 to 0402(SL200001100)	2009/08/06	Pre-MP
36	HW request	HW request	0.5	56	Change PR108、PR110 from 1K to 100K(SD034100380)	2009/08/06	Pre-MP
37	HW request	For Intel S3 POWER reduce	0.5	53	Add PR162 4.53K(SD034453180) Change PR130 from 1K to 2.26K(SD034226180)	2009/08/10	Pre-MP

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A1--> A2 Change List

2009/05/26
Page 33 SWAP HDD SATA_DTX_C_PRX_N1/P1
Page 38 Del DPIO42 (GFX_CORE_PWRGD) and ADD ME_EN in GPIO42 to PCH GPIO33 (For enable ME to entry manufactruing mode)
Page 12/37 Del PCH_SATA2_CE# and change PCH_SATA1_CE# for Esata redriver IC enable singal

2009/06/02
Page 30 Reverse JLVDS1 pin 36 and pin 37
Page 39 Reverse JKB1 pin defined
Page 12 colay Relatek CLK Gen
Page 39 Follow EMI request,add R486 and C9...
Page 24 switch the net name EC_SMB_DA2 and EC_SMB_CK2

2009/06/03
Page 40 add R490,R491,R493 and R494 for LED brightness
Page 38 change EC pin 75 from GFX_CORE_PWRGD to ME_EN

2009/06/04
change Y1,Y3,Y4,Y10,X1 crystal PCB footprint
Page 45 change R462 to 22k
Page 15 change R315 to 100k

A2--> A3 Change List

2009/06/25
Page 14 R305 pull high to +3VS_Delay
Page 15,24,38 Add ACIN_BUF for PCH/VGA
Page 24 Un-pop R177 (No use external Vbios ROM)
change R28 to 510K (for VGA Power on sequence)
Page5,6,7,44 Reserve INTEL Capella new design schematic
Page 24 SWAP Q57,Q58,Q62 Pin1 and PIN3,
change Q62 to UMA@
Page 38 change PWR_SUSP_LED to U38.84
Page 36,38,39 combine LED fuction to BT_ON#
Page 39 SWAP JP9
Page 40 Add discharge schematic for VGA_ON

A3-->C Change List

2009/07/06
Page 32 Switch the U57 Pin 27 and Pin 49 (IGPU_SELECT# and DGPU_SELECT#)

2009/07/08
Page 24 Add R833,for short +3VS to +3VS_DELAY
Page 25 Add R116 and R225 for Boradway MVREFDA/B and MVREFSA/B
Page 25 Add C473,C474,R265 and R327 for Boradway CLKTESTA/B
Page 27 Add R770 and R771
Page 32 Add R768,R769,R767,R786,R772 and Delete Q62,R793 to verify HDMI HPD
Page 18 Add R333 to pull down GPIO37 and change R293 to UMAO@

2009/07/10
change 4.7u_0805 to 4.7u_0603
Page 14 Add R104,R793,R342 and R341 for PEG_CLKREQ#
Page 38 update Board ID to 0.4 R364=100K,R365=56K

2009/07/13
Page 25 add R343,R344,R361,R498,R499 and R500 for broadway
Page 7 update 470uF to 330uF(C232, C186, C711, C221, C259 and C196)
Page 39 Update R5 and R6 package from 0402 to 0603...
Page 24 add Q76,C476 and R795 for +3VS_DELAY
Page 24 Switch Q9 and change the +3VS to +3VS_DELAY

C-->Pre-MP Change List

2009/07/17
Page 42 switch MIC1_LFE_L and MIC1_CEN_R

2009/07/28
Page 39 Add Q62 to replace D11
Page 25 Add R502 and R504

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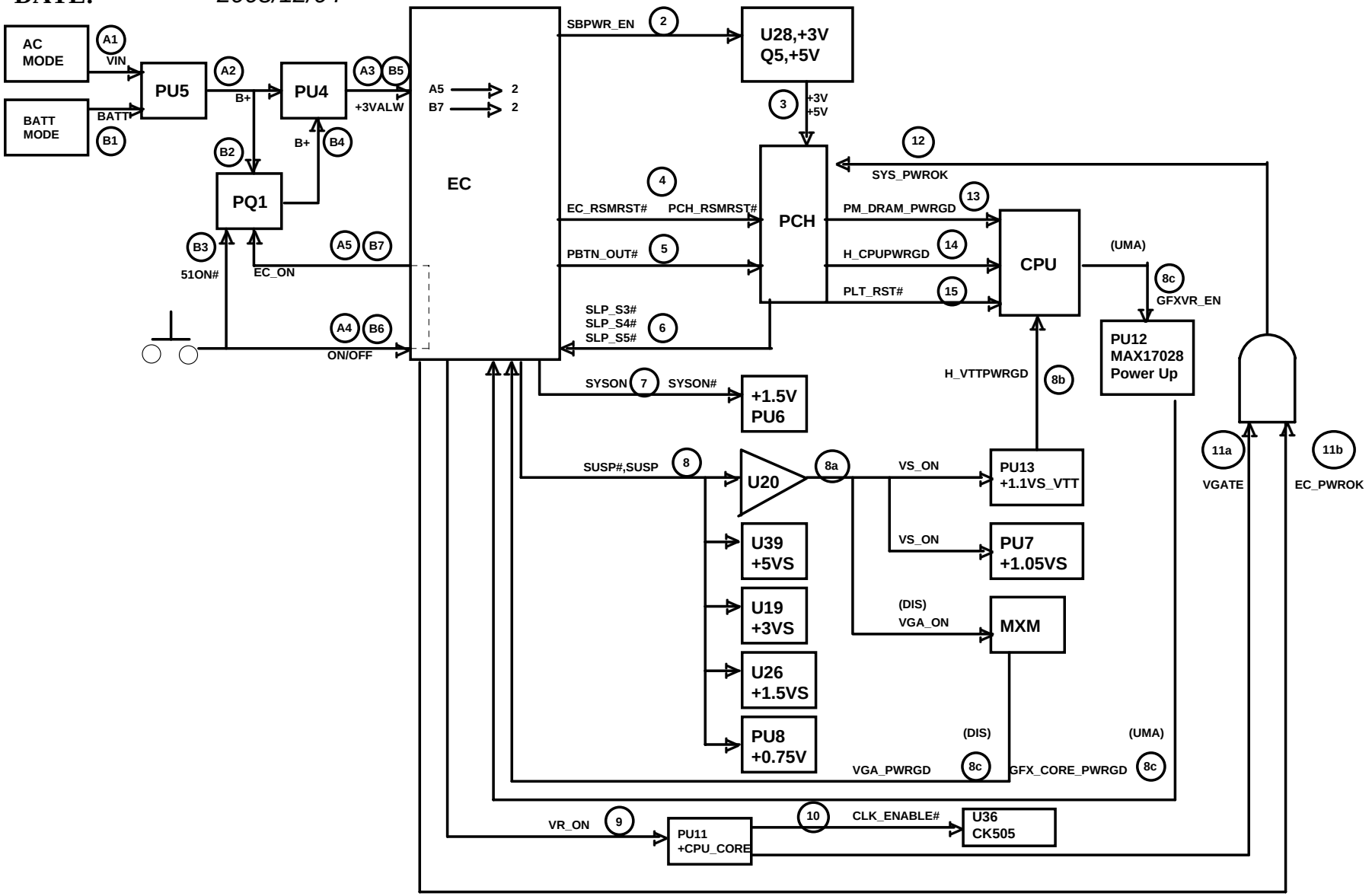
COMPAL CONFIDENTIAL

MODEL NAME: *KBLA0 Power Sequence Block Diagram*
PCB NAME: *LA4811P*
REVISION:
DATE: *2008/12/04*



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