2. Circuit Description

2-1. SGH-X700 RF Circuit Description

2-1-1. RX PART

- FRONT END MODULE(ANTENNA SWITCH MODULE + RX SAW FILTER) (U100)

It performs to switch Tx & Rx paths for GSM900, DCS1800 and PCS1900 with logic controls below.

- FEM Control Logic Table

	FESW1	FESW2
Tx Mode (GSM900)	H	L
Tx Mode (DCS1800/1900)	L	H
Rx Mode (GSM900)	L	L
Rx Mode (DCS1800)	L	L
Rx Mode (PCS1900)	L	L

- VC-TCXO (TCX100)

This module generates the 26MHz reference clock to drive the logic and RF systems.
It is turned on when the supply voltage (+VCC_SYN_2V8) is applied.
After buffering, the 26MHz reference clock is supplied to the other parts of the system through the transceiver pin CLKOUT.

- Transceiver (U102)

This chip is fully integrated GSM & GPRS tri-band transceiver with RF VCO, loop filters and most of the passive components required in it.
It also fully integrated fractional N RF synthesizer with AFC control possibility, RF VCO with integrated supply regulator. Semi integrated reference oscillator with integrated supply regulator.
RF Receiver front-end amplifies the E-GSM900, DCS1800 and PCS1900 aerial signal, convert the chosen channel down to a low IF of 100kHz.
In IF section, further amplifies the wanted channel, performs gain control to tune the output level to the desired value and rejects DC.

2-1-2. TX PART

The transmitter is fully differential using a direct up conversion architecture. It consists of a signal side band power up mixer. Gain is controlled by 6 dB via 3-wire serial bus programing. The fully integrated VCO and power mixer achieve LO suppression, quadrature phase error, quadrature amplitude balance and low noise floor specification. Output matching/balun components drive a standard 50 ohms single ended load.

2-2. Baseband Circuit description of SGH-X700

2-2-1. PCF50603 (U400)

- Power Management

  Eight low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable boost converter provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as RTC module and High Voltage Charge pump, Clock generator, aid in reducing both board area and system complexity.

  I2C BUS serial interface provides access to control and configuration registers. This interface gives a microprocessor full control of the PCF50603 and enables system designers to maximize both standby and talk times.

  Supervisory functions. including a reset generator, an input voltage monitor, and a temperature sensor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

- Pulse-Width Modulator

  The Backlight Brightness Modulator (BBM) contains a programmable Pulse-width modulator (PWM) to modulate the intensity of a series of LED's or to control a DC/DC converter that drives LCD backlight.

  This phone is using PWM control to modulate the LCD backlight brightness.

- Clock Generator

  The Clock Generator (CG) generates all clocks for internal and external usage. The 32.768 kHz crystal oscillator provides an accurate low clock frequency for the PCF50603 and other circuitry.

2-2-2. LCD

X700 has just one 1.9" TFT LCD. 16-bit data lines(LD(0)~LD(15)) transfers data and commands to LCD. There are couple of control signals such as RS, CS, RD, WR, etc. RS stands for "Register Select pin." When RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write operation is selected according to RD/WR signals. The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1. At the falling edge of CS input, serial data transfer is initiated. On the other hand, at the rising edge of CS input, the data transfer is ceased.

2-2-3. Key

Key recognition part is consisted of 8 ports from PCF5213EL1. KEY_ROW(0:4) & KEY_COL(0:4)

These signals performs with the matrix. Any input from the matrix informs the key status to key interface in the PCF5213EL1. Power on/off key is independent of the matrix. Therefore, 'power on/off' signal is directly connected with PCF50603 to turn PCF50603 on.

3.3V LDO(U700) enables Key LED on. Key LED consists of 12 LEDs. It is controlled by "Key_led_on" signal.

2-2-4. EMI ESD Filter (U500)

This system uses the EMI ESD filter (U500) to protect the device from noises from IF CONNECTOR part.

2-2-5. IF connetor (IFC500)

It has 18-pin. They are designed to allocate VBAT, V_EXT_CHARGE, USB_D+, +VBUS, USB_D-, TXD1, RXD1, AUX_ON, EXT1, EXT2 and GND. They connected to power supply IC, microprocessor and signal processor IC.

2-2-6. Battery Charge Management

X700 has a complete constant-current/constant-voltage linear charger for single cell lithium-ion batteries inside.
If Travel Adapter is connected, "V_EXT_CHARGE" begins to provide the charger IC (to battery) with power (current). When the charging operation is done, "End_of_charge" informs it to PCF5213EL1 to stop the operation. "CHG_ON" signal enables the charger IC to operate in adequate circumstances.

2-2-7. Audio - Part

X700 has several audio-outputs such as stere speaker, receiver, earphone, etc. RCV_P/N signals from CPU are connected to the receiver via analog switche (U602). MIC_P/N are connected to the main MIC as well.
YMU762 is a synthesizer LSI for mobile phones. This LSI has a built-in speaker amplifier for outputting sounds that are used by mobile phones in addition to game sounds and ringing melodies that are replayed by a synthesizer.
YMU762 has built a speaker amplifier of which maximum out is 580 mW at SPVDD=3.6V in this device. There is Stereophonic analog output for Headphone.

2-2-8. Memory (UME300)

X700 has KAP17SG00A-D4U4 as a memory module.
The KAP17SG00A-D4U4 is a Multi Chip Package Memory which combines 256Mbit Synchronous Burst Multi Bank NOR Flash Memory and 512Mbit OneNAND Flash and 128Mbit Synchronous Burst U tRAM.
It has 16 bit data line, HD[1~16] which is connected to PCF5213 and MV3315DOQ, also has 24 bit address lines, HA[1~24]. There are 3 chip select signals, CS0n_FLASH, CS1n_RAM, and CS4n_NAND.
In the wrting process, WEn is fallen to low and it enables writing process to operate. During reading process, OEn is fallen to low and it enables reading process to operate. Each chip select signals in the PCF5213EL1 choose different types of memory.

2-2-9. PCF5213EL1 (UCP200)

The PCF5213EL1 is mainly composed of embeded DSP and ARM core. The DSP subsystem includes the Saturn DSP core with embedded RAM and ROM, and a set of peripherals. It has 24k×16 bits PRAM, 104k×16 bits, 32k×16 XYRAM and 63k×16 XYROM in the DSP.
The ARM946E-S consists of an ARM9E-S processor core, 8 kbyte instruction cache and 8 kbyte data cache, tightly-coupled ITCM (Instruction Tightly Coupled Memory) and DTCM (Data Tightly Coupled Memory) memories, a memory protection unit, and an AMBA (Advanced Microcontroller Bus Architecture) AHB (Advanced High-performance Bus) bus interface with a write buffer.
HD(0:15), data lines and HA(0:23), address lines are connected to KAP17SG00A (memory), MV3018B (image dsp) and YMU762 (melody IC). It has 64 kbyte SC RAM (0.5 Mbit) and 32 kbyte SC program ROM for bootstrap loader in the ARM core.

HD(0:15), data lines and HA(0:23), address lines are connected to memory and YMU762 to communicate.
MV3018B(Camera DSP Chip) controls the communication between ARM core and DSP core.
OEn, WEn control the access of memory. KROW, and KCOL recognize the key string input status.
It has J-TAG control pins (TDI/TDO/TCK) for ARM and DSP core. J-SEL signal controls different access to ARM and DSP core.
ADC(Analog to Digital Convertor) receives the condition of temperature, battery type and battery voltage.

HD(0:15), data lines and HA(0:23), address lines are connected to memory and YMU762 to communicate.
MV3315DOQ(Camera DSP Chip) controls the communication between ARM core and DSP core.
OEn, WEn control the access of memory. KROW, and KCOL recognize the key string input status.
It has J-TAG control pins (TDI/TDO/TCK) for ARM and DSP core. J-SEL signal controls different access to ARM and DSP core.
ADC(Analog to Digital Convertor) receives the condition of temperature, battery type and battery voltage.

2-2-10. VC-TCXO-214C6 (TCX100, 26MHz)

This system has the 26MHz TCXO, TCO-5871U from Toyocom. AFC controlling signal form PCF5213EL1 controls frequency from 26MHz X-tal. It generates the clock frequency. This clock is connected to PCF5213EL1, YMU762 and UAA3587.

2-2-11. Camera DSP (U303, MV3315DOQ)

MV3315DOQ provides rich video functions up to 30-frame display with minimized tasks in the handset main processor as well as hardware based real-time JPEG compression and decompression. MV3315DOQ directly transmits and previews the RGB data to the LCD graphic memory by processing the sensor output data according to the handset's command. It can save the raw RGB data up to VGA resoultion into its image buffer and allows the host processor to download with scalable sized compressed data.
It utilizes 16 bit data bus for communication with the main processor, including bus interface types.