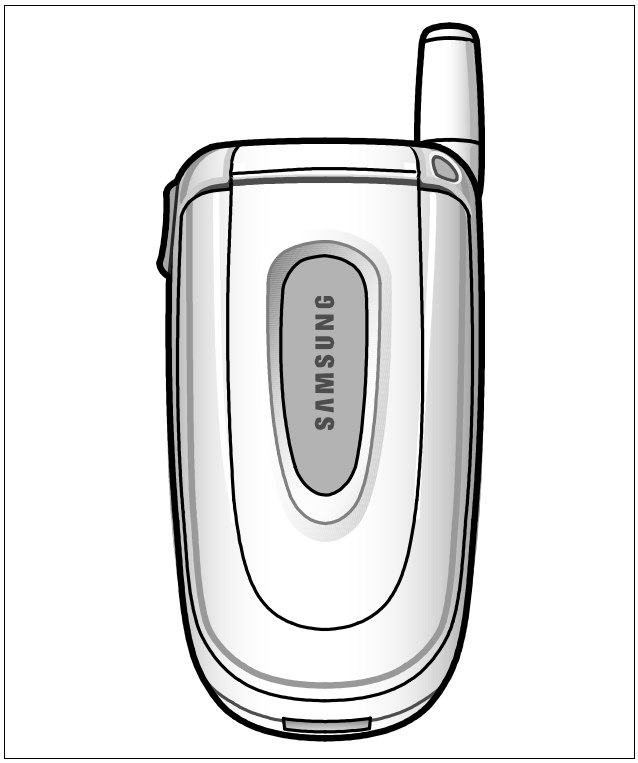
SAMSUNG

GSM TELEPHONE
SGH-X450

SERVICE Manual

GSM TELEPHONE



CONTENTS

ELECTRONICS

Code No.: GH68-04745A
BASIC.

1. SGH-X450 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1	PCS1900
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880	1850~1910 1930~1990
ARFCN range	1~124	0~124 & 975~1023	512~885	512~810
Tx/Rx spacing	45MHz	45MHz	95MHz	80MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm	-100dBm
TDMA Mux	8	8	8	8
Cell Radius	35Km	35Km	2Km	-

2. GSM TX power class

TX Power control level	GSM900
5	33±2 dBm
6	31±2 dBm
7	29±2 dBm
8	27±2 dBm
9	25±2 dBm
10	23±2 dBm
11	21±2 dBm
12	19±2 dBm
13	17±2 dBm
14	15±2 dBm
15	13±2 dBm
16	11±3 dBm
17	9±3dBm
18	7±3 dBm
19	5±3 dBm

TX Power control level	DCS1800
0	30±2 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

TX Power control level	PCS1900
0	30±2 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

2. SGH-X450 Circuit Description

1. SGH-X450 RF Circuit Description

1) RX PART

1. ASM(U201) → Switching Tx, Rx path for E`GSM900, DCS1800 and PCS1900 by logic controlling.

2. ASM Control Logic (U501, U502, U503) → Truth Table

	VC1	VC2	VC3
GSM Tx Mode	H	L	L
DCS / PCS Tx Mode	L	H	L
PCS Rx Mode	L	L	H
GSM / DCS Rx Mode	L	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (C220,C221,L204) → For filtering the frequency band between 925 ~ 960 MHz
- DCS FILTER (C218,C219,L203) → For filtering the frequency band 1805 and 1880 MHz.
- PCS SAW FILTER (F200) → For filtering the frequency band between 1930 and 1990 MHz

4. TC-VCXO (OSC100)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U100 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. SI 4205 (U100)

This chip integrates three differential-input LNAs.

The GSM input supports the E-GSM, DCS input supports the DCS1800, PCS input supports the PCS1900. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from frequency synthesizer. The RFLO frequency is between 1737.8 ~ 1989.9 MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

Also, this chip down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals.

After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U100 chip.
SI4205 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U200).
The PA output power and power ramping are well controlled by Auto Power Control circuit. We use offset PLL below

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

2. Baseband Circuit description of SGH-X450

1) PSC2106

1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life.A programmable LDO provides support for 1.8V, 3.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as two LED drivers and two call-alert drivers, aid in reducing both board area and system complexity.A four-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the PSC2106 and enables system designers to maximize both standby and talk times. Error reporting is provided via an interrupt signal and status register.Supervisory functions. including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

2. Battery Charge Management

A battery charge management block, incorporating an internal PMOS switch, and an 8-bit ADC, provides fast, efficient charging of single-cell Li-Ion battery. Used in conjunction with a current-limited voltage source, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard and LCD illumination. LED1_DRV is controlled via LED1_[0:2] and can be programmed to sink from 15mA to 60mA in 7.5mA steps. LED2_DRV is controlled via LED2_
[0:2] and can be programmed to sink from 5mA to 40mA in 5mA steps.
Both LED drivers are capable of sinking their maximum output current at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

4. Vibrator Motor Driver

The vibrator motor driver is a low-side, programmable voltage source designed to drive a small dc motor that silently alerts the user of an incoming call. The driver is controlled by VIB[0:1] and can be programmed to maintain a motor voltage of 1.3V, 2.0V, or 2.5V(relative to VBAT) while
sinking up to 100mA. For efficient use, the vibrator motor should be connected between the main battery and the VIB_DRV output.

2) Connector

1. LCD Connector

LCD is consisted of main LCD(color 65K UFB LCD). Chip select signals of EMI part in the trident, CLCD_EN, can enable main LCD. LED_EN signal enables white LED of main LCD and EL_EN signal enables dimming mode of main LCD.
These two signals are from IO part of the DSP in the trident. RST signal from 2106 initiates the initial process of the LCD.
16-bit data lines(D(0)~D(15)) transfers data and commands to LCD through emi_filter. Data and commands use A(2) signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So CP_WEN signal is used to write data or commands to LCD.
Power signals for LCD are +VBATT and VCCD.
SPK1P and SPK1N from CSP1093 are used for audio speaker. And YMU_VIB_EN from MA-3 enables the motor.

2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'.
CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

C. Battery Charge Management

3. Keypad connector

This is consisted of key interface pins in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix.
So power on/off signal is connected with PSC2106 to enable PSC2106. SVC_GREEN, SVC_RED and SVC_BLUE are from OCTL of CSP1093.
These signals decide the color of LED, service indicator.
Nine key LED use the +VBATT supply voltage. These are connected to BACKLIGHT signal in the PSC2106.
This signal enables LEDs with current control. FLIP_SNS informs the status of folder (open or closed) to the trident. This uses the hall effect IC, A3210ELH.
A magnet under main LCD enables A3210ELH which is on the main PCB.

4. EMI Filtering

This system uses the EMI Filter to reduce noise from LCD part. Some control signals are connected to LCD without EMI filtering.

3) IF connetor

It is 23-pin connector, and uses 18-pin at present. They are designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, VEXT, VTEST, VF, +VBATT and GND. They connected to power supply IC, microprocessor and signal processor IC.

4) Audio

AOUTAP, AOUTAN from CSP1093 is connected to the speaker via analog
switch. AOUTBP and AOUTBN are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.
YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.
As a synthesis, YMU762MA3 is equipped 16 voices with differenttones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexiblysupport application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU762 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor and a circuit for controlling LEDs synchornous with music.
For the headphone, it is provided with a stereophonic output terminal.
For the purpose of enabling YMU762MA3 to demonstarte its full capablities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible wiht multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for traning karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to systhesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

5) Memory

This system uses SHARP's memory, LRS1828.
It is consisted of 128M bits flash memory and 32M bits SCRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP1093. It has 22 bit address lines, A[1~22]. They are connected too. CP_CSROMEN and CO_CSROM2EN signals, chip select signals in the trident enable two memories. They use 3 volt supply voltage, VCCD. During wrting process, CP_WEN is low and it enables writing process to flash memory and SCRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or SCRAM to data lines. Each chip select signals in the trident select memory among 2 flash memory and SCRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use FLASH_RESET, which is buffered signal of RESET from PSC2106, for ESD protection. A[0] signal enables lower byte of SCRAM and UPPER_BYTE signal enables higher byte of SCRAM.

6) Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACCs(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface. DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP1093. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU762. ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core.
CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.

Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communicatios using data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).
And UP_CS/SCLK/SDI, control signals for PSC2106 are outputted through PPI pins. It has signal port for charging(CHG_DET), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD with DSP IP pins.

7) CSP1093

CSP1093 integrates the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions. The CSP1093 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP1093's internal register, and program CSP1093's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal

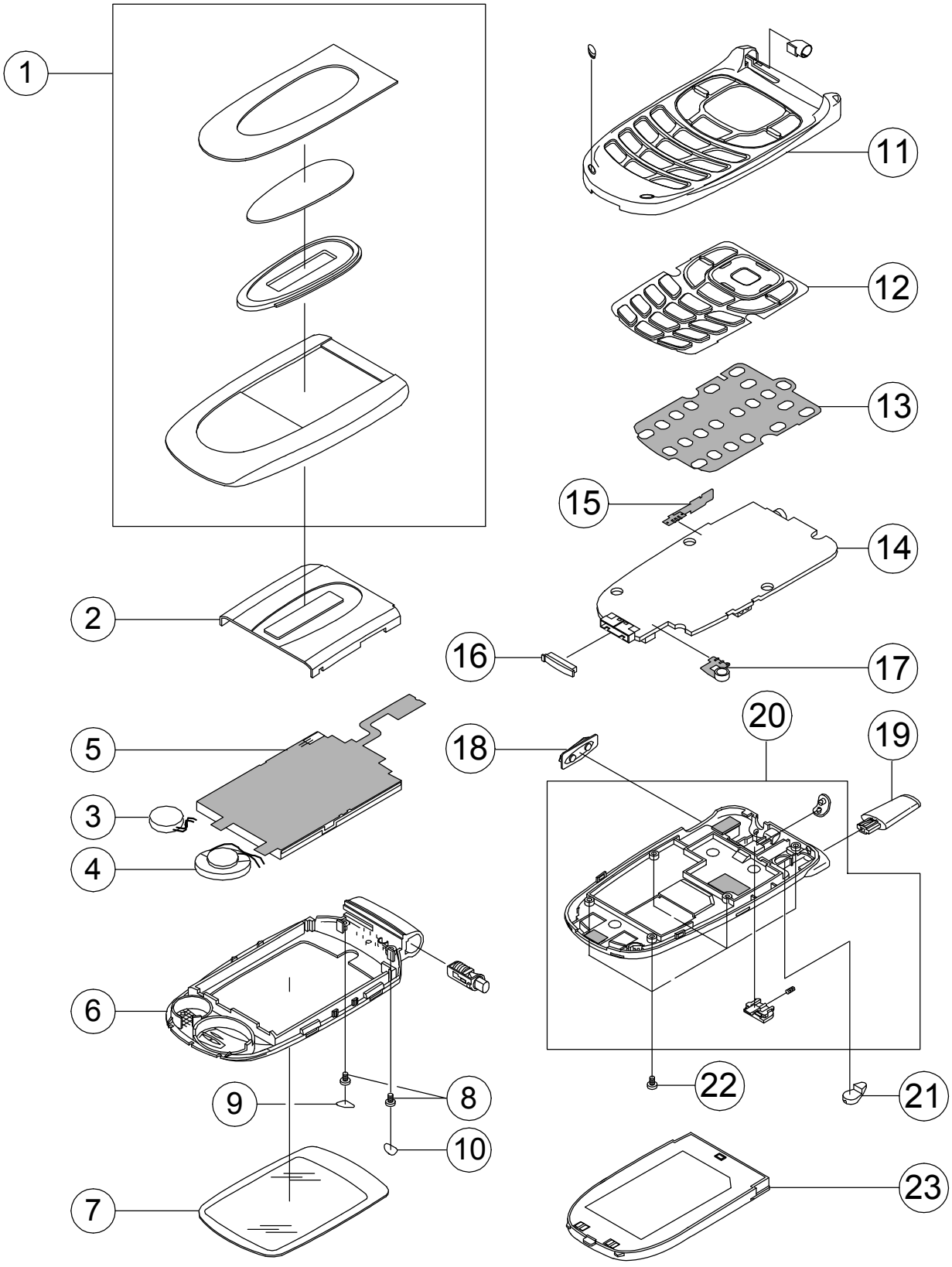
Register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP1093's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP1093 then notifies the DSP which has ample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

8) X-TAL(13MHz)

This system uses the 13MHz TCXO, TCO-9141B, Toyocom. AFC control signal form CSP1093 controls frequency from 13MHz x-tal. It generates the clock frequency. This clock is fed to CSP1093,Trident,YMU762 and Silab solution.

3. SGH-X450 Exploded View and its Parts list

1. Cellular phone Exploded View-1



2. Cellular phone Parts list

NO	Description	SEC CODE	Remark
1	FOLDER UPPER	GH75-03608A	
2	FRAME	GH72-11125A	
3	MOTOR	GH31-00077A	
4	SPEAKER	3001-001509	
5	MAIN LCD	GH07-00490A	
6	FOLDER LOWER	GH75-03609A	
7	WINDOW LCD	GH71-01539A	
8	SCREW	6001-001479	
9	SCREW CAP(L)	GH74-01466A	
10	SCREW CAP(R)	GH74-01467A	
11	FRONT COVER	GH75-03607	
12	KEYPAD	GH75-04141A	
13	DOME SHEET	GH59-01212A	
14	MAIN PBA	GH92-01595A	
15	VOLKEY FPCB	GH59-01213A	
16	IF COVER	GH73-01844A	
17	MIC	GH30-00090A	
18	VOLUME KEY	GH75-02846A	
19	ANTENNA	GH42-00374A	
20	REAR COVER	GH75-03610A	
21	RF COVER	GH73-01894A	
23	BATTERY	GH43-01074A	

3. Test Jig (GH80-00865A)

3-1. RF Test Cable
(GH39-00140A)

3-2. Test Cable
(GH39-00127A)

3-3. Serial Cable

3-4. Power Supply Cable

3-5. DATA CABLE
(GH39-00143B)

3-6. TA
(GH44-00184A)

4. SGH-X450 MAIN Electrical Parts List

SEC Code	Design LOC
0404-001172	D1101
0404-001172	D1102
0404-001172	D1103
0406-001083	ZD300
0406-001083	ZD301
0406-001152	ZD302
0501-000225	Q400
0504-000168	Q100
0504-001151	U701
0504-001151	U702
0504-001151	U703
0506-001052	U102
0601-001547	LED801
0601-001547	LED802
0601-001547	LED803
0601-001547	LED804
0601-001547	LED805
0601-001547	LED806
0601-001547	LED807
0601-001547	LED808
0601-001547	LED809
0601-001547	LED812
0604-001146	LED200
0801-000796	U1105
0801-000796	U1108
0801-000796	U1109
0801-002212	U1110
0801-002727	U1107
0801-002727	U1111
0801-002727	U1112
1009-001010	U802
1109-001274	U500
1203-001720	U1104
1203-002568	U100
1204-001960	U401
1204-001982	U1103
1204-001984	U700

SEC Code	Design LOC
1209-001219	U602
1209-001497	U101
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1405-001082	ZD201
1405-001082	ZD303
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1405-001082	ZD305
1405-001082	ZD306
1405-001082	ZD307
1405-001082	ZD401
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1405-001082	ZD800
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1405-001082	ZD802
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2007-000140	R424
2007-000141	R113
2007-000141	R407
2007-000141	R420
2007-000144	R701
2007-000146	R404
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2007-000157	R300
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SEC Code	Design LOC
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2007-000162	R503
2007-000162	R607
2007-000162	R710
2007-000162	R711
2007-000162	R712
2007-000163	R1101
2007-000167	R108
2007-000170	R1103
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2007-007107	R1008
2007-007139	R112
2007-007142	R111
2007-007142	R603
2007-007200	R106
2007-007200	R705
2007-007200	R706
2007-007306	R1109
2007-007306	R1111
2007-007306	R1112
2007-007306	R1113
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2203-000438	C414
2203-000585	C1137
2203-000585	C407
2203-000628	C614
2203-000628	C616
2203-000679	C430
2203-000679	C606
2203-000812	C100
2203-000812	C1012
2203-000812	C1015
2203-000812	C1016
2203-000812	C104
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2203-001124	C1142
2203-001259	C432
2203-001405	C607
2203-001412	C910
2203-001598	C102
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2203-001598	C114
2203-001598	C115
2203-001598	C118
2203-001598	C119
2203-002677	C1005
2203-002677	C1006
2203-002687	C401
2203-005061	C101
2203-005061	C103
2203-005061	C1103
2203-005061	C1104
2203-005061	C1109
2203-005061	C1110
2203-005061	C1111
2203-005061	C1112
2203-005061	C1113
2203-005061	C1114

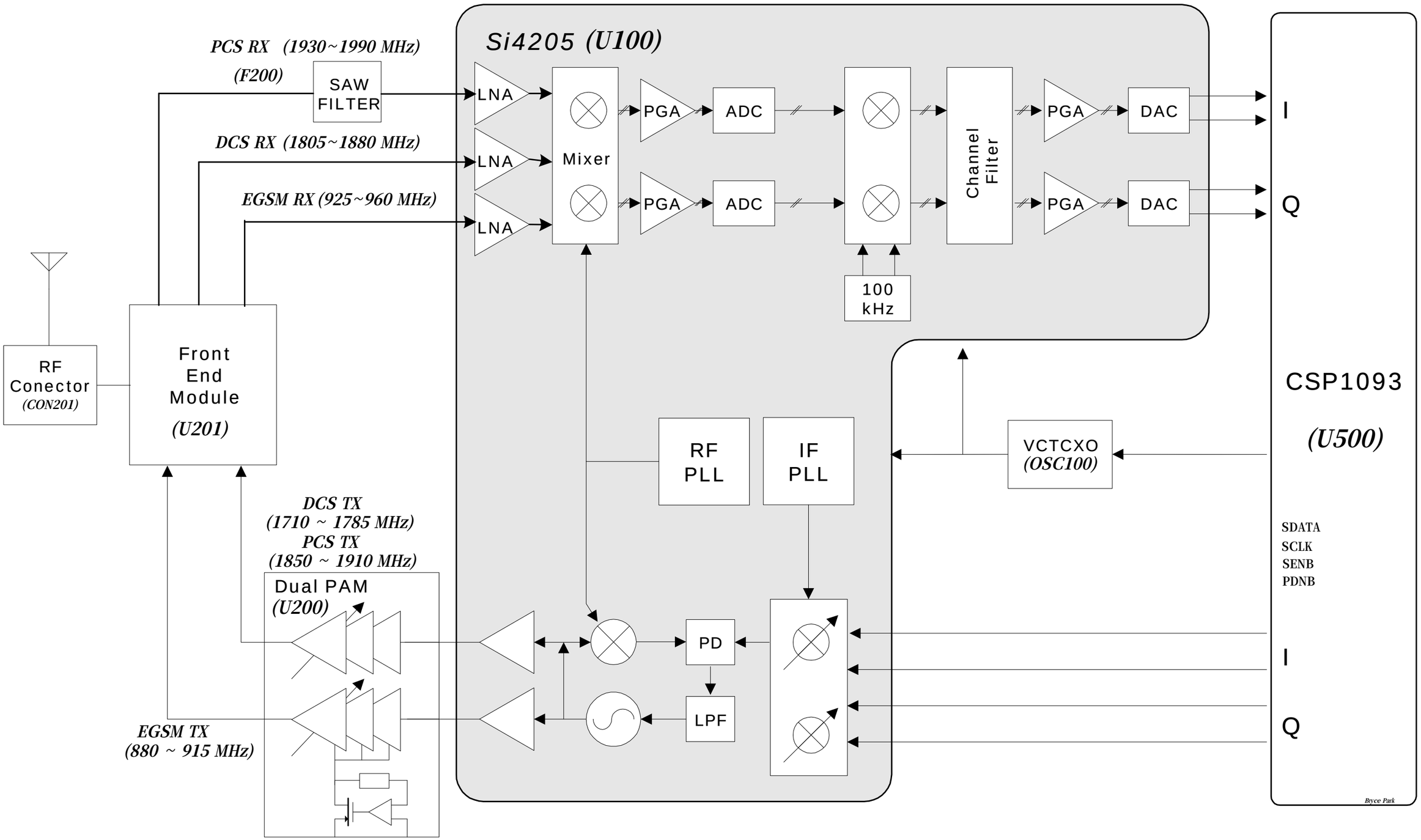
SEC Code	Design LOC
2203-005061	C1115
2203-005061	C1117
2203-005061	C1118
2203-005061	C1119
2203-005061	C1120
2203-005061	C1121
2203-005061	C1122
2203-005061	C1124
2203-005061	C1125
2203-005061	C120
2203-005061	C402
2203-005061	C408
2203-005061	C412
2203-005061	C417
2203-005061	C500
2203-005061	C501
2203-005061	C502
2203-005061	C605
2203-005061	C705
2203-005065	C1135
2203-005065	C232
2203-005065	C233
2203-005065	C400
2203-005065	C416
2203-005065	C704
2203-005234	C1001
2203-005234	C1009
2203-005234	C1010
2203-005288	C1003
2203-005288	C1004
2203-005481	C1116
2203-005482	C200
2203-005482	C811
2203-005483	C106
2203-005496	C1101
2203-005496	C403
2203-005496	C600

SEC Code	Design LOC
2203-005496	C609
2203-005496	C703
2203-005496	C903
2203-005503	C1144
2203-005509	C201
2404-001086	C425
2404-001100	C1106
2404-001100	C1107
2404-001100	C1134
2404-001105	C125
2404-001134	C1013
2404-001151	C409
2404-001268	C126
2404-001268	C404
2503-001041	C207
2503-001041	C208
2503-001053	C203
2503-001053	C204
2503-001053	C206
2503-001053	C211
2503-001053	C212
2503-001053	C213
2703-001733	L1003
2703-001949	L1000
2703-002176	L1017
2703-002207	L900
2703-002367	L1010
2703-002367	L1012
2703-002485	L1001
2703-002544	L1002
2801-003747	OSC601
2804-001492	U1102
2809-001266	OSC901
2904-001410	F1003
3404-001152	VOL_DN
3404-001152	VOL_UP
3705-001287	CON1

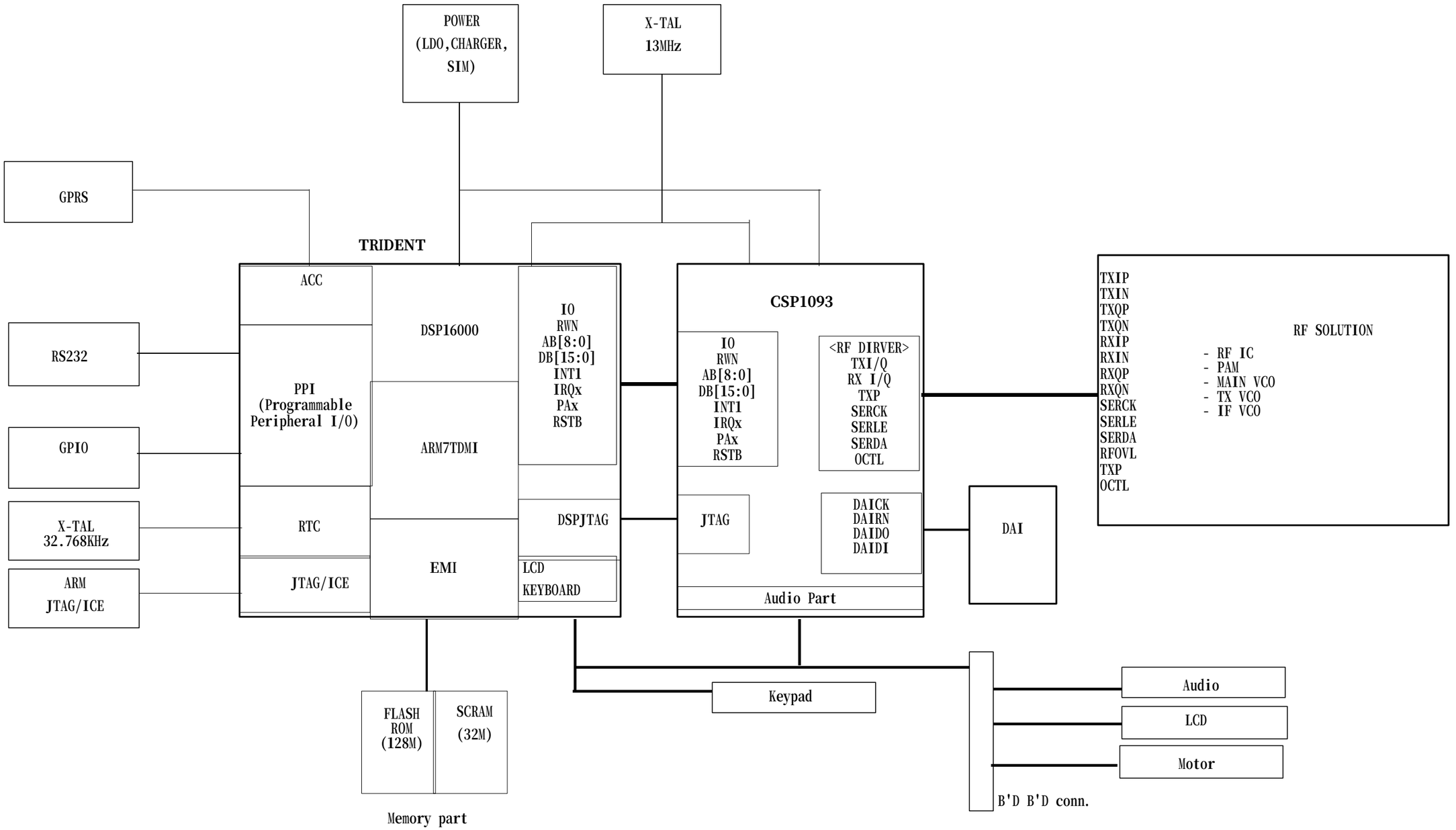
SEC Code	Design LOC
3709-001244	CN100
3711-005078	CN201
3711-005225	CN1101
3722-001715	CN401
4302-001130	M101
3710-002012	CN300
1001-001250	U400
1203-003045	U1106
2703-002636	L1006
1201-002042	U1000
2909-001208	U1001
1205-002384	U900
GH09-00023A	U601
GH13-00012A	U1101

5. SGH-X450 Block Diagrams

1. RF Solution Block Diagram

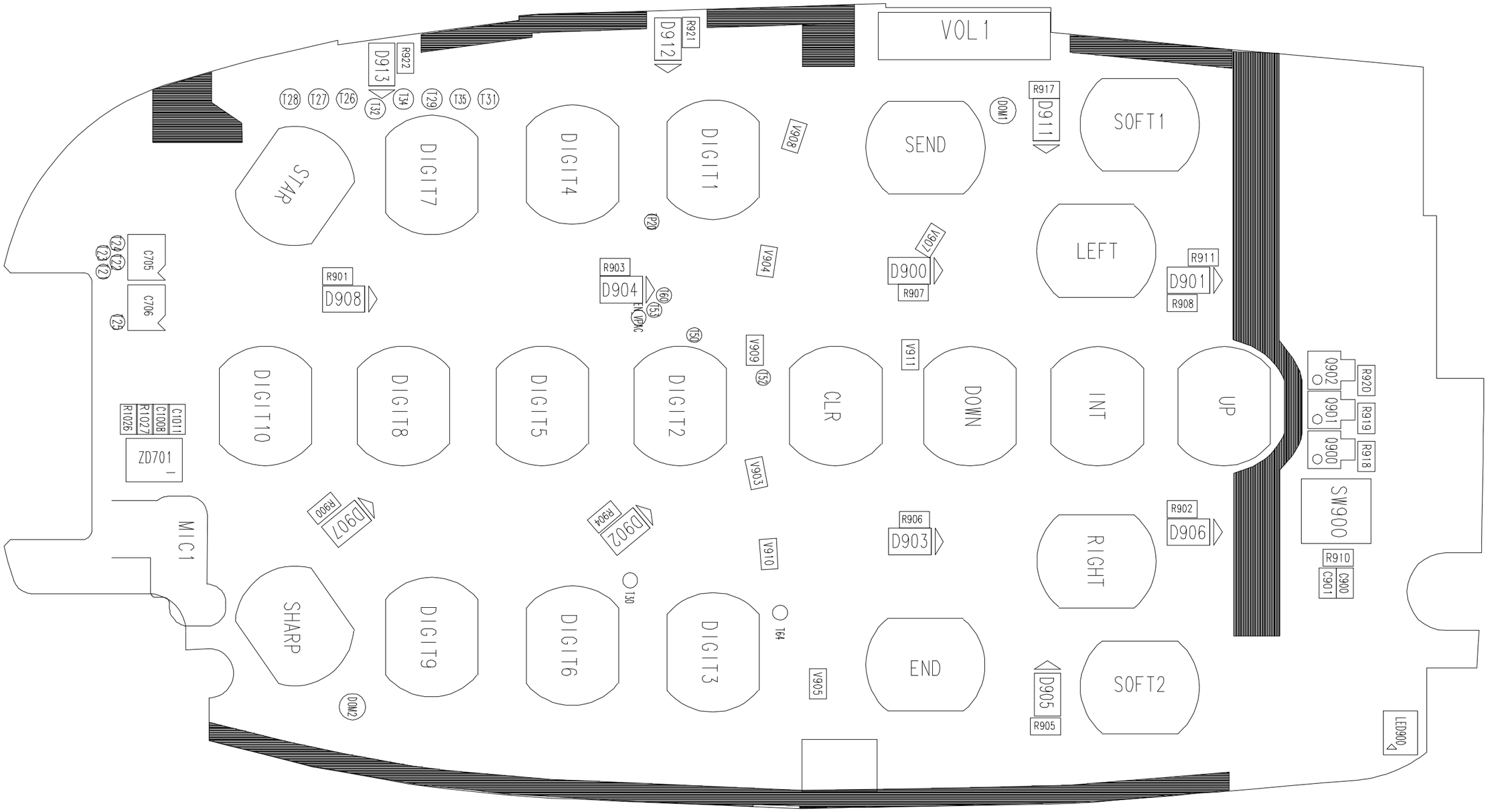


2. Base Band Solution Block Diagram

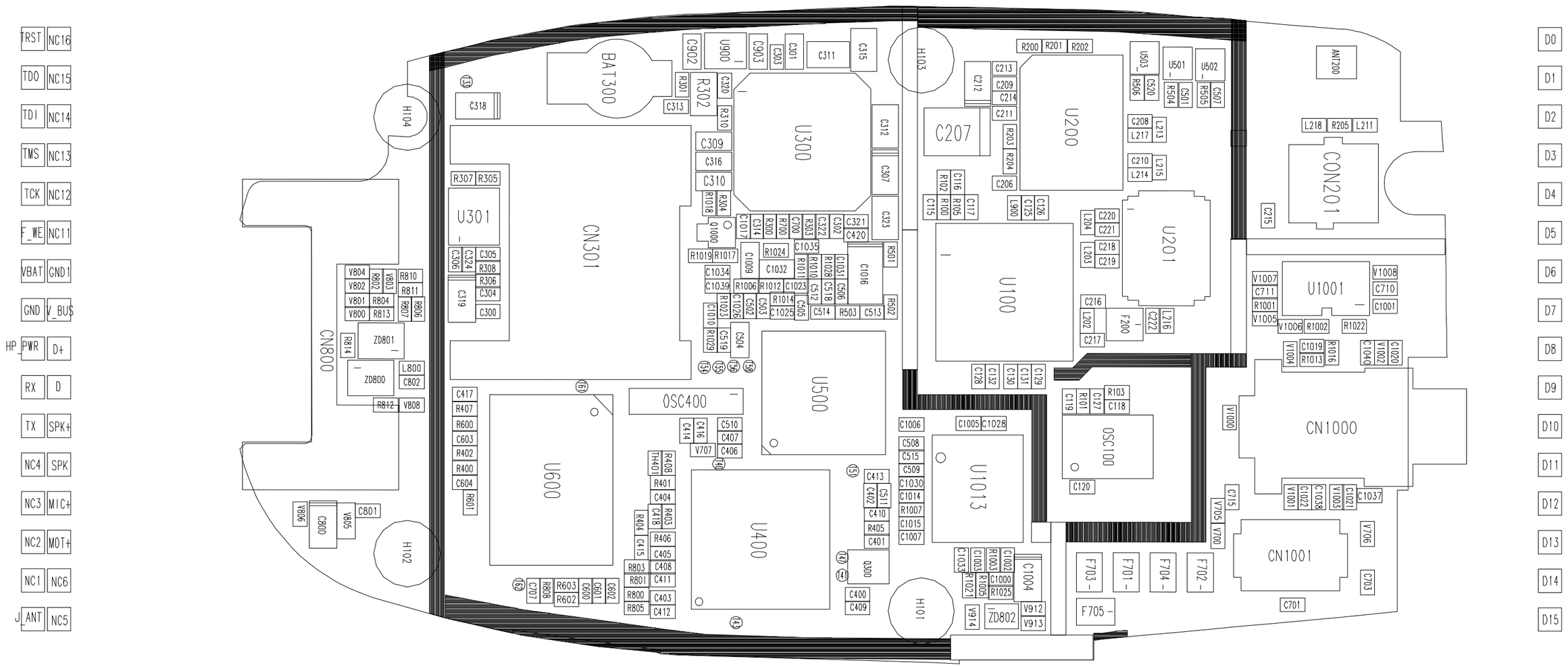


6. SGH-X450 PCB Diagrams

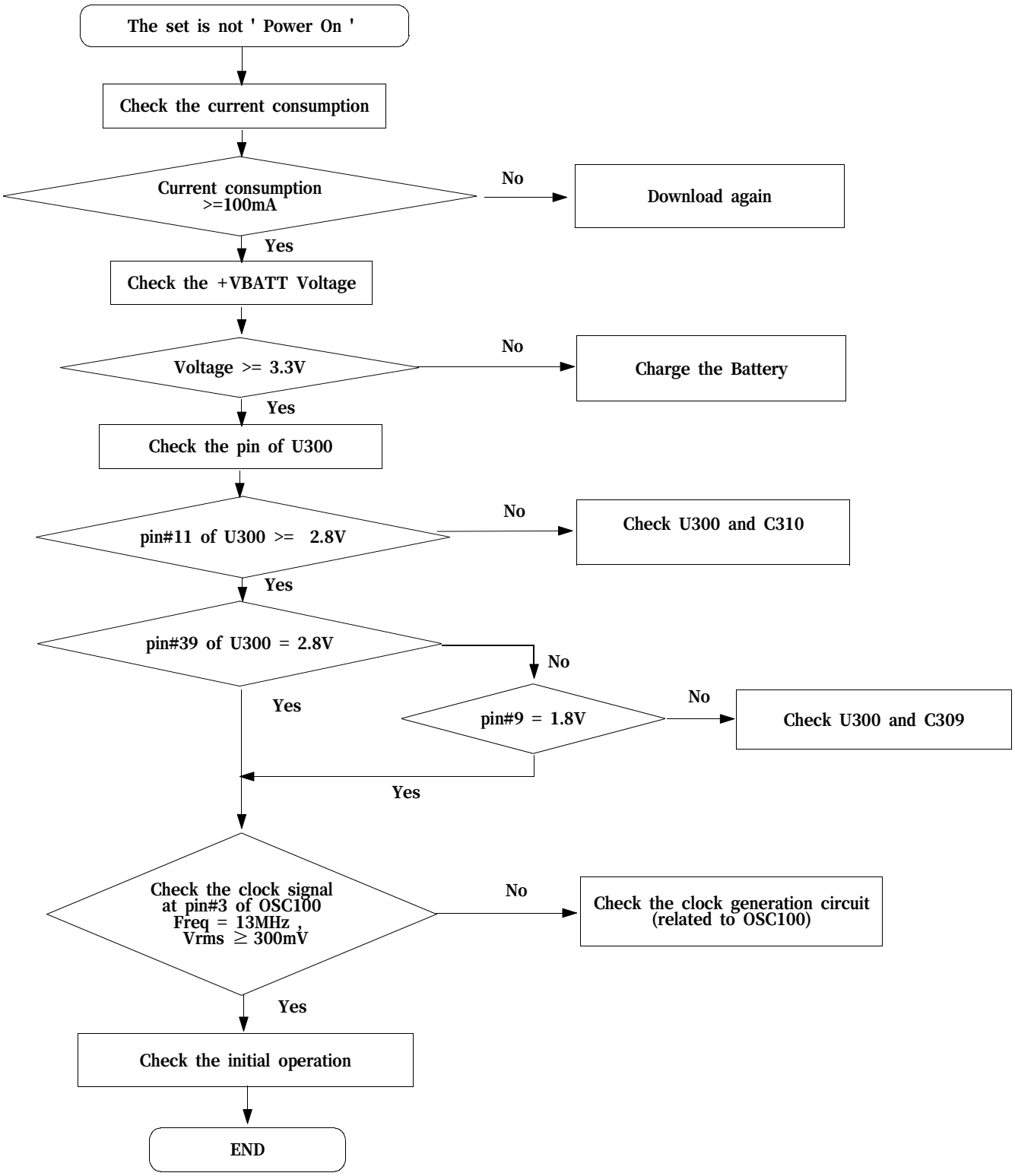
1. Main PCB Top Diagram



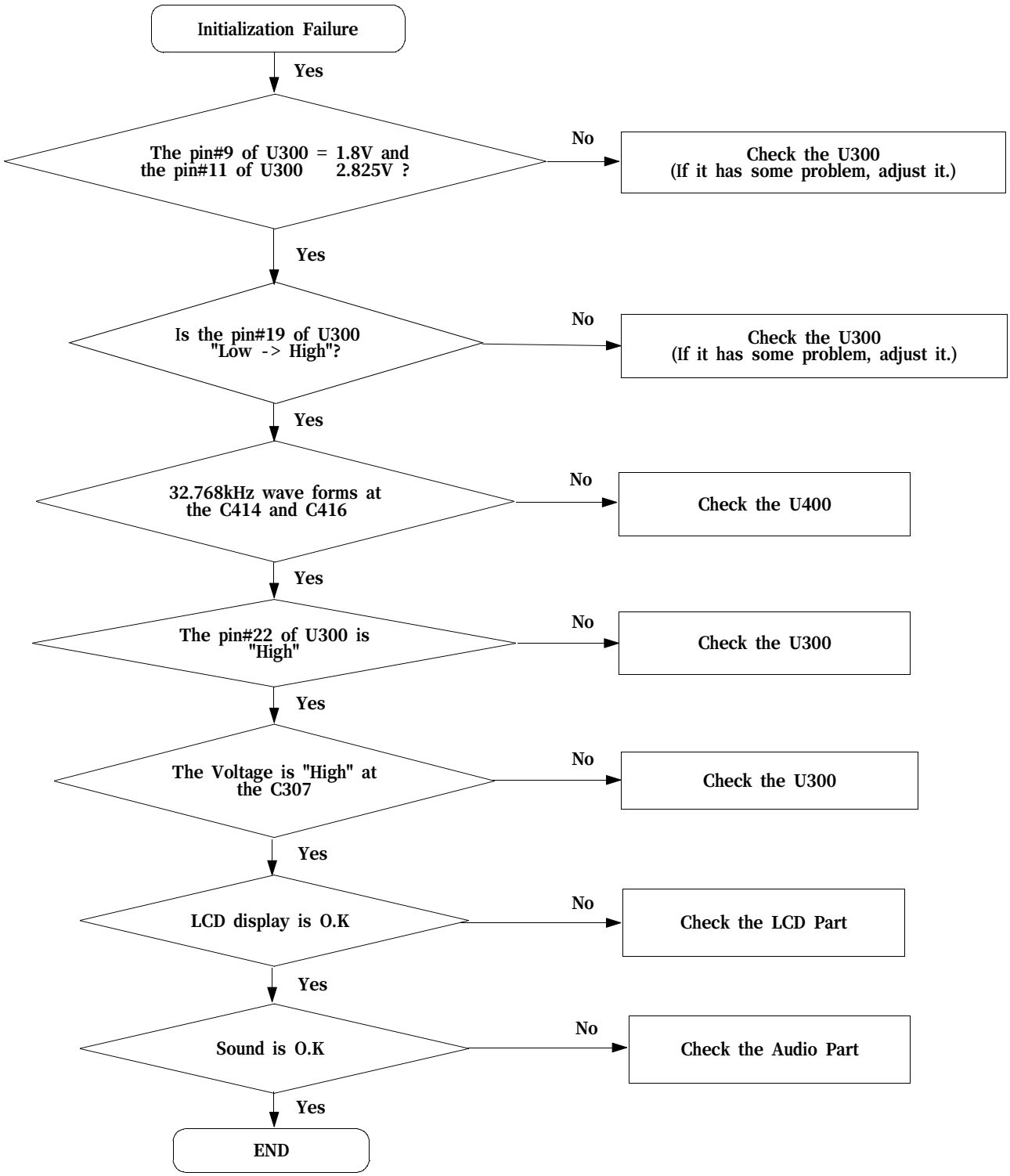
2. Main PCB Bottom Diagram



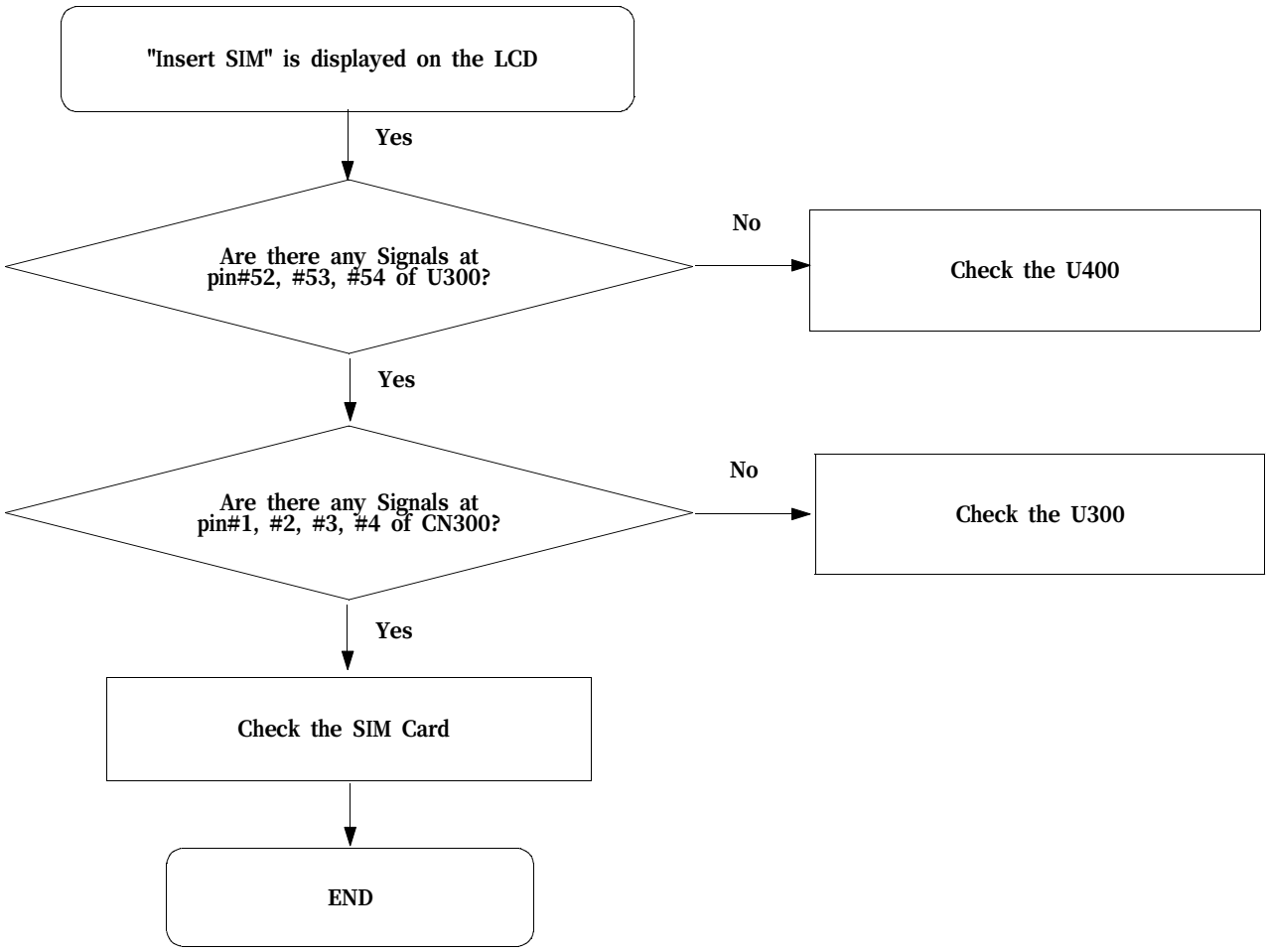
7. SGH-X450 Flow Chart of Troubleshooting



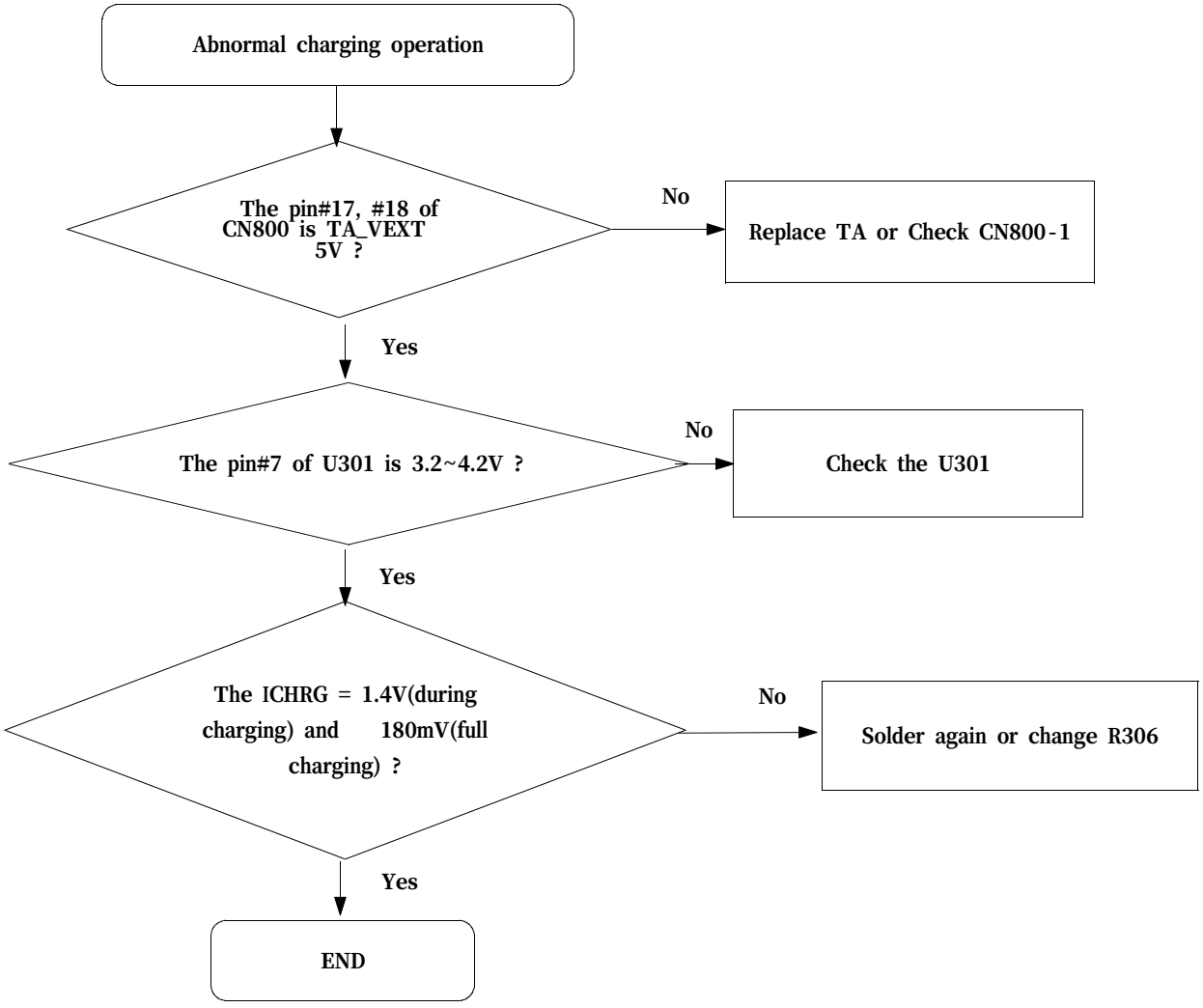
2. Initial

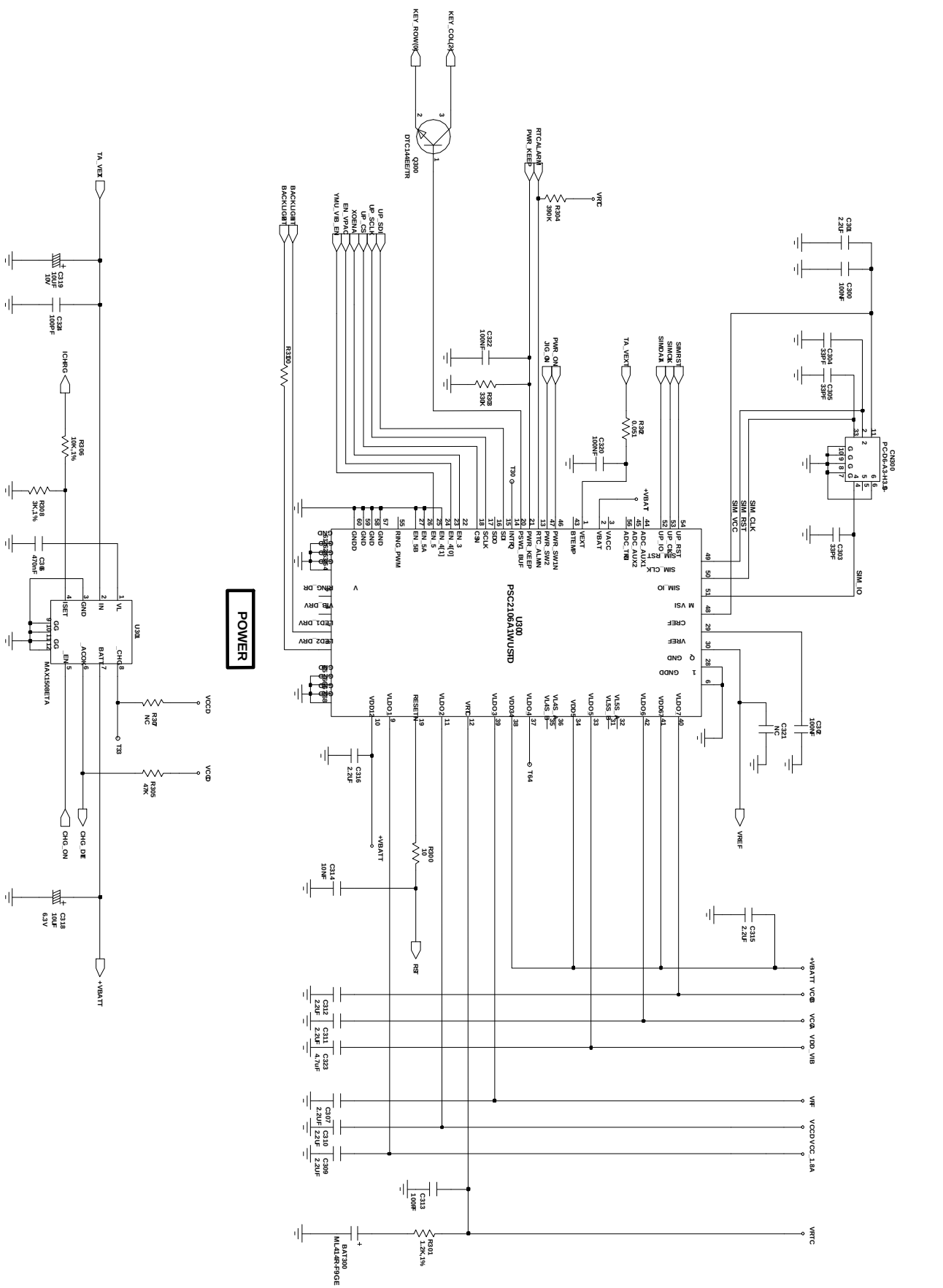


3. SIM Part

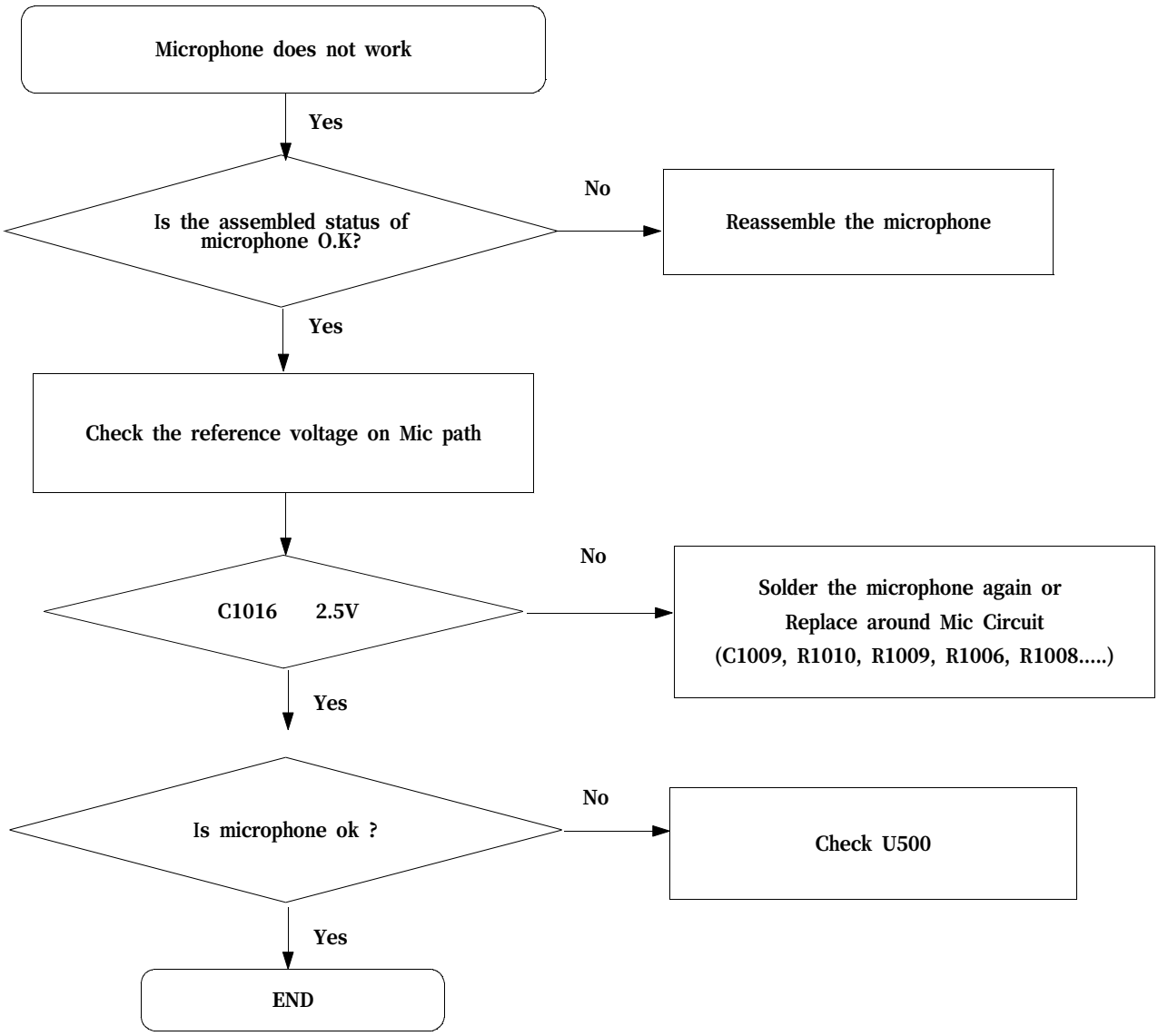


4. Charging Part

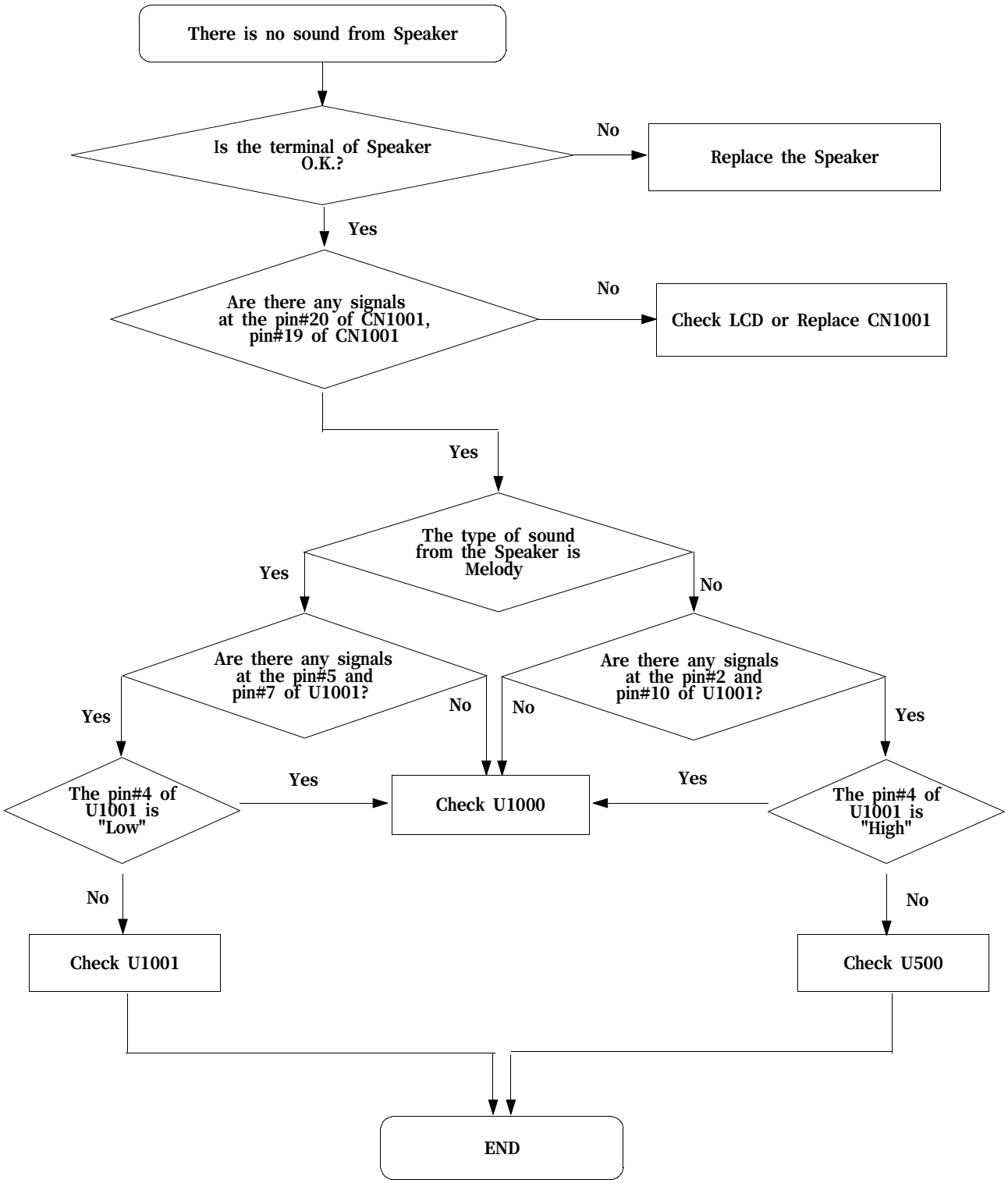


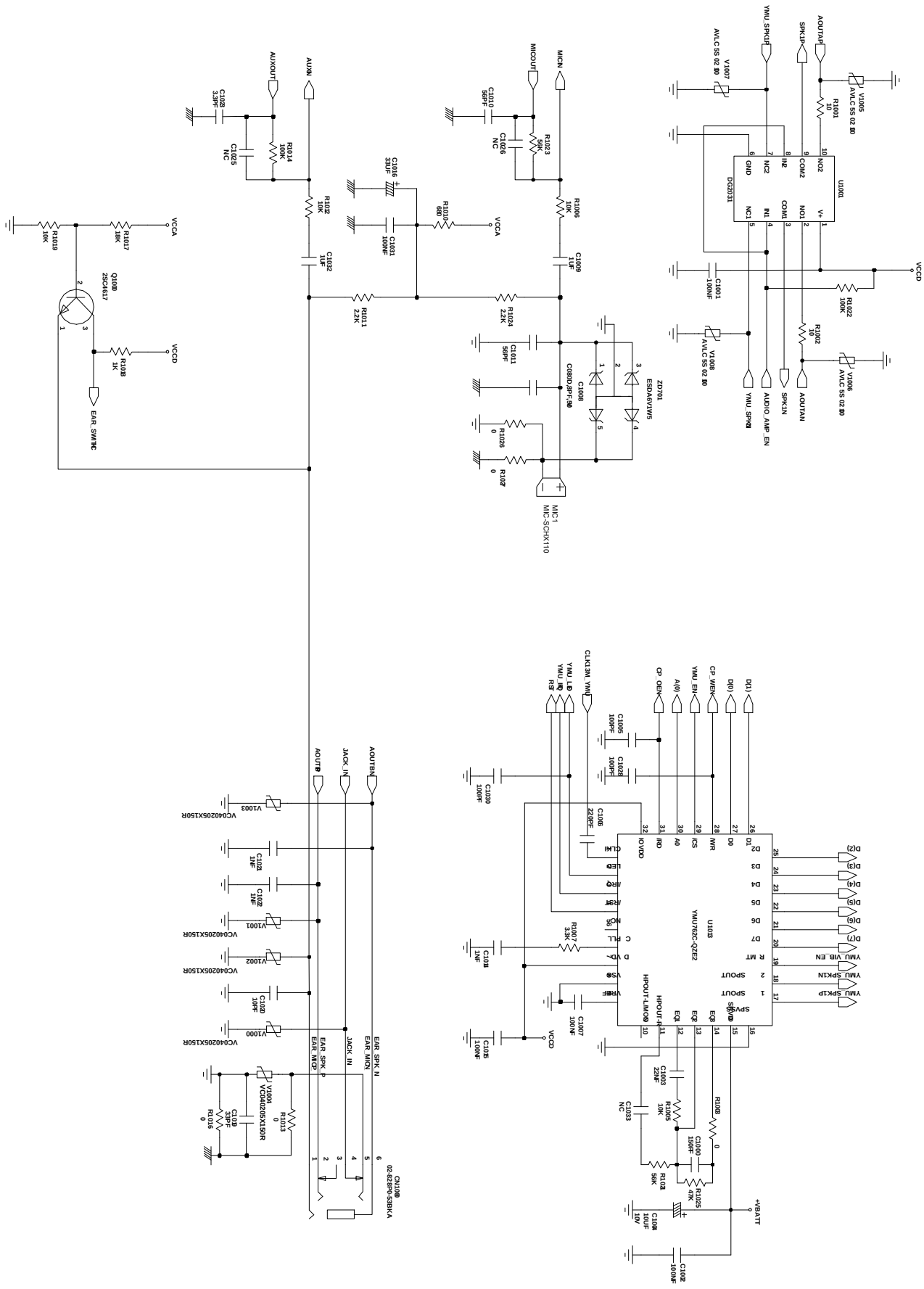


5. Microphone Part

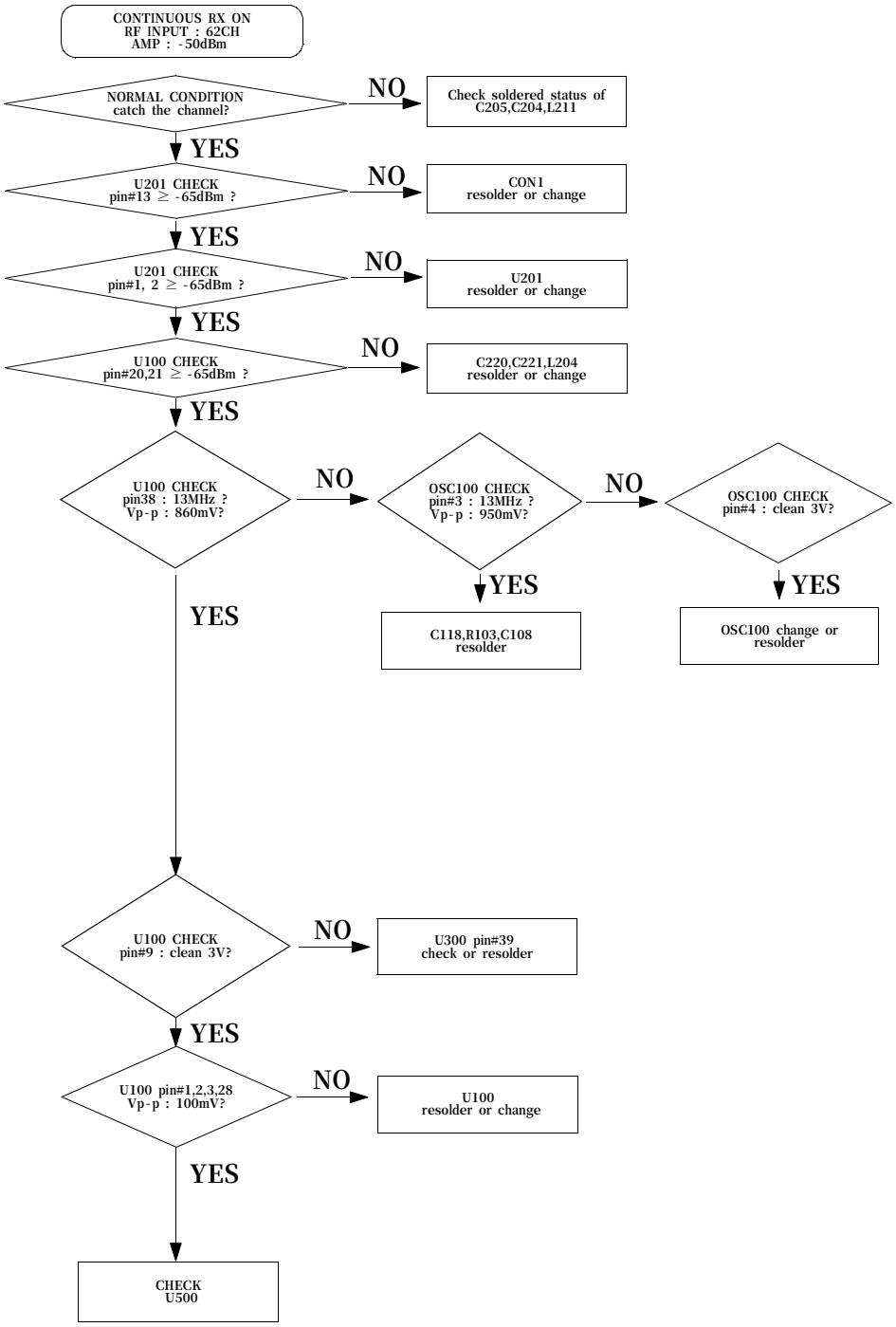


6. Speaker Part

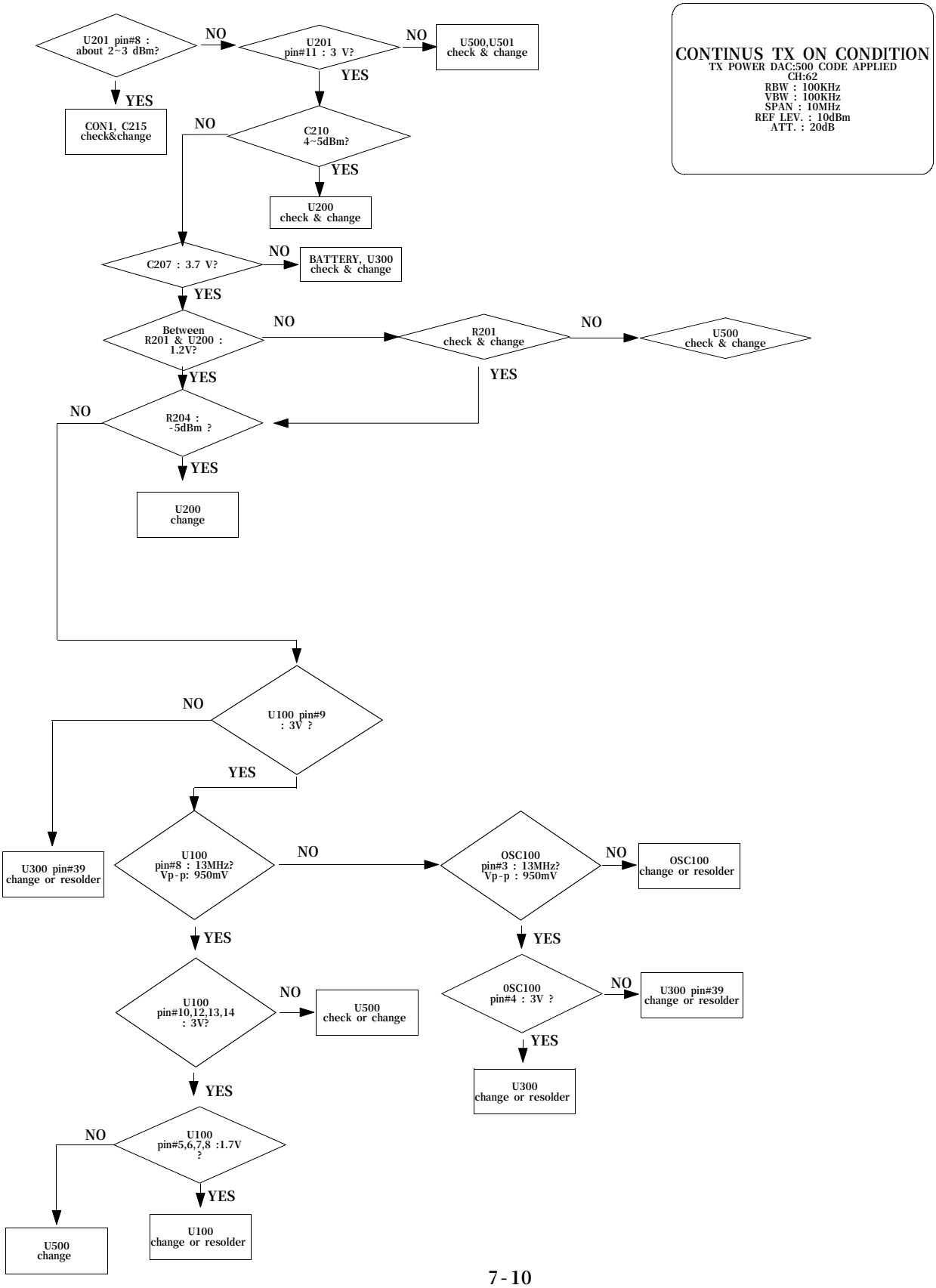




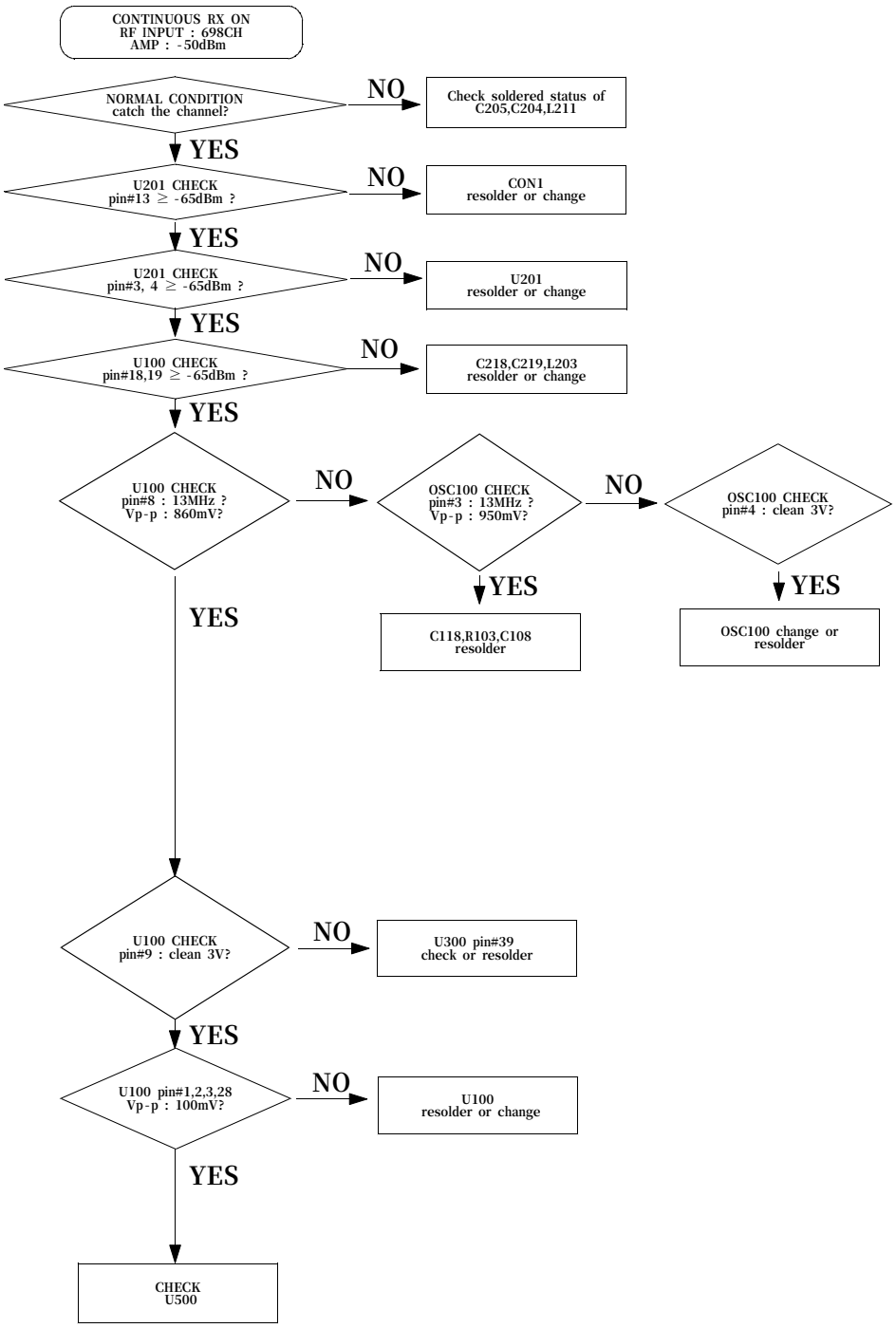
8. EGSM Reciever



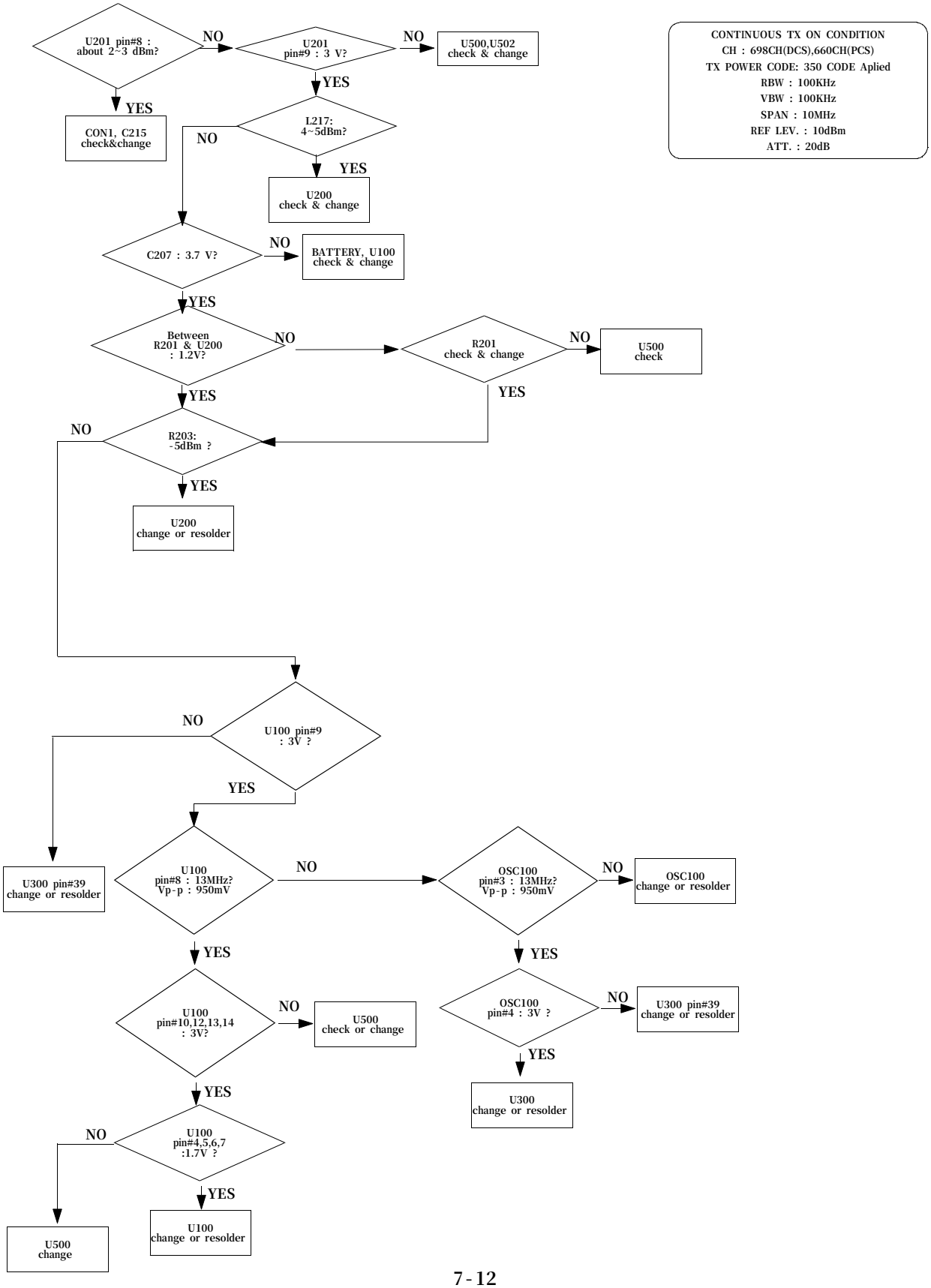
9. EGSM transmitter



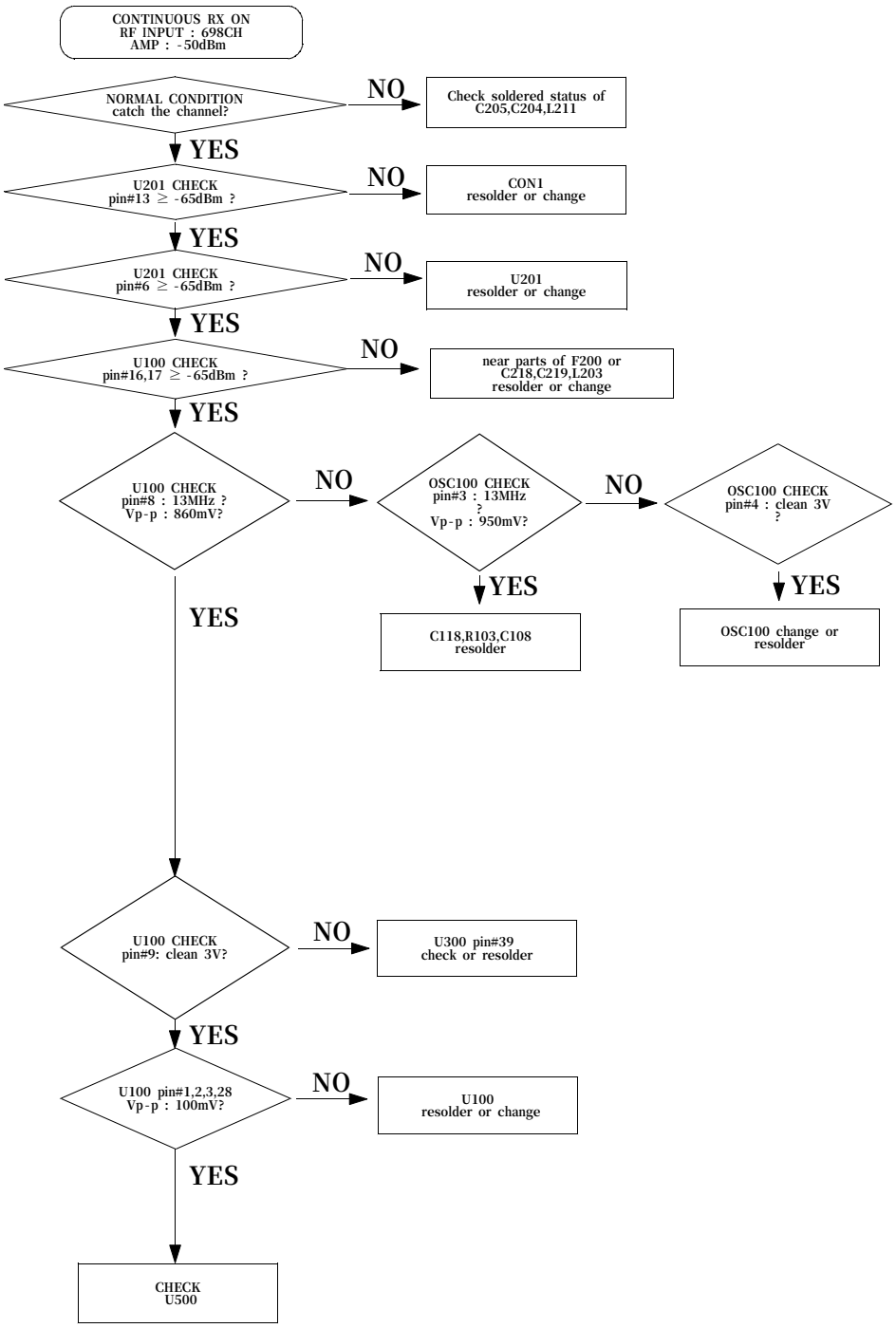
10. DCS Receiver



11. DCS transmitter



10. PCS Receiver



11. PCS transmitter