SAMSUNG

GSM TELEPHONE
SGH-V200

SERVICE Manual

GSM TELEPHONE

CONTENTS

1. SGH-V200 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1	PCS1900
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880	1850~1910 1930~1990
ARFCN range	1~124	0~124 & 975~1023	512~885	512~810
Tx/Rx spacing	45MHz	45MHz	95MHz	80MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm	-100dBm
TDMA Mux	8	8	8	8
Cell Radius	35Km	35Km	2Km	-

2. GSM TX power class

TX Power control level	GSM900
5	33±2 dBm
6	31±2 dBm
7	29±2 dBm
8	27±2 dBm
9	25±2 dBm
10	23±2 dBm
11	21±2 dBm
12	19±2 dBm
13	17±2 dBm
14	15±2 dBm
15	13±2 dBm
16	11±3 dBm
17	9±3dBm
18	7±3 dBm
19	5±3 dBm

TX Power control level	DCS1800
0	30±3 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

TX Power control level	PCS1900
0	30±3 dBm
1	28±3 dBm
2	26±3 dBm
3	24±3 dBm
4	22±3 dBm
5	20±3 dBm
6	18±3 dBm
7	16±3 dBm
8	14±3 dBm
9	12±4 dBm
10	10±4 dBm
11	8±4dBm
12	6±4 dBm
13	4±4 dBm
14	2±5 dBm
15	0±5 dBm

2. SGH-V200 Circuit Description

1. SGH-V200 RF Circuit Description

1) RX PART

1. ASM(U1005) → Switching Tx, Rx path for GSM900, DCS1800 and PCS1900 by logic controlling.
2. ASM Control Logic (U701, U702, U703) → Truth Table

	VC1	VC2	VC3
GSM Tx Mode	H	L	L
DCS / PCS Tx Mode	L	H	L
PCS Rx Mode	L	L	H
GSM / DCS Rx Mode	L	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (C1003,C1004,L1001) → For filtering the frequency band between 925 ~ 960 MHz
- DCS FILTER (C1005,C1006,L1002) → For filtering the frequency band 1805 and 1880 MHz.
- PCS SAW FILTER (F1003) → For filtering the frequency band between 1930 and 1990 MHz

4. TC-VCXO (OSC801)

To generate the 13MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U900 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. Si 4200 (U901)

This chip integrates three differential-input LNAs.

The GSM input supports the E-GSM, DCS input supports the DCS1800, PCS input supports the PCS1900. The LNA inputs are matched to the 200 ohm differential output SAW filters through eternal LC matching network.

Image-reject mixer downconverts the RF signal to a 100 KHz intermediate frequency(IF) with the RFLO from SI4133T frequency synthesizer. The RFLO frequency is between 1737.8 ~ 1989.9 MHz.

The Mixer output is amplified with an analog programmable gain amplifier(PGA), which is controlled by AGAIN.

The quadrature IF signal is digitized with high resolution A/D converts (ADC).

6. Si 4201 (U900)

The SI4201 down-converts the ADC output to baseband with a digital 100 KHz quadrature LO signal. Digital decimation and IIR filters perform channel selection to remove blocking and reference interface signals.

After channel selection, the digital output is scaled with a digital PGA, which is controlled with the DGAIN. DACs drive a differential analog signal onto the RXIP, RXIN, RXQP, RXQN pins to interface to standard analog-input baseband IC.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U902 chip.
SI4200 chip generates modulator signal which power level is about 1.5dBm and fed into Power Amplifier(U1008).
The PA output power and power ramping are well controlled by Auto
Power Control circuit. We use offset PLL below

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

2. Baseband Circuit description of SGH-V200

1. PSC2006

1.1. Power Management

Seven low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable boost converter provides support for 1.8V, 3.0V, and 5.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as an LED driver and two call-alert drivers, aid in reducing both board area and system complexity.
A three-wire serial interface unit(SIU) provides access to control and configuration registers. This interface gives a microprocessor full control of the PSC2006 and enables system designers to maximize both standby and talk times. Supervisory functions. including a reset generator, an input voltage monitor, and a thermal monitor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition(low microprocessor voltage, insufficient battery energy, or excessive die temperature).

1.2. Battery Charge Management

A battery charge management block provides fast, efficient charging of a single-cell Li-ion battery. Used in conjunction with a current-limited voltage source and an external PMOS pass transistor, this block safely conditions near-dead cells and provides the option of having fast-charge and top-off controlled internally or by the system's microprocessor.

1.3. Backlight LED Driver

The backlight LED driver is a low-side, programmable current source designed to control the brightness of the keyboard and LCD illumination. The driver is enabled by EN_LED, and its current setting is determined by LED[0:2]. Provided EN_LED is ‘1’, the driver can be programmed to sink from 12.5mA to 100mA in 12.5mA steps. LED_DRV is capable of sinking 100mA at a worst-case maximum output voltage of 0.6V. For efficient use, the LEDs is connected between the battery and the LED_DRV output.

1.4. Vibrator Motor Dirver

The vibrator motor driver is a low-side, programmable voltage source designed to drive a small dc motor that silently alerts the user of an incoming call. The driver is enabled by EN_VIB, and its voltage setting is determined by VIB[0:2]. Provided EN_VIB is a logic 1, the driver can be programmed to maintain a motor voltage of 1.1V to 2.5V in 20mV steps and while sinking up to 100mA. For efficient use, the vibrator motor should be connected between the main battery and the VIB_DRV output.

2. Connector

2-1. LCD Connector

LCD is consisted of main LCD(color 65K STN LCD) and small LCD(4-gray LCD). Chip select signals of EMI part in the trident, CLCD_EN_FO and GLCD_EN_FO, can enable Each LCD. LED_EN_FO signal enables white LED of main LCD and EL_EN_FO signal enables EL of small LCD. These two signals are from IO part of the DSP in the trident. RST signal from 2006 initiates the initial process of the LCD.

16-bit data lines(D(0)_FO~D(15)_FO) transfers data and commands to LCD through emi_filter. Data and commands use A(2)_FO signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So CP_WEN_FO signal is used to write data or commands to LCD. Power signals for LCD are V_bat and V_ccd.

SPK1P and SPK1N from CSP1093 are used for audio speaker. And VIB_EN_FO from enables the motor.

2-2. JTAG Connector

Trident has two JTAG ports which are for ARM core and DSP core(DSP16000). So this system has two port connector for these ports. Pins' initials for ARM core are 'CP_' and pins' initials for DSP core are 'DSP_'. CP_TDI and DSP_TDI signal are used for input of data. CP_TDO and DSP_TDO signals are used for the output of the data. CP_TCK and DSP_TCK signals are used for clock because JTAG communication is a synchronous. CP_TMS and DSP_TMS signals are test mode signals. The difference between these is the RESET_INT signal which is for ARM core RESET.

2-3. IRDA

This system uses IRDA module, HSDL_3201, HP's. This has signals, IRDA_EN(enable signal), IRDA_RX(input data) and IRDA_TX(output data). These signals are connected to PPI of trident. It uses two power signals. V_ccd is used for circuit and V_bat is used for LED.

2-4. Keypad connector

This is consisted of key interface pins among PPI in the trident, KEY_ROW[0~4] and KEY_COL[0~4]. These signals compose the matrix. Result of matrix informs the key status to key interface in the trident. Some pins are connected to varistor for ESD protection. And power on/off key is seperated from the matrix. So power on/off signal is connected with PSC2006 to enable PSC2006. SVC_GREEN, SVC_RED and SVC_BLUE are from OCTL of CSP1093. These signals decide the color of LED, service indicator. Eighteen key LED use the V_bat supply voltage. These are connected to BACKLIGHT signal in the PSC2006. This signal enables LEDs with current control. FLIP_SNS informs the status of folder (open or closed) to the trident. This uses the hall effect IC, A3210ELH. A magnet under main LCD enables A3210ELH which is on the key FPCB.

2-5. EMI Filter

This system uses the EMI filter, KNA32200-W3 to protect noise from LCD part. Some control signals are connected to LCD without EMI filter.

3. IF connetor

It is 24-pin connector, and uses 18-pin at present. They are designed to use SDS, DEBUG, DLC-DETECT, JIG_ON, VEXT, VTEST, VF, CF, VBAT and GND. They connected to power supply IC, microprocessor and signal processor IC.

4. Audio

AOUTAP from CSP1093 is connected to the main speaker. AOUTAN is connected to the speaker via audio-amp. AOUTBN and AOUTBP are connected to the ear-mic speaker via ear-jack. MICIN and MICOUT are connected to the main MIC. And AUXIN and AUXOUT are connected to the Ear-mic.

YMU762MA3 is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decorder that are included in this device.

As a synthesis, YMU762MA3 is equipped 16 voices with differenttones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects. Since the play data of YMU762MA3 are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexiblysupport application such as incoming call melody music distribution service. The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU759 includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibartor and a circuit for controlling LEDs synchornous with music.

For the headphone, it is provided with a stereophonic output terminal.

For the purpose of enabling YMU762MA3 to demonstarte its full capablities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible wiht multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for traning karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762MA3 directly interprets and plays blocks relevant to systhesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

5. Memory

This system uses SHARP's memory, LRS1395. It is consisted of 128M bits flash memory and16M bits SRAM. It has 16 bit data line, D[0~15] which is connected to trident, LCD or CSP1093. It has 22 bit address lines, A[1~22]. They are connected too. CP_CSROMEN and CO_CSROM2EN signals, chip select signals in the trident enable two memories. They use 3 volt supply voltage, V_ccd and 1.8 volt supply voltage, Vcc_1.8a in the PSC2006. During wrting process, CP_WEN is low and it enables writing process to flash memory and SRAM. During reading process, CP_OEN is low and it output information which is located at the address from the trident in the flash memory or SRAM to data lines. Each chip select signals in the trident select memory among 2 flash memory and 2 SRAM. Reading or writing procedure is processed after CP_WEN or CP_OEN is enabled. Memories use FLASH_RESET, which is buffered signal of RESET from PSC2006, for ESD protection. A[0] signal enables lower byte of SRAM and UPPER_BYTE signal enables higher byte of SRAM.

6. Trident

Trident is consisted of ARM core and DSP core. It has 20K*16bits RAM 144K*16bits ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of timer, one bit input/output unit(BIO), JTAG, EMI and HDS(Hardware Development System). ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), peripheral bridge, PPI, SSI(Synchronous Serial Interface), ACC(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface. DSP_AB[0~8], address lines of DSP core and DSP_DB[0~15], data lines of DSP core are connected to CSP1093. A[0~20], address lines of ARM core and D[0~15], data lines of ARM core are connected to memory, LCD and YMU759. ICP(Interprocessor Communication Port) controls the communication between ARM core and DSP core. CSROMEN, CSRAMEN and CS1N to CS4N in the ARM core are connected to each memory. WEN and OEN control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, YMU, Ear-jack, Ear-mic and CSP1093, need the compatible process.

Some PPI pins has many special functions. CP_KB[0~9] receive the status from key FPCB and are used for the communicatios using IRDA(IRDA_RX/TX/EN) and data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR). And UP_CS/SCLK/SDI, control signals for PSC2006 are outputted through PPI pins. It has signal port for charging(CHG_DET, CHG_STAT0), SIM_RESET and FLIP_SNS with which we knows open.closed status of folder. It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It recieves 13MHz clock in CKI pin from external TCXO and receives 32.768KHz clock from X1RTC. ADC(Analog to Digital Convertor) part receives the status of temperature, battery type and battery voltage. And control signals(DSP_INT, DSP_IO and DSP_RWN) for DSP core are used. It enables main LCD and small LCD with DSP IP pins.

7. CSP1093

CSP1093 integrates the timing and control functions for GSM 2+ mobile application with the ADC and DAC functions. The CSP1093 interfaces to the trident, via a 16-bit parallel interface. It serves as the interface that connects a DSP to the RF circuitry in a GSM 2+ mobile telephone. DSP can load 148 bits of burst data into CSP1093's internal register, and program CSP1093's event timing and control register with the exact time to send the burst. When the timing portion of the event timing and control register matches the internal quarter-bit counter and internal frame counter, the 148 bits in the internal register are GMSK modulated according to GSM 2+ standards. The resulting phase information is translated into I and Q differential output voltages that can be connected directly to an RF modulator at the TXOP and TXON pins. The DSP is notified when the transmission is completed. For receiving baseband data, a DSP can program CSP1093's event timing and control register with the exact time to start receiving I and Q samples through TXIP and TXIN pins. When that time is reached, the control portion of the event timing and control register will start the baseband receive section converting I and Q sample pairs. The samples are stored in a double-buffered register until the register contains 32 sample pairs. CSP1093 then notifies the DSP which has ample time to read the information out before the next 32 sample pairs are stored. The voice band ADC converter issues an interrupt to the DSP whenever it finishes converting a 16-bit PCM word. The DSP then reads the new input sample and simultaneously loads the voice band output DAC converter with a new PCM output word. The voice band output can be connected directly to a speaker via AOUTAN and AOUTAP pins and be connected to a Ear-mic speaker via AOUTBN and AOUTBP pins.

8. X-TAL(13MHz)

This system uses the 13MHz TCXO, TCO-9141B, Toyocom. AFC control signal form CSP1093 controls frequency from 13MHz x-tal. It generates the clock frequency. This clock is inverted through NOT gate, TC7S04FU and is connected to CSP1093. 13MHz clock for YMU759 uses a not-inverted clock. Clock for RF parts uses same type.

9.Camera DSP(LC99704B)

- This chipset is MCP product that combines the CCD Driver with on-chip booster circuit and analogue/digital mixed-signal processing IC.
  The booster circuit generate the supply voltages required for CCD drive.
  Cameras can use either a +2.8V or +3.0V or +3.3V only power supply system.
  The analogue / digital mixed-signal processing IC that integrates the signal-processing functions required in a CCD digital camera and a rich set of addtional functions on a single chip. Although the CDS(correlated dual sampling) and AGC circuit required for analog processing and the clamp circuit required for A/D conversion are normally povided on circuits, as well as an A/D converter, on a single chip.
  Additionally, it also includes the pulse generator circuits required for CCD drive, the logic circuits for the electronics iris, and the digital signal-processing circuits required to create the digital YUV signal output. This device can take advantage of the features of these digital signal-processing functions to provide auto white balance, automatic dropout detection and correction, mirror image output, and a single line of memory to provide flexibility in the external interface.
  This device assumes an internal master clock frequency in the range 16 ~27 MHz.
  Normally , either an external clock with that frequency is provided, or else a master clock oscillator circuit is constructed using the built-in oscillator inverter circuit.
  And this is also possible to control the CCD drive internal and enternal.

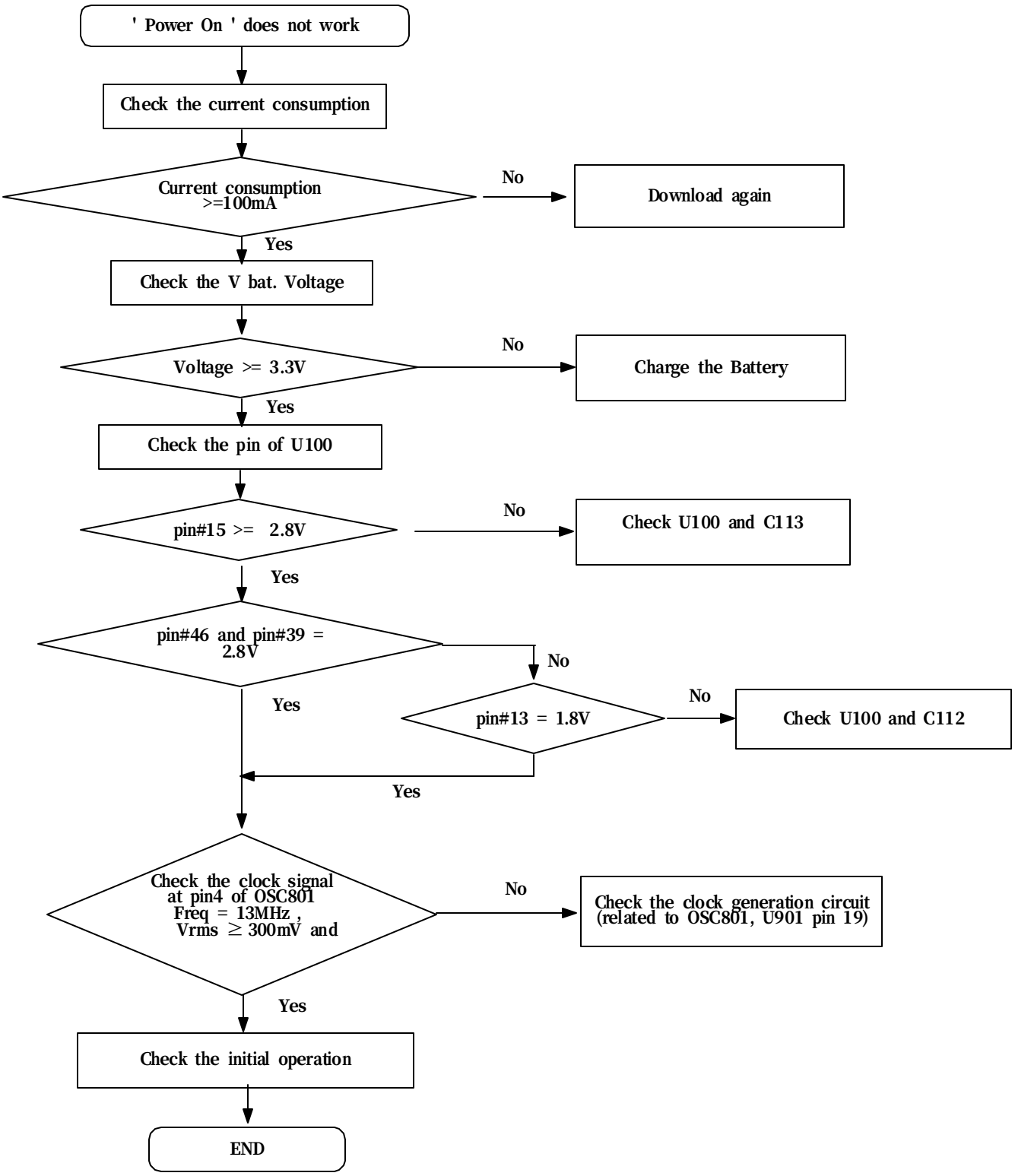
10. Camera ASIC(SSH 275)

This ASIC interfaces between CCD and LCD, and this chip compresses and expands input pictures from CCD with JPEG format.

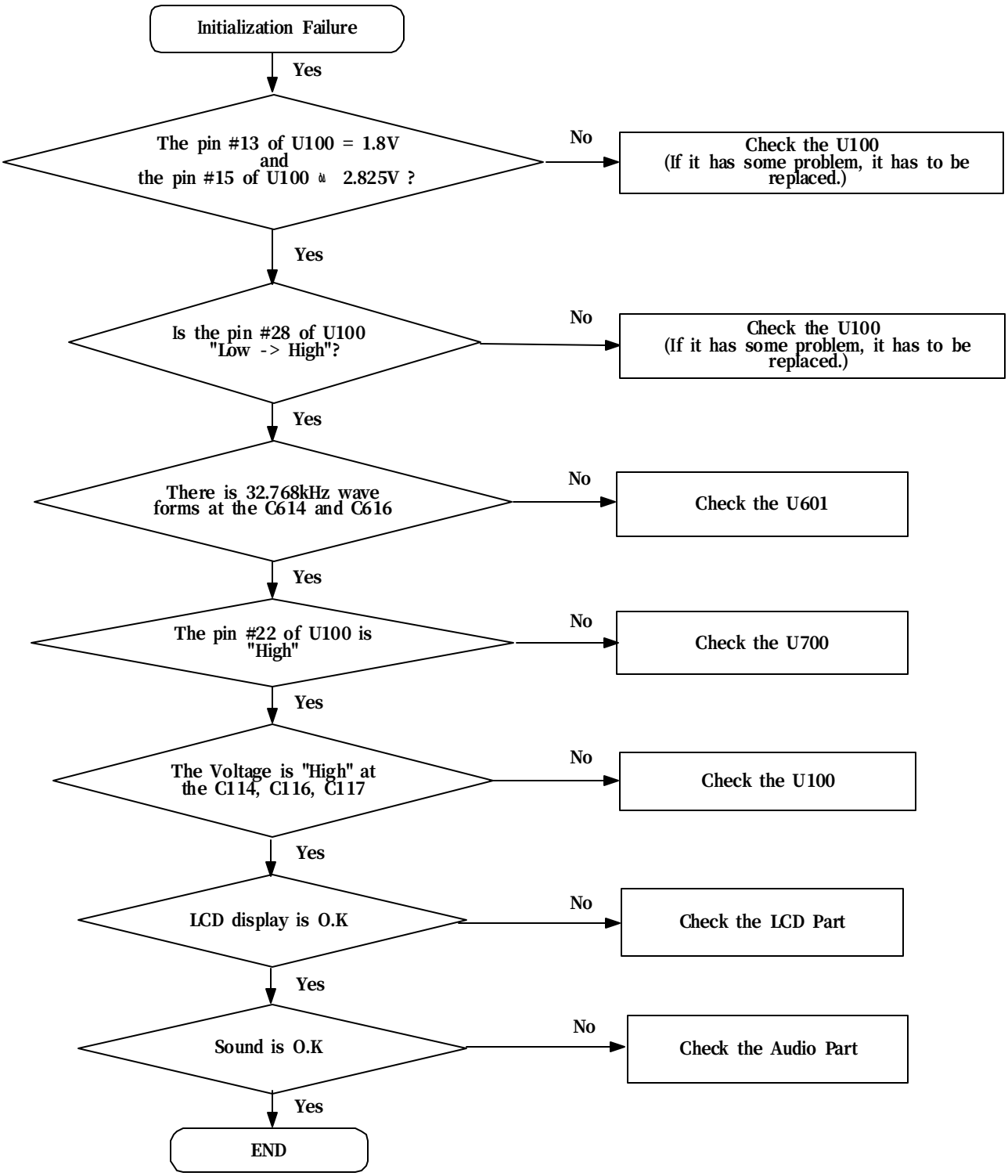
- CCD I/F : YUV422(16 bit) format, CIF fixed size.
  System clock providing CCD module (13.5 MHz) and Dot clock providing CCD module (13.5 MHz).
- CPU I/F : Accessible to JPEG controller, a control register including, JPEG code buffer, and a thumbnail picture buffer.
  Direct access to LCD controller by switching buses.
- LCD I/F : Support LCD controller.
  Accessible by switching 2 masters of the Host CPU or ASIC picture processing .
  Output format from ASIC is RGB565.
- I2C I/F : I2C master for CCD module control equipped.
  CCD module is accessible from CPU wiithout paying attention to I2C, as in the case of a normal register write/read.
- JPEG codec : YUV422 picture data is compressed to JPEG code, and JPEG code data is expanded to YUV422 picture data.
- Clock system : As for ASIC, 27 MHz clock input from outside is the main clock.
  2-divided 13.5 MHz is used as CCD module main clock output, dot clock output to CCD module, and ASIC inner clock

7. SGH-V200 Flow Chart of Troubleshooting

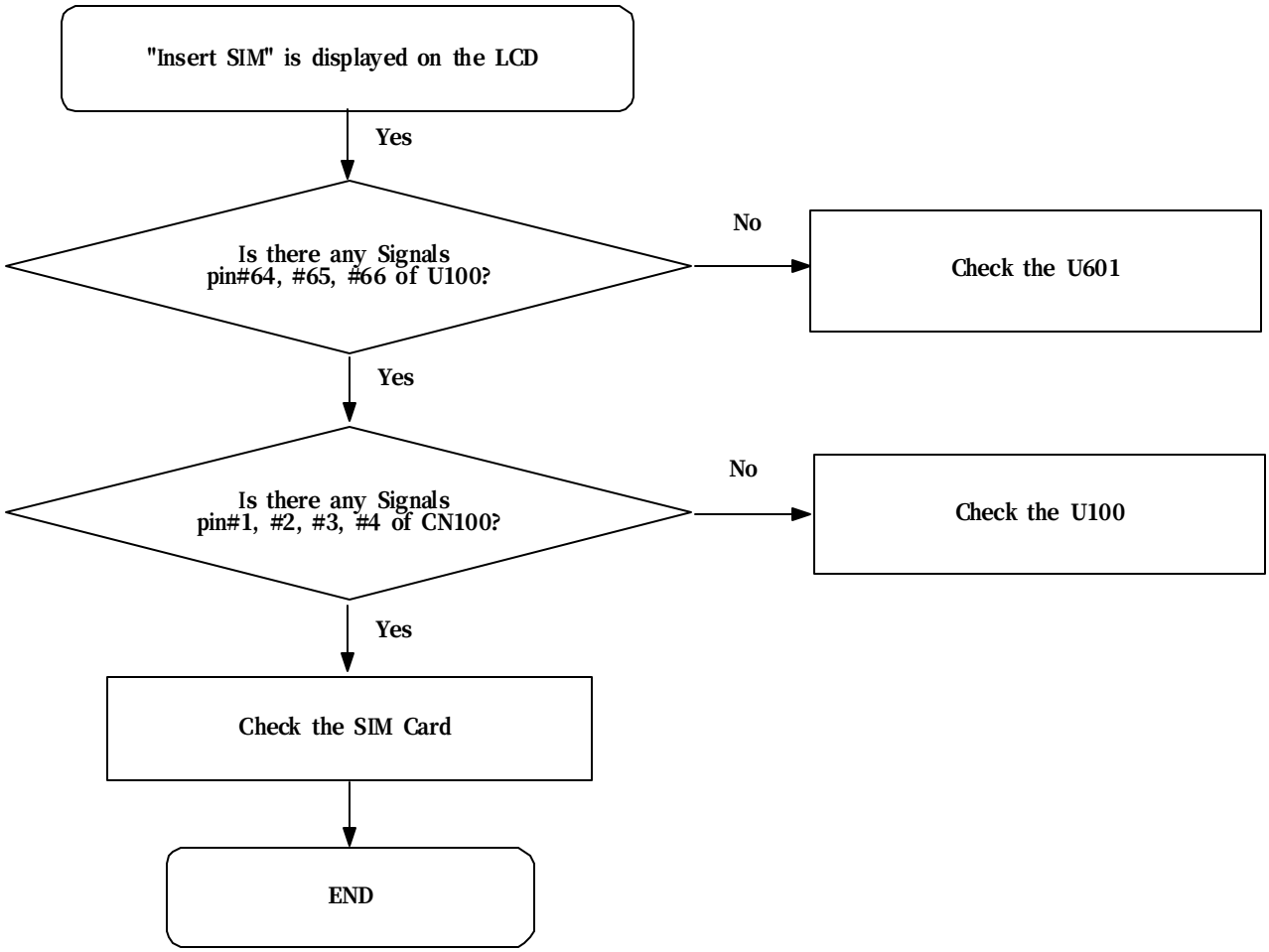
1. Power On



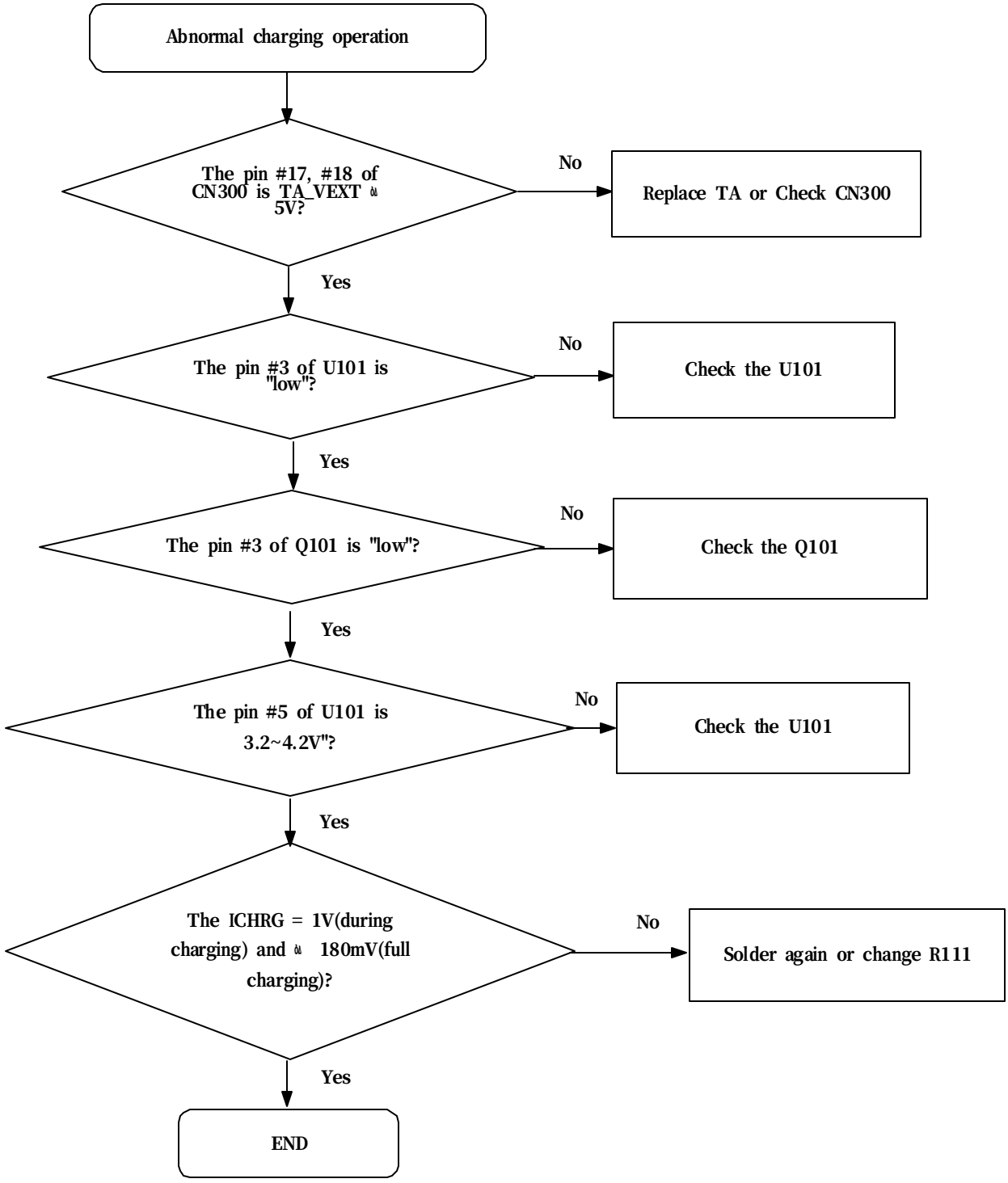
2. Initial

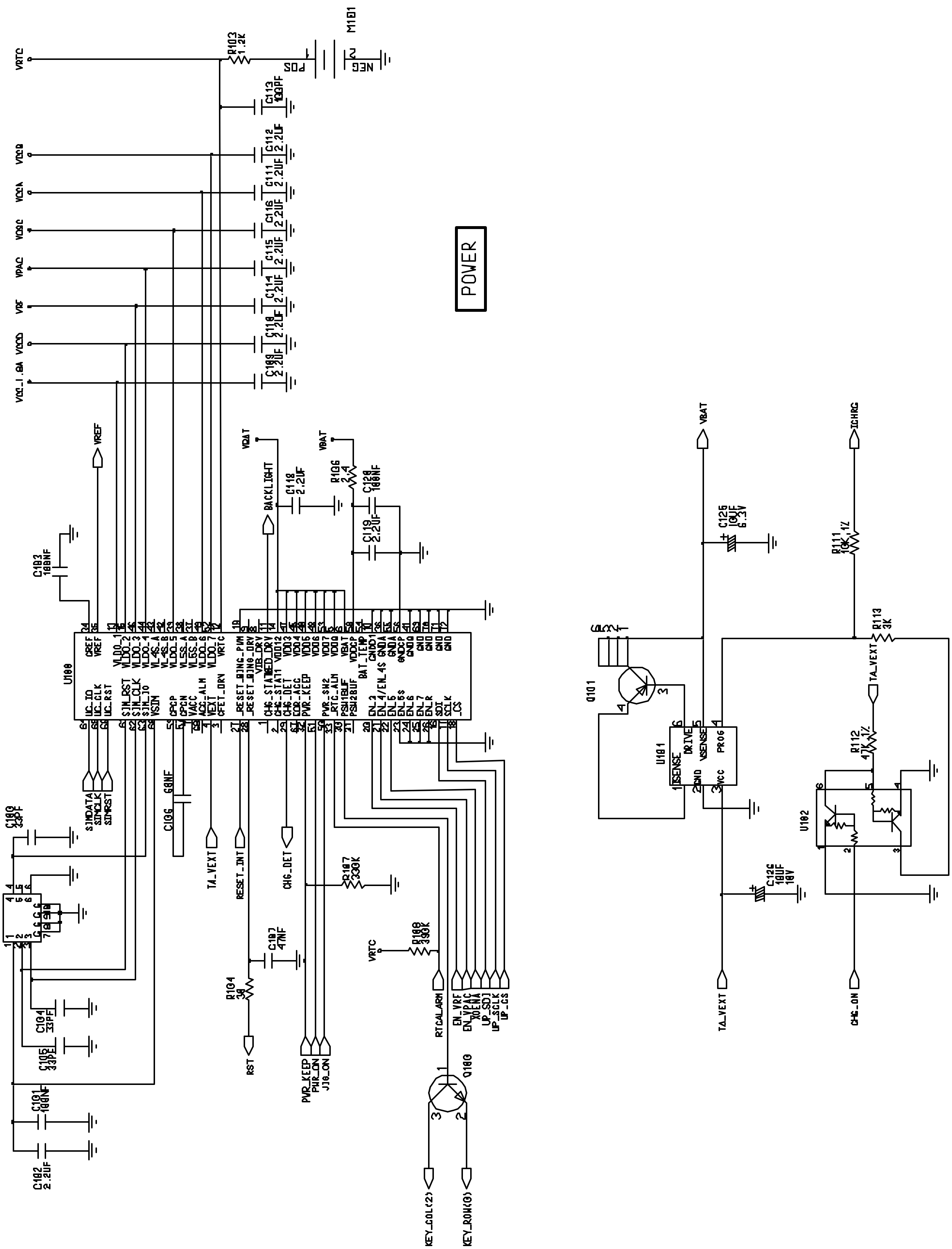

Initialization Failure
Yes
The pin #13 of U100 = 1.8V
and
the pin #15 of U100 = 2.825V ?
No
Check the U100
(If it has some problem, it has to be replaced.)
Yes
Is the pin #28 of U100
"Low -> High"?
No
Check the U100
(If it has some problem, it has to be replaced.)
Yes
There is 32.768kHz wave
forms at the C614 and C616
No
Check the U601
Yes
The pin #22 of U100 is
"High"
No
Check the U700
Yes
The Voltage is "High" at
the C114, C116, C117
No
Check the U100
Yes
LCD display is O.K
No
Check the LCD Part
Yes
Sound is O.K
No
Check the Audio Part
Yes
END

3. Sim Part

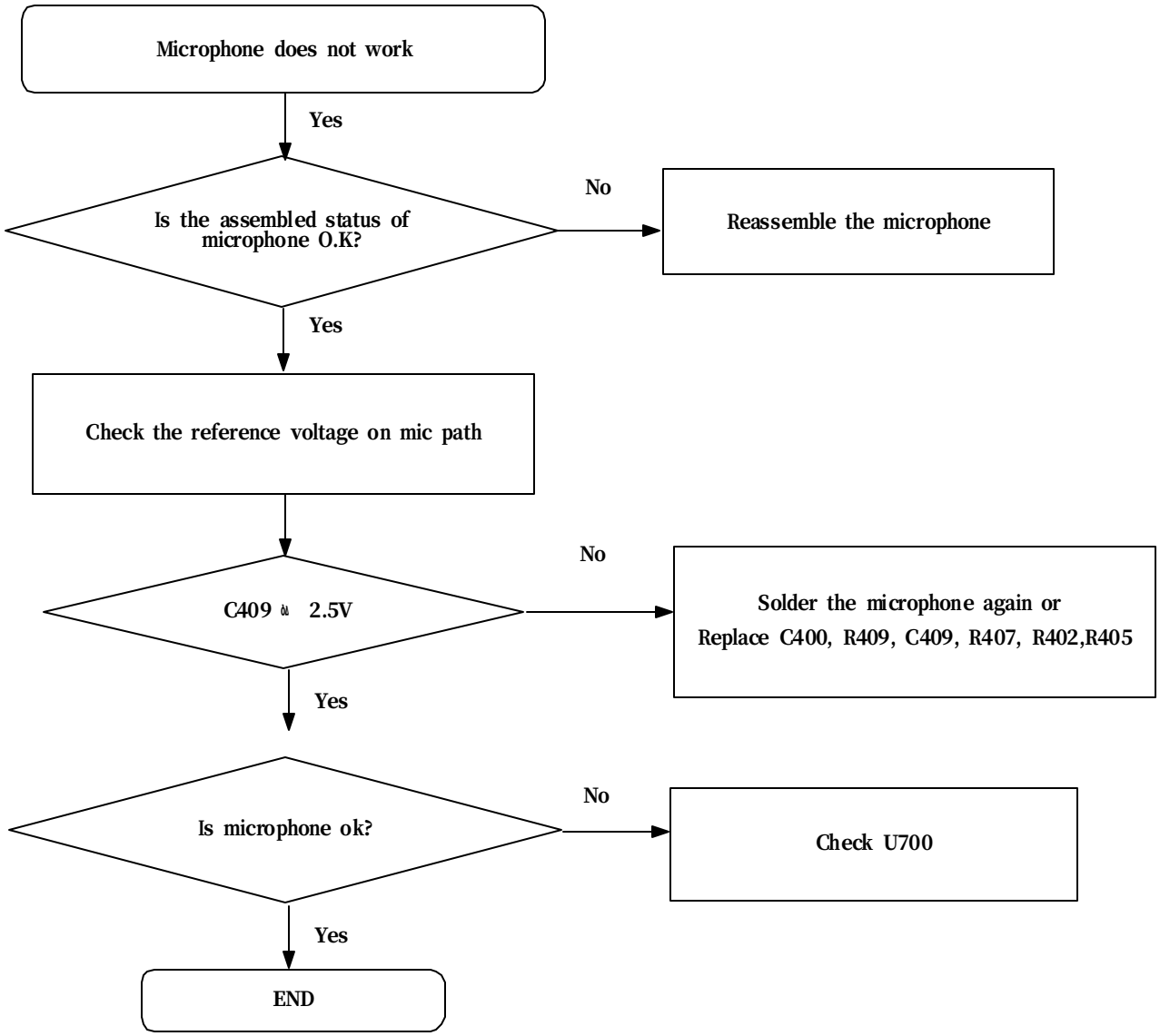

"Insert SIM" is displayed on the LCD
Yes
Is there any Signals pin#64, #65, #66 of U100?
No
Check the U601
Yes
Is there any Signals pin#1, #2, #3, #4 of CN100?
No
Check the U100
Yes
Check the SIM Card
END

4. Charging Part

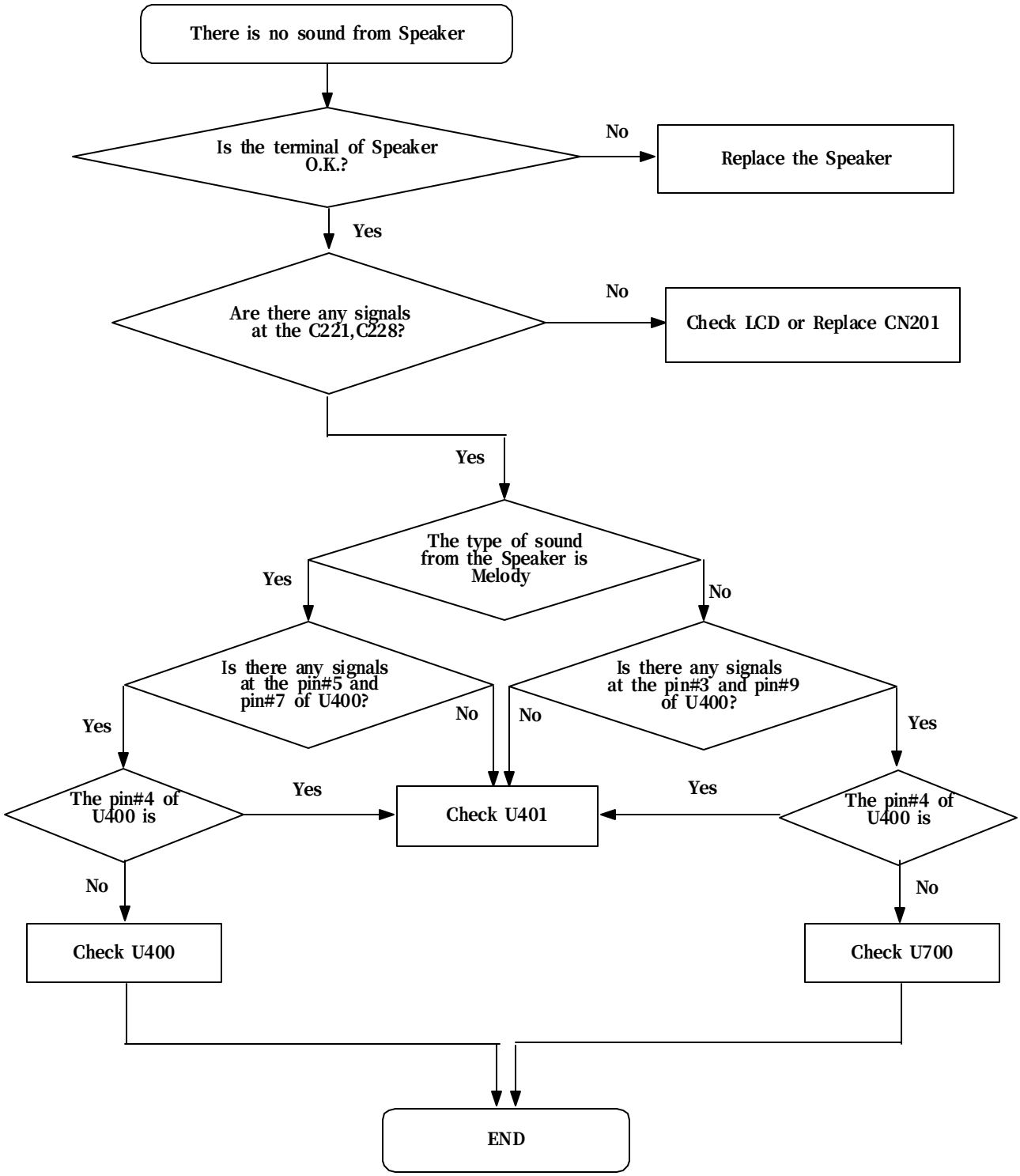


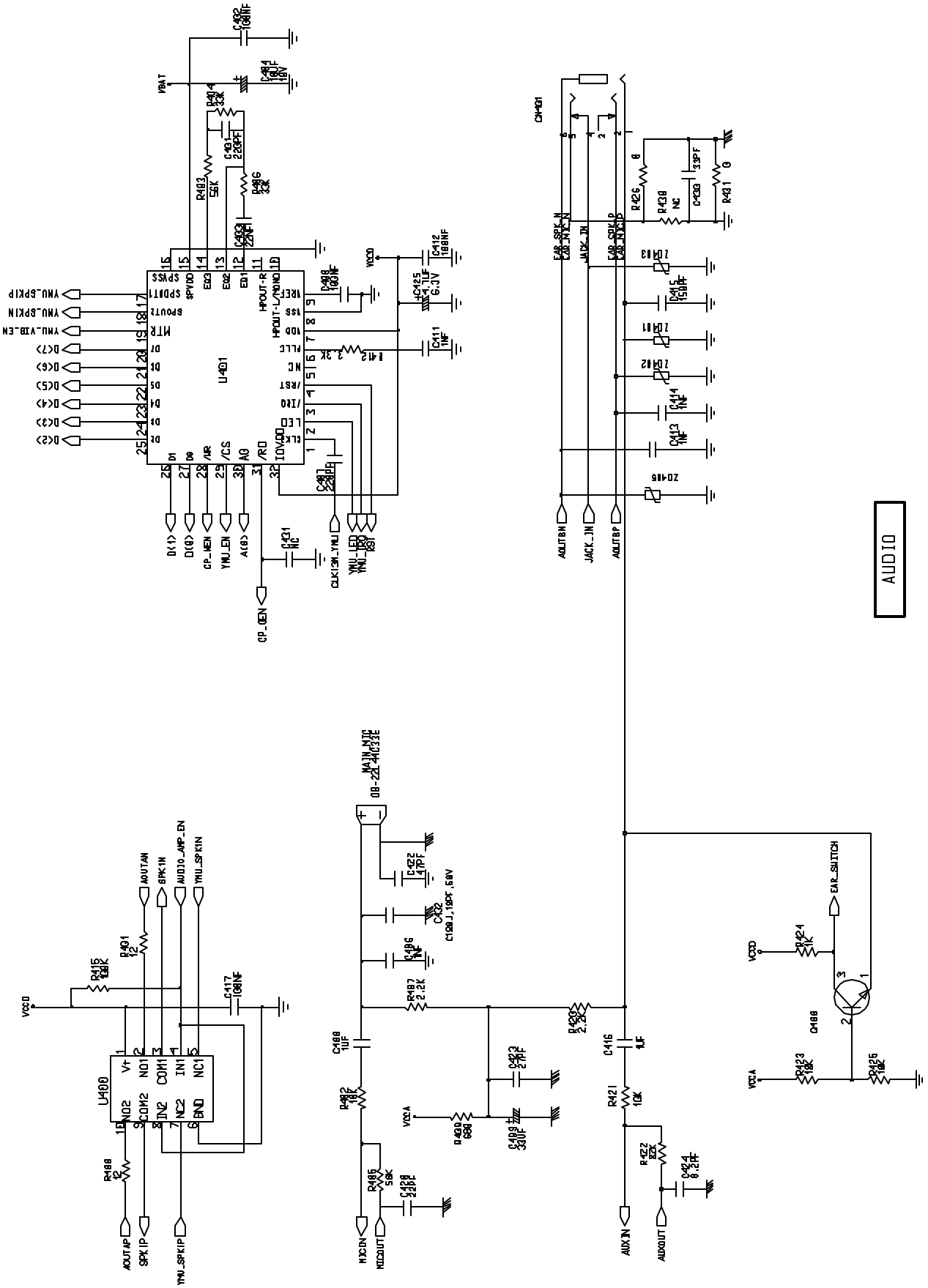

POWER

5. Microphone Part

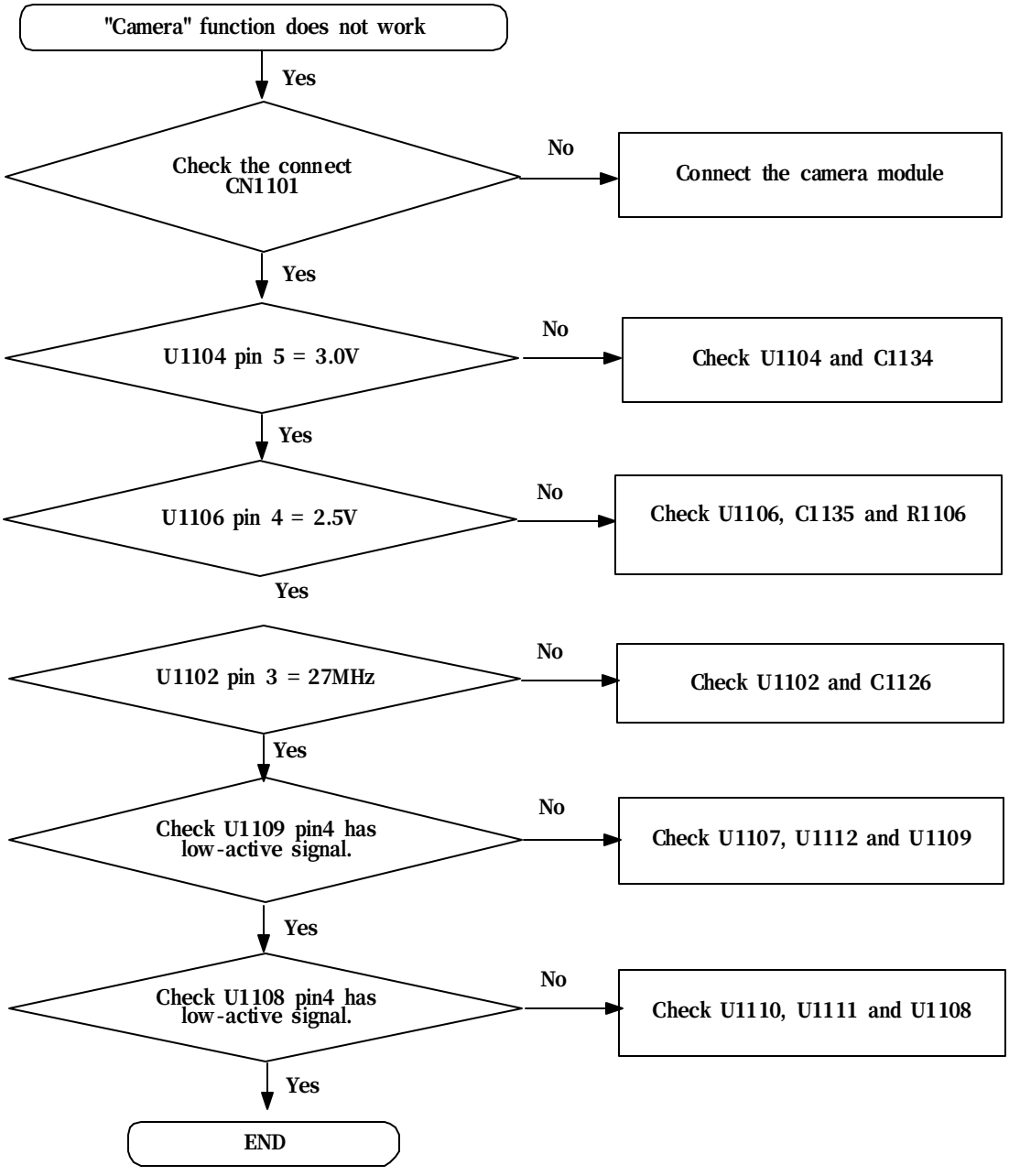


6. Speaker Part

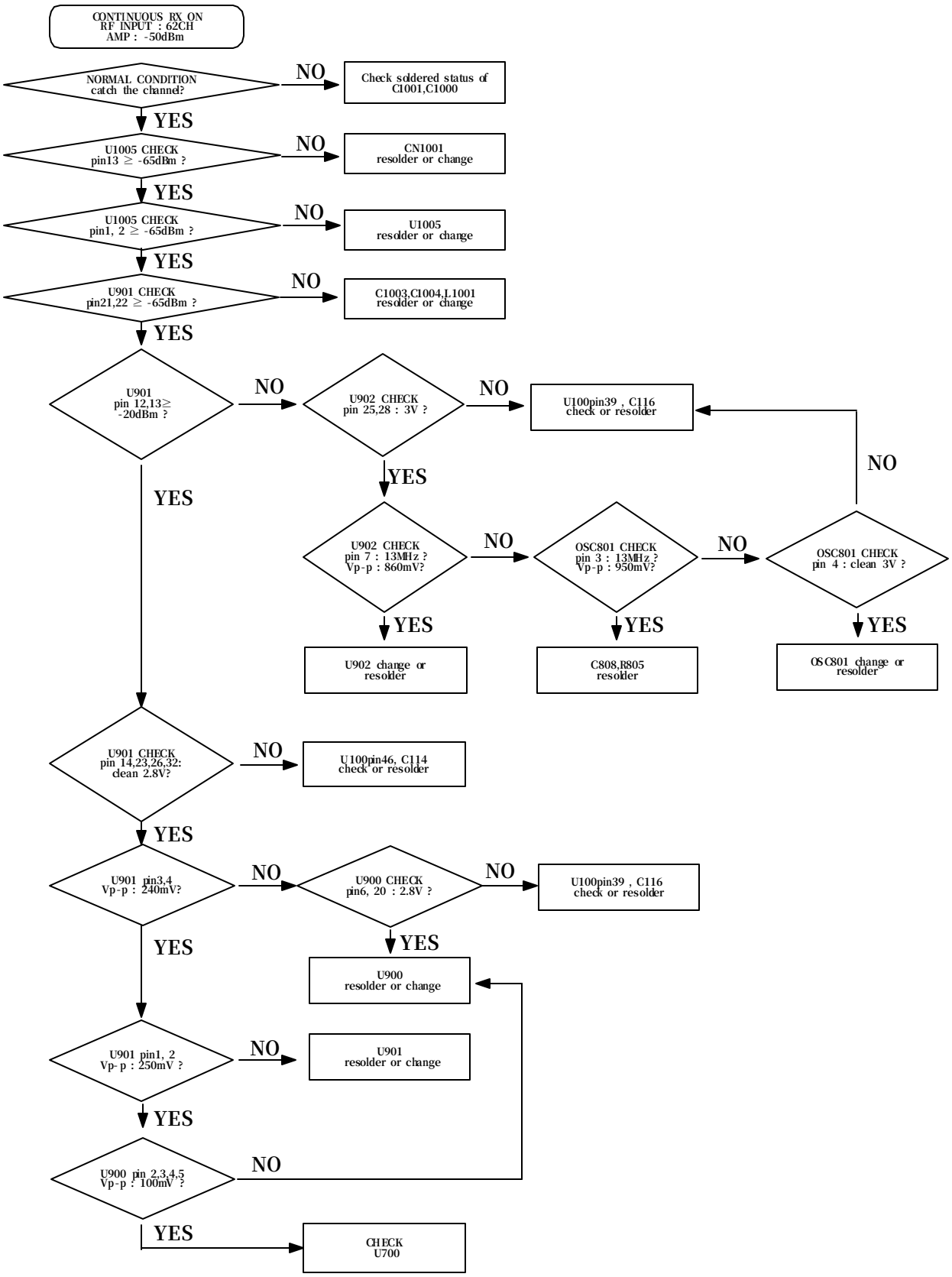



AUDIO
U400
U401
CN401
VBAT
VCCD
VCCA
MAIN_MIC
EAR_SWITCH
AUDIO_AMP_EN
YMU_SPKIN
SPK_IP
YMU_SPKIP
AUDTAN
AUDTBN
AUDTBP
JACK_IN
AUXIN
AUXOUT
MICIN
MICOUT
CP_MEN
CP_CEN
YMU_EN
YMU_LED
CLK13M_YMU

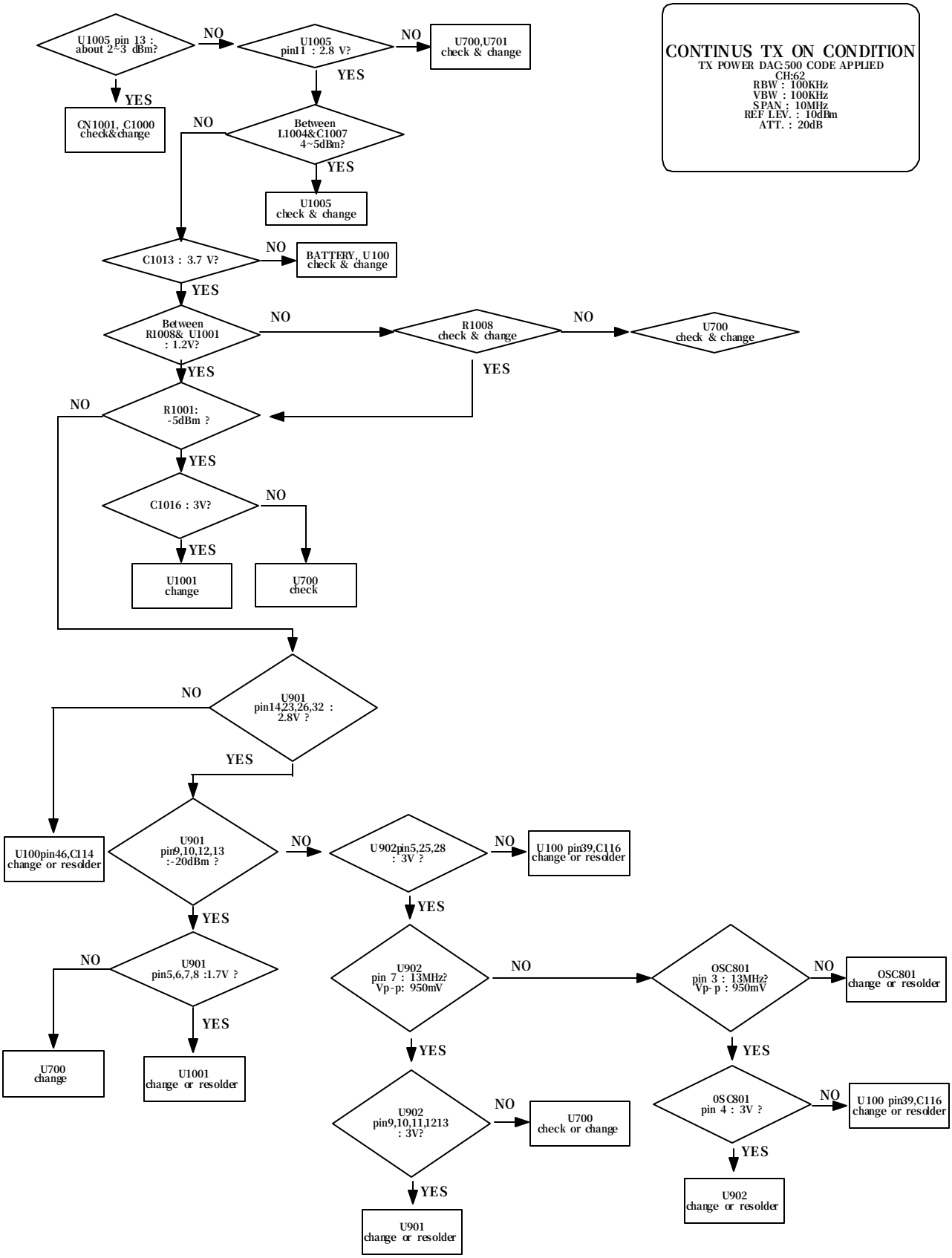
7. Camera part



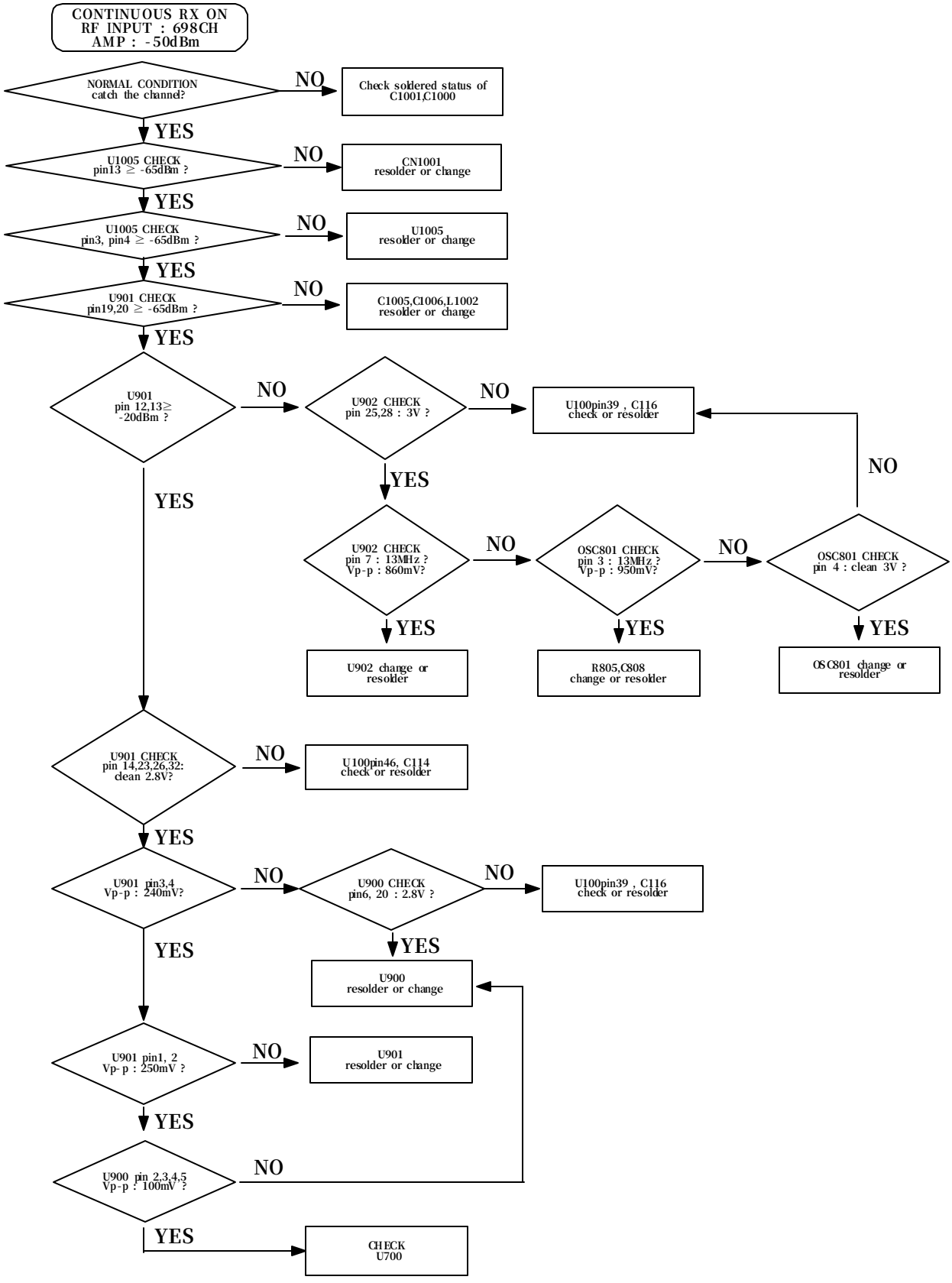
8. EGSM Reciever



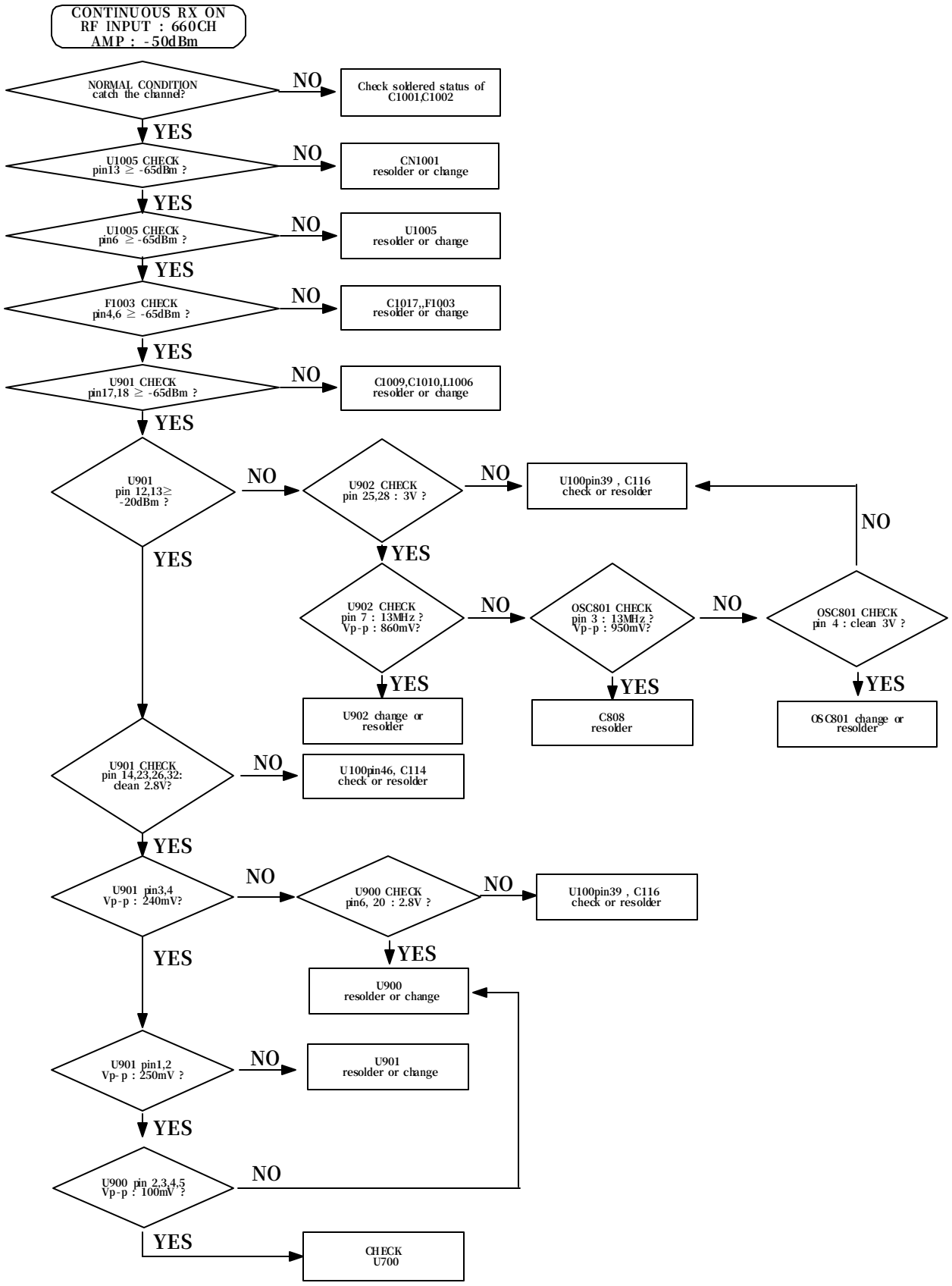
9. EGSM transmitter



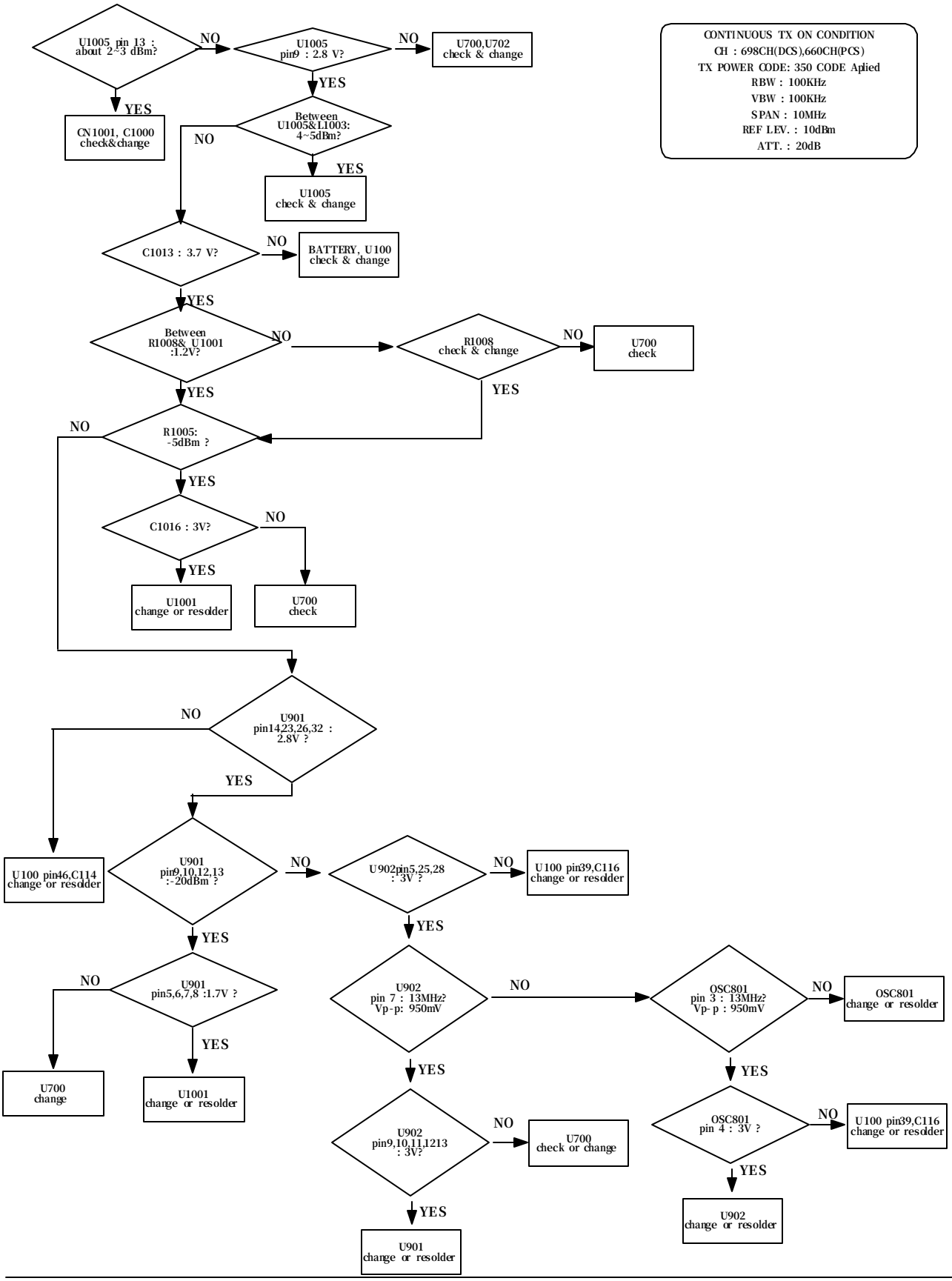
10. DCS Reciever

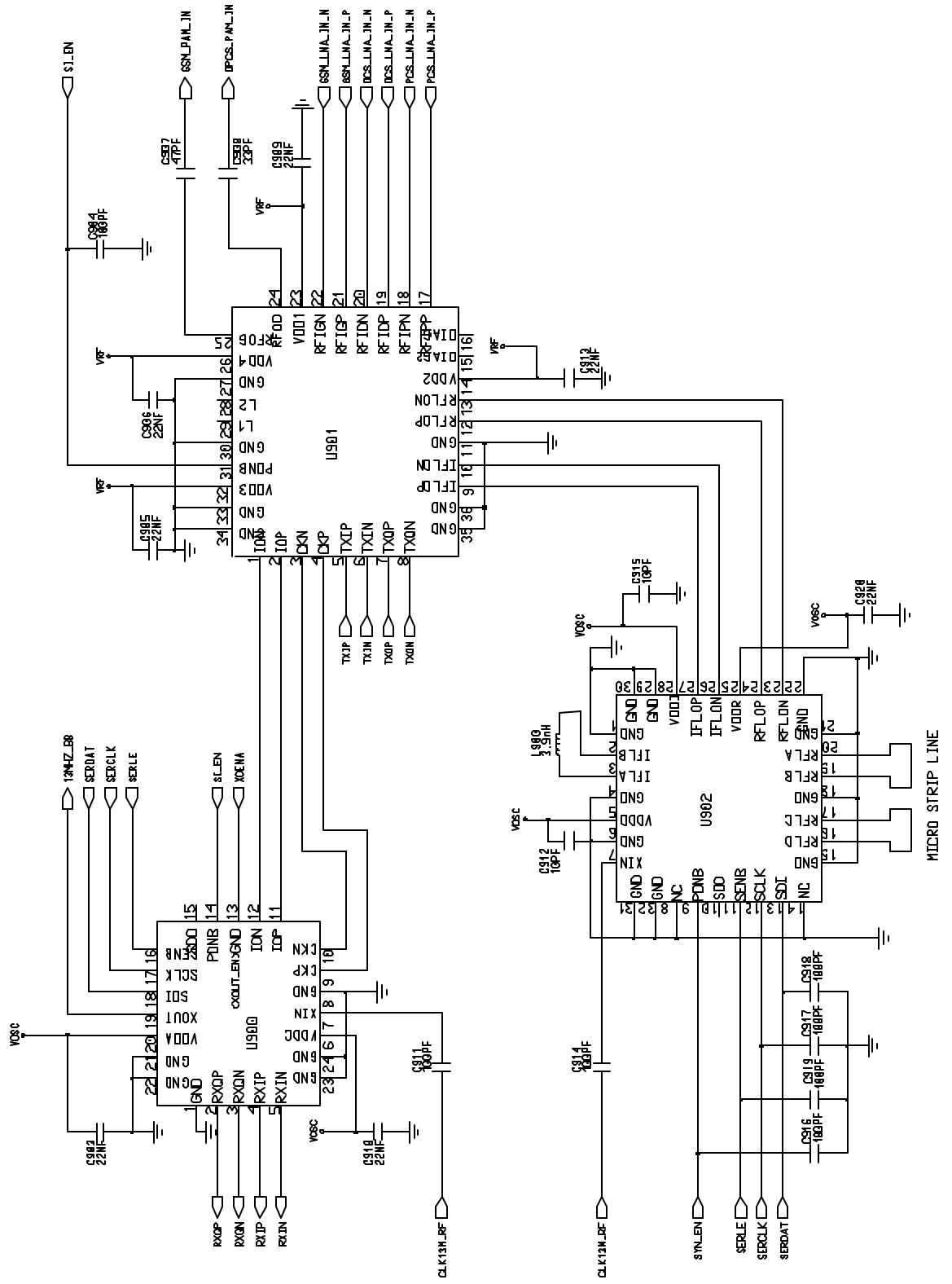


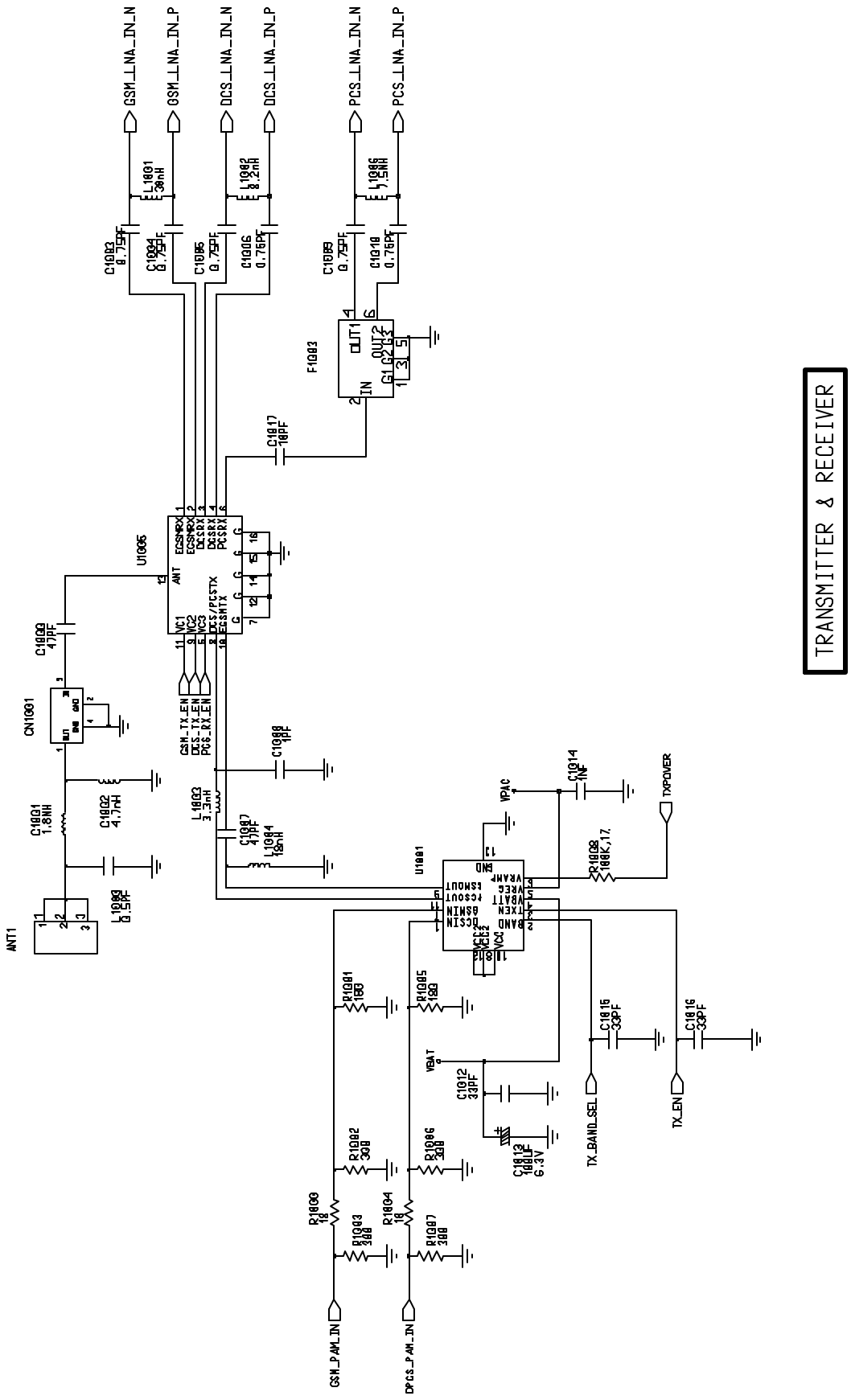
11. PCS Reciever



12. DPCS transmitter




SI-LAB
MICRO STRIP LINE
U901
U902
U900
SI_EN
GSM_PAM_IN
DPCS_PAM_IN
GSM_LNA_IN_N
GSM_LNA_IN_P
DCS_LNA_IN_N
DCS_LNA_IN_P
PCS_LNA_IN_N
PCS_LNA_IN_P
VRF
VOSC
TXIP
TXIN
TXQP
TXQN
RXQP
RXQN
RXIP
RXIN
CLK13M_RF
SYN_EN
SERLE
SERCLK
SERDAT


TRANSMITTER & RECEIVER
GSM_LNA_IN_N
GSM_LNA_IN_P
DCS_LNA_IN_N
DCS_LNA_IN_P
PCS_LNA_IN_N
PCS_LNA_IN_P
ANT1
U1005
U1001
F1003
CN1001
GSM_TX_EN
DCS_TX_EN
PCS_RX_EN
VPAC
TXPOWER
VBAT
TX_BAND_SEL
TX_EN
GSM_PAM_IN
DPCS_PAM_IN

4. SGH-V200 MAIN Electrical Parts List

SEC Code	Design LOC
GH71-00434A	ANT1
2203-000812	C100
2203-000995	C1000
2703-001729	C1001
2703-001747	C1002
2203-002677	C1003
2203-002677	C1004
2203-002677	C1005
2203-002677	C1006
2203-000995	C1007
2203-005288	C1008
2203-002677	C1009
2203-005061	C101
2203-002677	C1010
2203-000812	C1012
2404-001134	C1013
2203-000438	C1014
2203-000812	C1015
2203-000812	C1016
2203-000278	C1017
2203-001598	C102
2203-005061	C103
2203-000812	C104
2203-000812	C105
2203-005483	C106
2203-005481	C107
2203-001598	C109
2203-001598	C110
2203-000254	C1100
2203-005496	C1101
2203-000254	C1102
2203-005061	C1103
2203-005061	C1104
2203-000254	C1105
2404-001100	C1106
2404-001151	C1107
2203-000254	C1108

SEC Code	Design LOC
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2203-001598	C111
2203-005482	C1110
2203-005482	C1111
2203-005482	C1112
2203-005061	C1113
2203-005061	C1114
2203-005482	C1115
2203-005481	C1116
2203-005061	C1117
2203-005061	C1118
2203-005061	C1119
2203-001598	C112
2203-005061	C1120
2203-005061	C1121
2203-005061	C1122
2203-000254	C1123
2203-005061	C1124
2203-005061	C1125
2203-000254	C1126
2203-000254	C1127
2203-000254	C1128
2203-000254	C1129
2203-000233	C113
2203-000254	C1130
2203-000254	C1131
2203-000254	C1132
2203-000254	C1133
2404-001100	C1134
2203-005065	C1135
2203-000254	C1136
2203-000585	C1137
2203-000254	C1138
2203-001124	C1139
2203-001598	C114
2203-001124	C1140
2203-001124	C1141

SEC Code	Design LOC
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2203-000940	C1143
2203-005503	C1144
2203-001598	C115
2203-001598	C116
2203-001598	C118
2203-001598	C119
2203-005061	C120
2404-001105	C125
2404-001268	C126
2203-005482	C200
2203-005509	C201
2203-000438	C202
2203-000812	C203
2203-000812	C204
2203-000254	C205
2203-000812	C206
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2203-000812	C217
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2203-000812	C220
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2203-000438	C222
2203-000812	C223
2203-000812	C224
2203-000812	C225
2203-000812	C226

SEC Code	Design LOC
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2203-000812	C228
2203-000812	C229
2203-000812	C230
2203-000812	C231
2203-005065	C232
2203-005065	C233
2203-000233	C234
2203-000233	C235
2203-000233	C236
2203-005061	C237
2203-000233	C238
2203-000233	C239
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2203-000233	C241
2203-000233	C242
2203-005061	C243
2203-005061	C300
2203-005065	C400
2203-000585	C401
2203-005061	C402
2203-001405	C403
2404-001268	C404
2203-000438	C406
2203-000585	C407
2203-005061	C408
2404-001151	C409
2203-000438	C411
2203-005061	C412
2203-000438	C413
2203-000438	C414
2203-000359	C415
2203-005065	C416
2203-005061	C417
2203-000628	C420
2203-000995	C422
2203-000679	C423

SEC Code	Design LOC
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2404-001086	C425
2203-000812	C430
2203-000425	C432
2203-005061	C500
2203-005061	C501
2203-005061	C502
2203-000254	C504
2203-005496	C600
2203-000254	C601
2203-000254	C602
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2203-000628	C614
2203-000233	C615
2203-000628	C616
2203-000254	C617
2203-000233	C700
2203-000679	C701
2203-000679	C702
2203-005496	C703
2203-005065	C704
2203-005061	C705
2203-000254	C706
2203-000254	C707
2203-000254	C708
2203-000254	C709
2203-000254	C710

SEC Code	Design LOC
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2203-000254	C712
2203-000254	C713
2203-000812	C714
2203-000812	C715
2203-000812	C716
2203-000254	C800
2203-000386	C801
2007-007771	C805
2203-001412	C806
2203-000254	C807
2203-000254	C808
2203-000254	C809
2203-005482	C811
2203-001405	C903
2203-000233	C904
2203-001405	C905
2203-001405	C906
2203-000995	C907
2203-000812	C908
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2203-001405	C910
2203-000233	C911
2203-000278	C912
2203-001405	C913
2203-000233	C914
2203-000278	C915
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2203-000233	C919
2203-001405	C920
3709-001187	CN100
3705-001226	CN1001
3711-005079	CN1101
3711-005078	CN201
3710-001673	CN300

SEC Code	Design LOC
3722-001715	CN401
0404-001172	D1101
0404-001172	D1102
0404-001172	D1103
2904-001410	F1003
2203-002668	L1000
2703-002542	L1001
2703-002544	L1002
2703-001178	L1003
2703-001722	L1004
2703-002543	L1006
2703-001751	L900
0604-001146	LED200
0601-001547	LED801
0601-001547	LED802
0601-001547	LED803
0601-001547	LED804
0601-001547	LED805
0601-001547	LED806
0601-001547	LED807
0601-001547	LED808
0601-001547	LED809
0601-001547	LED810
0601-001547	LED811
0601-001547	LED813
0601-001547	LED814
0601-001547	LED815
0601-001547	LED816
0601-001547	LED817
0601-001547	LED818
0601-001547	LED819
0601-001547	LED820
0601-001547	LED821
4302-001130	M101
2801-004025	OSC601
2809-001260	OSC801
0504-000168	Q100

SEC Code	Design LOC
0502-001201	Q101
0501-000225	Q400
2007-001288	R1000
2007-001307	R1001
2007-007008	R1002
2007-007008	R1003
2007-001288	R1004
2007-001307	R1005
2007-007008	R1006
2007-007008	R1007
2007-007107	R1008
2007-001319	R103
2007-001291	R104
2007-007200	R106
2007-000758	R107
2007-000167	R108
2007-000982	R1100
2007-000163	R1101
2007-000170	R1103
2007-000148	R1104
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2007-007771	R1106
2007-007306	R1109
2007-007142	R111
2007-001305	R1110
2007-007306	R1111
2007-007306	R1112
2007-007306	R1113
2007-007139	R112
2007-001323	R113
2007-007771	R1200
2007-000172	R200
2007-000157	R300
2007-000157	R301
2007-000140	R302
2007-000140	R303
2007-000140	R304

SEC Code	Design LOC
2007-000140	R305
2007-000140	R306
2007-007771	R307
2007-003001	R400
2007-003001	R401
2007-000148	R402
2007-000159	R403
2007-000775	R404
2007-000159	R405
2007-000775	R406
2007-000141	R407
2007-001119	R409
2007-001325	R412
2007-000162	R415
2007-000141	R420
2007-000148	R421
2007-000161	R422
2007-001333	R423
2007-000140	R424
2007-000148	R425
2007-007771	R426
2203-005503	R431
2007-000172	R502
2007-007771	R503
2007-000157	R600
2007-000170	R601
2007-000157	R602
2007-007142	R603
2007-007308	R604
2007-007308	R605
2007-000172	R606
2007-000162	R607
2007-000144	R701
2007-007200	R705
2007-007200	R706
2007-000172	R800
2007-001308	R801

SEC Code	Design LOC
2007-007405	R802
2007-000138	R805
2007-001306	R806
2007-001306	R807
2007-001306	R808
2007-001306	R809
2007-001306	R810
2007-001306	R811
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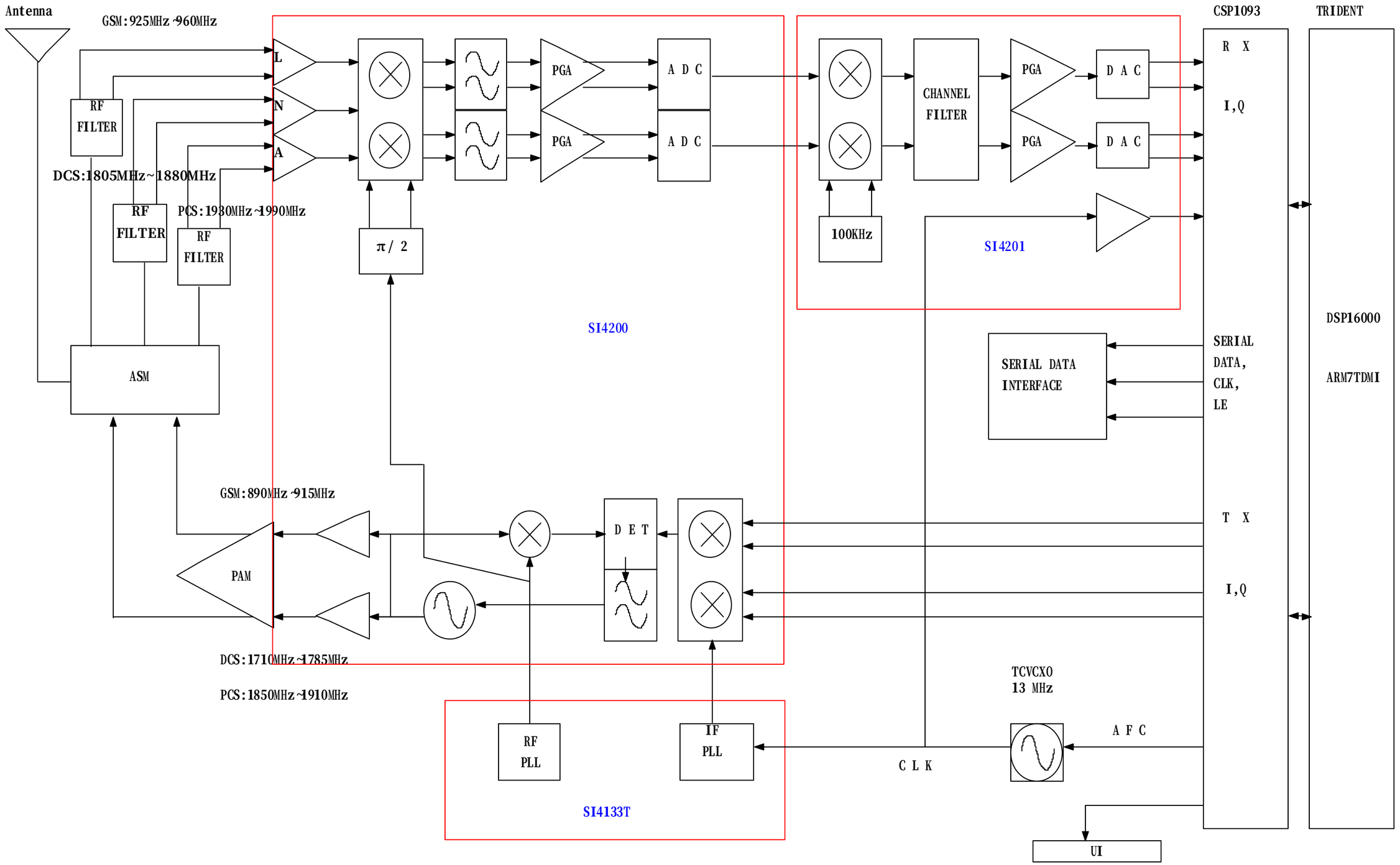
2007-001306	R818
2007-001306	R819
2007-001306	R820
2007-001306	R821
2007-001306	R822
2007-001306	R823
2007-001306	R824
2007-001306	R825
2007-007008	R826
1203-002568	U100
1201-001889	U1001
2909-001191	U1005
1203-002127	U101
0506-001052	U102
GH13-00012A	U1101
2804-001492	U1102
1204-001982	U1103
1203-001720	U1104
0801-000796	U1105
1203-002704	U1106
0801-002727	U1107
0801-000796	U1108
0801-000796	U1109
0801-002212	U1110

SEC Code	Design LOC
0801-002727	U1111
0801-002727	U1112
1001-001183	U400
1204-001960	U401
1109-001273	U500
GH09-00020A	U601
1209-001219	U602
1204-001984	U700
0504-001042	U701
0504-001042	U702
0504-001042	U703
1009-001010	U802
1205-002185	U900
1205-002268	U901
1209-001434	U902
3404-001152	VOL_DN
3404-001152	VOL_UP
0406-001083	ZD300
0406-001083	ZD301
0406-001152	ZD302
1405-001082	ZD303
1405-001082	ZD304
1405-001082	ZD305
1405-001082	ZD306
1405-001082	ZD307
1405-001018	ZD308
1405-001082	ZD401
1405-001082	ZD402
1405-001082	ZD403
1405-001082	ZD405
GH92-01414A	
GH41-00380A	

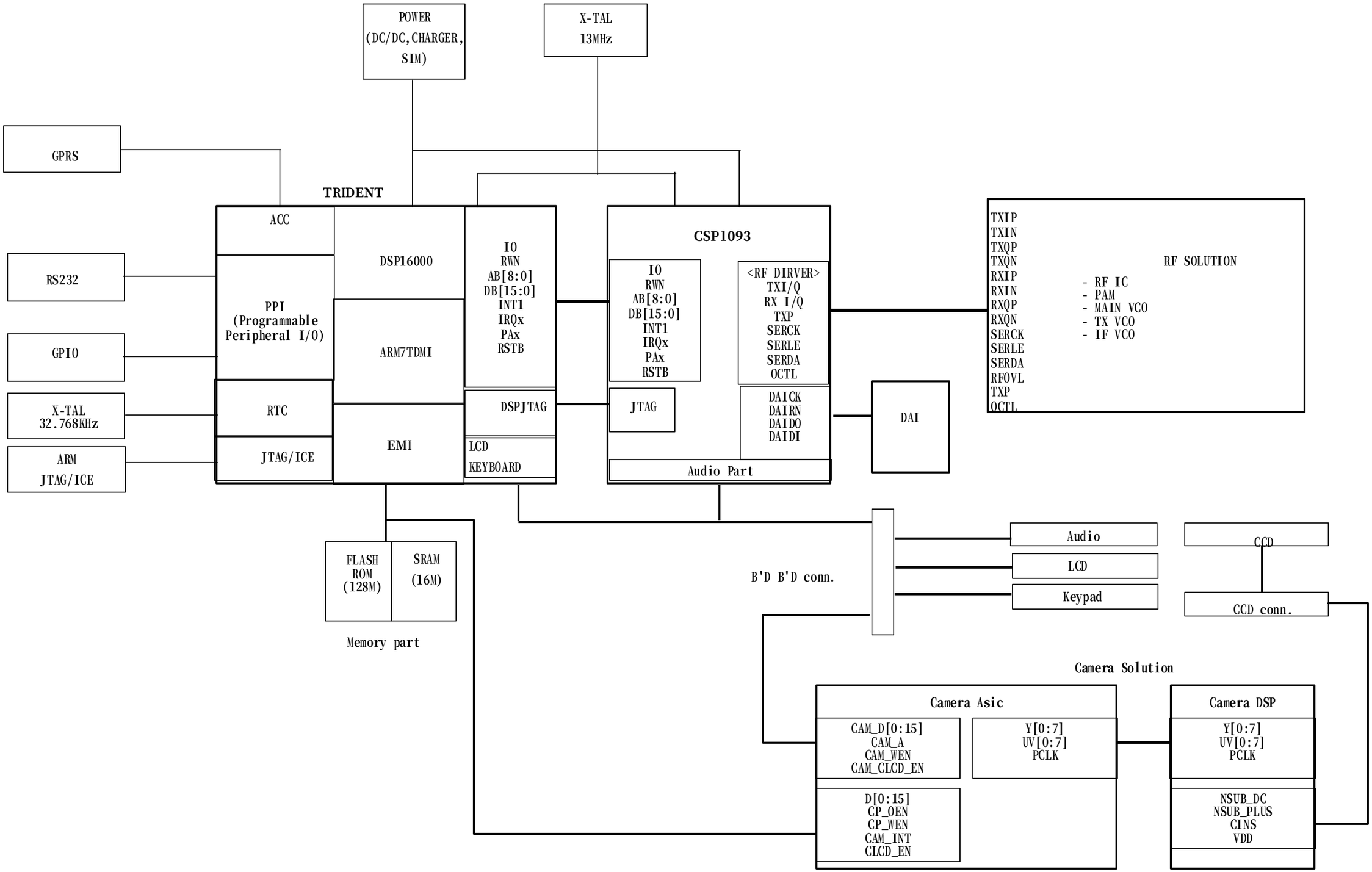
MEMO

5. SGH-V200 Block Diagrams

1. RF Solution Block Diagram

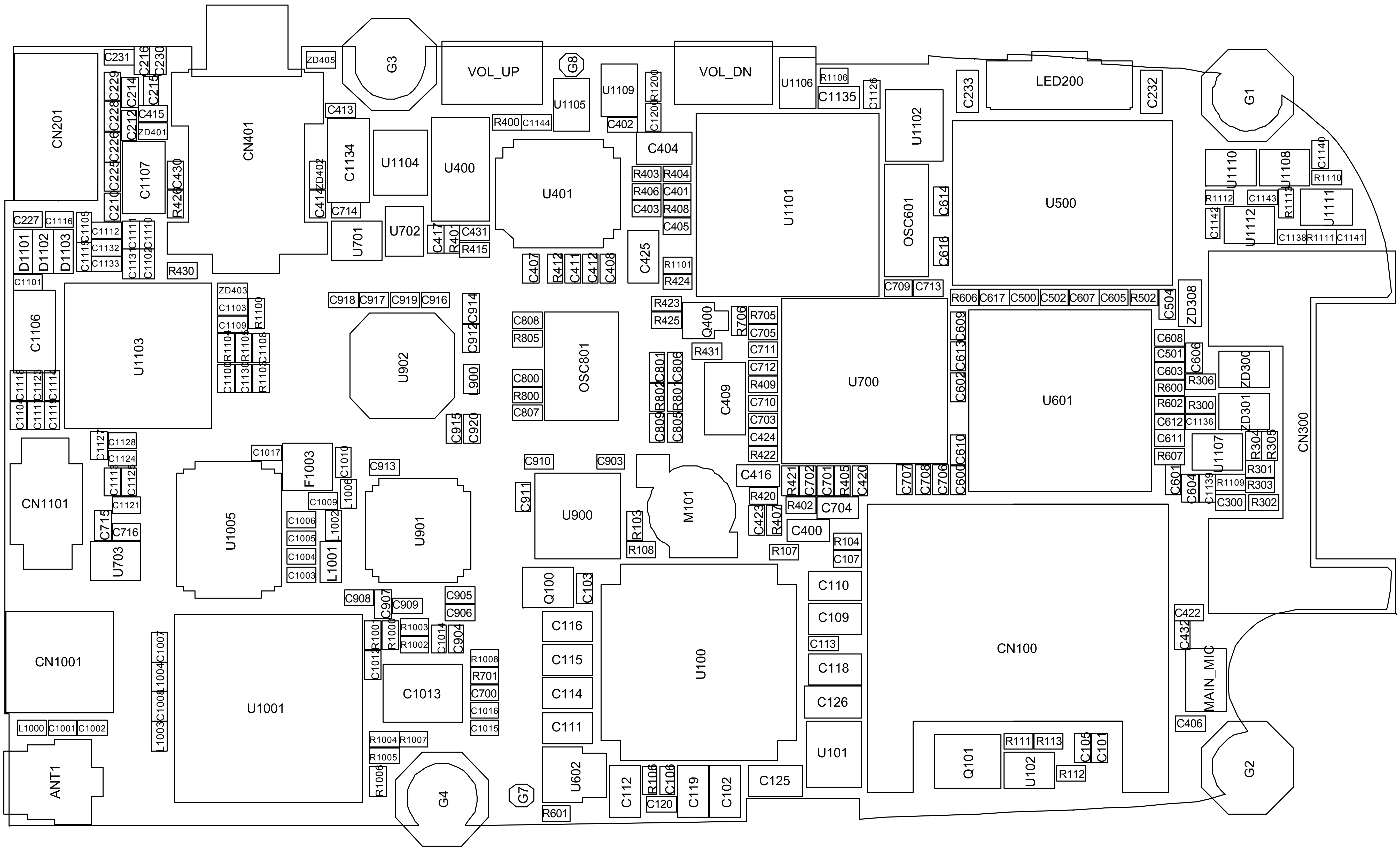


2. Base Band Solution Block Diagram

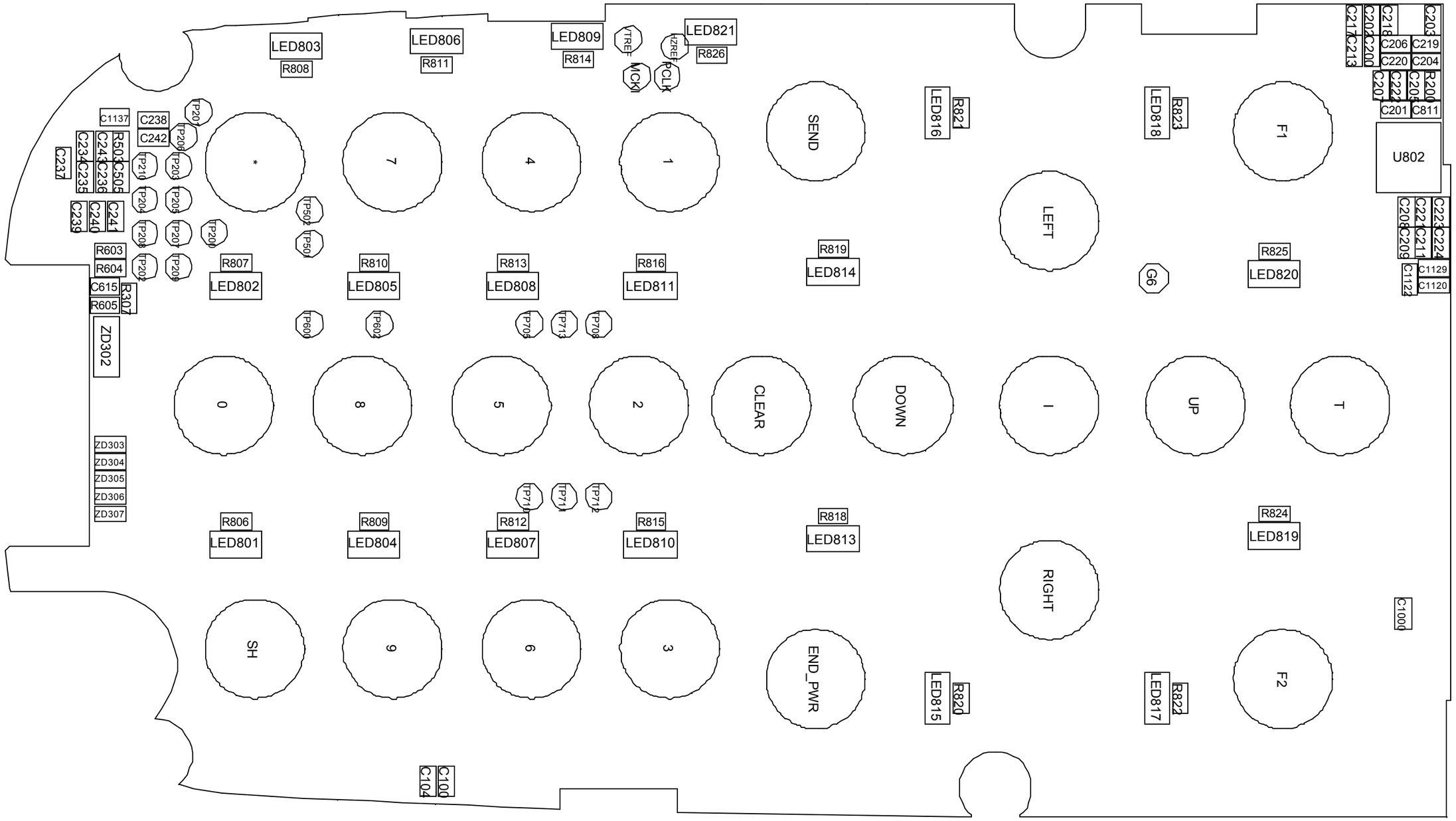


6. SGH-V200 PCB Diagrams

1. Main PCB Top Diagram



2. Main PCB Bottom Diagram



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BASIC.