

Compal Confidential

ZIWB2/ZIWB3/ZIWE1 DIS M/B Schematics Document

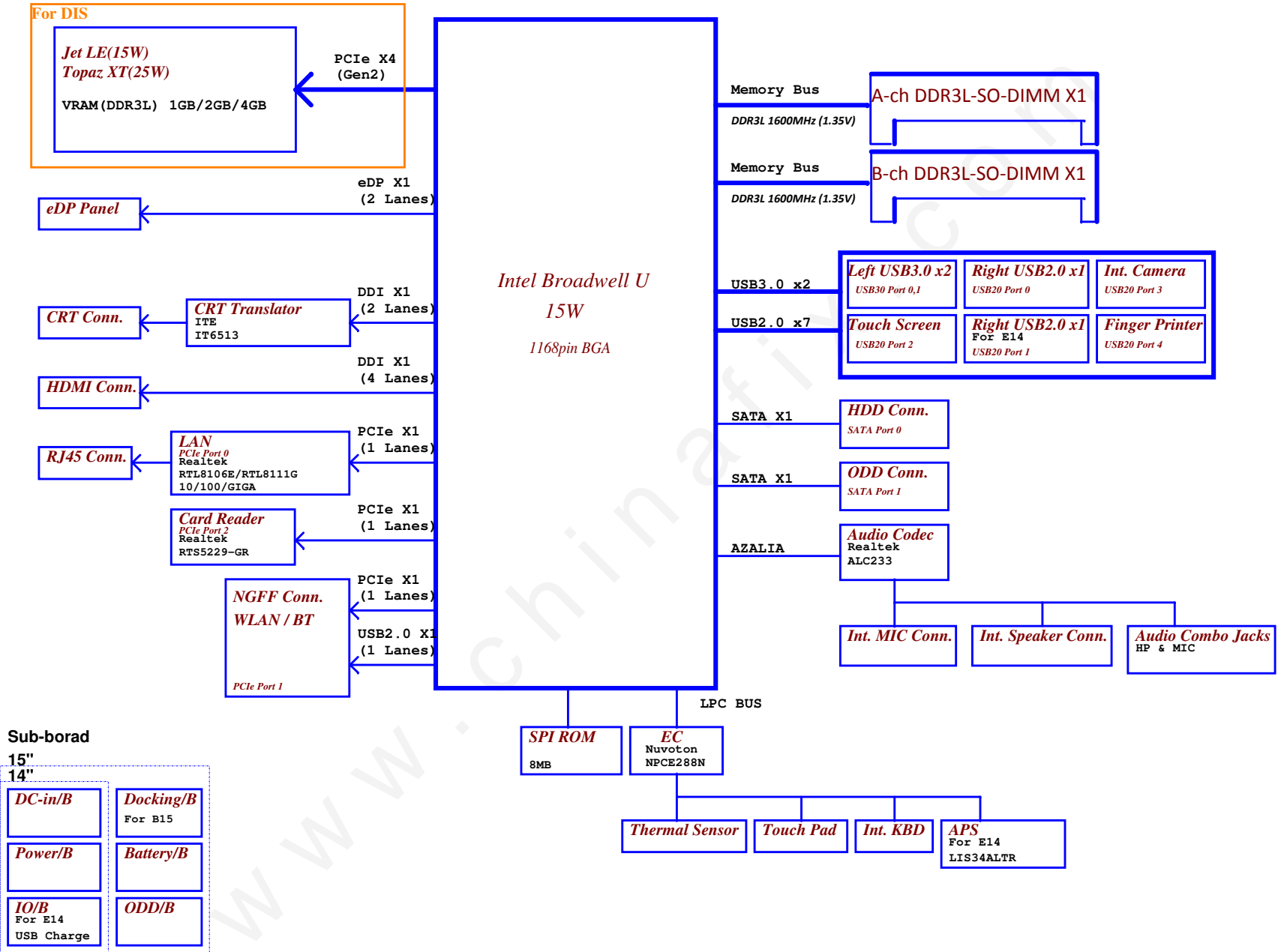
Intel Boardwell U Processor with DDR3L

2014-02-10

LA-B092P

REV : 1.0

Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title Cover Page
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Voltage Rails

power plane	State	+B	+5VALW	+1.5V	+3VS +3VVS +1.5VS +V1_05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0		○	○	○	○
S3		○	○	○	X
S5 S4/AC		○	○	X	X
S5 S4/ Battery only		○	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

USB Port Table

	USB 2.0 Port	3 External USB Port
EHCI1	UHCI0	0 USB Port (Left Side) ^{USB3.0}
		1 USB Port (Left Side) ^{USB3.0}
		2 Touch Screen
	UHCI1	3 Camera
		4
		5
UHCI3	6	
	7	
	8	
EHCI2	UHCI4	9 USB Port (Right Side USB-BD)
		10 Mini Card(WLAN)
	UHCI5	11 Card Reader
		12
		13

BOM Structure Table

Item	BOM Structure
ZIWB2 (14")	B14@
ZIWB3 (15")	B15@
ZIWE1 (14")	E14@
CPU_SA00006SM20	i5_4200U@
CPU_SA00007AM00	QFSY@
CPU_SA00006SU30	i3_4100U@
CPU_SA000072Q10	i3_4005U@
CPU_SA00006SX20	i3_4010U@
LAN 10/100 Transformer	100@
LAN GIGA Transformer	GIGA@
LAN Switch mode	SWITCH@
LAN RTL8106E-CG	8106ELDO@
LAN RTL8111GS-CG	8111GLDO@
LAN RTL8106EUS-CG	8106ESW@
LAN RTL8111GUS-CG	8111GSW@
Audio_233	233@
Audio_233VB	233VB@
For B15	Docking@
For B14, E14	NoDocking@
For Deep Sleep	DS3@
For No Deep Sleep	NoDS3@
WLAN Support ISCT	ISCT@
WLAN No Support ISCT	NoISCT@
For Intel ZERO ODD	ZODD@
For No Intel ZERO ODD	NoZODD@
For Green CLK	GCLK@
For No Green CLK	NoGCLK@
For No Green CLK	NoGCLKDIS@
Green CLK IC For DIS	GCLKDIS@
Green CLK IC For UMA	GCLKUMA@
GPU support Single Rank	SR@
GPU support Dual Rank	DR@
GPU Jet LE	JET@
GPU Topaz XT	TOPAZ@
For DIS	PX@
For UMA	UMA@
Camera	COMS@
APS (G-sensor)	GS@
Touch Screen	TS@
HDMI	HDMI@
USB 2.0	USB2@
USB 3.0	USB3@
Full HD Panel (2 Lane)	FHD@
ENE EC 9012	9012@
HDMI Royalty	45@
Connector	ME@
VRAM indentify	X76@
Un-pop component for EMI	@EMI@
Un-pop component for ESD	@ESD@
DA600140000	PCB_14_DIS@
DA600141000	PCB_14_UMA@
DA600140100	PCB_15_DIS@
DA600141100	PCB_15_UMA@

Only in DIS Schematic

Only in DIS Schematic

No USE

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x	Thermal Sensor	0100 1100

PCH SM Bus address

AMD-GPU SM Bus address

Device	Address	Device	Address
DDR_JDIMM1	1010 000x A0h	Internal thermal sensor	0100 0001 41h
DDR_JDIMM2	1010 010x A4h		

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	+3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	+3VGS	X	X	X	X	+3VS	+3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	+3VS	+3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	+3VGS	X	+3VS	X	X	+3VS	X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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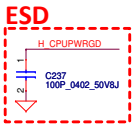
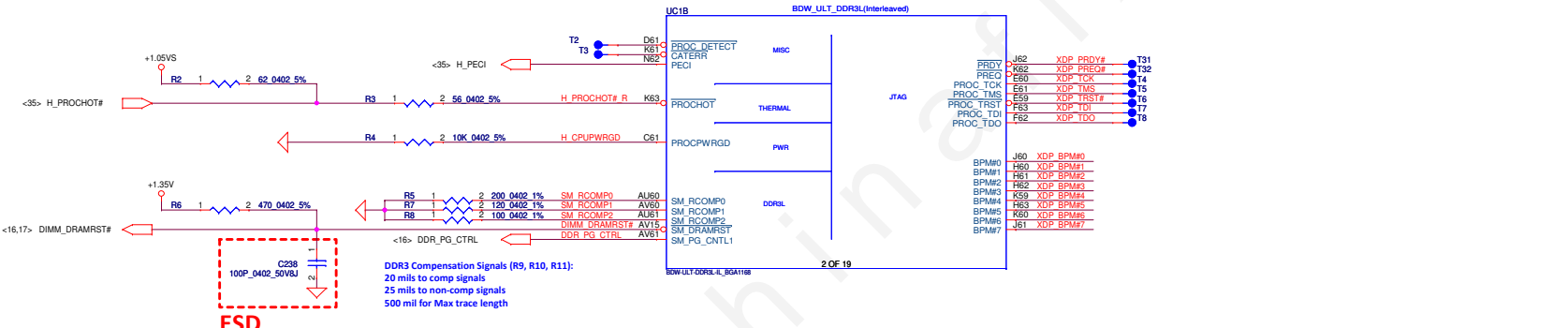
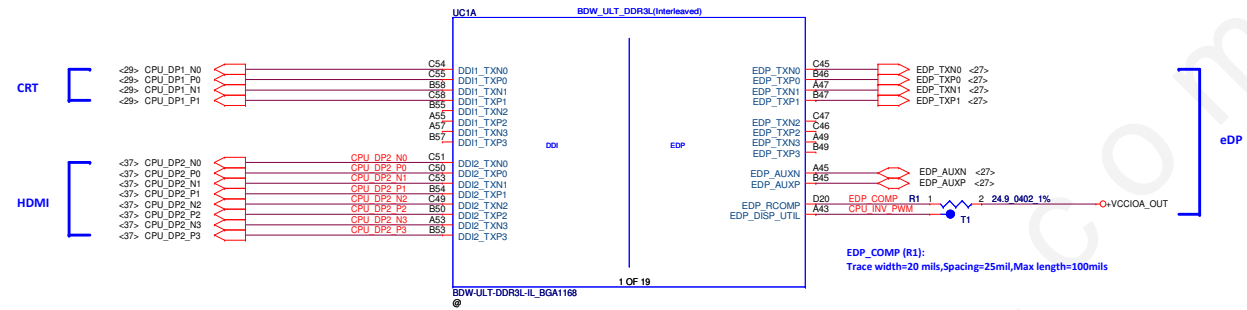


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- DAZ
DAZ14J00101
PCB 14I LA-B091P REV0 M/B DIS 3
PCB_B14_DIS@
- DAZ
DAZ14L00101
PCB 14K LA-B091P REV0 M/B DIS 6
PCB_B15_DIS@
- DAZ
DAZ14N00101
PCB 14K LA-B091P REV0 M/B DIS 6
PCB_E14_DIS@
- DAZ
DAZ14J00201
PCB 14I LA-B092P REV0 M/B UMA 3
PCB_B14_UMA@
- DAZ
DAZ14L00201
PCB 14K LA-B092P REV0 M/B UMA 6
PCB_B15_UMA@
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DAZ14N00201
PCB 14K LA-B092P REV0 M/B UMA 6
PCB_E14_UMA@



ESD

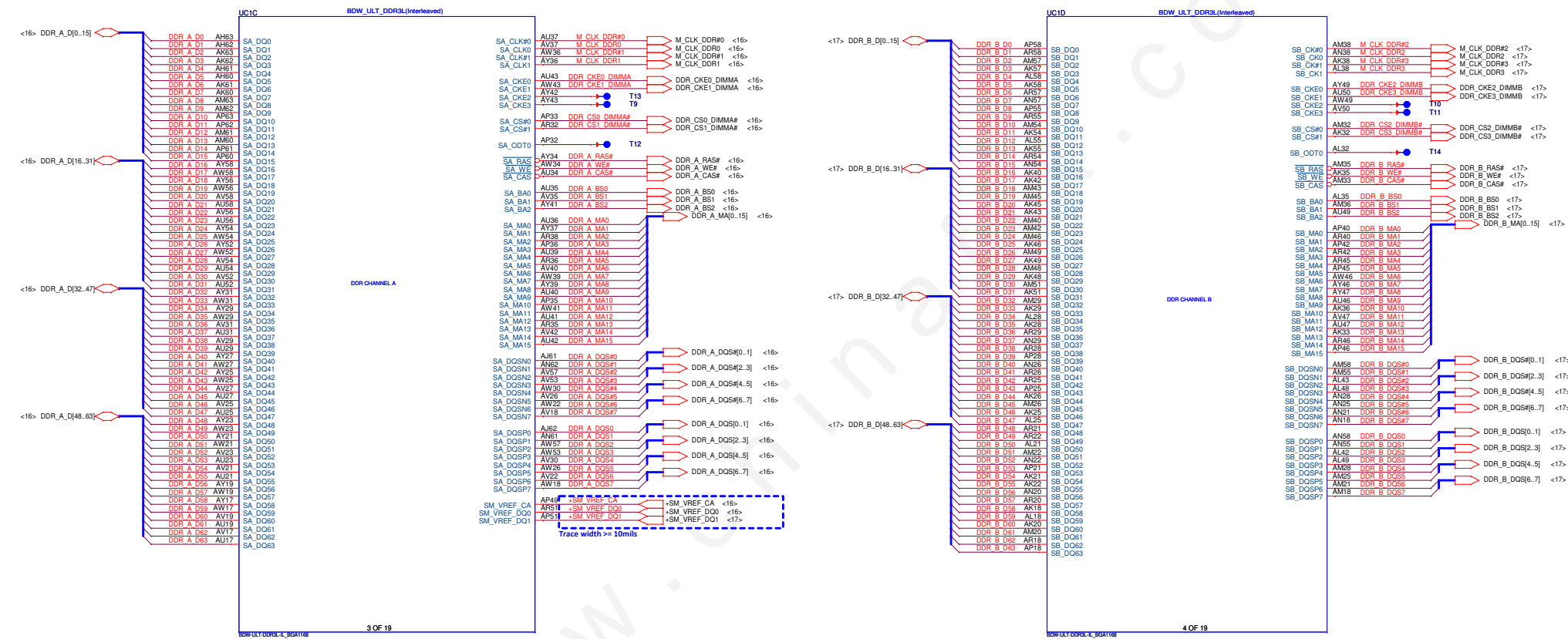
C238
100P_0402_50VJ

DDR3 Compensation Signals (R9, R10, R11):
20 mils to comp signals
25 mils to non-comp signals
500 mil for Max trace length

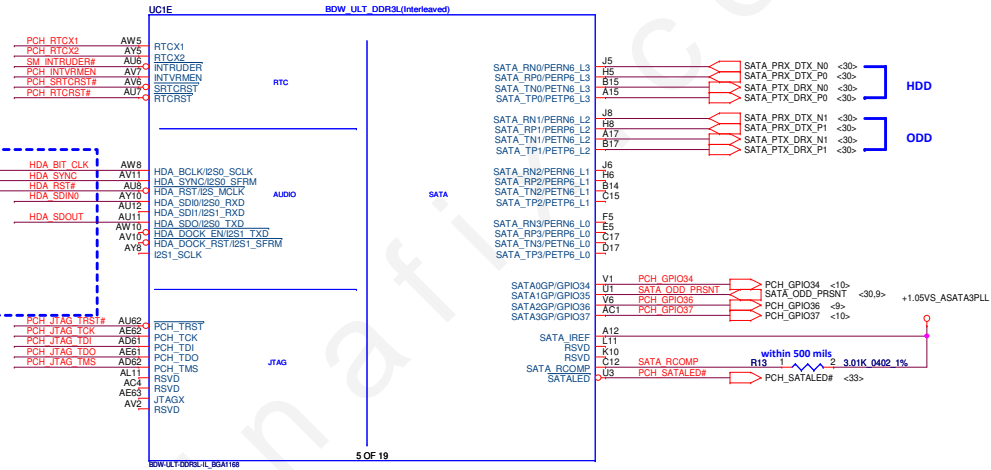
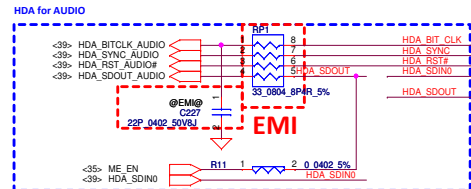
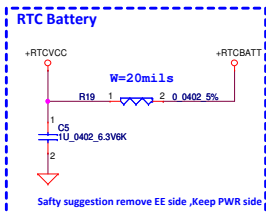
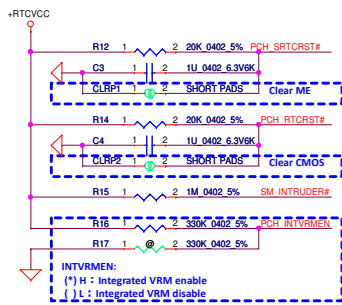
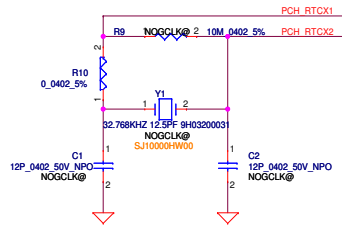
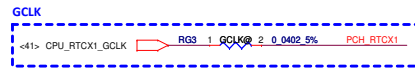
- UC1
SA00007G030
Intel 2957U 1.4G 2M D0 2u:BGA CPU
2957U@
- UC1
SA00007G230
S IC CL8064701569500 QFAN D0 1.7G BGA
3558U@
- UC1
SA00006SLA0
S IC CL8064701477202 QEVD C0 1.8G BGA
I7_4500U@
- UC1
SA00006SMC0
S IC CL8064701477702 SR170 C0 1.6G C38I
I3_4500U@
- UC1
SA00007AM00
S IC CL8064701614813 QFSY C0 1.6G BGA
QFSY@
- UC1
SA00006SL30
S IC CL8064701476302 SR16P C0 1.8G C38I
I3_4100U@
- UC1
SA00007C350
S IC CL8064701478404 QEAR D0 1.7G C38
I3_4005U@
- UC1
SA00006SX80
S IC CL8064701478202 SR16Q C0 1.7G C38I
I3_4010U@

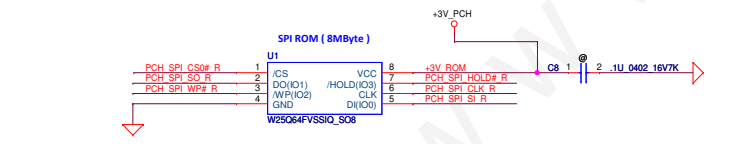
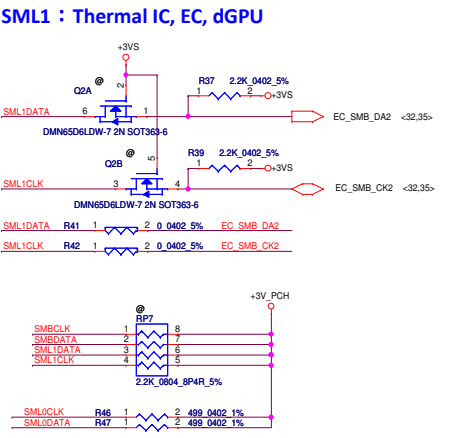
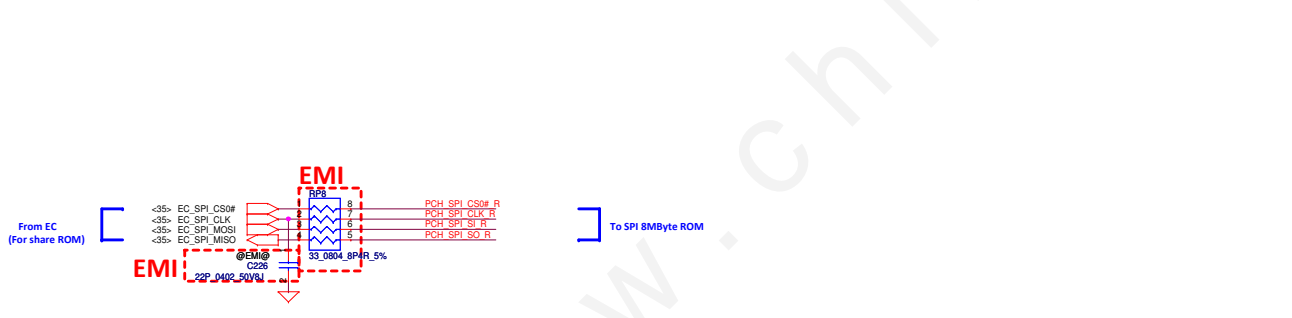
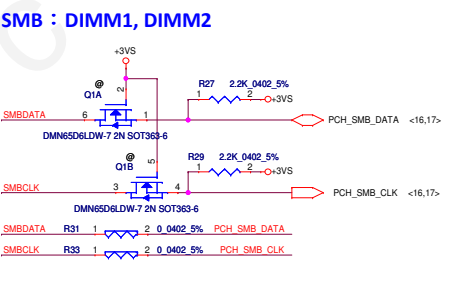
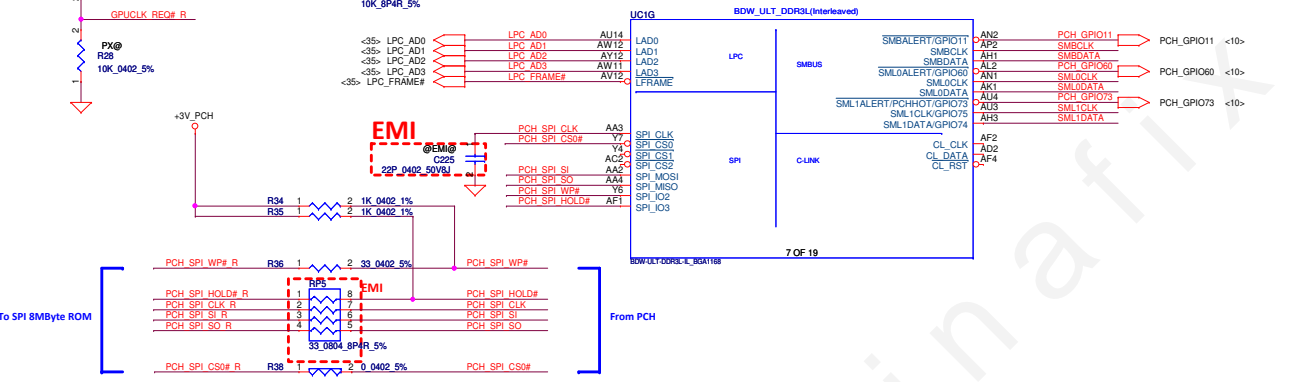
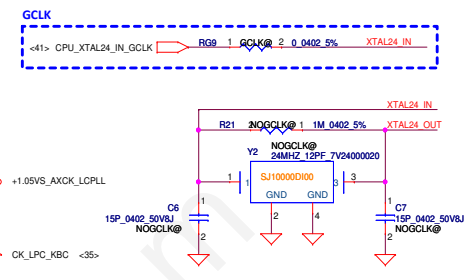
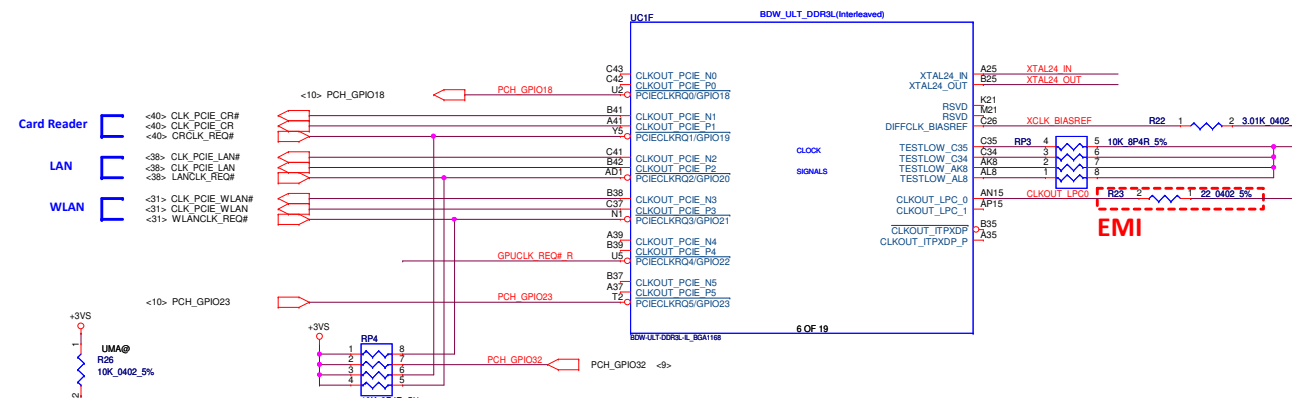
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Interleaved Memory



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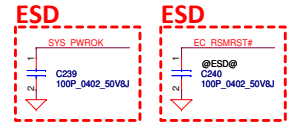




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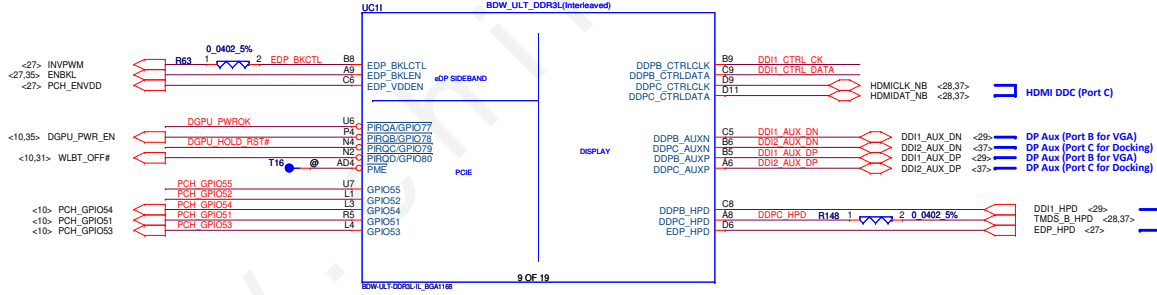
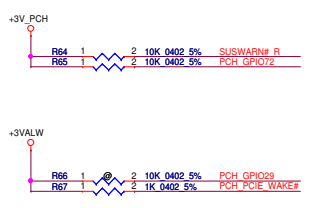
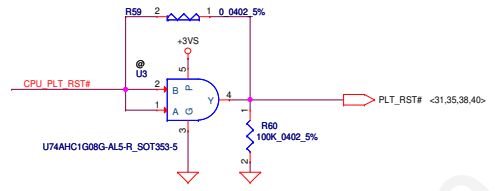
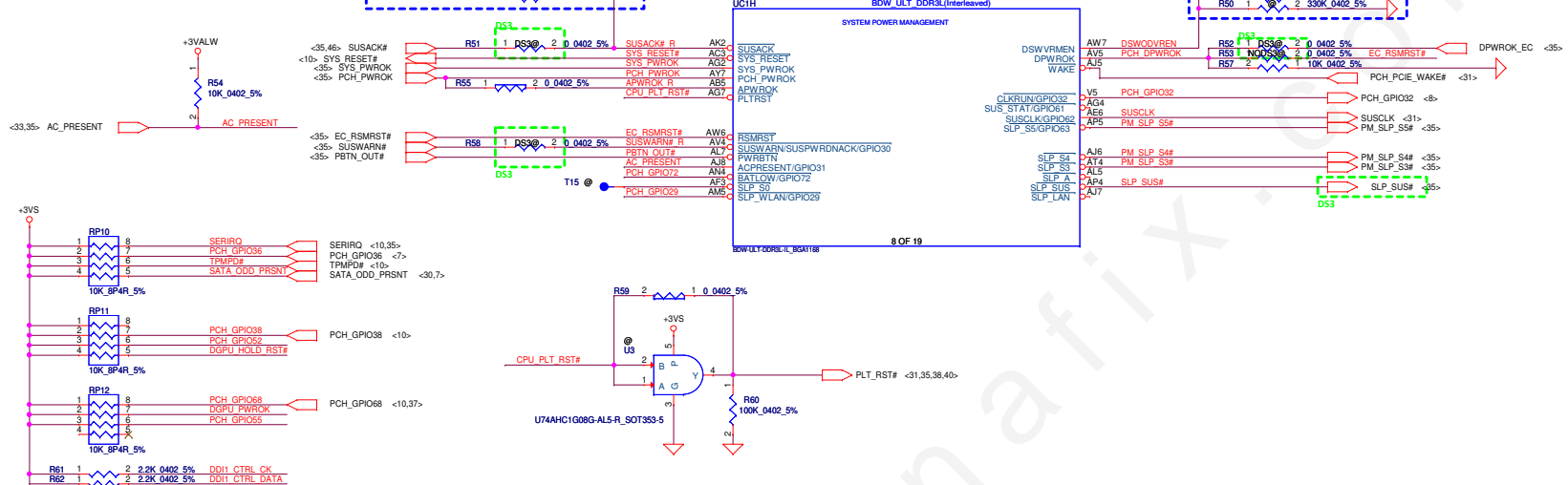


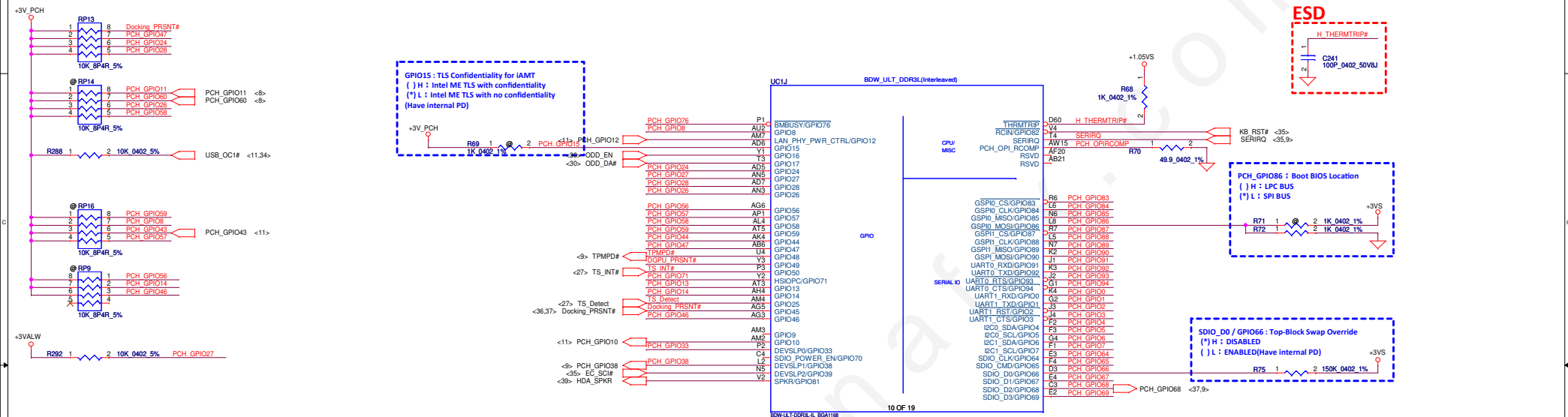
Function	(X)DS3 (X)SBA	(O)DS3 (X)SBA	(X)DS3 (O)SBA
R51	X	O	X
R55	O	O	X
R56	X	X	O
R58	X	O	X
R52	X	O	X
R53	O	X	O



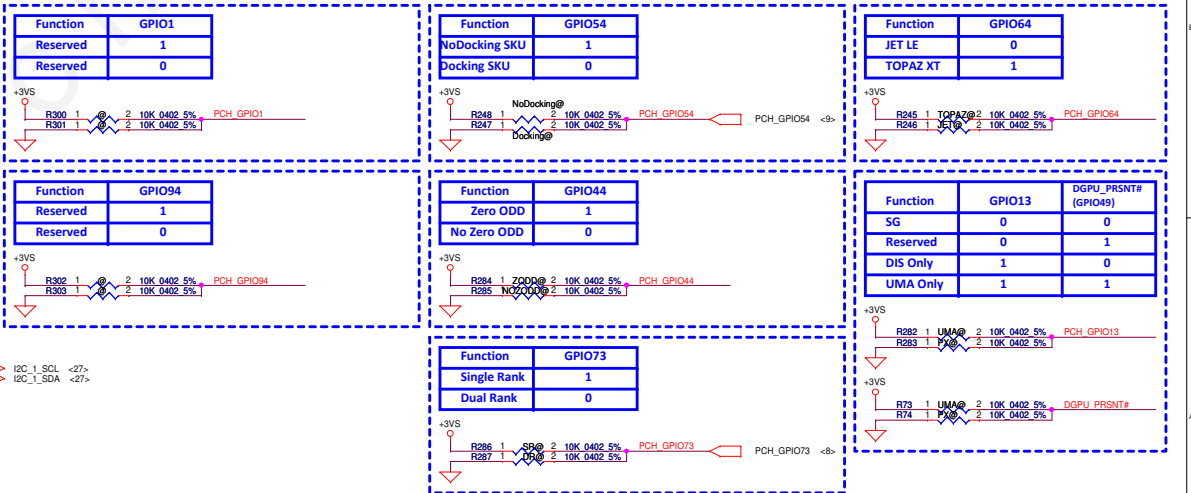
Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit
CAN be NC, if not support Deep Sx
SUSWARN# R R48 1 @ 2 0 0402 5%

DSWDDVREN - On Die DSW VR Enable
(*): H : Enable(DEFAULT)
(): L : Disable
R49 1 @ 2 330K 0402 5%
R50 1 @ 2 330K 0402 5%





BIOS Strap Pin

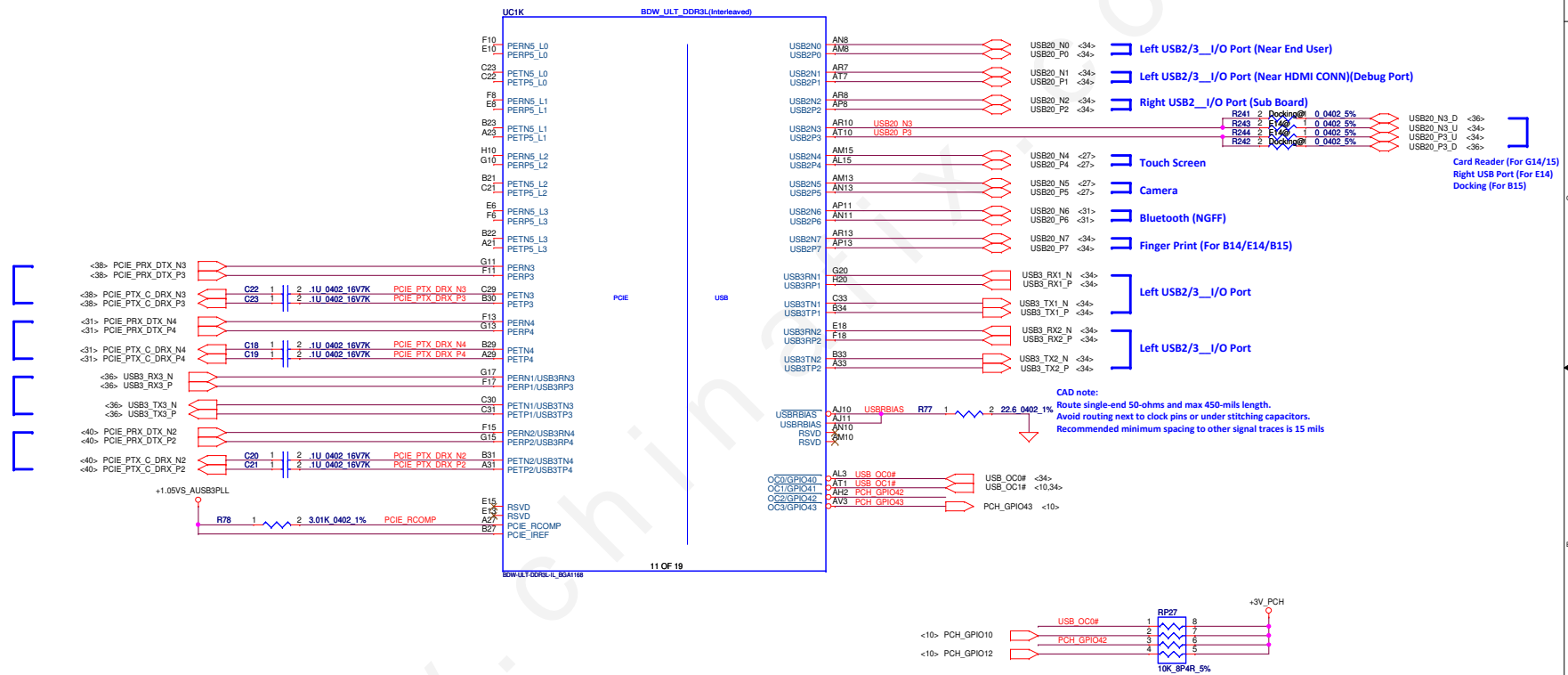


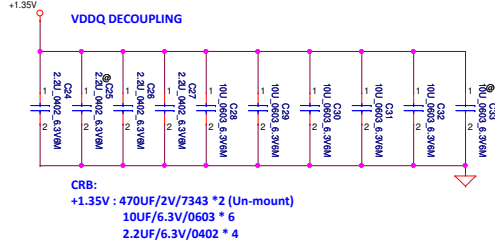
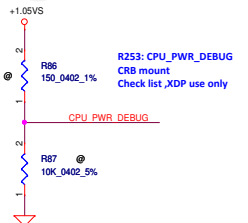
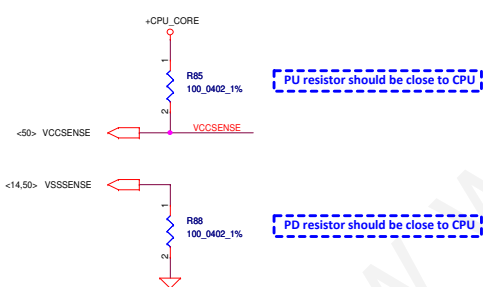
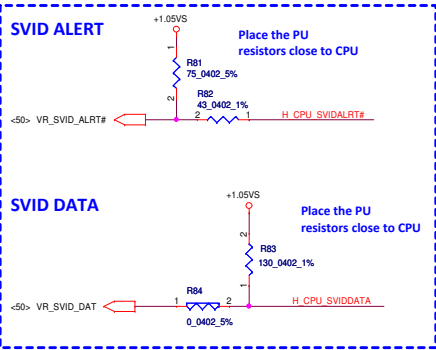
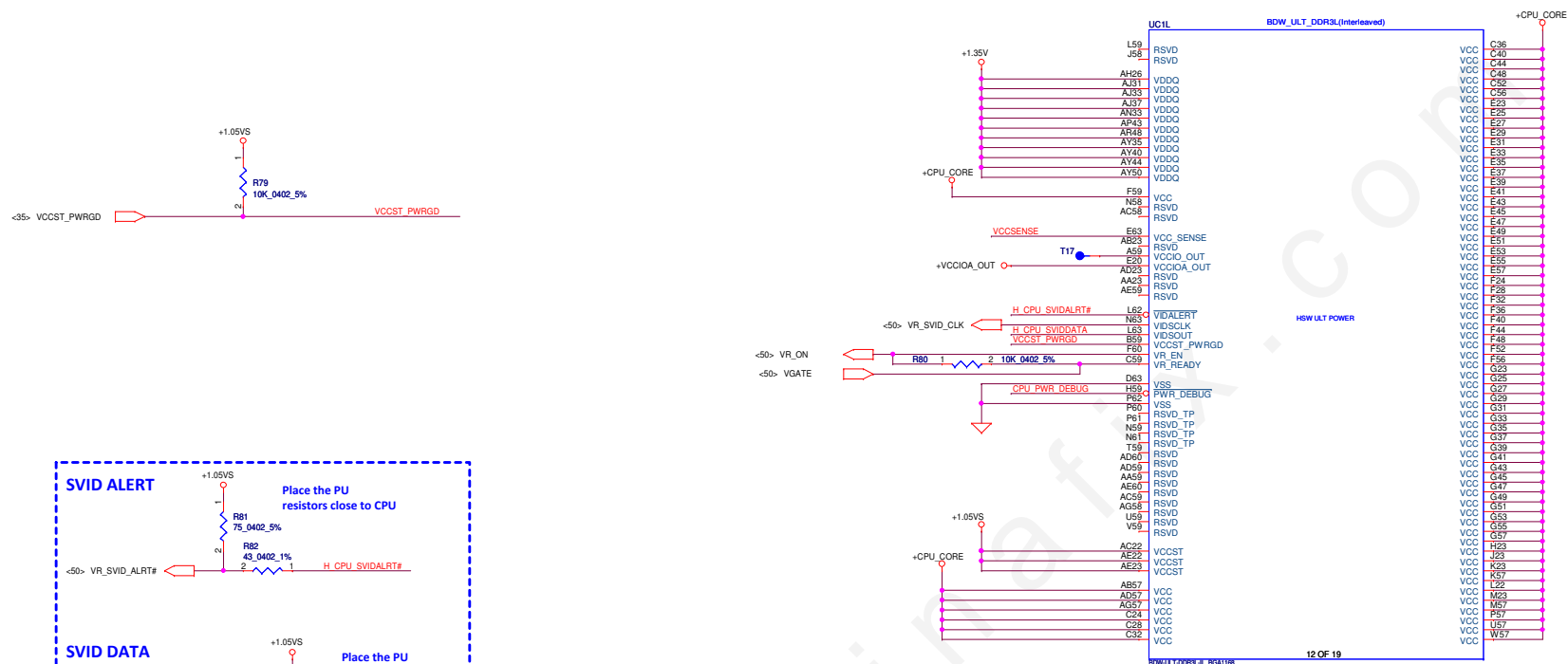
LAN

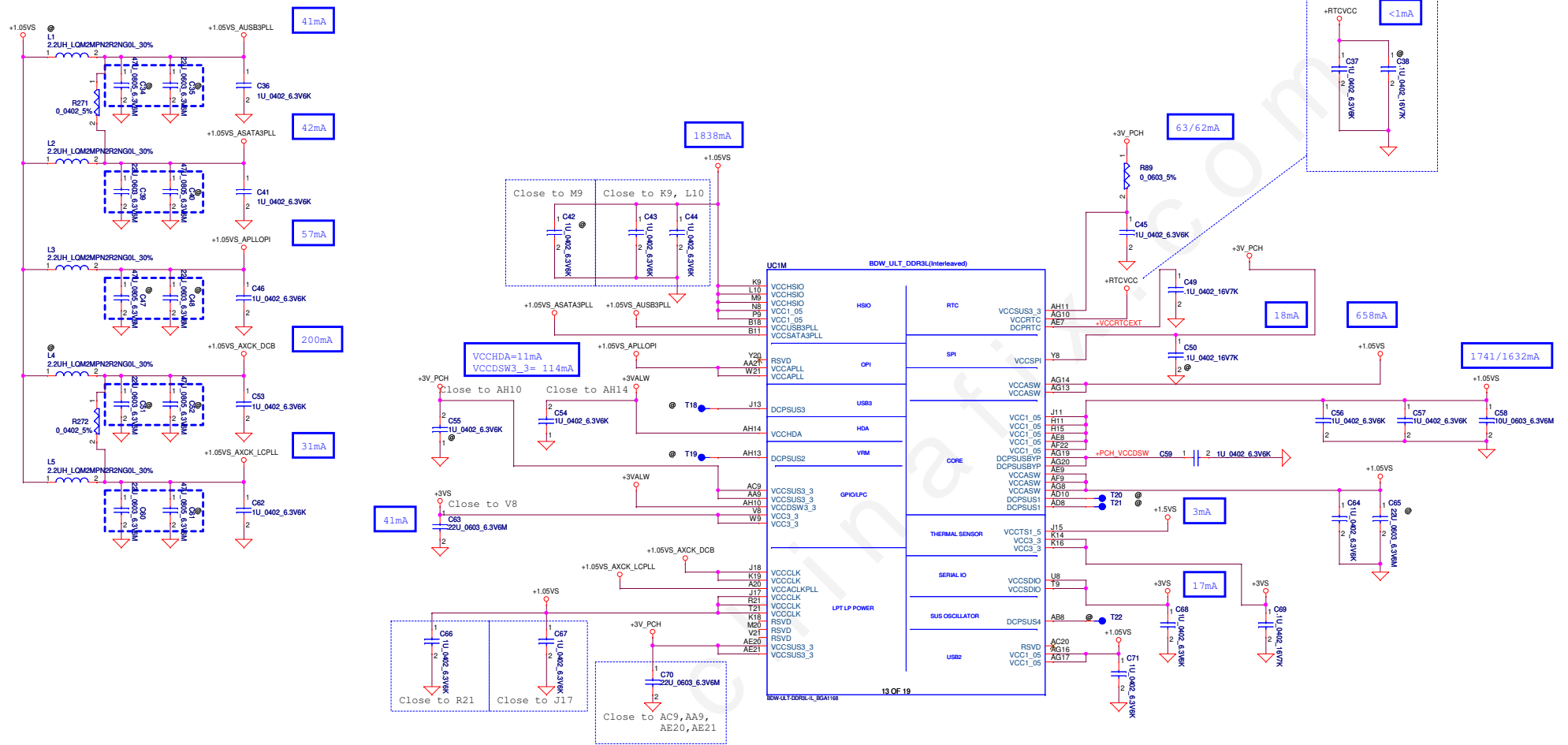
WLAN

USB2/3 Docking
(For B15)

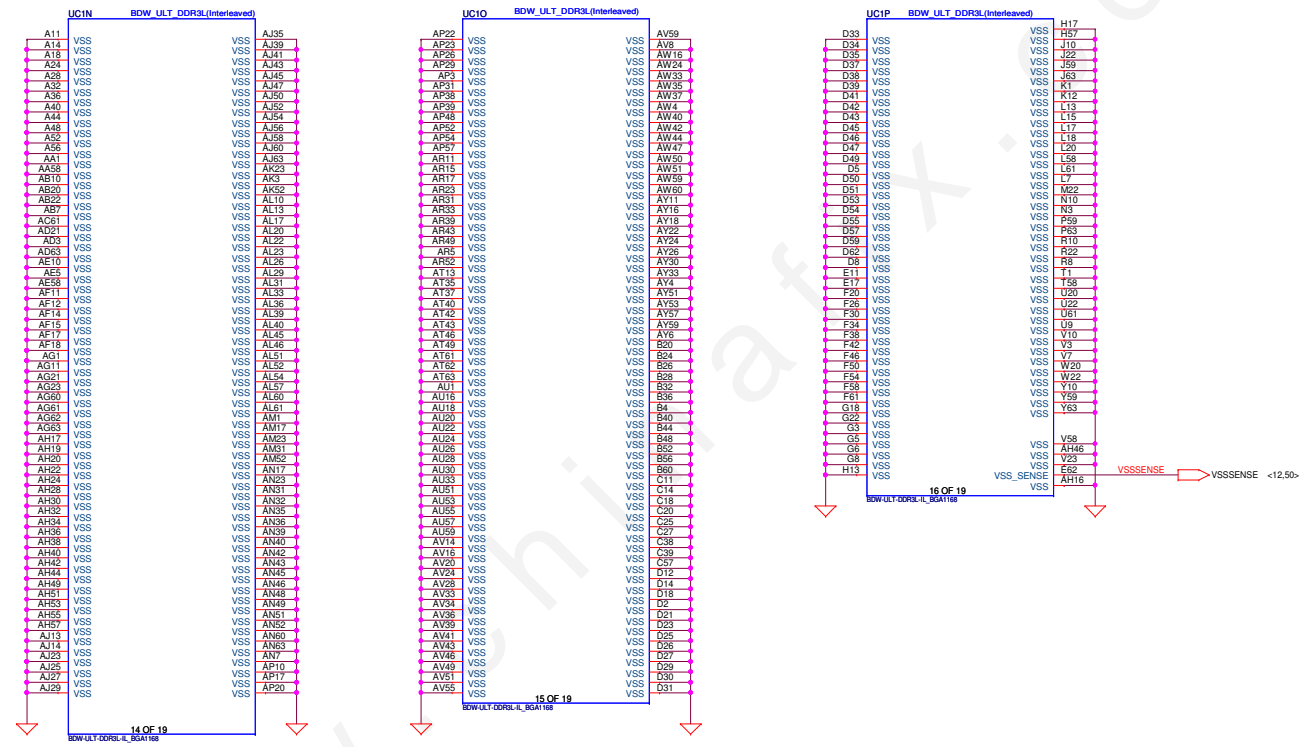
Card Reader
(For B14/E14/B15)



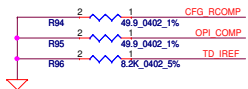
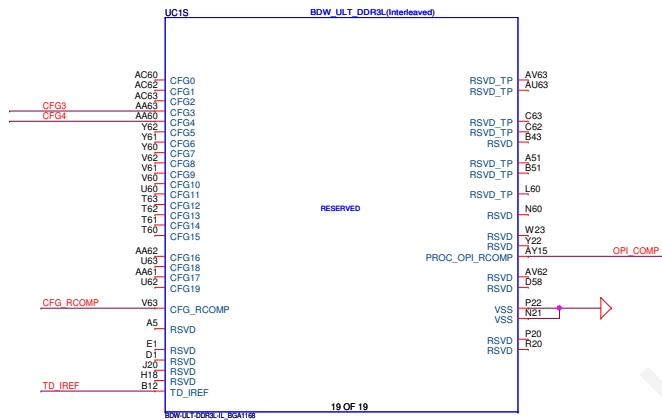
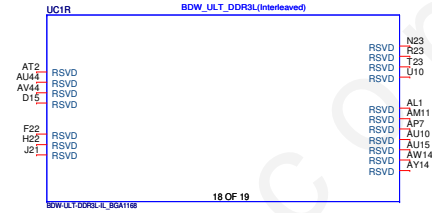
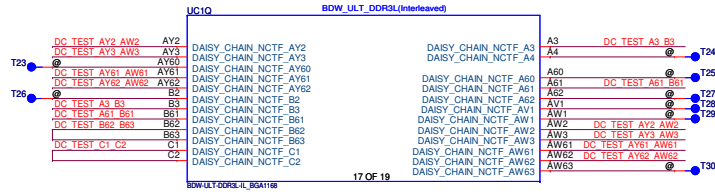




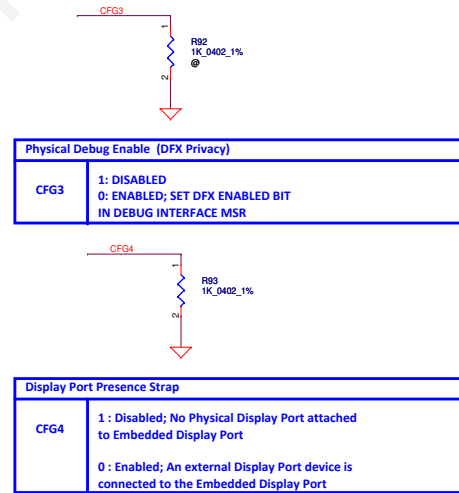
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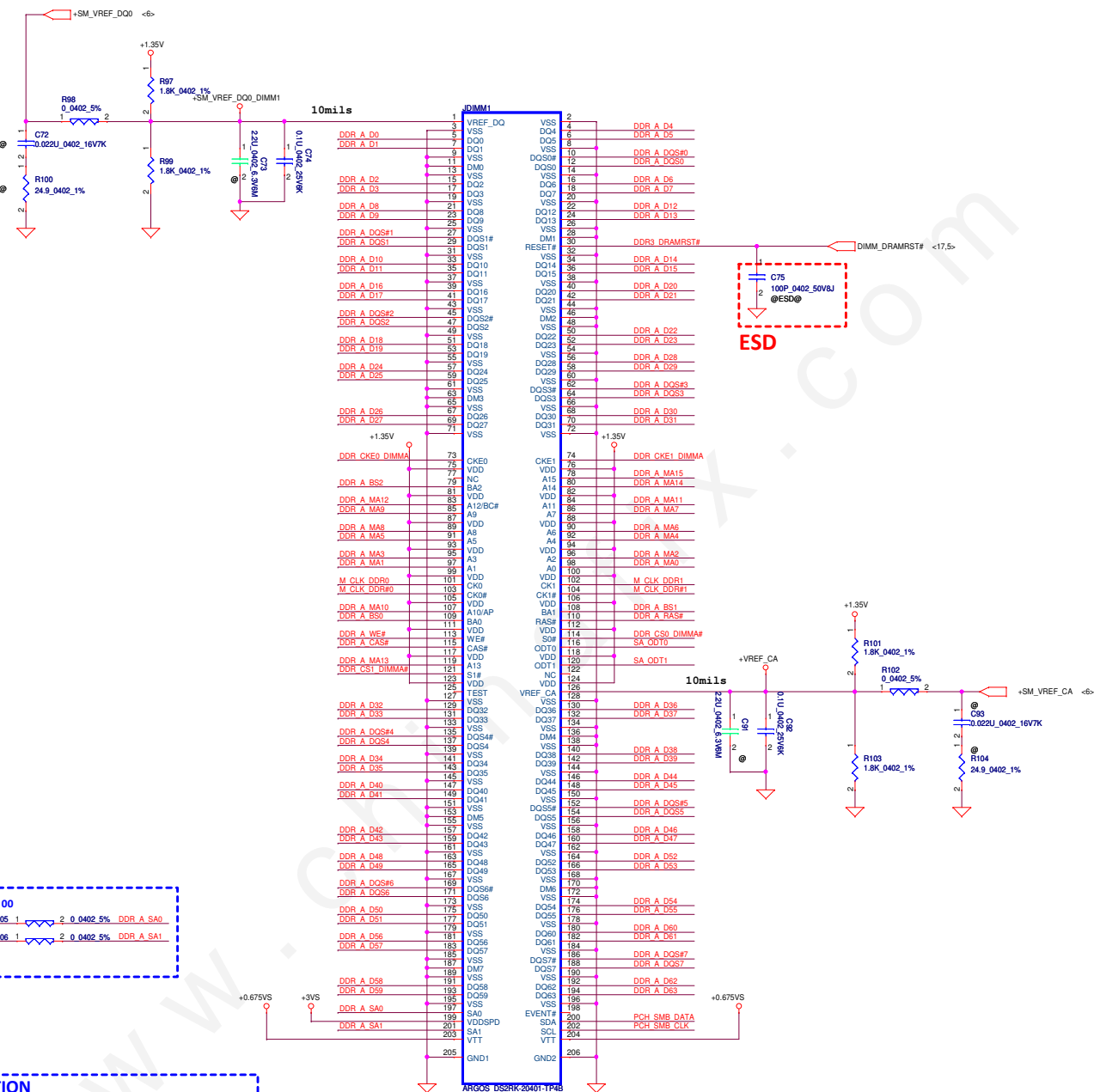
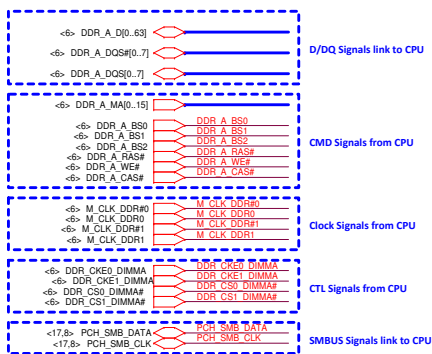
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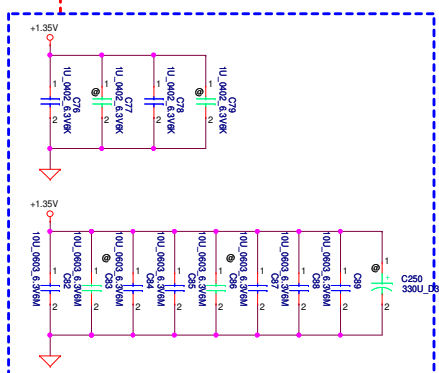
CFG Straps for Processor



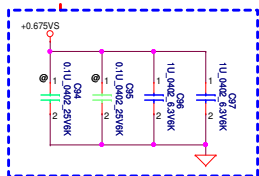
DIMM1 Reverse Type Near CPU



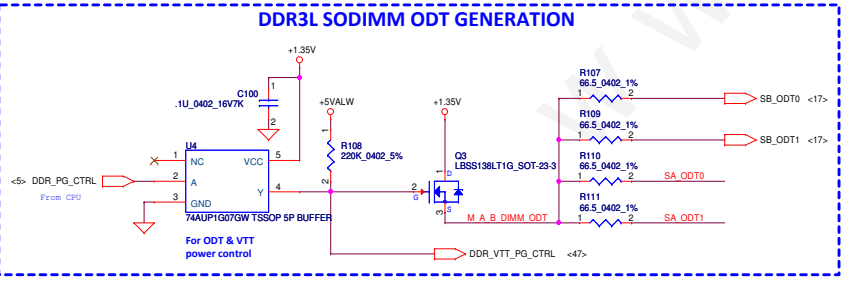
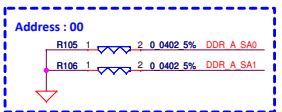
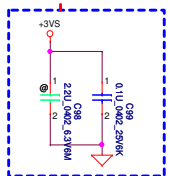
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



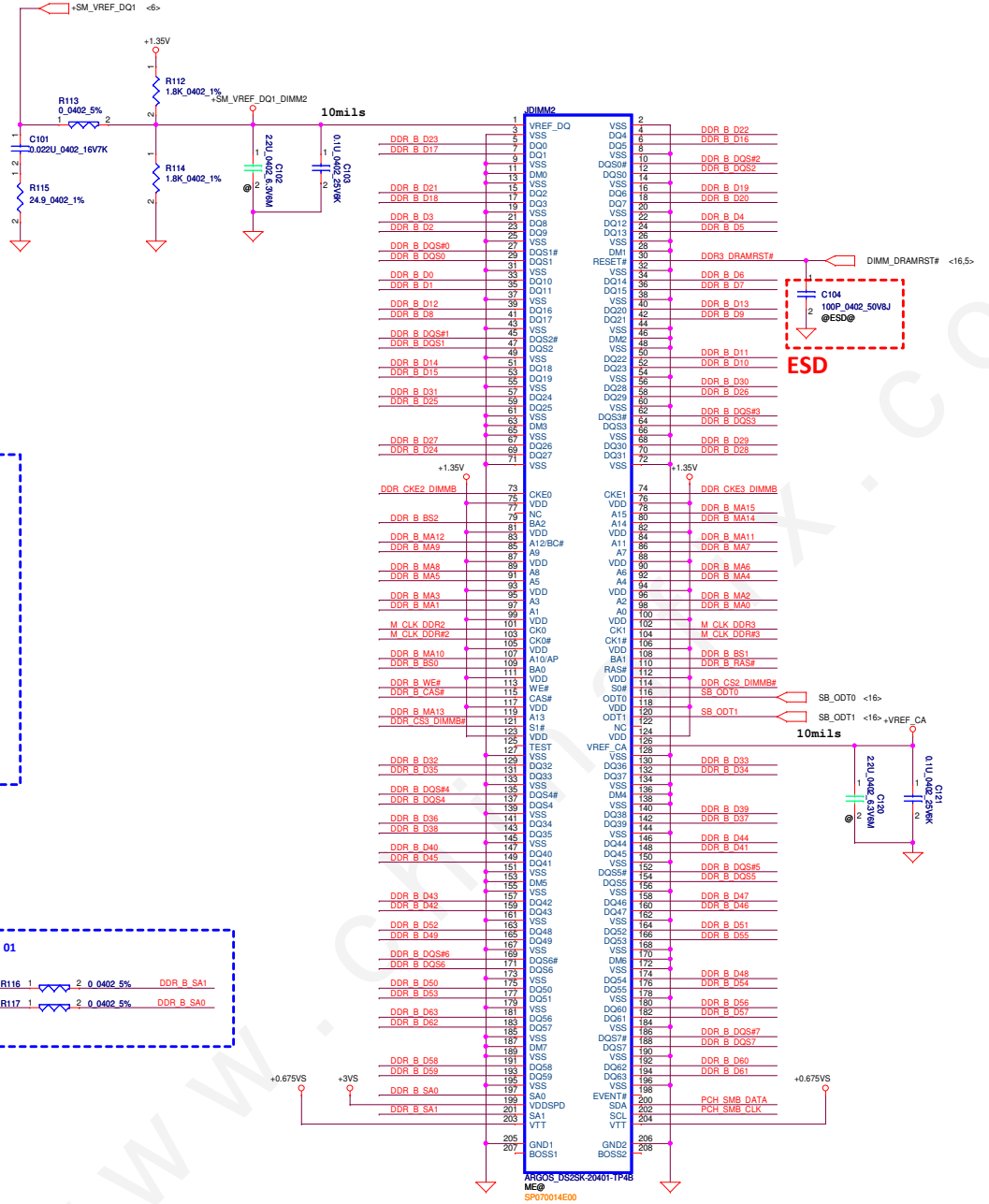
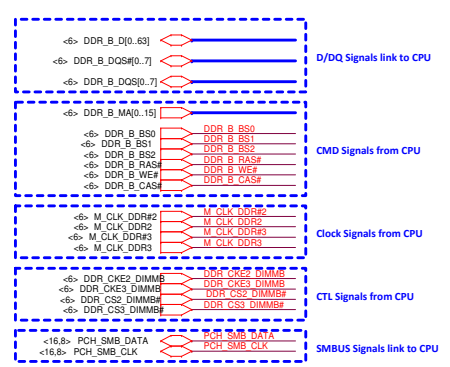
Layout Note:
Place near JDIMM1.199



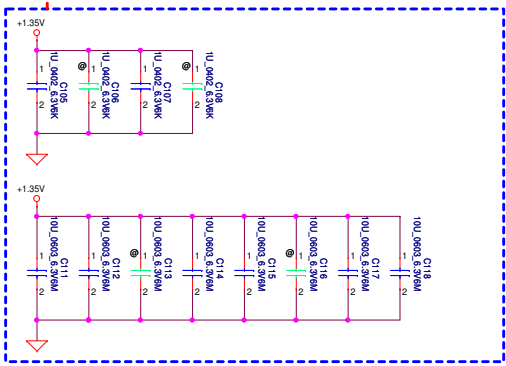
ARGOS_DS98K-2041-TP46
ME@
SP070014000

Interleaved Memory

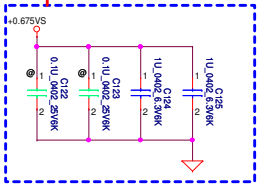
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Issued Date	2011/06/24	Deciphered Date			
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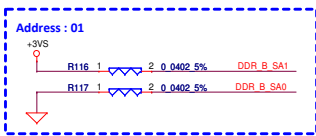
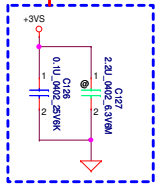
Layout Note:
Place near JDIMM2



Layout Note:
Place near JDIMM2.203,204



Layout Note:
Place near JDIMM2.199



Interleaved Memory

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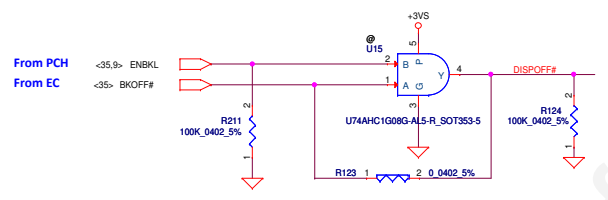
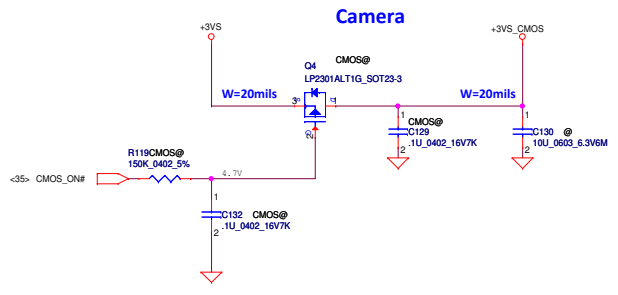
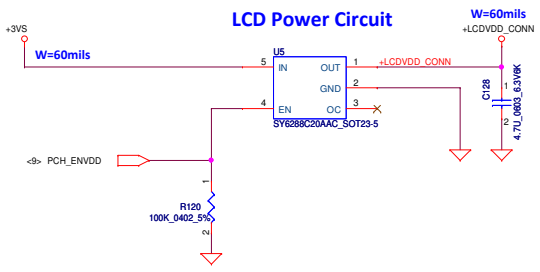
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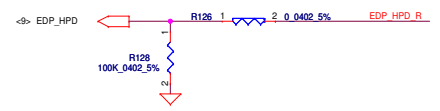


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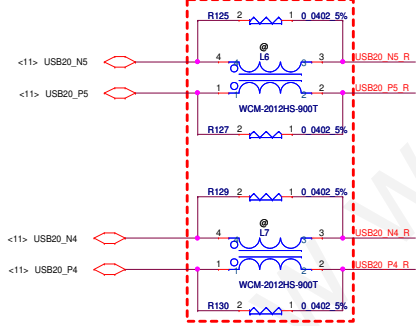
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eDP CONN.



Camera

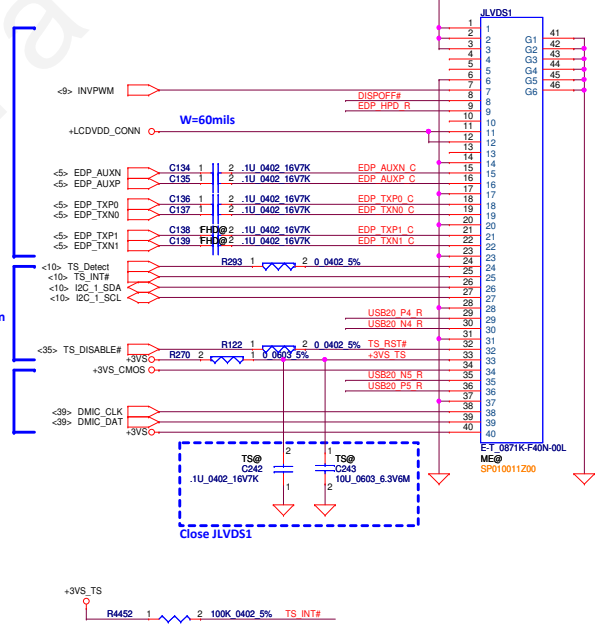


Touch Screen

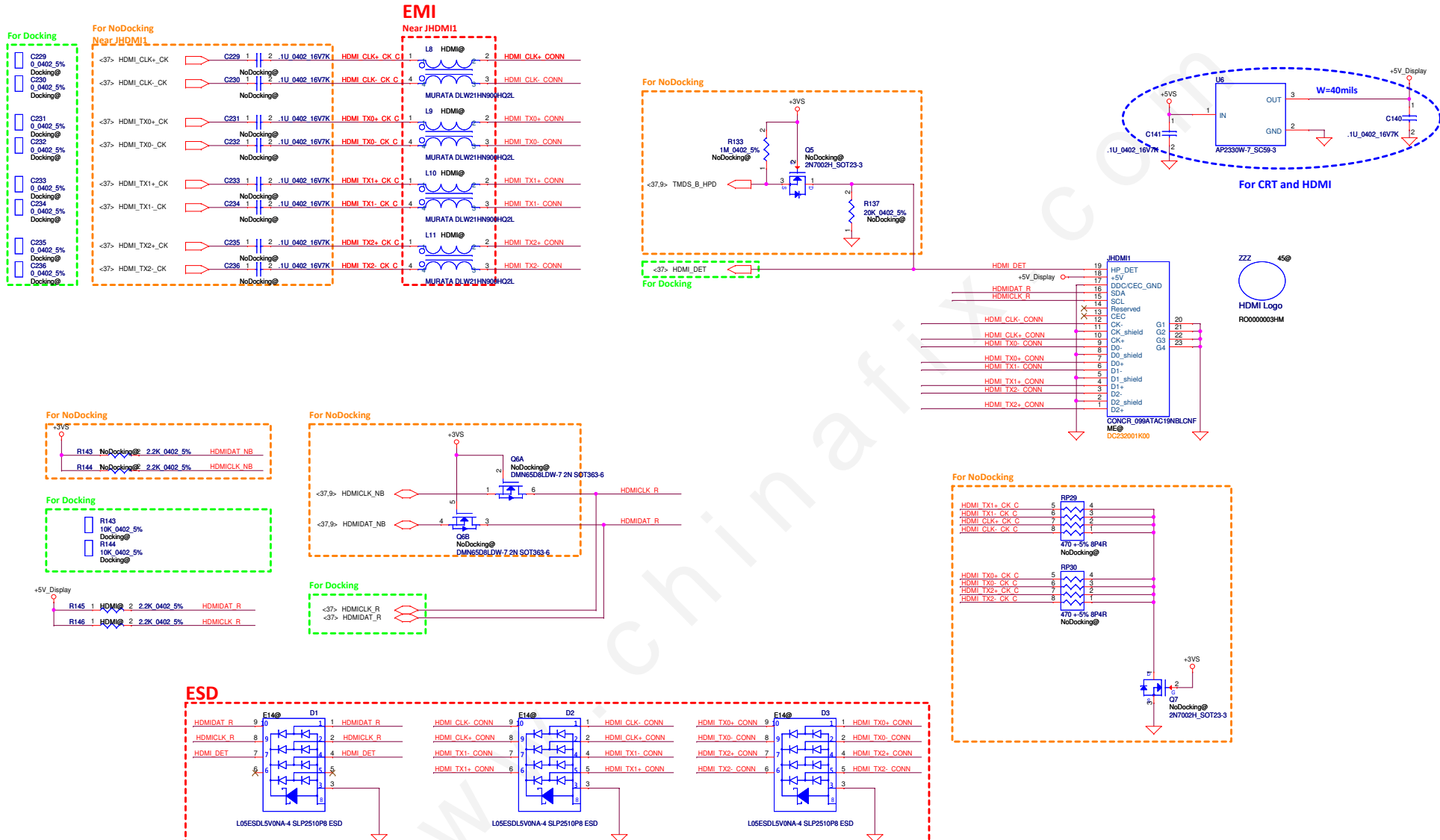
Reserve T33 for Presence Detect

Touch Screen

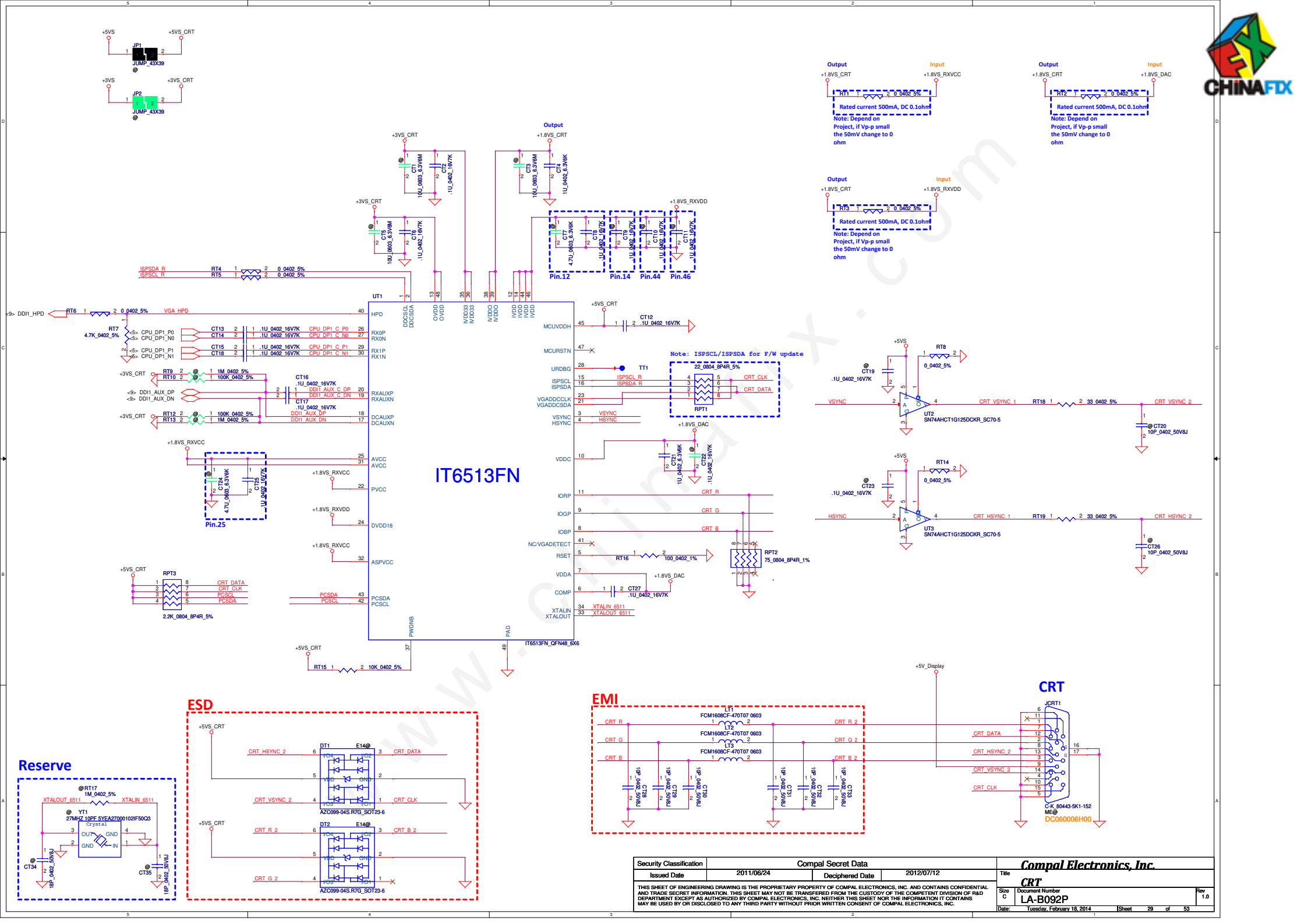
Camera DMIC



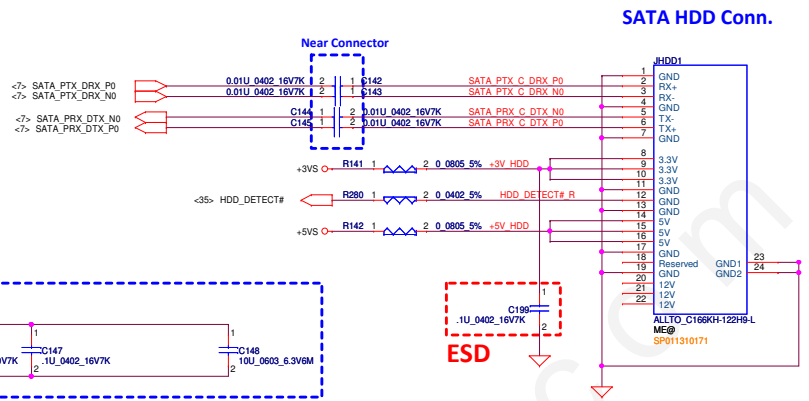
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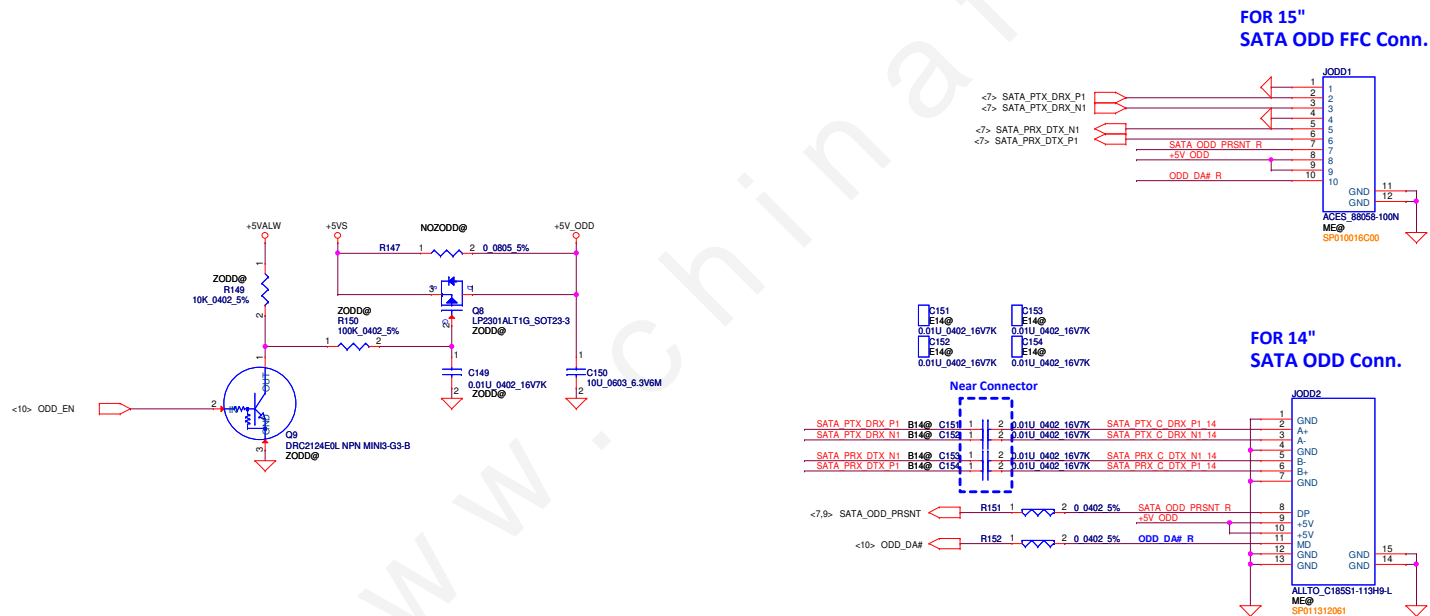
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HDD

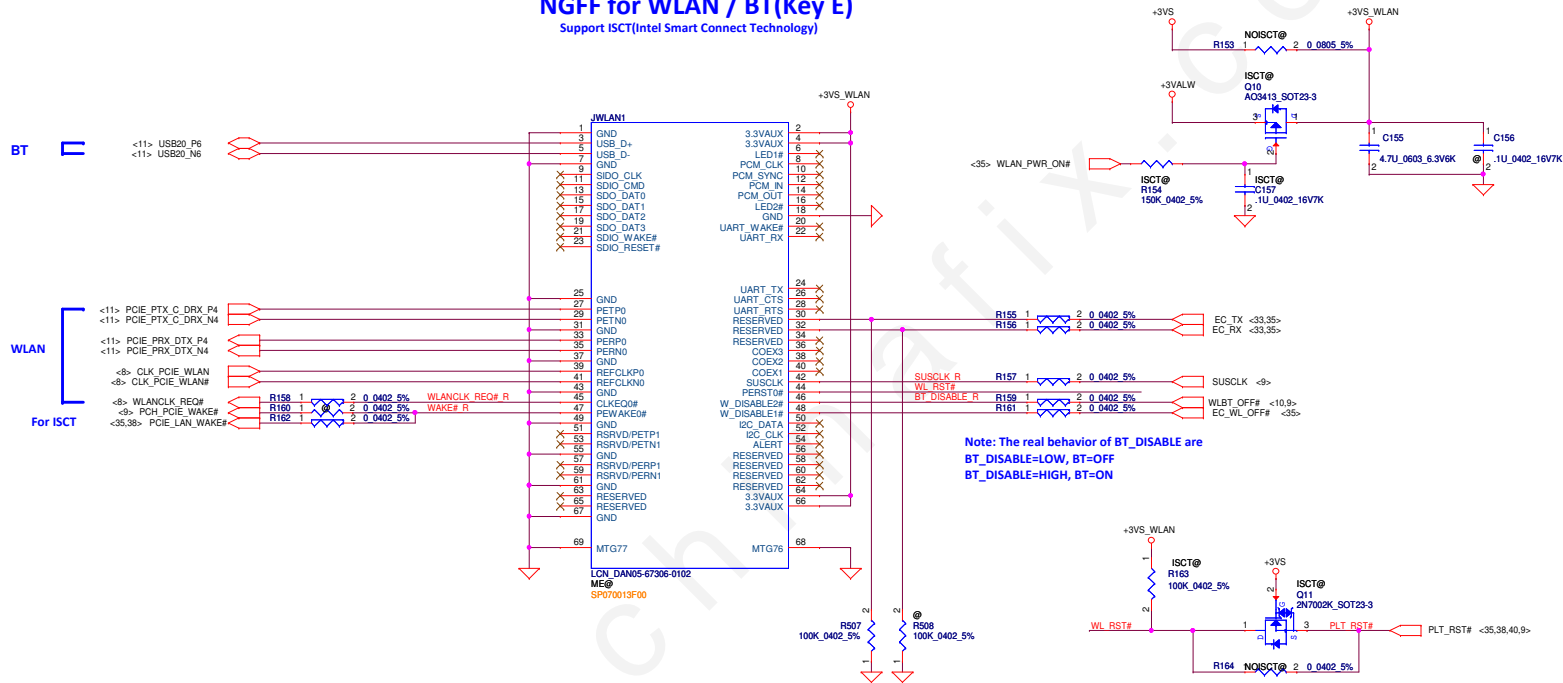


ODD



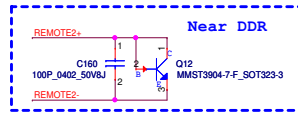
NGFF for WLAN / BT(Key E)

Support ISCT(Intel Smart Connect Technology)

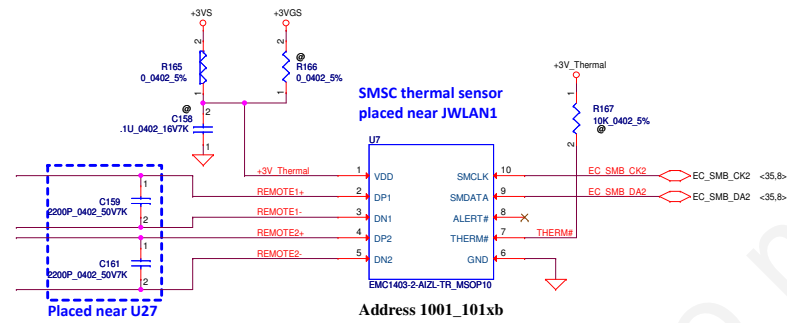


Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

3 Channel

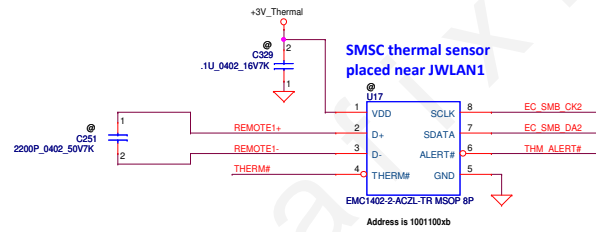


REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

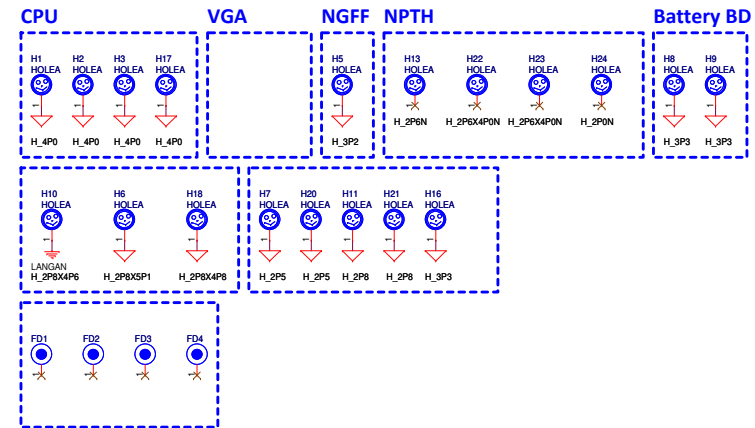
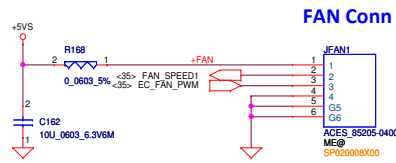


Address 1001_101xb

2 Channel



Address is 1001100xb

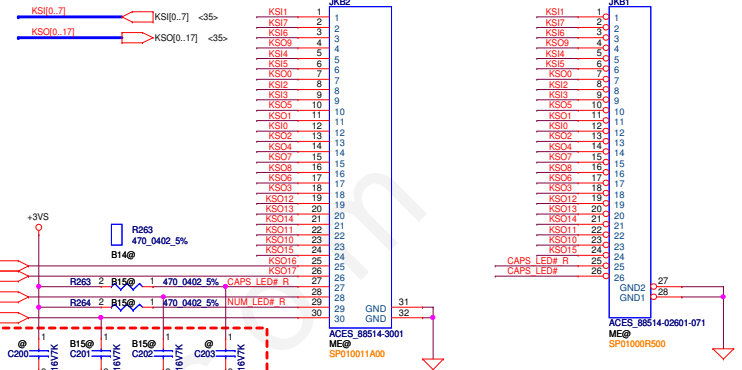
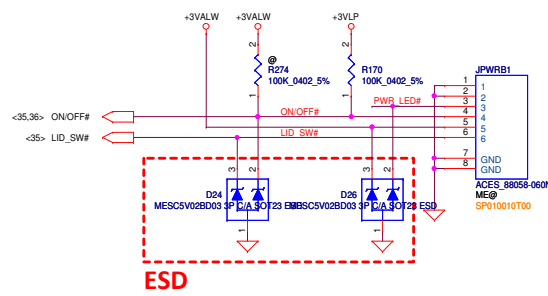
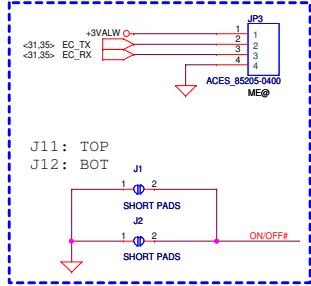




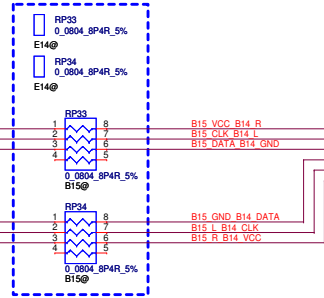
KB For B15

KB For B14/E14

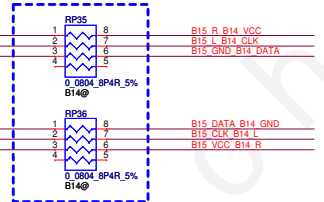
For Debug



For B15/E14



For B14

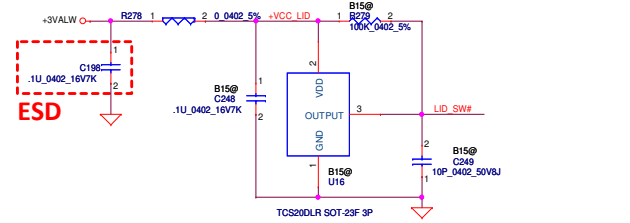
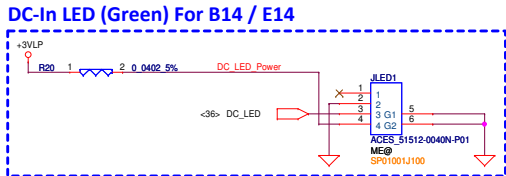
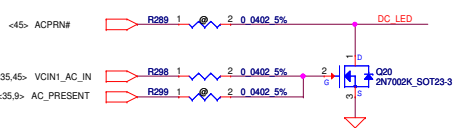
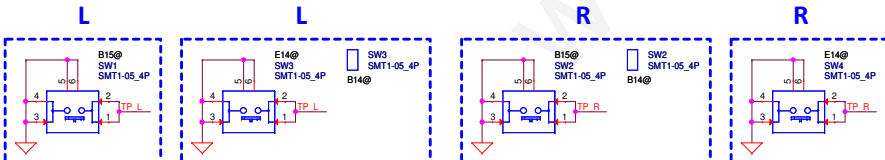


For B15/E14 TP module(100*50)

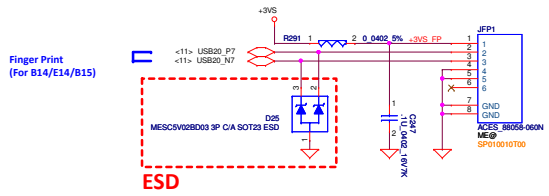
1	1	VCC	1	VCC
2	2	CLK	2	CLK
3	3	DAT	3	DAT
4	4	GND	4	L
5	5	L	5	R
6	6	R	6	GND

For B14 TP module(84*42)

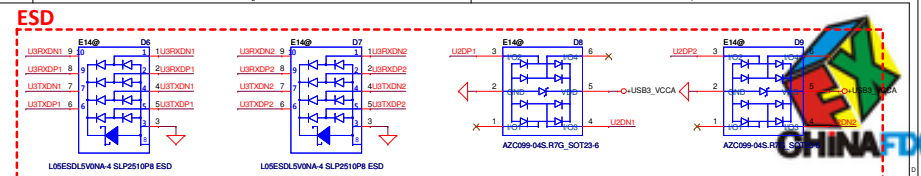
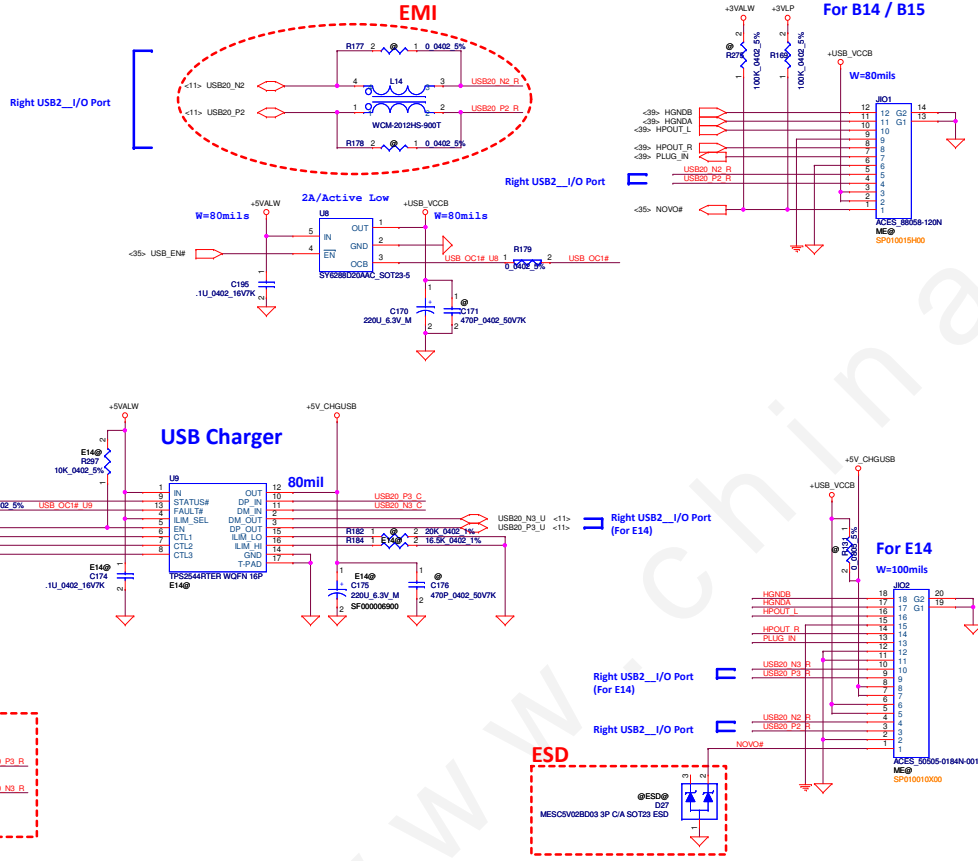
6	1	VCC	1	VCC
5	2	CLK	2	CLK
4	3	DAT	3	DAT
3	4	GND	4	L
2	5	L	5	R
1	6	R	6	GND



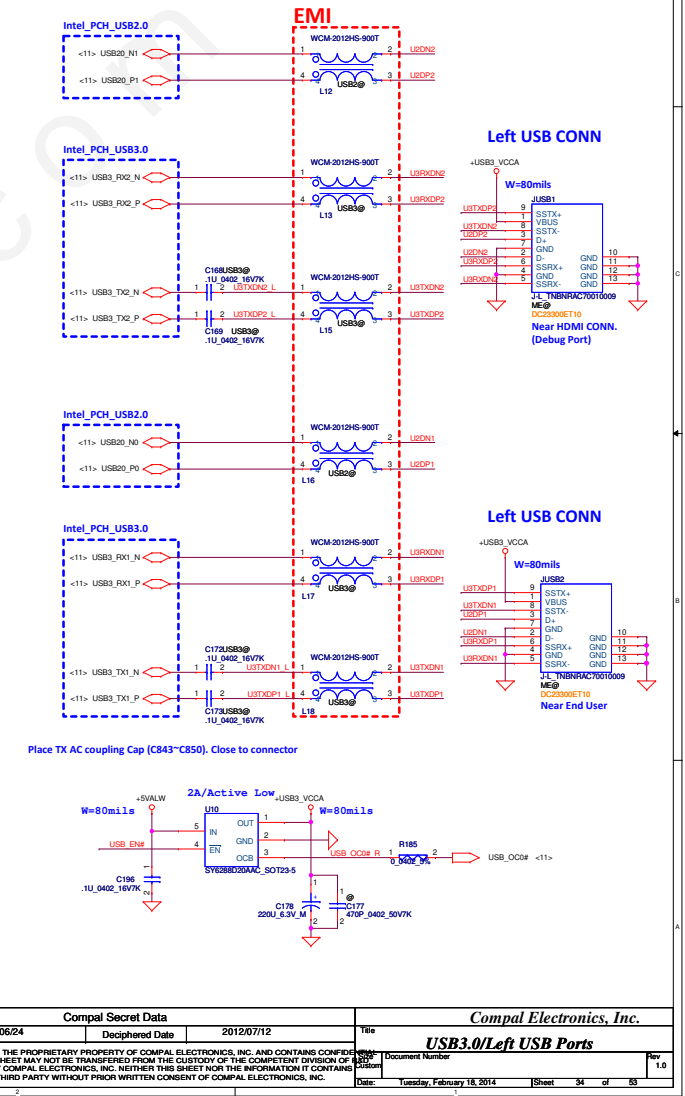
Finger Print



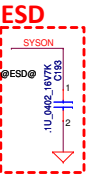
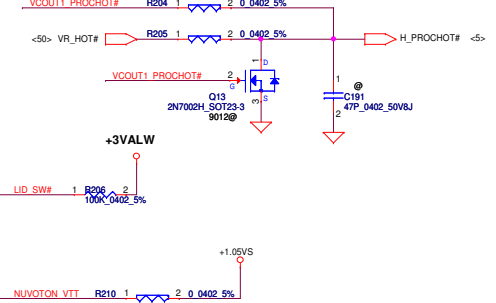
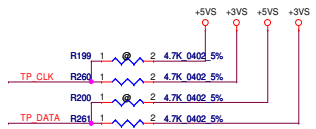
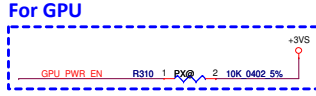
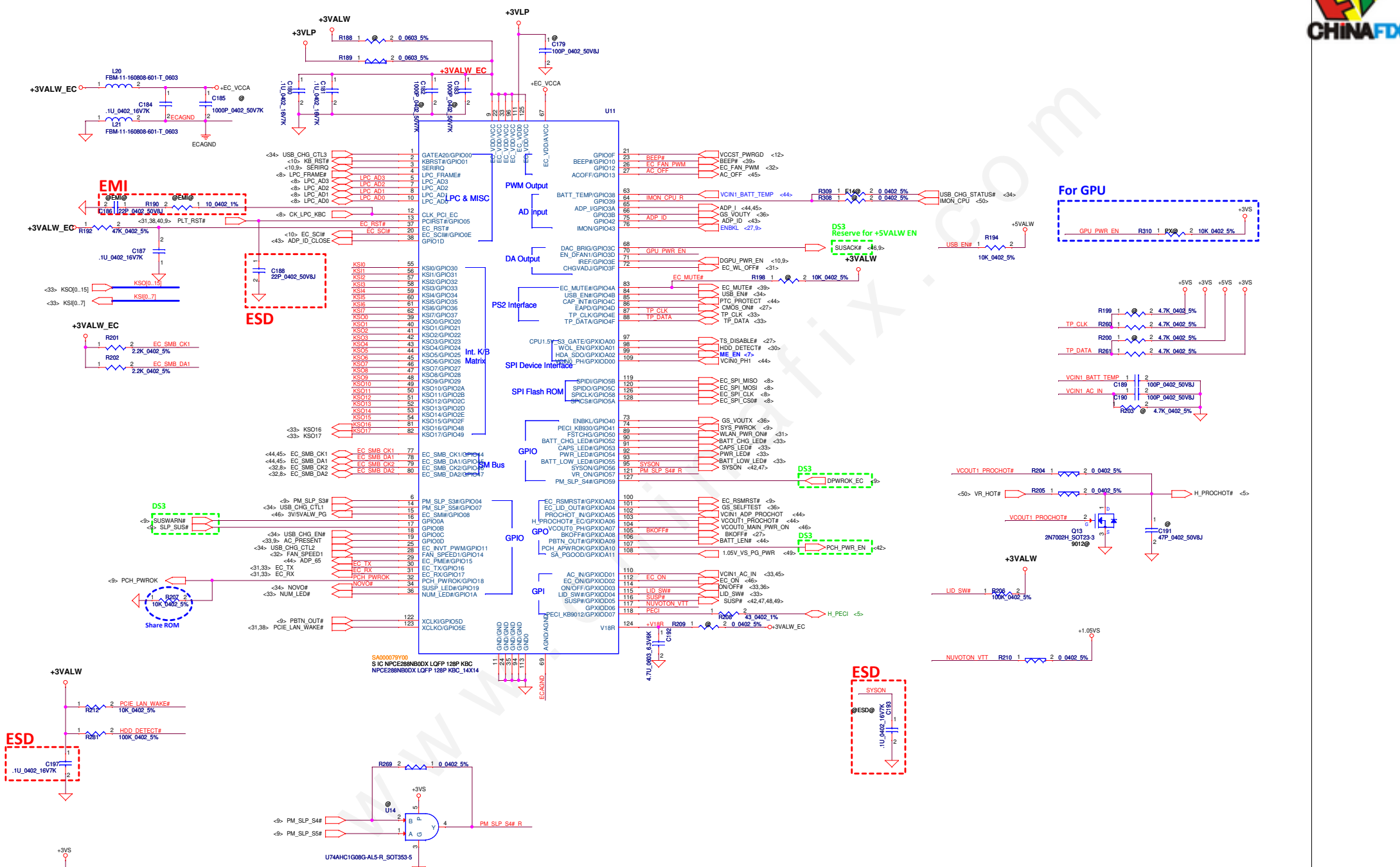
USB2.0_Port

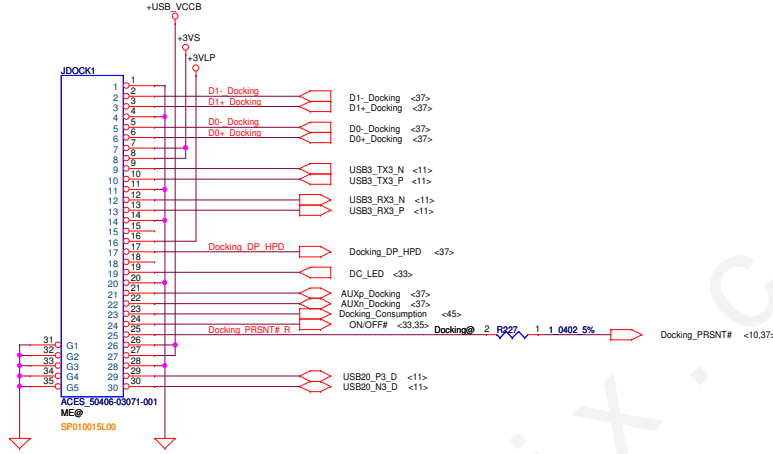


USB3.0_Port

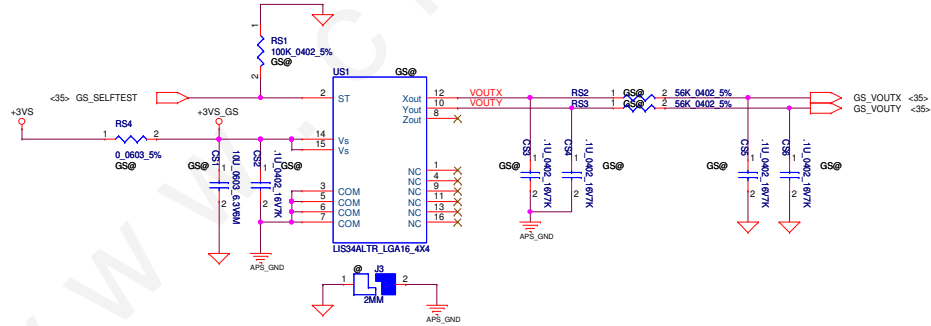


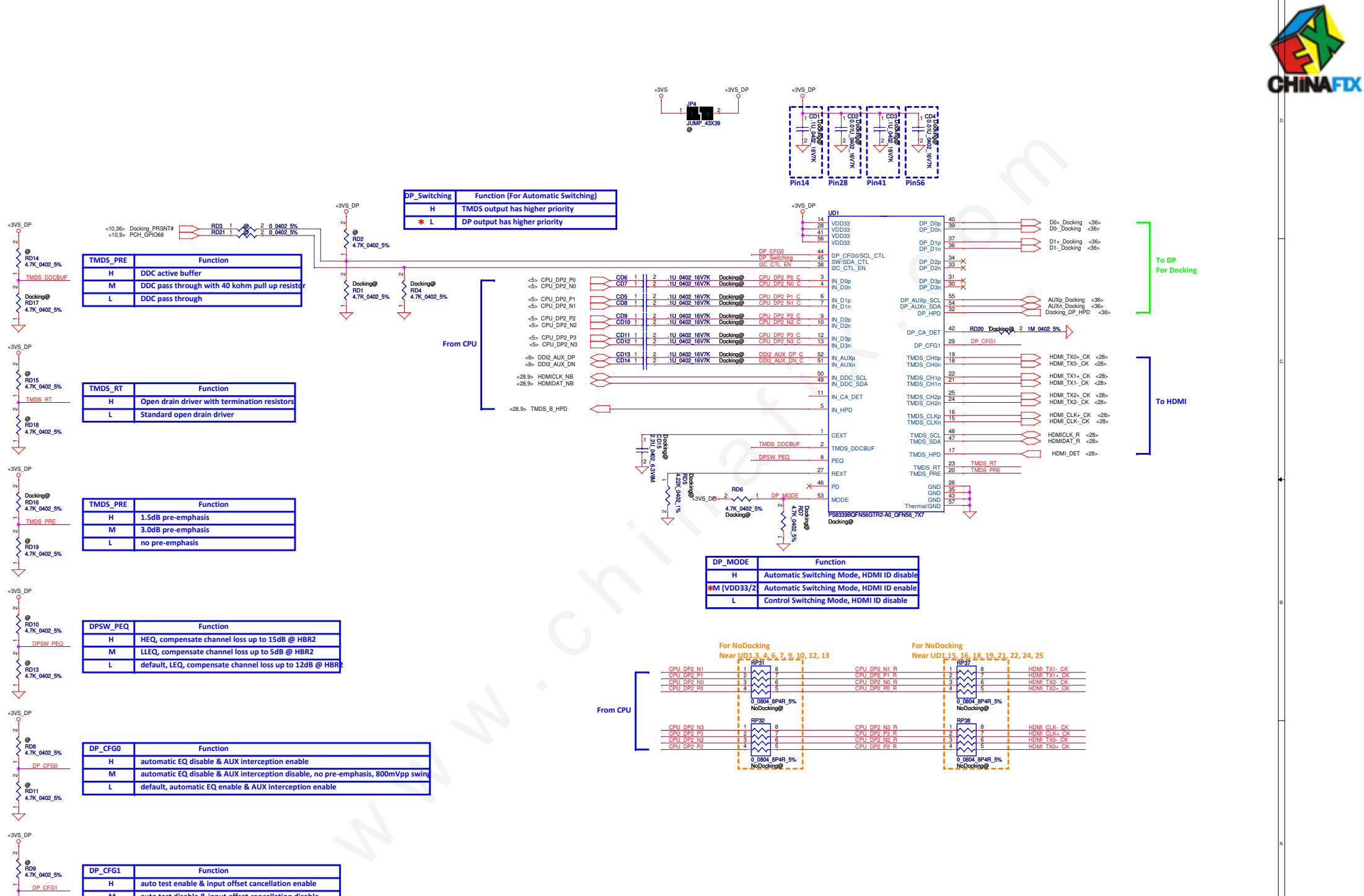
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				USB3.0/Left USB Ports	
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APS (G-Sensor)





DP_Switching	Function (For Automatic Switching)
H	TMDS output has higher priority
* L	DP output has higher priority

TMDS_PRE	Function
H	DDC active buffer
M	DDC pass through with 40 kohm pull up resistor
L	DDC pass through

TMDS_RT	Function
H	Open drain driver with termination resistors
L	Standard open drain driver

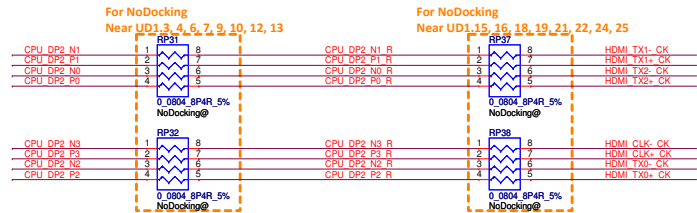
TMDS_PRE	Function
H	1.5dB pre-emphasis
M	3.0dB pre-emphasis
L	no pre-emphasis

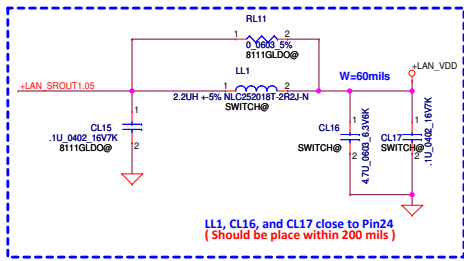
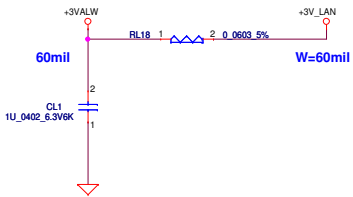
DPSW_PEQ	Function
H	HEQ, compensate channel loss up to 15dB @ HBR2
M	LLEQ, compensate channel loss up to 5dB @ HBR2
L	default, LEQ, compensate channel loss up to 12dB @ HBR2

DP_CFG0	Function
H	automatic EQ disable & AUX interception enable
M	automatic EQ disable & AUX interception disable, no pre-emphasis, 800mVpp swing
L	default, automatic EQ enable & AUX interception enable

DP_CFG1	Function
H	auto test enable & input offset cancellation enable
M	auto test disable & input offset cancellation disable
L	default, auto test disable & input offset cancellation enable

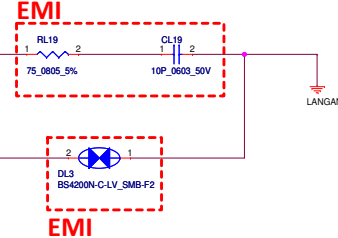
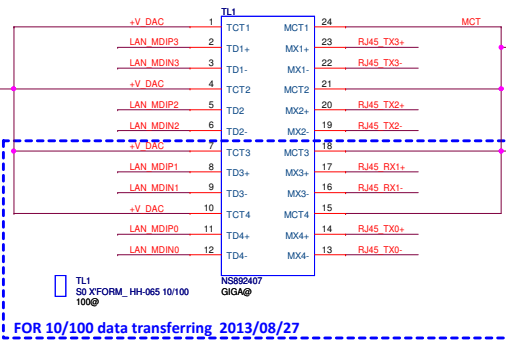
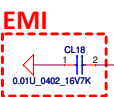
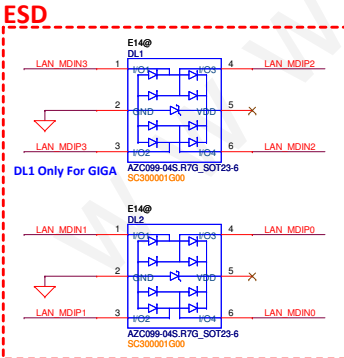
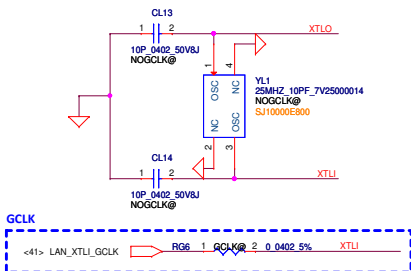
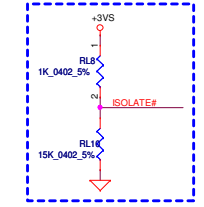
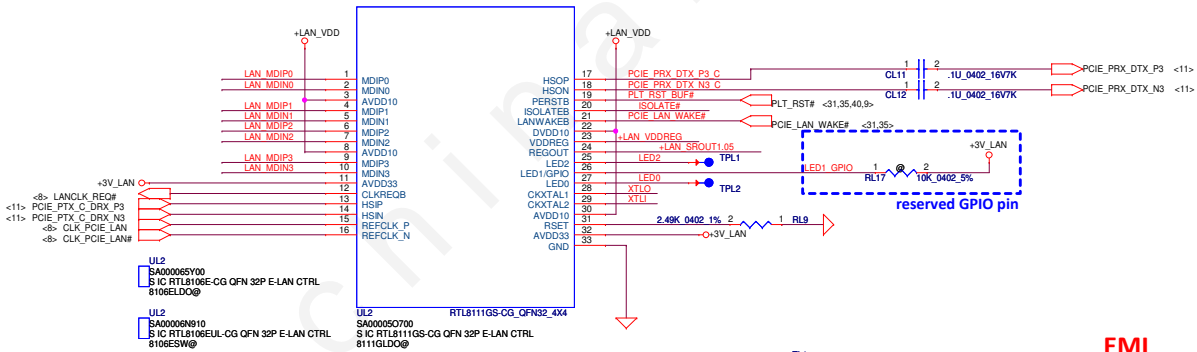
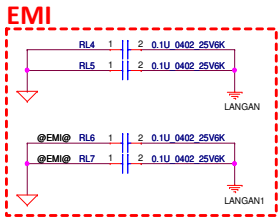
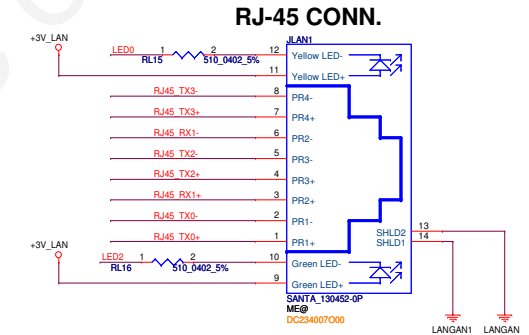
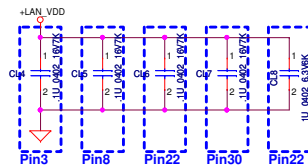
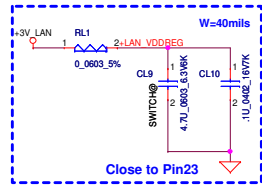
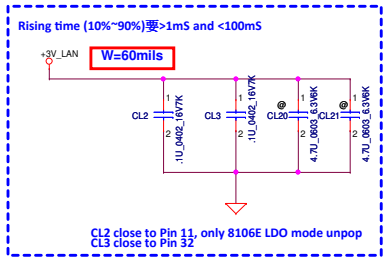
DP_MODE	Function
H	Automatic Switching Mode, HDMI ID disable
*M (VDD33/2)	Automatic Switching Mode, HDMI ID enable
L	Control Switching Mode, HDMI ID disable

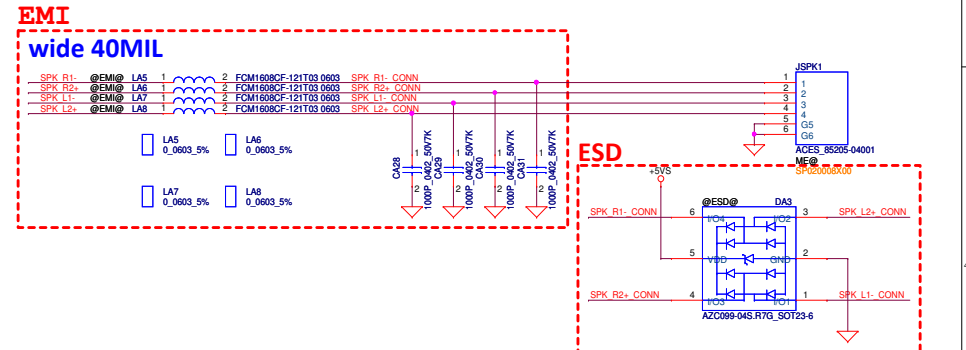
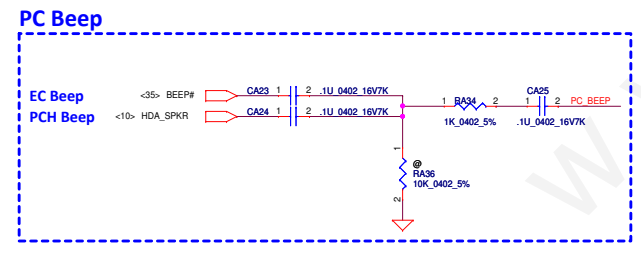
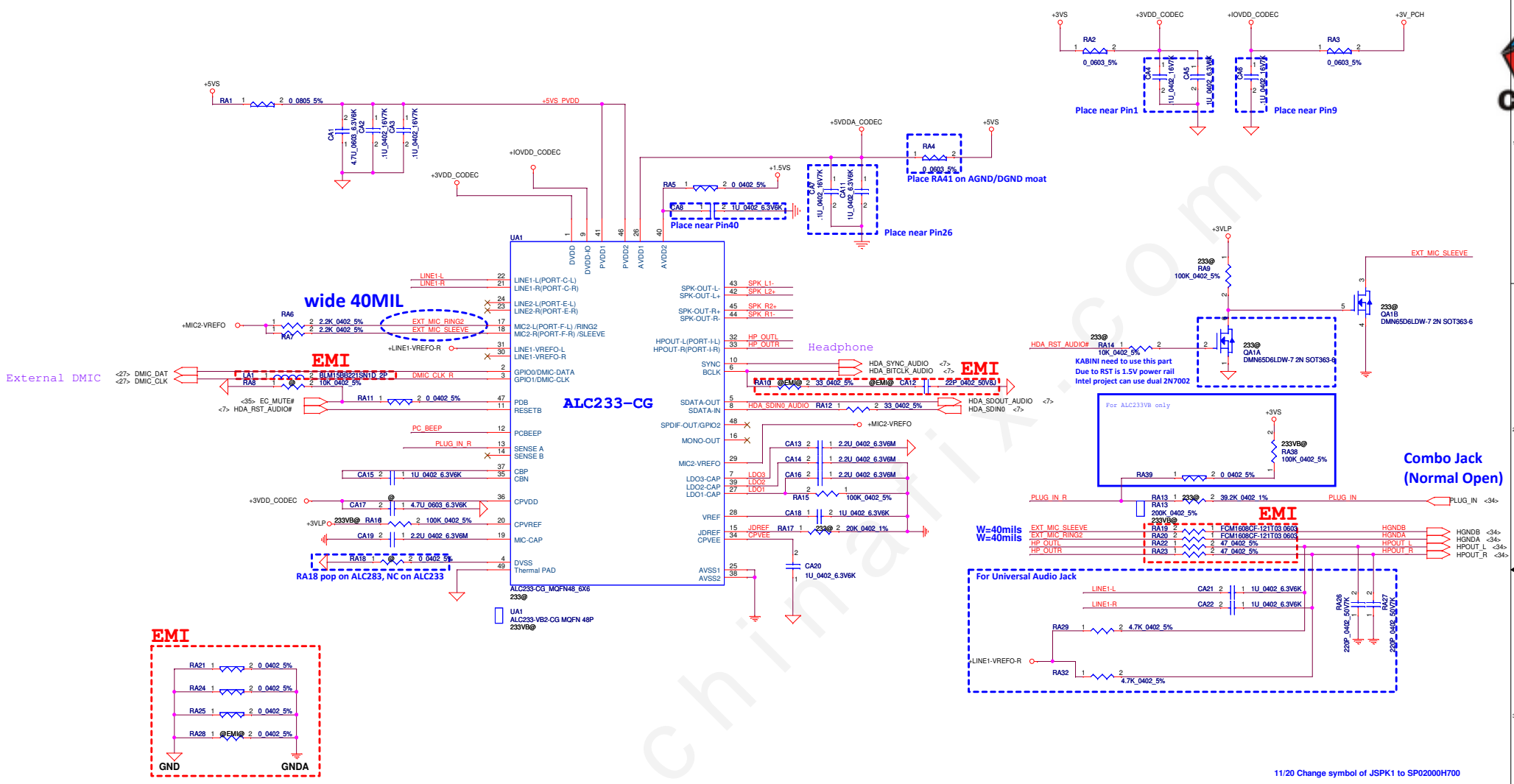




	1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005Y700	RTL8111G	LDO	X	X	X	O
	RTL8111G	External	X	X	X	O
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X
SA000065Y00	RTL8106E	LDO	X	X	X	X

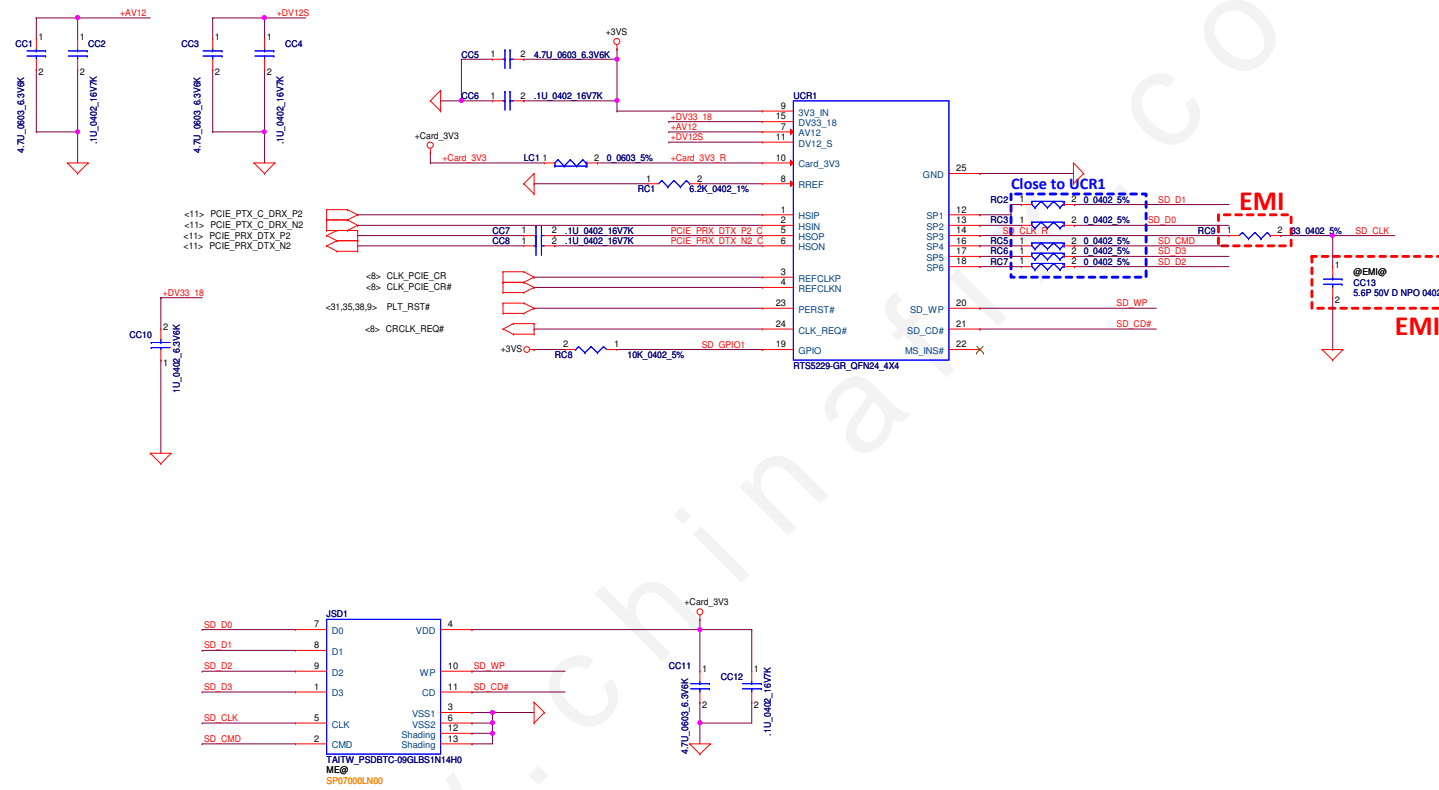
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.

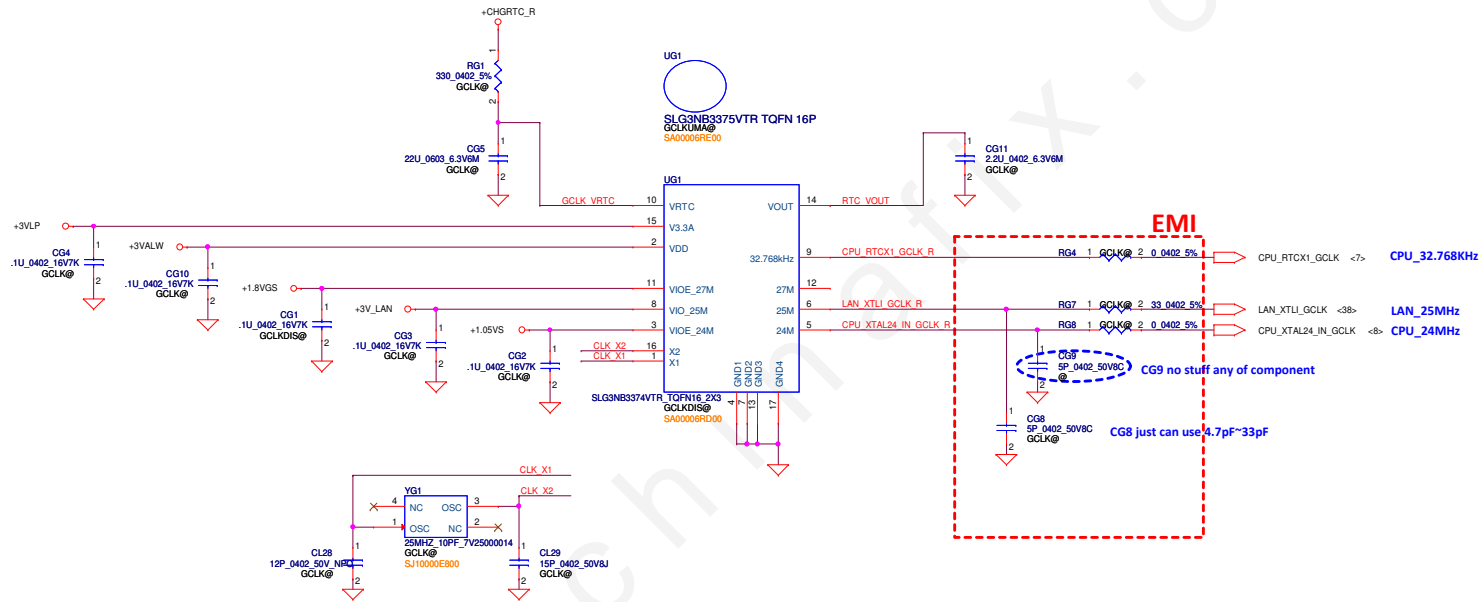




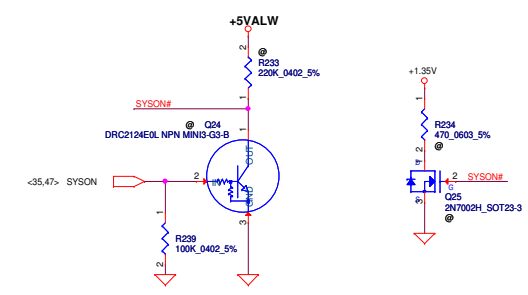
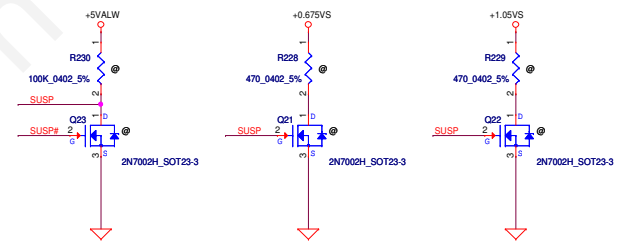
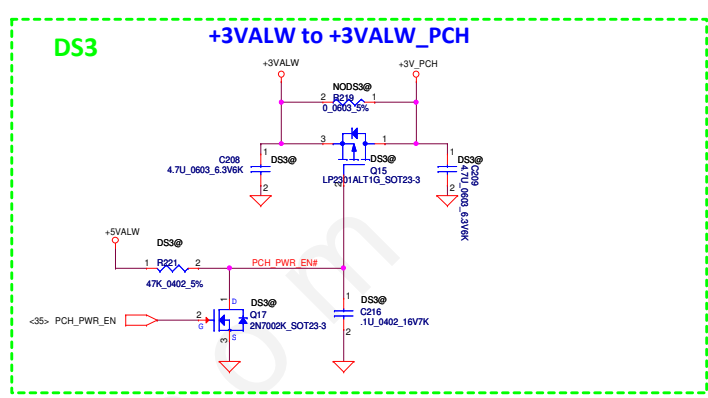
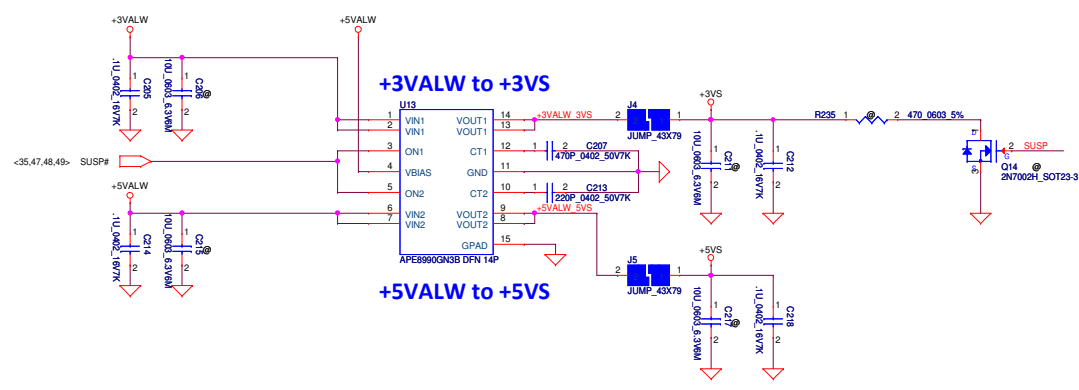
11/20 Change symbol of JSPK1 to SP2000H700

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Size	C	Document Number	LA-B092P	Rev
Date	Wednesday, February 18, 2014	Sheet	39 of 53	1.0

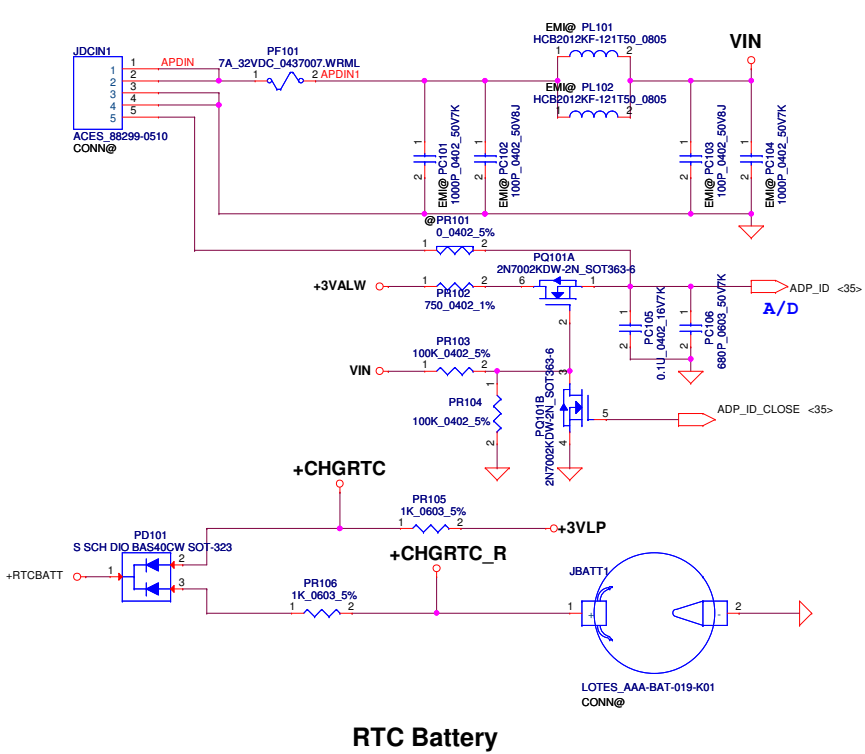




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				GCLK
				LA-B092P
Date: Tuesday, February 18, 2014				Rev 1.0
Sheet 41 of 53				



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Size	C	Document Number	LA-B092P	Rev
Date:	Tuesday, February 18, 2014	Sheet	42 of 53	1.0

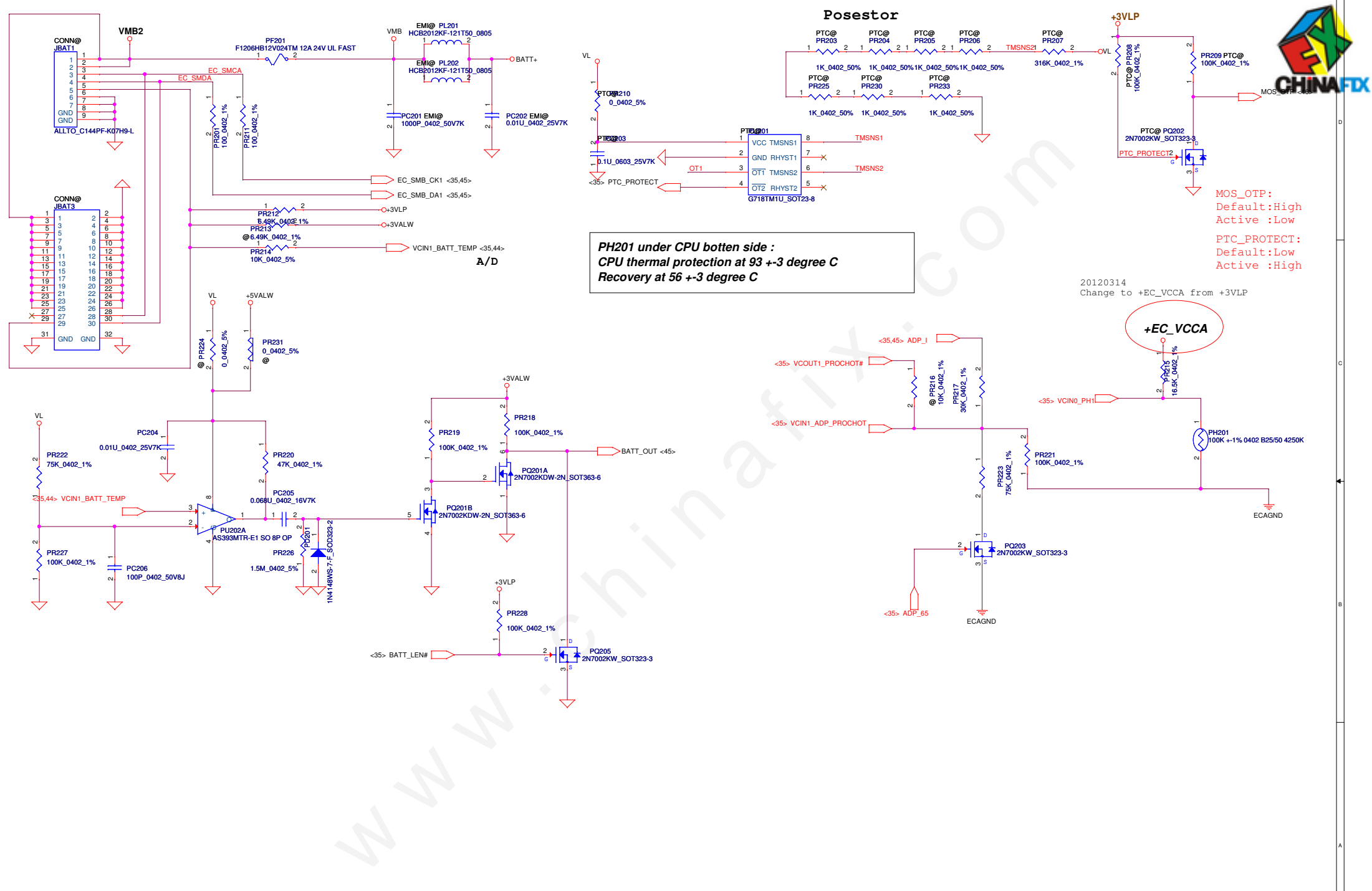


ADP_ID		
AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

RTC Battery

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				PWR DCIN / RTC Battery
				Rev
				BE_BDW 1.0
				Date: Tuesday, February 18, 2014 Sheet 43 of 53



PH201 under CPU bottom side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C

20120314
 Change to +EC_VCCA from +3VLP

MOS_OTP:
 Default:High
 Active :Low

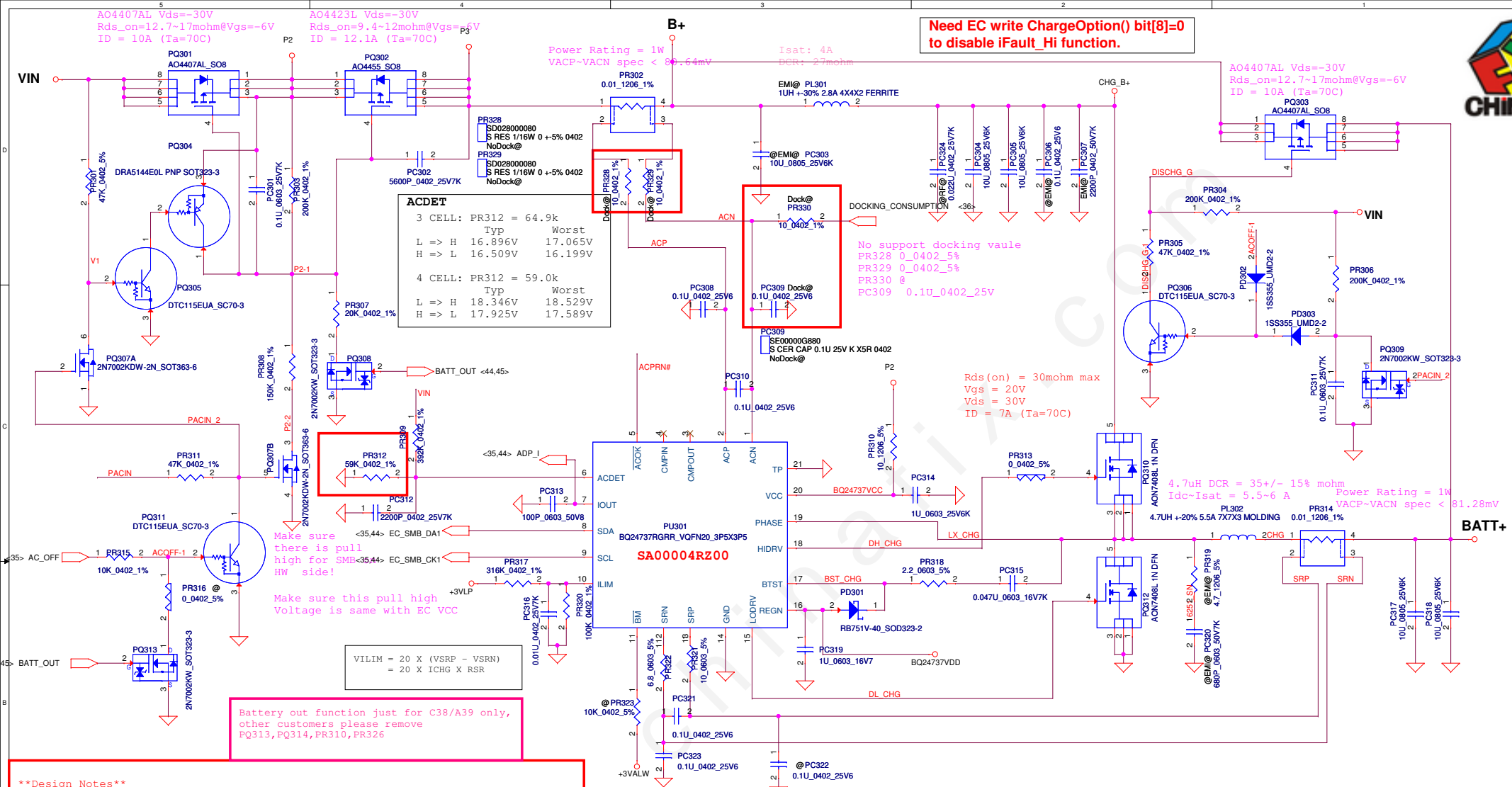
PTC_PROTECT:
 Default:Low
 Active :High

135W: 150W(Turbo_V=1.2) active 135W(Turbo_V=1.072) recovery
90W : 100W(Turbo_V=1.2) active 90W(Turbo_V=0.903) recovery
65W : 70W(Turbo_V=1.2) active 65W(Turbo_V=0.918) recovery
45W : 65W(Turbo_V=1.2) active 45W(Turbo_V=0.829) recovery

Security Classification	Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Customer
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				BE BDW
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Need EC write ChargeOption() bit[8]=0 to disable iFault_HI function.



Make sure there is pull high for SMB<35,44> EC_SMB_DA1 HW side!

Make sure this pull high Voltage is same with EC VCC

Battery out function just for C38/A39 only, other customers please remove PQ313, PQ314, PR310, PR326

****Design Notes****

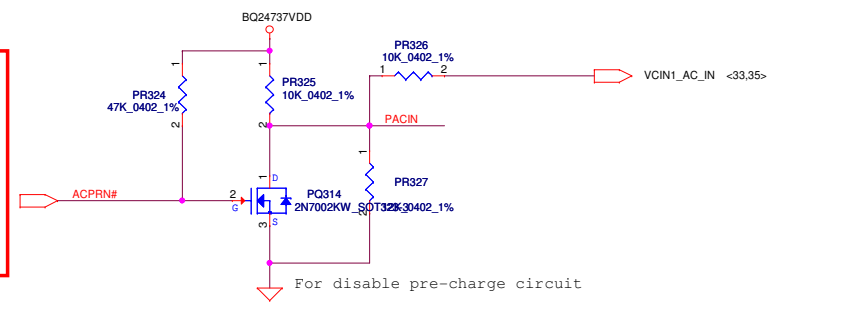
Maximum Charging current 2.0A
 Battery discharge power 55W.
 #Register Setting
 1. 0X12 bit8 set 0 (default 1) to disable IFAULT HI if add ISN choke
 2. 0X12 bit3 set 1 (default 0) to enable turbo boost function
 3. 0X12 bit[12:11] set 00 (default 11) to set BAT
 Depletion Comparator Threshold
 Falling Threshold = 59.19% of voltage regulation limit (~2.486V/cell)
 4. Disable turbo when AC only
 #Circuit Design
 1. Make sure there is pull high for SMB on HW side
 2. Use 10X10 choke and 3X3 H/L side MOSFET
 Charge current 2.0A
 Power loss : 1.82W
 Power density : 0.81 (15X15)
 3. If use 4S per cell 4.35V battery, need change PR313 to 59K for ACDET setting)
 4. For hybrid design, need double check PQ301,PQ302,PQ303,PQ309 component rating
 #Protect function
 1. ACOVP : ACDET voltage > 3.15V
 2. Charger timeout : No communication within 175s(default)
 3. ACOC : 3.33 X Input current DAC setting(default)
 4. CHGOCP : 3/4.5/6A based on current setting
 5. BATOVP : 104%
 6. BATLOWV : 2.5V
 7. TSHUT : 155C
 8. IFAULT HI : 750mV (default)
 9. IFAULT LOW : 135mV (default)

Module model information
 BQ24737_V1.mdd for dual layer

Rds(on) = 30mohm max
 Vgs = 20V
 Vds = 30V
 ID = 7A (Ta=70C)

No support docking vaule
 PR328 0_0402_5%
 PR329 0_0402_5%
 PR330 @
 PC309 0.1U_0402_25V

4.7uH DCR = 35 +/- 15% mohm
 Idc-Isat = 5.5-6 A
 Power Rating = 1W
 VACP-VACN spec < 81.28mV



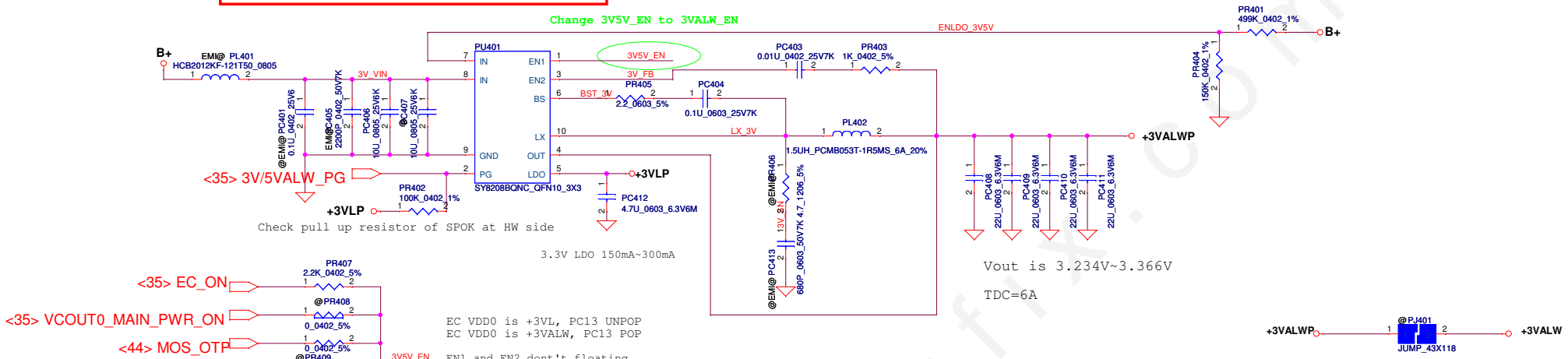
Security Classification		Compal Secret Data		Title	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Charger BQ24737	
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				BE_BDW	
				Date: Tuesday, February 18, 2014	Sheet 45 of 53

Module model information
SY8208E_V2.mdd

EN1 and EN2 don't floating

Change 3V5V_EN to 3VALW_EN

ENLDO_3V5V



<35> 3V/5VALW_PG

Check pull up resistor of SPOK at HW side

3.3V LDO 150mA~300mA

Vout is 3.234V~3.366V

TDC=6A

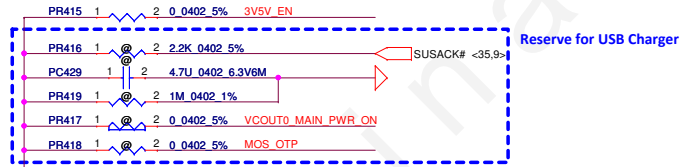
<35> EC_ON

<35> VCOUT0_MAIN_PWR_ON

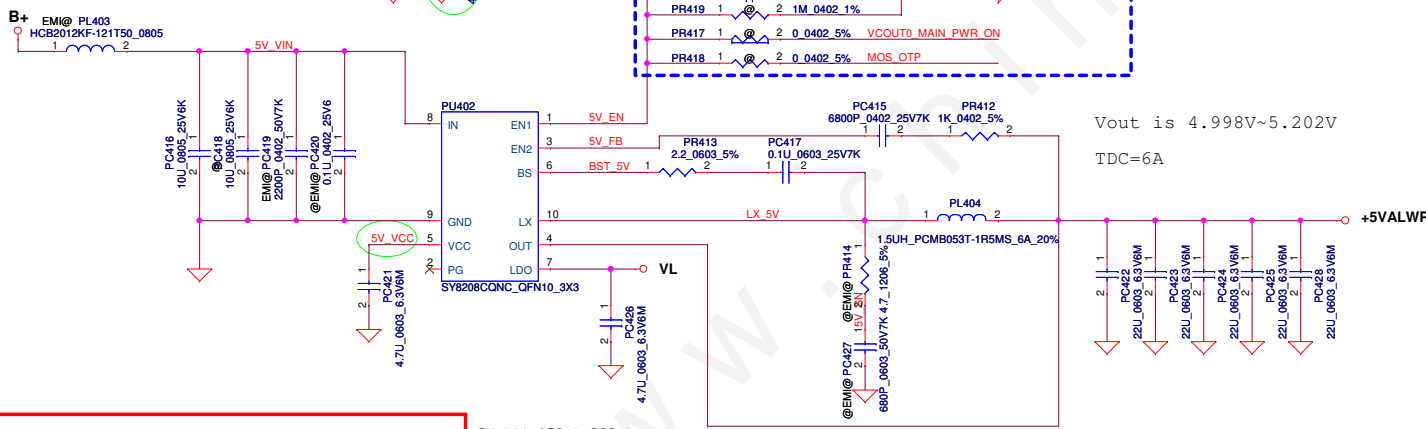
<44> MOS_OTP

EC VDD0 is +3VL, PC13 UNPOP
EC VDD0 is +3VALW, PC13 POP

EN1 and EN2 don't floating



Reserve for USB Charger



Vout is 4.998V~5.202V

TDC=6A

5V LDO 150mA~300mA



Module model information
SY8208C_V2.mdd

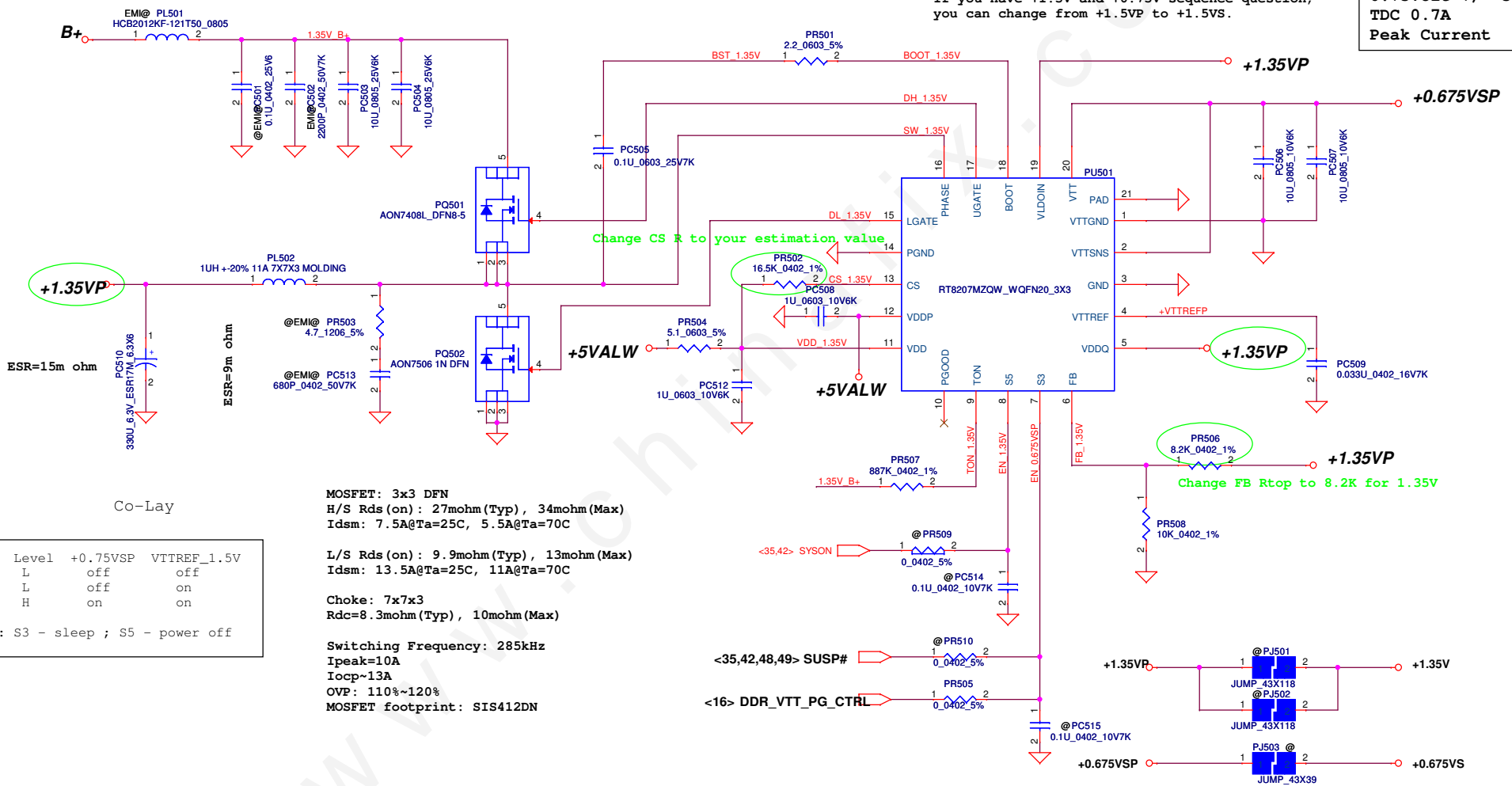
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title
				+3VALW/+5VALW
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Module model information
 RT8207M_v1.mdd For Single layer
 RT8207M_v2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
 If you have +1.5V and +0.75V sequence question,
 you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
 TDC 0.7A
 Peak Current 1A



Mode	Level	+0.75VSP	VITREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

MOSFET: 3x3 DFN
 H/S Rds (on) : 27mohm (Typ) , 34mohm (Max)
 Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

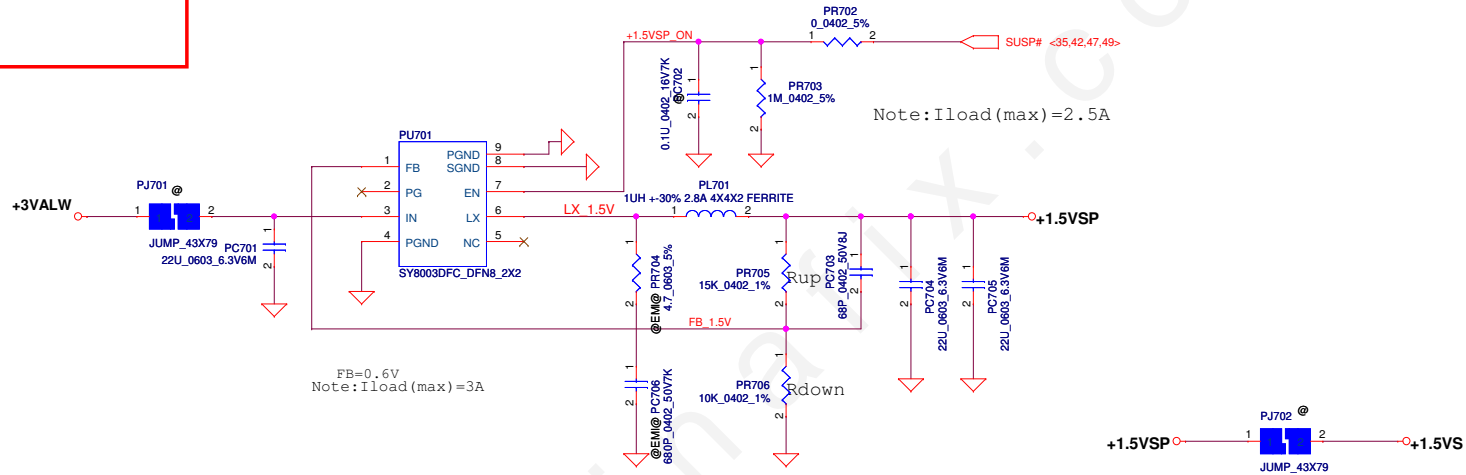
L/S Rds (on) : 9.9mohm (Typ) , 13mohm (Max)
 Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
 Rdc=8.3mohm (Typ) , 10mohm (Max)

Switching Frequency: 285kHz
 Ipeak=10A
 Iocp~13A
 OVP: 110%~120%
 MOSFET footprint: SIS412DN

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Issued Date	2011/06/24	Deciphered Date	2012/07/12	RT8207M	
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				Custom	1.0
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Module model information
SY8003_V1.mdd



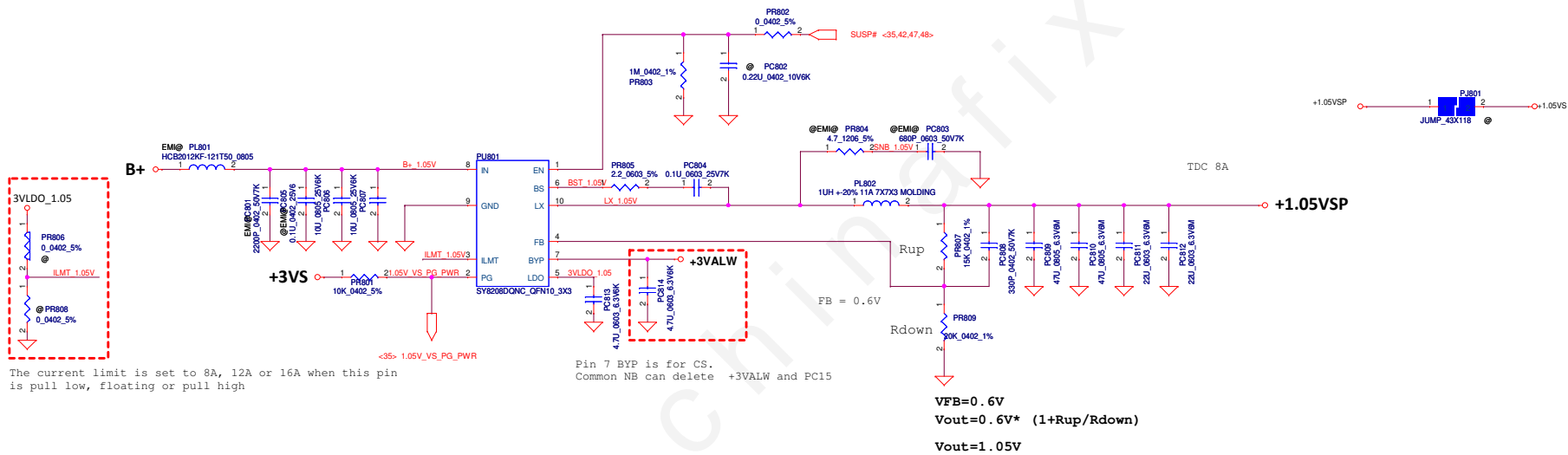
Note:
When design $V_{in}=5V$, please stuff snubber
to prevent V_{in} damage

$$V_{out}=0.6V * (1+R_{up}/R_{down})$$

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				Document Number	Rev
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Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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Module model information:
ISL95813 (for 15W & 28W CPU)

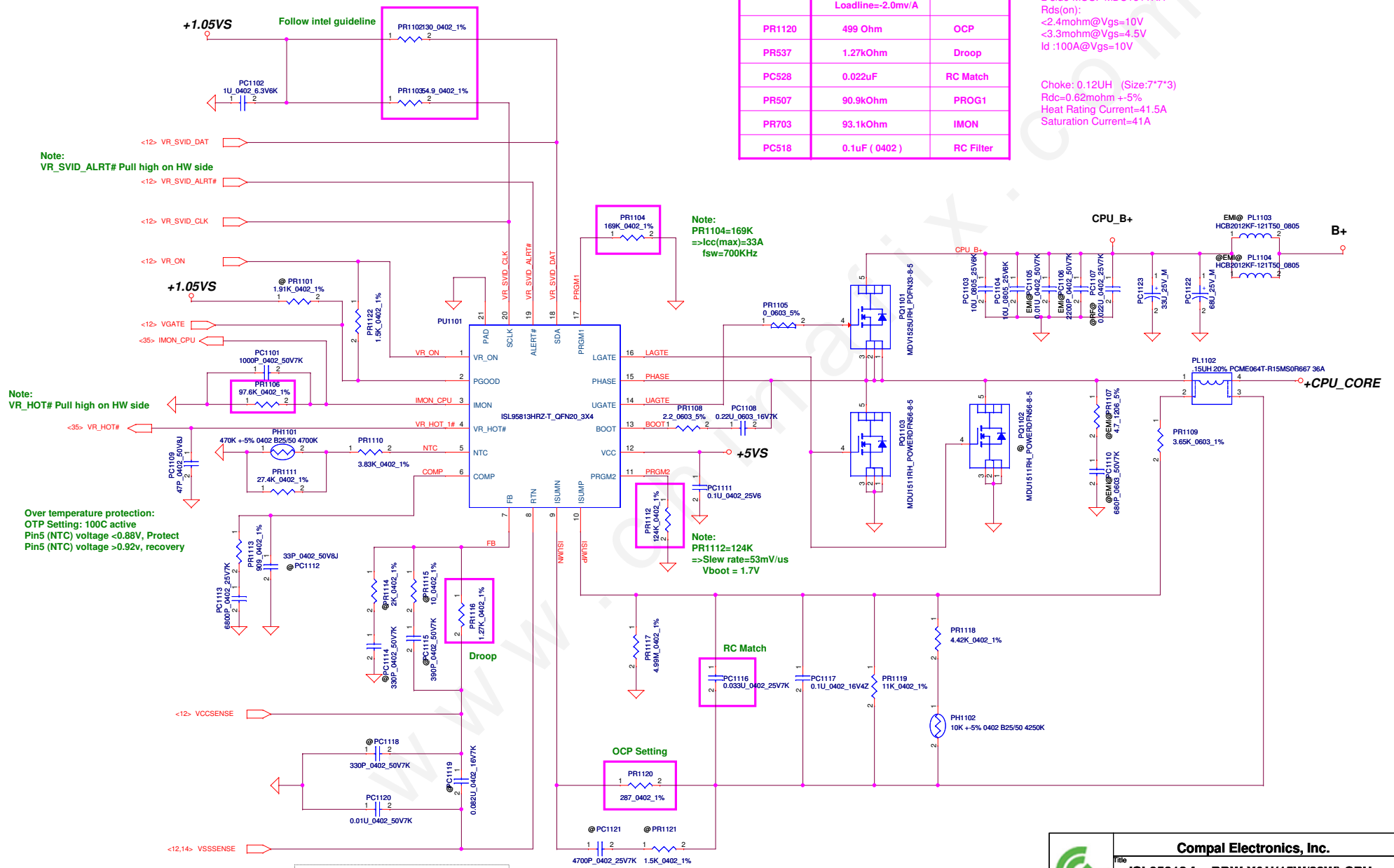
Base on BDW_PDDG Rev_0_73

Location	15W	Note
	TDC	
MAX	32A	
OCF	39A	
	Loadline=-2.0mv/A	
PR1120	499 Ohm	OCF
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Fdc=0.62mohm +5%
Heat Rating Current=41.5A
Saturation Current=41A



Note:
VR_SVID_ALERT# Pull high on HW side

Note:
VR_HOT# Pull high on HW side

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

Note:
PR1104=169K
=>Icc(max)=33A
fsw=700KHz

Note:
PR1112=124K
=>Slew rate=53mV/us
Vboot = 1.7V

Droop

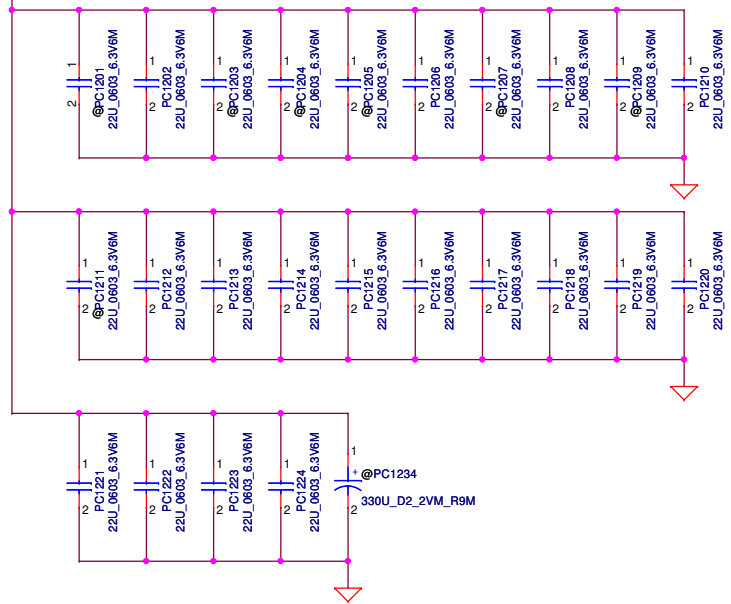
RC Match

OCF Setting

Local sense put on HW site

+CPU_CORE

24 X 22u/0603



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Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
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9					
10					
11					
12					
13					
14					
15					
16					
17					

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ZIWB2/ZIWB3/ZIWE1 HW PIR List



Item	Page	MODIFICATION LIST	PURPOSE	
1	P. 36	Modify DP_SEL schematic	Because the first design is wrong.	EVT TO DVT
2	P. 34	Delete D28	It already reserve in sub BD	
3	P. 36	Modify HPD schematic	Because the first design is wrong.	
4	P. 36	Modify DP AUX schematic	Cap already reserve in sub BD	
5	P. 20	Reserve +1.05VS to +0.95VGS	AMD' s suggestion	
6	P. 33	Add D26 for ESD		
7	P. 42	Add RV198, RV199	AMD' s suggestion	DVT TO PVT
1	P. 35	change U11.111 power rail to +3VLP	It only use +3VLP	
2	P. 33	un-pop R294, pop R295.	B series' s LED need to follow E series	
3	P. 10	Add R247, R248	For BIOS Stap Pin	
4	P. 37	Change DP Switch IC solution	For HDMI audio issue	
5	P. 35	Add C197 for ESD		
6	P. 33	Add C198 for ESD		
7	P. 30	Add C199 for ESD		
1	P. 33	Reserve R298, R299 for DC-in LED control	To avoid LED shimmer	PVT TO PRE-MP
2	P. 38	Change DL1 and DL2 footprint for ESD		

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