MX3(Maddog 2.5) VER : 3A

X'TAL 14.318MHz
CLOCK GENERATOR CY28547LFXCT P16

Merom 478 uFCPGA P2,P3

Thermal Sensor & Fan P37

BATT Charger MAX8724 P39

BATT Selector MAX8724 P40

VCORE MAX8770 P41

System 5V/3.3V ISL6236 P42

1.8V/1.05V MAX8717 P43

5/3.3/2.5/1.5 /1.25/0.9 V P44

AC/BATT Conn. P45

DDRII SO-DIMM 1 P15

Dual Channel DDR2 533/667 MHz

FSB 667/800 Mhz

DDRII SO-DIMM 2 P15

Dual Channel DDR2 533/667 MHz

NB Crestline 965GM 1299 uFCBGA P4,P5,P6,P7,P8,P9,P10

LVDS

E-switch PI2PCIE412-DZHE P18

LVDS

TFT LCD Panel P18

MXM III-NB8E (GT/SE/GLM) VRAM 256M VRAM 512M P17

LVDS

HDMI

HDMI P19

HDMI Port IO board

IO board (Audio-Left Side; HDMI-Right Side) P38

PCI-E 16X Lane

SPDIF_MXM

HDD (SATA) P28

SATA0

DMI 4X Lane

SB ICH8M-E 652 BGA P11,P12,P13,P14

PCI-E 6X Lane

PCIE-1

Express Card P26

USB 5

Module BAY

HDD / ODD (SATA) P28

SATA1

HDD / ODD (PATA) P28

PATA

USB 2.0 x 9

X'TAL 24.576MHz

PCIE-3

IEEE 1394B Controller FW643 P24

IEEE 1394B Port IO board

PCI Bus

Azalia

X'TAL 32.768KHz

LPC

PCIE-4

MINI Card 1 WLAN P25

USB 6

USB 0

USB 1

USB Port x 2 Left Side IO board

USB 2

USB Port x 1 Right Side P27 & IO board

PCIE-5

MINI Card 3 Robson P25

Mini PCI (for Debug) P46

7 in 1 Card Reader Controller R5C833 P29,P30

X'TAL 32.768KHz

EC WPC8769LDG P31

SPDIF_MXM

Azalia Audio Controller ALC885 P22,P23

USB 3

ELC P34,P35,P36

USB 4

Bluetooth P33

X'TAL 25MHz

PCIE-6

10M/100M/1G LAN BCM5787M P20,P21

Transformer HPL-5001-3 IO board

RJ45 IO board

7 in 1 Card Reader connector P30

SPI ROM P31

Touch Pad P32

KB Conn. P32

CIR P33

USB 7

CCD P18

USB 8

MINI Card 2 Wireless-USB P25

Audio Amplifier MAX9789A P22

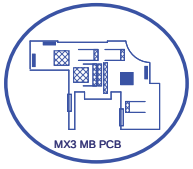
Phone Jack 1 HP/MIC/Line Out/SPDIF IO board

Phone Jack 2 HP/MIC /Line Out IO board

DMIC P18

Speaker P22

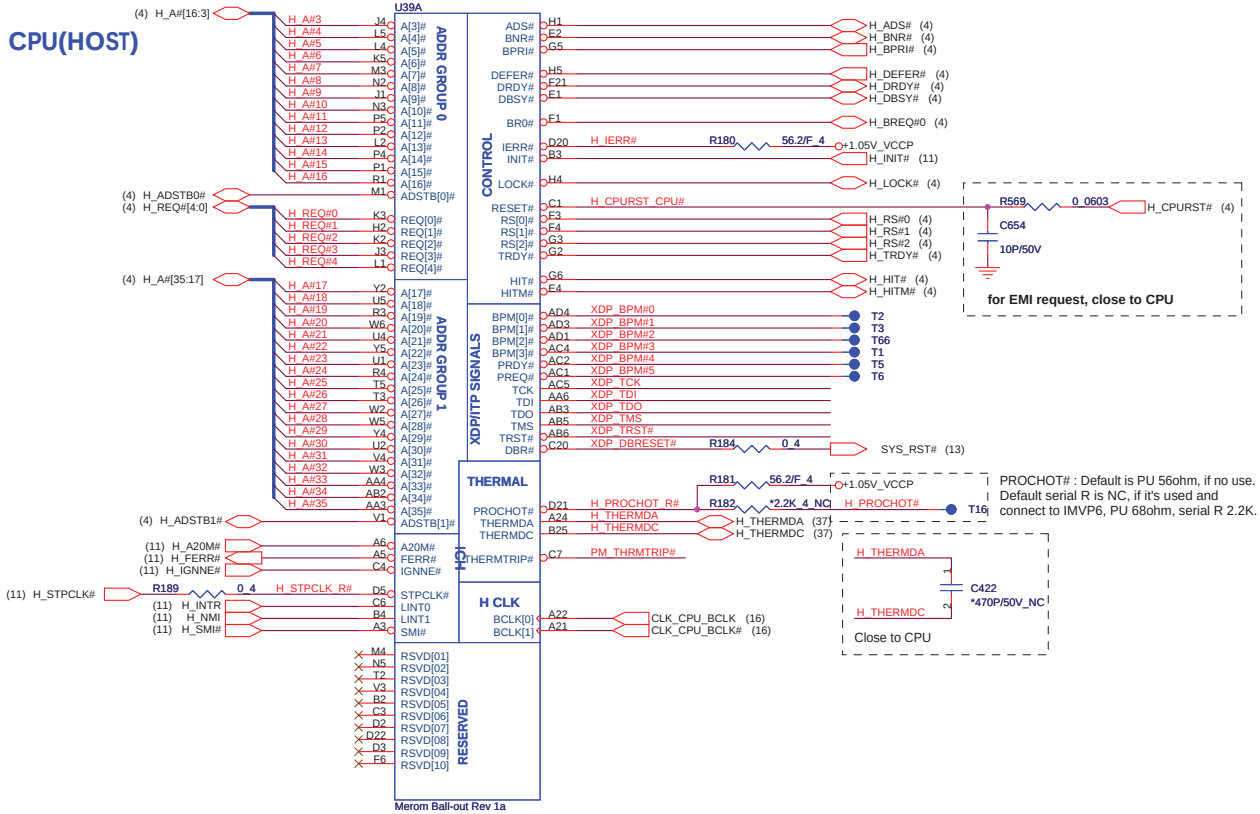
D_1011: change PCB version from D to E

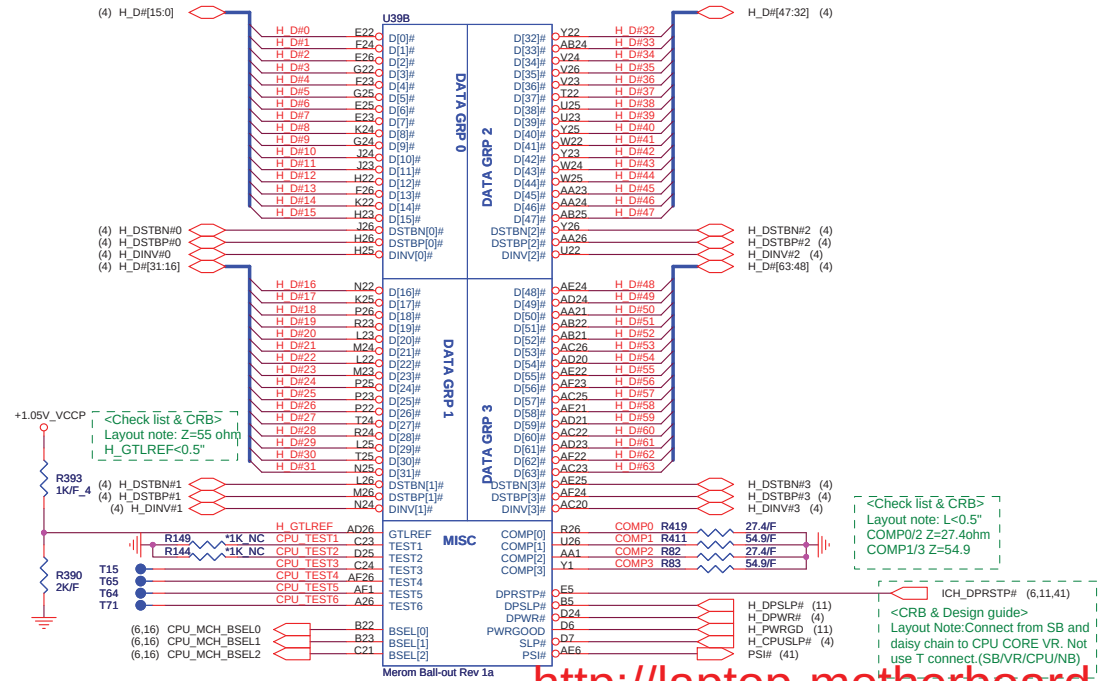


QUANTA COMPUTER

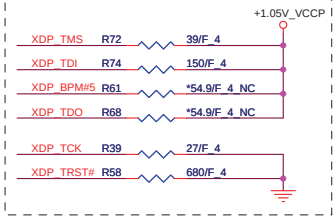
Title	Block Diagram	
Size	Document Number MX3	Rev 3A
Date	Friday, October 12, 2007	Sheet 1 of 53

CPU(HOST)





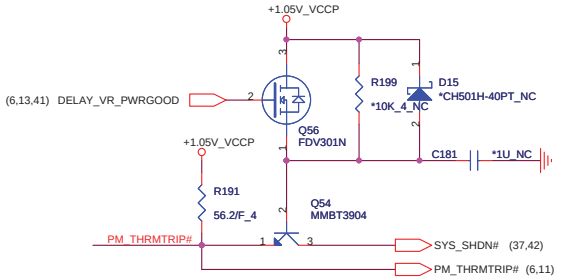
PU/PD (ITP700)



ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	PU Depop	+3.3V_RUN	Close to CK505 Pin37

Thermal Trip



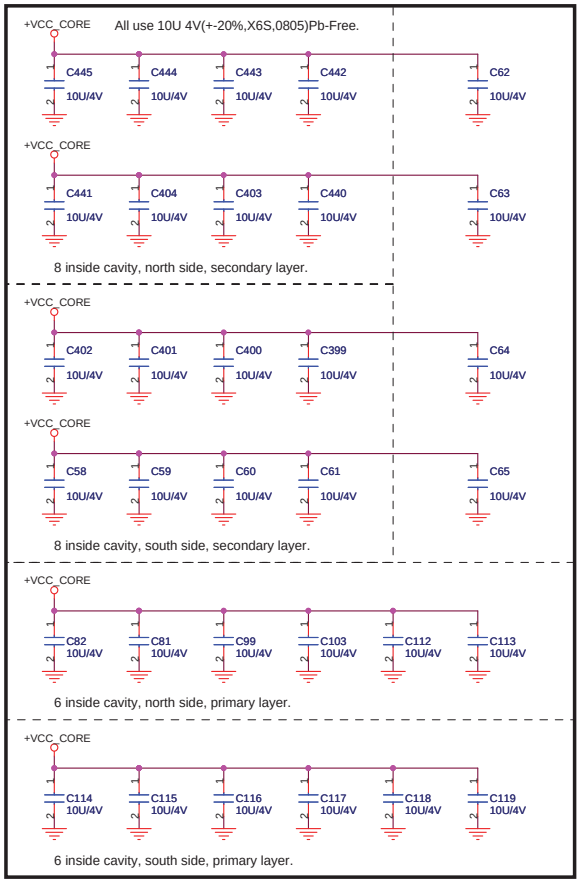
<CRB & Design guide>
Layout Note: Thermal trip should connect to ICH8 & GMCH without T-ing (ZS1 default NC)

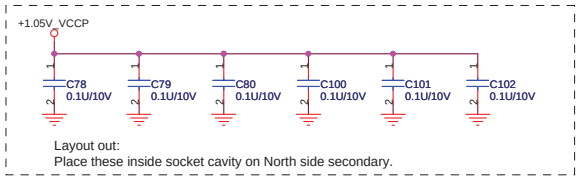
FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

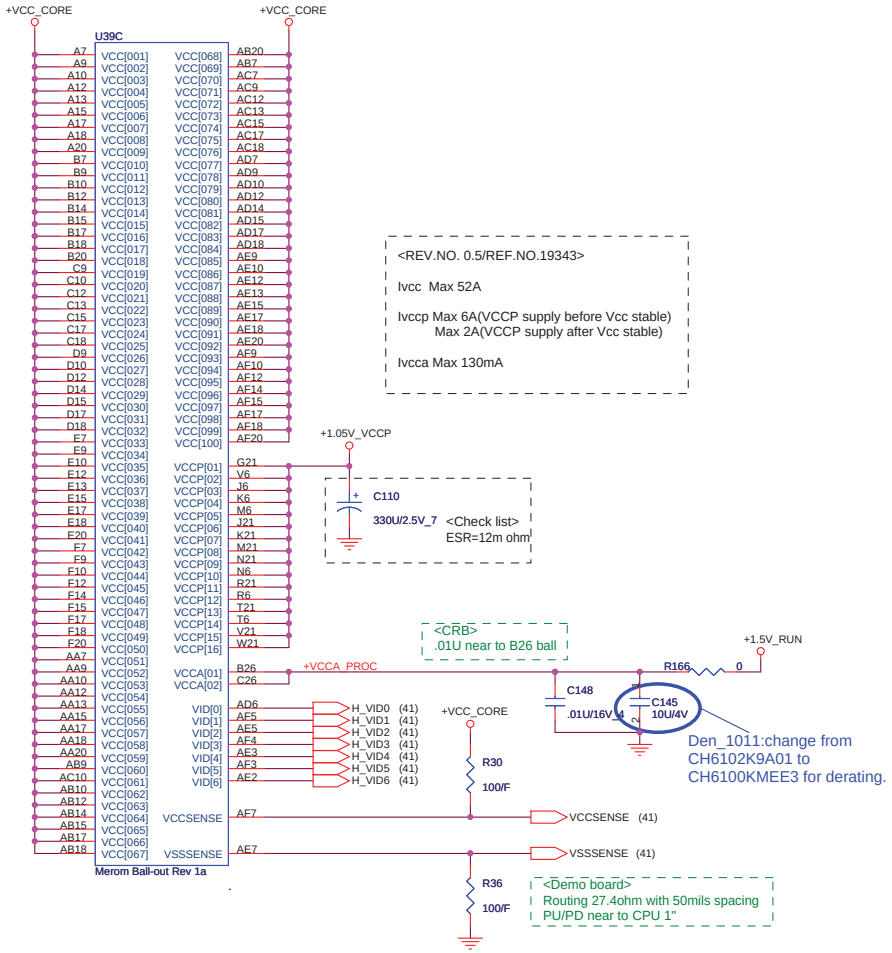
QUANTA COMPUTER

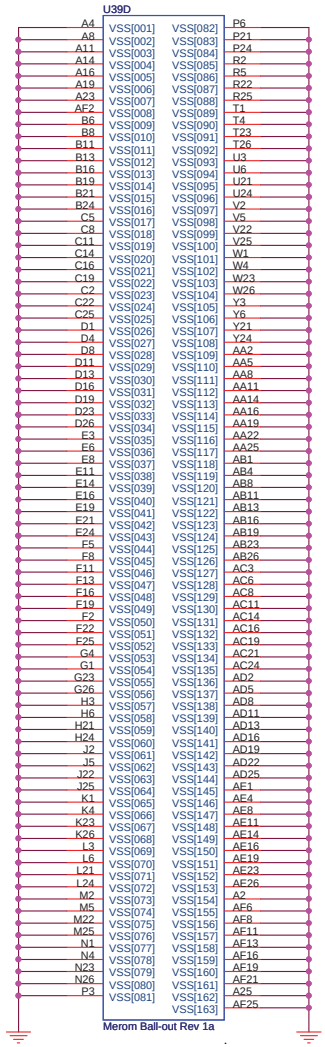
Title	CPU Host(1/2)	
Size	Document Number MX3	Rev 2A
Date: Friday, October 12, 2007	Sheet 2 of 53	

CPU(Power)









QUANTA COMPUTER

Title	CPU Power(2/2)	
Size	Document Number MX3	Rev 3A
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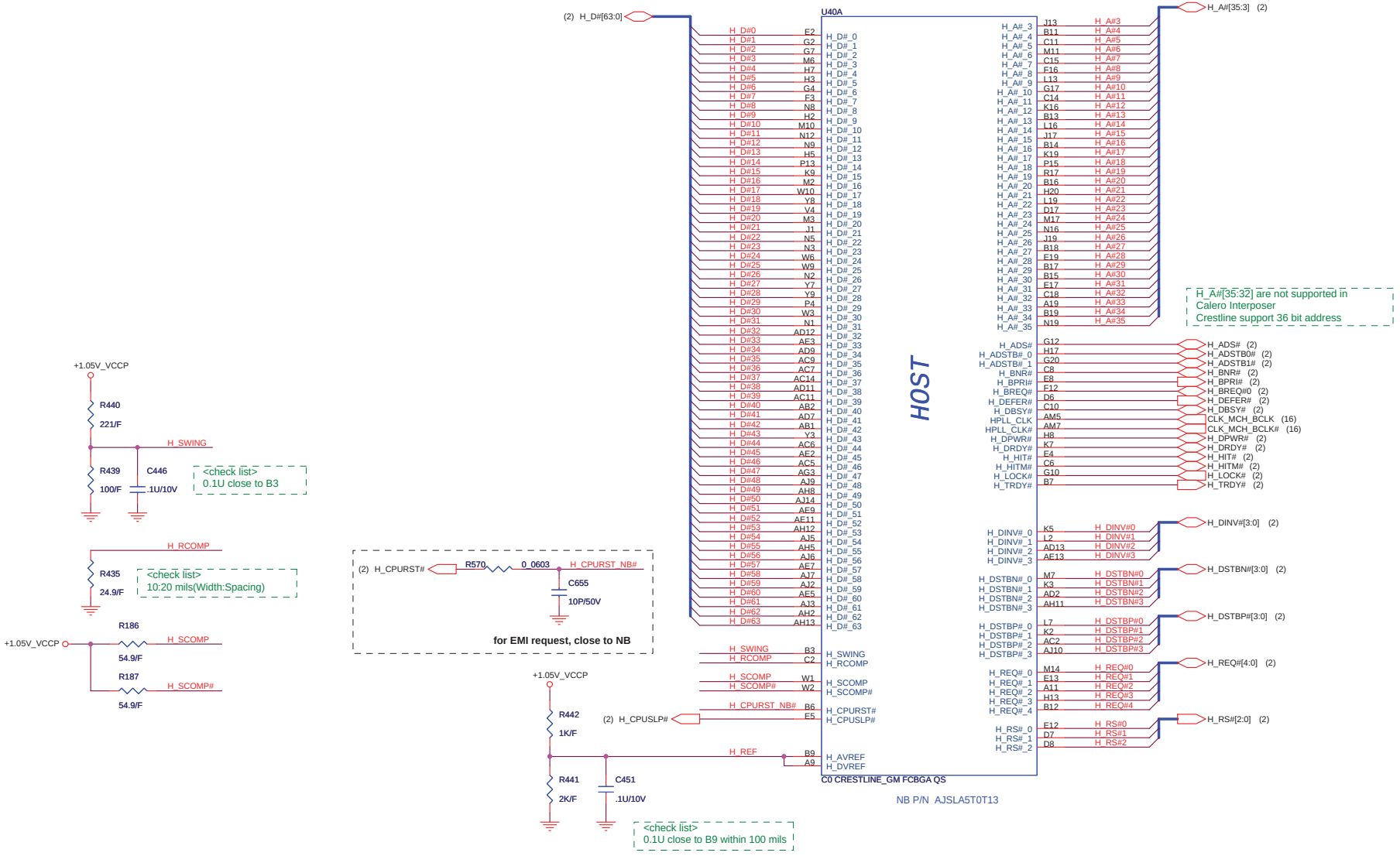
NB(HOST)



Title	GMCH Host(1/7)
Size	Document Number MX3
Rev	2B
Date	Friday, October 12, 2007
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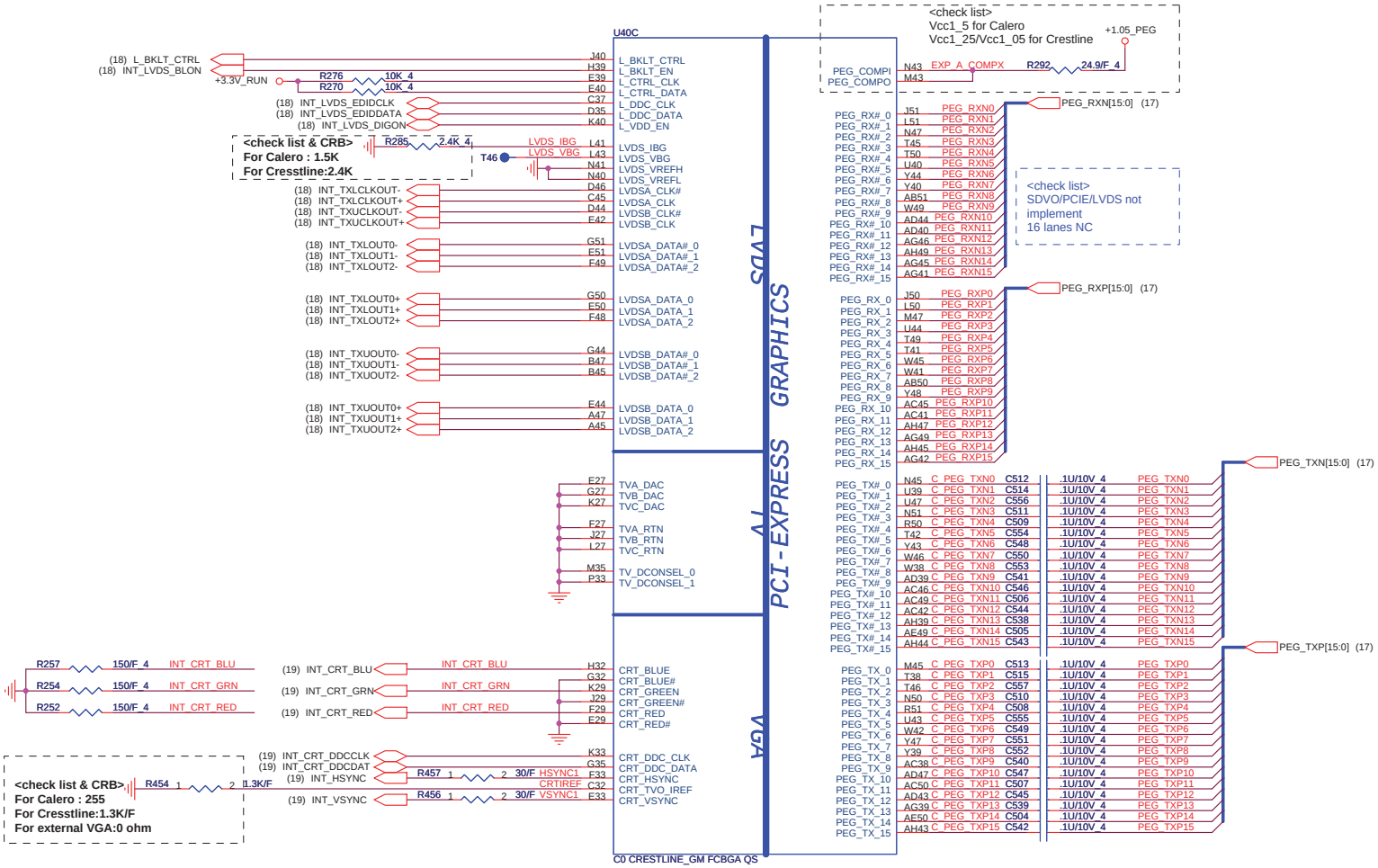

QUANTA COMPUTER		
Title	GMCH Graphics(2/7)	
Size	Document Number MX3	Rev 2B
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Strapping table

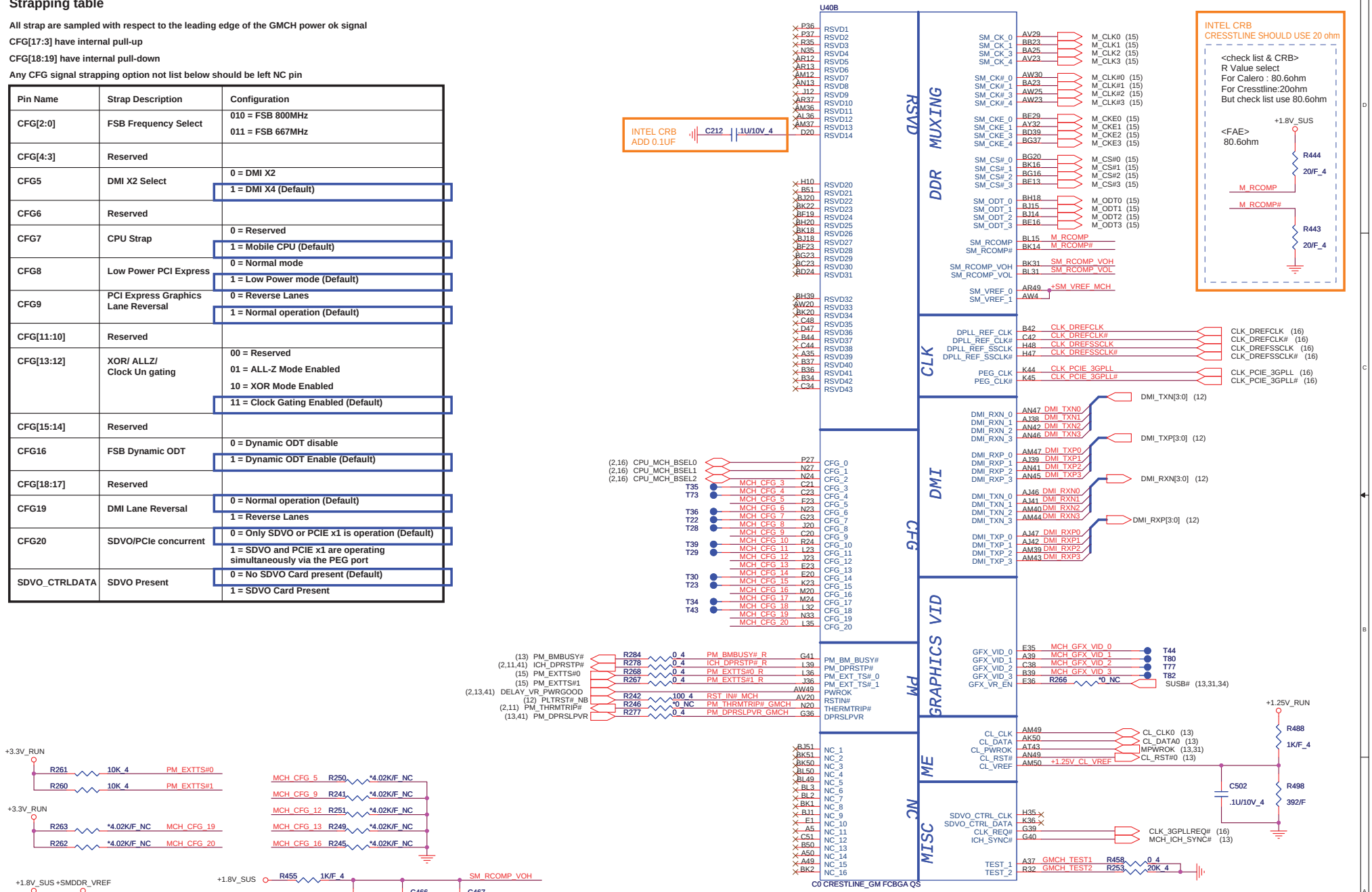
All strap are sampled with respect to the leading edge of the GMCH power ok signal

CFG[17:3] have internal pull-up

CFG[18:19] have internal pull-down

Any CFG signal strapping option not list below should be left NC pin

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4 (Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU (Default)
CFG8	Low Power PCI Express	0 = Normal mode 1 = Low Power mode (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation (Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ ALLZ/ Clock Un gating	00 = Reserved 01 = ALL-Z Mode Enabled 10 = XOR Mode Enabled 11 = Clock Gating Enabled (Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable (Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal operation (Default) 1 = Reverse Lanes
CFG20	SDVO/PCIe concurrent	0 = Only SDVO or PCIE x1 is operation (Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present (Default) 1 = SDVO Card Present



QUANTA COMPUTER

Title	GMCH Strapping(3/7)	
Size	Document Number MX3	Rev 2B
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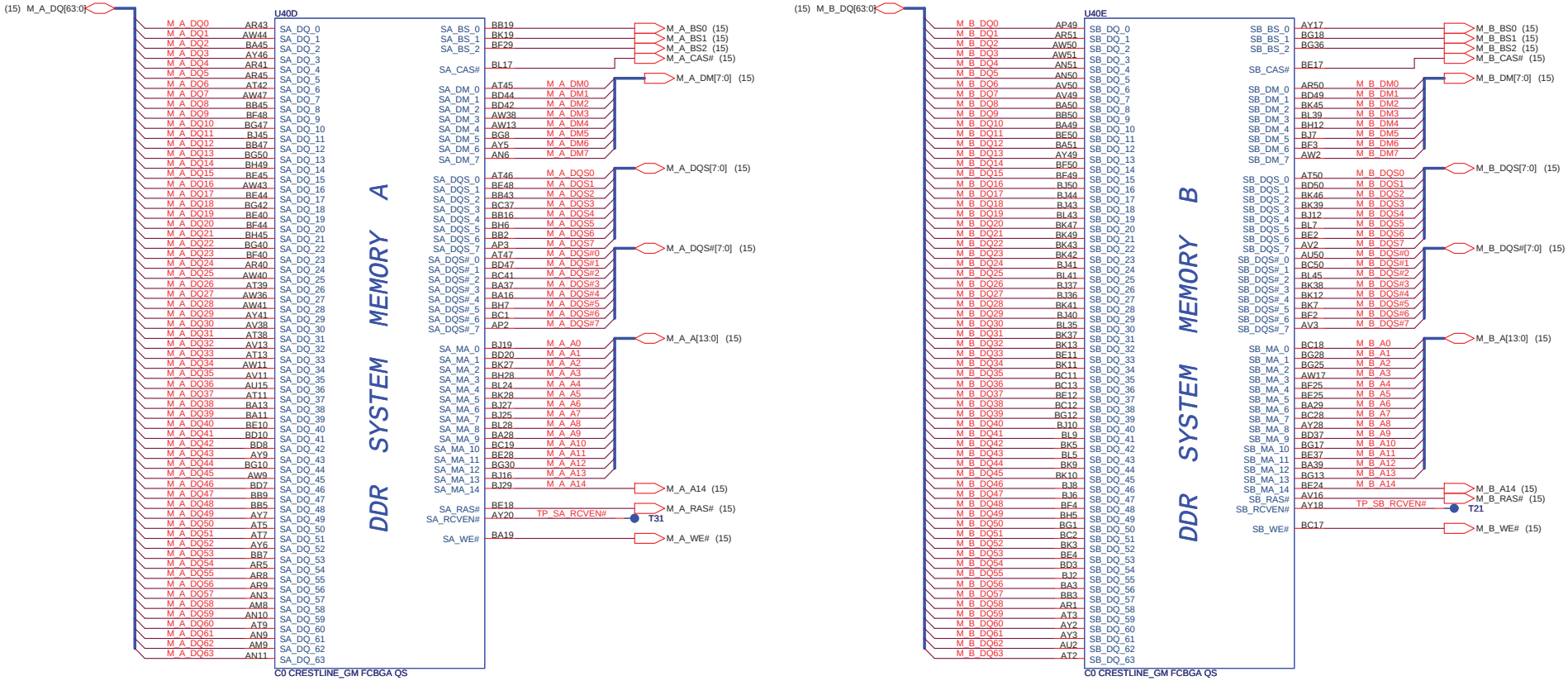
NB(Memory controller)



QUANTA COMPUTER

Title	GMCH DDRII(4/7)	
Size	Document Number MX3	Rev 2B
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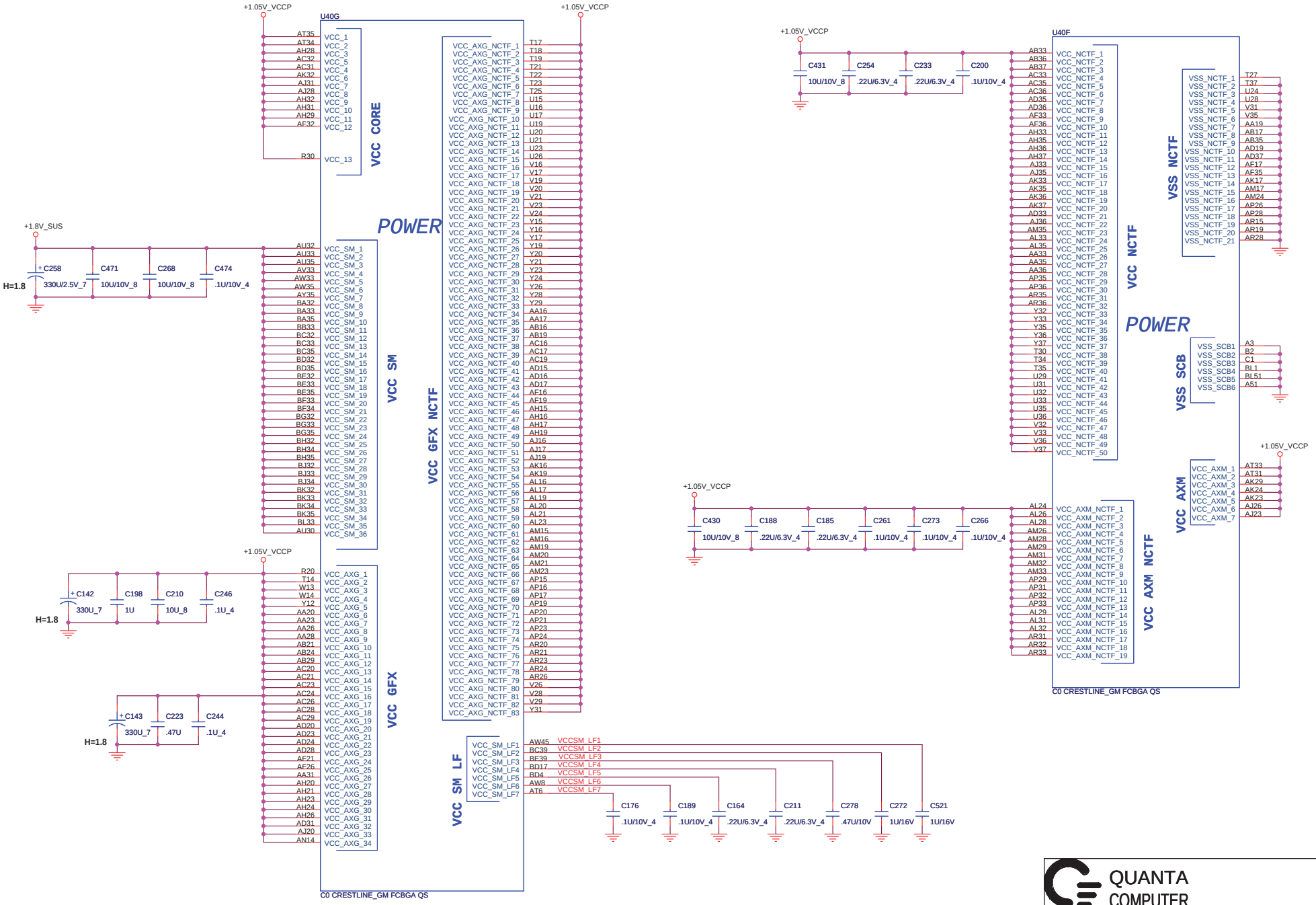
NB(Power-1)



Title	GMCH Power-1(5/7)
Size	Document Number MX3
Rev	2B
Date	Friday, October 12, 2007
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NB(Power-2)

CRT/TV Disable/Enable guideline

Ball	Enable	Disable	Ball	Enable	Disable
VCCA_CRT	3.3V	GND	VCCA_C_TVO	3.3V	GND
VCCD_CRT	1.5V	GND	VCCD_TVO	1.5V	1.5V
VCCDQ_CRT	1.5V	GND	VCCABG_DAC	3.3V	GND
VCCA_A_TVO	3.3V	GND	VSSABG_DAC	GND	GND
VCCA_B_TVO	3.3V	GND	VCC_SYNC	3.3V	GND

LVDS Disable/Enable guideline

Signal	If SDVO Disable LVDS Disable	If SDVO enable LVDS Disable	If SDVO enable LVDS enable
VCCD_LVDS	GND	1.8V	1.8V
VCCA_LVDS	GND	GND	1.8V
VCCTX_LVDS	GND	GND	1.8V
	EXTERNAL		INTERNAL

<FAE>
INT VGA disable
VCCSYNC connect to GND

<FAE>
INT VGA disable
VCCD_TVDAC still +1.5V

CRB RECOMMEND
180OHM@100MHz
Rdc= 0.09OHM (max)

<CRB>
+1.25V AND +1.25M shall be
+1.5V for Calero Interposer

<FAE>
VCC_RXR_DMI and VCC_PEG
connect to+1.05V

U40H
C0 CRESTLINE_GM FCBGA QS

Title	GMCH Power-2(6/7)
Size	Document Number MX3
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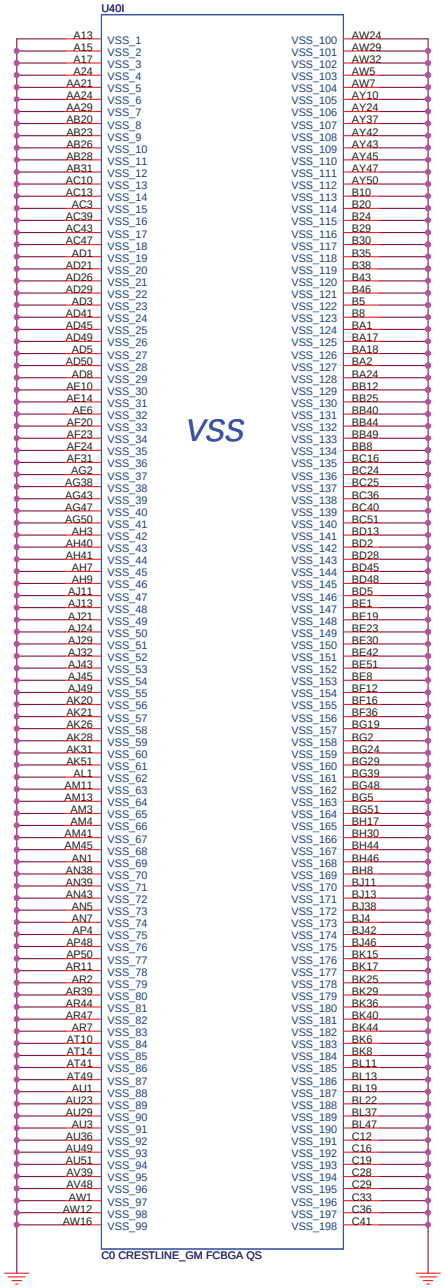
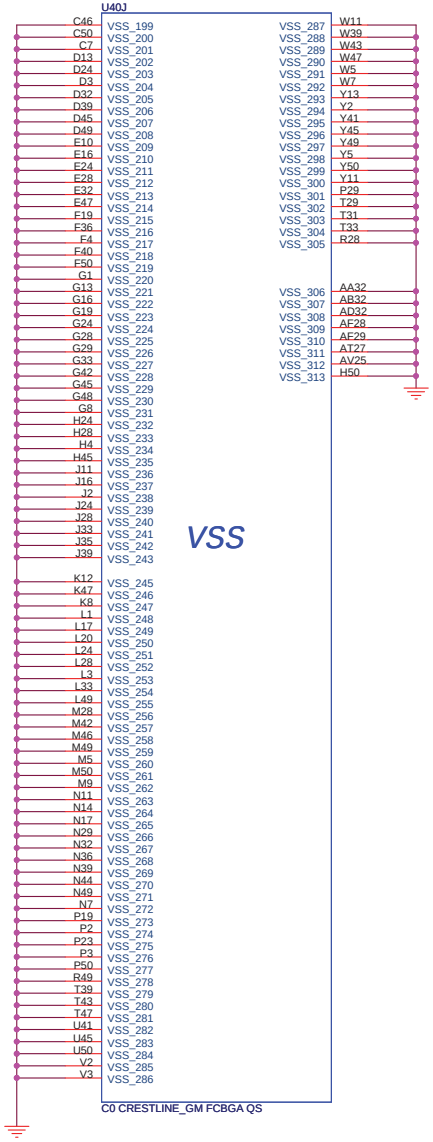
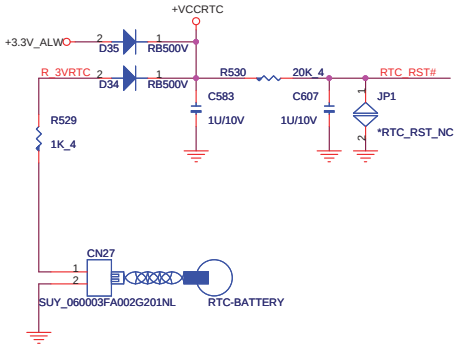




QUANTA COMPUTER

Title	GMCH Power-3(7/7)	
Size	Document Number MX3	Rev 2B
Date: Friday, October 12, 2007	Sheet 10 of 53	

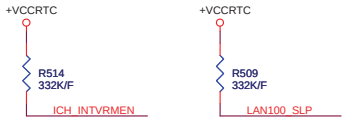
RTC



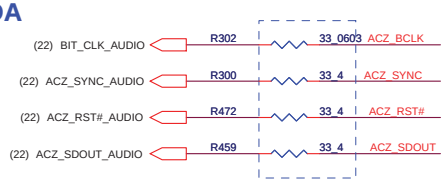
SB Strap

As Intel's review(Apr.,17,2007), internal VR must be enabled.

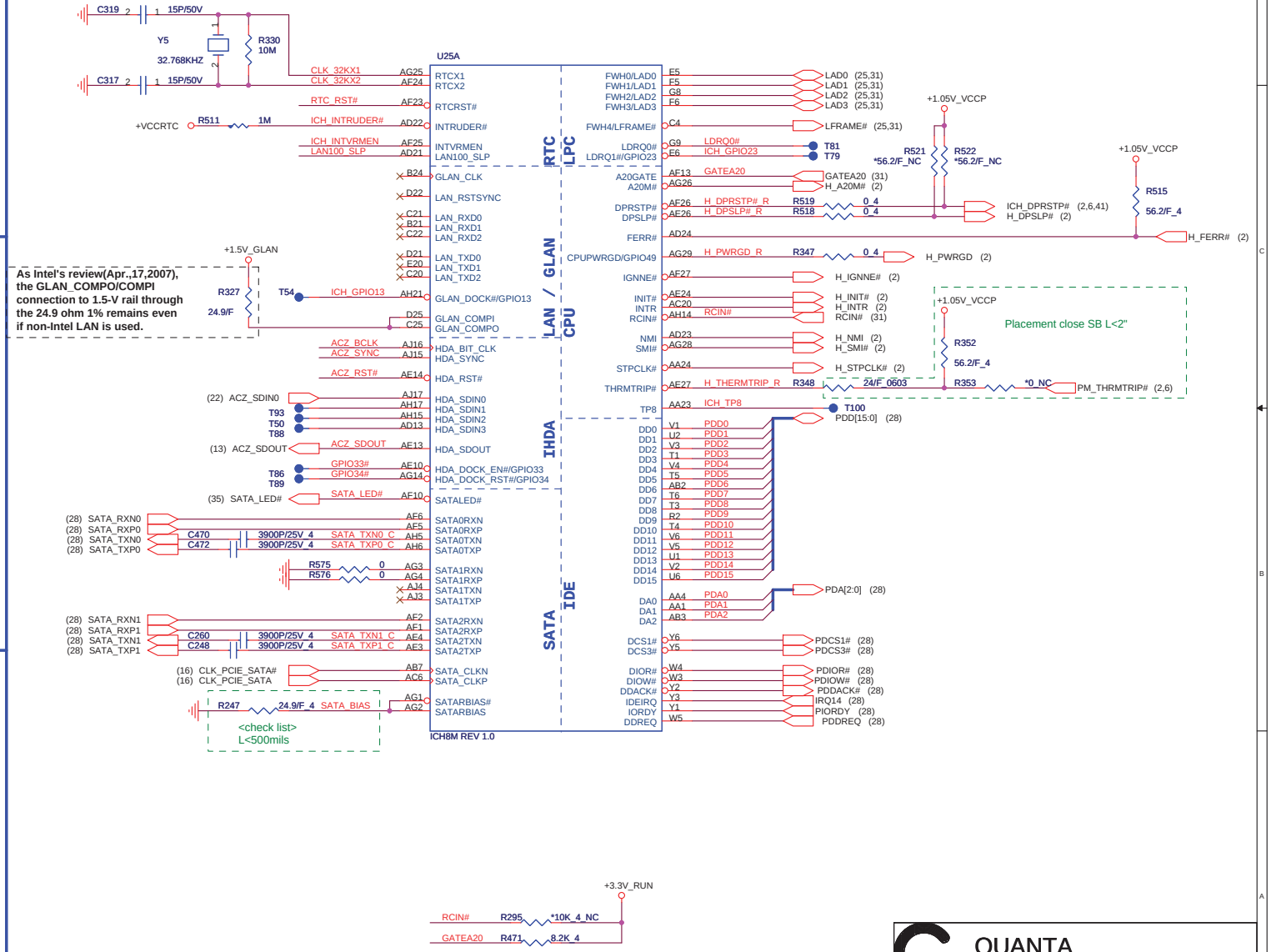
INTVRMEN	Low = Internal VR disable
	High = Internal VR enable(Default)
LAN100_SLP	Low = Internal VR disable
	High = Internal VR enable(Default)



HDA



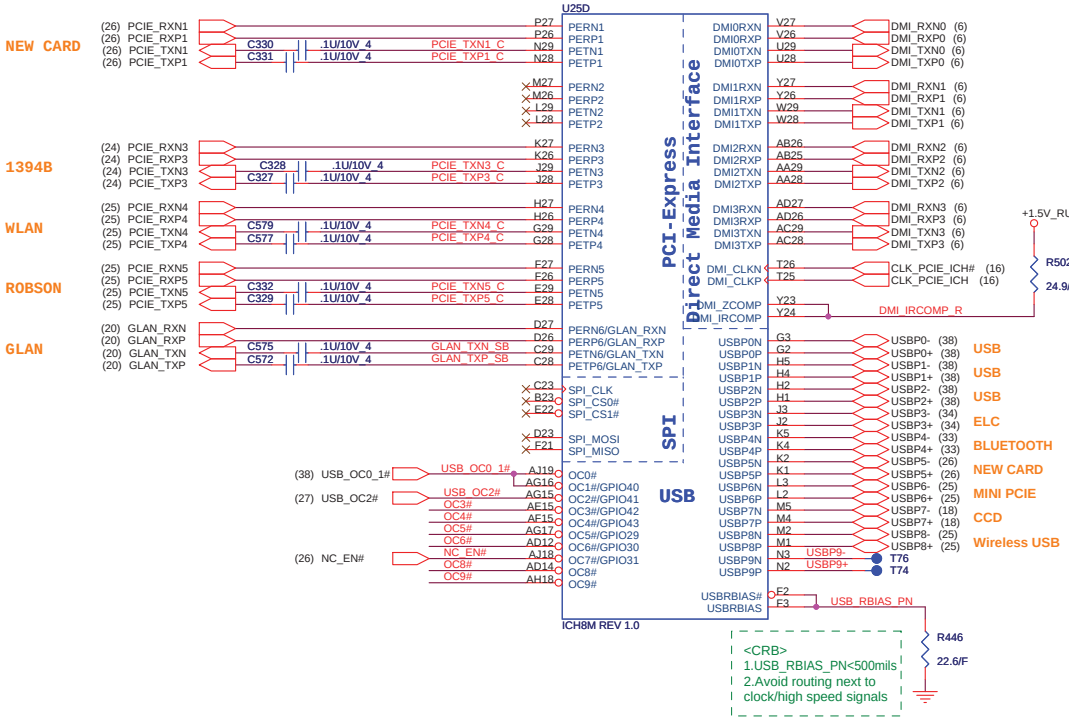
Close to SB,Length <2.5"



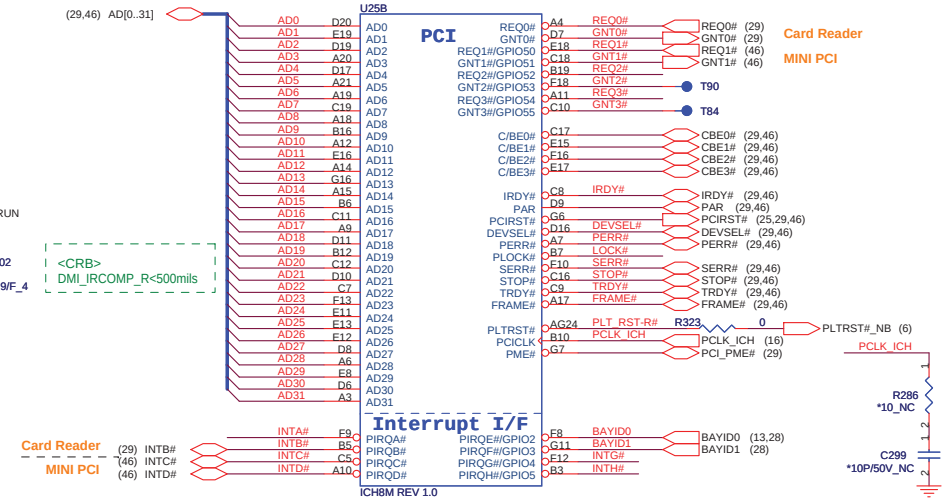
QUANTA COMPUTER

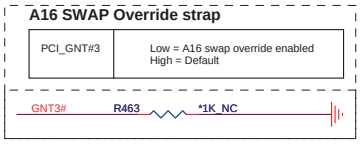
Title	ICH8M Host(1/4)	
Size	Document Number MX3	Rev 2B
Date	Friday, October 12, 2007	Sheet 11 of 53

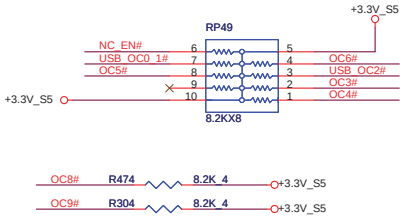
SB-PCIE/USB/DMI

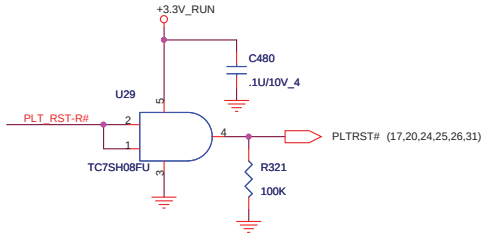


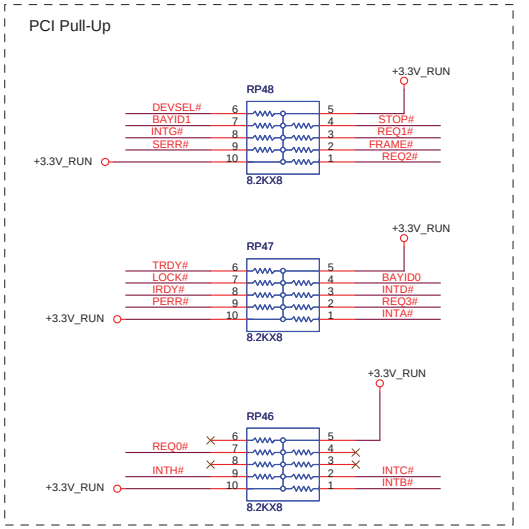
SB-PCI











QUANTA COMPUTER			
Title	ICH8M PCIE/PCI/USB(2/4)		
Size	Document Number MX3		Rev 2B
Date: Friday, October 12, 2007		Sheet 12 of 53	

SB-GPIO

As Intel's review(Apr.,17,2007), add 0 ohm between SMBus & SMLINK to let SMBus of ICH8M work in slave mode.

SMB_CLK_ME R477 0 PCLK_SMB
SMB_DATA_ME R482 0 PDAT_SMB

<FAE>
CRB STP_PCI# PU is no stuff. CRB STP_CPU# always keeps high to ensure ME alive in M1 state. (CLK_MCH_BCLK/# must keep alive to make ME work) I think there will be update for this design, I suggest you to keep PU and 0Ω isolation resistors for this signal.

+3.3V_RUN
R484 *10K_NC
R491 *10K_NC
(16) PM_STPPCI#
(16) PM_STPCPU#
R490 0
R483 0
PM_STPPCI_ICH#
PM_STPCPU_ICH#

C333 .1U/10V_4
U31 NC7SZ04
(41) VR_PWRGD_CK410#

(16,25,26) PCLK_SMB
(16,25,26) PDAT_SMB
T97
PCLK_SMB
PDAT_SMB
CL_RST#1
SMB_CLK_ME
SMB_DATA_ME
RI#
T75
LPC_PD#
(2) SYS_RST#
SYS_RST#
(6) PM_BMBUSY#
SMB_ALERT#
(29,31,46) CLKRUN#
CLKRUN#
(20,24,25,26,31) PCIE_WAKE#
(29,31,46) SERIRQ
(31) THERM_ALERT_SB#
PCIE_WAKE#
SERIRQ
VR_PWRGD_CLKEN
T55
TP7
(31) KBSMI#
(31,32) LID_HALL_EN#
D19 CH501H-40PT
D18 CH501H-40PT
D23 CH501H-40PT
(31) SCI#
(28,31) BAYINS#
KBSMI# ICH
LID591# ICH
ICH_GPIO7
SCI#
BAYINS# R
BOARD_ID0
BOARD_ID1
BOARD_ID2
BOARD_ID3
ICH_GPIO27
T59
RST_BAY# R
(16) SATACLKREQ#
T78
T85
SATACLKREQ#
ICH_GPIO38
ICH_GPIO39
ICH_GPIO48
(22) PCSPK
PCSPK
MCH_ICH_SYNC# R
ICH_TP3

<check list>
internal PD

+3.3V_RUN R294 *10K_4_NC
(6) MCH_ICH_SYNC# R296 0_4

add for RST_BAY#
+3.3V_RUN
C310 .1U/16V
U26 TC7SH08FU
(28) RST_BAY#
RST_BAY# R
R310 100K
R313 *0_NC

U25C ICH8M REV 1.0

SMB:
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1

SATA GPIO:
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
AJ12 AJ10 AE11 AG11
R293 8.2K_4
R281 8.2K_4
R468 8.2K_4
R467 8.2K_4
+3.3V_RUN

Clocks:
CLK14 AG9
CLK48 G5
14M_ICH
CLKUSB_48
14M_ICH (16)
CLKUSB_48 (16)
SUSCLK D3

SYS GPIO:
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#

Power MGT:
SLP_S3# AG23
SLP_S4# AF21
SLP_S5# AD18
SLP_S3#
SLP_S4#
SLP_S5#
R315 100/F_4
R309 100/F_4
SUSB# (6,31,34)
SUSC# (31)
T94
S4_STATE#/GPIO26 AH27
ICH_GPIO26
T60
PWROK AE23
ICH_PWROK
DPRSLPVR/GPIO16 AJ14
PM_DPRSLPVR_R
R301 100/F_4
PM_DPRSLPVR (6,41)
BATLOW# AE21
PM_BATLOW# R
PWRBTN# C2
DNBSWON# (31)
LAN_RST# AH20
PM_LAN_ENABLE_R
R306 10K_4
RSMRST# AG27
PM_RSMRST# R
CK_PWRGD E1
CK_PWRGD (16)
CLPWROK E3
MPWROK (6,31)
SLP_M# AJ25
T58

GPIO Controller Link:
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
CL_CLK0 F23
CL_CLK1 AE18
T92
CL_CLK0 (6)
CL_DATA0 F22
CL_DATA1 AE19
T95
CL_DATA0 (6)
CL_VREF0 D24
CL_VREF1 AH23
CL_VREF0_SB
CL_VREF1_SB
CL_RST# AJ23
CL_RST#0 (6)

MISC:
MEM_LED/GPIO24 AJ27
ME_EC_ALERT/GPIO10 AJ24
EC_ME_ALERT/GPIO14 AE22
WOL_EN/GPIO9 AG19
ICH_GPIO10
ICH_GPIO14
ICH_GPIO9
T56
T99
BAYON# (28)
R334 10K_4
+3.3V_S5

R273 0_4 BAYID0 (12,28)

Close to SB
14M_ICH
CLKUSB_48
R461 *33_4_NC
R451 *10_4_NC
C473 *10P_4_NC
C457 *10P_4_NC

<FAE>
Since your CPU VRM has no DPRSTP# pin, connect PM_DPRSLPVR to IMVP6 is correct

If no use internal LAN MAC connect LAN_RST# to PLTRST#
Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.

+3.3V_S5
R505 *3.24K/F_NC
R503 *453/F_4_NC
C534 *.1U/10V_4_NC
+3.3V_RUN
R506 3.24K/F
R501 453/F_4
C532 .1U/10V_4

Controller Link 1 VREF for IAMT support only

+3.3V_S5
PCLK_SMB R333 2.2K_4
PDAT_SMB R500 2.2K_4
SMB_CLK_ME R481 10K_4
SMB_DATA_ME R489 10K_4
RI# R480 10K_4
PCIE_WAKE# R479 1K_4
PM_BATLOW# R R492 8.2K_4
BAYINS# R R496 10K
SCI# R473 10K_4
CL_RST#1 R577 *10K_NC

+3.3V_S5
SMB_ALERT# R493 10K_4
SYS_RST# R470 10K_4
ICH_GPIO10 R318 10K_4
RST_BAY# R R312 10K_4

ICH_GPIO14 R504 10K_4
ICH_GPIO9 R307 100K_4
VR_PWRGD_CLKEN R494 100K_4
ICH_PWROK R317 10K_4

No Reboot strap

HDA_SPKR	Low = Default
	High = No Reboot

+3.3V_RUN
PCSPK R464 *10K_4_NC
KBSMI# ICH R256 10K_4
LID591# ICH R259 10K_4
ICH_GPIO39 R288 10K_4
INTEL CRB SHOW IT

+3.3V_RUN
SERIRQ R469 10K_4
CLKRUN# R283 8.2K_4

INTEL FAE (08/17)
"Add RSMRST# isolation (important!!! See ww22 Santa Rosa MoW)"
+3.3V_S5
R351 *0_4_NC
R345 4.7K_4
PM_RSMRST# R
Q71 MMBT3906
RSMRST# (31)
TO ICH8
FROM uR(EC)
R344 10K_4
D25 BAV99
D24 BAV99
R339 2.2K_4

+3.3V_RUN
R465 *1K_NC
ACZ_SDOUT (11)
ICH_TP3
R311 *1K_NC

XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

+3.3V_RUN
C476 .1U/16V_4
U28 TC7SH08FU
(2,6,41) DELAY_VR_PWRGOOD
(31) PWROK_EC
DELAY_VR_PWRGOOD
PWROK_EC
ICH_PWROK
R322 100K_4

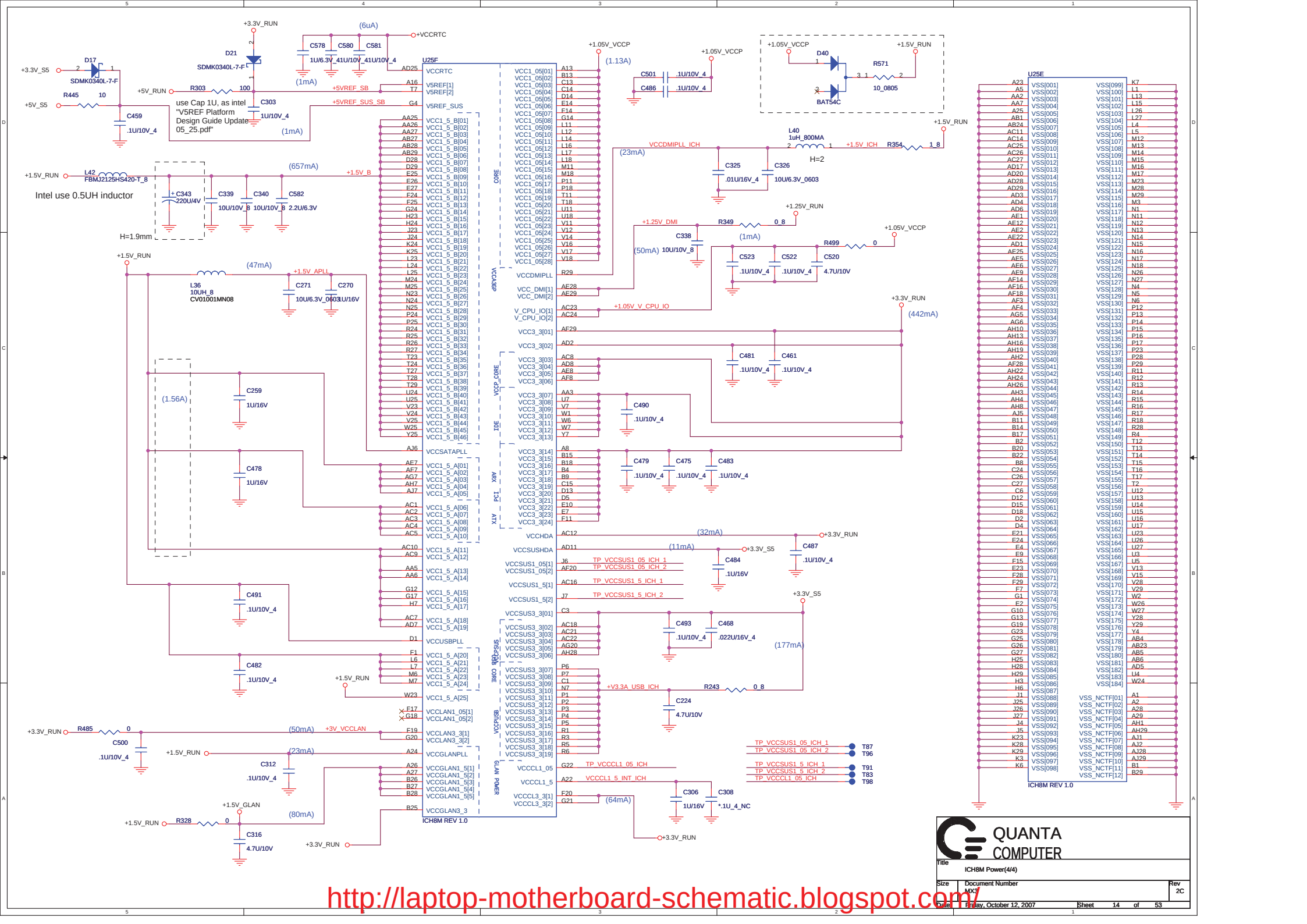
Board ID	ID3	ID2	ID1	ID0
EVT	0	0	0	0
DVT-1	0	0	0	1
DVT-2	0	0	1	0
PVT	0	0	1	1
Ramp1	0	1	0	0

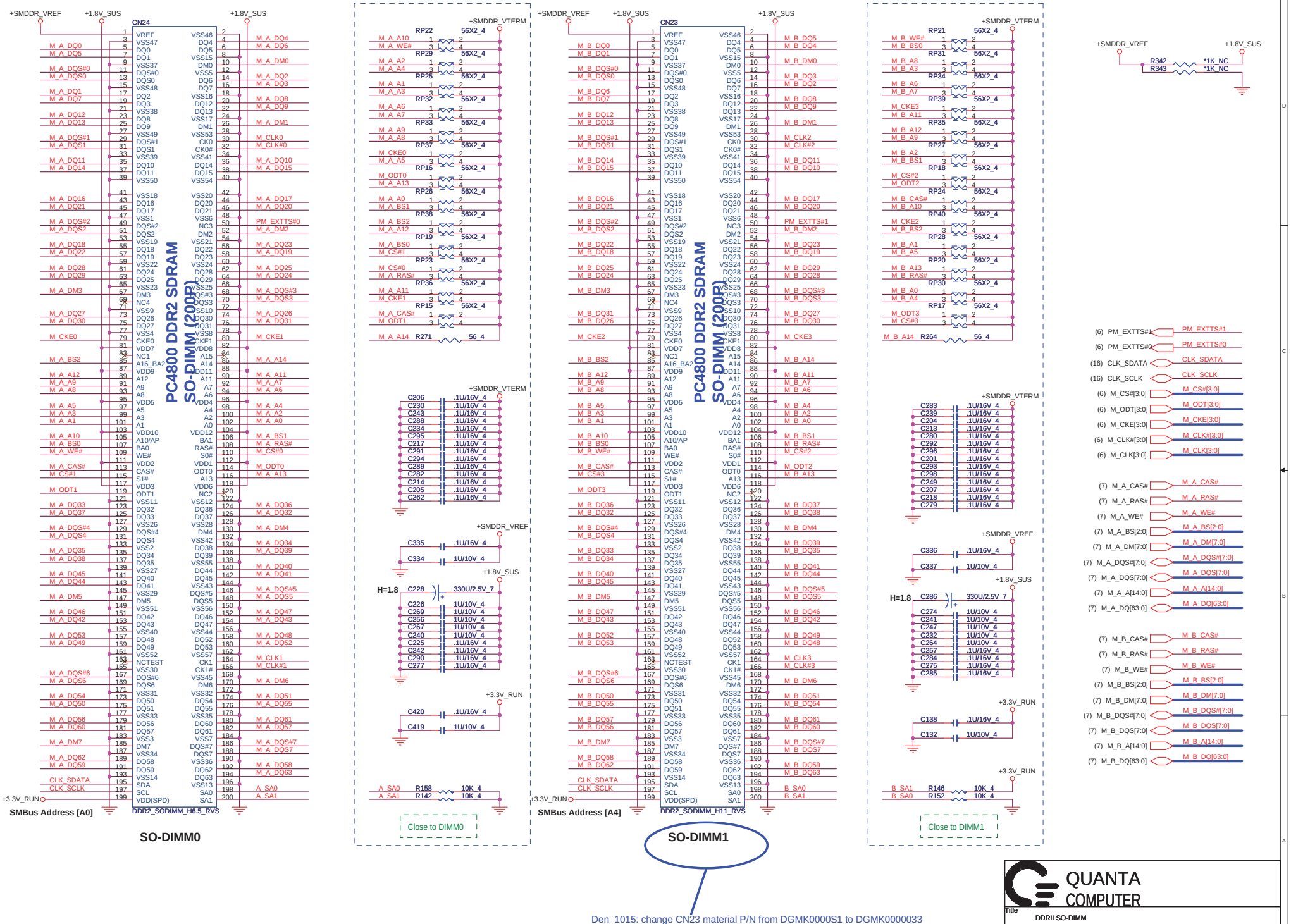
Den_1011: change BID from 0011 to 0100 for Ramp1

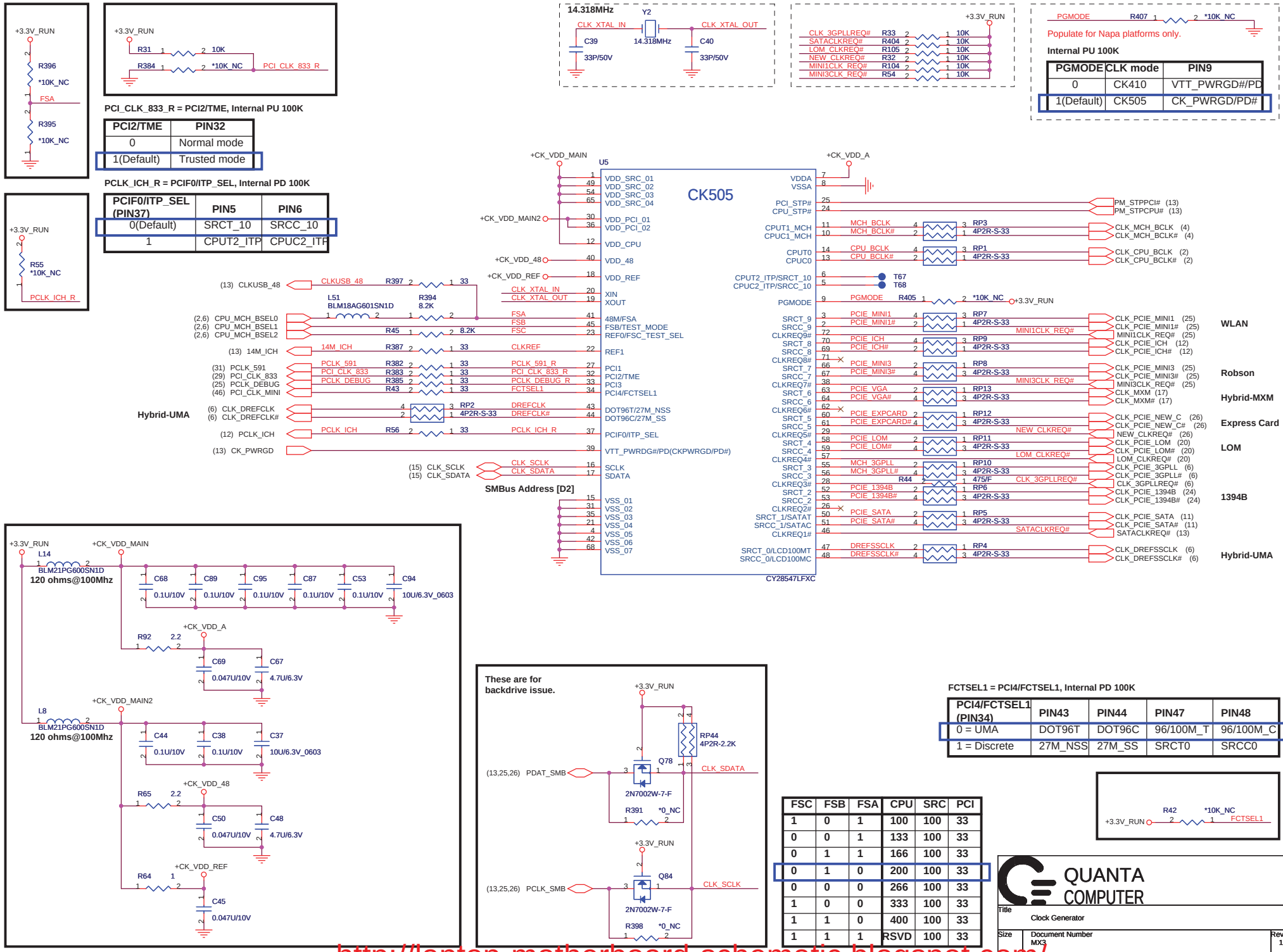
+3.3V_RUN
R282 *10K_4_NC
BOARD_ID3
R287 10K_4
+3.3V_RUN
R462 10K_4
BOARD_ID2
R466 *10K_4_NC
+3.3V_RUN
R290 *10K_4_NC
BOARD_ID1
R291 10K_4
+3.3V_RUN
R275 *10K_4_NC
BOARD_ID0
R280 10K_4

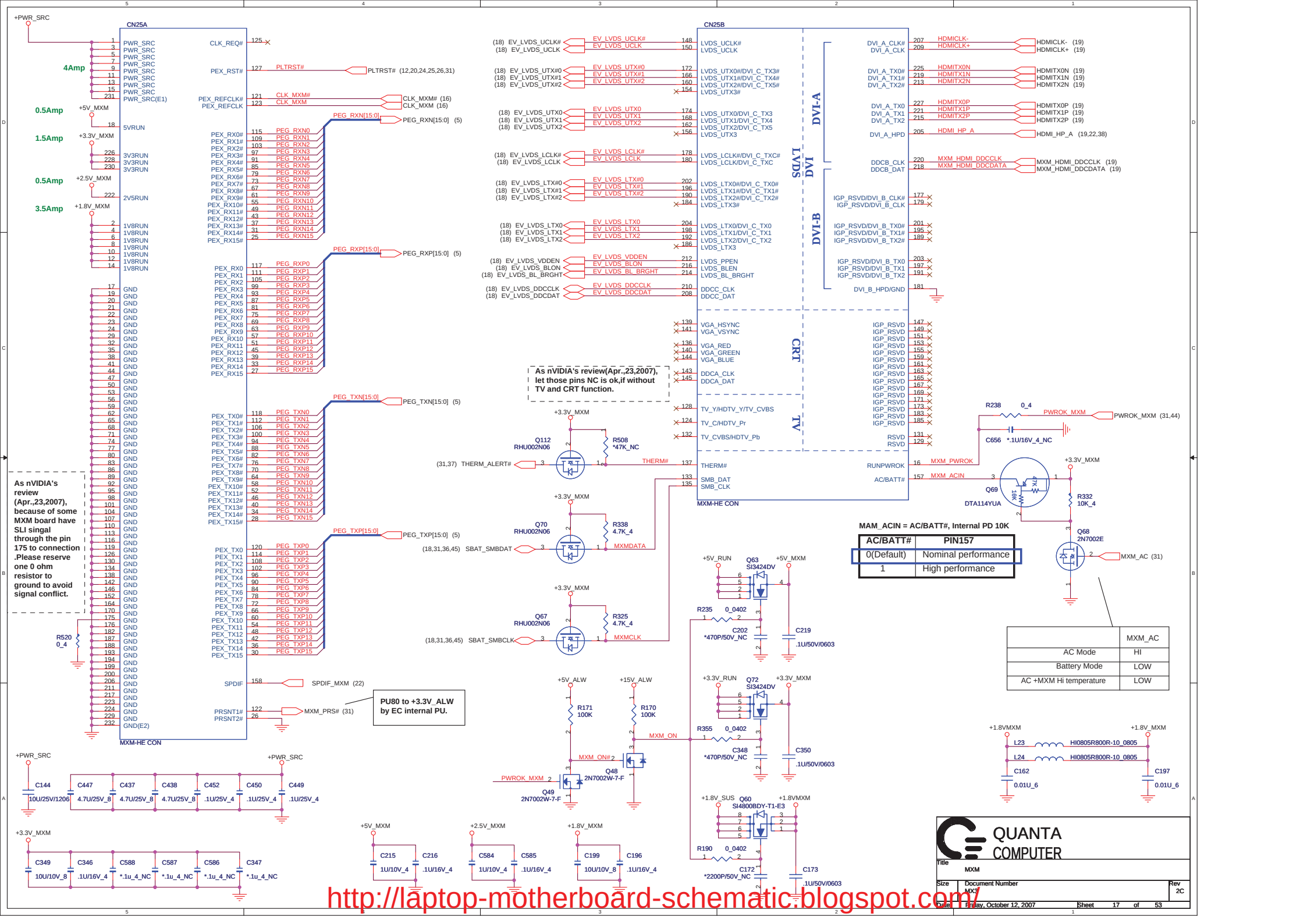
QUANTA COMPUTER

Title	ICH8M GPIO(3/4)	
Size	Document Number MX3	Rev 3A
Date	Monday, October 15, 2007	Sheet 13 of 53

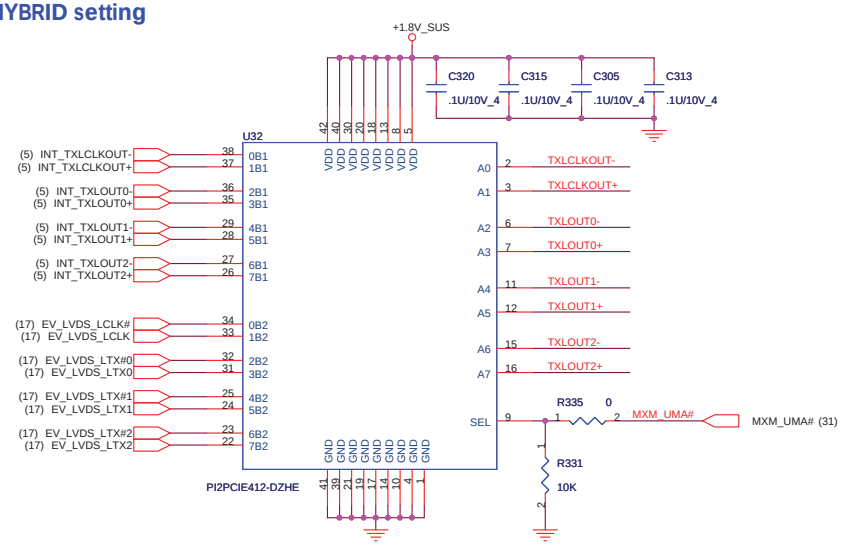


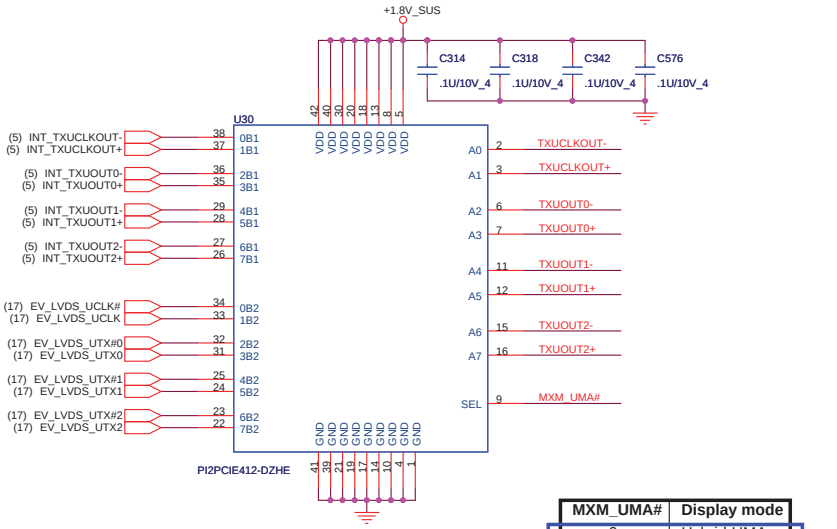




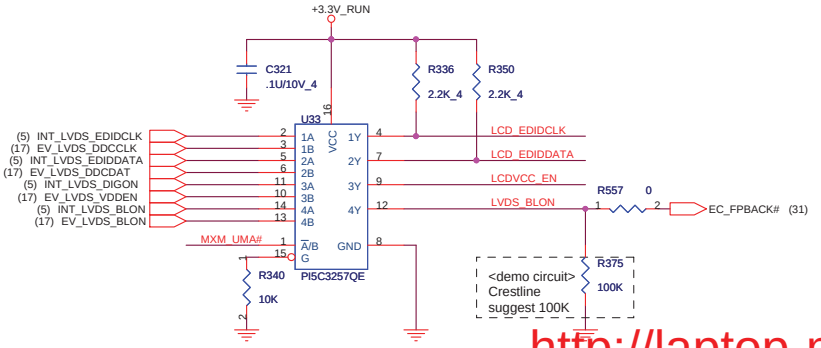

CN25A
MXM-HE CON
CN25B
MXM-HE CON
DVI-A
DVI-B
LVDS
DVI
CRT
TV
4Amp
0.5Amp
1.5Amp
0.5Amp
3.5Amp
+PWR_SRC
+5V_MXM
+3.3V_MXM
+2.5V_MXM
+1.8V_MXM
5VRUN
3V3RUN
2V5RUN
1V8RUN
GND
CLK_REQ#
PEX_RST#
PEX_REFCLK#
PEX_REFCLK
PLTRST# (12,20,24,25,26,31)
CLK_MXM# (16)
CLK_MXM (16)
PEG_RXN[15:0]
PEG_RXP[15:0]
PEG_TXN[15:0]
PEG_TXP[15:0]
SPDIF
SPDIF_MXM (22)
PRSNT1#
PRSNT2#
MXM_PRS# (31)
As nVIDIA's review (Apr.,23,2007), because of some MXM board have SLI singal through the pin 175 to connection .Please reserve one 0 ohm resistor to ground to avoid signal conflict.
R520 0_4
As nVIDIA's review(Apr.,23,2007), let those pins NC is ok,if without TV and CRT function.
PU80 to +3.3V_ALW by EC internal PU.
Q112 RHU002N06
R508 *47K_NC
THERM_ALERT#
THERM#
Q70 RHU002N06
R338 4.7K_4
SBAT_SMBDAT
MXMDATA
Q67 RHU002N06
R325 4.7K_4
SBAT_SMBCLK
MXMCLK
Q63 SI3424DV
R235 0_0402
C202 *470P/50V_NC
C219 .1U/50V/0603
Q72 SI3424DV
R355 0_0402
C348 *470P/50V_NC
C350 .1U/50V/0603
Q60 SI4800BDY-T1-E3
R190 0_0402
C172 *2200P/50V_NC
C173 .1U/50V/0603
R171 100K
R170 100K
MXM_ON
MXM_ON#
Q48 2N7002W-7-F
Q49 2N7002W-7-F
PWROK_MXM
R238 0_4
C656 *.1U/16V_4_NC
Q69 DTA114YUA
R332 10K_4
Q68 2N7002E
MXM_ACIN
MXM_PWROK
MXM_AC (31)
MAM_ACIN = AC/BATT#, Internal PD 10K
AC/BATT# | PIN157
0(Default) | Nominal performance
1 | High performance
MXM_AC
AC Mode | HI
Battery Mode | LOW
AC +MXM Hi temperature | LOW
L23 HI0805R800R-10_0805
L24 HI0805R800R-10_0805
C162 0.01U_6
C197 0.01U_6
C144 10U/25V/1206
C447 4.7U/25V_8
C437 4.7U/25V_8
C438 4.7U/25V_8
C452 .1U/25V_4
C450 .1U/25V_4
C449 .1U/25V_4
C349 10U/10V_8
C346 .1U/16V_4
C588 *.1u_4_NC
C587 *.1u_4_NC
C586 *.1u_4_NC
C347 *.1u_4_NC
C215 1U/10V_4
C216 .1U/16V_4
C584 1U/10V_4
C585 .1U/16V_4
C199 10U/10V_8
C196 .1U/16V_4
QUANTA COMPUTER
Title MXM
Size Document Number MX3 Rev 2C
Date Friday, October 12, 2007 Sheet 17 of 53
http://laptop-motherboard-schematic.blogspot.com/

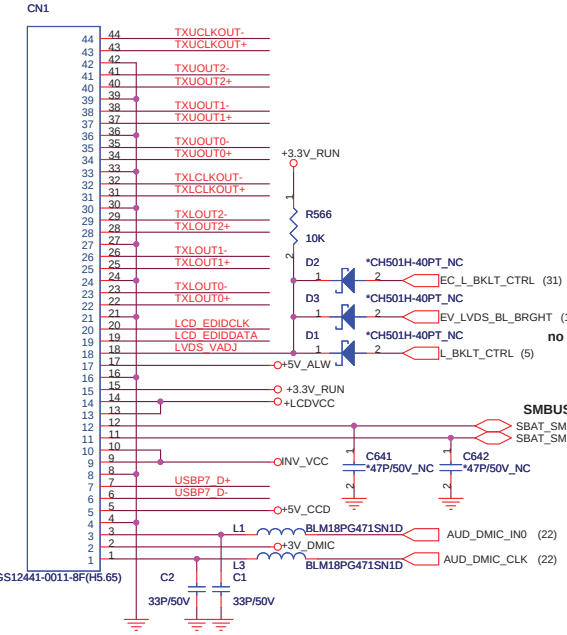
HYBRID setting





MXM_UMA#	Display mode
0	Hybrid-UMA
1	Hybrid-MXM

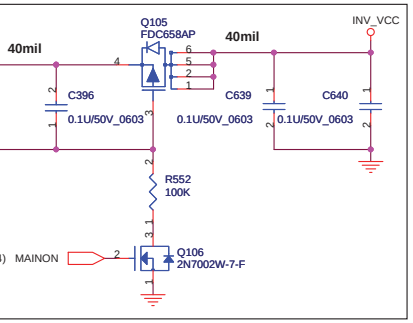


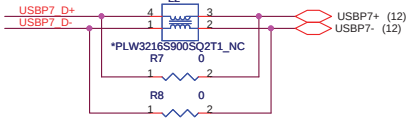


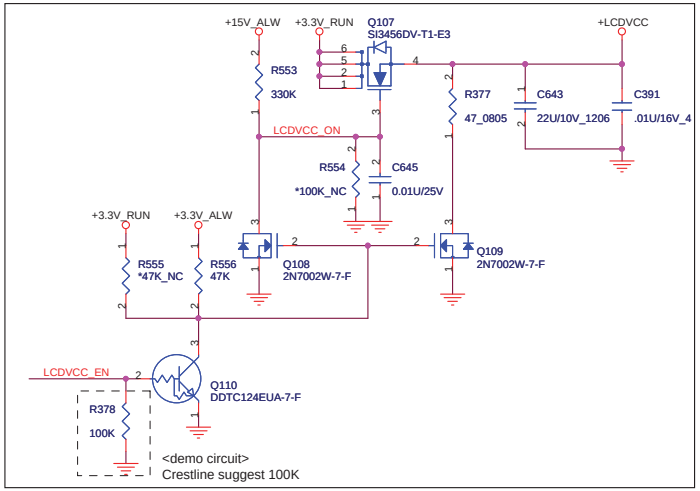
no DPST support

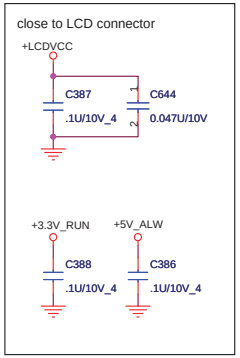
SMBUS Address [58]
SBAT_SMBCLK (17,31,36,45)
SBAT_SMBDAT (17,31,36,45)

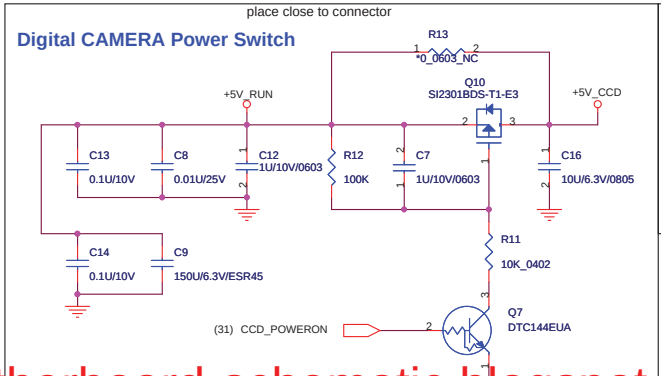
Add : A9H --Contrast
AAH --Backlight

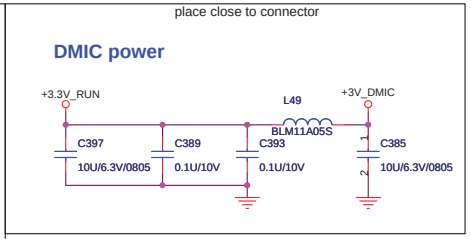








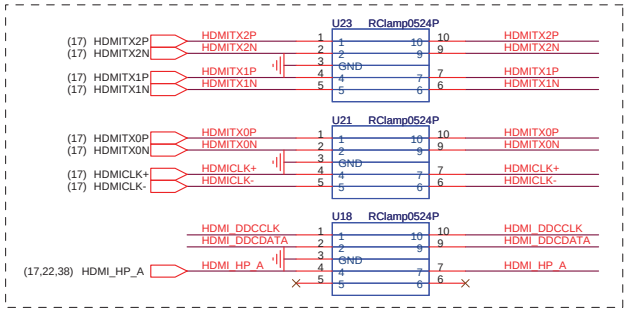




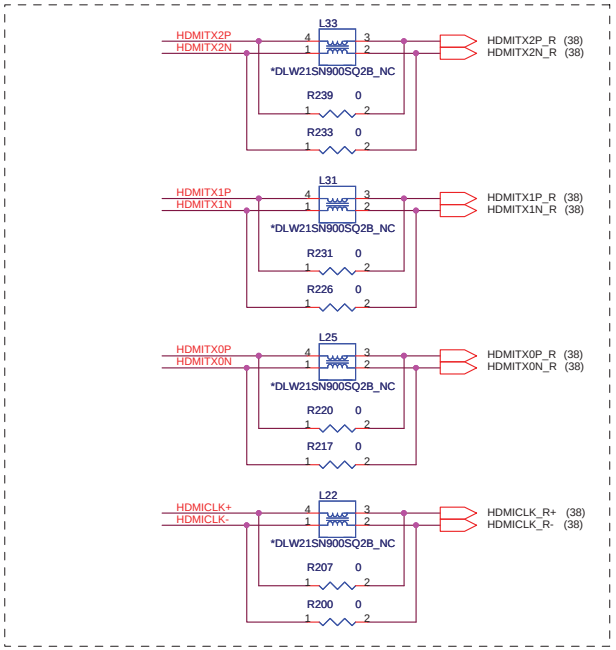
QUANTA COMPUTER

Title	LVDS/E-switch/CCD/DMIC	
Size	Document Number MX3	Rev 2A
Date: Friday, October 12, 2007	Sheet 18 of 53	

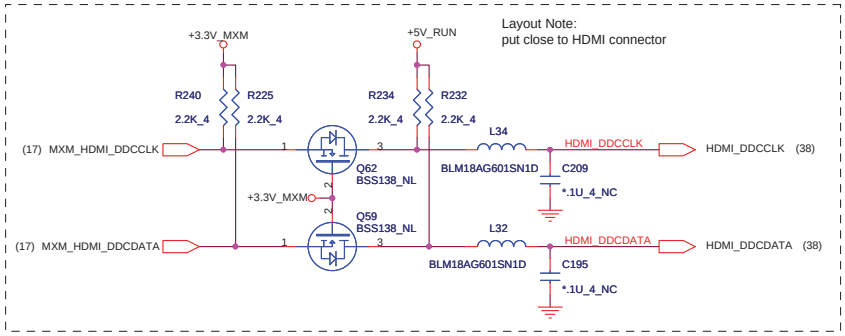
HDMI



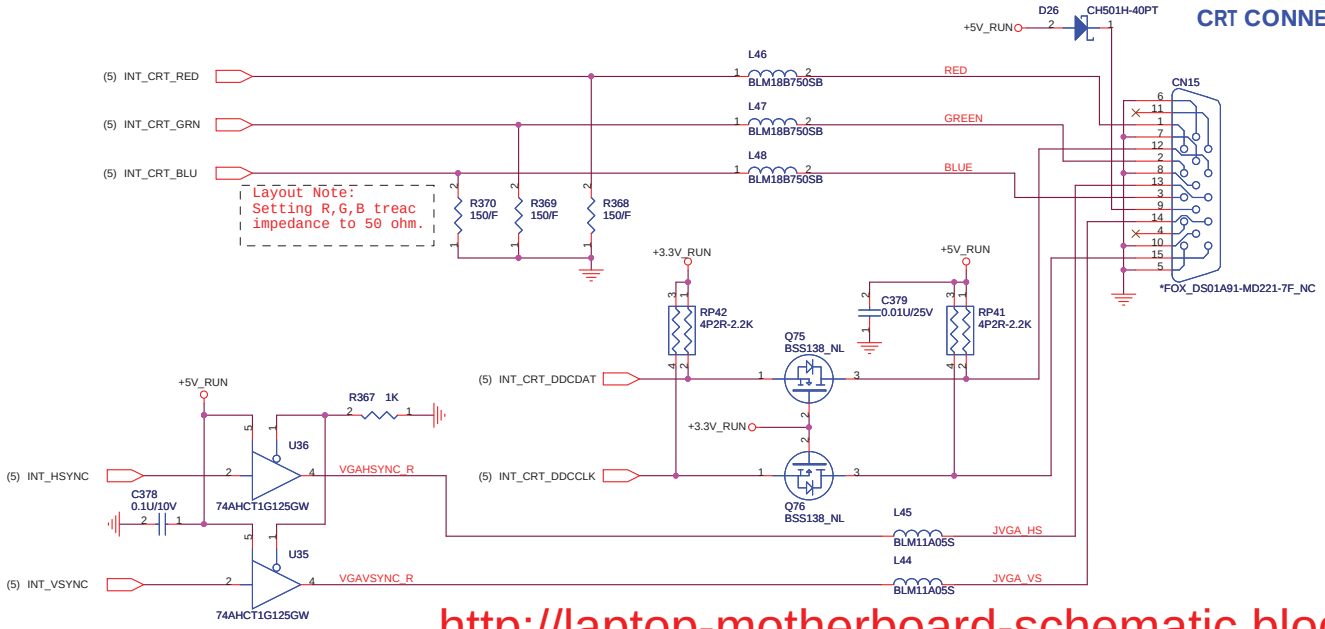
for ESD



for EMI

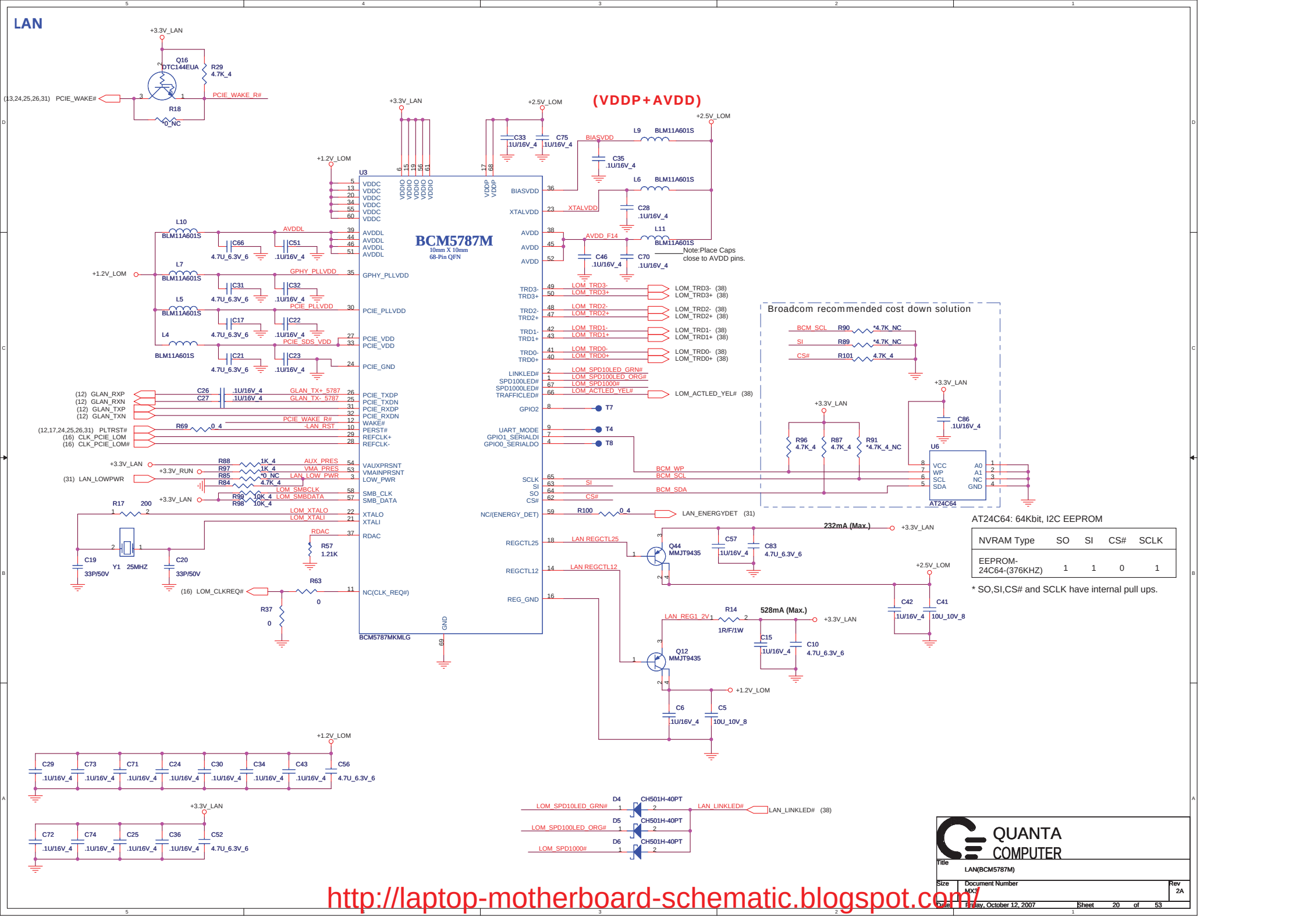


CRT CONNECTOR FOR Debug



QUANTA COMPUTER		
Title	HDMI & CRT(for debug)	
Size	Document Number MX3	Rev 2B
Date	Friday, October 12, 2007	Sheet 19 of 53

LAN



AT24C64: 64Kbit, I2C EEPROM

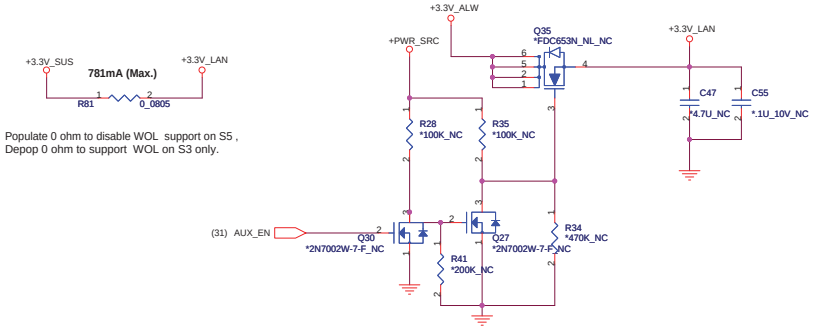
NVRAM Type	SO	SI	CS#	SCLK
EEPROM-24C64-(376KHZ)	1	1	0	1

* SO,SI,CS# and SCLK have internal pull ups.

QUANTA COMPUTER

Title	LAN(BCM5787M)	
Size	Document Number MX3	Rev 2A
Date: Friday, October 12, 2007	Sheet 20 of 53	

LAN POWER



QUANTA COMPUTER

Title	LAN Power	
Size	Document Number MX3	Rev 1A
Date: Friday, October 12, 2007	Sheet 21 of 53	

Codec

PORT_X Pin: W/S=10/10
VREFOUT_X Pin: W/S=10/10
FOR HP : W/S=20/20
Power Pin : 20mil

Layout

Analog

The Gap between Analog & Digital should be 60 ~ 100 mil

Digital

Width : 50 mil

Realtek : Tied at one point only under the codec or near the codec

add more three 0 ohm for EMI solution

Place sense Res close to Audio Codec SENSE B
PORT E : 39.2K 1% ; PORT F : 20K 1%
PORT G : 10K 1% ; PORT H : 5.1K 1%

ALC885

(PORT B)

(PORT E)

Place sense Res close to Audio Codec SENSE A
PORT A : 39.2K 1% ; PORT B : 20K 1%
PORT C : 10K 1% ; PORT D : 5.1K 1%

PC BEEP CONTROL

For SPDIF Out switch between SPDIF Jack & HDMI, default is to SPDIF Jack.

nVDIA Card	ATI_HP# = HI
ATI Card or UMA	ATI_HP# = LOW

MAX9789A TQFN 32PIN

AUDIO AMPLIFIER

Q57, Vgs(th) Max. = 1.6V, ALC885 pin 47 (SPDIF/EAPD) has a bias 1.6V as high.

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

FB 60ohm +-25% 100MHz, 3A, 0.05ohm DC

close to amplifier pin 8.

close to amplifier pin 18.

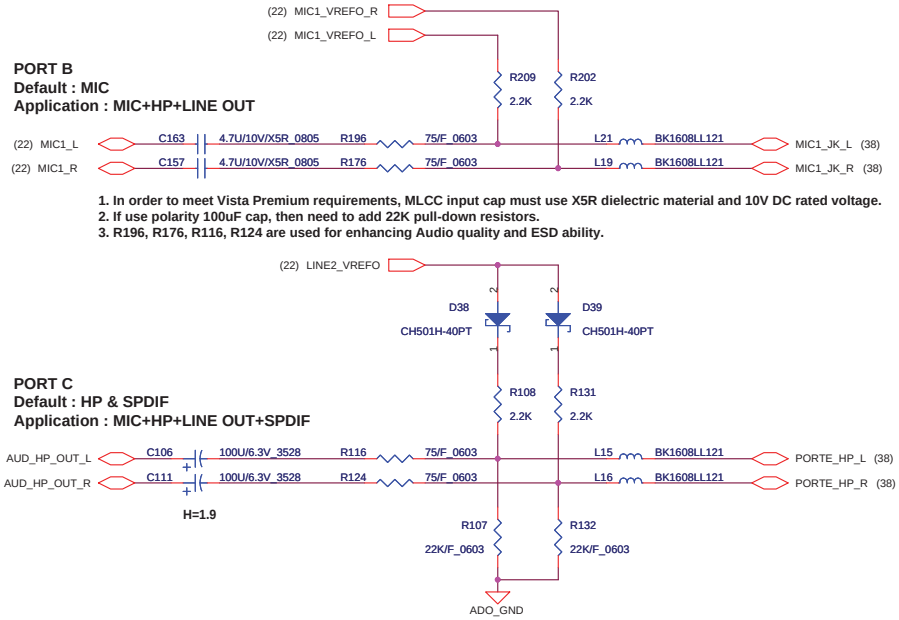
For TPA6040A, pop Cap, depop Res.

For TPA6040A, pop Cap, depop Res.

Int. Stereo Speakers

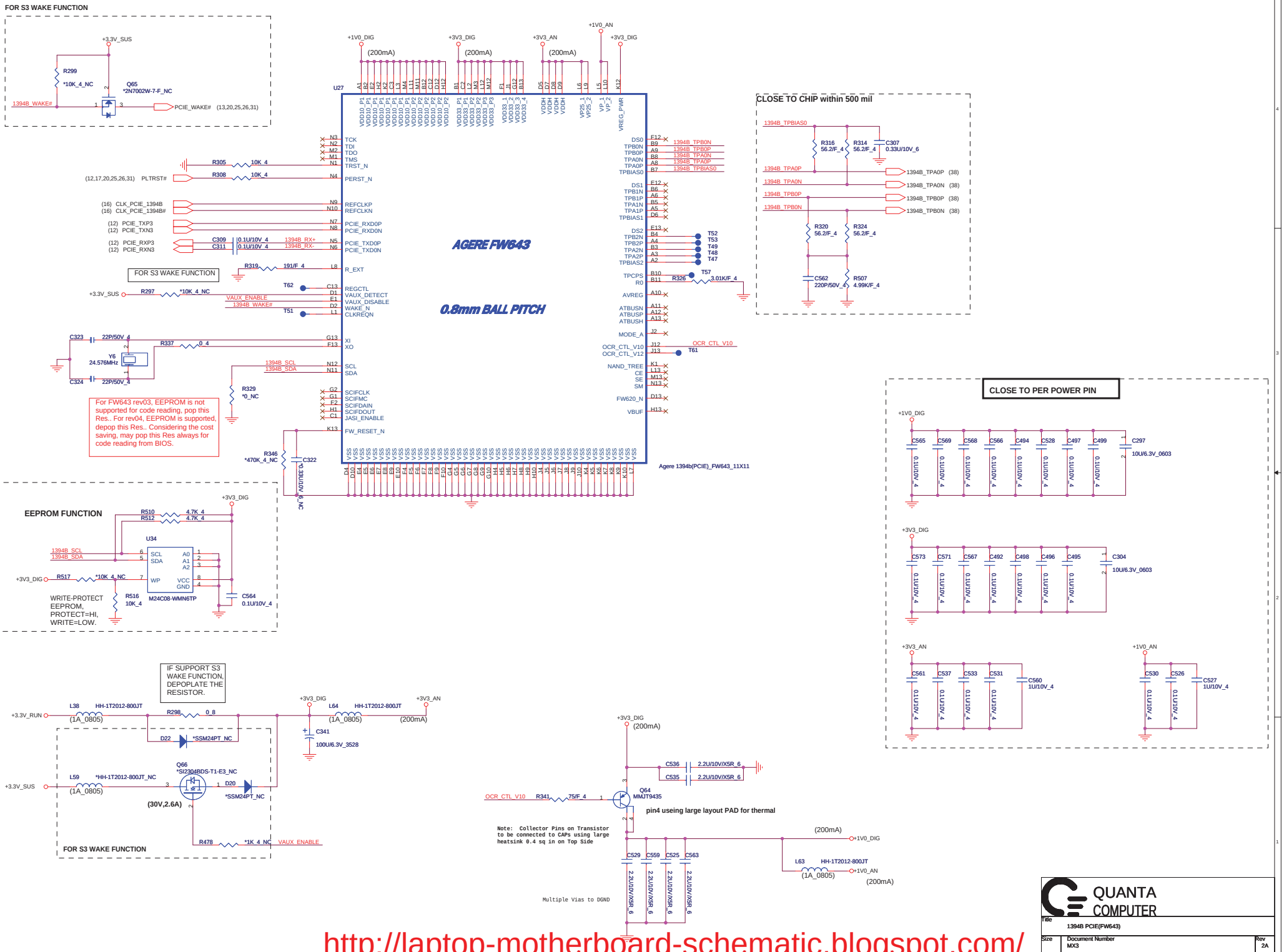
QUANTA COMPUTER

Title: Audio ALC885/AMP/SPK
Size: Document Number: MX3
Rev: 2C
Date: Friday, October 12, 2007
Sheet 22 of 53



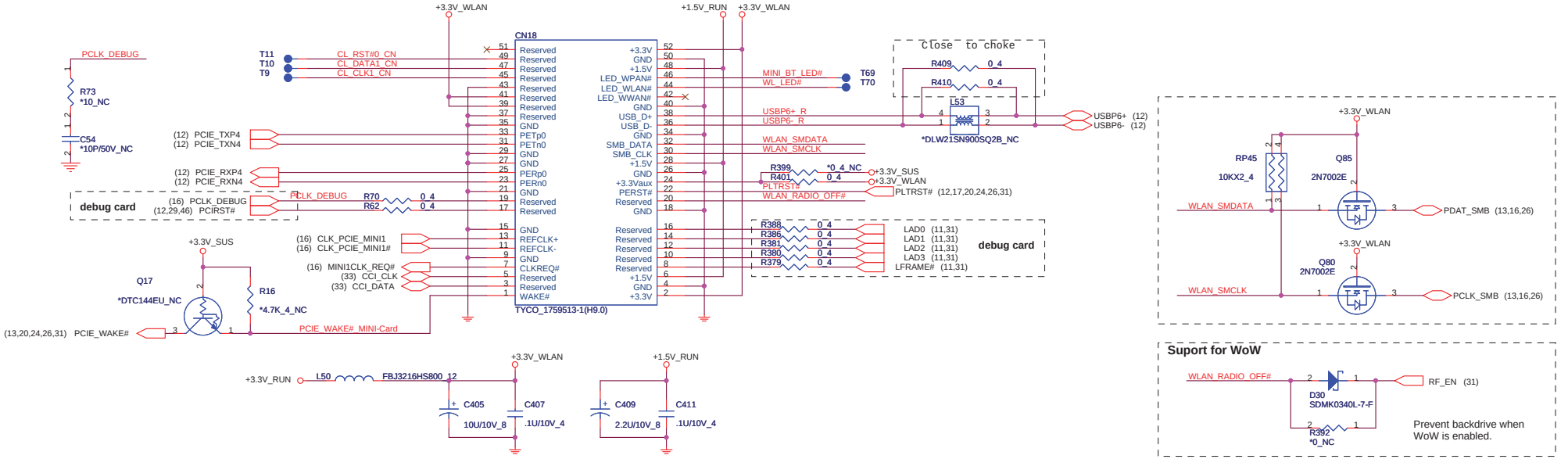
QUANTA COMPUTER

Title	Audio HP/MIC		
Size	Document Number MX3		Rev 2A
Date	Friday, October 12, 2007	Sheet 23 of 53	

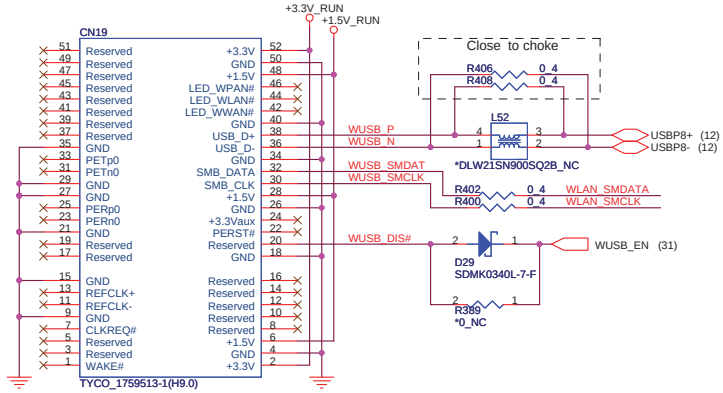


MINI-Card

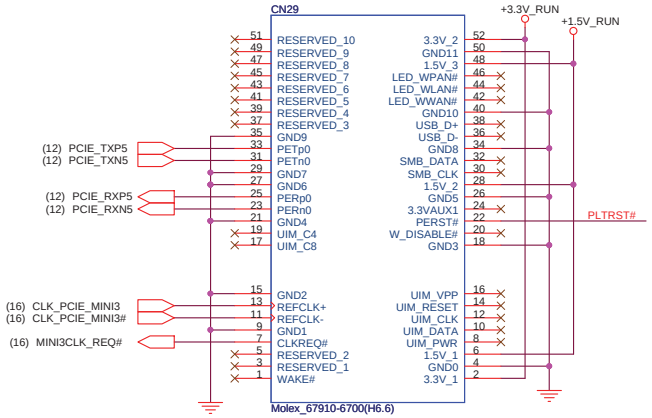
MiniCard connector - WLAN



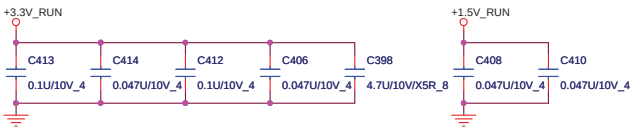
MiniCard connector - Wireless-USB



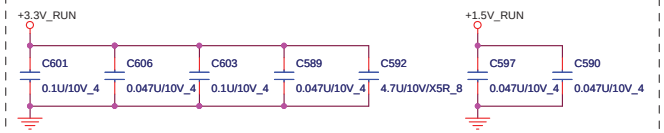
MiniCard connector - Robson



Place as close as possible to WUSB connector



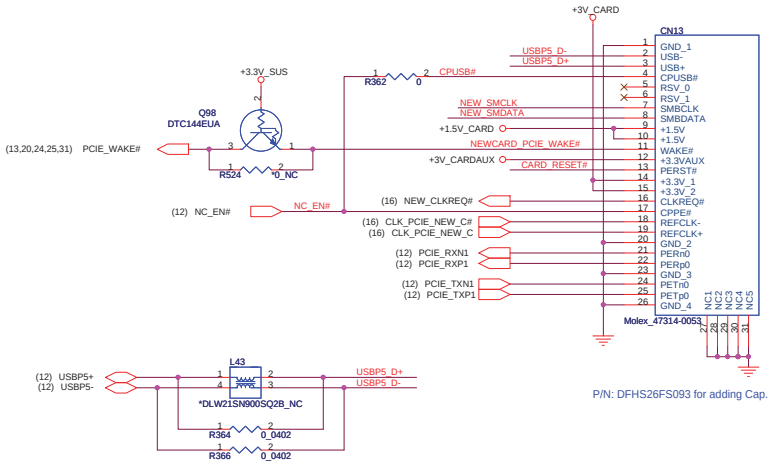
Place as close as possible to Robson connector



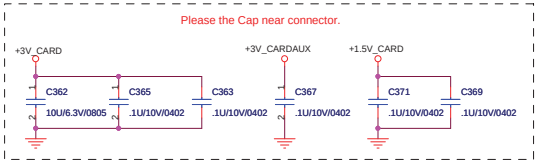
QUANTA COMPUTER

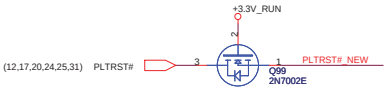
Title	Mini Card(WLAN/WUSB/Rob)	
Size	Document Number MX3	Rev 1A
Date	Friday, October 12, 2007	Sheet 25 of 53

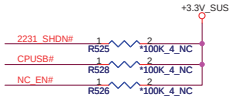
Express Card

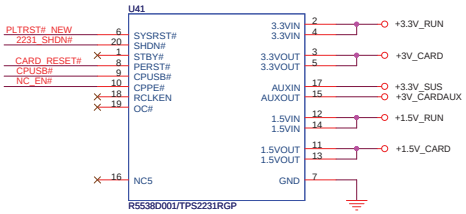


P/N: DFHS26FS093 for adding Cap.

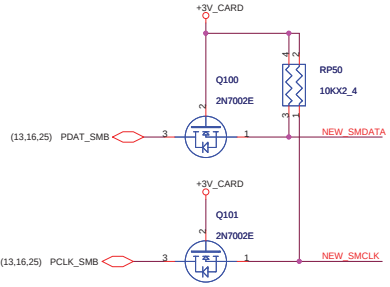


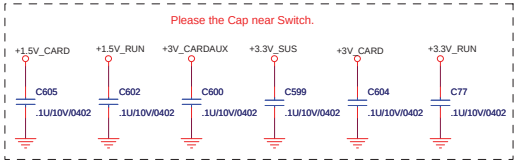






+1.5V_CARD Max. 650mA, Average 500mA
+3V_CARD Max. 1300mA, Average 1000mA
+3V_CARDAUX Max. 400mA, Average 275mA

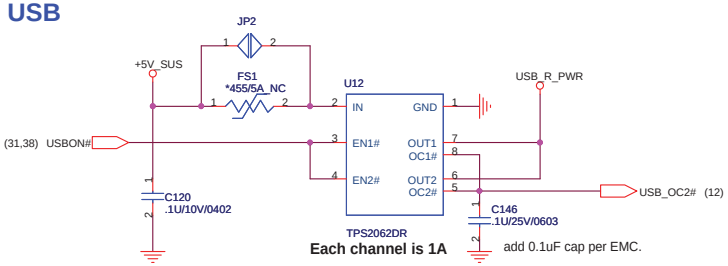




QUANTA COMPUTER

Title	Express Card	
Size	Document Number MX3	Rev 2B
Date: Friday, October 12, 2007	Sheet 26 of 53	

USB



H29 H-C236D110P2
H27 h-c276d110i150p2
H24 H-TC236BC276I150D110P2

AUDIO
H16 H-TC236BC276D118P2
ADO_GND

H2 h-c276d110i150p2

Guild point
H30 H-TC110BC177D110P2
H17 H-TC106BC177D106P2

H3 h-c276d126i166p2

H23 H-TC236BC276I174D134P2
H19 H-TC236BC276I174D134P2
H28 H-TB8_5X7BC12I4_4D3_4P2
H31 h-c276d134i174p2
H20 h-c276d134i174p2
H4 h-c276d134i174p2

H10 h-c276d138i178p2

CPU Fan
H9 h-c276d138i197p2

H7 h-c315d102i142p2
H8 h-c315d102i142p2
H13 h-c315d102i142p2
H14 h-c315d102i142p2

MXM Card
H18 *h-c315d138i178p2_NC
H21 *h-c315d138i178p2_NC
H15 h-c315d138i178p2
H22 h-c315d138i178p2

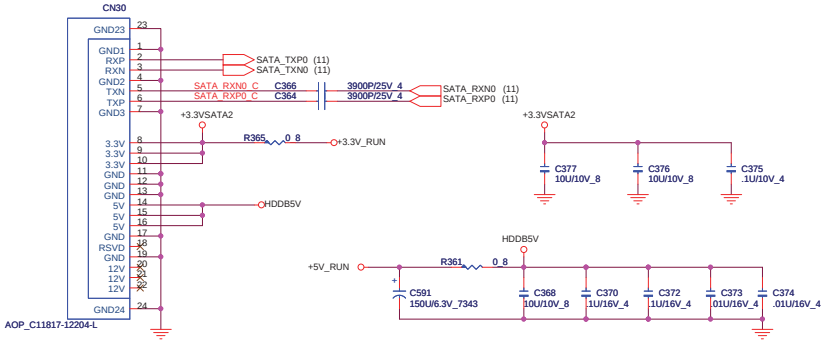
Mini Card
H5 h-c315d138i178p2
H6 h-c315d138i178p2
H11 h-c315d138i178p2
H12 h-c315d138i178p2
H25 h-c315d138i178p2
H26 h-c315d138i178p2

H1 h-tc236bc276d110i150p2

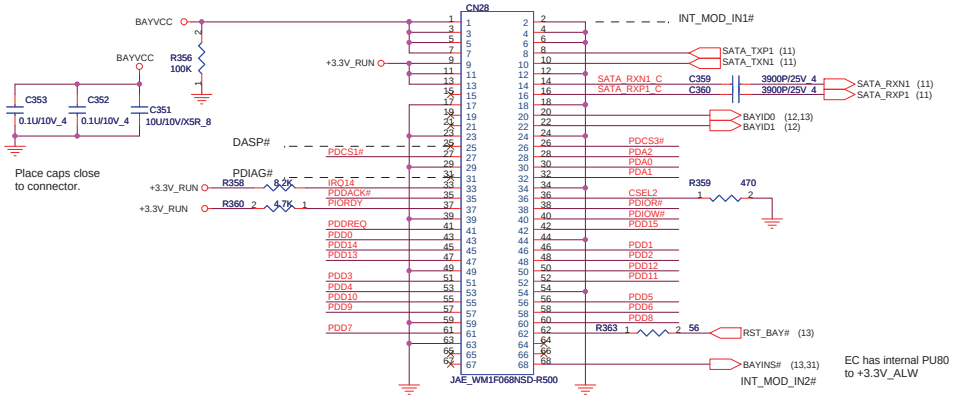
QUANTA COMPUTER

Title	Right Side USB Power/Hole	
Size	Document Number MX3	Rev 2B
Date: Friday, October 12, 2007	Sheet 27 of 53	

Main



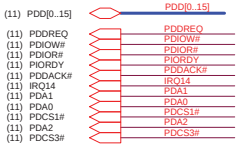
BAY(ODD,HDD)

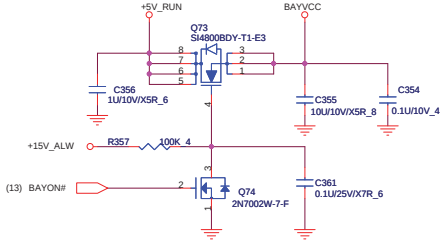


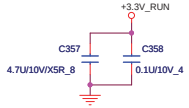
EC has internal PU80 to +3.3V_ALW

LBAY_ID_STATUS

LEFT BAYID1	LEFT BAYID0	STATUS	
0	0	(SATA)	ODD
1	0		HDD
0	1	(PATA)	ODD
1	1		HDD

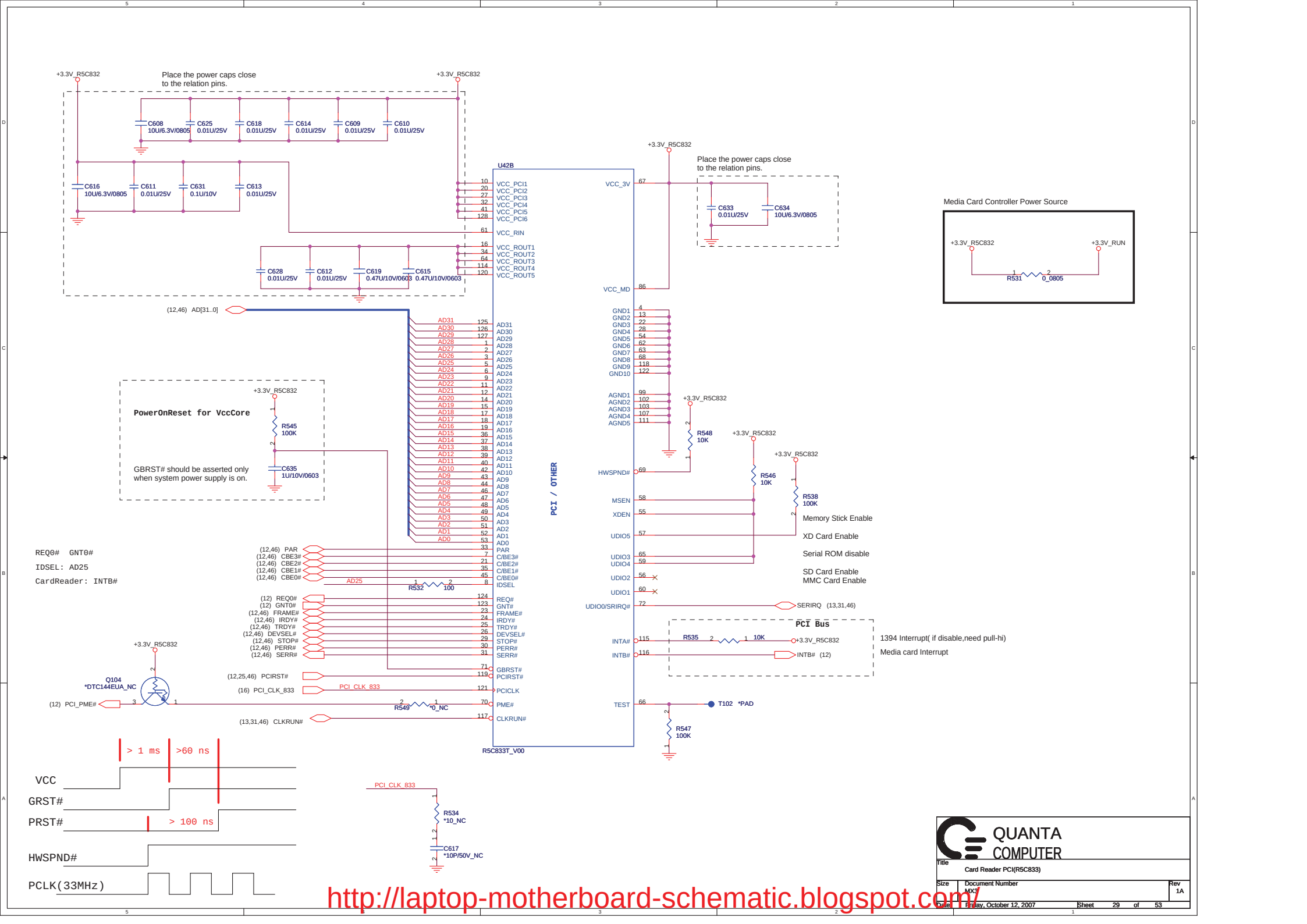


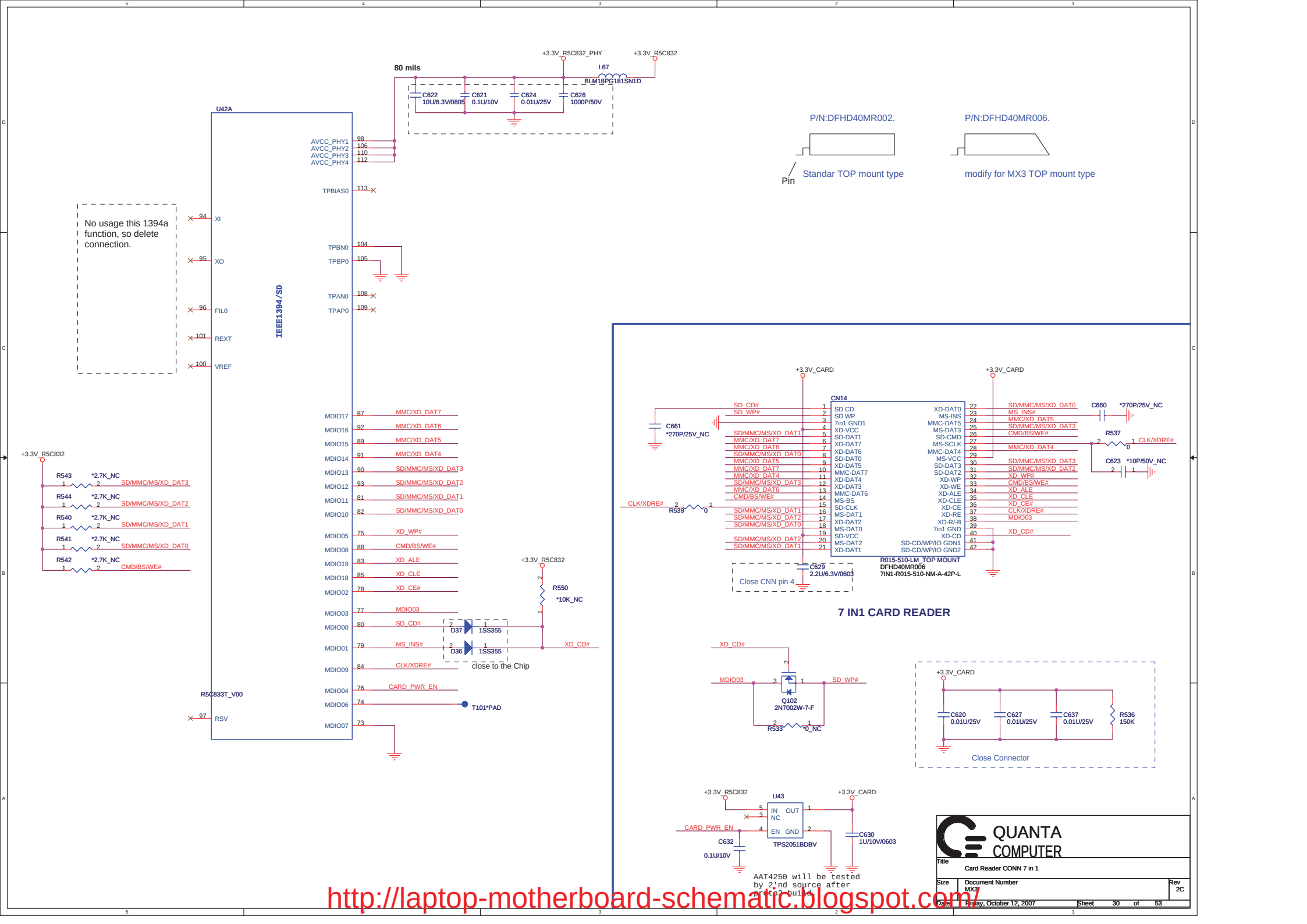




QUANTA COMPUTER

Title	SATA-HDD & Module Bay	
Size	Document Number MX3	Rev 1A
Date: Friday, October 12, 2007	Sheet 28 of 53	





1/13 Comfirm by vendor mail:
VBAT for keep PLL power let power up can quick.
If no VBAT will switch to VCCpower.
If PLL no power will cause boot time delay.

1/13 Comfirm by vendor mail:
VDD must power up after
VCC/AVCC

+3.3V_ALW 25mA (Typ.) L30 BLM18AG601SN1D
+A3VPCU
+VCCRTC 2.5uA (Typ.)
+3.3V_RUN 10mA (Typ.)

C190 2.2U/10V_8 C423 .1U/10V_4 C439 .1U/10V_4 C428 .1U/10V_4 C421 .1U/10V_4 C107 .1U/10V_4
C182 .1U/10V_4 C191 10U/10V_8
C424 .1U/10V_4
C156 .1U/10V_4 C150 10U/10V_8
8769AGND

U16 WPC8769LDG

VCC1 VCC2 VCC3 VCC4 VCC5 AVCC VBAT VDD

TEMP_PBAT (45)
TEMP_SBAT (45)
ADAPT_OC_IINP (39)
C180 .1U/10V_4
+3.3V_RUN
R436 8.2K_4
R438 *0_4_NC
R437 0_4
THERM_ALERT# (17,37)
THERM_ALERT_SB# (13)
THERM_ALERT_EC#
ACC_ON (35)
SM_ON (35)

PCLK_591 R185 *22_4_NC C158 *10P_4_NC

(11,25) LFRAME# 3 LFRAME
(11,25) LAD0 126 LAD0
(11,25) LAD1 127 LAD1
(11,25) LAD2 128 LAD2
(11,25) LAD3 1 LAD3
(16) PCLK_591 2 LCLK
(13,29,46) CLKRUN# 8 CLKRUN/GPIO11/HGPIO02
(11) GATEA20 121 GA20
(11) RCIN# 122 KBRST
(13) SCI# 29 ECSCI
(22) ATI_HP# 6 GPIO24/HGPIO01
(32) INSTANT_ON# 124 LPCPD/GPIO10/HGPIO00
(12,17,20,24,25,26) PLTRST# 7 LRESET
(18) MXM_UMA# 123 PWUREQ/GPIO63
(13,29,46) SERIRQ 125 SERIRQ
(13) KBSMI# 9 SMI/GPIO64
LPC

D7 CH501H-40PT SCI# uR T72

08/10 FAE: SMI DOESN'T NEED DIODE

A/D
AD0/GPI90 97
AD1/GPI91 98
AD2/GPI92 99
AD3/GPI93 100 THERM_ALERT_EC#
AD4/GPIO05 108 ACC_ON (35)
AD5/GPIO04 96 SM_ON (35)

D/A
DA0/GPI94 101 CC-SET (39)
DA1/GPI95 105 CPUFAN_SET# (37)
DA2/GPI96 106 MXMFAN_SET# (37)
DA3/GPI97 107 R117 0_4 LED_KEYBD_PRESENT# (36)

GPIO
GPIO01 64 R574 0 AW_PWR_BTN_OUT ACIN (34,39,40,44)
GPIO03 95 NBSWON# AW_PWR_BTN_OUT (36)
GPIO06/HGPIO06 93 R592 0_4 NBSWON# (32)
GPIO07/HGPIO07 94 SUSB# LID_HALL_EN# (13,32)
GPIO23 119 SUSB# (6,13,34)
GPIO30 109 EC_FPBACK# (18)
GPIO31 120 BT_ON (35)
GPIO32 65 WUSB_EN (25)
GPIO33 66 R112 0_4 MMB_SMBINT SCROLL_ON (36)
GPIO36 15 MMB_SMBINT (36)
GPIO40 16 VRON (41)
GPIO42/TCK 17 PWROK_MXM MAINON (18,22,43,44)
GPIO43/TMS 20 PWROK_MXM (17,44)
GPIO44/TDI 21 AMP_MUTE# (22)
GPIO45 22 AUX_EN (21)
GPIO46/TRST 23 LAN_ENERGYDET SUSON (34,42,43,44)
GPIO47/DEN0 24 LAN_ENERGYDET (20)
GPIO50/TDO 25 CHG_SBATT (34,40)
GPIO51 26 CHG_PBATT (34,40)
GPIO52/RDY 27 LAN_LOWPWR MXM_PRS# (17)
GPIO53 28 HWPG LAN_LOWPWR (20)
GPIO81 91 DNBSWON# uR D16 CH501H-40PT DNBSWON# (13)
GPO82/HGPO00/TRIS 110 BT_POWERON# (33)
GPO84/HGPO01/BADDR0 112 CCD_POWERON CCD_POWERON (18)
T17 08/10 FAE: ADD TP FOR DEBUG
CCD_POWERON ACITVE LO => HI

KB
(32) MX0 54 KBSIN0
(32) MX1 55 KBSIN1
(32) MX2 56 KBSIN2
(32) MX3 57 KBSIN3
(32) MX4 58 KBSIN4
(32) MX5 59 KBSIN5
(32) MX6 60 KBSIN6
(32) MX7 61 KBSIN7
MY0
(32) MY0 53 KBSOUT0/JENK
(32) MY1 52 KBSOUT1/TCK
(32) MY2 51 KBSOUT2/TMS
(32) MY3 50 KBSOUT3/TDI
(32) MY4 49 KBSOUT4
(32) MY5 48 KBSOUT5/TDO
(32) MY6 47 KBSOUT6/RDY
(32) MY7 43 KBSOUT7
(32) MY8 42 KBSOUT8
(32) MY9 41 KBSOUT9
(32) MY10 40 KBSOUT10
(32) MY11 39 KBSOUT11
(32) MY12 38 KBSOUT12/GPIO64
(32) MY13 37 KBSOUT13/GPIO63
(32) MY14 36 KBSOUT14/GPIO62
(32) MY15 35 KBSOUT15/GPIO61/XOR_OUT
(32) MY16 34 KBSOUT16/GPIO60
(35) WLAN_ON 33 KBSOUT17/GPIO57/HGPIO03

TIMER
TA1/GPIO56 31 R115 *0_4_NC PCIE_WAKE# (13,20,24,25,26)
TA2/GPIO20 117 MXM_FAN_TACH (37)
TB1/GPIO14/HGPIO04 63 CPU_FAN_TACH (37)
A_PWM0 32 EC_L_BKLT_CTRL (18)
A_PWM1/GPIO21 118 USBON# (27,38)
B_PWM0/GPIO13 62 VOL_ON (36)

SPI
SPI_DI/GPIO77 84 AUDIO_AVDD_ON (22)
SPI_DO/GPO76/SHBM 83 RF_EN RF_EN (25)
SPI_SCK/GPIO75 82 T14 ELC_RESET (34)

SMB
(37,45) PBAT_SMBCLK PBAT_SMBCLK 70 SCL1
(37,45) PBAT_SMBDAT PBAT_SMBDAT 69 SDA1
(17,18,36,45) SBAT_SMBCLK SBAT_SMBCLK 67 SCL2/GPIO61
(17,18,36,45) SBAT_SMBDAT SBAT_SMBDAT 68 SDA2/GPIO62

IR
GPIO72 75 RSMRST# uR R136 0_4 RSMRST# (13)
GPIO70 73 SUSC# (13)
GPIO71 74 PWROK_EC_uR R134 0_4 PWROK_EC (13)
SIN_CR/CIRRX/GPIO87 113 PBAT_DSCHG (40)
GPIO34/CIRRX2 14 CIRRX2 (33)
CIRTX/GPIO16/HGPIO04 114 SBAT_PRES# (40)
SOUT_CR/GPO83/BADDR1 111 SOUT_CR_DEBUG

PS/2
(32) TBCLK 72 PSCLK1
(32) TBDATA 71 PSDAT1
(36) CAPS_ON 10 PSCLK2/GPIO26
(36) NUM_ON 11 PSDAT2/GPIO27
(44) S5_ON 12 PSCLK3/GPIO25
(13,28) BAYINS# 13 PSDAT3/GPIO12

FIU
F_SDI 86 SPI_SDI_uR
F_SDO 87 SPI_SDO_uR R203 22 SPI_SDO_uR_R
F_CS0 90 SPI_CS0#_uR
F_SCK 92 SPI_SCK_uR R197 22 SPI_SCK_uR_R
SWD/GPIO66 81 SWD_DEBUG R165 0_4 MXM_AC (17)
T12
CLKOUT/GPIO55 30 TP_RIM_ON (32)
VCC_POR 85 VCC_POR# R192 4.7K_4 +3.3V_ALW
VREF 104 VREF_uR R213 0_4 +A3VPCU

Den_1012: del R210 and EC_SOUT_CR_DEBUG net,because CN6 del.

for EMI

Den_1012: add for TP LED ON/OFF control.

32KX1/32KCLKIN 77 8768_32KX1
32KX2 79 8768_32KX2
R150 20M
Y4 32.768KHZ
R157 33K/F
C130 15P/50V
C149 15P/50V
8769AGND

08/10 FAE:
Add one GND pad under Xtal, and keep cleance.

1/13 Comfirm by vendor mail :
Connect to AGND

GND1 GND2 GND3 GND4 GND5 GND6 AGND VCORF
L18 HZ0603B601R-00
C104 1U/16V
VCORF uR 44

0~AVCC power for DA pin power reference

08/14 FAE:
Please connect VREF(uRider pin104) to +A3VPCU instead of +3VPCU.

	MXM_AC
AC Mode	HI
Battery Mode	LOW
AC +MXM Hi temperature	LOW

+3.3V_RUN
R145 10K_4 HWPG
R143 0_4
D11 CH501H-40PT (44) HWPG_1.5V_RUN
D9 CH501H-40PT (42) HWPG_3/5V_SUS
D10 CH501H-40PT (43) HWPG_1.05V_VCCP
D8 CH501H-40PT (43) HWPG_1.8V_SUS

08/10 FAE:
L58 can change from BEAD to short.
But, please put AGND & 32K CAP & AVCC CAP at one point.

Keep BEAD for safe.

SM BUS PU

+3.3V_ALW
PBAT_SMBCLK R129 4.7K_4
PBAT_SMBDAT R130 4.7K_4
SBAT_SMBCLK R119 4.7K_4
SBAT_SMBDAT R128 4.7K_4
AW_PWR_BTN_OUT R572 10K
+3.3V_RUN
MMB_SMBINT R573 *10K_NC

I/O ADDRESS SETTING

	I/O Address	
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

BADDR0 CCD_POWERON R212 10K_4
BADDR1 SOUT_CR_DEBUG R211 *10K_4_NC
SHBM RF_EN R169 10K_4

1/13 Comfirm by vendor mail :
Disabled ('1') if using FWH device on LPC.
Enabled ('0') if using SPI flash for both system BIOS and EC firmware

U9 24LC08
+3.3V_ALW
PBAT_SMBCLK
PBAT_SMBDAT
SCL SDA A0 A1 A2 WP VCC GND
C98 .1U/10V_4
SMBus Address [A0]

SPI FLASH

+3.3V_ALW
R174 10K_4
U19 W25X80VSSIG
SPI_SDI_uR SPI_SDO_uR_R SPI_SCK_uR_R SPI_CS0#_uR
SO SI SCK CE VDD HOLD WP VSS
C155 .1U/10V_4

1/13 Comfirm by vendor mail :
If the Southbridge enables 'Long Wait Abort' by default, the flash device should be 50MHz (or faster)

Internal Keyboard or JTAG setting

+3.3V_ALW
R113 10K_4
R114 *10K_4_NC
R148 *10K_4_NC
MY0
CHG_SBATT

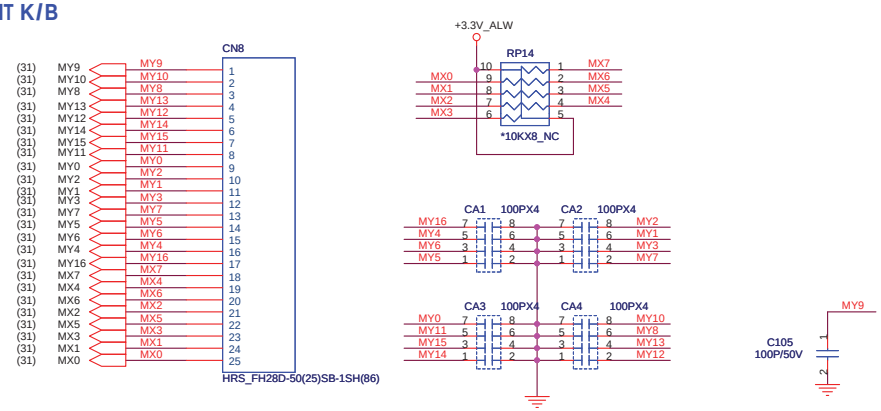
JEN0# = CHG_SBATT, JENK# = MY0; Internal PU(30K) for JEN0#, PU(80K) for JENK#

JEN0# (Pin 24)	JENK# (Pin 53)	Functionality of Pins 17,20,21,23,25,27	Functionality of Pins 47,48,50,51,52
1(Default)	1(Default)	GPIO Port signals	Keyboard Scan outputs
0	1	JTAG singnals	Keyboard Scan outputs
1	0	GPIO Port signals	JTAG singnals
0	0	Illegal Strap Combination	

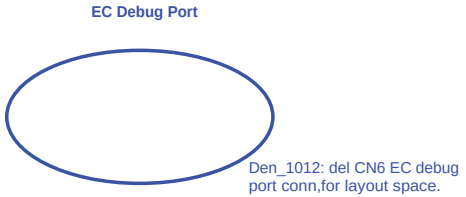
QUANTA COMPUTER

Title	EC(WPC8769LDG)	
Size	Document Number MX3	Rev 3A
Date: Friday, October 12, 2007	Sheet 31 of 53	

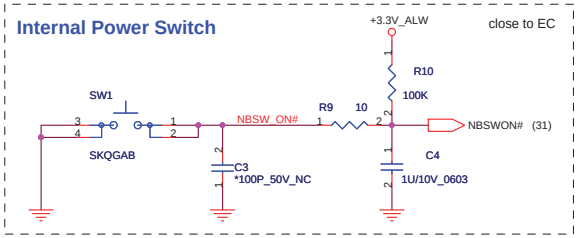
INT K/B



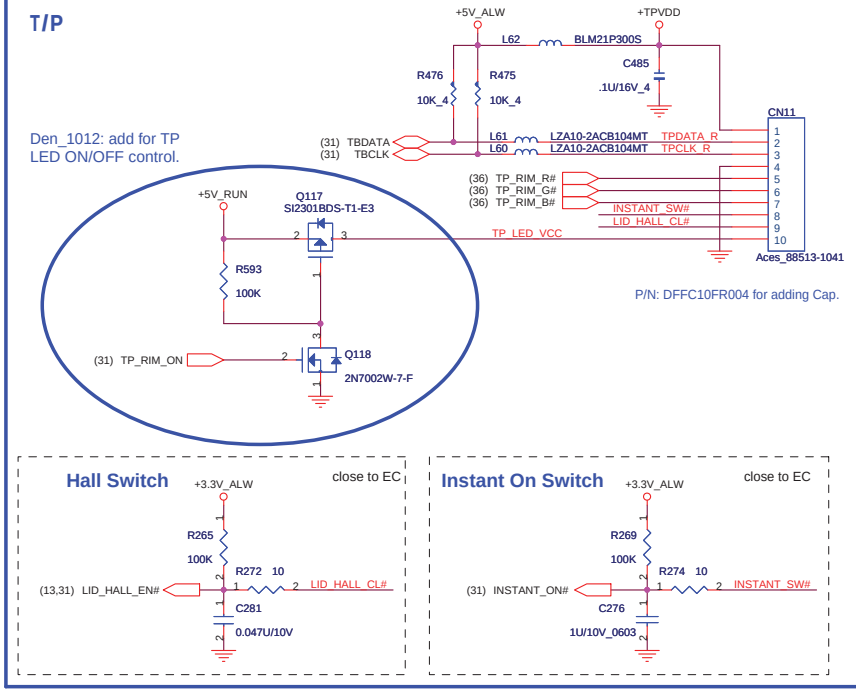
DEBUG PORT



Internal Power Switch



T/P



QUANTA COMPUTER

Title	KB/TP/SW/Hall IC/Debug	
Size	Document Number MX3	Rev 3A
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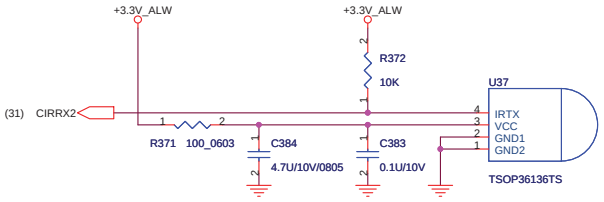
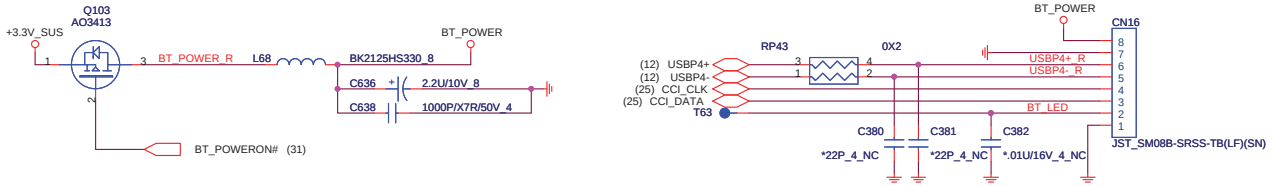
CIR module



BLUETOOTH MODULE CONNECTOR



QUANTA COMPUTER

Title	CIR & BT	
Size	Document Number MX3	Rev 2B
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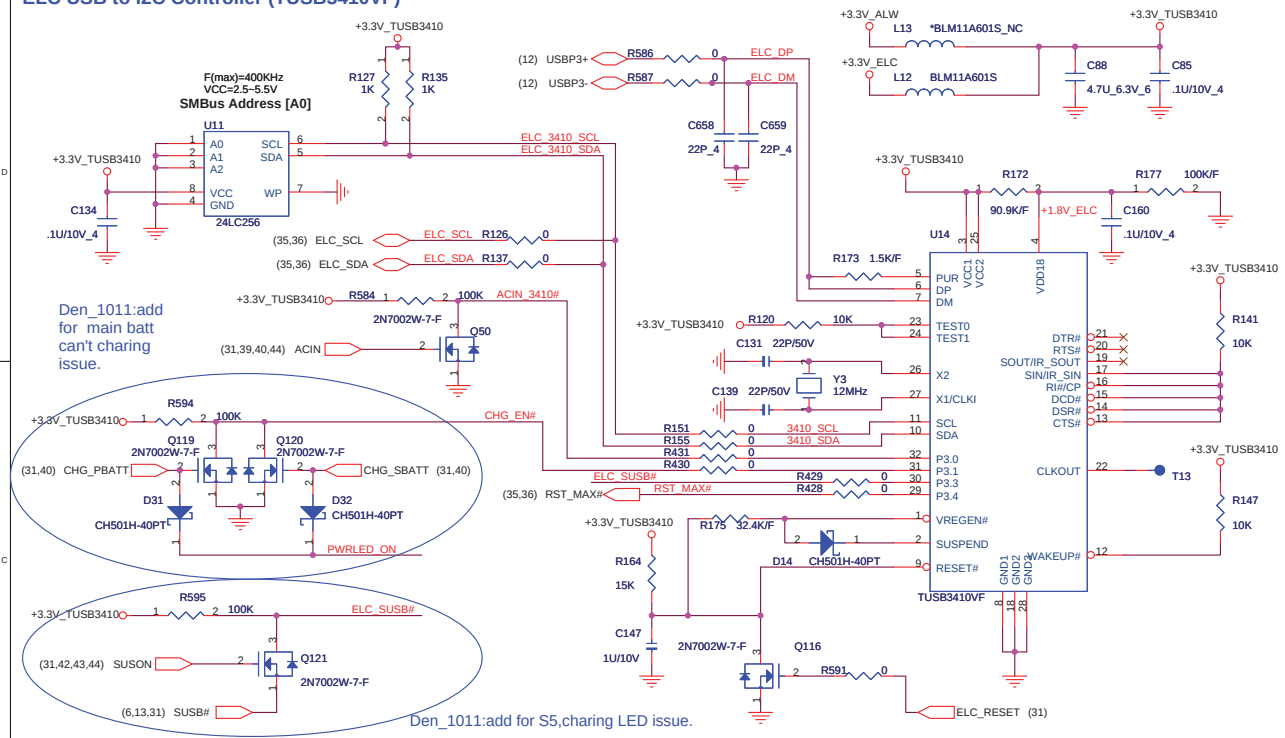
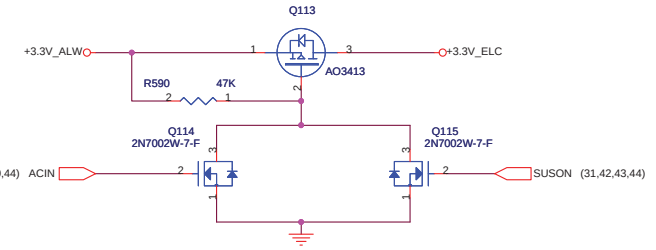
ELC USB to I2C Controller (TUSB3410VF)

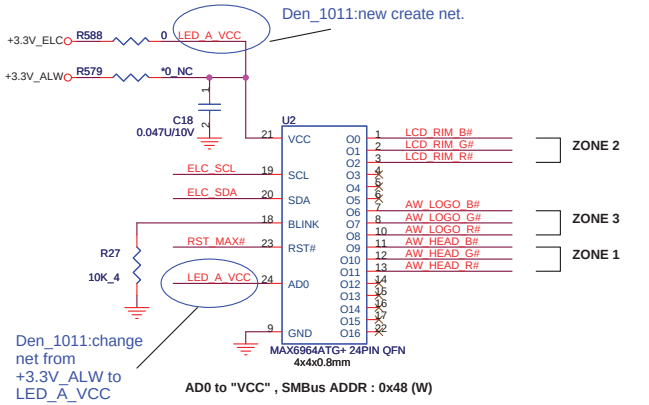


Den_1011:add for main batt can't charing issue.

Den_1011:add for S5,charing LED issue.



ZONE 1,2,3 --- ELC Controller (LCD Panel, A-Cover)

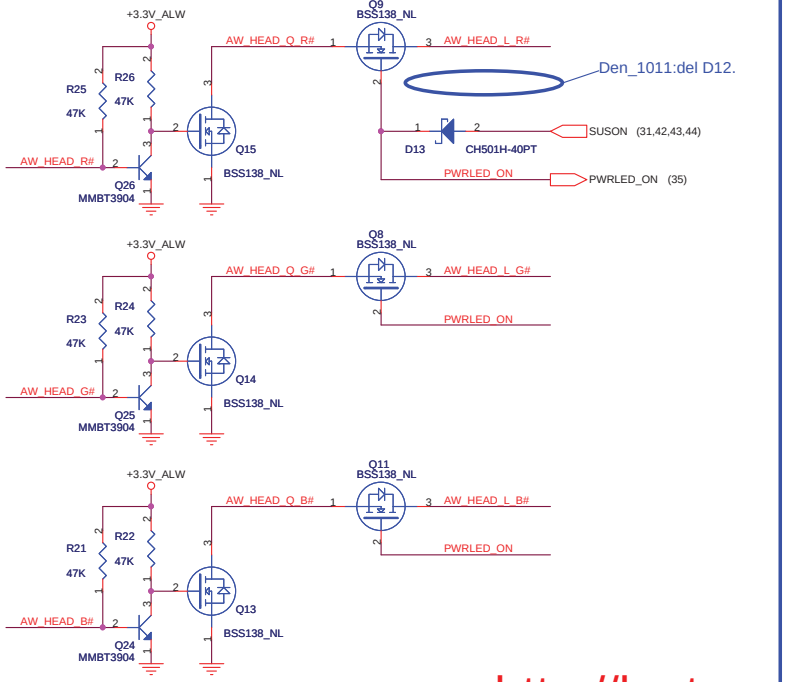


Den_1011:new create net.

Den_1011:change net from +3.3V_ALW to LED_A_VCC

ZONE 1 --- AW Head Buffer (A-Cover, RGB LED*3)

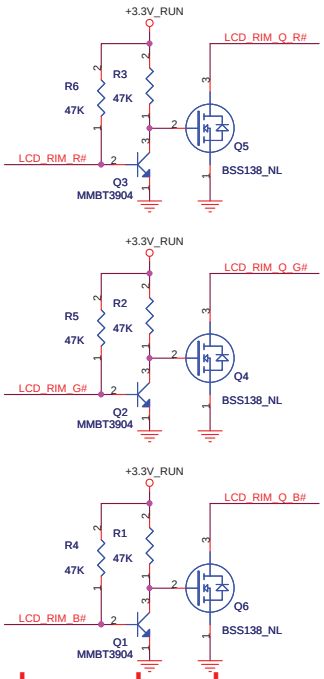
BSS138_NL, ID (max) = 0.22A



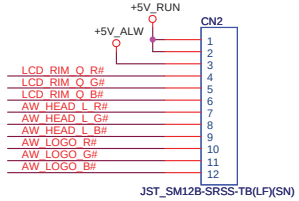
Den_1011:del D12.

ZONE 2 --- LCD RIM Buffer (A-Cover, RGB LED*4)

BSS138_NL, ID (max) = 0.22A



LED Connector (12 Pins) --- MB to LCD Panel (A-Cover)



ZONE 3 --- AW Logo (A-Cover, RGB LED*2)

QUANTA COMPUTER

Title	ELC TUSB3410VF & ZONE 1~3	
Size	Document Number MX3	Rev 3A
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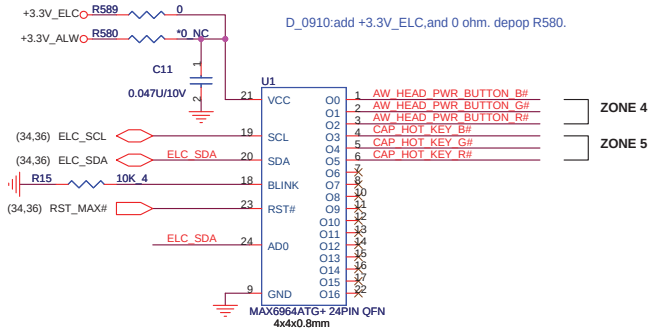
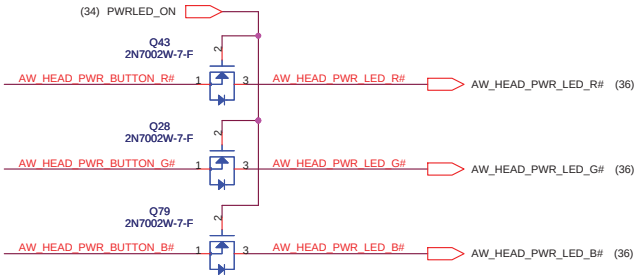
ZONE 4,5 --- ELC Controller (MMB Right/Left Board, C-Cover)

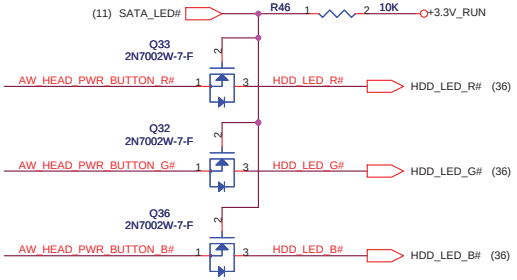


AD0 to "SDA" , SMBus ADDR : 0xC8 (W)

ZONE 4 --- Power Status--AW_Head_RIM (C-Cover, RGB LED*1)

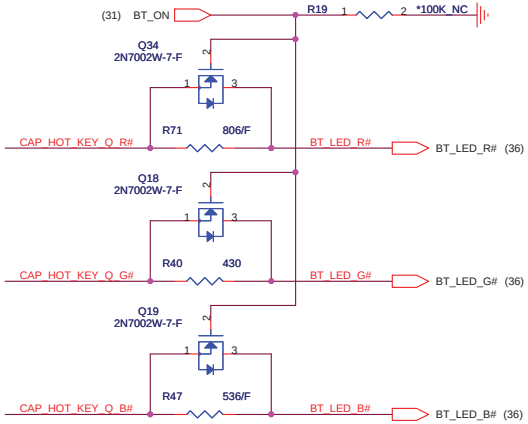


ZONE 4 --- HDD ACT--AW_Head_Eyes (C-Cover, RGB LED*1)



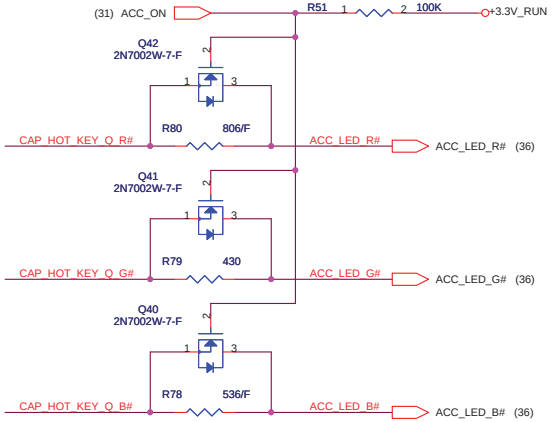
ZONE 5 --- BT (Bluetooth) LED

BT_ON: H (Brightness = 100%)
L (Brightness = 10%)



ZONE 5 --- ACC (Alienware command center) LED

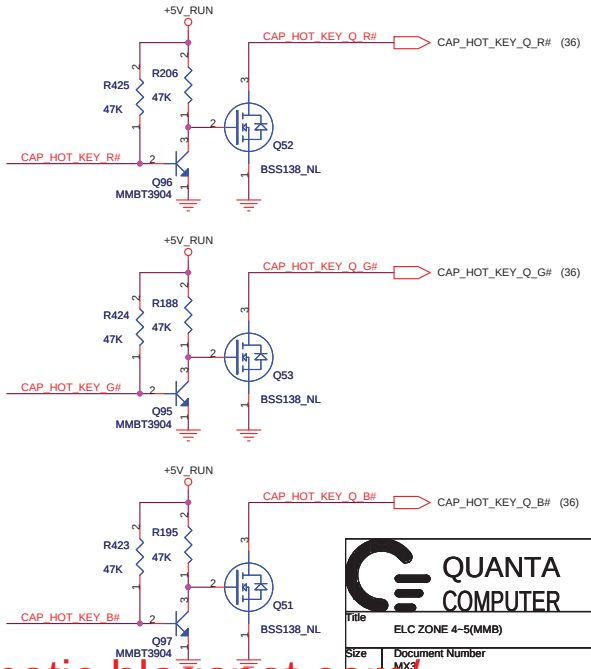
ACC_ON: H (Brightness = 100%)
L (Brightness = 10%)



ZONE 5 --- LED Buffer (C-Cover, RGB LED*7)

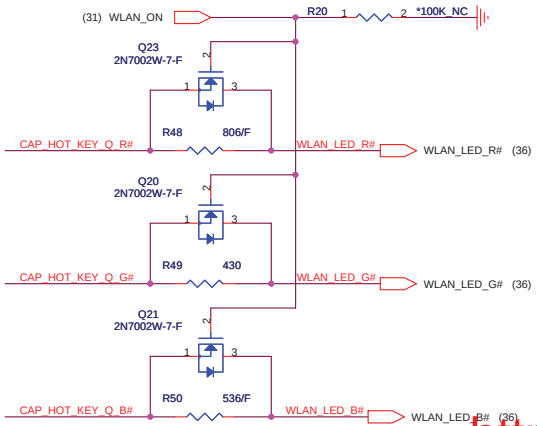
1.MMB Right -- BT/WLAN/ACC/SM (RGB LED*4)
2.MMB Left -- Caps/Num/Scroll Lock (RGB LED*3)

BSS138_NL, ID (max) = 0.22A



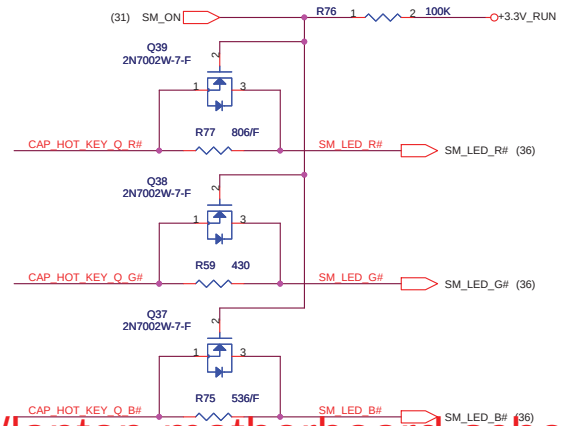
ZONE 5 --- WLAN (Wireless LAN) LED

WLAN_ON: H (Brightness = 100%)
L (Brightness = 10%)



ZONE 5--- SM (Silent Mode) LED

SM_ON: H (Brightness = 100%)
L (Brightness = 10%)



QUANTA COMPUTER

Title	ELC ZONE 4~5(MMB)	
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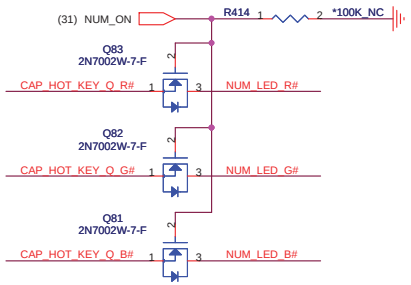
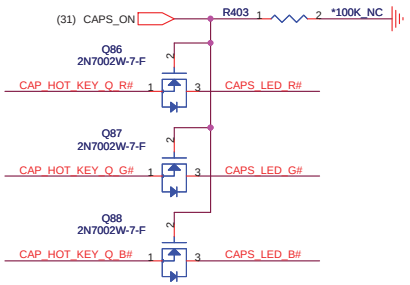
ZONE 5 --- NUM (Num Lock) LED

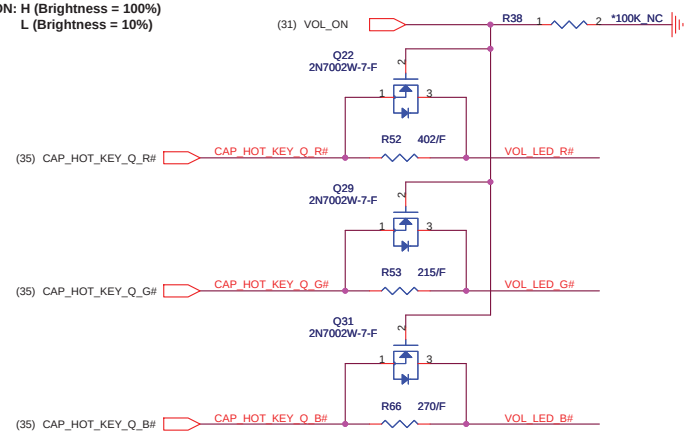


ZONE 5 --- CAPS (Caps Lock) LED

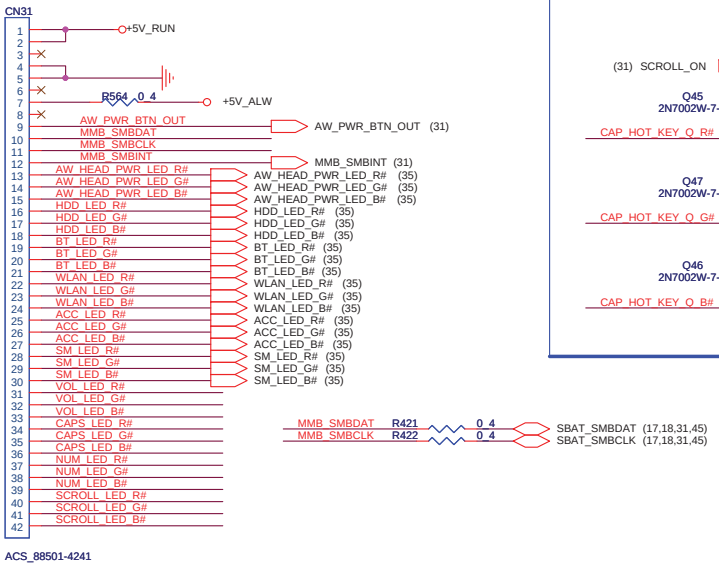


ZONE 5 --- VOL (Volumn Slider) LED

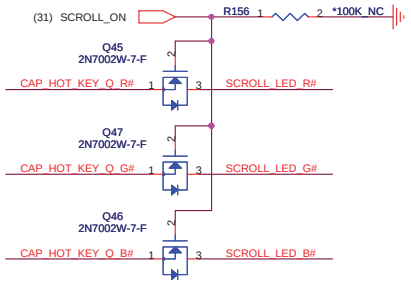
VOL_ON: H (Brightness = 100%)
L (Brightness = 10%)



MMB CONN (42Pins)

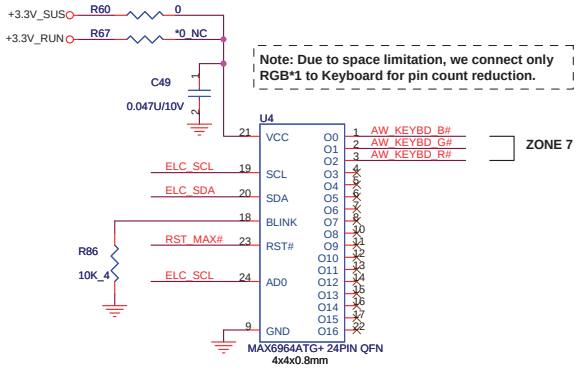


ZONE 5 --- SCROLL (Scroll Lock) LED



ZONE 7 --- ELC Controller (Keyboard)

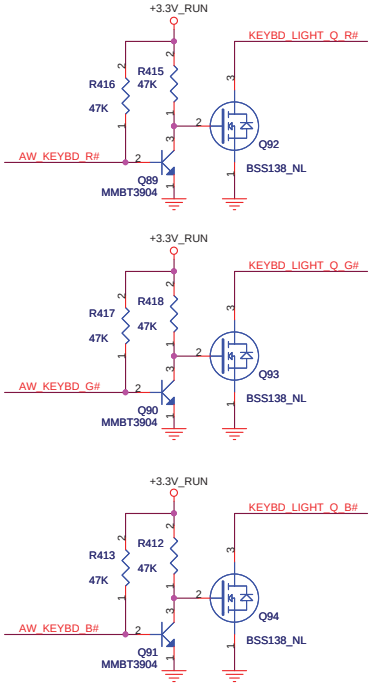
Note: LED Vendor: EVERLIGHT
P/N:12-23A/R6GHBHC-A01/2D



AD0 to "SCL" , SMBus ADDR : 0xC0 (W)

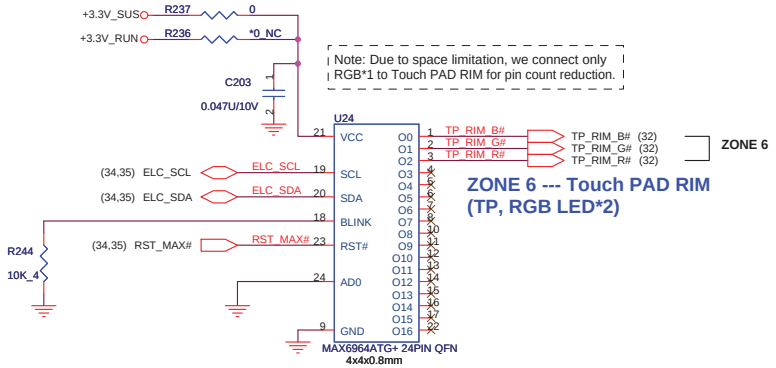
ZONE 7 --- Keyboard Buffer (KB, RGB LED*9)

BSS138_NL, ID (max) = 0.22A



ZONE 6 --- ELC Controller (Touch PAD RIM)

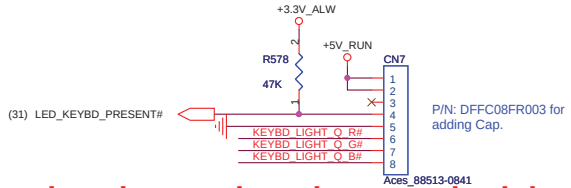
Note: LED Vendor: EVERLIGHT
P/N:12-23A/R6GHBHC-A01/2D



ZONE 6 --- Touch PAD RIM (TP, RGB LED*2)

AD0 to "GND" , SMBus ADDR : 0x40 (W)

LED Connector (8 Pins) --- MB to Keyboard



QUANTA COMPUTER

Title	ELC ZONE 5~7(MMB,TP,KB)	
Size	Document Number MX3	Rev 2B
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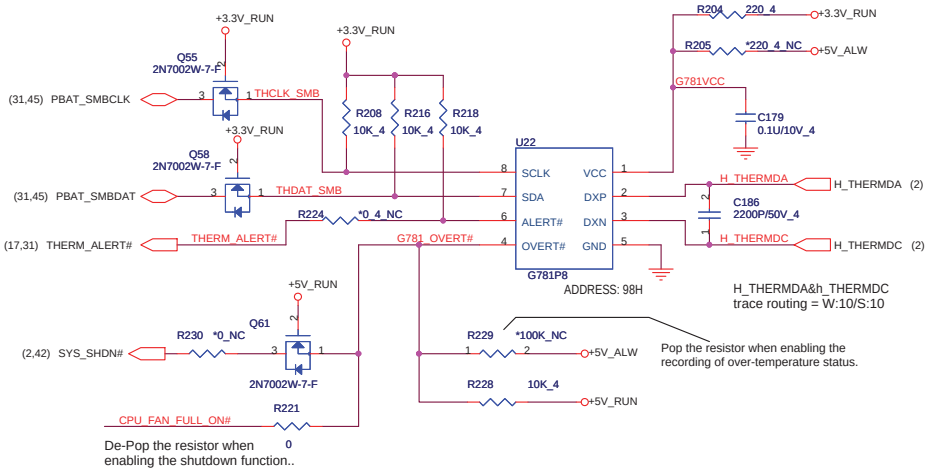
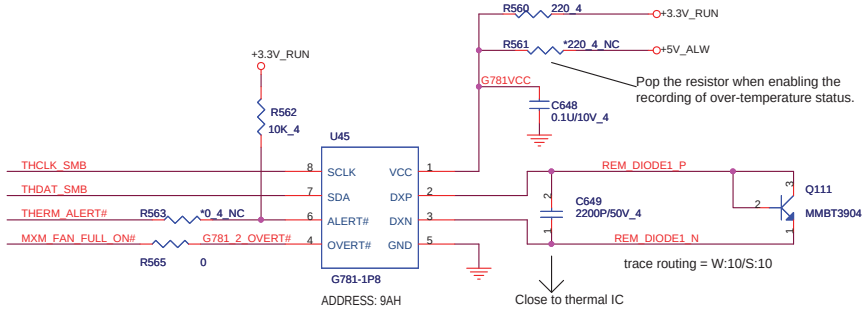
THERMAL

A: FOR CPU TEMP.
B: MB SKIN TEMP (CPU SIDE)



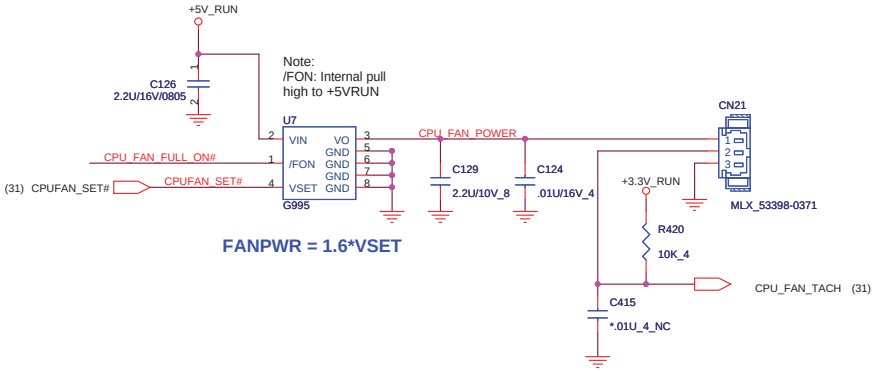
Note: The Over-Temperature flags stay high until cleared by POR, or until the status byte register is read.

C: FOR MXM MODULE TEMP.
D: MB SKIN TEMP (MXM MODULE)

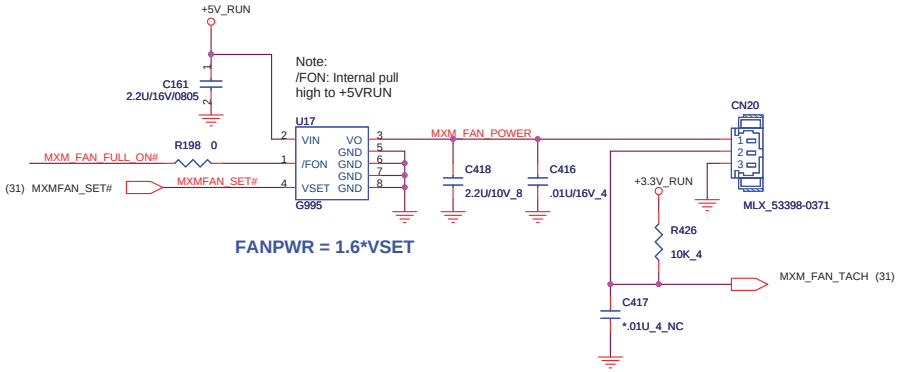


Note: The Over-Temperature flags stay high until cleared by POR, or until the status byte register is read.

CPU FAN



MXM FAN



QUANTA COMPUTER

Title	Thermal & Fan	
Size	Document Number MX3	Rev 2A
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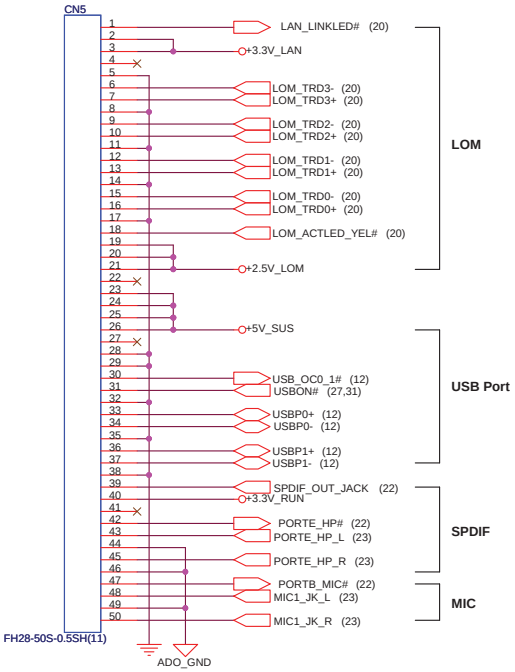
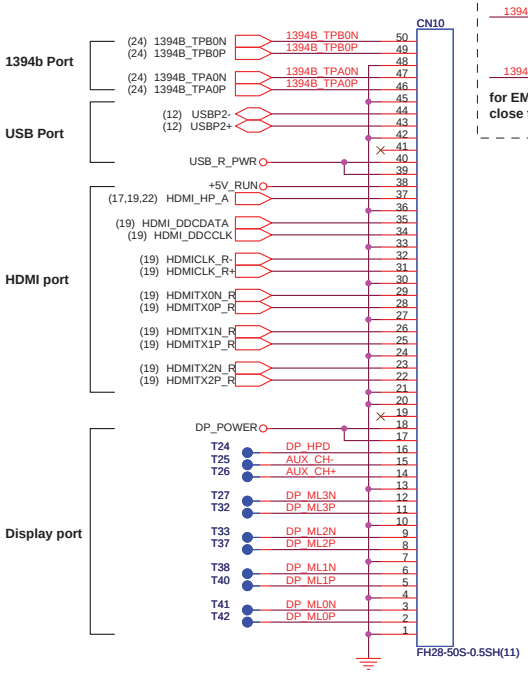
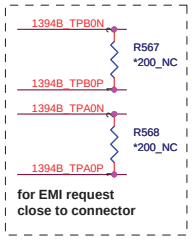
to AUDIO board connector



to HDMI board connector





QUANTA COMPUTER

Title	To IO Board	
Size	Document Number MX3	Rev 2A
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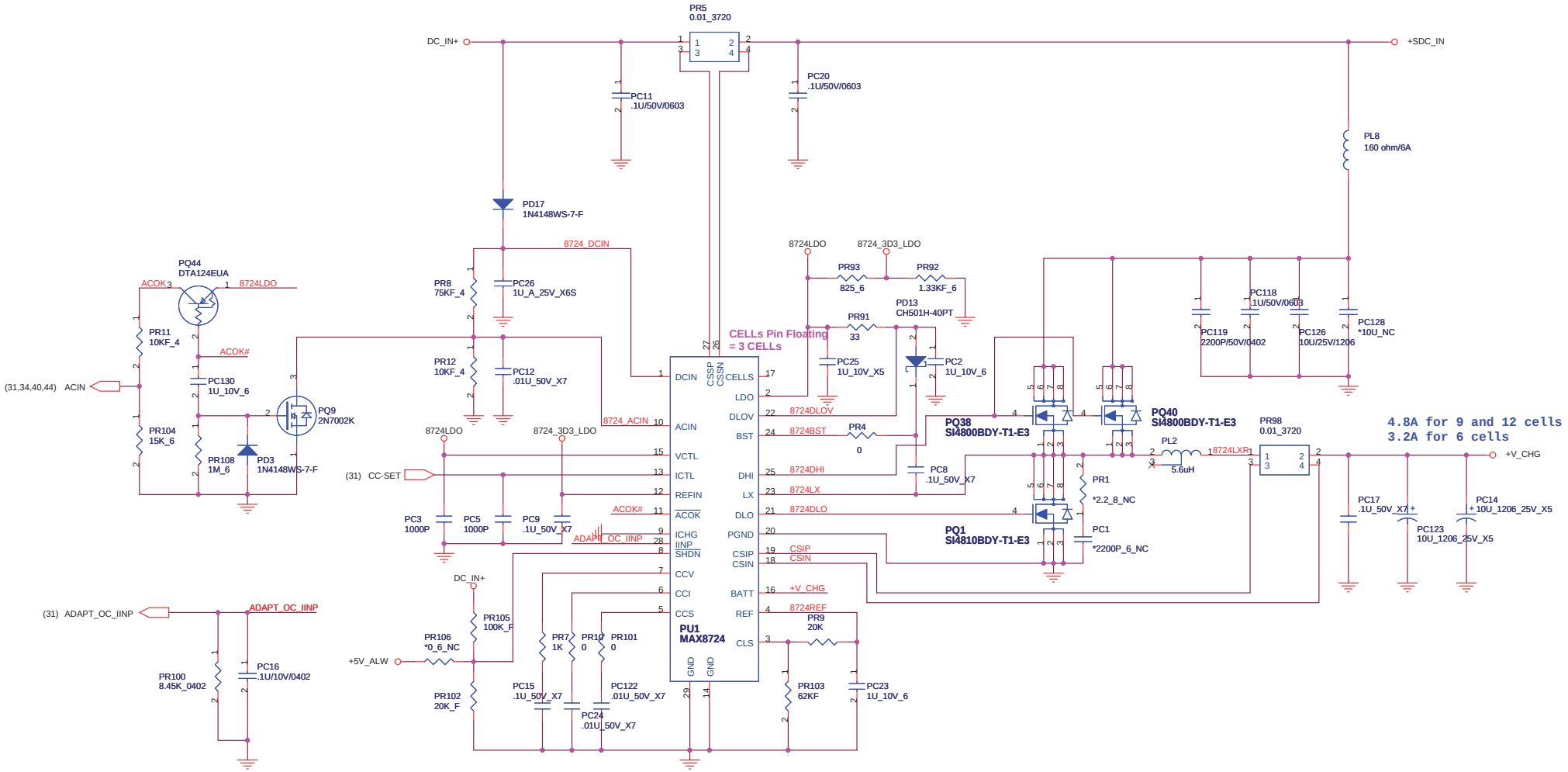

QUANTA COMPUTER

Title	Charger(MAX8724)	
Size	Document Number MX3	Rev 2C
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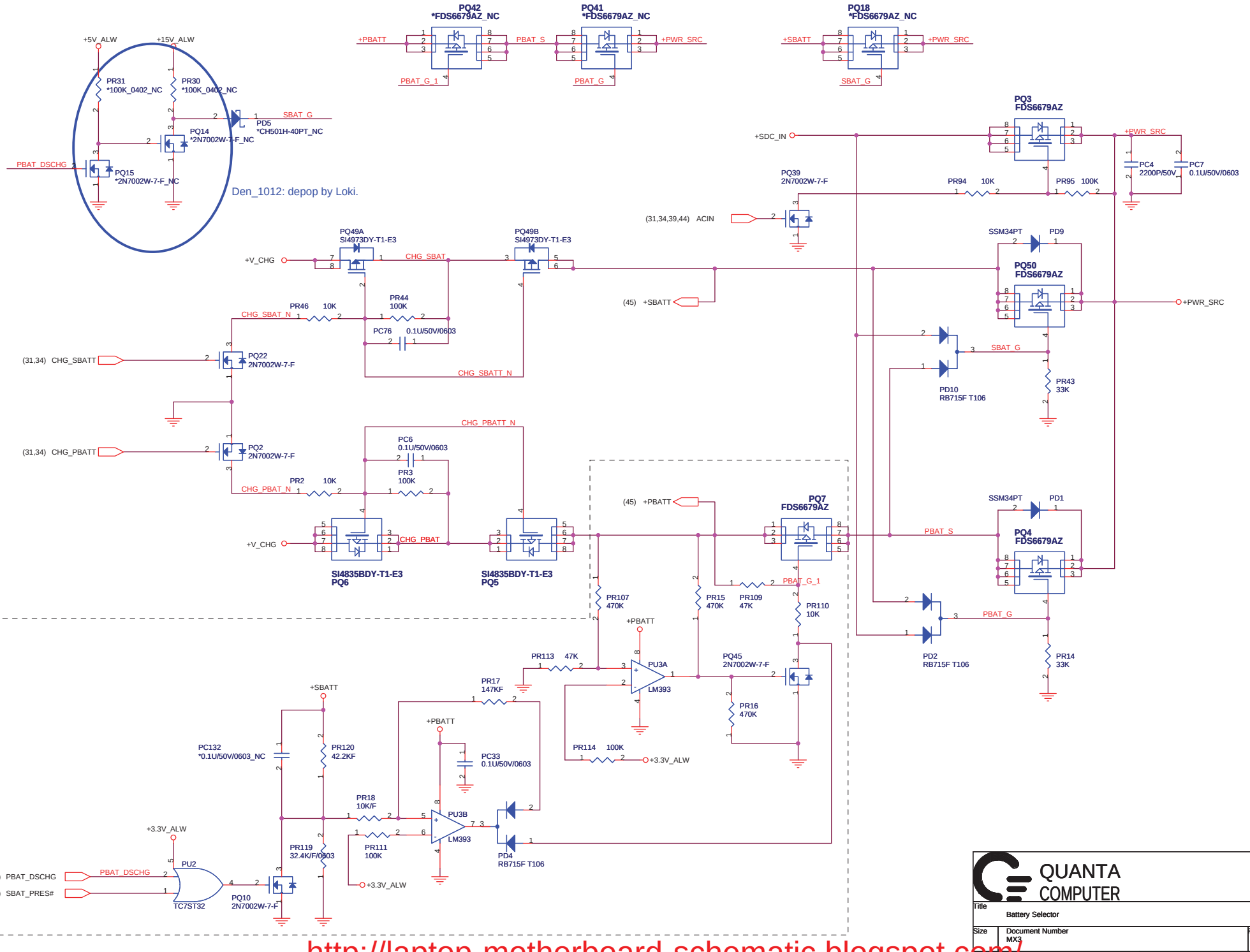
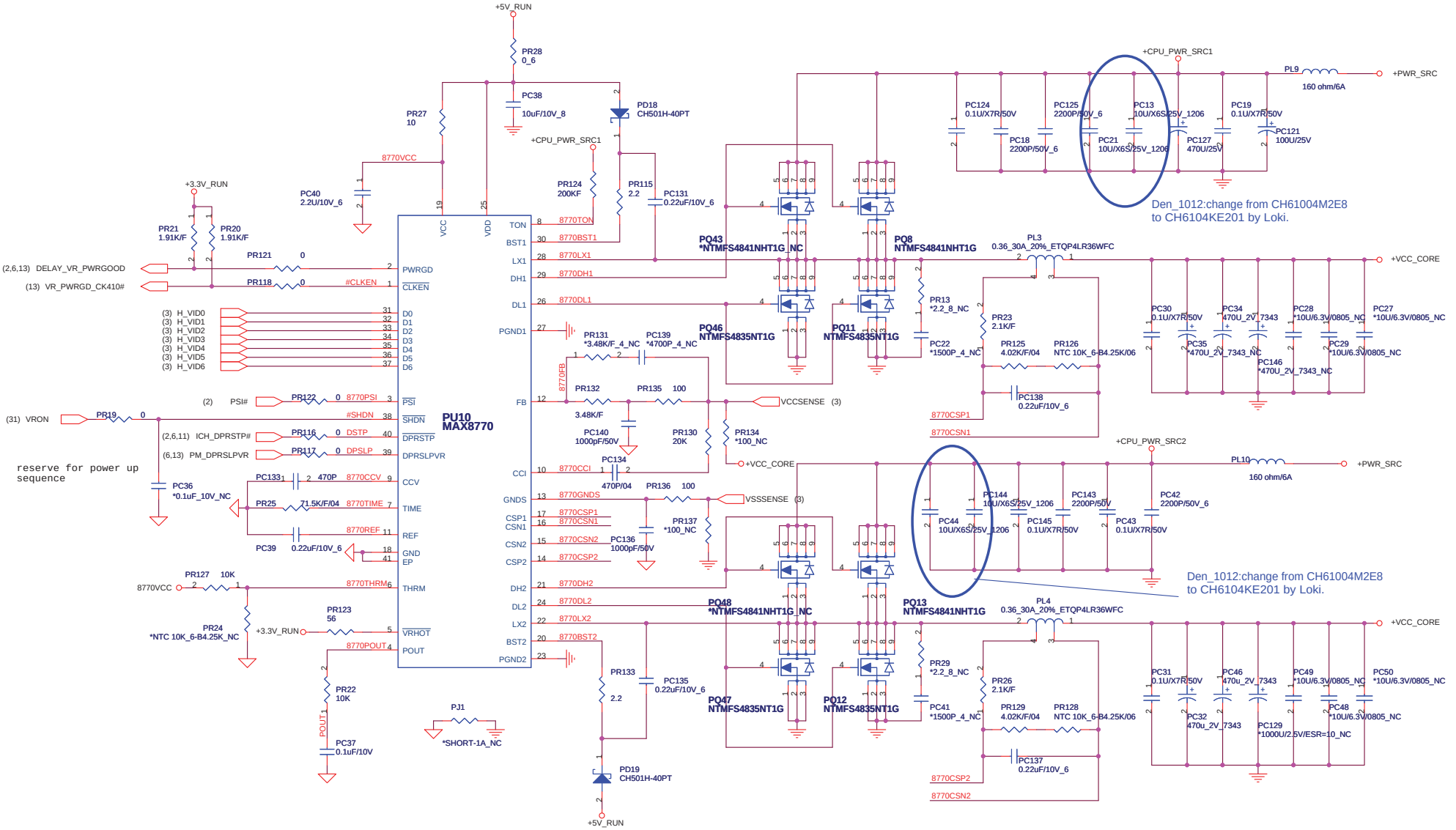


QUANTA COMPUTER		
Title	Battery Selector	
Size	Document Number MX3	Rev 3A
Date: Friday, October 12, 2007	Sheet 40 of 53	



QUANTA COMPUTER

Title	CPU Core_2 phase(MAX8770)	
Size	Document Number MX3	Rev 3A
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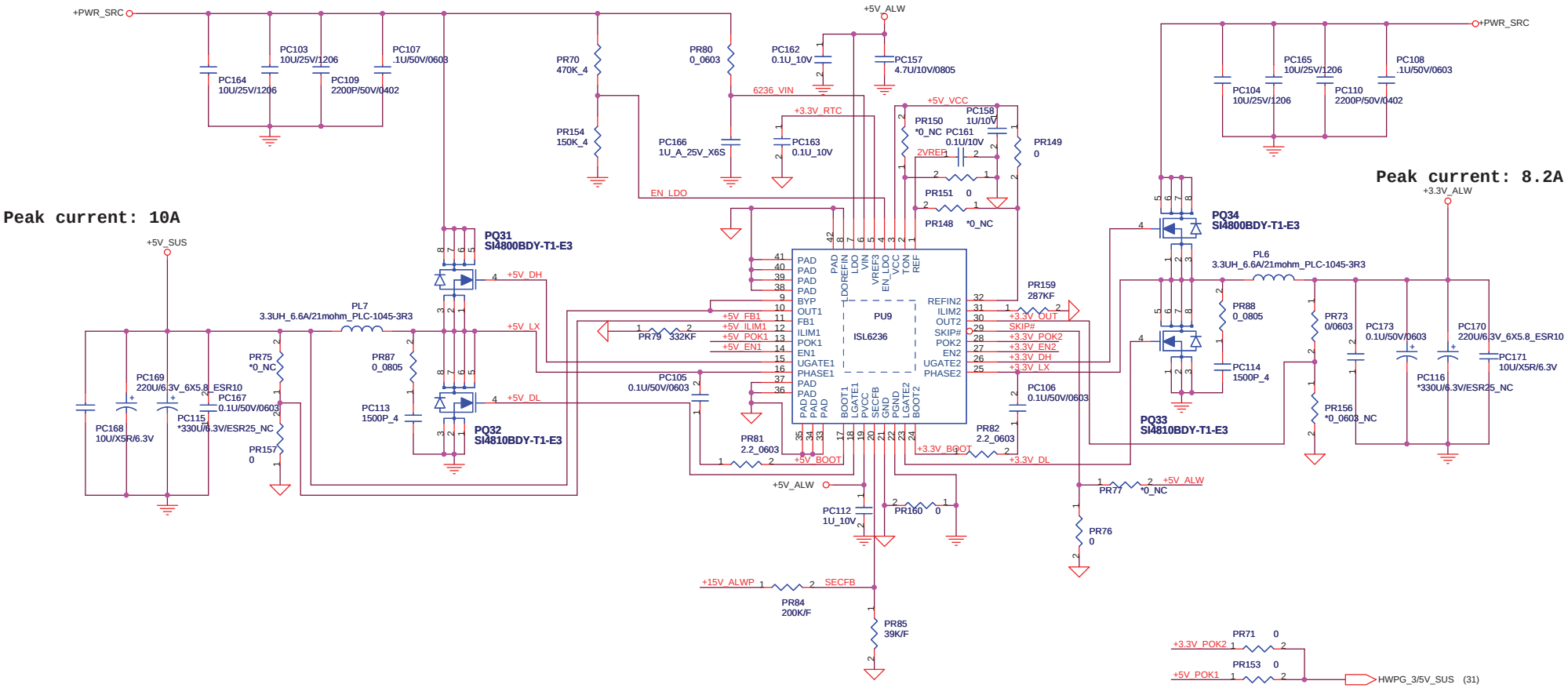

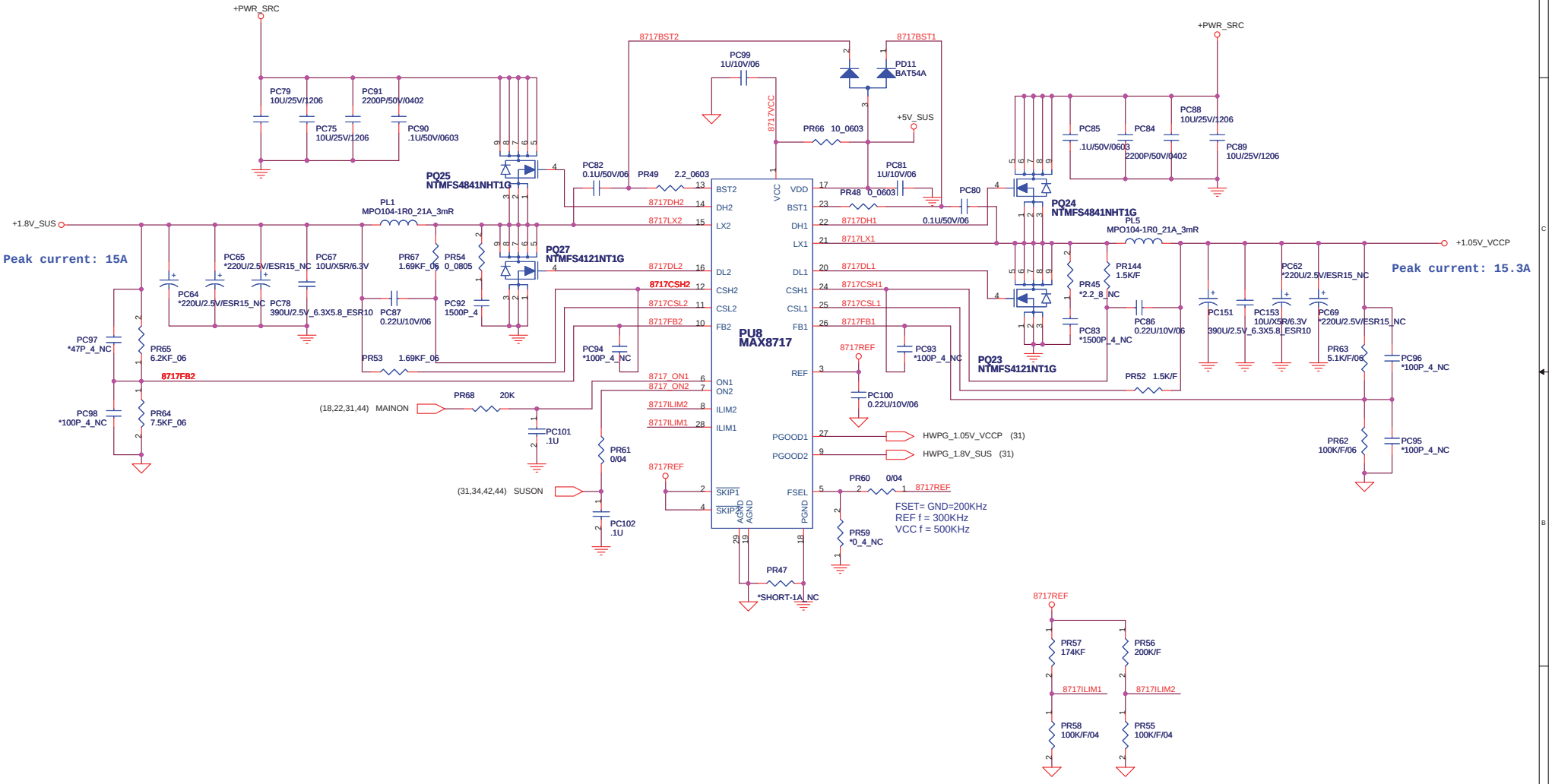

QUANTA COMPUTER

Title	1.8V/1.05V(MAX8717)
Size	Document Number: MX3
Rev	2C
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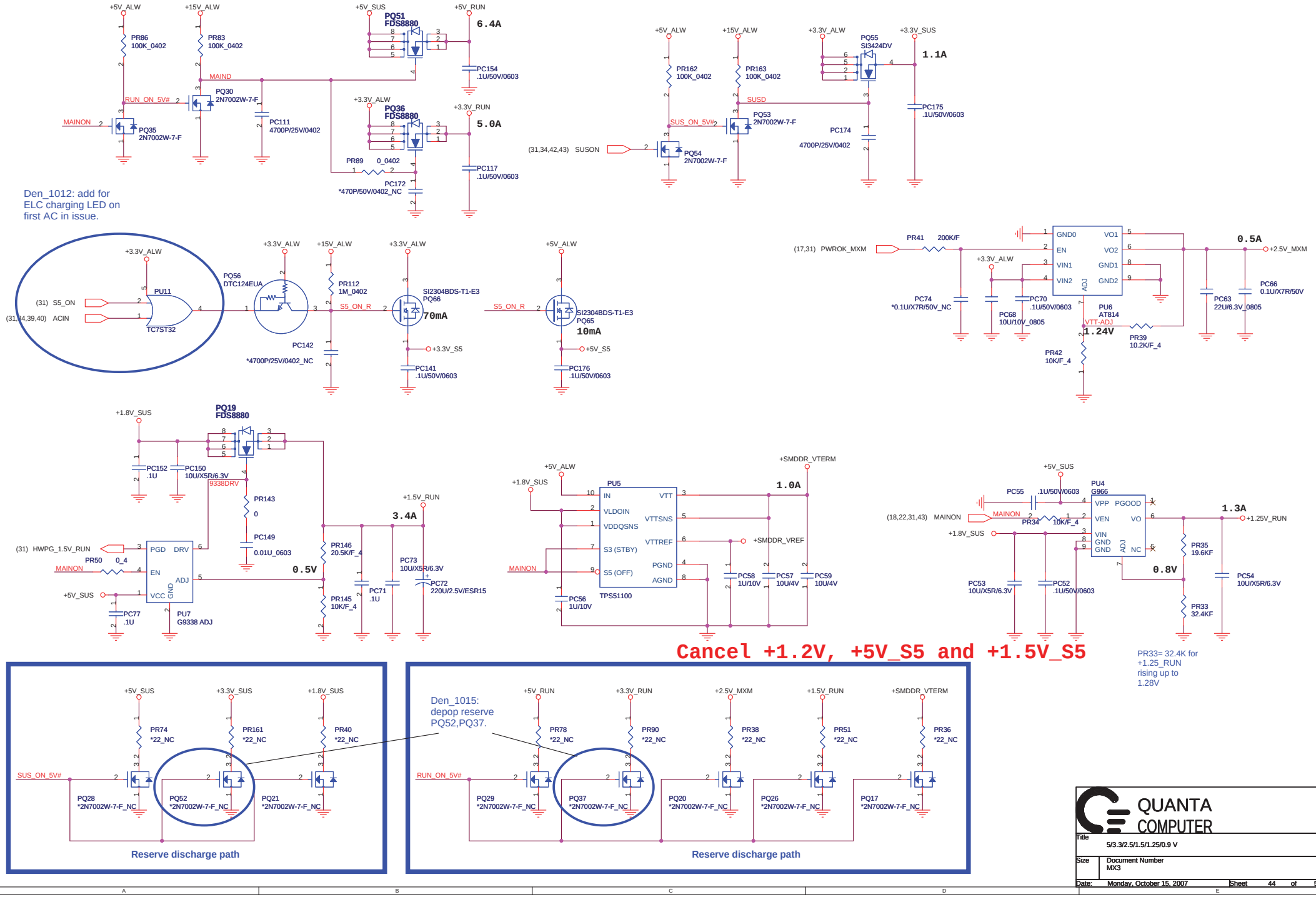

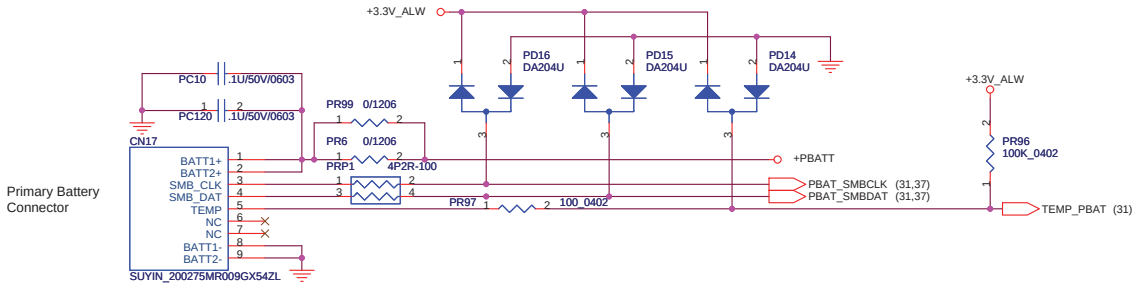

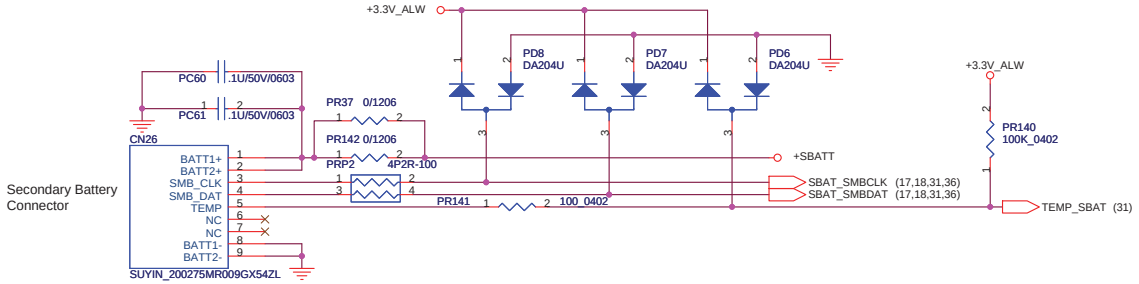

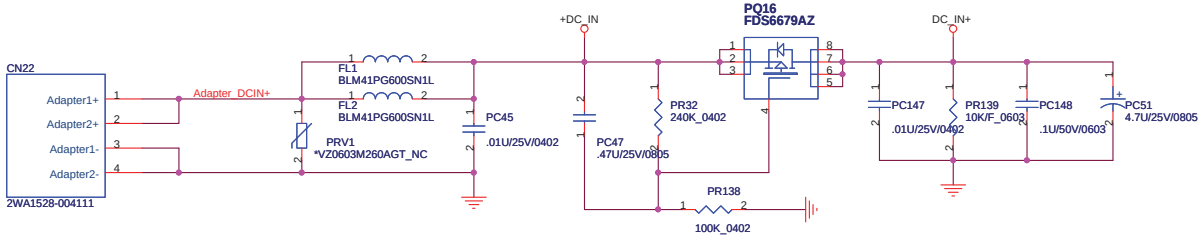

QUANTA COMPUTER		
Title: DCIN & Battery		
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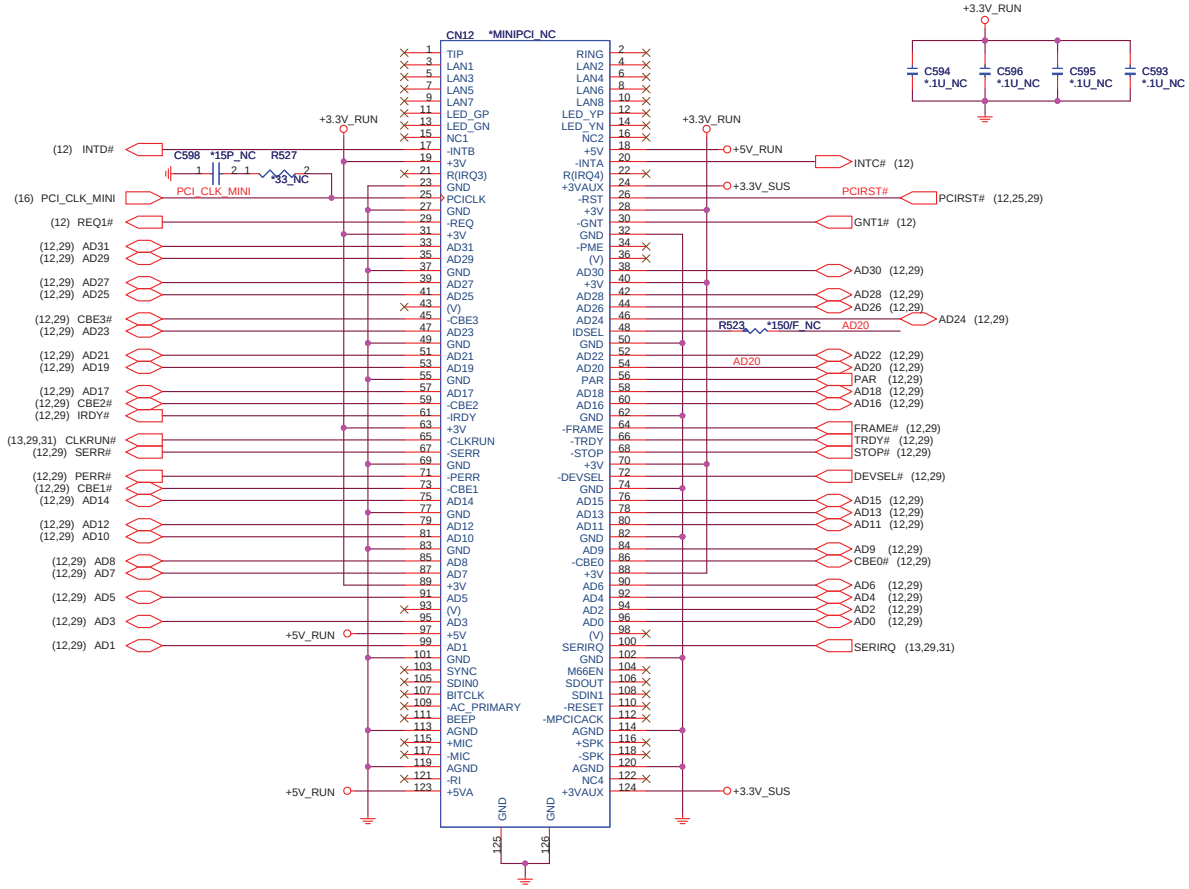
ID Select : AD20
Interrupt Pin : INTC#, INTD#
Request Indicate : REQ1#
Grant Indicate : GNT1#

DEBUG PURPOSE ONLY



QUANTA COMPUTER

Title	Mini PCI(for debug)	
Size	Document Number MX3	Rev 1A
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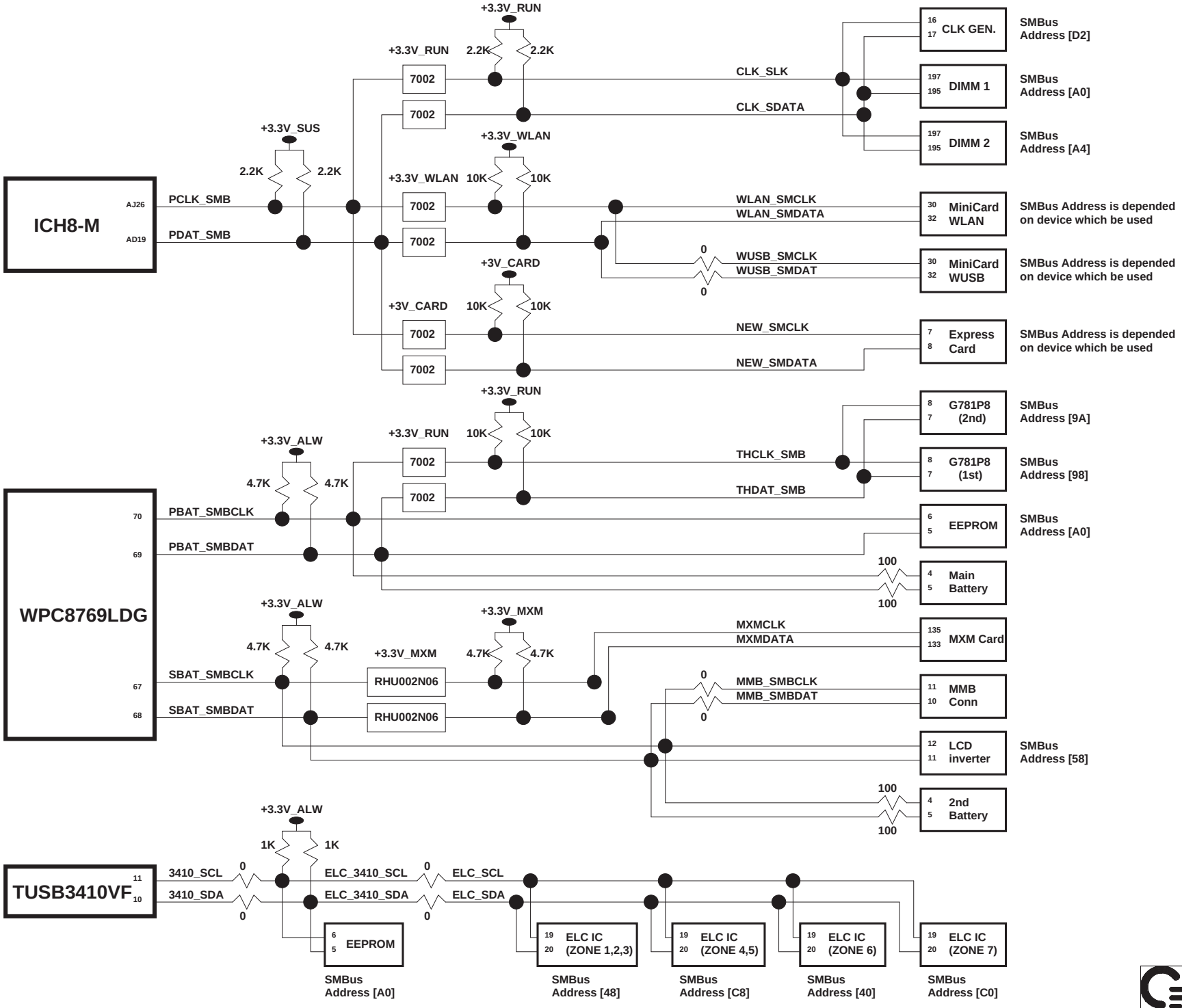

QUANTA COMPUTER

Title	SMBus Block	
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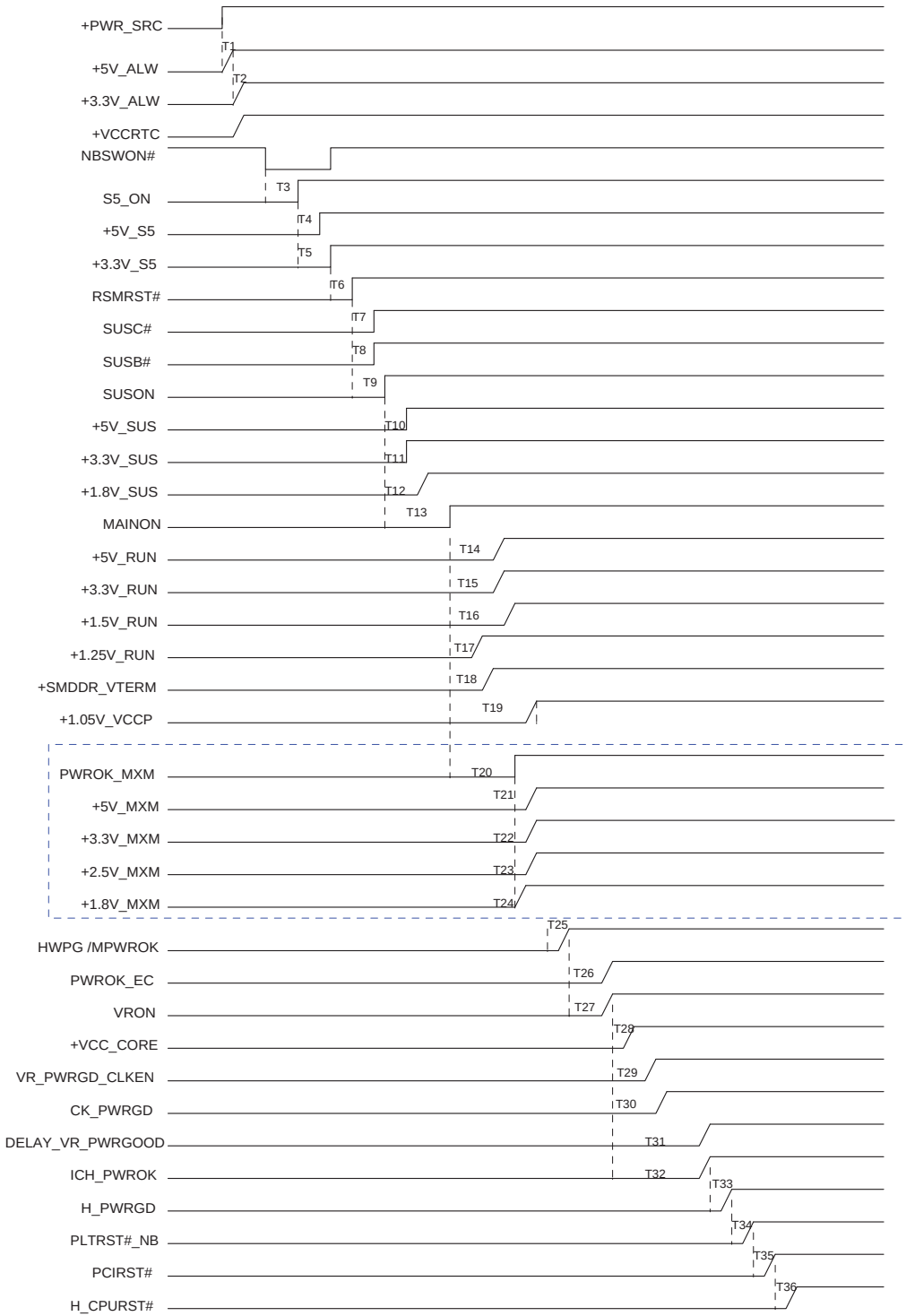
MX3 Power On Timing



ITEM	Measure Point			Time
T1	+PWR_SRC	To	+5V_ALW	
T2	+5V_ALW	To	+3.3V_ALW	
T3	NBSWON#	To	S5_ON	
T4	S5_ON	To	+5V_S5	
T5	S5_ON	To	+3.3V_S5	
T6	+3.3V_S5	To	RSMRST#	
T7	RSMRST#	To	SUSC#	
T8	RSMRST#	To	SUSB#	
T9	RSMRST#	To	SUSON	
T10	SUSON	To	+5V_SUS	
T11	SUSON	To	+3.3V_SUS	
T12	SUSON	To	+1.8V_SUS	
T13	SUSON	To	MAINON	
T14	MAINON	To	+5V_RUN	
T15	MAINON	To	+3.3V_RUN	
T16	MAINON	To	+1.5V_RUN	
T17	MAINON	To	+1.25V_RUN	
T18	MAINON	To	+SMDDR_VTERM	
T19	MAINON	To	+1.05V_VCCP	
T20	MAINON	To	PWROK_MXM	
T21	PWROK_MXM	To	+5V_MXM	
T22	PWROK_MXM	To	+3.3V_MXM	
T23	PWROK_MXM	To	+2.5V_MXM	
T24	PWROK_MXM	To	+1.8V_MXM	
T25	+1.05V_VCCP	To	HWPG /MPWROK	
T26	HWPG /MPWROK	To	PWROK_EC	
T27	HWPG /MPWROK	To	VRON	
T28	VRON	To	+VCC_CORE	
T29	VRON	To	VR_PWRGD_CLKEN	
T30	VRON	To	CK_PWRGD	
T31	VRON	To	DELAY_VR_PWRGOOD	
T32	VRON	To	ICH_PWROK	
T33	ICH_PWROK	To	H_PWRGD	
T34	H_PWRGD	To	PLTRST#_NB	
T35	PLTRST#_NB	To	PCIRST#	
T36	PCIRST#	To	H_CPURST#	

QUANTA COMPUTER

Title	Power On Sequence	
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