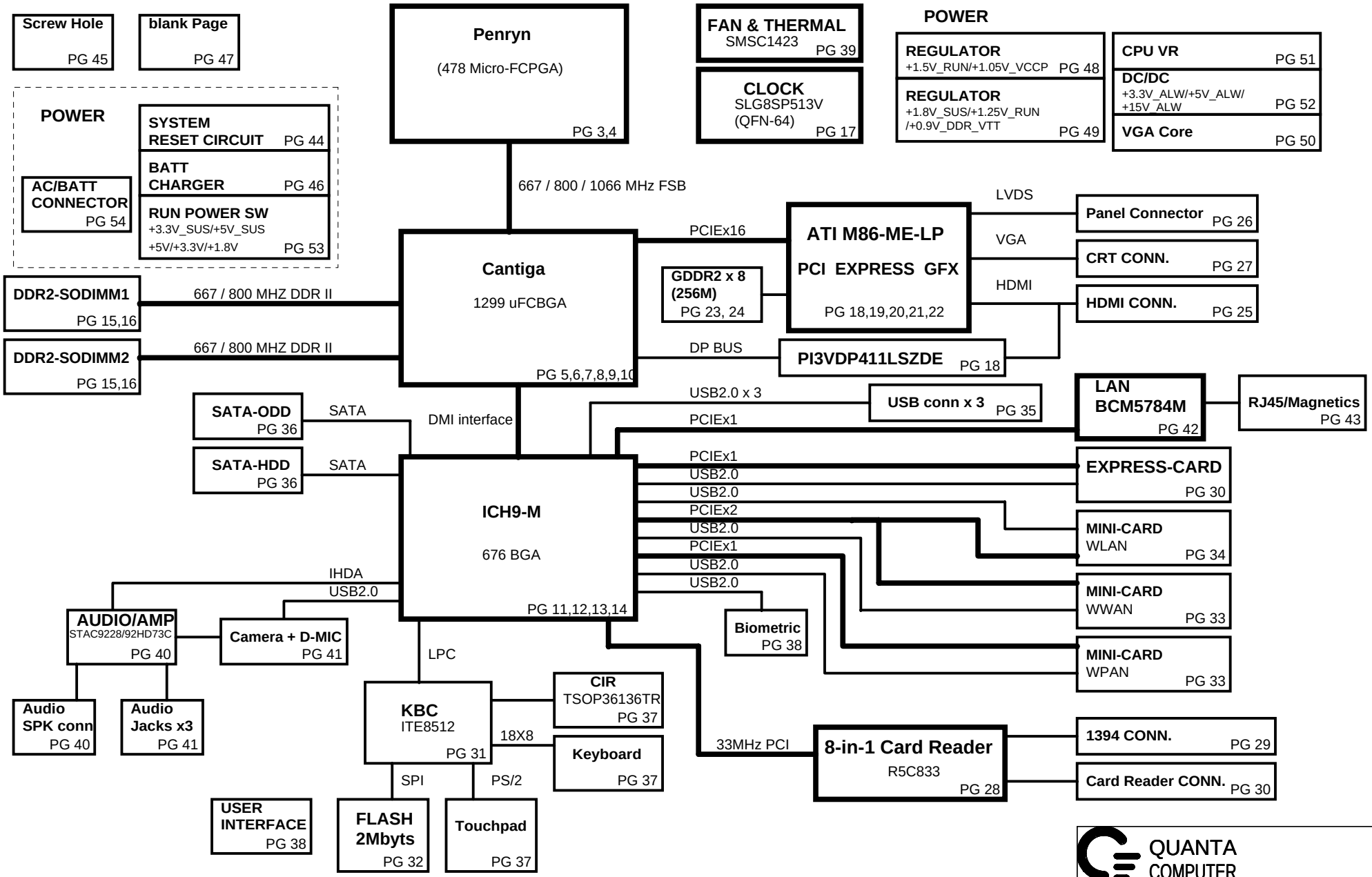
GM5(B) Pacino Intel Discrete & UMA Block Diagram

VER : B2A



QUANTA COMPUTER

Title	Schematic Block Diagram1	
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Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	4,26,32,34,48,49,50,51,52,55	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	11,14,31,32	RTC		S0~S5
+3.3V_ALW	+3.3V	3,13,26,31,32,34,36,37,38,44,46,49,52,53,54	8051 POWER	ALWON	S0~S5
+5V_ALW	+5V	35,36,46,48,49,52,53,54	LCD/CHARGE POWER	ALWON	S0~S5
+15V_ALW	+15V	26,36,37,52,53	LARGE POWER	+5V_ALW	S0~S5
+3.3V_LAN	+3.3V	42,43	LAN POWER	AUX_ON	
+5V_SUS	+5V	14,38,50,51,53	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	3,11,12,13,14,20,30,37,38,43,48,49,50,51,53	SLP_S5# CTRLD POWER	3.3V_SUS_ON	
+1.8V_SUS	+1.8V	6,8,9,15,48,49,50,53,55	SODIMM POWER	DDR_ON	
+0.9V_DDR_VTT	+0.9V	16,49,53	SODIMM POWER	0.9V_DDR_VTT_ON	
+5V_RUN	+5V	14,20,25,27,36,37,38,39,40,41,53	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	6,8,9,11,12,13,14,15,17,19,20,22,25,26,27,28, 30,33,34,36,38,39,40,41,42,53,55	SLP_S3# CTRLD POWER	3.3V_RUN_ON	
+1.8V_RUN	+1.8V	19,20,21,22,23,24,25,38,53	SDVO POWER	RUN_ON	
+1.5V_RUN	+1.5V	4,9,14,30,33,34,48,,53,55	CANTIGA/ICH8 POWER	1.5V_RUN_ON	
+1.05V_VCCP	+1.05V	3,4,5,6,8,9,11,14,37,48,55	CPU/CANTIGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.5V	4,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN#	
+5V_HDD	+5V	36	HDD Power	HDDC_EN#	
+5V_ALW2	+5V	37,38.52,53	LED power source	LDO output	

GND PLANE	PAGE	DESCRIPTION
8731AGND	46	
AGND_0.9V	49	
AGND_DC/DC	52	
AGND_DC2	48	
AGND_DDR	49	
AGND_ISL6260	51	
GND	ALL	

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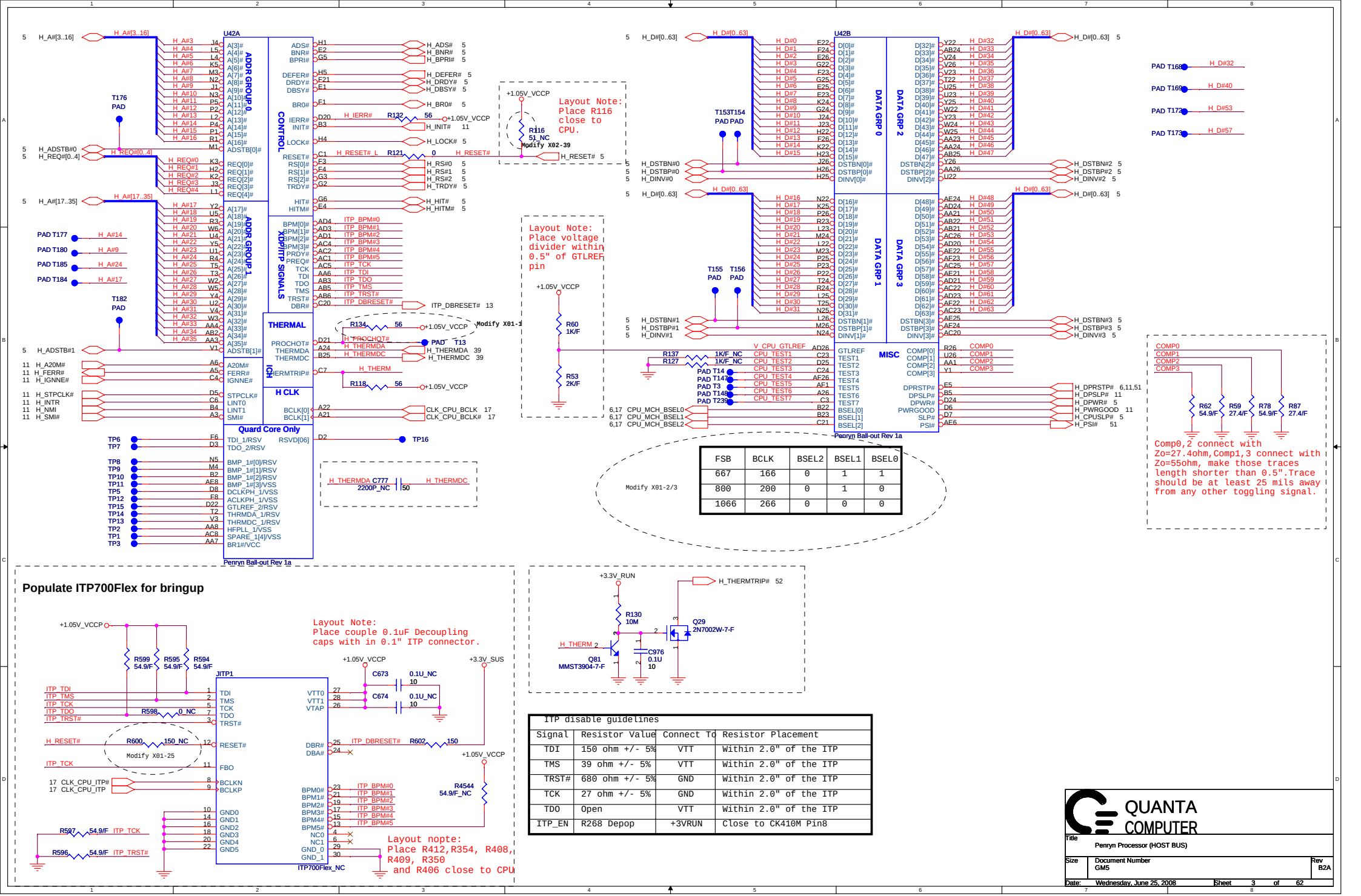

FSB	BCLK	BSEL2	BSEL1	BSEL0
667	166	0	1	1
800	200	0	1	0
1066	266	0	0	0

ITP disable guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm +/- 5%	VTT	Within 2.0" of the ITP
TMS	39 ohm +/- 5%	VTT	Within 2.0" of the ITP
TRST#	680 ohm +/- 5%	GND	Within 2.0" of the ITP
TCK	27 ohm +/- 5%	GND	Within 2.0" of the ITP
TDO	Open	VTT	Within 2.0" of the ITP
ITP_EN	R268 Depop	+3VRUN	Close to CK410M Pin8

QUANTA COMPUTER

Title	Penryn Processor (HOST BUS)	
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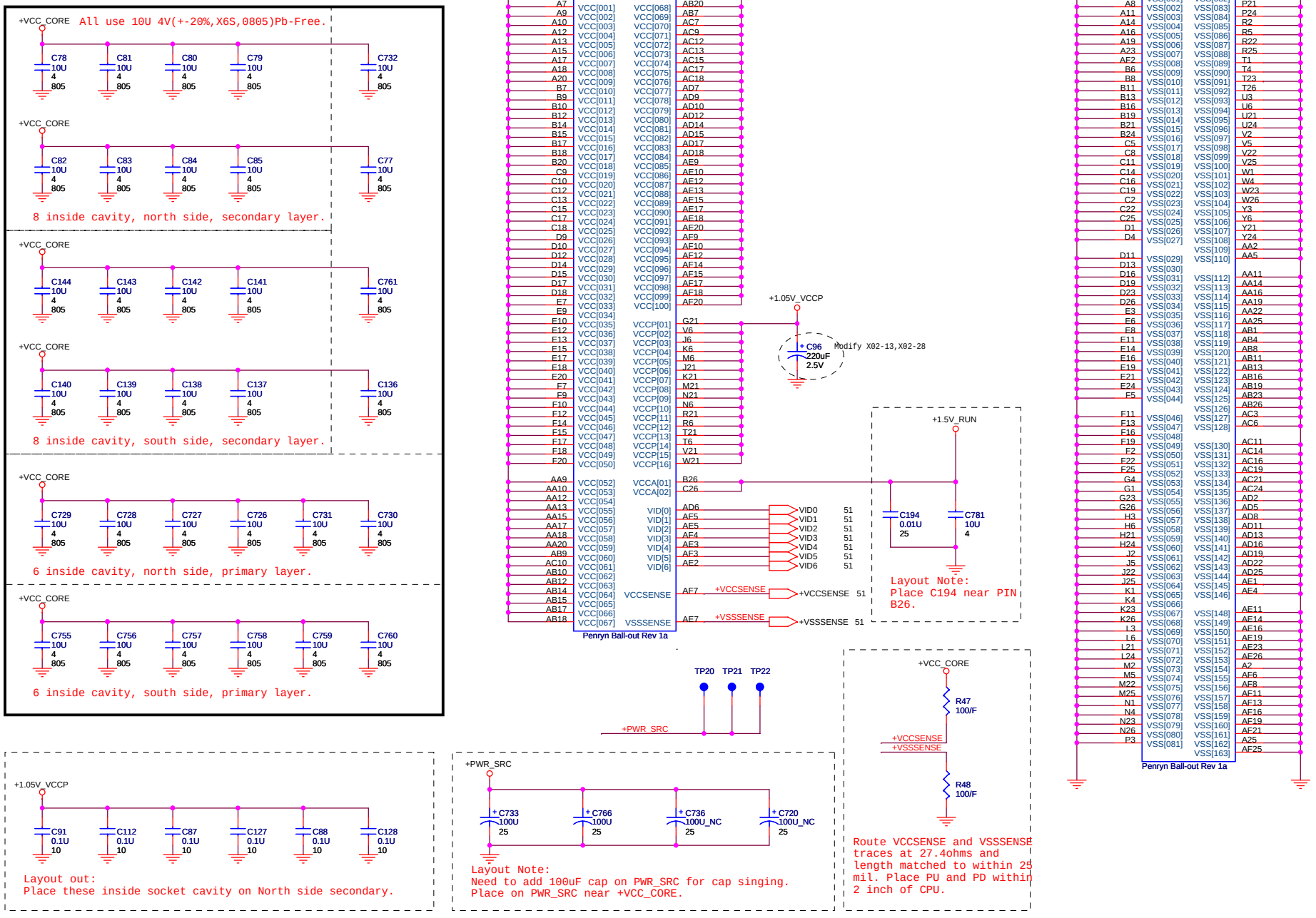

Title	Penryn Processor (HOST BUS)
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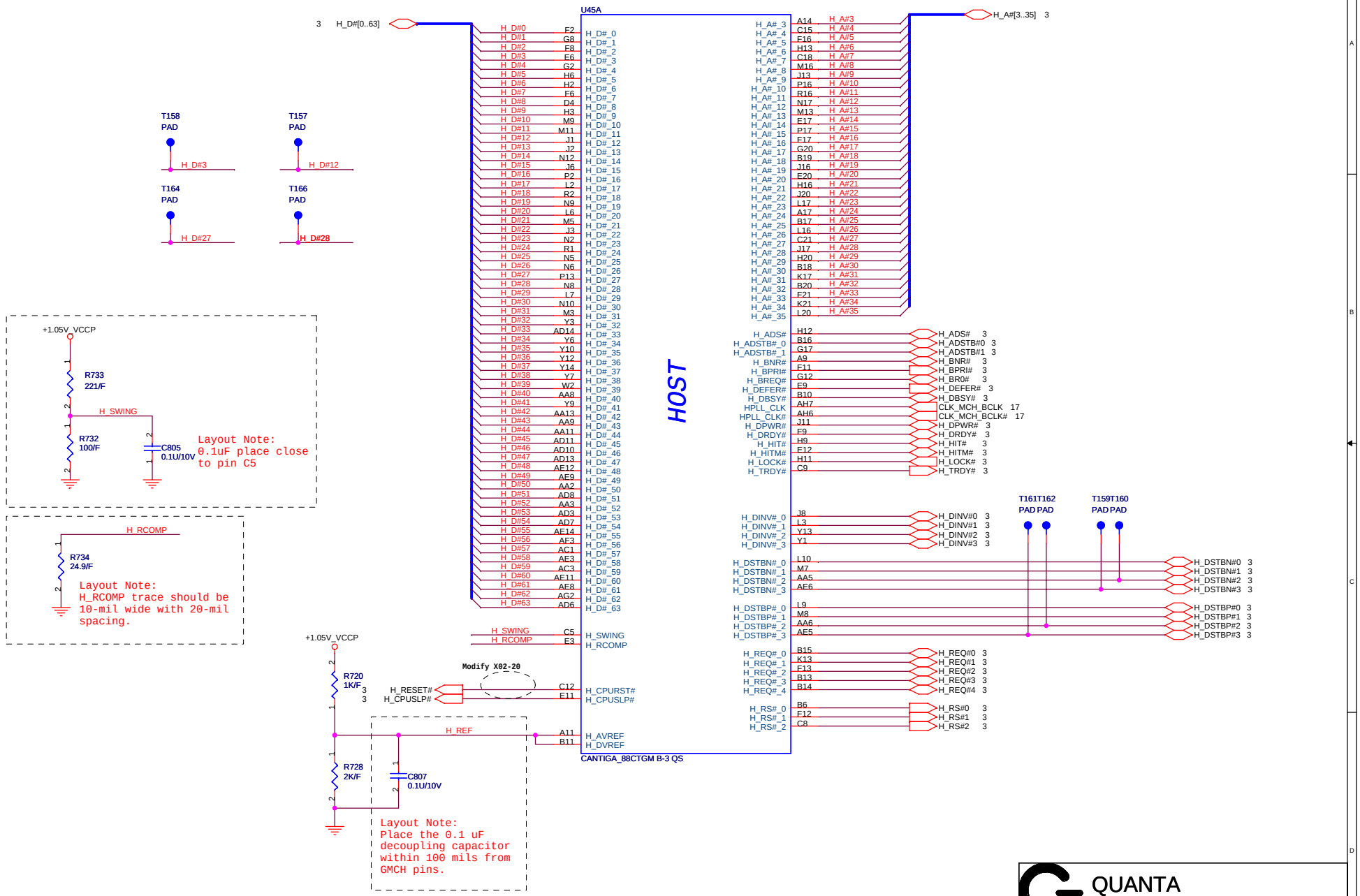
U45A
HOST
CANTIGA_88CTGM B-3 QS
3 H_D#[0..63]
H_A#[3..35] 3
T158 PAD
T157 PAD
T164 PAD
T166 PAD
H_D#3
H_D#12
H_D#27
H_D#28
+1.05V_VCCP
R733 221/F
R732 100/F
C805 0.1U/10V
H_SWING
Layout Note: 0.1uF place close to pin C5
H_RCOMP
R734 24.9/F
Layout Note: H_RCOMP trace should be 10-mil wide with 20-mil spacing.
Modify X02-20
R720 1K/F
R728 2K/F
C807 0.1U/10V
H_REF
Layout Note: Place the 0.1 uF decoupling capacitor within 100 mils from GMCH pins.
T161T162 PAD PAD
T159T160 PAD PAD
QUANTA COMPUTER
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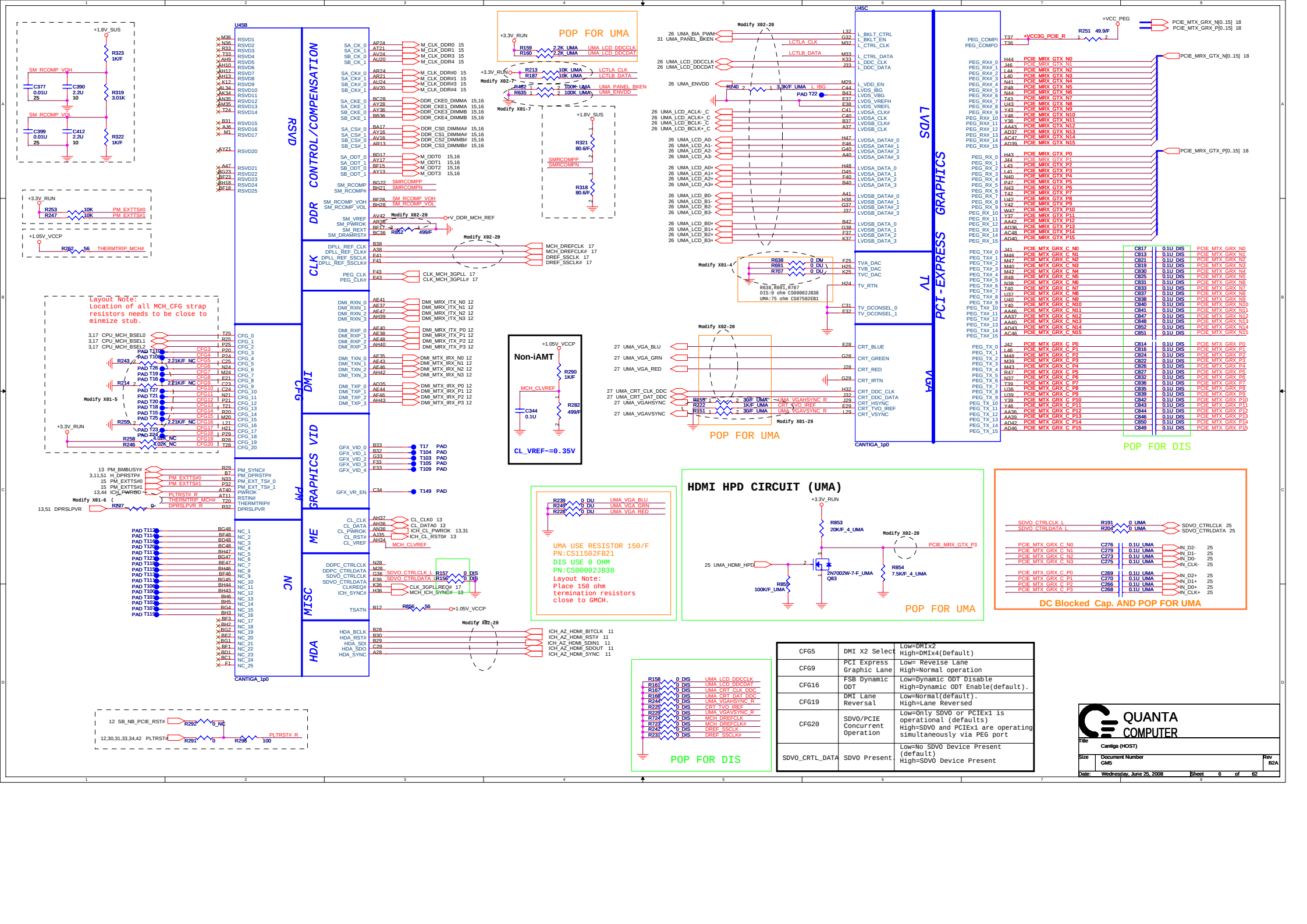

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	SDVO/PCIE Concurrent Operation	Low=Only SDVO or PCIEx1 is operational (defaults) High=SDVO and PCIEx1 are operating simultaneously via PEG port
SDVO_CRTL_DATA	SDVO Present	Low=No SDVO Device Present (default) High=SDVO Device Present

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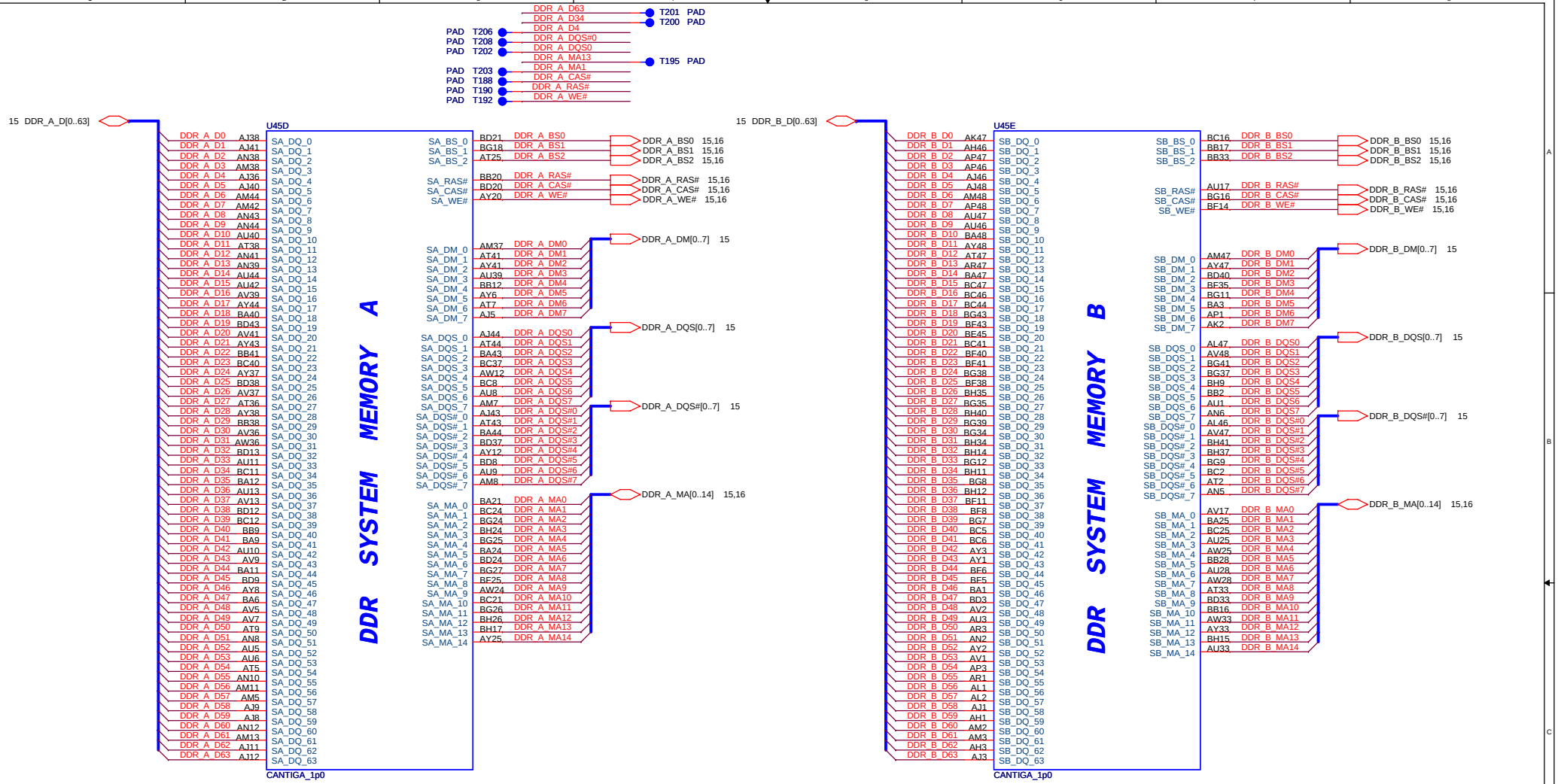

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2-22 JM

Added for SI recommend.

U45G

+1.8V_SUS

C994 0.1U/10V

C995 0.1U/10V

C996 0.1U/10V

2600mA

VCC SM POWER

VCC_SM_1 … VCC_SM_42/NC

VCC GFX NCTF

VCC_AXG_NCTF_1 … VCC_AXG_NCTF_60

W28 V28 W26 V26 W25 V25 W24 V24 V23 AM21 AL21 AK21 W21 V21 U21 AM20 AK20 W20 U20 AM19 AL19 AK19 AJ19 AH19 AG19 AF19 AE19 AB19 AA19 Y19 W19 V19 U19 AM17 AK17 AH17 AG17 AF17 AE17 AC17 AB17 Y17 W17 V17 AM16 AL16 AK16 AJ16 AH16 AG16 AF16 AE16 AC16 AB16 AA16 Y16 W16 V16 U16

+1.05V_VCCP

R117 0_0805_UMA

R256 0_0805_DIS

R66 0_0805_DIS

R113 0_0805_DIS

VCC_AXG_1 … VCC_AXG_42

VCC GFX

+1.05V_VCCP

R721 10_UMA/0_DIS

R726 10_UMA/0_DIS

AJ14 VCC_AXG_SENSE

AH14 VSS_AXG_SENSE

VCC SM LF

VCC_SM_LF1 … VCC_SM_LF7

AV44 AM40 AV21 AY5 AM10 BB13 VCCSM_LF1 … VCCSM_LF7

C355 0.1U/10V C362 0.1U/10V C371 0.22U/10V C367 0.22U/10V C372 0.47U/10V C365 1U/10V C363 1U/10V

CANTIGA_1p0

Ivcc_axg=6326.84mA

VCC_AXG_NCTF

C297 0.1U_UMA C308 0.1U_UMA C857 22U_UMA 805 4 C291 10U_UMA 805 6.3 C330 1U_UMA 603 10 C314 0.47U_UMA 603 10

+3.3V_RUN

R170 10

+VCC_GMCH_L

D6 SDMK0340L-7-F

Layout Note:
Inside GMCH cavity.
Ivcc=1930.4+508.12=2438.52mA

+1.05V_VCCP

Modify X02-28

C988 220uF 2.5V

C307 22U/4V C294 0.22U/10V C300 0.22U/10V C333 0.1U/10V

Layout Note:
370 mils from edge.

R101 0_0805_UMA

R63 0_0805_UMA

+1.05V_VCCP

C986 330U_NC

C987 220uF_NC 2.5V

Modify X02-28

Layout Note:
370 mils from edge.

+1.8V_SUS

Modify X02-13, X02-28

C430 0.1U/10V

C438 220uF 2.5V

VCC_SM

C415 22U/4V C422 22U/4V

Layout Note:
Place C233 where LVDS and DDR2 taps.

Layout Note:
Place on the edge.

U45F

AG34 AC34 AB34 AA34 Y34 V34 U34 AM33 AK33 AJ33 AG33 AF33 AE33 AC33 AA33 Y33 W33 V33 U33 AH28 AF28 AC28 AA28 AJ26 AG26 AE26 AC26 AH25 AG25 AF25 AG24 AJ23 AH23 AF23 T32

VCC_1 … VCC_35

VCC CORE POWER

+1.05V_VCCP

VCC_NCTF_1 … VCC_NCTF_44

AM32 AL32 AK32 AJ32 AH32 AG32 AE32 AC32 AA32 Y32 W32 U32 AM30 AL30 AK30 AH30 AG30 AF30 AE30 AC30 AB30 AA30 Y30 W30 V30 U30 AL29 AK29 AJ29 AH29 AG29 AE29 AC29 AA29 Y29 W29 V29 AL28 AK28 AL26 AK26 AK25 AK24 AK23

VCC NCTF

UMA: Places R721, R726 to 10 ohm.
Dis: Please R721, R726 to 0 ohm.

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CANTIGA_1p0

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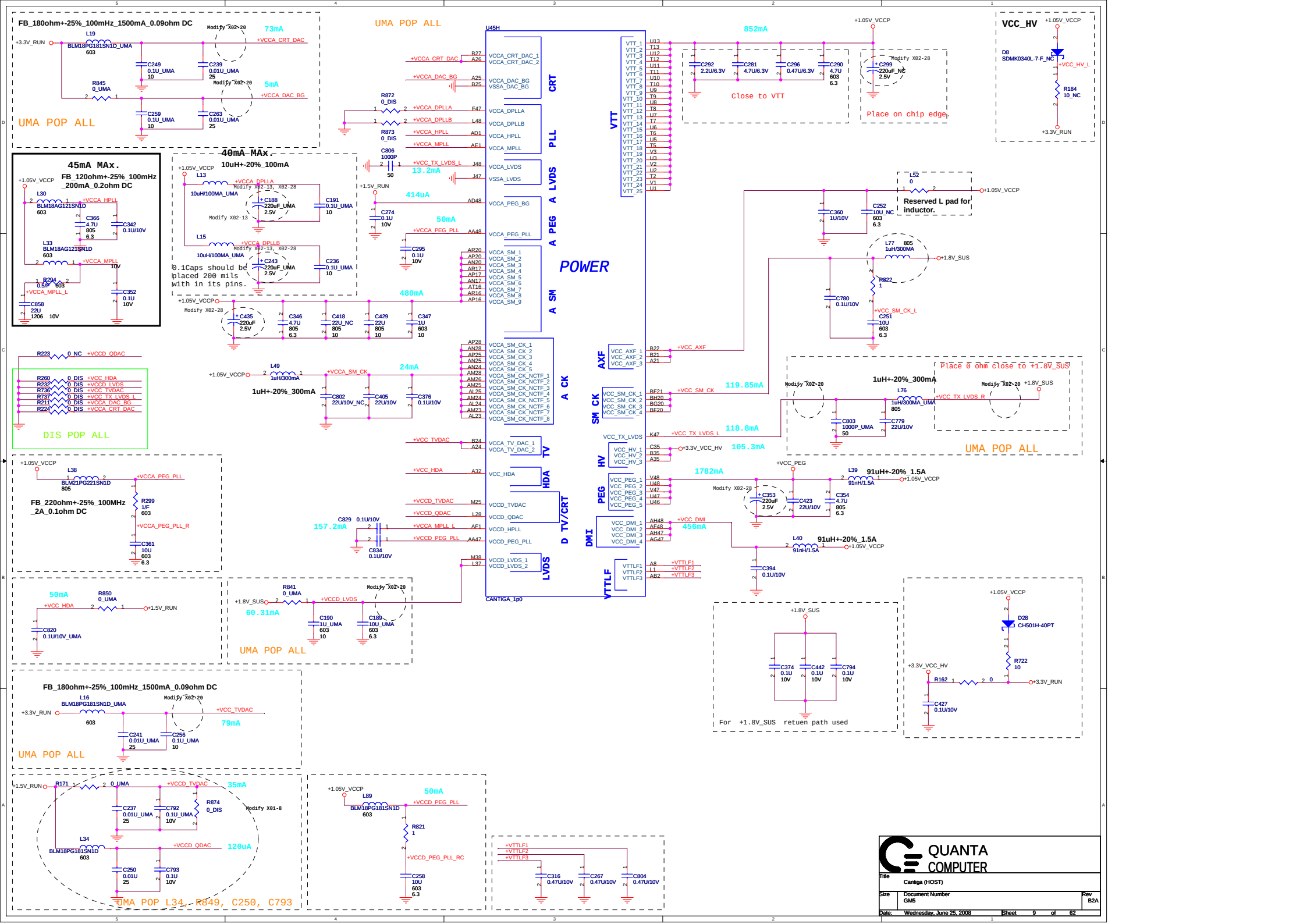
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
UMA POP ALL
45mA MAx.
FB_120ohm+-25%_100mHz_200mA_0.2ohm DC
40mA MAx.
10uH+-20%_100mA
0.1Caps should be placed 200 mils with in its pins.
DIS POP ALL
FB_220ohm+-25%_100MHz_2A_0.1ohm DC
1uH+-20%_300mA
FB_180ohm+-25%_100mHz_1500mA_0.09ohm DC
UMA POP L34, R849, C250, C793
U45H
CANTIGA_1p0
CRT
PLL
A LVDS
A PEG
POWER
A SM
A CK
TV
HDA
D TV/CRT
LVDS
VTT
AXF
SM CK
HV
PEG
DMI
VTTLF
852mA
Close to VTT
Place on chip edge.
VCC_HV
Reserved L pad for inductor.
Place 0 ohm close to +1.8V_SUS
119.85mA
118.8mA
105.3mA
1782mA
456mA
91uH+-20%_1.5A
For +1.8V_SUS retuen path used
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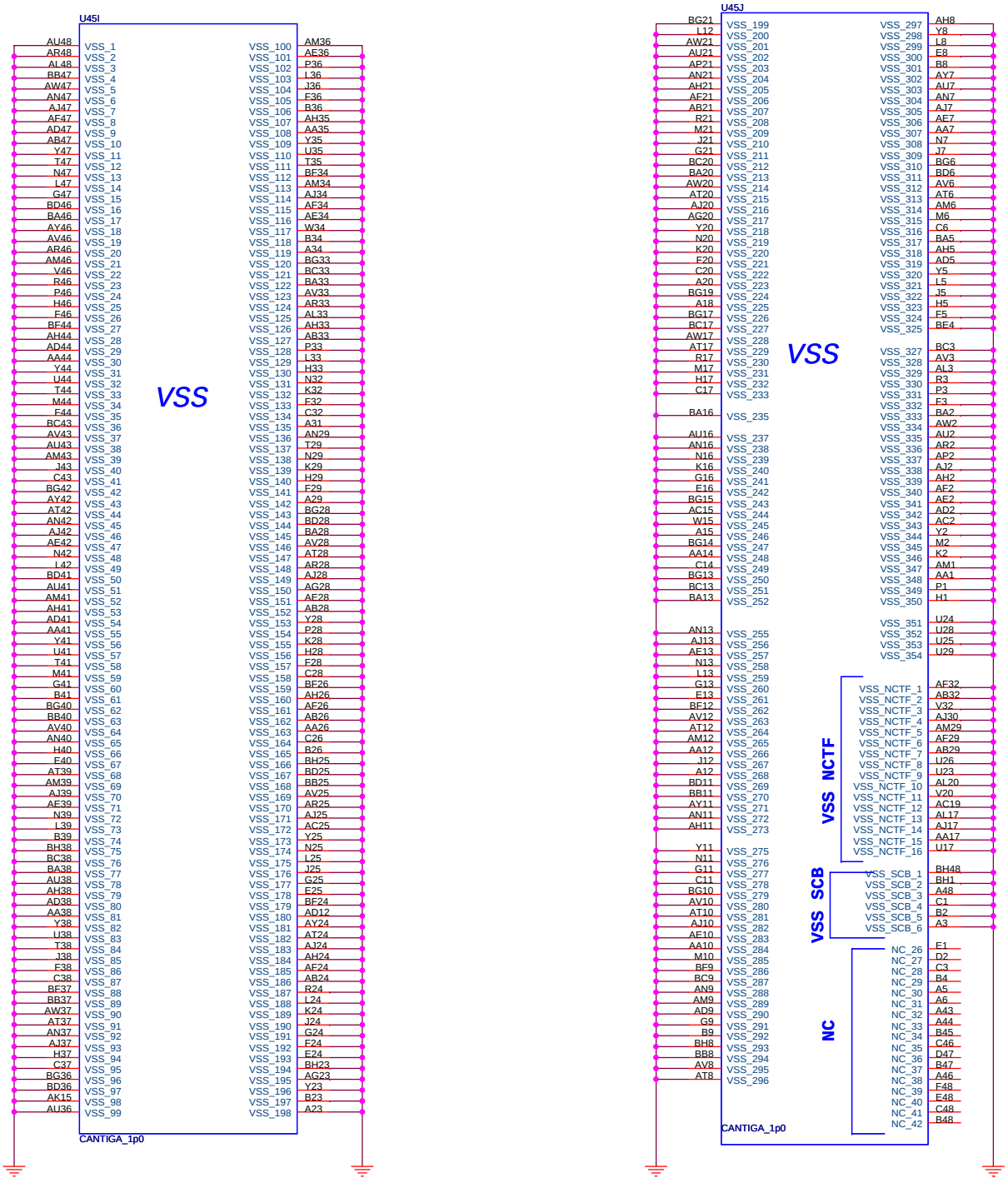

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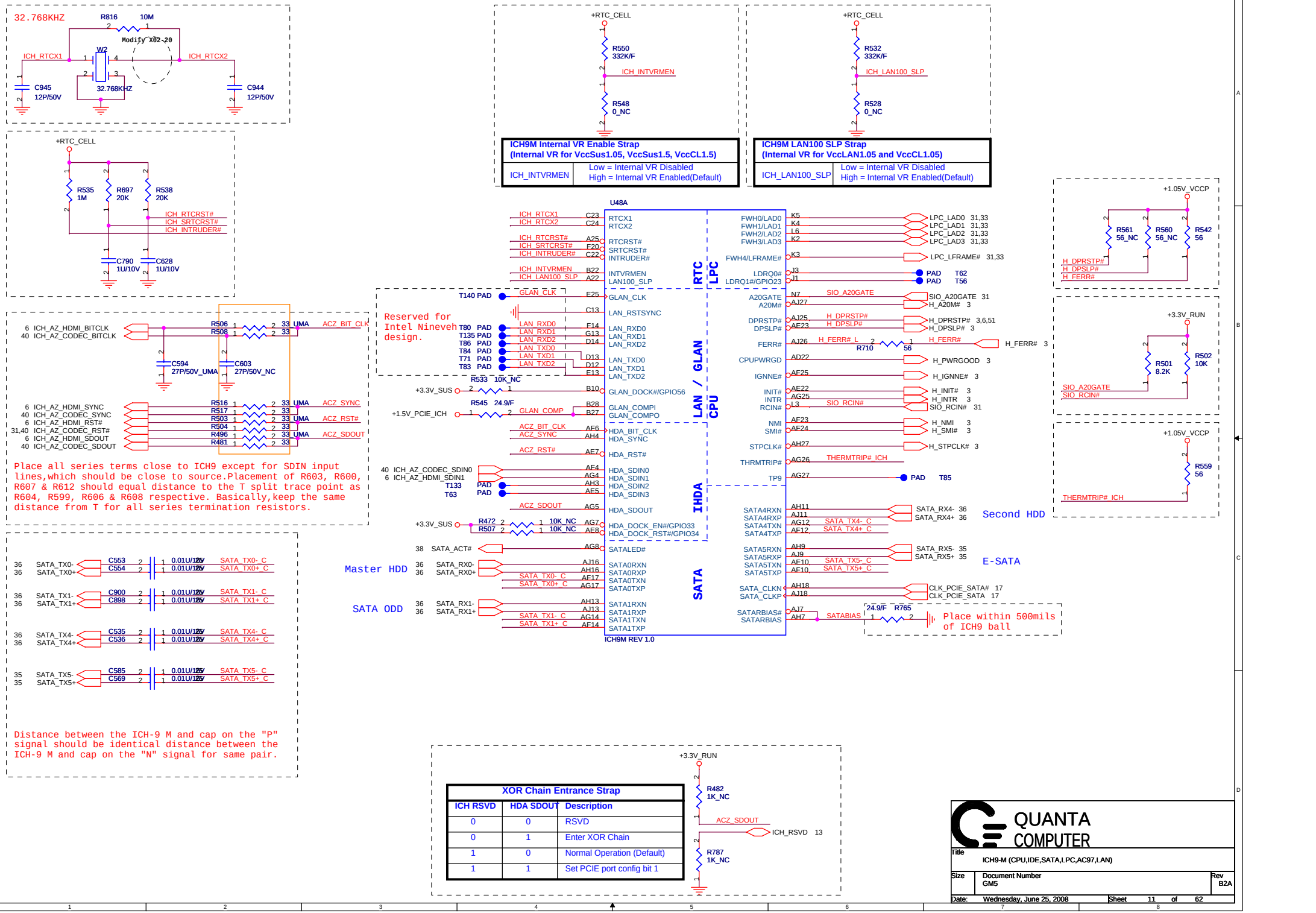
32.768KHZ
R816 10M
Modify X02-20
W2
ICH_RTCX1
ICH_RTCX2
C945 12P/50V
32.768KHZ
C944 12P/50V
+RTC_CELL
R535 1M
R697 20K
R538 20K
ICH_RTCRST#
ICH_SRTCRST#
ICH_INTRUDER#
C790 1U/10V
C628 1U/10V
+RTC_CELL
R550 332K/F
ICH_INTVRMEN
R548 0_NC
ICH9M Internal VR Enable Strap
(Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)
ICH_INTVRMEN
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
+RTC_CELL
R532 332K/F
ICH_LAN100_SLP
R528 0_NC
ICH9M LAN100 SLP Strap
(Internal VR for VccLAN1.05 and VccCL1.05)
ICH_LAN100_SLP
Low = Internal VR Disabled
High = Internal VR Enabled(Default)
U48A
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
LAN / GLAN
CPU
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
IHDA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP9
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
ICH9M REV 1.0
Reserved for Intel Nineveh design.
T140 PAD
T80 PAD
T135 PAD
T86 PAD
T84 PAD
T71 PAD
T83 PAD
R533 10K_NC
+3.3V_SUS
R545 24.9/F
+1.5V_PCIE_ICH
GLAN_COMP
R472 10K_NC
R507 10K_NC
+3.3V_SUS
T133 PAD
T63 PAD
38 SATA_ACT#
Master HDD
SATA ODD
36 SATA_RX0-
36 SATA_RX0+
36 SATA_RX1-
36 SATA_RX1+
SATA_TX0- C
SATA_TX0+ C
SATA_TX1- C
SATA_TX1+ C
LPC_LAD0 31,33
LPC_LAD1 31,33
LPC_LAD2 31,33
LPC_LAD3 31,33
LPC_LFRAME# 31,33
PAD T62
PAD T56
SIO_A20GATE
SIO_A20GATE 31
H_A20M# 3
H_DPRSTP# 3,6,51
H_DPSLP# 3
H_FERR# 3
R710 56
H_PWRGOOD 3
H_IGNNE# 3
H_INIT# 3
H_INTR 3
SIO_RCIN# 31
H_NMI 3
H_SMI# 3
H_STPCLK# 3
THERMTRIP#_ICH
PAD T85
Second HDD
SATA_RX4- 36
SATA_RX4+ 36
SATA_TX4- C
SATA_TX4+ C
E-SATA
SATA_RX5- 35
SATA_RX5+ 35
SATA_TX5- C
SATA_TX5+ C
CLK_PCIE_SATA# 17
CLK_PCIE_SATA 17
SATABIAS
24.9/F R765
Place within 500mils of ICH9 ball
+1.05V_VCCP
R561 56_NC
R560 56_NC
R542 56
H_DPRSTP#
H_DPSLP#
H_FERR#
+3.3V_RUN
R501 8.2K
R502 10K
SIO_A20GATE
SIO_RCIN#
+1.05V_VCCP
R559 56
THERMTRIP#_ICH
6 ICH_AZ_HDMI_BITCLK
40 ICH_AZ_CODEC_BITCLK
R506 33_UMA
R508 33
ACZ_BIT_CLK
C594 27P/50V_UMA
C603 27P/50V_NC
6 ICH_AZ_HDMI_SYNC
40 ICH_AZ_CODEC_SYNC
6 ICH_AZ_HDMI_RST#
31,40 ICH_AZ_CODEC_RST#
6 ICH_AZ_HDMI_SDOUT
40 ICH_AZ_CODEC_SDOUT
R516 33_UMA
R517 33
R503 33_UMA
R504 33
R496 33_UMA
R481 33
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
Place all series terms close to ICH9 except for SDIN input lines,which should be close to source.Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically,keep the same distance from T for all series termination resistors.
40 ICH_AZ_CODEC_SDIN0
6 ICH_AZ_HDMI_SDIN1
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDOUT
36 SATA_TX0-
36 SATA_TX0+
C553
C554
0.01U/25V
SATA_TX0- C
SATA_TX0+ C
36 SATA_TX1-
36 SATA_TX1+
C900
C898
SATA_TX1- C
SATA_TX1+ C
36 SATA_TX4-
36 SATA_TX4+
C535
C536
SATA_TX4- C
SATA_TX4+ C
35 SATA_TX5-
35 SATA_TX5+
C585
C569
SATA_TX5- C
SATA_TX5+ C
Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.
+3.3V_RUN
R482 1K_NC
ACZ_SDOUT
ICH_RSVD 13
R787 1K_NC
XOR Chain Entrance Strap
ICH RSVD
HDA SDOUT
Description
0 0 RSVD
0 1 Enter XOR Chain
1 0 Normal Operation (Default)
1 1 Set PCIE port config bit 1
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ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)
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Place TX DC blocking caps close ICH8.

33 PCIE_TX1-
33 PCIE_TX1+
C953 C955 0.1U
PCIE_TXN1_C
PCIE_TXP1_C

34 PCIE_TX2-
34 PCIE_TX2+
C951 C952 0.1U
PCIE_TXN2_C
PCIE_TXP2_C

33 PCIE_TX3-
33 PCIE_TX3+
C949 C950 0.1U
PCIE_TXN3_C
PCIE_TXP3_C

30 PCIE_TX4-
30 PCIE_TX4+
C948 C947 0.1U
PCIE_TXN4_C
PCIE_TXP4_C

42 PCIE_TX6-/GLAN_TX-
42 PCIE_TX6+/GLAN_TX+
C946 C954 0.1U
GLAN_TXN_C
GLAN_TXP_C

MiniWWAN
MiniWLAN
MiniWPAN
Express Card
Giga Bit LOM

PCI-Express
Direct Media Interface
SPI
USB

U48D
ICH9M REV 1.0

DMI_ZCOMP
DMI_IRCOMP
DMI_COMP
R529 24.9/F
+1.5V_PCIE_ICH
Place within 500mils

Side pair Top / left
Side pair bottom / left
Side pair top/right(DB)
Side pair Bot right(DB)
WLAN
Mini Card (WWAN)
Mini Card (WPAN)
Express Card
USB W/ E-SATA port
Biometric
Camera

ICH_SPI_CS1#_R
PCI_GNT0#
R451 1K_NC
R546 1K_NC

Boot BIOS Strap

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

Places within 500 mils of the ICH9
R763 22.6/F
USBRBIAS

PCI Pullups
RP42
RP40
+3.3V_RUN

SB_WPAN_PCIE_RST# R468 20K
SB_WWAN_PCIE_RST# R791 20K
SB_WLAN_PCIE_RST# R467 20K
SB_LOM_PCIE_RST# R477 20K
SB_NB_PCIE_RST# R495 20K
BIOS should not enable the internal GPIO pull up resistor.

WWAN Noise - ICH improvements
C918 C915 C916 C917 C922 C923 C924 C925 0.1U_NC

RP49 10KX8
+3.3V_SUS
R711 R712 10K

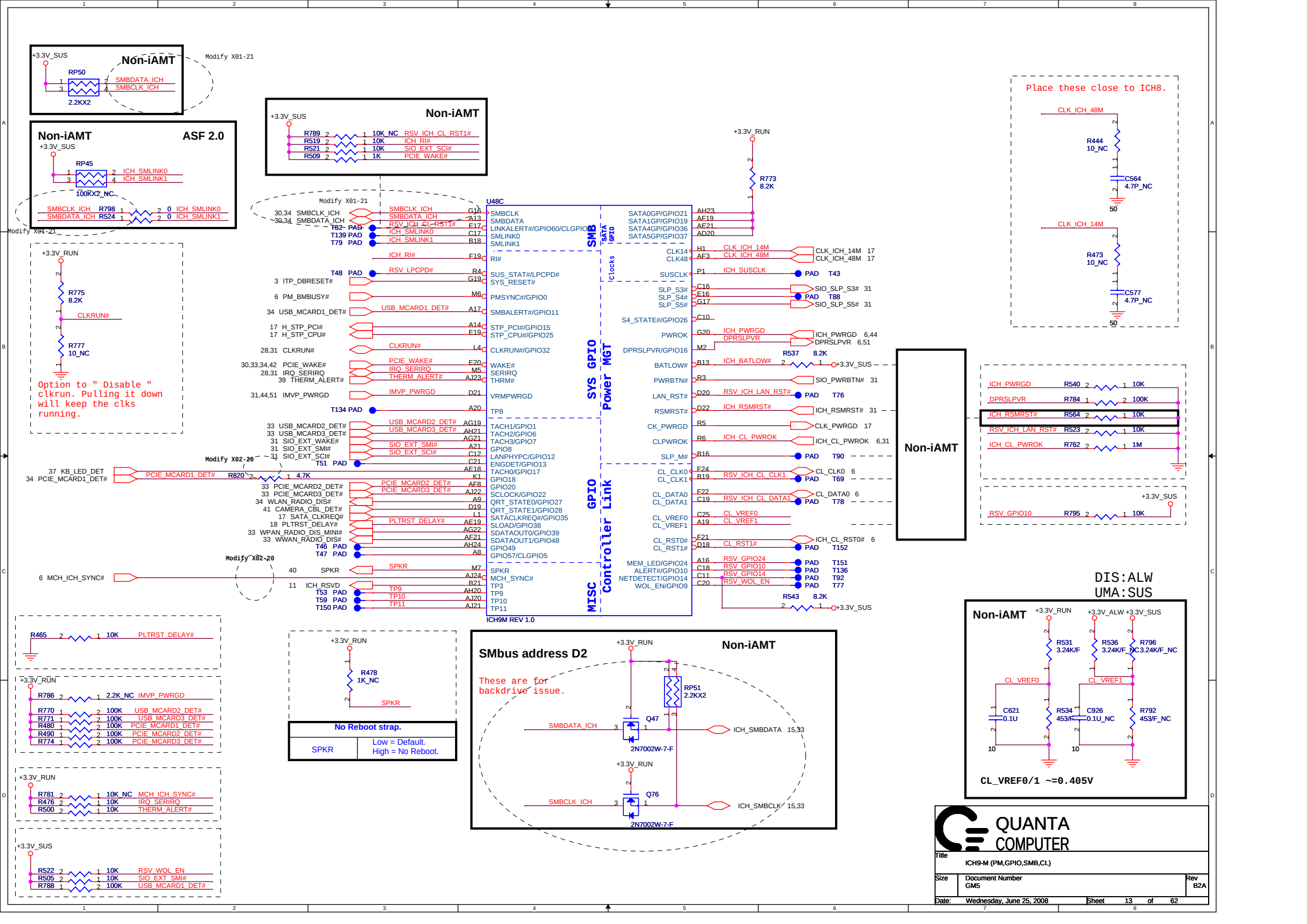
PCI_GNT3#
R474 1K_NC
A16 away override strap.
SB_NB_PCIE_RST# Low = A16 swap override enabled. High = Default.

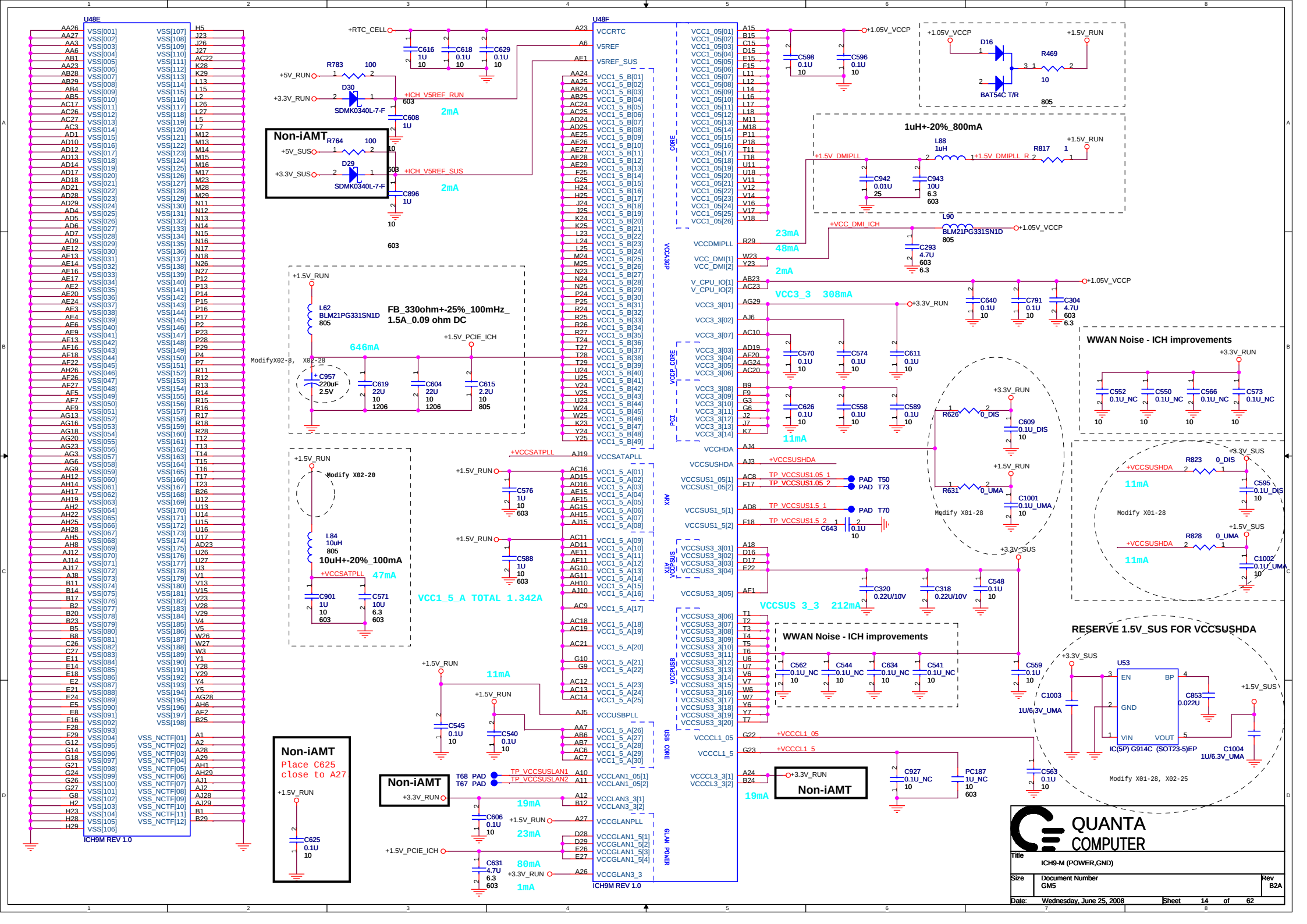
Non-iAMT
Add Buffers as needed for Loading and fanout concerns.
C887 0.047U
U47 TC7SZ32FU(T5L,F,T)
PCI_RST# G
PCI_RST# 28
C958 0.047U
U50 TC7SZ32FU(T5L,F,T)
PCI_PLTRST#
PLTRST# 6,30,31,33,34,42

CLK_PCI_ICH
R772 10_NC
C907 8.2P_NC
Reserved for EMI.Place resister and cap close to ICH.

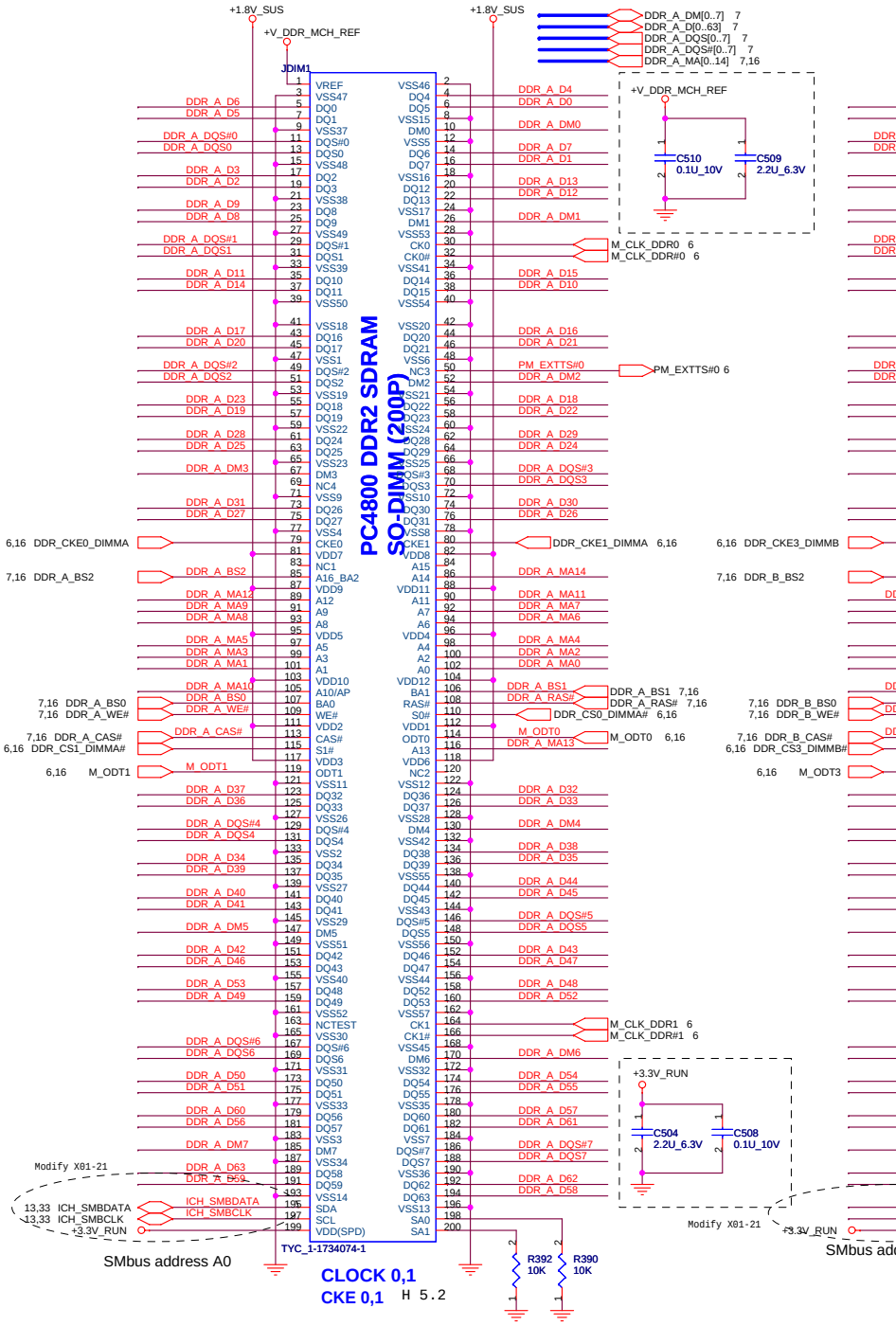
28 PCI_AD[0..31]
U48B
PCI
Interrupt I/F
ICH9M REV 1.0

PCI_PIRQA# PCI_PIRQB# PCI_PIRQC# PCI_PIRQD#
T55 PAD
T132 PAD

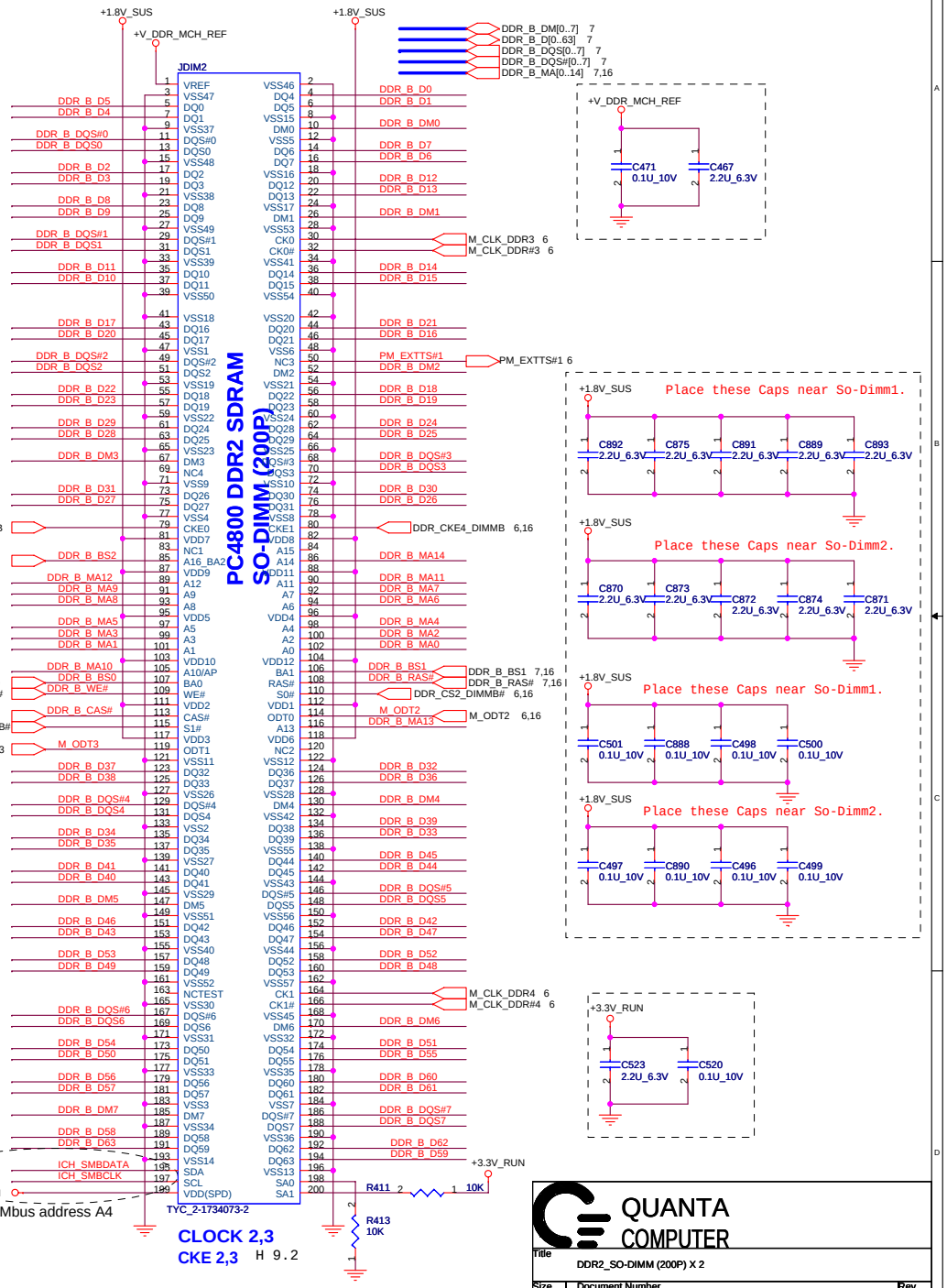

Non-iAMT
Modify X01-21
RP50
SMBDATA_ICH
SMBCLK_ICH
2.2KX2
Non-iAMT
ASF 2.0
RP45
ICH_SMLINK0
ICH_SMLINK1
100KX2_NC
SMBCLK_ICH R798
SMBDATA_ICH R524
0 ICH_SMLINK0
0 ICH_SMLINK1
Modify X01-21
Non-iAMT
R789 10K_NC RSV_ICH_CL_RST1#
R519 10K ICH_RI#
R521 10K SIO_EXT_SCI#
R509 1K PCIE_WAKE#
U48C
SMBCLK
SMBDATA
LINKALERT#/GPIO60/CLGPIO3
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
PMSYNC#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP8
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
LANPHYPC/GPIO12
ENGDET/GPIO13
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
GPIO49
GPIO57/CLGPIO5
SPKR
MCH_SYNC#
TP3
TP9
TP10
TP11
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M REV 1.0
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA4GP/GPIO36
SATA5GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST0#
CL_RST1#
MEM_LED/GPIO24
ALERT#/GPIO10
NETDETECT/GPIO14
WOL_EN/GPIO9
+3.3V_RUN
R773 8.2K
CLK_ICH_14M
CLK_ICH_48M
ICH_SUSCLK
SIO_SLP_S3# 31
SIO_SLP_S4#
SIO_SLP_S5# 31
ICH_PWRGD 6,44
DPRSLPVR 6,51
R537 8.2K
+3.3V_SUS
SIO_PWRBTN# 31
RSV_ICH_LAN_RST#
ICH_RSMRST# 31
CLK_PWRGD 17
ICH_CL_PWROK 6,31
ICH_CL_RST0# 6
CL_RST1#
RSV_GPIO24
RSV_GPIO10
RSV_GPIO14
RSV_WOL_EN
R543 8.2K
Non-iAMT
Place these close to ICH8.
CLK_ICH_48M
R444 10_NC
C564 4.7P_NC
CLK_ICH_14M
R473 10_NC
C577 4.7P_NC
ICH_PWRGD R540 10K
DPRSLPVR R784 100K
ICH_RSMRST# R564 10K
RSV_ICH_LAN_RST# R523 10K
ICH_CL_PWROK R762 1M
RSV_GPIO10 R795 10K
DIS:ALW
UMA:SUS
Non-iAMT
R531 3.24K/F
R536 3.24K/F_NC
R796 3.24K/F_NC
CL_VREF0
CL_VREF1
C621 0.1U
R534 453/F
C926 0.1U_NC
R792 453/F_NC
CL_VREF0/1 ~=0.405V
Modify X01-21
30,34 SMBCLK_ICH
30,34 SMBDATA_ICH
T82 PAD
T139 PAD
T79 PAD
ICH_RI#
T48 PAD
RSV_LPCPD#
3 ITP_DBRESET#
6 PM_BMBUSY#
34 USB_MCARD1_DET#
17 H_STP_PCI#
17 H_STP_CPU#
28,31 CLKRUN#
30,33,34,42 PCIE_WAKE#
28,31 IRQ_SERIRQ
39 THERM_ALERT#
31,44,51 IMVP_PWRGD
T134 PAD
33 USB_MCARD2_DET#
33 USB_MCARD3_DET#
31 SIO_EXT_WAKE#
31 SIO_EXT_SMI#
31 SIO_EXT_SCI#
T51 PAD
Modify X02-20
37 KB_LED_DET
34 PCIE_MCARD1_DET#
R820 4.7K
33 PCIE_MCARD2_DET#
33 PCIE_MCARD3_DET#
34 WLAN_RADIO_DIS#
41 CAMERA_CBL_DET#
17 SATA_CLKREQ#
18 PLTRST_DELAY#
33 WPAN_RADIO_DIS_MINI#
33 WWAN_RADIO_DIS#
T46 PAD
T47 PAD
Modify X02-20
6 MCH_ICH_SYNC#
40 SPKR
11 ICH_RSVD
T53 PAD
T59 PAD
T150 PAD
R465 10K PLTRST_DELAY#
+3.3V_RUN
R786 2.2K_NC IMVP_PWRGD
R770 100K USB_MCARD2_DET#
R771 100K USB_MCARD3_DET#
R480 100K PCIE_MCARD1_DET#
R490 100K PCIE_MCARD2_DET#
R774 100K PCIE_MCARD3_DET#
+3.3V_RUN
R781 10K_NC MCH_ICH_SYNC#
R476 10K IRQ_SERIRQ
R500 10K THERM_ALERT#
+3.3V_SUS
R522 10K RSV_WOL_EN
R505 10K SIO_EXT_SMI#
R788 100K USB_MCARD1_DET#
+3.3V_RUN
R775 8.2K
CLKRUN#
R777 10_NC
Option to " Disable " clkrun. Pulling it down will keep the clks running.
+3.3V_RUN
R478 1K_NC
SPKR
No Reboot strap.
SPKR
Low = Default.
High = No Reboot.
SMbus address D2
These are for backdrive issue.
+3.3V_RUN
RP51 2.2KX2
SMBDATA_ICH
Q47
2N7002W-7-F
ICH_SMBDATA 15,33
+3.3V_RUN
SMBCLK_ICH
Q76
2N7002W-7-F
ICH_SMBCLK 15,33
QUANTA COMPUTER
Title
ICH9-M (PM,GPIO,SMB,CL)
Size
Document Number
GM5
Rev
B2A
Date:
Wednesday, June 25, 2008
Sheet 13 of 62


U48E
ICH9M REV 1.0
U48F
ICH9M REV 1.0
Non-iAMT
Non-iAMT
Non-iAMT
Non-iAMT
WWAN Noise - ICH improvements
WWAN Noise - ICH improvements
RESERVE 1.5V_SUS FOR VCCSUSHDA
1uH+-20%_800mA
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
10uH+-20%_100mA
VCC1_5_A TOTAL 1.342A
VCC3_3 308mA
VCCSUS 3_3 212mA
QUANTA COMPUTER
ICH9-M (POWER,GND)
Wednesday, June 25, 2008

MASTER

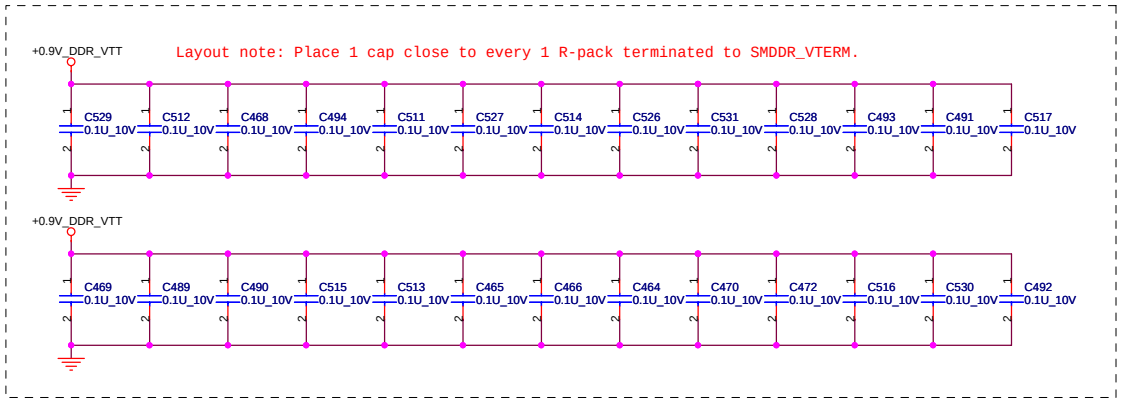


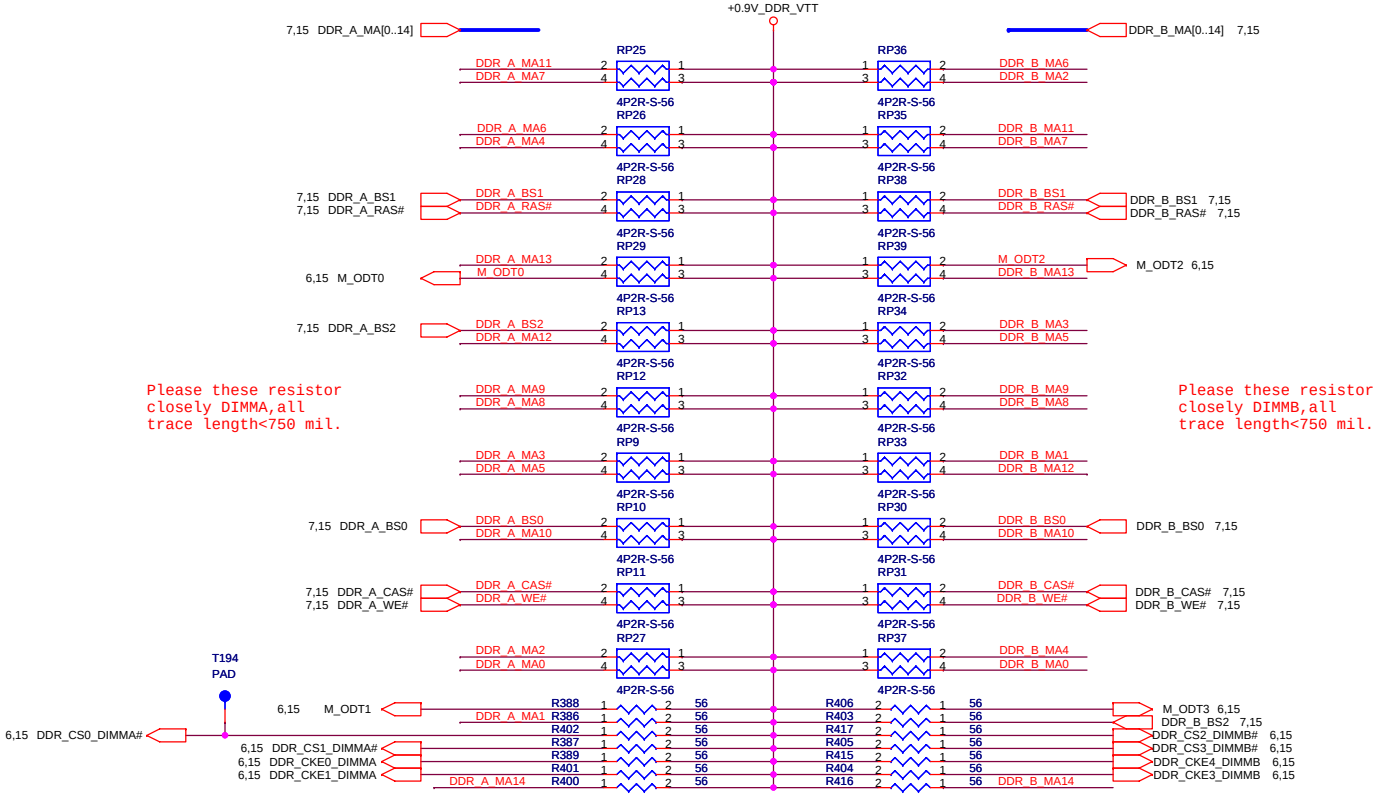
SLAVE



QUANTA COMPUTER

Title	DDR2_SO-DIMM (200P) X 2	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 15 of 62	





QUANTA COMPUTER

Title	DDR2 RES. ARRAY	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 16 of 62	

Add capacitor pads for improving WWAN.

C457 1 2 27P CLK_ICH_48M
C440 1 2 27P_NC CLK_ICH_14M
C431 1 50 2 27P_NC CLK_PCI_8512
C432 1 50 2 27P_NC CLK_PCI_PCCARD
C439 1 50 2 27P_NC CLK_PCI_ICH
50

Y2
CLK_XTAL_IN 1 2 CLK_XTAL_OUT
14.318MHZ
C437 33P
C443 33P
14.318MHz

U19
CK505
QFN64
SLG8SP513V

+CK_VDD_PCI 9 VDD_PCI
4 VDD_REF
+CK_VDD_PLL3 23 VDD_PLL3
+CK_VDD_48 16 VDD_48
+CK_VDD_SRC 46 VDD_SRC
62 VDD_CPU
+CK_VDD_MAIN 19 VDD_IO
27 VDD_IO
33 VDD_IO
43 VDD_IO
52 VDD_IO
56 VDD_IO
15 GND
18 GND
22 GND
26 GND
30 GND
36 GND
49 GND
59 GND
1 GND

CPU-0 61 CPU_BCLK
CPU-0# 60 CPU_BCLK#
CPU-1 58 MCH_BCLK
CPU-1# 57 MCH_BCLK#
SRC-8/CPU_ITP 54 CPU_ITP
SRC-8#/CPU_ITP# 53 CPU_ITP#
SRC-0/DOT96 20 DOT96_SSC
SRC-0#/DOT96# 21 DOT96_SSC#
SRC-1/SE1 24 27M_NSS
SRC-1#/SE2 25 27M_SS
SRC-2/SATA 28 PCIE_SATA
SRC-2#/SATA# 29 PCIE_SATA#
CR#_C/SRC-3 31 PCIE_MINI3
CR#_D/SRC-3# 32 PCIE_MINI3#
SRC-4 34 MCH_3GPLL
SRC-4# 35 MCH_3GPLL#
PCI_STOP#/SRC-5 45
CPU_STOP#/SRC5-5# 44
SRC-6 48 PCIE_EXPCARD
SRC-6# 47 PCIE_EXPCARD#
CR#_F/SRC-7 51 MINI1CLK_REQ# C
CR#_E/SRC-7# 50 CARD_CLK_REQ# C
SRC-9 37 PCIE_MINI2
SRC-9# 38 PCIE_MINI2#
SRC-10 41 PCIE_ICH
SRC-10# 42 PCIE_ICH#
CR#_H/SRC-11 40 PCIE_LOM
CR#_G/SRC-11# 39 PCIE_LOM#
GND 65

RP5 0 CLK_CPU_BCLK 3 CLK_CPU_BCLK# 3
RP7 0 CLK_MCH_BCLK 5 CLK_MCH_BCLK# 5
RP17 0 CLK_PCIE_MINI1 34 CLK_PCIE_MINI1# 34
RP4 0_DIS CLK_PCIE_VGA 18 CLK_PCIE_VGA# 18
RP8 0_DIS CLK_VGA_27M_NSS 19 CLK_VGA_27M_SS 19
RP16 0 CLK_PCIE_SATA 11 CLK_PCIE_SATA# 11
RP18 0 CLK_PCIE_MINI3 33 CLK_PCIE_MINI3# 33
RP20 0 CLK_MCH_3GPLL 6 CLK_MCH_3GPLL# 6
H_STP_PCI# 13 H_STP_CPU# 13
RP24 0 CLK_PCIE_EXPCARD 30 CLK_PCIE_EXPCARD# 30
475/F MINI1CLK_REQ# 34 CARD_CLK_REQ# 30
RP21 0 CLK_PCIE_MINI2 33 CLK_PCIE_MINI2# 33
RP23 0 CLK_PCIE_ICH 12 CLK_PCIE_ICH# 12
RP22 0 CLK_PCIE_LOM 42 CLK_PCIE_LOM# 42

to ATI VGA

+3.3V_RUN
H_STP_PCI# R397 2 1 10K
H_STP_CPU# R396 2 1 10K

13 SATA_CLKREQ# SATA_CLKREQ# R365 475
6 CLK_3GPLLREQ# CLK_3GPLLREQ# R364 475/F
33 CLK_LPC_DEBUG CLK_LPC_DEBUG R363 22
28 CLK_PCI_PCCARD CLK_PCI_PCCARD R354 33
31 CLK_PCI_8512 CLK_PCI_8512 R353 33
12 CLK_PCI_ICH CLK_PCI_ICH R350 33
13 CLK_ICH_48M CLK_ICH_48M R375 33
3,6 CPU_MCH_BSEL0 L55 BLM18SG260 R372 8.2K
3,6 CPU_MCH_BSEL1 R374 8.2K
3,6 CPU_MCH_BSEL2 R367 8.2K
13 CLK_ICH_14M CLK_ICH_14M R366 33
13 CLK_PWRGD

SATA_CLKREQ# C 8
CLK_3GPLLREQ# C 10
PCI_PCCARD 11
PCI_SIO 12
27M_SEL 13
PCI_ICH 14
FSA 17
FSB 64
FSC 5
55
63
CLK_XTAL_OUT 2
CLK_XTAL_IN 3
CLK_SDATA 6
CLK_SCLK 7

CR#_A/PCI-0
CR_B/PCI-1
TME/PCI-2
SRC5_EN/PCI-3
27M_SEL/PCI-4
ITP_EN/PCIF-5#
FSA/USB48
FSB/TEST_MODE
FSC/TEST_SEL/REF
RESET#
CK_PWRGD/PD#
XOUT
XIN
SDATA
SCLK

CLK_LPC_DEBUG FOR DEBUG
NEED POP RESISTOR

POP RESISTOR FOR UMA
to MCH DPLL_REF_CLK
DOT96_SSC RP6 0_UMA MCH_DREFCLK 6 MCH_DREFCLK# 6
Modify X01-9
to MCH DPLL_REF_SSCLK
27M_NSS RP14 0_UMA DREF_SSCLK 6 DREF_SSCLK# 6
CPU_ITP RP15 0_NC CLK_CPU_ITP 3 CLK_CPU_ITP# 3
POP for ITP use

+3.3V_RUN
CLK_3GPLLREQ# R355 2 1 10K
SATA_CLKREQ# R356 2 1 10K
CARD_CLK_REQ# R398 2 1 10K
MINI1CLK_REQ# R399 2 1 10K
PCI_PCCARD R343 1 10K_NC
PCI_SIO R352 1 10K_NC
PCI_ICH R341 1 10K_NC

UMA without iAMT
+3.3V_RUN
L58 BLM21PG600SN1D 805 120 ohms@100Mhz
+CK_VDD_MAIN
C459 0.1U C476 0.1U C486 0.1U C462 0.1U C473 0.1U C485 0.1U C487 10U_NC
L51 BLM21PG600SN1D 805 120 ohms@100Mhz
R359 2.2 +CK_VDD_PCI C446 0.1U C1005 0.1U
R391 2.2 +CK_VDD_PLL3 C461 0.1U
R358 2.2 +CK_VDD_48 C448 0.1U C447 4.7U
R377 2.2 +CK_VDD_SRC 603 C460 0.1U C993 0.1U

Non-iAMT
SMbus address D2
These are for backdrive issue.
+3.3V_RUN
RP3 2.2KX2
26,31,39 SMBDAT1 Q40 2N7002W-7-F CLK_SDATA
26,31,39 SMBCLK1 Q39 2N7002W-7-F CLK_SCLK

PCI_ICH
R339 10K_NC
R340 10K_NC

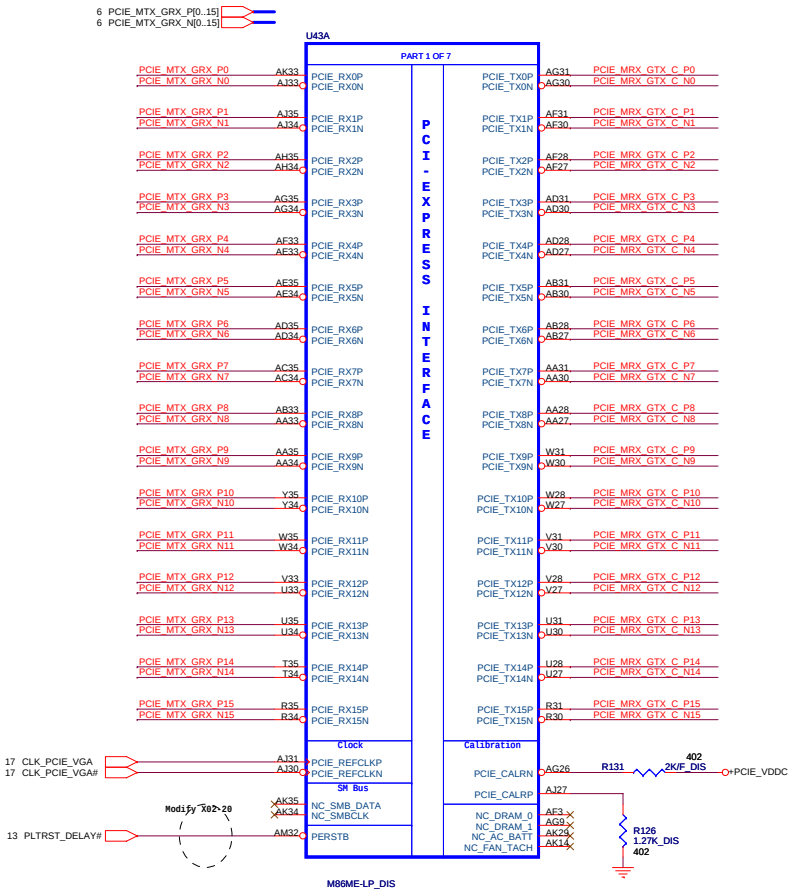
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

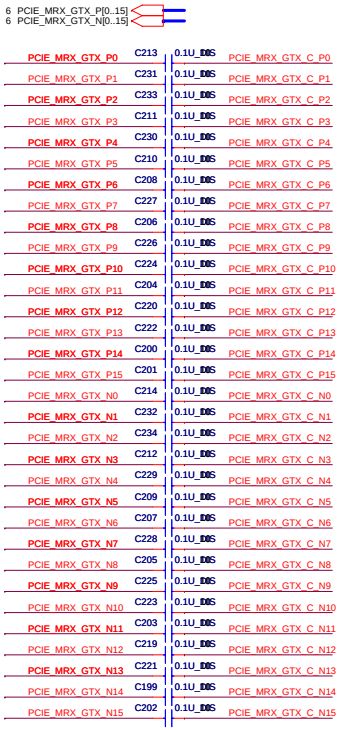
27M_SEL
+3.3V_RUN
R351 10K_DIS
27M_SEL
R342 10K_UMA

27M_SEL (PIN13)	PIN20	PIN21	PIN24	PIN25
0=UMA	DOT96T	DOT96C	96/ 100M_T	96/ 100M_C
1 = Disc. GRFX down	SRCT0	SRCC0	27Mout	27MSSout

QUANTA COMPUTER

Title	CLOCK GENERATOR	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 17 of 62	





QUANTA COMPUTER

Title	VGA-M82-S (PCIe)	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 18 of 62	

MEMORY APERTURE SIZE SELECT				
MEMORY SIZE	CFG3 GPIO9	CFG2 GPIO13	CFG1 GPIO12	CFG0 GPIO11
128MB	X	0	0	0
256MB	X	0	0	1
64MB	X	0	1	0
512MB	X	1	0	0

Memory Straps	RAM_ TYPE_CFG3	RAM_ TYPE_CFG2	RAM_ TYPE_CFG1	RAM_ TYPE_CFG0
400 MHz 256MB(16M*16) Hynix	1	1	1	1
400 MHz 256MB(16M*16) Qimonda	1	1	1	0
500 MHz 256MB(16M*16) Hynix	1	1	0	1
500 MHz 256MB(16M*16) Qimonda	1	1	0	0
500 MHz 256MB(16M*16) Samsung	1	0	1	1

8/15: The strap on VIP[3] is for enabling HD Audio on M86.

VRAM SIZE

VRAM TYPE

HDMI CONN

GFX_CORE_CNTRL_TABLE		
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.1V

DIS only

Layout Note:
Place 150 ohm termination resistors close to ATI CHIP.

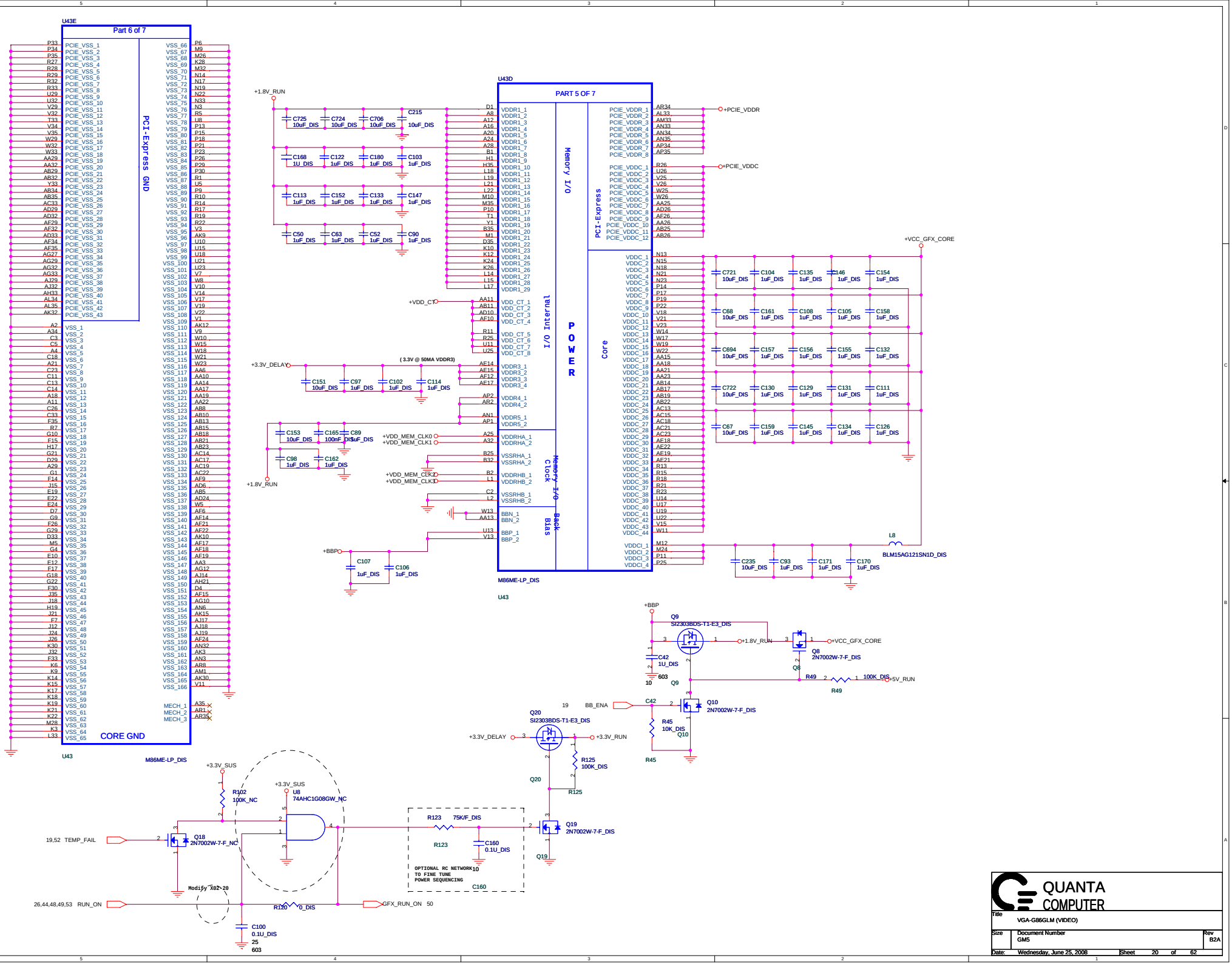
LVDS

HDMI

CRT

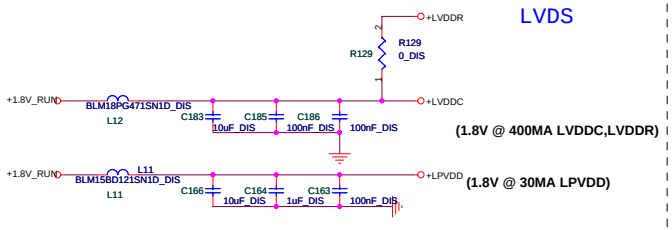
QUANTA COMPUTER

Title	VGA-G86GLM (VIDEO)	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 19 of 62	

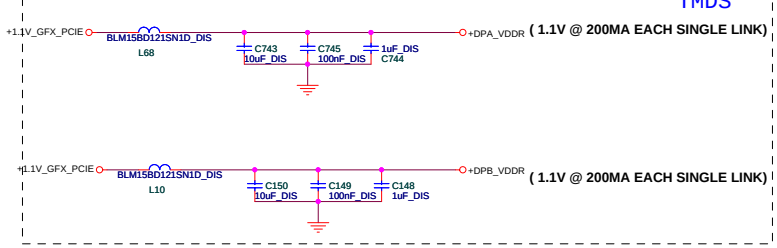


Title	VGA-G86GLM (VIDEO)
Size	Document Number GM5
Rev	B2A
Date:	Wednesday, June 25, 2008
Sheet	20 of 62

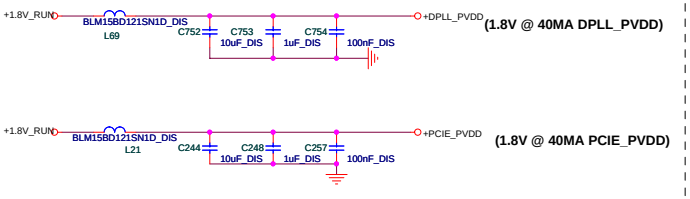
LVDS

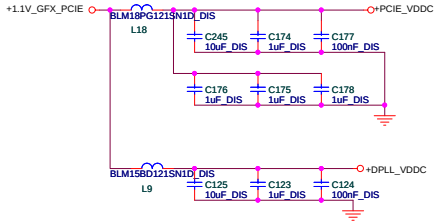


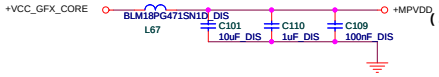
TMDS

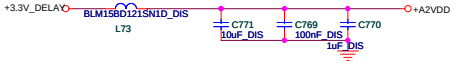


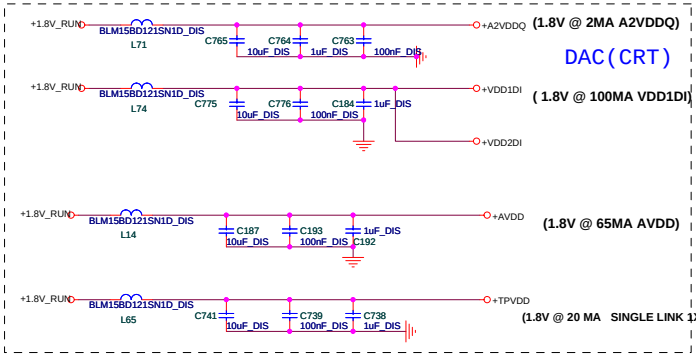
PLL_CLK

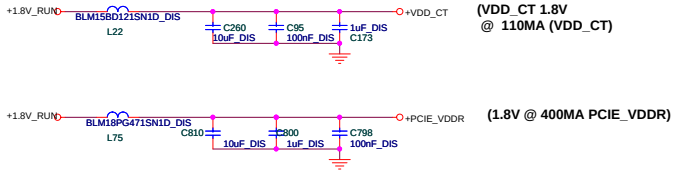






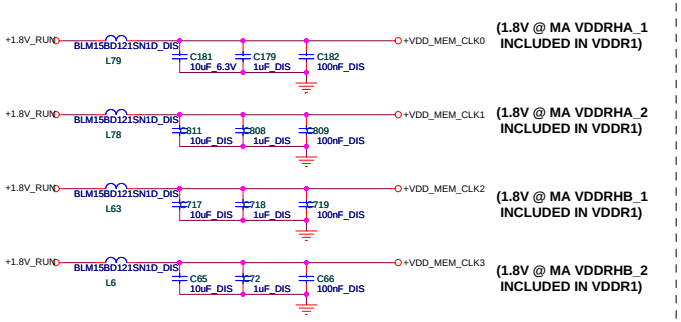






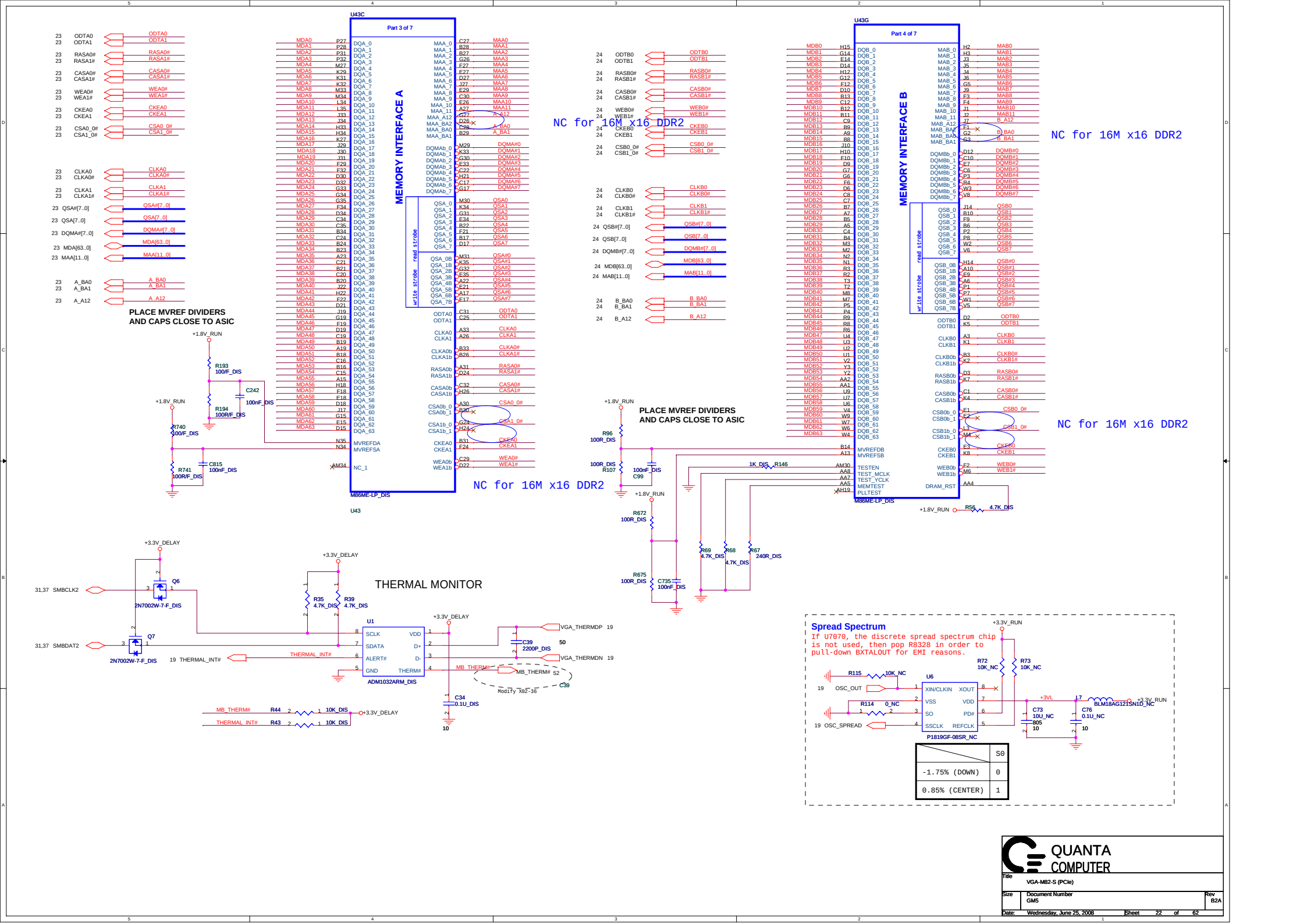
PLACE ALL DECOUPLING AS CLOSE TO ASIC AS POSSIBLE

MEM IO CLK

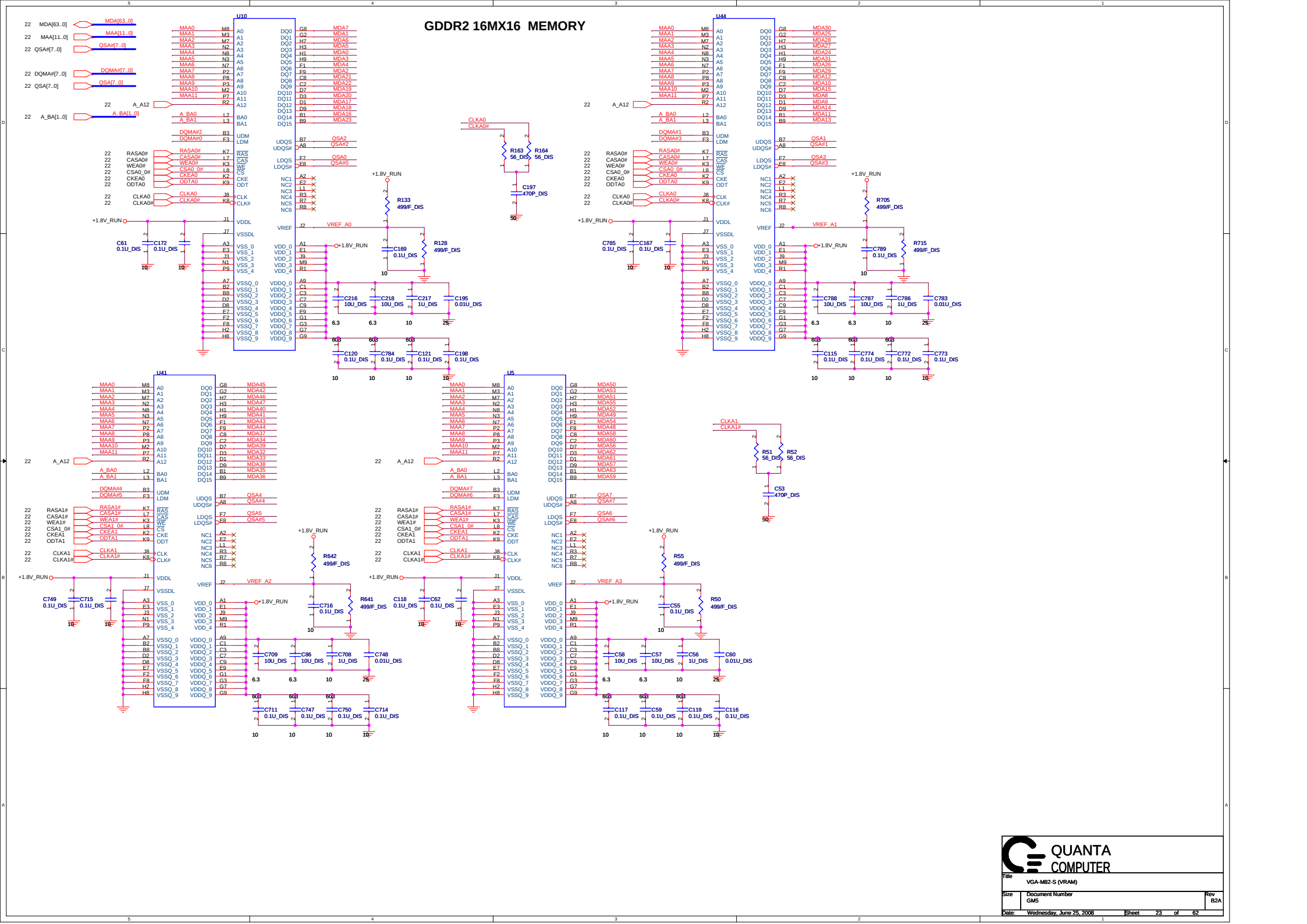


QUANTA COMPUTER

Title	VGA-G86GLM (VIDEO)	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 21 of 62	


U43C
Part 3 of 7
MEMORY INTERFACE A
M88ME-LP_DIS
U43
NC for 16M x16 DDR2
U43G
Part 4 of 7
MEMORY INTERFACE B
M88ME-LP_DIS
NC for 16M x16 DDR2
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
+1.8V_RUN
R193 100/F_DIS
R194 100R/F_DIS
C242 100nF_DIS
R740 100/F_DIS
R741 100R/F_DIS
C815 100nF_DIS
PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC
R96 100R_DIS
R107 100R_DIS
C99 100nF_DIS
1K_DIS_R146
R672 100R_DIS
R675 100R_DIS
C735 100nF_DIS
R69 4.7K_DIS
R68 4.7K_DIS
R67 240R_DIS
R56 4.7K_DIS
THERMAL MONITOR
+3.3V_DELAY
Q6 2N7002W-7-F_DIS
Q7 2N7002W-7-F_DIS
R35 4.7K_DIS
R39 4.7K_DIS
U1
ADM1032ARM_DIS
SCLK
SDATA
ALERT#
GND
VDD
D+
D-
THERM#
THERMAL_INT#
MB_THERM#
C39 2200P_DIS
C34 0.1U_DIS
R44 10K_DIS
R43 10K_DIS
VGA_THERMDP 19
VGA_THERMDN 19
MB_THERM# 52
Modify X02-36
Spread Spectrum
If U7070, the discrete spread spectrum chip is not used, then pop R8328 in order to pull-down BXTALOUT for EMI reasons.
+3.3V_RUN
R72 10K_NC
R73 10K_NC
R115 10K_NC
R114 0_NC
U6
P1819GF-08SR_NC
XIN/CLKIN
XOUT
VSS
VDD
SO
PD#
SSCLK
REFCLK
OSC_OUT
OSC_SPREAD
+3VL
L7 BLM18AG121SN1D_NC
C73 10U_NC 805
C76 0.1U_NC
S0
-1.75% (DOWN) 0
0.85% (CENTER) 1
QUANTA COMPUTER
Title
VGA-M82-S (PCIe)
Size
Document Number
GM5
Rev
B2A
Date: Wednesday, June 25, 2008
Sheet 22 of 62

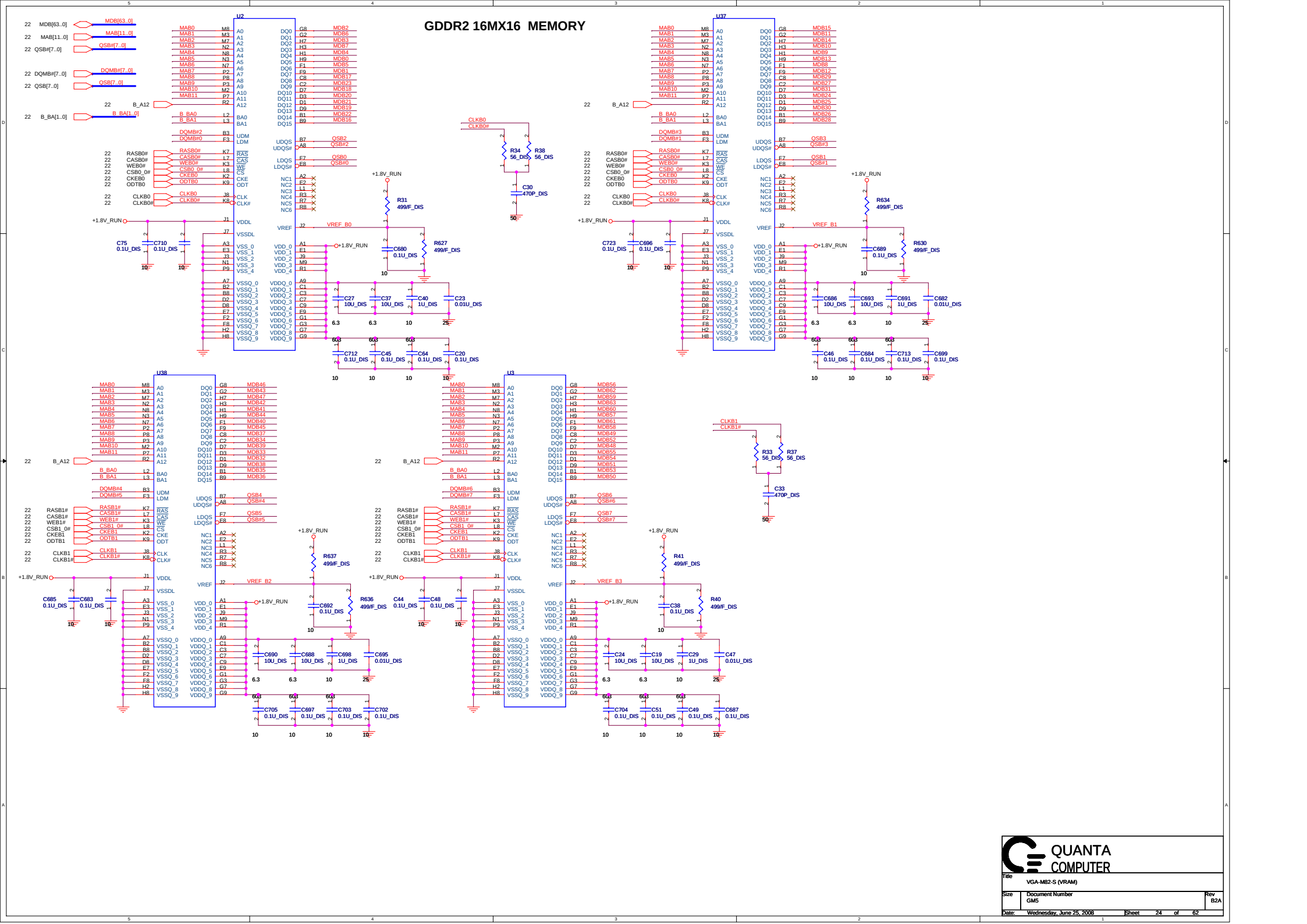
GDDR2 16MX16 MEMORY



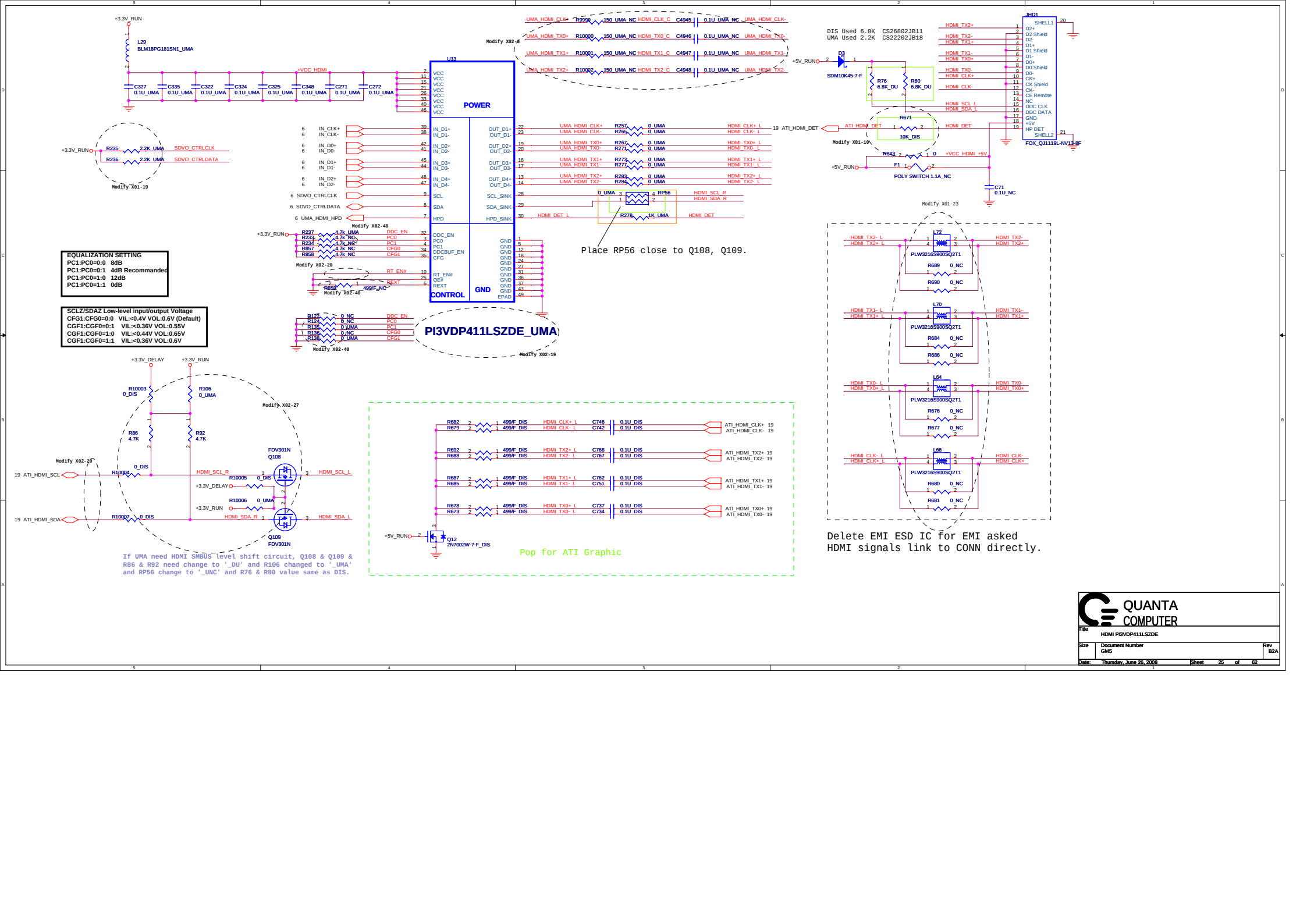
QUANTA COMPUTER

Title	VGA-M82-S (VRAM)	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 23 of 62	

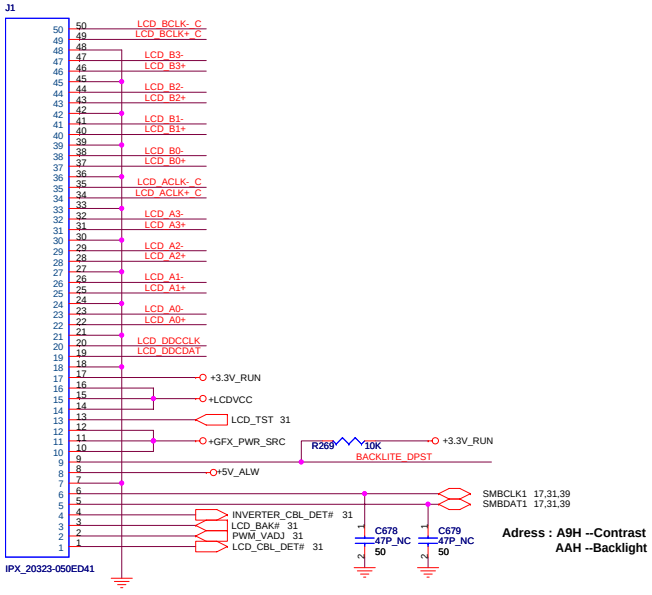
GDDR2 16MX16 MEMORY



QUANTA COMPUTER			
Title	VGA-M82-S (VRAM)		
Size	Document Number GM5		Rev B2A
Date: Wednesday, June 25, 2008		Sheet 24 of 62	

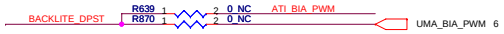

+3.3V_RUN
L29
BLM18PG181SN1_UMA
+VCC_HDMI
C327 0.1U_UMA
C335 0.1U_UMA
C322 0.1U_UMA
C324 0.1U_UMA
C325 0.1U_UMA
C348 0.1U_UMA
C271 0.1U_UMA
C272 0.1U_UMA
U13
POWER
VCC
GND
CONTROL
PI3VDP411LSZDE_UMA
Modify X02-19
Modify X02-40
Modify X02-20
Modify X02-27
Modify X01-19
Modify X01-10
Modify X01-23
R235 2.2K_UMA SDVO_CTRLCLK
R236 2.2K_UMA SDVO_CTRLDATA
UMA_HDMI_CLK+ R9999 150_UMA_NC HDMI_CLK_C C4945 0.1U_UMA_NC UMA_HDMI_CLK-
UMA_HDMI_TX0+ R10000 150_UMA_NC HDMI_TX0_C C4946 0.1U_UMA_NC UMA_HDMI_TX0-
UMA_HDMI_TX1+ R10001 150_UMA_NC HDMI_TX1_C C4947 0.1U_UMA_NC UMA_HDMI_TX1-
UMA_HDMI_TX2+ R10002 150_UMA_NC HDMI_TX2_C C4948 0.1U_UMA_NC UMA_HDMI_TX2-
DIS Used 6.8K CS26802JB11
UMA Used 2.2K CS22202JB18
D3
SDM10K45-7-F
R76 6.8K_DU
R80 6.8K_DU
R671 10K_DIS
F1 POLY SWITCH 1.1A_NC
C71 0.1U_NC
JHD1
FOX_QJ1119L-NV13-8F
R237 4.7K_UMA
R233 4.7K_NC
R234 4.7K_NC
R857 4.7K_NC
R858 4.7K_NC
R852 499/F_NC
R127 0_NC
R124 0_NC
R135 0_UMA
R136 0_NC
R138 0_UMA
RP56
R278 1K_UMA
EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB
SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CFG1:CFG0=0:1 VIL:<0.36V VOL:0.55V
CFG1:CFG0=1:0 VIL:<0.44V VOL:0.65V
CFG1:CFG0=1:1 VIL:<0.36V VOL:0.6V
Place RP56 close to Q108, Q109.
+3.3V_DELAY
R10003 0_DIS
R106 0_UMA
R86 4.7K
R92 4.7K
FDV301N Q108
R10004 0_DIS
R10005 0_DIS
R10006 0_UMA
R10007 0_DIS
Q109 FDV301N
If UMA need HDMI SMBUS level shift circuit, Q108 & Q109 & R86 & R92 need change to '_DU' and R106 changed to '_UMA' and RP56 change to '_UNC' and R76 & R80 value same as DIS.
R682 R679 499/F_DIS HDMI_CLK+_L HDMI_CLK-_L C746 C742 0.1U_DIS
R692 R688 499/F_DIS HDMI_TX2+_L HDMI_TX2-_L C768 C767 0.1U_DIS
R687 R685 499/F_DIS HDMI_TX1+_L HDMI_TX1-_L C762 C751 0.1U_DIS
R678 R673 499/F_DIS HDMI_TX0+_L HDMI_TX0-_L C737 C734 0.1U_DIS
Q12 2N7002W-7-F_DIS
Pop for ATI Graphic
L72 PLW3216S900SQ2T1
L70 PLW3216S900SQ2T1
L64 PLW3216S900SQ2T1
L66 PLW3216S900SQ2T1
R689 R690 R684 R686 R676 R677 R680 R681 0_NC
Delete EMI ESD IC for EMI asked HDMI signals link to CONN directly.
QUANTA COMPUTER
Title HDMI PI3VDP411LSZDE
Size Document Number GM5 Rev 82A
Date: Thursday, June 26, 2008 Sheet 25 of 62

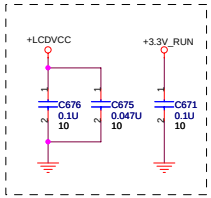
FOR ATI&UMA DIFFERENT LVDS PATH

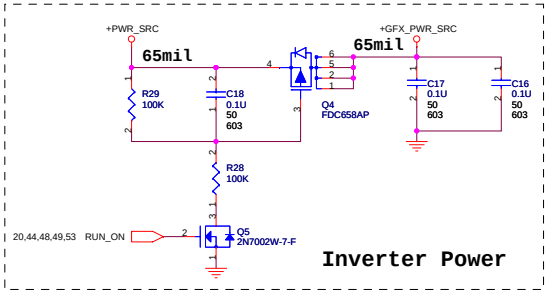


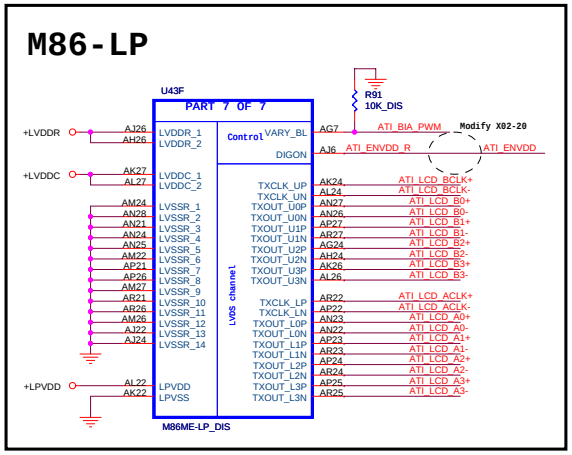
Adress : A9H --Contrast
AAH --Backlight

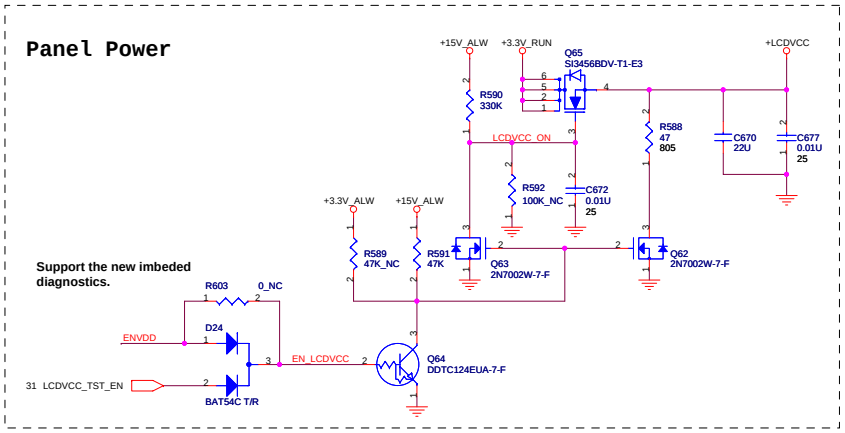
GFX_PWR_SRC layout note:
40 mil trace for tube type
45 mil for white LED type
65 mil for RGB LED type

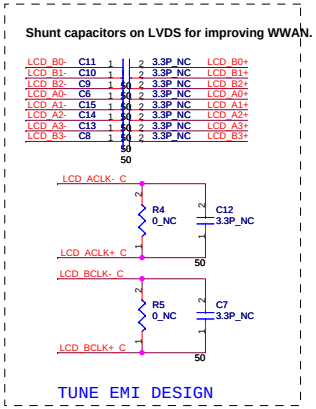






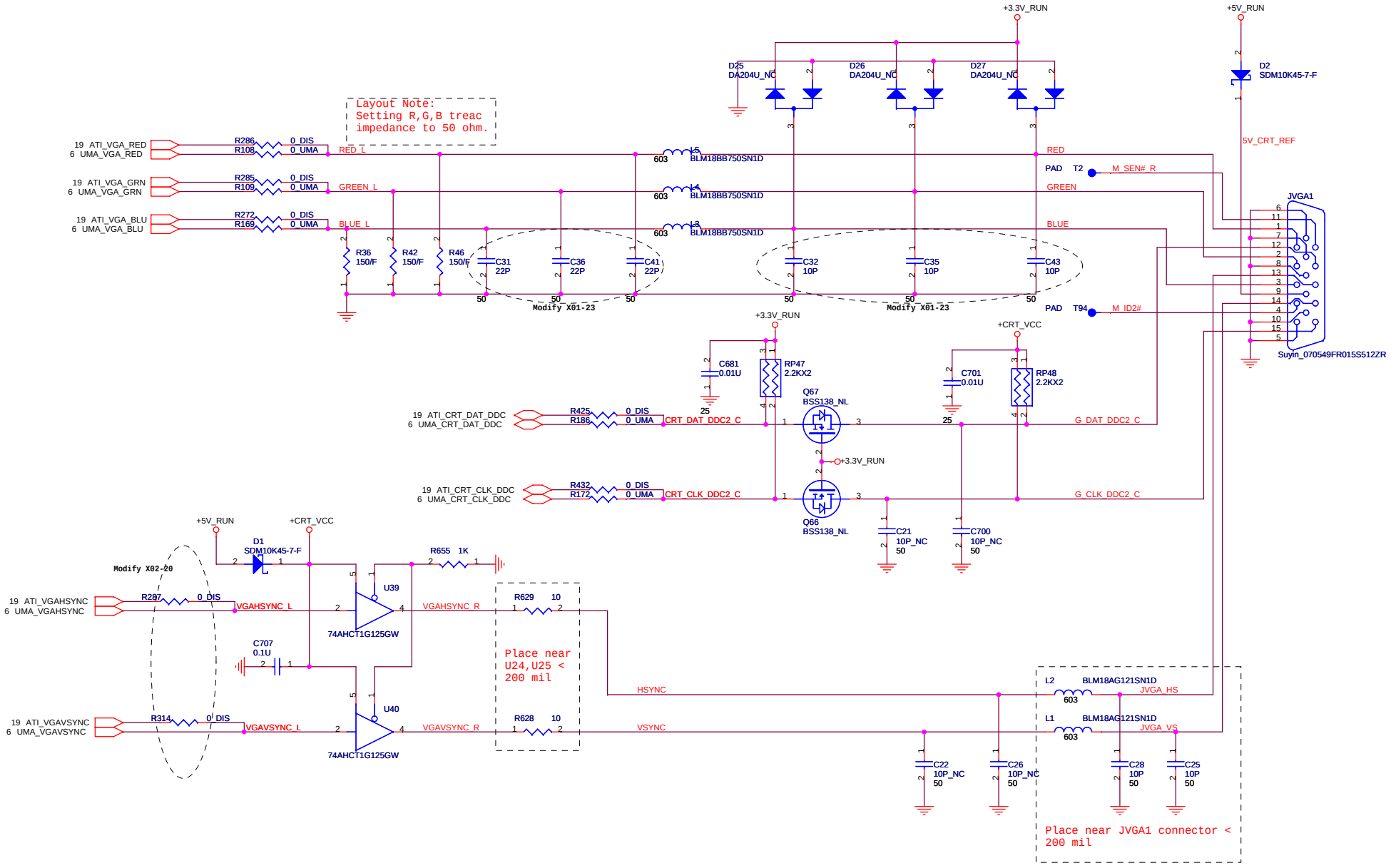






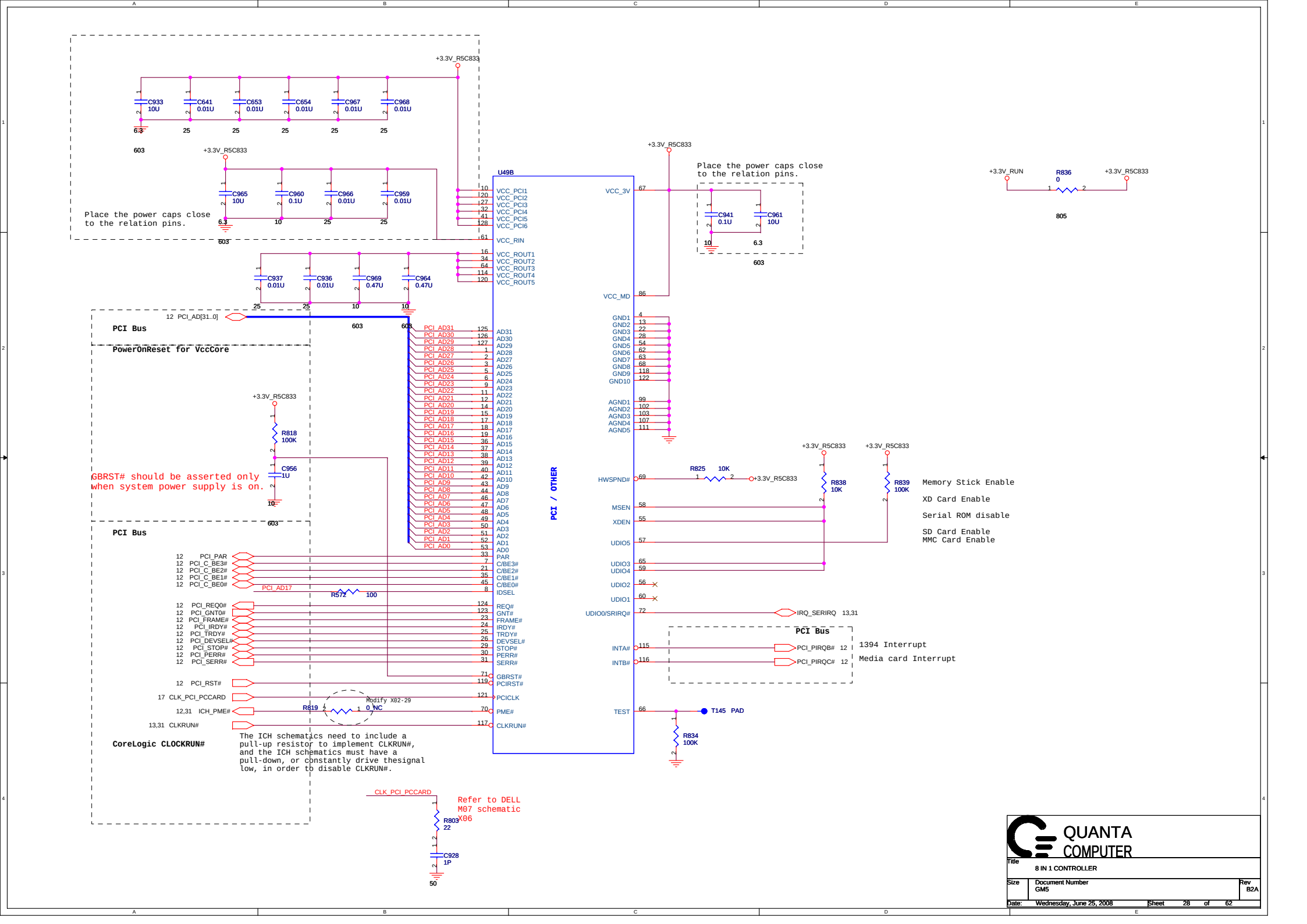
QUANTA COMPUTER

Title	LCD CONN & CK-SSCD	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 26 of 62	



QUANTA COMPUTER

Title	CRT&TV CONN	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 27 of 62	



Title	8 IN 1 CONTROLLER	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 28 of 62	

80 mils

L85
BLM18PG181SN1D
modify
+3.3V_RUN_PHY
+3.3V_R5C833

C938 10U 603
C935 0.1U 10
C636 0.01U 25
C635 1000P 50
603

Place these caps as close to the R5C833 as possible.

U49A

AVCC_PHY1 98
AVCC_PHY2 106
AVCC_PHY3 110
AVCC_PHY4 112
6.3

AS CLOSE AS POSSIBLE TO R5C833

TPBIAS0 113
TPBIAS0
C929 0.33U 603 16
C931 0.01U 25
R802 56.2/F
R801 56.2/F

TPBN0 104 TPB0N
TPBP0 105 TPB0P
TPAN0 108 TPA0N
TPAP0 109 TPA0P

R800 56.2/F
R799 56.2/F
C930 270P 25
R794 5.11K/F

*TPA0P/TPA0N,TPB0P/TPB0N pair trace : As close as possible.
*TPA0P/TPA0N,TPB0P/TPB0N pair trace : Same length electrically.
*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

Circuit area : As small as possible.

GUARD GND

C940 22P 50
1394_XI
94 XI
Y4 24.576MHZ
C939 22P 50
1394_XO
95 XO
Modify X02-20

C934 0.01U_NC 25
RICOH_FILO
96 FIL0

R793 10K/F
RICOH_REXT
101 REXT

C932 0.01U 25
RICOH_VREF
100 VREF

Place these caps as close to the IC as possible.

IEEE1394/SD

97 RSV

MDIO17 87 XD/MMC_DATA7 30
MDIO16 92 XD/MMC_DATA6 30
MDIO15 89 XD/MMC_DATA5 30
MDIO14 91 XD/MMC_DATA4 30
MDIO13 90 SD/XD/MS_DATA3 30
MDIO12 93 SD/XD/MS_DATA2 30
MDIO11 81 SD/XD/MS_DATA1 30
MDIO10 82 SD/XD/MS_DATA0 30

MDIO05 75 XD_WP# 30
MDIO08 88 SD/XD/MS_CMD 30
MDIO19 83 XD_ALE 30
MDIO18 85 XD_CLE 30
MDIO02 78 XD_CE# 30

MDIO03 77 SD_WP#(XDR/B#) 30
MDIO00 80 SD_CD# 30
SD_CD#
D32 1SS355
MDIO01 79 MS_INS# 30
MS_INS#
D33 1SS355
MDIO09 84 SD/XD/MS_CLK 30
MDIO04 76 MC_PWR_CTRL_0 30
MDIO06 74 PAD
T141
MDIO07 73

+3.3V_R5C833
R814 10K_NC
close to the Chip
XD_CDSW# 30

AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

L82
DLW21HN181SQ2L_NC
R751 0
R750 0
R752 0
R754 0
L83
DLW21HN181SQ2L_NC

TPB0N TPB0-
TPB0P TPB0+
TPA0N TPA0-
TPA0P TPA0+

CON1
FOX_UV31413-WS51P-7F

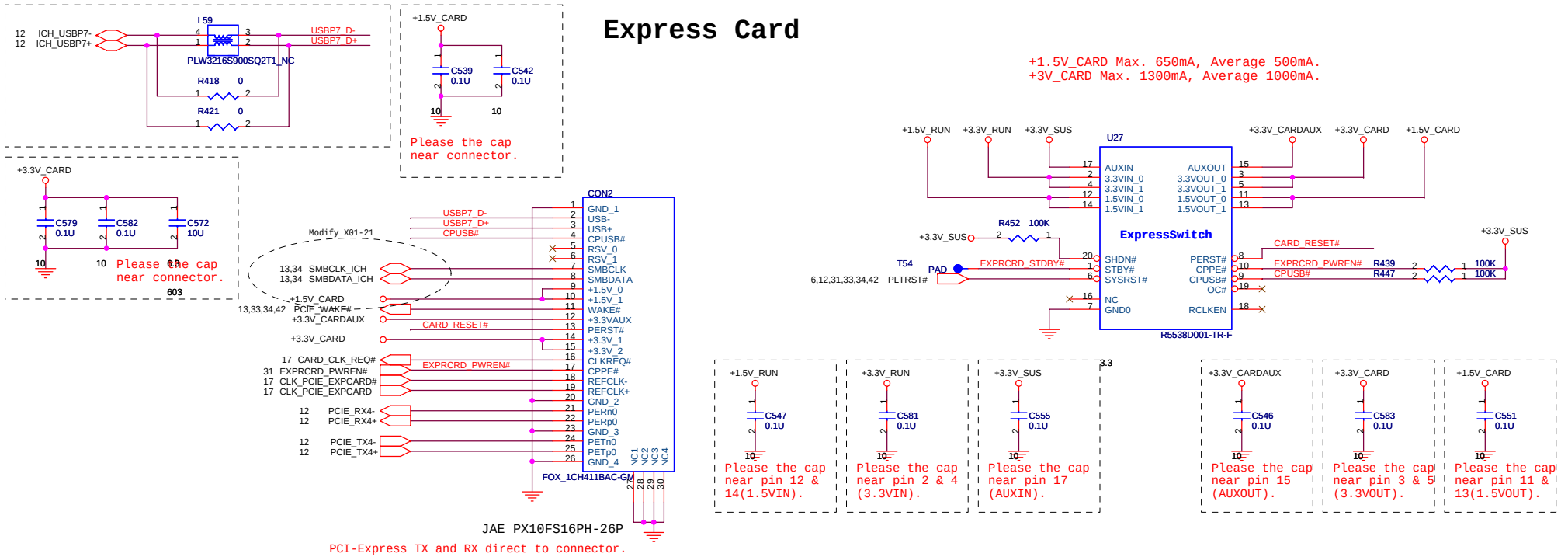
TPB0-
TPB0+
TPA0-
TPA0+

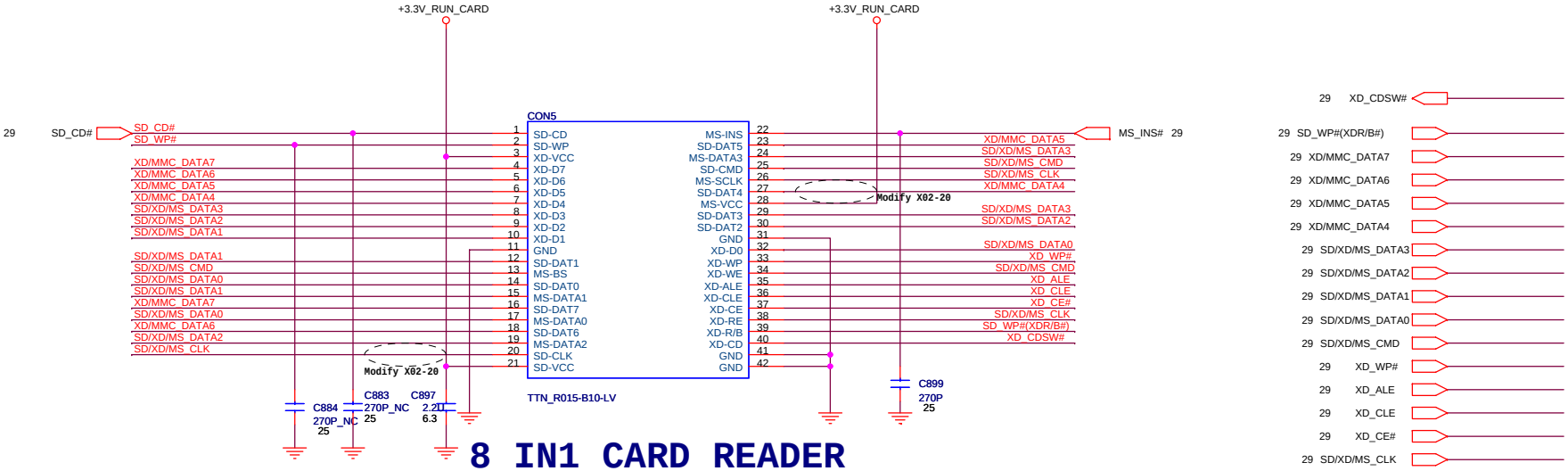
QUANTA COMPUTER

Title	IEEE 1394	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 29 of 62	

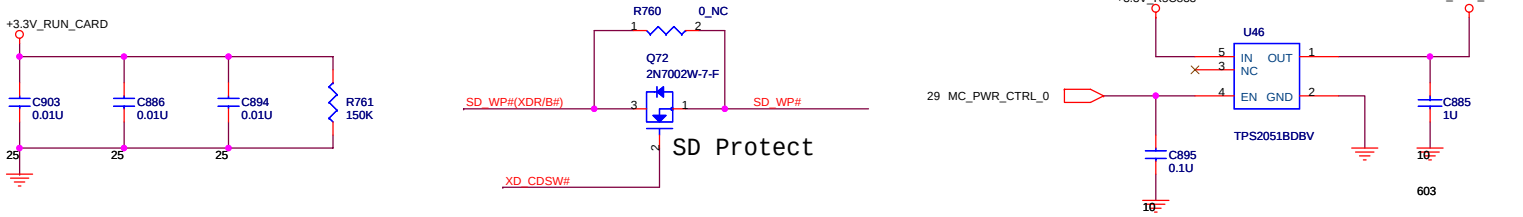
Express Card

+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.

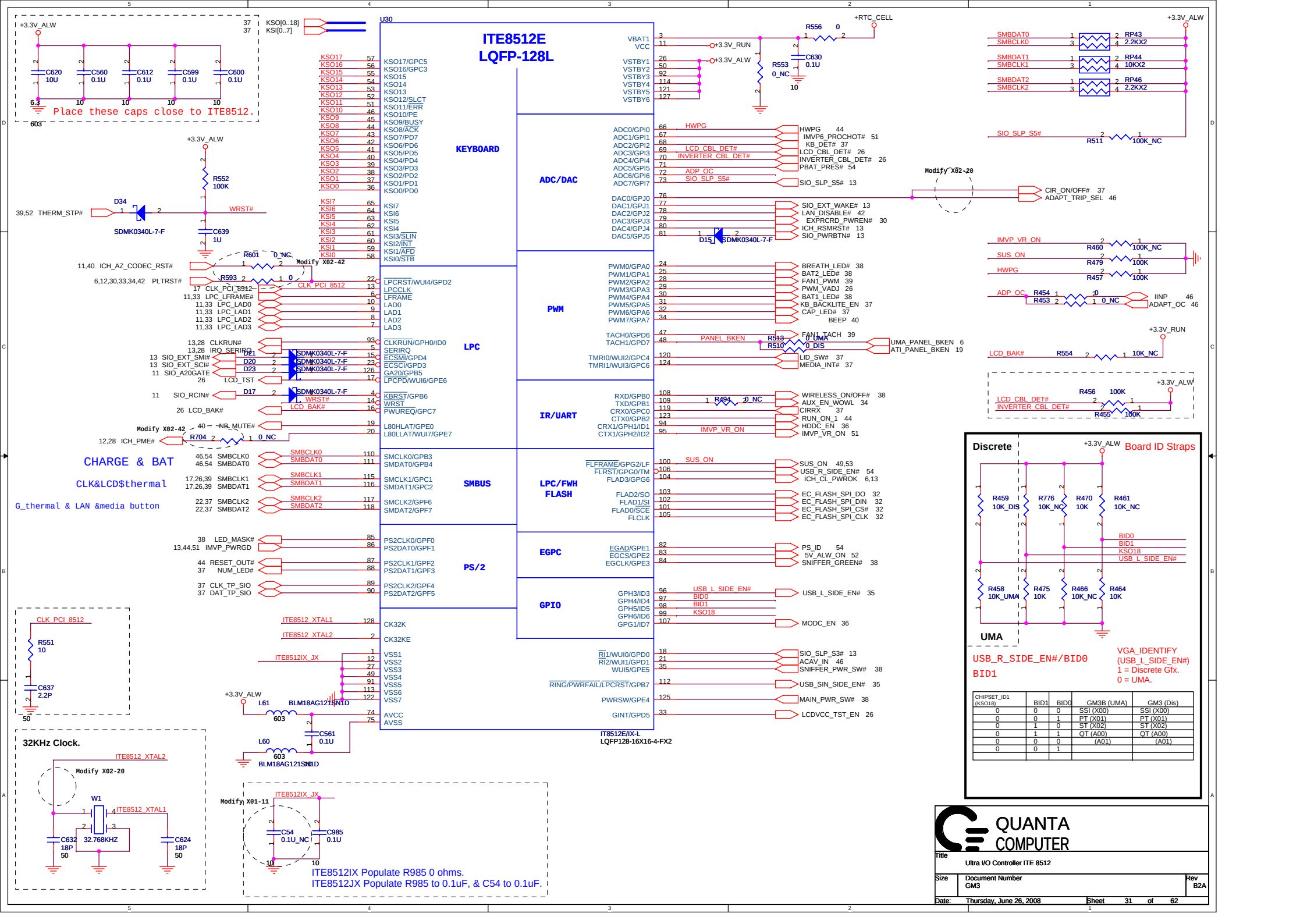




8 IN1 CARD READER

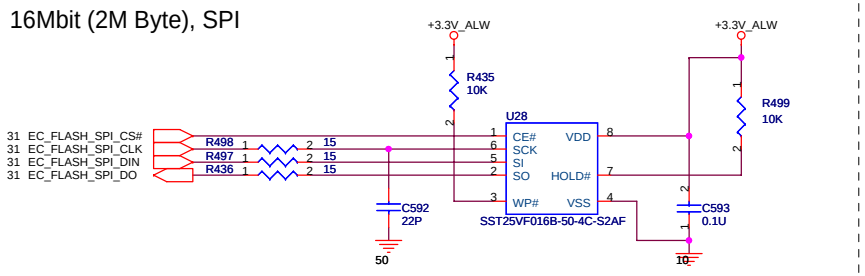


Title	ExpressCard/SmartCard	
Size	Document Number GM5	Rev B2A
Date:	Wednesday, June 25, 2008	Sheet 30 of 62

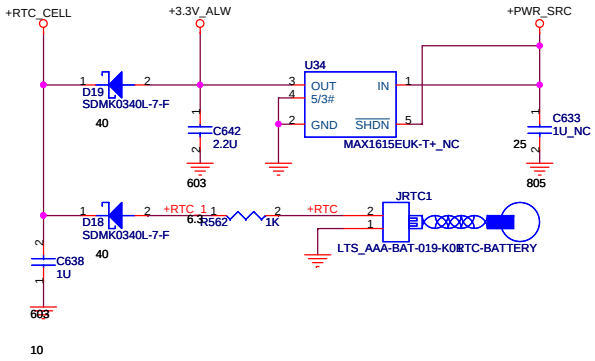


CHIPSET_ID1 (KSO18)	BID1	BID0	GM3B (UMA)	GM3 (Dis)
0	0	0	SSI (X00)	SSI (X00)
0	0	1	PT (X01)	PT (X01)
0	1	0	ST (X02)	ST (X02)
0	1	1	QT (A00)	QT (A00)
0	0	0	(A01)	(A01)
0	0	1		

16Mbit (2M Byte), SPI

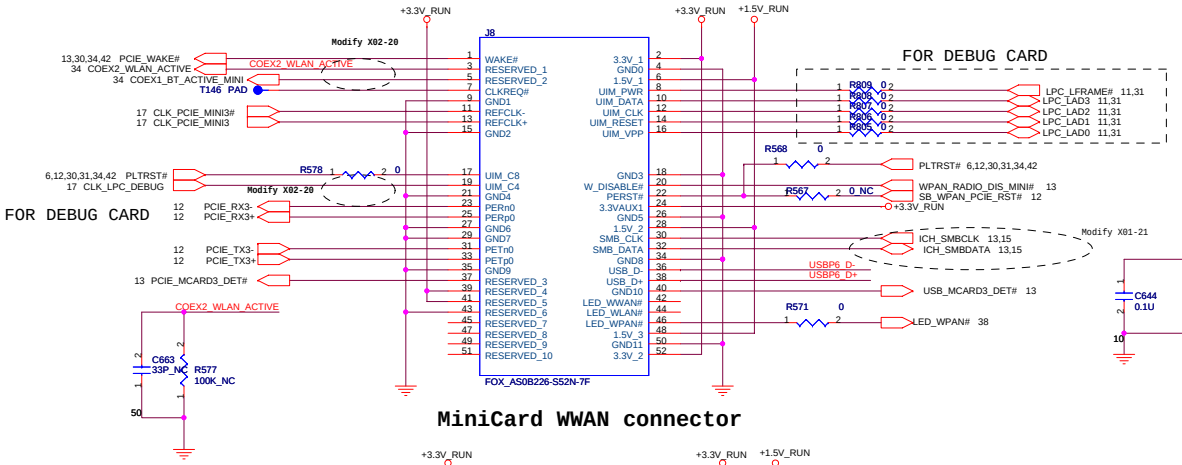


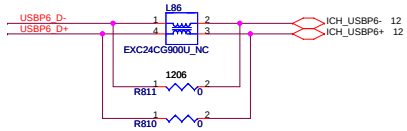
RTC BATTERY

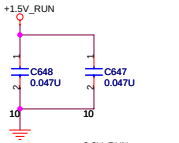


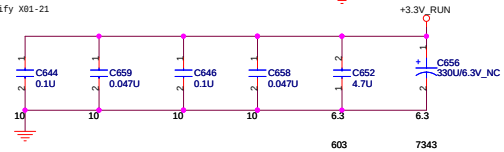
QUANTA COMPUTER		
Title	Ultra I/O Controller ECE5028	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 32 of 62	

MiniCard Robson, UWB connector

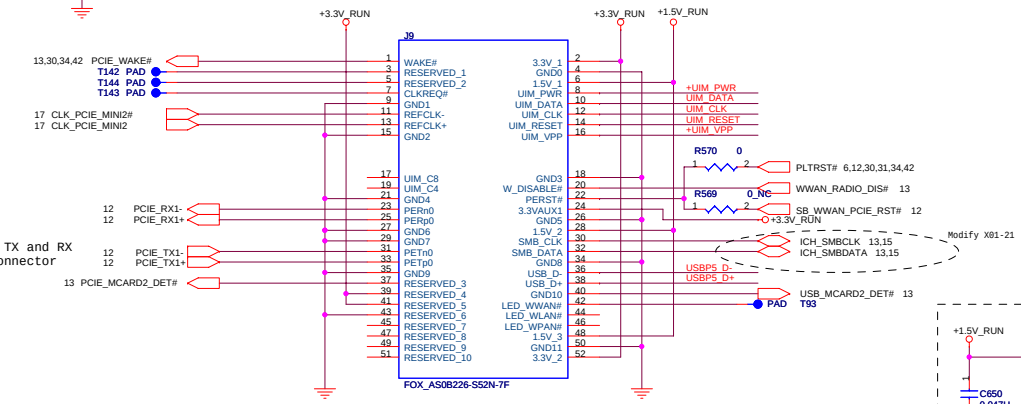




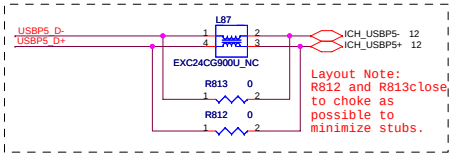


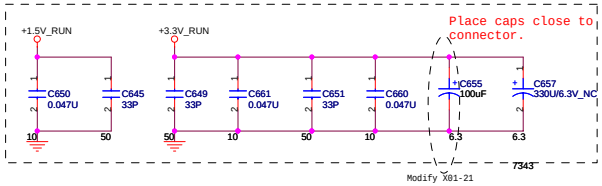


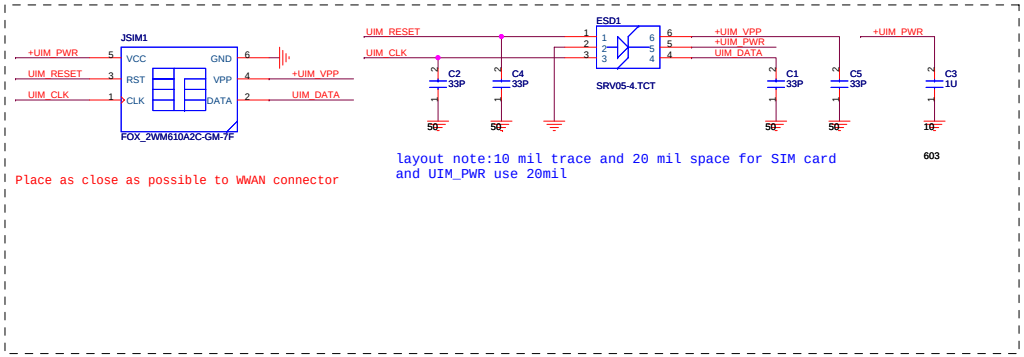
MiniCard WWAN connector



PCI-Express TX and RX direct to connector

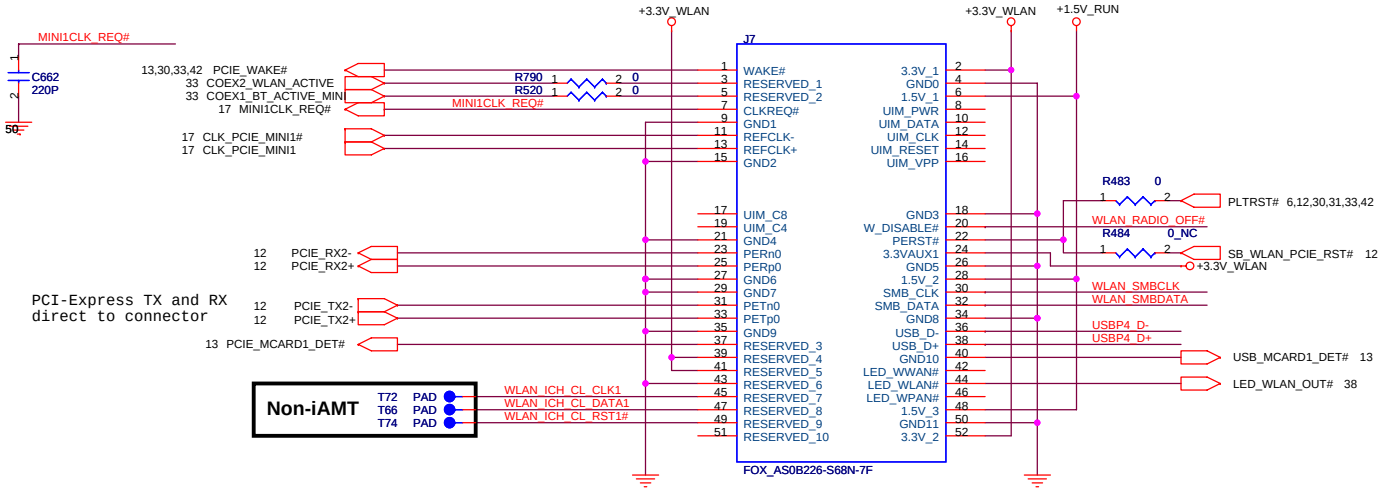


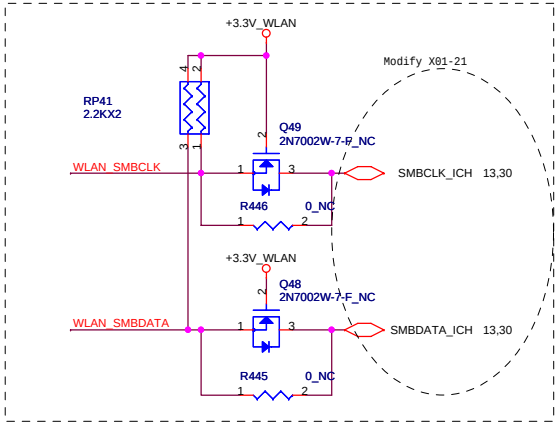


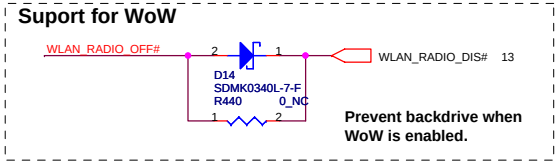


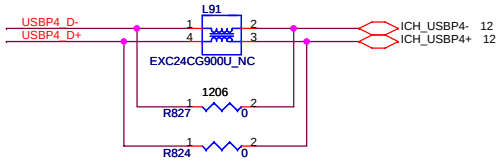
QUANTA COMPUTER		
Title: WWAN, WPAN		
Size	Document Number: GM5	Rev: B2A
Date: Wednesday, June 25, 2008	Sheet 33 of 62	

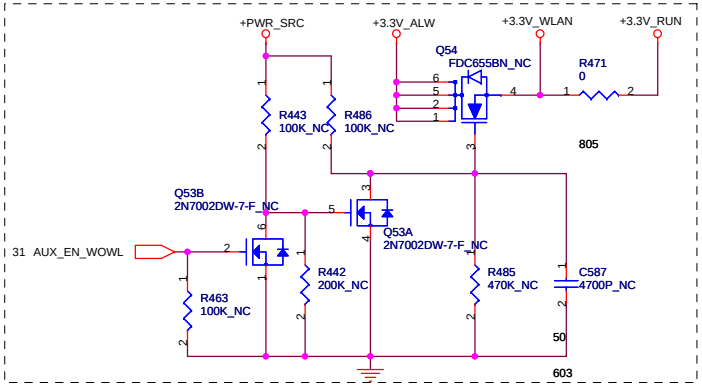
MiniCard WLAN connector

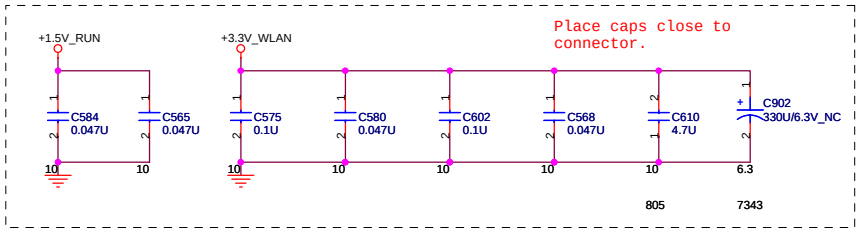






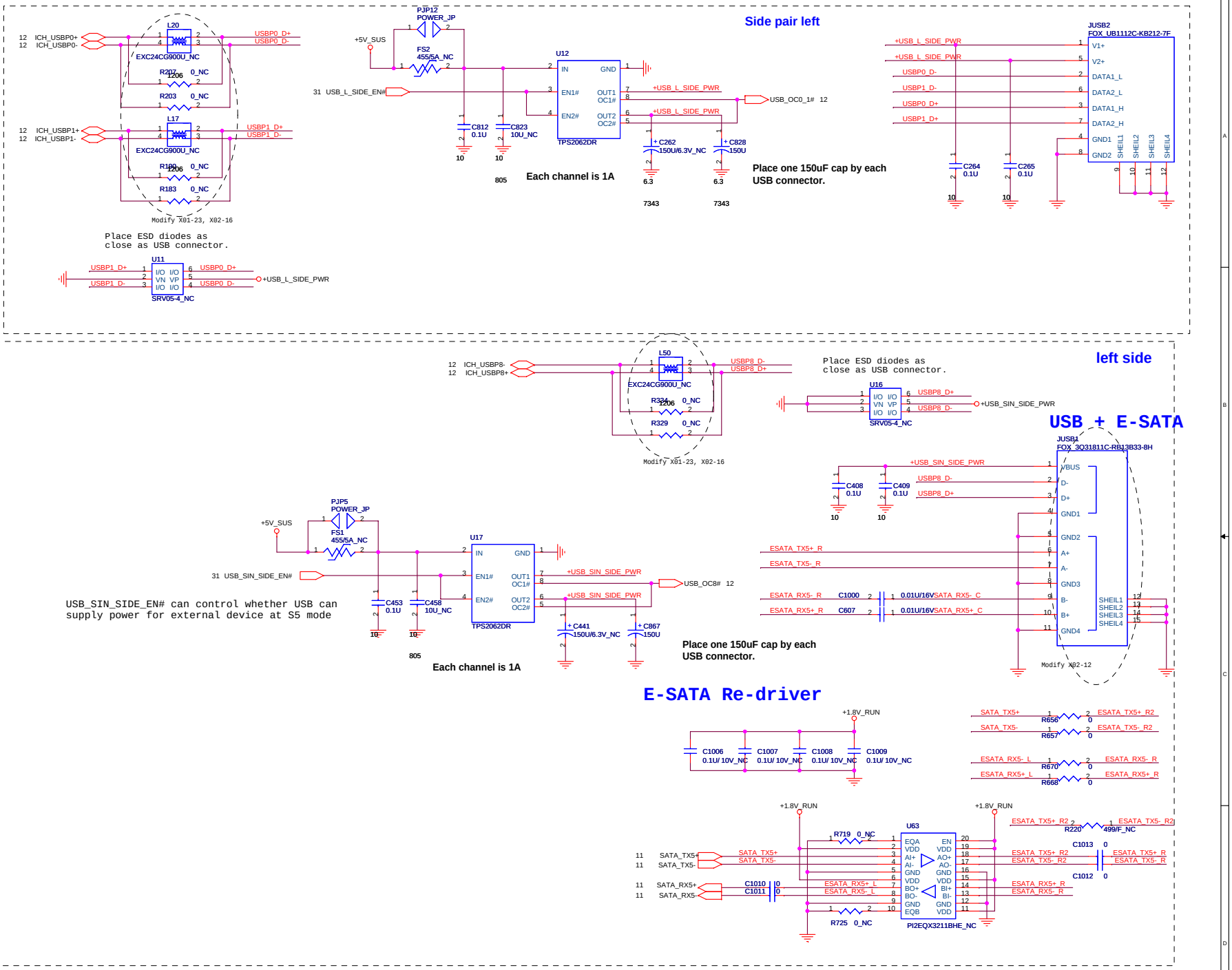






QUANTA COMPUTER

Title	WLAN	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 34 of 62	



QUANTA COMPUTER

Title	External USB	
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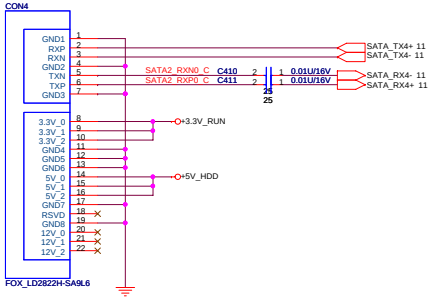
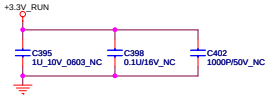
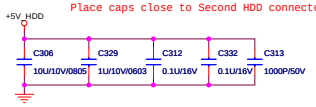
Second HDD

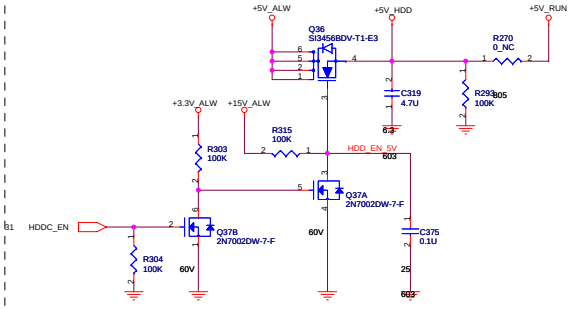
SATA Connector.



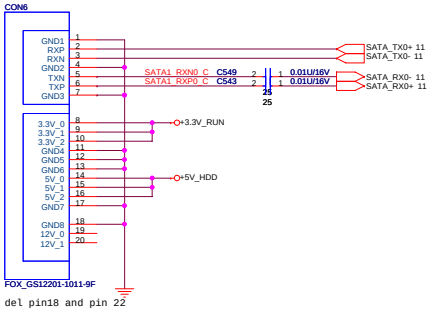


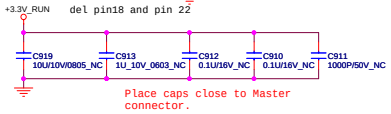


Place caps close to Second HDD connector.

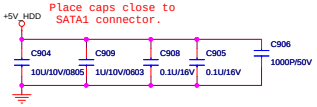


Master



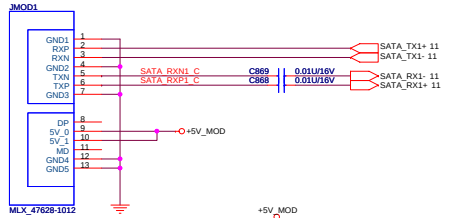


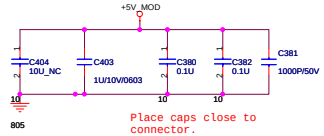
Place caps close to Master connector.



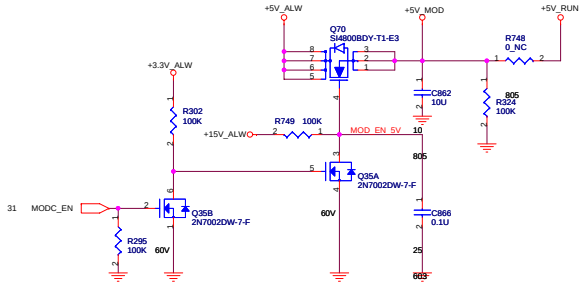
Place caps close to SATA1 connector.

ODD Connector





Place caps close to connector.



QUANTA COMPUTER		
Title: SATA (HDD&CD_ROM)		
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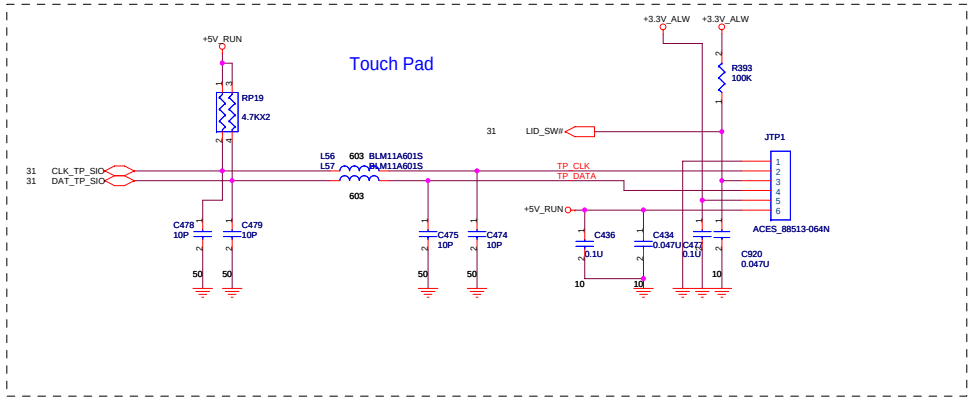

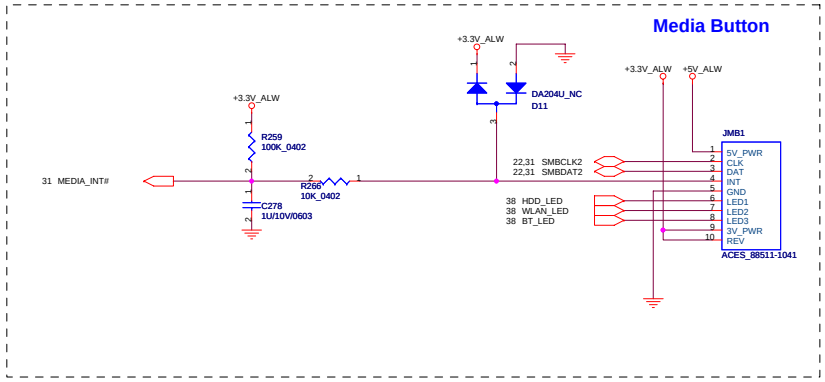

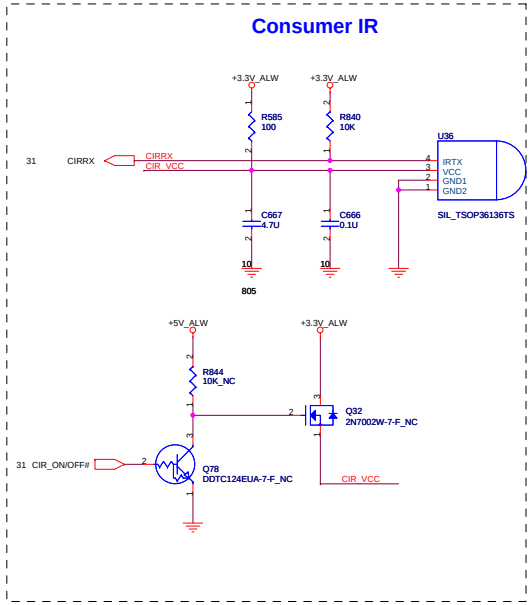

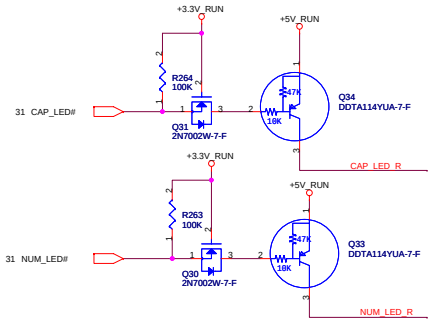

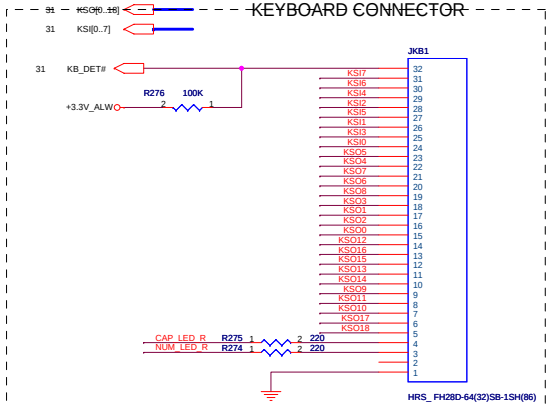

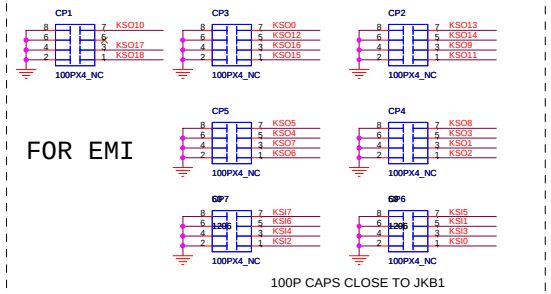

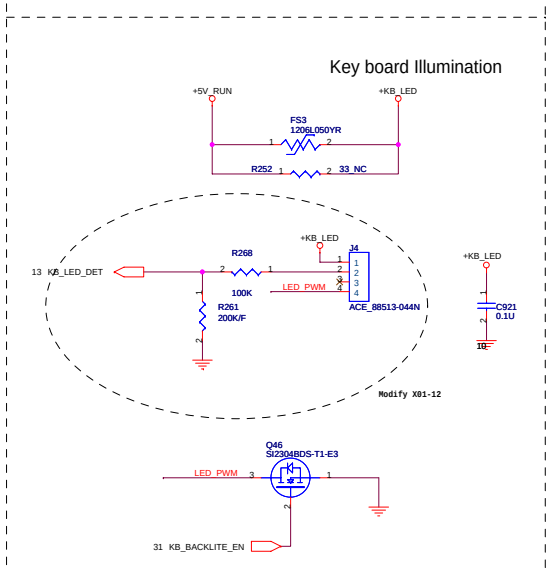

QUANTA COMPUTER			
Title: TOUCH PAD, BULE TOOTH & FIR			
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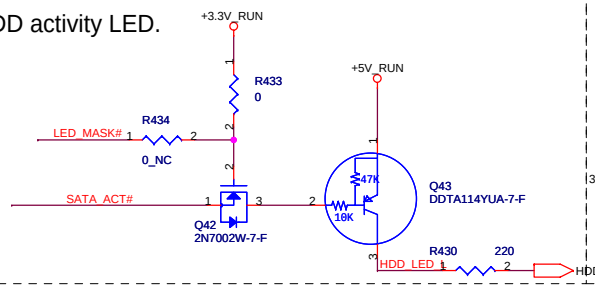
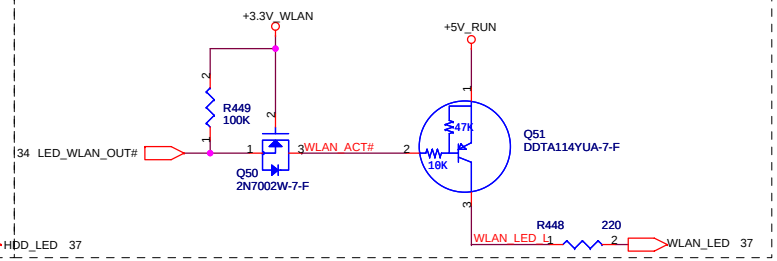
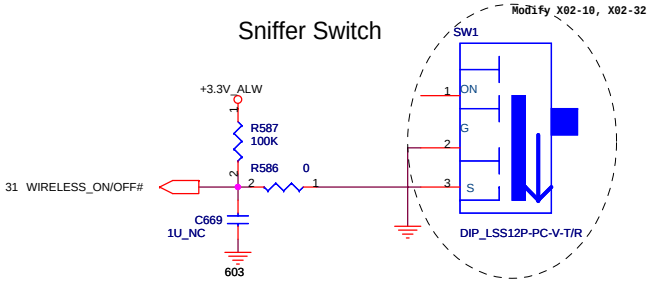
HDD activity LED.



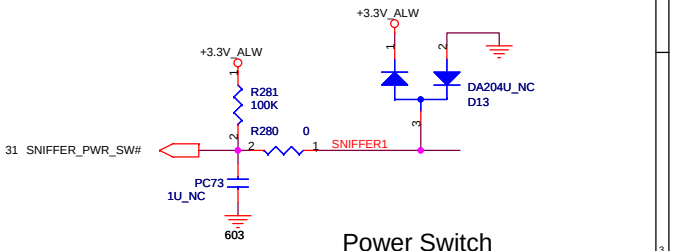
WLAN



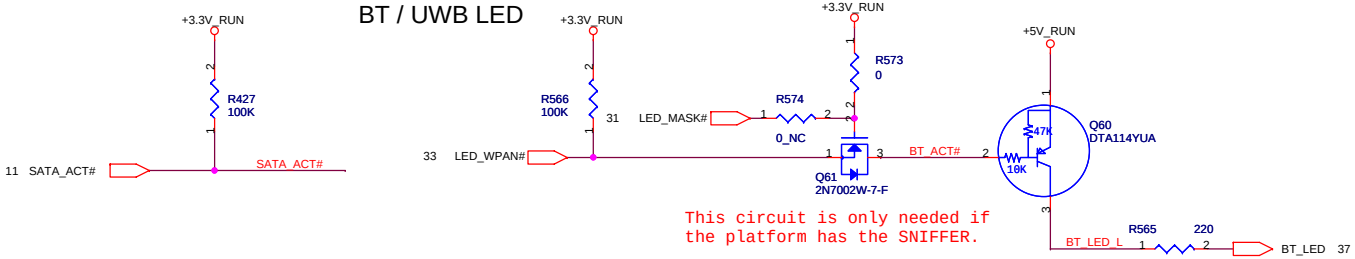
Sniffer Switch



Sniffer Switch ON/OFF

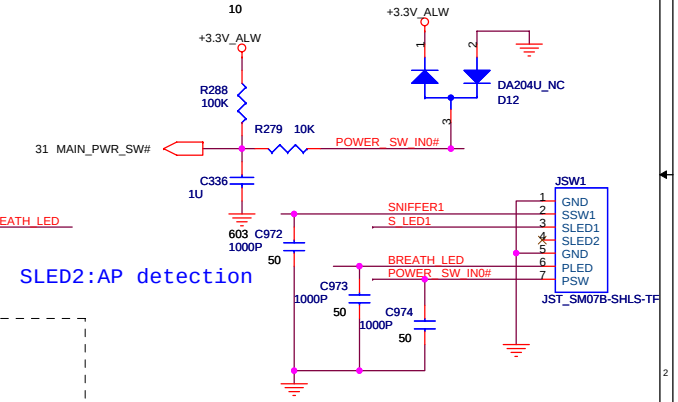


BT / UWB LED



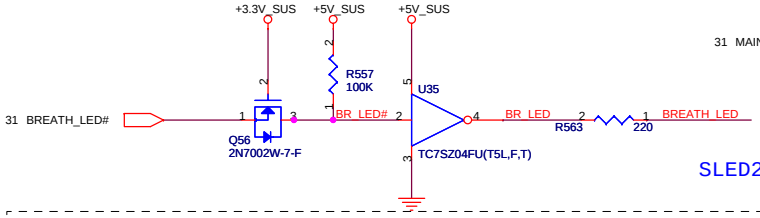
This circuit is only needed if the platform has the SNIFFER.

Power Switch

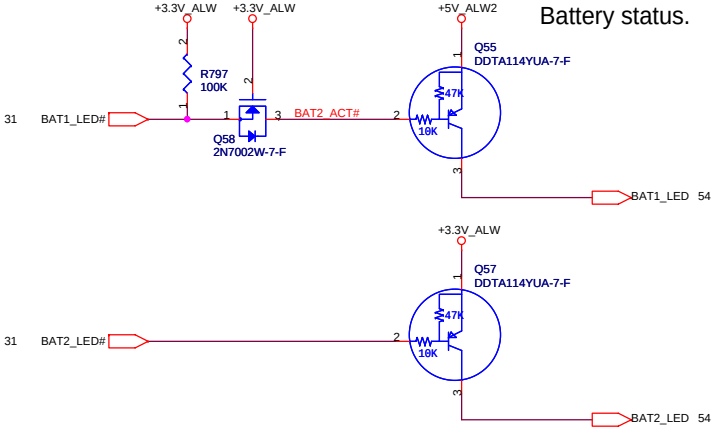


SLED2:AP detection

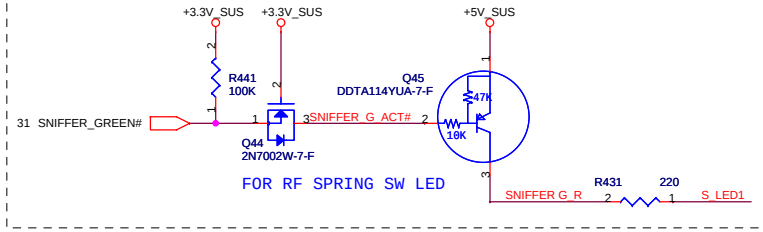
Power & Suspend.



Battery status.

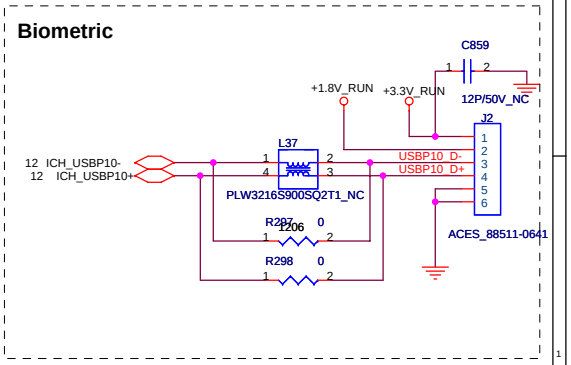


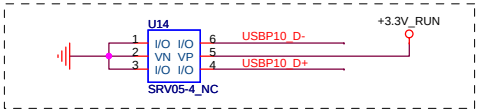
Sniffer LED



FOR RF SPRING SW LED

Biometric





QUANTA COMPUTER

Title	SWITCH, KEYBOARD & LED	
Size	Document Number GM5	Rev B2A
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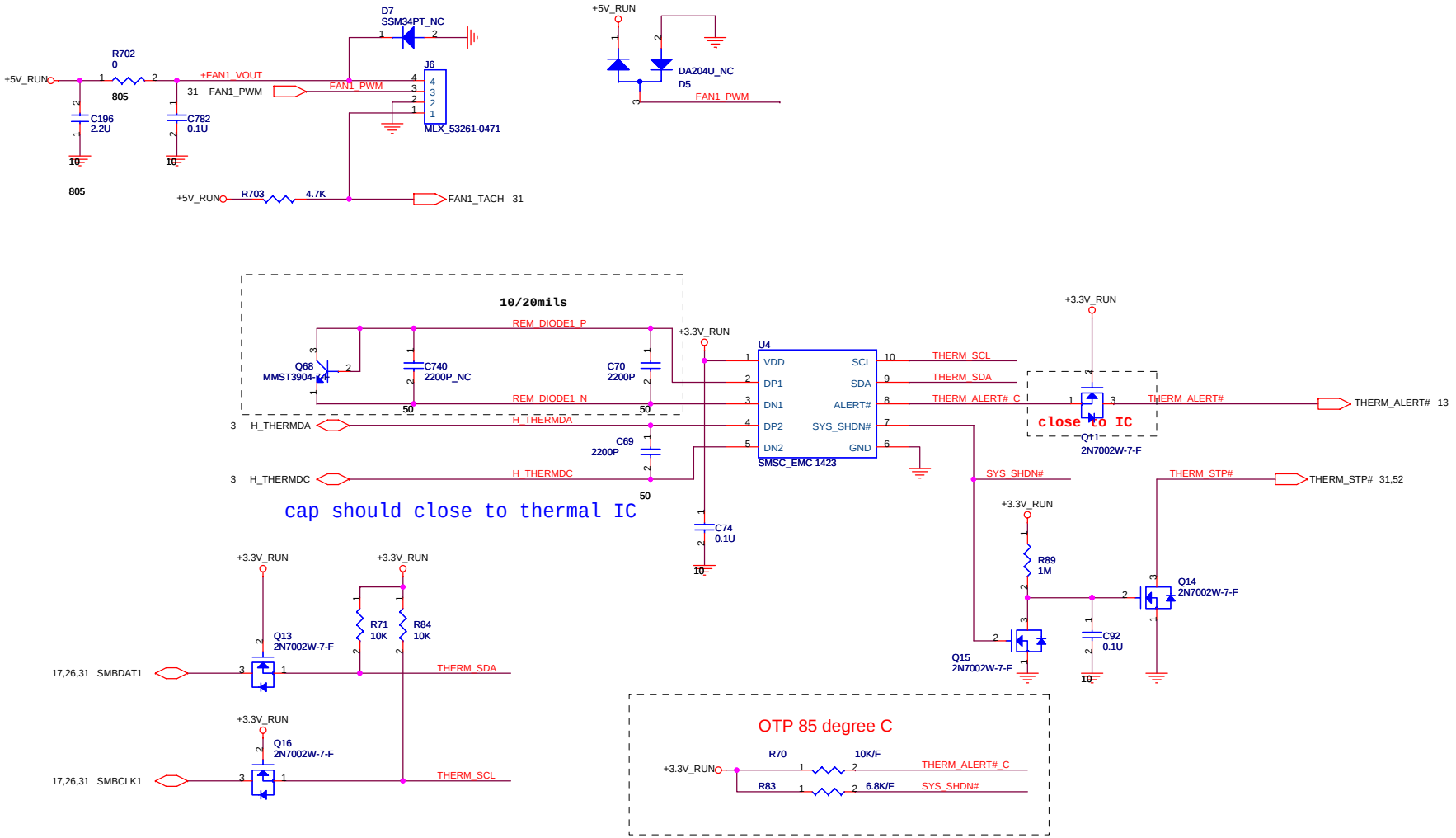

QUANTA COMPUTER		
Title	FAN & THERMAL	
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GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

INTERNAL SPEAKER AMP

TPA6040A4
QFN 32PIN

Layout Note:
Place close U23 pin 23.

Layout Note:
Close to U1 Pin 34

Layout Note:
Place close to pin 18.

Layout Note:
Place close U23

AZALIA (HD) CODEC

FB_60ohm+-25%_100MHz
_3A_0.05ohm DC

Layout Note:
Close to U1 Pin 13

R71,R69 close to U1, Let DVDD width be 10-mils

Layout Note:
Place close to pin 8.

IDT_92HD73C1X5PRGXC1X

Modify X02-26

Modify X01-28

Modify X02-14

Title	Azelia CODEC
Size	Document Number: GM5
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QUANTA COMPUTER

Headphone Jack
Stereo MIC Jack

Array Microphone & Camera

+3.3V_RUN
R289 100K
CAMERA_CBL_DET#

JCAMERA1
USBP11_D+
USBP11_D-
+3.3V_CCD
40 DMIC_DATA — L36 0 603 DMIC_DATA_R
40 DMIC_CLK — L35 22 603 DMIC_CLK_R
13 CAMERA_CBL_DET# — CAMERA_CBL_DET#
I-pex 20374-010E-31

+3.3V_CCD trace width
use 25 mils

DMIC_DATA — C358 33P_NC 50
L41 BLM18AG121SN1D 603
+3.3V_RUN — +3.3V_CCD
C373 10U 805 10
C364 10U 805 10
DMIC_CLK — C357 33P_NC 50

12 ICH_USBP11- / 12 ICH_USBP11+ — L46 EXC24CG900U_NC — USBP11_D- / USBP11_D+
R312 1206 0
R313 0

R419 100K — MIC1_JD
+3.3V_RUN
R414 100K — HP2_JD
R412 100K — HP1_JD
100K

JACK 2 (MIC)
JACK 1 (HP2)
JACK 3 (HP)

JAUDIO1
40 AUD_MIC1_VREFO
40 AUD_MIC_L
40 AUD_MIC_R
40 AUD_HP2_L1
40 AUD_HP2_R1
AUD_HP1_L1
AUD_HP1_R1
40 MIC1_JD — MIC1_JD
40 HP2_JD — HP2_JD
40 HP1_JD — HP1_JD
MLE_48227-1501

40 AUD_HP1_L — C567 1206 2.2U 50 — AUD_HP1_L_R — R9997 2.2K — AUD_HP1_L0 — C4943 50 220P
40 AUD_HP1_R — C586 1206 2.2U 50 — AUD_HP1_R_R — R9998 2.2K — AUD_HP1_R0 — C4944 220P 50

U29 MAX4411ETP
AUD_HP1_L0
AUD_HP1_R0
40 AMP_HP1_SHUD# — SHDNR / SHDNL
C578 1206 2.2U 25 — C1P / C1N
PVSS / SVSS
C556 2.2U 1206 10
OUTL — AUD_HP1_L1
OUTR — AUD_HP1_R1
NC1 NC2 NC3 NC4 NC5 NC6
SVDD — +3.3V_RUN
PVDD
PGND
SGND
C557 1U 805 16

+VDDA
R584 100K
U51A LM358ADR2G
Modify X02-33
R581 1K
C665 2.2U 805 10
R835 100K
JP11 FOX_HS8102E
INT_MIC_C_L+ — C664 2.2U 805 10 — R580 1K
INT_MIC_2_L+
INT_MIC_2_L-
C962 0.1U 603 16 — INT_MIC_L1+ — R832 10K — INT_MIC_L0+
C963 0.1U 603 16 — INT_MIC_L1- — R833 10K — INT_MIC_L0-
R583 1K
INT_MIC_C_L- — C668 2.2U 805 10 — R582 1K
D22 SM05_NC
Layout Note:
Place close to CODEC.
+VDDA
C971 0.1U 10
U51B LM358ADR2G
INT_MIC_IN_OP — C970 0.1U 603 16 — AUD_INT_MIC_IN 40
R837 100K

QUANTA COMPUTER

Title	AUDIO CONN	
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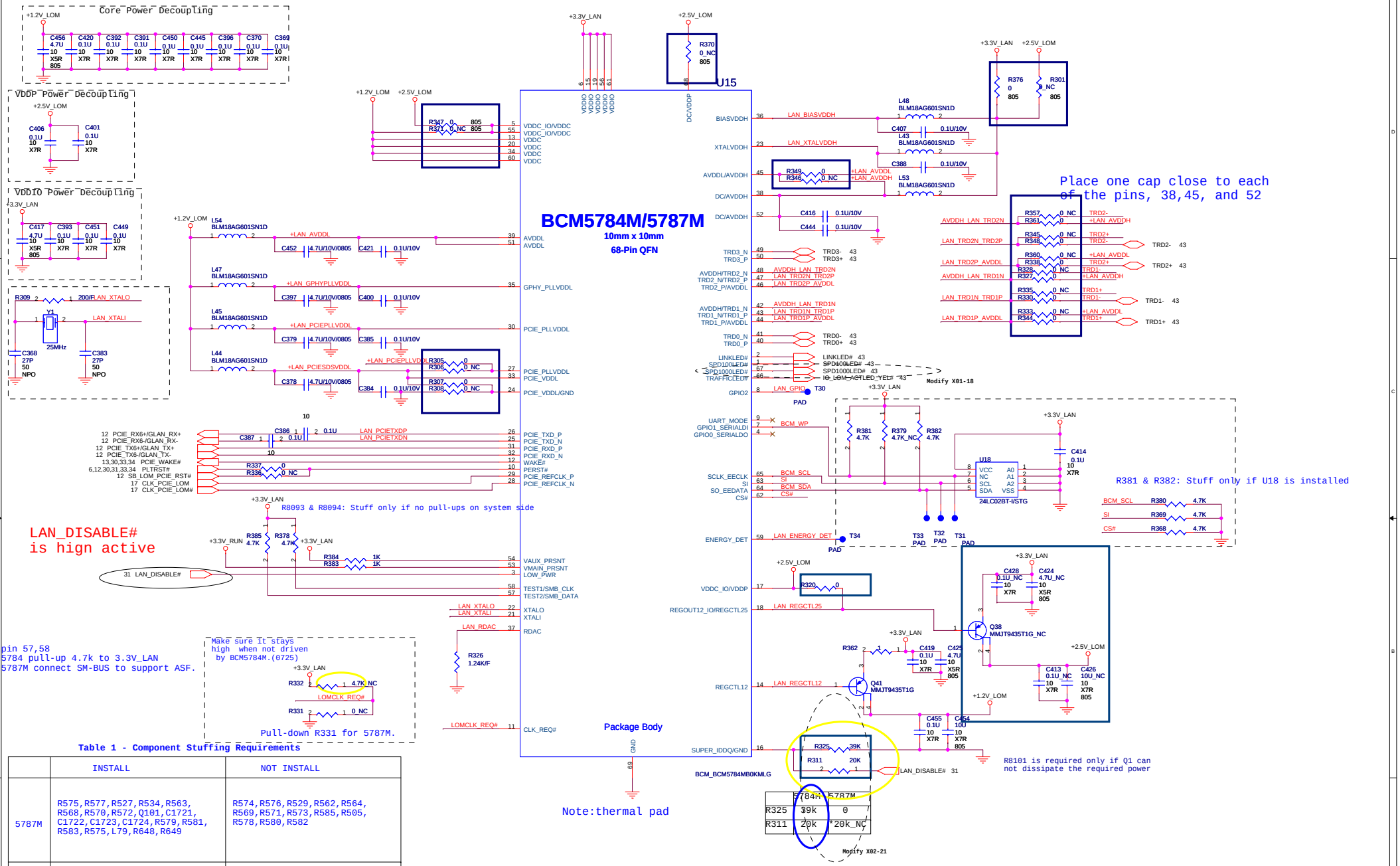

Table 1 - Component Stuffing Requirements

	INSTALL	NOT INSTALL
5787M	R575,R577,R527,R534,R563, R568,R570,R572,Q101,C1721, C1722,C1723,C1724,R579,R581, R583,R575,L79,R648,R649	R574,R576,R529,R562,R564, R569,R571,R573,R585,R505, R578,R580,R582
5784	R574,R576,R529,R562,R564, R569,R571,R573,R585,R505, R578,R580,R582	R575,R577,R527,R534,R563, R568,R570,R572,Q101,C1721, C1722,C1723,C1724,R579,R581, R583,R575,L79,R648,R649

	5784M	5787M
R325	39k	0
R311	20k	*20k_NC

QUANTA COMPUTER

Title	LAN	
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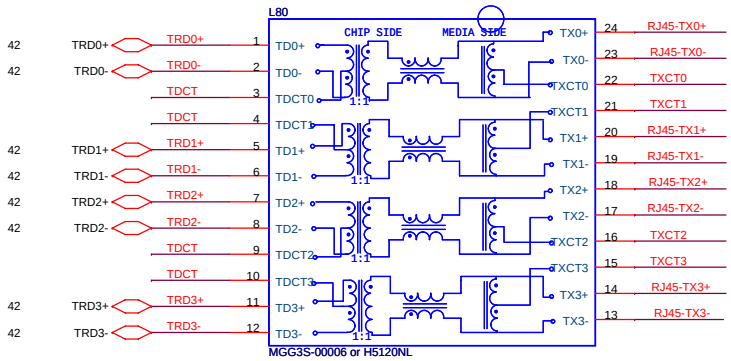
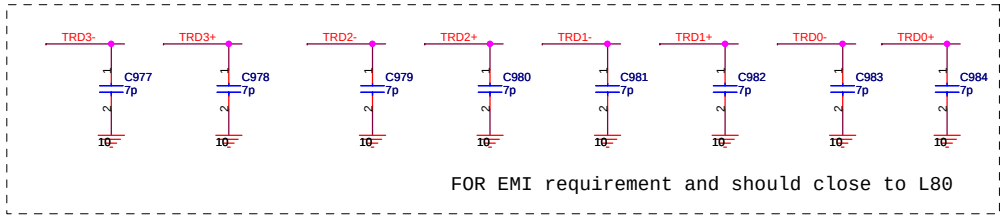
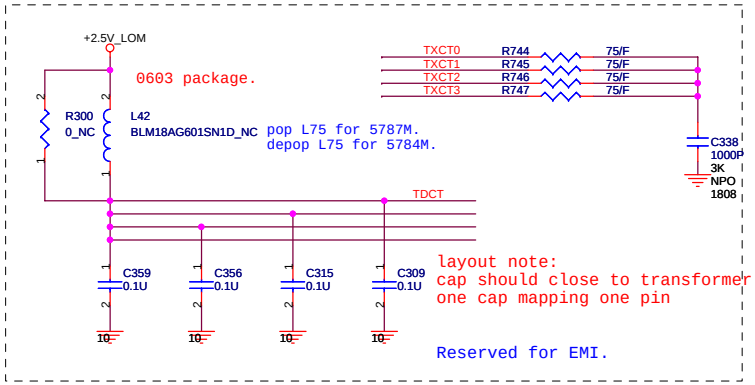
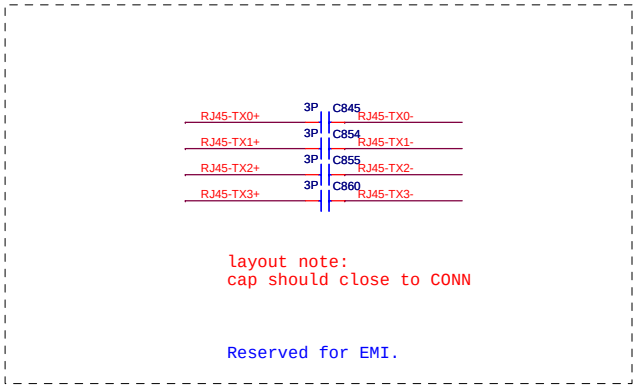
RJ-45 Connector

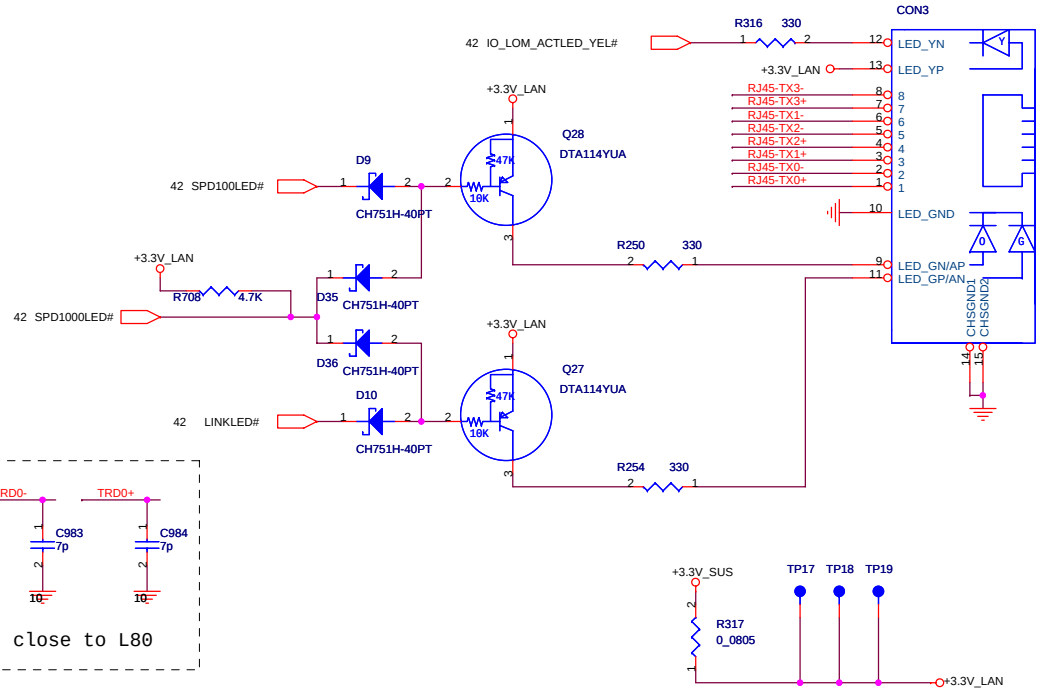
TRANSFORM



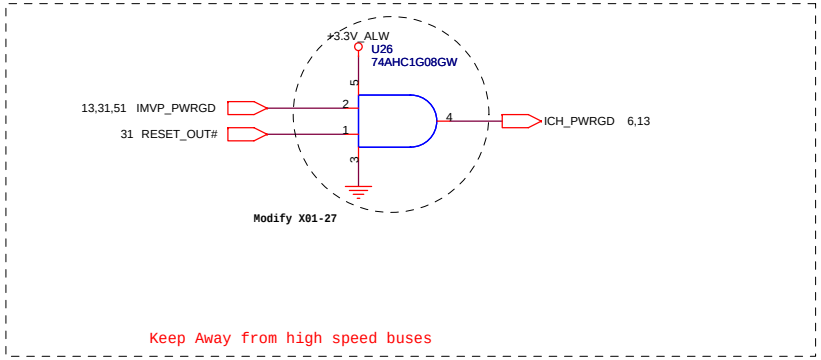


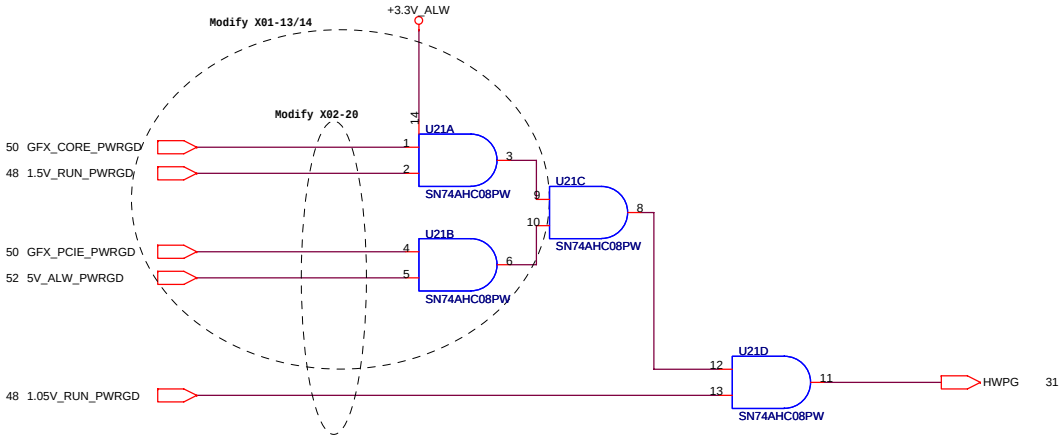


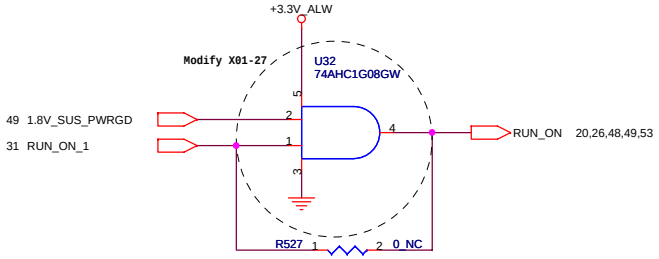


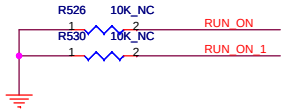


QUANTA COMPUTER			
Title	LAN SWITCH		
Size	Document Number GM5		Rev B2A
Date:	Wednesday, June 25, 2008	Sheet 43 of 62	









QUANTA COMPUTER

Title	System Reset Circuit	
Size	Document Number GM5	Rev B2A
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TH1
H-C394D126P2

TH2
H-TC276BC236D126P2

TH3
H-TC276BC236D126P2

TH4
H-TC394BC315D126P2

TH5
H-TC394BC315D126P2

TH6
H-C256D130P2

TH7
H-TC276BC354D126P2

TH8
H-TC394BC276D126P2

TH9
h-c315d189p2

TH10
H-C315D157I197P2

TH11
H-C315D157I197P2

TH12
H-C315D126P2

TH13
H-C256D126P2

TH14
H-C433D433N

TH15
H-C276D126P2

TH16
H-TC394BC236D126P2

TH17
H-C315D157I197P2

TH18
H-C315D157I197P2

TH19
H-TC276BC236D110P2

TH20
H-C315D157I197P2

TH23
H-TC197BC236D65P2

TH24
H-TC197BC236D65P2

TH25
H-TC197BC236D104P2

TH26
H-TC197BC236D65P2

TH27
H-TC197BC236D104P2

TH28
H-TC197BC236D65P2

TH29
H-TC275BC492D110P2

TH30
H-TC394BC315D126P2

TH31
h-tr8x9bc276d126p2

TH33
H-C118D118N

TH34
h-c236d110p2

TH35
h-c236d110p2

TH32
h-o71x118d31x78p2

TH36
h-o71x118d31x78p2

QUANTA COMPUTER

Title	Battery Selector	
Size	Document Number GM3	Rev B2A
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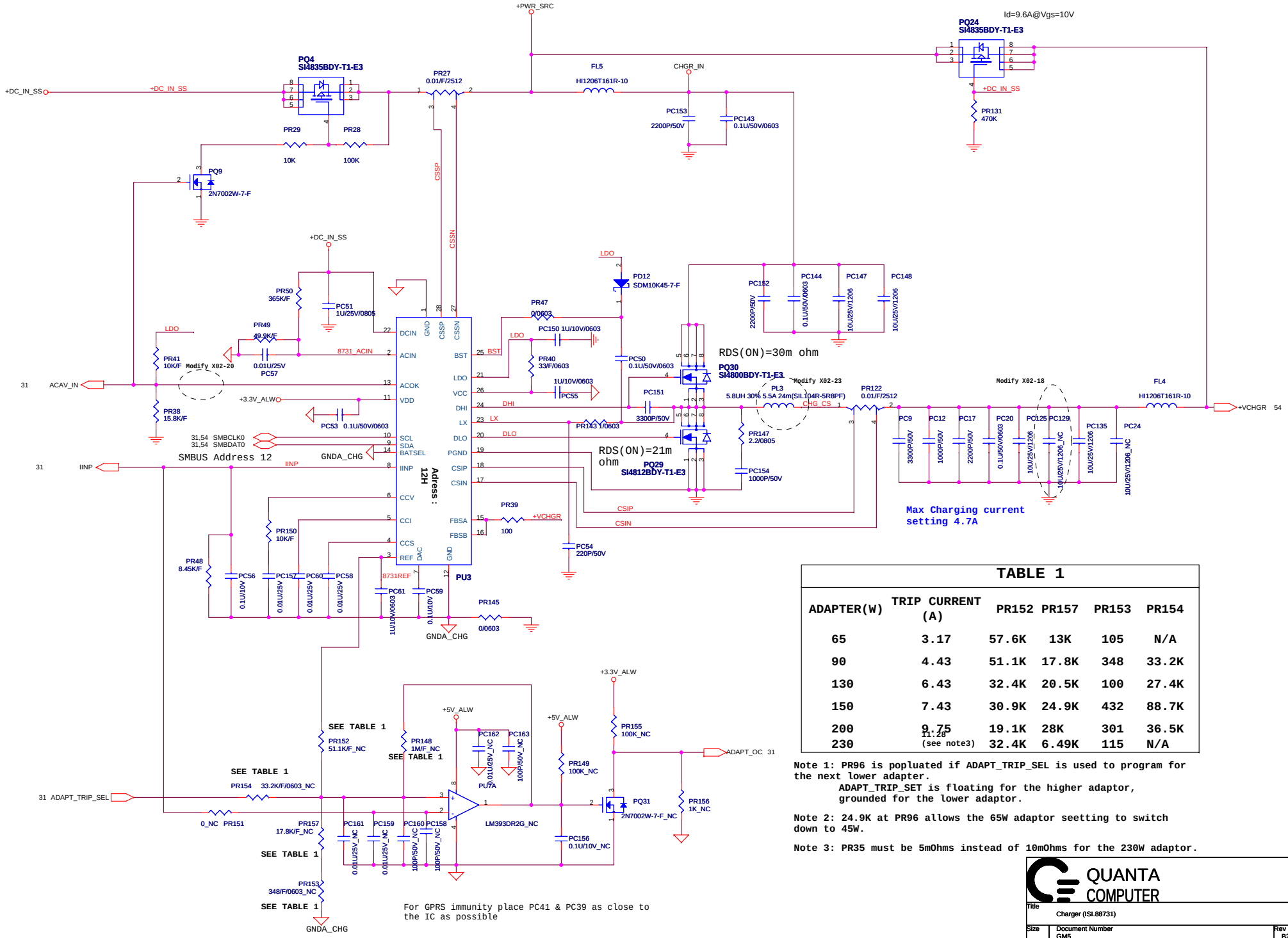

TABLE 1

ADAPTER(W)	TRIP CURRENT (A)	PR152	PR157	PR153	PR154
65	3.17	57.6K	13K	105	N/A
90	4.43	51.1K	17.8K	348	33.2K
130	6.43	32.4K	20.5K	100	27.4K
150	7.43	30.9K	24.9K	432	88.7K
200	9.75	19.1K	28K	301	36.5K
230	11.28 (see note3)	32.4K	6.49K	115	N/A

Note 1: PR96 is popluated if ADAPT_TRIP_SEL is used to program for the next lower adapter.
ADAPT_TRIP_SET is floating for the higher adaptor, grounded for the lower adaptor.

Note 2: 24.9K at PR96 allows the 65W adaptor seetting to switch down to 45W.

Note 3: PR35 must be 5mOhms instead of 10mOhms for the 230W adaptor.

QUANTA COMPUTER

Title	Charger (ISL88731)	
Size	Document Number GM5	Rev B2A
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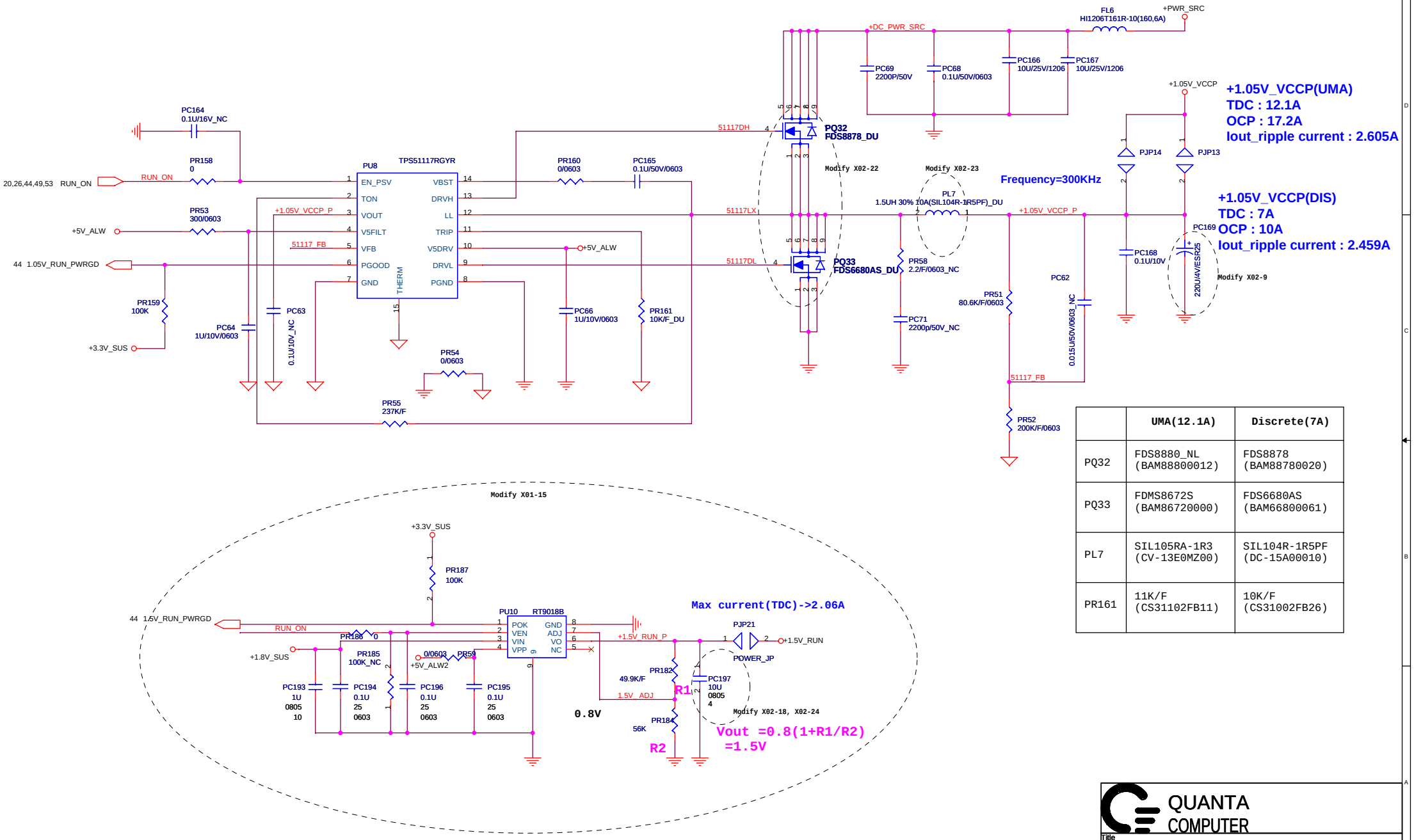
QUANTA COMPUTER

Title		
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 47 of 62	



	UMA(12.1A)	Discrete(7A)
PQ32	FDS8880_NL (BAM88800012)	FDS8878 (BAM88780020)
PQ33	FDMS8672S (BAM86720000)	FDS6680AS (BAM66800061)
PL7	SIL105RA-1R3 (CV-13E0MZ00)	SIL104R-1R5PF (DC-15A00010)
PR161	11K/F (CS31102FB11)	10K/F (CS31002FB26)

QUANTA COMPUTER

Title		
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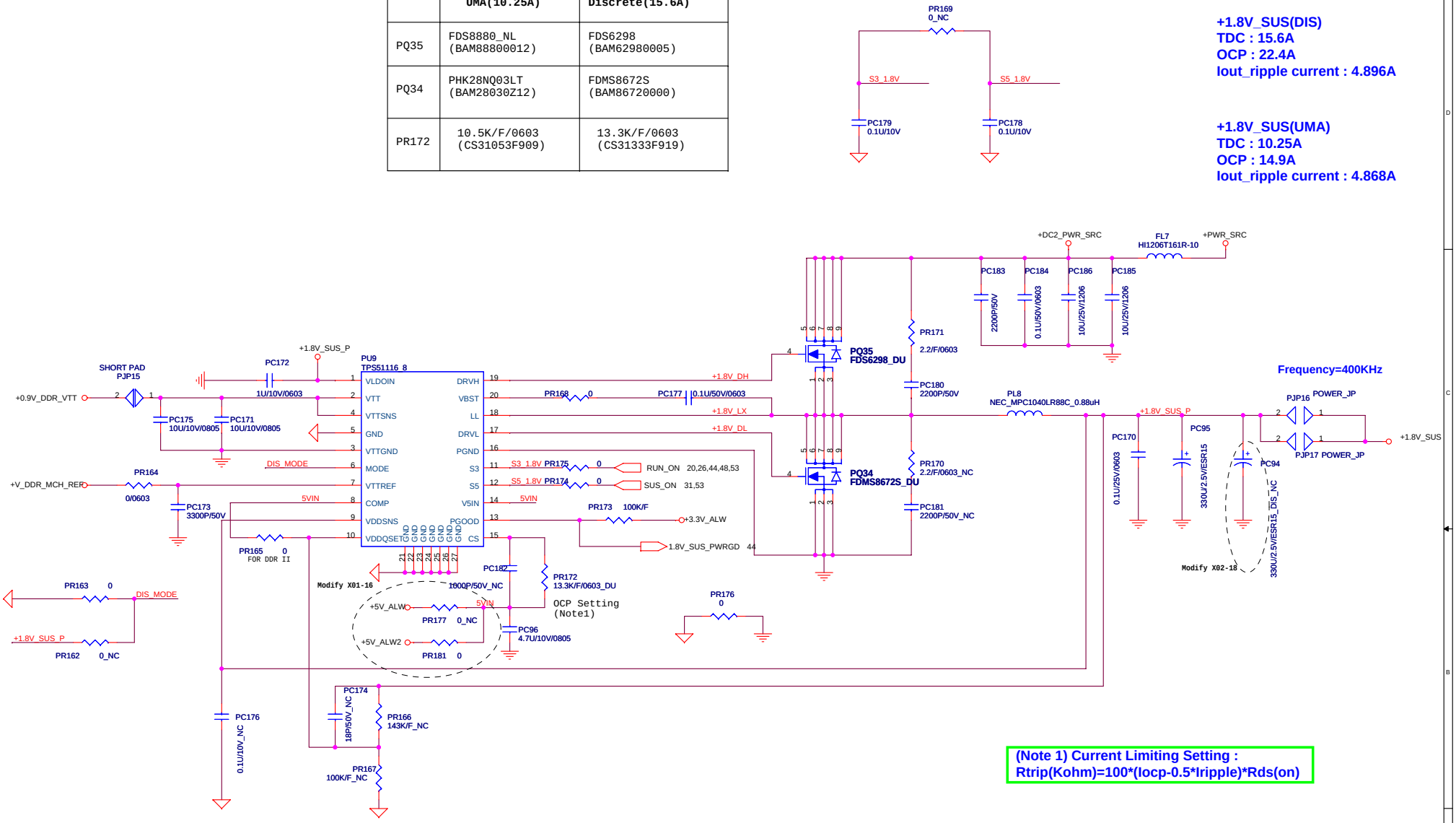
	UMA(10.25A)	Discrete(15.6A)
PQ35	FDS8880_NL (BAM88800012)	FDS6298 (BAM62980005)
PQ34	PHK28NQ03LT (BAM28030Z12)	FDMS8672S (BAM86720000)
PR172	10.5K/F/0603 (CS31053F909)	13.3K/F/0603 (CS31333F919)

+1.8V_SUS(DIS)
TDC : 15.6A
OCP : 22.4A
Iout_ripple current : 4.896A

+1.8V_SUS(UMA)
TDC : 10.25A
OCP : 14.9A
Iout_ripple current : 4.868A



(Note 1) Current Limiting Setting :
Rtrip(Kohm)=100*(Iocp-0.5*Iripple)*Rds(on)

QUANTA COMPUTER

Title	1.8VSUS & 0.9VTT (TPS51116)	
Size	Document Number GM5	Rev B2A
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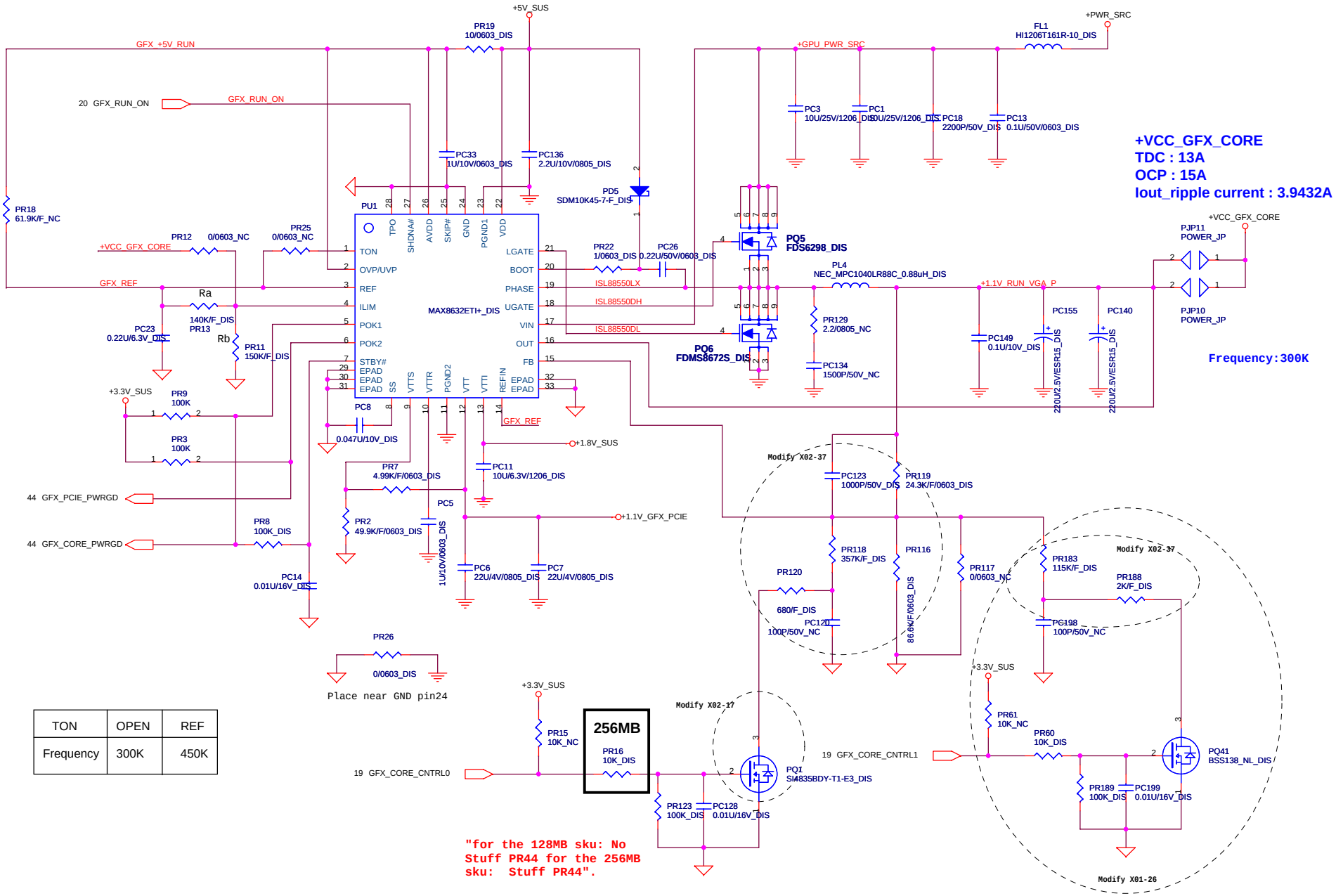

TON	OPEN	REF
Frequency	300K	450K

ILIM	Iovp=(2*(Rb/(Ra+Rb))*0.1*(1/RDSON)+(I_DELTA/2)
SKIP#	AVDD = Low-noise, forced-PWM mode. GND = Pulse-skipping operation.
OVP/UVP	The overvoltage limit is 116% of Vout. The undervoltage limit is 70% of Vout.

GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	+VCC_GFX_CORE
LOW	LOW	0.9V
HIGH	LOW	0.95V
HIGH	HIGH	1.1V

QUANTA COMPUTER

Title	VGA DC/DC	
Size	Document Number GM5	Rev B2A
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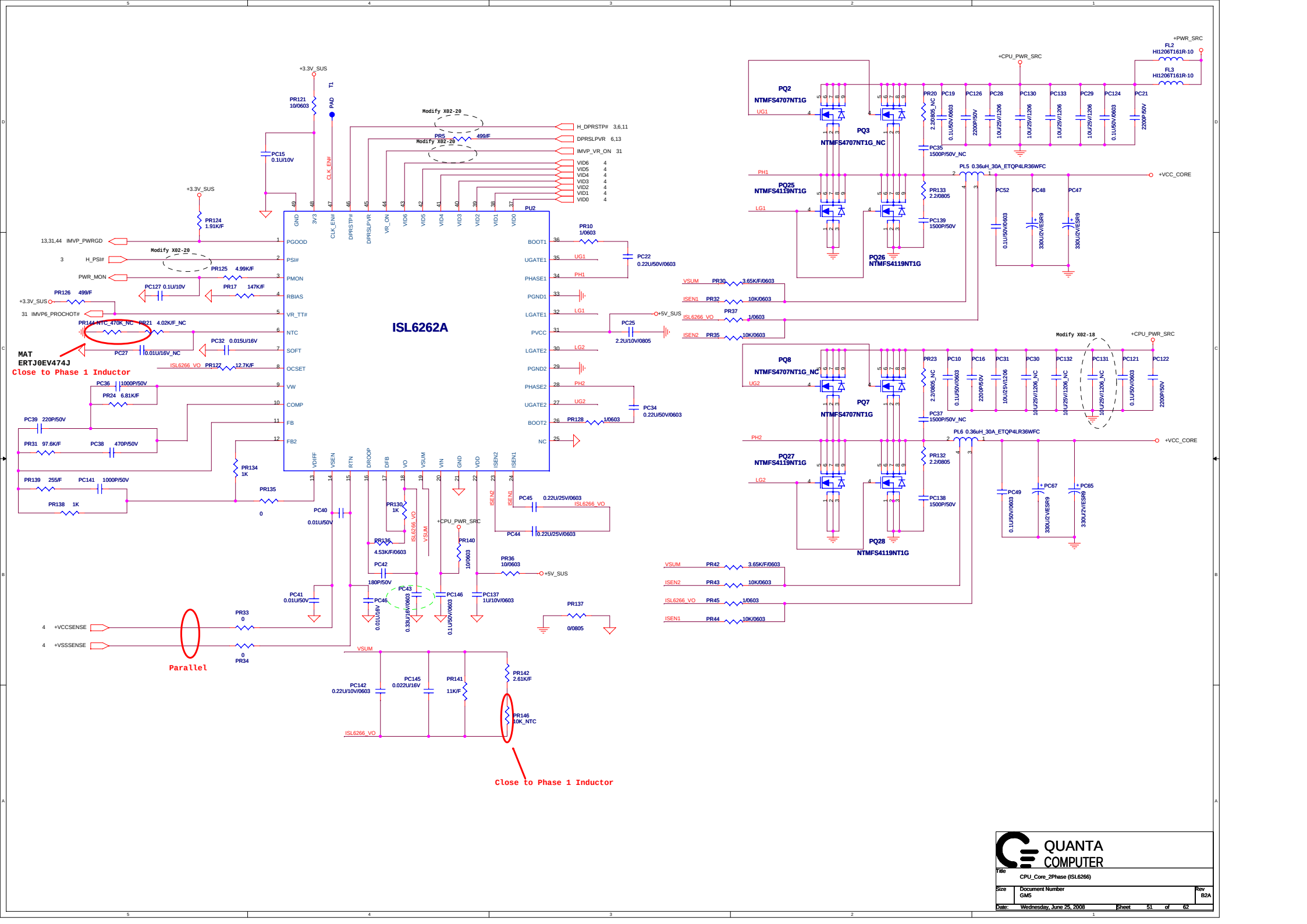

Title	CPU_Core_2Phase (ISL6266)		
Size	Document Number GM5		Rev B2A
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QUANTA COMPUTER

DC/DC +3V_ALW/+5V_SUS/+5V_ALW /+15V_ALW

+5V_ALW
TDC : 7.25A
OCP : 9.8A
Iout_ripple current : 2.84A

Frequency=400KHz

+3.3V_ALW
TDC : 6.2A
OCP : 8.6A
Iout_ripple current : 2.78A

Frequency=300KHz

Place these CAPs close to FETs

Place these CAPs close to FETs

No Install for ISL6236
Install 10 ohm for MAX8778

Modify X01-17

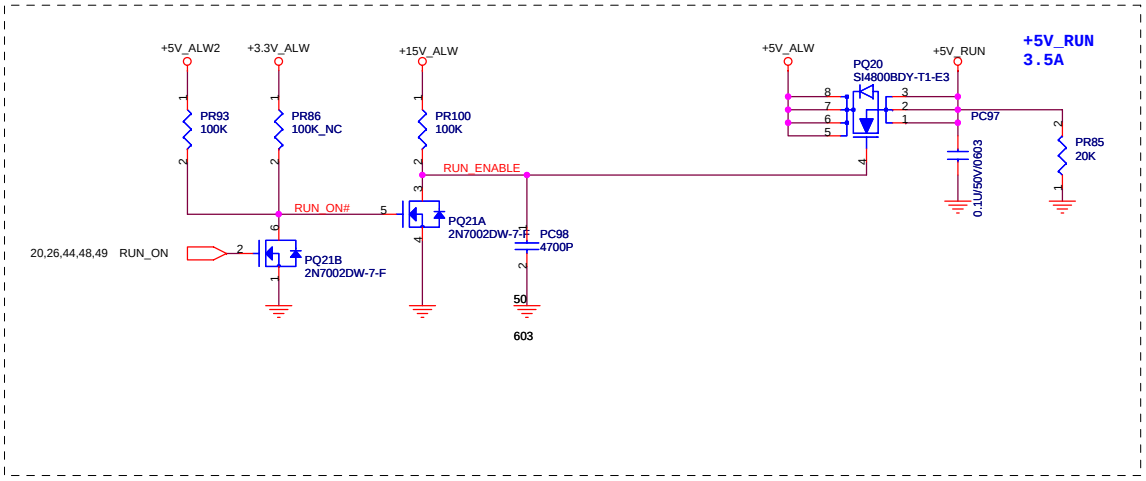
Modify X01-30

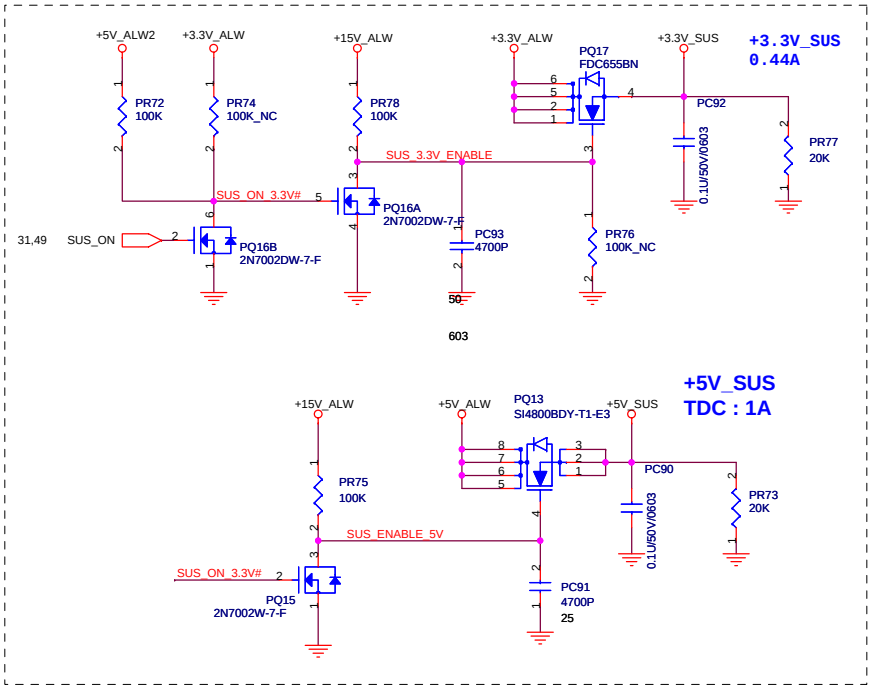
Modify X02-33

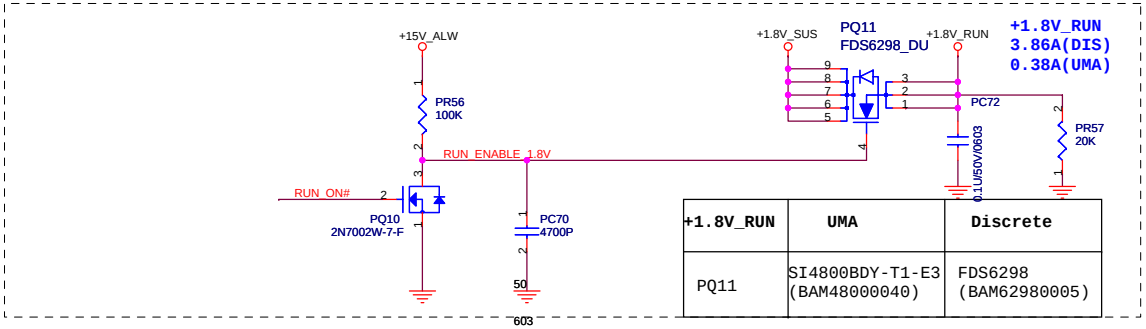
Modify X02-20

Modify X01-20 , X02-36

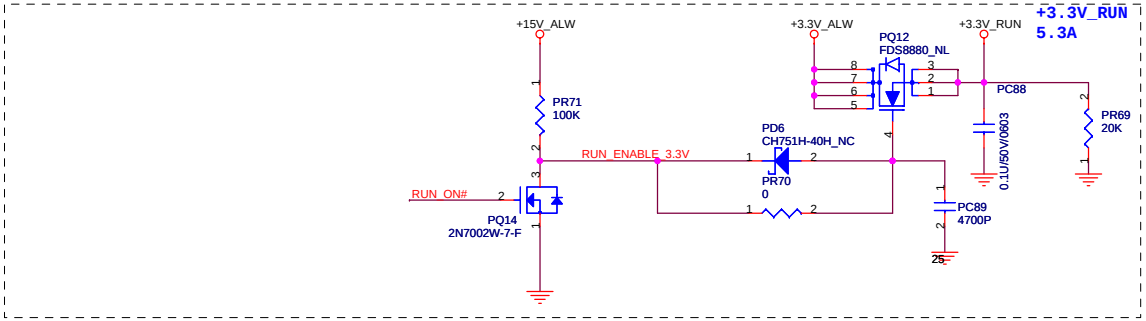
Title	VGA DC/DC		
Size	Document Number GM5		Rev B2A
Date:	Wednesday, June 25, 2008	Sheet 52 of 62	

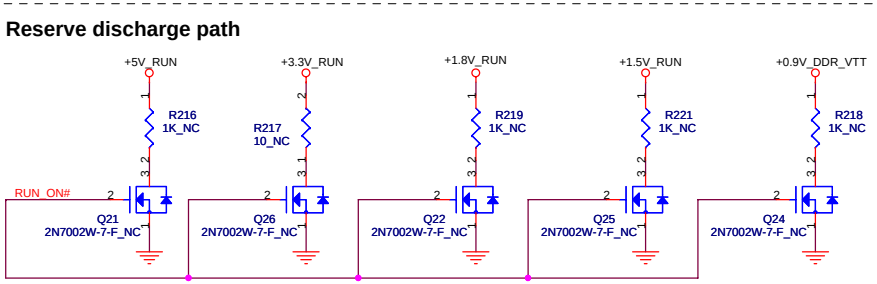


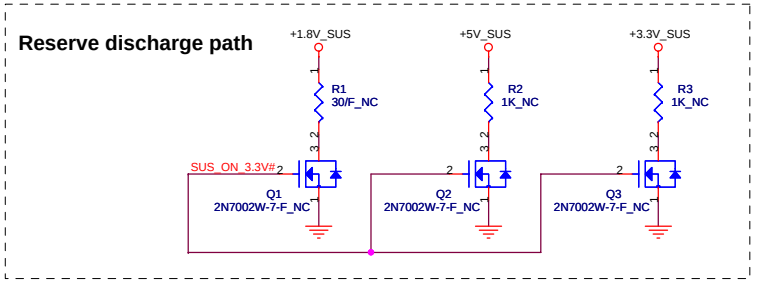




+1.8V_RUN	UMA	Discrete
PQ11	SI4800BDY-T1-E3 (BAM48000040)	FDS6298 (BAM62980005)

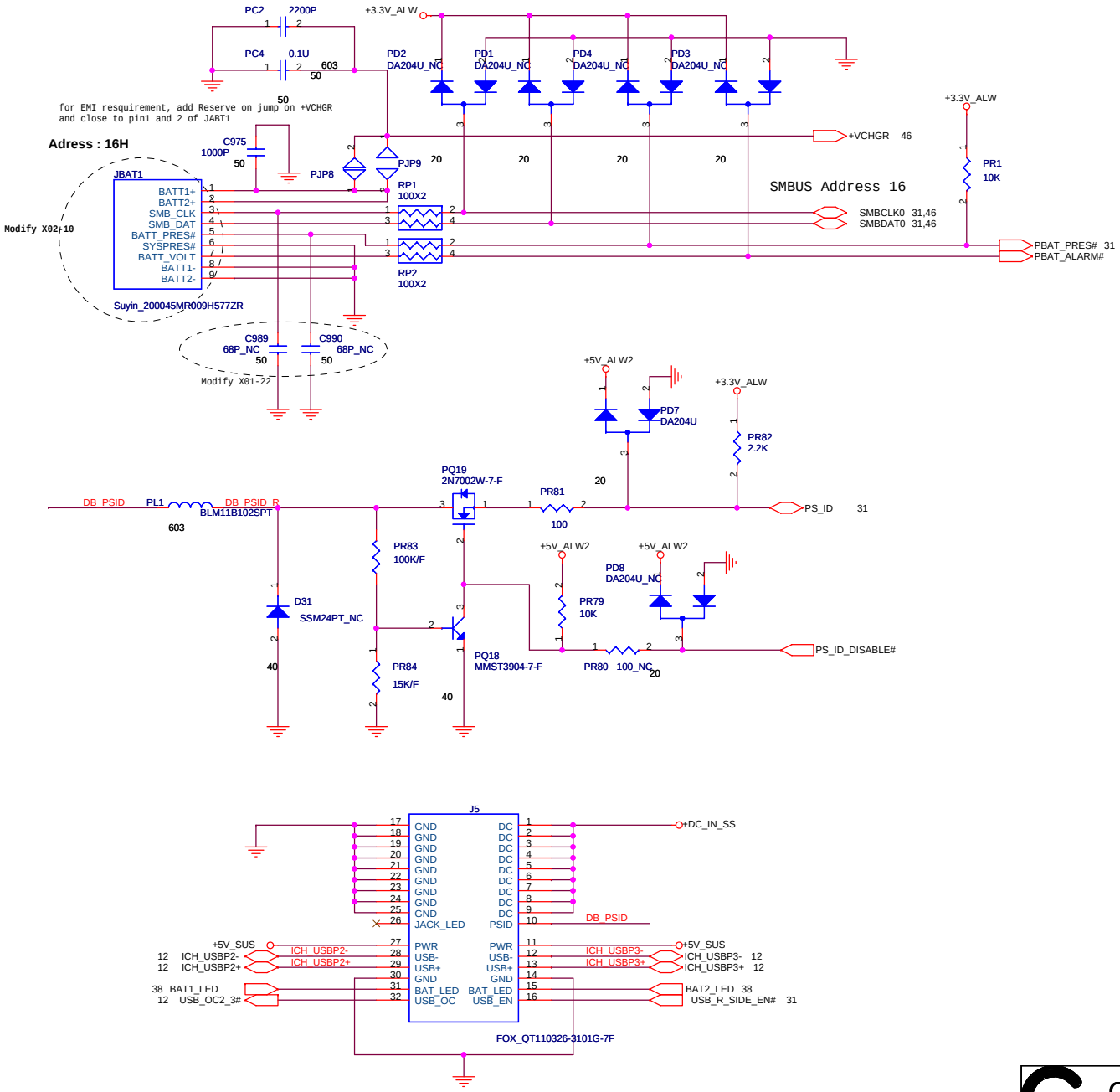






QUANTA COMPUTER

Title	RUN POWER SW	
Size	Document Number GM5	Rev B2A
Date: Wednesday, June 25, 2008	Sheet 53 of 62	



QUANTA COMPUTER

Title	DCIN,BATT CONNECTOR	
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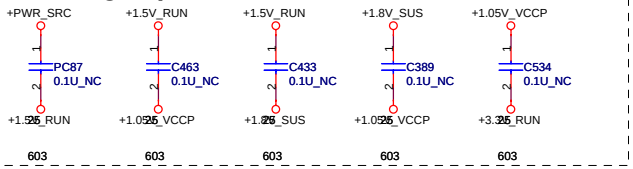
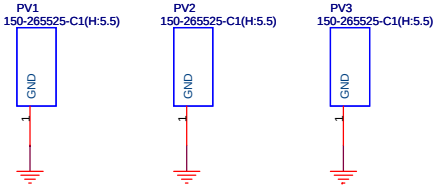
Reserved for EMI.

Stitching caps





Page 26
SATA (HDD&CD_ROM)

Page 27
PCCARD /CONN

Page 31
SIO(MEC5025)

Page 38
Azelia CODEC

Page 40
LAN(BCM5755M)

Page 48
1.5VRUN,1.05V(VTT)

Page 49
1.25V,1.8V,0.9V

Page 51
CPU_MAX8786(3phase)

Page 52
D/D Power

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Title	EMI CAP	
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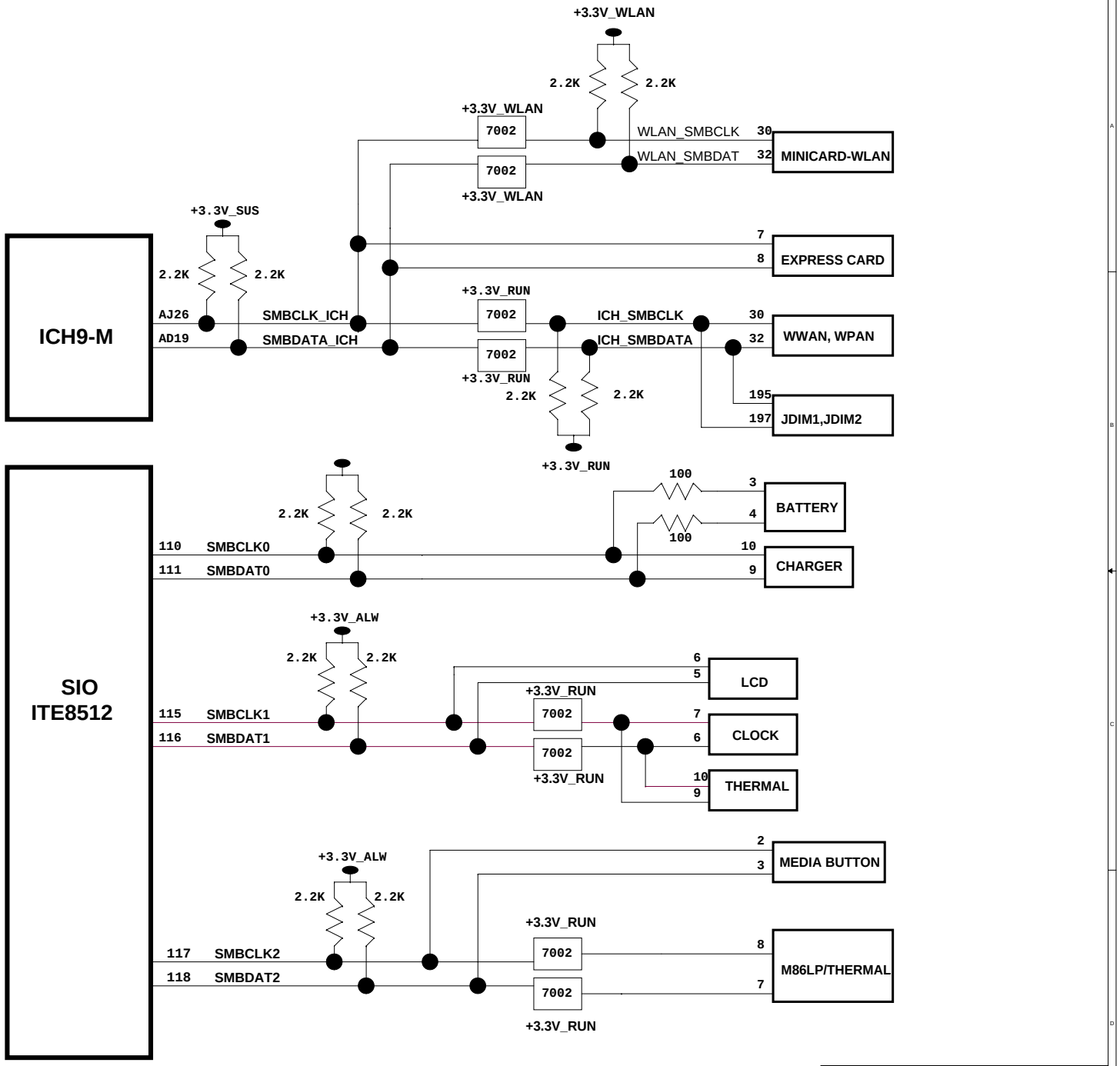

QUANTA COMPUTER

Title	SMBUS BLOCK	
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POWER STATES

State \ Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0	HIGH	HIGH	HIGH					
S3 (Suspend to RAM) / M1	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M1	LOW	HIGH	HIGH					
S5 (SOFT OFF) / M1	LOW	HIGH	LOW					
S3 (Suspend to RAM) / M-OFF	LOW	HIGH	HIGH					
S4 (Suspend to DISK) / M-OFF	LOW	LOW	HIGH					
S5 (SOFT OFF) / M-OFF	LOW	LOW	LOW					

PM TABLE

State \ power plane	+3.3V_ALW +3.3V_RTC_LDO +3.3V_WLAN +5V_ALW +15V_ALW	+1.8V_SUS +1.8V_LOM +3.3V_LAN +3.3V_SUS +5V_SUS	+0.9V_DDR_VTT +1.05V_VCCP +1.25V_RUN +1.5V_CARD +1.5V_RUN +3.3V_CARD +3.3V_CARDAUX +3.3V_R5C832 +3.3V_RUN	+3.3V_RUN_CARD +2.5V_RUN +5V_MOD +5V_RUN +5V_SPK_AMP +CPU_PWR_SRC +VCC_CORE +VDDA	+DC_IN +DC_IN_SS +PWR_SRC +RTC_CELL
S0	ON	ON	ON		ON
S3	ON	ON	OFF		ON
S5 S4/AC	ON	OFF	OFF		ON
S5 S4/AC don't exist	OFF	OFF	OFF		ON

PCI TABLE

PCI DEVICE	IDSEL	REQ#/GNT#	PIRQ
R5C833	AD17	REQ#0 / GNT#0	PIRQB: 1394 PIEQD: Card reader

	USB PORT#	DESTINATION
ICH9-M	0	Side pair Top / left
	1	Side pair bottom / left
	2	Side pair top/right(DB)
	3	Side pair Bot right(DB)
	4	WLAN
	5	Mini Card (WWAN)
	6	Mini Card (WPAN)
	7	Express Card
	8	USB W/ E-SATA port
	9	Reserved
	10	Biometric
	11	Camera
ECE 5011	1	None
	2	None
	3	None
	4	None

PCI EXPRESS	DESTINATION
Lane 1	MINI CARD-1 WWAN
Lane 2	MINI CARD-2 WLAN
Lane 3	MINI CARD-3 WPAN
Lane 4	Express Card
Lane 5	None
Lane 6	None

QUANTA COMPUTER

Title	Schematic Block Diagram1	
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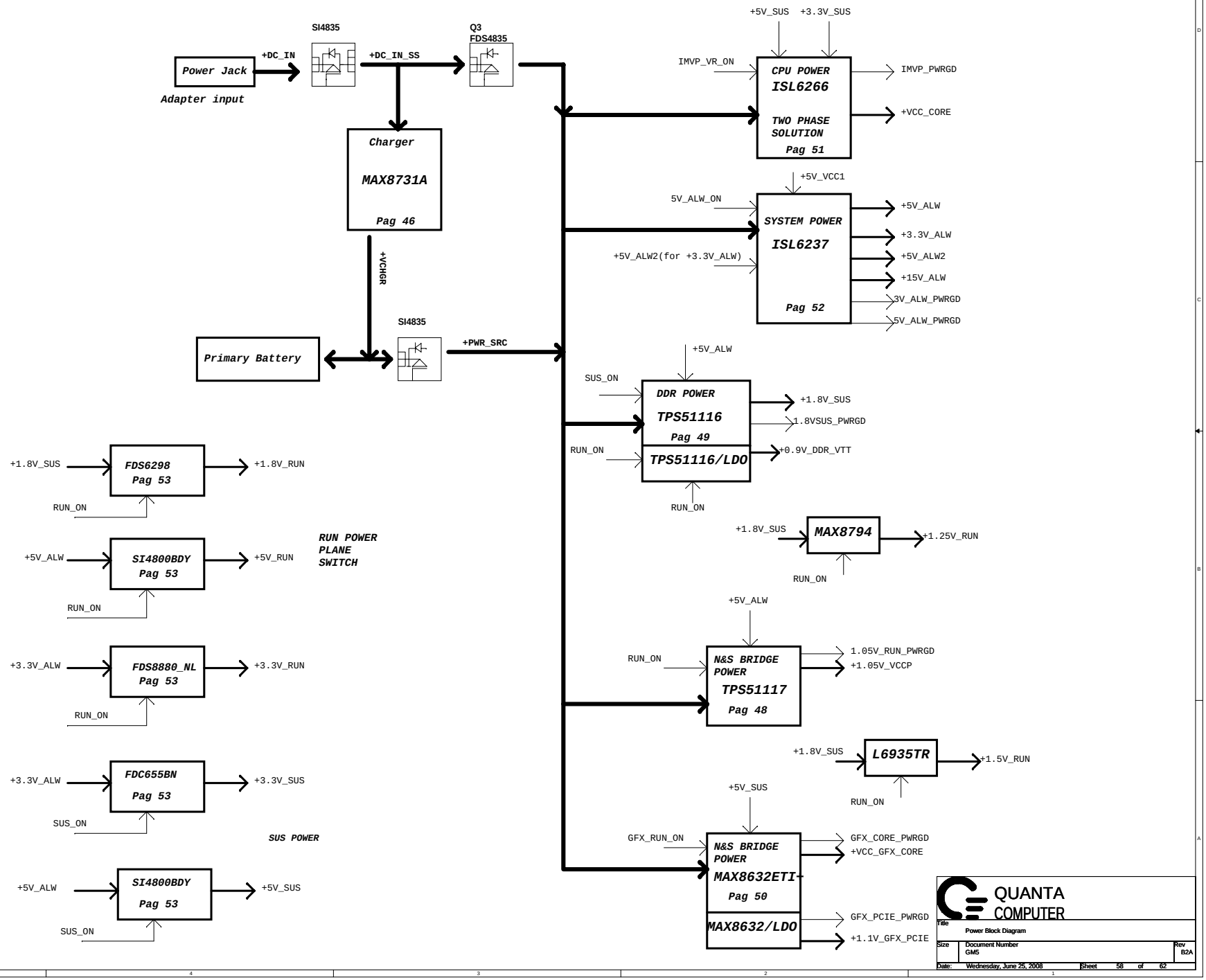
GM3 Power Design Block Diagram
2007/09/06



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Title	Power Block Diagram	
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Pacino MV of Intel					

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Model	Item	Page	Date	Rev.	Description
Pacino MV of Intel	1	03	4/8 2008	B2A	Change R134 value 56 Ohm met intel design guide line
	2	03	4/8 2008	B2A	Del Q69,R693 this CKT is unnecessary
	3	03	4/8 2008	B2A	Modify BSEL table
	4	06	4/8 2008	B2A	Reserved R638,R691,R707 footprint for disable TV-out function on UMA board
	5	06	4/8 2008	B2A	NC R243,R214,R255 to met NB configuration setting
	6	06	4/8 2008	B2A	Del R261 prevent back driver(from +5V_ALW2 to +1.05_VCCP when R261 stuffed)
	7	06	4/8 2008	B2A	Changed R635,R462 BOM setting for DIS board boot fail
	8	09	4/8 2008	B2A	Changed L34,L77,C250,C793,C191,C236,C792,R223,R171,L13,L15,C188,C243,C237 BOM setting for DIS board boot fail
	9	17	4/8 2008	B2A	Exchange NET 27M_SS and 27M_NSS fixed UMA DREF_SSCLK/DREF_SSCLK# reversed
	10	25	4/8 2008	B2A	Change R671 value from 0 Ohm to 10K Ohm fixed HDMI detect function unstable
	11	31	4/8 2008	B2A	NC C54 fixed ITE8512 ver:J GPIO backdriver during the ITE8512 initial
	12	37	4/8 2008	B2A	Modify J4 pin define prevent FCC burned
	13	44	4/8 2008	B2A	Del R426 .It's unnecessary
	14	44	4/8 2008	B2A	Change net 1.25V_RUN_PWRGD to GFX_CORE_PWRGD, 3V_ALW_PWRGD TO GFX_PCIE_PWRGD
	15	48	4/8 2008	B2A	Change 1.5V_RUN CKT for cost down
	16	49	4/8 2008	B2A	Changed PU9 power source to +5V_ALW2 for 1.8V_SUS_PWRGD assert when PU9 power down
	17	52	4/8 2008	B2A	Change PC106 value from 0.1U/50V TO 1U/10V for power engineer request
	18	42	4/12 2008	B2A	Connect U15 Pin67 to D35&D36 cathode.Fixed 1G LED can't blink issue
	19	25	4/16 2008	B2A	Change R235,R236 value to met design gildeline
	20	52	4/17 2008	B2A	Add PQ40 for GPU over temp. protection
	21	21,28,29,32,34	4/17 2008	B2A	Change ICH SMBus topology to provent back drive
	22	54	4/17 2008	B2A	ADD C989,C990 for EMI request
	23	27,35	4/21 2008	B2A	POP C32,C35,C43 with 10p,C31,C36,C41 with 22p POP L17,L20,L50 Depop R207,R203,R190,R183,R334,R329
	24	28	4/21 2008	B2A	Change R819 to diode prevent back driver from ICH to cardbus
	25	3	4/22 2008	B2A	Change R600 value to met spec
	26	19,50	4/22 2008	B2A	ADD GFX POWER voltage control to 3 level
	27	44	4/22 2008	B2A	Change U26,U32 to 74AHC1G08GW to met design
	28	14,40	4/22 2008	B2A	Separate DIS/UMA HDA power for codec/ICH9 to met Design guideline
	29	6	4/24 2008	B2A	Change R222 to 1K to met Design guideline

QUANTA COMPUTER

Model	Item	Page	Date	Rev.	Description
Pacino MV of Intel	1	25	6/6 2008		Change L64, L66, L70, L72 to CXCG900U000.
	2	43	6/6 2008		Change L80 to DB0FX6LAN01.
	3	09	6/6 2008		Change D28 to BC010K45004.
	4	46	6/6 2008		Change PQ4, PQ24 to BAM48350001.
	5	53	6/6 2008		Change PQ17 to BAM34560102.
	6	25	6/11 2008		Reserve R9999, R10000, R10001, R10002, C4945, C4946, C4947, C4948 for EMI solution.
	7	6	6/11 2008		Change R187,R213 pull high to +3.3V_RUN to solve backdrive in S3.
	8	14	6/11 2008		Change C957 from CH0220KMJ81 to CH71001M8B2
	9	48	6/11 2008		Change PC169 from CH733KM8826 to CH722KMT800
	10	54	6/11 2008		Change JBAT1 from DFHD09MR013 to DFHD09MR019
	11	11-14	6/11 2008		Change U48 from AJ0QP220T05 to AJ0QT100T01
	12	35	6/11 2008		Change JUSB1 from DFHS04FR126 to DFHS11FR018
	13	4,8,9	6/11 2008		Change C96, C188, C243, C438 to CH71001M8B2
	14	40	6/11 2008		Change J3 from DFHD04MR040 to DFWF04FR001
	15	38	6/11 2008		Change SW1 from DHLLSS12P03 to DHLLSS12P01
	16	35	6/11 2008		Change L17, L20, L50 from CX0SQ2T1001 to DC09004A014
	17	50	6/11 2008		Change PQ1 from BAM00350000 to BAM48350024
	18	51,46, 48,49	6/11 2008		NC PC131, PC129, PC197, PC94 depended on internal notice.
	19	25	6/11 2008		Change U13 to UMA part.
	20		6/11 2008		Delete reserved 0-ohm resisters: R192, R139, R226, R144, R145, R181, R248, R197, R198, R188, R189, R173, R195, R177, R208, R174, R196, R178, R215, R201, R176, R200, R179, R202, R175, R199, R180, R153, R152, R154, R149, R150, R238, R851, R717, R716, R241, R230, R206, R209, R210, R212, R245, R846, R847, R140, R848, R730, R842, R815, R871, R778, R769, R718, R664, R647, R665, R663, R709, R701, R700, R694, R105, R143, R77, R81, R75, R182, R185, R804, R767, R768, R683, R437, R547, R576, R575, R579, R428, R424, R422, R420, R423, PR46, RPR14, PR4, PR6, PR91
	21	42	6/12 2008		Change R325 to 39K-ohm and R311 to 20K-ohm for LAN chip, BCM5784M.
	22	48	6/12 2009		Change PQ32 & PQ33 subsystem ID to PWR.Plane.Regulator_1p05v1p5v.
	23	46, 48	6/12 2009		Change PL3 to CV-5855TZ04 & PL7 to DC-15A00002.
	24	48	6/12 2009		Populate PC197 by power's request.
	25	14	6/12 2009		Change U53 to DELL PSL LDO part and schematic
	26	40	6/13 2009		Change Audio codec U31 to revision C1, AL73C1XSB03 for ST build.
	27	25	6/13 2009		For HDMI pre-test item, DDC/CEC Capacitanoea, add low-Capacitance MOSs on SM-BUS between HDMI connector and PI3VDP411LSZDE.
	28		6/13 2009		Change C96, C988, C987, C438, C188, C243, C435, C299, C353, C957 to 220uF CAP/2.5V, CH7221M8816.
	29	28	6/13 2009		Depopulate R819, because R5C833 don't need PME#.
	30	31	6/13 2009		Change the BID to ST stage.
	31		6/13 2009		Change L87, L86, L91, L20, L17, L50, L46 to CXCG900U000.
	32	38	6/13 2009		Change SW1 to DHLLSS12P03
	33	41, 52	6/13 2009		Delete reserved 0-ohm resisters R826 and PR92.
	34	52	6/13 2009		Reserve a CAP PC200 for glith reducing of TEMP_FAIL.
	35	33	6/17 2009		Change C655 to 100uF CAP, CH7101M8800.
	36	19, 52	6/18 2010		DELL's request on thermal detect pin
	37	50	6/19 2010		Change PR119 to CS32433F915(0603), PR116 to CS38663F904(0603), PR118 to CS43572FB07(0402), R120 to CS16803F913(0603), PR183 to CS41152FB08(0402), PR188 to CS22002FB01(0402) to meet GPU core voltage step: 0.9V, 0.95V and 1.1V.
	38	3,4	6/23 2009		Change CPU socket(U42) P/N to DGT*8000001(Foxconn)
	39	3	6/23 2009		NC R116 for H_RESET# glitch.
	40	25	6/24 2009		Fine-tune the emphasis and the equalization of HDMI. 1. Pull OC0, OC2 to high and Pull OC1, OC3 to low. 2. Pull EQ_1 to low and pull EQ_0 to high.
	41	15	6/24 2009		Change JDIM1 to H=5.6mm connector, DGMK0000015 and JDIM2 to H=10.1mm connector, DGMK0000016.
	42	31	6/26 2009		NC R601, R704 and populate R593 for avtivating platform reset signal.

QUANTA COMPUTER

Model	Item	Page	Date	Rev.	Description
Pacino MV of Intel					

QUANTA COMPUTER

Title: A00 change list		
Size	Document Number: GM3	Rev: B2A
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