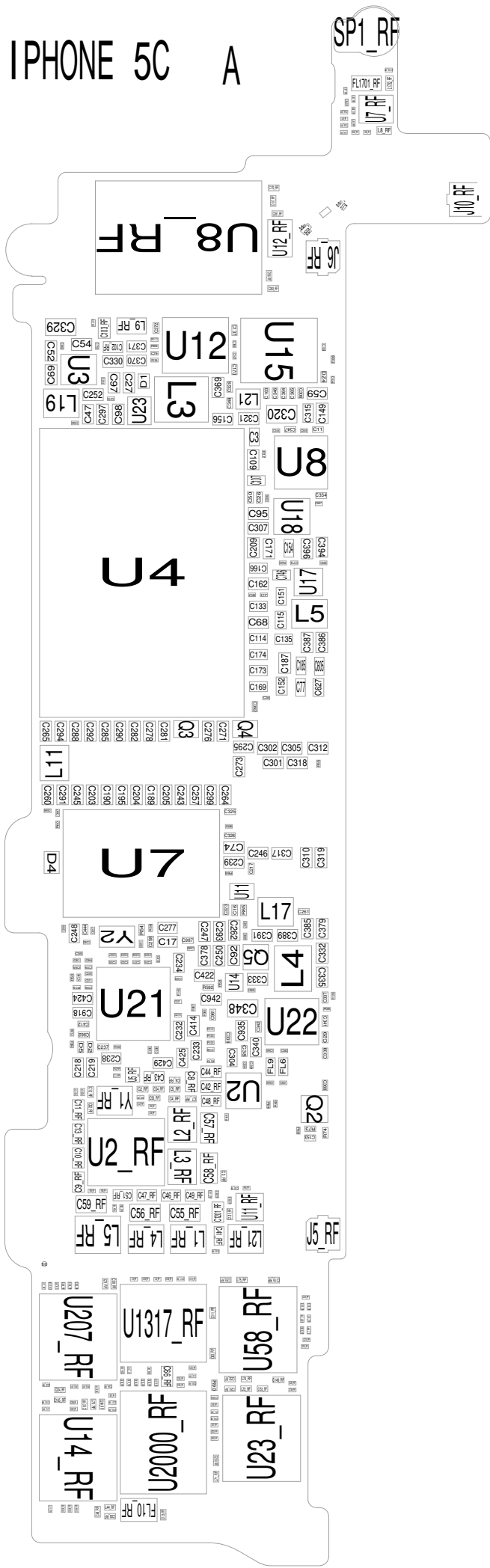


IPHONE 5C A

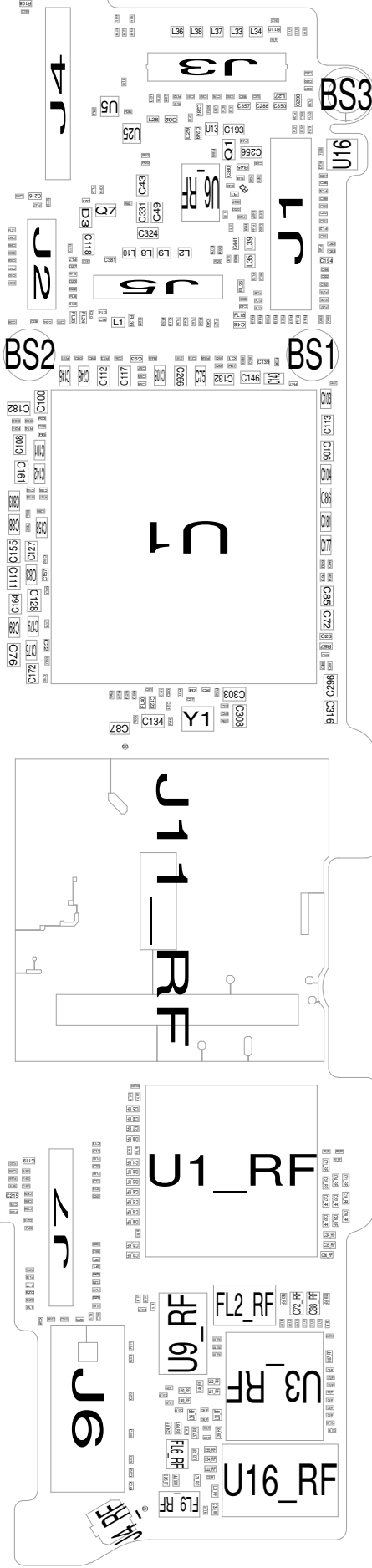


SP3_RF

IPHONE 5C B

U20_RF

CL1



1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IPHONE 5C 原理图

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
2	0001669557	ENGINEERING RELEASED		2012-10-14

X155 PROTO1 SINGLE BRD

Mon Oct 8 11:06:07 2012

TO DO: CLEANUP ALTERNATES FOR X155

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0648	138S0652	ALTERNATE	?	4.7UF CERM 0402 6.3V
339S0177	339S0176	ALTERNATE	?	H5P ALTERNATE
339S0178	339S0176	ALTERNATE	?	H5P ALTERNATE

X155 BOM CALLOUTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9584	1	SCH, SINGLE_BRD, X155	SCH	Y	?
820-3329	1	PCB, SINGLE_BRD, X155	PCB	Y	?
825-6838	1	LABEL FOR X155 639-3796	EEEE_F284	Y	EEEE_16G

PDF PAGE	CSA PAGE	CONTENTS	SYNC MASTER	DATE
2	2	H5P JTAG, USB ,PLL	N/A	N/A
3	3	H5P GPIO & CONTROL	N/A	N/A
4	4	H5P IO POWER	N/A	N/A
5	5	H5P SOC/CPU/SRAM PWR	N/A	N/A
6	6	H5P W/ NAND	N/A	N/A
7	7	H5P VIDEO	N/A	N/A
8	8	BUTTON FLEX B2B	N/A	N/A
9	9	L67 AUDIO CODEC (1/2)	N/A	N/A
10	10	L67 AUDIO CODEC (2/2)	N/A	N/A
11	11	CG FLEX B2B	N/A	N/A
12	12	AGATHA PMU(1/2)	N/A	N/A
13	13	AGATHA PMU(2/2)	N/A	N/A
14	14	CHESTNUT + BACKLIGHT DRIVER	N/A	N/A
15	15	SPKR AMP + LED DRIVER	N/A	N/A
16	16	TRISTAR	N/A	N/A
17	17	DOCKFLEX B2B	N/A	N/A
18	18	D404 (TOUCH B2B, DRIVER ICS)	N/A	N/A
19	19	LCM CONNECTOR	N/A	N/A
20	20	SENSORS	N/A	N/A
21	21	CAM0 CONNECTOR	N/A	N/A
22	22	BATT B2B, TPS, PD FEATURES	N/A	N/A
23	23	RADIO_MLB HIERARCH. SYMBOL	N/A	N/A

COMPASS BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
639-4024	1	ST GYRO - COMPASS POP	U16	Y	COMPASS_POP

NAND BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	NAND, 19NM, 16GX8, MLC, PPN1.5	U4	Y	NAND_16G

HORIZONTAL CAP BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0801	5	HRZN CAPS_1:10UF,0402,6.3V	C422,C74,C92,C250,C265	Y	HRZN_CAP_GRP1
138S0801	5	HRZN CAPS_1:10UF,0402,6.3V	C293,C294,C257,C299,C262	Y	HRZN_CAP_GRP2
138S0801	5	HRZN CAPS_1:10UF,0402,6.3V	C264,C378,C189,C203,C245	Y	HRZN_CAP_GRP3
138S0801	5	HRZN CAPS_1:10UF,0402,6.3V	C190,C204,C239,C246,C195	Y	HRZN_CAP_GRP4
138S0801	5	HRZN CAPS_1:10UF,0402,6.3V	C205,C243,C247,C252,C297	Y	HRZN_CAP_GRP5
138S0801	5	HRZN CAPS_1:10UF,0402,6.3V	C386,C387,C333,C332,C335	Y	HRZN_CAP_GRP6
138S0801	3	HRZN CAPS_1:10UF,0402,6.3V	C42_RF,C43_RF,C44_RF	Y	HRZN_CAP_GRP7
138S0801	1	HRZN CAPS_1:10UF,0402,6.3V	C1201_RF	Y	HRZN_CAP_GRP8
138S0801	4	HRZN CAPS_1:10UF,0402,6.3V	C182,C307,C209,C187	Y	HRZN_CAP_GRP10
138S0794	2	HRZN CAPS_1:10UF,0402,10V	C52,C156	Y	HRZN_CAP_GRP11
138S0582	1	4.7UF 0.55MM HEIGHT	C193	Y	LOW_Z_CAP

BOARD ID RADIO BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0621	1	1.00M 1% 01005	R25_RF	Y	N51_CFG_A
118S0732	1	50K 1% 01005	R26_RF	Y	N51_CFG_A
117S0159	1	470K 5% 01005	R25_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_A
118S0726	1	162K 1% 01005	R26_RF	Y	N53_CFG_A
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_B
118S0623	1	267K 1% 01005	R26_RF	Y	N53_CFG_B
118S0659	1	255K 1% 01005	R25_RF	Y	N48_CFG_A
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_A
118S0689	1	147K 1% 01005	R25_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N49_CFG_A
118S0650	1	499K 1% 01005	R26_RF	Y	N49_CFG_A
118S0732	1	50K 1% 01005	R25_RF	Y	N49_CFG_B
118S0621	1	1.00M 1% 01005	R26_RF	Y	N49_CFG_B

GYRO BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1158	1	ST GYRO	U8	Y	GYRO_ST
132S0391	1	ST GYRO - CP CAP	C11	Y	GYRO_ST

CHESTNUT BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1172	1	TI CHESTNUT	U3	Y	CHESTNUT_TI
152S1649	1	TI CHESTNUT - 1.5 UH IND	L19	Y	CHESTNUT_TI
338S1168	1	INTERSIL CHESTNUT	U3	Y	CHESTNUT_INTERSIL
152S1611	1	INTERSIL CHESTNUT -2.2 UH IND	L19	Y	CHESTNUT_INTERSIL

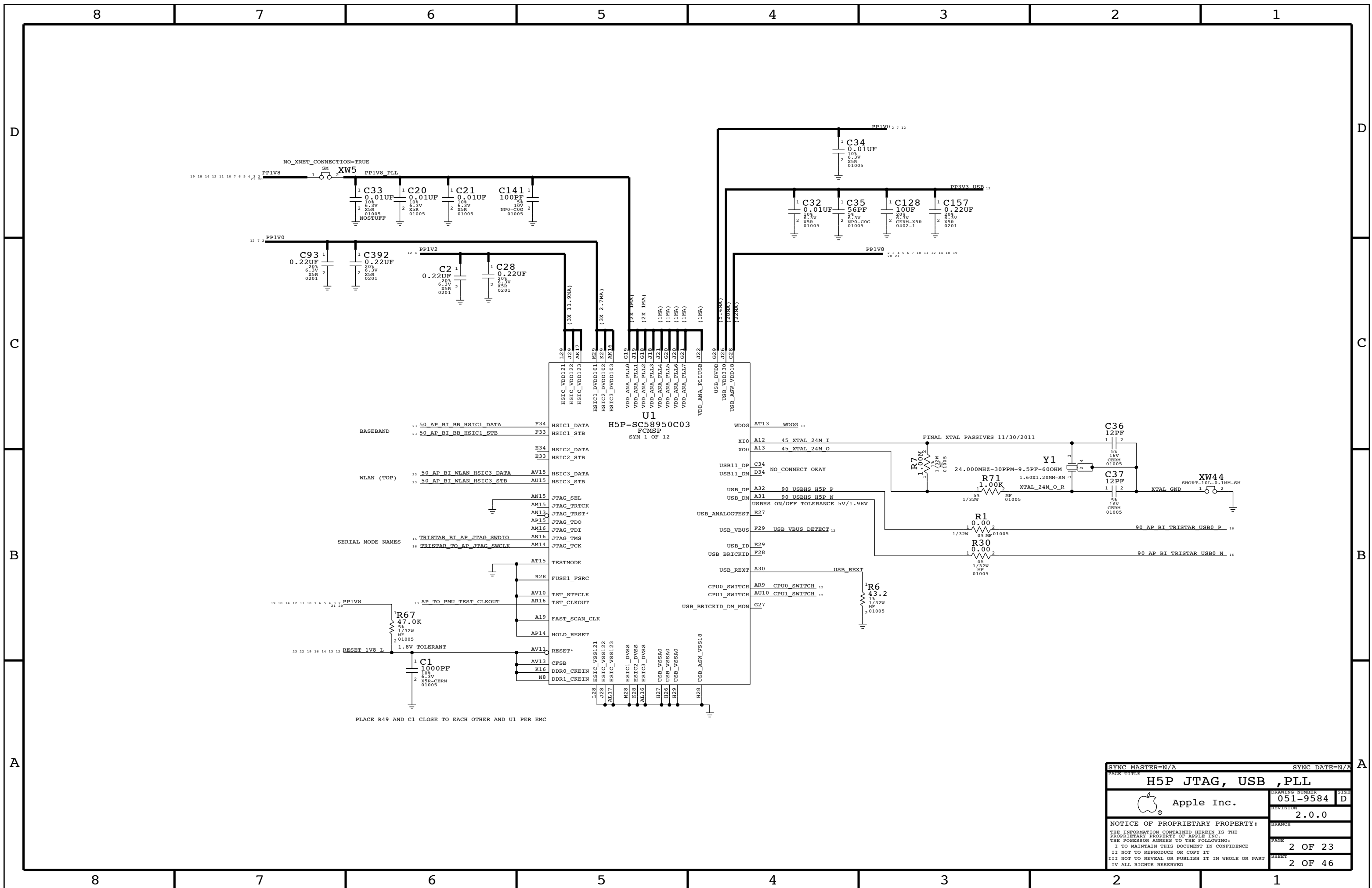
TRISTAR BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	CBTL1608A1UK,WCSF,TRISTAR	U2	Y	TRISTAR
343S0639	1	CBTL1610A0UK,WCSF,TRISTAR2	U2	Y	TRISTAR2
118S0671	2	RES 150HM 01005 5%	R102,R103	Y	TRISTAR
117S0202	2	RES 200HM 01005 5%	R102,R103	Y	TRISTAR2

SCH 051-9584
BRD 820-3329

BOM 639-3796 X155

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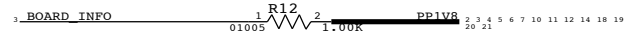
PAGE TITLE		SYNC DATE=N/A	
H5P JTAG, USB, PLL			
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		REVISION	2.0.0
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		PAGE	2 OF 23
		SHEET	2 OF 46
		SIZE	D

BOARD_REV[3:0]={EHCI_PORT3,EHCI_PORT_PWR2,EHCI_PORT_PWR1,EHCI_PORT_PWR0}
 FLOAT=LOW, PULLUP=HIGH
 1111 X155 INITIAL
 1101 - PROTO1 TRISTAR <---PROTO1 SELECTED
 1100 - PROTO1 TRISTAR 2

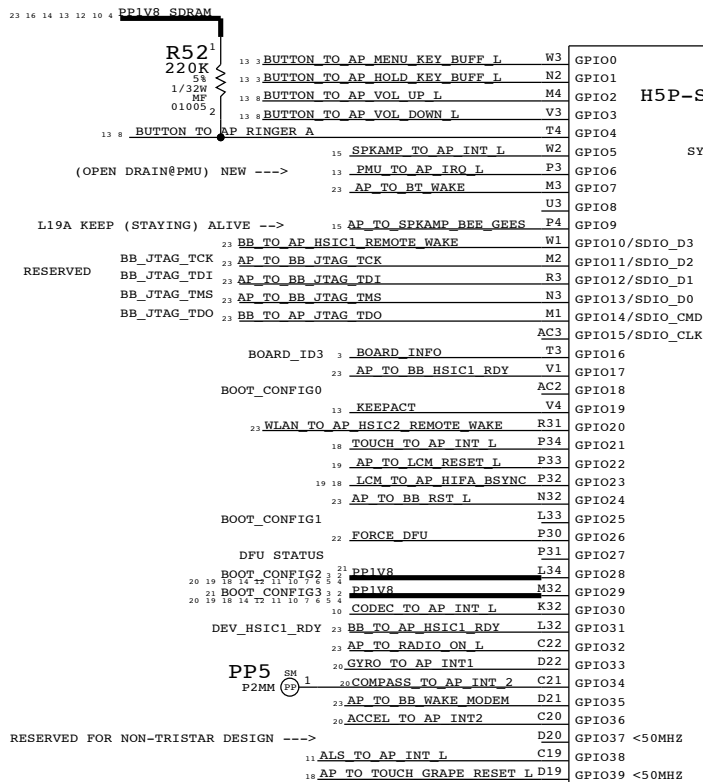
BOARD_ID[3:0]={GPIO16,SPI0_MISO,SPI0_MOSI,SPI0_SCLK}
 FLOAT=LOW, PULLUP=HIGH
 1010 X155 MLB <--- SELECTED

BOOT_CONFIG[3:0]={GPIO29_CONFIG3,GPIO28_CONFIG2,GPIO25_CONFIG1,GPIO18_CONFIG0}
 FLOAT=LOW, PULLUP=HIGH
 0000 SPI0
 0001 SPI3
 0010 SPI0 W/TEST
 0011 SPI3 W/TEST
 1000 FM10 2 CS
 1001 FM10 4 CS
 1010 FM10 4CS W/TEST
 1011 RESERVED
 1100 FM11 2 CS
 1101 FM11 4 CS
 1110 FM10/1 2/2 CS <--- SELECTED
 1101 FM10/1 4/4 CS
 1110 FM10/1 4/4 CS W/TEST
 1111 RESERVED

COMMON PULL UP FOR BOARD_REV, BOARD_ID AND BOOT_CONFIG PINS



R12 MUST WIN OVER 6X INTERNAL PULL-DOWNS THAT ARE ~100K

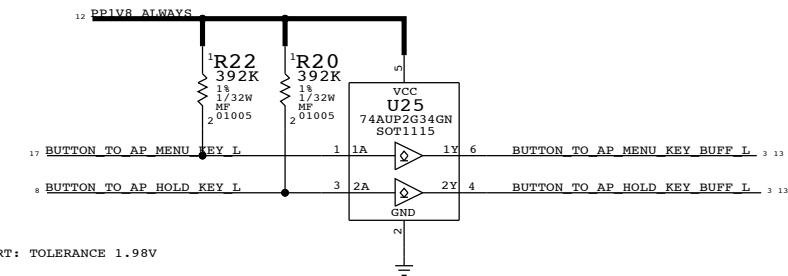


RESERVED FOR NON-TRISTAR DESIGN --->
 17 AP_TO_HEADSET_HS3_CTRL AT11
 17 AP_TO_HEADSET_HS4_CTRL AP12

Pin	Signal	Chip Pin	Function
1	EHCI_PORT_PWR0	AD3	BOARD_REV0
2	EHCI_PORT_PWR1	AD4	BOARD_REV1
3	EHCI_PORT_PWR2	AD5	BOARD_REV2
4	EHCI_PORT_PWR3	AD6	BOARD_REV3
5	GPIO0	AT6	GYRO_TO_AP_INT2
6	GPIO1	AP8	VIB_PWM
7	GPIO2	AP1	45 AP_TO_TOUCH_CLK32K_RESET_L
8	GPIO3	AR15	VIB_LDO_EN
9	GPIO4	AU12	AP_TO_LEDDRV_EN
10	GPIO5	AA3	BB_TO_AP_UART1_CTS_L
11	GPIO6	AB2	AP_TO_BB_UART1_RTS_L
12	GPIO7	AB3	BB_TO_AP_UART1_RXD
13	GPIO8	AF5	AP_TO_BB_UART1_TXD
14	GPIO9	AG3	TRISTAR_TO_AP_INT1
15	GPIO10	AA1	ACCEL_TO_AP_INT1
16	GPIO11	AE2	TRISTAR_TO_AP_ACC_UART2_RXD
17	GPIO12	AF3	AP_TO_TRISTAR_ACC_UART2_TXD
18	GPIO13	AH3	BT_TO_AP_UART3_CTS_L
19	GPIO14	AB1	AP_TO_BT_UART3_RTS_L
20	GPIO15	AF4	BT_TO_AP_UART3_RXD
21	GPIO16	AG4	AP_TO_BT_UART3_TXD
22	GPIO17	AJ4	AP_TO_BB_JTAG_TRST_L
23	GPIO18	AE1	AP_TO_CAM_RF_VDDCORE_EN
24	GPIO19	AJ2	WLAN_TO_AP_UART4_RXD
25	GPIO20	AH4	AP_TO_WLAN_UART4_TXD
26	GPIO21	AK4	AP_BI_BATTERY_SWI
27	GPIO22	AJ3	BB_TO_AP_RESET_DET_L
28	GPIO23	AH2	BB_TO_AP_PP_SYNC
29	GPIO24	AL1	AP_TO_SPKAMP_RESET_L
30	GPIO25	AK3	TRISTAR_TO_AP_DEBUG_UART6_RXD
31	GPIO26	AD1	AP_TO_TRISTAR_DEBUG_UART6_TXD
32	GPIO27	AU13	FMI
33	GPIO28	AR14	FMI
34	GPIO29	AR13	I2C2
35	GPIO30	AT12	SPI3

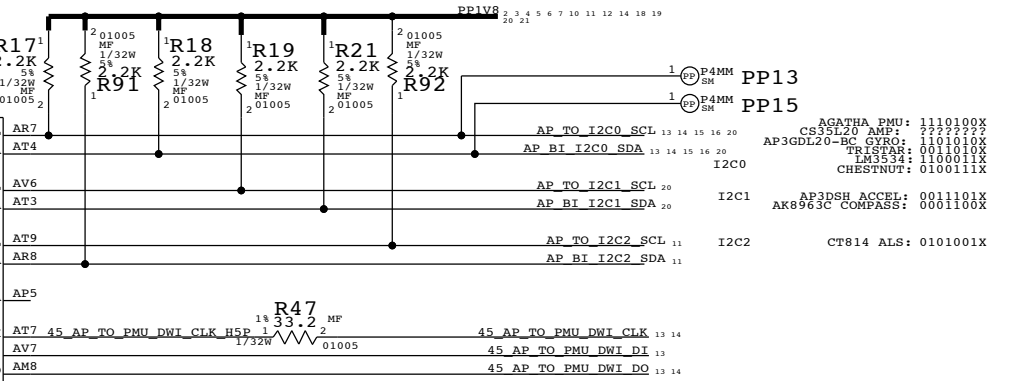
FMI, 00=1.8V | 01=3.0V | 10=3.3V
 I2C2, 0=1.8V | 1=3.0V
 SPI3, 0=1.8V | 1=3.0V

MENU & POWER / HOLD KEY



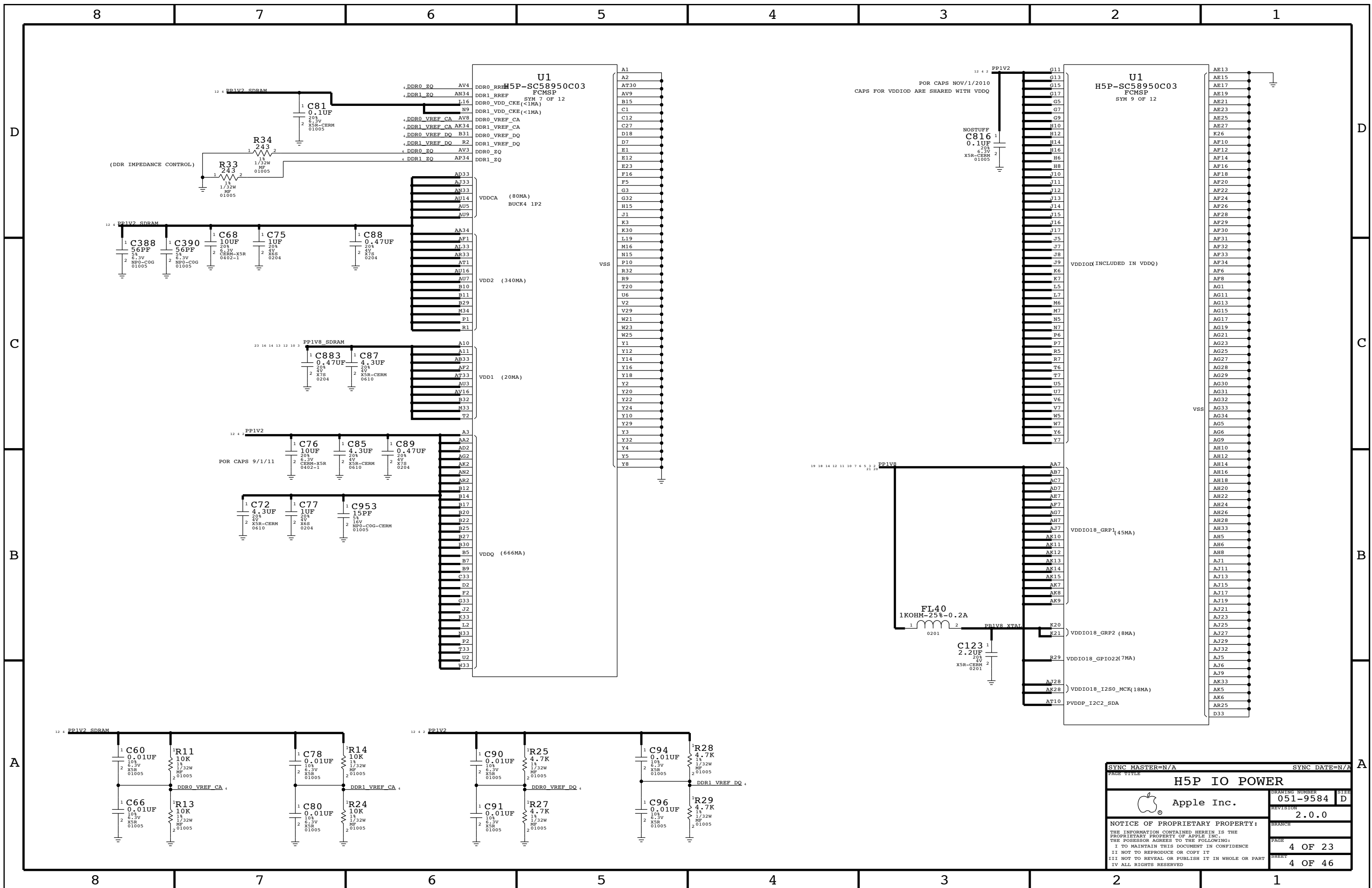
DEBUG UART: TOLERANCE 1.98V

Pin	Signal	Chip Pin	Function
1	CODEC ASP	AP30	I2S0_MCK
2	CODEC ASP	AM30	I2S0_BCLK
3	CODEC ASP	AH31	I2S0_LRCLK
4	CODEC ASP	AH32	I2S0_DIN
5	CODEC ASP	AH33	I2S0_DOUT
6	BASEBAND	AK29	I2S1_MCK
7	BASEBAND	AL31	I2S1_BCLK
8	BASEBAND	AN31	I2S1_LRCLK
9	BASEBAND	AH29	I2S1_DIN
10	BASEBAND	AH32	I2S1_DOUT
11	CODEC XSP & SPKR AMP	AM29	I2S2_MCK
12	CODEC XSP & SPKR AMP	AM28	I2S2_BCLK
13	CODEC XSP & SPKR AMP	AJ31	I2S2_LRCLK
14	CODEC XSP & SPKR AMP	AM33	I2S2_DIN
15	CODEC XSP & SPKR AMP	AN30	I2S2_DOUT
16	BLUETOOTH	AM31	I2S3_MCK
17	BLUETOOTH	AK31	I2S3_BCLK
18	BLUETOOTH	AL28	I2S3_LRCLK
19	BLUETOOTH	AL30	I2S3_DIN
20	BLUETOOTH	AP31	I2S3_DOUT
21	CODEC VSP	AK30	I2S4_MCK
22	CODEC VSP	AM32	I2S4_BCLK
23	CODEC VSP	AP32	I2S4_LRCLK
24	CODEC VSP	AK32	I2S4_DIN
25	CODEC VSP	AR32	I2S4_DOUT
26	BOARD_ID2	AR31	SPDIF
27	BOARD_ID1	AM4	SPI0_MISO
28	BOARD_ID0	AR5	SPI0_MOSI
29	LCM TO AP PIFA	AM2	SPI0_SCLK
30	LCM TO AP PIFA	AP3	SPI0_SSIN
31	TOUCH TO AP SPI1 MISO	AN3	SPI1_MISO
32	AP TO TOUCH SPI1 MOSI	AL3	SPI1_MOSI
33	AP TO TOUCH SPI1 CLK	AK1	SPI1_SCLK
34	AP TO TOUCH SPI1 CS L	AR4	SPI1_SSIN
35	FCAM TO AP ALS INT L	AN4	SPI2_MISO
36	BB TO AP IPC GPIO	AM3	SPI2_MOSI
37	AP TO WLAN HSIC2 RDY	AN6	SPI2_SCLK
38	WLAN TO AP HSIC2 RDY	AN1	SPI2_SSIN
39	CODEC TO AP SPI3 MISO	AP9	SPI3_MISO
40	AP TO CODEC SPI3 MOSI	AM9	SPI3_MOSI
41	AP TO CODEC SPI3 CLK	AM13	SPI3_SCLK
42	AP TO CODEC SPI3 CS L	AN12	SPI3_SSIN

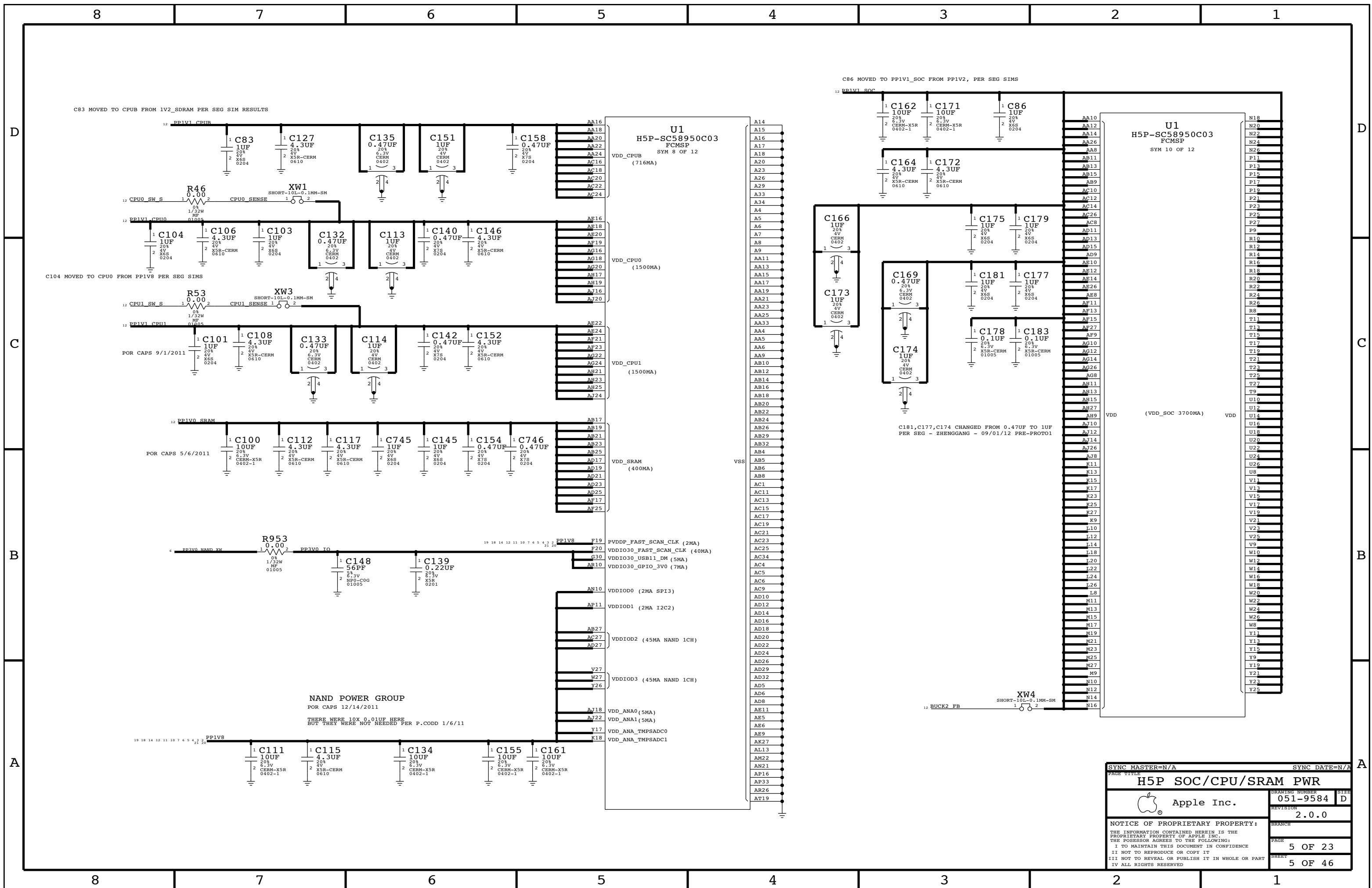


Pin	Signal	Chip Pin	Function
1	I2C0	AR7	I2C0_SCL
2	I2C0	AT4	I2C0_SDA
3	I2C1	AV6	I2C1_SCL
4	I2C1	AT3	I2C1_SDA
5	I2C2	AT9	I2C2_SCL
6	I2C2	AR8	I2C2_SDA
7	SPI0	AM8	DWI_DO
8	SPI0	AV7	DWI_DI
9	SPI0	AT7	DWI_CLK
10	SPI0	AV7	DWI_DI
11	SPI0	AM8	DWI_DO
12	SPI0	AV7	DWI_DI
13	SPI0	AT7	DWI_CLK
14	SPI0	AV7	DWI_DI
15	SPI0	AM8	DWI_DO
16	SPI0	AV7	DWI_DI
17	SPI0	AT7	DWI_CLK
18	SPI0	AV7	DWI_DI
19	SPI0	AM8	DWI_DO
20	SPI0	AV7	DWI_DI
21	SPI0	AT7	DWI_CLK
22	SPI0	AV7	DWI_DI
23	SPI0	AM8	DWI_DO
24	SPI0	AV7	DWI_DI
25	SPI0	AT7	DWI_CLK
26	SPI0	AV7	DWI_DI
27	SPI0	AM8	DWI_DO
28	SPI0	AV7	DWI_DI
29	SPI0	AT7	DWI_CLK
30	SPI0	AV7	DWI_DI
31	SPI0	AM8	DWI_DO
32	SPI0	AV7	DWI_DI
33	SPI0	AT7	DWI_CLK
34	SPI0	AV7	DWI_DI
35	SPI0	AM8	DWI_DO
36	SPI0	AV7	DWI_DI
37	SPI0	AT7	DWI_CLK
38	SPI0	AV7	DWI_DI
39	SPI0	AM8	DWI_DO
40	SPI0	AV7	DWI_DI
41	SPI0	AT7	DWI_CLK
42	SPI0	AV7	DWI_DI
43	SPI0	AM8	DWI_DO
44	SPI0	AV7	DWI_DI
45	SPI0	AT7	DWI_CLK
46	SPI0	AV7	DWI_DI
47	SPI0	AM8	DWI_DO
48	SPI0	AV7	DWI_DI
49	SPI0	AT7	DWI_CLK
50	SPI0	AV7	DWI_DI
51	SPI0	AM8	DWI_DO
52	SPI0	AV7	DWI_DI
53	SPI0	AT7	DWI_CLK
54	SPI0	AV7	DWI_DI
55	SPI0	AM8	DWI_DO
56	SPI0	AV7	DWI_DI
57	SPI0	AT7	DWI_CLK
58	SPI0	AV7	DWI_DI
59	SPI0	AM8	DWI_DO
60	SPI0	AV7	DWI_DI
61	SPI0	AT7	DWI_CLK
62	SPI0	AV7	DWI_DI
63	SPI0	AM8	DWI_DO
64	SPI0	AV7	DWI_DI
65	SPI0	AT7	DWI_CLK
66	SPI0	AV7	DWI_DI
67	SPI0	AM8	DWI_DO
68	SPI0	AV7	DWI_DI
69	SPI0	AT7	DWI_CLK
70	SPI0	AV7	DWI_DI
71	SPI0	AM8	DWI_DO
72	SPI0	AV7	DWI_DI
73	SPI0	AT7	DWI_CLK
74	SPI0	AV7	DWI_DI
75	SPI0	AM8	DWI_DO
76	SPI0	AV7	DWI_DI
77	SPI0	AT7	DWI_CLK
78	SPI0	AV7	DWI_DI
79	SPI0	AM8	DWI_DO
80	SPI0	AV7	DWI_DI
81	SPI0	AT7	DWI_CLK
82	SPI0	AV7	DWI_DI
83	SPI0	AM8	DWI_DO
84	SPI0	AV7	DWI_DI
85	SPI0	AT7	DWI_CLK
86	SPI0	AV7	DWI_DI
87	SPI0	AM8	DWI_DO
88	SPI0	AV7	DWI_DI
89	SPI0	AT7	DWI_CLK
90	SPI0	AV7	DWI_DI
91	SPI0	AM8	DWI_DO
92	SPI0	AV7	DWI_DI
93	SPI0	AT7	DWI_CLK
94	SPI0	AV7	DWI_DI
95	SPI0	AM8	DWI_DO
96	SPI0	AV7	DWI_DI
97	SPI0	AT7	DWI_CLK
98	SPI0	AV7	DWI_DI
99	SPI0	AM8	DWI_DO
100	SPI0	AV7	DWI_DI

SYNC MASTER=N/A		SYNC DATE=N/A	
H5P GPIO & CONTROL			
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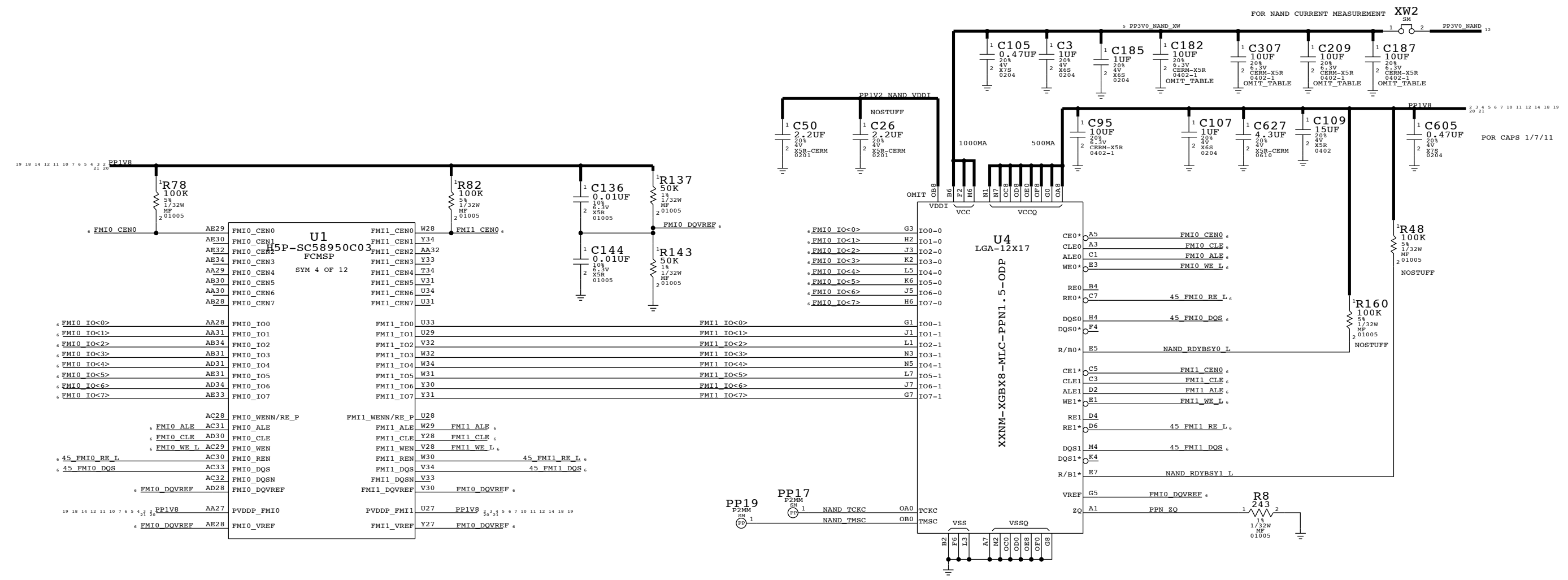


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H5P SOC/CPU/SRAM PWR			
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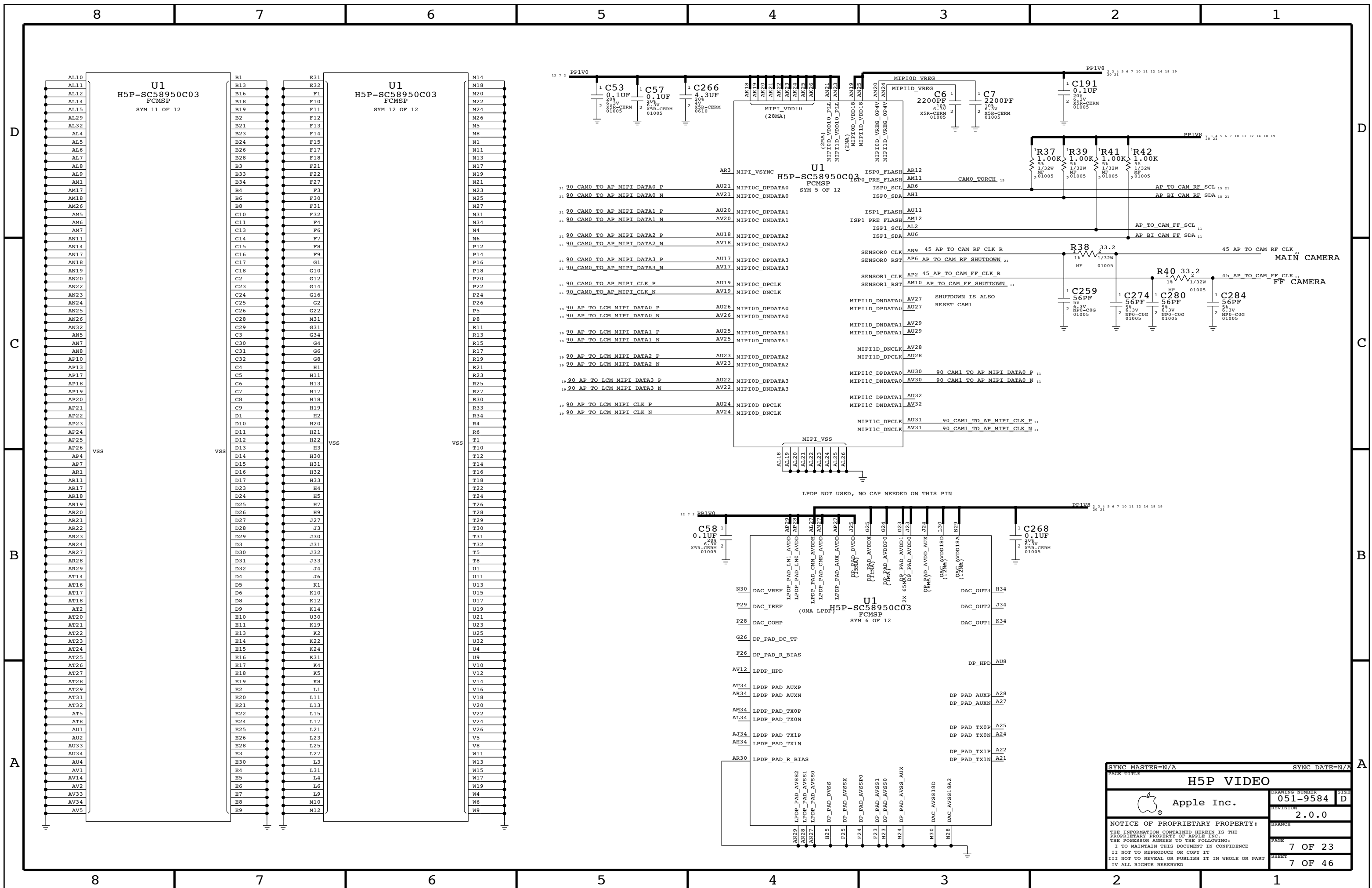
NAND



- PP2 P4MM SH 1 FMIO IO<0>
- PP3 P4MM SH 1 45_FMIO_RE_L
- PP14 P4MM SH 1 45_FMIO_DQS

NOTE: NAND PADS SHOULD BE SHIELDED FROM TRACES WITH A GROUND PLANE

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H5P W/ NAND			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	2.0.0
		BRANCH	
		PAGE	6 OF 23
		SHEET	6 OF 46



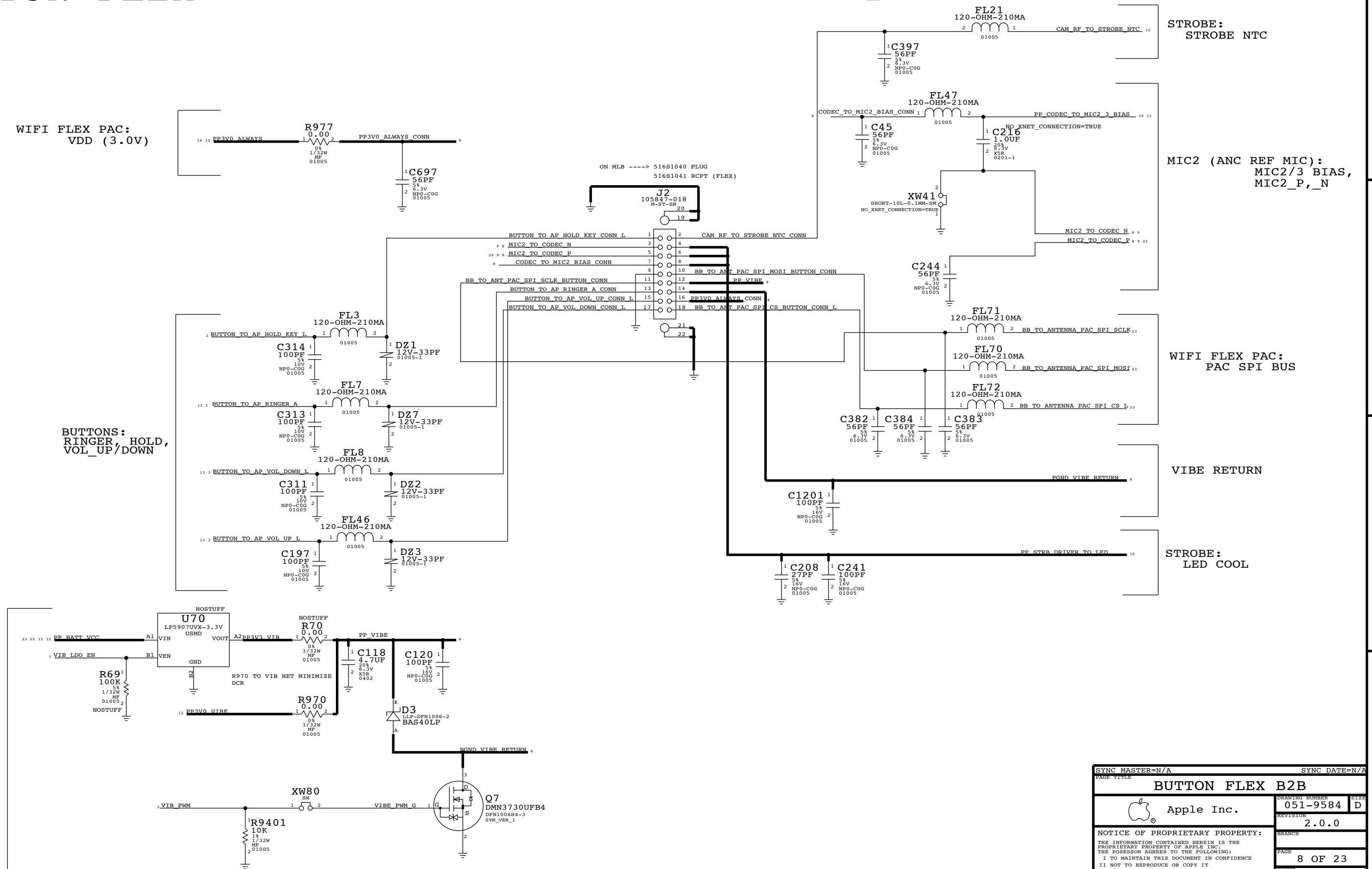
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Apple Inc.		DRAWING NUMBER	SIZE
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		SHEET	
		7 OF 46	

BUTTON FLEX (VIBE DRIVER, BUTTONS, ANC REF MIC, STROBE, STROBE_NTC)

WIFI FLEX PAC:
VDD (3.0V)

BUTTONS:
RINGER, HOLD,
VOL_UP/DOWN

VIBE DRIVE



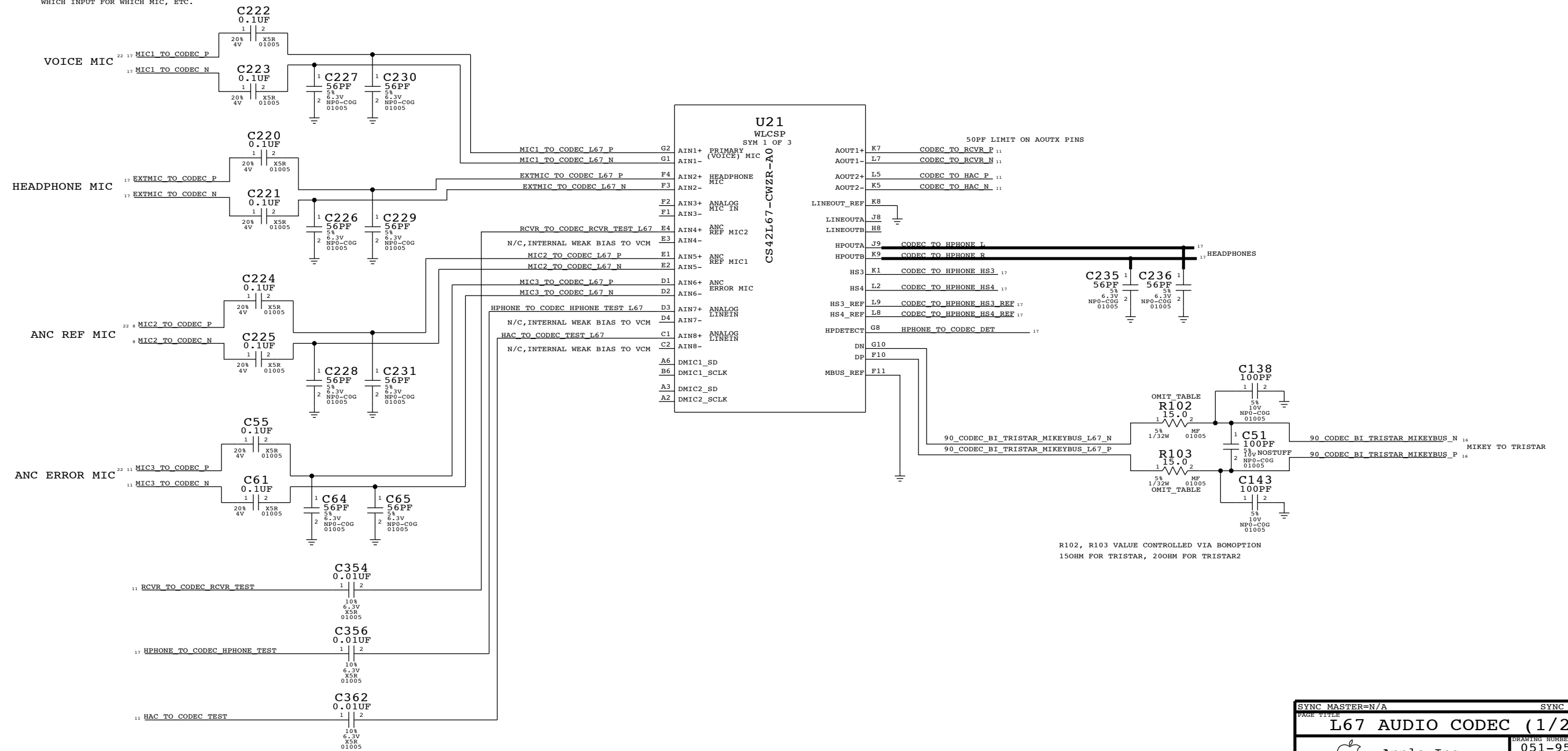
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BUTTON FLEX B2B			
	DRAWING NUMBER		SIZE
	051-9584		D
REVISION		BRANCH	
2.0.0			
PAGE		SHEET	
8 OF 23		8 OF 46	
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L67 AUDIO CODEC

AUDIO I/O

(ANALOG MIC IN, DIG MIC IN, HPOUT, LINEOUT, RECEIVER OUT, MIKEYBUS)

TO DO: REVIEW AUDIO MIC PATHS,
WHICH BIAS OUTPUT USED FOR WHICH MIC,
WHICH INPUT FOR WHICH MIC, ETC.



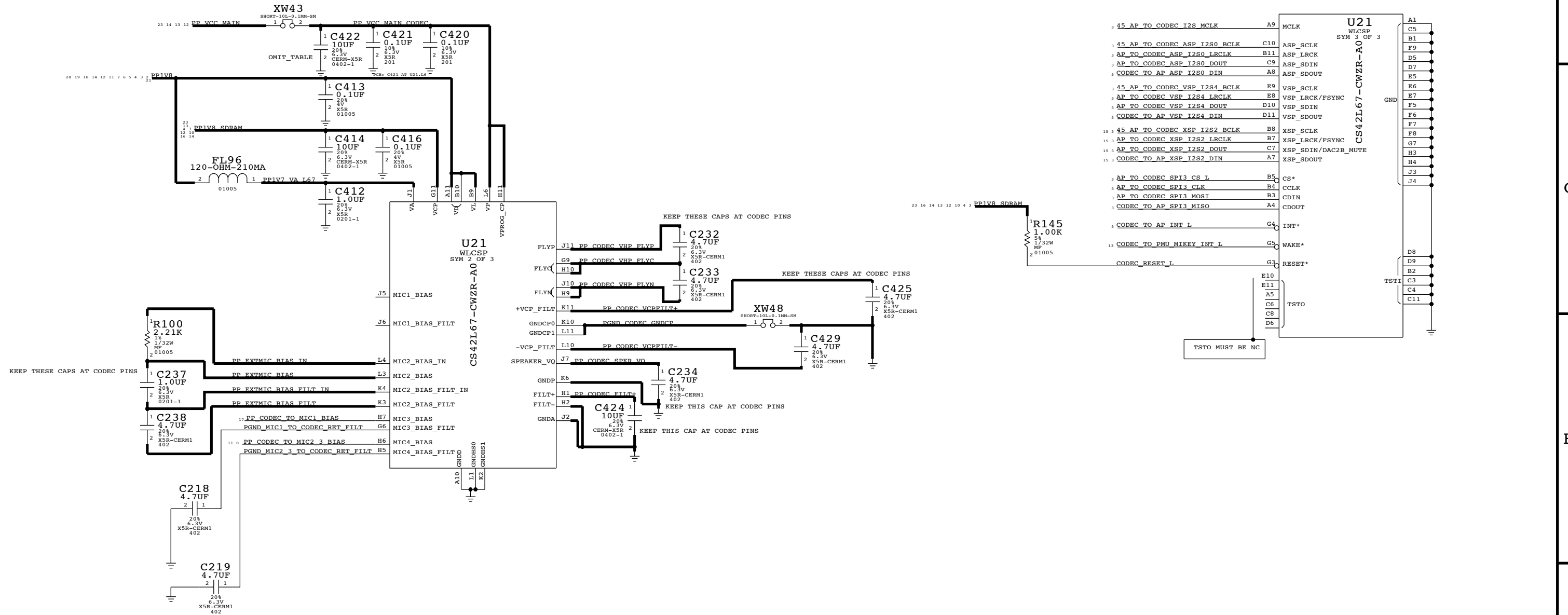
R102, R103 VALUE CONTROLLED VIA BOMOPTION
150HM FOR TRISTAR, 200HM FOR TRISTAR2

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE L67 AUDIO CODEC (1/2)			
DRAWING NUMBER 051-9584		SIZE D	
REVISION 2.0.0		BRANCH	
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED			
PAGE 9 OF 23		SHEET 9 OF 46	

L67 AUDIO CODEC

POWER, MICBIAS

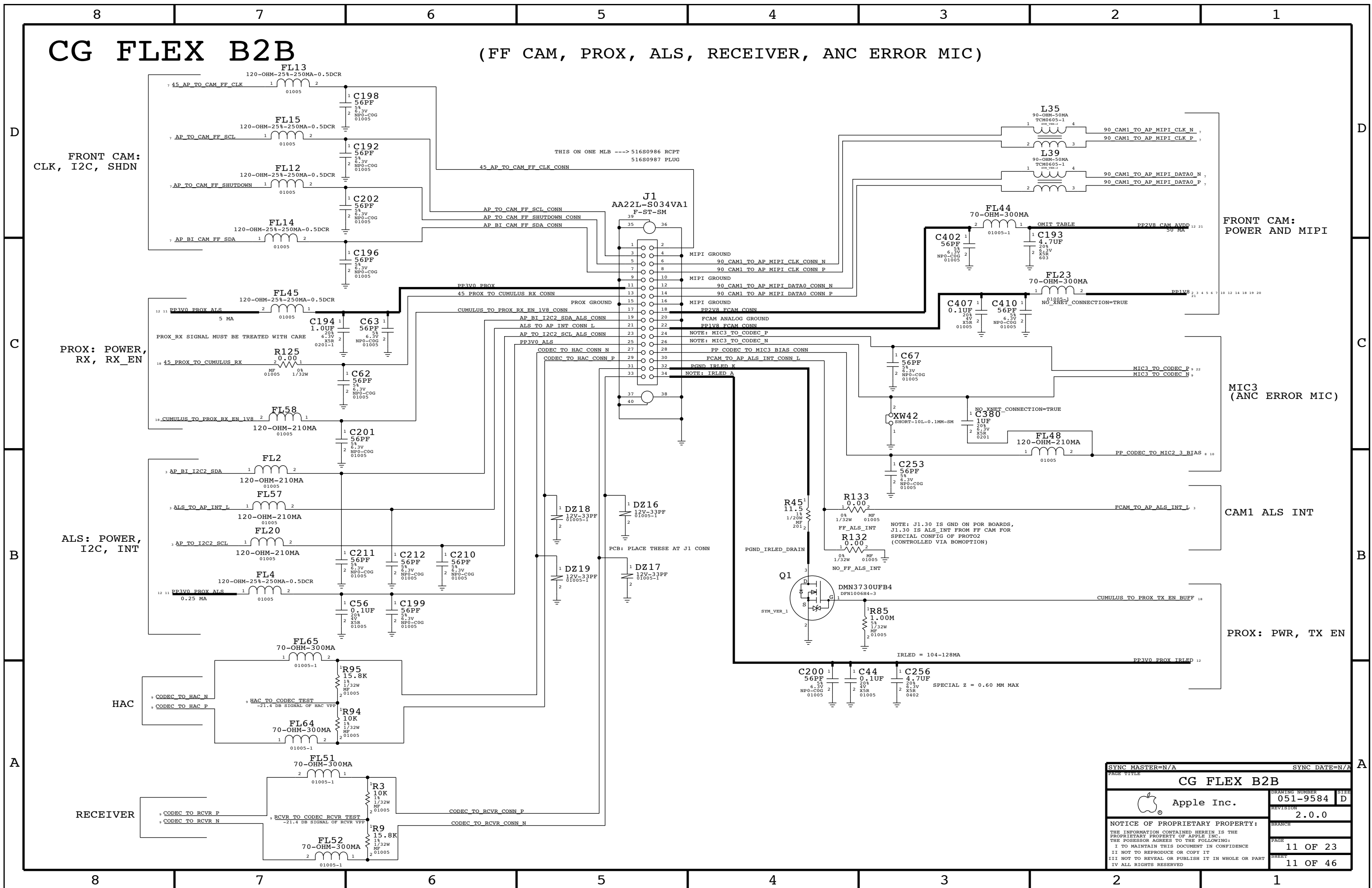
DIGITAL SYSTEM I/O



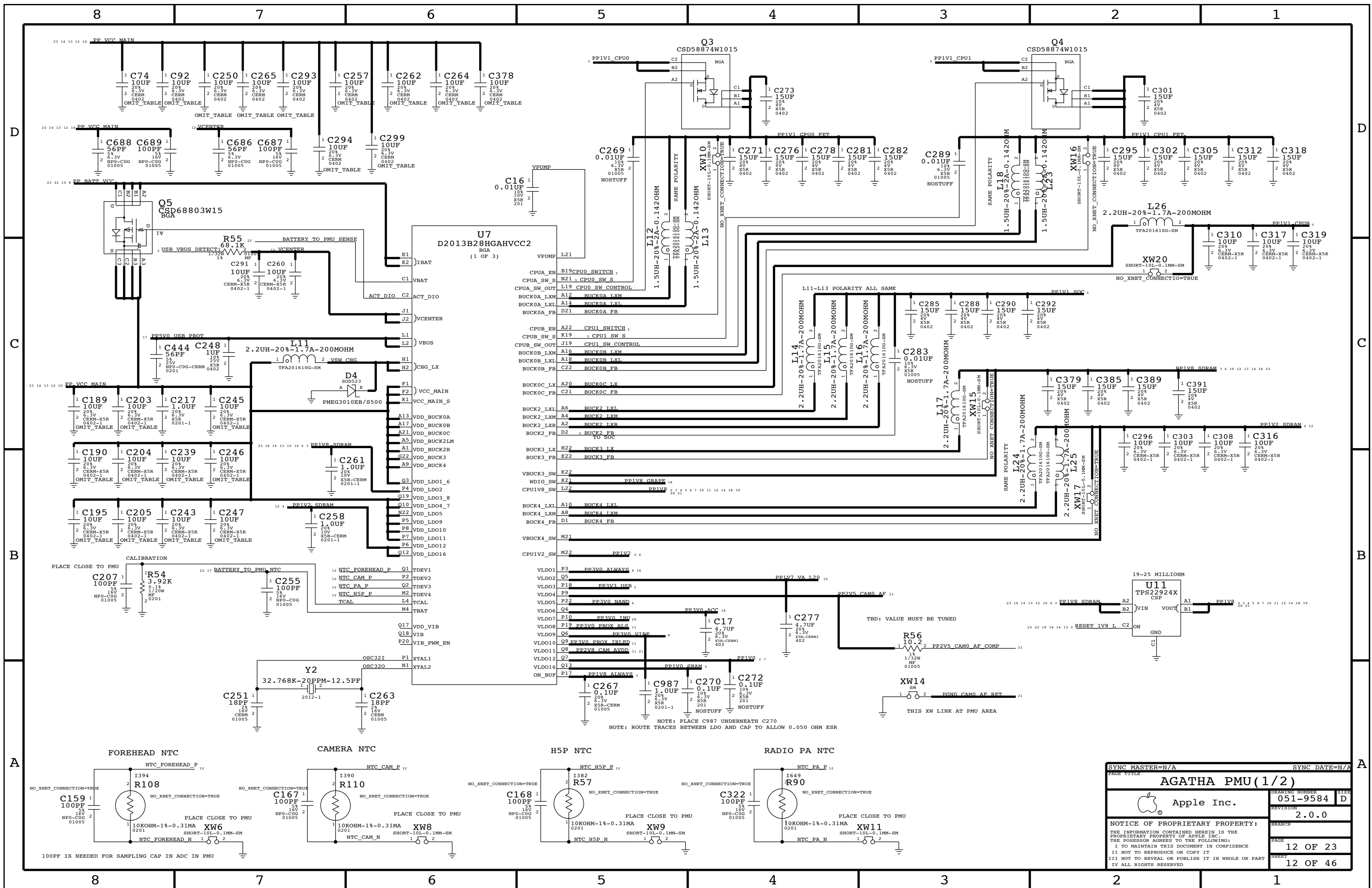
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L67 AUDIO CODEC (2/2)			
Apple Inc.		DRAWING NUMBER	051-9584
		REVISION	2.0.0
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THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	10 OF 23
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		SHEET	10 OF 46
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CG FLEX B2B

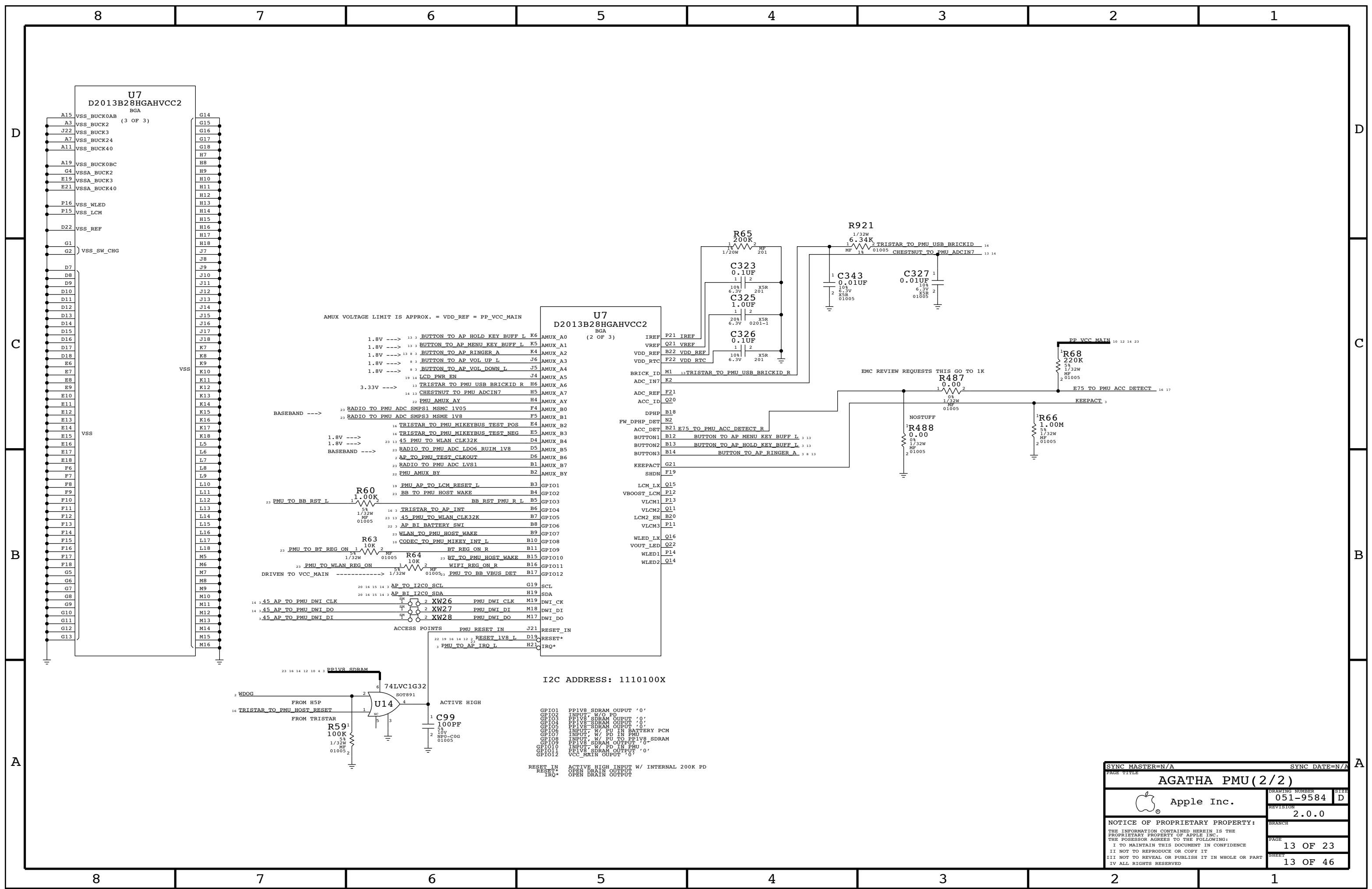
(FF CAM, PROX, ALS, RECEIVER, ANC ERROR MIC)



PAGE TITLE		SYNC DATE=N/A	
CG FLEX B2B			
Apple Inc.	DRAWING NUMBER	051-9584	SIZE D
	REVISION	2.0.0	
NOTICE OF PROPRIETARY PROPERTY:			BRANCH
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:			PAGE
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE			11 OF 23
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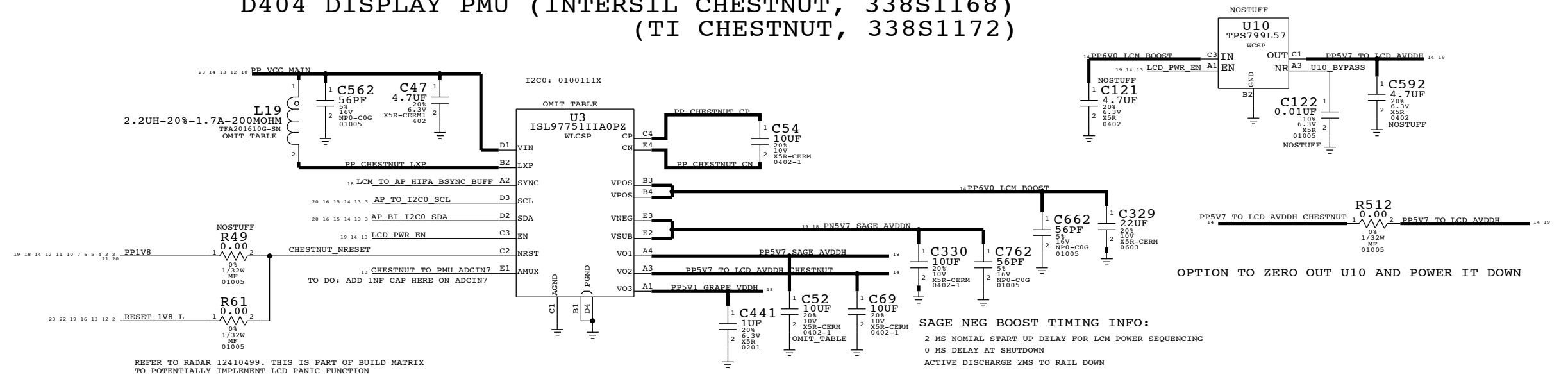
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AGATHA PMU (1/2)			
Apple Inc.	DRAWING NUMBER	051-9584	SIZE
	REVISION	2.0.0	
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		PAGE	12 OF 23
		SHEET	12 OF 46



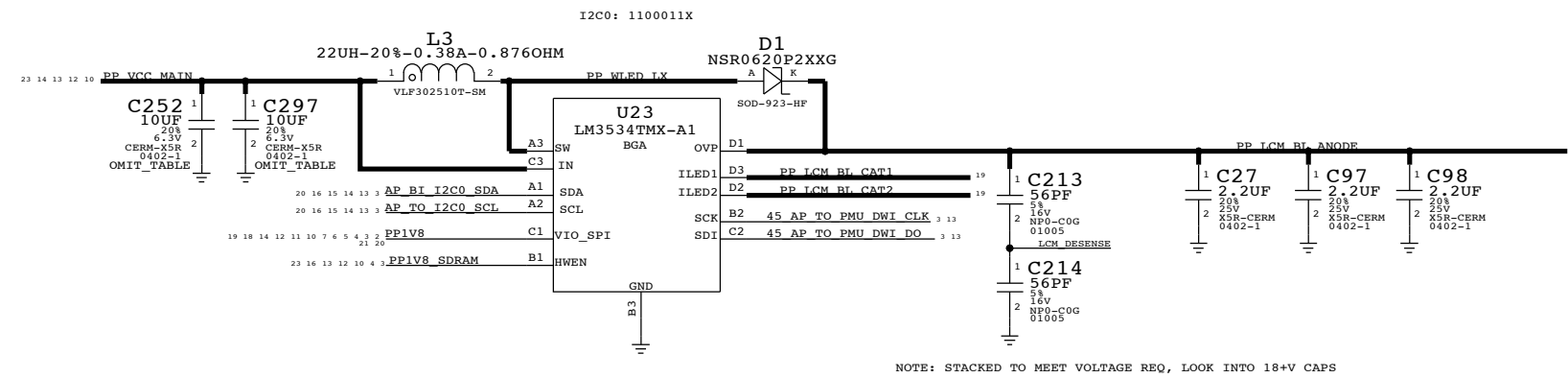
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Apple Inc.		DRAWING NUMBER	051-9584	SIZE	D
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PAGE		13 OF 23		SHEET	
		13 OF 46			

CHESTNUT, BACKLIGHT DRIVER

D404 DISPLAY PMU (INTERSIL CHESTNUT, 338S1168) (TI CHESTNUT, 338S1172)



D404 BACKLIGHT DRIVER

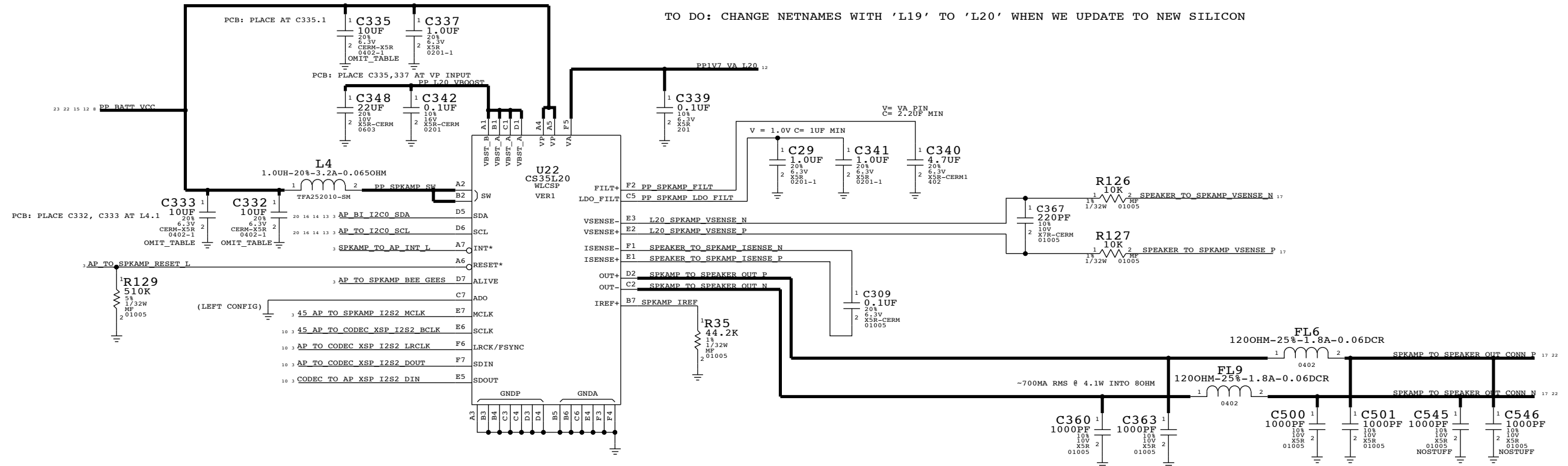


PAGE TITLE		SYNC DATE=N/A	
CHESTNUT + BACKLIGHT DRIVER			
DRAWING NUMBER		051-9584	SIZE D
REVISION		2.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSSESSOR AGREES TO THE FOLLOWING:		PAGE	
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		14 OF 23	
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SPEAKER AMP, LED DRIVER

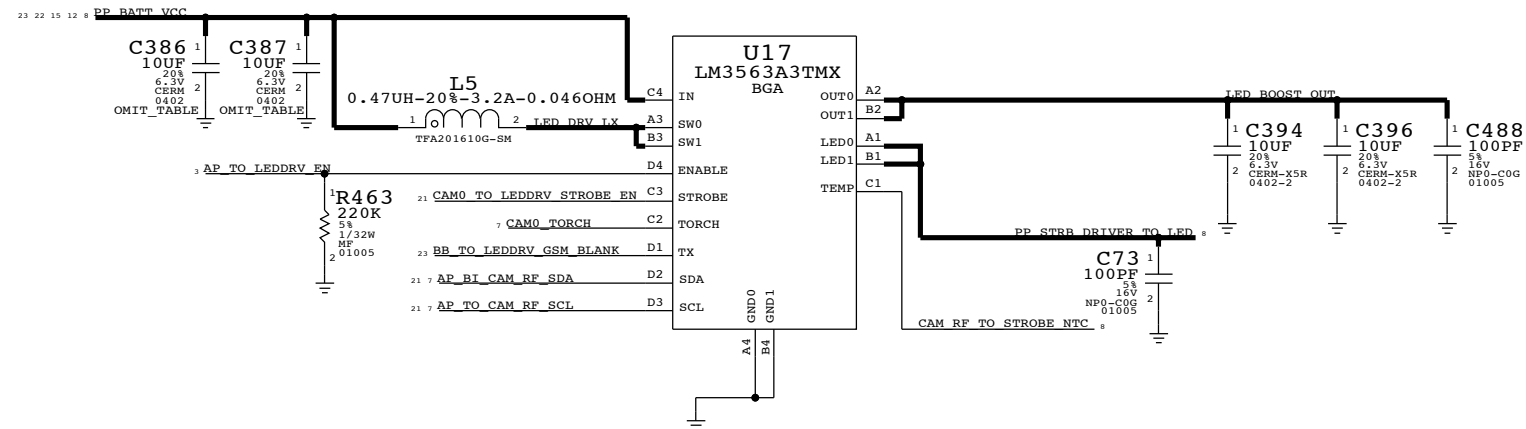
SPEAKER AMP (REPLACED WITH L20)

I2C ADDRESS: 1000000X



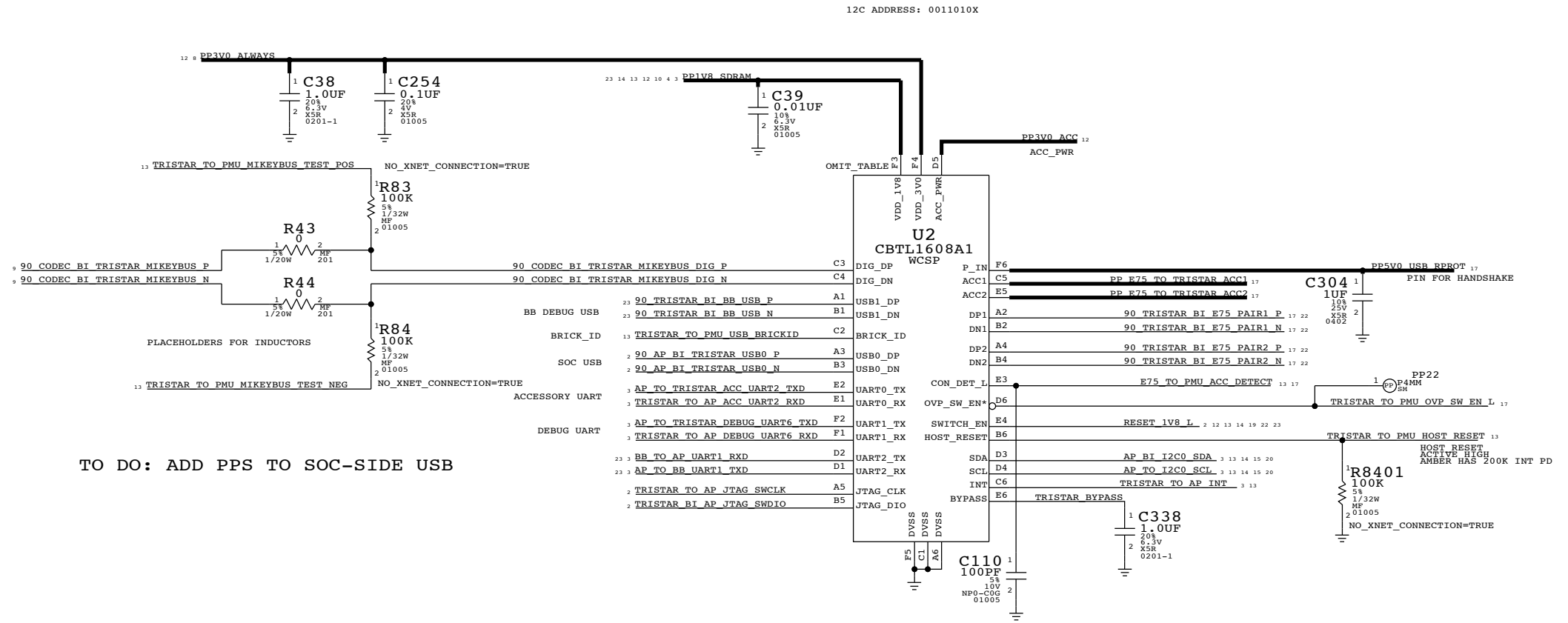
LED DRIVER

I2C ADDRESS: 1100011X




SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
SPKR AMP + LED DRIVER			
DRAWING NUMBER		051-9584	
REVISION		2.0.0	
NOTICE OF PROPRIETARY PROPERTY:		BRANCH	
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I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE		15 OF 23	
II NOT TO REPRODUCE OR COPY IT		SHEET	
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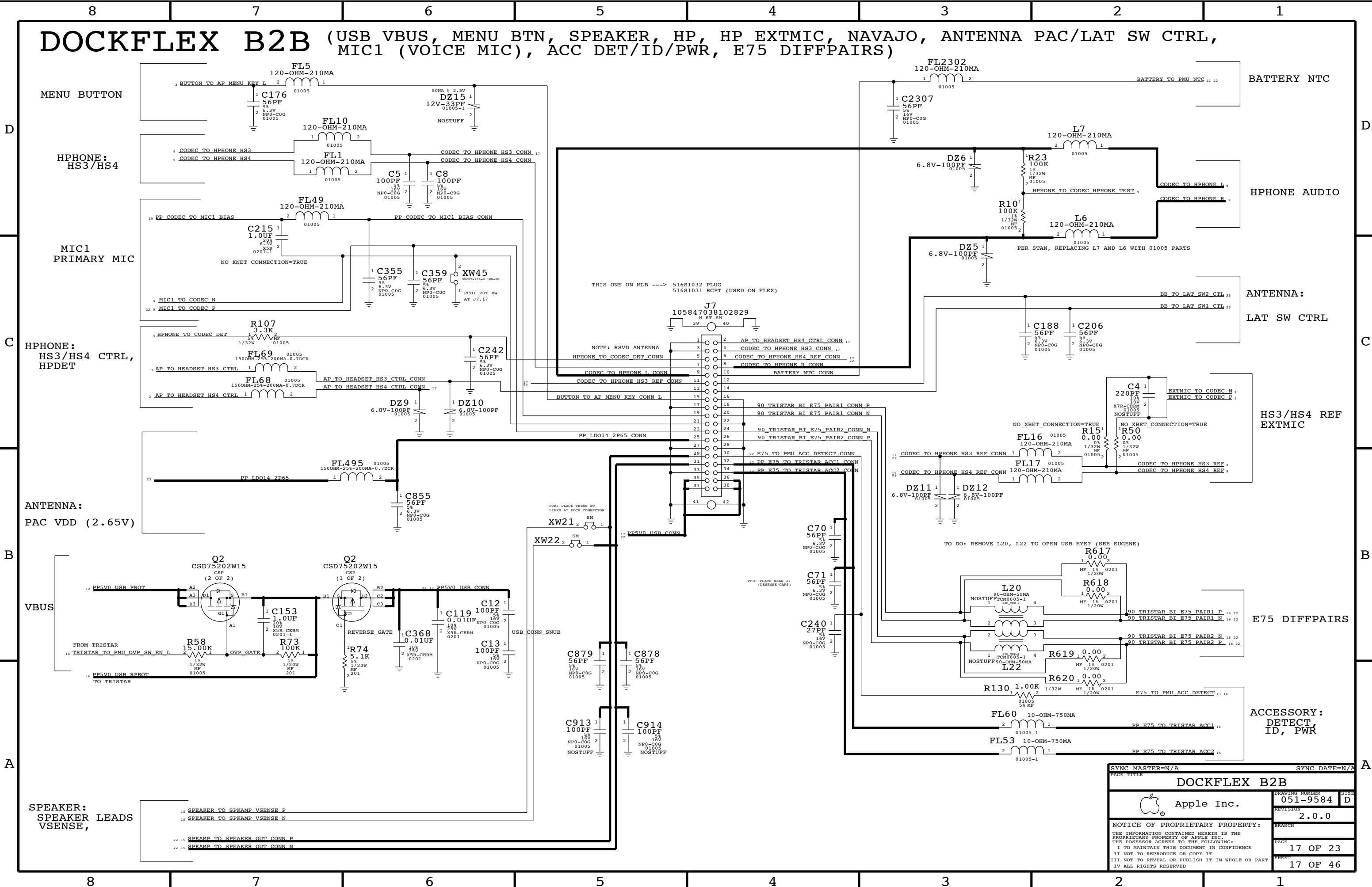
TRISTAR



TO DO: ADD PPS TO SOC-SIDE USB

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE			
TRISTAR			
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		REVISION	2.0.0
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		PAGE	16 OF 23
		SHEET	16 OF 46

DOCKFLEX B2B (USB VBUS, MENU BTN, SPEAKER, HP, HP EXTMIC, NAVAJO, ANTENNA PAC/LAT SW CTRL, MIC1 (VOICE MIC), ACC DET/ID/PWR, E75 DIFFPAIRS)



SYNC MASTER=N/A		SYNC DATE=N/A	
DOCKFLEX B2B			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	
		2.0.0	
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		PAGE	
		17	23
		SHEET	
		17	46

D404 (B2B, DRIVER ICS)

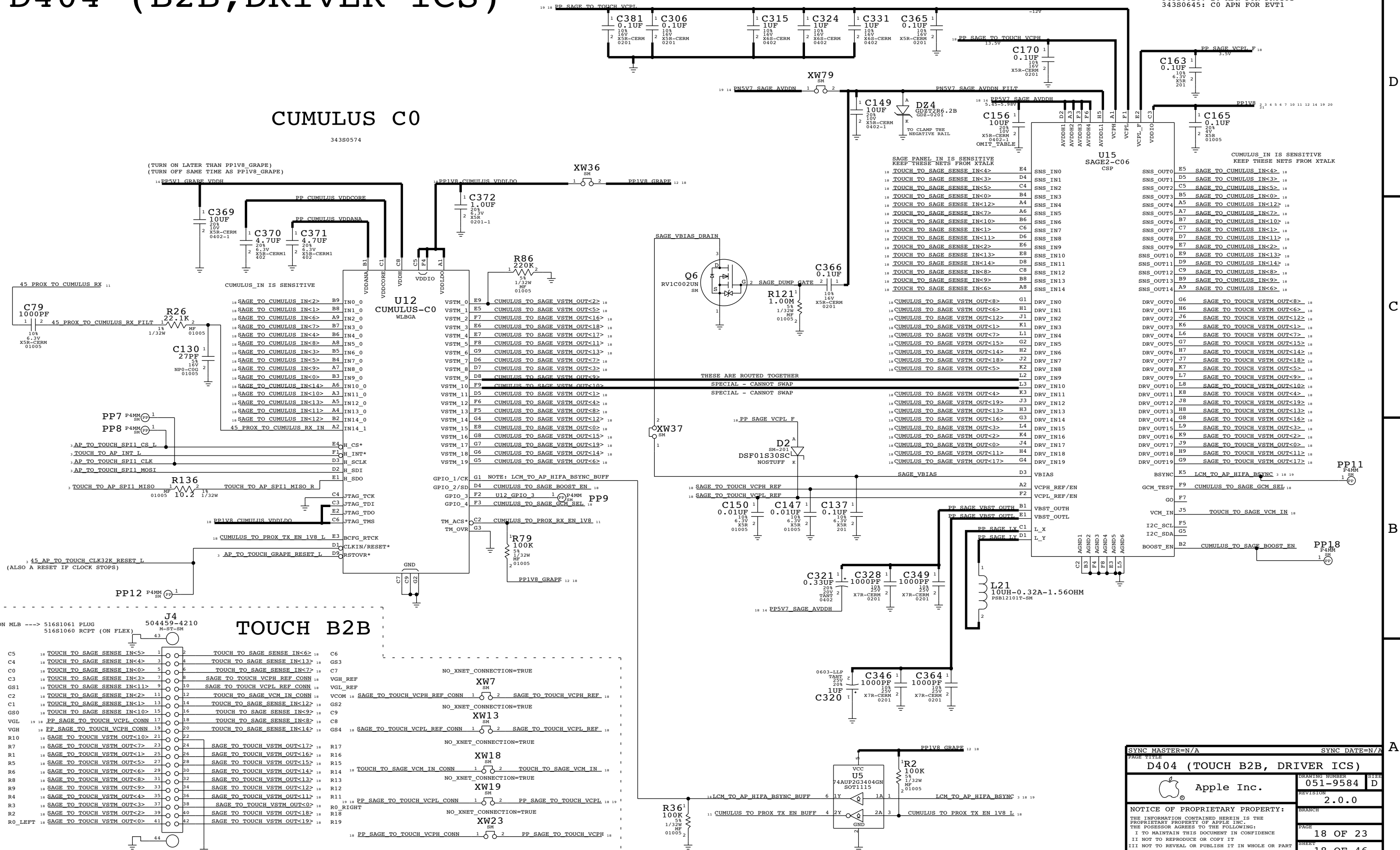
SAGE2 C0

343S0628: B0 APN FOR PROTO1
343S0645: C0 APN FOR EVT1

CUMULUS C0

343S0574

(TURN ON LATER THAN PPIV8_GRAPE)
(TURN OFF SAME TIME AS PPIV8_GRAPE)



TOUCH B2B

504459-4210

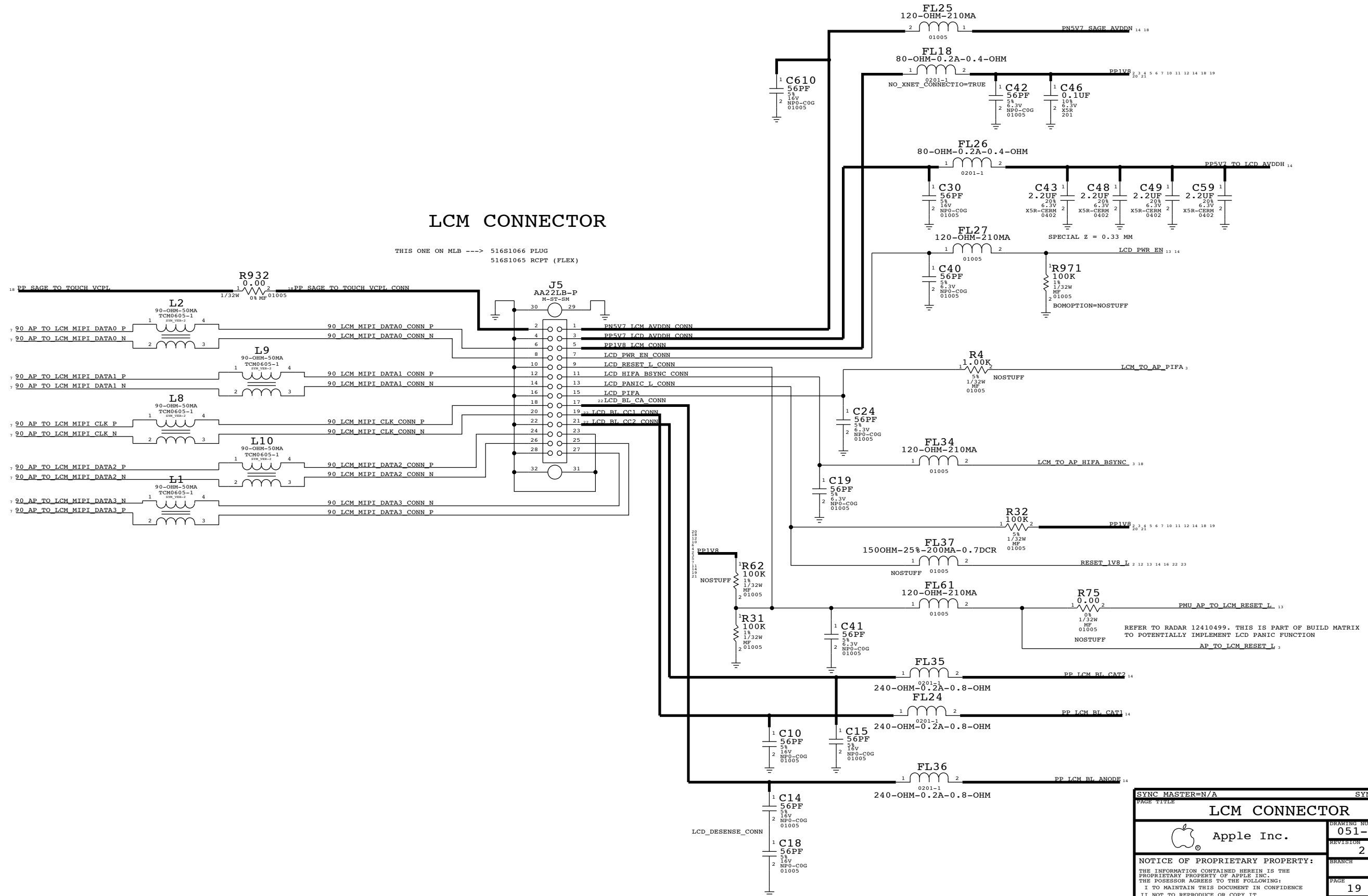
TOUCH B2B	CUMULUS C0
TOUCH TO SAGE SENSE IN<5>	B9 IN0_0
TOUCH TO SAGE SENSE IN<4>	B8 IN1_0
TOUCH TO SAGE SENSE IN<0>	A9 IN2_0
TOUCH TO SAGE SENSE IN<3>	B7 IN3_0
TOUCH TO SAGE SENSE IN<11>	B6 IN4_0
TOUCH TO SAGE SENSE IN<2>	A8 IN5_0
TOUCH TO SAGE SENSE IN<1>	B5 IN6_0
TOUCH TO SAGE SENSE IN<10>	B4 IN7_0
TOUCH TO SAGE SENSE IN<9>	A7 IN8_0
PP SAGE TO TOUCH VCPL_CONN	B3 IN9_0
PP SAGE TO TOUCH VCPH_CONN	A6 IN10_0
SAGE TO TOUCH VSTM OUT<10>	A3 IN11_0
SAGE TO TOUCH VSTM OUT<7>	B2 IN12_0
SAGE TO TOUCH VSTM OUT<1>	A5 IN13_0
SAGE TO TOUCH VSTM OUT<5>	B1 IN14_0
SAGE TO TOUCH VSTM OUT<8>	A4 IN15_0
SAGE TO TOUCH VSTM OUT<9>	B0 IN16_0
SAGE TO TOUCH VSTM OUT<4>	A2 IN17_0
SAGE TO TOUCH VSTM OUT<3>	B0 IN18_0
SAGE TO TOUCH VSTM OUT<2>	A1 IN19_0
SAGE TO TOUCH VSTM OUT<0>	B0 IN20_0

SYNC MASTER=N/A	SYNC DATE=N/A
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D404 (TOUCH B2B, DRIVER ICS)	
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BRANCH	PAGE: 18 OF 23
SHEET	18 OF 46

LCM B2B

LCM CONNECTOR

THIS ONE ON MLB ----> 516S1066 PLUG
516S1065 RCPT (FLEX)



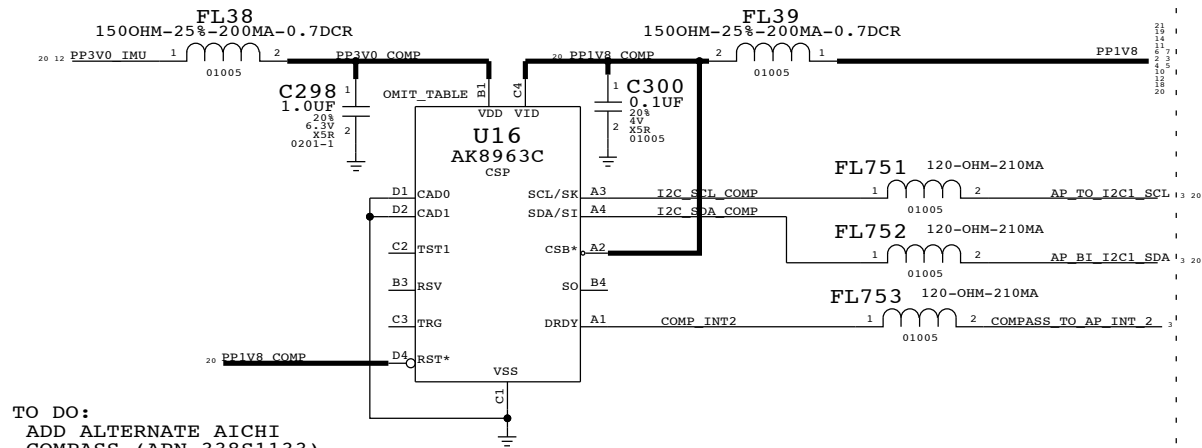
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LCM CONNECTOR			
		DRAWING NUMBER	051-9584
		REVISION	2.0.0
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		PAGE	19 OF 23
		SHEET	19 OF 46

SENSORS

THIS PART OUTSIDE OF SHIELD

COMPASS

COMPASS DEVICE: 338S1014
COMPASS INTERPOSER: 998-5120

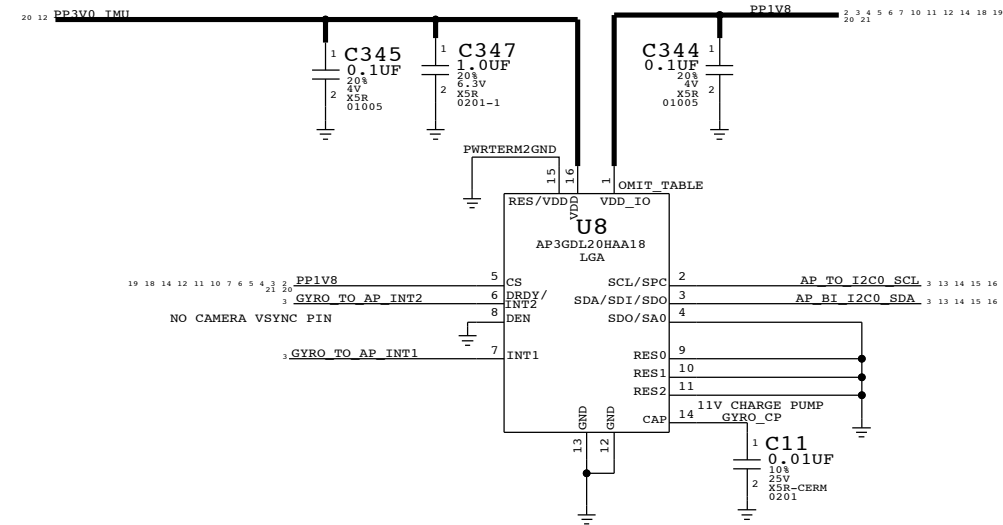


TO DO:
ADD ALTERNATE AICHI
COMPASS (APN 338S1133)

THESE PARTS INSIDE OF SHIELD

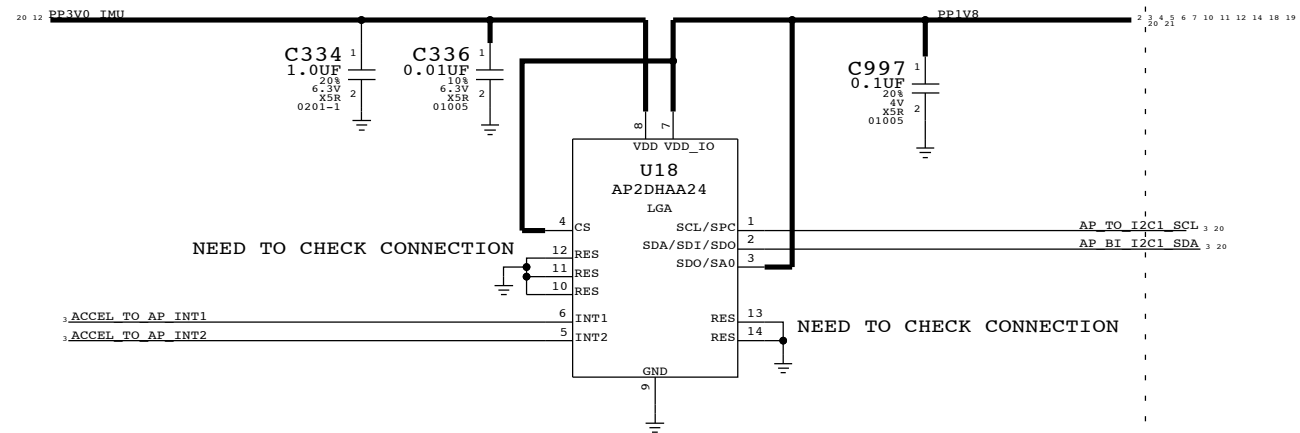
GYRO

AP3GDL20H, APN 338S1158



ACCELEROMETER

AP2DHAA, APN 338S1114



TO DO: VERIFY CONNECTIONS ON ACCEL (CS, SDO PINS)

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE OSCAR + SENSORS			
Apple Inc.	DRAWING NUMBER	051-9584	SIZE D
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		SHEET	20 OF 46

CAM0: MAIN CAMERA CONNECTOR

8 7 6 5 4 3 2 1

D

D

C

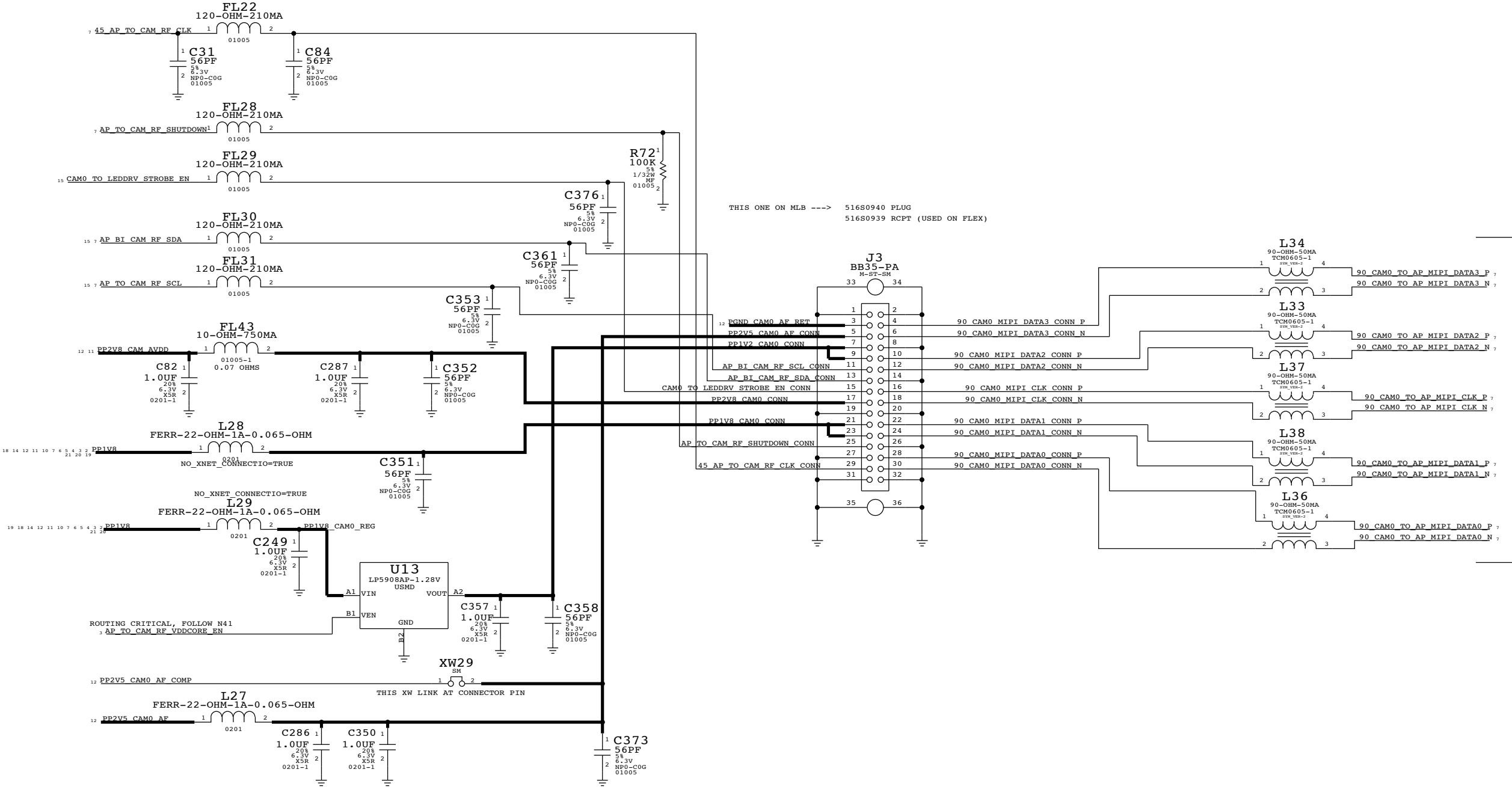
C

B

B

A

A



THIS ONE ON MLB ----> 516S0940 PLUG
516S0939 RCPT (USED ON FLEX)

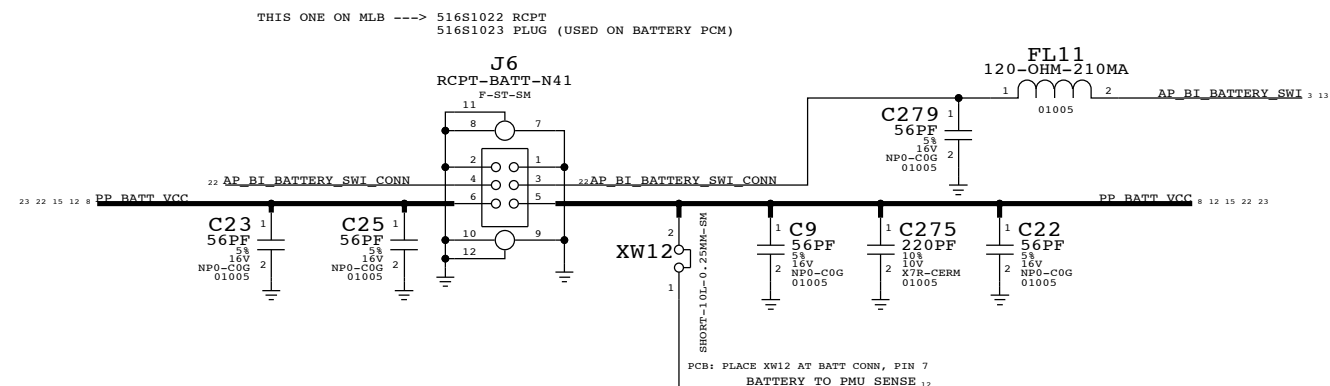
CAM0:
4-LANE MIPI

SYNC MASTER=N/A		SYNC DATE=N/A	
CAM0 CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	21 OF 23
		SHEET	21 OF 46

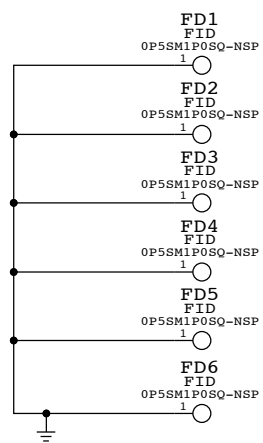
8 7 6 5 4 3 2 1

BATT CONN, TPS, STANDOFFS/SHIELDS/FIDUCIALS

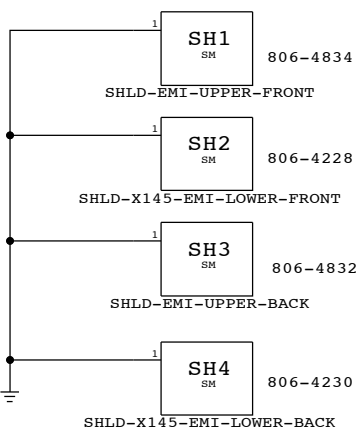
BATTERY CONN



FIDUCIALS

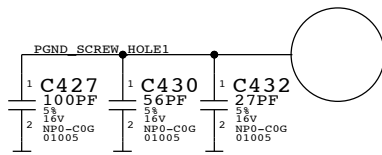


SHIELDS

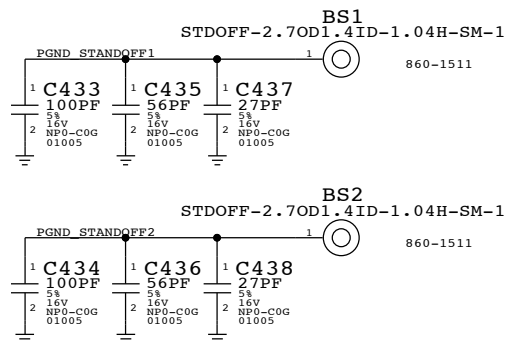


AC COUPLED SCREW HOLES + STANDOFFS (ON NORTH END OF SINGLE_BRD, TO MITIGATE COMPASS RETURN CURRENTS)

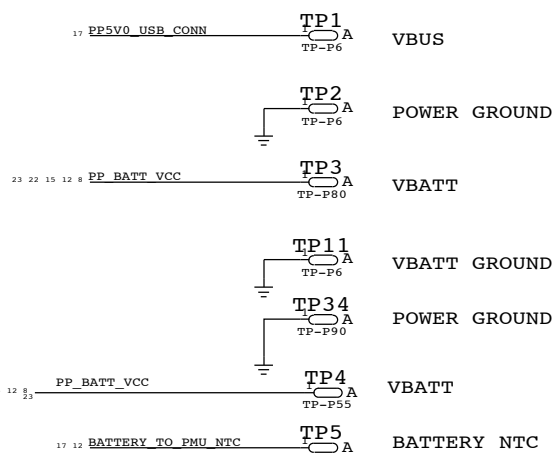
SCREW HOLES



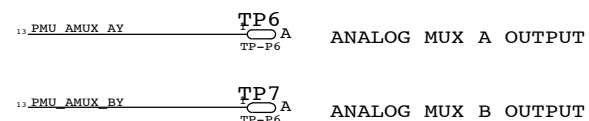
STANDOFFS



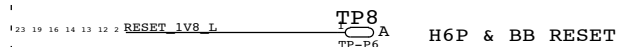
POWER TP



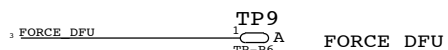
SUPER TP



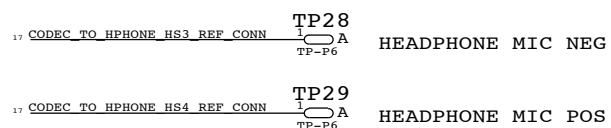
RESET



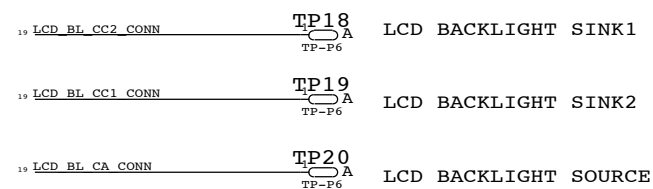
DFU



HEADPHONE MIC

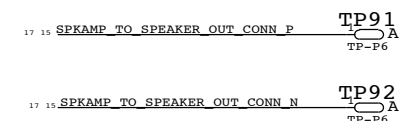


LCM BACKLIGHT

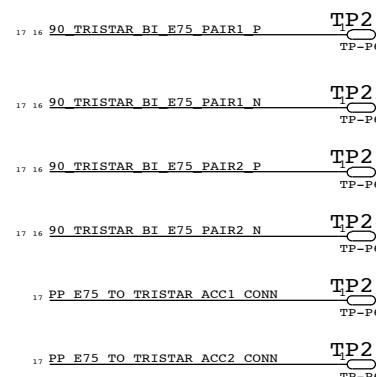


TESTPOINTS

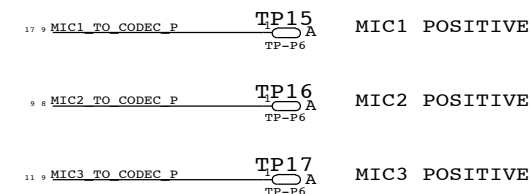
SPKAMP OUTPUT TP



E75 - USB/UART/ID/POWER



MIC AUDIO



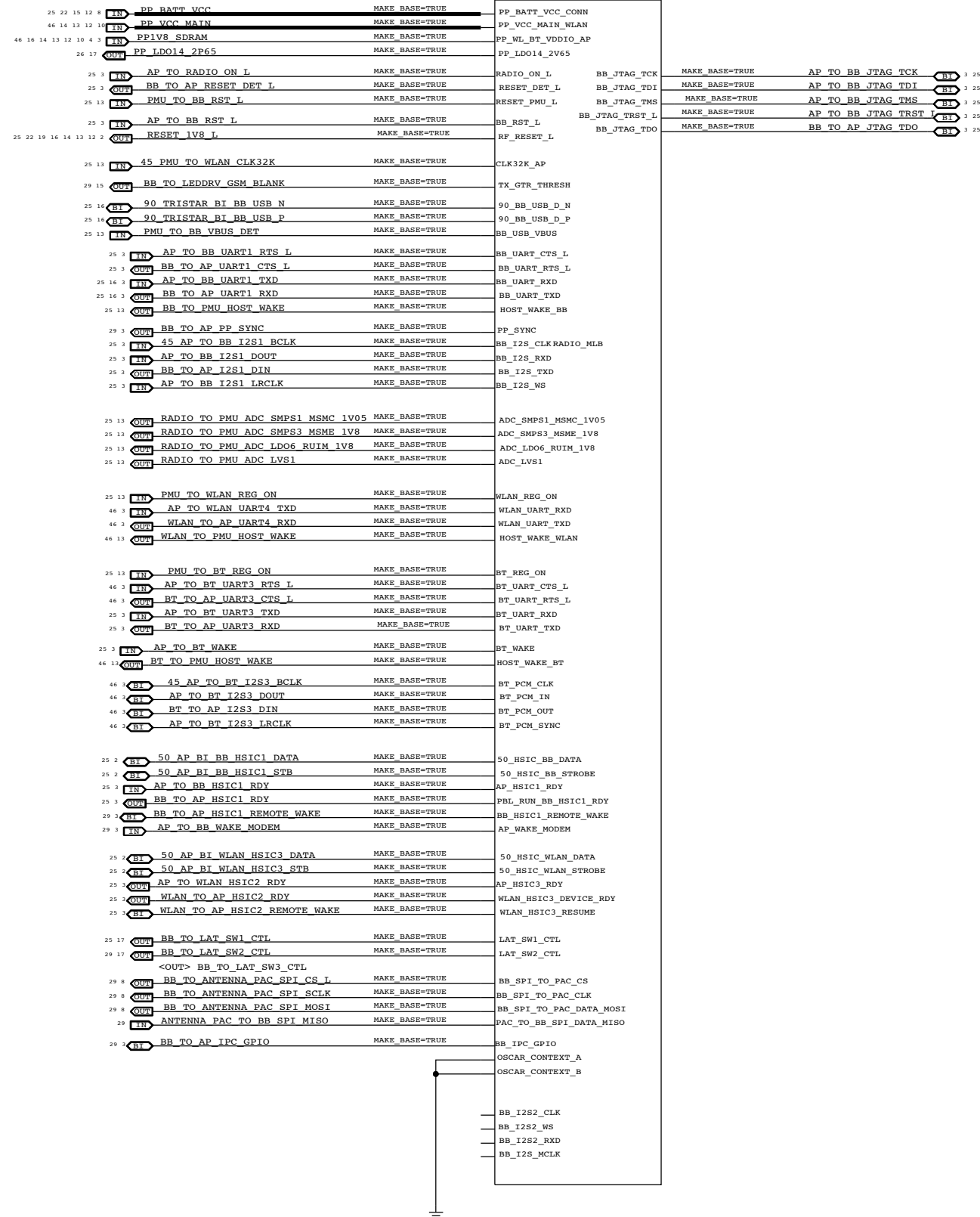
DRIVE MIC WRT NEAREST GROUND TEST POINT

SYNC MASTER=N/A		SYNC DATE=N/A	
BATT B2B, TPS, PD FEATURES			
Apple Inc.		DRAWING NUMBER 051-9584	SIZE D
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		BRANCH	SHEET 22 OF 46

RADIO_MLB HIERARCHICAL SYMBOL

AP/RADIO INTERFACE

RF
I612



SYNC MASTER=N/A		SYNC DATE=N/A	
RADIO_MLB HIERARCH. SYMBOL			
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		23 OF 23	
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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
2	0001669557	ENGINEERING RELEASED		2012-10-14

X155 RADIO_MLB SUBDESIGN - PROTO1

10/3/2012


PDF PAGE	CONTENTS
2	AP INTERFACE & DEBUG CONNECTORS
3	CELLULAR PMU: (1 OF 2)
4	CELLULAR PMU: (2 OF 2)
5	CELLULAR BASEBAND: (1 OF 2)
6	CELLULAR BASEBAND: (2 OF 2)
7	CELLULAR RF TRANSCEIVER: (1 OF 2)
8	CELLULAR RF TRANSCEIVER: (2 OF 2)
9	CELLULAR FRONT END: TX AND RX MATCHING
10	CELLULAR FRONT END: SAW BANKS
11	CELLULAR FRONT END: BAND 1/4 PAT
12	CELLULAR FRONT END: BAND 2/3 PAD
13	CELLULAR FRONT END: BAND 20 PAD
14	CELLULAR FRONT END: BAND 5/8 PAD
15	CELLULAR FRONT END: BAND 13/17 PAD
16	CELLULAR FRONT END: PA DCDC CONVERTER
17	CELLULAR FRONT END: 2G FEM
18	CELLULAR FRONT END: RX DIVERSITY
19	CELLULAR FRONT END: GPS LNA
20	CELLULAR FRONT END: ANTENNA FEEDS
21	FRONT END LOGIC TABLE (1 OF 2)
22	FRONT END LOGIC TABLE (2 OF 2)
23	WIFI/BT: MODULE AND FRONT END

BOARD ID BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0621	1	1.00M 1% 01005	R25_RF	Y	N51_CFG_A
118S0732	1	50K 1% 01005	R26_RF	Y	N51_CFG_A
117S0159	1	470K 5% 01005	R25_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_A
118S0726	1	162K 1% 01005	R26_RF	Y	N53_CFG_A
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_B
118S0623	1	267K 1% 01005	R26_RF	Y	N53_CFG_B
118S0659	1	255K 1% 01005	R25_RF	Y	N48_CFG_A
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_A
118S0689	1	147K 1% 01005	R25_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N49_CFG_A
118S0650	1	499K 1% 01005	R26_RF	Y	N49_CFG_A
118S0732	1	50K 1% 01005	R25_RF	Y	N49_CFG_B
118S0621	1	1.00M 1% 01005	R26_RF	Y	N49_CFG_B

SCH : 951-2446
 BOM : 939-0308
 BOARD : 920-2148

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
951-2446	1	X145_RADIO_MLB	SCH	Y	
825-2029	1	EEE FOR 939-0308	EEEE_????	Y	NA

DRAWING TITLE		X155 RADIO_MLB SCHEMATIC	
 Apple Inc.	DRAWING NUMBER	051-9584	SIZE
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		SHEET	24 OF 46

AP INTERFACE & DEBUG CONNECTORS

AP CONNECTIONS

IN = FROM AP
OUT = TO AP

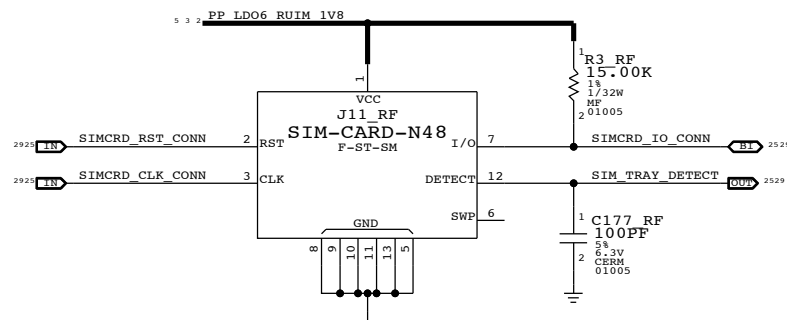
- 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
- PP BATT VCC CONN
- PP VCC MAIN WLAN
- TX GTR THRESH
- BB_RST_L
- RESET_DET_L
- RADIO_ON_L
- RESET_PMU_L
- HOST_WAKE_BB
- RF_RESET_L
- PBL_RUN_BB_HSI1_RDY
- WLAN_HSI3_RESUME
- AP_WAKE_MODEM
- AP_HSI1_RDY
- 50_HSI1_BB_DATA
- 50_HSI1_BB_STROBE
- BB_HSI1_REMOTE_WAKE
- BB_UART_TXD
- BB_UART_RXD
- BB_UART_RTS_L
- BB_UART_CTS_L
- BB_USB_VBUS
- 90_BB_USB_D_P
- 90_BB_USB_D_N
- BB_I2S_CLK
- BB_I2S_WS
- BB_I2S_TXD
- BB_I2S_RXD
- PP_SYNC
- PP_WL_BT_VDDIO_AP
- CLK32K_AP
- WLAN_REG_ON
- WLAN_UART_TXD
- WLAN_UART_RXD
- HOST_WAKE_WLAN
- WLAN_HSI3_DEVICE_RDY
- AP_HSI3_RDY
- 50_HSI1_WLAN_DATA
- 50_HSI1_WLAN_STROBE
- HOST_WAKE_BT
- BT_UART_TXD
- BT_UART_RXD
- BT_UART_RTS_L
- BT_UART_CTS_L
- BT_REG_ON
- BT_PCM_CLK
- BT_PCM_SYNC
- BT_PCM_OUT
- BT_PCM_IN
- LAT_SW1_CTL
- LAT_SW2_CTL
- BB_SPT_TO_PAC_CS
- BB_SPT_TO_PAC_DATA_MOST
- BB_SPT_TO_PAC_CLK
- PAC_TO_BB_SPT_DATA_MISO
- PP_LDO14_2V65
- BB_JTAG_TCK
- BB_JTAG_TDI
- BB_JTAG_TMS
- BB_JTAG_TRST_L
- BB_JTAG_TDO
- ADC_SMPS1_MSMC_1V05
- ADC_SMPS3_MSME_1V8
- ADC_LDO6_RUIM_1V8
- ADC_LVS1
- BB_IPC_GPIO
- OSCAR_CONTEXT_A
- OSCAR_CONTEXT_B
- BB_I2S2_CLK
- BB_I2S2_WS
- BB_I2S_MCLK
- BB_I2S2_RXD

PROBE POINTS

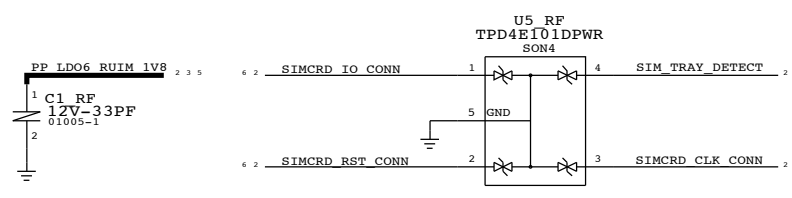
- PP1 RF P4MM 1 BB_ERROR_FLAG
- PP2 RF P4MM 1 SLEEP_CLK_32K
- PP3 RF P4MM 1 PMIC_SSB1
- PP10 RF P4MM-NSM 1 19F2M_MDM
- PP11 RF P4MM 1 CLK32K_AP
- PP14 RF P4MM 1 AP_HSI3_RDY
- PP15 RF P4MM 1 WLAN_HSI3_DEVICE_RDY
- PP16 RF P4MM 1 WLAN_HSI3_RESUME
- PP19 RF P4MM-NSM 1 WTR_SSB1_TX_GPS
- PP20 RF P4MM-NSM 1 WTR_SSB1_PRX_DRX
- PP21 RF P4MM 1 WTR_RX_ON
- PP22 RF P4MM 1 WTR_RF_ON
- PP40 RF P4MM 1 WLAN_COEX_TXD
- PP41 RF P4MM 1 LTE_COEX_TXD
- PP42 RF P4MM 1 50_HSI1_BB_STROBE
- PP43 RF P4MM 1 50_HSI1_BB_DATA
- PP44 RF P4MM 1 50_HSI1_WLAN_STROBE
- PP45 RF P4MM 1 50_HSI1_WLAN_DATA
- PP46 RF P4MM 1 BT_UART_TXD
- PP47 RF P4MM 1 BT_UART_RXD

- PP4 RF P4MM 1 BB_I2S_CLK
- PP5 RF P4MM 1 BB_I2S_WS
- PP6 RF P4MM 1 BB_I2S_RXD
- PP7 RF P4MM 1 BB_I2S_TXD

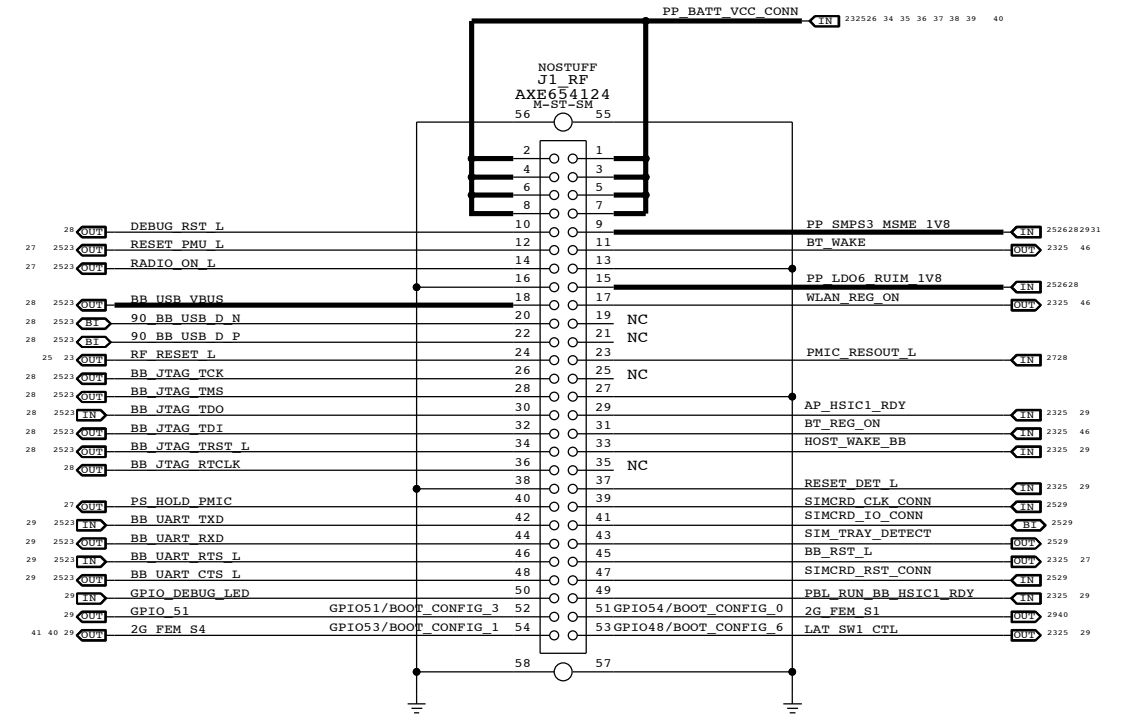
SIM CARD CONNECTOR



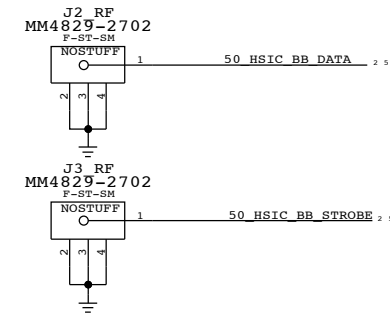
SIM CARD ESD PROTECTION



DEBUG CONNECTOR



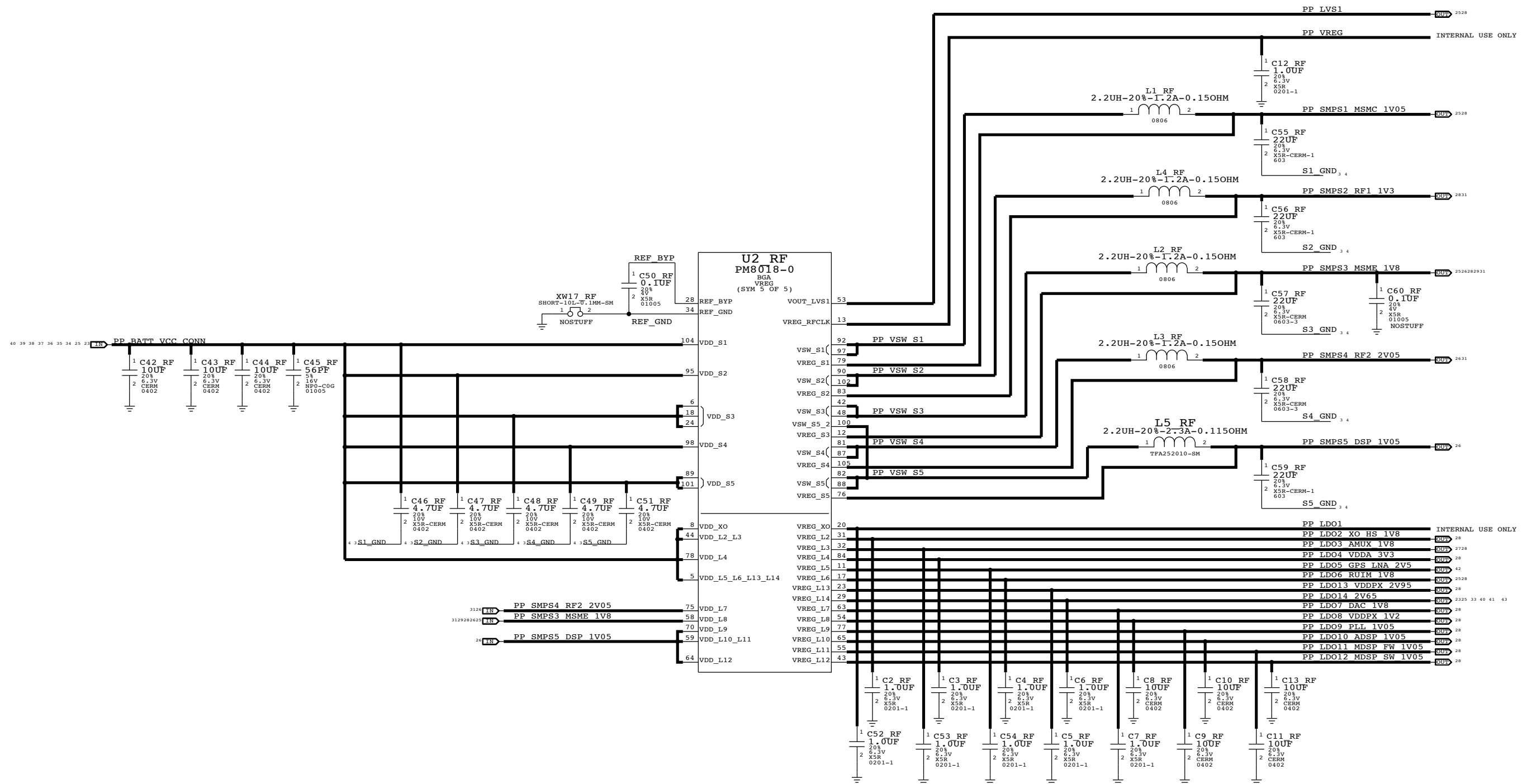
BOOT OPTIONS	BOOT CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION								
		6	5	4	3	2	1	0		
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	1	X
BOOT_HSI1_OPTION	0X02	X	1	0	0	0	0	0	1	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1	X
ENABLE_SAHARA_PROTOCOL	0X08	X	1	0	0	1	0	X	X	X



- PP SMPS1_MSMC_1V05
- PP SMPS3_MSME_1V8
- PP_LDO6_RUIM_1V8
- PP_LVS1
- XW12 RF SHORT-10L-0.1MM-SM 1 2 ADC_SMPS1_MSMC_1V05
- XW13 RF SHORT-10L-0.1MM-SM 1 2 ADC_SMPS3_MSME_1V8
- XW14 RF SHORT-10L-0.1MM-SM 1 2 ADC_LDO6_RUIM_1V8
- XW15 RF SHORT-10L-0.1MM-SM 1 2 ADC_LVS1

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SHEET		25 OF 46		

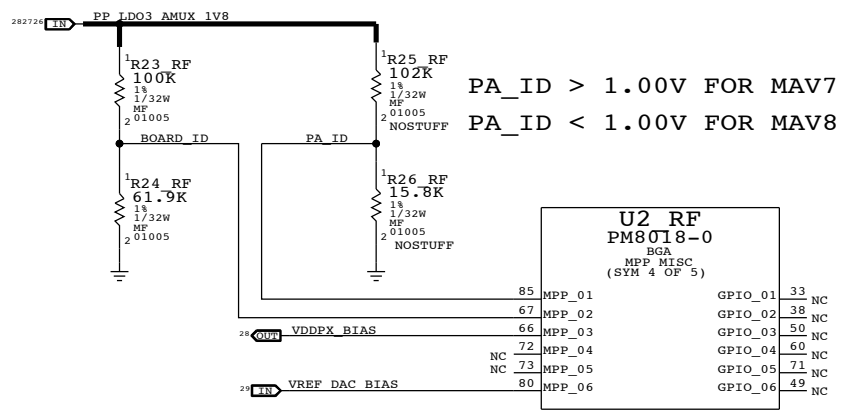
PMU (1 OF 2)



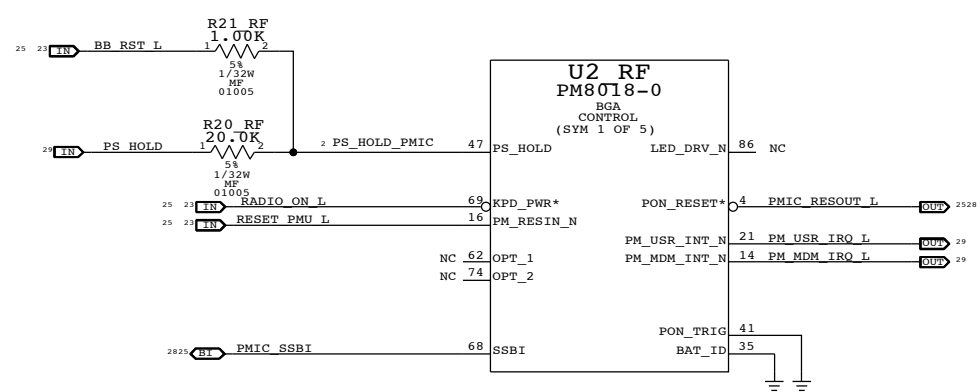
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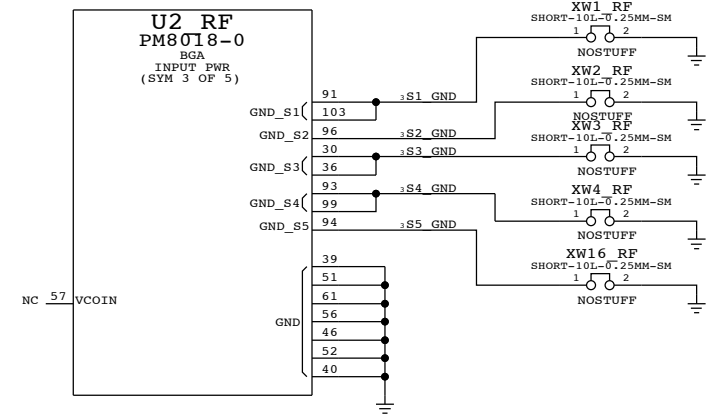
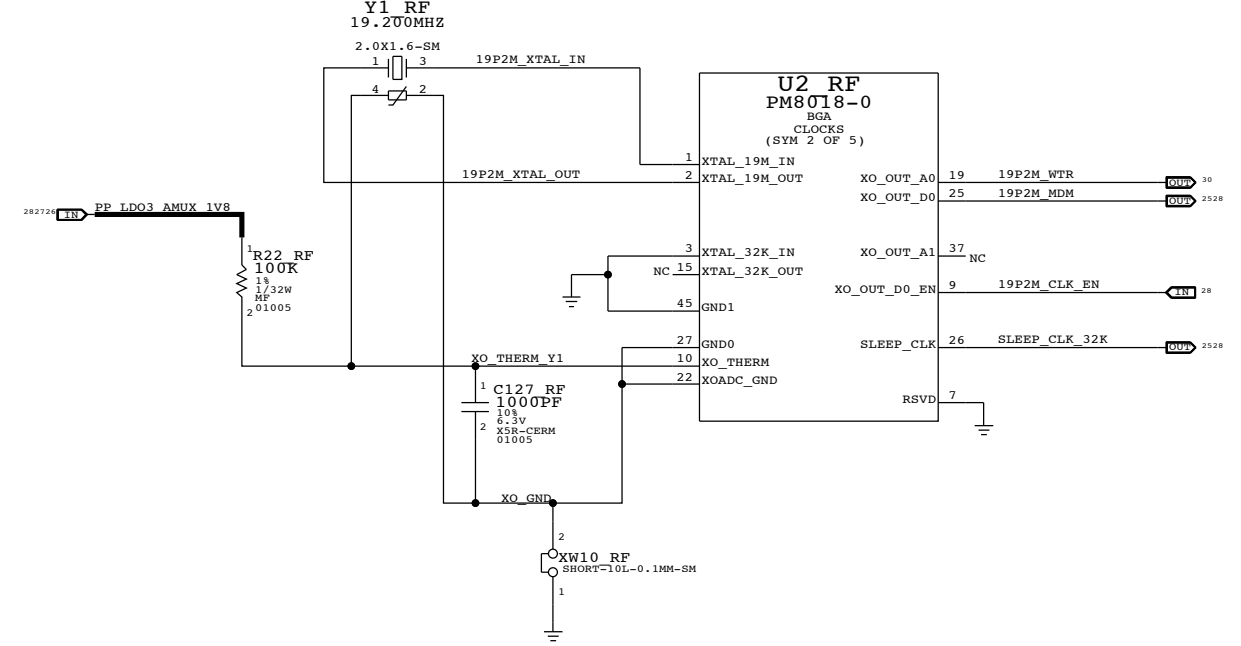
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT



PA THERMISTOR REMOVED TO MATCH N41, AP SECTION
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.

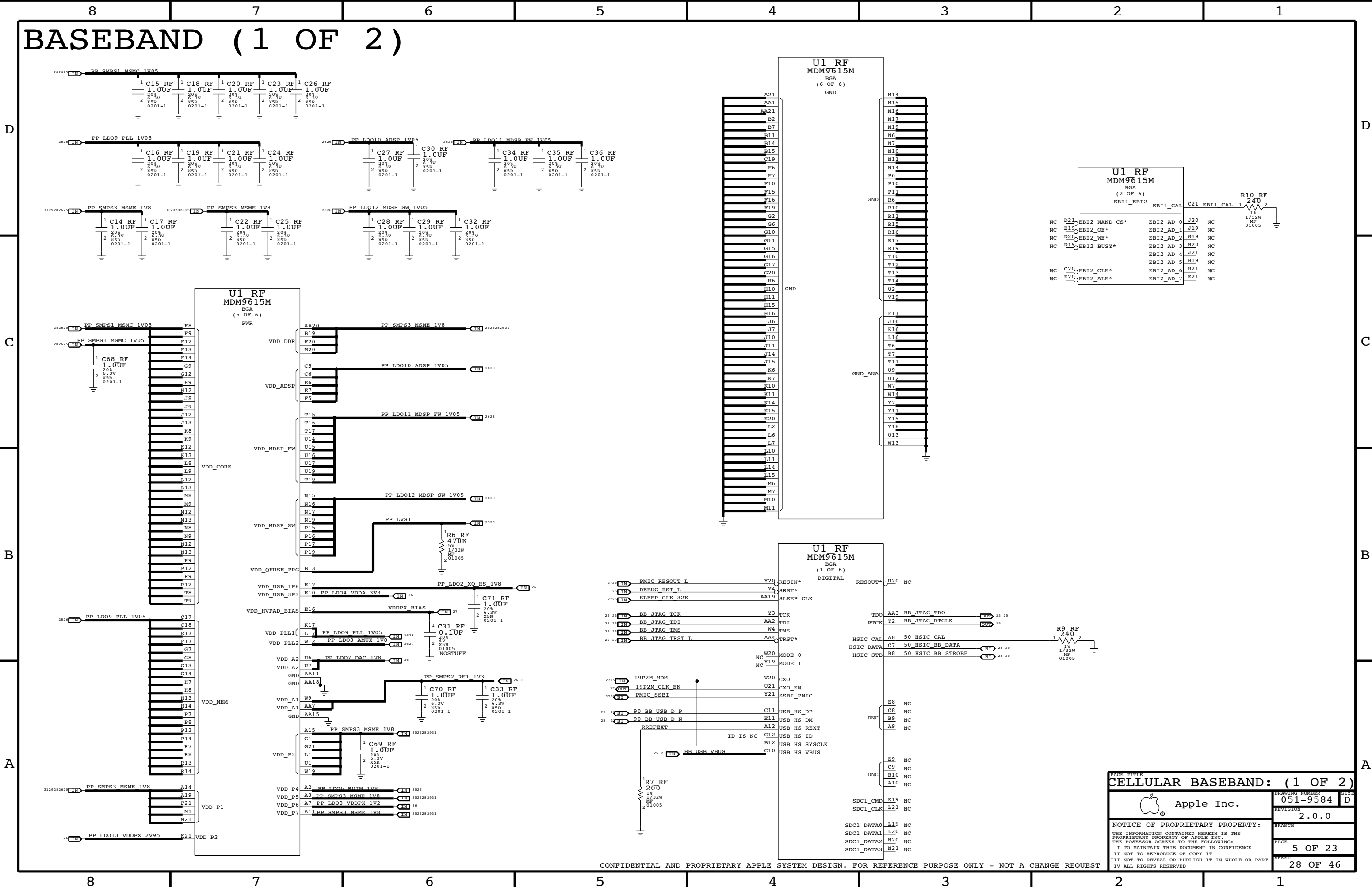


GND NEEDS TO BE CLEARED UNDER THIS CRYSTAL
TO MINIMIZE THERMAL DRIFT



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BASEBAND (1 OF 2)



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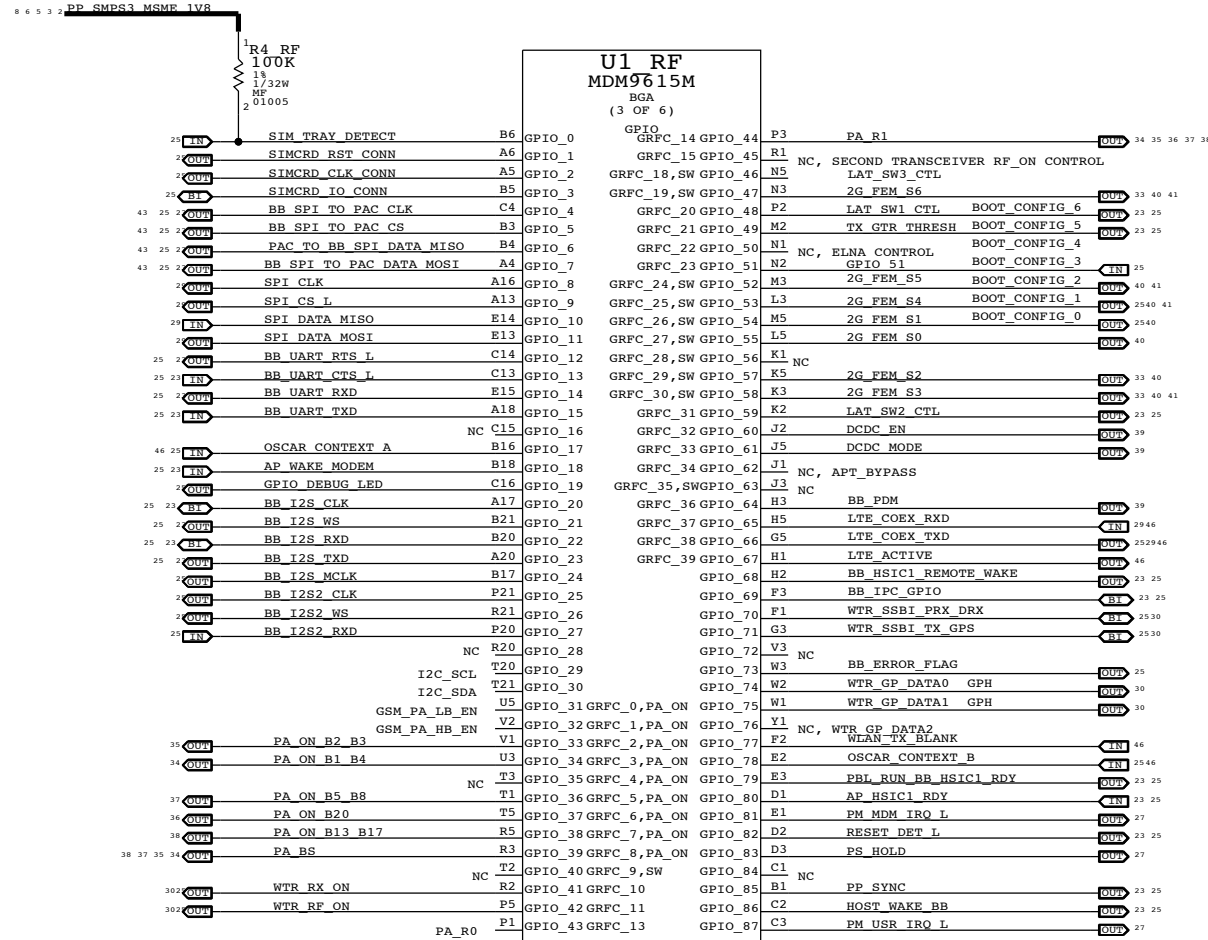
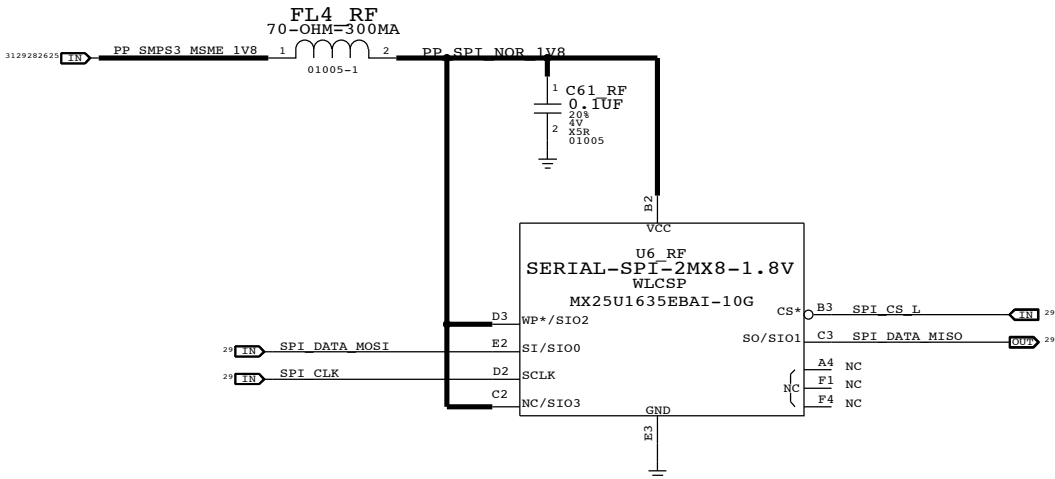
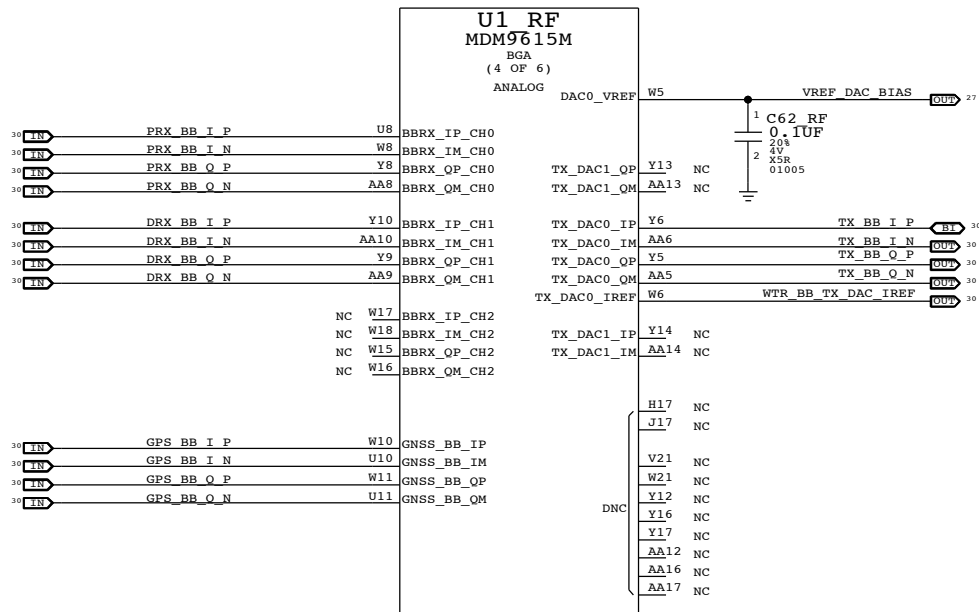
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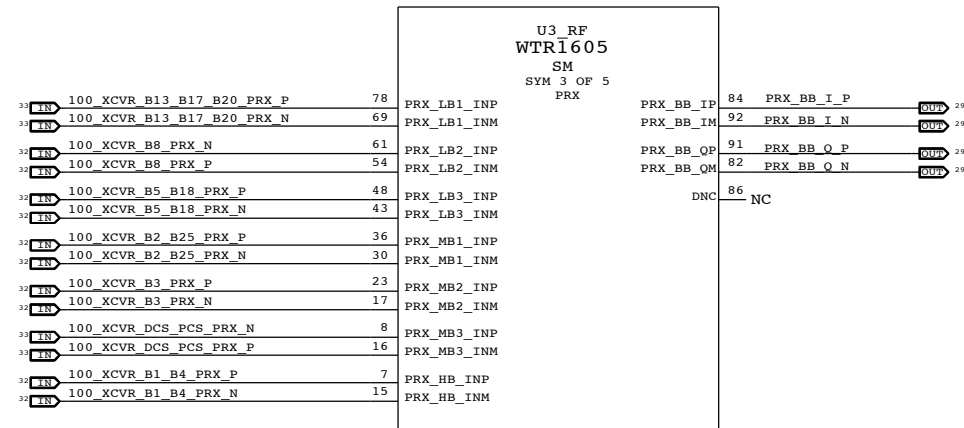


LTE WLAN PRIORITY [ALIAS] LTE COEX_RXD [PIN] 2946
 LTE FRAME SYNC [ALIAS] LTE COEX_TXD [PIN] 252946

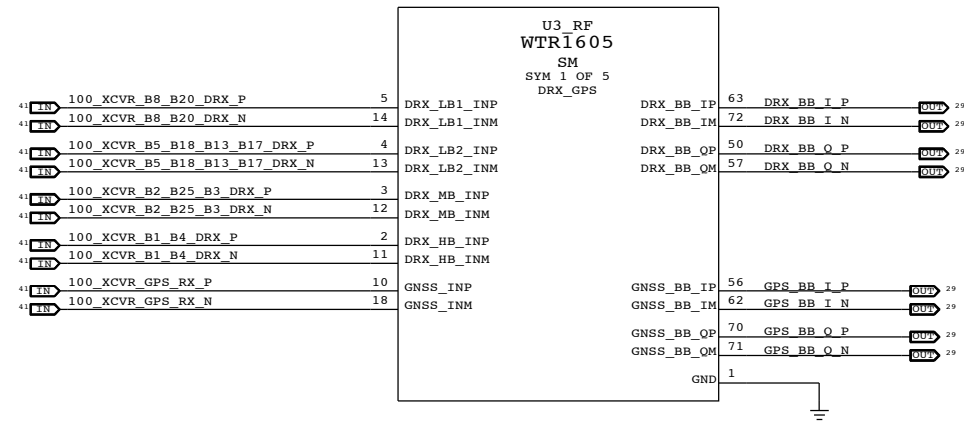
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RF TRANSCEIVER (1 OF 4)

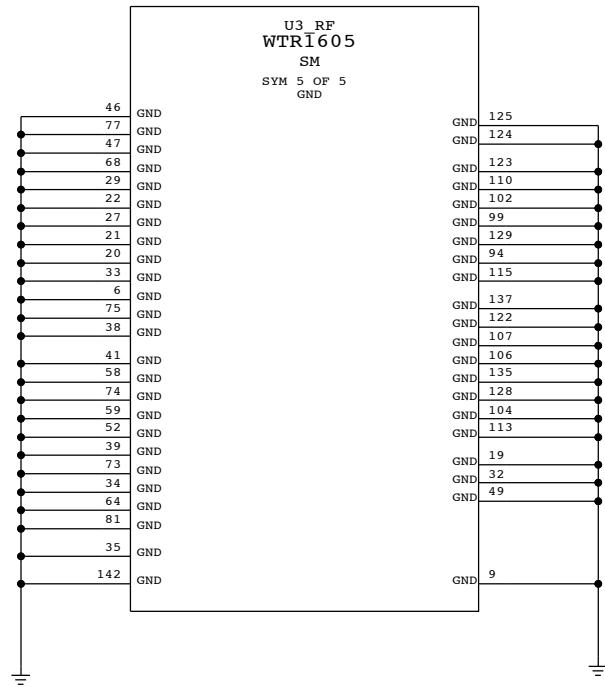
PRX TRANSCEIVER RF AND IQ PORTS



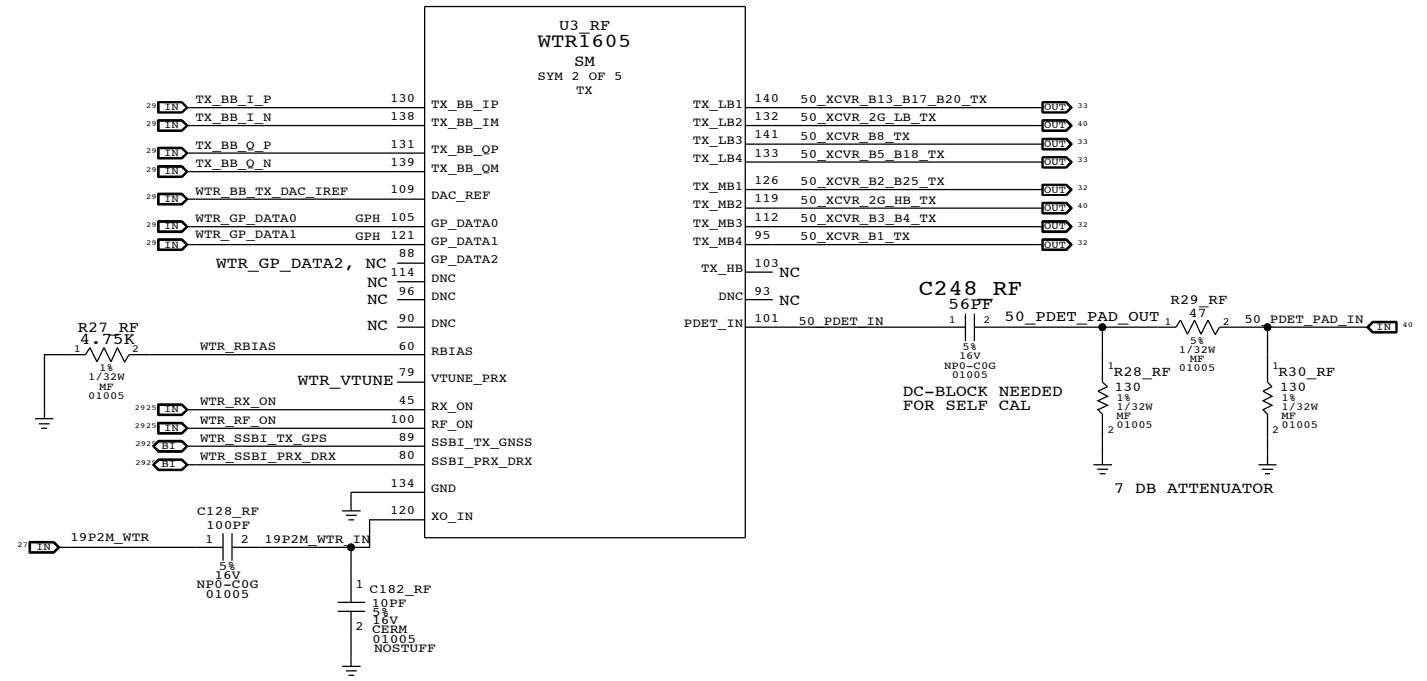
DRX TRANSCEIVER RF AND IQ PORTS



TRANSCEIVER GROUND CONNECTIONS



TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



CELLULAR RF TRANSCEIVER: (1 OF 2)

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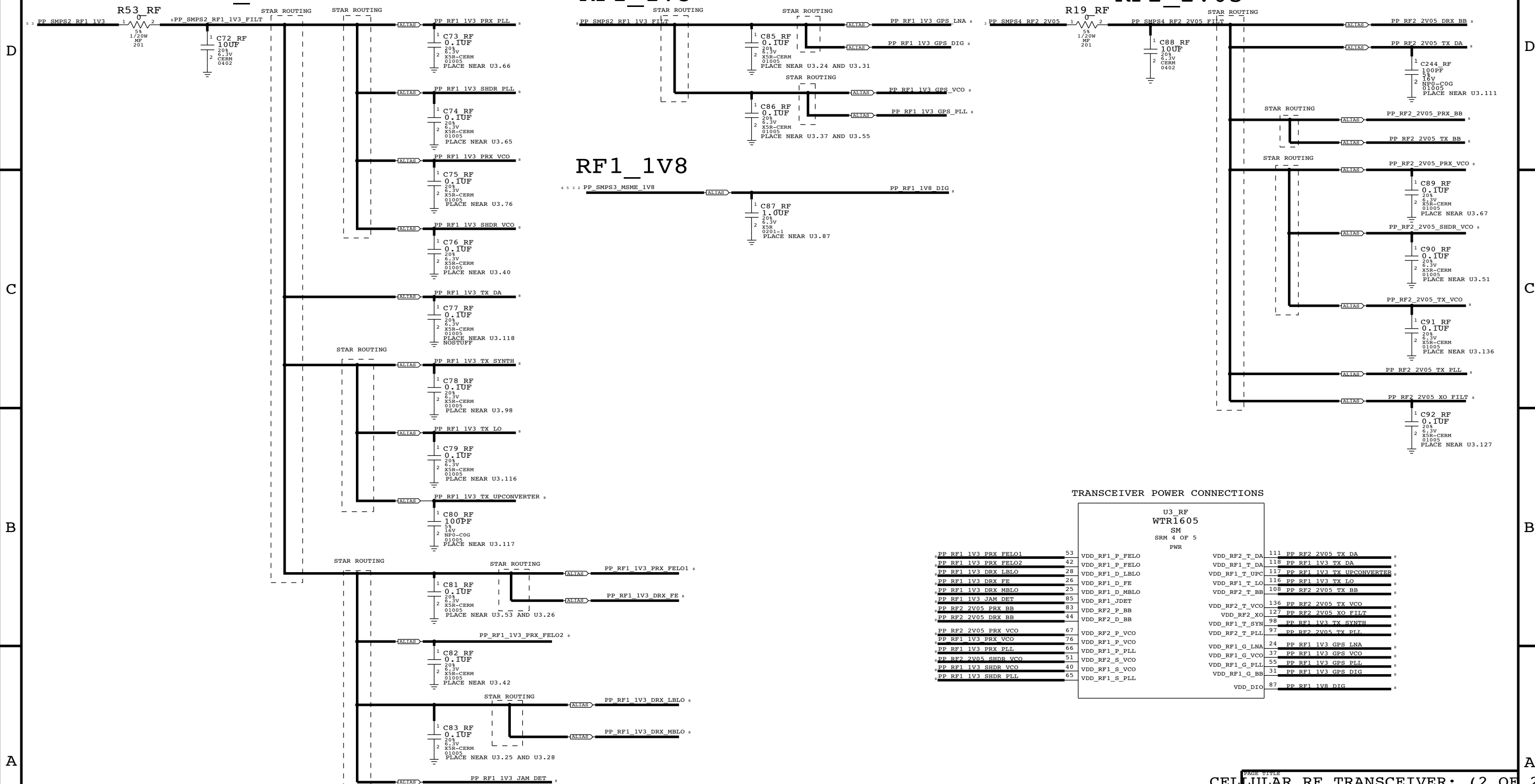
RF TRANSCEIVER (2 OF 2)

RF1_1V3

RF1_1V3

RF2_2V05

RF1_1V8



TRANSCEIVER POWER CONNECTIONS

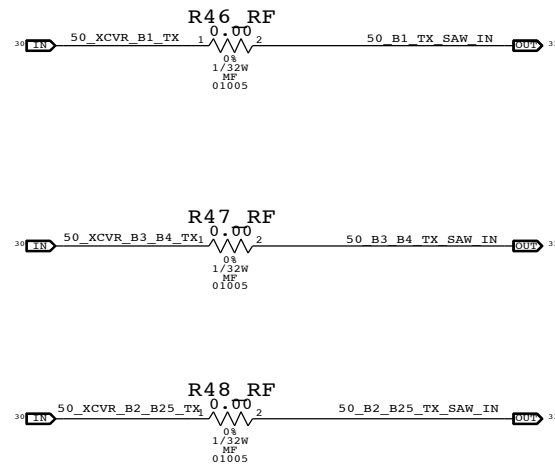
U3_RF		WTR1605		SM		SRM 4 OF 5		PWR	
PP RF1 1V3 PRX FELO1	53	VDD_RF1_P_FELO		VDD_RF2_T_DA	111	PP RF2 2V05 TX DA			
PP RF1 1V3 PRX FELO2	42	VDD_RF1_P_FELO		VDD_RF1_T_DA	118	PP RF1 1V3 TX DA			
PP RF1 1V3 DRX LBLO	28	VDD_RF1_D_LBLO		VDD_RF1_T_UPC	117	PP RF1 1V3 TX UPCONVERTER			
PP RF1 1V3 DRX FE	26	VDD_RF1_D_FE		VDD_RF1_T_LO	116	PP RF1 1V3 TX LO			
PP RF1 1V3 DRX MBLO	25	VDD_RF1_D_MBLO		VDD_RF2_T_BB	108	PP RF2 2V05 TX BB			
PP RF1 1V3 JAM DET	85	VDD_RF1_JDET		VDD_RF2_T_VCO	136	PP RF2 2V05 TX VCO			
PP RF2 2V05 PRX BB	83	VDD_RF2_P_BB		VDD_RF2_XO	127	PP RF2 2V05 XO FILT			
PP RF2 2V05 DRX BB	44	VDD_RF2_D_BB		VDD_RF1_T_SYN	98	PP RF1 1V3 TX SYNTH			
PP RF2 2V05 PRX VCO	67	VDD_RF2_P_VCO		VDD_RF2_T_PLL	97	PP RF2 2V05 TX PLL			
PP RF1 1V3 PRX VCO	76	VDD_RF1_P_VCO		VDD_RF1_G_LNA	24	PP RF1 1V3 GPS LNA			
PP RF1 1V3 PRX PLL	66	VDD_RF1_P_PLL		VDD_RF1_G_VCO	37	PP RF1 1V3 GPS VCO			
PP RF2 2V05 SHDR VCO	51	VDD_RF2_S_VCO		VDD_RF1_G_PLL	55	PP RF1 1V3 GPS PLL			
PP RF1 1V3 SHDR VCO	40	VDD_RF1_S_VCO		VDD_RF1_G_BB	31	PP RF1 1V3 GPS DIG			
PP RF1 1V3 SHDR PLL	55	VDD_RF1_S_PLL		VDD_DIO	87	PP RF1 1V8 DIG			

CELLULAR RF TRANSCEIVER: (2 OF 2)

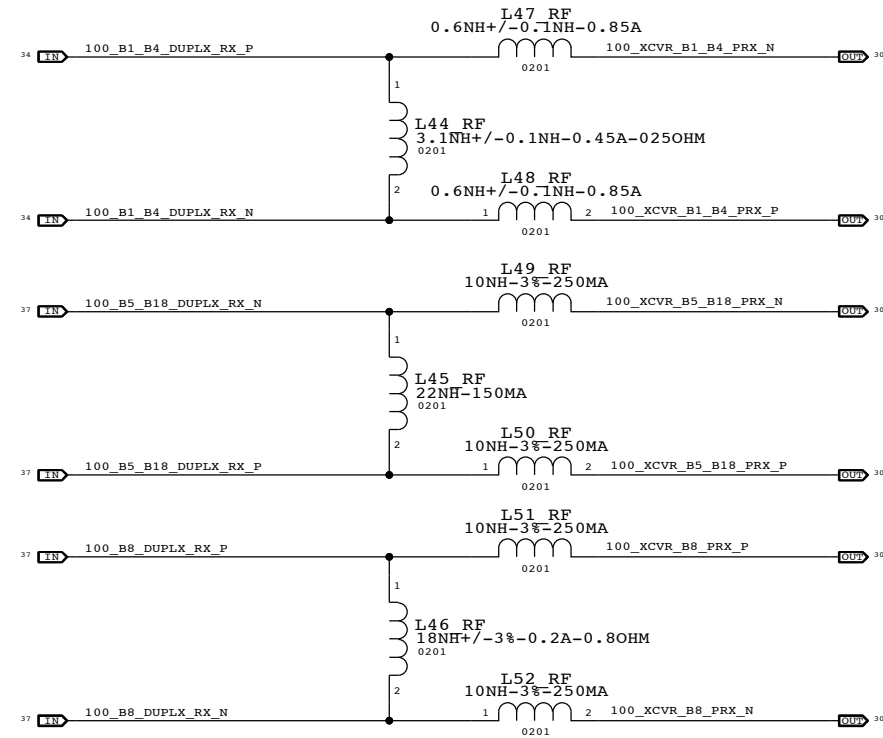
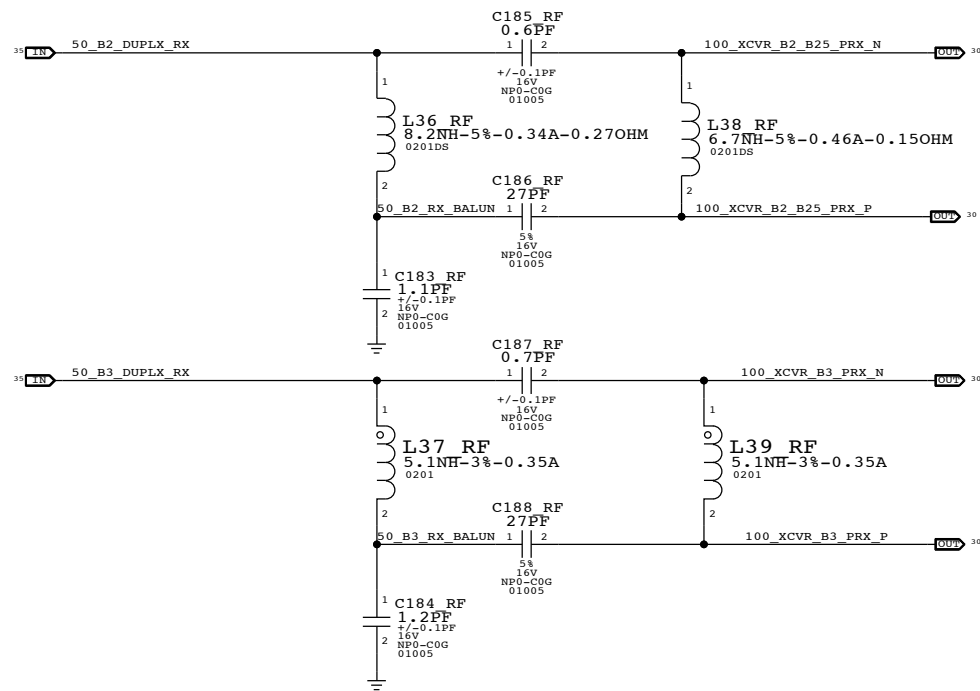
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TRANSCEIVER TX AND RX MATCHING

TX MATCHING NETWORKS



RX MATCHING NETWORKS



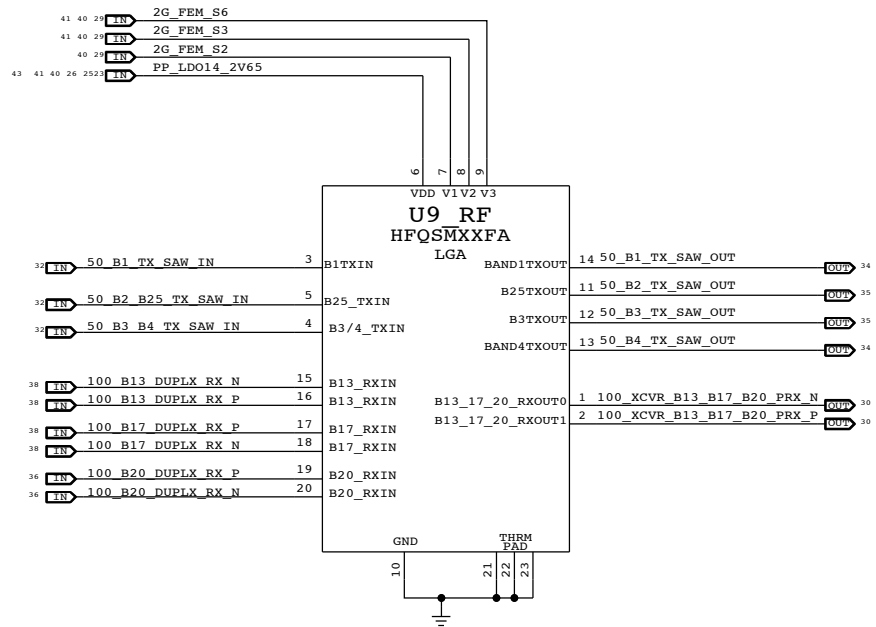
CELLULAR FRONT END: TX AND RX MATCHING

PAGE TITLE		DRAWING NUMBER	
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		32 OF 46	

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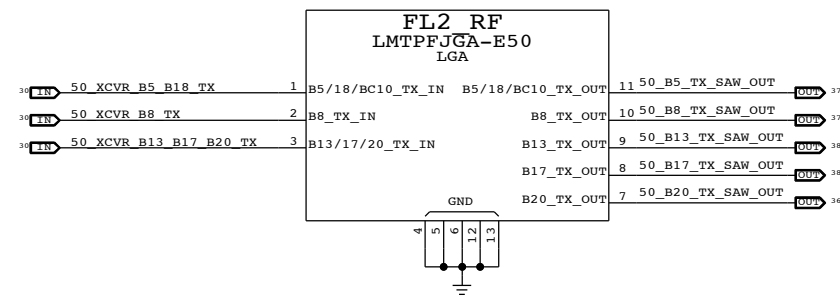
SAW BANKS

HB TX SAW BANK + B13/B17/B20 DP6T SWITCH AND MATCHING

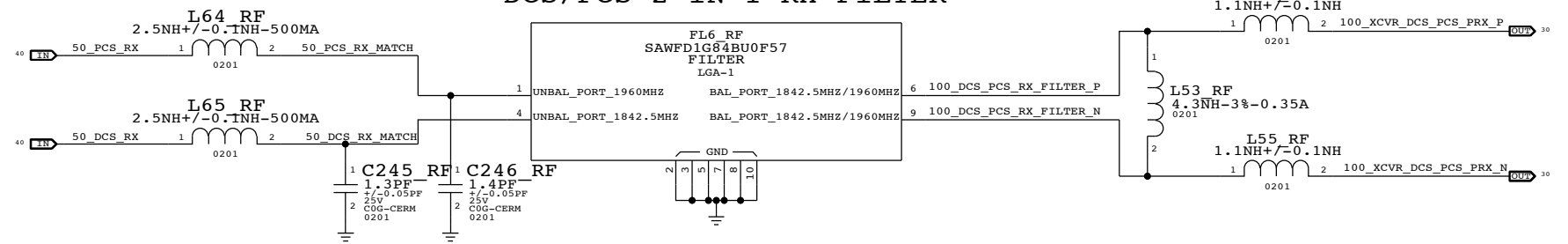


BAND	S6	S3	S2
B3 TX	HIGH	X	X
B4 TX	LOW	X	X
B13 RX	X	HIGH	HIGH
B17 RX	X	HIGH	LOW
B20 RX	X	LOW	HIGH

LB TX SAW BANK



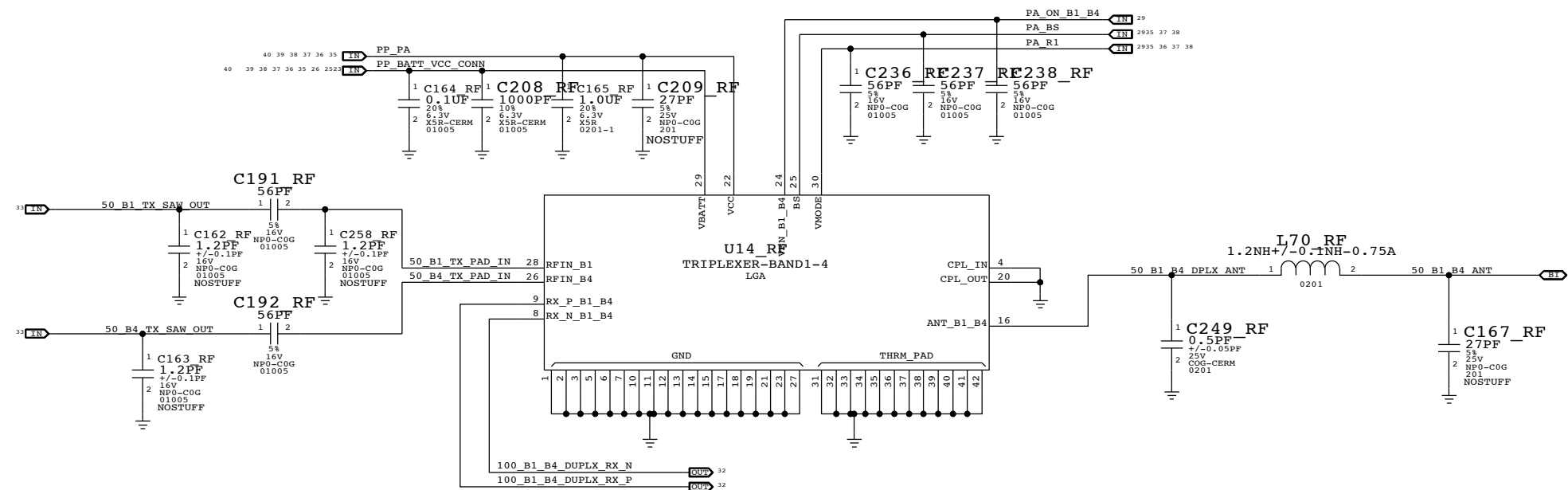
DCS/PCS 2-IN-1 RX FILTER



CELLULAR FRONT END: SAW BANKS

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BAND 1/4 PAT



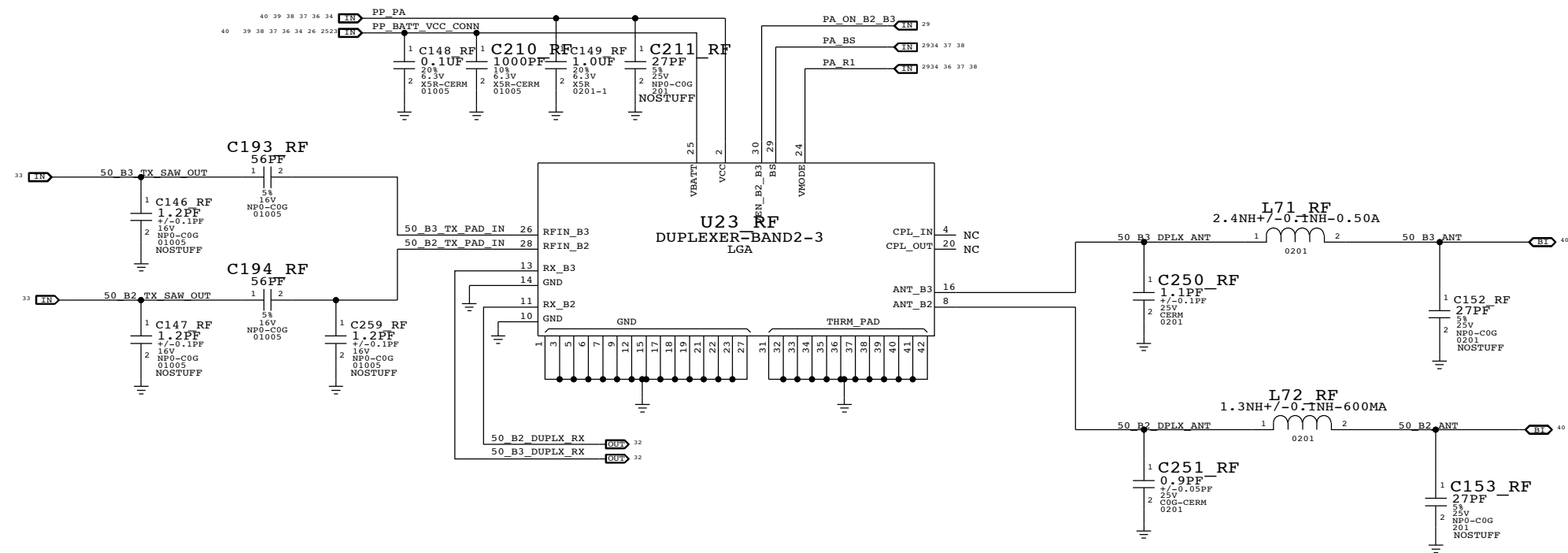
BAND	PA POWER MODE	PA_BS	PA_ON_B1_B4	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B4	HPM	0	1	0
B4	LPM	0	1	1
B1	HPM	1	1	0
B1	LPM	1	1	1

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	PAGE	11 OF 23		
	SHEET	34 OF 46		

BAND 2/3 PAD



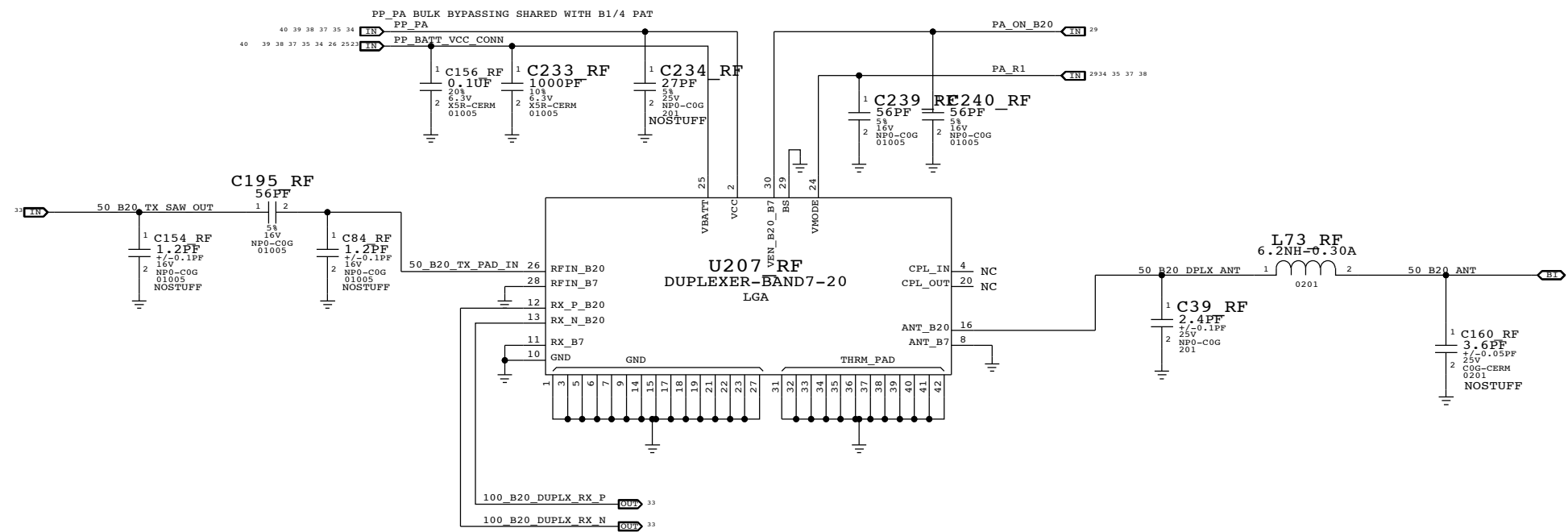
BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

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PAGE	12 OF 23			
SHEET	35 OF 46			

BAND 20 PAD

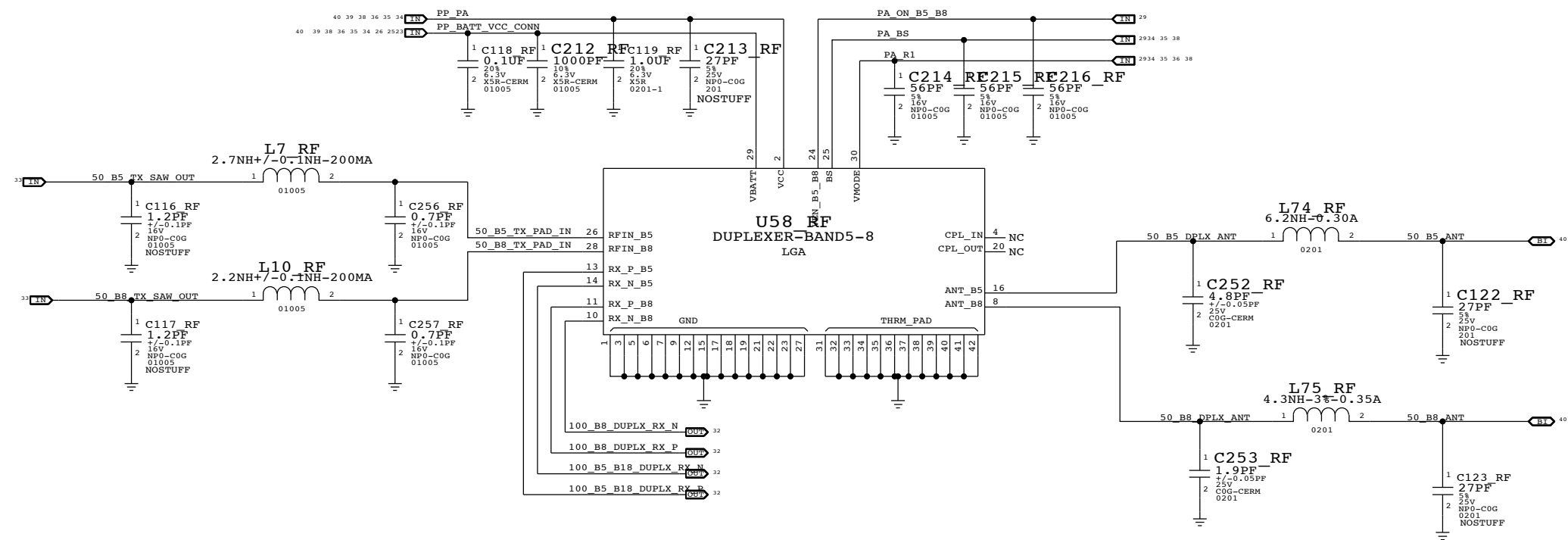


BAND	PA POWER MODE	PA_ON_B20	PA_R1
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

CELLULAR FRONT END: BAND 20 PAD

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BAND 5/8 PAD

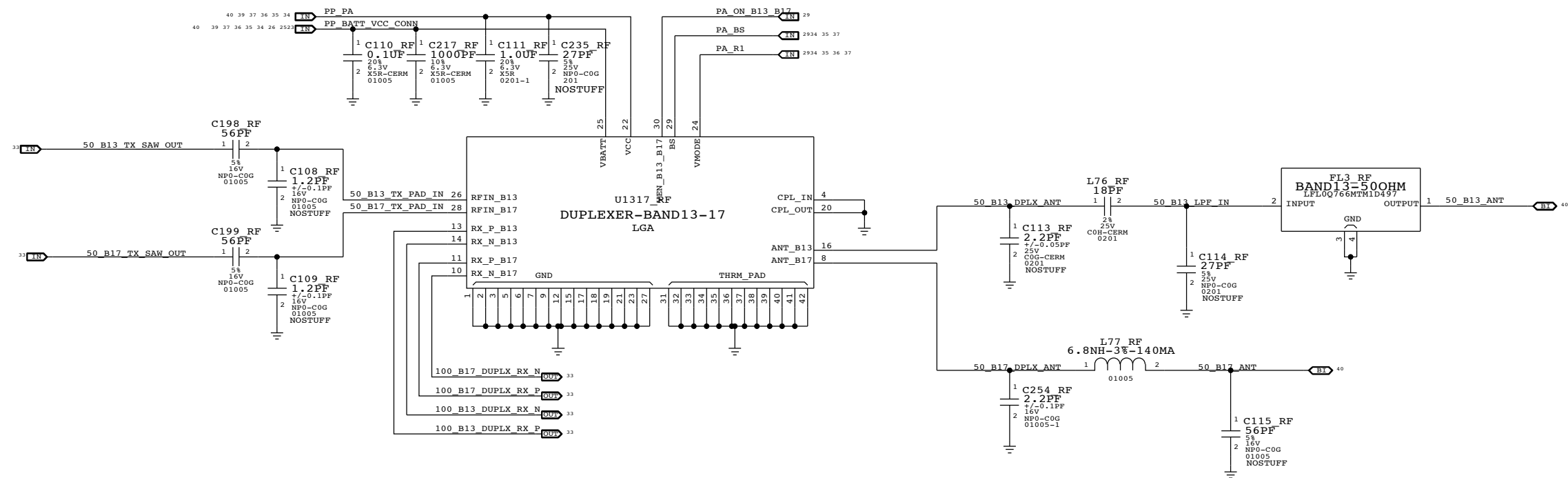


BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

CELLULAR FRONT END: BAND 5/8 PAD

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BAND 13/17 PAD

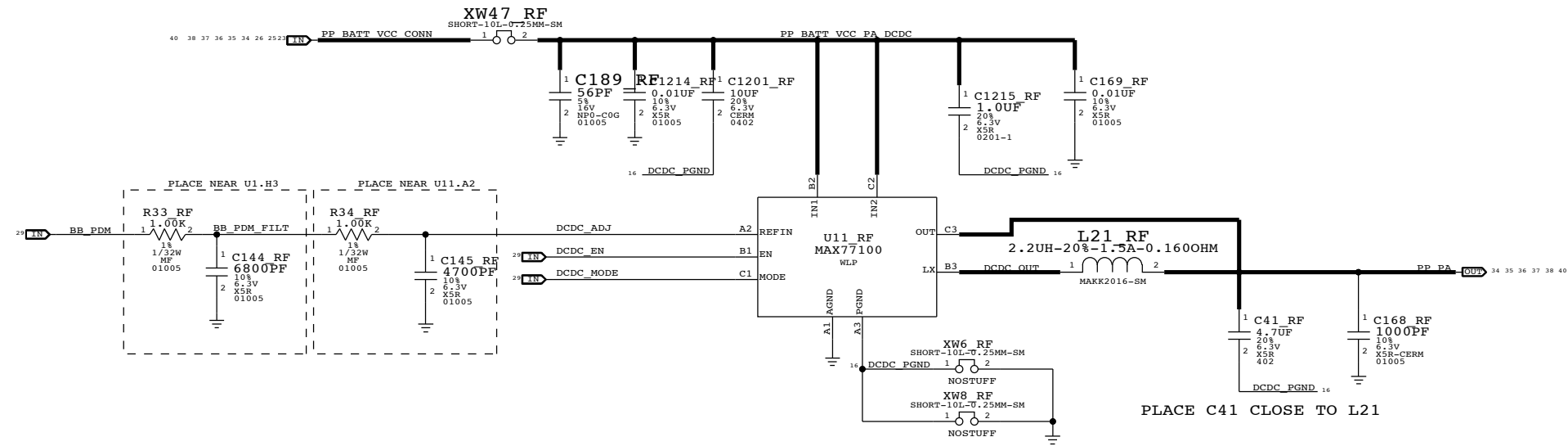


BAND	PA POWER MODE	PA_BS	PA_ON_B13_B17	PA_R1
=====	=====	=====	=====	=====
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

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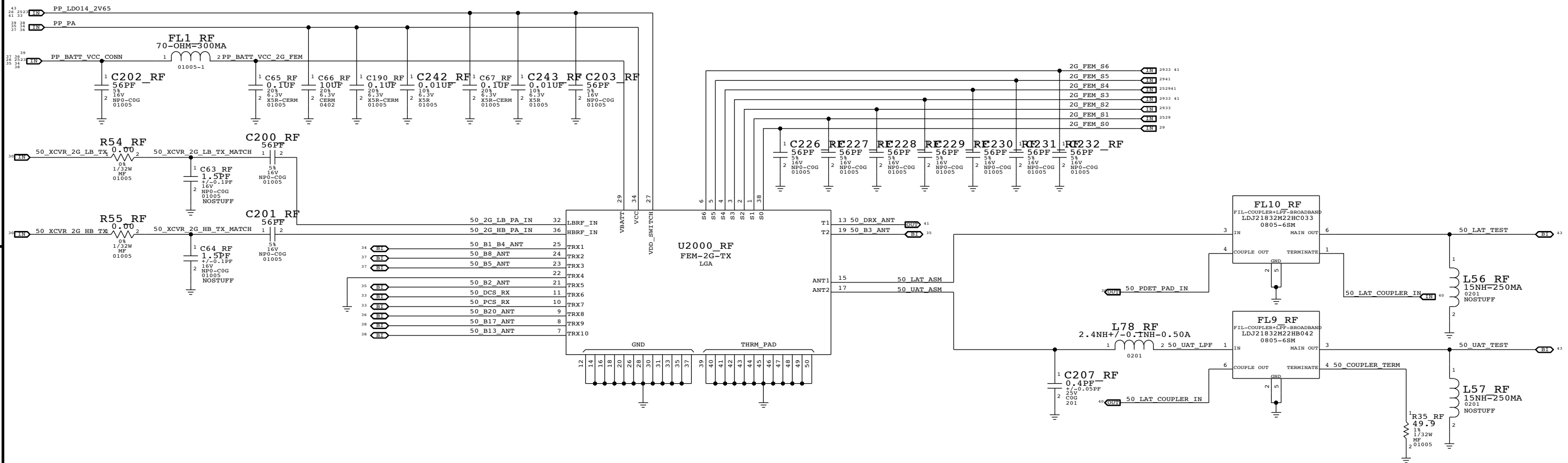
PA DC/DC CONVERTER



CELLULAR FRONT END: PA DCDC CONVERTER

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		PAGE 16 OF 23	SHEET 39 OF 46

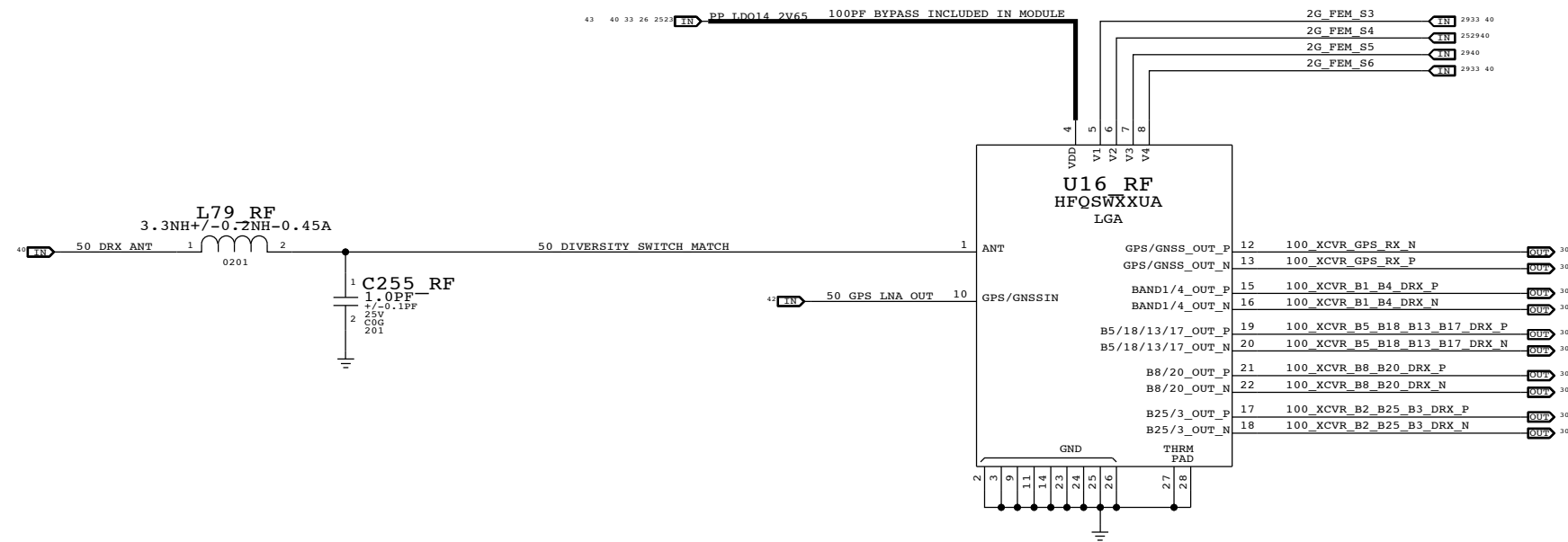
2G FEM



SEE PGS. 21-22 FOR 2G FEM LOGIC TABLE

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RX DIVERSITY



BAND	S6	S5	S4	S3
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH

SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES

CELLULAR FRONT END: RX DIVERSITY

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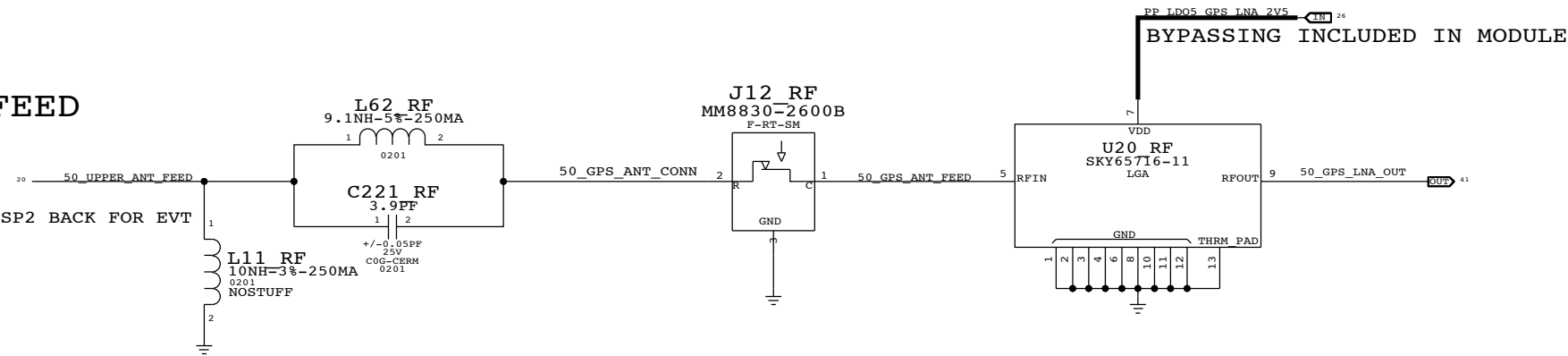
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GPS

GPS FEED

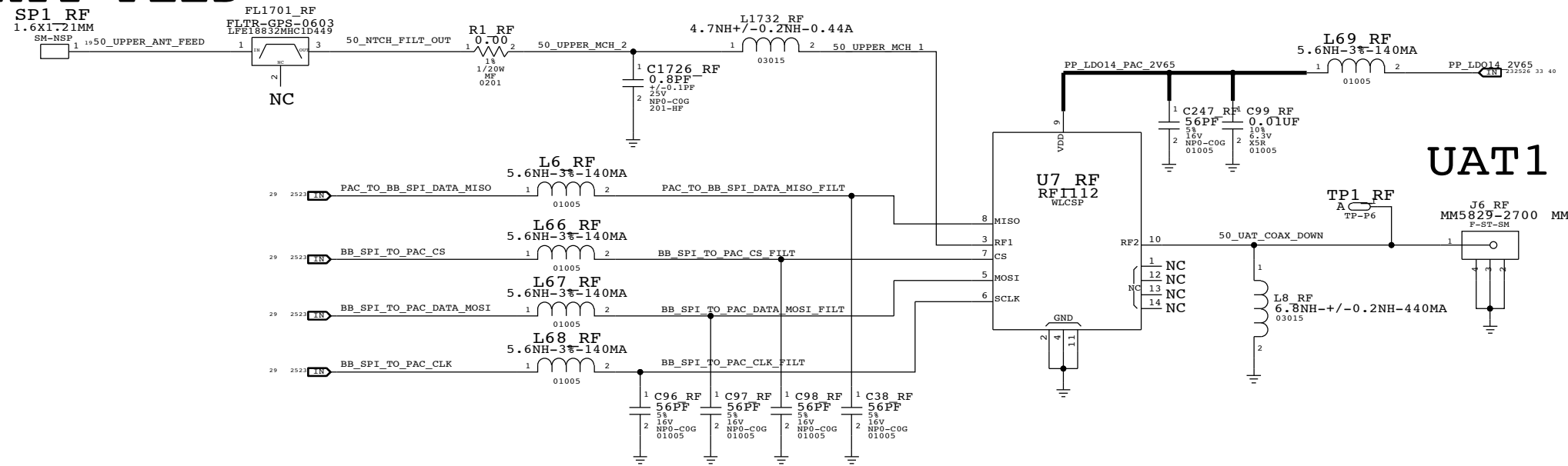
NOTE: ADD SP2 BACK FOR EVT



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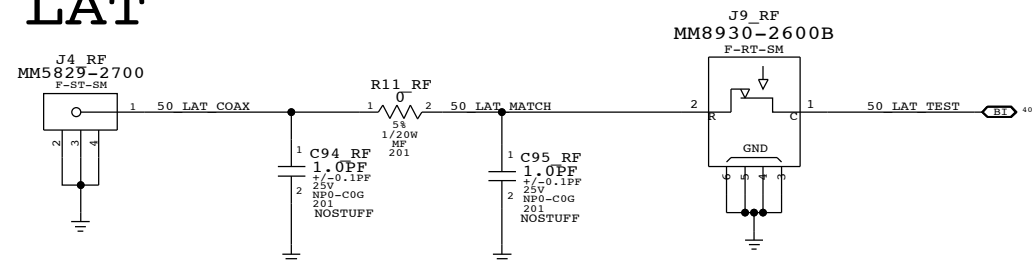
ANTENNA FEEDS

UAT1 FEED



UAT1 COAX

LAT



CELLULAR FRONT END: ANTENNA FEEDS


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FRONT END LOGIC TABLE (1 OF 2)

BAND	S6	S5	S4	S3	S2	S1	S0	TX/PRX PATH	DRX PATH
LB TX, IDLE, LAT	HIGH	HIGH	HIGH	LOW	LOW	HIGH	HIGH	LAT	UAT
LB TX, IDLE, UAT	HIGH	HIGH	HIGH	LOW	LOW	LOW	HIGH	UAT	LAT
LB TX, LAT, HPM	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LAT	UAT
LB TX, UAT, HPM	HIGH	HIGH	HIGH	LOW	HIGH	LOW	HIGH	UAT	LAT
LB TX, LAT, LPM	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LOW	LAT	UAT
LB TX, UAT, LPM	HIGH	HIGH	HIGH	LOW	HIGH	LOW	LOW	UAT	LAT
LB TX, HIGH Z, LAT, HPM	HIGH	HIGH	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
LB TX, HIGH Z, UAT, HPM	HIGH	HIGH	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
LB TX, HIGH Z, LAT, LPM	HIGH	HIGH	LOW	LOW	HIGH	HIGH	LOW	LAT	UAT
LB TX, HIGH Z, UAT, LPM	HIGH	HIGH	LOW	LOW	HIGH	LOW	LOW	UAT	LAT
HB TX, IDLE, LAT	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LAT	UAT
HB TX, IDLE, UAT	HIGH	HIGH	HIGH	HIGH	LOW	LOW	HIGH	UAT	LAT
HB TX, LAT, HPM	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LAT	UAT
HB TX, UAT, HPM	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	UAT	LAT
HB TX, LAT, LPM	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	LAT	UAT
HB TX, UAT, LPM	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	LOW	UAT	LAT
HB TX, HIGH Z, LAT, HPM	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
HB TX, HIGH Z, UAT, HPM	HIGH	HIGH	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
HB TX, HIGH Z, LAT, LPM	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LOW	LAT	UAT
HB TX, HIGH Z, UAT, LPM	HIGH	HIGH	LOW	HIGH	HIGH	LOW	LOW	UAT	LAT
GSM850 RX, LAT	HIGH	LOW	HIGH	HIGH	LOW	HIGH	HIGH	LAT	UAT
GSM850 RX, UAT	HIGH	LOW	HIGH	HIGH	LOW	LOW	HIGH	UAT	LAT
GSM900 RX, LAT	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	LAT	UAT
GSM900 RX, UAT	HIGH	LOW	HIGH	HIGH	HIGH	LOW	HIGH	UAT	LAT
GSM1900 RX, LAT	LOW	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
GSM1900 RX, UAT	LOW	HIGH	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
GSM1800 RX, LAT	HIGH	LOW	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
GSM1800 RX, UAT	HIGH	LOW	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
TERMINATED, UAT	HIGH	LOW	HIGH	LOW	HIGH	HIGH	HIGH	UAT	LAT
TERMINATED, LAT	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LAT	UAT

LAT = LOWER ANTENNA
 UAT = UPPER ANTENNA

FRONT END LOGIC TABLE (1 OF 2)

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		SHEET 44 OF 46

FRONT END LOGIC TABLE - DEV2 (2 OF 2)

BAND	S6	S5	S4	S3	S2	S1	S0	TX/PRX PATH	DRX PATH
B1/BC6, LAT	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B1/BC6, UAT	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B2/B25/BC1, LAT	LOW	HIGH	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B2/B25/BC1, UAT	LOW	HIGH	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B3, LAT	HIGH	LOW	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B3, UAT	HIGH	LOW	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B4/BC15, LAT	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B4/BC15, UAT	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B5/B6/B18/BC0/BC10, LAT	LOW	LOW	HIGH	LOW	HIGH	HIGH	HIGH	LAT	UAT
B5/B6/B18/BC0/BC10, UAT	LOW	LOW	HIGH	LOW	HIGH	LOW	HIGH	UAT	LAT
B8, LAT	LOW	LOW	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
B8, UAT	LOW	LOW	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
B13, LAT	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LAT	UAT
B13, UAT	LOW	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	UAT	LAT
B17, LAT	LOW	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LAT	UAT
B17, UAT	LOW	HIGH	HIGH	HIGH	LOW	LOW	HIGH	UAT	LAT
B20, LAT	LOW	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LAT	UAT
B20, UAT	LOW	HIGH	HIGH	LOW	HIGH	LOW	HIGH	UAT	LAT
OFF	LOW	LOW	HIGH	HIGH	X	X	X	X	X
STANDBY	LOW	LOW	LOW	LOW	LOW	LOW	LOW	X	X

LAT = LOWER ANTENNA

UAT = UPPER ANTENNA

OFF = LOWEST POWER STATE WITHOUT REMOVING LDO14_2V65 POWER

STANDBY = ADDED TO SUPPORT EXISTING SW ARCHITECTURE. NOT TO BE USED AS A LOW POWER STATE.

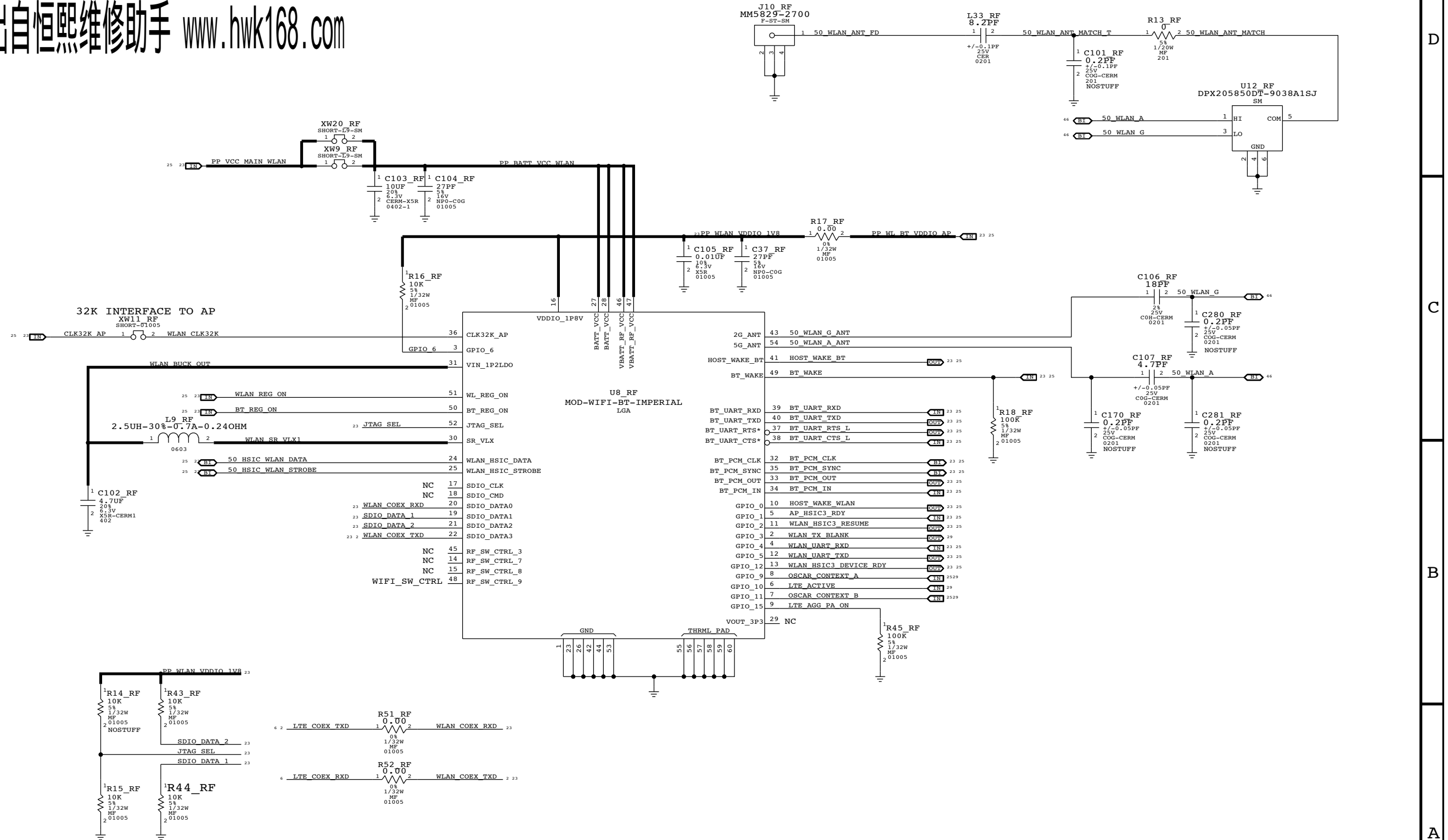
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WLAN/BT

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UAT2



PULL-UP ON GPIO6, SDIO_DATA_2 & PULL-DOWN ON SDIO_DATA_1 REQUIRED FOR HSIC BOOTSTRAPPING

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