

- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IPHONE 5C 原理图

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
2	0001669557	ENGINEERING RELEASED		2012-10-14

X155 PROTO1 SINGLE BRD

Mon Oct 8 11:06:07 2012

TO DO: CLEANUP ALTERNATES FOR X155

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0648	138S0652	ALTERNATE	?	4.7UF CERM 0402 6.3V
339S0177	339S0176	ALTERNATE	?	H5P ALTERNATE
339S0178	339S0176	ALTERNATE	?	H5P ALTERNATE

X155 BOM CALLOUTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9584	1	SCH, SINGLE BRD, X155	SCH	Y	?
820-3329	1	PCB, SINGLE BRD, X155	PCB	Y	?
825-6838	1	LABEL FOR X155 639-3796	EEEE_F284	Y	EEEE_16G

PDF PAGE	CSA PAGE	CONTENTS	SYNC MASTER	DATE
2	2	H5P JTAG, USB ,PLL	N/A	N/A
3	3	H5P GPIO & CONTROL	N/A	N/A
4	4	H5P IO POWER	N/A	N/A
5	5	H5P SOC/CPU/SRAM PWR	N/A	N/A
6	6	H5P W/ NAND	N/A	N/A
7	7	H5P VIDEO	N/A	N/A
8	8	BUTTON FLEX B2B	N/A	N/A
9	9	L67 AUDIO CODEC (1/2)	N/A	N/A
10	10	L67 AUDIO CODEC (2/2)	N/A	N/A
11	11	CG FLEX B2B	N/A	N/A
12	12	AGATHA PMU(1/2)	N/A	N/A
13	13	AGATHA PMU(2/2)	N/A	N/A
14	14	CHESTNUT + BACKLIGHT DRIVER	N/A	N/A
15	15	SPKR AMP + LED DRIVER	N/A	N/A
16	16	TRISTAR	N/A	N/A
17	17	DOCKFLEX B2B	N/A	N/A
18	18	D404 (TOUCH B2B, DRIVER ICS)	N/A	N/A
19	19	LCM CONNECTOR	N/A	N/A
20	20	SENSORS	N/A	N/A
21	21	CAM0 CONNECTOR	N/A	N/A
22	22	BATT B2B, TPS, PD FEATURES	N/A	N/A
23	23	RADIO_MLB HIERARCH. SYMBOL	N/A	N/A

COMPASS BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
639-4024	1	ST GYRO - COMPASS POP	U16	Y	COMPASS_POP

NAND BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	NAND, 19NM, 16GB, MLC, PPN1.5	U4	Y	NAND_16G

HORIZONTAL CAP BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C422,C74,C92,C250,C265	Y	HRZN_CAP_GRP1
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C293,C294,C257,C299,C262	Y	HRZN_CAP_GRP2
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C264,C378,C189,C203,C245	Y	HRZN_CAP_GRP3
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C190,C204,C239,C246,C195	Y	HRZN_CAP_GRP4
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C205,C243,C247,C252,C297	Y	HRZN_CAP_GRP5
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C386,C387,C333,C332,C335	Y	HRZN_CAP_GRP6
138S0801	5	HRZN CAPS 1:10UF,0402,6.3V	C42_RF,C43_RF,C44_RF	Y	HRZN_CAP_GRP7
138S0801	1	HRZN CAPS 1:10UF,0402,6.3V	C1201_RF	Y	HRZN_CAP_GRP8
138S0801	4	HRZN CAPS 1:10UF,0402,6.3V	C182,C307,C209,C187	Y	HRZN_CAP_GRP10
138S0794	2	HRZN CAPS 1:10UF,0402,10V	C52,C156	Y	HRZN_CAP_GRP11
138S0582	1	4.7UF 0.55MM HEIGHT	C193	Y	LOW_Z_CAP

BOARD ID RADIO BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0621	1	1.00M 1% 01005	R25_RF	Y	N51_CFG_A
118S0732	1	50K 1% 01005	R26_RF	Y	N51_CFG_A
117S0159	1	470K 5% 01005	R25_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_A
118S0726	1	162K 1% 01005	R26_RF	Y	N53_CFG_A
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_B
118S0623	1	267K 1% 01005	R26_RF	Y	N53_CFG_B
118S0659	1	255K 1% 01005	R25_RF	Y	N48_CFG_A
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_A
118S0689	1	147K 1% 01005	R25_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N49_CFG_A
118S0650	1	499K 1% 01005	R26_RF	Y	N49_CFG_A
118S0732	1	50K 1% 01005	R25_RF	Y	N49_CFG_B
118S0621	1	1.00M 1% 01005	R26_RF	Y	N49_CFG_B

GYRO BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1158	1	ST GYRO	U8	Y	GYRO_ST
132S0391	1	ST GYRO - CP CAP	C11	Y	GYRO_ST

CHESTNUT BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1172	1	TI CHESTNUT	U3	Y	CHESTNUT_TI
152S1649	1	TI CHESTNUT - 1.5 UH IND	L19	Y	CHESTNUT_TI
338S1168	1	INTERSIL CHESTNUT	U3	Y	CHESTNUT_INTERSIL
152S1611	1	INTERSIL CHESTNUT -2.2 UH IND	L19	Y	CHESTNUT_INTERSIL

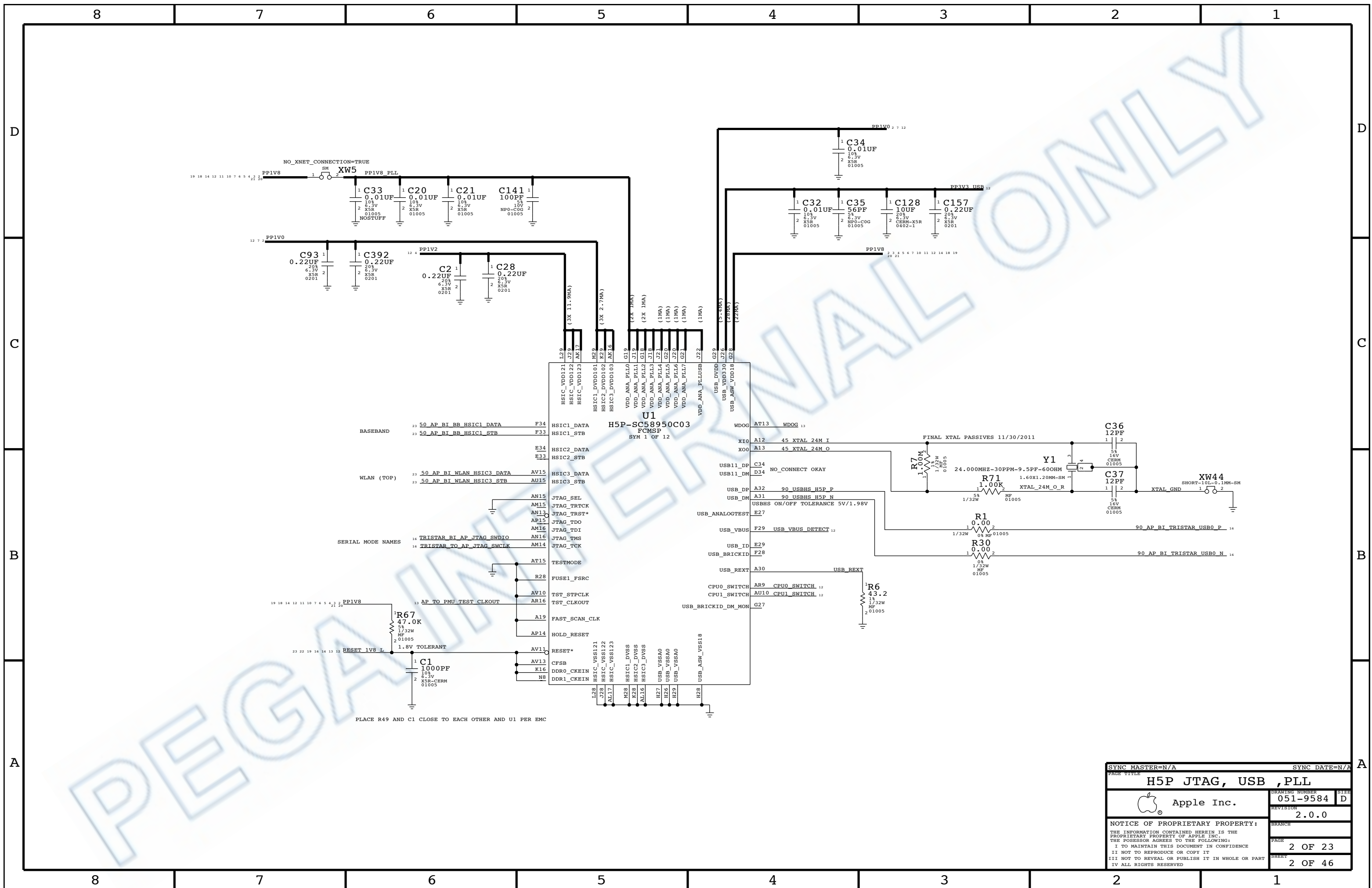
TRISTAR BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	CBTL1608A1UK,WCSF,TRISTAR	U2	Y	TRISTAR
343S0639	1	CBTL1610A0UK,WCSF,TRISTAR2	U2	Y	TRISTAR2
118S0671	2	RES 150HM 01005 5%	R102,R103	Y	TRISTAR
117S0202	2	RES 200HM 01005 5%	R102,R103	Y	TRISTAR2

SCH 051-9584
BRD 820-3329

BOM 639-3796 X155

DRAWING TITLE		SCH, SINGLE BRD, X155	
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PLACE R49 AND C1 CLOSE TO EACH OTHER AND U1 PER EMC

PAGE TITLE		SYNC DATE=N/A	
H5P JTAG, USB, PLL			
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	REVISION	2.0.0	BRANCH
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SHEET		2 OF 46	

```

BOARD_REV[3:0]={EHCI_PORT3,EHCI_PORT_PWR2,EHCI_PORT_PWR1,EHCI_PORT_PWR0}
FLOAT=LOW, PULLUP=HIGH
1111 X155 INITIAL
1101 - PROTO1 TRISTAR <---PROTO1 SELECTED
1100 - PROTO1 TRISTAR 2

```

```

BOARD_ID[3:0]={GPIO16,SPI0_MISO,SPI0_MOSI,SPI0_SCLK}
FLOAT=LOW, PULLUP=HIGH
1010 X155 MLB <--- SELECTED

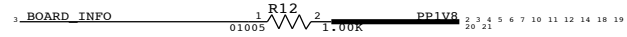
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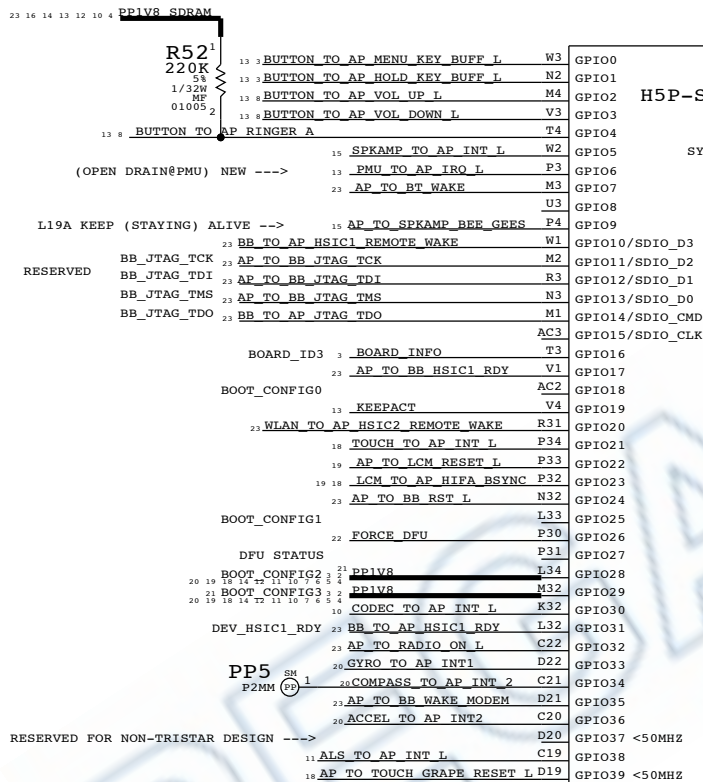
BOOT_CONFIG[3:0]={GPIO29_CONFIG3,GPIO28_CONFIG2,GPIO25_CONFIG1,GPIO18_CONFIG0}
FLOAT=LOW, PULLUP=HIGH
0000 SPI0
0001 SPI3
0010 SPI0 W/TEST
0011 SPI3 W/TEST
0100 FMIO 2CS
0101 FMIO 4CS
0110 FMIO 4CS W/TEST
0111 RESERVED
1000 FMIO 2 CS
1001 FMIO 4 CS
1010 FMIO 4CS W/TEST
1100 FMIO/1 2/2 CS <--- SELECTED
1101 FMIO/1 4/4 CS
1110 FMIO/1 4/4 CS W/TEST
1111 RESERVED

```

COMMON PULL UP FOR BOARD_REV, BOARD_ID AND BOOT_CONFIG PINS



R12 MUST WIN OVER 6X INTERNAL PULL-DOWNS THAT ARE ~100K



```

17 AP_TO_HEADSET_HS3_CTRL AT11
17 AP_TO_HEADSET_HS4_CTRL AP12

```

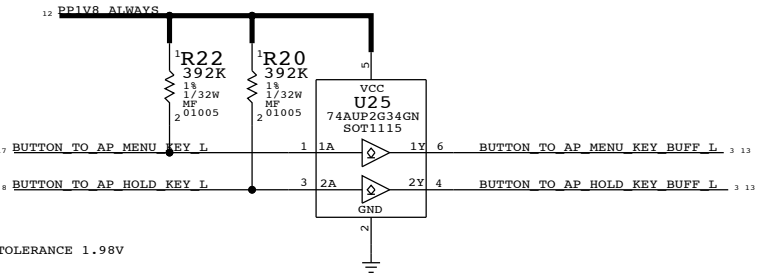
GPIO	Function	Pin
GPIO0	EHCI_PORT_PWR0	AE4
GPIO1	EHCI_PORT_PWR1	AD3
GPIO2	EHCI_PORT_PWR2	AD4
GPIO3	EHCI_PORT_PWR3	AE3
GPIO4		
GPIO5	TMR32_PWM0	AT6
GPIO6	TMR32_PWM1	AP8
GPIO7	TMR32_PWM2	AP1
GPIO8		
GPIO9		
GPIO10	UART0_RXD	AR15
GPIO11	UART0_TXD	AU12
GPIO12		
GPIO13	UART1_CTSN	AA3
GPIO14	UART1_RTSN	AB2
GPIO15	UART1_RXD	AB3
GPIO16	UART1_TXD	AF5
GPIO17		
GPIO18	UART2_CTSN	AG3
GPIO19	UART2_RTSN	AA1
GPIO20	UART2_RXD	AE2
GPIO21	UART2_TXD	AF3
GPIO22		
GPIO23	UART3_CTSN	AH3
GPIO24	UART3_RTSN	AB1
GPIO25	UART3_RXD	AF4
GPIO26	UART3_TXD	AG4
GPIO27		
GPIO28	UART4_CTSN/SPI4_SSN	AJ4
GPIO29	UART4_RTSN/SPI4_SCLK	AE1
GPIO30	UART4_RXD/SPI4_MISO	AJ2
GPIO31	UART4_TXD/SPI_MOSI	AH4
GPIO32		
GPIO33	UART5_RXD	AK4
GPIO34	UART5_TXD	AJ3
GPIO35		
GPIO36	UART6_CTSN	AH2
GPIO37	UART6_RTSN	AL1
GPIO38	UART6_RXD	AK3
GPIO39	UART6_TXD	AD1
GPIO40		
GPIO41		
GPIO42		
GPIO43		
GPIO44		
GPIO45		
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GPIO96		
GPIO97		
GPIO98		
GPIO99		
GPIO100		

```

FMI, 00=1.8V | 01=3.0V | 10=3.3V
I2C2, 0=1.8V | 1=3.0V
SPI3, 0=1.8V | 1=3.0V

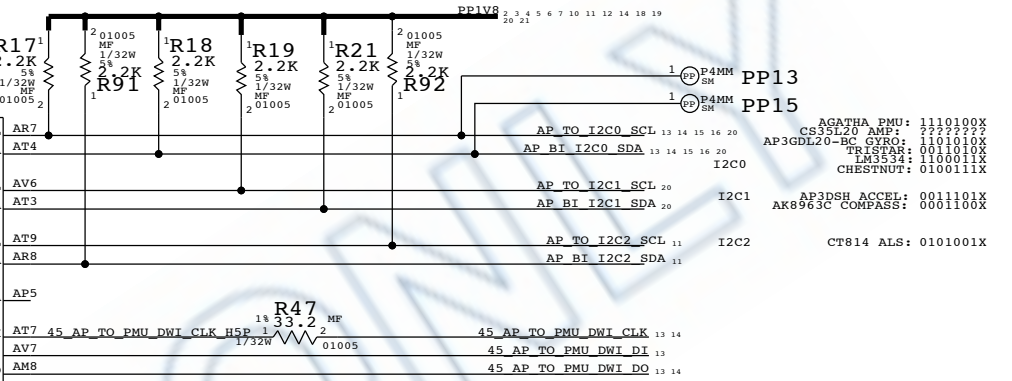
```

MENU & POWER / HOLD KEY

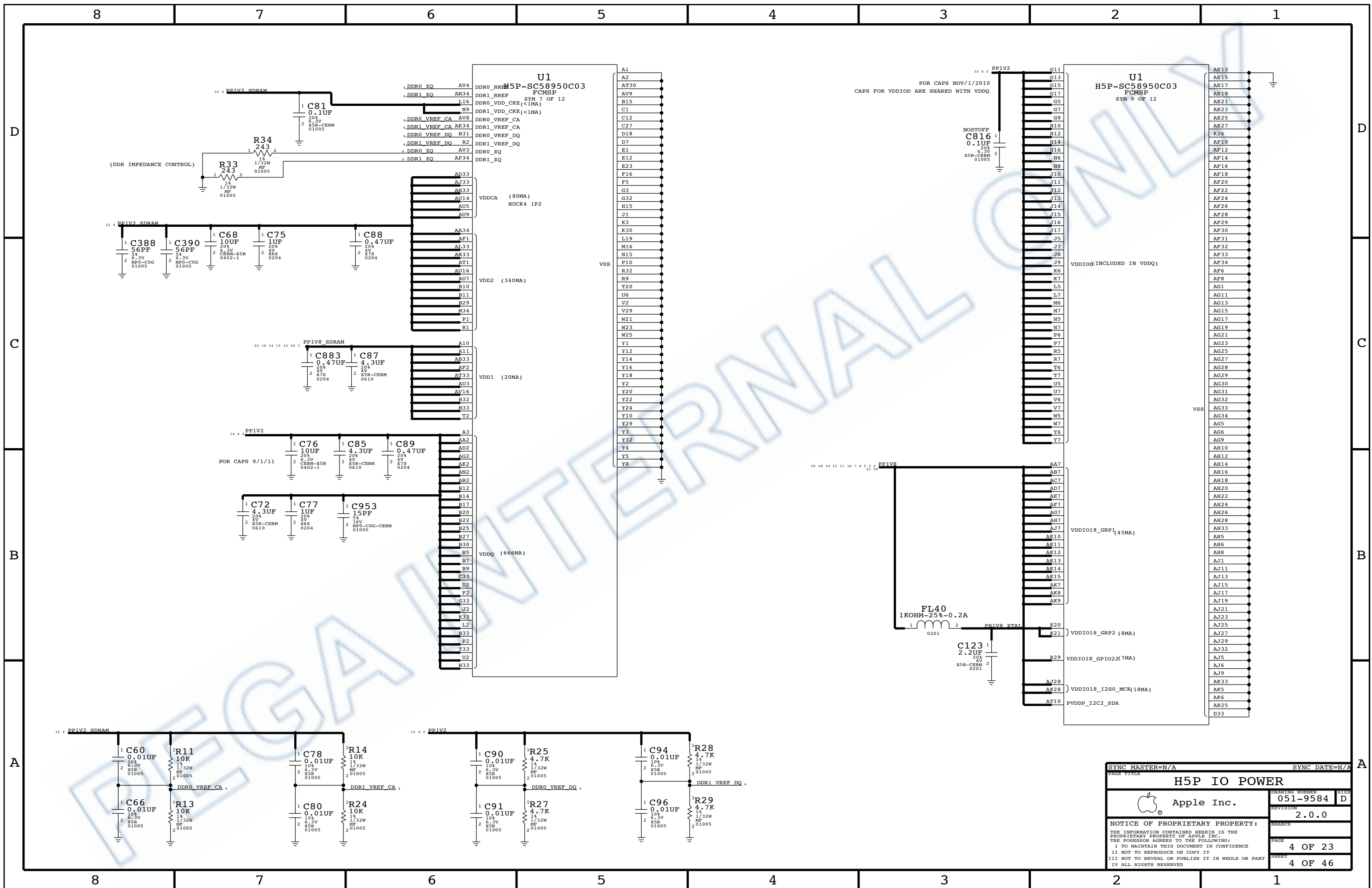


DEBUG UART: TOLERANCE 1.98V

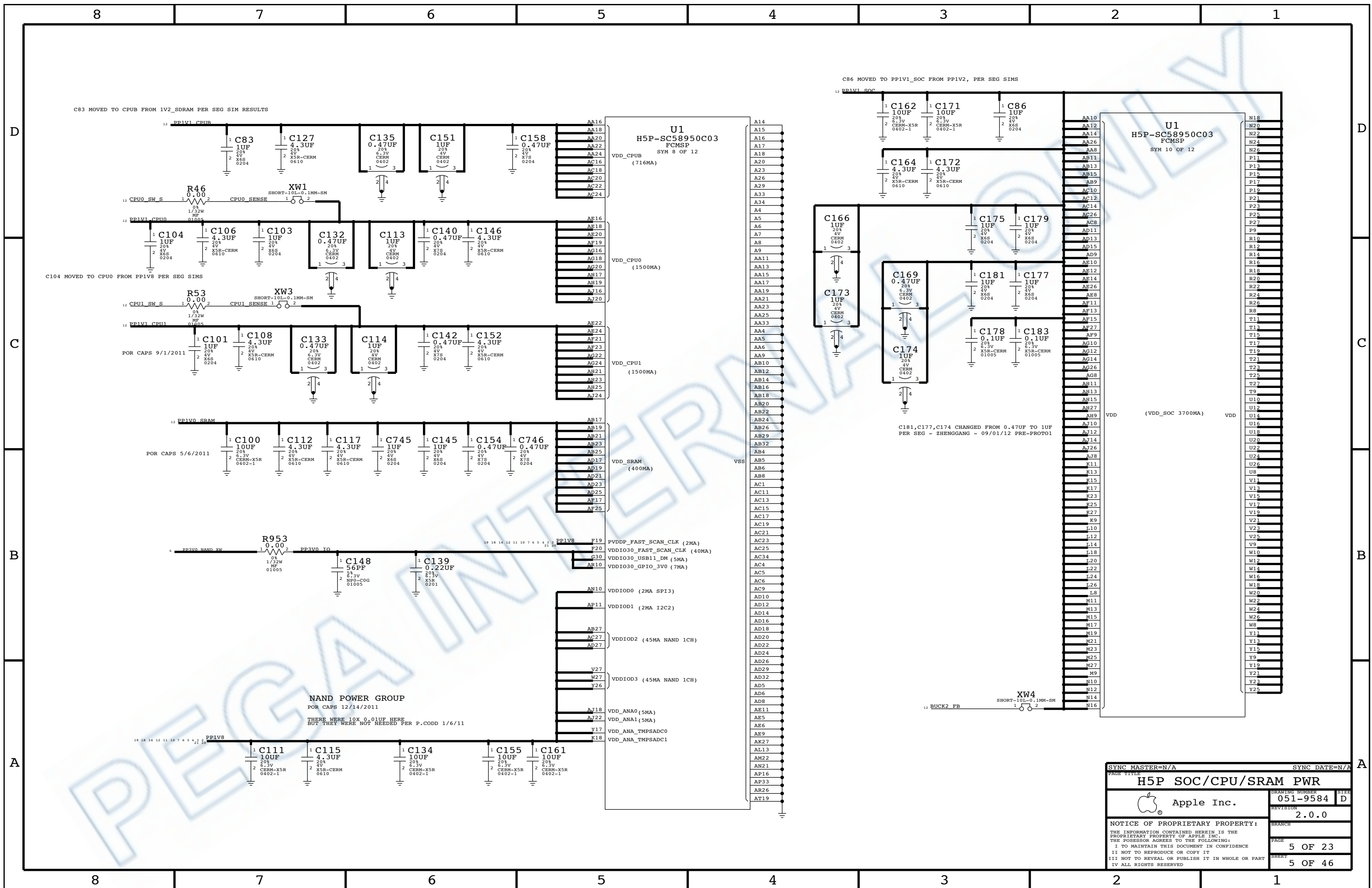
Pin	Function	Pin	Function
1	45 AP TO CODEC I2S_MCLK	13	I2S0_MCK
2	45 I2S0_MCK_R	14	I2S0_BCLK
3	45 AP TO CODEC ASP I2S0_BCLKM30	15	I2S0_LRCK
4	45 AP TO CODEC ASP I2S0_LRCLK AH31	16	I2S0_DIN
5	CODEC TO AP ASP I2S0_DINAH30	17	I2S0_DOUT
6	45 AP TO CODEC ASP I2S0_DOUTAH30	18	I2S1_MCK
7		19	I2S1_BCLK
8		20	I2S1_LRCK
9		21	I2S1_DIN
10		22	I2S1_DOUT
11		23	I2S2_MCK
12		24	I2S2_BCLK
13		25	I2S2_LRCK
14		26	I2S2_DIN
15		27	I2S2_DOUT
16		28	I2S3_MCK
17		29	I2S3_BCLK
18		30	I2S3_LRCK
19		31	I2S3_DIN
20		32	I2S3_DOUT
21		33	I2S4_MCK
22		34	I2S4_BCLK
23		35	I2S4_LRCK
24		36	I2S4_DIN
25		37	I2S4_DOUT
26		38	SPDIF
27		39	SPI0_MISO
28		40	SPI0_MOSI
29		41	SPI0_SCLK
30		42	SPI0_SSN
31		43	SPI1_MISO
32		44	SPI1_MOSI
33		45	SPI1_SCLK
34		46	SPI1_SSN
35		47	SPI2_MISO
36		48	SPI2_MOSI
37		49	SPI2_SCLK
38		50	SPI2_SSN
39		51	SPI3_MISO
40		52	SPI3_MOSI
41		53	SPI3_SCLK
42		54	SPI3_SSN



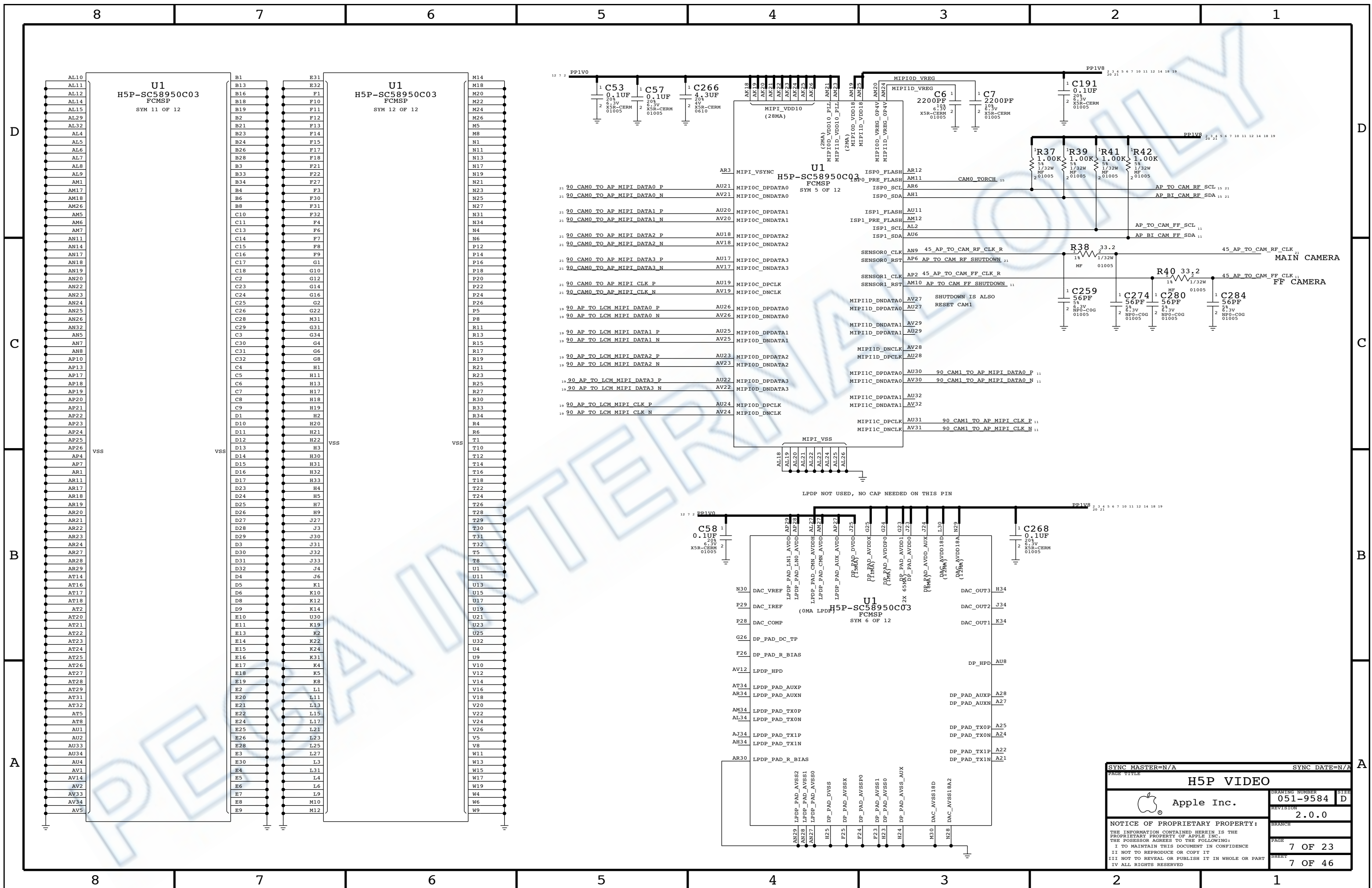
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H5P GPIO & CONTROL			
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H5P IO POWER			
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H5P SOC/CPU/SDRAM PWR			
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BUTTON FLEX (VIBE DRIVER, BUTTONS, ANC REF MIC, STROBE, STROBE_NTC)

WIFI FLEX PAC:
VDD (3.0V)

BUTTONS:
RINGER, HOLD,
VOL_UP/DOWN

VIBE DRIVE

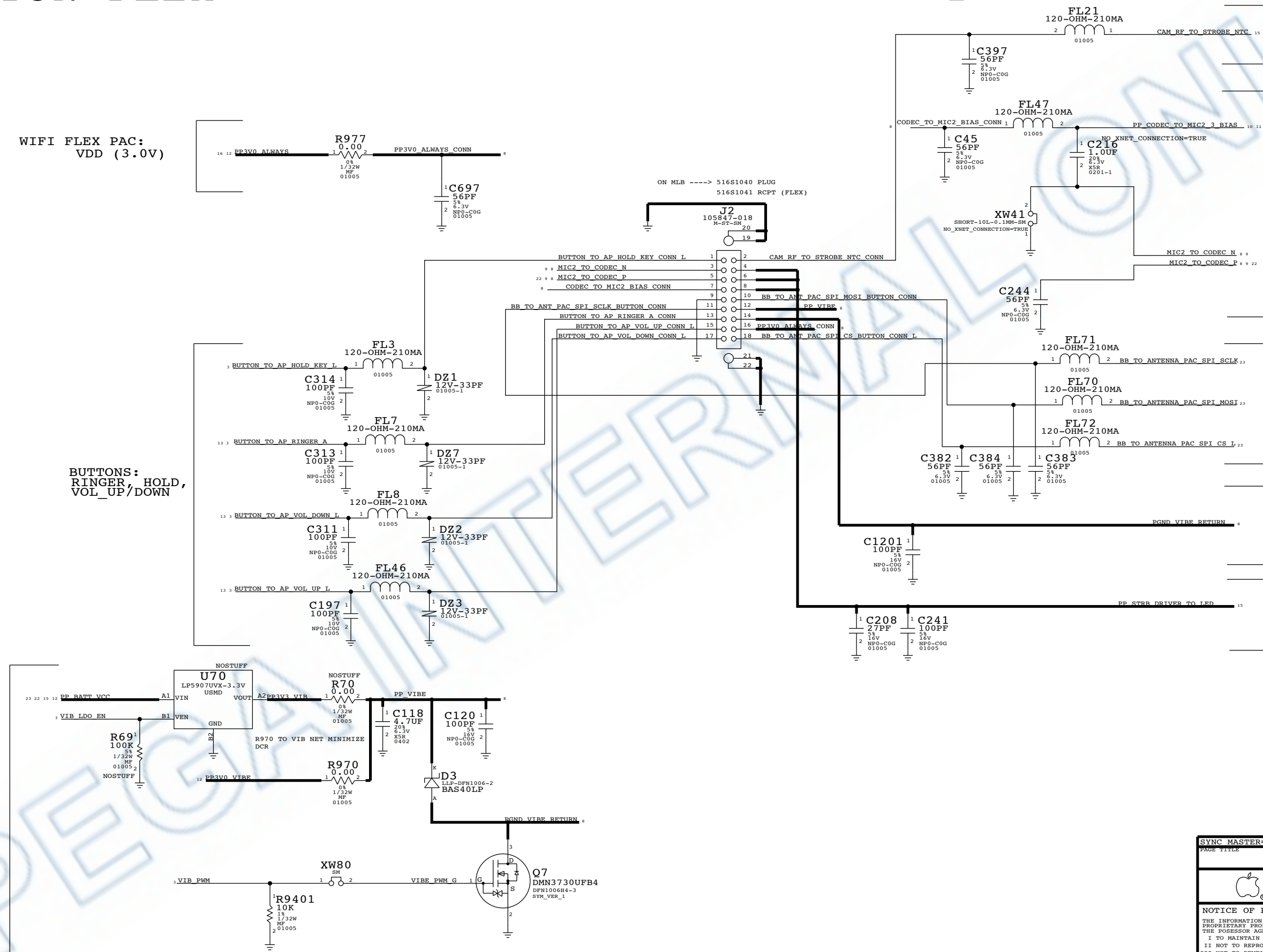
STROBE:
STROBE NTC

MIC2 (ANC REF MIC):
MIC2/3 BIAS,
MIC2_P,_N

WIFI FLEX PAC:
PAC SPI BUS

VIBE RETURN

STROBE:
LED COOL



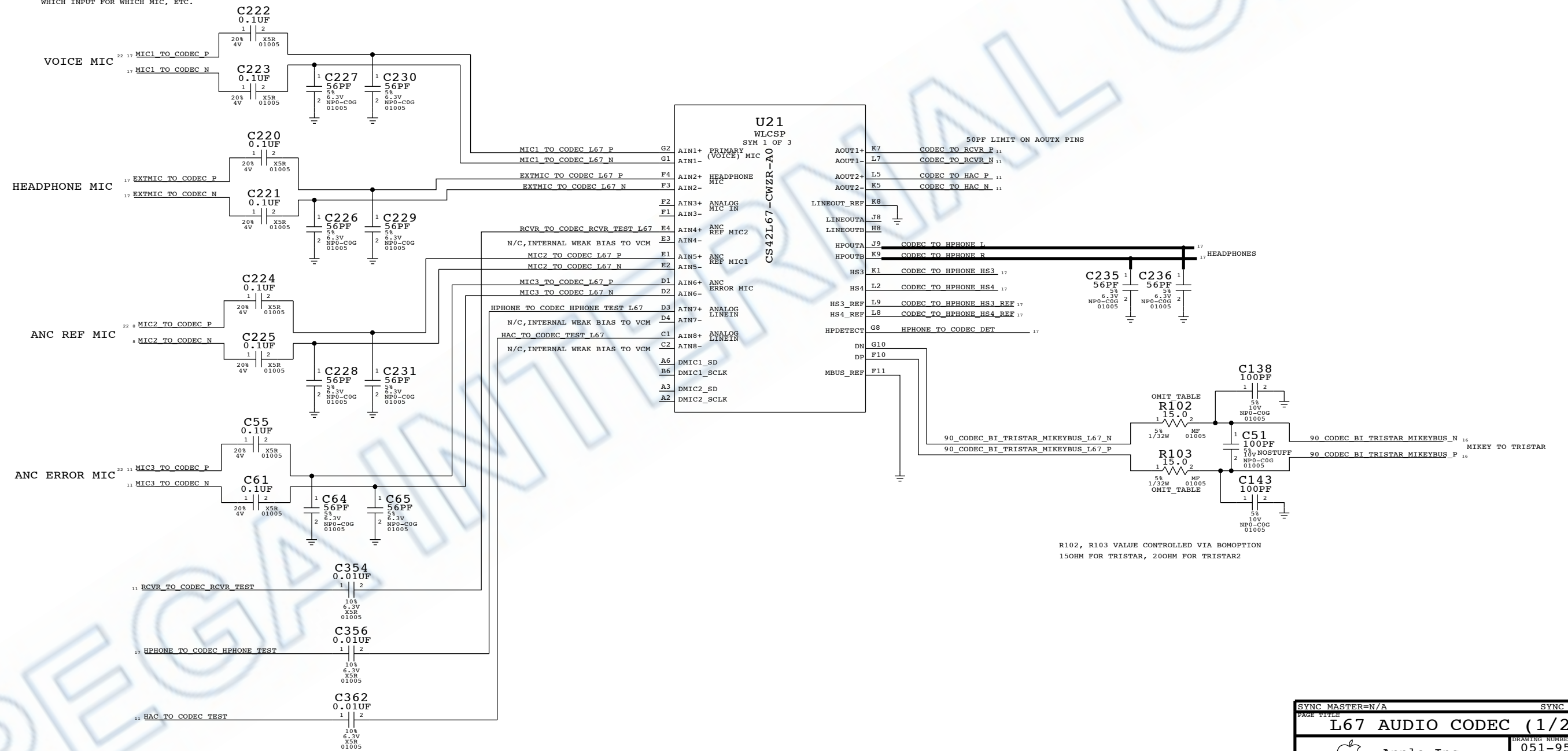
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		SHEET	8 OF 46

L67 AUDIO CODEC

AUDIO I/O

(ANALOG MIC IN, DIG MIC IN, HPOUT, LINEOUT, RECEIVER OUT, MIKEYBUS)

TO DO: REVIEW AUDIO MIC PATHS,
WHICH BIAS OUTPUT USED FOR WHICH MIC,
WHICH INPUT FOR WHICH MIC, ETC.



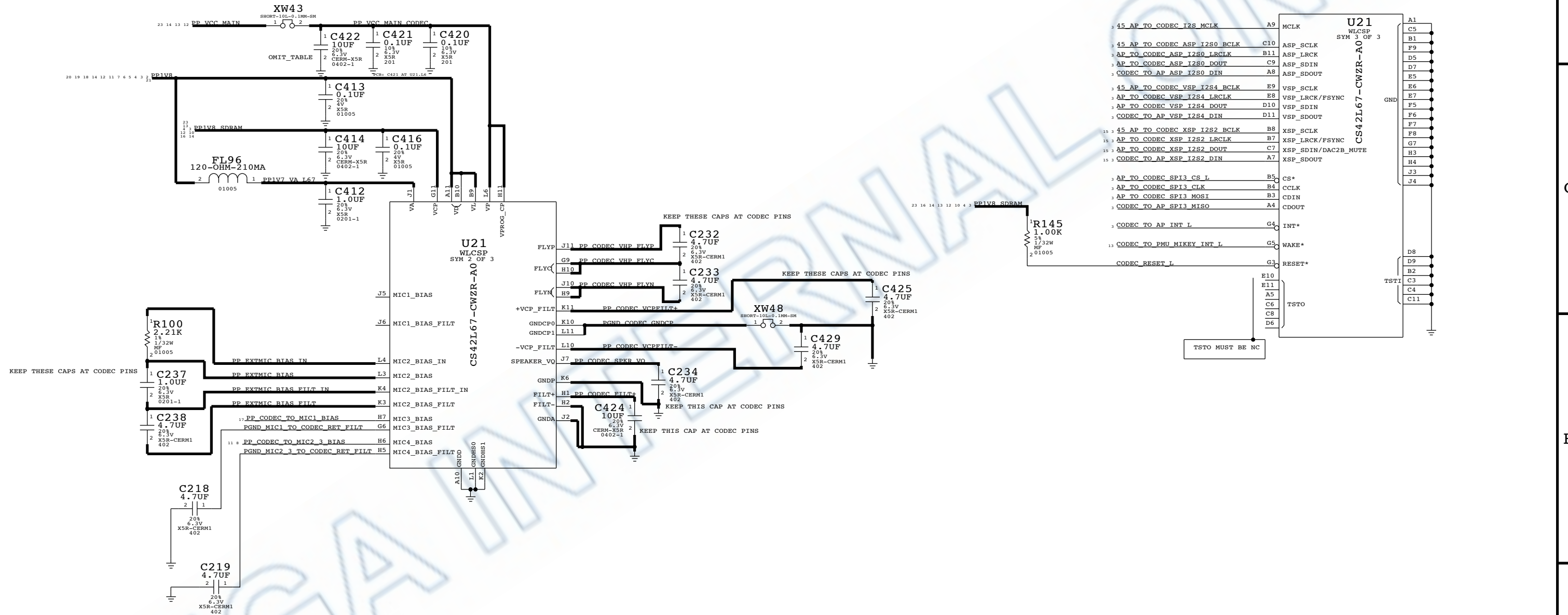
R102, R103 VALUE CONTROLLED VIA BOMOPTION
150HM FOR TRISTAR, 200HM FOR TRISTAR2

SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE L67 AUDIO CODEC (1/2)			
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L67 AUDIO CODEC

POWER, MICBIAS

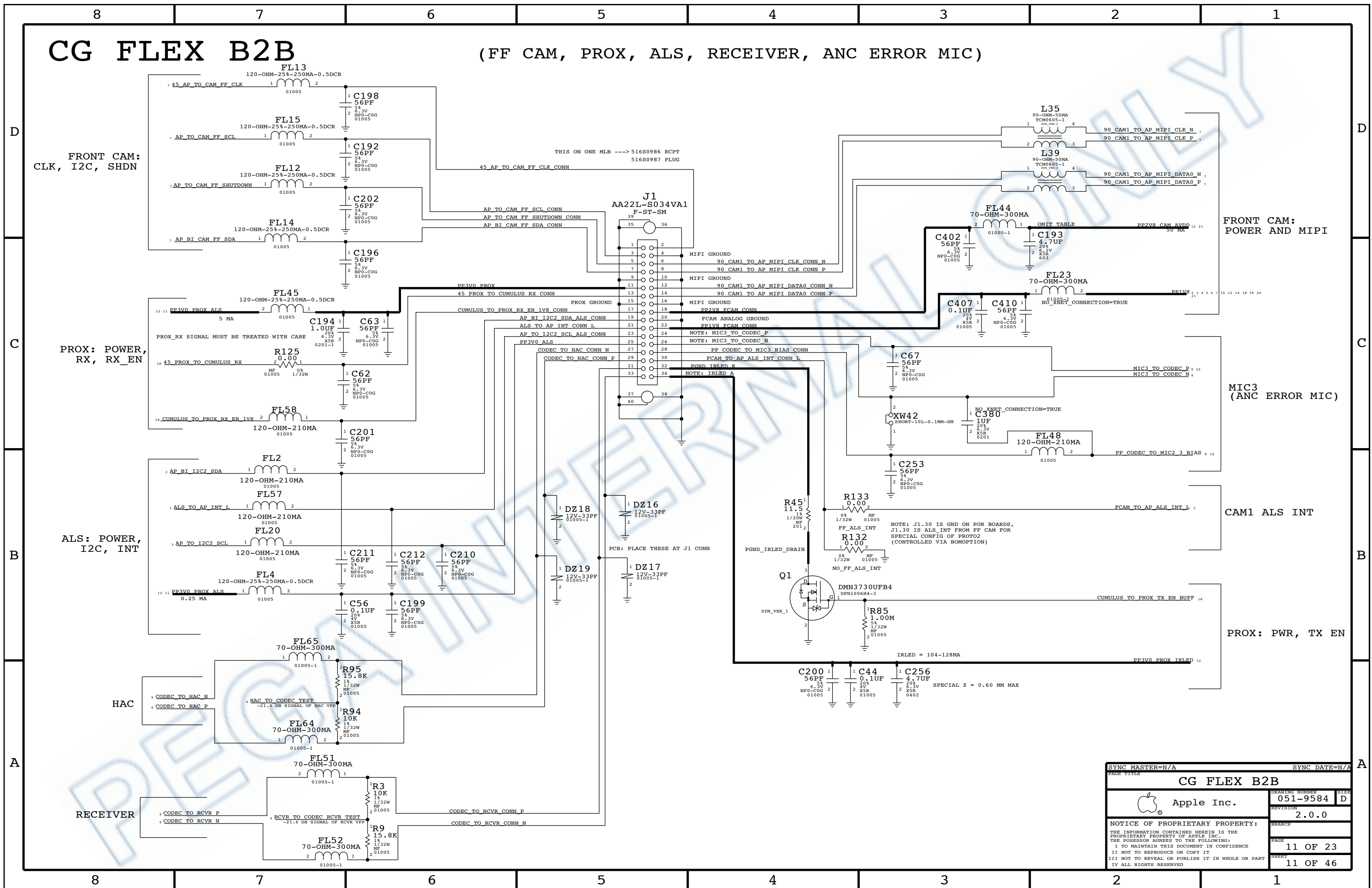
DIGITAL SYSTEM I/O



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CG FLEX B2B

(FF CAM, PROX, ALS, RECEIVER, ANC ERROR MIC)



FRONT CAM:
CLK, I2C, SHDN

FRONT CAM:
POWER AND MIPI

PROX: POWER,
RX, RX_EN

MIC3
(ANC ERROR MIC)

ALS: POWER,
I2C, INT

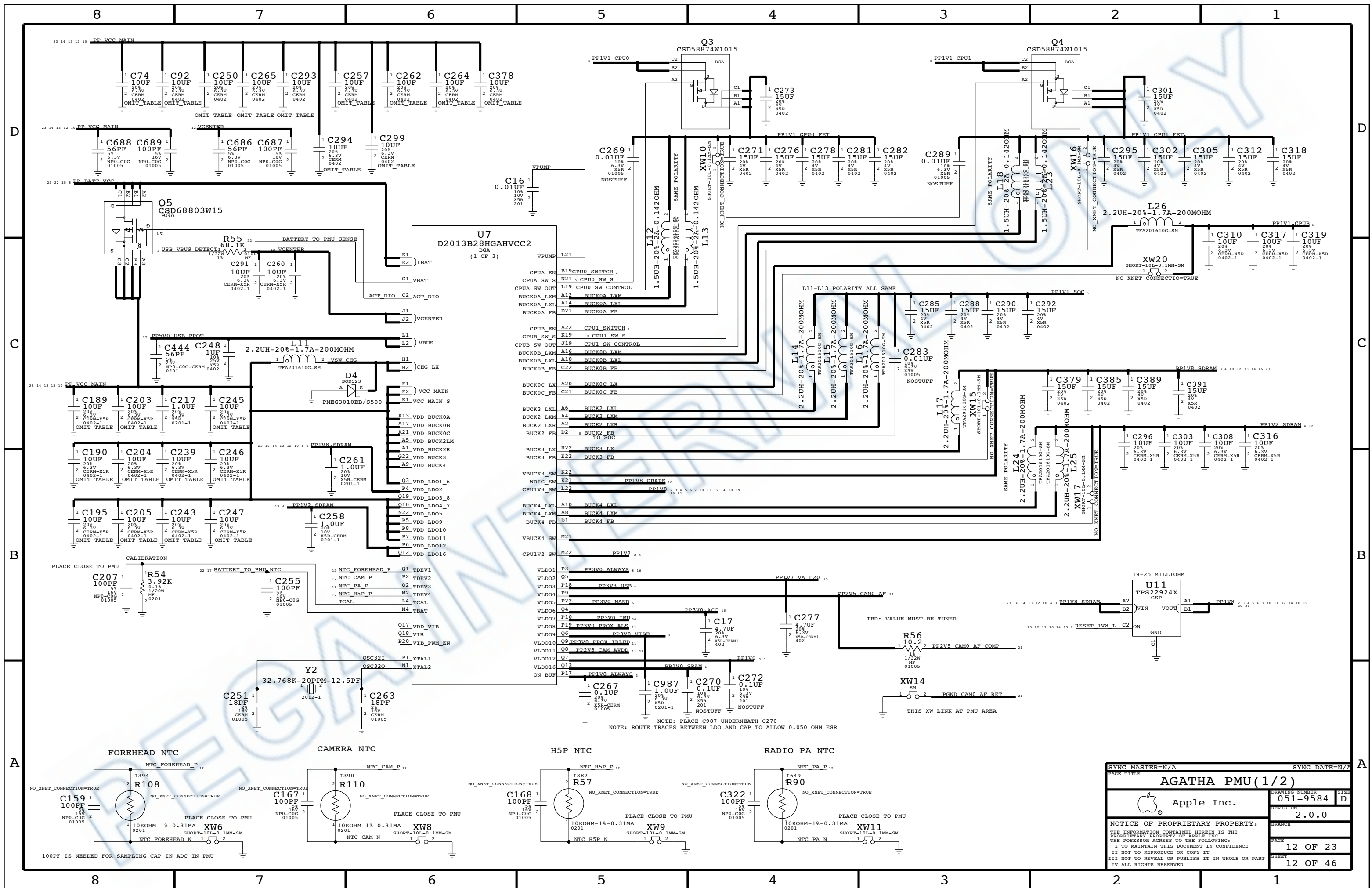
CAM1 ALS INT

PROX: PWR, TX EN

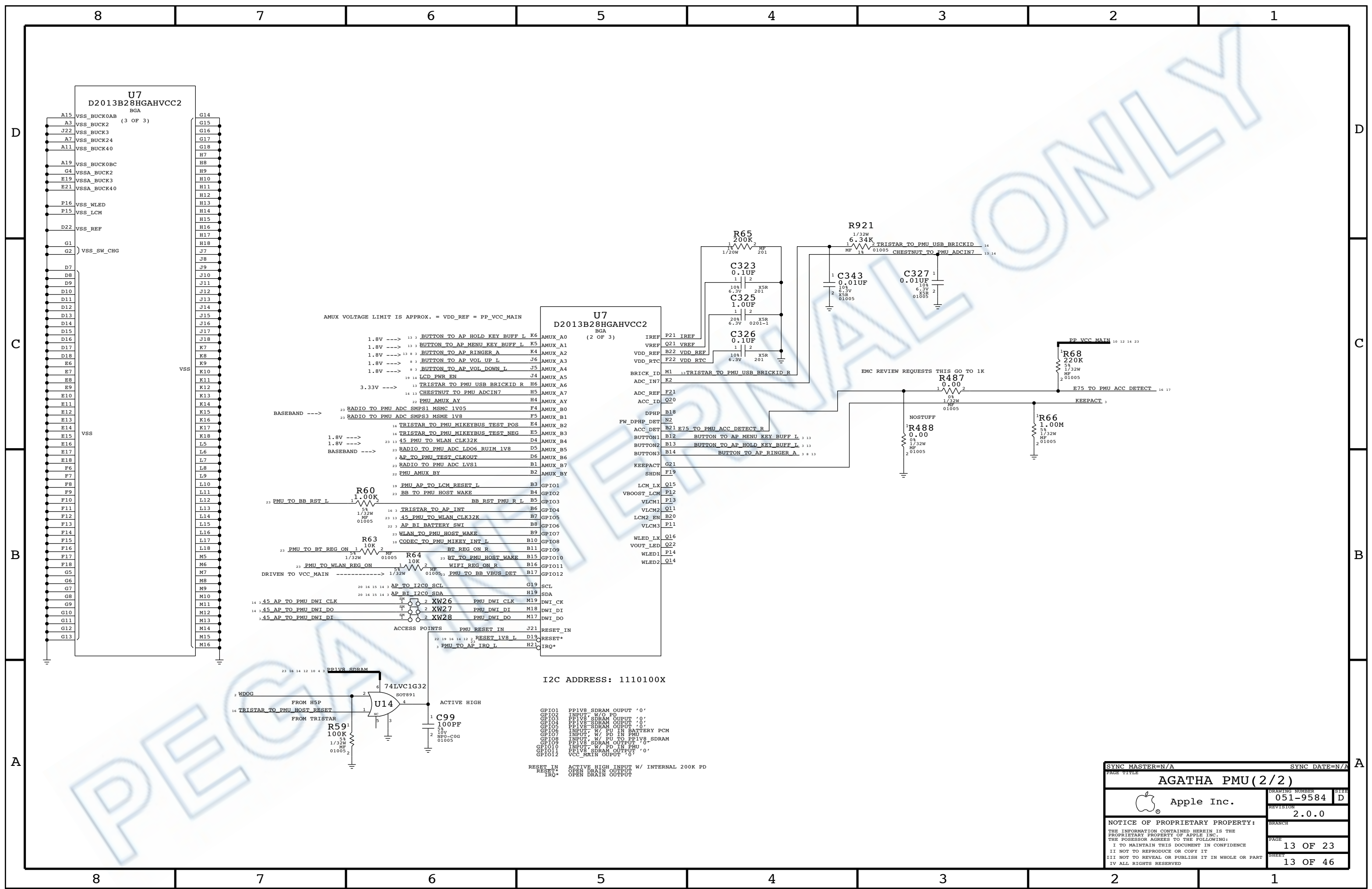
HAC

RECEIVER

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AGATHA PMU (1/2)			
Apple Inc.	DRAWING NUMBER	051-9584	SIZE
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AMUX VOLTAGE LIMIT IS APPROX. = VDD_REF = PP_VCC_MAIN

Signal	Value	Pin	Function
1.8V	---	13	BUTTON TO AP HOLD KEY BUFF L
1.8V	---	13	BUTTON TO AP MENU KEY BUFF L
1.8V	---	13	BUTTON TO AP RINGER A
1.8V	---	8	BUTTON TO AP VOL UP L
1.8V	---	8	BUTTON TO AP VOL DOWN L
3.33V	---	12	TRISTAR TO PMU USB BRICKID R
3.33V	---	14	CHESTNUT TO PMU ADCIN7
BASEBAND	---	23	RADIO TO PMU ADC SMP3 MSME LV05
BASEBAND	---	23	RADIO TO PMU ADC SMP3 MSME LV8
1.8V	---	16	TRISTAR TO PMU MIKEYBUS TEST POS
1.8V	---	16	TRISTAR TO PMU MIKEYBUS TEST NEG
1.8V	---	23	45 PMU TO WLAN CLK32K
BASEBAND	---	23	RADIO TO PMU ADC LDO6 RUM LV8
		2	AP TO PMU TEST_CLKOUT
		2	RADIO TO PMU ADC LVS1
		2	PMU AMUX BY
		19	PMU AP TO LCM RESET L
		23	BB TO PMU HOST WAKE
		23	PMU TO BB RST L
		16	TRISTAR TO AP INT
		23	45 PMU TO WLAN CLK32K
		23	AP BI BATTERY SHI
		23	WLAN TO PMU HOST WAKE
		23	CODEC TO PMU MIKEY INT L
		23	BT REG ON R
		23	PMU TO WLAN REG ON
		23	BT TO PMU HOST WAKE
		23	CODEC TO PMU MIKEY INT R
		23	WIFI REG ON R
		23	PMU TO BB VBUS DET
		20	15 14 3
		20	15 14 3
		14	45 AP TO PMU DWI CLK
		14	45 AP TO PMU DWI DO
		14	45 AP TO PMU DWI DI

Pin	Signal	Function
1	IREF	P21 IREF
2	VREF	Q21 VREF
3	VDD_REF	B22 VDD_REF
4	VDD_RTC	F22 VDD_RTC
5	BRICK_ID	M1 TRISTAR TO PMU USB BRICKID R
6	ADC_IN7	K2
7	ADC_REF	F21
8	ACC_ID	Q20
9	DPHP	B18
10	FW DPHP_DET	N2
11	ACC_DET	B21 E75 TO PMU ACC DETECT R
12	BUTTON1	B12 BUTTON TO AP MENU KEY BUFF L
13	BUTTON2	B13 BUTTON TO AP HOLD KEY BUFF L
14	BUTTON3	B14 BUTTON TO AP RINGER A
15	KEEPACT	G21
16	SHDN	F19
17	LCM_LX	Q15
18	VBOOST_LCM	P12
19	VLCM1	P13
20	VLCM2	Q11
21	LCM2_EN	B20
22	VLCM3	P11
23	WLED_LX	Q16
24	VOUT_LED	Q22
25	WLED1	P14
26	WLED2	Q14

I2C ADDRESS: 1110100X

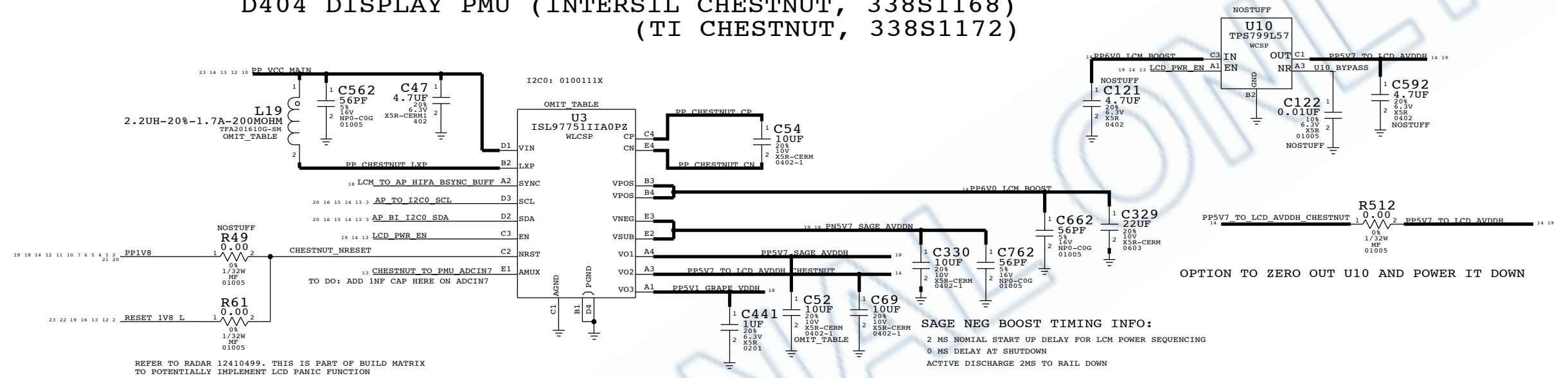
GPIO Pin	Function
GPIO1	PP1V8 SDRAM OUTPUT '0'
GPIO2	INPUT* W/O PD
GPIO3	PP1V8 SDRAM OUTPUT '0'
GPIO4	PP1V8 SDRAM OUTPUT '0'
GPIO5	PP1V8 SDRAM OUTPUT '0'
GPIO6	INPUT* W/ PU IN BATTERY PCM
GPIO7	INPUT* W/ PD IN PMU
GPIO8	INPUT* W/ PU TO PP1V8 SDRAM
GPIO9	PP1V8 SDRAM OUTPUT '0'
GPIO10	INPUT* W/ PD IN PMU
GPIO11	PP1V8 SDRAM OUTPUT '0'
GPIO12	VCC_MAIN OUTPUT '0'

RESET_IN ACTIVE HIGH INPUT W/ INTERNAL 200K PD
 RESET* OPEN DRAIN OUTPUT
 IRQ* OPEN DRAIN OUTPUT

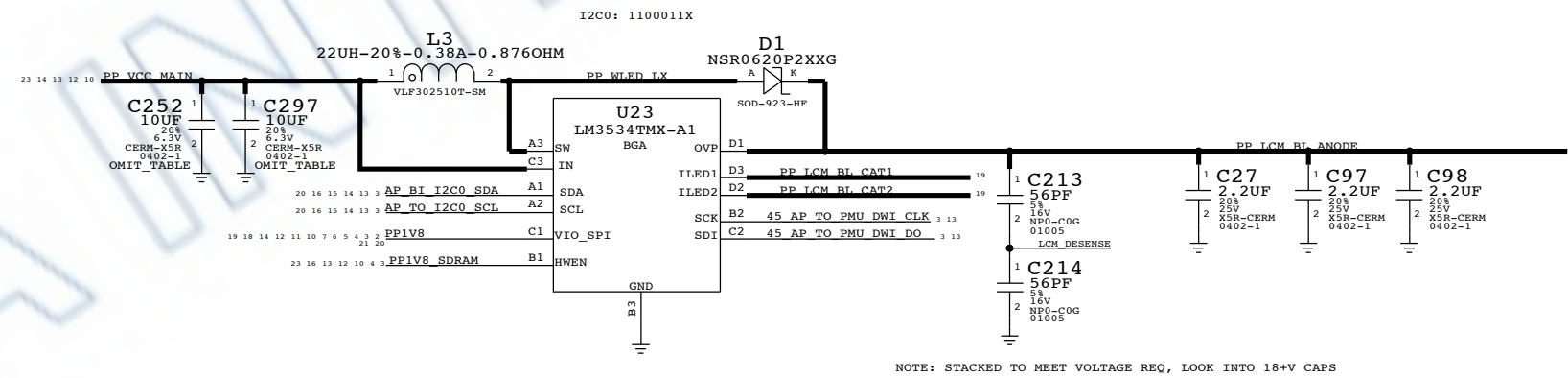
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AGATHA PMU (2/2)					
Apple Inc.		DRAWING NUMBER	051-9584	SIZE	D
		REVISION	2.0.0	BRANCH	
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		13 OF 46			

CHESTNUT, BACKLIGHT DRIVER

D404 DISPLAY PMU (INTERSIL CHESTNUT, 338S1168) (TI CHESTNUT, 338S1172)



D404 BACKLIGHT DRIVER

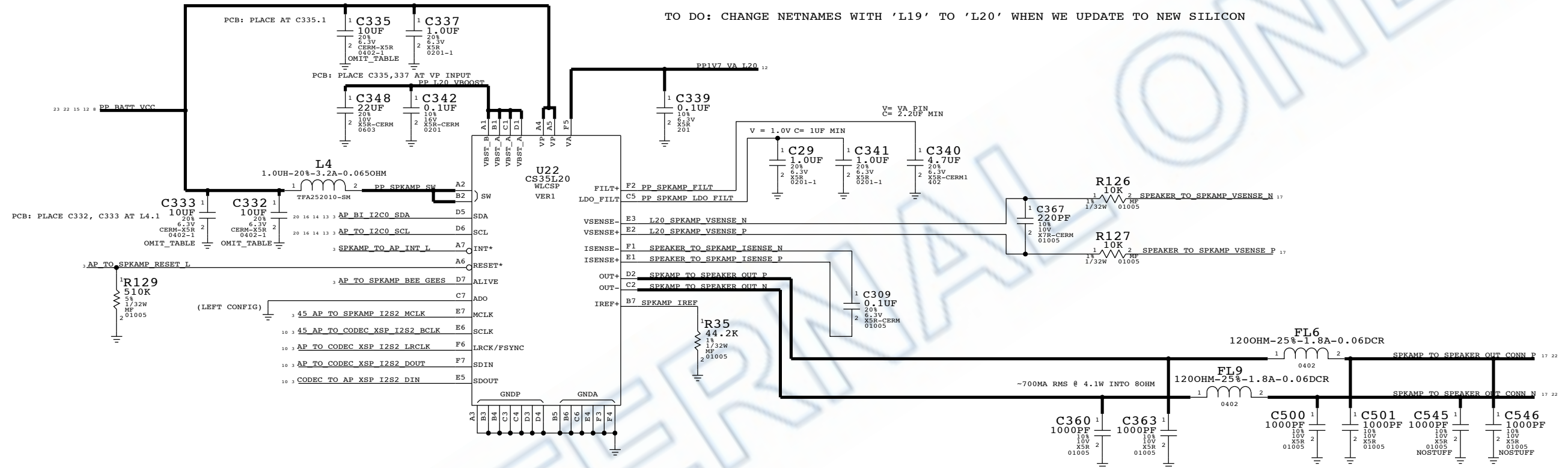


PAGE TITLE		SYNC DATE=N/A	
CHESTNUT + BACKLIGHT DRIVER			
Apple Inc.	DRAWING NUMBER	051-9584	SIZE
	REVISION	2.0.0	D
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SPEAKER AMP, LED DRIVER

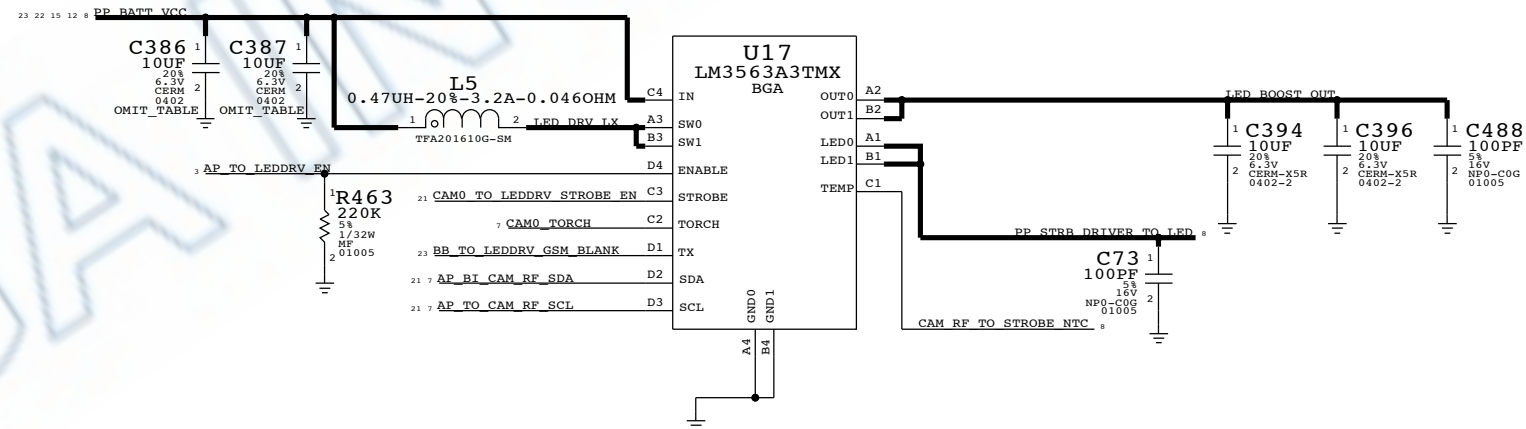
SPEAKER AMP (REPLACED WITH L20)

I2C ADDRESS: 1000000X



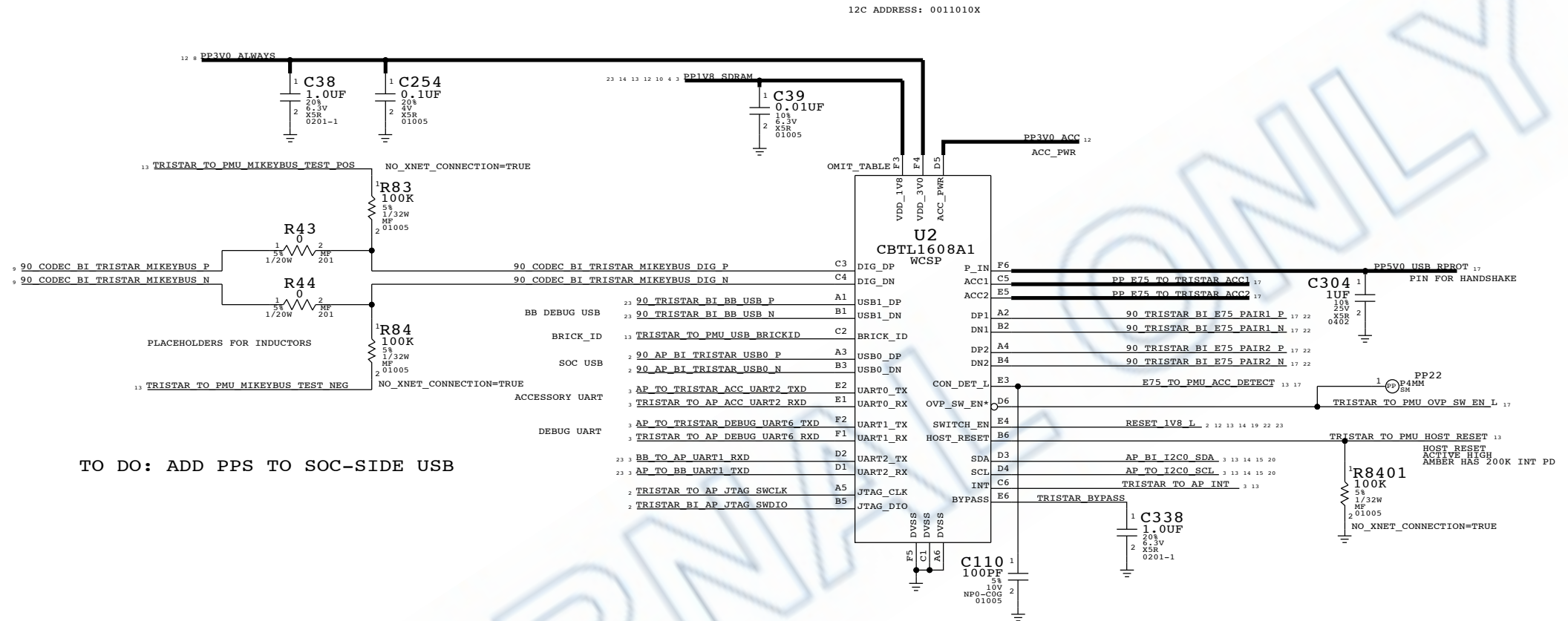
LED DRIVER

I2C ADDRESS: 1100011X



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE SPKR AMP + LED DRIVER			
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		SHEET	15 OF 46

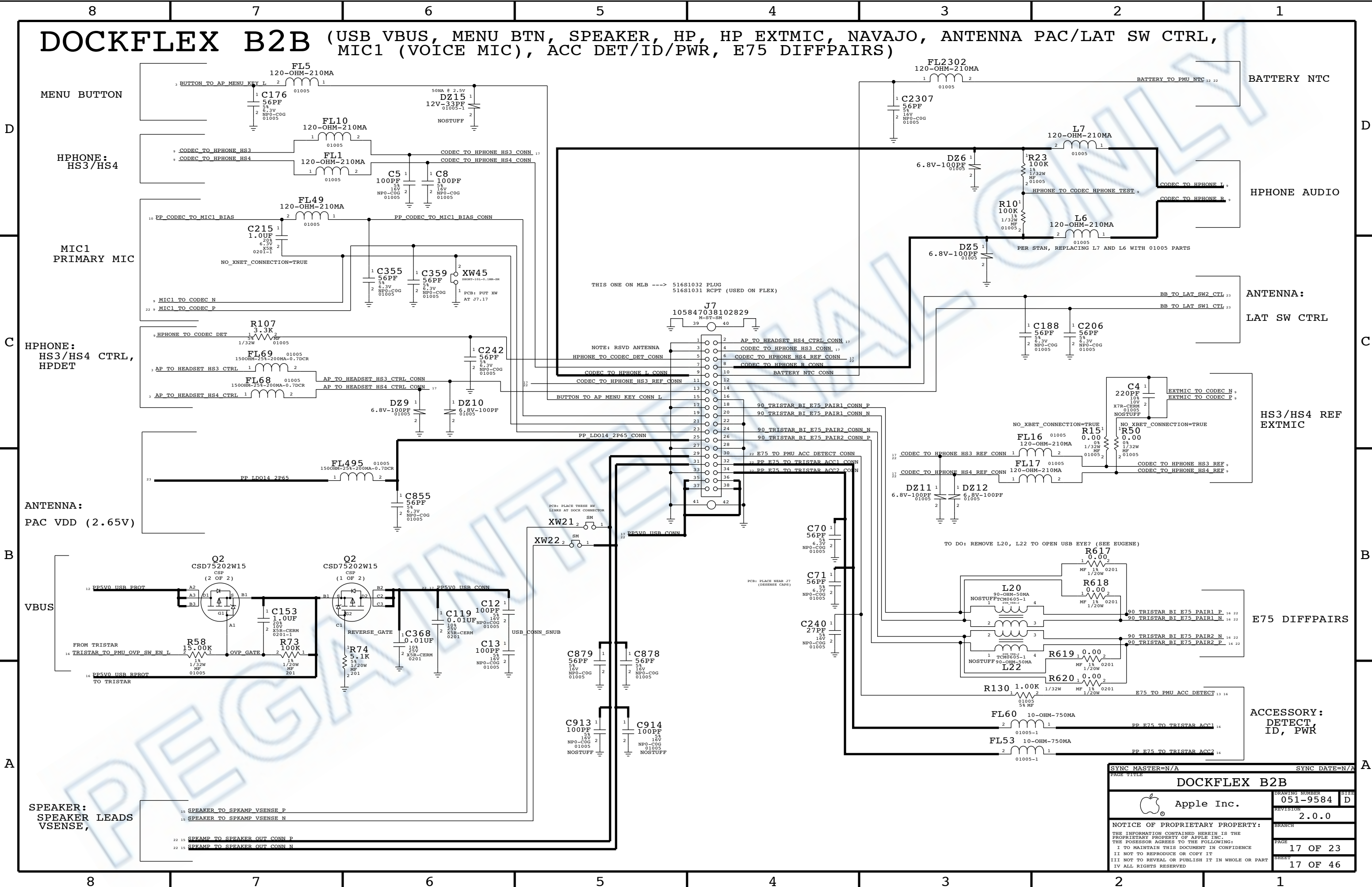
TRISTAR



TO DO: ADD PPS TO SOC-SIDE USB

SYNC MASTER=N/A		SYNC DATE=N/A	
TRISTAR			
Apple Inc.		DRAWING NUMBER	SIZE
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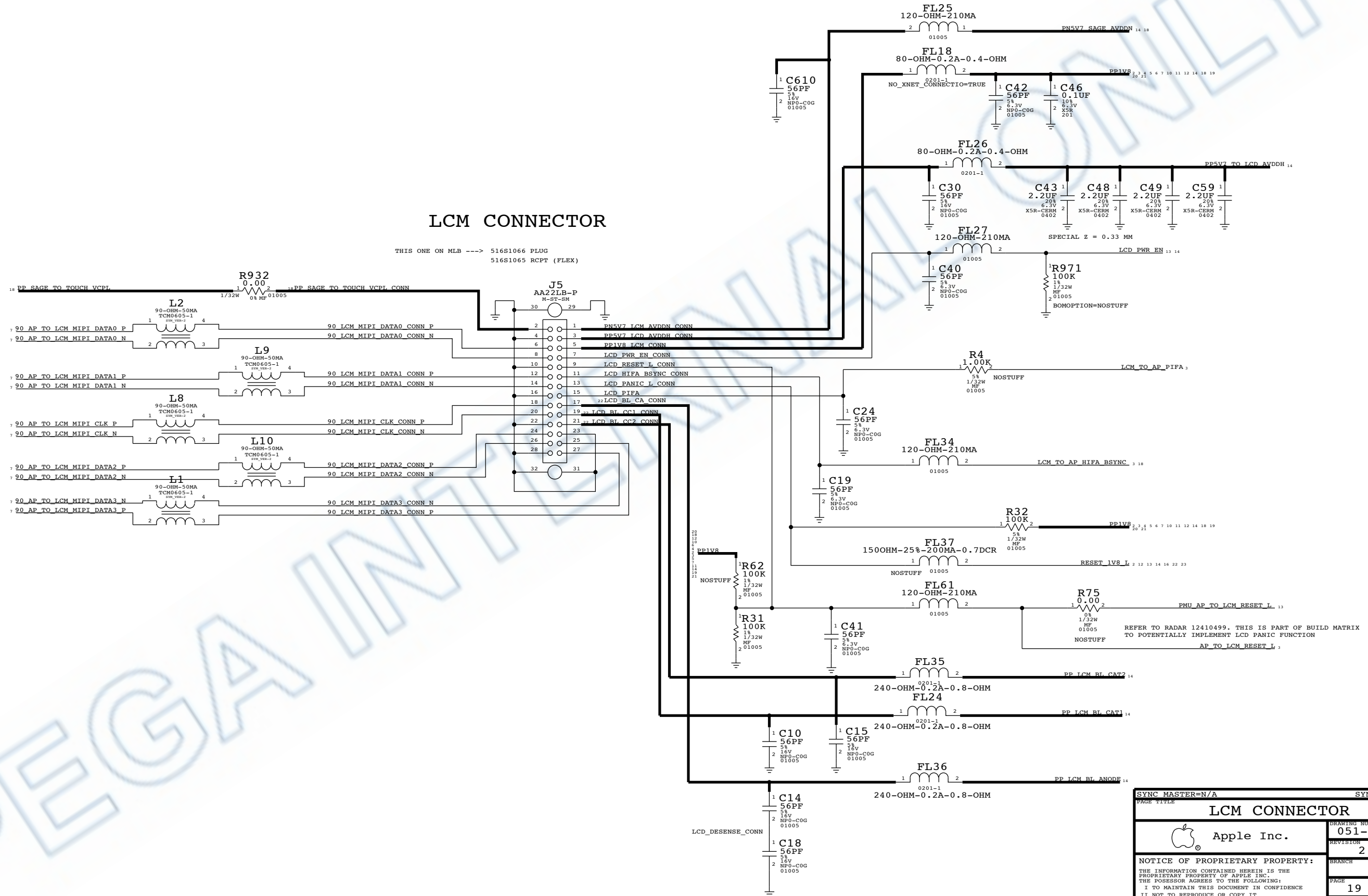
DOCKFLEX B2B (USB VBUS, MENU BTN, SPEAKER, HP, HP EXTMIC, NAVAJO, ANTENNA PAC/LAT SW CTRL, MIC1 (VOICE MIC), ACC DET/ID/PWR, E75 DIFFPAIRS)



SYNC MASTER=N/A		SYNC DATE=N/A	
DOCKFLEX B2B			
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LCM B2B

LCM CONNECTOR



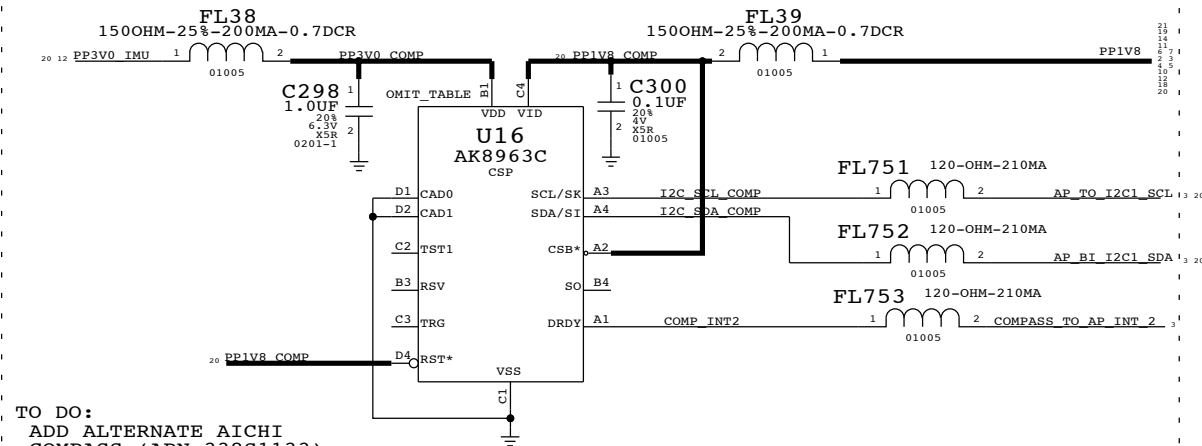
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LCM CONNECTOR			
DRAWING NUMBER	051-9584	SIZE	D
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SENSORS

THIS PART OUTSIDE OF SHIELD

COMPASS

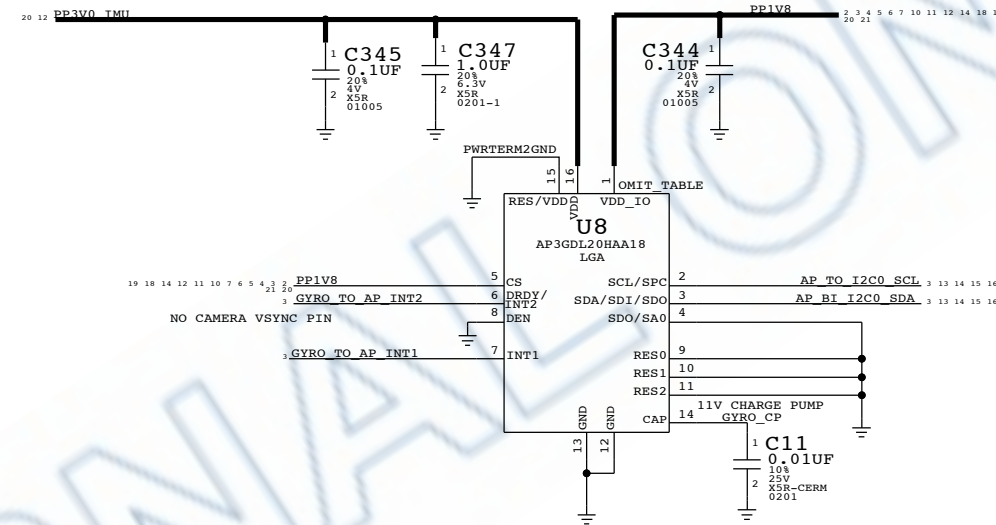
COMPASS DEVICE: 338S1014
COMPASS INTERPOSER: 998-5120



THESE PARTS INSIDE OF SHIELD

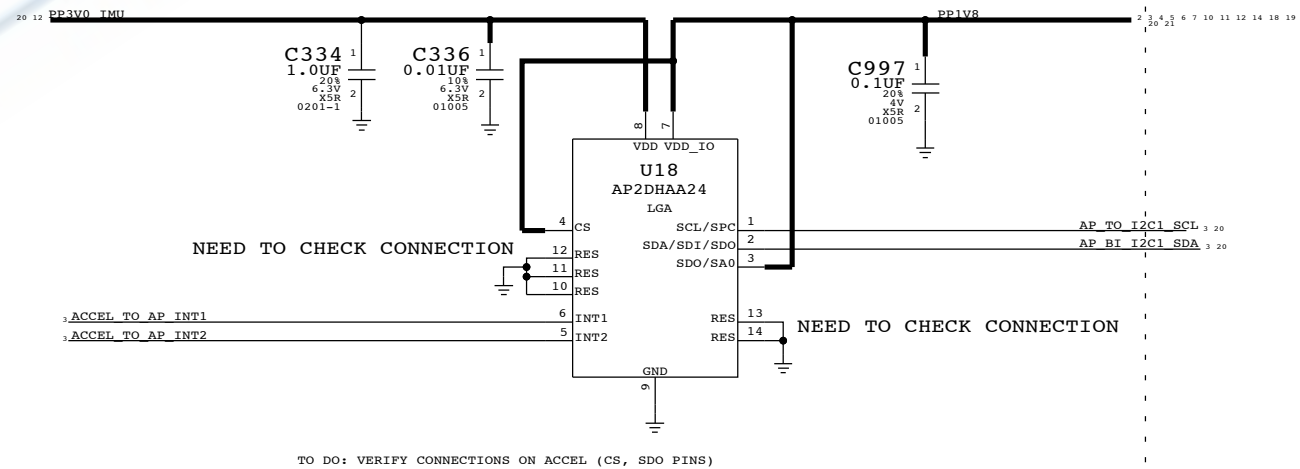
GYRO

AP3GDL20H, APN 338S1158



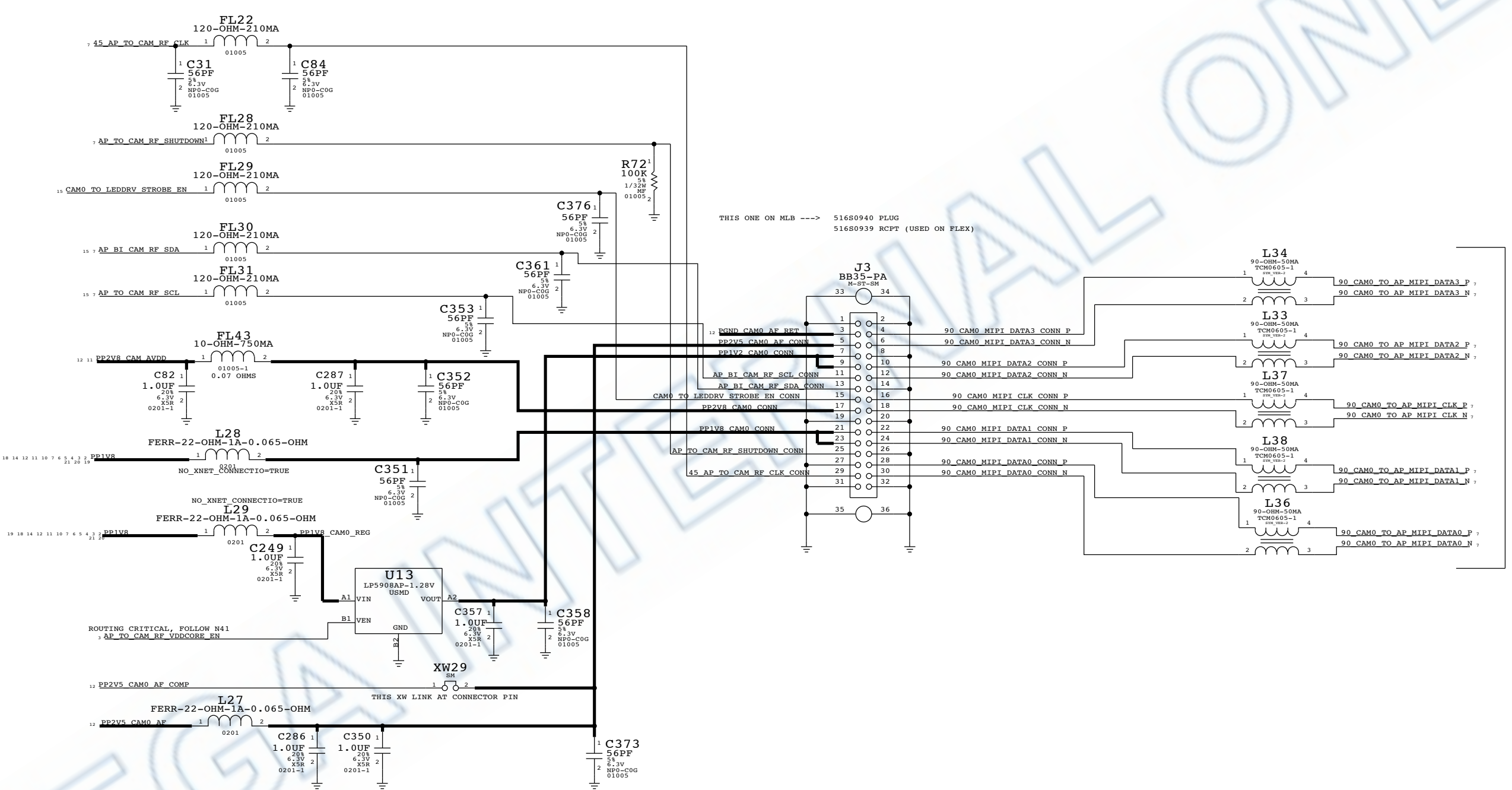
ACCELEROMETER

AP2DHAA, APN 338S1114



PAGE TITLE		SYNC MASTER=N/A		SYNC DATE=N/A	
OSCAR + SENSORS					
Apple Inc.		DRAWING NUMBER	051-9584	SIZE	D
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CAM0: MAIN CAMERA CONNECTOR

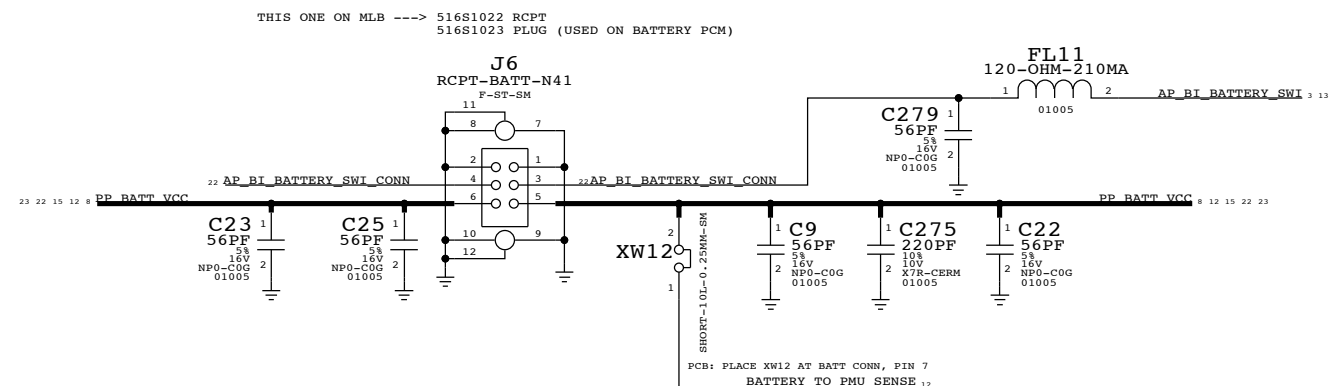


CAM0:
4-LANE MIPI

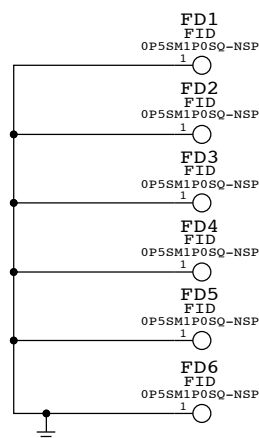
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CAM0 CONNECTOR			
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		SHEET	21 OF 46
		SIZE	D

BATT CONN, TPS, STANDOFFS/SHIELDS/FIDUCIALS

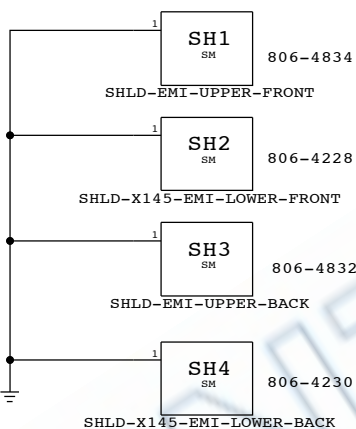
BATTERY CONN



FIDUCIALS

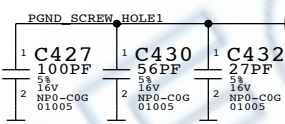


SHIELDS

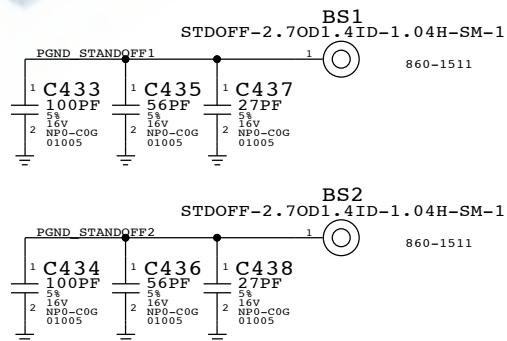


AC COUPLED SCREW HOLES + STANDOFFS (ON NORTH END OF SINGLE_BRD, TO MITIGATE COMPASS RETURN CURRENTS)

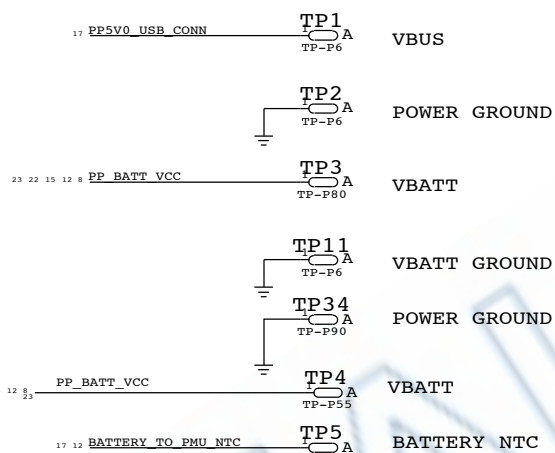
SCREW HOLES



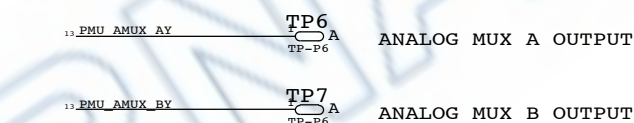
STANDOFFS



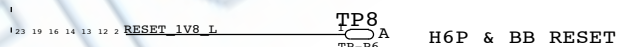
POWER TP



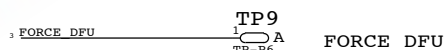
SUPER TP



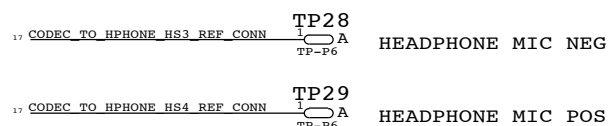
RESET



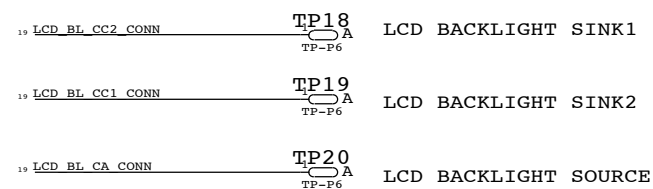
DFU



HEADPHONE MIC

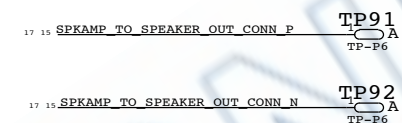


LCM BACKLIGHT

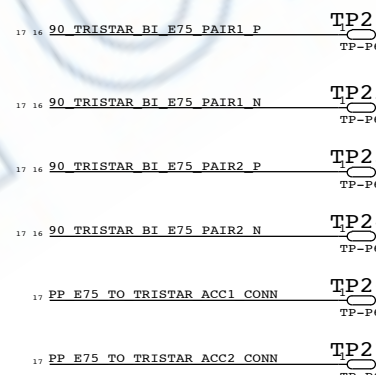


TESTPOINTS

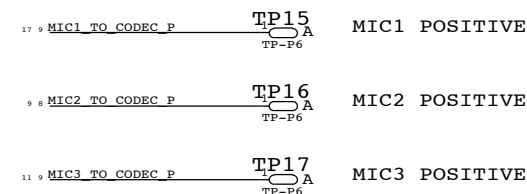
SPKAMP OUTPUT TP



E75 - USB/UART/ID/POWER



MIC AUDIO



DRIVE MIC WRT NEAREST GROUND TEST POINT

SYNC MASTER=N/A		SYNC DATE=N/A	
BATT B2B, TPS, PD FEATURES			
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RADIO_MLB HIERARCHICAL SYMBOL

AP/RADIO INTERFACE

RF
I612



SYNC MASTER=N/A		SYNC DATE=N/A	
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PEGASUS INTERNAL ONLY

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1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
2	0001669557	ENGINEERING RELEASED		2012-10-14

X155 RADIO_MLB SUBDESIGN - PROTO1

10/3/2012

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2	AP INTERFACE & DEBUG CONNECTORS
3	CELLULAR PMU: (1 OF 2)
4	CELLULAR PMU: (2 OF 2)
5	CELLULAR BASEBAND: (1 OF 2)
6	CELLULAR BASEBAND: (2 OF 2)
7	CELLULAR RF TRANSCEIVER: (1 OF 2)
8	CELLULAR RF TRANSCEIVER: (2 OF 2)
9	CELLULAR FRONT END: TX AND RX MATCHING
10	CELLULAR FRONT END: SAW BANKS
11	CELLULAR FRONT END: BAND 1/4 PAT
12	CELLULAR FRONT END: BAND 2/3 PAD
13	CELLULAR FRONT END: BAND 20 PAD
14	CELLULAR FRONT END: BAND 5/8 PAD
15	CELLULAR FRONT END: BAND 13/17 PAD
16	CELLULAR FRONT END: PA DCDC CONVERTER
17	CELLULAR FRONT END: 2G FEM
18	CELLULAR FRONT END: RX DIVERSITY
19	CELLULAR FRONT END: GPS LNA
20	CELLULAR FRONT END: ANTENNA FEEDS
21	FRONT END LOGIC TABLE (1 OF 2)
22	FRONT END LOGIC TABLE (2 OF 2)
23	WIFI/BT: MODULE AND FRONT END

BOARD ID BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
118S0621	1	1.00M 1% 01005	R25_RF	Y	N51_CFG_A
118S0732	1	50K 1% 01005	R26_RF	Y	N51_CFG_A
117S0159	1	470K 5% 01005	R25_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N51_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_A
118S0726	1	162K 1% 01005	R26_RF	Y	N53_CFG_A
118S0626	1	100K 1% 01005	R25_RF	Y	N53_CFG_B
118S0623	1	267K 1% 01005	R26_RF	Y	N53_CFG_B
118S0659	1	255K 1% 01005	R25_RF	Y	N48_CFG_A
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_A
118S0689	1	147K 1% 01005	R25_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R26_RF	Y	N48_CFG_B
118S0626	1	100K 1% 01005	R25_RF	Y	N49_CFG_A
118S0650	1	499K 1% 01005	R26_RF	Y	N49_CFG_A
118S0732	1	50K 1% 01005	R25_RF	Y	N49_CFG_B
118S0621	1	1.00M 1% 01005	R26_RF	Y	N49_CFG_B

SCH : 951-2446
 BOM : 939-0308
 BOARD : 920-2148

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
951-2446	1	X145_RADIO_MLB	SCH	Y	
825-2029	1	EEE FOR 939-0308	EEEE_????	Y	NA

DRAWING TITLE		DRAWING NUMBER	SIZE
X155 RADIO_MLB SCHEMATIC		051-9584	D
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1

AP INTERFACE & DEBUG CONNECTORS

AP CONNECTIONS

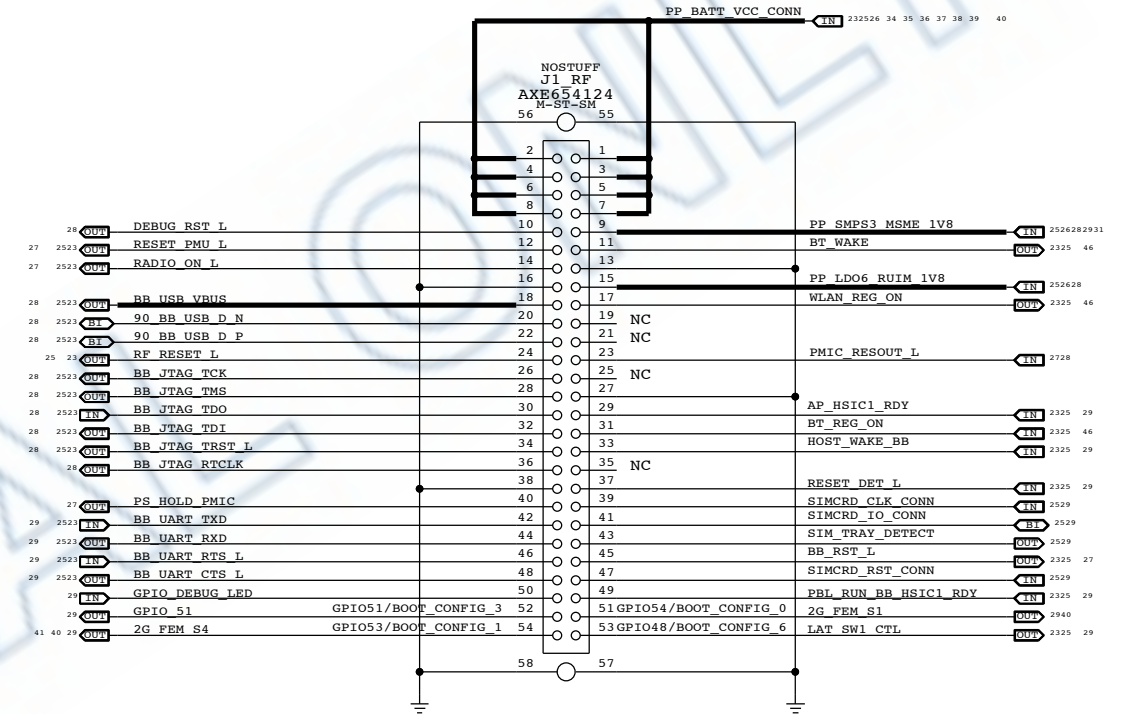
IN = FROM AP
OUT = TO AP

17	PP BATT VCC CONN	OUT
22	PP VCC MAIN WLAN	OUT
4	TX GTR THRESH	OUT
4	BB_RST_L	OUT
4	RESET_DET_L	OUT
4	RADIO_ON_L	OUT
4	RESET_PMU_L	OUT
6	HOST_WAKE_BB	OUT
6	RF_RESET_L	OUT
6	PBL_RUN_BB_HSI1_RDY	OUT
23	WLAN_HSI3_RESUME	OUT
23	AP_WAKE_MODEM	OUT
6	AP_HSI1_RDY	OUT
6	50_HSI1_BB_DATA	OUT
6	50_HSI1_BB_STROBE	OUT
6	BB_HSI1_REMOTE_WAKE	OUT
6	BB_UART_TXD	OUT
6	BB_UART_RXD	OUT
6	BB_UART_RTS_L	OUT
6	BB_UART_CTS_L	OUT
6	BB_USB_VBUS	OUT
6	90_BB_USB_D_P	OUT
6	90_BB_USB_D_N	OUT
6	BB_I2S_CLK	OUT
6	BB_I2S_WS	OUT
6	BB_I2S_TXD	OUT
6	BB_I2S_RXD	OUT
6	PP_SYNC	OUT
23	PP_WL_BT_VDDIO_AP	OUT
23	CLK32K_AP	OUT
23	WLAN_REG_ON	OUT
23	WLAN_UART_TXD	OUT
23	WLAN_UART_RXD	OUT
23	HOST_WAKE_WLAN	OUT
23	WLAN_HSI3_DEVICE_RDY	OUT
23	AP_HSI3_RDY	OUT
23	50_HSI1_WLAN_DATA	OUT
23	50_HSI1_WLAN_STROBE	OUT
23	HOST_WAKE_BT	OUT
23	BT_WAKE	OUT
23	BT_UART_TXD	OUT
23	BT_UART_RXD	OUT
23	BT_UART_RTS_L	OUT
23	BT_UART_CTS_L	OUT
23	BT_REG_ON	OUT
23	BT_PCM_CLK	OUT
23	BT_PCM_SYNC	OUT
23	BT_PCM_OUT	OUT
23	BT_PCM_IN	OUT
6	LAT_SW1_CTL	OUT
6	LAT_SW2_CTL	OUT
20	BB_SPI_TO_PAC_CS	OUT
20	BB_SPI_TO_PAC_DATA_MOSTI	OUT
20	BB_SPI_TO_PAC_CLK	OUT
20	PAC_TO_BB_SPI_DATA_MISO	OUT
10	PP_LDO14_2V65	OUT
5	BB_JTAG_TCK	OUT
5	BB_JTAG_TDI	OUT
5	BB_JTAG_TMS	OUT
5	BB_JTAG_TRST_L	OUT
5	BB_JTAG_TDO	OUT
23	ADC_SMPS1_MSME_1V05	OUT
23	ADC_SMPS3_MSME_1V8	OUT
23	ADC_LDO6_RUIM_1V8	OUT
23	ADC_LVS1	OUT
23	BB_IPC_GPIO	OUT
23	OSCAR_CONTEXT_A	OUT
23	OSCAR_CONTEXT_B	OUT

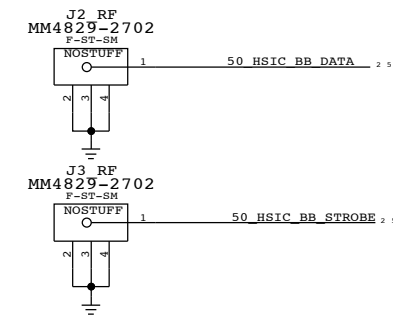
PROBE POINTS

PP1 RF	1	BB_ERROR_FLAG	6
PP2 RF	1	SLEEP_CLK_32K	4,5
PP3 RF	1	PMIC_SSB1	4,5
PP10 RF	1	19F2M_MDM	4,5
PP11 RF	1	CLK32K_AP	2,23
PP14 RF	1	AP_HSI3_RDY	2,23
PP15 RF	1	WLAN_HSI3_DEVICE_RDY	2,23
PP16 RF	1	WLAN_HSI3_RESUME	2,23
PP19 RF	1	WTR_SSB1_TX_GPS	6,7
PP20 RF	1	WTR_SSB1_PRX_DRX	6,7
PP21 RF	1	WTR_RX_ON	6,7
PP22 RF	1	WTR_RF_ON	6,7
PP40 RF	1	WLAN_COEX_TXD	23
PP41 RF	1	LTE_COEX_TXD	6,23
PP42 RF	1	50_HSI1_BB_STROBE	2,5
PP43 RF	1	50_HSI1_BB_DATA	2,5
PP44 RF	1	50_HSI1_WLAN_STROBE	2,23
PP45 RF	1	50_HSI1_WLAN_DATA	2,23
PP46 RF	1	BT_UART_TXD	2,23
PP47 RF	1	BT_UART_RXD	2,23
PP4 RF	1	BB_I2S_CLK	2,4
PP5 RF	1	BB_I2S_WS	2,4
PP6 RF	1	BB_I2S_RXD	2,4
PP7 RF	1	BB_I2S_TXD	2,4

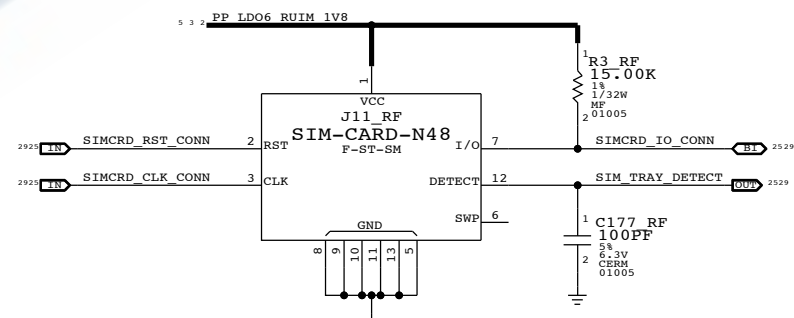
DEBUG CONNECTOR



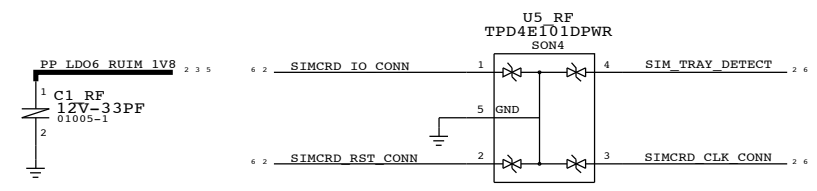
BOOT OPTIONS	BOOT CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION								
		6	5	4	3	2	1	0		
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	0	X
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	0	1	0	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1	X
ENABLE_SAHARA_PROTOCOL	0X08	X	1	0	0	1	0	X	X	X



SIM CARD CONNECTOR

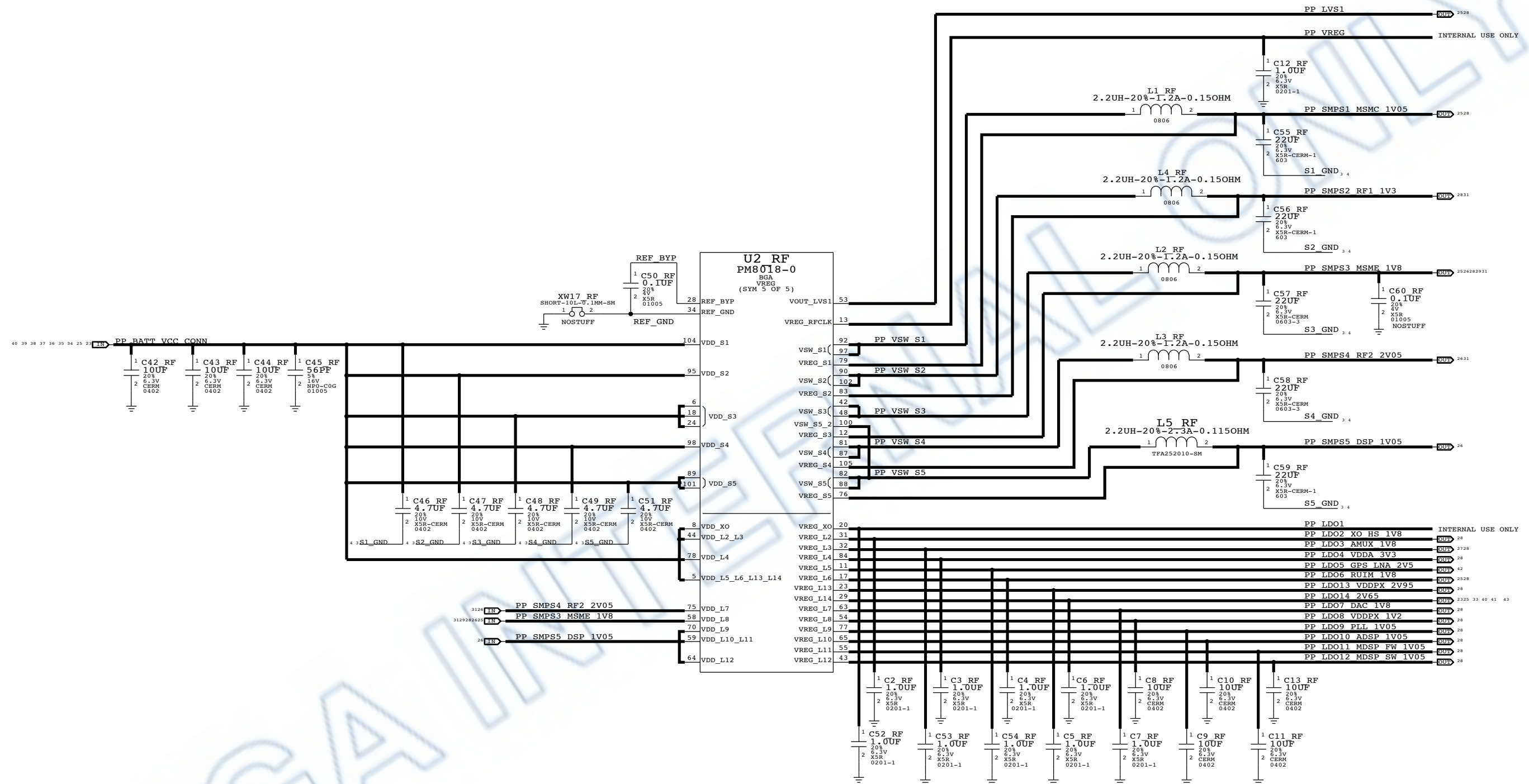


SIM CARD ESD PROTECTION



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AP INTERFACE & DEBUG CONNECTORS		051-9584		D
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		2.0.0		
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SHEET		25 OF 46		

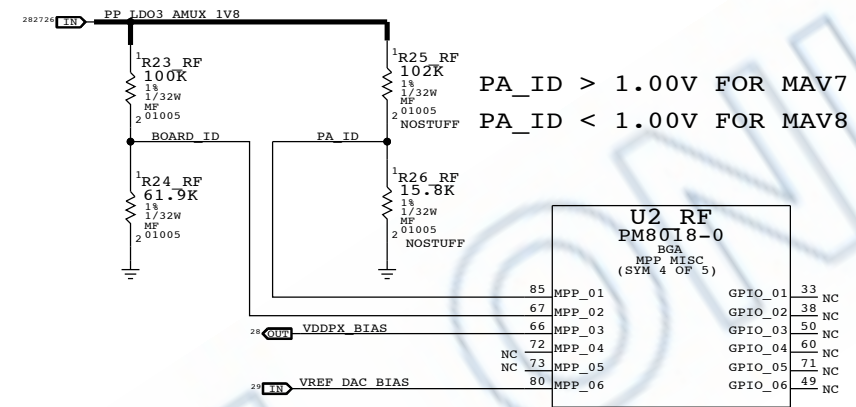
PMU (1 OF 2)



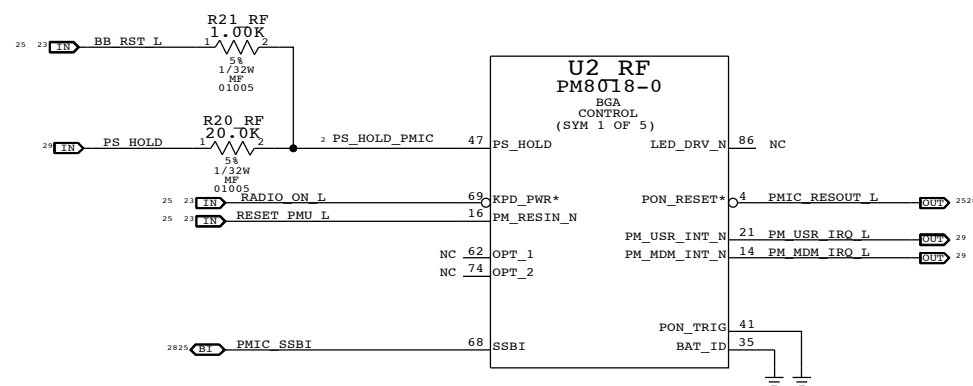
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	SHEET	26 OF 46
	SIZE	D

PMU (2 OF 2)

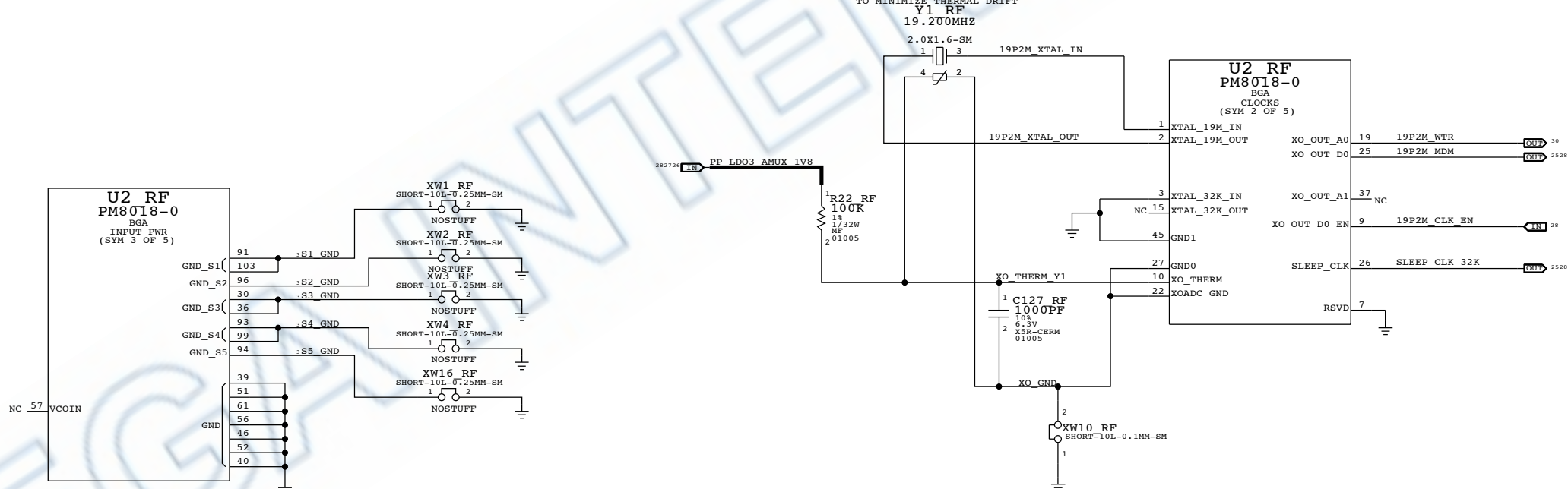
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT



PA THERMISTOR REMOVED TO MATCH N41, AP SECTION
NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.

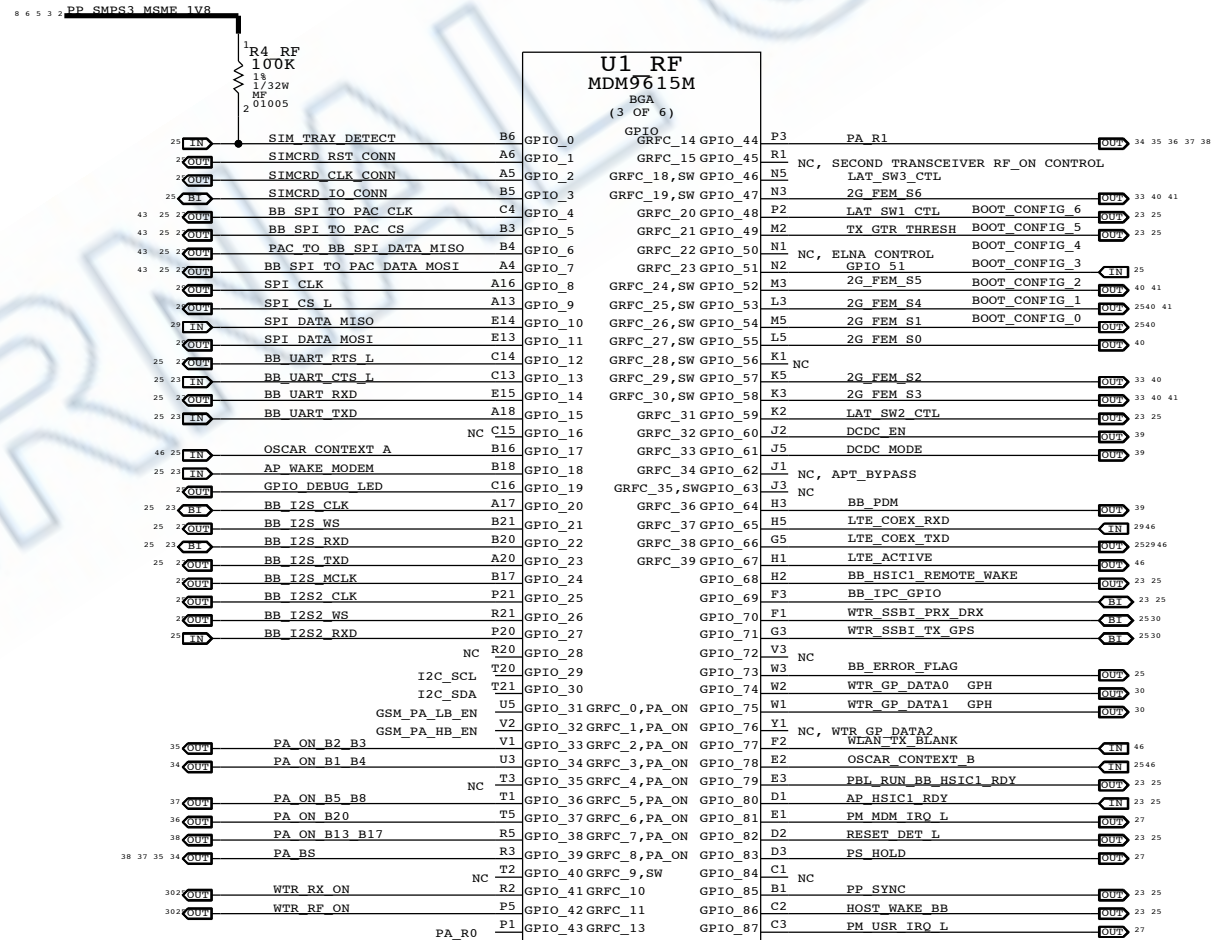
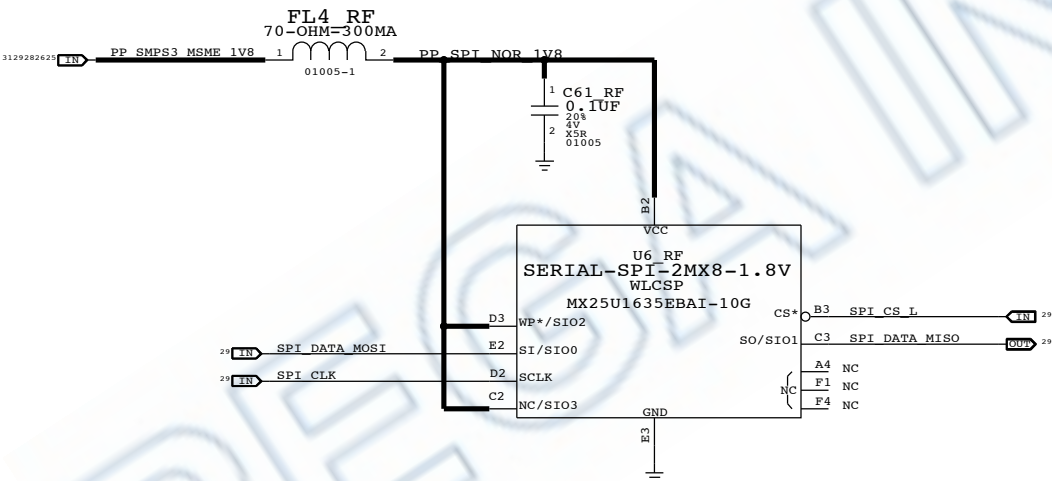
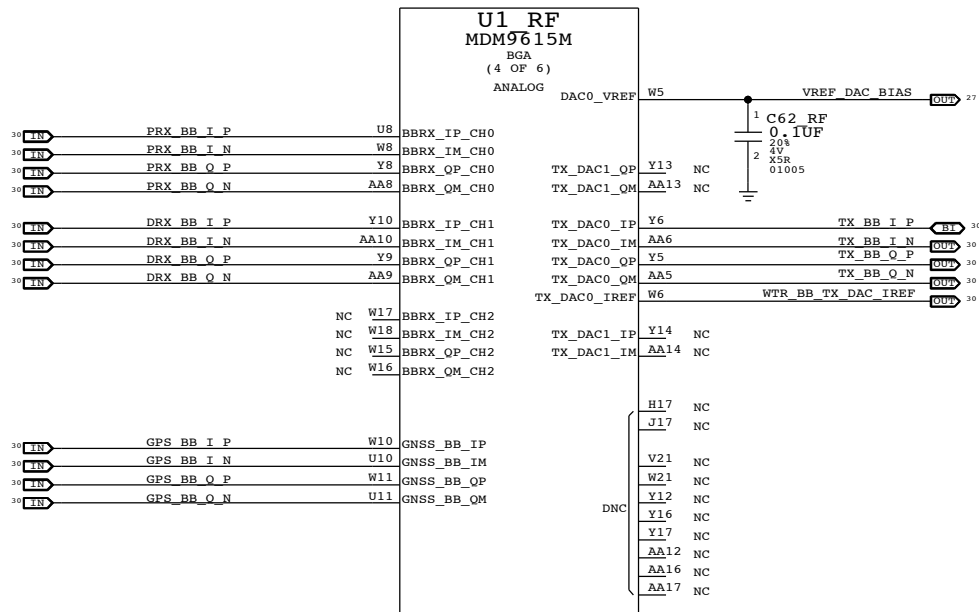


GND NEEDS TO BE CLEARED UNDER THIS CRYSTAL
TO MINIMIZE THERMAL DRIFT



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BASEBAND (2 OF 2)

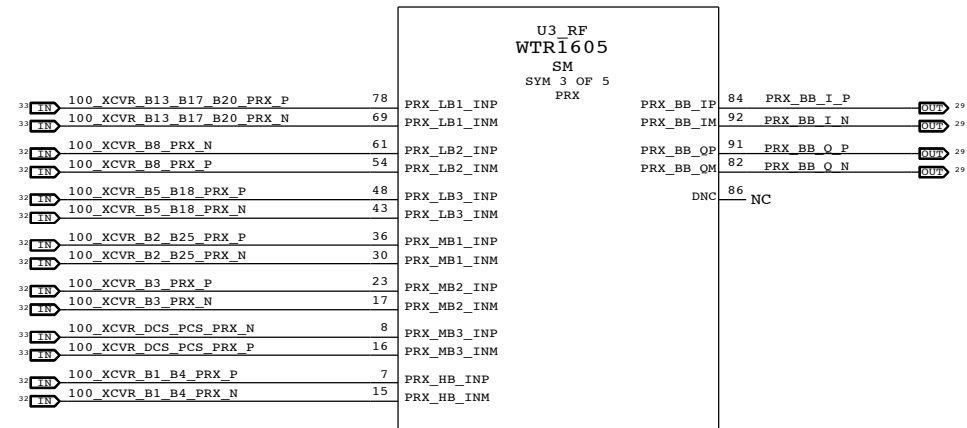


LTE WLAN PRIORITY [ALIAS] LTE COEX_RXD [2946]
LTE FRAME SYNC [ALIAS] LTE COEX_TXD [252946]

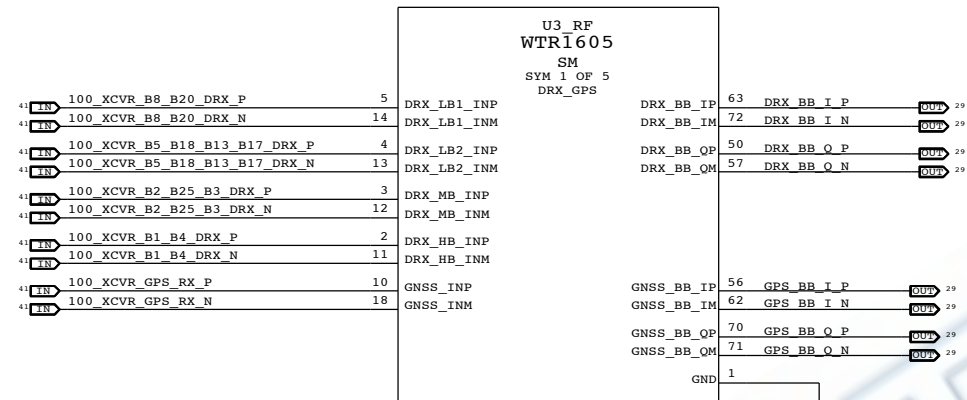
PAGE TITLE CELLULAR BASEBAND: (2 OF 2)		
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RF TRANSCEIVER (1 OF 4)

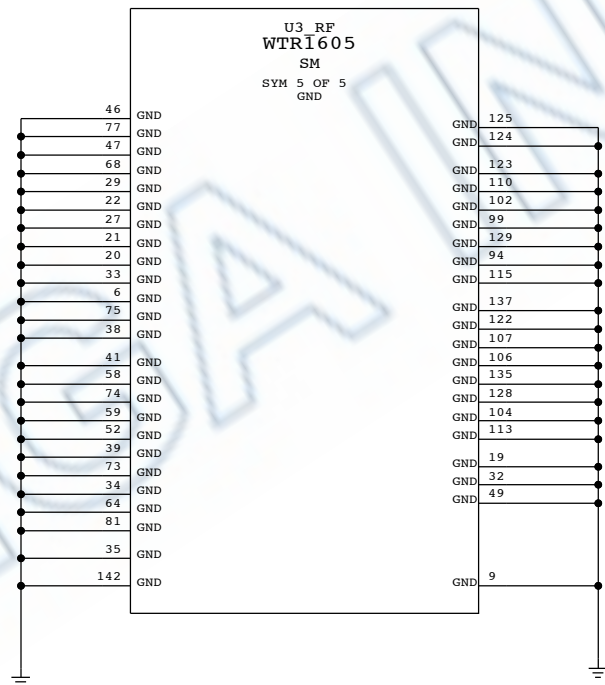
PRX TRANSCEIVER RF AND IQ PORTS



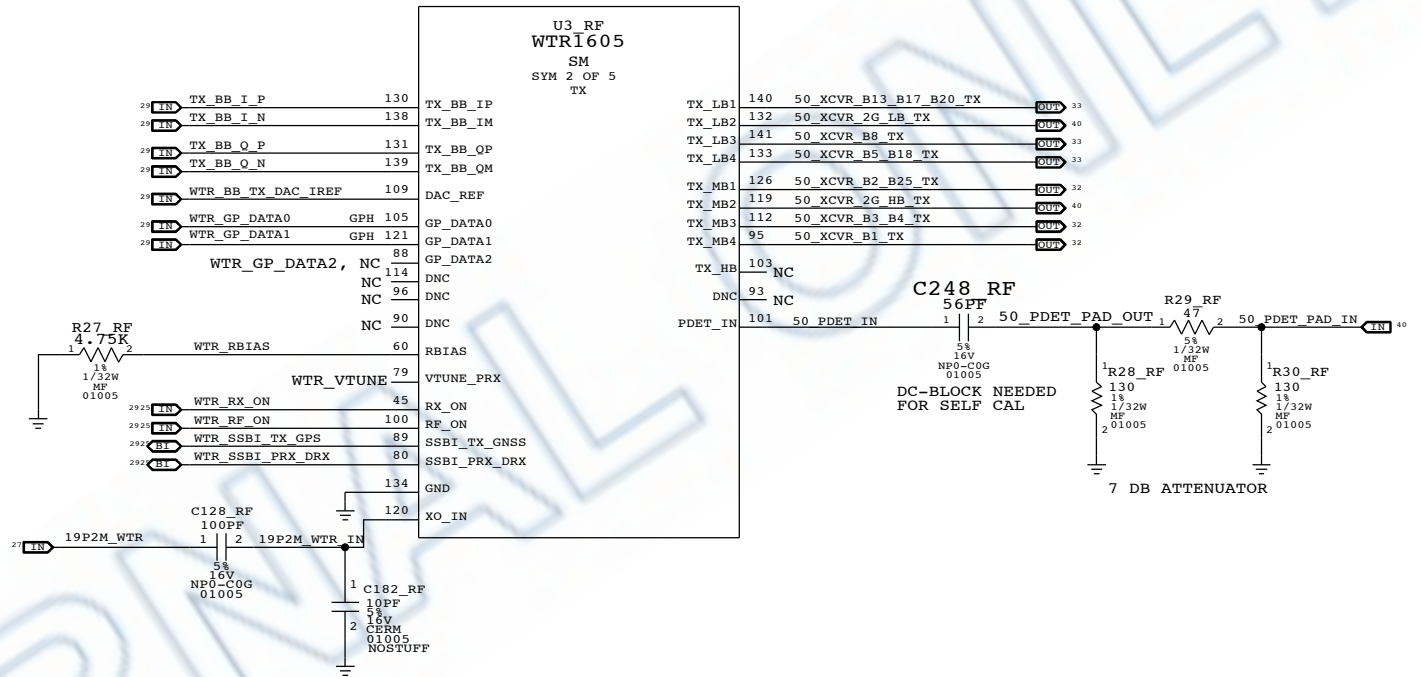
DRX TRANSCEIVER RF AND IQ PORTS



TRANSCEIVER GROUND CONNECTIONS



TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



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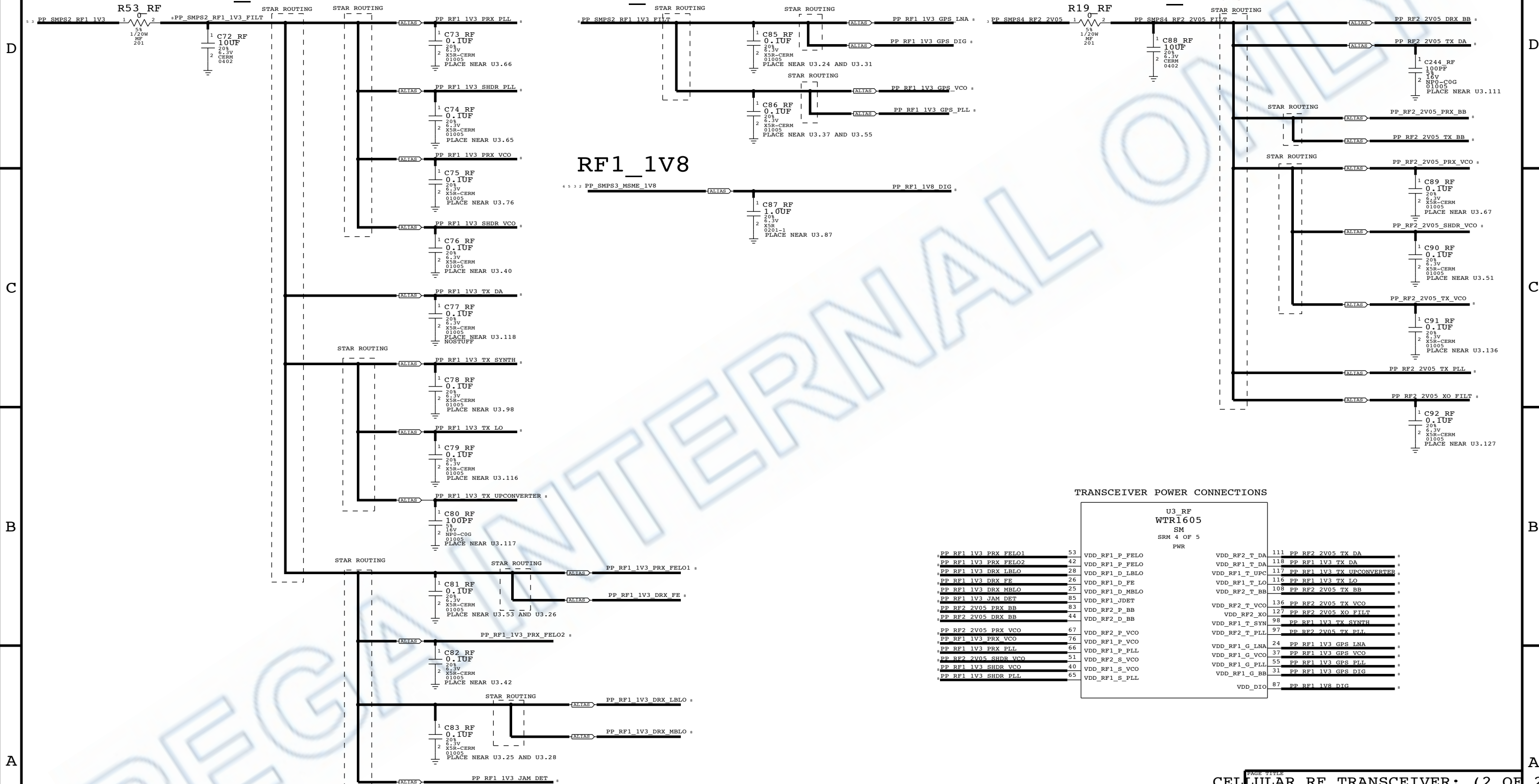
RF TRANSCEIVER (2 OF 2)

RF1_1V3

RF1_1V3

RF2_2V05

RF1_1V8



TRANSCEIVER POWER CONNECTIONS

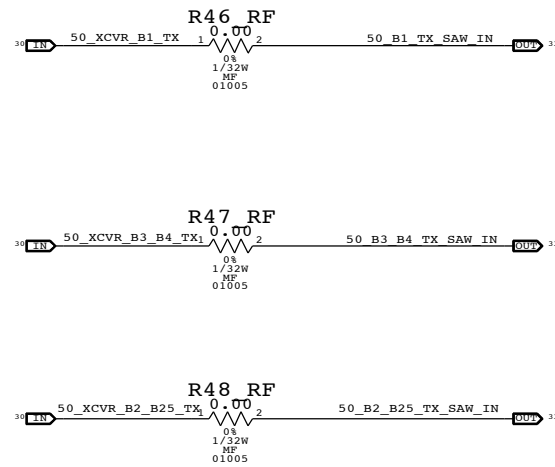
U3_RF		WTR1605		SM		SRM 4 OF 5		PWR	
PP RF1 1V3 PRX FELO1	53	VDD_RF1_P_FELO		VDD_RF2_T_DA	111	PP RF2 2V05 TX DA			
PP RF1 1V3 PRX FELO2	42	VDD_RF1_P_FELO		VDD_RF1_T_DA	118	PP RF1 1V3 TX DA			
PP RF1 1V3 DRX LBLO	28	VDD_RF1_D_LBLO		VDD_RF1_T_UPC	117	PP RF1 1V3 TX UPCONVERTER			
PP RF1 1V3 DRX FE	26	VDD_RF1_D_FE		VDD_RF1_T_LO	116	PP RF1 1V3 TX LO			
PP RF1 1V3 DRX MBLO	25	VDD_RF1_D_MBLO		VDD_RF2_T_BB	108	PP RF2 2V05 TX BB			
PP RF1 1V3 JAM DET	85	VDD_RF1_JDET		VDD_RF2_T_VCO	136	PP RF2 2V05 TX VCO			
PP RF2 2V05 PRX BB	83	VDD_RF2_P_BB		VDD_RF2_XO	127	PP RF2 2V05 XO FILT			
PP RF2 2V05 DRX BB	44	VDD_RF2_D_BB		VDD_RF1_T_SYN	98	PP RF1 1V3 TX SYNTH			
PP RF2 2V05 PRX VCO	67	VDD_RF2_P_VCO		VDD_RF2_T_PLL	97	PP RF2 2V05 TX PLL			
PP RF1 1V3 PRX VCO	76	VDD_RF1_P_VCO		VDD_RF1_G_LNA	24	PP RF1 1V3 GPS LNA			
PP RF1 1V3 PRX PLL	66	VDD_RF1_P_PLL		VDD_RF1_G_VCO	37	PP RF1 1V3 GPS VCO			
PP RF2 2V05 SHDR VCO	51	VDD_RF2_S_VCO		VDD_RF1_G_PLL	55	PP RF1 1V3 GPS PLL			
PP RF1 1V3 SHDR VCO	40	VDD_RF1_S_VCO		VDD_RF1_G_BB	31	PP RF1 1V3 GPS DIG			
PP RF1 1V3 SHDR PLL	55	VDD_RF1_S_PLL		VDD_DIO	87	PP RF1 1V8 DIG			

CELLULAR RF TRANSCEIVER: (2 OF 2)

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TRANSCEIVER TX AND RX MATCHING

TX MATCHING NETWORKS



RX MATCHING NETWORKS

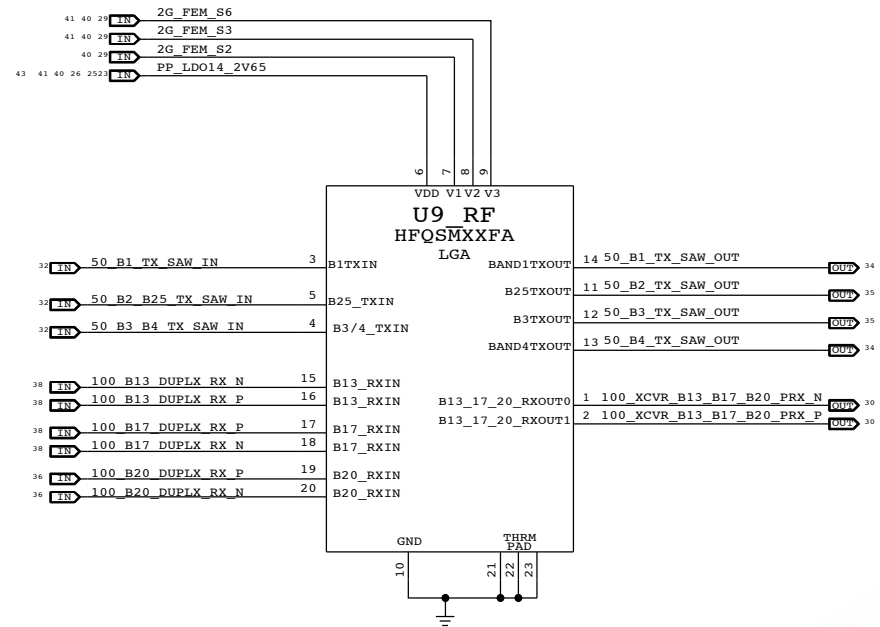


CELLULAR FRONT END: TX AND RX MATCHING

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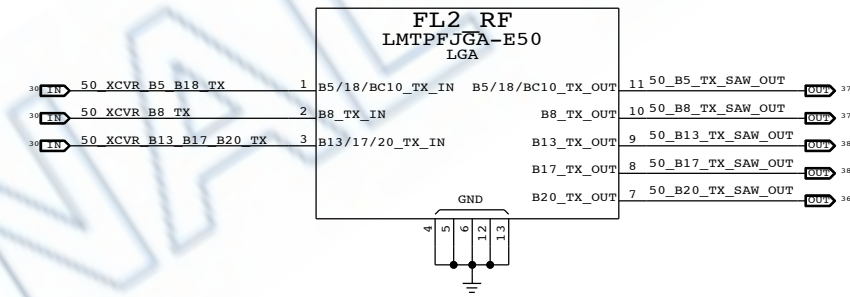
SAW BANKS

HB TX SAW BANK + B13/B17/B20 DP6T SWITCH AND MATCHING

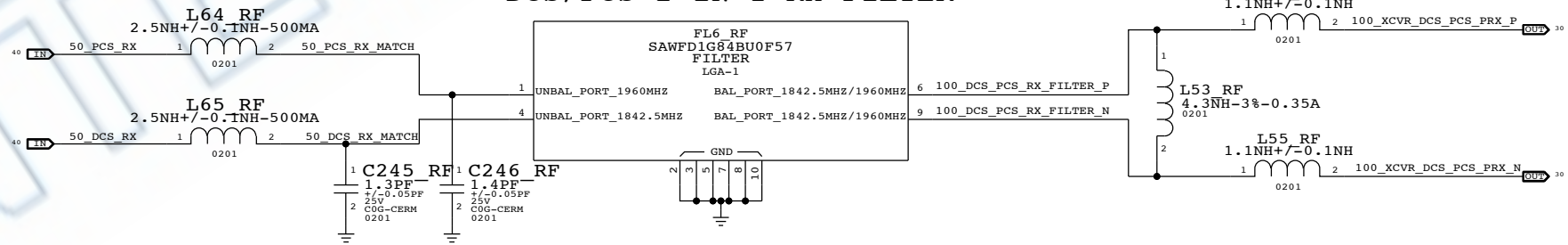


BAND	S6	S3	S2
B3 TX	HIGH	X	X
B4 TX	LOW	X	X
B13 RX	X	HIGH	HIGH
B17 RX	X	HIGH	LOW
B20 RX	X	LOW	HIGH

LB TX SAW BANK



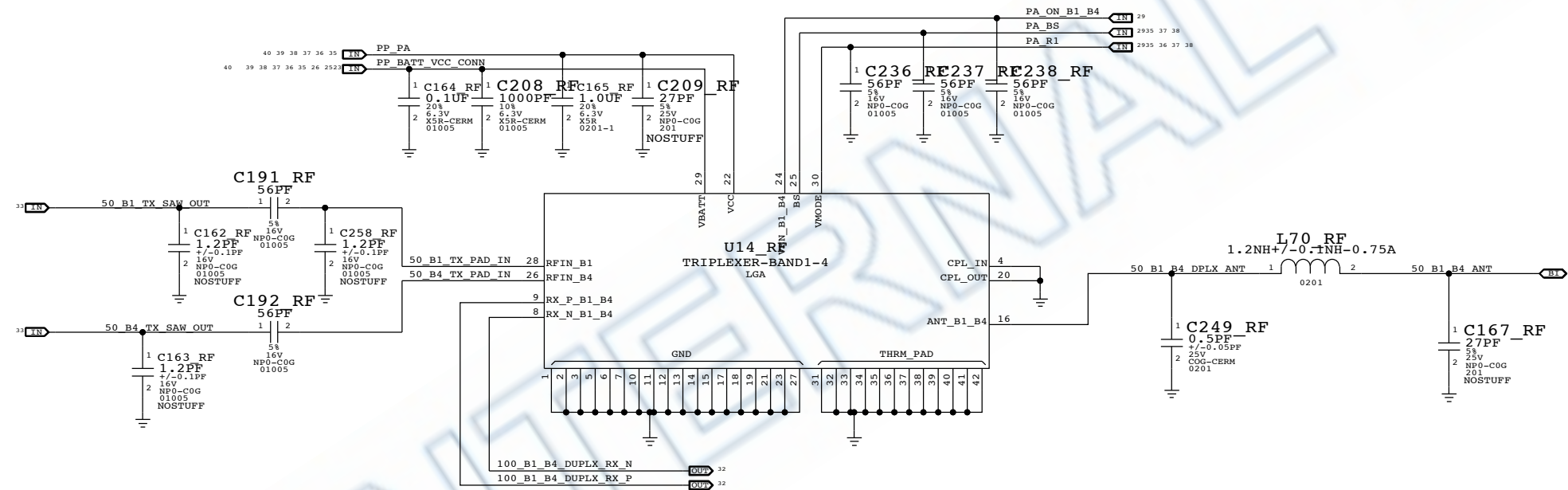
DCS/PCS 2-IN-1 RX FILTER



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BAND 1/4 PAT



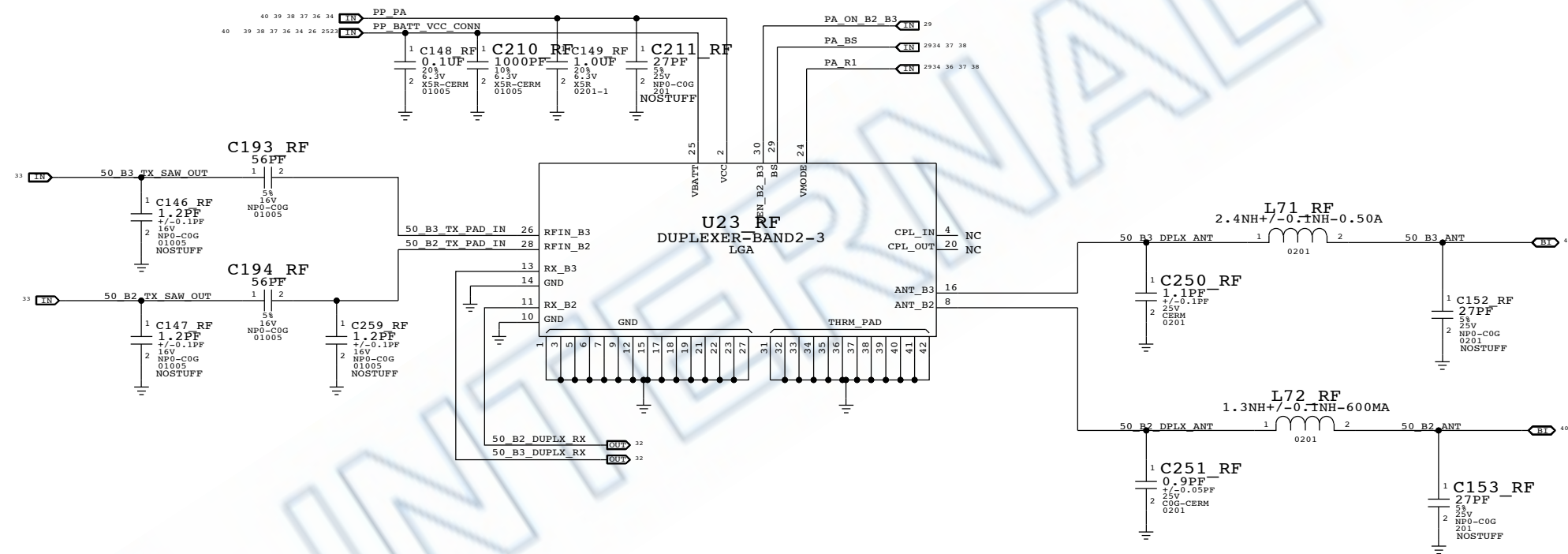
BAND	PA POWER MODE	PA_BS	PA_ON_B1_B4	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B4	HPM	0	1	0
B4	LPM	0	1	1
B1	HPM	1	1	0
B1	LPM	1	1	1

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BAND 2/3 PAD



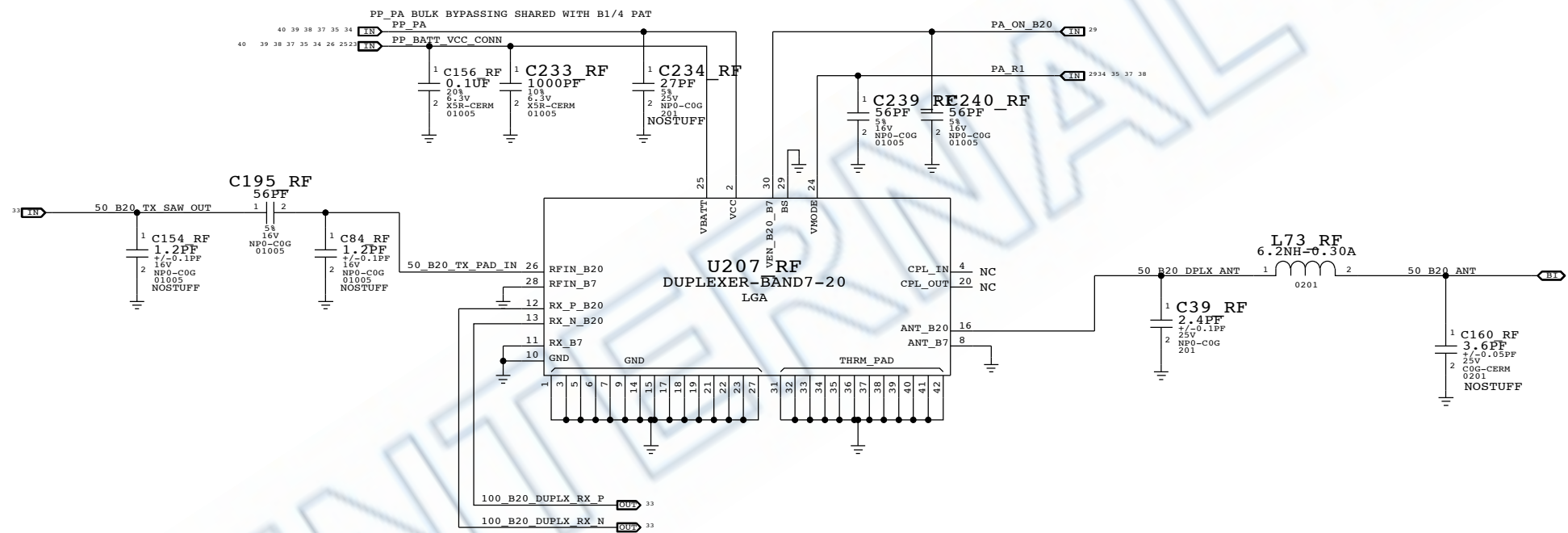
BAND	PA POWER MODE	PA BS	PA_ON B2 B3	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

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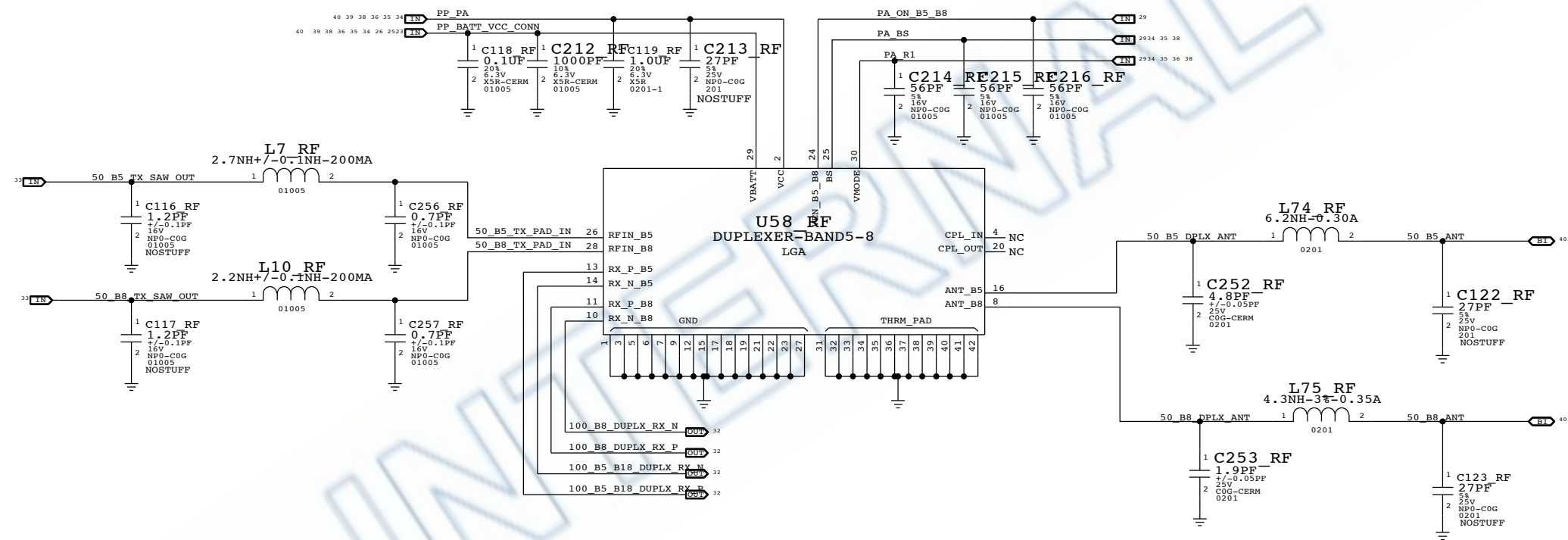
BAND 20 PAD



BAND	PA POWER MODE	PA_ON_B20	PA_R1
POWER DOWN	LPM	0	0
STANDBY	X	0	X
B20	HPM	1	0
B20	LPM	1	1

PAGE TITLE CELLULAR FRONT END: BAND 20 PAD		DRAWING NUMBER 051-9584	SIZE D
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BAND 5/8 PAD

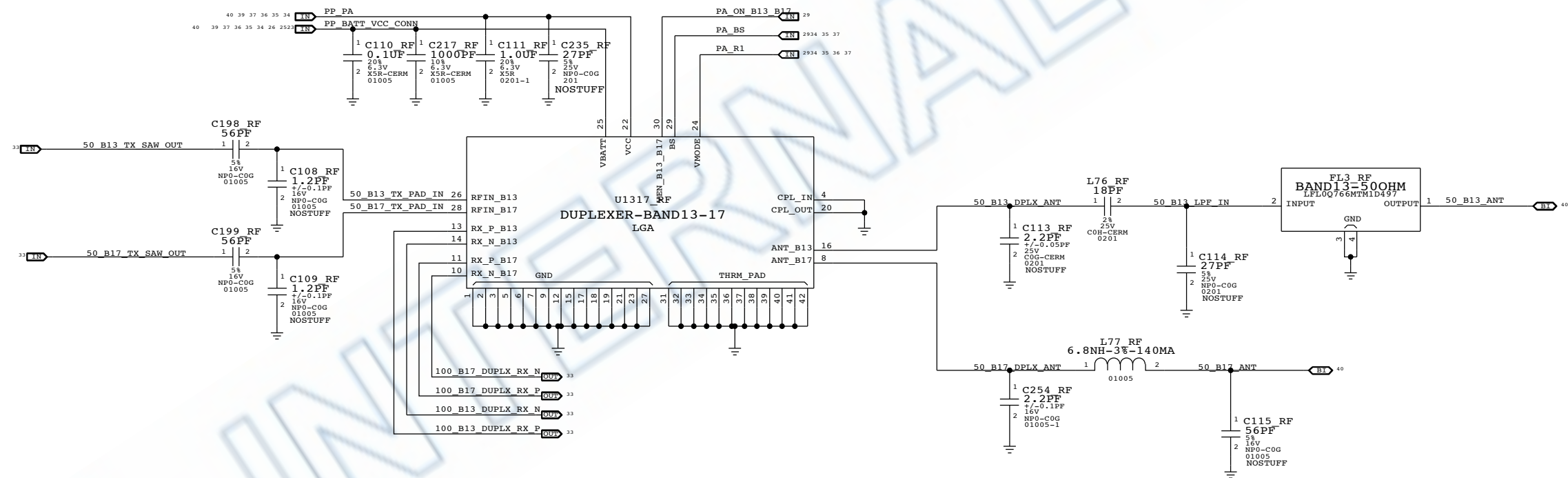


BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

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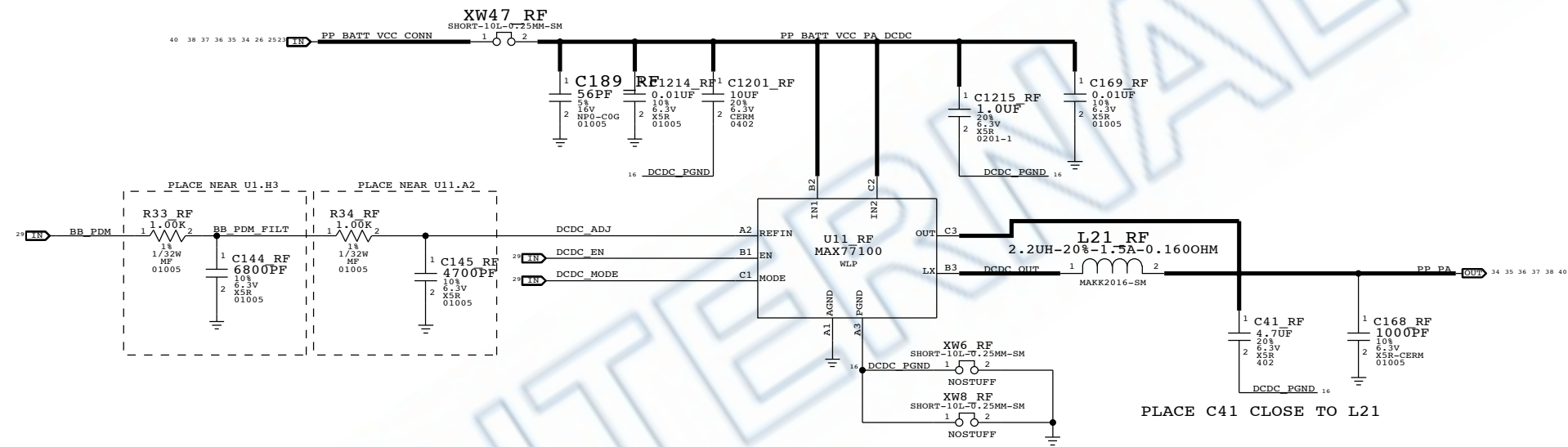
BAND 13/17 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B13_B17	PA_R1
POWER DOWN	X	0	0	0
STANDBY	X	X	0	X
B17	HPM	0	1	0
B17	LPM	0	1	1
B13	HPM	1	1	0
B13	LPM	1	1	1

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PA DC/DC CONVERTER

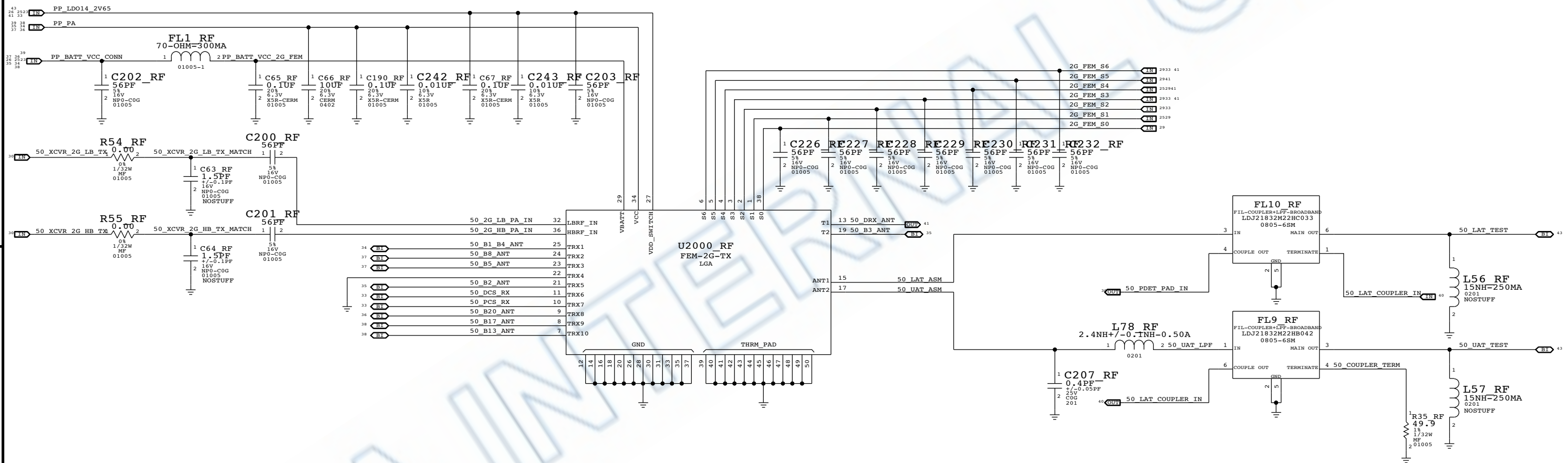


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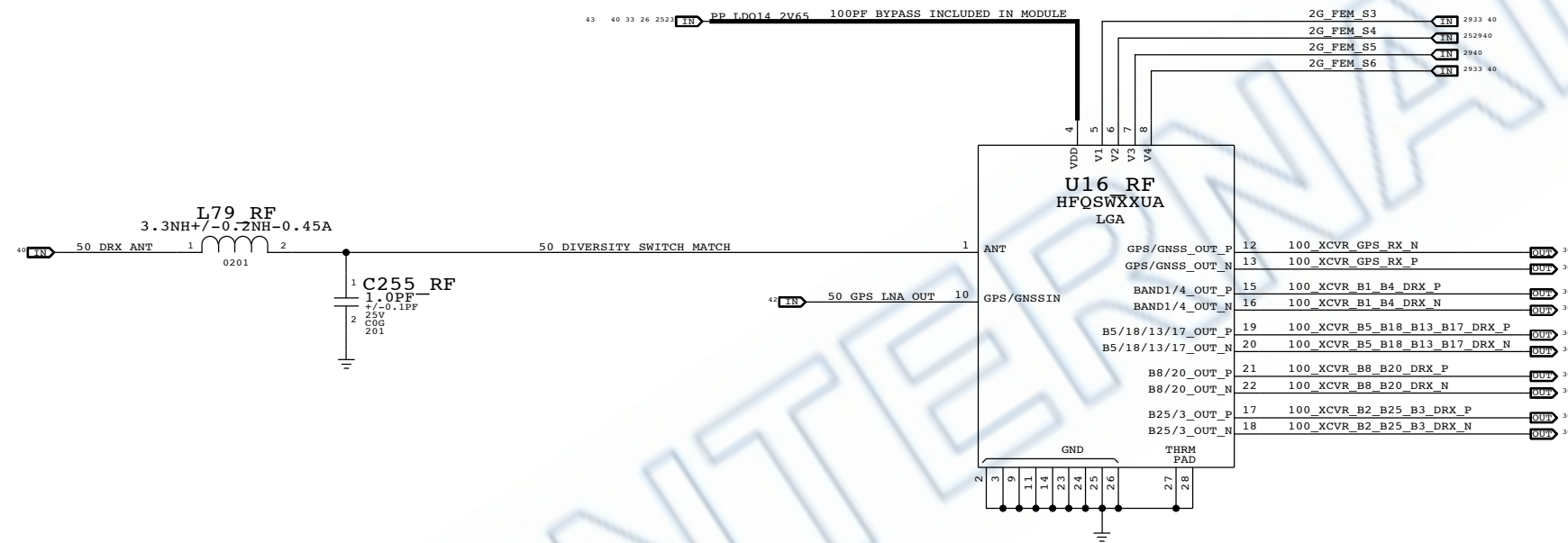
2G FEM



SEE PGS. 21-22 FOR 2G FEM LOGIC TABLE

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RX DIVERSITY



BAND	S6	S5	S4	S3
B1/B4	LOW	LOW	LOW	LOW
B2/25	LOW	HIGH	LOW	LOW
B3	HIGH	LOW	LOW	LOW
B5/6/18	LOW	LOW	HIGH	LOW
B8	LOW	LOW	LOW	HIGH
B13/17	LOW	HIGH	HIGH	HIGH
B20	LOW	HIGH	HIGH	LOW
OFF	LOW	LOW	HIGH	HIGH

SWITCH IS TERMINATED IN ALL OTHER POSSIBLE STATES

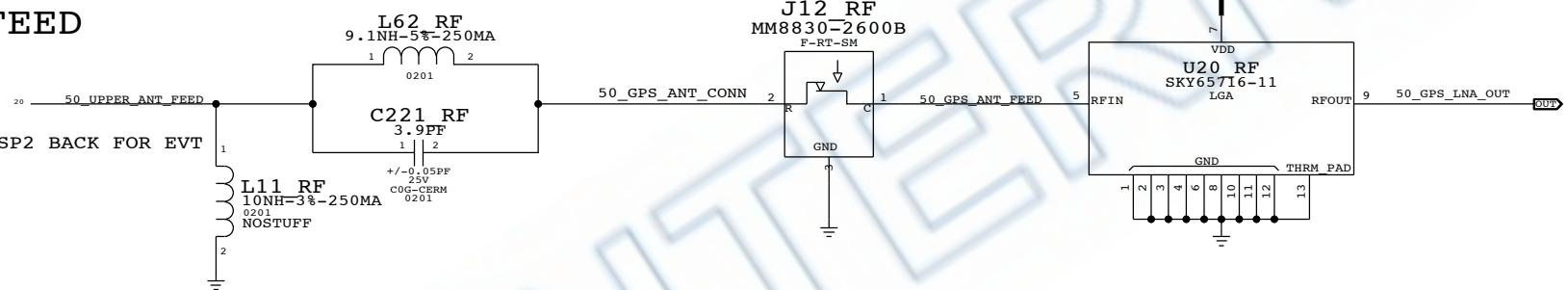
CELLULAR FRONT END: RX DIVERSITY

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GPS

GPS FEED

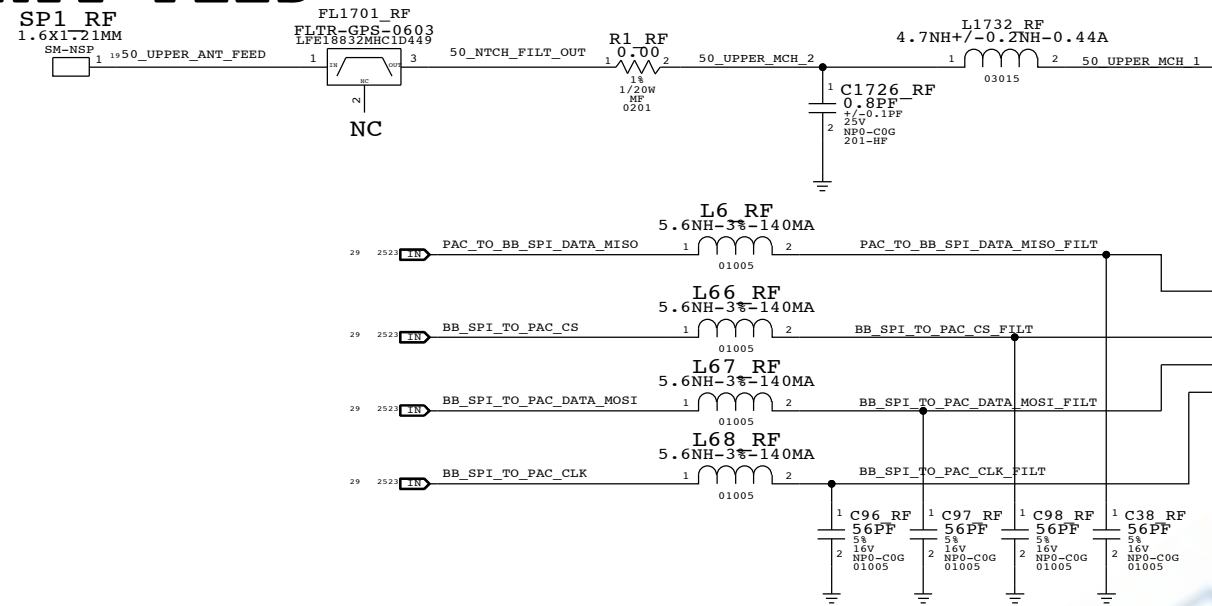
NOTE: ADD SP2 BACK FOR EVT



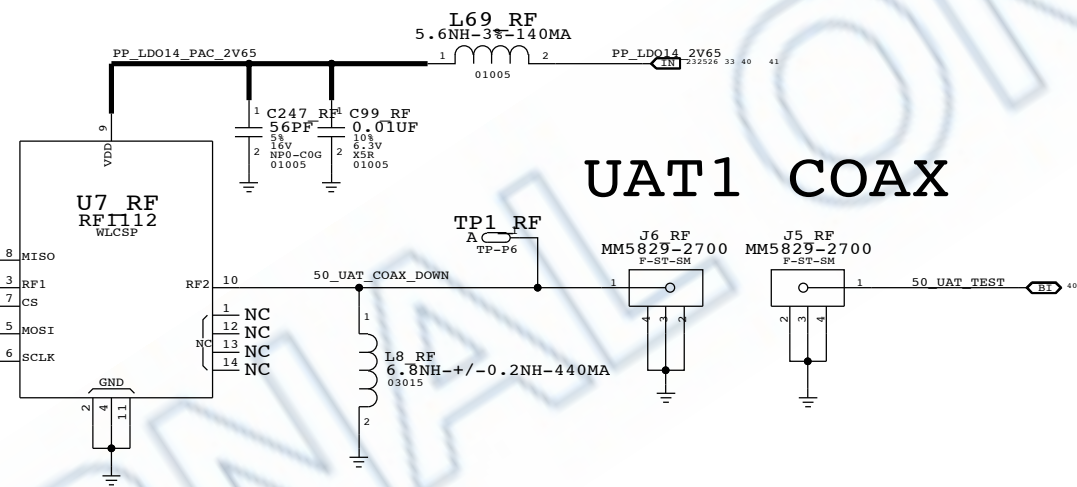
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ANTENNA FEEDS

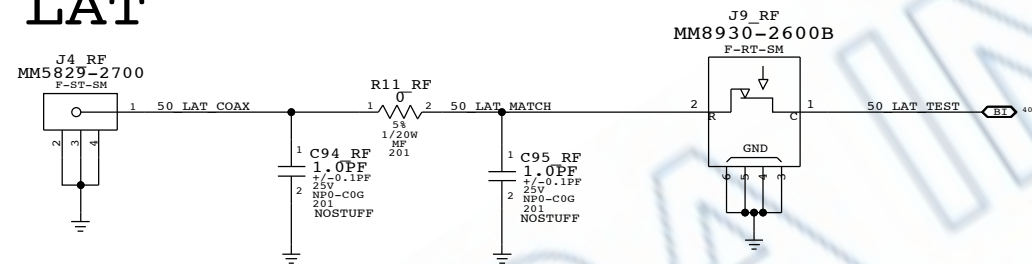
UAT1 FEED



UAT1 COAX



LAT




PAGE TITLE		CELLULAR FRONT END: ANTENNA FEEDS	
DRAWING NUMBER		051-9584	SIZE D
REVISION		2.0.0	BRANCH
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FRONT END LOGIC TABLE (1 OF 2)

BAND	S6	S5	S4	S3	S2	S1	S0	TX/PRX PATH	DRX PATH
LB TX, IDLE, LAT	HIGH	HIGH	HIGH	LOW	LOW	HIGH	HIGH	LAT	UAT
LB TX, IDLE, UAT	HIGH	HIGH	HIGH	LOW	LOW	LOW	HIGH	UAT	LAT
LB TX, LAT, HPM	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LAT	UAT
LB TX, UAT, HPM	HIGH	HIGH	HIGH	LOW	HIGH	LOW	HIGH	UAT	LAT
LB TX, LAT, LPM	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LOW	LAT	UAT
LB TX, UAT, LPM	HIGH	HIGH	HIGH	LOW	HIGH	LOW	LOW	UAT	LAT
LB TX, HIGH Z, LAT, HPM	HIGH	HIGH	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
LB TX, HIGH Z, UAT, HPM	HIGH	HIGH	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
LB TX, HIGH Z, LAT, LPM	HIGH	HIGH	LOW	LOW	HIGH	HIGH	LOW	LAT	UAT
LB TX, HIGH Z, UAT, LPM	HIGH	HIGH	LOW	LOW	HIGH	LOW	LOW	UAT	LAT
HB TX, IDLE, LAT	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LAT	UAT
HB TX, IDLE, UAT	HIGH	HIGH	HIGH	HIGH	LOW	LOW	HIGH	UAT	LAT
HB TX, LAT, HPM	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LAT	UAT
HB TX, UAT, HPM	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	UAT	LAT
HB TX, LAT, LPM	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	LAT	UAT
HB TX, UAT, LPM	HIGH	HIGH	HIGH	HIGH	HIGH	LOW	LOW	UAT	LAT
HB TX, HIGH Z, LAT, HPM	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
HB TX, HIGH Z, UAT, HPM	HIGH	HIGH	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
HB TX, HIGH Z, LAT, LPM	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LOW	LAT	UAT
HB TX, HIGH Z, UAT, LPM	HIGH	HIGH	LOW	HIGH	HIGH	LOW	LOW	UAT	LAT
GSM850 RX, LAT	HIGH	LOW	HIGH	HIGH	LOW	HIGH	HIGH	LAT	UAT
GSM850 RX, UAT	HIGH	LOW	HIGH	HIGH	LOW	LOW	HIGH	UAT	LAT
GSM900 RX, LAT	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	LAT	UAT
GSM900 RX, UAT	HIGH	LOW	HIGH	HIGH	HIGH	LOW	HIGH	UAT	LAT
GSM1900 RX, LAT	LOW	HIGH	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
GSM1900 RX, UAT	LOW	HIGH	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
GSM1800 RX, LAT	HIGH	LOW	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
GSM1800 RX, UAT	HIGH	LOW	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
TERMINATED, UAT	HIGH	LOW	HIGH	LOW	HIGH	HIGH	HIGH	UAT	LAT
TERMINATED, LAT	HIGH	LOW	HIGH	LOW	HIGH	LOW	HIGH	LAT	UAT

LAT = LOWER ANTENNA
 UAT = UPPER ANTENNA

FRONT END LOGIC TABLE (1 OF 2)

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FRONT END LOGIC TABLE - DEV2 (2 OF 2)

BAND	S6	S5	S4	S3	S2	S1	S0	TX/PRX PATH	DRX PATH
B1/BC6, LAT	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B1/BC6, UAT	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B2/B25/BC1, LAT	LOW	HIGH	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B2/B25/BC1, UAT	LOW	HIGH	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B3, LAT	HIGH	LOW	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B3, UAT	HIGH	LOW	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B4/BC15, LAT	LOW	LOW	LOW	LOW	HIGH	HIGH	HIGH	LAT	UAT
B4/BC15, UAT	LOW	LOW	LOW	LOW	HIGH	LOW	HIGH	UAT	LAT
B5/B6/B18/BC0/BC10, LAT	LOW	LOW	HIGH	LOW	HIGH	HIGH	HIGH	LAT	UAT
B5/B6/B18/BC0/BC10, UAT	LOW	LOW	HIGH	LOW	HIGH	LOW	HIGH	UAT	LAT
B8, LAT	LOW	LOW	LOW	HIGH	HIGH	HIGH	HIGH	LAT	UAT
B8, UAT	LOW	LOW	LOW	HIGH	HIGH	LOW	HIGH	UAT	LAT
B13, LAT	LOW	HIGH	HIGH	HIGH	HIGH	HIGH	HIGH	LAT	UAT
B13, UAT	LOW	HIGH	HIGH	HIGH	HIGH	LOW	HIGH	UAT	LAT
B17, LAT	LOW	HIGH	HIGH	HIGH	LOW	HIGH	HIGH	LAT	UAT
B17, UAT	LOW	HIGH	HIGH	HIGH	LOW	LOW	HIGH	UAT	LAT
B20, LAT	LOW	HIGH	HIGH	LOW	HIGH	HIGH	HIGH	LAT	UAT
B20, UAT	LOW	HIGH	HIGH	LOW	HIGH	LOW	HIGH	UAT	LAT
OFF	LOW	LOW	HIGH	HIGH	X	X	X	X	X
STANDBY	LOW	LOW	LOW	LOW	LOW	LOW	LOW	X	X


LAT = LOWER ANTENNA

UAT = UPPER ANTENNA

OFF = LOWEST POWER STATE WITHOUT REMOVING LDO14_2V65 POWER

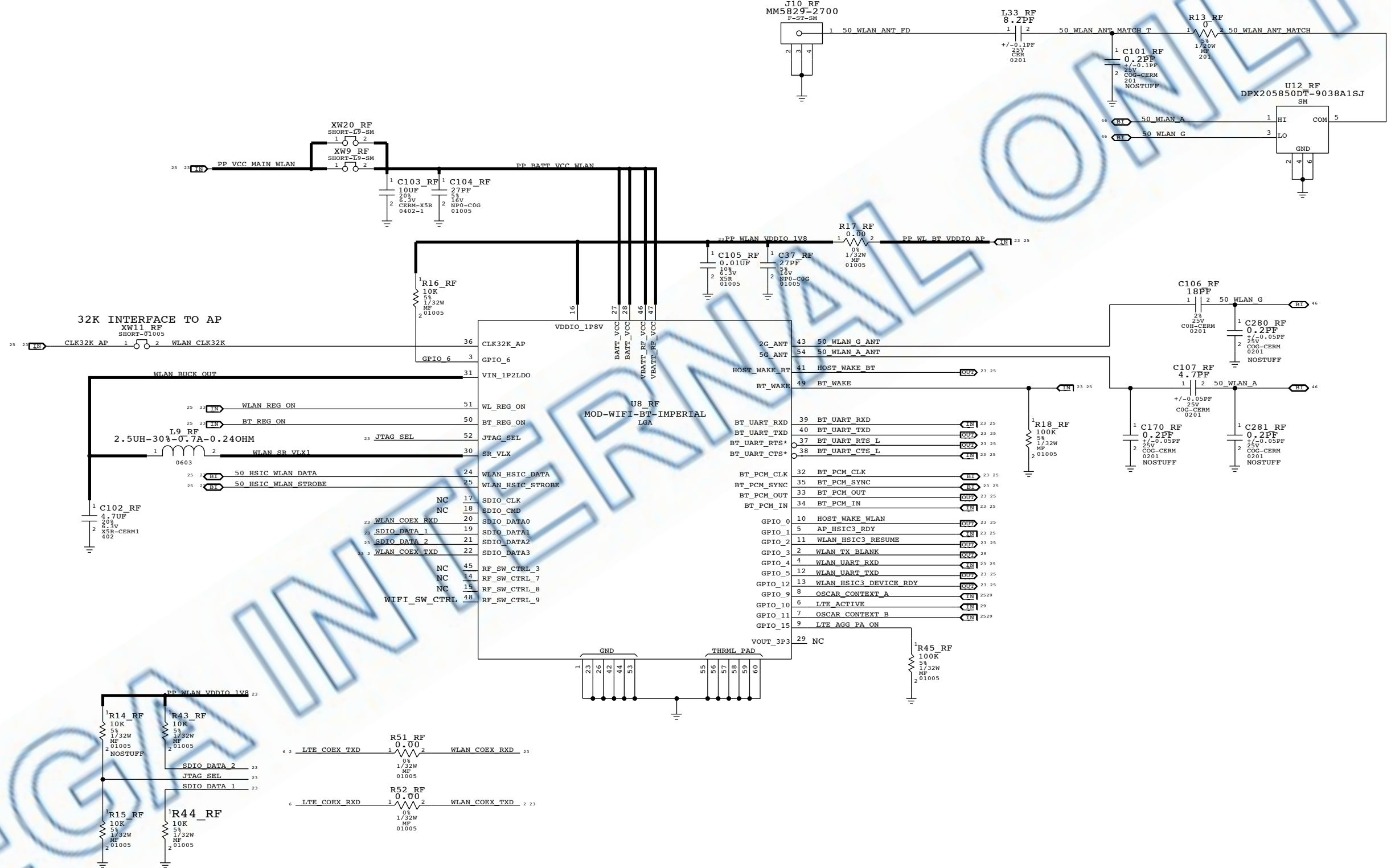
STANDBY = ADDED TO SUPPORT EXISTING SW ARCHITECTURE. NOT TO BE USED AS A LOW POWER STATE.

FRONT END LOGIC TABLE (2 OF 2)

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WLAN/BT

UAT2



PULL-UP ON GPIO6, SDIO_DATA_2 & PULL-DOWN ON SDIO_DATA_1 REQUIRED FOR HSIC BOOTSTRAPPING

PAGE TITLE		DRAWING NUMBER		SIZE
WIFI/BT: MODULE AND FRONT END		051-9584		D
Apple Inc.		REVISION		2.0.0
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