

TOP SIDE ASSEMBLY

APPLE				TITLE PCBF , X200 MLB (C1)	
THIS IS THE PROPERTY OF APPLE AND IT MUST BE RETURNED					
ORIG DIV	DESIGNER HURLEY	DATE 01/08/13	SCALE 1:1	DRAWING NUMBER 820-4124-A	
<p>NOTES: ARTWORK VIEWED FROM COMPONENT SIDE. PCB SHALL CONFORM TO STANDARDS AS DEFINED IN APPLE SPECIFICATION 062-0031 (DOUBLE-SIDED BOARDS) OR 062-0073 (MULTI-LAYER BOARDS) AS APPLICABLE.</p>				<p>NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE THE POSSESSOR AGREES TO THE FOLLOWING (I) TO MAINTAIN THIS DOCUMENT IN CONFIDENCE (II) NOT TO REPRODUCE OR COPY IT (III) NOT TO REVEAL OR PUBLISH IT</p>	

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

X200 | MLB-C1

LAST_MODIFIED= Tue Oct 29 15:52:27 2013

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
A	0002535199	PRODUCTION RELEASED		2014-01-13

SCH AND BOARD PART NUMBERS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-0886	1	SCH_MLB-C1_X200	SCH1	
820-4124	1	PCBF_MLB-C1_X200	PCB1	

PDF CSA CONTENTS

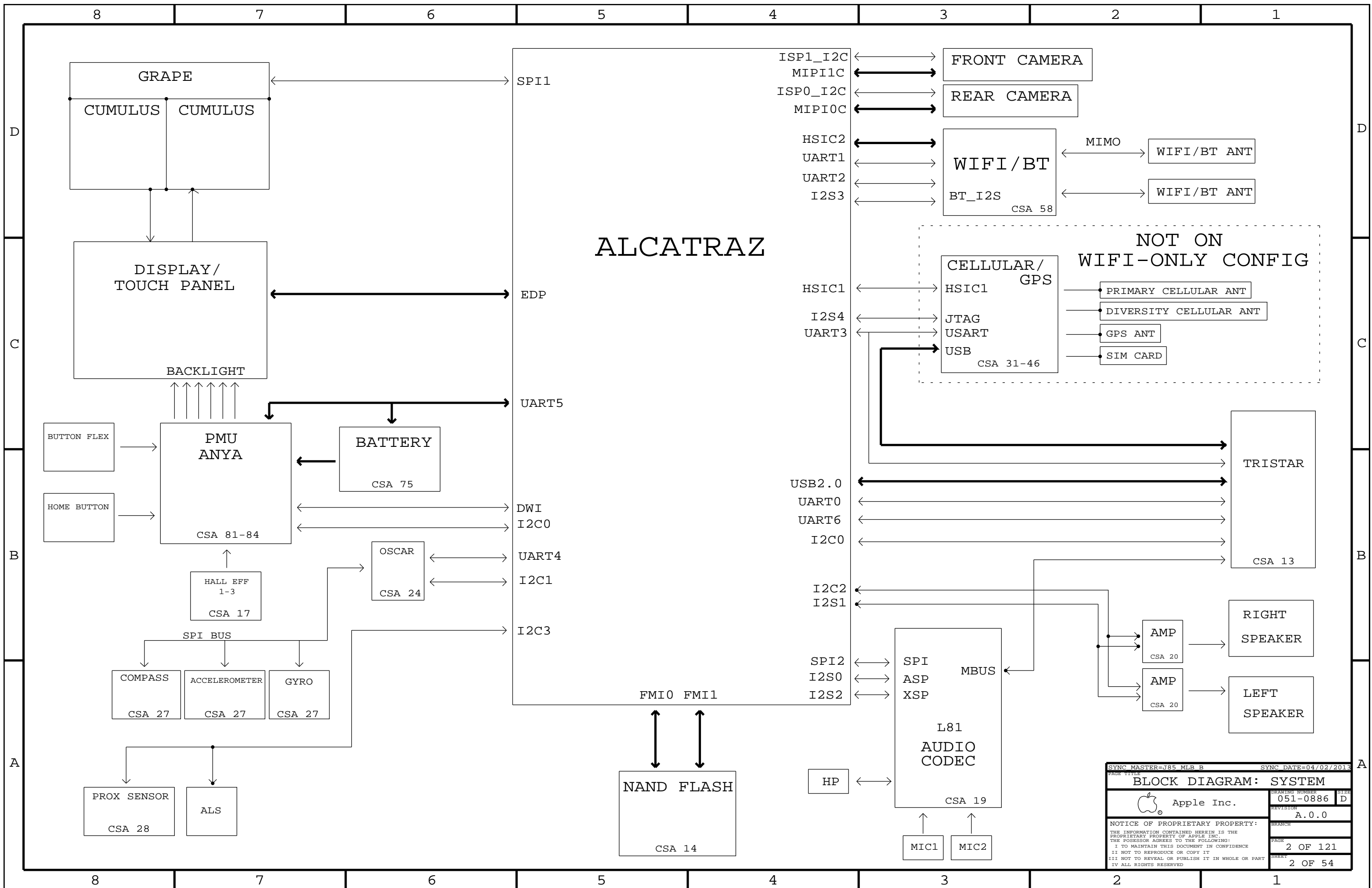
PDF	CSA	CONTENTS	SYNC MASTER	DATE
21	27	SENSOR: ACCEL, COMPASS, GYRO	N/A	N/A
22	28	SENSOR: PROX	J85_MLB_I2	05/12
23	29	CAMERA: REAR CONN & FILTERS	N/A	N/A
24	30	CELL: AP INTERFACE & DEBUG CONNECTORS	RADIO_MLB_I2	08/29/2013
25	32	CELL: BASEBAND PMU (1 OF 2)	RADIO_MLB_I2	08/29/2013
26	33	CELL: BASEBAND PMU (2 OF 2)	RADIO_MLB_I2	08/29/2013
27	34	CELL: BASEBAND (1 OF 2)	RADIO_MLB_I2	08/29/2013
28	35	CELL: BASEBAND (2 OF 2)	RADIO_MLB_I2	08/29/2013
29	36	CELL: RF TRANSCEIVER (1 OF 2)	RADIO_MLB_I2	08/29/2013
30	37	CELL: RF TRANSCEIVER (2 OF 2)	RADIO_MLB_I2	08/29/2013
31	38	CELL: RX MATCHING	RADIO_MLB_I2	08/29/2013
32	39	CELL: RF TRANSCEIVER (3 OF 4)	RADIO_MLB_I2	08/29/2013
33	40	CELL: PENTABAND PA	RADIO_MLB_I2	08/29/2013
34	41	CELL: BAND 2/3 PAD	RADIO_MLB_I2	08/29/2013
35	42	CELL: BAND 7/20 PAD	RADIO_MLB_I2	08/29/2013
36	43	CELL: BAND 5/8 PAD	RADIO_MLB_I2	08/29/2013
37	44	CELL: 2G PA	RADIO_MLB_I2	08/29/2013
38	45	CELL: PA DCDC CONVERTER	RADIO_MLB_I2	08/29/2013
39	46	CELL: ASM AND HB LTE FRONT-END	RADIO_MLB_I2	08/29/2013
40	47	CELL: RX DIVERSITY	RADIO_MLB_I2	08/29/2013
41	48	CELL: GPS	RADIO_MLB_I2	08/29/2013
42	49	CELL: ANTENNA FEEDS	RADIO_MLB_I2	08/29/2013
43	57	IO: FILTERS & HOTBAR CONN	N/A	04/18/2011
44	58	WIFI/BT: MODULE	WIFI_DEV05	20/2013
45	75	POWER: BATTERY CONNECTOR	N/A	N/A
46	81	PMU: ANYA PAGE 1	J72_MLB_I1	26/2012
47	82	PMU: ANYA PAGE 2	J85_MLB_I2	03/2012
48	83	PMU: ANYA PAGE 3	J72_MLB_I1	26/2012
49	84	PMU: ANYA PAGE 4	J72_MLB_I1	26/2012
50	85	POWER: PPIV8_SW	J85_MLB_I2	03/2012
51	90	SEP: EEPROM & SOC DEBUG	J72_MLB_I1	26/2012
52	93	TEST: TP/HOLES/FIDUCIALS	J85_MLB_I2	03/12
53	94	TEST: EE TP/PP	J72_MLB_I1	26/2012
54	121	POWER: ALIASES	J72_MLB_I1	26/2012

PDF CSA CONTENTS

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
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3	4	BOM TABLES	J72_MLB_I1	26/2012
4	6	SOC: MAIN	N/A	04/18/2011
5	7	SOC: I/OS	N/A	05/05/2011
6	8	SOC: NAND	N/A	04/18/2011
7	9	SOC: DP, MIPI	MLB	05/04/2012
8	10	SOC: SRAM, IO PWRS	N/A	04/18/2011
9	11	SOC: VDD, SRAM, CPU, GPU PWRS	N/A	04/18/2011
10	12	SOC: MISC & ALIASES	N/A	04/11/2011
11	13	IO: TRISTAR	N/A	N/A
12	14	NAND STORAGE	MLB	05/04/2012
13	17	TOUCH: SUPPORT CKT & CONN	N/A	06/21/2010
14	18	AUDIO: HP FLEX CONN	N/A	03/31/2011
15	19	AUDIO: L81 CODEC	KAVITHA	01/18/2012
16	20	AUDIO: CS35L19A AMPS	KAVITHA	01/18/2012
17	21	BUTTON: CONN	N/A	N/A
18	22	VIDEO: EDP SUPPORT & CONN	J85_MLB_I2	05/2012
19	24	SENSOR: OSCAR	J72_MLB_I1	26/2012
20	26	CAMERA: FF-ALS CONN & FILTERS	J85_MLB_I2	03/2012

DRAWING TITLE		SCH, MLB-C1, X200	
DRAWING NUMBER	051-0886	SIZE	D
	REVISION		A.0.0
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DRAWING



SYNC MASTER=J85 MLB B		SYNC DATE=04/02/2013	
BLOCK DIAGRAM: SYSTEM			
Apple Inc.		DRAWING NUMBER	051-0886
		REVISION	A.0.0
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE
16GB_PROD
32GB_PROD
64GB_PROD
128GB_PROD
DEVELOPMENT_JTAG_TAP
JTAG_DAP
MLB (WDOG TO PMU)

WIFI BOM OPTIONS

ANDGATE_TI
FERRITE_TY
FERRITE_IDK

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0207	1	H6P + 1GB ELPIDA	U0652	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0208	339S0207		U0652	HYNIX DDR

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0656	1	IC,PMU,ANYA,D2089A1,OTFXX,FCCSP342	U8100	CRITICAL	

FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0921	1	TOS,19NM,PPN1.5,C,DDP,16GB	U1400	16GB
335S0922	1	TOS,19NM,PPN1.5,C,ODP,32GB	U1400	32GB
335S0923	1	TOS,19NM,PPN1.5,C,ODP,64GB	U1400	64GB
335S0929	1	TOS,19NM,PPN1.5,C,12DP,64GB	U1400	96GB
335S0924	1	TOS,19NM,PPN1.5,C,16DP,128GB	U1400	128GB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0930	335S0921	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0931	335S0922	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0932	335S0923	64GB	U1400	HYNIX 20NM PPN1.5 64GB

U2200

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S4272	1	IC,SIGMA1423V,PMU SW,SEESFF3,AA,TDFH	U2200	

NOTE: FOLLOWING J72, U2200 USES 353S3672 FOOTPRINT (353S4272 HAS SMALLER PADS DUE TO NEW DFM RULES)

4.3UF CAP

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0702	138S0657		C1009,C1015...	RDAR #13988471

WIFI

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
339S0223	339S0213		U5800	

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-6207	1	FENCE,TALL,MLB,X221	FD_FENCE_MLB	CRITICAL	
806-7613	1	FENCE,RADIO,MLB,C BRD,X221	FD_CAN_RADIO	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-5393 (X200C1 GOOD)	FNJD	CRITICAL	EEEE_X200C_GOOD
825-7639	1	EEEE FOR 639-5394 (X200C1 BETTER)	FNJ5	CRITICAL	EEEE_X200C_BETTER
825-7639	1	EEEE FOR 639-5385 (X200C1 BEST)	FNJ9	CRITICAL	EEEE_X200C_BEST
825-7639	1	EEEE FOR 639-5386 (X200C1 BEST+)	FNJH	CRITICAL	EEEE_X200C_BEST+
825-7639	1	EEEE FOR 639-5387 (X200C1 ULTIMATE)	FNJ6	CRITICAL	EEEE_X200C_ULTIMATE
825-7639	1	EEEE FOR 639-5388 (X200C1 GOOD IVS)	FNJ8	CRITICAL	EEEE_X200C_GOOD_IVS
825-7639	1	EEEE FOR 639-5389 (X200C1 BETTER IVS)	FNJF	CRITICAL	EEEE_X200C_BETTER_IVS
825-7639	1	EEEE FOR 639-5390 (X200C1 BEST IVS)	FNJC	CRITICAL	EEEE_X200C_BEST_IVS
825-7639	1	EEEE FOR 639-5391 (X200C1 BEST+ IVS)	FNJ7	CRITICAL	EEEE_X200C_BEST+_IVS
825-7639	1	EEEE FOR 639-5392 (X200C1 ULTIMATE IVS)	FNJG	CRITICAL	EEEE_X200C_ULTIMATE_IVS

GYRO

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S1192	1	GYRO, ST MICRO	U2720	CRITICAL	GYRO_STMICRO
338S1218	1	GYRO, INVENSENSE	U2720	CRITICAL	GYRO_INVENSENSE
132S0391	1	CAP 0.01UF 25V 0201	C2726	CRITICAL	GYRO_STMICRO
132S0288	1	CAP 0.1UF 16V 0201	C2726	CRITICAL	GYRO_INVENSENSE

338S1158 OLD GYRO - ST MICRO
 OLDER INVENSENSE P/N 338S1135
 OLD INVENSENSE P/N 338S1200 (3/22/13)

ACCEL

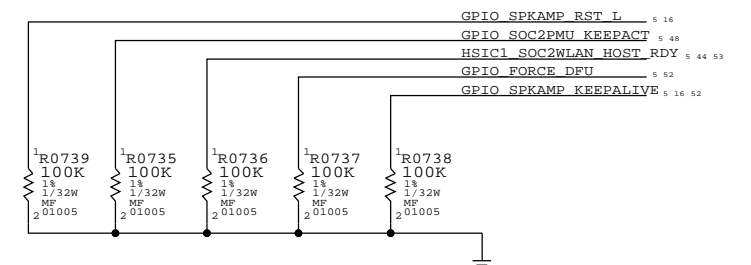
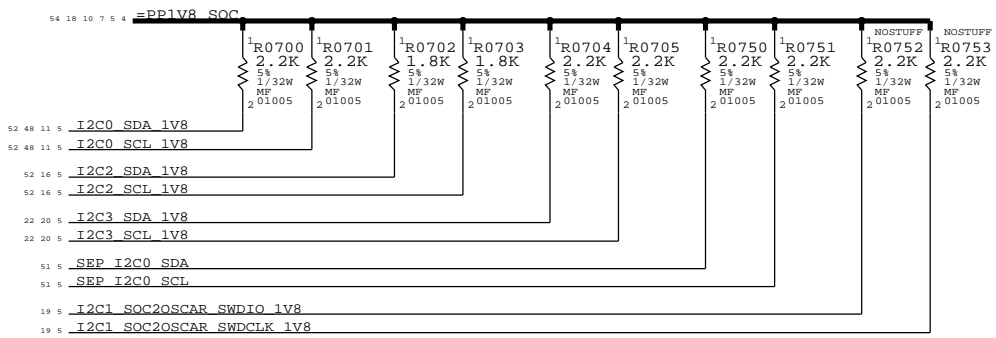
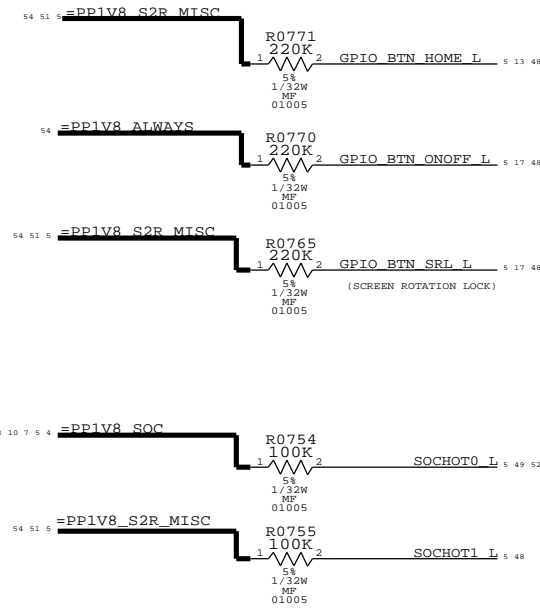
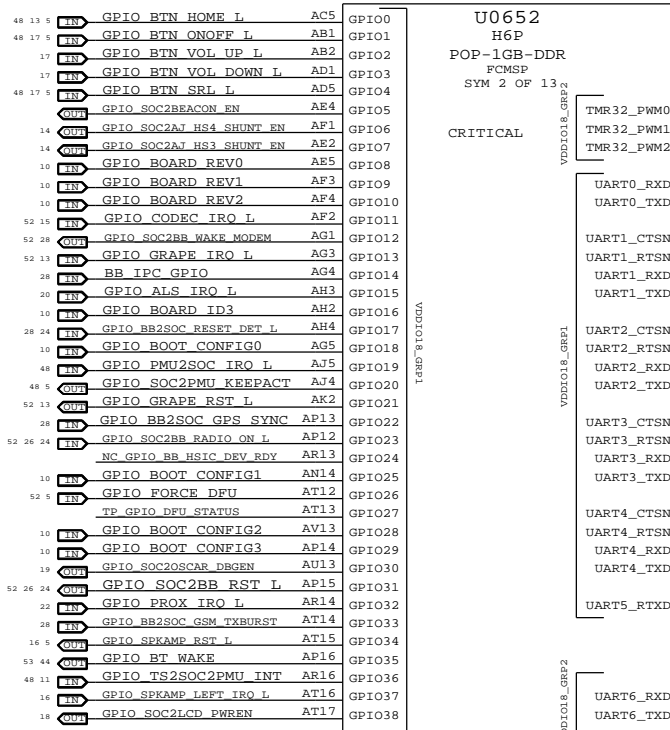
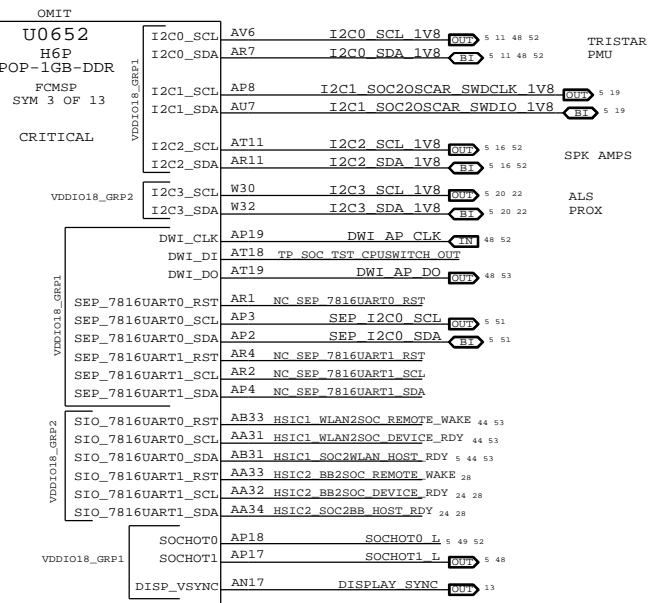
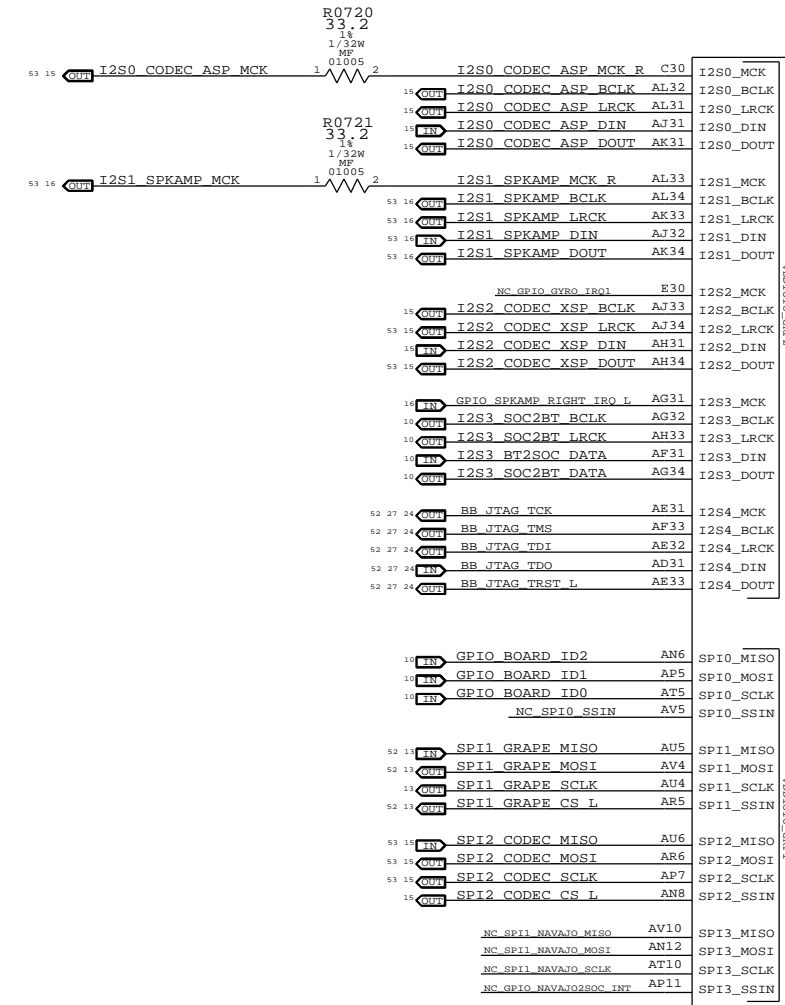
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338S1163	1	IC,ACCEL,3-AXIS,DIG,BMA282,LGA14	U2700	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:

338S1233 ST MICRO - DISQUAL'ED
 338S1114 OLD ACCEL - ST MICRO
 338S1191 OLD ACCEL - ST MICRO

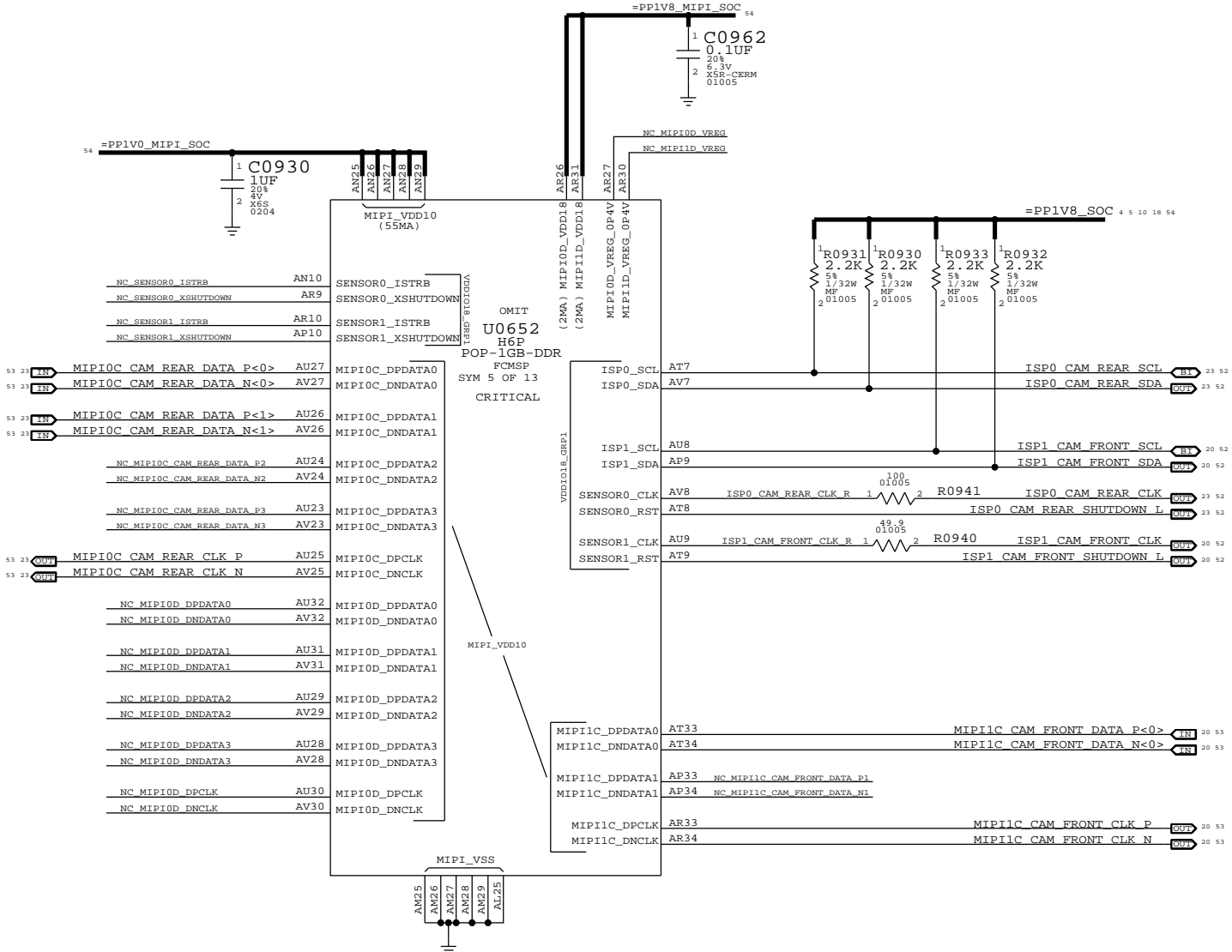
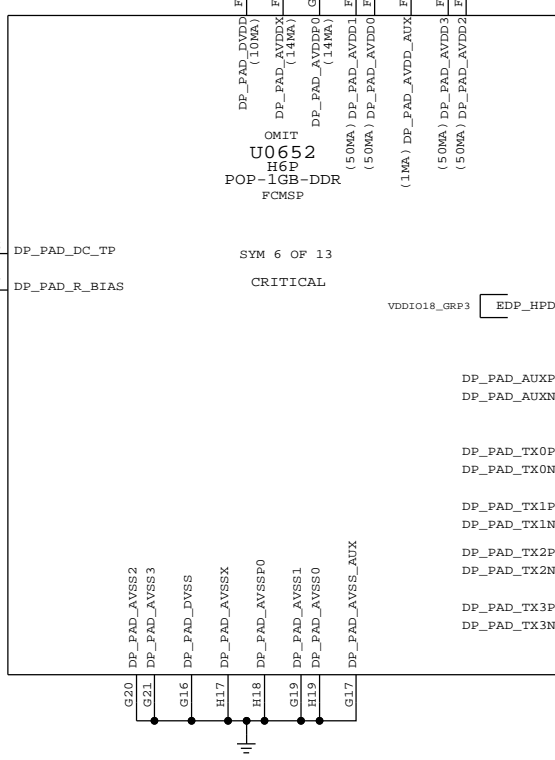
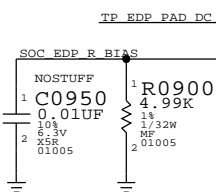
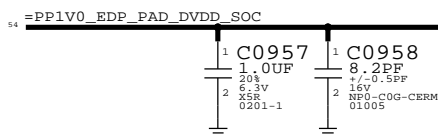
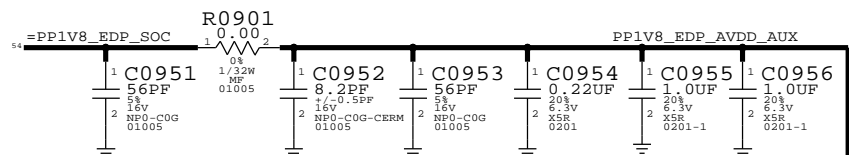
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SOC I/OS

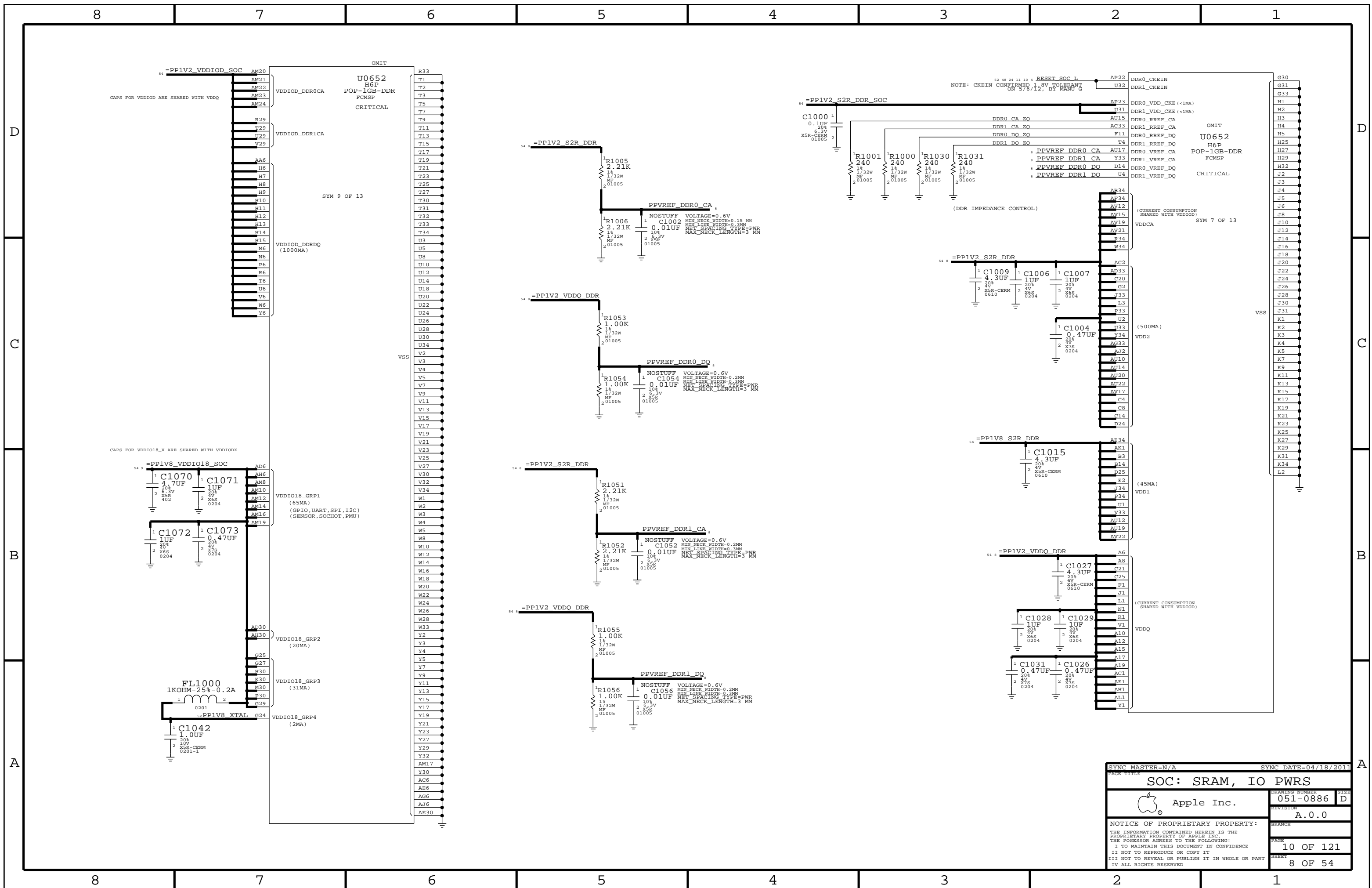


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DISPLAYPORT



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SOC: DP, MIPI			
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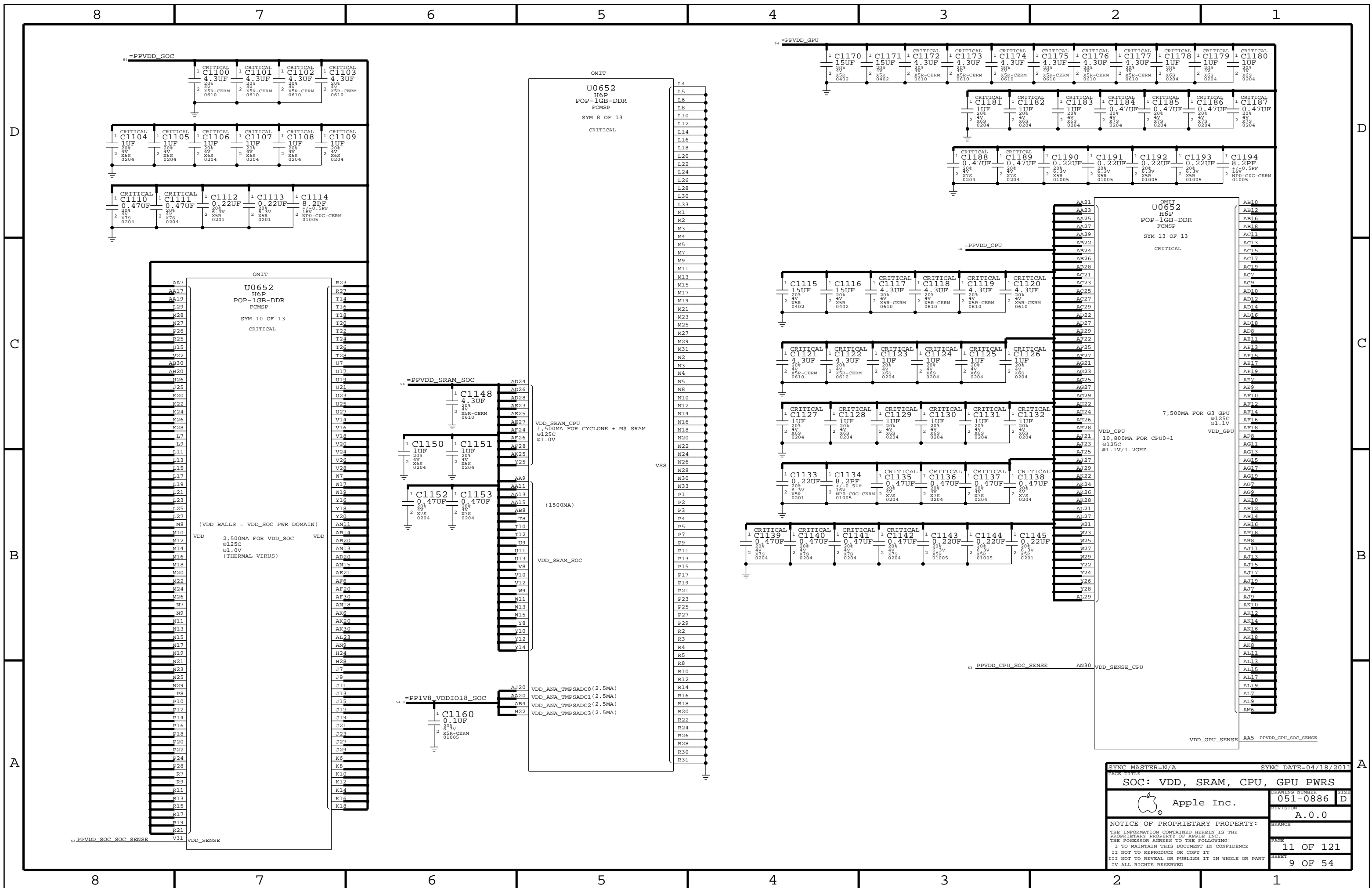
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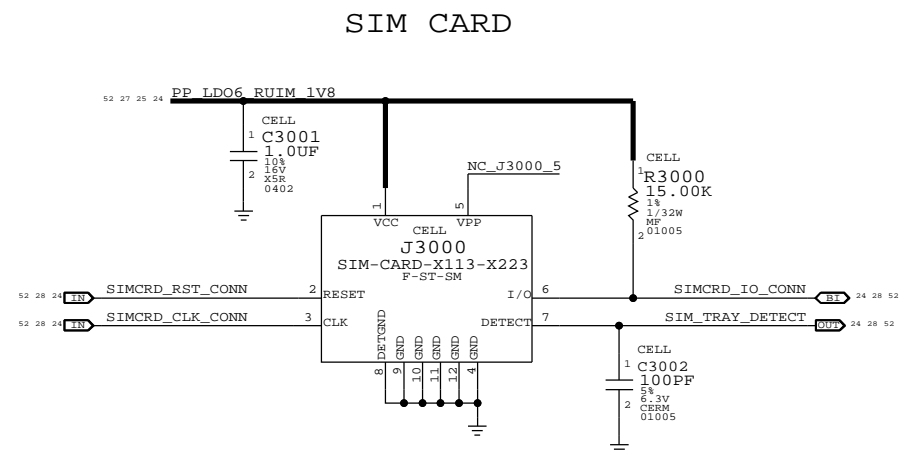
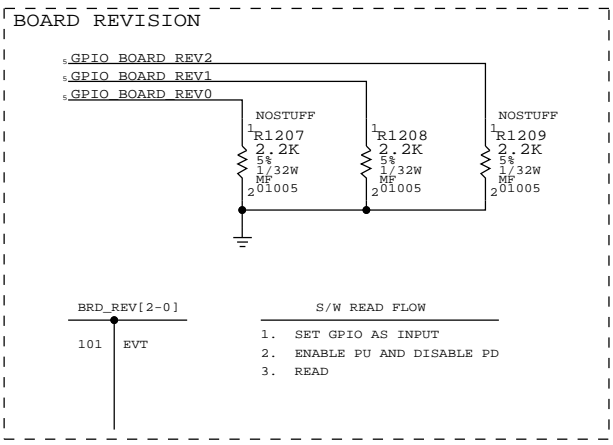
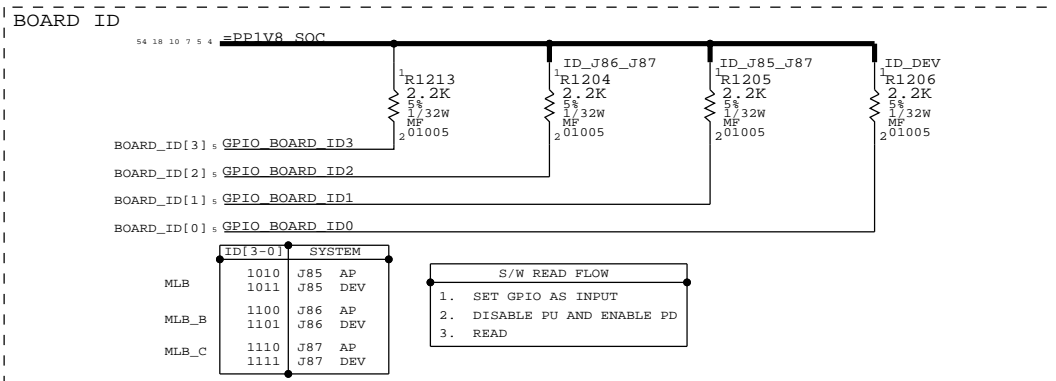
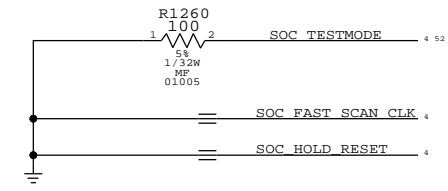
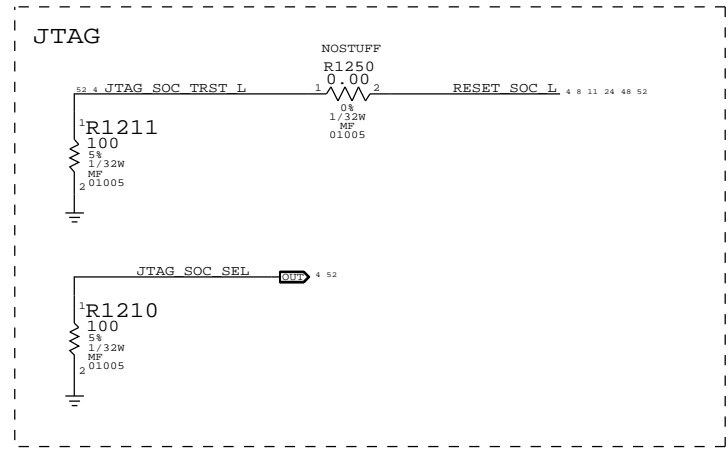
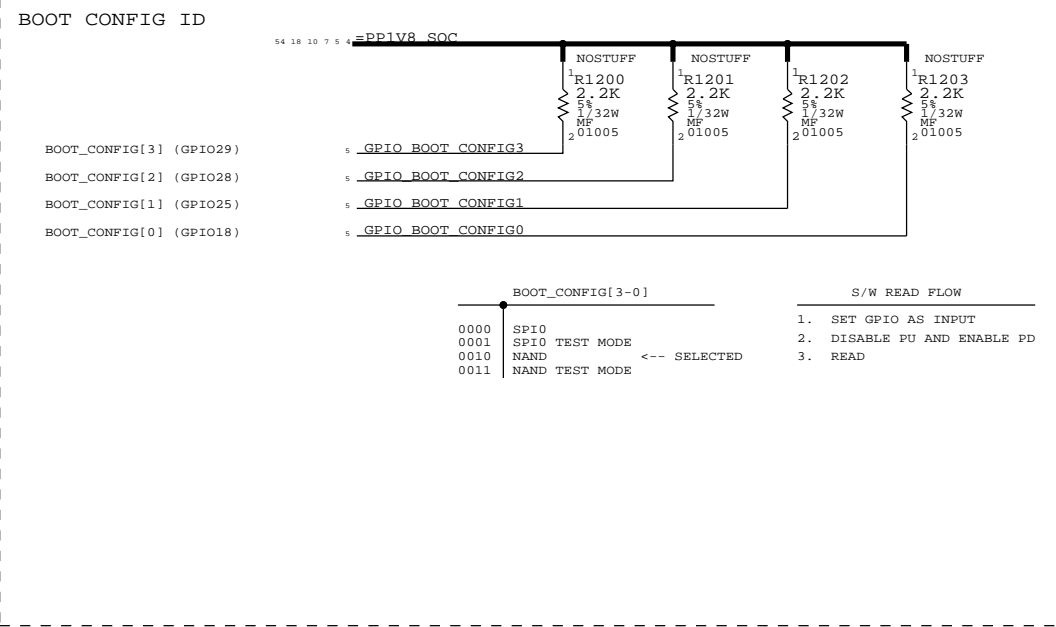
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CKPLUS RULE EXCEPTIONS	REQUIRED
SCHEMATIC DEFINED CONSTRAINTS (YES/NO)	NO

SYNC MASTER=N/A SYNC DATE=04/11/2011

SOC: MISC & ALIASES

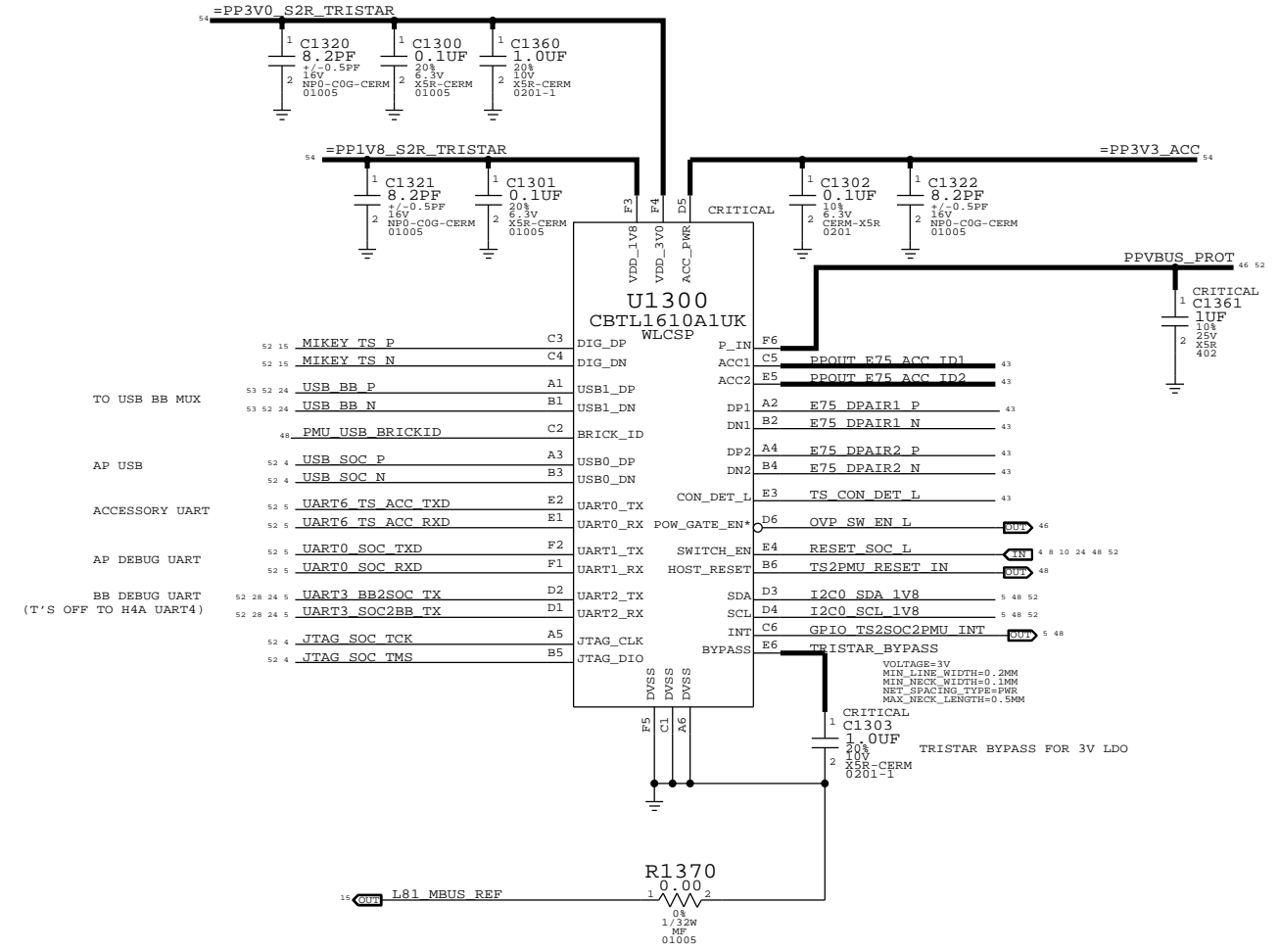
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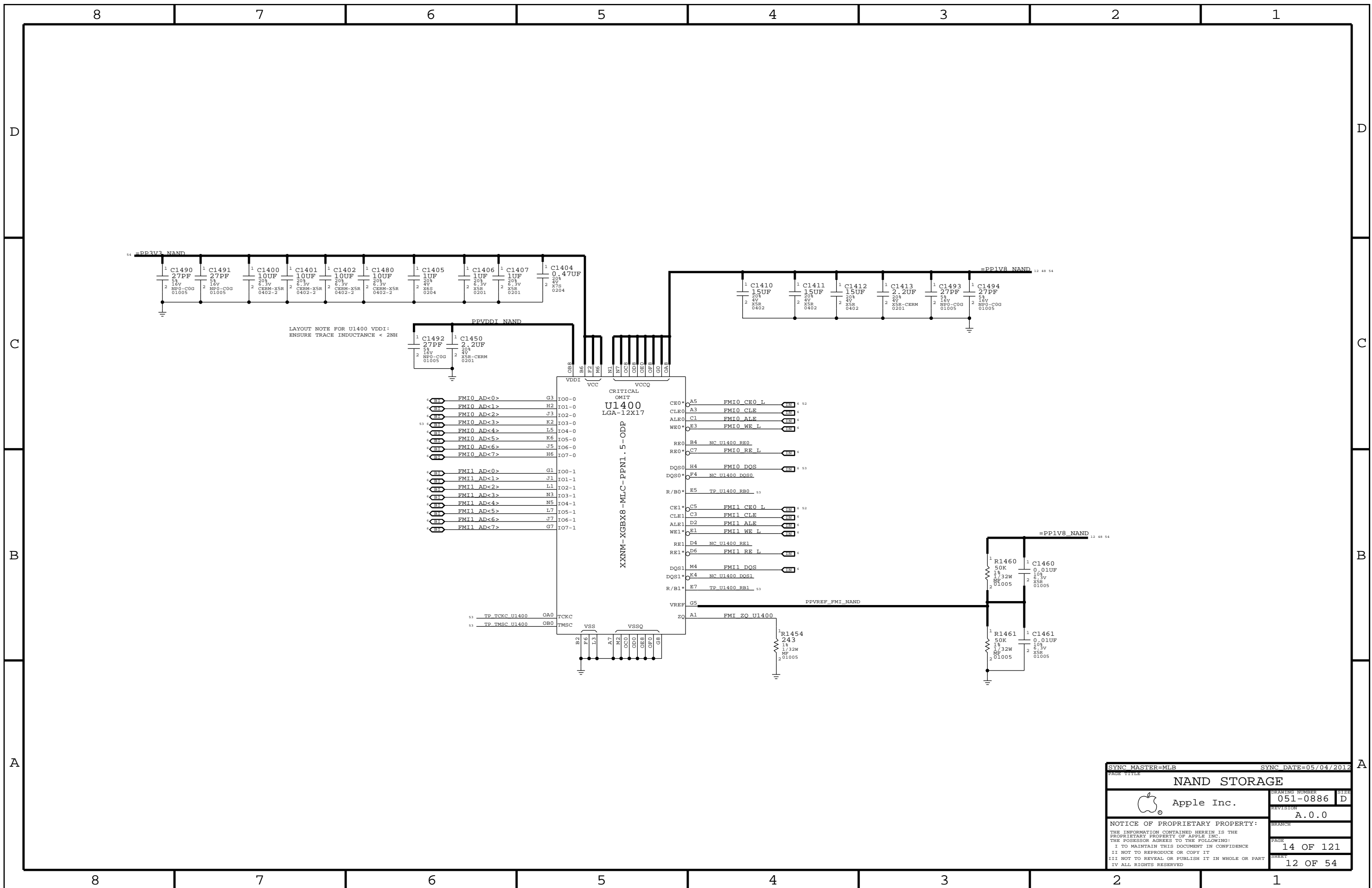
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343S0658 = TRISTAR 2, A1
 998-5855 = TRISTAR 2, TC
 343S0639 = TRISTAR 2, A0
 343S0614 = TRISTAR 1

TRISTAR



SYNC MASTER=N/A		SYNC DATE=N/A	
IO: TRISTAR			
Apple Inc.		DRAWING NUMBER	SIZE
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		PAGE	
		13 OF 121	
		SHEET	
		11 OF 54	

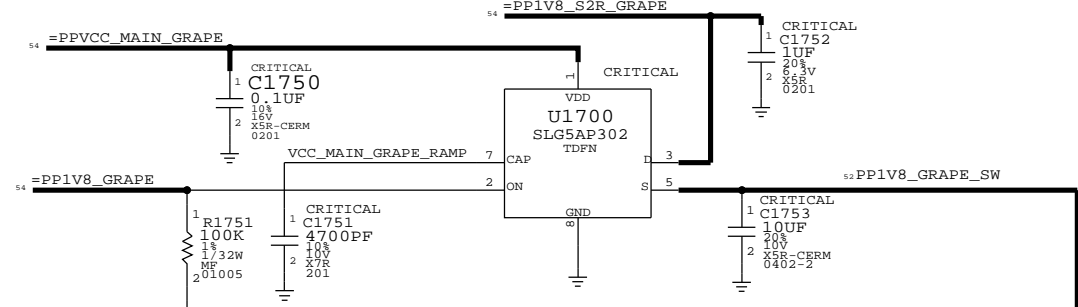
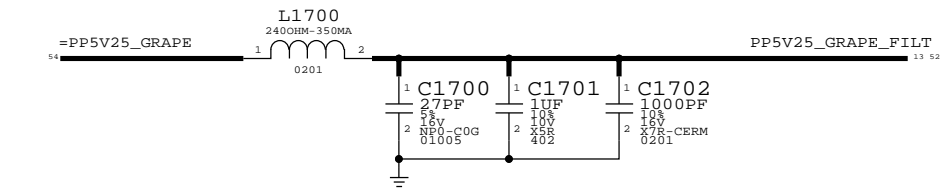


LAYOUT NOTE FOR U1400 VDDI:
ENSURE TRACE INDUCTANCE < 2NH

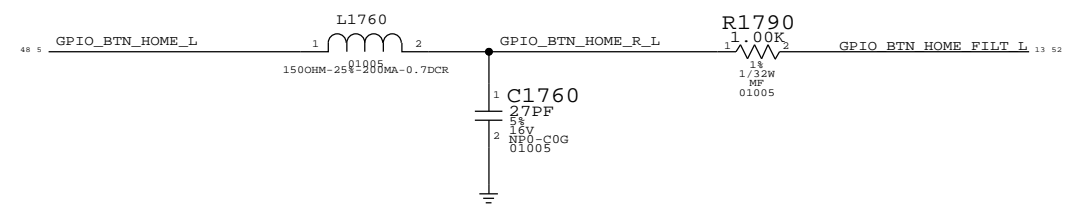
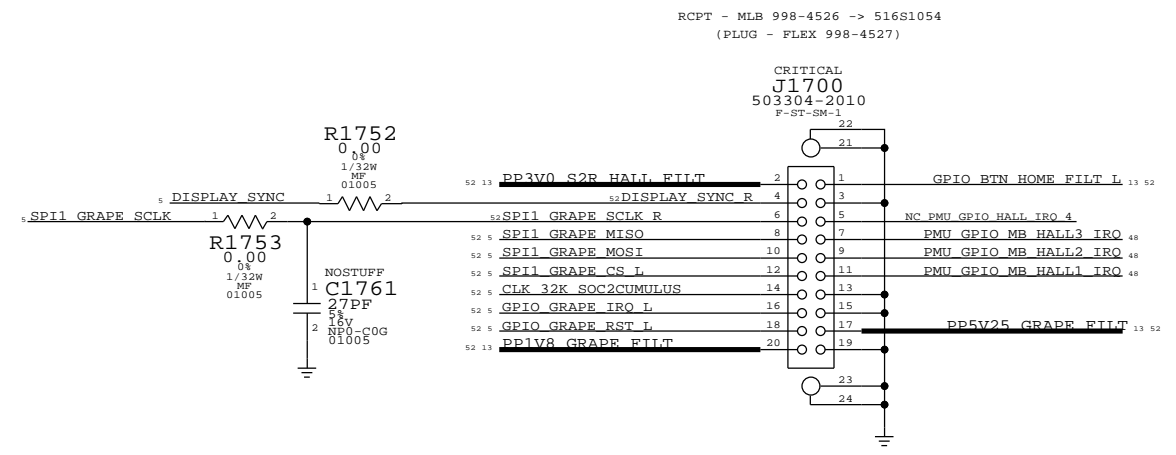
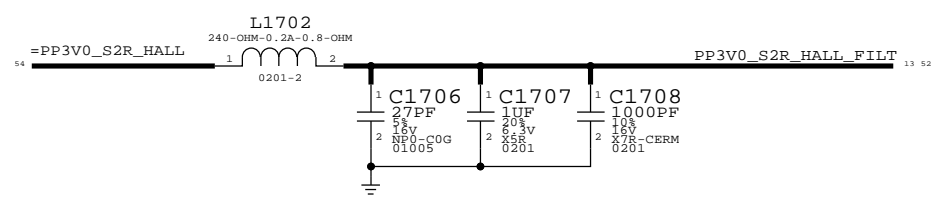
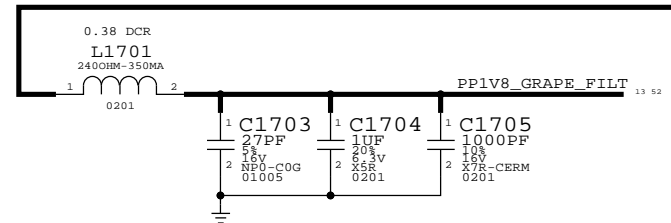
- CRITICAL OMIT**
- U1400**
LGA-12X17
- XXNM-XGBX8-MLC-PPN1.5-ODP**
- 6 FMI0_AD<0> G3 IO0-0
 - 6 FMI0_AD<1> H2 IO1-0
 - 6 FMI0_AD<2> J3 IO2-0
 - 6 FMI0_AD<3> K2 IO3-0
 - 6 FMI0_AD<4> L5 IO4-0
 - 6 FMI0_AD<5> K6 IO5-0
 - 6 FMI0_AD<6> J5 IO6-0
 - 6 FMI0_AD<7> H6 IO7-0
 - 6 FMI1_AD<0> G1 IO0-1
 - 6 FMI1_AD<1> J1 IO1-1
 - 6 FMI1_AD<2> L1 IO2-1
 - 6 FMI1_AD<3> N3 IO3-1
 - 6 FMI1_AD<4> N5 IO4-1
 - 6 FMI1_AD<5> L7 IO5-1
 - 6 FMI1_AD<6> J7 IO6-1
 - 6 FMI1_AD<7> G7 IO7-1

SYNC MASTER=MLB		SYNC DATE=05/04/2012	
NAND STORAGE			
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		PAGE	14 OF 121
		SHEET	12 OF 54

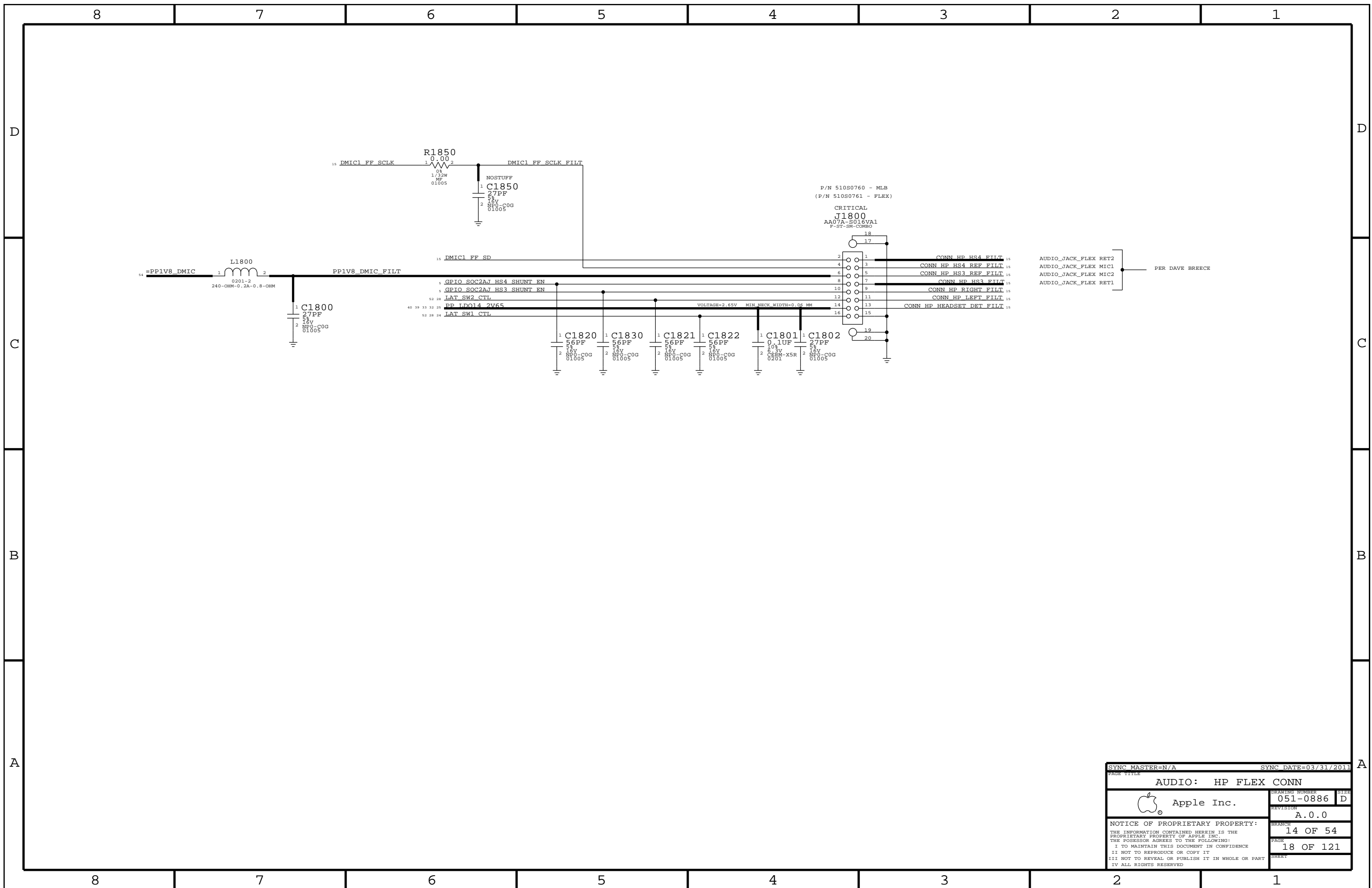
TOUCH SUBSYSTEM



LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION



SYNC MASTER=N/A		SYNC DATE=06/21/2010	
PAGE TITLE TOUCH: SUPPORT CKT & CONN			
DRAWING NUMBER 051-0886		SIZE D	
REVISION A.0.0		BRANCH	
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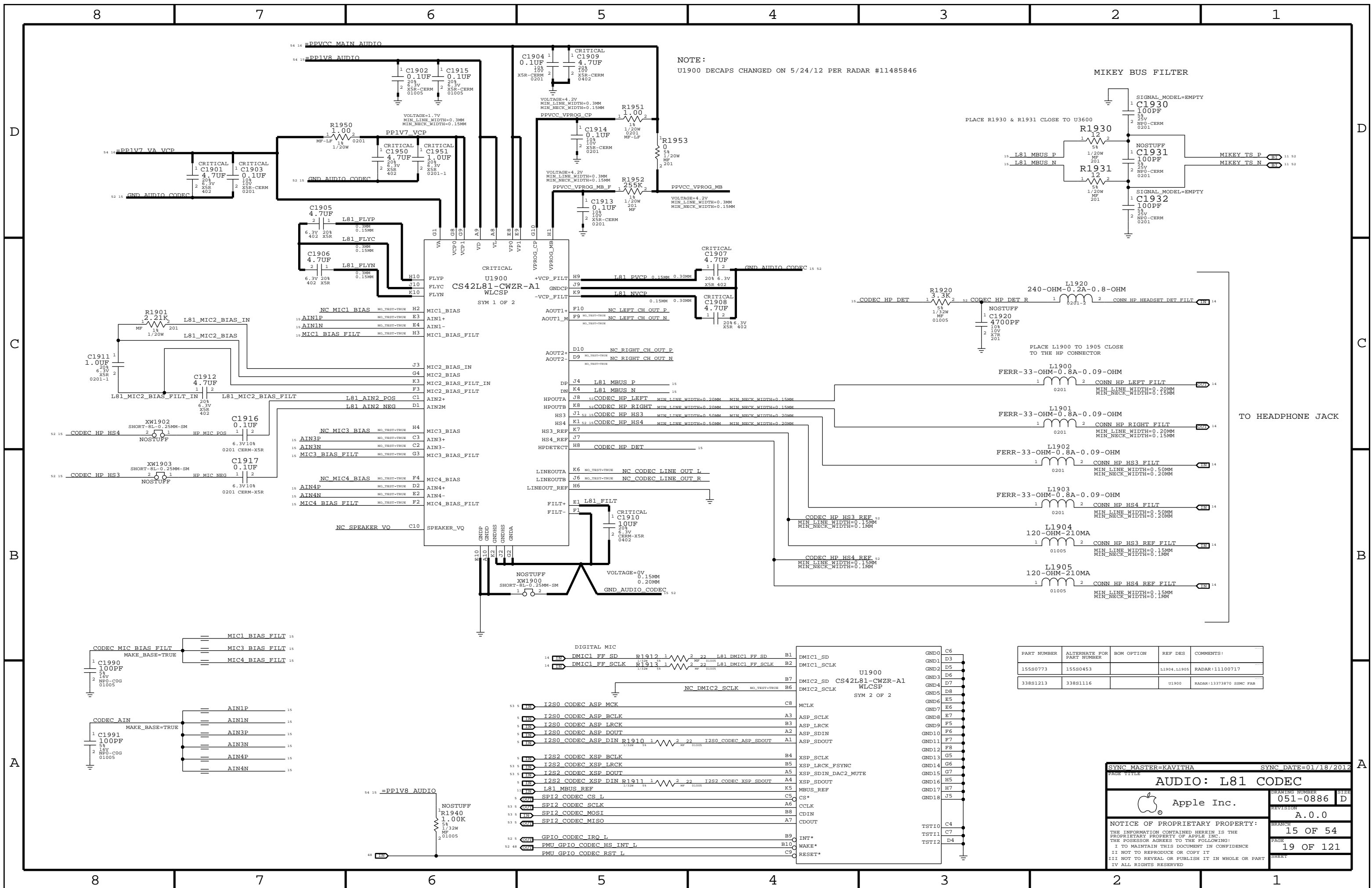
P/N 510S0760 - MLB
(P/N 510S0761 - FLEX)

CRITICAL
J1800
AA07A-S016VA1
F-ST-SM-COMBO

AUDIO_JACK_FLEX RET2
AUDIO_JACK_FLEX MIC1
AUDIO_JACK_FLEX MIC2
AUDIO_JACK_FLEX RET1

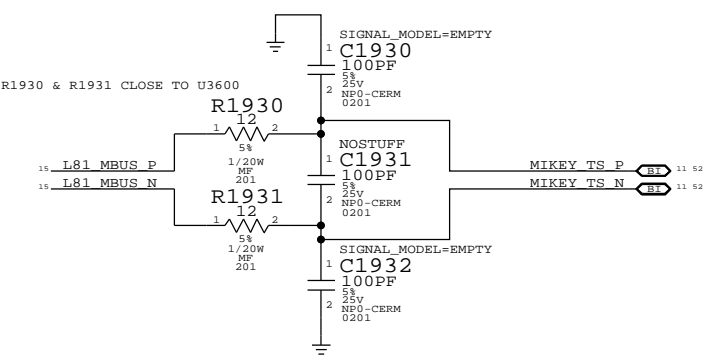
PER DAVE BREECE

SYNC MASTER=N/A		SYNC DATE=03/31/2011	
AUDIO: HP FLEX CONN			
		DRAWING NUMBER	SIZE
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		PAGE	18 OF 121
		SHEET	



NOTE:
U1900 DECAPS CHANGED ON 5/24/12 PER RADAR #11485846

MIKEY BUS FILTER



TO HEADPHONE JACK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580773	15580453		L1904, L1905	RADAR:11100717
33881213	33881116		U1900	RADAR:13373870 SEMC FAB

SYNC MASTER=KAVITHA SYNC DATE=01/18/2012

AUDIO: L81 CODEC

Apple Inc.

DRAWING NUMBER: 051-0886 SIZE: D

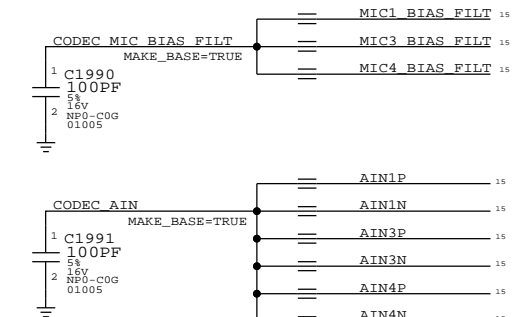
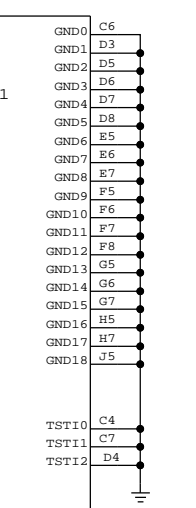
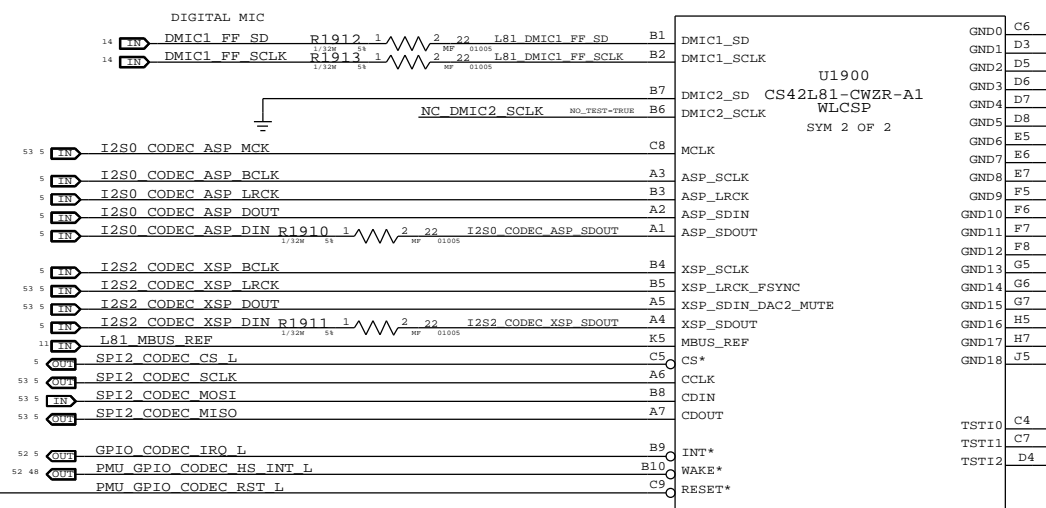
REVISION: A.0.0

BRANCH: 15 OF 54

PAGE: 19 OF 121

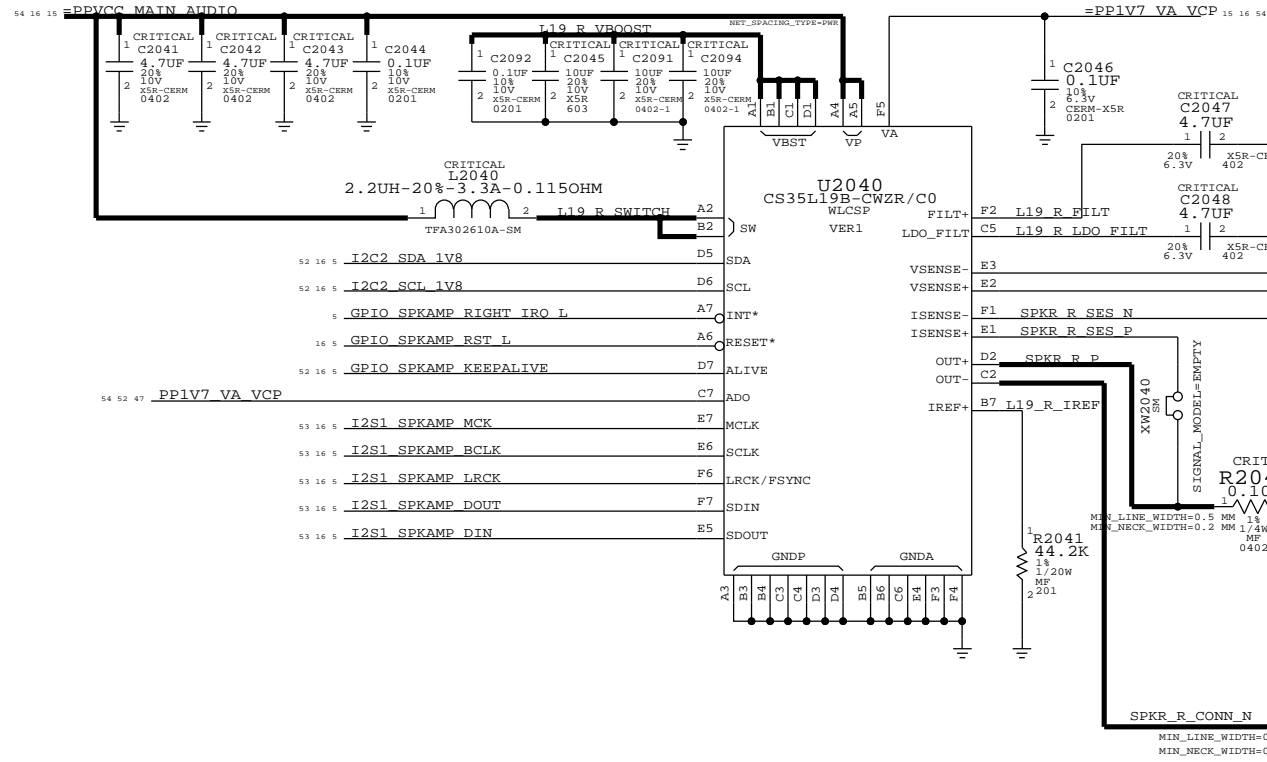
SHEET

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RIGHT SPEAKER AMP

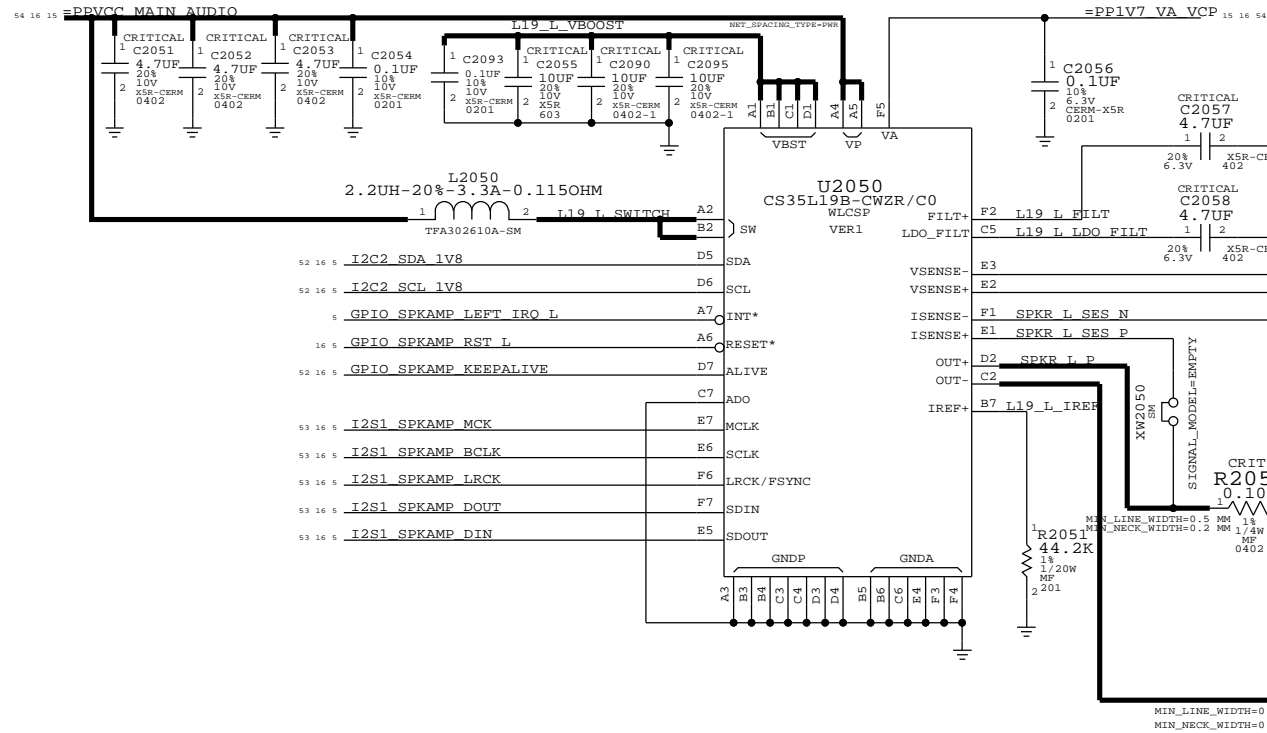
I2C ADDRESS: 100001X



SPEAKER CONNECTOR

LEFT SPEAKER AMP

I2C ADDRESS: 100000X



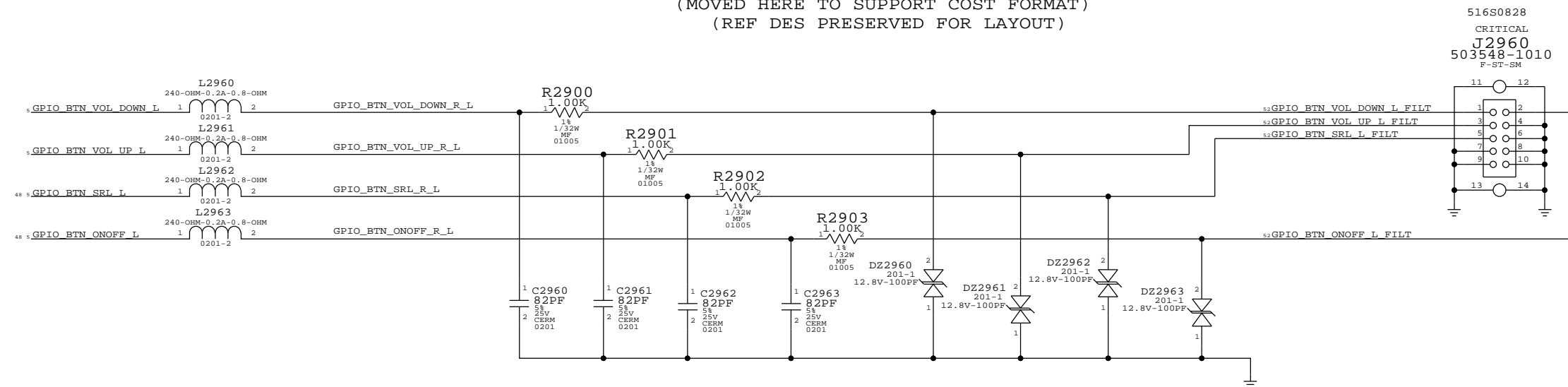
UPDATED: DEC 13

1. ALL THE EMI/DESENSE FILTER COMPONENTS HAVE BEEN REMOVED BASED ON PERFORMANCE ON J65
2. THE CURRENT VERSION OF L19 IS B0 AND WILL CHANGE TO C0 BY MARCH 2013. C0 FIXES PROCESS ISSUES.

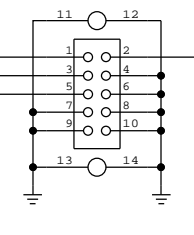
SYNC MASTER=KAVITHA		SYNC DATE=01/18/2012	
PAGE TITLE			
AUDIO: CS35L19A AMPS		DRAWING NUMBER	SIZE
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		16 OF 54	

BUTTON CONNECTOR

(MOVED HERE TO SUPPORT COST FORMAT)
(REF DES PRESERVED FOR LAYOUT)

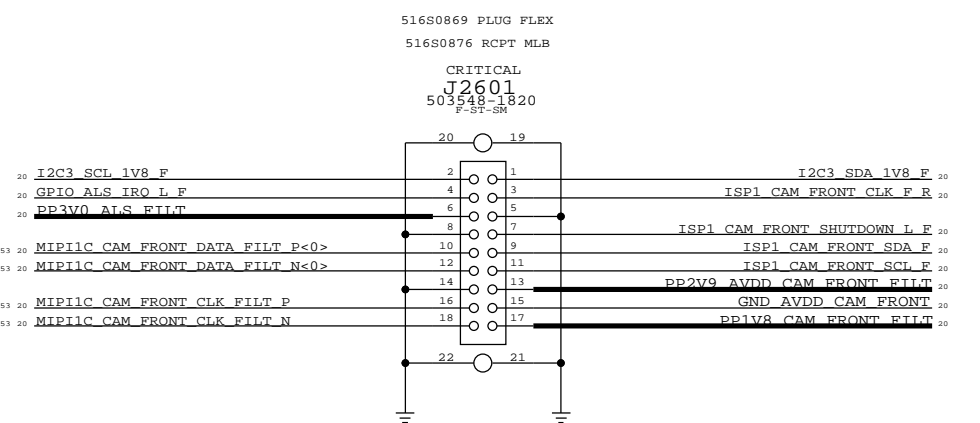
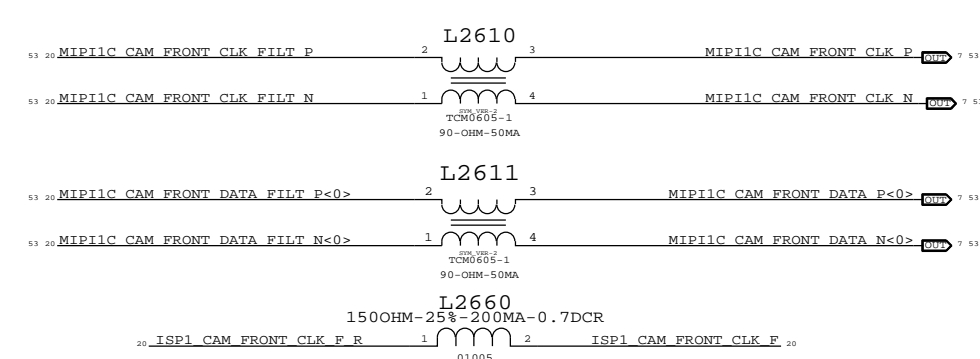
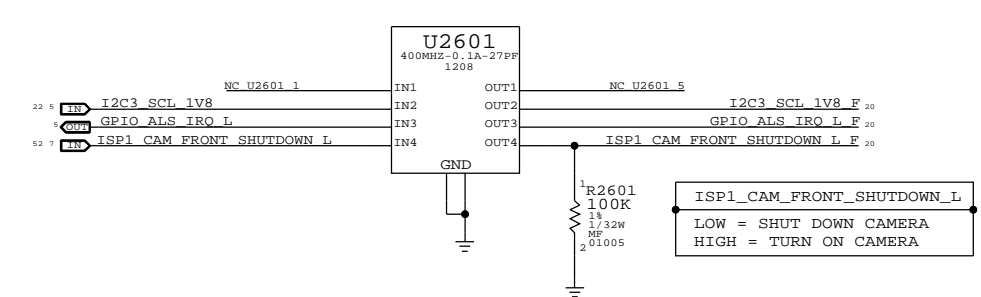
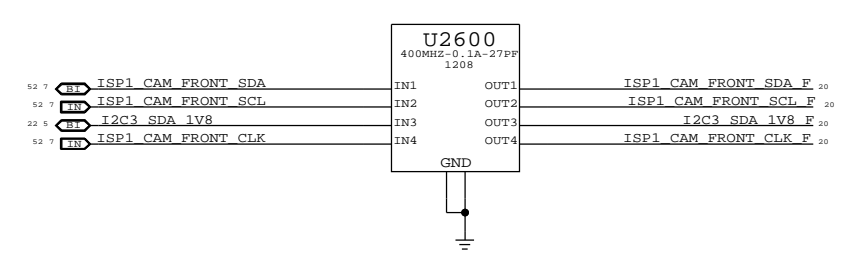
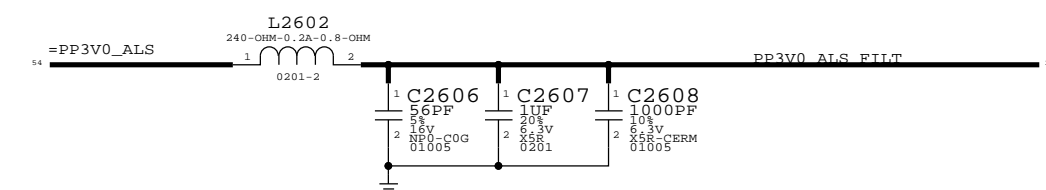
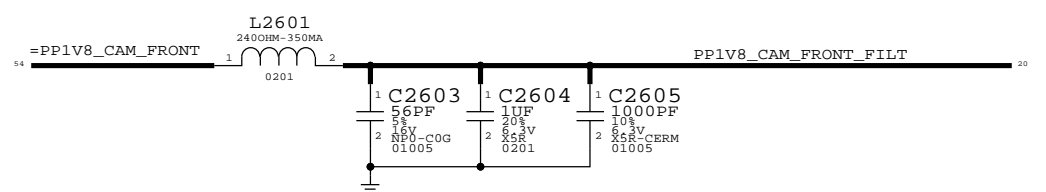
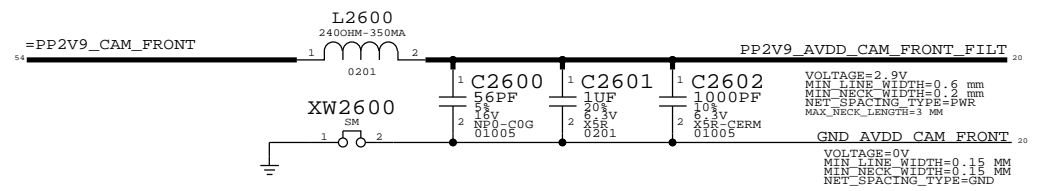


516S0828
CRITICAL
J2960
503548-1010
P-ST-SM



SYNC MASTER=N/A		SYNC DATE=N/A	
BUTTON: CONN			
Apple Inc.		DRAWING NUMBER	SIZE
		051-0886	D
		REVISION	
		A.0.0	
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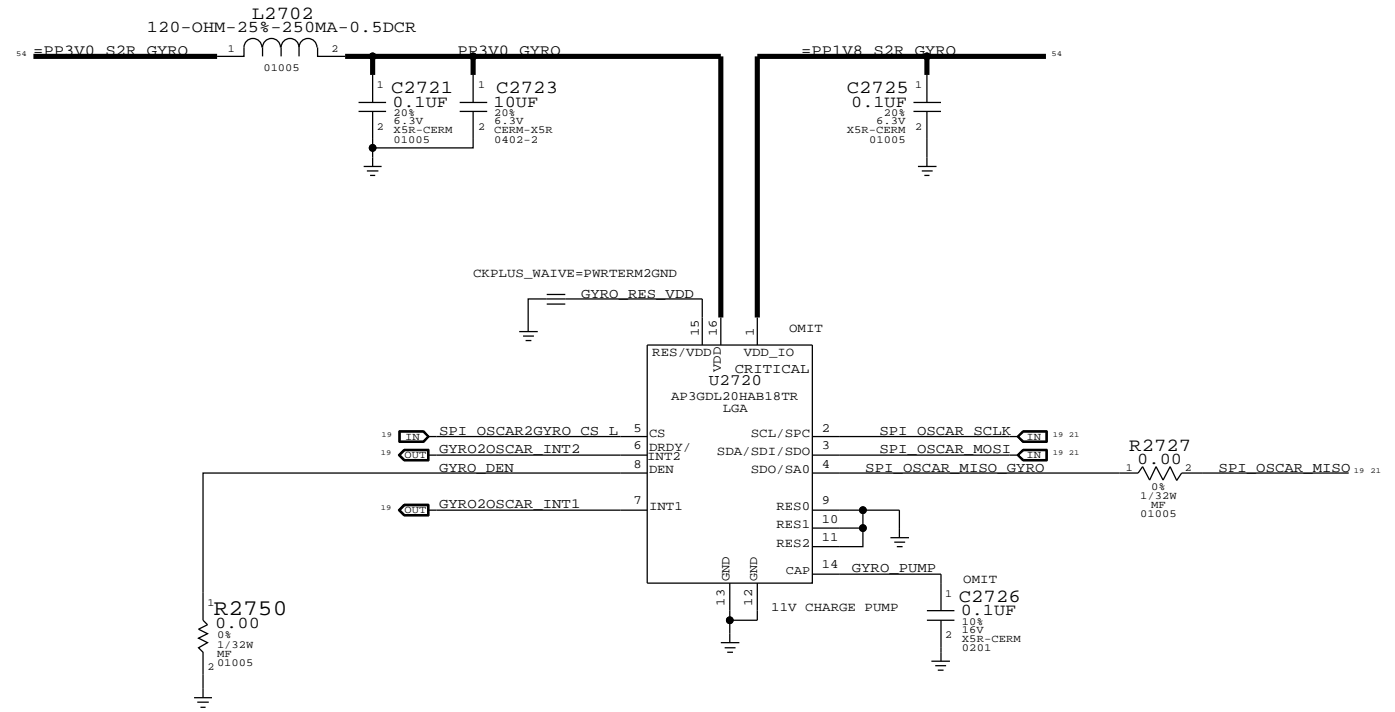
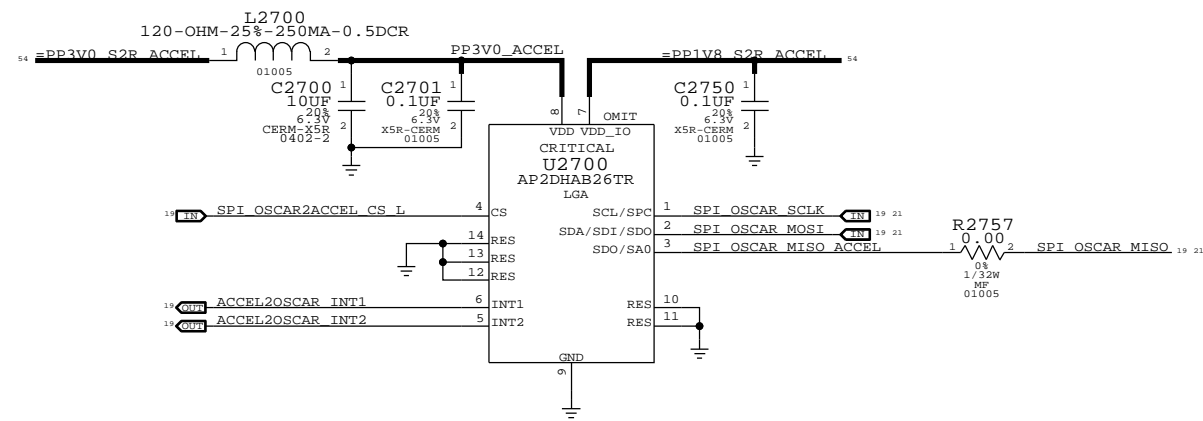
VGA FRONT CAMERA CONNECTOR



PAGE TITLE		SYNC MASTER=J85 MLB C		SYNC DATE=12/03/2012	
CAMERA: FF-ALS CONN & FILTERS					
DRAWING NUMBER		051-0886		SIZE	
REVISION		A.0.0		D	
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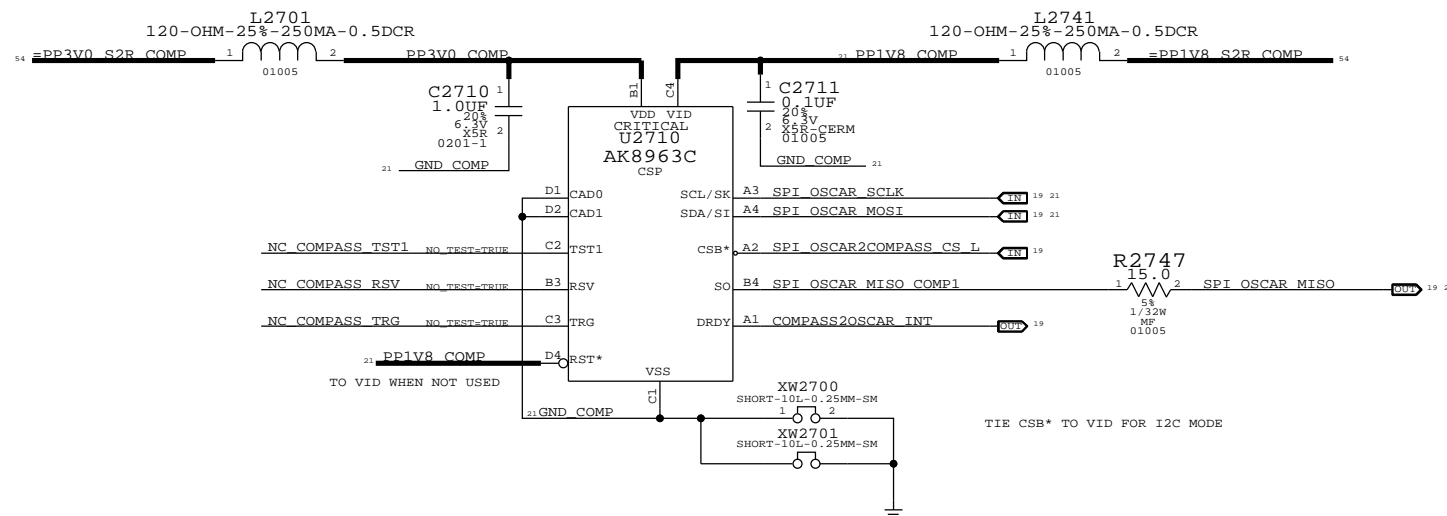
GYRO

ACCELEROMETER



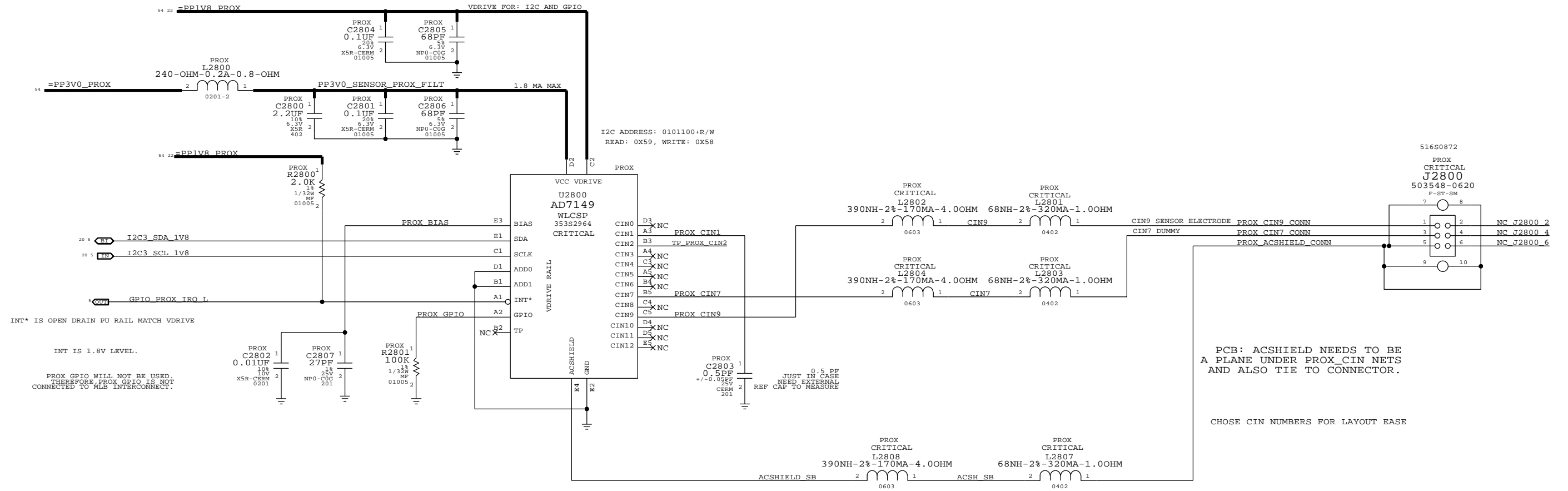
COMPASS

APN 338S1014



SYNC MASTER=N/A		SYNC DATE=N/A	
PAGE TITLE: SENSOR: ACCEL, COMPASS, GYRO			
DRAWING NUMBER: 051-0886		SIZE: D	
REVISION: A.0.0		BRANCH:	
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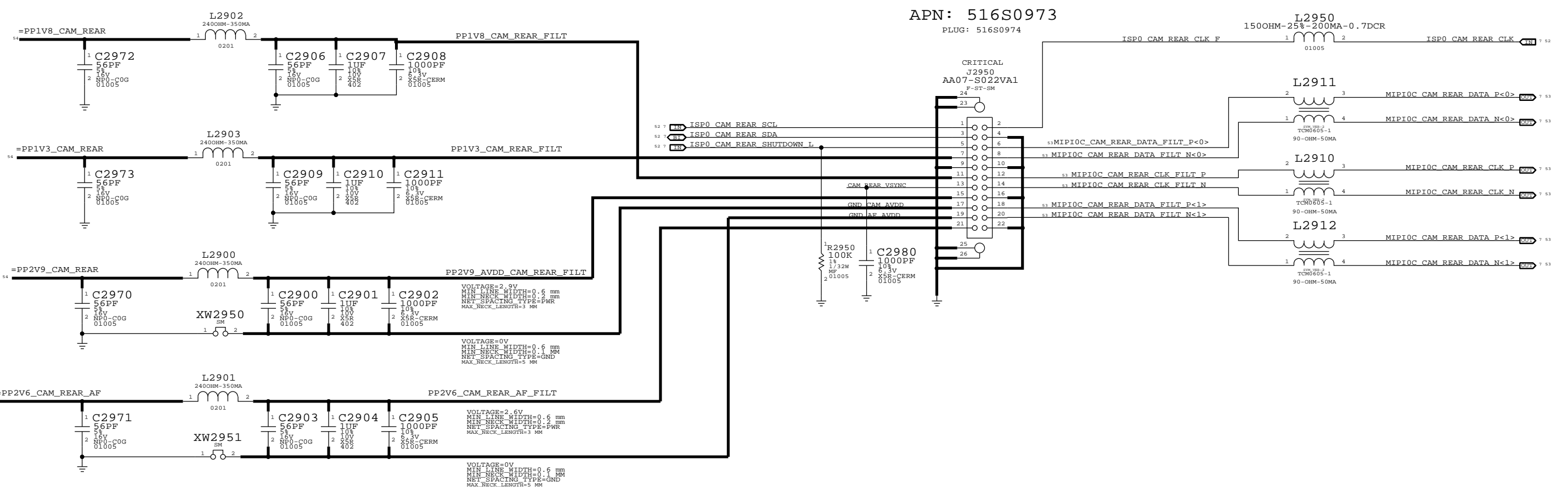
PROX SENSOR



PCB: ENSURE ACSHIELD PLANE UNDER U3200, NO GND PLANE NEAR PROX_CIN NETS..

SYNC MASTER=J85 MLB C		SYNC DATE=12/05/12	
PAGE TITLE			
SENSOR: PROX		DRAWING NUMBER	SIZE
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REAR CAMERA CONNECTOR



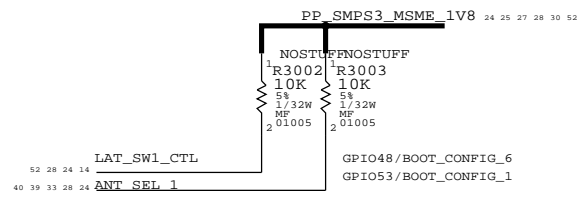
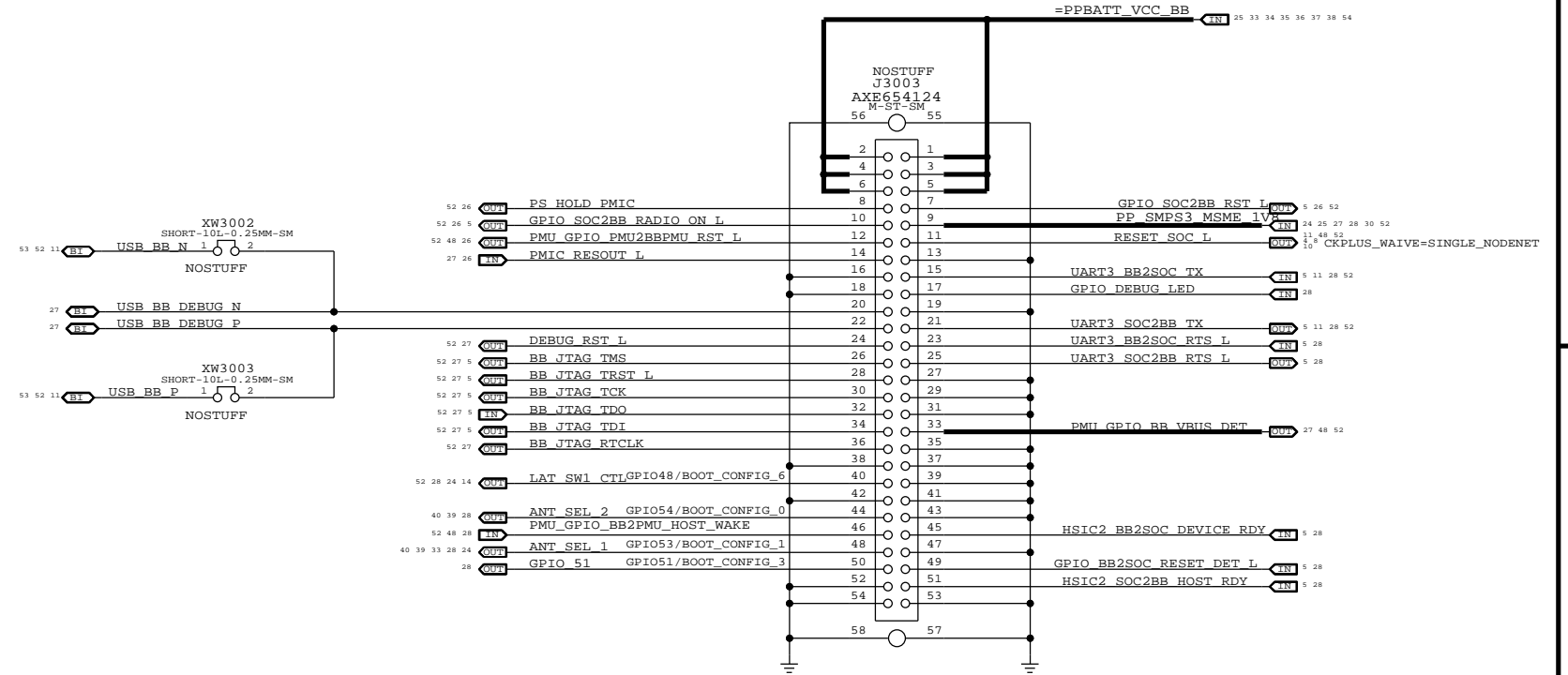
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CAMERA: REAR CONN & FILTERS			
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AP INTERFACE & DEBUG CONNECTORS

PROBE POINTS

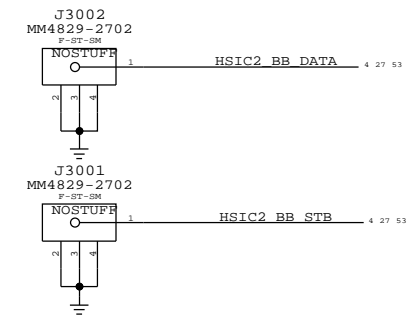
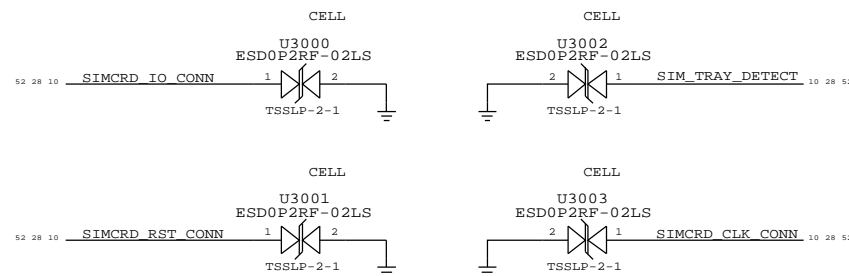
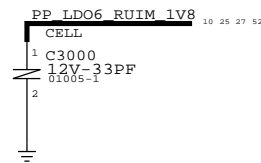
PP3000	P4MM	1	BB_ERROR_FLAG	28
PP3001	P4MM	1	SLEEP_CLK_32K	26 27
PP3002	P4MM	1	PMIC_SSBI	26 27
PP3003	P4MM	1	19P2M_MDM	26 27
PP3008	P4MM	1	WTR_SSBI_TX_GPS	28 29
PP3009	P4MM	1	WTR_SSBI_PRX_DRX	28 29
PP3010	P4MM	1	WTR_RX_ON	28 29
PP3011	P4MM	1	WTR_RF_ON	28 29
PP3012	P4MM	1	UART_WLAN2BB_LTE_COEX	28 44
PP3013	P4MM	1	UART_BB2WLAN_LTE_COEX	28 44

DEBUG CONNECTOR



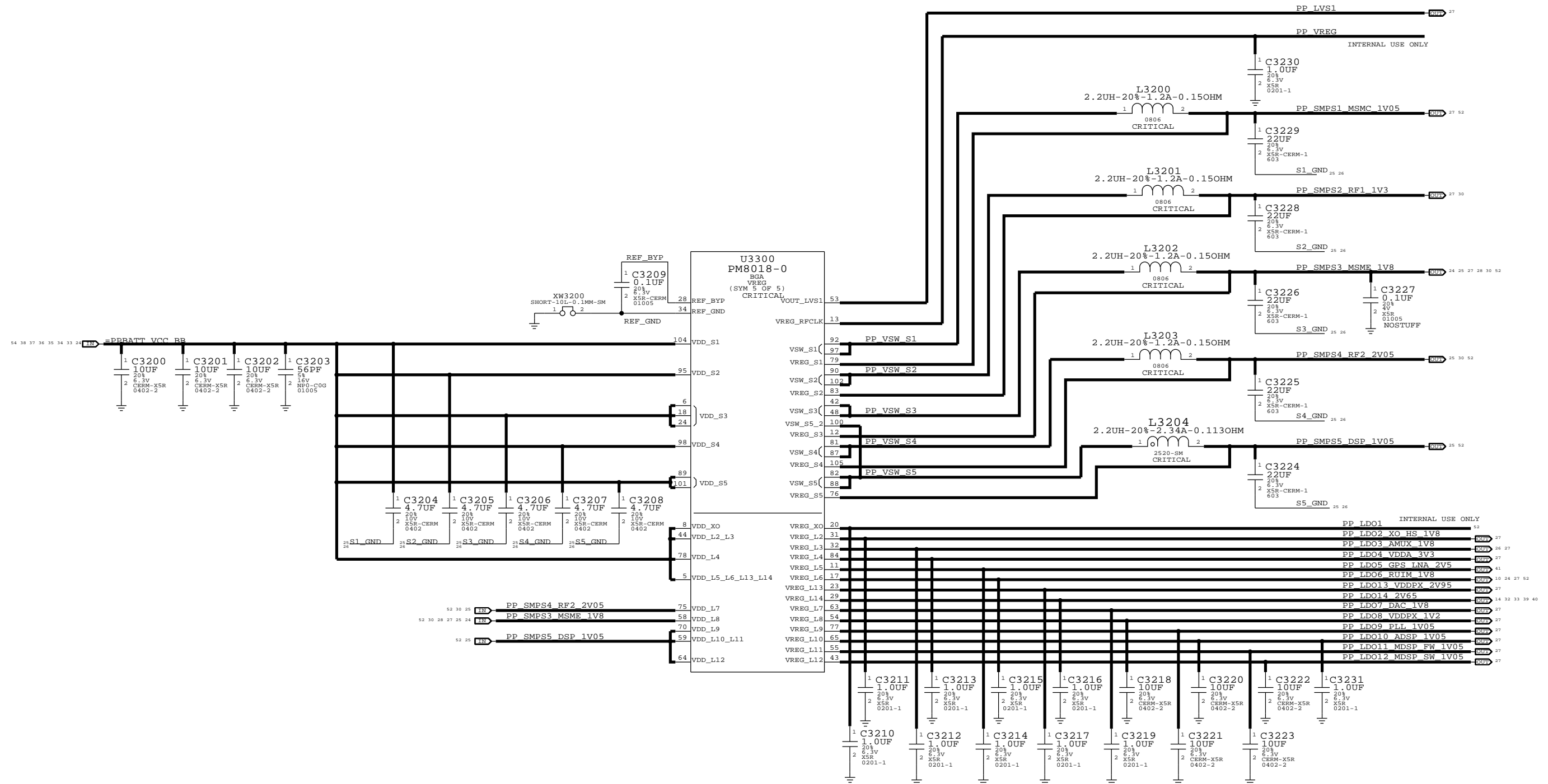
BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION								
		6	5	4	3	2	1	0		
BOOT_DEFAULT_OPTION	0x00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0x01	X	1	0	0	0	0	0	0	1
BOOT_HSIC_OPTION	0x02	X	1	0	0	0	0	0	1	0
BOOT_USB_OPTION	0x03	X	1	0	0	0	0	0	1	1
ENABLE SAHARA PROTOCOL	0x08	X	1	0	0	1	0	X	X	X

SIM CARD ESD PROTECTION



PAGE TITLE		
CELL:AP INTERFACE & DEBUG CONNECTORS		
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	30 OF 121	
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PMU (1 OF 2)



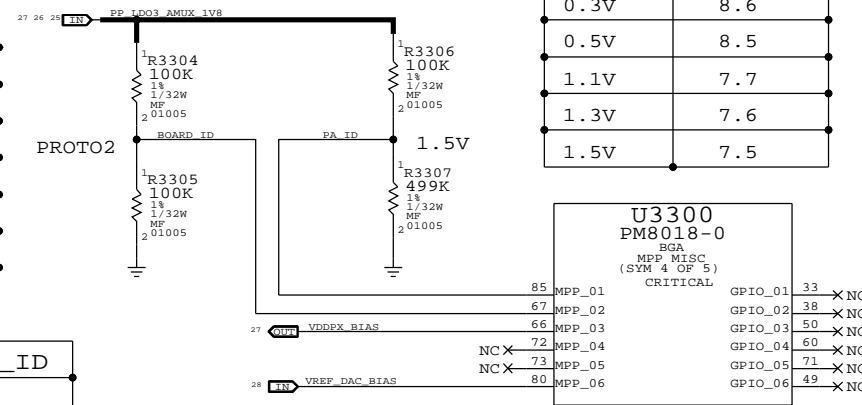
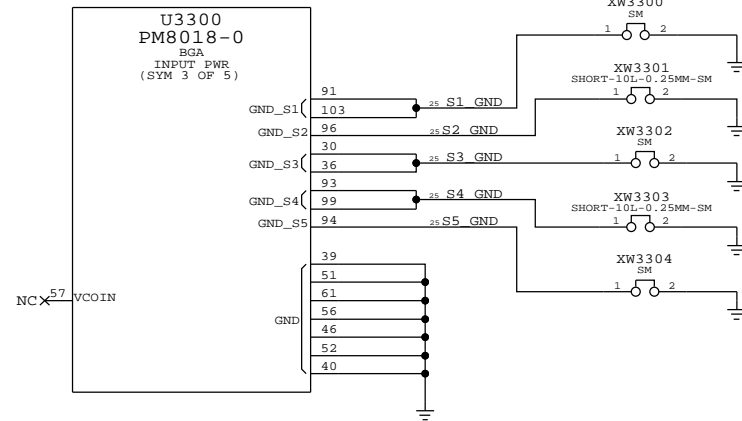
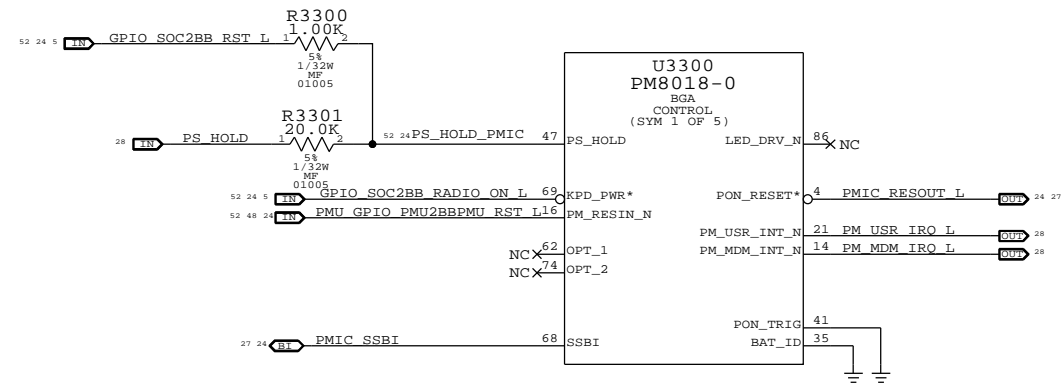
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REVISION	BRANCH	PAGE
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PMU (2 OF 2)

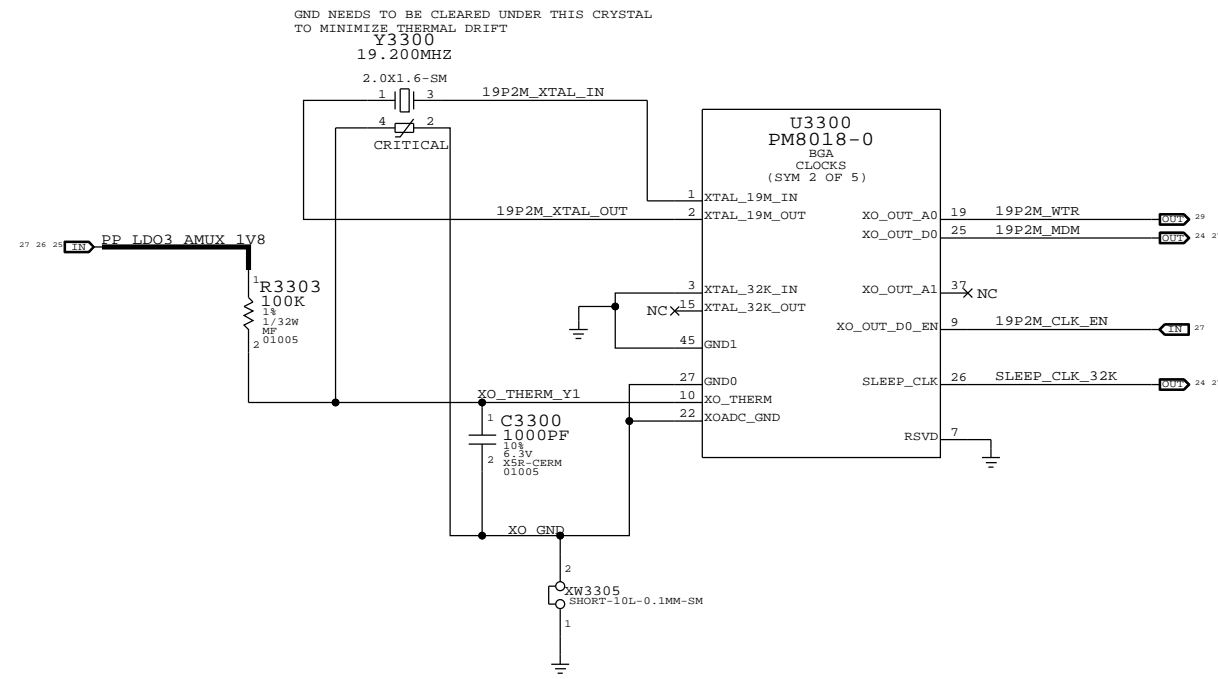
BOARD_ID	REVISION
0.7V	PROTO1
0.9V	PROTO2
1.1V	EVT1
1.3V	EVT2
1.5V	DVT
1.7V	PVT

BB GPIO_29	PRODUCT_ID
1 (1.8V)	JXX
0 (NC, PD)	NXX

PA_ID	MAV VER
0.1V	8.7
0.3V	8.6
0.5V	8.5
1.1V	7.7
1.3V	7.6
1.5V	7.5



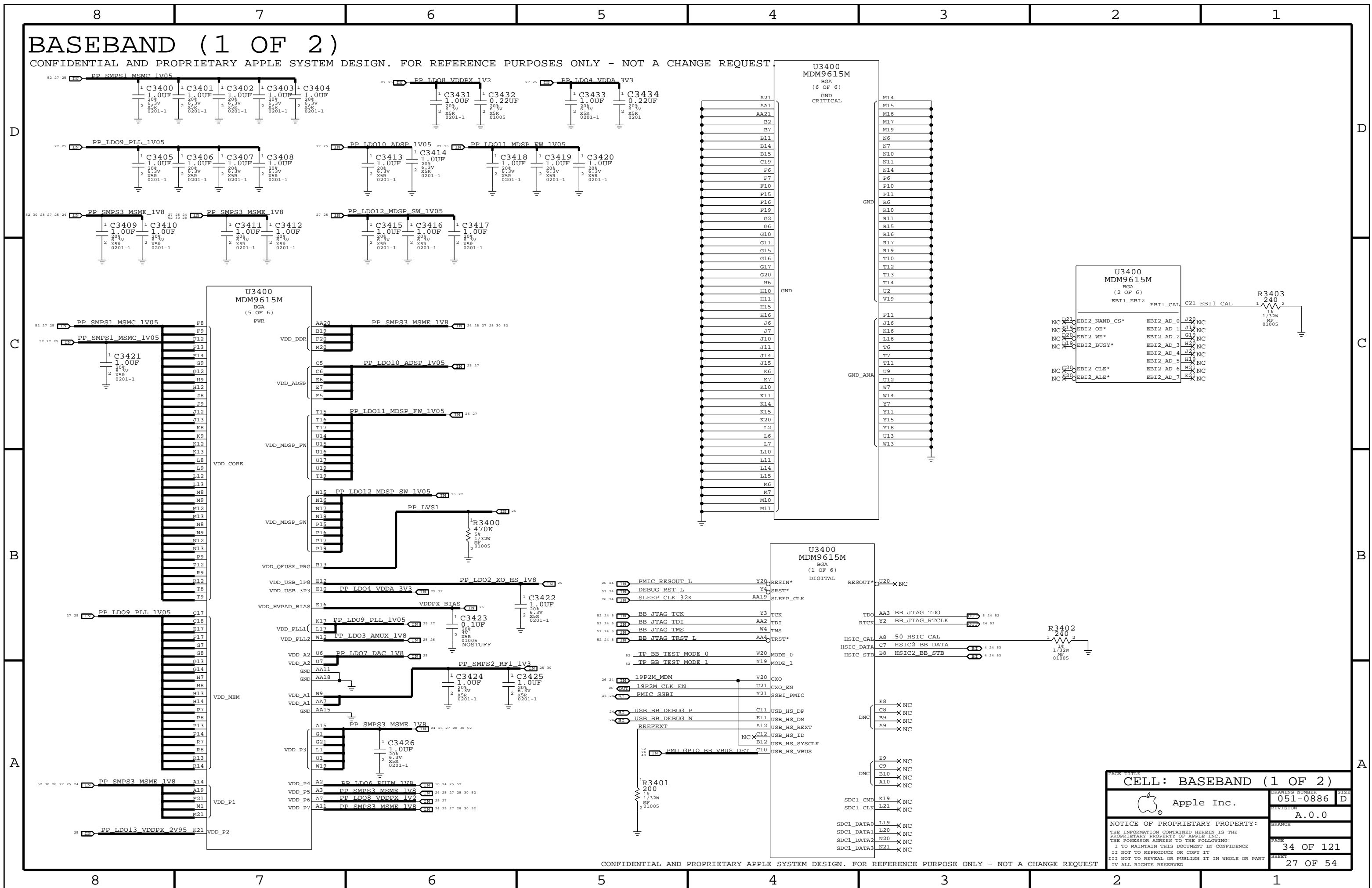
AP SECTION NEEDS ITS OWN THERMISTOR PLACED NEAR THE PA'S.



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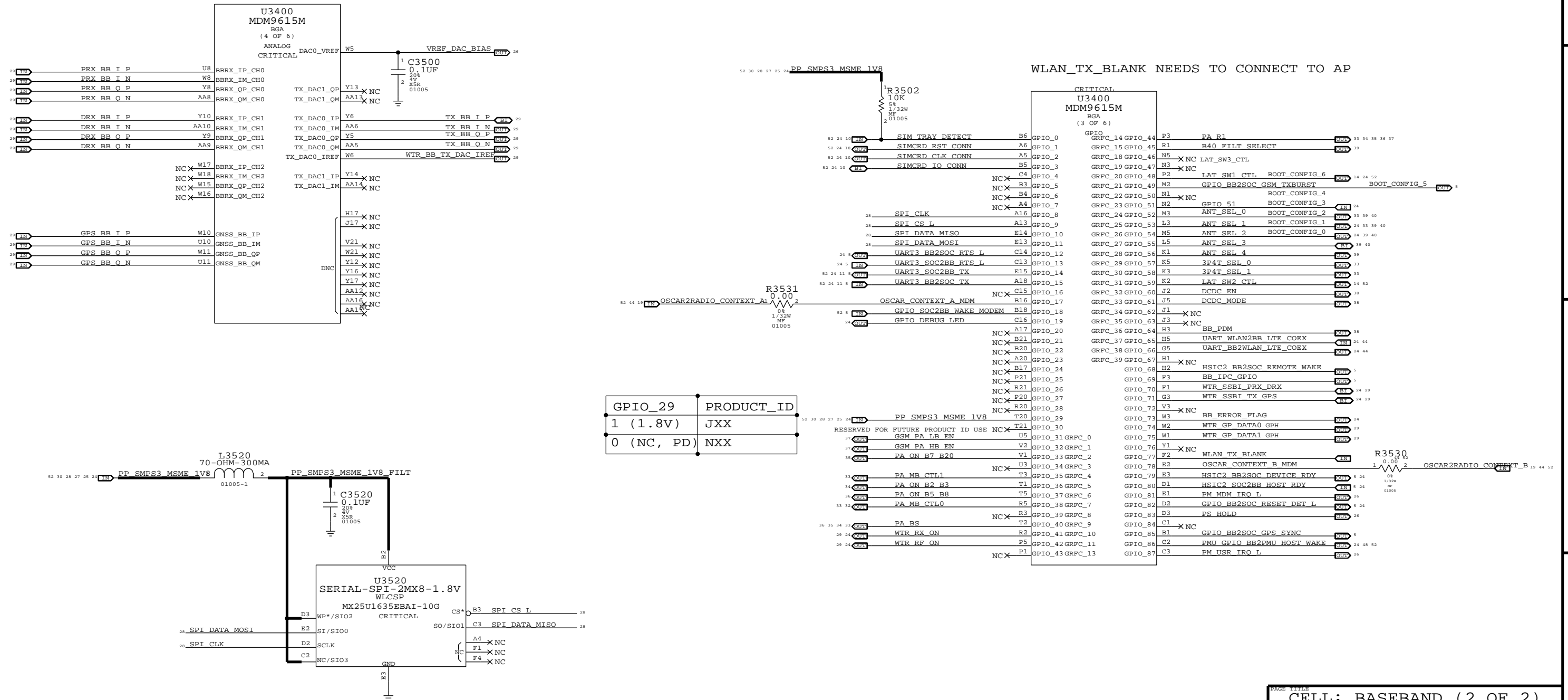
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BASEBAND (2 OF 2)



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Apple Inc.

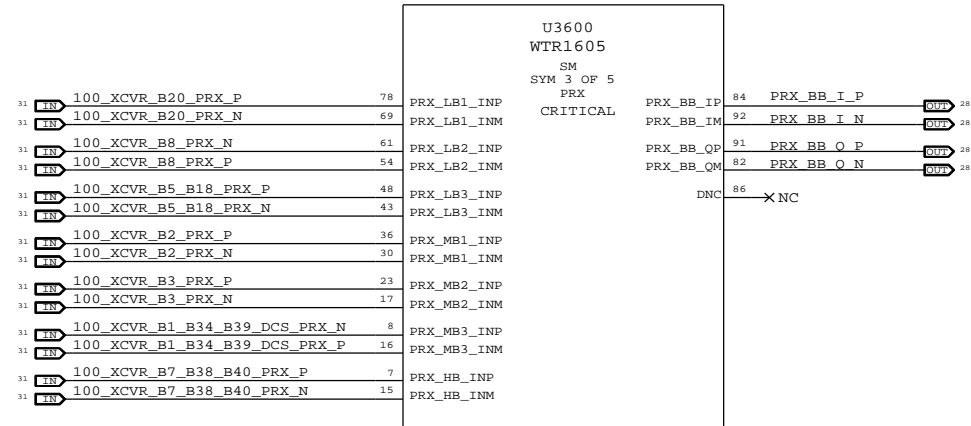
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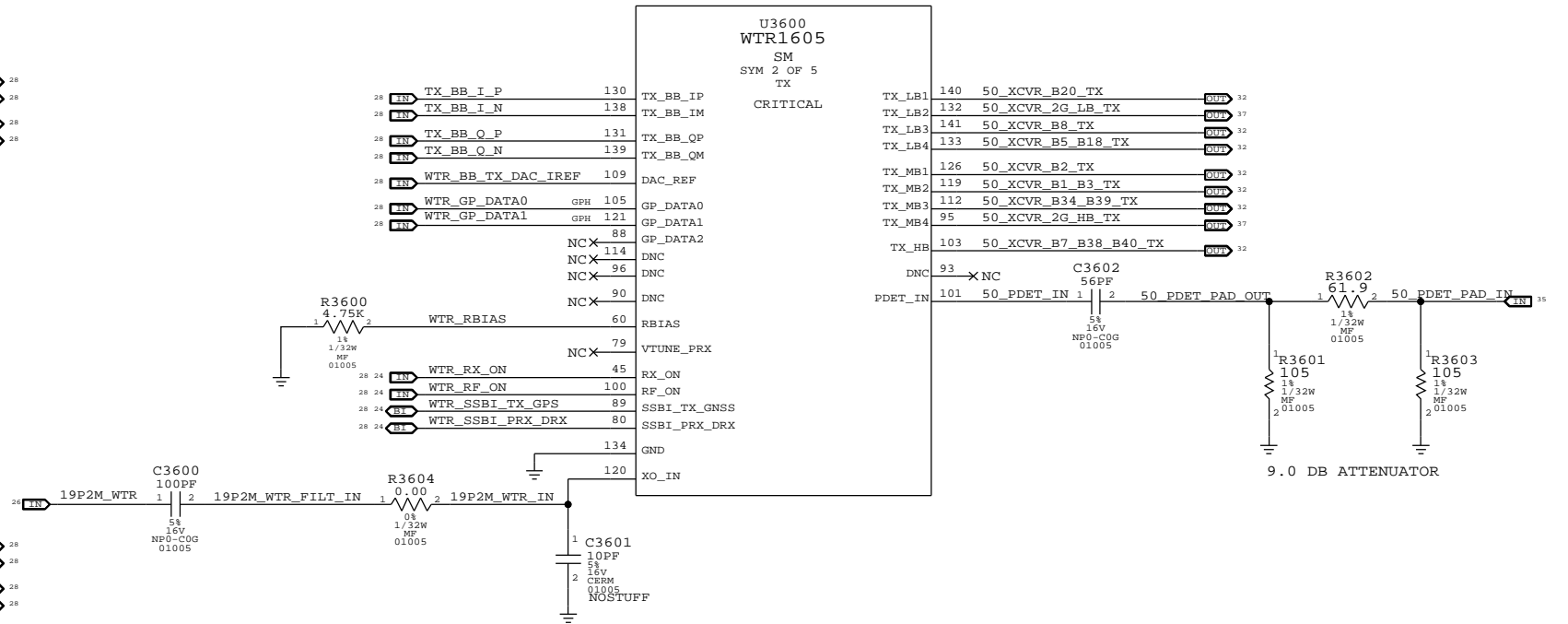
PAGE: 35 OF 121
 SHEET: 28 OF 54

RF TRANSCEIVER (1 OF 2)

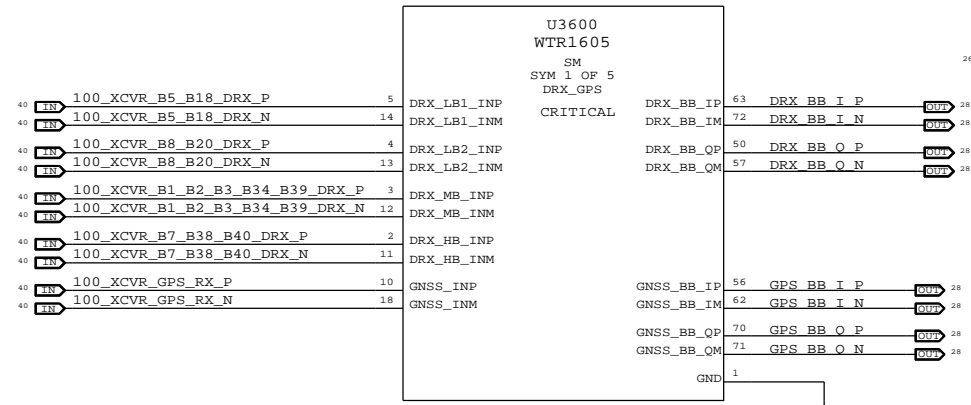
PRX TRANSCEIVER RF AND IQ PORTS



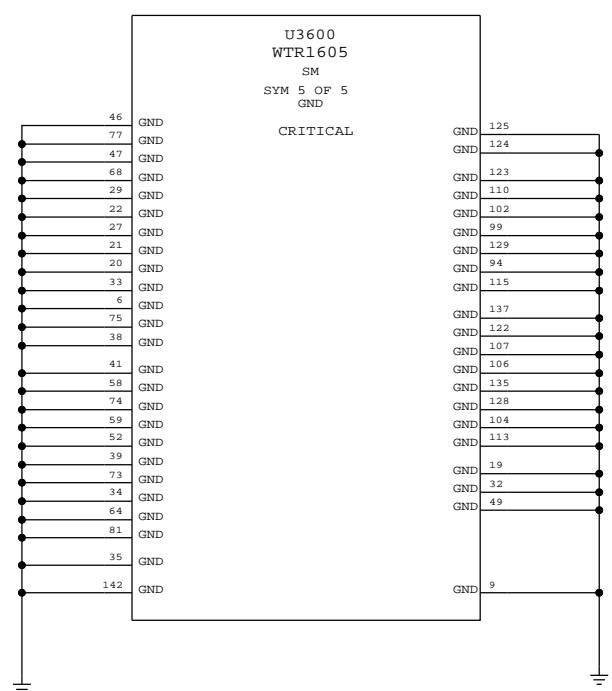
TRANSCEIVER PHASE CONTROL, TX RF & IQ PORTS



DRX TRANSCEIVER RF AND IQ PORTS

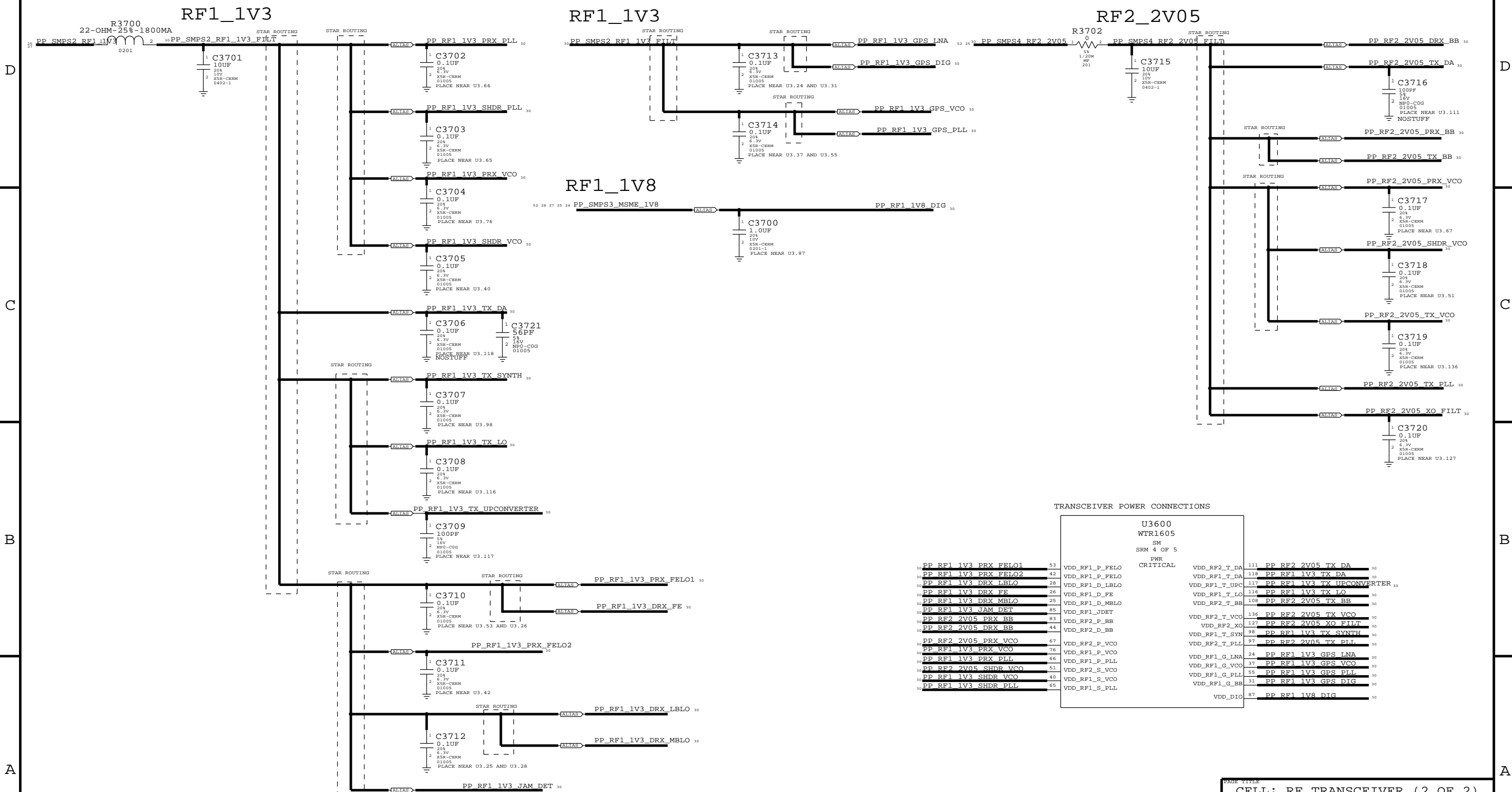


TRANSCEIVER GROUND CONNECTIONS



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		29 OF 54

RF TRANSCEIVER (2 OF 2)

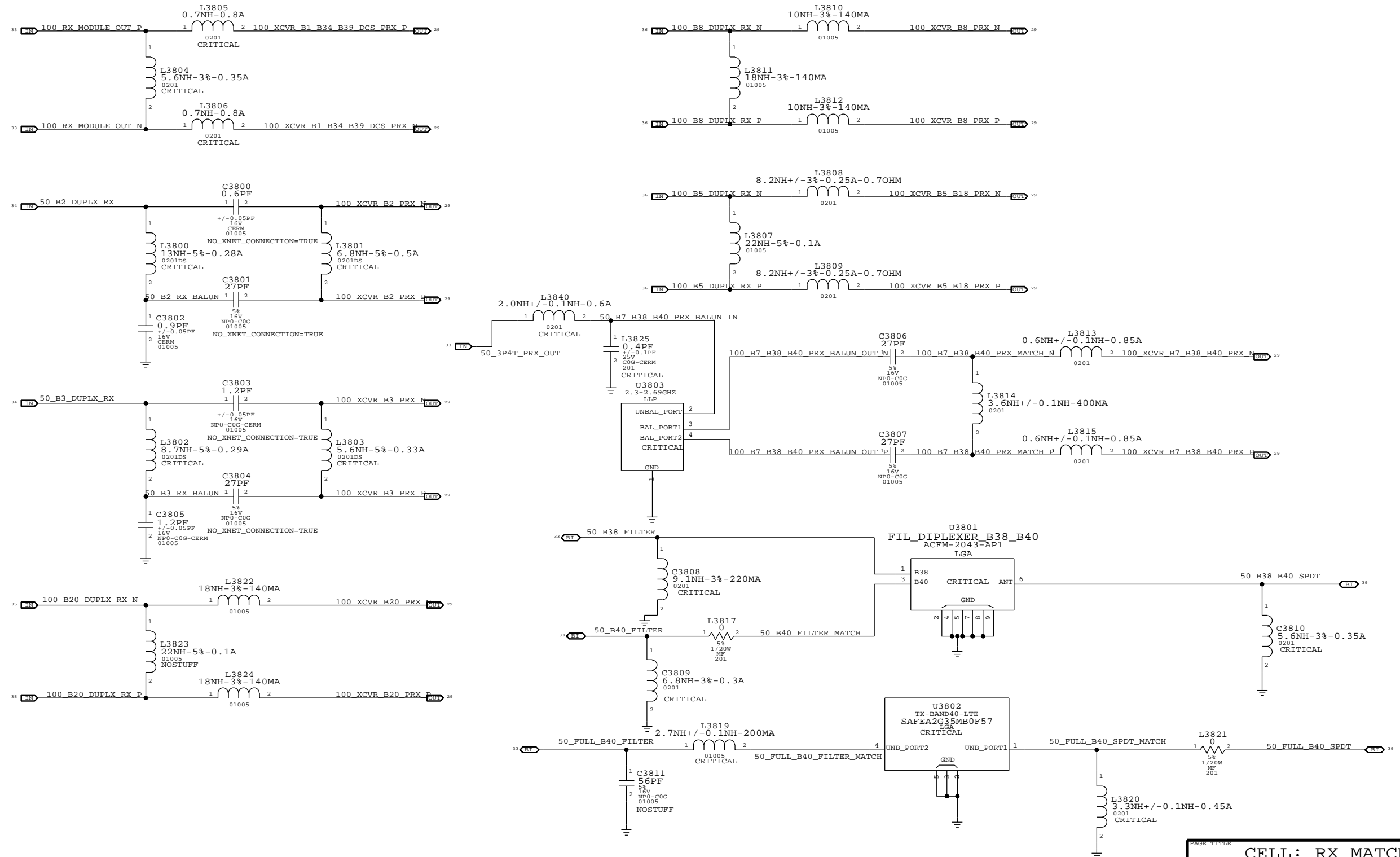


TRANSCEIVER POWER CONNECTIONS

U3600		U3600	
WTR1605		WTR1605	
SM		SM	
SRM 4 OF 5		SRM 4 OF 5	
PWR		PWR	
CRITICAL		CRITICAL	
30 PP_RF1_1V3_PRX_FEL01	53 VDD_RF1_P_FEL0	VDD_RF2_T_DA	111 PP_RF2_2V05_TX_DA
30 PP_RF1_1V3_PRX_FEL02	42 VDD_RF1_P_FEL0	VDD_RF1_T_DA	118 PP_RF1_1V3_TX_DA
30 PP_RF1_1V3_DRX_LBLO	28 VDD_RF1_D_LBLO	VDD_RF1_T_UPC	117 PP_RF1_1V3_TX_UPCONVERTER
30 PP_RF1_1V3_DRX_FE	26 VDD_RF1_D_FE	VDD_RF1_T_LO	116 PP_RF1_1V3_TX_LO
30 PP_RF1_1V3_DRX_MBLO	25 VDD_RF1_D_MBLO	VDD_RF2_T_BB	108 PP_RF2_2V05_TX_BB
30 PP_RF1_1V3_JAM_DET	85 VDD_RF1_JDET	VDD_RF2_T_VCO	136 PP_RF2_2V05_TX_VCO
30 PP_RF2_2V05_PRX_BB	83 VDD_RF2_P_BB	VDD_RF2_XO	127 PP_RF2_2V05_XO_FILT
30 PP_RF2_2V05_DRX_BB	44 VDD_RF2_D_BB	VDD_RF1_T_SYN	98 PP_RF1_1V3_TX_SYNTH
30 PP_RF2_2V05_PRX_VCO	67 VDD_RF2_P_VCO	VDD_RF2_T_PLL	97 PP_RF2_2V05_TX_PLL
30 PP_RF1_1V3_PRX_VCO	76 VDD_RF1_P_VCO	VDD_RF1_G_LNA	24 PP_RF1_1V3_GPS_LNA
30 PP_RF1_1V3_PRX_PLL	66 VDD_RF1_P_PLL	VDD_RF1_G_VCO	37 PP_RF1_1V3_GPS_VCO
30 PP_RF2_2V05_SHDR_VCO	51 VDD_RF2_S_VCO	VDD_RF1_G_PLL	55 PP_RF1_1V3_GPS_PLL
30 PP_RF1_1V3_SHDR_VCO	40 VDD_RF1_S_VCO	VDD_RF1_G_BB	31 PP_RF1_1V3_GPS_DIG
30 PP_RF1_1V3_SHDR_PLL	65 VDD_RF1_S_PLL	VDD_DIO	87 PP_RF1_1V8_DIG

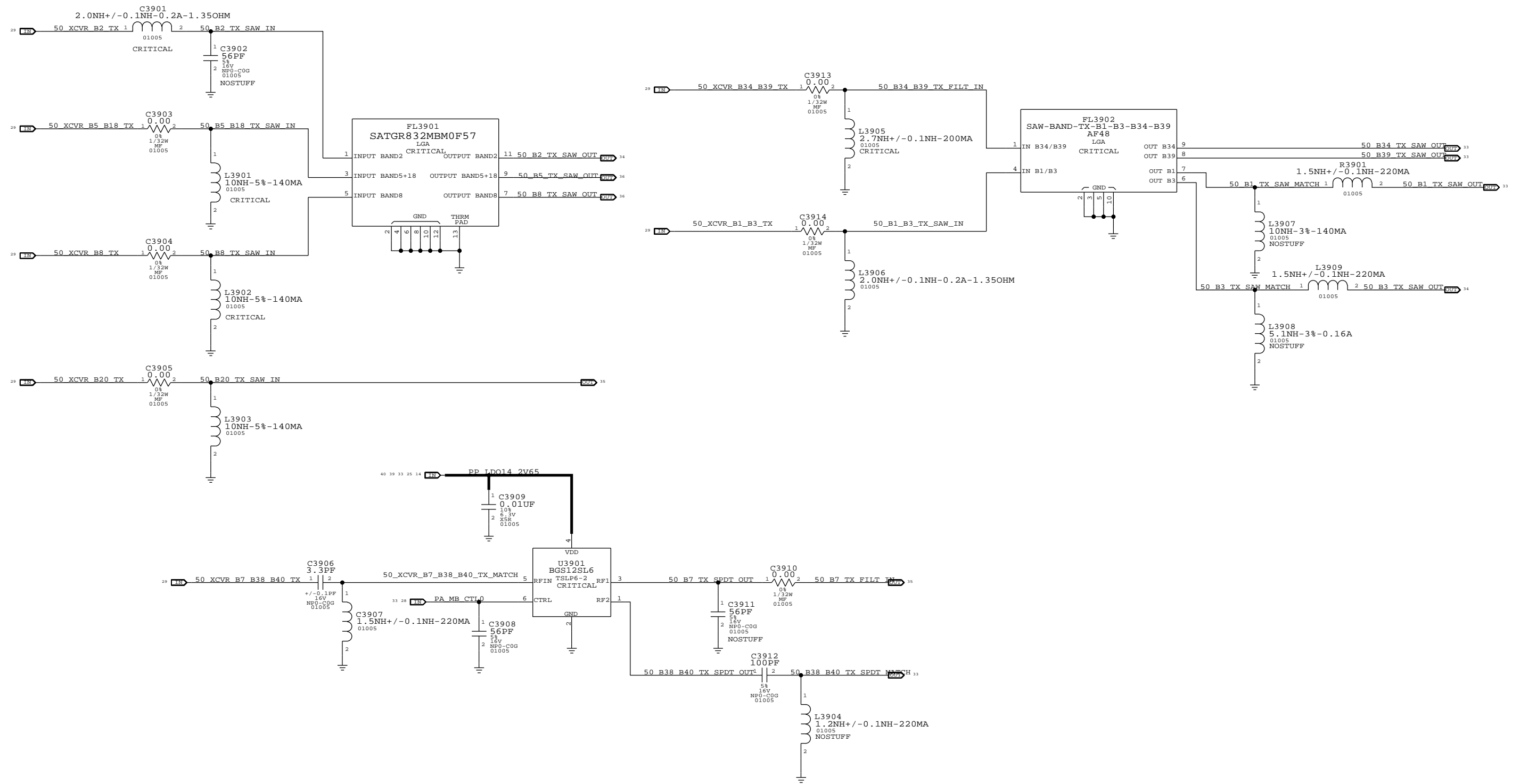
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CELL: RF TRANSCEIVER (2 OF 2)		
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BRANCH	PAGE	37 OF 121
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RX MATCHING



CELL: RX MATCHING		
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	SHEET 31 OF 54	

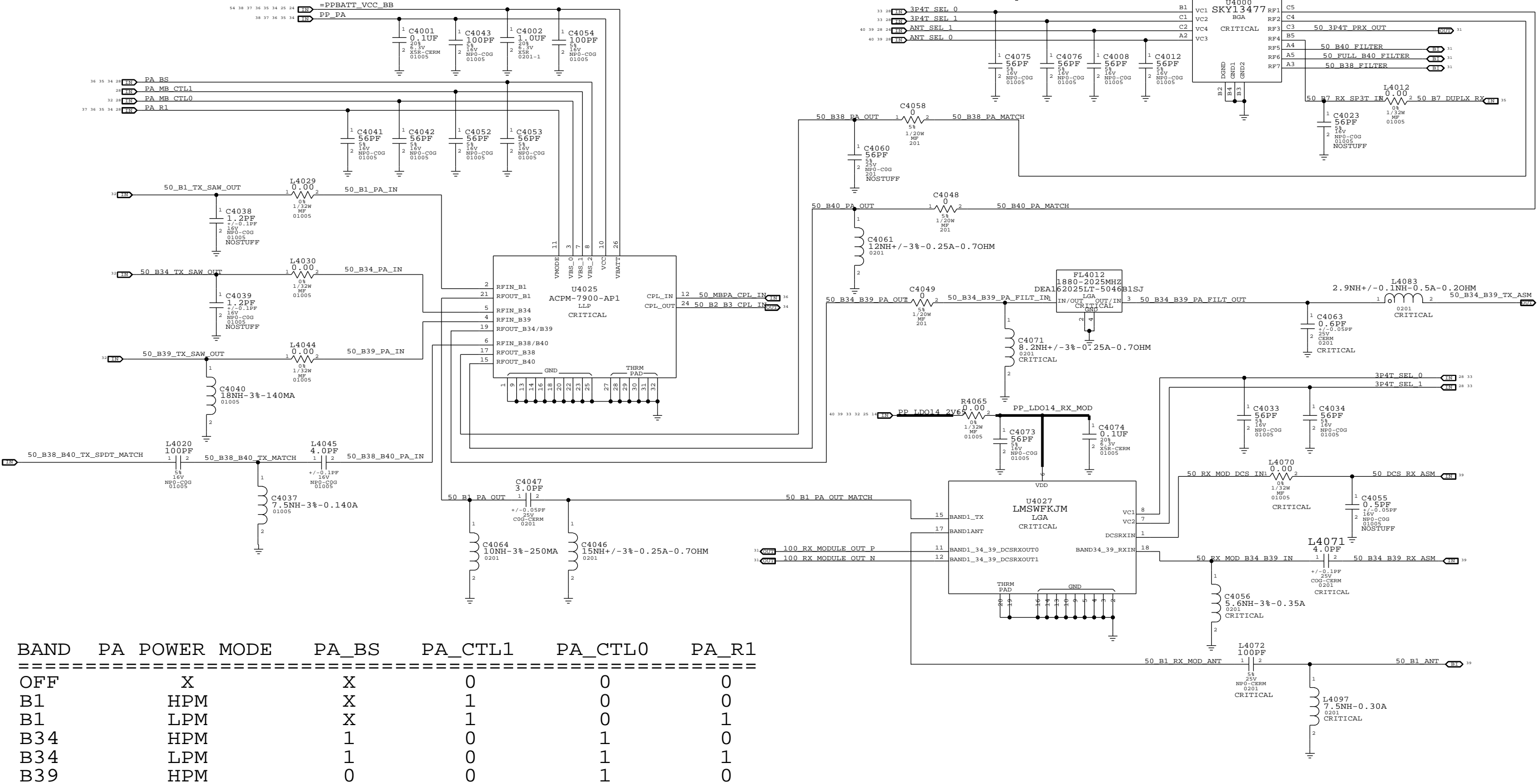
TX INTERSTAGE FILTERS



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BAND 1 / 34 / 39 / 38 / 40 TX

D
C
B
A

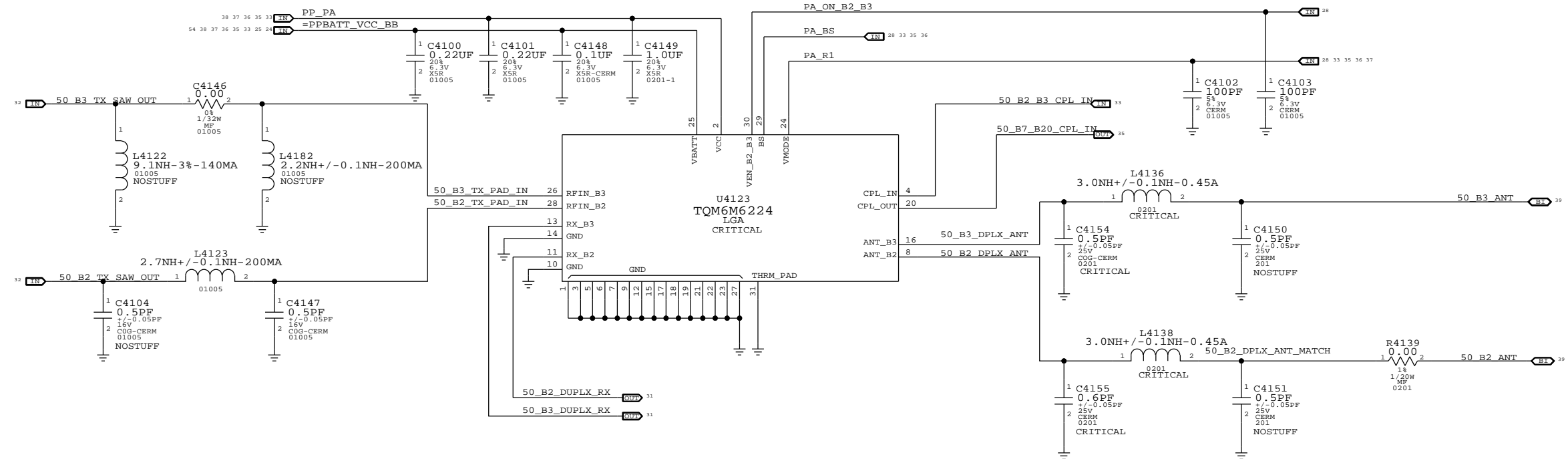


BAND	PA POWER MODE	PA_BS	PA_CTL1	PA_CTL0	PA_R1
OFF	X	X	0	0	0
B1	HPM	X	1	0	0
B1	LPM	X	1	0	1
B34	HPM	1	0	1	0
B34	LPM	1	0	1	1
B39	HPM	0	0	1	0
B39	LPM	0	0	1	1
B38	HPM	1	1	1	0
B38	LPM	1	1	1	1
B40	HPM	0	1	1	0
B40	LPM	0	1	1	1

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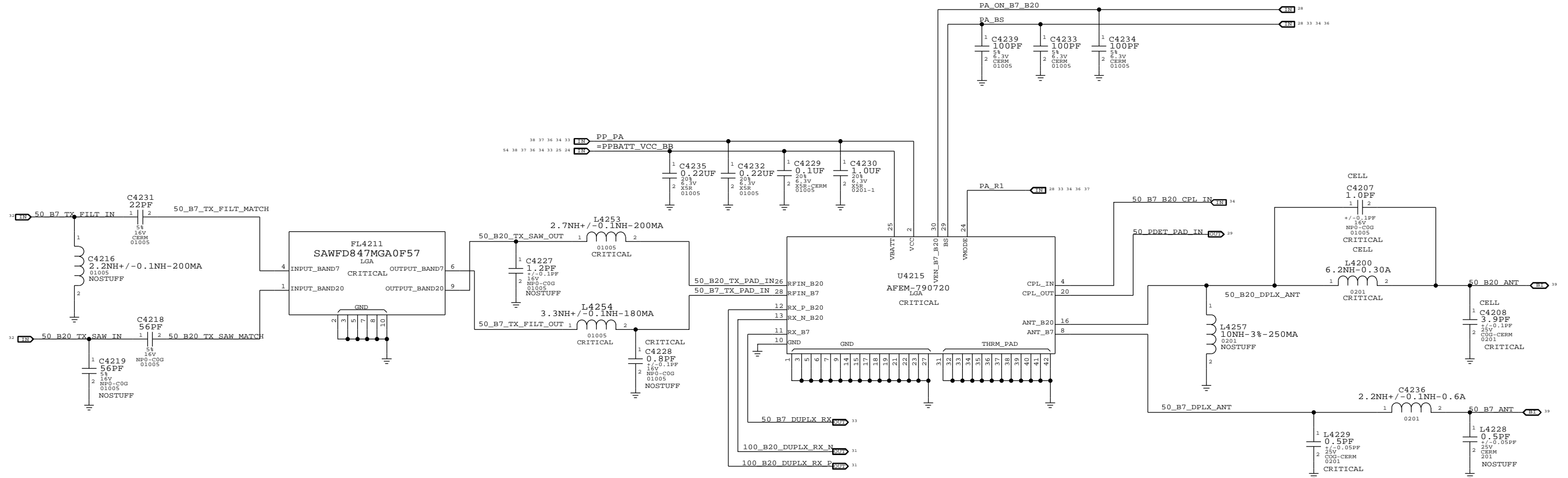
BAND 2/3 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B2_B3	PA_R1
OFF	X	X	0	X
B3	HPM	0	1	0
B3	LPM	0	1	1
B2	HPM	1	1	0
B2	LPM	1	1	1

PAGE TITLE CELL: BAND 2/3 PAD		
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	REVISION	A.0.0
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		PAGE 41 OF 121
		SHEET 34 OF 54

BAND 20/7 PAD

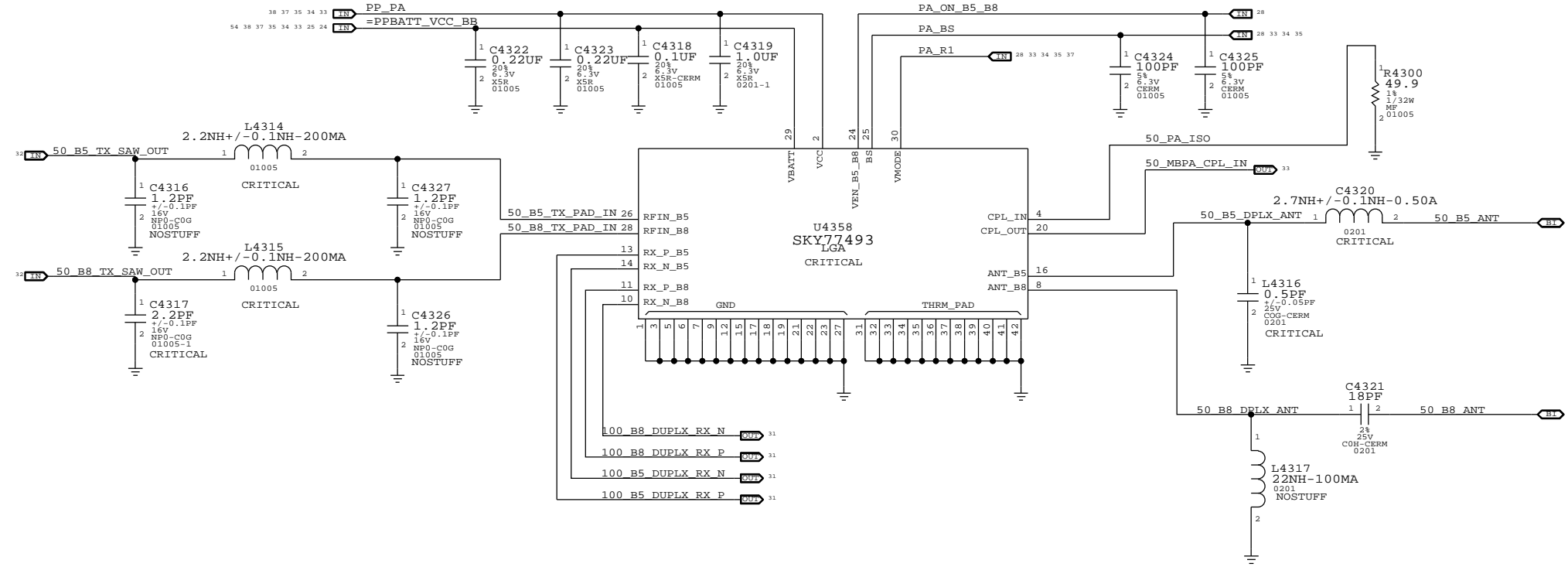


BAND	PA POWER MODE	PA_BS	PA_ON_B20_B7	PA_R1
OFF	X	X	0	X
B20	HPM	0	1	0
B20	LPM	0	1	1
B7	HPM	1	1	0
B7	LPM	1	1	1

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BAND 5/8 PAD



BAND	PA POWER MODE	PA_BS	PA_ON_B5_B8	PA_R1
OFF	X	X	0	X
B5	HPM	0	1	0
B5	LPM	0	1	1
B8	HPM	1	1	0
B8	LPM	1	1	1

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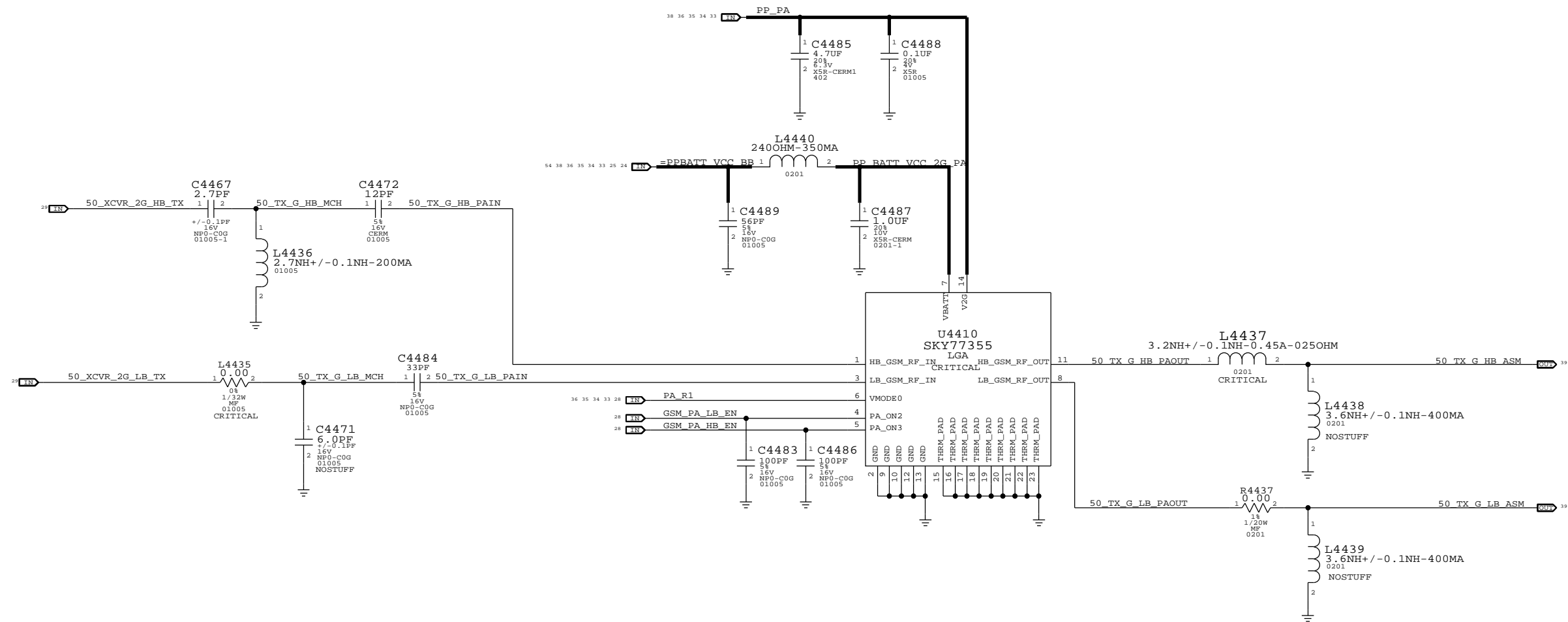
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2G PA

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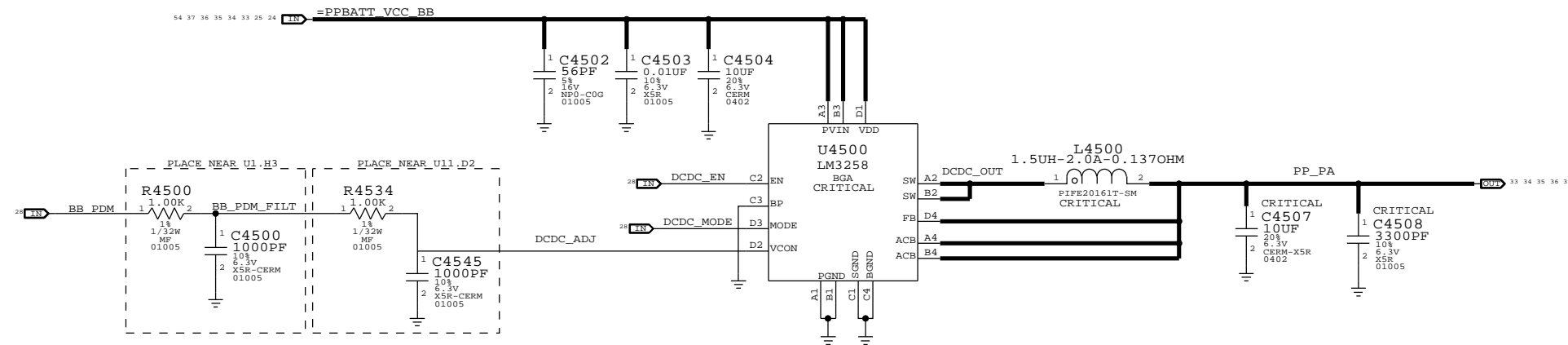
2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA_R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8



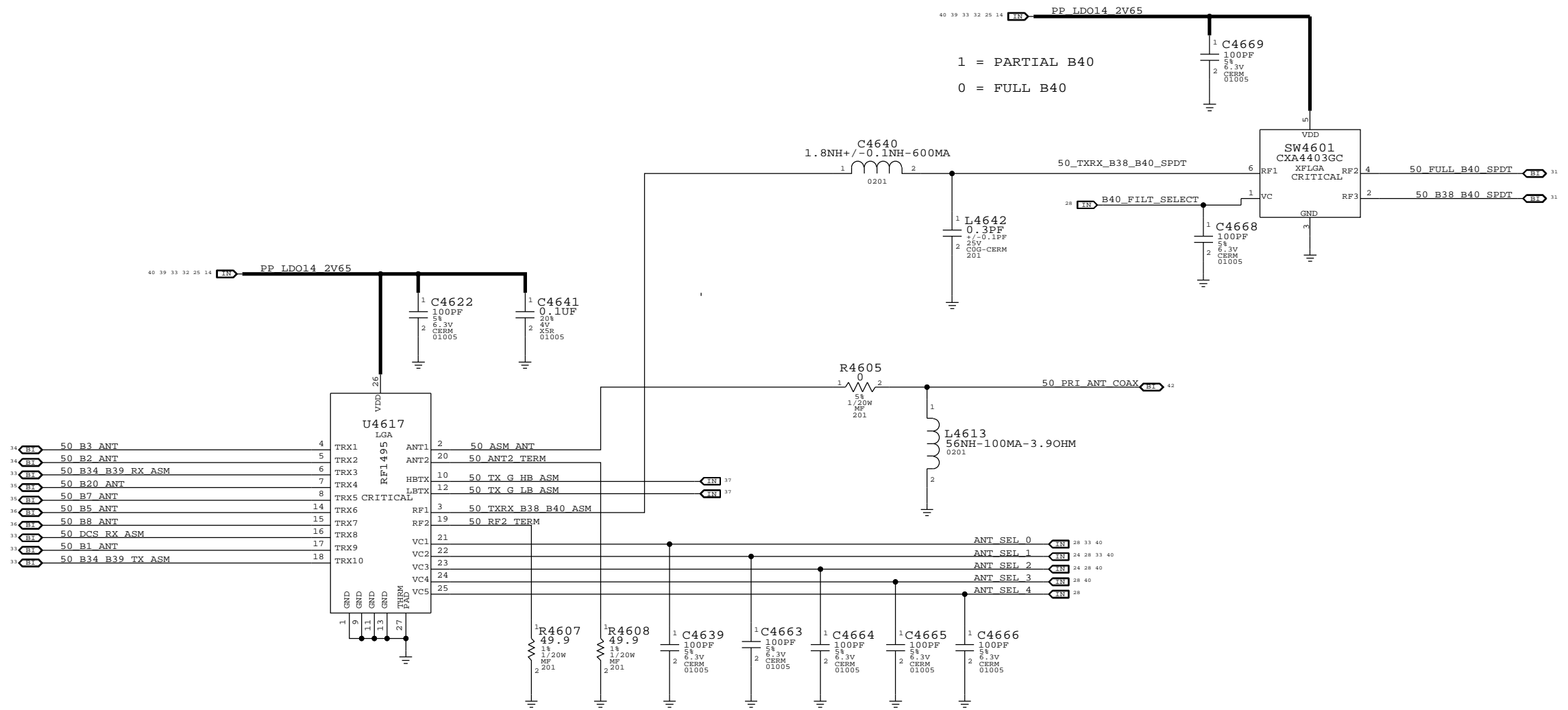
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	SHEET	37 OF 54
	SIZE	D

PA DC/DC CONVERTER



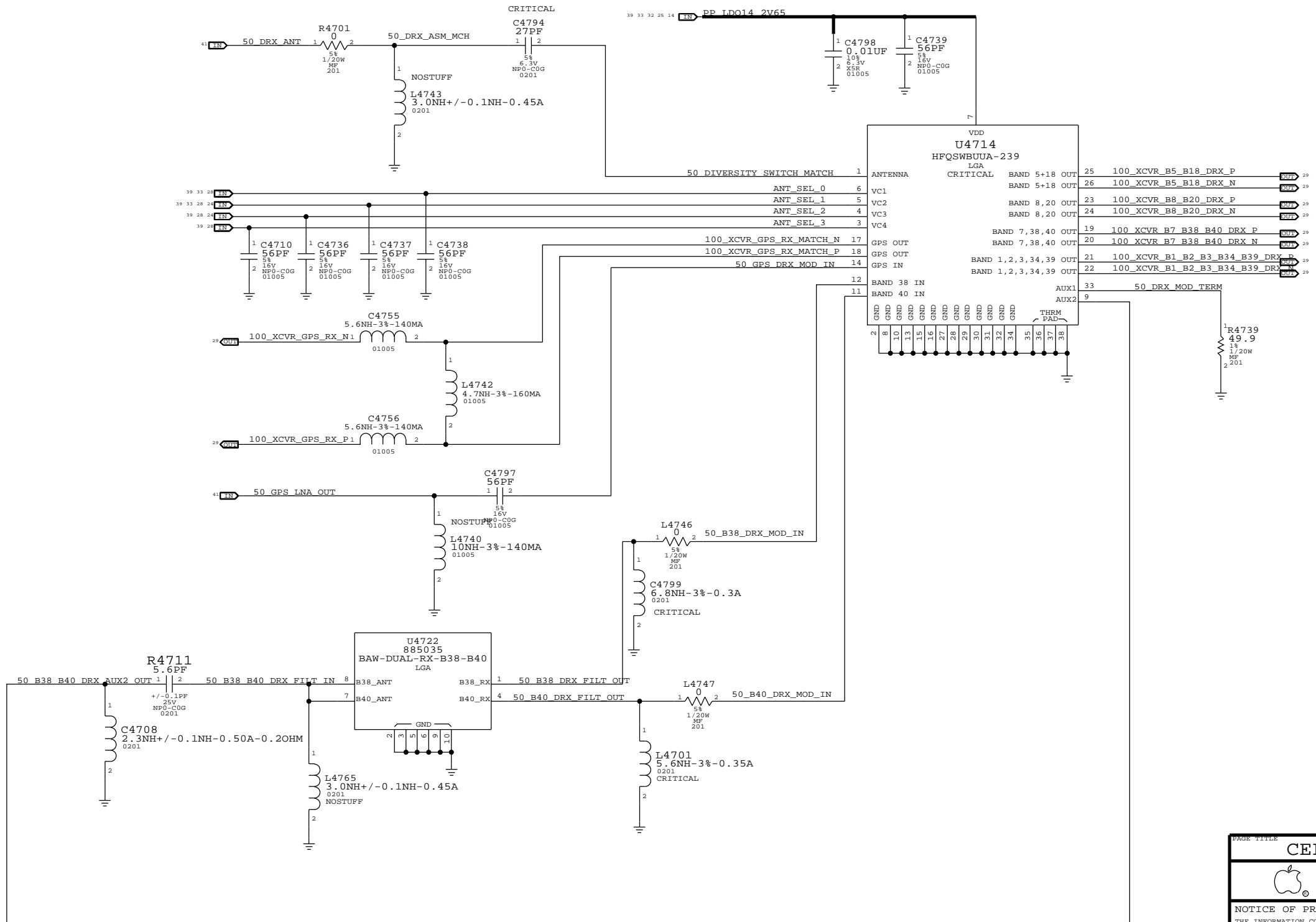
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PRIMARY ASM



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RX DIVERSITY

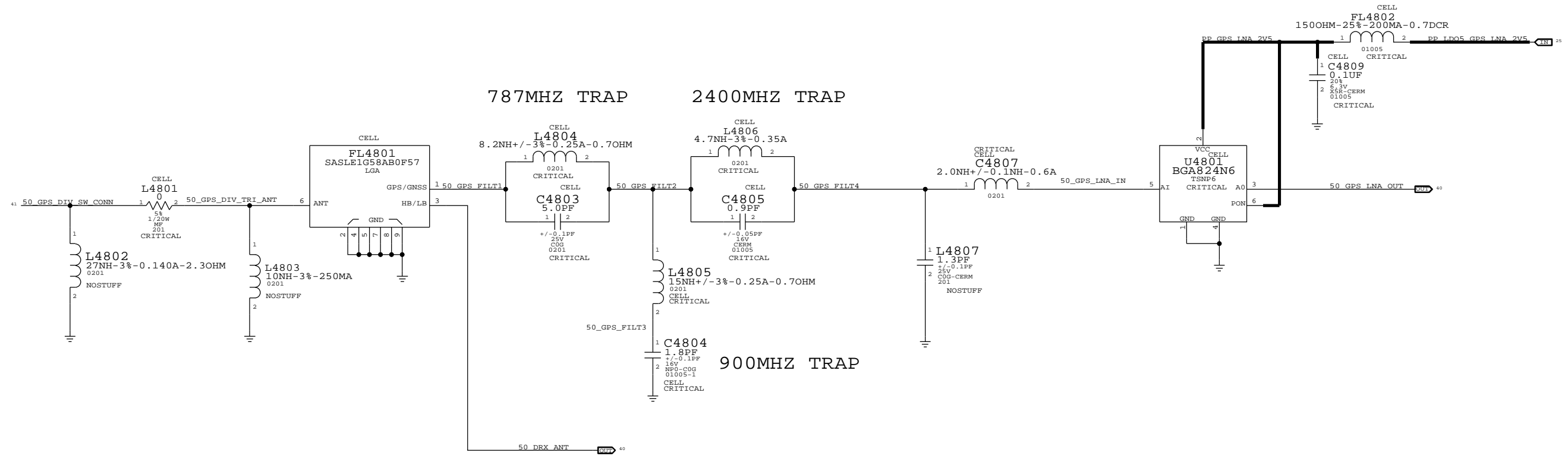


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PAGE TITLE		CELL: RX DIVERSITY	
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GPS

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GPS_DRX_ANT



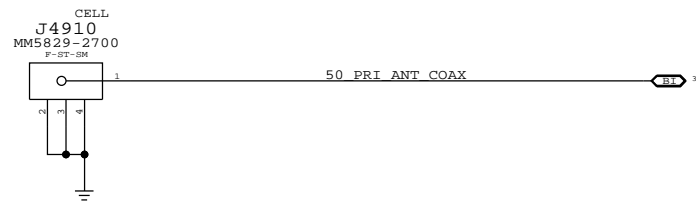
TOP MOUNT

TOP MOUNT

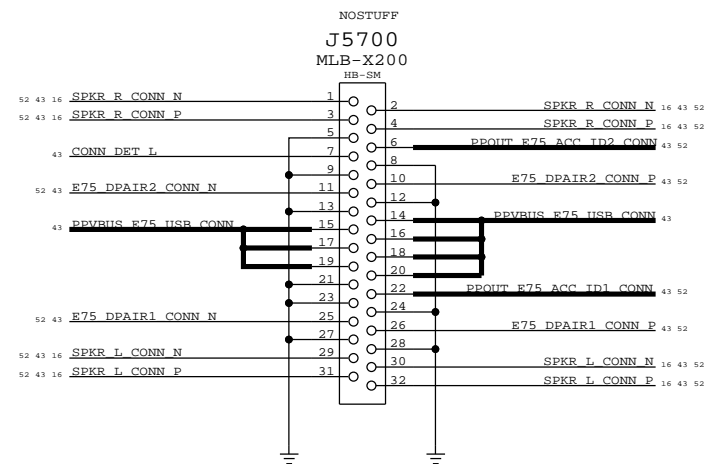
SYNC MASTER=RADIO MLB 87		SYNC DATE=10/29/2013	
CELL: GPS			
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ANTENNA FEEDS

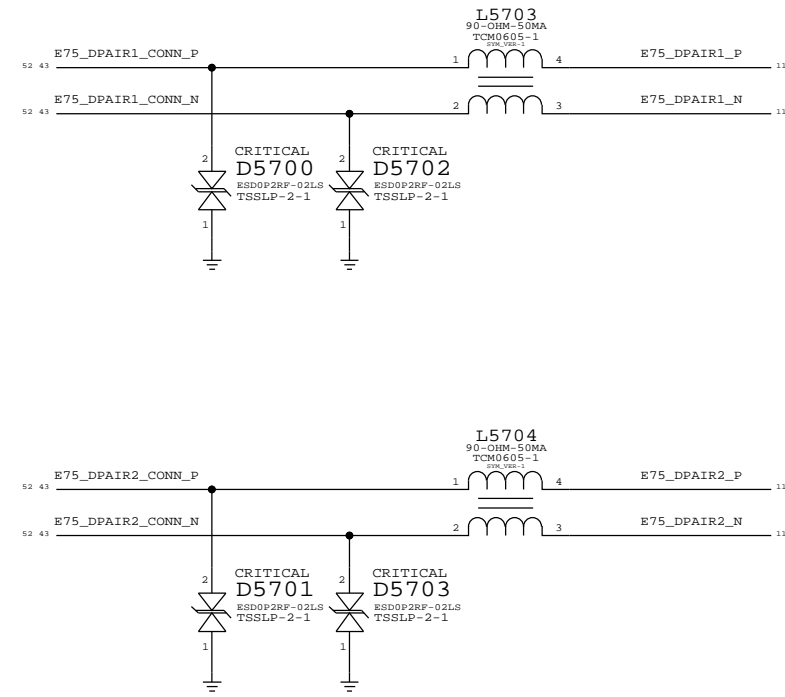
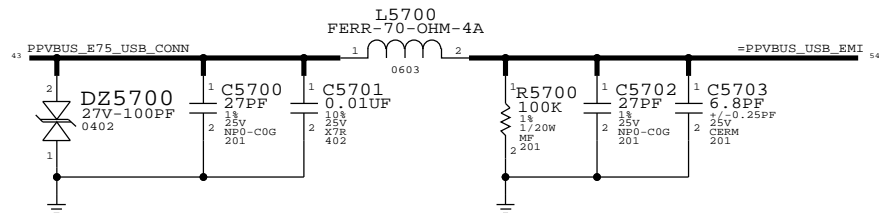
PRI_ANT COAX

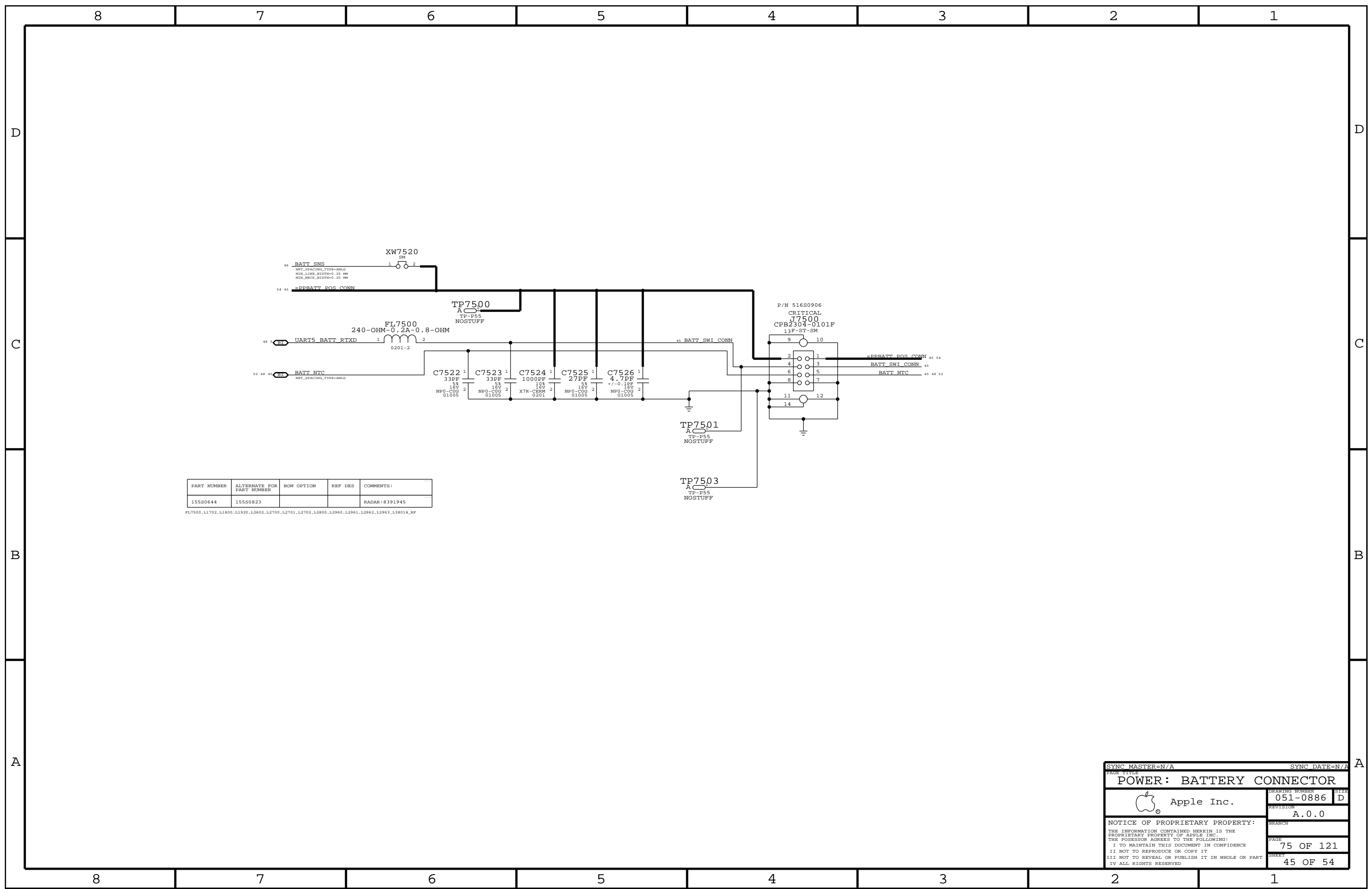


SYNC MASTER=RADIO MLB 87		SYNC DATE=10/29/2013	
CELL: ANTENNA FEEDS			
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		PAGE	49 OF 121
		SHEET	42 OF 54

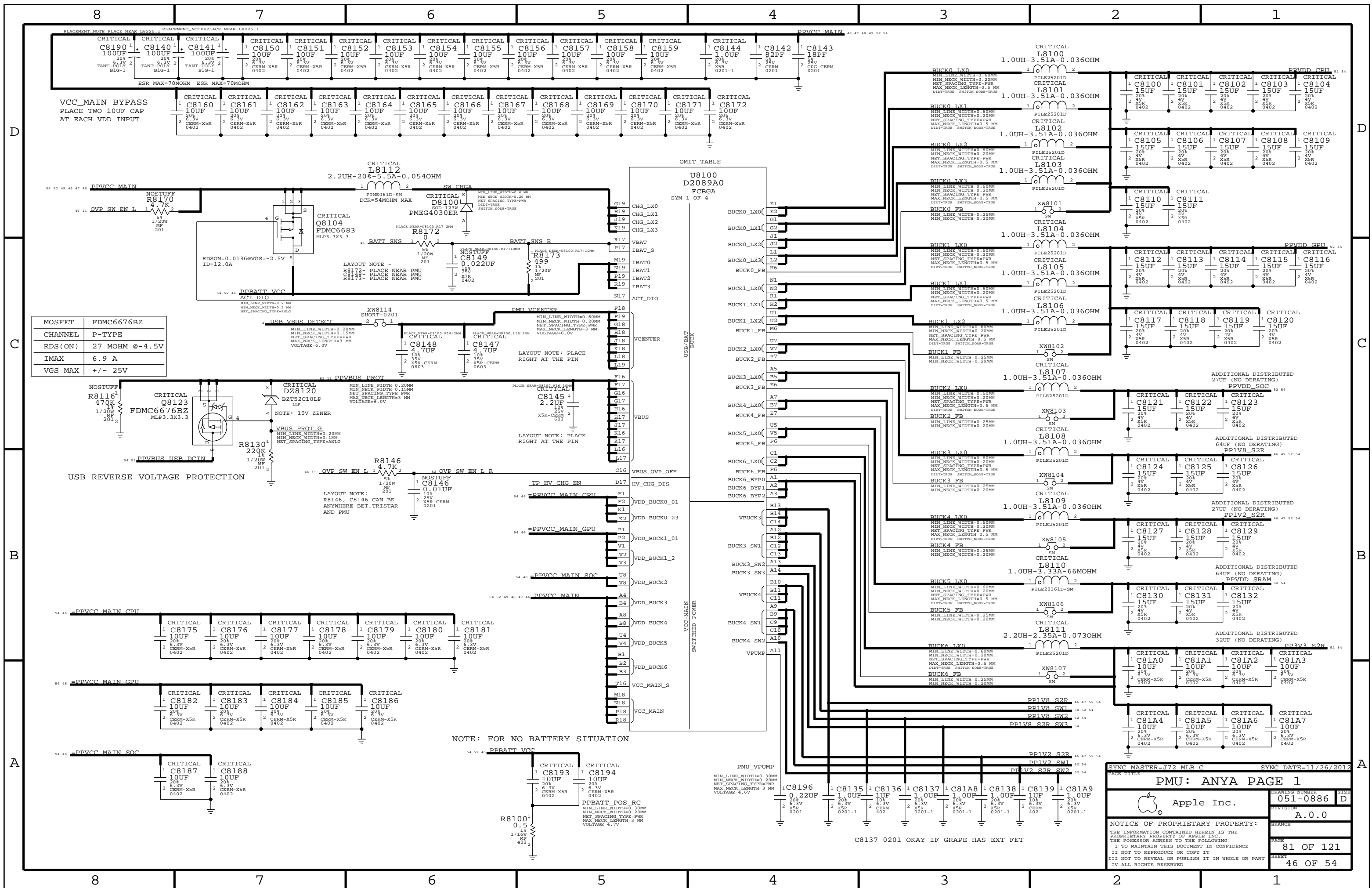


NOTE: SPKR_L_CONN_N AND SPKR_L_CONN_P WERE SWAPPED ON 5/22/12 PER RADAR #11526818





SYNC MASTER=N/A SYNC DATE=N/A
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MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

PPVCC MAIN CPU	C8175	C8176	C8177	C8178	C8179	C8180	C8181
PPVCC MAIN GPU	C8182	C8183	C8184	C8185	C8186		
PPVCC MAIN SOC	C8187	C8188					

U8100	D2089A0
FCBGA	
SYM	1 OF 4

CHG_LX0	G19
CHG_LX1	H19
CHG_LX2	J19
CHG_LX3	K19
VBAT	P17
IBAT_S	M19
IBAT0	N19
IBAT1	P19
IBAT2	R19
IBAT3	S19
ACT_DIO	N17
VCENTER	F18
	G18
	H18
	J18
	K18
	L18
	M18
	N18
	P18
	Q18
	R18
	S18
	T18
	U18
	V18
	W18
	X18
	Y18
	Z18

BUCK0_LX0	E1
BUCK0_LX1	G1
BUCK0_LX2	J1
BUCK0_LX3	L1
BUCK0_FB	H6
BUCK1_LX0	N1
BUCK1_LX1	R1
BUCK1_LX2	U1
BUCK1_FB	M6
BUCK2_LX0	U7
BUCK2_FB	P7
BUCK3_LX0	A5
BUCK3_FB	E6
BUCK4_LX0	A7
BUCK4_FB	E7
BUCK5_LX0	U5
BUCK5_FB	P6
BUCK6_LX0	C1
BUCK6_FB	F6
BUCK6_BY0	A1
BUCK6_BY1	A2
BUCK6_BY2	A3
VBUCK3	B13
	B14
	C14
	A12
	B12
	C12
	C13
	A13
	A14
BUCK3_SW1	B10
BUCK3_SW2	B11
BUCK3_SW3	C11
	A9
	B9
	C9
	A10
BUCK4_SW1	B10
BUCK4_SW2	B11
	C11
	A9
	B9
	C9
	A10
VPUMP	A11

CHG_LX0	G19
CHG_LX1	H19
CHG_LX2	J19
CHG_LX3	K19
VBAT	P17
IBAT_S	M19
IBAT0	N19
IBAT1	P19
IBAT2	R19
IBAT3	S19
ACT_DIO	N17
VCENTER	F18
	G18
	H18
	J18
	K18
	L18
	M18
	N18
	P18
	Q18
	R18
	S18
	T18
	U18
	V18
	W18
	X18
	Y18
	Z18

BUCK0_LX0	E1
BUCK0_LX1	G1
BUCK0_LX2	J1
BUCK0_LX3	L1
BUCK0_FB	H6
BUCK1_LX0	N1
BUCK1_LX1	R1
BUCK1_LX2	U1
BUCK1_FB	M6
BUCK2_LX0	U7
BUCK2_FB	P7
BUCK3_LX0	A5
BUCK3_FB	E6
BUCK4_LX0	A7
BUCK4_FB	E7
BUCK5_LX0	U5
BUCK5_FB	P6
BUCK6_LX0	C1
BUCK6_FB	F6
BUCK6_BY0	A1
BUCK6_BY1	A2
BUCK6_BY2	A3
VBUCK3	B13
	B14
	C14
	A12
	B12
	C12
	C13
	A13
	A14
BUCK3_SW1	B10
BUCK3_SW2	B11
BUCK3_SW3	C11
	A9
	B9
	C9
	A10
BUCK4_SW1	B10
BUCK4_SW2	B11
	C11
	A9
	B9
	C9
	A10
VPUMP	A11

CHG_LX0	G19
CHG_LX1	H19
CHG_LX2	J19
CHG_LX3	K19
VBAT	P17
IBAT_S	M19
IBAT0	N19
IBAT1	P19
IBAT2	R19
IBAT3	S19
ACT_DIO	N17
VCENTER	F18
	G18
	H18
	J18
	K18
	L18
	M18
	N18
	P18
	Q18
	R18
	S18
	T18
	U18
	V18
	W18
	X18
	Y18
	Z18

BUCK0_LX0	E1
BUCK0_LX1	G1
BUCK0_LX2	J1
BUCK0_LX3	L1
BUCK0_FB	H6
BUCK1_LX0	N1
BUCK1_LX1	R1
BUCK1_LX2	U1
BUCK1_FB	M6
BUCK2_LX0	U7
BUCK2_FB	P7
BUCK3_LX0	A5
BUCK3_FB	E6
BUCK4_LX0	A7
BUCK4_FB	E7
BUCK5_LX0	U5
BUCK5_FB	P6
BUCK6_LX0	C1
BUCK6_FB	F6
BUCK6_BY0	A1
BUCK6_BY1	A2
BUCK6_BY2	A3
VBUCK3	B13
	B14
	C14
	A12
	B12
	C12
	C13
	A13
	A14
BUCK3_SW1	B10
BUCK3_SW2	B11
BUCK3_SW3	C11
	A9
	B9
	C9
	A10
BUCK4_SW1	B10
BUCK4_SW2	B11
	C11
	A9
	B9
	C9
	A10
VPUMP	A11

CHG_LX0	G19
CHG_LX1	H19
CHG_LX2	J19
CHG_LX3	K19
VBAT	P17
IBAT_S	M19
IBAT0	N19
IBAT1	P19
IBAT2	R19
IBAT3	S19
ACT_DIO	N17
VCENTER	F18
	G18
	H18
	J18
	K18
	L18
	M18
	N18
	P18
	Q18
	R18
	S18
	T18
	U18
	V18
	W18
	X18
	Y18
	Z18

BUCK0_LX0	E1
BUCK0_LX1	G1
BUCK0_LX2	J1
BUCK0_LX3	L1
BUCK0_FB	H6
BUCK1_LX0	N1
BUCK1_LX1	R1
BUCK1_LX2	U1
BUCK1_FB	M6
BUCK2_LX0	U7
BUCK2_FB	P7
BUCK3_LX0	A5
BUCK3_FB	E6
BUCK4_LX0	A7
BUCK4_FB	E7
BUCK5_LX0	U5
BUCK5_FB	P6
BUCK6_LX0	C1
BUCK6_FB	F6
BUCK6_BY0	A1
BUCK6_BY1	A2
BUCK6_BY2	A3
VBUCK3	B13
	B14
	C14
	A12
	B12
	C12
	C13
	A13
	A14
BUCK3_SW1	B10
BUCK3_SW2	B11
BUCK3_SW3	C11
	A9
	B9
	C9
	A10
BUCK4_SW1	B10
BUCK4_SW2	B11
	C11
	A9
	B9
	C9
	A10
VPUMP	A11

SYNC MASTER=J72 MLB C SYNC DATE=11/26/2012

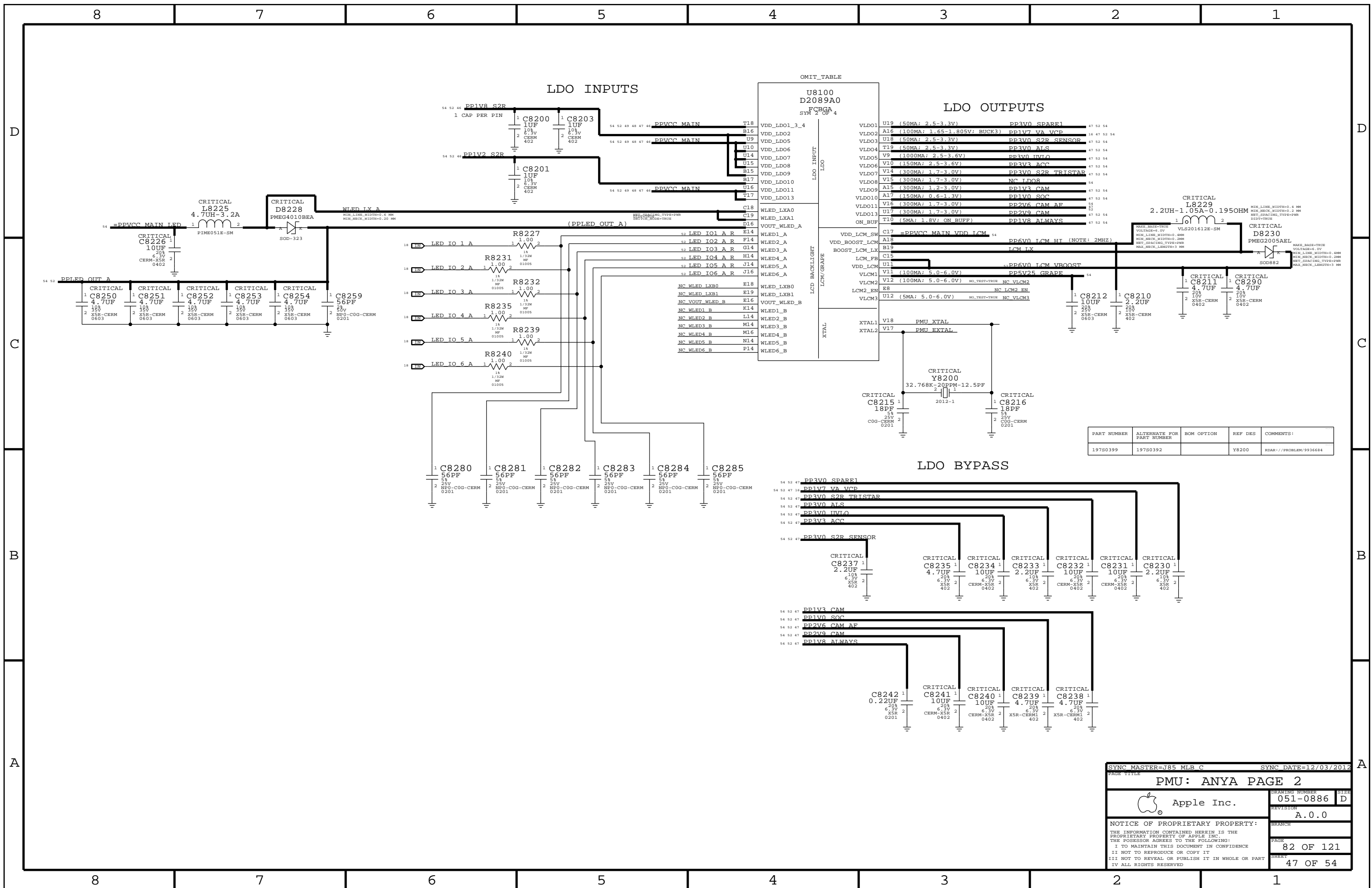
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C8137 0201 OKAY IF GRAPE HAS EXT FET



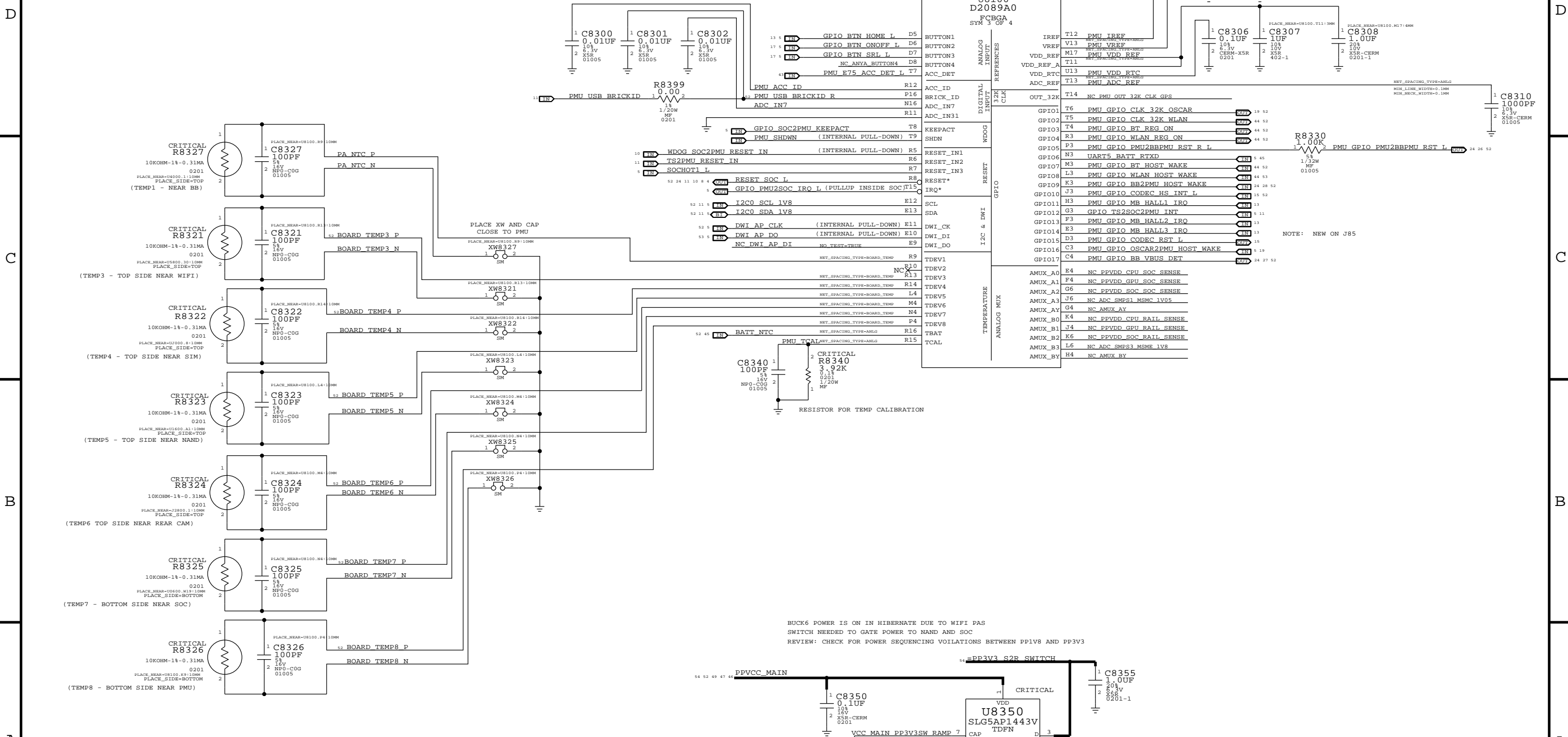
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0399	197S0392		Y8200	RDAR://PROBLEM/9936684

SYNC MASTER=J85 MLB C		SYNC DATE=12/03/2012	
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REVIEW: VERIFY NC ON TDEV2 IS OK

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0739	138S0706		C8308	

I2C ADDRESS: 0111100X (0X78)



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
107S0150	107S0208	R8321, R8322	R8323, R8324	RDAR: // PROBLEM/8380167
118S0764	118S0717		R8340	RDAR: // PROBLEM/8380167

BUCK6 POWER IS ON IN HIBERNATE DUE TO WIFI PAS
 SWITCH NEEDED TO GATE POWER TO NAND AND SOC
 REVIEW: CHECK FOR POWER SEQUENCING VIOLATIONS BETWEEN PP1V8 AND PP3V3

SYNC MASTER=J72 MLB C SYNC DATE=11/26/2012

PMU: ANYA PAGE 3

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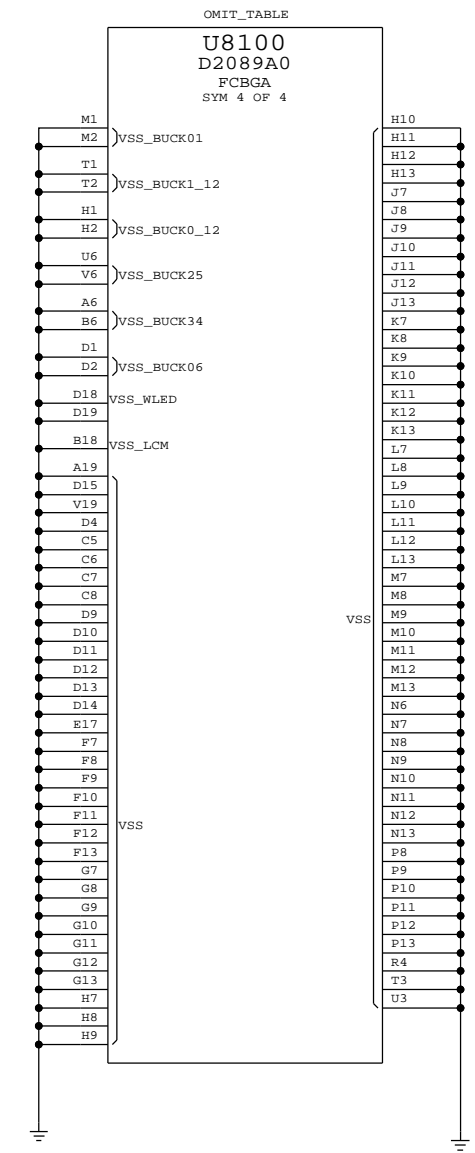
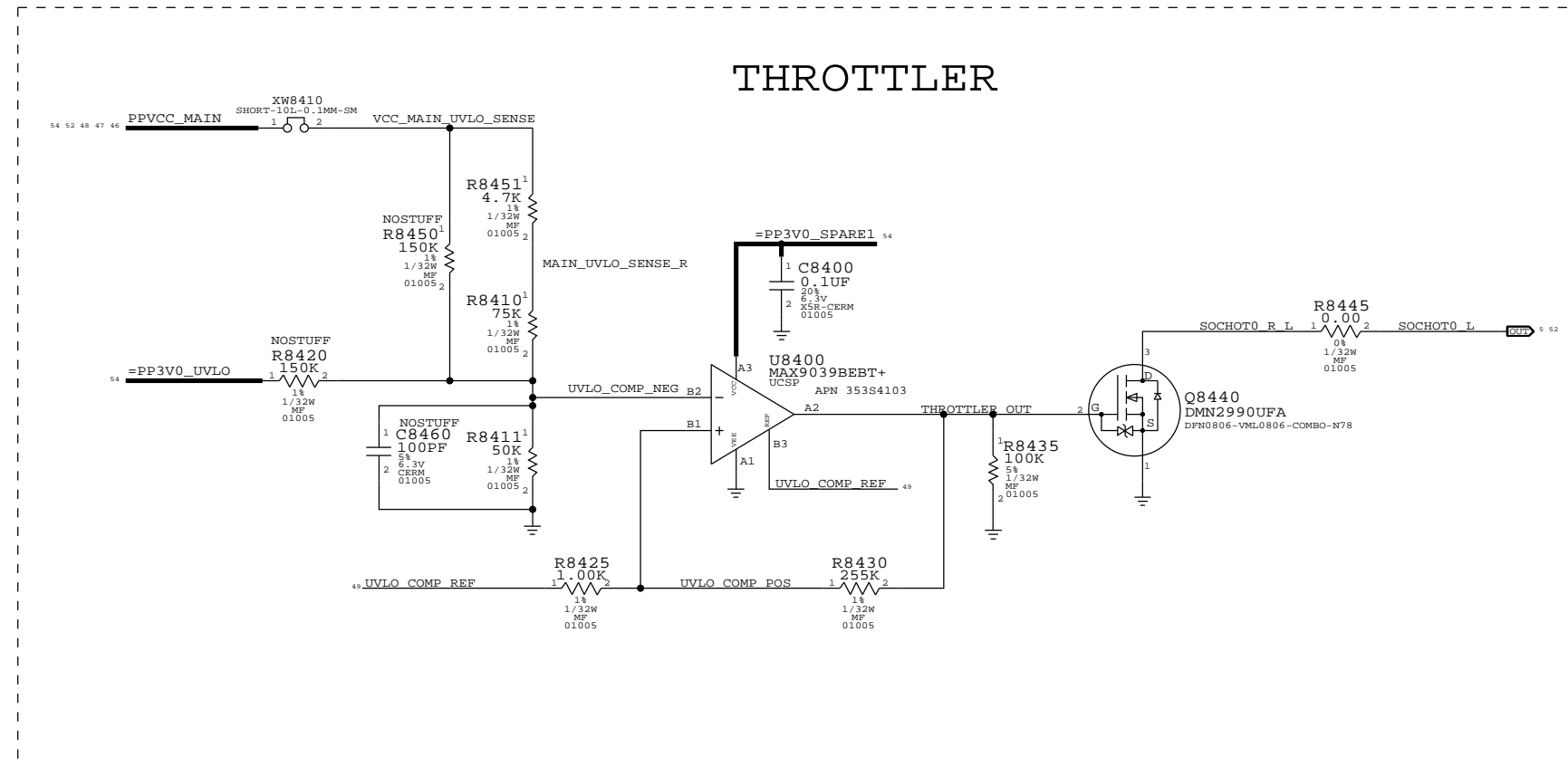
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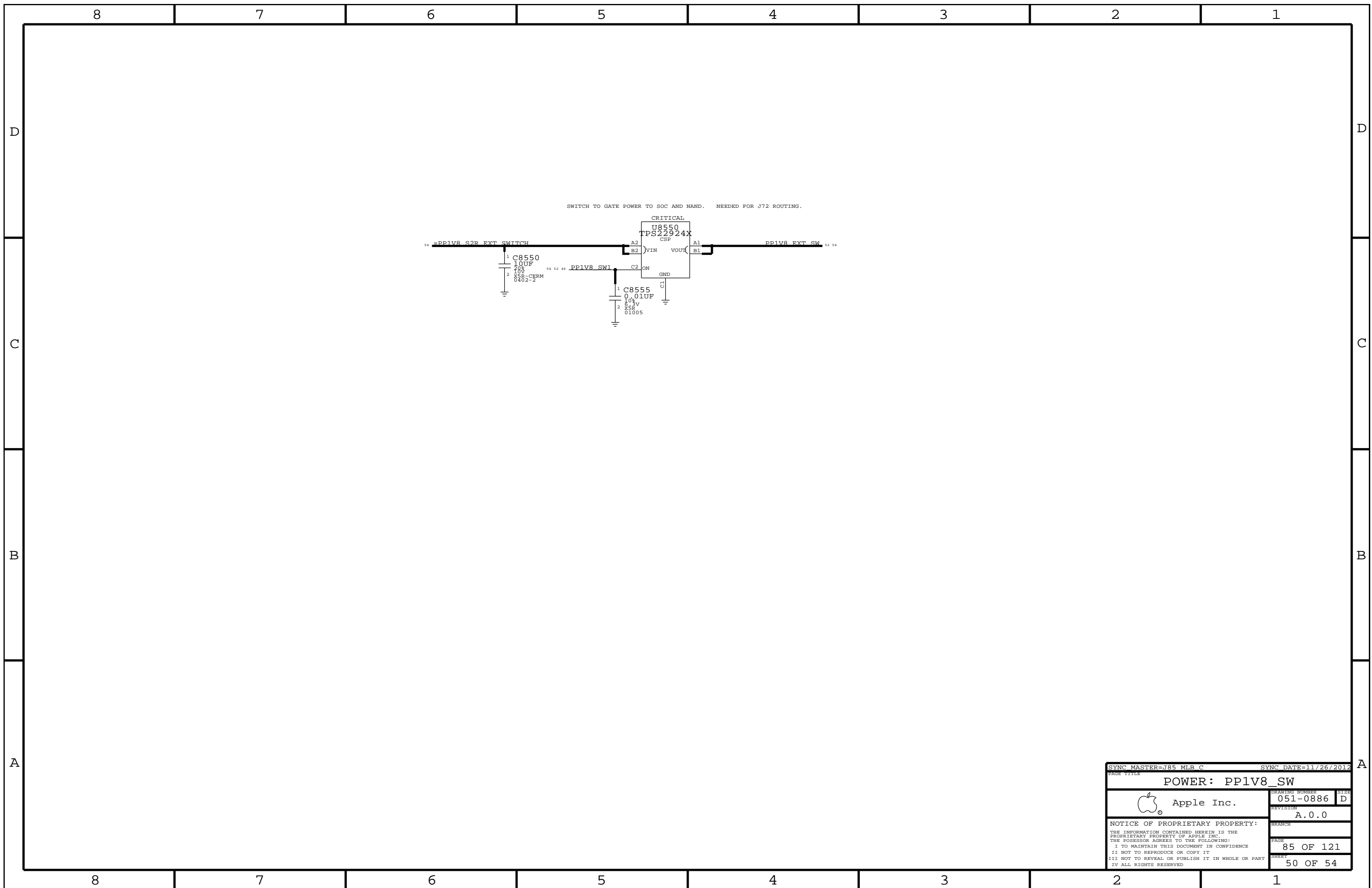
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SYNC MASTER=J85 MLB C		SYNC DATE=11/26/2012	
POWER: PP1V8_SW			
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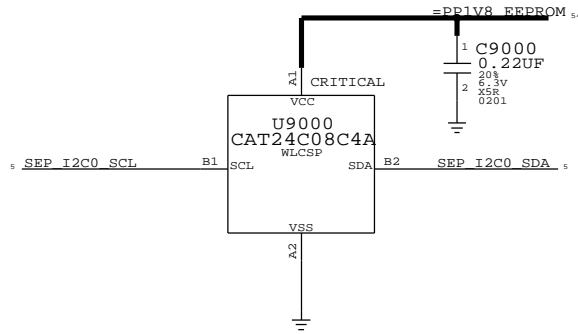
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DEBUG

TP9002
TP-P55

SEP EEPROM

UNPROGRAMMED P/N: 335S0894



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TP9300 GPIO CODEC IRO L 5 15
 A TP9304 PMU GPIO CODEC HS INT L 15 48
 A TP9303 BATT NTC 45 48
 TP9305 PPLED OUT A 47 54
 A TP9396 PP3V0 UVLO 47 54
 TP9397 PP3V0 SPARE1 47 54
 A TP9398 SOCHOT0 L 5 49
 TP9312 BOARD TEMP3 P 48
 A TP9313 BOARD TEMP4 P 48
 TP9314 BOARD TEMP5 P 48
 A TP9315 BOARD TEMP6 P 48
 TP9316 BOARD TEMP7 P 48
 A TP9317 BOARD TEMP8 P 48
 TP9318 CLK 32K SOC2CUMULUS 5 13
 TP9320 CODEC HP DET R 15
 A TP9321 CODEC HP HS3 15
 TP9322 CODEC HP HS3 REF 15
 A TP9323 CODEC HP HS4 15
 A TP9324 CODEC HP HS4 REF 15
 TP9325 CODEC HP LEFT 15
 A TP9326 CODEC HP RIGHT 15
 TP9328 DISPLAY SYNC R 13
 A TP9329 DWI AP CLK 5 48
 TP9330 E75 DPAIR1 CONN N 43
 A TP9331 E75 DPAIR1 CONN P 43
 TP9332 E75 DPAIR2 CONN N 43
 A TP9333 E75 DPAIR2 CONN P 43
 TP9334 FMIO CE0 L 6 12
 A TP9335 FMIO CE0 L 6 12
 TP9336 GND
 A TP9337 GND AUDIO CODEC 15
 TP9338 GPIO BTN HOME FILT L 13
 A TP9339 GPIO BTN ONOFF L FILT 17
 TP9340 GPIO BTN SRL L FILT 17
 A TP9341 GPIO BTN VOL DOWN L FILT 17
 TP9342 GPIO BTN VOL UP L FILT 17
 A TP9343 GPIO FORCE DFU 5
 TP9344 GPIO GRAPE IRO L 5 13
 A TP9345 GPIO GRAPE RST L 5 13
 TP9346 GPIO SOC2BB WAKE MODEM 5 28
 A TP9347 GPIO SPKAMP KEEPALIVE 5 16
 TP9348 I2C0 SCL 1V8 5 11 48
 A TP9349 I2C0 SDA 1V8 5 11 48
 TP9350 I2C2 SCL 1V8 5 16
 A TP9351 I2C2 SDA 1V8 5 16
 TP9352 ISP0 CAM REAR CLK 7 23
 A TP9353 ISP0 CAM REAR SCL 7 23
 TP9354 ISP0 CAM REAR SDA 7 23
 A TP9355 ISP0 CAM REAR SHUTDOWN L 7 23
 TP9356 ISP1 CAM FRONT CLK 7 20
 A TP9357 ISP1 CAM FRONT SCL 7 20
 TP9358 ISP1 CAM FRONT SDA 7 20
 A TP9359 ISP1 CAM FRONT SHUTDOWN L 7 20
 TP9360 JTAG SOC SEL 4 10
 A TP9361 JTAG SOC TCK 4 11
 TP9362 JTAG SOC TDI 4
 A TP9363 JTAG SOC TMS 4 11
 TP9364 JTAG SOC TRST L 4 10
 A TP9365 JTAG WLAN SEL 44
 TP9366 OSCAR2RADIO CONTEXT A 19 28 44
 A TP9367 OSCAR2RADIO CONTEXT B 19 28 44
 TP9368 WLAN TX BLANK 28 44
 A TP9369 LAT SW1 CTL 14 24 28
 TP9370 LAT SW2 CTL 14 24 28
 A TP9371 LED IO1 A R 47
 TP9372 LED IO2 A R 47
 A TP9373 LED IO3 A R 47
 TP9374 LED IO4 A R 47
 A TP9375 LED IO5 A R 47
 TP9376 LED IO6 A R 47
 A TP9377 MIKEY TS N 11 15
 A TP9378 MIKEY TS P 11 15

TP9380 OVP SW EN L R 46
 A TP9382 PMU GPIO BT HOST WAKE 44 48
 A TP9383 PMU GPIO BT REG ON 44 48
 TP9384 PMU GPIO CLK 32K OSCAR 19 48
 A TP9385 PMU GPIO CLK 32K WLAN 44 48
 TP9387 PMU USB BRICKID R 48
 A TP9388 PP1V0 SOC 47 54
 TP9389 PP1V2 S2R 46 47 54
 A TP9390 PP1V2 S2R SW2 46 54
 TP9391 PP1V2 SW1 46 54
 TP9393 PP1V7 VA VCP 16 47 54
 A TP9395 PP1V8 ALWAYS 47 54
 TP9320 PP1V8 EXT SW 50 54
 A TP9321 PP1V8 GRAPE FILT 13
 TP9322 PP1V8 GRAPE SW 13
 A TP9323 PP1V8 PLL SOC F 4
 A TP9324 PP1V8 S2R 46 47 54
 TP9326 PP1V8 S2R SW3 COMP 54
 A TP9327 PP1V8 SW1 46 50 54
 TP9328 PP1V8 SW2 46 54
 A TP9329 PP1V8 XTAL 8
 TP9330 PP2V6 CAM AF 47 54
 A TP9338 PP3V0 S2R HALL FILT 13
 TP9340 PP3V0 S2R SENSOR 47 54
 A TP9341 PP3V0 S2R TRISTAR 47 54
 TP9343 PP3V3 ACC 47 54
 A TP9344 PP3V3 S2R 46 54
 TP9345 PP3V3 SW 48 54
 A TP9346 PP5V25 GRAPE FILT 13
 TP9348 PP6V0 LCM VBOOST 47
 A TP9349 PPBATT VCC 46 54
 TP9350 PPLED BACK REG A 18
 TP9351 PPROUT E75 ACC ID1 CONN 43
 A TP9352 PPROUT E75 ACC ID2 CONN 43
 TP9353 PPVBUS PROT 11 46
 A TP9354 PPVBUS USB DCIN 46 54
 TP9355 PPVCC MAIN 46 47 48 49 54
 A TP9356 PPVCC MAIN LCD SW CONN 18
 TP9357 PPVDD CPU 46 54
 A TP9358 PPVDD GPU 46 54
 TP9359 PPVDD SOC 46 54
 A TP9360 PPVDD SRAM 46 54

TP93G4 PP SMPS4 RF2 2V05 25 30
 A TP93G9 SOC TESTMODE 4 10
 TP93H1 SPI1 GRAPE CS L 5 13
 A TP93H2 SPI1 GRAPE MISO 5 13
 TP93H3 SPI1 GRAPE MOSI 5 13
 A TP93H4 SPI1 GRAPE SCLK R 13
 TP93H5 SPKR L CONN N 16 43
 A TP93H6 SPKR L CONN P 16 43
 TP93H7 SPKR R CONN N 16 43
 A TP93H8 SPKR R CONN P 16 43
 TP93I1 TP JTAG SOC TDO 4
 A TP93I2 TP JTAG WLAN TCK 44
 TP93I3 TP JTAG WLAN TRST L 44
 A TP93I4 UART0 SOC RXD 5 11
 A TP93I5 UART0 SOC TXD 5 11
 TP93I6 UART3 BB2SOC TX 5 11 24 28
 A TP93I7 UART3 SOC2BB TX 5 11 24 28
 TP93I8 UART6 TS ACC RXD 5 11
 A TP93I9 UART6 TS ACC TXD 5 11
 TP93J0 USB SOC N 4 11
 A TP93J1 USB SOC P 4 11
 TP93J9 PP3V0 ALS 47 54
 A TP93JA PP2V9 CAM 47 54
 A TP93JB PP1V3 CAM 47 54
 TP93JC PMU GPIO WLAN REG ON 44 48

RF TEST POINTS

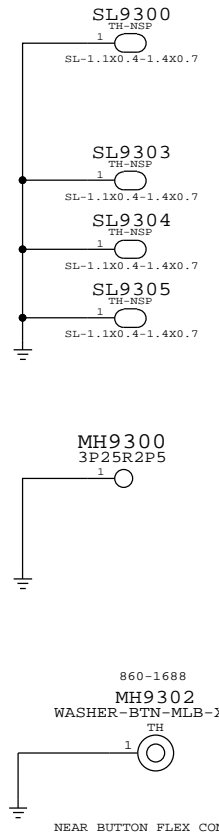
TP93G1 PP SMPS1 MSME 1V05 25 27
 A TP93G2 PP SMPS3 MSME 1V8 24 25 27 28 30
 TP93G5 PP SMPS5 DSP 1V05 25
 A TP93H5 PP LDO1 25
 TP93H9 TP BB TEST MODE 0 27
 TP93I0 TP BB TEST MODE 1 27
 A TP93J0 SIMCRD RST CONN 10 24 28
 A TP93J5 SIMCRD CLK CONN 10 24 28
 TP93K7 SIMCRD IO CONN 10 24 28
 A TP93K8 SIM TRAY DETECT 10 24 28
 TP93F3 PP LDO6 RUM 1V8 10 24 25 27
 A TP93J7 GPIO SOC2BB RADIO ON L 5 24 26
 TP93J3 GPIO SOC2BB RST L 5 24 26
 A TP93J4 PMU GPIO PMU2BBPMU RST L 24 26 48
 TP93B1 PMU GPIO BB2PMU HOST WAKE 24 28 48
 A TP93J5 PS HOLD PMIC 24 26
 TP9327 DEBUG RST L 24 27
 A TP9306 BB JTAG RTCLK 24 27
 TP9307 BB JTAG TCK 5 24 27
 A TP9308 BB JTAG TDI 5 24 27
 TP9309 BB JTAG TDO 5 24 27
 A TP9310 BB JTAG TMS 5 24 27
 TP9311 BB JTAG TRST L 5 24 27
 A TP93J6 USB BB N 11 24 53
 TP93J7 USB BB P 11 24 53
 A TP93G6 RESET SOC L 4 8 10 11 24 48
 TP93J8 PMU GPIO BB VBUS DET 24 27 48

STANDOFFS: P/N 860-1657
 STD9300
 STDOFF-3.3X1.8R1.28H-SM

STD9301
 STDOFF-3.3X1.8R1.28H-SM

STANDOFF: P/N 860-1683
 STD9302
 STDOFF-3.3X2.2R1.35H-SM-1

PLATED THROUGH HOLES
 DRILL SIZE: 1.1MM X 0.4MM
 PLATING SIZE: 1.4MM X 0.7MM



SYNC MASTER=J85 MLB C		SYNC DATE=12/03/12	
TEST: TP/HOLES/FIDUCIALS			
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EE CHARACTERIZATION TP

FOR FRANK (SEG)

NAND

PP9401	1	FMI0_DQS	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.D34:2MM	4 12 53
PP9402	1	FMI0_AD<3>	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652.C34:2MM	6 12
PP9403	1	FMI0_DQS	PLACE_NEAR=U0652.D34:2MM	4 12 53
PP9410	1	TP_TCKC_U1400		12
PP9411	1	TP_TMSC_U1400		12
PP9412	1	TP_U1400_RB0		12
PP9413	1	TP_U1400_RB1		12

DWI

PP9405	1	DWI_AP_DO	PLACE_SIDE=BOTTOM PLACE_NEAR=U8100:2MM	6 48
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AUDIO

PP9406	1	I2S0_CODEC_ASP_MCK	PLACE_NEAR=U1900:2MM	6 15
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PP9416	1	I2S2_CODEC_XSP_LRCK	PLACE_NEAR=U1900:2MM	6 15
PP9417	1	I2S2_CODEC_XSP_DOUT	PLACE_NEAR=U1900:2MM	6 15

PP9419	1	I2S1_SPKAMP_MCK	PLACE_NEAR=U2040:2MM	6 16
PP9420	1	I2S1_SPKAMP_BCLK	PLACE_NEAR=U2040:2MM	6 16
PP9421	1	I2S1_SPKAMP_LRCK	PLACE_NEAR=U2040:2MM	6 16
PP9422	1	I2S1_SPKAMP_DOUT	PLACE_NEAR=U2040:2MM	6 16
PP9423	1	I2S1_SPKAMP_DIN	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	6 16

PP9424	1	SPI2_CODEC_SCLK	PLACE_NEAR=U1900:2MM	6 15
PP9425	1	SPI2_CODEC_MOSI	PLACE_NEAR=U1900:2MM	6 15
PP9426	1	SPI2_CODEC_MISO	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	6 15

GRAPE

OSCAR

PP9428	1	UART4_SOC2OSCAR_TXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U2400:2MM	6 19
PP9429	1	UART4_OSCAR2SOC_RXD	PLACE_SIDE=BOTTOM PLACE_NEAR=U0652:2MM	6 19

UART5

PP9450	1	PPVDD_SOC_SOC_SENSE	PLACE_NEAR=U0652.V31:1MM	
PP9451	1	PPVDD_CPU_SOC_SENSE	PLACE_NEAR=U0652.AN30:1MM	

WIFI

PP9480	1	HSIC1_WLAN2SOC_DEVICE_RDY		5 44
PP9481	1	HSIC1_WLAN2SOC_REMOTE_WAKE		5 44
PP9482	1	PMU_GPIO_WLAN_HOST_WAKE		44 48
PP9483	1	HSIC1_SOC2WLAN_HOST_RDY		5 44

GPIO_BT_WAKE	FUNC_TEST=TRUE	5 44
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FOR HSIC CHARACTERIZATION

PP9460	1	HSIC1_WLAN_DATA	PLACE_NEAR=U0652.AM33:3MM	4 44 53
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PP9462	1	HSIC1_WLAN_DATA	PLACE_NEAR=U5800.13:3MM	4 44 53
PP9463	1	HSIC1_WLAN_STB	PLACE_NEAR=U5800.14:3MM	4 44

PP9468	1	UART1_BT2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9469	1	UART1_SOC2BT_TX	PLACE_NEAR=U5800:3MM	5 44

PP9471	1	UART2_WLAN2SOC_TX	PLACE_NEAR=U0652:3MM	5 44
PP9472	1	UART2_SOC2WLAN_TX	PLACE_NEAR=U5800:3MM	5 44

BASEBAND

USB_BB_P	FUNC_TEST=TRUE	11 24 52
USB_BB_N	FUNC_TEST=TRUE	11 24 52

FOR HSIC CHARACTERIZATION

PP9465	1	HSIC2_BB_STB	PLACE_NEAR=U0652.B27:3MM	4 24 27
PP9466	1	HSIC2_BB_DATA	PLACE_NEAR=U3400.C7:3MM	4 24 27

PROX

HIGH SPEED, NO TEST

MIPI0C_CAM_REAR_CLK_P	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_CLK_N	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_DATA_P<0..3>	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_DATA_N<0..3>	NO_TEST=TRUE	7 23 53
MIPI0C_CAM_REAR_CLK_FILT_P	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_CLK_FILT_N	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_DATA_FILT_P<0..3>	NO_TEST=TRUE	23
MIPI0C_CAM_REAR_DATA_FILT_N<0..3>	NO_TEST=TRUE	23
MIPI0C_CAM_FRONT_CLK_P	NO_TEST=TRUE	7 20 53
MIPI0C_CAM_FRONT_CLK_N	NO_TEST=TRUE	7 20 53
MIPI0C_CAM_FRONT_DATA_P<0>	NO_TEST=TRUE	7 20 53
MIPI0C_CAM_FRONT_DATA_N<0>	NO_TEST=TRUE	7 20 53
MIPI0C_CAM_FRONT_CLK_FILT_P	NO_TEST=TRUE	20
MIPI0C_CAM_FRONT_CLK_FILT_N	NO_TEST=TRUE	20
MIPI0C_CAM_FRONT_DATA_FILT_P<0>	NO_TEST=TRUE	20
MIPI0C_CAM_FRONT_DATA_FILT_N<0>	NO_TEST=TRUE	20
EDP_DATA_P<0..3>	NO_TEST=TRUE	7 18
EDP_DATA_N<0..3>	NO_TEST=TRUE	7 18
EDP_DATA_EMI_P<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_N<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_CONN_P<0..3>	NO_TEST=TRUE	18
EDP_DATA_EMI_CONN_N<0..3>	NO_TEST=TRUE	18

CAMERA

PP9440	1	MIPI1C_CAM_FRONT_CLK_P	PLACE_NEAR=U0652.AR33:3MM	7 20 53
PP9441	1	MIPI1C_CAM_FRONT_CLK_N	PLACE_NEAR=U0652.AR34:3MM	7 20 53
PP9442	1	MIPI1C_CAM_FRONT_DATA_P<0>	PLACE_NEAR=U0652.AT33:3MM	7 20 53
PP9443	1	MIPI1C_CAM_FRONT_DATA_N<0>	PLACE_NEAR=U0652.AT34:3MM	7 20 53
PP9444	1	MIPI0C_CAM_REAR_CLK_P	PLACE_NEAR=U0652.AU25:3MM	7 23 53
PP9445	1	MIPI0C_CAM_REAR_CLK_N	PLACE_NEAR=U0652.AV25:3MM	7 23 53
PP9446	1	MIPI0C_CAM_REAR_DATA_P<0>	PLACE_NEAR=U0652.AU27:3MM	7 23 53
PP9447	1	MIPI0C_CAM_REAR_DATA_N<0>	PLACE_NEAR=U0652.AV27:3MM	7 23 53

SYNC MASTER=J72_MLB_C		SYNC DATE=11/26/2012	
PAGE TITLE			
TEST: EE TP/PP			
Apple Inc.		DRAWING NUMBER	051-0886
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POWER CONNECTIONS

BUCK0

52 46 PPVDD_CPU == =PPVDD_CPU 9

BUCK1

52 46 PPVDD_GPU == =PPVDD_GPU 9

BUCK2

52 46 PPVDD_SOC == =PPVDD_SOC 9

BUCK3

52 47 44 PP1V8_S2R == =PP1V8_S2R_MISC 5 51
 == =PP1V8_S2R_VDDIO_WLAN_BT 44
 == =PP1V8_S2R_TRISTAR 11
 == =PP1V8_S2R_DDR 8
 == =PP1V8_S2R_GRAPE 13
 == =PP1V8_S2R_EXT_SWITCH 50
 == =PP1V8_S2R_REAR_CAMERA 13
 == =PP1V8_S2R_MESA 13
 == =PP1V8_S2R_VDD_CORE_GPS 13
 == =PP1V8_S2R_VDD_IO_GPS 13

BUCK3_SW

52 50 46 PP1V8_SW1 == =PP1V8_AUDIO 15
 == =PP1V8_DMIC 14
 == =PP1V8_CAM_FRONT 20
 == =PP1V8_CAM_REAR 23
 == =PP1V8_PROX 22

BUCK3_EXT SW

52 50 46 PP1V8_SW1 == =PP1V8_VDDIO18_SOC 8 9
 == =PP1V8_SOC 4 5 7 10 18
 == =PP1V8_MIPI_SOC 7
 == =PP1V8_EDP_SOC 7
 == =PP1V8_NAND_SOC 6
 == =PP1V8_NAND 12 48
 == =PP1V8_PLL_SOC 4
 == =PP1V8_SPKRAMP 13
 == =PP1V8_EEPROM 51
 == =PP1V8_BEACON 13

BUCK3_SW2

52 46 PP1V8_SW2 == =PP1V8_GRAPE 13

BUCK3_SW3

46 PP1V8_S2R_SW3 == =PP1V8_S2R_GYRO 21
 == =PP1V8_S2R_ACCEL 21
 == =PP1V8_S2R OSCAR 19

BUCK3_SW3 COMP

54 52 PP1V8_S2R_SW3_COMP == =PP1V8_S2R_COMP 21

PP1V8_S2R_SW3 SHOULD BE ON IN HIBERNATE CURRENTLY POWERS OSCAR AND 1.8V RAIL ON SENSOR

BUCK4

52 47 46 PP1V2_S2R == =PP1V2_S2R_DDR 8
 == =PP1V2_S2R_DDR_SOC 8
 == =PP1V2_S2R_CAM_REAR 8

BUCK4_SW

52 46 PP1V2_SW1 == =PP1V2_VDDO_DDR 8
 == =PP1V2_VDDIOD_SOC 8
 == =PP1V2_HSIC_SOC 4

BUCK4_SW2

52 46 PP1V2_S2R_SW2 == =PP1V2_S2R OSCAR 19

PP1V2_S2R_SW2 SHOULD BE ON IN HIBERNATE PROVIDE 1.2V TO OSCAR

BUCK5

52 46 PPVDD_SRAM == =PPVDD_SRAM_CPU 9
 == =PPVDD_SRAM_SOC 9

BUCK6

52 46 PP3V3_S2R == =PP3V3_S2R_SWITCH 48
 == =PP3V3_S2R_WIFI_PA 44

BUCK6_SW

52 48 PP3V3_SW == =PP3V3_EDP_PU 13
 == =PP3V3_NAND 13
 == =PP3V3_USB_SOC 4

LDO1

52 47 PP3V0_SPARE1 == =PP3V0_SPARE1 49

LDO2

52 47 16 PP1V7_VA_VCP == =PP1V7_VA_VCP 15 16

LDO3

52 47 PP3V0_S2R_SENSOR == =PP3V0_S2R_HALL 13
 == =PP3V0_S2R_GYRO 21
 == =PP3V0_S2R_ACCEL 21
 == =PP3V0_S2R_COMP 21

LDO3 SHOULD BE ON IN HIBERNATE COMPASS, ACCEL, GYRO, PROX ARE ON OSCAR HALL EFFECT NEEDS TO BE ON IN HIBERNATE

LDO4

52 47 PP3V0_ALS == =PP3V0_ALS 20
 == =PP3V0_PROX 22
 == =PP3V0_HP_ALS 22
 == =PP3V0_IO_ALS 22

SHOULD IO ALS POWER HERE?

LDO5

52 47 PP3V0_UVLO == =PP3V0_UVLO 49

LDO6

52 47 PP3V3_ACC == =PP3V3_ACC 11

LDO7

52 47 PP3V0_S2R_TRISTAR == =PP3V0_S2R_TRISTAR 11

LDO7 SHOULD BE ON IN HIBERNATE

LDO8

47 NC_LDO8 NO_TEST=TRUE == =NC_LDO8

LDO9

52 47 PP1V3_CAM == =PP1V3_CAM_FRONT 23
 == =PP1V3_CAM_REAR 23

BACKUP RAIL. CAN BE BOOSTED TO MEET 1.1V MIN ON CAMERA IF NEEDED.

LDO10

52 47 PP1V0_SOC == =PP1V0_USB_SOC 4
 == =PP1V0_MIPI_SOC 7
 == =PP1V0_EDP_PAD_DVDD_SOC 7

LDO11

52 47 PP2V6_CAM_AF == =PP2V6_CAM_REAR_AF 23

LDO13

52 47 PP2V9_CAM == =PP2V9_CAM_FRONT 20
 == =PP2V9_CAM_REAR 23

VLCM1

47 PP5V25_GRAPE == =PP5V25_GRAPE 13

CHARGER MAIN

52 49 48 47 46 PPVCC_MAIN == =PPVCC_MAIN_AUDIO 15 16
 == =PPVCC_MAIN_LED 47
 == =PPVCC_MAIN_DOCK 43
 == =PPVCC_MAIN_DEV 46
 == =PPVCC_MAIN_CPU 46
 == =PPVCC_MAIN_GPU 46
 == =PPVCC_MAIN_SOC 46
 == =PPVCC_MAIN_GRAPE 13
 == =PPVCC_MAIN_LCD 18
 == =PPVCC_MAIN_NAVAJA 47
 == =PPVCC_MAIN_VDD_LCM 44
 == =PPVCC_MAIN_WLAN 44
 == =PPVCC_MAIN_GPS 44

BATTERY

52 46 PPBATT_VCC == =PPBATT_POS_CONN 45
 == =PPBATT_VCC_BB 24 25 33 34 35 36 37 38
 == =PPBATT_AUDIO 45

USB POWER INPUT

52 46 PPVBUS_USB_DCIN == =PPVBUS_USB_EMI 43

ON_BUF

52 47 PP1V8_ALWAYS == =PP1V8_ALWAYS 5

BACKLIGHT BOOST

52 47 PPLED_OUT_A == =PPLED_REG_A 18

SYNC MASTER=j72 MLB C SYNC DATE=11/26/2012

POWER: ALIASES



Apple Inc.

DRAWING NUMBER 051-0886 SIZE D

REVISION A.0.0

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