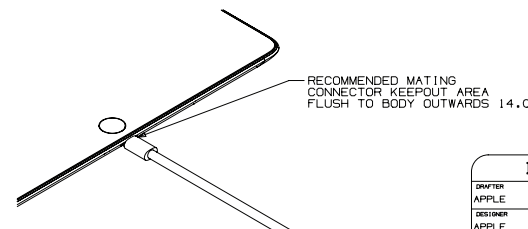
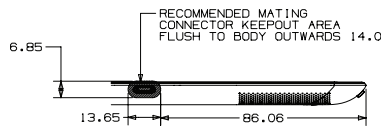
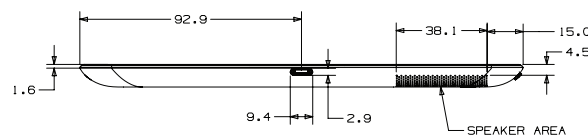
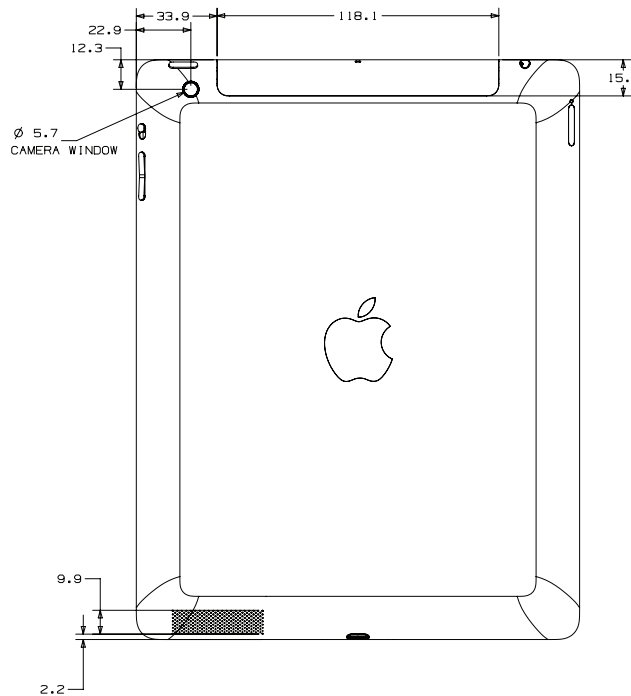
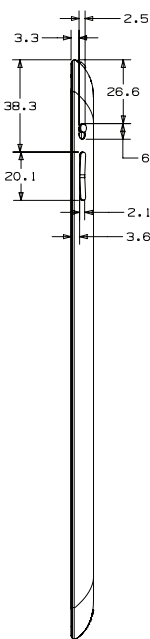
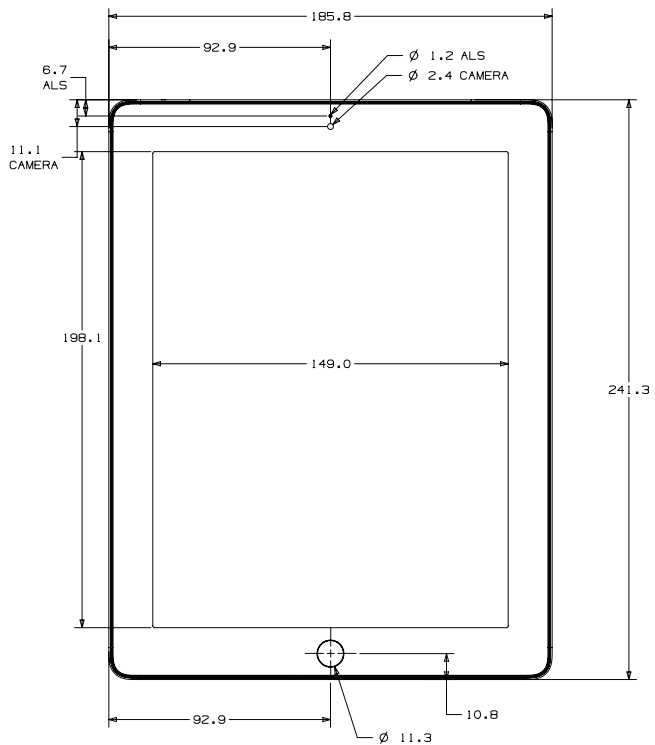
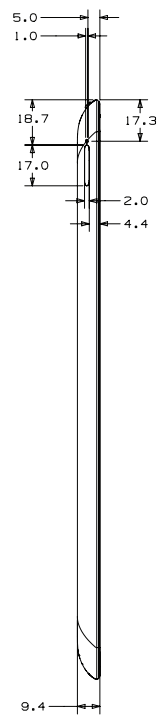
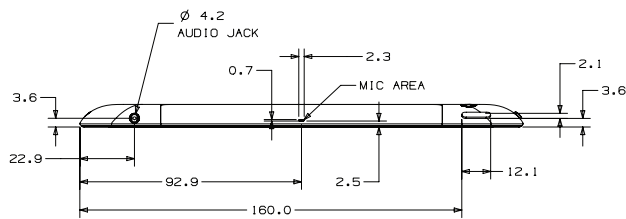
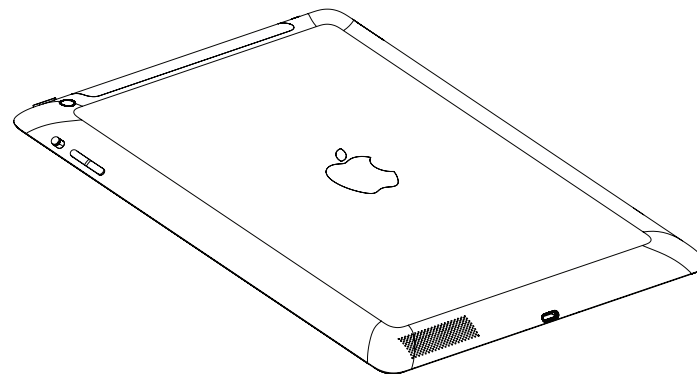
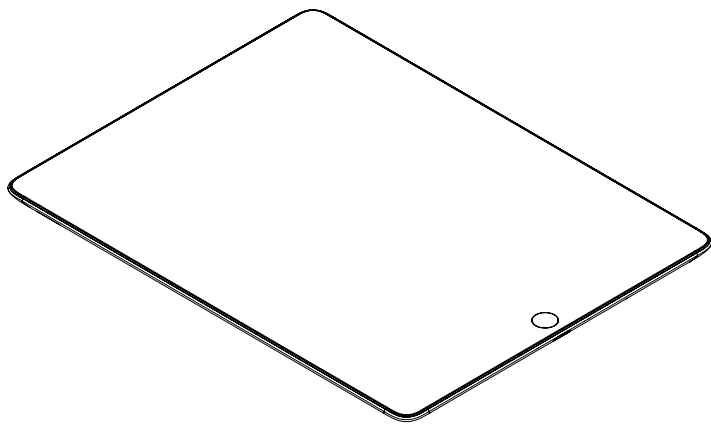


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REV	EDM	DESCRIPTION OF REVISION



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TOLERANCES	TITLE	IPAD WI-FI + CELLULAR (4TH GENERATION)	
X.X ±0.2	DRAWING NUMBER	REV. 02	
X.XX ±0.10	SCALE	NONE	
X.XXX ±0.050	SIZE	SHT 1 OF 1	
ANGLES ±0.5°	SCALE	NONE	
DO NOT SCALE DRAWINGS	THIRD ANGLE PROJECTION	NX GENERATED	

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD DATE
A	0001554595	PRODUCTION RELEASED	2012-07-26

iPad 4th Gen

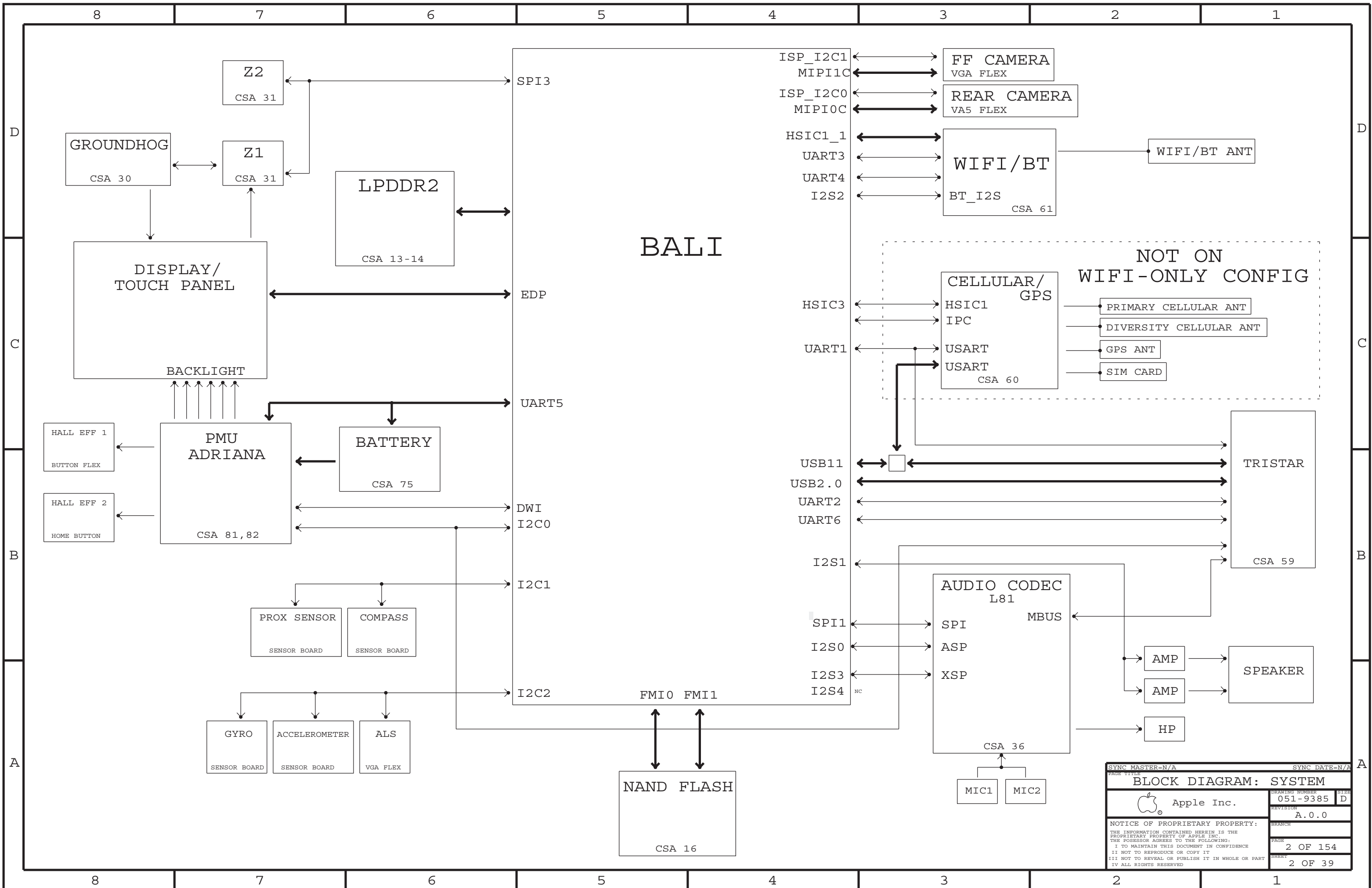
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PDF	CSA	CONTENTS	SYNC MASTER	DATE	(SYSTEM DRI)
1	1	Table of Contents	N/A	N/A	(AMANDA)
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A	(AMANDA)
3	4	BOM TABLES	N/A	N/A	(AMANDA)
4	6	AP: MAIN	N/A	N/A	(TERRY)
5	7	AP: I/Os	N/A	N/A	(AMANDA)
6	8	AP: NAND	N/A	N/A	(TERRY)
7	9	AP: TV, DP, MIPI	N/A	N/A	(TERRY)
8	10	AP: DDR	N/A	N/A	(TERRY)
9	11	AP: POWER	N/A	N/A	(TERRY)
10	12	AP: MISC & ALIASES	N/A	N/A	(TERRY)
11	13	DDR 0 AND 1	N/A	N/A	(TERRY)
12	14	DDR 2 AND 3	N/A	N/A	(TERRY)
13	16	NAND	N/A	N/A	(AMANDA)
14	21	ALIASES	N/A	N/A	(AMANDA)
15	22	VIDEO: EDP CONNECTOR	N/A	N/A	(JOE)
16	30	GRAPE: GROUNDHOG, CONN, BOOST	N/A	N/A	(AMANDA)
17	31	GRAPE: Z1, Z2	N/A	N/A	(AMANDA)
18	36	AUDIO: L81 CODEC	N/A	N/A	(TERRY)
19	37	AUDIO: SPEAKER AMP	N/A	N/A	(TERRY)
20	54	SENSOR FLEX CONN	N/A	N/A	(MARK)
21	55	SENSOR CONN FILTERS 1	N/A	N/A	(MARK)
22	56	SENSOR CONN FILTERS 2	N/A	N/A	(MARK)
23	57	E75 DOCK SUPPORT	N/A	N/A	(JOE)
24	58	IO FLEX CONN	N/A	N/A	(JOE)
25	59	TRISTAR	N/A	N/A	(JOE)
26	60	CONNECTOR: CELLULAR	N/A	N/A	(AMANDA)
27	61	WIFI/BT	N/A	N/A	(MATT)
28	75	POWER: BATTERY CONNECTOR	MADHAVI	12/06/2011	(MADHAVI)
29	81	PMU: ADRIANA PAGE 1	MADHAVI	12/06/2011	(MADHAVI)
30	82	PMU: ADRIANA PAGE 2	MADHAVI	12/06/2011	(MADHAVI)

PDF	CSA	CONTENTS	SYNC MASTER	DATE	(SYSTEM DRI)
31	83	PMU: ADRIANA PAGE 3	MADHAVI	12/06/2011	(MADHAVI)
32	90	DEBUG/MISC.	MLB	11/09/2011	(AMANDA)
33	93	TEST/HOLES/FIDUCUALS	N/A	N/A	(AMANDA)
34	121	POWER ALIASES	N/A	N/A	(MADHAVI)
35	150	CONSTRAINTS: MLB RULES	MIKE	11/30/2011	(AMANDA)
36	151	CONSTRAINTS: LOW SPEED BUS	MIKE	11/30/2011	(AMANDA)
37	152	CONSTRAINTS: DISPLAY/AUDIO	MIKE	11/30/2011	(AMANDA)
38	153	CONSTRAINTS: DDR/FMI	MIKE	11/30/2011	(AMANDA)
39	154	CONSTRAINTS: POWER / GND	MIKE	11/30/2011	(AMANDA)

DRAWING
MLB
DRAWING

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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD: 16GB CONFIG
32GB_PROD: 32GB CONFIG
64GB_PROD: 64GB CONFIG
DEV: DEV BOARD ONLY

MLB: MLB BOARD ONLY
MLB_A: WIFI ONLY CONFIG
MLB_B: CELLULAR CONFIG
MLB_C: CELLULAR CONFIG
MLB_D: LEGACY CELLULAR CONFIG
MLB_E: LEGACY CELLULAR CONFIG

BOM GROUP	BOM OPTIONS
BASIC	COMMON, ALTERNATE

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
806-4195	1	FENCE, NAND, TOP, MLB, X140	PD_FENCE_NAND	CRITICAL	
806-3493	1	FENCE, LARGE, TOP, MLB, X140	PD_FENCE_LARGE	CRITICAL	
806-3956	1	FENCE, AMP, MLB, X140	PD_FENCE_AMP	CRITICAL	
806-4196	1	FENCE, 1, BTM, MLB, X140	PD_FENCE_BT1	CRITICAL	
806-3492	1	FENCE, 2, BTM, MLB, X140	PD_FENCE_BT2	CRITICAL	

BARCODE LABEL/EEEE CODES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7838	1	EEEE FOR 639-3736 (MLB A 16G)	EEEE_F1WD	CRITICAL	EEEE_MLB_A_16G
825-7838	1	EEEE FOR 639-3737 (MLB A 32G)	EEEE_F1WH	CRITICAL	EEEE_MLB_A_32G
825-7838	1	EEEE FOR 639-3738 (MLB A 64G)	EEEE_F1W8	CRITICAL	EEEE_MLB_A_64G
825-7838	1	EEEE FOR 639-4176 (MLB A 128G)	EEEE_F80Q	CRITICAL	EEEE_MLB_A_128G
825-7838	1	EEEE FOR 639-3263 (MLB B 16G)	EEEE_DWKG	CRITICAL	EEEE_MLB_B_16G
825-7838	1	EEEE FOR 639-3739 (MLB B 32G)	EEEE_F1W7	CRITICAL	EEEE_MLB_B_32G
825-7838	1	EEEE FOR 639-3740 (MLB B 64G)	EEEE_F1WC	CRITICAL	EEEE_MLB_B_64G
825-7838	1	EEEE FOR 639-4177 (MLB B 128G)	EEEE_F80P	CRITICAL	EEEE_MLB_B_128G
825-7838	1	EEEE FOR 639-3741 (MLB C 16G)	EEEE_F1WG	CRITICAL	EEEE_MLB_C_16G
825-7838	1	EEEE FOR 639-3742 (MLB C 32G)	EEEE_F1WF	CRITICAL	EEEE_MLB_C_32G
825-7838	1	EEEE FOR 639-3743 (MLB C 64G)	EEEE_F1W9	CRITICAL	EEEE_MLB_C_64G
825-7838	1	EEEE FOR 639-4178 (MLB C 128G)	EEEE_F80R	CRITICAL	EEEE_MLB_C_128G

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-9385	1	SCH, MLB, X140	SCH1	CRITICAL	
820-3249	1	PCBF, MLB, X140	PCB1	CRITICAL	

SOC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0598	1	IC, SOC, H5G, FCBGA1089, 0.5MM	U0600	CRITICAL	

PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0622	1	IC, PMU, ADRIANA, D2018A1, FCBGA	U8100	CRITICAL	

SDRAM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0636	2	LPDDR2, 533MHZ, 512MB, SAMSUNG, 38NM	U1300, U1400	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0637	333S0636		U1300, U1400	LPDDR2, 533MHZ, HYNIX, 38NM
333S0638	333S0636		U1400, U1400	LPDDR2, 533MHZ, ELPIDA, 38NM

NAND

16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0878	1	TOSHIBA PP1.5 16GB	U1600	CRITICAL	16GB_PROD

32GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0879	1	TOSHIBA PP1.5 32GB	U1600	CRITICAL	32GB_PROD

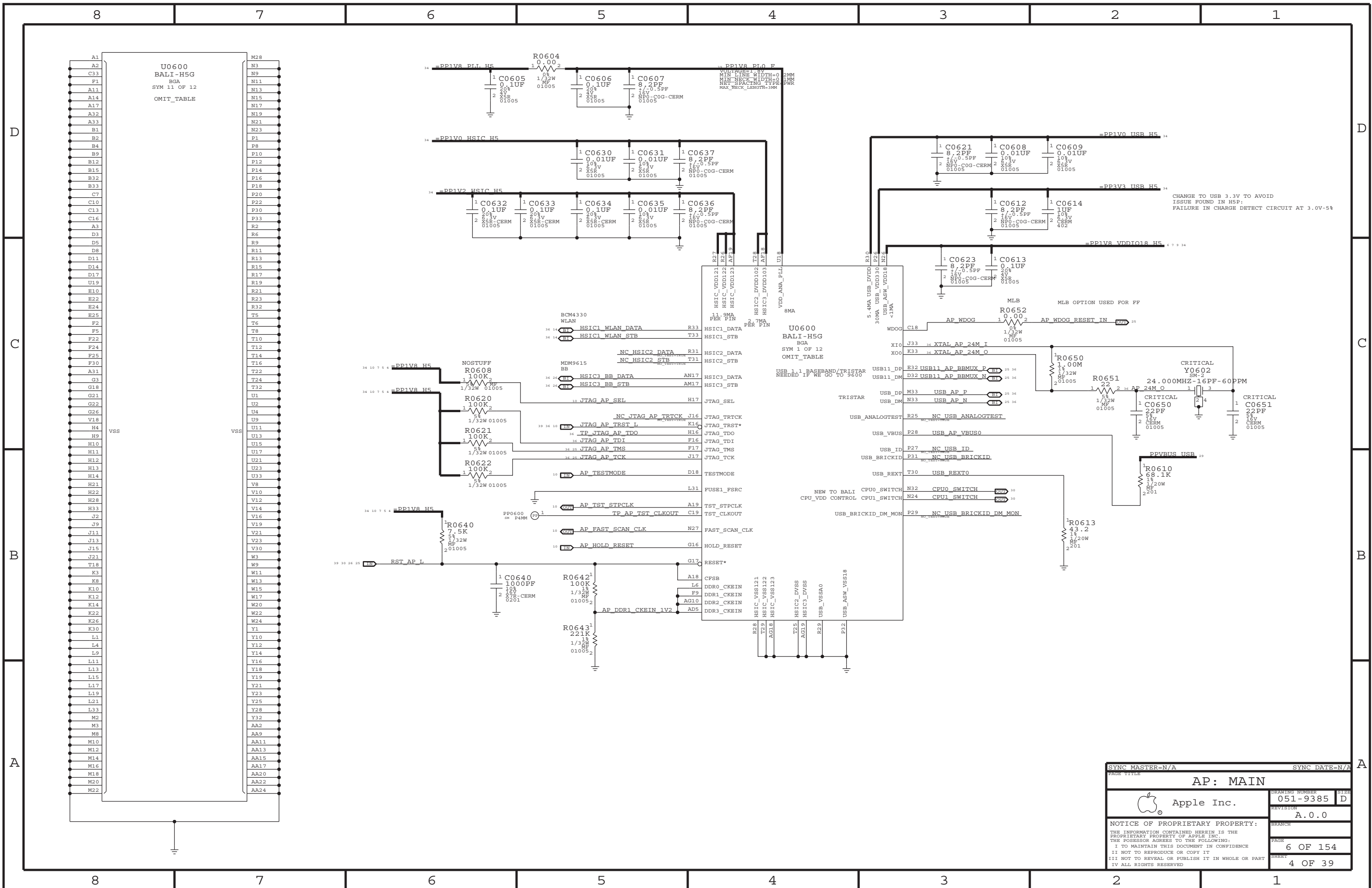
64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0880	1	TOSHIBA PP1.5 64GB	U1600	CRITICAL	64GB_PROD

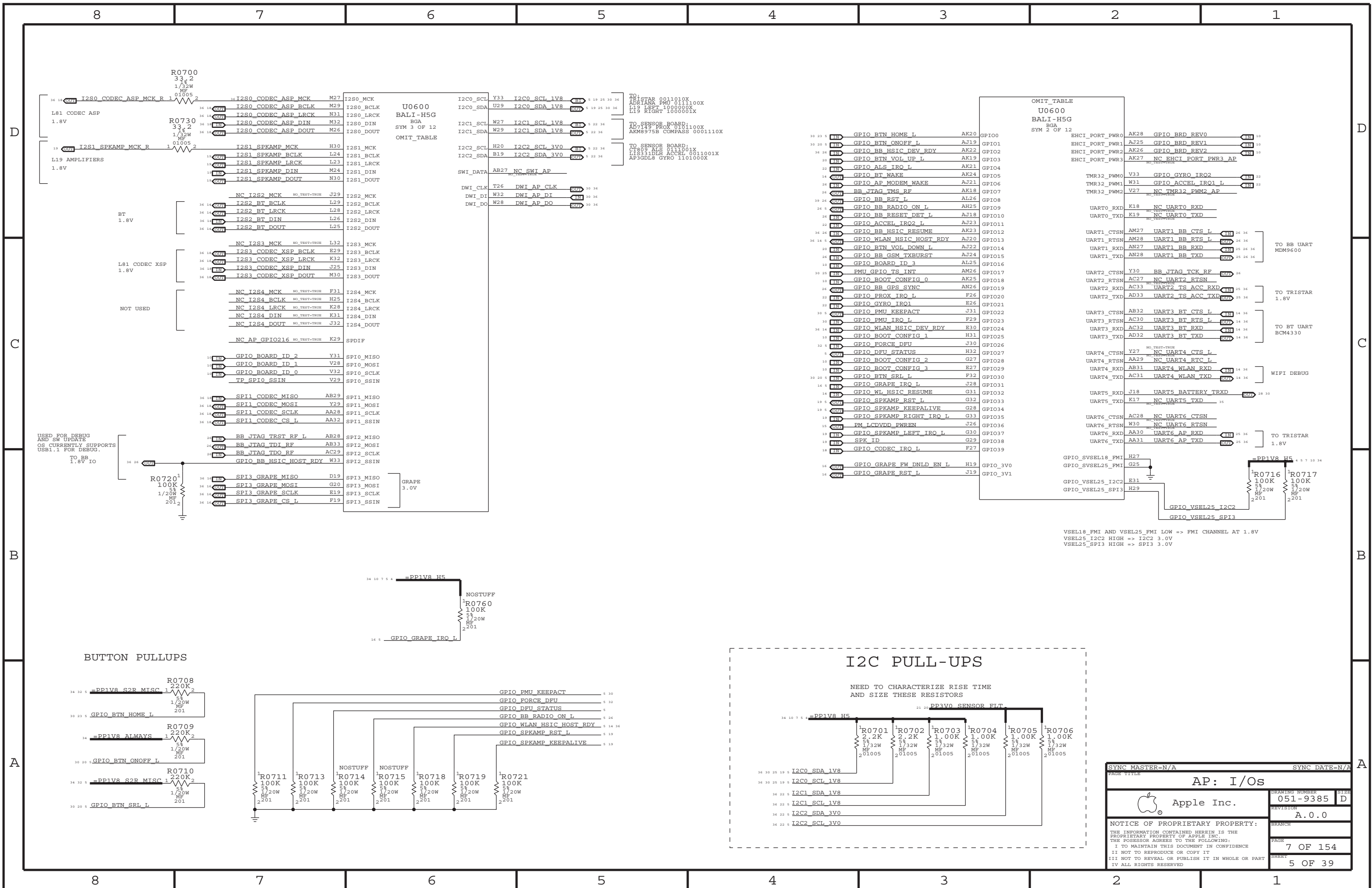
128GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0912	1	TOSHIBA PP1.5 128GB	U1600	CRITICAL	128GB_PROD

SYNC MASTER=N/A		SYNC DATE=N/A	
BOM TABLES			
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I2S0 CODEC ASP MCK R 1
L81 CODEC ASP
1.8V

I2S1 SPKAMP MCK R 1
L19 AMPLIFIERS
1.8V

BT
1.8V

L81 CODEC XSP
1.8V

NOT USED

USED FOR DEBUG
AND SW UPDATE
OS CURRENTLY SUPPORTS
USB1.1 FOR DEBUG.
TO BB
1.8V IO

R0720
100K
1/20W
201

U0600
BALI-H5G
BGA
SYM 3 OF 12
OMIT_TABLE

TO TRISTAR 0011010X
ADRIANA PMU 0111100X
L19 LEFT 1000000X
L19 RIGHT 1000001X

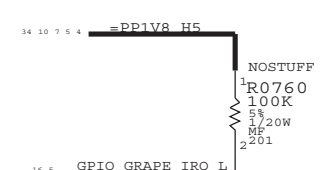
TO SENSOR BOARD
CF809 ALS 0111001X
L1831DLH ACCEL 0011001X
AF3GDL8 GYRO 1101000X

OMIT_TABLE
U0600
BALI-H5G
BGA
SYM 2 OF 12

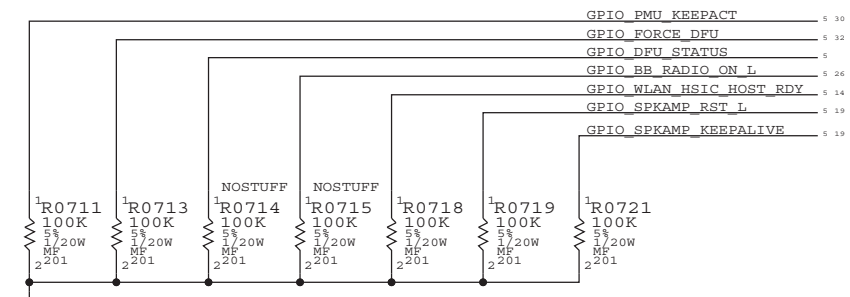
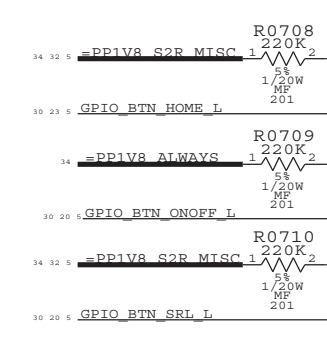
GPIO_BTN_HOME_L	AK20	GPIO10
GPIO_BTN_ONOFF_L	AJ19	GPIO1
GPIO_BB_HSIC_DEV_RDY	AK22	GPIO2
GPIO_BTN_VOL_UP_L	AK19	GPIO3
GPIO_ALS_IRO_L	AK21	GPIO4
GPIO_BT_WAKE	AK24	GPIO5
GPIO_AP_MODEM_WAKE	AJ21	GPIO6
BB_JTAG_TMS_RF	AK18	GPIO7
GPIO_BB_RST_L	AL26	GPIO8
GPIO_BB_RADIO_ON_L	AH25	GPIO9
GPIO_BB_RESET_DET_L	AJ18	GPIO10
GPIO_ACCEL_IRO2_L	AJ23	GPIO11
GPIO_BB_HSIC_RESUME	AK23	GPIO12
GPIO_WLAN_HSIC_HOST_RDY	AJ20	GPIO13
GPIO_BTN_VOL_DOWN_L	AJ22	GPIO14
GPIO_BB_GSM_TXBURST	AJ24	GPIO15
GPIO_BOARD_ID_3	AL25	GPIO16
PMU_GPIO_TS_INT	AM26	GPIO17
GPIO_BOOT_CONFIG_0	AK25	GPIO18
GPIO_BB_GPS_SYNC	AN26	GPIO19
GPIO_PROX_IRO_L	F26	GPIO20
GPIO_GYRO_IRO1	E26	GPIO21
GPIO_PMU_KEEPACT	J31	GPIO22
GPIO_PMU_IRO_L	F29	GPIO23
GPIO_WLAN_HSIC_DEV_RDY	E30	GPIO24
GPIO_BOOT_CONFIG_1	H31	GPIO25
GPIO_FORCE_DFU	J30	GPIO26
GPIO_DFU_STATUS	H32	GPIO27
GPIO_BOOT_CONFIG_2	G27	GPIO28
GPIO_BOOT_CONFIG_3	E27	GPIO29
GPIO_BTN_SRL_L	F32	GPIO30
GPIO_GRAPE_IRO_L	J28	GPIO31
GPIO_WL_HSIC_RESUME	G31	GPIO32
GPIO_SPKAMP_RST_L	G32	GPIO33
GPIO_SPKAMP_RIGHT_IRO_L	G33	GPIO35
EM_LCDVDD_PWREN	J26	GPIO36
GPIO_SPKAMP_LEFT_IRO_L	G30	GPIO37
SPK_ID	G29	GPIO38
GPIO_CODEC_IRO_L	F27	GPIO39
GPIO_GRAPE_FW_DNLD_EN_L	H19	GPIO_3V0
GPIO_GRAPE_RST_L	J19	GPIO_3V1

EHCI_PORT_PWR0	AK28	GPIO BRD_REV0
EHCI_PORT_PWR1	AJ25	GPIO BRD_REV1
EHCI_PORT_PWR2	AK26	GPIO BRD_REV2
EHCI_PORT_PWR3	AK27	NC EHCI_PORT_PWR3_AP
TMR32_PWM0	V33	GPIO GYRO_IRO2
TMR32_PWM1	W31	GPIO ACCEL_IRO1_L
TMR32_PWM2	V27	NC TMR32_PWM2_AP
UART0_RXD	K18	NC UART0_RXD
UART0_TXD	K19	NC UART0_TXD
UART1_CTSN	AM27	UART1_BB_CTS_L
UART1_RTSN	AM28	UART1_BB_RTS_L
UART1_RXD	AN27	UART1_BB_RXD
UART1_TXD	AN28	UART1_BB_TXD
UART2_CTSN	Y30	BB_JTAG_TCK_RF
UART2_RTSN	AC27	NC UART2_RTSN
UART2_RXD	AC33	UART2_TS_ACC_RXD
UART2_TXD	AD33	UART2_TS_ACC_TXD
UART3_CTSN	AB32	UART3_BT_CTS_L
UART3_RTSN	AC30	UART3_BT_RTS_L
UART3_RXD	AC32	UART3_BT_RXD
UART3_TXD	AD32	UART3_BT_TXD
UART4_CTSN	Y27	NC UART4_CTS_L
UART4_RTSN	AA29	NC UART4_RTS_L
UART4_RXD	AB31	UART4_WLAN_RXD
UART4_TXD	AC31	UART4_WLAN_TXD
UART5_RXD	J18	UART5_BATTERY_TRXD
UART5_TXD	K17	NC UART5_TXD
UART6_CTSN	AC28	NC UART6_CTSN
UART6_RTSN	W30	NC UART6_RTSN
UART6_RXD	AA30	UART6_AP_RXD
UART6_TXD	AA31	UART6_AP_TXD

VSEL18_FMI AND VSEL25_FMI LOW => FMI CHANNEL AT 1.8V
VSEL25_I2C2 HIGH => I2C2 3.0V
VSEL25_SPI3 HIGH => SPI3 3.0V

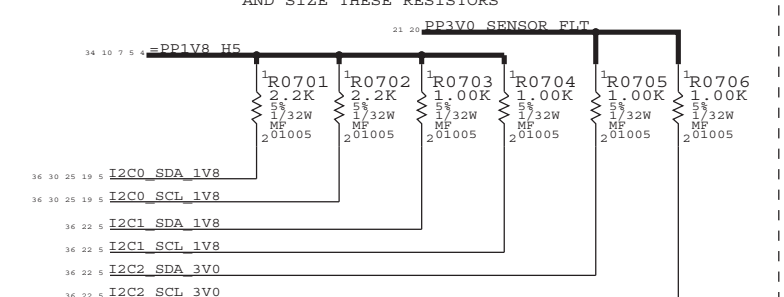


BUTTON PULLUPS

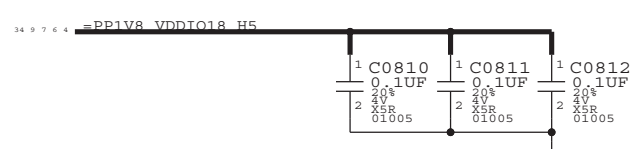
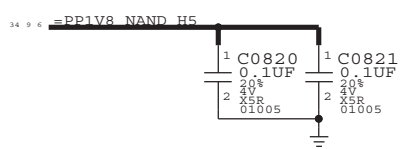
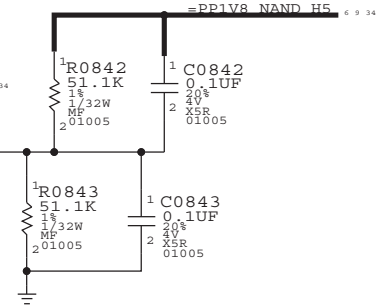
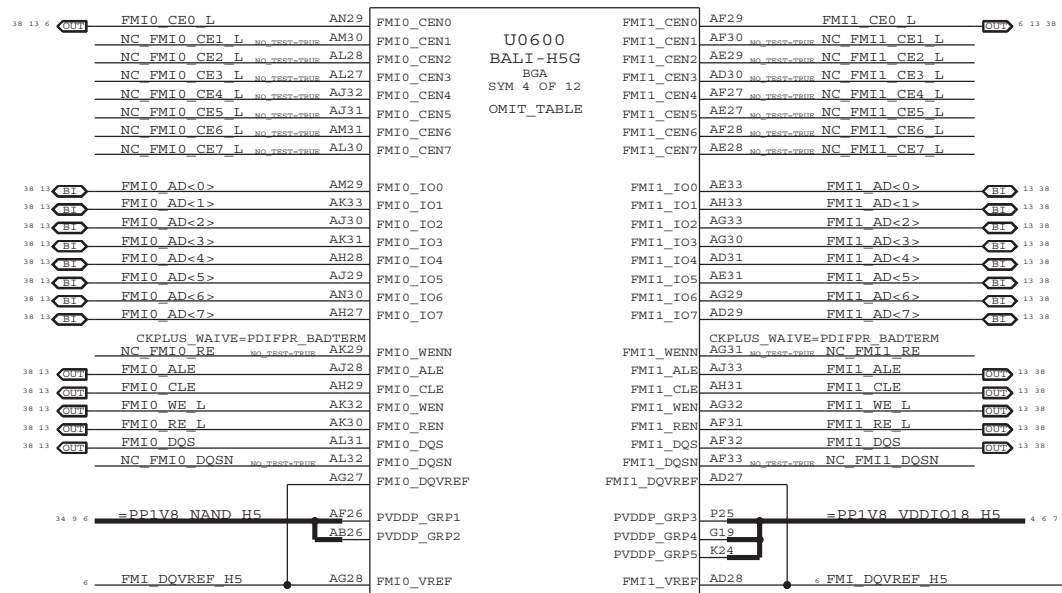
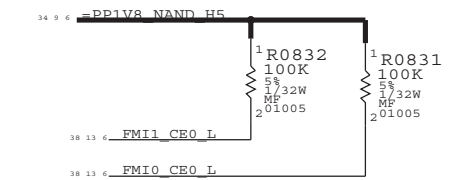
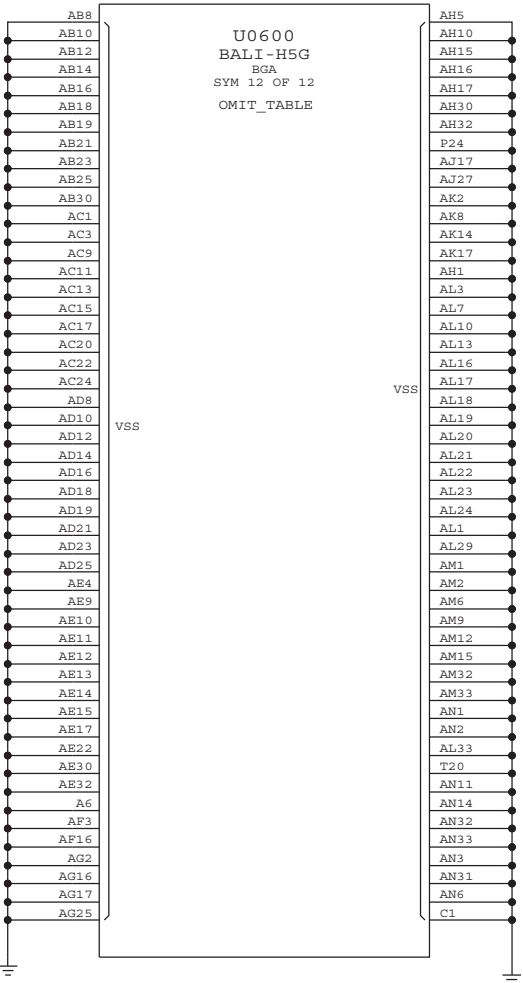
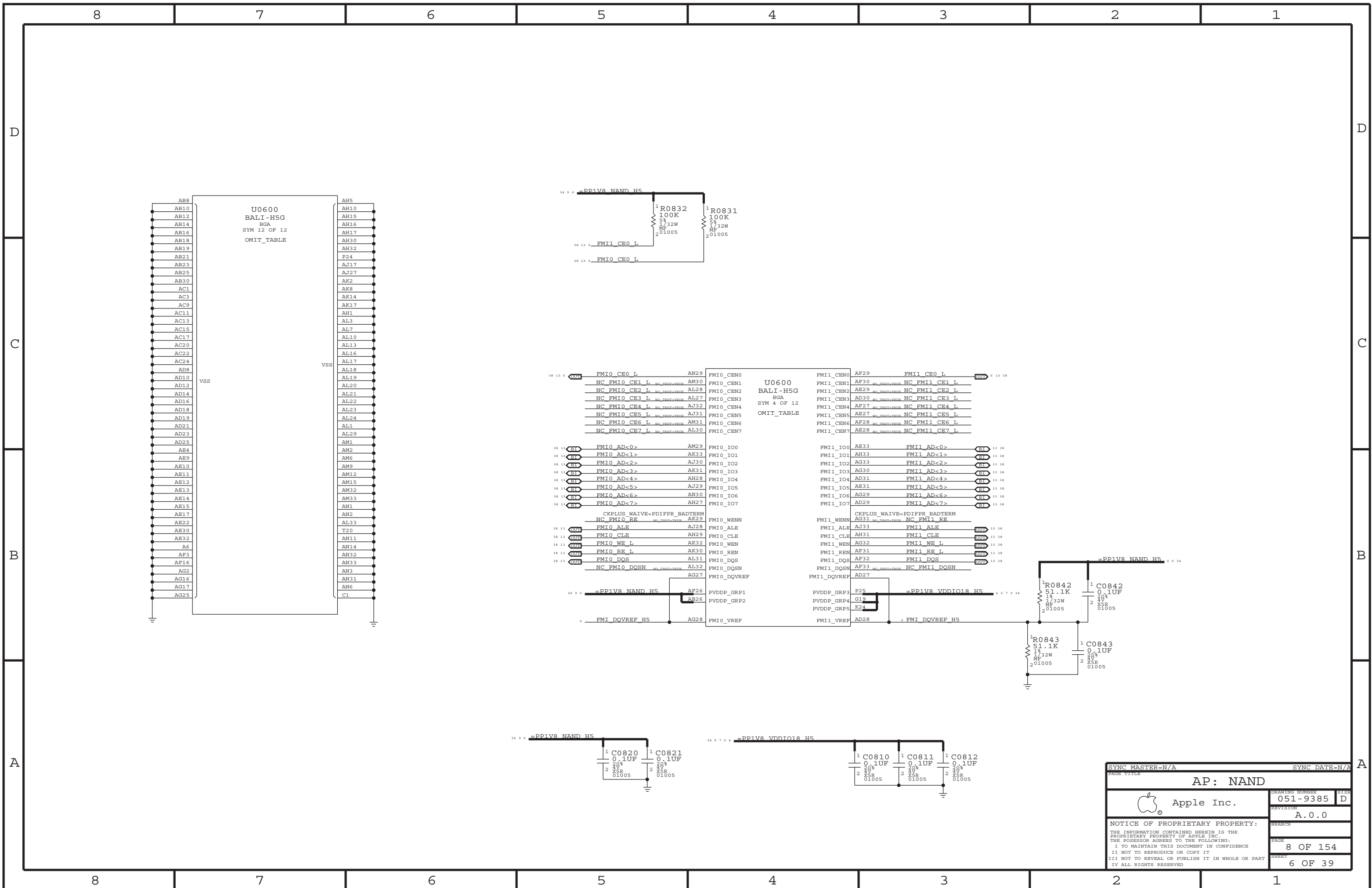


I2C PULL-UPS

NEED TO CHARACTERIZE RISE TIME
AND SIZE THESE RESISTORS

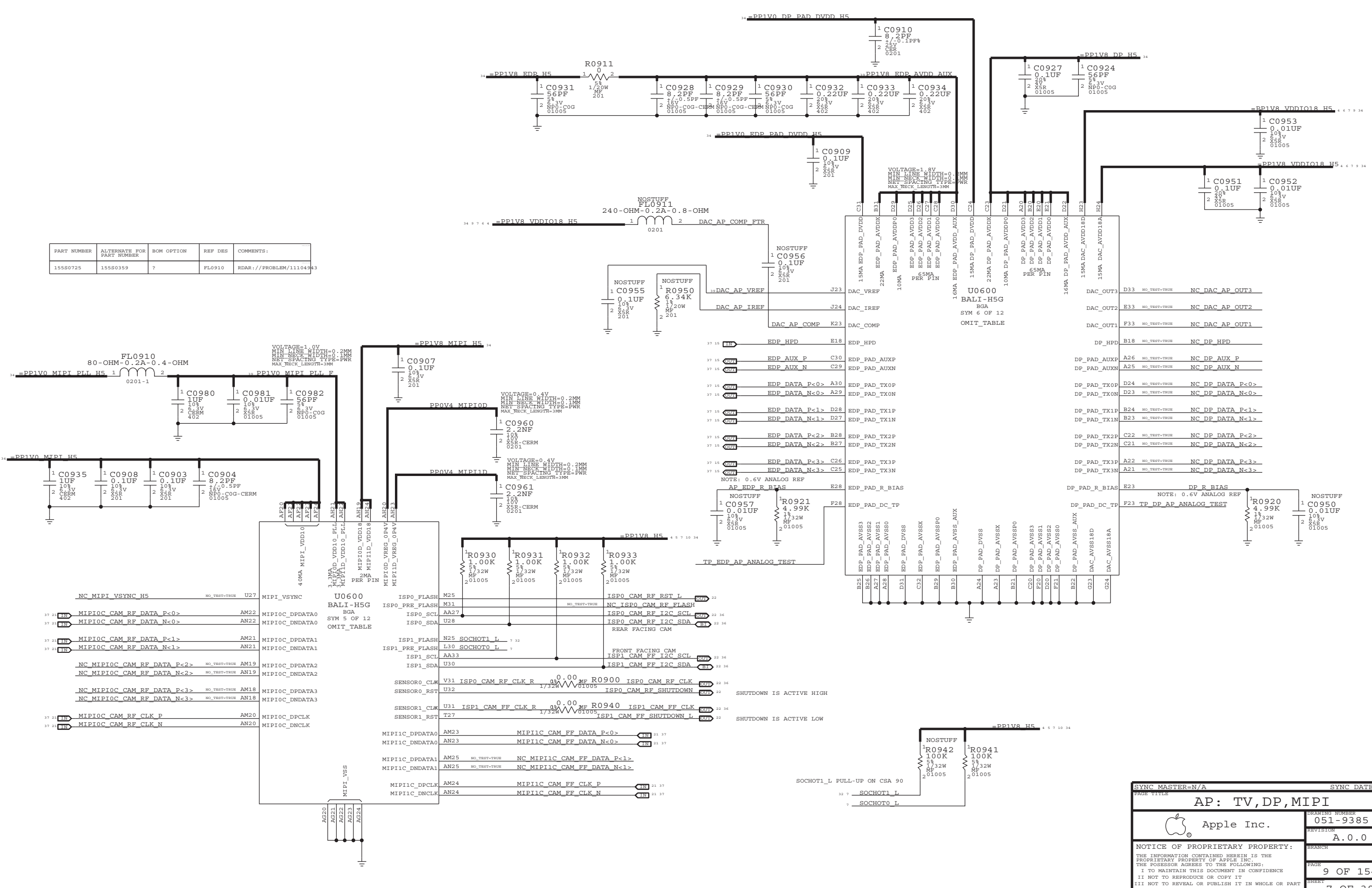


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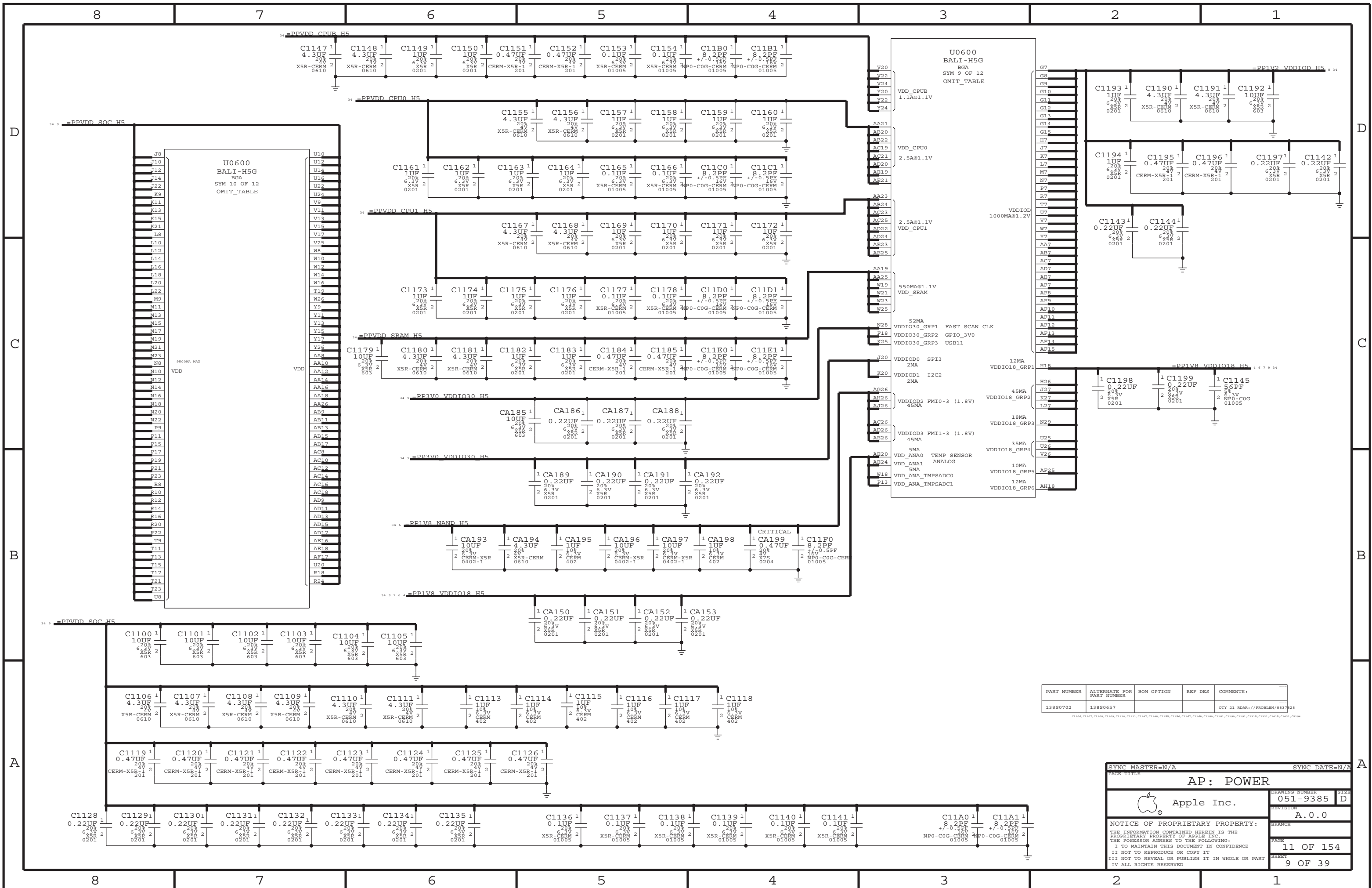


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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15550725	15550359	?	FL0910	RDAR://PROBLEM/11104943



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Apple Inc.	DRAWING NUMBER	051-9385	SIZE D
	REVISION	A.0.0	
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
138S0702	138S0657			QTY 21 BEAR:///PROBLEM/883728

SYNC MASTER=N/A SYNC DATE=N/A

AP: POWER

Apple Inc.

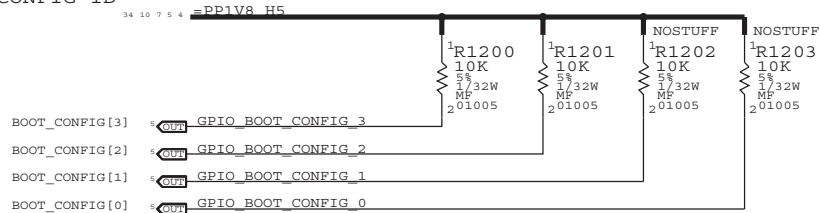
DRAWING NUMBER: 051-9385
REVISION: A.0.0

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BRANCH: 11 OF 154
PAGE: 9 OF 39

BOOT CONFIG ID

STUFF FOR FORM FACTOR BOARD



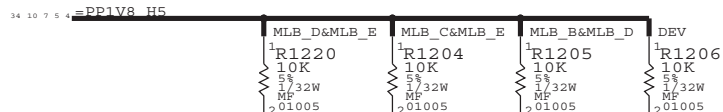
BOOT_CONFIG[3]	GPIO_BOOT_CONFIG_3
BOOT_CONFIG[2]	GPIO_BOOT_CONFIG_2
BOOT_CONFIG[1]	GPIO_BOOT_CONFIG_1
BOOT_CONFIG[0]	GPIO_BOOT_CONFIG_0

BOOT_CONFIG[3-0]		S/W READ FLOW
1100	FMIO/1 2/2 CS	1. SET GPIO AS INPUT
1101	FMIO/1 4/4 CS	2. DISABLE PU AND ENABLE PD
1110	FMIO/1 4/4 CS WITH TEST	3. READ

FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI1
0010	SPI0 W/TEST
0011	SPI1 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FMIO 2 CS
1001	FMIO 4 CS
1010	FMIO 4CS W/TEST
1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

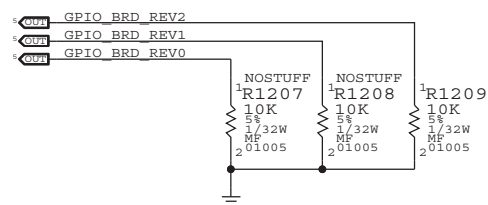
BOARD ID



BOARD_ID[3]	GPIO_BOARD_ID_3
BOARD_ID[2]	GPIO_BOARD_ID_2
BOARD_ID[1]	GPIO_BOARD_ID_1
BOARD_ID[0]	GPIO_BOARD_ID_0

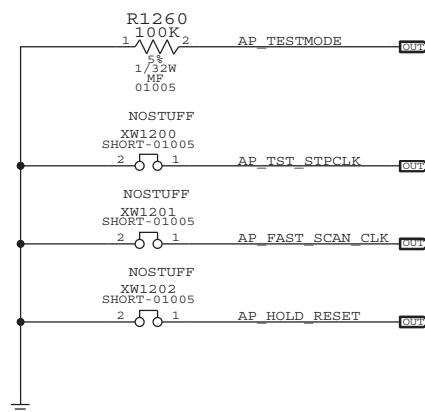
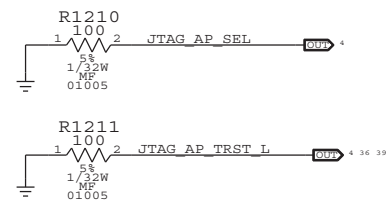
BOARD_ID[3-0]		S/W READ FLOW
0000	X140 AP WLAN (MLB A)	1. SET GPIO AS INPUT
0001	X140 DEV WLAN	2. DISABLE PU AND ENABLE PD
0010	X140 AP BB_41 (MLB B)	3. READ
0011	X140 DEV BB_41	
0100	X140 AP BB_42 (MLB C)	
0101	X140 DEV BB_42	
1010	X140 AP BB_26A (MLB D)	
1011	X140 DEV BB_26A	
1110	X140 AP BB_26 (MLB E)	
1111	X140 DEV BB_26	

BOARD REVISION

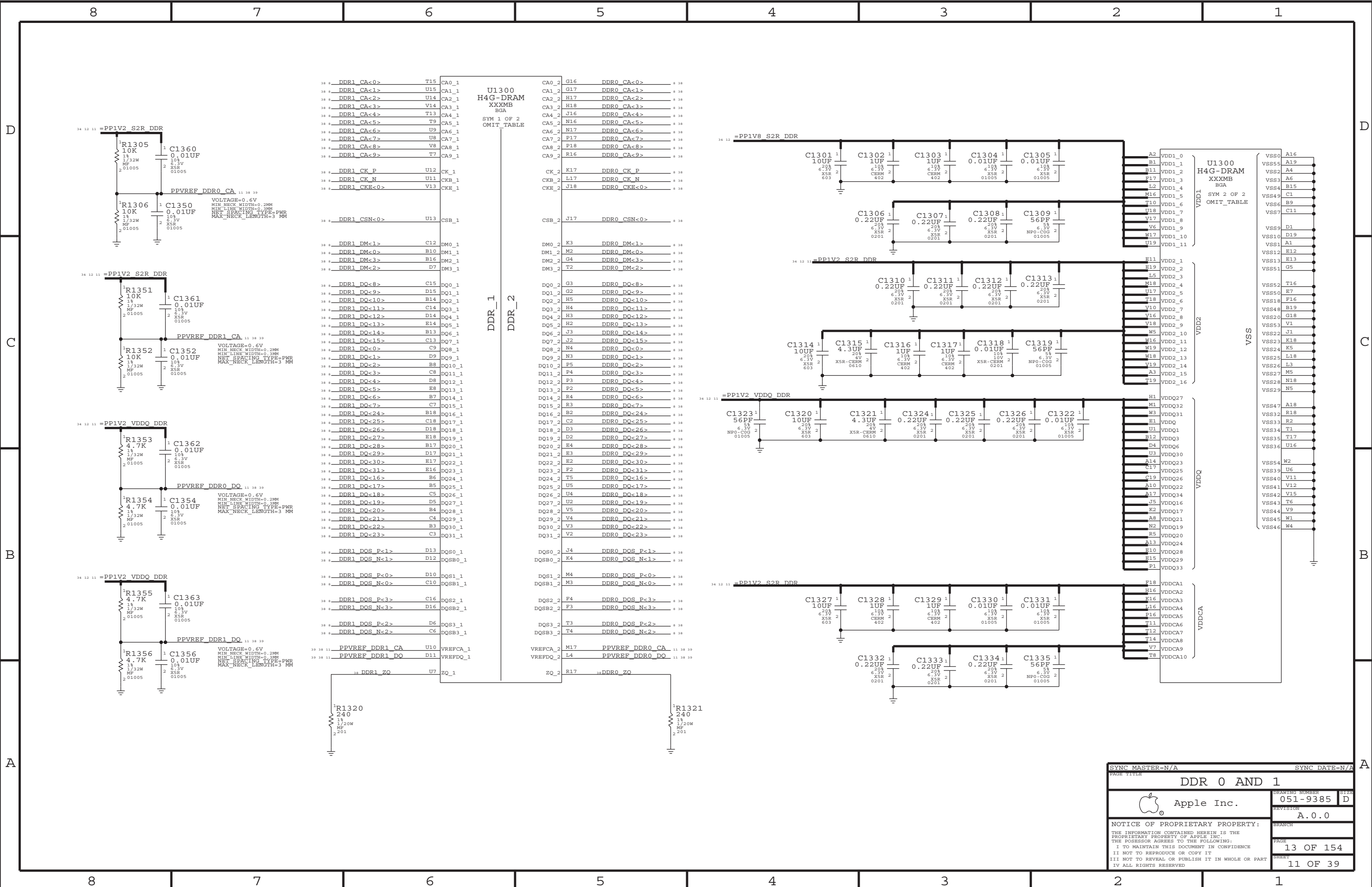


BRD_REV[2-0]		S/W READ FLOW
000	PROTO	1. SET GPIO AS INPUT
001	PROTO 2	2. ENABLE PU AND DISABLE PD
010	EVT	3. READ
011	DVT	

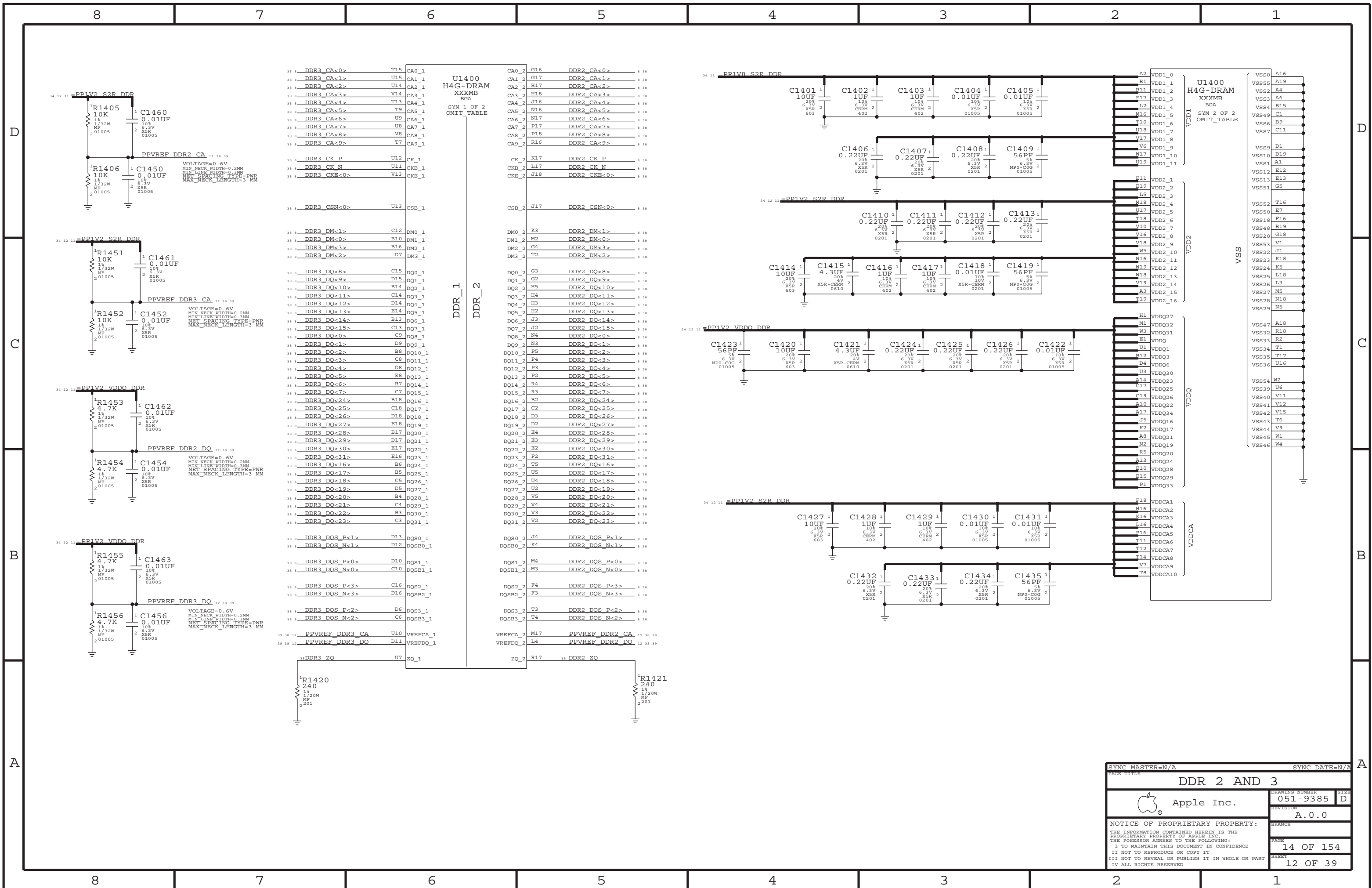
JTAG



SYNC MASTER=N/A		SYNC DATE=N/A	
AP: MISC & ALIASES			
Apple Inc.		DRAWING NUMBER	051-9385
		REVISION	A.0.0
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U1400 H4G-DRAM XXXMB BGA
SYM 1 OF 2 OMIT_TABLE

34 12 11	PP1V2 S2R DDR	CA0_1	G16	DDR2_CA<0>	38
		CA1_1	G17	DDR2_CA<1>	38
		CA2_1	H17	DDR2_CA<2>	38
		CA3_1	H18	DDR2_CA<3>	38
		CA4_1	J16	DDR2_CA<4>	38
		CA5_1	N16	DDR2_CA<5>	38
		CA6_1	N17	DDR2_CA<6>	38
		CA7_1	P17	DDR2_CA<7>	38
		CA8_1	P18	DDR2_CA<8>	38
		CA9_1	R16	DDR2_CA<9>	38
		CK_1	K17	DDR2_CK_P	38
		CKB_1	L17	DDR2_CK_N	38
		CKE_1	J18	DDR2_CKE<0>	38
		CSB_1	J17	DDR2_CSN<0>	38
		DM0_1	K3	DDR2_DM<1>	38
		DM1_1	M2	DDR2_DM<0>	38
		DM2_1	G4	DDR2_DM<3>	38
		DM3_1	T2	DDR2_DM<2>	38
		DQ0_1	G3	DDR2_DQ<8>	38
		DQ1_1	G2	DDR2_DQ<9>	38
		DQ2_1	H5	DDR2_DQ<10>	38
		DQ3_1	H4	DDR2_DQ<11>	38
		DQ4_1	H3	DDR2_DQ<12>	38
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		DQ25_1	U5	DDR2_DQ<17>	38
		DQ26_1	U4	DDR2_DQ<18>	38
		DQ27_1	U2	DDR2_DQ<19>	38
		DQ28_1	V5	DDR2_DQ<20>	38
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		DQ31_1	V2	DDR2_DQ<23>	38
		DQS0_1	J4	DDR2_DOS_P<1>	38
		DQSB0_1	K4	DDR2_DOS_N<1>	38
		DQS1_1	M4	DDR2_DOS_P<0>	38
		DQSB1_1	M3	DDR2_DOS_N<0>	38
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		DQSB2_1	F3	DDR2_DOS_N<3>	38
		DQS3_1	T3	DDR2_DOS_P<2>	38
		DQSB3_1	T4	DDR2_DOS_N<2>	38
39 38 12	PPVREF_DDR3_CA	U10	VREFCA_1	PPVREF_DDR2_CA	12 38 39
39 38 12	PPVREF_DDR3_DO	D11	VREFDQ_1	PPVREF_DDR2_DO	12 38 39
	DDR3_ZQ	U7	ZQ_1	ZQ_2	R17 18 DDR2_ZQ

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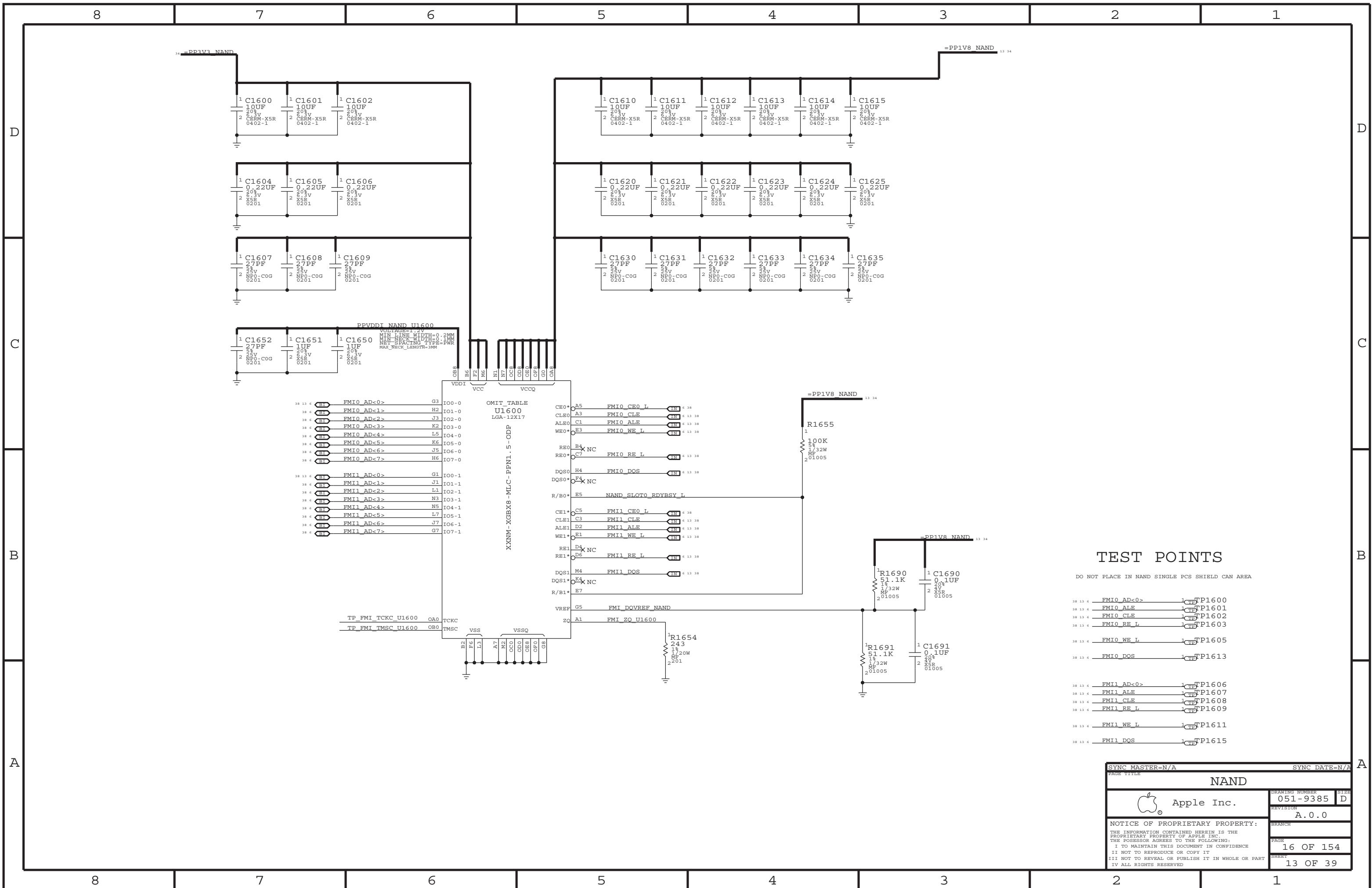
DDR 2 AND 3

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TEST POINTS

DO NOT PLACE IN NAND SINGLE PCS SHIELD CAN AREA

- 38 13 6 FMI0_AD<0> 1 TP1600
- 38 13 6 FMI0_AD<1> 1 TP1601
- 38 13 6 FMI0_AD<2> 1 TP1602
- 38 13 6 FMI0_AD<3> 1 TP1603
- 38 13 6 FMI0_AD<4> 1 TP1605
- 38 13 6 FMI0_AD<5> 1 TP1613
- 38 13 6 FMI1_AD<0> 1 TP1606
- 38 13 6 FMI1_AD<1> 1 TP1607
- 38 13 6 FMI1_AD<2> 1 TP1608
- 38 13 6 FMI1_AD<3> 1 TP1609
- 38 13 6 FMI1_AD<4> 1 TP1611
- 38 13 6 FMI1_AD<5> 1 TP1615

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NAND			
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WIFI ALIASES

34 4	HSIC1 WLAN DATA	WAKE_BA0E_T200	50 HSIC WLAN DATA	27
34 4	HSIC1 WLAN STB	WAKE_BA0E_T200	50 HSIC WLAN STROBE	27
34 5	GPIO WLAN HSIC_HOST_RDY	WAKE_BA0E_T200	AP HSIC3_RDY	27
34 5	GPIO WLAN HSIC_DEV_RDY	WAKE_BA0E_T200	DEV HSIC3_RDY	27
30	PMU GPIO WLAN_REG_ON	WAKE_BA0E_T200	WLAN_REG_ON	27
30	PMU GPIO WLAN_HOST_WAKE	WAKE_BA0E_T200	HOST_WAKE_WLAN	27
30	PMU GPIO_BT_REG_ON	WAKE_BA0E_T200	BT_REG_ON	27
30	PMU GPIO_BT_HOST_WAKE	WAKE_BA0E_T200	HOST_WAKE_BT	27
30	GPIO_BT_WAKE	WAKE_BA0E_T200	BT_WAKE	27
34 5	UART3_BT_RXD	WAKE_BA0E_T200	BT_UART_TXD	27
34 5	UART3_BT_TXD	WAKE_BA0E_T200	BT_UART_RXD	27
34 5	UART3_BT_CTS_L	WAKE_BA0E_T200	BT_UART_RTS_L	27
34 5	UART3_BT_RTS_L	WAKE_BA0E_T200	BT_UART_CTS_L	27
34 30	PMU GPIO_CLK_32K_WLAN	WAKE_BA0E_T200	CLK32K_AP	27
34 5	I2S2_BT_BCLK	WAKE_BA0E_T200	BT_PCM_CLK	27
34 5	I2S2_BT_DOUT	WAKE_BA0E_T200	BT_PCM_IN	27
34 5	I2S2_BT_DIN	WAKE_BA0E_T200	BT_PCM_OUT	27
34 5	I2S2_BT_LRCK	WAKE_BA0E_T200	BT_PCM_SYNC	27
34 5	UART4_WLAN_RXD	WAKE_BA0E_T200	WLAN_UART_TXD	27
34 5	UART4_WLAN_TXD	WAKE_BA0E_T200	WLAN_UART_RXD	27
30	GPIO_WL_HSIC_RESUME	WAKE_BA0E_T200	WLAN_HSIC3_RESUME	27
34	VDDIO_WLAN_BT_1V8	WAKE_BA0E_T200	PP_WL_BT_VDDIO_AP	27

C


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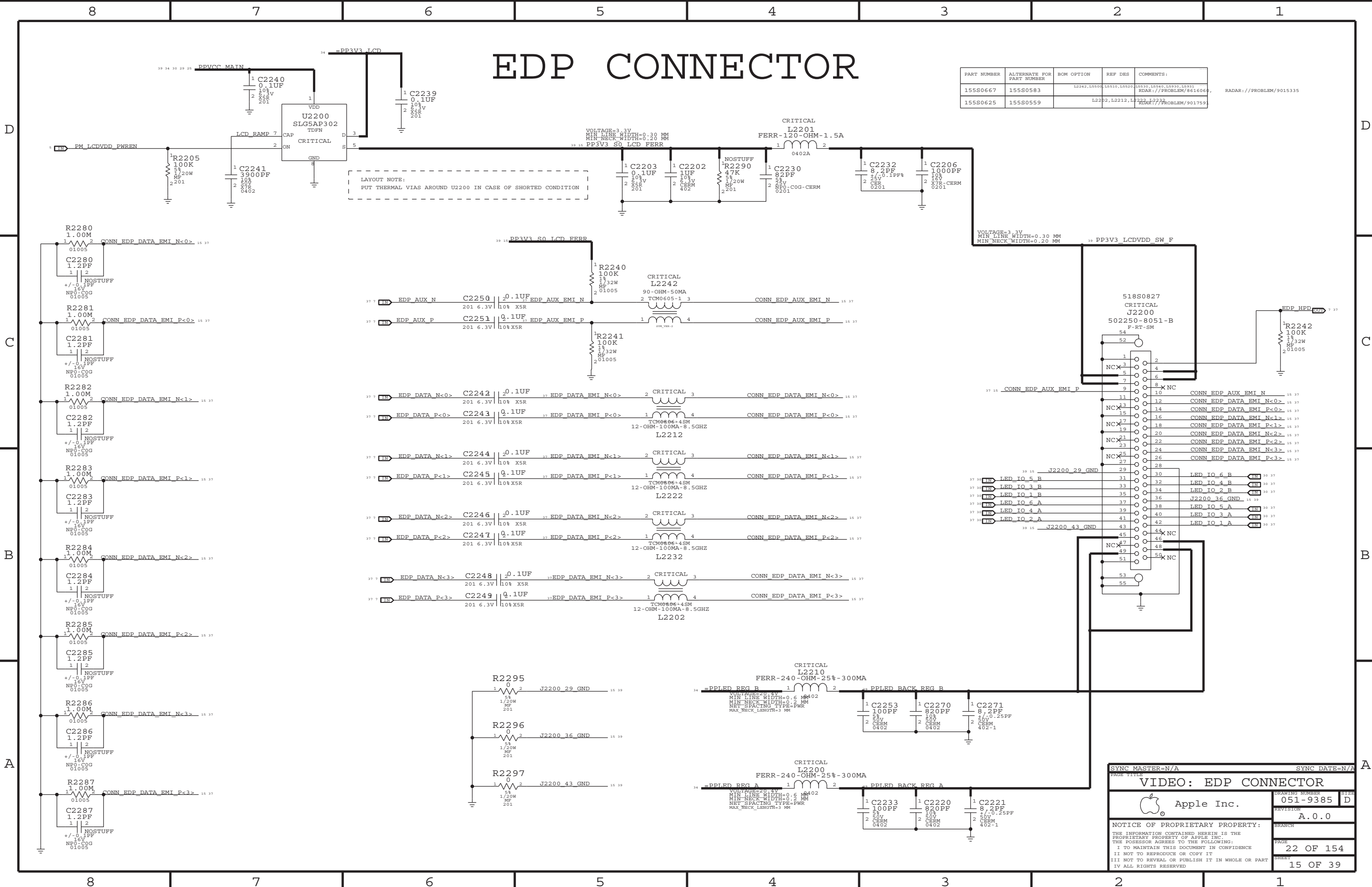
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1

EDP CONNECTOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
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155S0625	155S0559	L2202, L2212, L2222, L2232, L2242, L2244, L2245, L2246, L2247, L2248, L2249	L2202, L2212, L2222, L2232, L2242, L2244, L2245, L2246, L2247, L2248, L2249	155S0, 15540, 15590, 15931 RDAR://PROBLEM/901759

RADAR://PROBLEM/9015335



LAYOUT NOTE:
PUT THERMAL VIAS AROUND U2200 IN CASE OF SHORTED CONDITION

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MIN LINE WIDTH=0.30 MM
MIN NECK WIDTH=0.20 MM

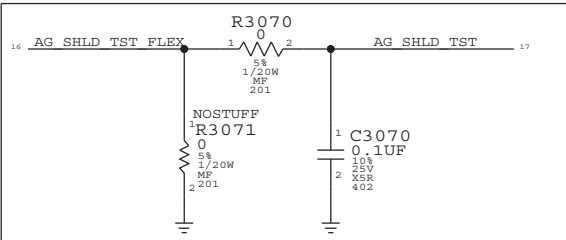
VOLTAGE=20.4V
MIN LINE WIDTH=0.6 MM
MIN NECK WIDTH=0.2 MM
NET SPACING TYPE=PWR
MAX NECK LENGTH=3 MM

VOLTAGE=20.4V
MIN LINE WIDTH=0.6 MM
MIN NECK WIDTH=0.2 MM
NET SPACING TYPE=PWR
MAX NECK LENGTH=3 MM

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VIDEO: EDP CONNECTOR			
Apple Inc.		DRAWING NUMBER	SIZE
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		REVISION	A.0.0
PAGE		22 OF 154	
SHEET		15 OF 39	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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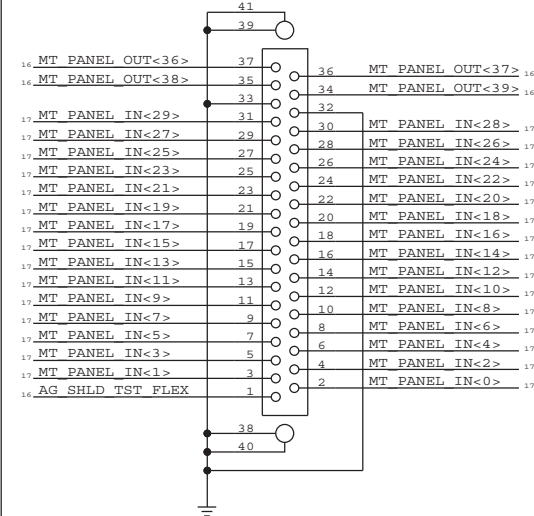
CONNECTORS TO GRAPE FLEX



P/N 518S0828

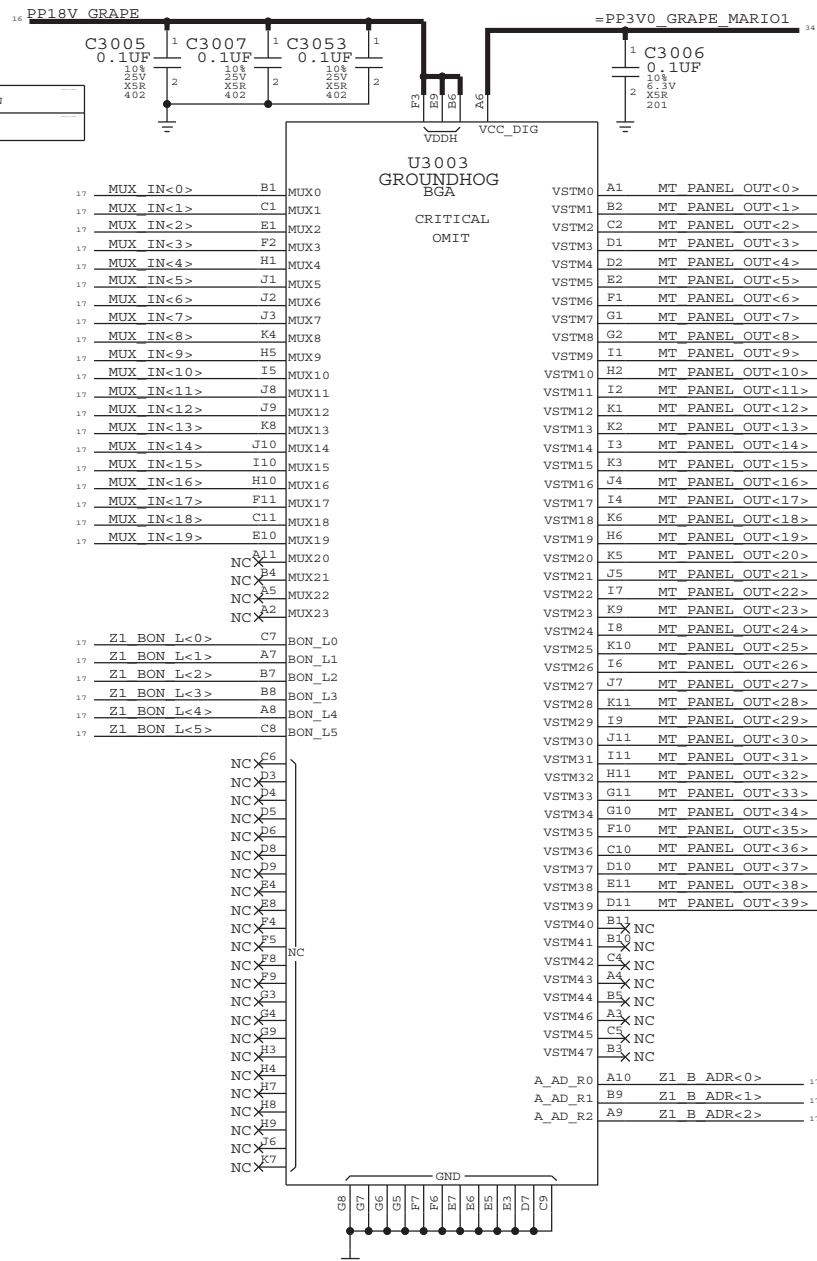
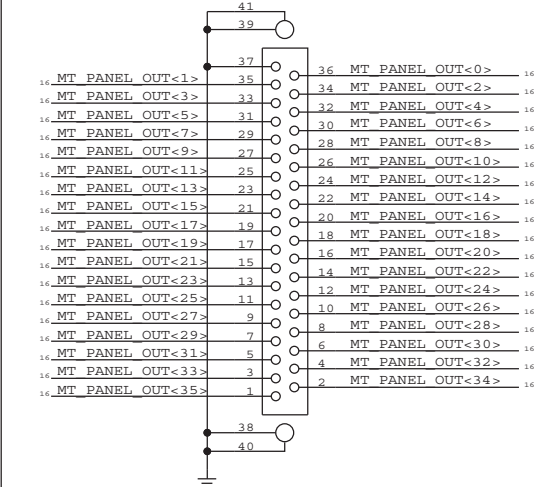
MATES WITH LEFTMOST GRAPE FLEX TAIL

CRITICAL
J3010
502250-8037-B
F-RT-SM

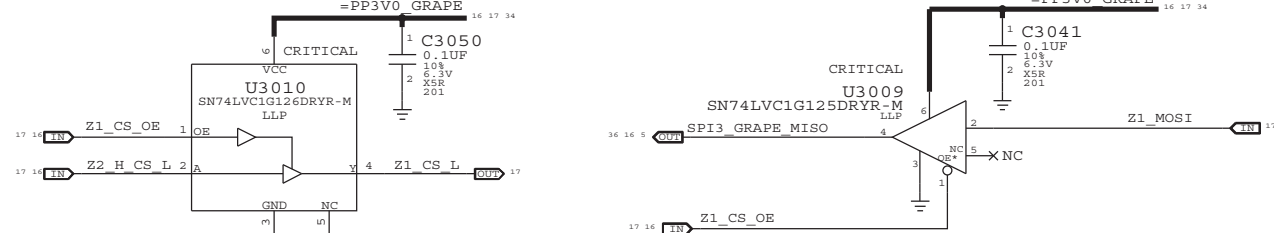
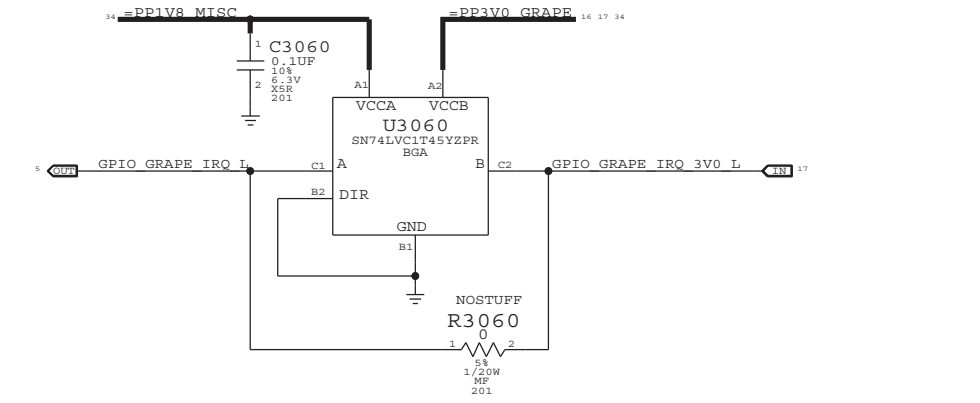
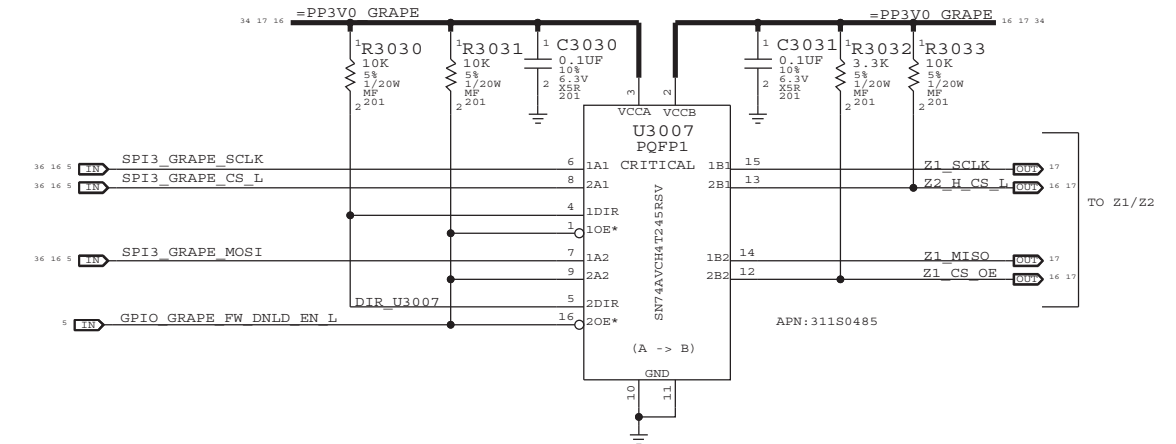
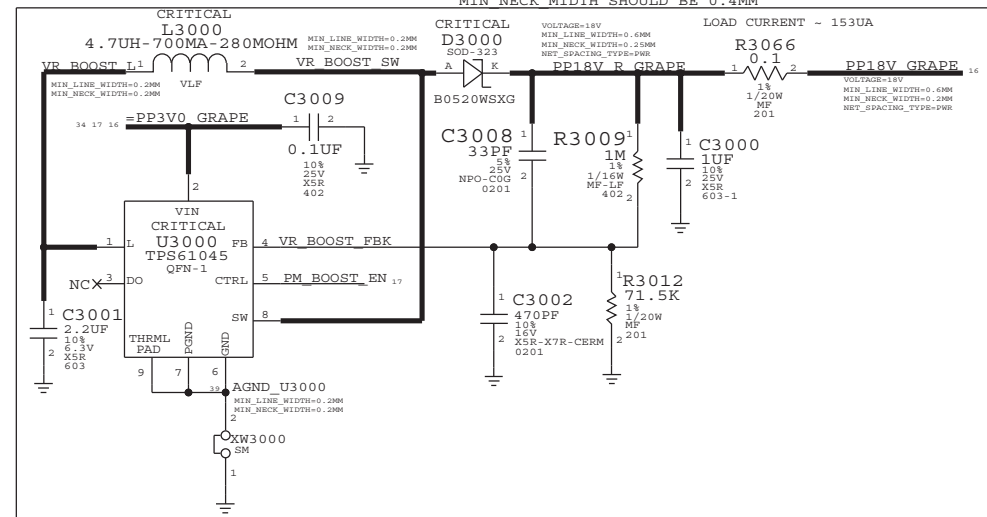


MATES WITH RIGHTMOST GRAPE FLEX TAIL

CRITICAL
J3011
502250-8037-B
F-RT-SM



BOOST CONVERTOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180523	31180485		U3007	
31180524	31180533		U3009	
31180525	31180532		U3010	

SYNC MASTER=N/A SYNC DATE=N/A

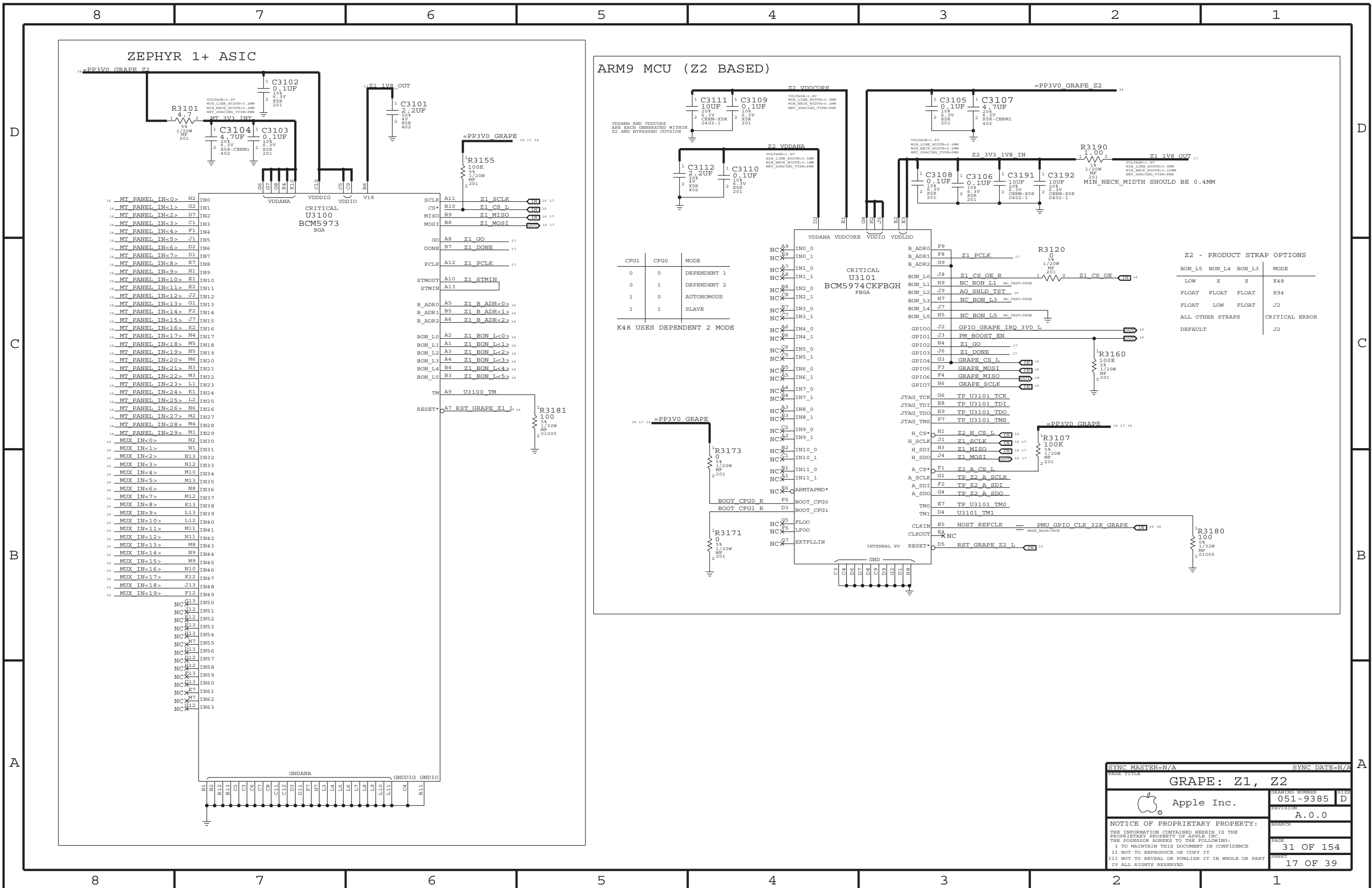
GRAPE: GROUNDHOG, CONN, BOOST

Apple Inc.

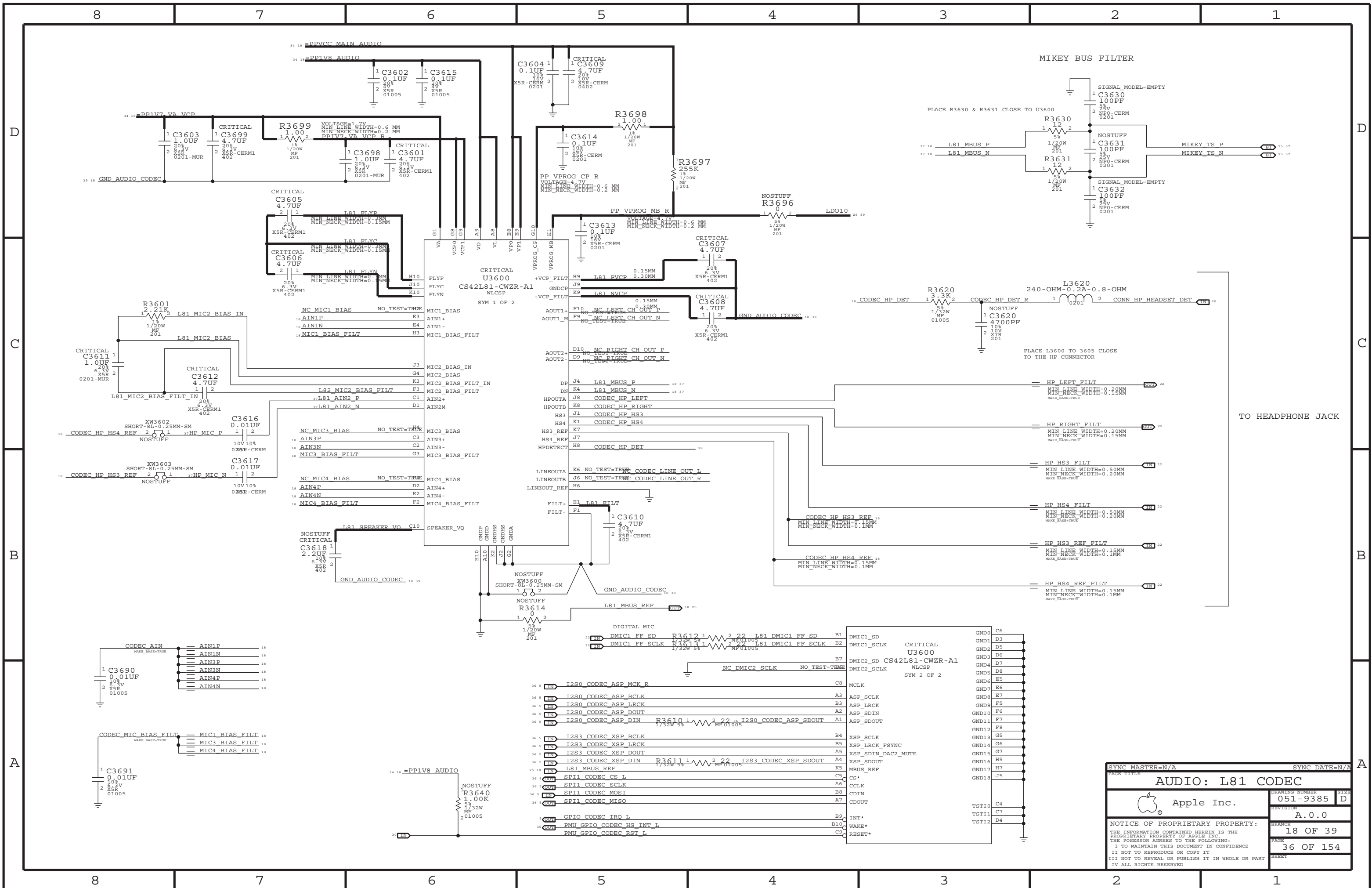
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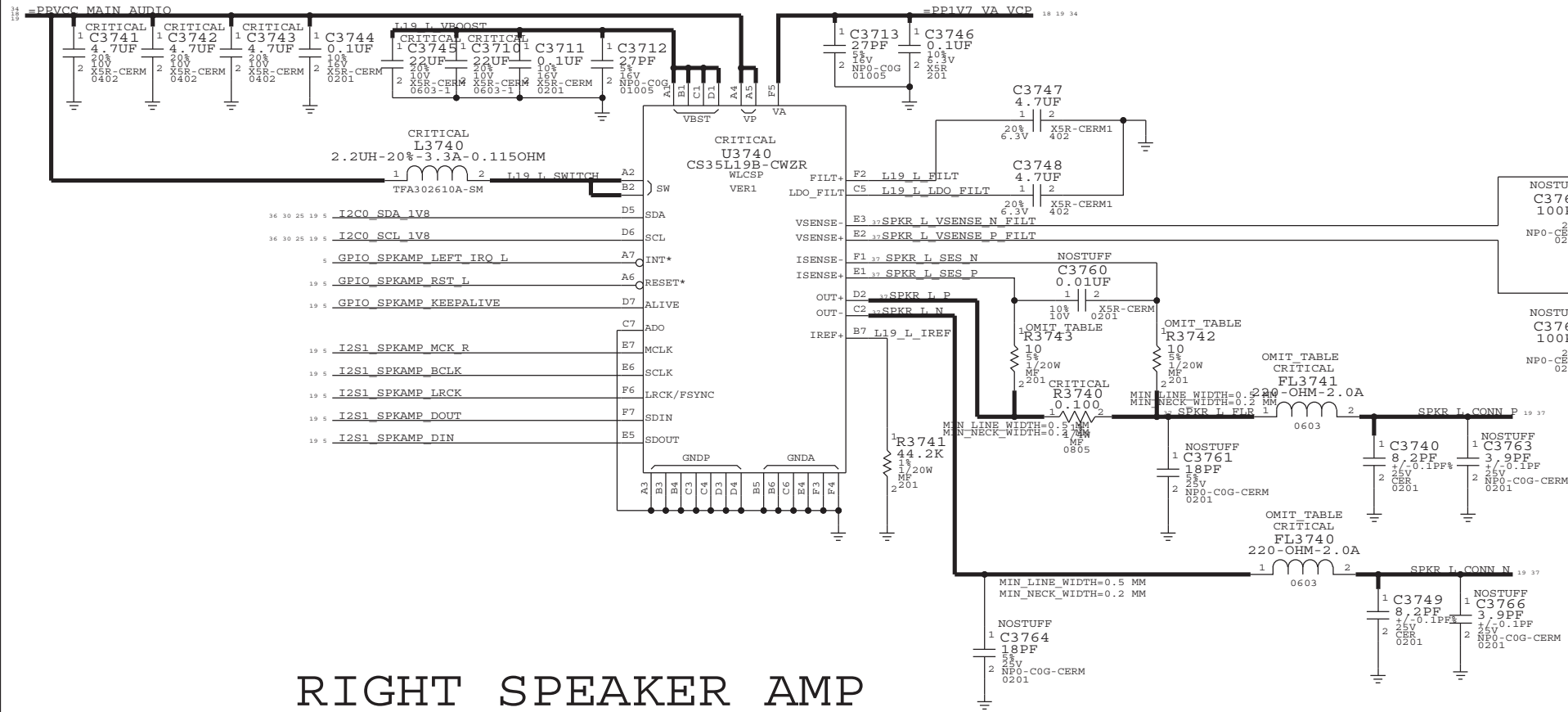


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LEFT SPEAKER AMP

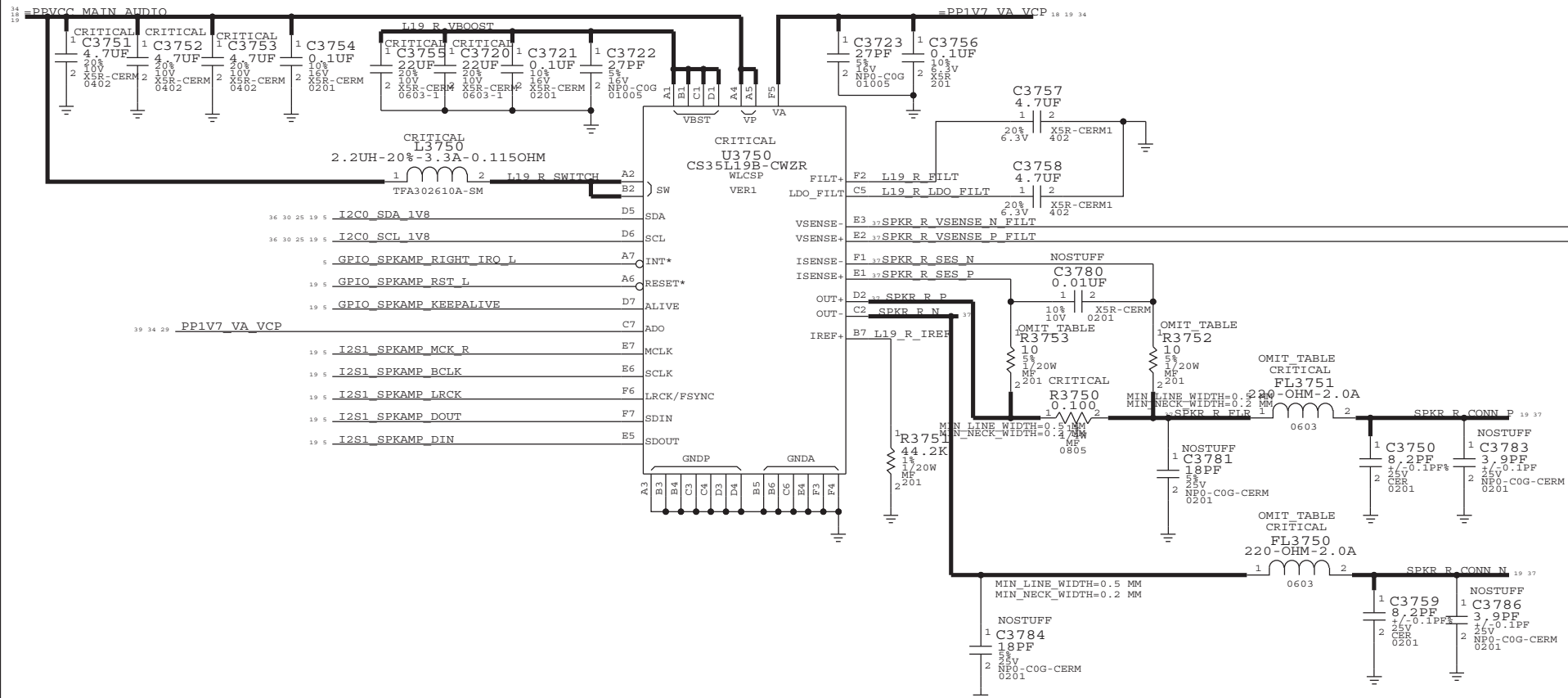
I2C ADDRESS: 1000000X

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
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113S0022	4	RES,MP,1/10W,00HM,5,0603,SMD,LP	FL3740,FL3741,FL3750,FL3751	?	?

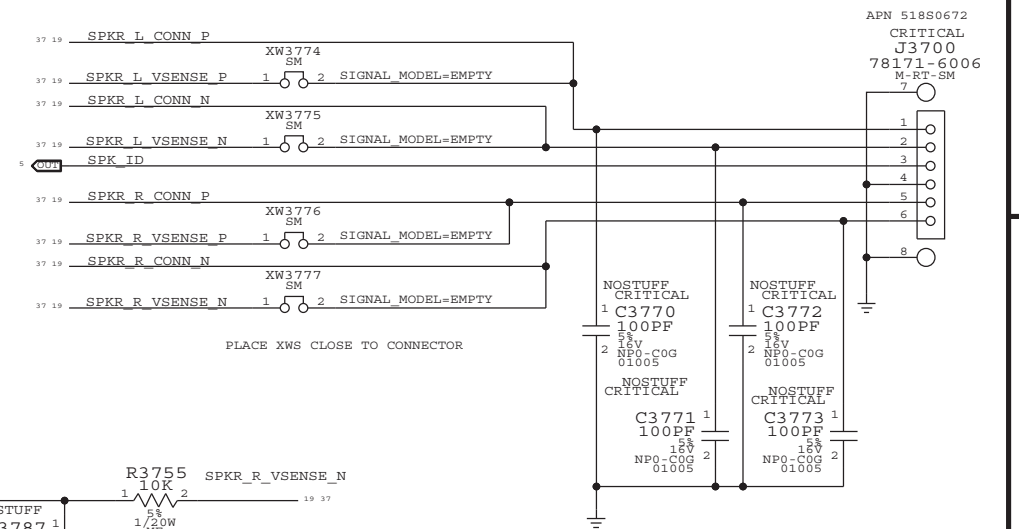


RIGHT SPEAKER AMP

I2C ADDRESS: 1000001X



SPEAKER CONNECTOR



SYNC MASTER=N/A		SYNC DATE=N/A	
AUDIO: SPEAKER AMP			
Apple Inc.		DRAWING NUMBER	SIZE
		051-9385	D
		REVISION	
		A.0.0	
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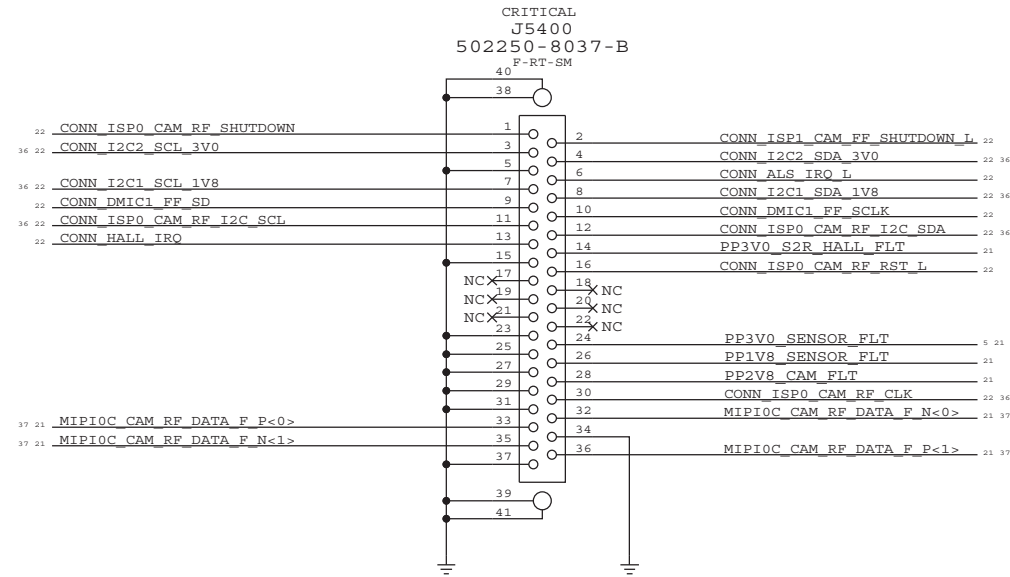
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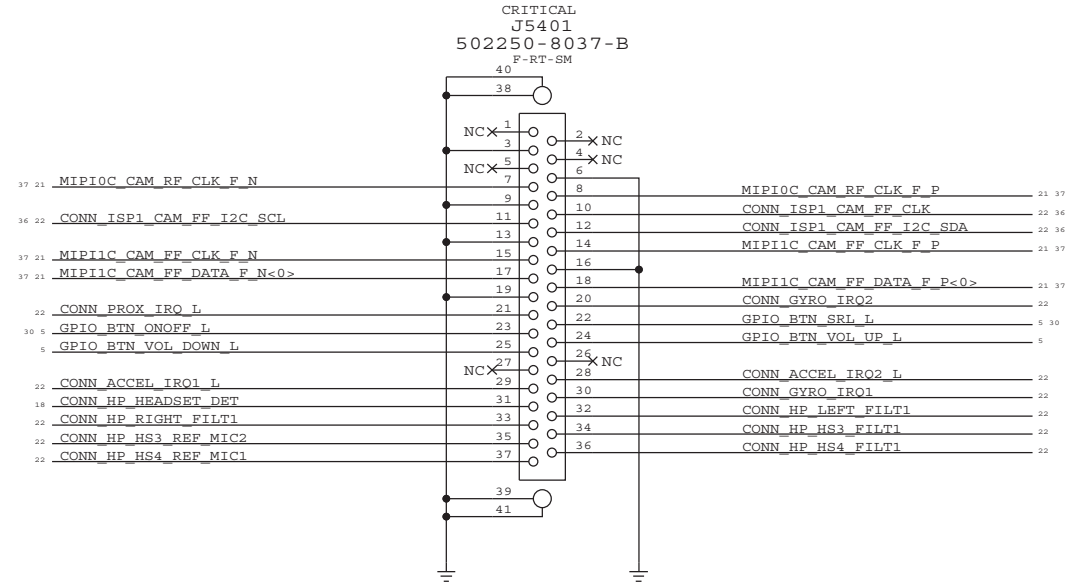
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APN: 518S0828



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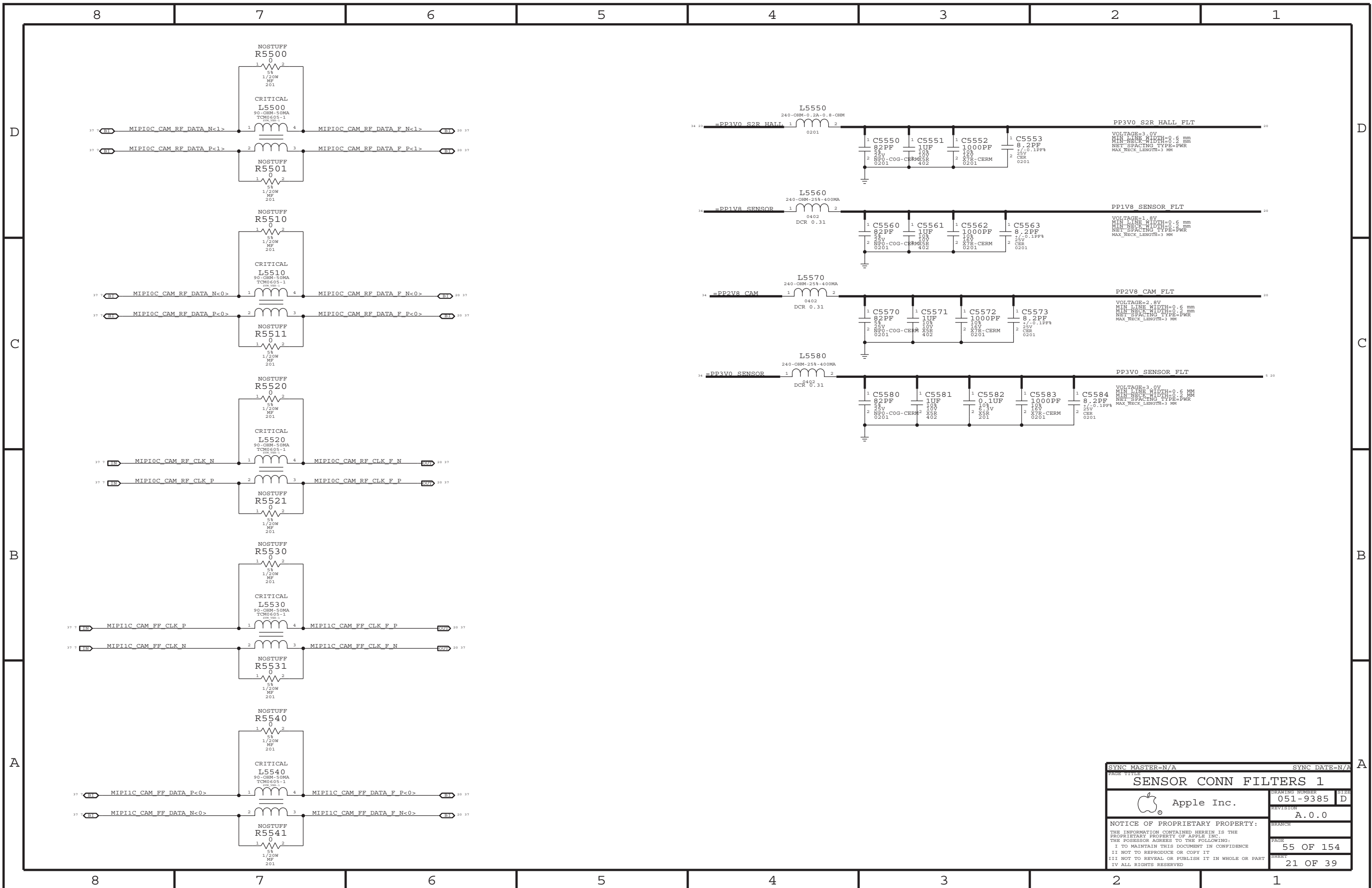
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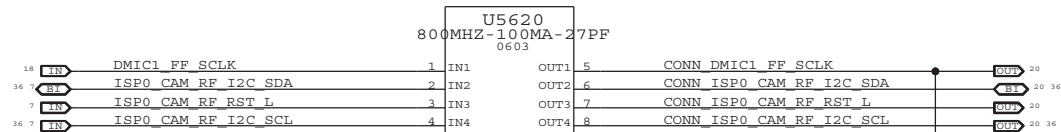
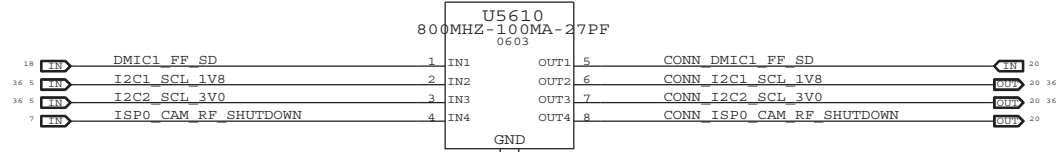
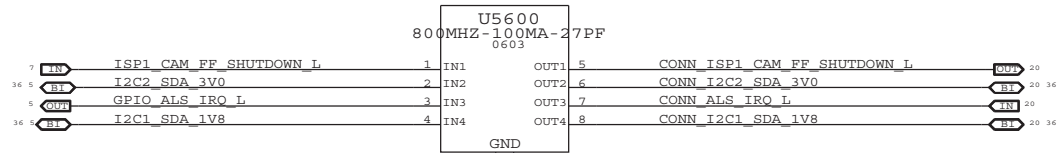
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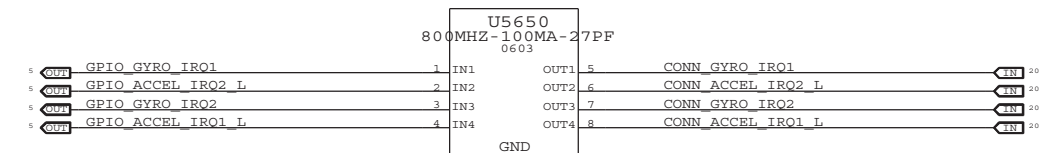
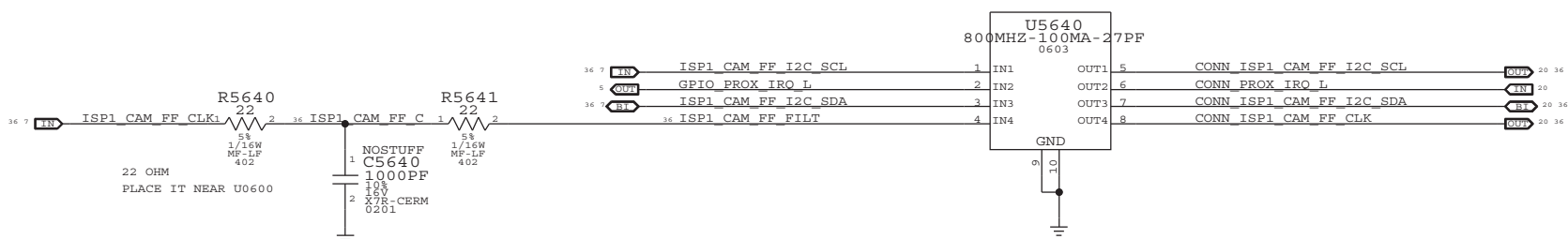
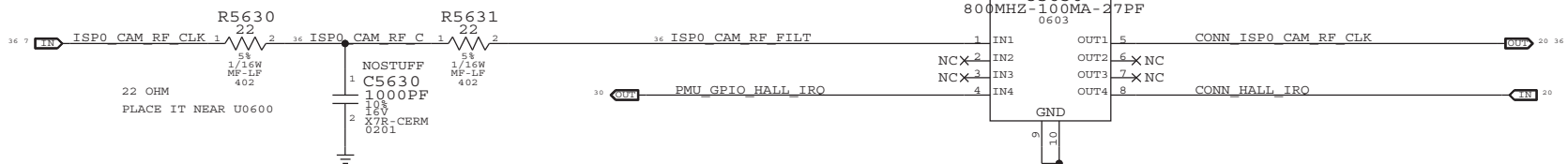
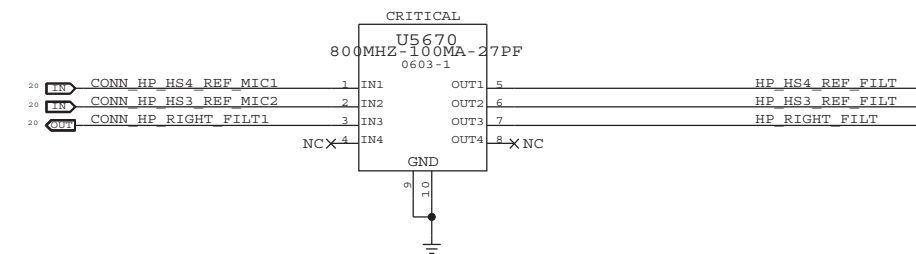
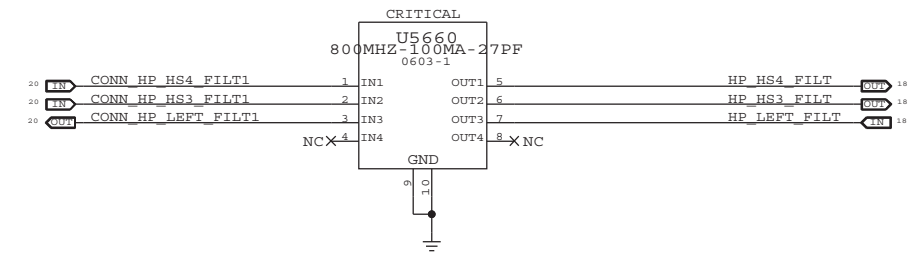
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		DRAWING NUMBER	051-9385
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		PAGE	55 OF 154
		SHEET	21 OF 39
		SIZE	D

PART NUMBER	ALTERNATE FOR PART NUMBER	BOB OPTION	REF DES	COMMENTS
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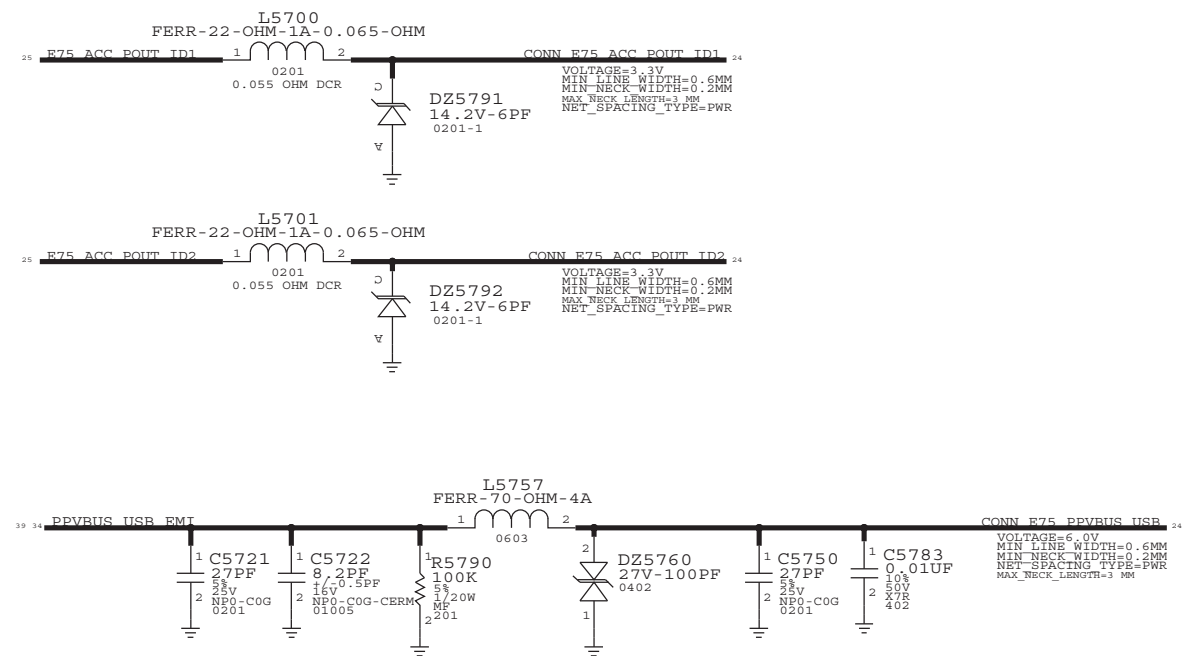


DO NOT STUFF WITHOUT AUDIO TEAM APPROVAL AND RECHARACTERIZATION

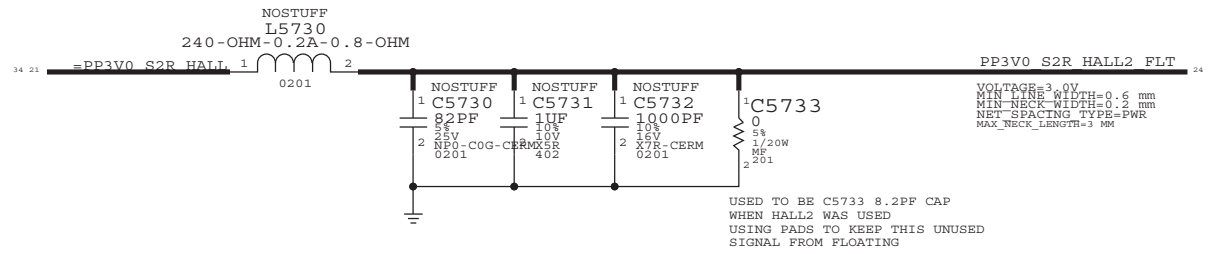
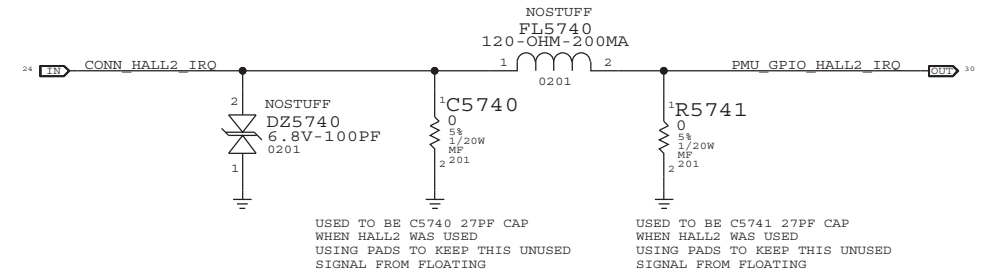
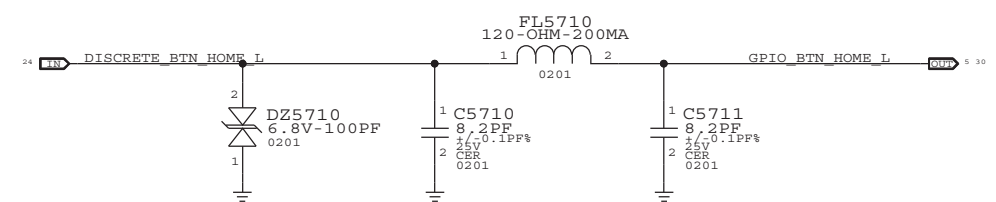
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1 C5620
27PF
5V
2 NPO-COG
0201



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DRAWING NUMBER: 051-9385		SIZE: D	
REVISION: A.0.0		BRANCH:	
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PAGE: 56 OF 154		SHEET: 22 OF 39	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0116	377S0108		DZ5760	RDAR://PROBLEM/8370432
155S0320	155S0513		L5700, L5701	RDAR://PROBLEM/9625601
155S0657	155S0537		FL5710, FL5790	
155S0741	155S0397		L5757	RDAR://PROBLEM/1123881



SYNC MASTER=N/A		SYNC DATE=N/A	
E75 DOCK SUPPORT			
Apple Inc.		DRAWING NUMBER	SIZE
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		A.0.0	
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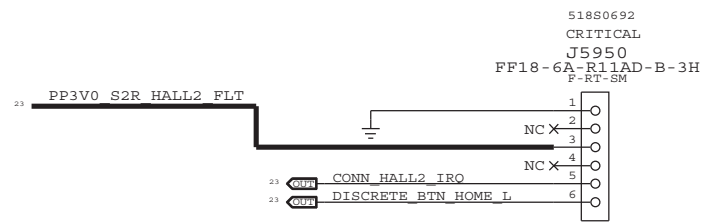
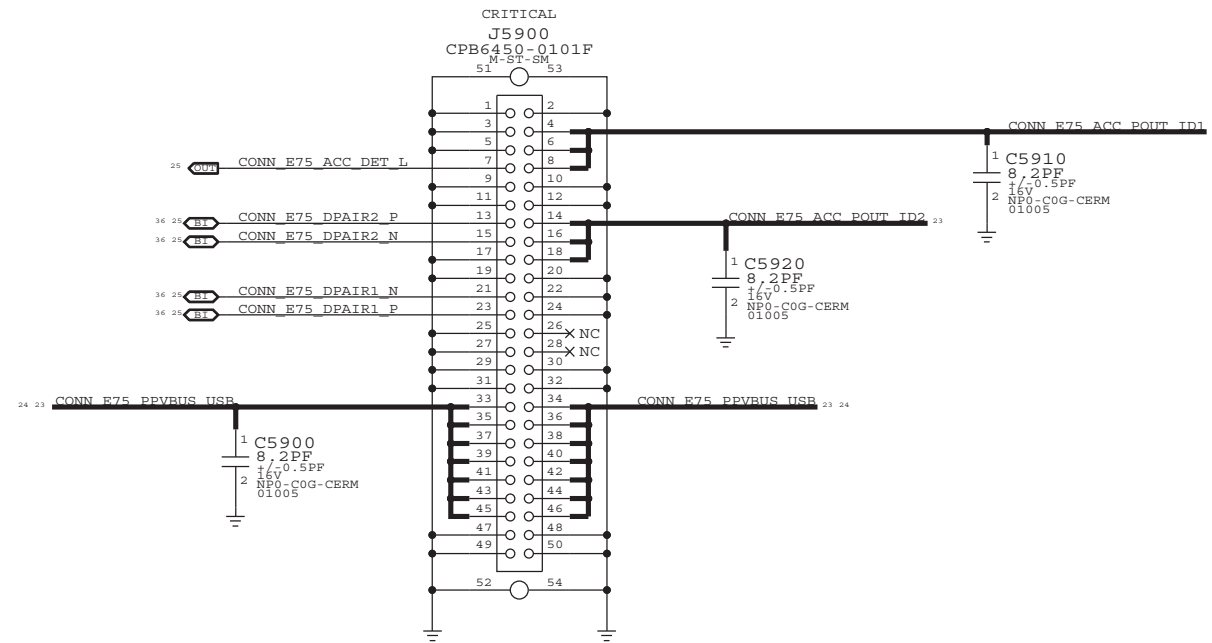
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IO FLEX CONNECTOR

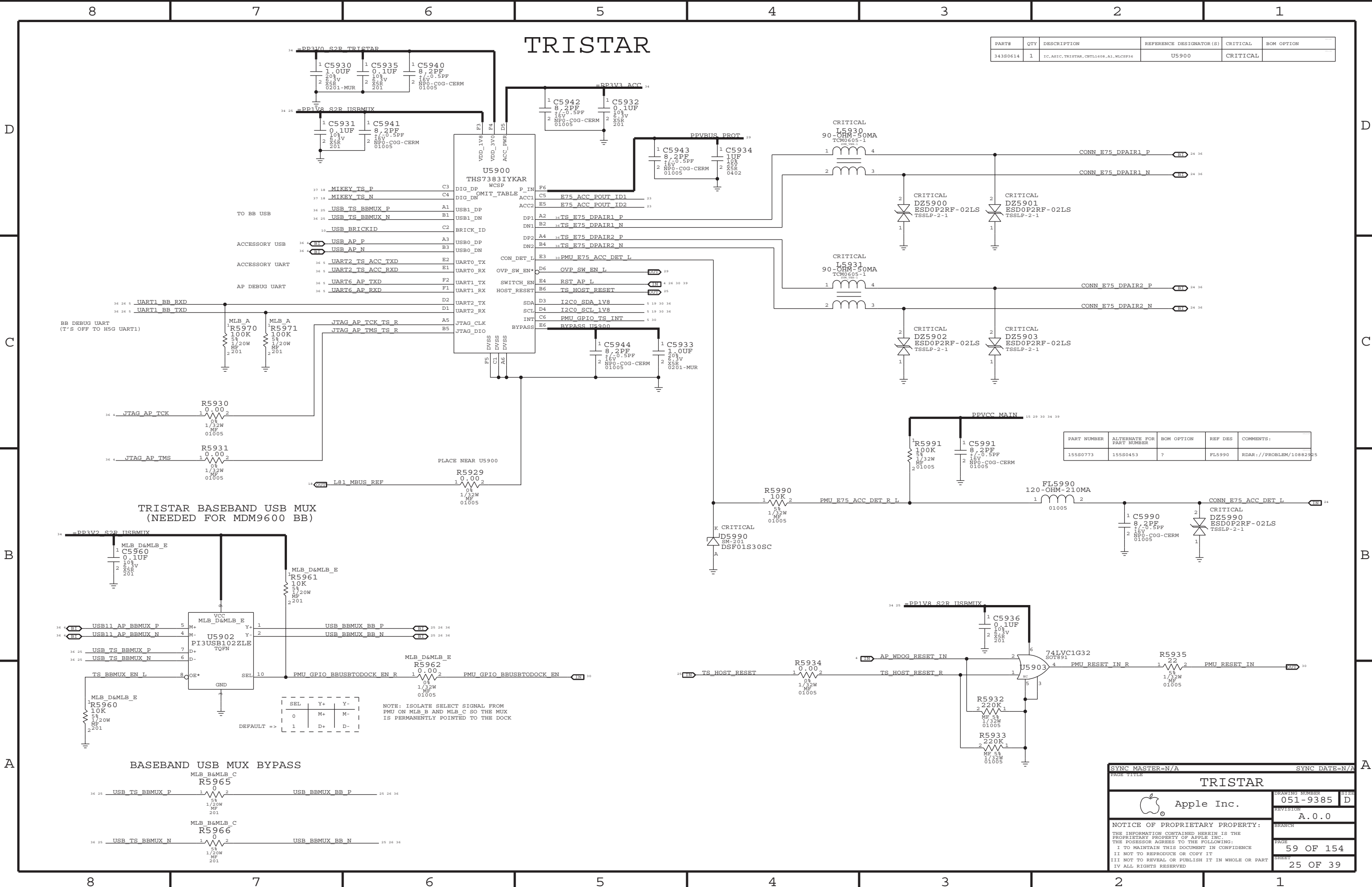
PN 516S0542 (PLUG - MALE)



SYNC MASTER=N/A		SYNC DATE=N/A	
IO FLEX CONN			
Apple Inc.		DRAWING NUMBER	SIZE
		051-9385	D
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		PAGE	58 OF 154
		SHEET	24 OF 39

TRISTAR

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0614	1	IC,ASIC,TRISTAR,CSTL1608,A1,MLCSP36	U5900	CRITICAL	



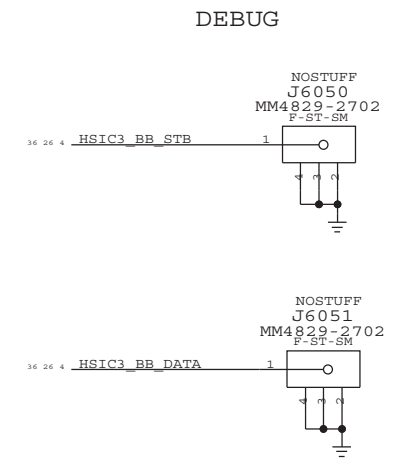
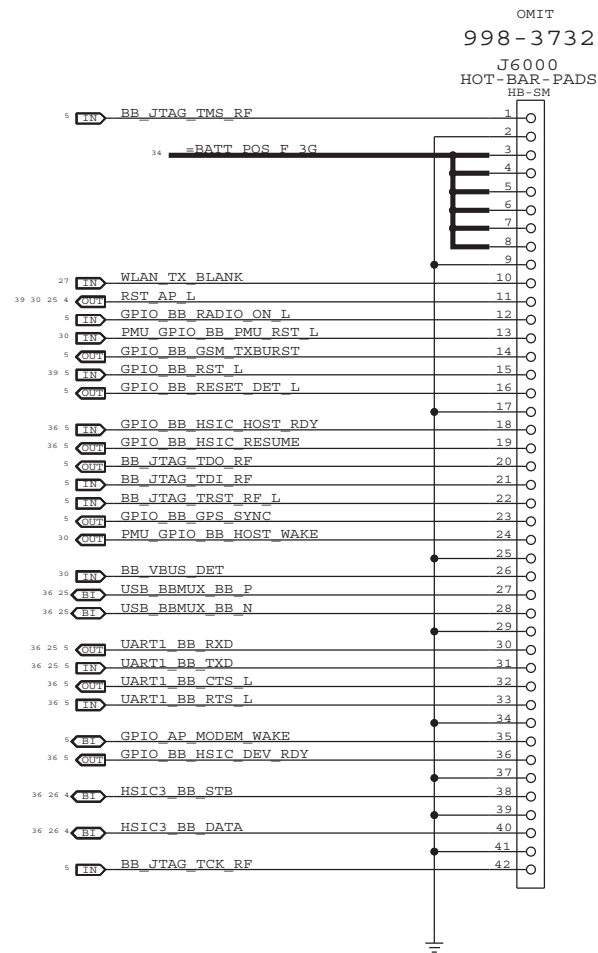
TRISTAR BASEBAND USB MUX (NEEDED FOR MDM9600 BB)

BASEBAND USB MUX BYPASS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
155580773	155580453	?	FL5990	RDAR://PROBLEM/10882925

SYNC MASTER=N/A		SYNC DATE=N/A	
TRISTAR			
Apple Inc.		DRAWING NUMBER	SIZE
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A.0.0		59 OF 154	25 OF 39

CELLULAR/GPS HOTBAR PADS



SYNC MASTER=N/A		SYNC DATE=N/A	
CONNECTOR: CELLULAR			
Apple Inc.		DRAWING NUMBER 051-9385	SIZE D
		REVISION A.0.0	BRANCH
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WLAN/BT

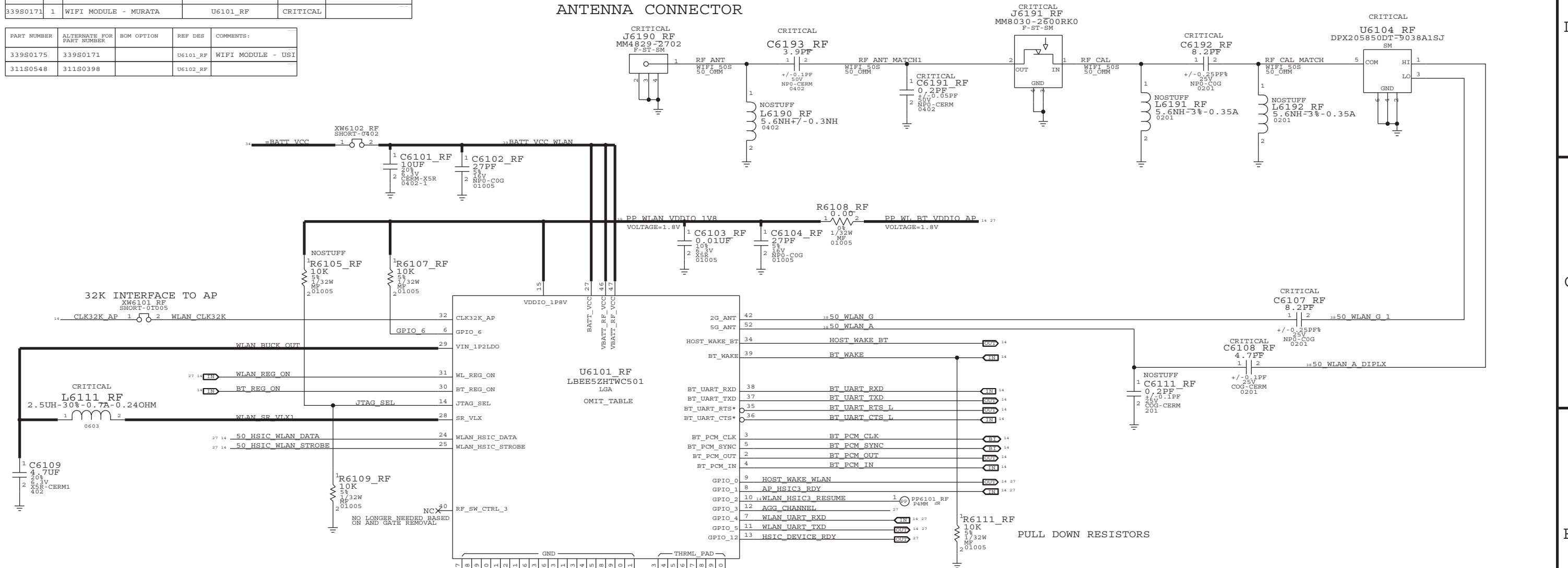
CONFIDENTIAL AND PROPRIETARY APPLE SYSTEM DESIGN

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
339S0171	1	WIFI MODULE - MURATA	U6101_RF	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
339S0175	339S0171		U6101_RF	WIFI MODULE - USI
311S0548	311S0398		U6102_RF	

ANTENNA CONNECTOR

CONDUCTED TEST PORT



GPIO6	SDIO_DATA<1>	SDIO_DATA<2>	MODE	DEFAULT ARM STATE
0	X	X	SDIO	IN RESET
1	X	0	GSPI	IN RESET
1	0	1	HSIC	OUT OF RESET
1	1	1	BOOTLESS HSIC	IN RESET

CHANGE LIST

- 07FEB2012 MUSHTAQ COPIED FROM N41, ADDED J2 ANT MATCH/CONN C6107 FROM 20PF TO 8.2PF, C6108 FROM 10PF TO 4.7PF U6104 FROM SOSHIN TO MURATA LFD212G45DS5D355
- 13FEB2012 AMANDA CHANGED OMIT TO OMIT TABLE AND UPDATED BOM OPTION TABLES TO ALTERNATE TABLES REMOVED BOM TABLE FOR C6111_RF (NOW ALWAYS NOSTUFF)

27 14	WLAN_REG_ON	1	PP6102_RF
27 14	HOST_WAKE_WLAN	1	PP6103_RF
27 14	AP_HSIC3_RDY	1	PP6104_RF
27 14	DEV_HSIC3_RDY	1	PP6105_RF
27 14	WLAN_UART_RXD	1	PP6106_RF
27 14	WLAN_UART_TXD	1	PP6107_RF
27 14	AGG_CHANNEL	1	PP6109_RF
27 14	50_HSIC_WLAN_DATA	1	PP6110_RF
27 14	50_HSIC_WLAN_STROBE	1	PP6111_RF
27 14	HSIC_DEVICE_RDY	1	PP6112_RF

PAGE TITLE		SYNC DATE=N/A	
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Apple Inc.		DRAWING NUMBER	SIZE
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		27 OF 39	

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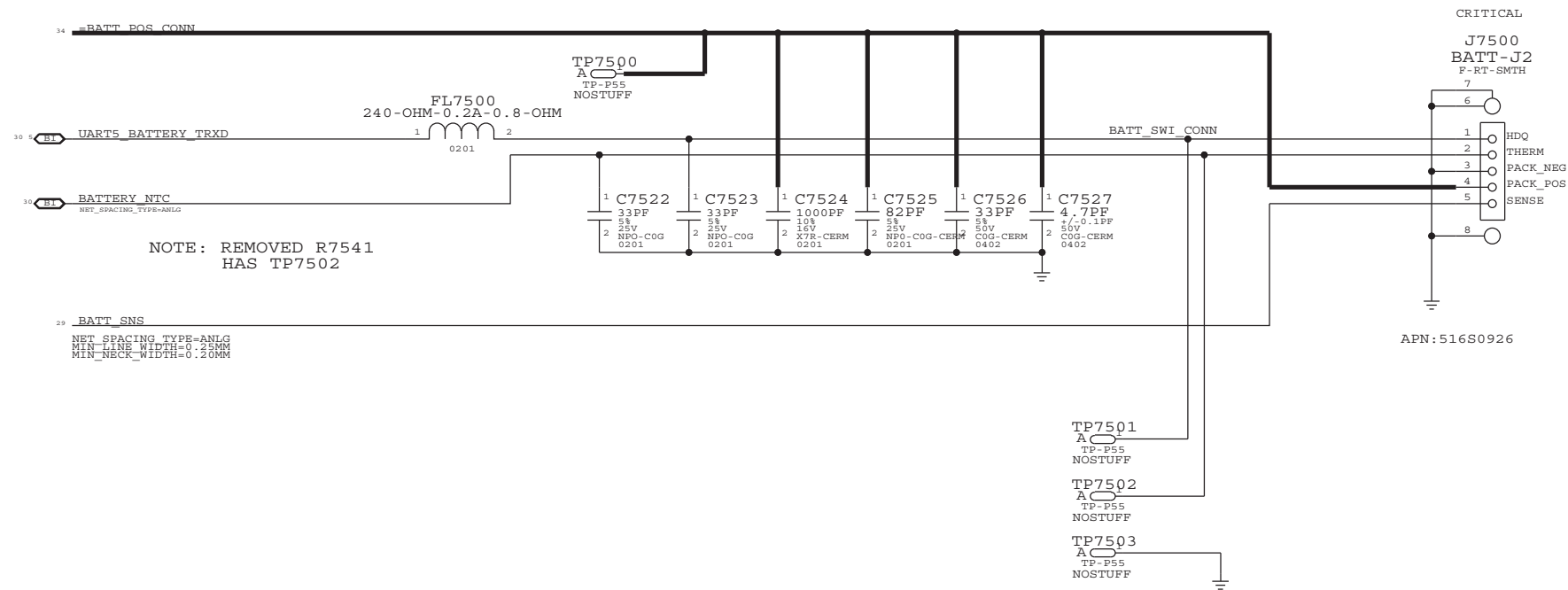
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PART NUMBER	ALTERNATE FOR PART NUMBER	BOB OPTION	REF DES	COMMENTS
155S0644	155S0274	?		RDAR://PROBLEM/11282371

FL7500, L3620, L5550, L5730



SYNC MASTER=MADHAVI		SYNC DATE=12/06/2011	
POWER: BATTERY CONNECTOR			
Apple Inc.		DRAWING NUMBER 051-9385	SIZE D
		REVISION A.0.0	BRANCH
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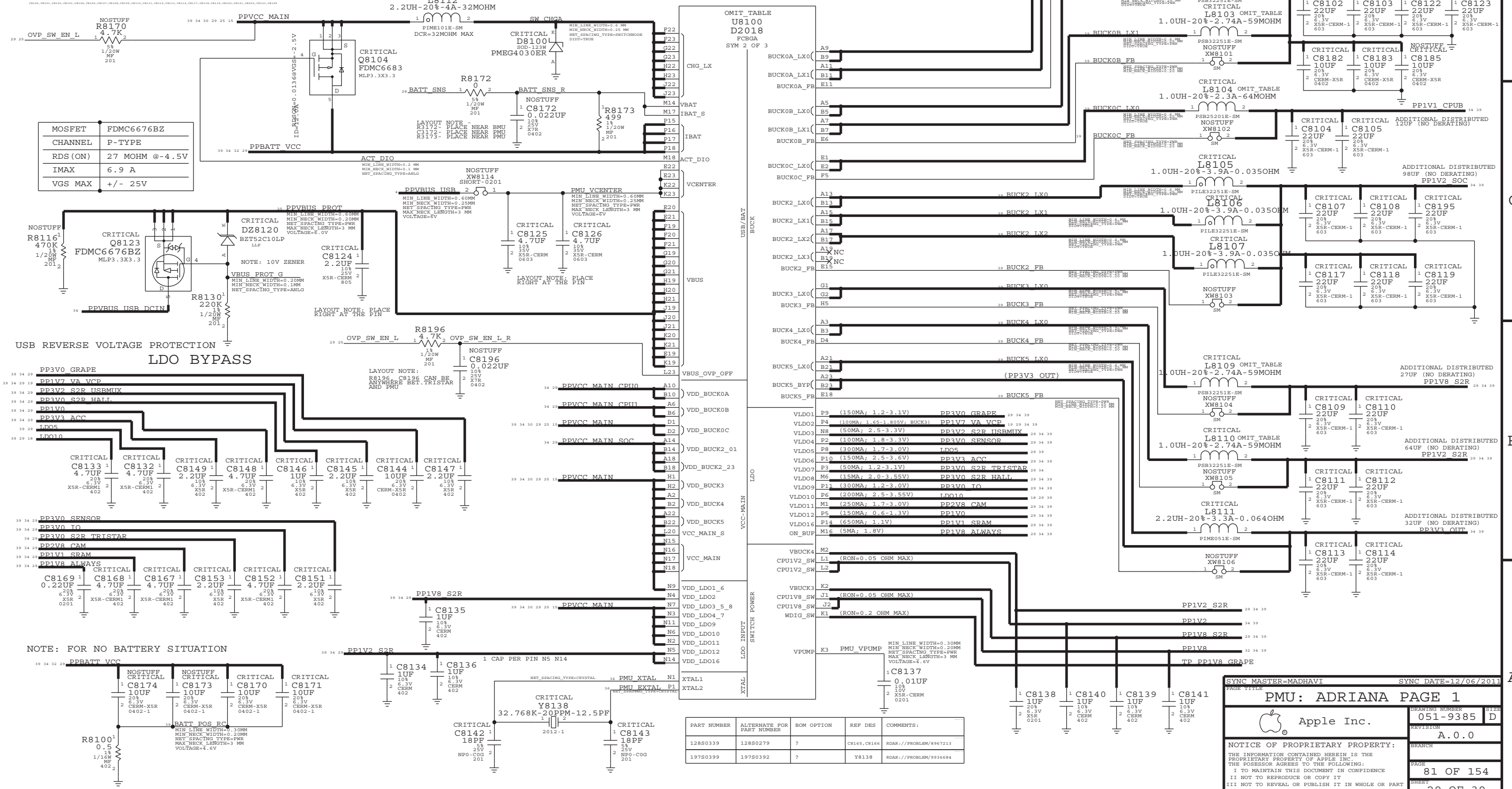
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VCC MAIN BYPASS
TOTAL CAPS = ~400UF
PLACE ONE 10UF CAP
AT EACH VDD INPUT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S1637	6	IND, 1.0UH, 20%, 59MO, 2.74A	L8100, L8101, L8102, L8103, L8104, L8110	CRITICAL	
152S1638	1	IND, 1.0UH, 20%, 64MO, 2.3A	L8104	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S1452	152S1292	?	L8111	RDAR://PROBLEM/8376462
138S0676	138S0654	?	?	?

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0339	128S0279	?	C8165, C8166	RDAR://PROBLEM/8967213
197S0399	197S0392	?	Y8138	RDAR://PROBLEM/9336464

SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PMU: ADRIANA PAGE 1

Apple Inc.

DRAWING NUMBER: 051-9385 D

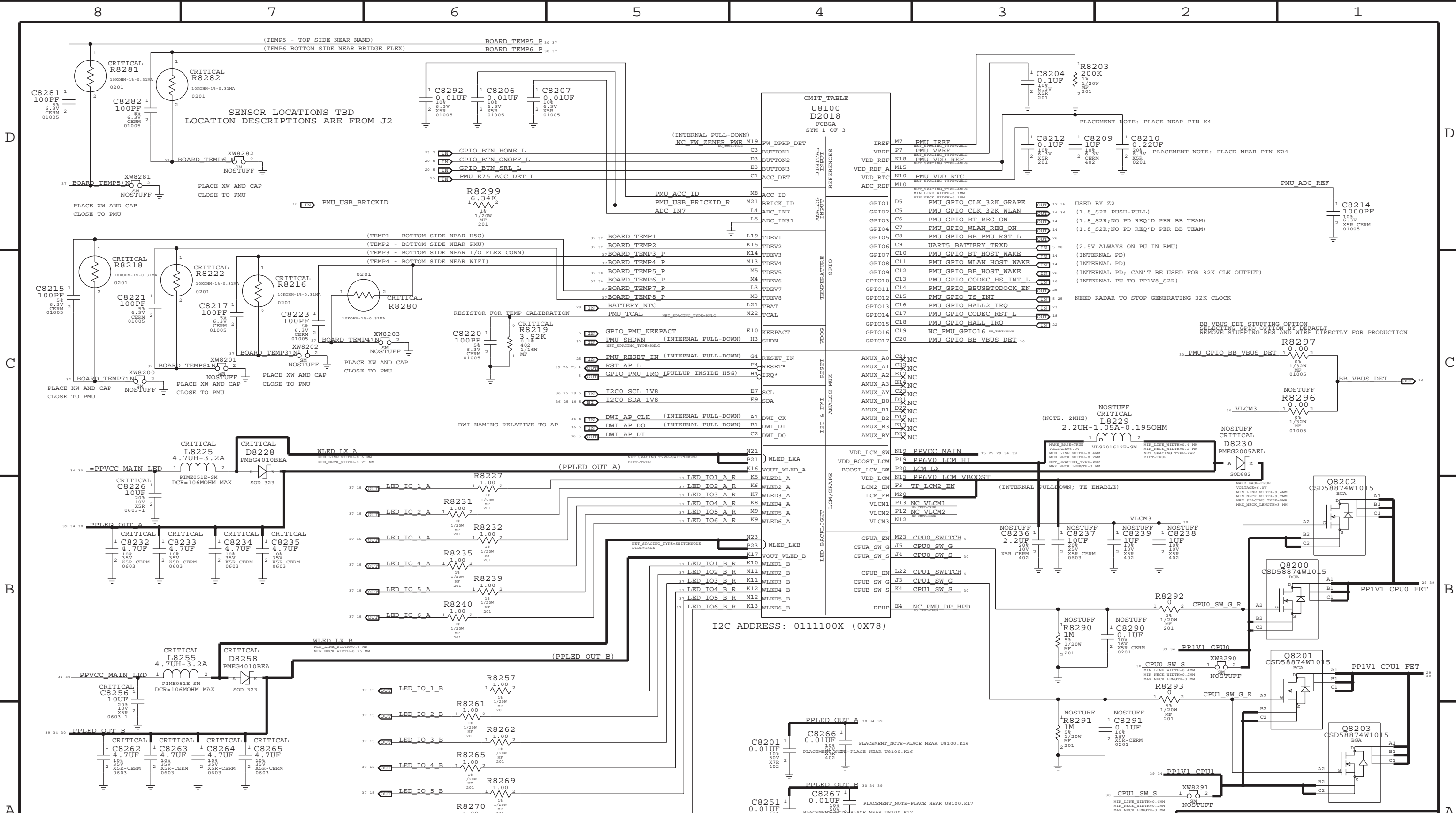
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PAGE: 81 OF 154

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PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS
10780150	10780208	?		RDAR://PROBLEM/8180367

SYNC MASTER=MADHAVI SYNC DATE=12/06/2011

PMU: ADRIANA PAGE 2

Apple Inc.

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REVISION: A.0.0

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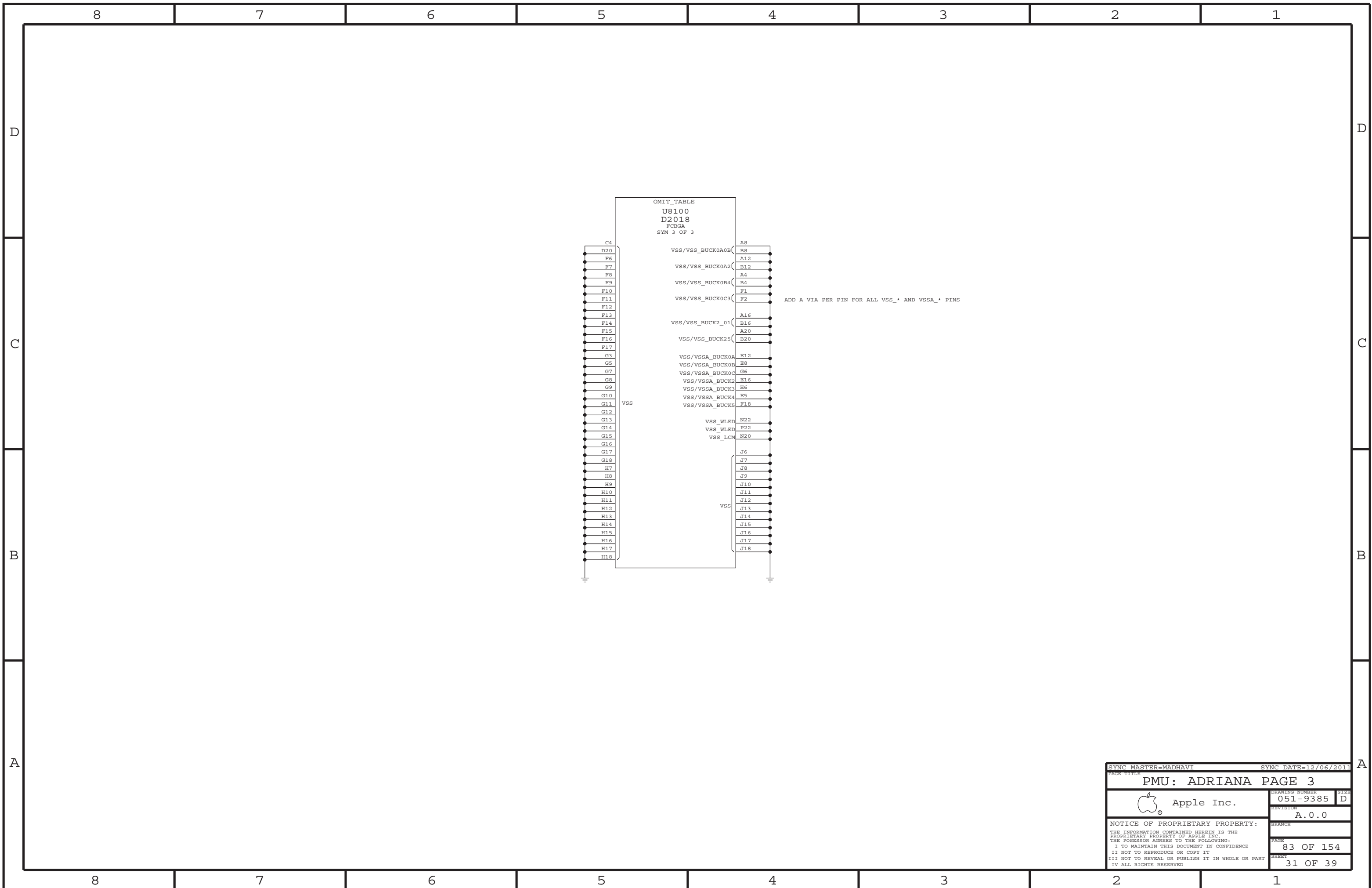
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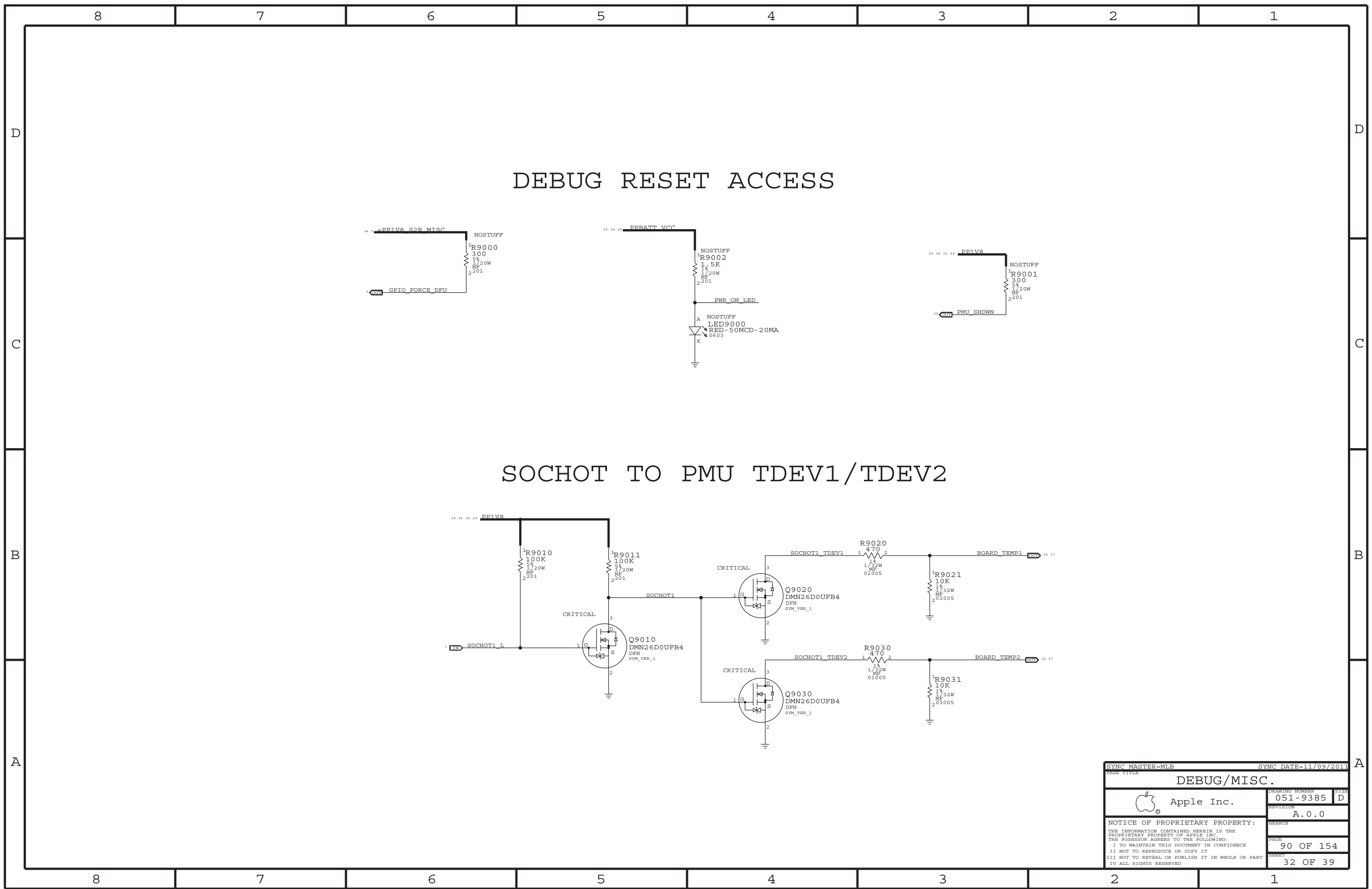
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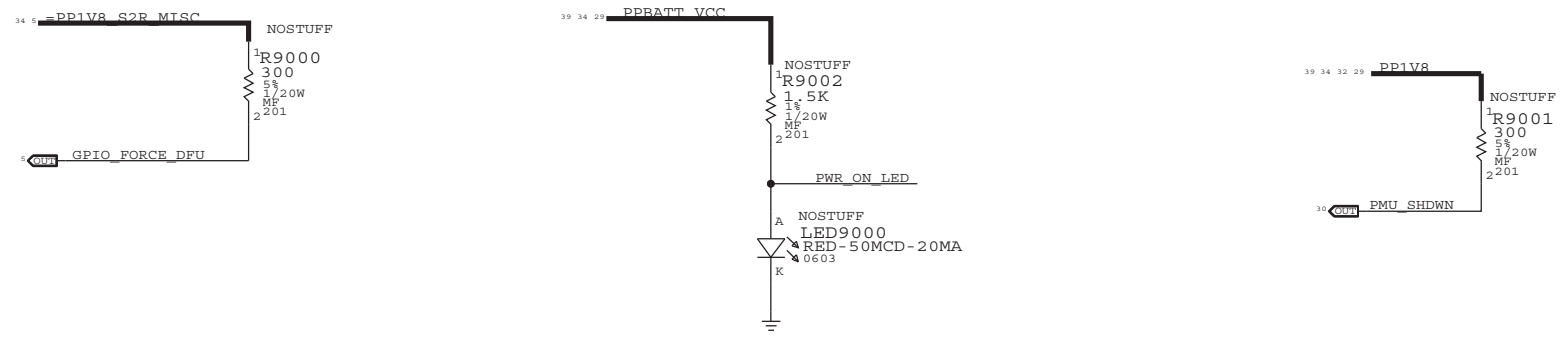
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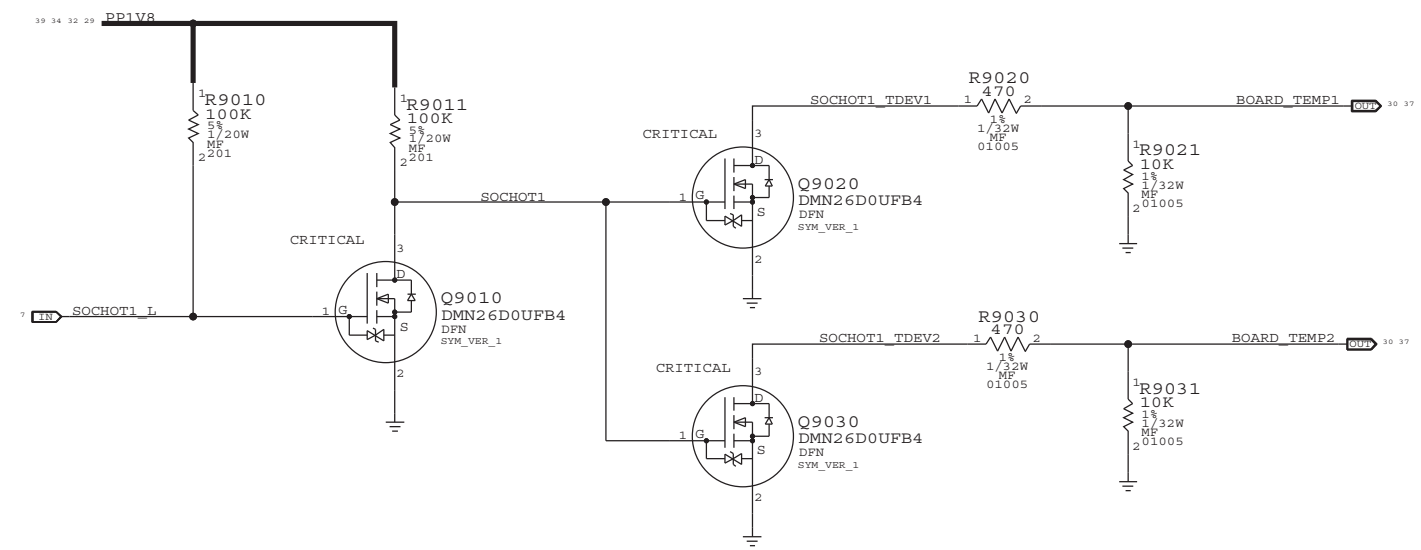
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		SHEET 31 OF 39	




DEBUG RESET ACCESS



SOCHOT TO PMU TDEV1/TDEV2



SYNC MASTER=MLB		SYNC DATE=11/09/2011	
DEBUG/MISC.			
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		051-9385	D
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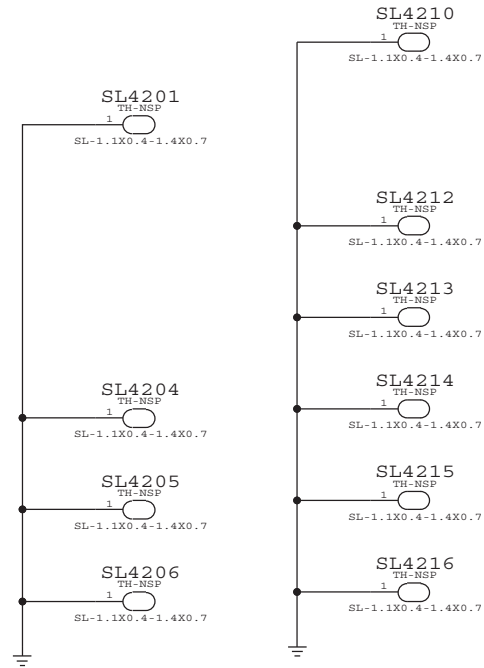
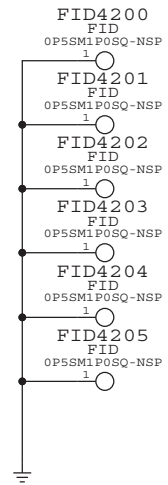
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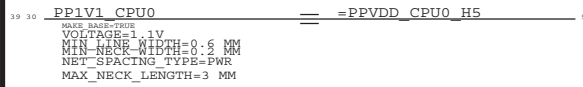
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 PLATING SIZE: 1.4MM X 0.7MM



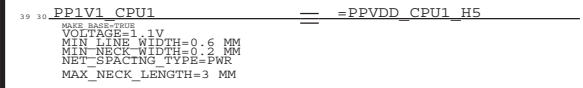
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Apple Inc.	DRAWING NUMBER	051-9385	SIZE D
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		SHEET	33 OF 39

POWER CONNECTIONS

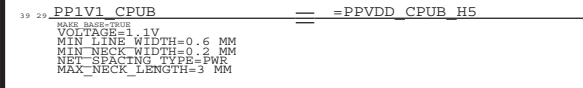
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BUCK0B



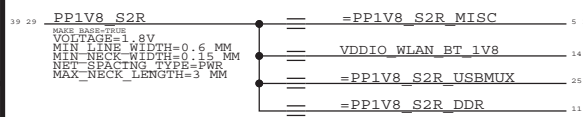
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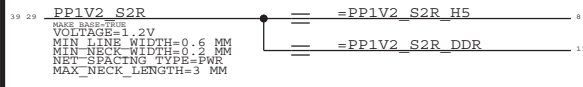
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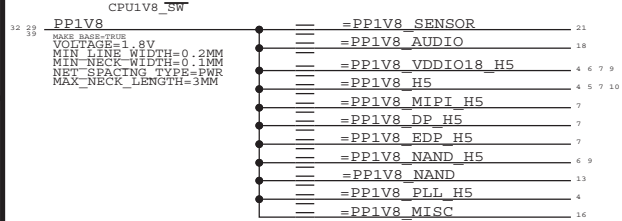
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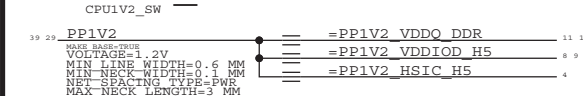
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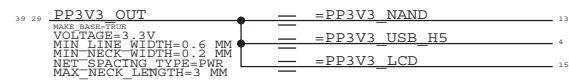
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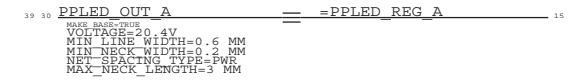
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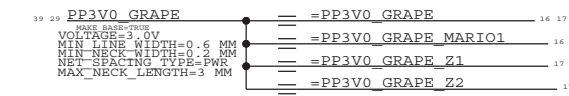
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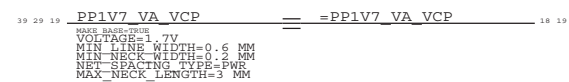
BACKLIGHT BOOST



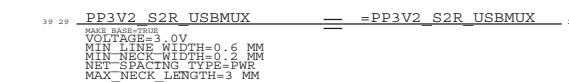
LDO1



LDO2



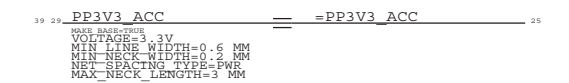
LDO3 (NO LONGER NEEDED)



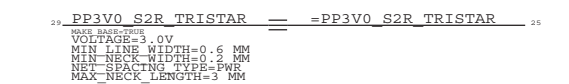
LDO4



LDO6



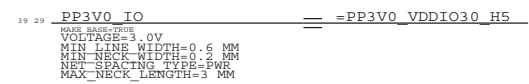
LDO7



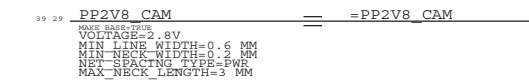
LDO8



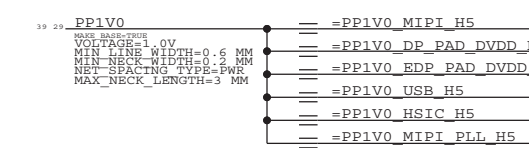
LDO9



LDO11



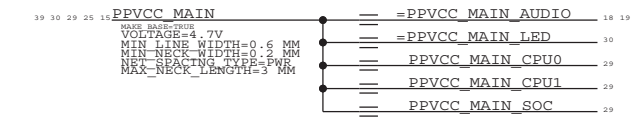
LDO12



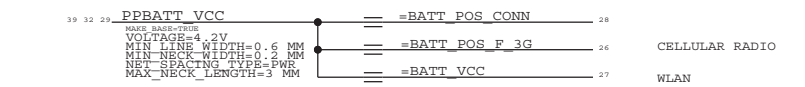
LDO16



CHARGER MAIN



BATTERY



USB POWER INPUT



PAGE TITLE		SYNC DATE=N/A	
POWER ALIASES			
Apple Inc.	DRAWING NUMBER	051-9385	SIZE
	REVISION	A.0.0	
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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA, BGA06-06, BGA_P4	MM	16.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	3.0 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

**SINGLE-ENDED PHYSICAL RULES
45 OHMS**

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL2, ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL3, ISL8	Y	0.065 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4, ISL7	Y	0.053 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL5	Y	0.072 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL6	Y	0.059 MM	0.055 MM	3.0 MM		

90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP, BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
90_OHM_DIFF	ISL2, ISL9	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL3, ISL8	Y	0.062 MM	0.052 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL4, ISL7	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
90_OHM_DIFF	ISL5, ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.105 MM	0.105 MM

DDR 45 OHMS SINGLE-ENDED PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_45_OHM_SE	TOP, BOTTOM	Y	0.105 MM	0.105 MM	3.0 MM		
DDR_45_OHM_SE	ISL2	Y	0.055 MM	0.055 MM	3.0 MM		
DDR_45_OHM_SE	ISL3	Y	0.065 MM	0.065 MM	3.0 MM		
DDR_45_OHM_SE	ISL4	Y	0.053 MM	0.053 MM	3.0 MM		
DDR_45_OHM_SE	ISL5, ISL6	Y	0.072 MM	0.072 MM	3.0 MM		
DDR_45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

DDR 90 OHMS DIFFERENTIAL PAIR PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DDR_90_OHM_DIFF	TOP, BOTTOM	Y	0.090 MM	0.090 MM	=STANDARD	0.170 MM	0.170 MM
DDR_90_OHM_DIFF	ISL2	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL3	Y	0.062 MM	0.062 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL4	Y	0.051 MM	0.051 MM	=STANDARD	0.190 MM	0.190 MM
DDR_90_OHM_DIFF	ISL5, ISL6	Y	0.066 MM	0.066 MM	=STANDARD	0.180 MM	0.180 MM
DDR_90_OHM_DIFF	*	N	0.056 MM	0.056 MM	=STANDARD	0.180 MM	0.180 MM

WIFI PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
WIFI_50S	TOP, BOTTOM	Y	0.245 MM	0.2 MM	=STANDARD		
WIFI_50S	*	N	=STANDARD	=STANDARD	=STANDARD		
WIFI_PWR100	*	Y	0.10 MM	0.050 MM	=STANDARD		
WIFI_PWR100	*	Y	1.00 MM	0.100 MM	=STANDARD		

MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20 MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.09 MM	10 MM	0.10 MM	0.10 MM
LED	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM
TEMP_SENSE	*	Y	0.1 MM	0.09 MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

TCF VERSION (USING SPACING RULE)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TCF_VERSION	*	0.104 MM	?

0.104 - 11/30/2011

TCF_VERSION NC_UART5_TXD ASSIGNING RULE TO NC NET

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.100 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?
BGA_P4_SPA	*	0.200 MM	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.050 MM	?
OP08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.075 MM	?
2:1_SPACING	*	0.100 MM	?
2.5:1_SPACING	*	0.125 MM	?
3:1_SPACING	*	0.150 MM	?
4:1_SPACING	*	0.200 MM	?
5:1_SPACING	*	0.250 MM	?
OP5MM_SPACING	*	0.5 MM	?
OP64MM_SPACING	*	0.64 MM	?
OP2_SPACING	*	0.20 MM	?

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

POWER


PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PWR	*	Y	0.6MM	0.20 MM	3.0 MM		
GND_PH	*	Y	0.6MM	0.075 MM	3.0 MM		
PWR_PMU	*	Y	0.6MM	0.20 MM	3.0 MM		

MISC

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING
*	*	BGA_P4	BGA_P4_SPA

NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

CONSTRAINTS: MLB RULES	
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Clock Signal Constraints

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: CLK_50S, *, 45_OHM_SE

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: CLK, *, *, 3:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for PMU GPIO CLK, ISPI CAM FF CLK, I2S0 CODEC ASP MCK, etc.

UART

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: UART_50S, *, 45_OHM_SE

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: UART, *, *, 3:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for UART2 TS ACC RXD, UART4 WLAN RXD, etc.

SPI

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: SPI_50S, *, 45_OHM_SE

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: SPI, *, *, 2:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for SPI3 GRAPE MISO, SPI2 IPC MISO, etc.

DWI

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: DWI, *, *, 2:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for DWI AP CLK, DWI AP DI, DWI AP DO

JTAG

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: JTAG, *, *, 2:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for JTAG AP TCK, JTAG AP TMS, etc.

I2C

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: I2C_50S, *, 45_OHM_SE

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: I2C, *, *, 1.5:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for I2C1 SDA 1V8, I2C0 SDA 1V8, etc.

XTAL

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: CRYSTAL, *, *, 5:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for XTAL AP 24M I, XTAL AP 24M O, etc.

I2S

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: I2S_50S, *, 45_OHM_SE

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: I2S, *, *, 3:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for I2S0 CODEC ASP BCLK, I2S3 CODEC XSP BCLK, etc.

USB

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: USB_90D, *, 90_OHM_DIFF

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: USB, *, *, 4:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for USB AP P, USB AP N, USB BBMUX BB P, etc.

HSIC

Table with 3 columns: NET_PHYSICAL_TYPE, AREA_TYPE, PHYSICAL_RULE_SET. Row 1: HSIC, *, 45_OHM_SE

Table with 4 columns: NET_SPACING_TYPE1, NET_SPACING_TYPE2, AREA_TYPE, SPACING_RULE_SET. Row 1: HSIC, *, *, 4:1_SPACING

Table with 4 columns: ELECTRICAL_CONSTRAINT_SET, PHYSICAL, NET_TYPE, SPACING. Lists constraints for HSIC3 BB DATA, HSIC3 BB STB, etc.

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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI0C	*	*	4:1_SPACING
MIPI1C	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_P	7 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_N	7 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<0>	7 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<0>	7 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_P<1>	7 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_N<1>	7 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_P	20 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_CLK_F_N	20 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<0>	20 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<0>	20 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_P<1>	20 21
HE80	MIPI_90D	MIPI0C	MIPI0C_CAM_RF_DATA_F_N<1>	20 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_P	7 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_N	7 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_P<0>	7 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_N<0>	7 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_P	20 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_CLK_F_N	20 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_P<0>	20 21
HE80	MIPI_90D	MIPI1C	MIPI1C_CAM_FF_DATA_F_N<0>	20 21

AUDIO/SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HE80	AUDIO_DIFF	AUDIO	HP_MIC_P	18
HE80	AUDIO_DIFF	AUDIO	HP_MIC_N	18
HE80	AUDIO_DIFF	AUDIO	L81_AIN2_P	18
HE80	AUDIO_DIFF	AUDIO	L81_AIN2_N	18
HE80	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N_FILT	19
HE80	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P_FILT	19
HE80	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_N	19
HE80	AUDIO_DIFF	AUDIO	SPKR_L_VSENSE_P	19
HE80	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N_FILT	19
HE80	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P_FILT	19
HE80	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_N	19
HE80	AUDIO_DIFF	AUDIO	SPKR_R_VSENSE_P	19
HE80	SPEAKER	AUDIO	SPKR_L_P	19
HE80	SPEAKER	AUDIO	SPKR_L_N	19
HE80	SPEAKER	AUDIO	SPKR_L_CONN_P	19
HE80	SPEAKER	AUDIO	SPKR_L_CONN_N	19
HE80	SPEAKER	AUDIO	SPKR_R_P	19
HE80	SPEAKER	AUDIO	SPKR_R_N	19
HE80	SPEAKER	AUDIO	SPKR_R_CONN_P	19
HE80	SPEAKER	AUDIO	SPKR_R_CONN_N	19
HE80	SPEAKER	AUDIO	SPKR_L_FLR	19
HE80	SPEAKER	AUDIO	SPKR_R_FLR	19
HE80	AUDIO_DIFF	AUDIO	SPKR_L_SES_N	19
HE80	AUDIO_DIFF	AUDIO	SPKR_L_SES_P	19
HE80	AUDIO_DIFF	AUDIO	SPKR_R_SES_N	19
HE80	AUDIO_DIFF	AUDIO	SPKR_R_SES_P	19
HE80	USB_90D	USB	MIKEY_TS_P	18 25
HE80	USB_90D	USB	MIKEY_TS_N	18 25
HE80	USB_90D	USB	L81_MBUS_P	18
HE80	USB_90D	USB	L81_MBUS_N	18

EMBEDDED DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET	NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
EDP_90D	*	90_OHM_DIFF	EDP_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
EDP	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HE80	EDP_90D	EDP	EDP_AUX_P	7 15
HE80	EDP_90D	EDP	EDP_AUX_N	7 15
HE80	EDP_90D	EDP	EDP_HPD	7 15
HE80	EDP_90D	EDP	EDP_DATA_P<0>	7 15
HE80	EDP_90D	EDP	EDP_DATA_N<0>	7 15
HE80	EDP_90D	EDP	EDP_DATA_P<1>	7 15
HE80	EDP_90D	EDP	EDP_DATA_N<1>	7 15
HE80	EDP_90D	EDP	EDP_DATA_P<2>	7 15
HE80	EDP_90D	EDP	EDP_DATA_N<2>	7 15
HE80	EDP_90D	EDP	EDP_DATA_P<3>	7 15
HE80	EDP_90D	EDP	EDP_DATA_N<3>	7 15
HE80	EDP_90D	EDP	EDP_AUX_EMI_P	15
HE80	EDP_90D	EDP	EDP_AUX_EMI_N	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_P<0>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_N<0>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_P<1>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_N<1>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_P<2>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_N<2>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_P<3>	15
HE80	EDP_90D	EDP	EDP_DATA_EMI_N<3>	15
HE80	EDP_90D	EDP	CONN_EDP_AUX_EMI_P	15
HE80	EDP_90D	EDP	CONN_EDP_AUX_EMI_N	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<0>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<0>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<1>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<1>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<2>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<2>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_P<3>	15
HE80	EDP_90D	EDP	CONN_EDP_DATA_EMI_N<3>	15

BACKLIGHT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LED	*	LED

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LEDA	*	*	3:1_SPACING
LEDB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HE80	LED	LEDA	LED_I01_A_R	30
HE80	LED	LEDB	LED_I01_B_R	30
HE80	LED	LEDA	LED_I02_A_R	30
HE80	LED	LEDB	LED_I02_B_R	30
HE80	LED	LEDA	LED_I03_A_R	30
HE80	LED	LEDB	LED_I03_B_R	30
HE80	LED	LEDA	LED_I04_A_R	30
HE80	LED	LEDB	LED_I04_B_R	30
HE80	LED	LEDA	LED_I05_A_R	30
HE80	LED	LEDB	LED_I05_B_R	30
HE80	LED	LEDA	LED_I06_A_R	30
HE80	LED	LEDB	LED_I06_B_R	30
HE80	LED	LEDA	LED_I01_A	15 30
HE80	LED	LEDB	LED_I01_B	15 30
HE80	LED	LEDA	LED_I02_A	15 30
HE80	LED	LEDB	LED_I02_B	15 30
HE80	LED	LEDA	LED_I03_A	15 30
HE80	LED	LEDB	LED_I03_B	15 30
HE80	LED	LEDA	LED_I04_A	15 30
HE80	LED	LEDB	LED_I04_B	15 30
HE80	LED	LEDA	LED_I05_A	15 30
HE80	LED	LEDB	LED_I05_B	15 30
HE80	LED	LEDA	LED_I06_A	15 30
HE80	LED	LEDB	LED_I06_B	15 30

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
BOARD_TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
BOARD_TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE			
	PHYSICAL	SPACING		
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP1	30 32
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP2	30 32
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_P	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP3_N	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_P	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP4_N	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_P	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP5_N	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_P	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP6_N	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_P	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP7_N	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_P	30
HE80	BOARD_TEMP	BOARD_TEMP	BOARD_TEMP8_N	30

SYNC MASTER=MIKE	SYNC DATE=11/30/2011
CONSTRAINTS: DISPLAY/AUDIO	
Apple Inc.	DRAWING NUMBER 051-9385 SIZE D
REVISION A.0.0	BRANCH
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DDR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_50S	*	DDR_45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DDR	*	*	3:1_SPACING

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DDR_90D	*	DDR_90_OHM_DIFF

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
DDR0	DDR_50S	DDR	DDR0_CA<9..0>
DDR0	DDR_50S	DDR	DDR0_DM<3..0>
DDR0	DDR_90D	DDR	DDR0_CK_P
DDR0	DDR_90D	DDR	DDR0_CK_N
DDR0	DDR_50S	DDR	DDR0_CKE<1..0>
DDR0	DDR_50S	DDR	DDR0_CSN<2..0>
DDR0	DDR_50S	DDR	DDR0_ZO
DDR0	DDR_50S	DDR	DDR0_DQ<7..0>
DDR0	DDR_90D	DDR	DDR0_DQS_P<0>
DDR0	DDR_90D	DDR	DDR0_DQS_N<0>
DDR0	DDR_50S	DDR	DDR0_DQ<15..8>
DDR0	DDR_90D	DDR	DDR0_DQS_P<1>
DDR0	DDR_90D	DDR	DDR0_DQS_N<1>
DDR0	DDR_50S	DDR	DDR0_DQ<23..16>
DDR0	DDR_90D	DDR	DDR0_DQS_P<2>
DDR0	DDR_90D	DDR	DDR0_DQS_N<2>
DDR0	DDR_50S	DDR	DDR0_DQ<31..24>
DDR0	DDR_90D	DDR	DDR0_DQS_P<3>
DDR0	DDR_90D	DDR	DDR0_DQS_N<3>
DDR1	DDR_50S	DDR	DDR1_CA<9..0>
DDR1	DDR_50S	DDR	DDR1_DM<3..0>
DDR1	DDR_90D	DDR	DDR1_CK_P
DDR1	DDR_90D	DDR	DDR1_CK_N
DDR1	DDR_50S	DDR	DDR1_CKE<1..0>
DDR1	DDR_50S	DDR	DDR1_CSN<2..0>
DDR1	DDR_50S	DDR	DDR1_ZO
DDR1	DDR_50S	DDR	DDR1_DQ<7..0>
DDR1	DDR_90D	DDR	DDR1_DQS_P<0>
DDR1	DDR_90D	DDR	DDR1_DQS_N<0>
DDR1	DDR_50S	DDR	DDR1_DQ<15..8>
DDR1	DDR_90D	DDR	DDR1_DQS_P<1>
DDR1	DDR_90D	DDR	DDR1_DQS_N<1>
DDR1	DDR_50S	DDR	DDR1_DQ<23..16>
DDR1	DDR_90D	DDR	DDR1_DQS_P<2>
DDR1	DDR_90D	DDR	DDR1_DQS_N<2>
DDR1	DDR_50S	DDR	DDR1_DQ<31..24>
DDR1	DDR_90D	DDR	DDR1_DQS_P<3>
DDR1	DDR_90D	DDR	DDR1_DQS_N<3>
DDR2	DDR_50S	DDR	DDR2_CA<9..0>
DDR2	DDR_50S	DDR	DDR2_DM<3..0>
DDR2	DDR_90D	DDR	DDR2_CK_P
DDR2	DDR_90D	DDR	DDR2_CK_N
DDR2	DDR_50S	DDR	DDR2_CKE<1..0>
DDR2	DDR_50S	DDR	DDR2_CSN<2..0>
DDR2	DDR_50S	DDR	DDR2_ZO
DDR2	DDR_50S	DDR	DDR2_DQ<7..0>
DDR2	DDR_90D	DDR	DDR2_DQS_P<0>
DDR2	DDR_90D	DDR	DDR2_DQS_N<0>
DDR2	DDR_50S	DDR	DDR2_DQ<15..8>
DDR2	DDR_90D	DDR	DDR2_DQS_P<1>
DDR2	DDR_90D	DDR	DDR2_DQS_N<1>
DDR2	DDR_50S	DDR	DDR2_DQ<23..16>
DDR2	DDR_90D	DDR	DDR2_DQS_P<2>
DDR2	DDR_90D	DDR	DDR2_DQS_N<2>
DDR2	DDR_50S	DDR	DDR2_DQ<31..24>
DDR2	DDR_90D	DDR	DDR2_DQS_P<3>
DDR2	DDR_90D	DDR	DDR2_DQS_N<3>
DDR3	DDR_50S	DDR	DDR3_CA<9..0>
DDR3	DDR_50S	DDR	DDR3_DM<3..0>
DDR3	DDR_90D	DDR	DDR3_CK_P
DDR3	DDR_90D	DDR	DDR3_CK_N
DDR3	DDR_50S	DDR	DDR3_CKE<1..0>
DDR3	DDR_50S	DDR	DDR3_CSN<2..0>
DDR3	DDR_50S	DDR	DDR3_ZO
DDR3	DDR_50S	DDR	DDR3_DQ<7..0>
DDR3	DDR_90D	DDR	DDR3_DQS_P<0>
DDR3	DDR_90D	DDR	DDR3_DQS_N<0>
DDR3	DDR_50S	DDR	DDR3_DQ<15..8>
DDR3	DDR_90D	DDR	DDR3_DQS_P<1>
DDR3	DDR_90D	DDR	DDR3_DQS_N<1>
DDR3	DDR_50S	DDR	DDR3_DQ<23..16>
DDR3	DDR_90D	DDR	DDR3_DQS_P<2>
DDR3	DDR_90D	DDR	DDR3_DQS_N<2>
DDR3	DDR_50S	DDR	DDR3_DQ<31..24>
DDR3	DDR_90D	DDR	DDR3_DQS_P<3>
DDR3	DDR_90D	DDR	DDR3_DQS_N<3>

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND0	*	*	2:1_SPACING
NAND1	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
FMIO	NAND_50S	NAND0	FMIO_AD<0>
FMIO	NAND_50S	NAND0	FMIO_AD<1>
FMIO	NAND_50S	NAND0	FMIO_AD<2>
FMIO	NAND_50S	NAND0	FMIO_AD<3>
FMIO	NAND_50S	NAND0	FMIO_AD<4>
FMIO	NAND_50S	NAND0	FMIO_AD<5>
FMIO	NAND_50S	NAND0	FMIO_AD<6>
FMIO	NAND_50S	NAND0	FMIO_AD<7>
FMIO	NAND_50S	NAND0	FMIO_ALE
FMIO	NAND_50S	NAND0	FMIO_CE0_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE1_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE2_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE3_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE4_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE5_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE6_L
FMIO	NAND_50S	NAND0	TP_FMIO_CE7_L
FMIO	NAND_50S	NAND0	FMIO_CLE
FMIO	NAND_50S	NAND0	FMIO_DQS
FMIO	NAND_50S	NAND0	FMIO_RE_L
FMIO	NAND_50S	NAND0	FMIO_WE_L
FMI1	NAND_50S	NAND1	FMI1_AD<0>
FMI1	NAND_50S	NAND1	FMI1_AD<1>
FMI1	NAND_50S	NAND1	FMI1_AD<2>
FMI1	NAND_50S	NAND1	FMI1_AD<3>
FMI1	NAND_50S	NAND1	FMI1_AD<4>
FMI1	NAND_50S	NAND1	FMI1_AD<5>
FMI1	NAND_50S	NAND1	FMI1_AD<6>
FMI1	NAND_50S	NAND1	FMI1_AD<7>
FMI1	NAND_50S	NAND1	FMI1_ALE
FMI1	NAND_50S	NAND1	FMI1_CE0_L
FMI1	NAND_50S	NAND1	TP_FMI1_CE2_L
FMI1	NAND_50S	NAND1	TP_FMI1_CE4_L
FMI1	NAND_50S	NAND1	TP_FMI1_CE5_L
FMI1	NAND_50S	NAND1	TP_FMI1_CE6_L
FMI1	NAND_50S	NAND1	TP_FMI1_CE7_L
FMI1	NAND_50S	NAND1	FMI1_CLE
FMI1	NAND_50S	NAND1	FMI1_DQS
FMI1	NAND_50S	NAND1	FMI1_RE_L
FMI1	NAND_50S	NAND1	FMI1_WE_L

DDR VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
PPVREF	PWR	DDR0	PPVREF_DDR0_CA
PPVREF	PWR	DDR0	PPVREF_DDR0_DO
PPVREF	PWR	DDR1	PPVREF_DDR1_CA
PPVREF	PWR	DDR1	PPVREF_DDR1_DO
PPVREF	PWR	DDR2	PPVREF_DDR2_CA
PPVREF	PWR	DDR2	PPVREF_DDR2_DO
PPVREF	PWR	DDR3	PPVREF_DDR3_CA
PPVREF	PWR	DDR3	PPVREF_DDR3_DO

WIFI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
WIFI_50S	*	WIFI_50S
WIFI_PWR100	*	WIFI_PWR100
WIFI_PWR1000	*	WIFI_PWR1000

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
50 WLAN G	WIFI_50S		50 WLAN G
50 WLAN A	WIFI_50S		50 WLAN A
50 WLAN G 1	WIFI_50S		50 WLAN G 1
50 WLAN A DIPLX	WIFI_50S		50 WLAN A DIPLX
50 WIFI ANT FD 2	WIFI_50S		50 WIFI ANT FD 2
50 WIFI ANT FD 1	WIFI_50S		50 WIFI ANT FD 1
50 WIFI ANT FD	WIFI_50S		50 WIFI ANT FD

SYNC MASTER=MIKE SYNC DATE=11/30/2011

CONSTRAINTS: DDR/FMI		DRAWING NUMBER 051-9385	SIZE D
Apple Inc.		REVISION A.0.0	BRANCH
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PWR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PP_PWR	*	PWR_PMU

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PWR	*	*	3:1_SPACING

VOLTAGE	NET_TYPE			
	PHYSICAL	SPACING		
1.1V	PP_PWR	PWR	BUCK0A_LX0	29
1.1V	PP_PWR	PWR	BUCK0A_LX1	29
1.1V	PP_PWR	PWR	BUCK0A_FB	29
1.1V	PP_PWR	PWR	PP1V1_CPU0_FET	29 30
1.1V	PP_PWR	PWR	BUCK0B_LX0	29
1.1V	PP_PWR	PWR	BUCK0B_LX1	29
1.1V	PP_PWR	PWR	BUCK0B_FB	29
1.1V	PP_PWR	PWR	PP1V1_CPU1_FET	29 30
1.1V	PP_PWR	PWR	BUCK0C_LX0	29
1.1V	PP_PWR	PWR	BUCK0C_FB	29
1.1V	PP_PWR	PWR	PP1V1_CPUB	29 34
1.2V	PP_PWR	PWR	BUCK2_LX0	29
1.2V	PP_PWR	PWR	BUCK2_LX1	29
1.2V	PP_PWR	PWR	BUCK2_LX2	29
1.2V	PP_PWR	PWR	BUCK2_FB	29
1.2V	PP_PWR	PWR	PP1V2_SOC	29 34
1.8V	PP_PWR	PWR	BUCK3_LX0	29
1.8V	PP_PWR	PWR	BUCK3_FB	29
1.8V	PP_PWR	PWR	PP1V8_S2R	29 34
1.2V	PP_PWR	PWR	BUCK4_LX0	29
1.2V	PP_PWR	PWR	BUCK4_FB	29
1.2V	PP_PWR	PWR	PP1V2_S2R	29 34
1.1V	PP_PWR	PWR	BUCK5_LX0	29
1.1V	PP_PWR	PWR	BUCK5_FB	29
3.3V	PP_PWR	PWR	PP3V3_OUT	29 34
3.0V	PP_PWR	PWR	PP3V0_GRAPE	29 34
1.7V	PP_PWR	PWR	PP1V7_VA_VCP	19 29 34
3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
3.2V	PP_PWR	PWR	LDO5	29
3.3V	PP_PWR	PWR	PP3V3_ACC	29 34
3.0V	PP_PWR	PWR	PP3V0_S2R_HALL	29 34
3.0V	PP_PWR	PWR	PP3V2_S2R_USBMUX	29 34 39
3.0V	PP_PWR	PWR	PP3V0_IO	29 34
3.0V	PP_PWR	PWR	PP3V0_SENSOR	29 34
2.8V	PP_PWR	PWR	PP2V8_CAM	29 34
1.0V	PP_PWR	PWR	PP1V0	29 34
1.1V	PP_PWR	PWR	PP1V1_SRAM	29 34
1.8V	PP_PWR	PWR	PP1V8_ALWAYS	29 34
1.2V	PP_PWR	PWR	PP1V2	29 34
1.8V	PP_PWR	PWR	DSP_SW	29 32 34
1.8V	PP_PWR	PWR	PP1V8_GRAPE	29 32 34
4.7V	PP_PWR	PWR	PPVCC_MAIN	15 25 29 30 34
4.2V	PWR500	PWR	PPBATT_VCC	29 32 34
6.0V	PP_PWR	PWR	PP6V0_LCM_HI	30
6.0V	PP_PWR	PWR	LCM_LX	30
6.0V	PP_PWR	PWR	PP6V0_LCM_VBOOST	30
5.25V	PP_PWR	PWR	PP5V25_VLCM1	30
1.1V	PP_PWR	PWR	PP1V1_CPU0	30 34
1.1V	PP_PWR	PWR	PP1V1_CPU1	30 34
20.4V	PP_PWR	PWR	PPLED_OUT_A	30 34
20.4V	PP_PWR	PWR	PPLED_OUT_B	30 34
1.8V	PP_PWR	PWR	PP1V8_PLO_F	4
1.0V	PP_PWR	PWR	PP1V0_MIPI_PLL_F	7
1.8V	PP_PWR	PWR	PP1V8_EDP_AVDD_AUX	7
1.8V	PP_PWR	PWR	PP1V8_DP_AVDD_AUX	7
3.3V	PP_PWR	PWR	PP3V3_S0_LCD_FERR	15
3.3V	PP_PWR	PWR	PP3V3_LCIVDD_SW_F	15
20.4V	PWR500	PWR	PPLED_BACK_REG_B	15
20.4V	PP_PWR	PWR	PPLED_BACK_REG_A	15
6V	PP_PWR	PWR	PPVBUS_USB_EMI	23 34
0.6V	PP_PWR	PWR	PPVREF_DDR0_CA	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR0_DO	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR1_CA	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR1_DO	11 38
0.6V	PP_PWR	PWR	PPVREF_DDR2_CA	12 38
0.6V	PP_PWR	PWR	PPVREF_DDR2_DO	12 38
0.6V	PP_PWR	PWR	PPVREF_DDR3_CA	12 38
0.6V	PP_PWR	PWR	PPVREF_DDR3_DO	12 38
4.6V	PP_PWR	PWR	DAC_AP_VREF	7
4.6V	PP_PWR	PWR	BATT_POS_RC	29
4.6V	PP_PWR	PWR	BATT_VCC_WLAN	27
1.8V	PP_PWR	PWR	PP_WLAN_VDDIO_1V8	27
3.55V	PP_PWR	PWR	LDO10	18 29

GND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
GND	*	GND_PH

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
VOLTAGEX0V	GND	GND	GND
VOLTAGEX0V	GND	GND	GND_AUDIO_CODEC
VOLTAGEX0V	GND	GND	GND_SPKR_AMP1
VOLTAGEX0V	GND	GND	GND_SPKR_AMP2
VOLTAGEX0V	GND	GND	AGND_U3000
VOLTAGEX0V	GND	GND	J2200_29_GND
VOLTAGEX0V	GND	GND	J2200_36_GND
VOLTAGEX0V	GND	GND	J2200_43_GND

RST

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
RST	*	*	4:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	PHYSICAL	SPACING	
	RST	RST	BB_TRST_L
	RST	RST	DBG_RST
	RST	RST	DEBUG_RST_L
	RST	RST	GSM_TXBURST_IND
	RST	RST	JTAG_AP_TRST_L
	RST	RST	RST_AP_1V8_L
	RST	RST	RST_AP_L
	RST	RST	GPIO_BB_RST_L
	RST	RST	RST_BB_PMU_L
	RST	RST	RST_BT_L
	RST	RST	RST_DET_L
	GRAPE	RST	RST_GRAPE_L
	RST	RST	RST_L63_L
	RST	RST	RST_PMU_IN
	RST	RST	RST_WLAN_L
	RST	RST	SIMCRD_RST
	RST	RST	UD881_RST
	RST	RST	UD882_RST

SYNC MASTER=MIKE SYNC DATE=11/30/2011

CONSTRAINTS: POWER / GND

Apple Inc.

DRAWING NUMBER: 051-9385 SIZE: D

REVISION: A.0.0

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