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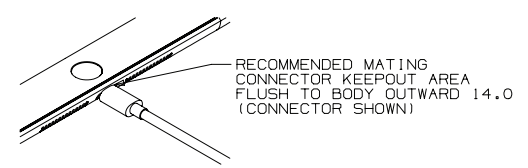
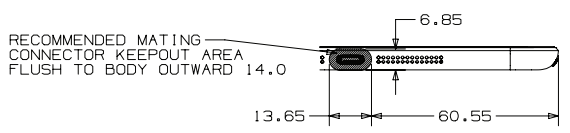
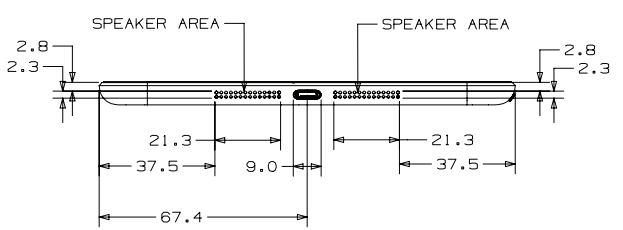
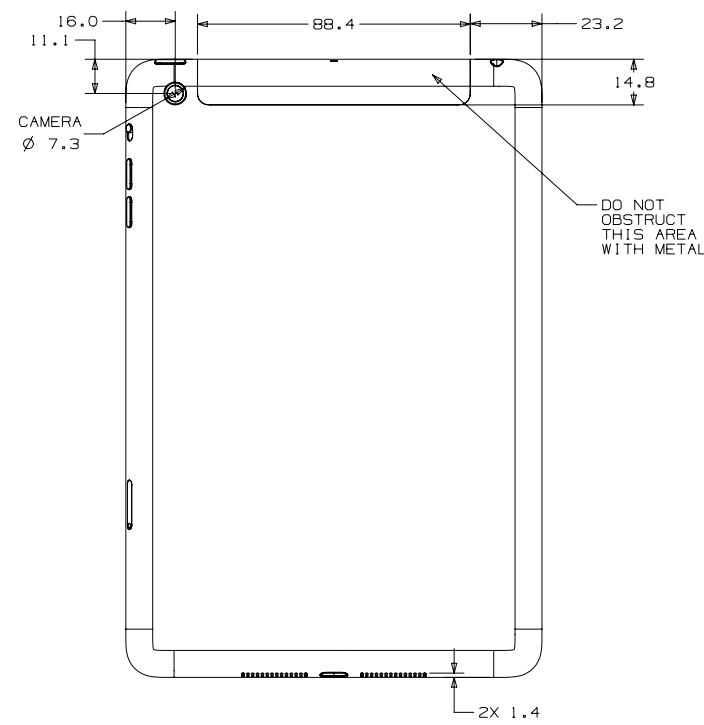
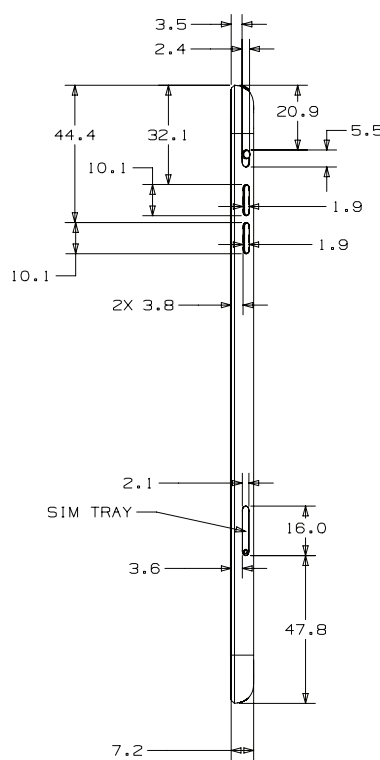
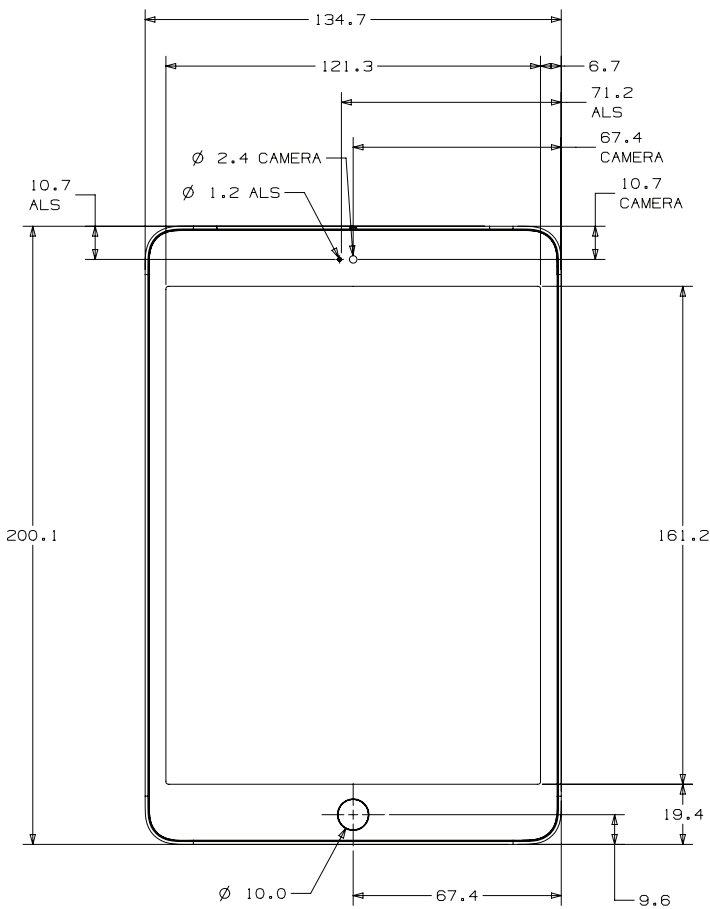
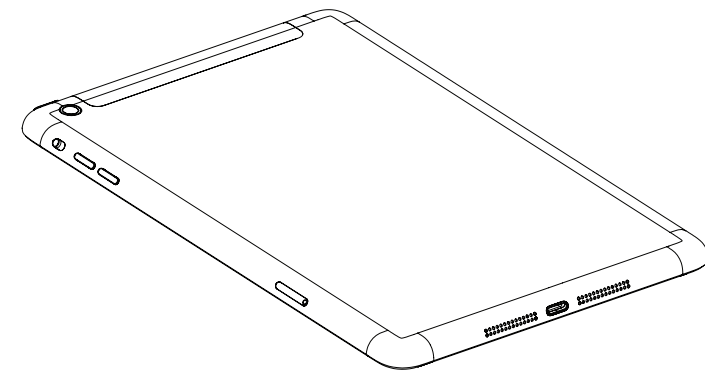
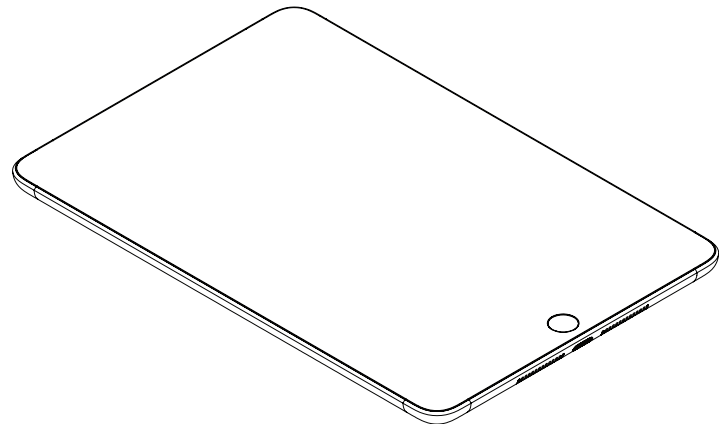
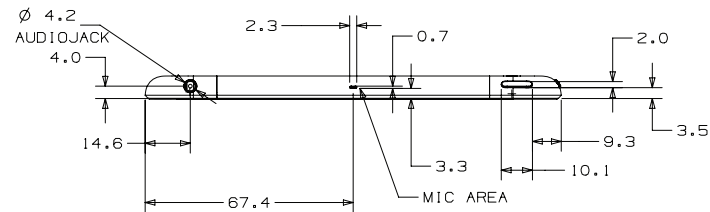
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REV	EDD#	DESCRIPTION OF REVISION

NOTES: (UNLESS OTHERWISE SPECIFIED)



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DESIGNER APPLE INC.	DATE	TITLE <b>IPAD MINI WITH WI-FI + 4G</b>	
DIMENSIONS ARE IN MILLIMETERS		DRAWING NUMBER	
TOLERANCES		REV.	
X.X	$\pm 0.2$		
X.XX	$\pm 0.10$		
X.XXX	$\pm 0.050$		
ANGLES	$\pm 0.5^\circ$		
DO NOT SCALE DRAWINGS			
THIRD ANGLE PROJECTION	SIZE <b>D</b>	SCALE NONE	SHT 1 OF 1

4

3

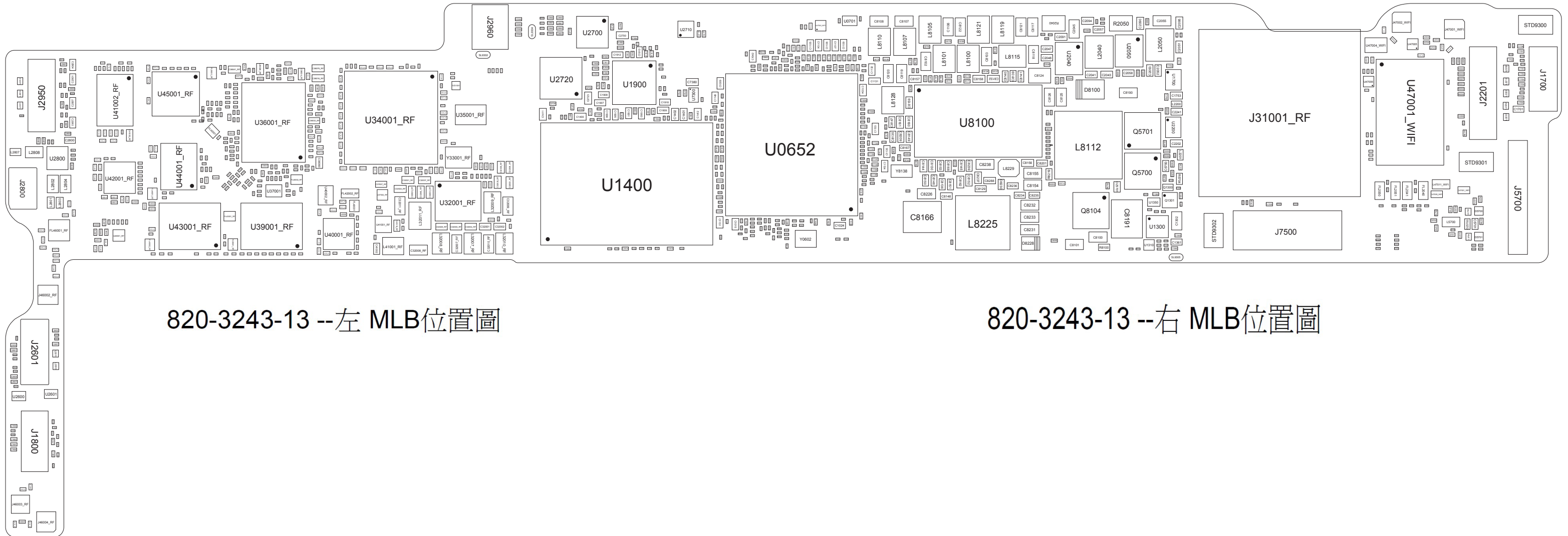
2

NX GENERATED

Diesel157

Diesel157

www.mobile-files.com



820-3243-13 --左 MLB位置圖

820-3243-13 --右 MLB位置圖

Diesel157

Diesel157

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.  
 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.  
 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD	DATE
13	0001520462	ENGINEERING RELEASED		2012-07-02

# X123 MAIN LOGIC BOARD

DVT  
 LAST\_MODIFIED=Wed Jun 27 16:39:53 2012

SCH AND BOARD PART NUMBERS

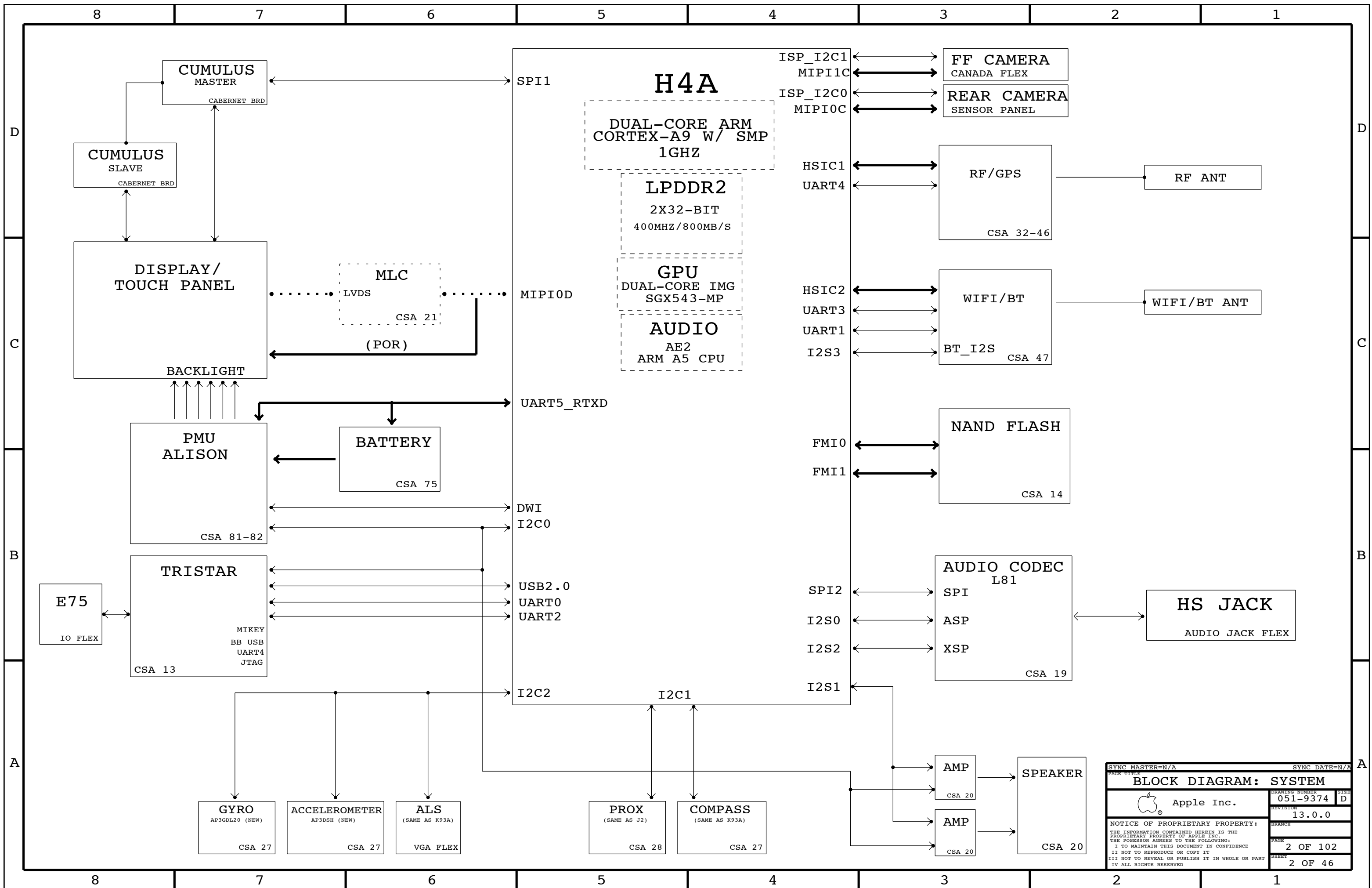
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-9374	1	SCH,MLB,X123	SCH1	
820-3243	1	PCB,MLB,X123	PCB1	

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	N/A	N/A
2	2	BLOCK DIAGRAM: SYSTEM	N/A	N/A
3	6	AP: MAIN	N/A	04/18/2011
4	7	AP: I/Os	N/A	05/05/2011
5	8	AP: FLASH MEMORY INTERFACE	N/A	04/18/2011
6	9	AP: TV/DP/MIPI/CAMERA	MLB	05/04/2012
7	10	AP: PWR	N/A	04/18/2011
8	11	AP: PWR	N/A	04/18/2011
9	12	AP: MISC & ALIASES	N/A	04/11/2011
10	13	E75 SUPPORT	N/A	N/A
11	14	NAND STORAGE	MLB	05/04/2012
12	17	TOUCH: FLEX CONNECTOR	N/A	06/21/2010
13	18	AUDIO JACK FLEX CONN	N/A	03/31/2011
14	19	AUDIO: L81 CODEC	KAVITHA	01/18/2012
15	20	AUDIO: CS35L19A AMPS	KAVITHA	01/18/2012
16	22	VIDEO: MIPI CONNECTOR	N/A	N/A
17	26	FF CAM & MIC CONNECTORS	N/A	N/A
18	27	INERTIAL SENSORS	N/A	N/A
19	28	PROX SENSOR	N/A	N/A
20	29	BUTTON & REAR CAMERA CONN	N/A	N/A

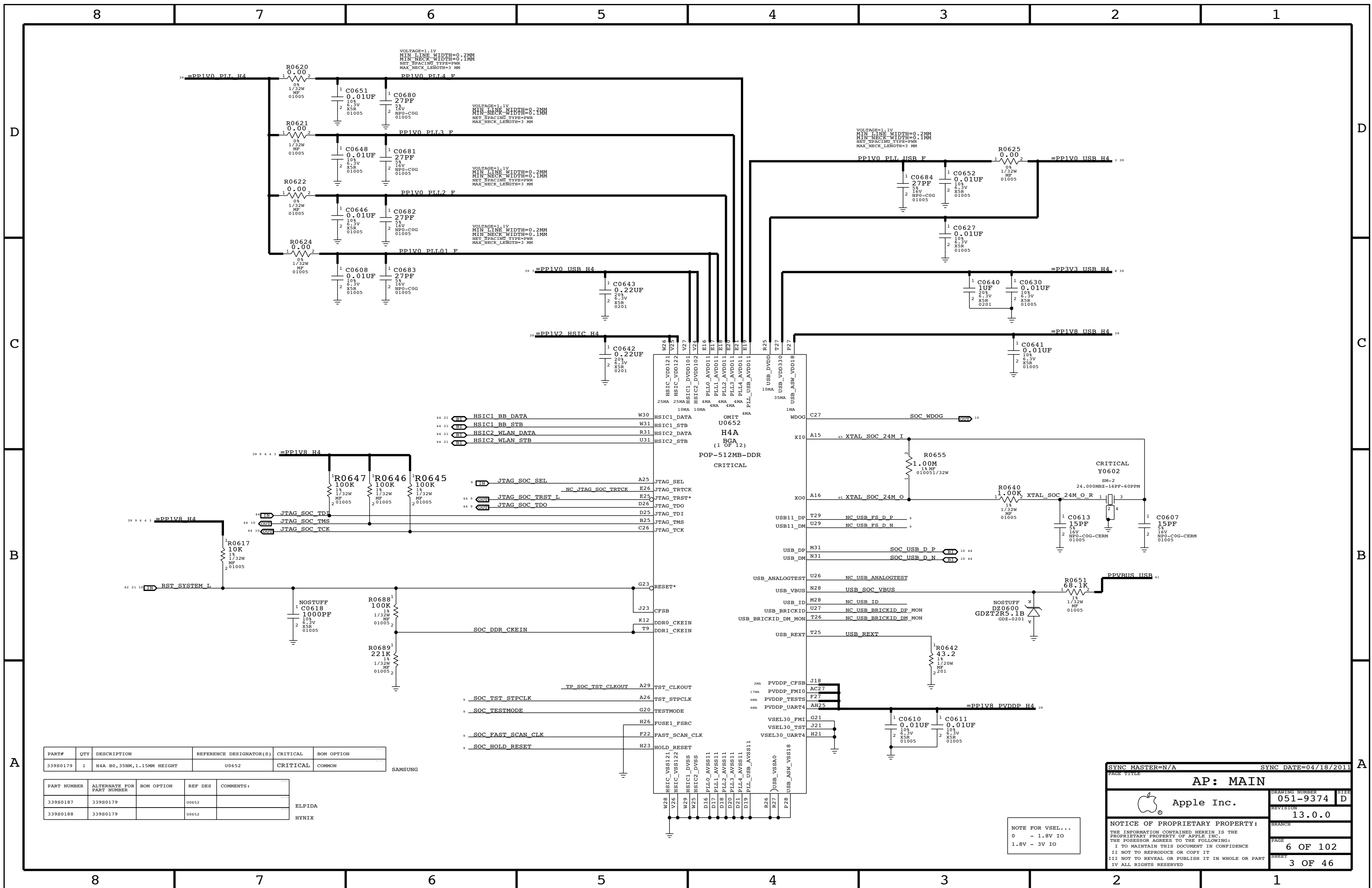
PDF	CSA	CONTENTS	SYNC MASTER	DATE
21	31	SYSTEM & DEBUG CONNECTORS	JORGE	06/27/2012
22	32	BASEBAND PMU (1 OF 2)	JORGE	06/27/2012
23	33	BASEBAND PMU (2 OF 2)	JORGE	06/27/2012
24	34	BASEBAND (1 OF 2)	JORGE	06/27/2012
25	35	MOBILE DATA MODEM (2 OF 2)	JORGE	06/27/2012
26	36	RF TRANSCEIVER (1 OF 3)	JORGE	06/27/2012
27	37	RF TRANSCEIVER (2 OF 3)	JORGE	06/27/2012
28	38	RF TRANSCEIVER (3 OF 3)	JORGE	06/27/2012
29	39	BAND 5/8 PAD	JORGE	06/27/2012
30	40	BAND 13 PA	JORGE	06/27/2012
31	41	2G PA, DCDC CONVERTER	JORGE	06/27/2012
32	42	DCS RX, ASM	JORGE	06/27/2012
33	43	BAND 1/4 PAD	JORGE	06/27/2012
34	44	BAND2 PAD	JORGE	06/27/2012
35	45	RX DIVERSITY	JORGE	06/27/2012
36	46	GPS	JORGE	06/27/2012
37	47	WIFI/BT	JORGE	06/27/2012
38	57	IO FLEX: DOCK COMPONENTS	N/A	04/18/2011
39	73	Power: Aliases	N/A	N/A
40	75	POWER: BATTERY CONNECTOR	N/A	N/A
41	81	Power: PMU	N/A	N/A
42	82	POWER: PMU	N/A	05/09/2011
43	93	MECHANICAL PARTS	N/A	N/A
44	100	CONSTRAINTS: ASSIGNMENTS	N/A	N/A
45	101	CONSTRAINTS: ASSIGNMENTS	N/A	N/A
46	102	CONSTRAINTS: MLB RULES	N/A	N/A

DRAWING TITLE		SCH,MLB,X123	
DRAWING NUMBER	051-9374	SIZE	D
	REVISION		13.0.0
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<b>BLOCK DIAGRAM: SYSTEM</b>			
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		REVISION	
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33980179	1	H4A B0, 35NM, 1.15MM HEIGHT	U0652	CRITICAL	COMMON

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33980187	33980179		U0652	
33980188	33980179		U0652	

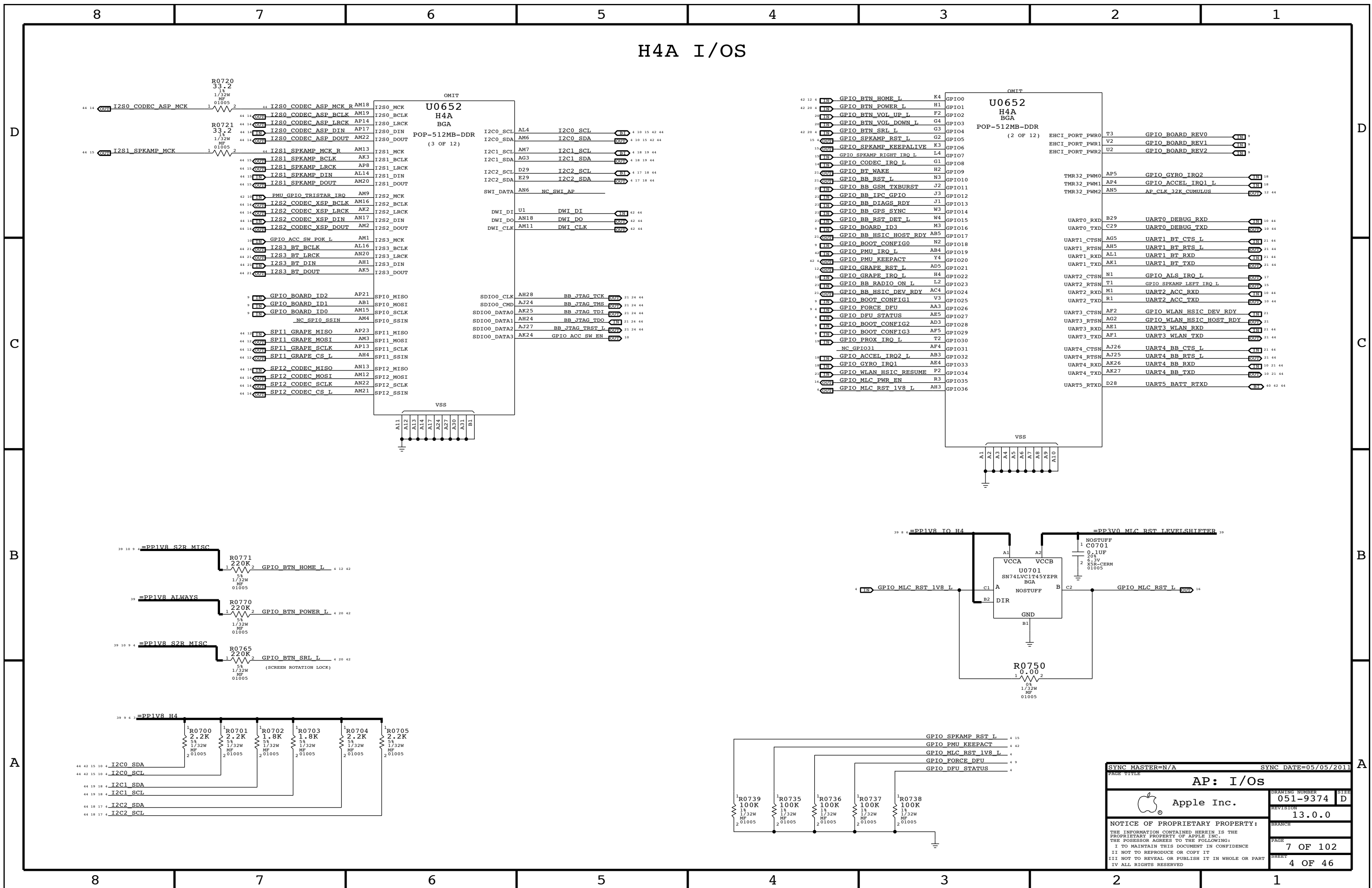
ELPIDA  
HYNIX

SAMSUNG

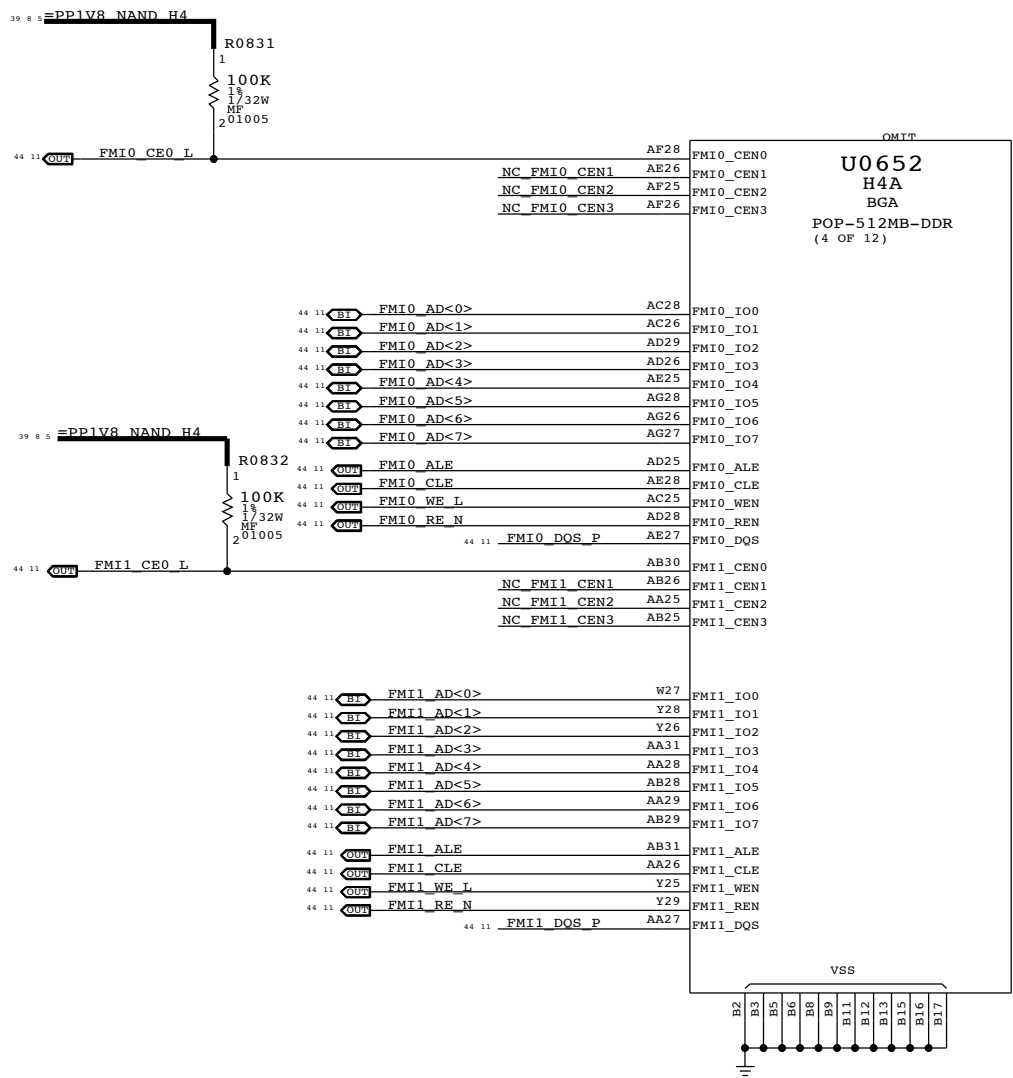
NOTE FOR VSEL...  
0 - 1.8V IO  
1.8V - 3V IO

PAGE TITLE		SYNC DATE=04/18/2011	
<b>AP: MAIN</b>		DRAWING NUMBER	SIZE
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		13.0.0	
		PAGE	SHEET
		6 OF 102	3 OF 46

# H4A I/OS



SYNC MASTER=N/A		SYNC DATE=05/05/2011	
<b>AP: I/OS</b>			
		DRAWING NUMBER	051-9374
		REVISION	13.0.0
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		PAGE	7 OF 102
		SHEET	4 OF 46

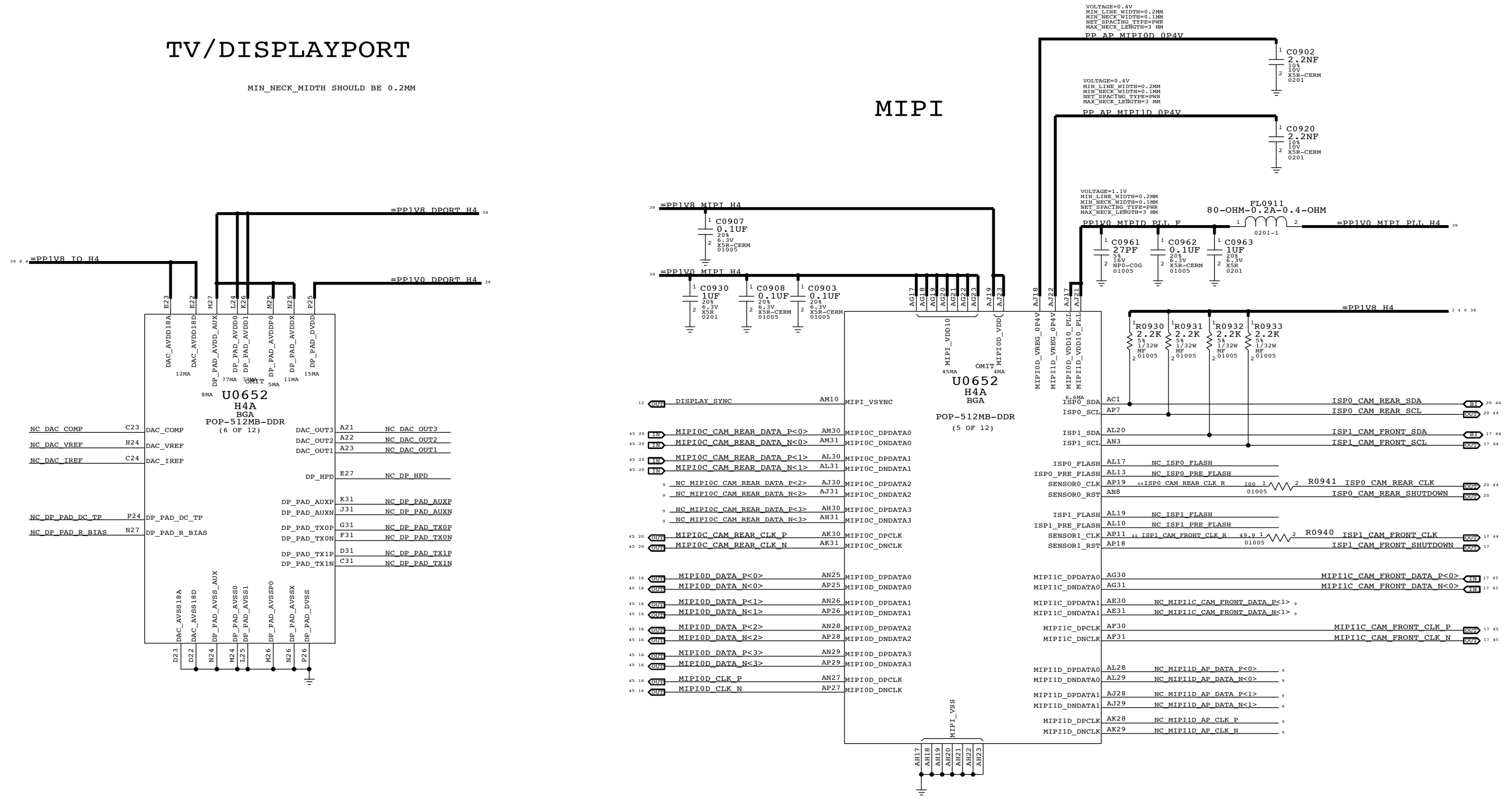


PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580725	15580359		FL0911	RADAR: 11363497

# TV/DISPLAYPORT

MIN\_NECK\_WIDTH SHOULD BE 0.2MM

# MIPI

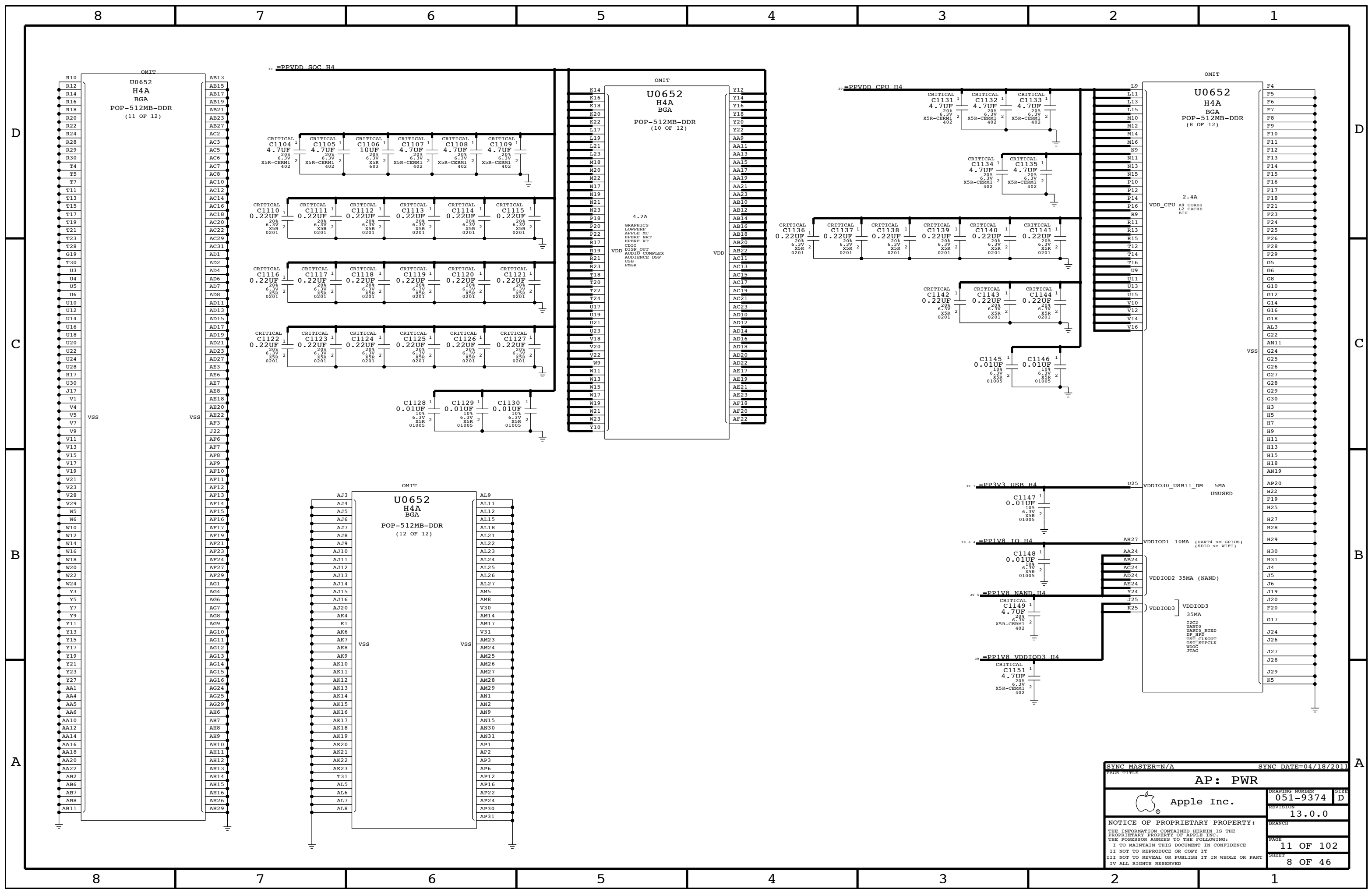


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PAGE TITLE			
AP: TV/DP/MIPI/CAMERA			
DRAWING NUMBER		SIZE	
051-9374		D	
REVISION		PAGE	
13.0.0		9 OF 102	
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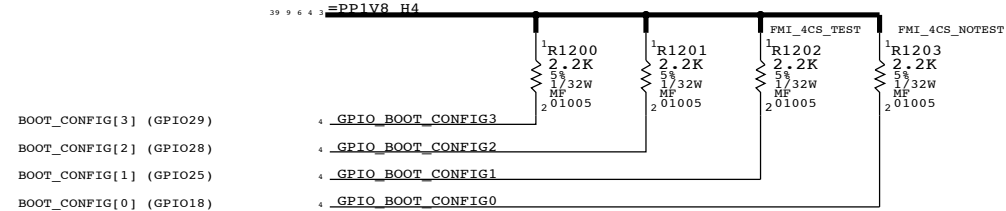


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<b>AP: PWR</b>		DRAWING NUMBER	SIZE
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		SHEET	8 OF 46

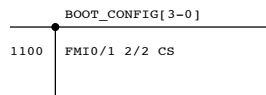
BOOT CONFIG ID



BOOT\_CONFIG[3] (GPIO29)  
 BOOT\_CONFIG[2] (GPIO28)  
 BOOT\_CONFIG[1] (GPIO25)  
 BOOT\_CONFIG[0] (GPIO18)

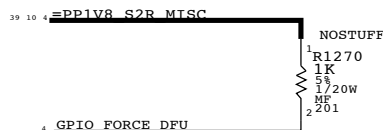
FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMIO 2CS
0101	FMIO 4CS
0110	FMIO 4CS W/TEST
0111	RESERVED
1000	FM11 2 CS
1001	FM11 4 CS
1010	FM11 4CS W/TEST
1011	RESERVED
1100	FMIO/1 2/2 CS
1101	FMIO/1 4/4 CS
1110	FMIO/1 4/4 CS W/TEST
1111	RESERVED

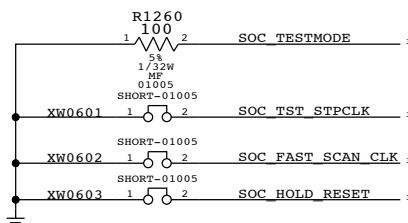
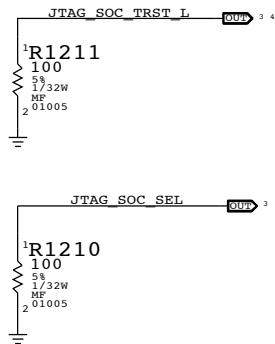


- S/W READ FLOW
1. SET GPIO AS INPUT
  2. DISABLE PU AND ENABLE PD
  3. READ

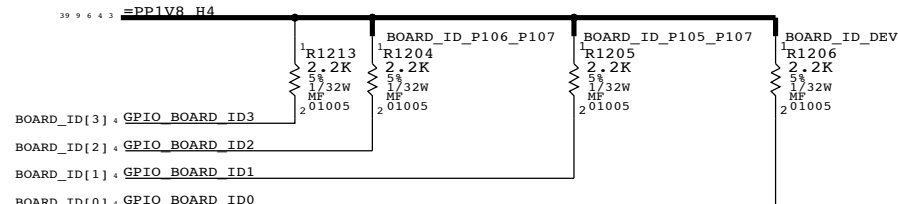
NOTE: PADS USED FOR DEBUG



JTAG



BOARD ID

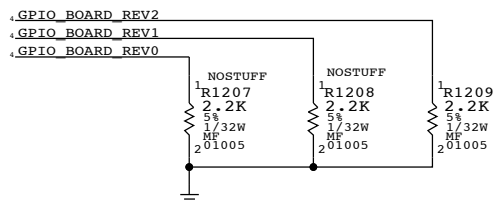


BOARD\_ID[3] GPIO\_BOARD\_ID3  
 BOARD\_ID[2] GPIO\_BOARD\_ID2  
 BOARD\_ID[1] GPIO\_BOARD\_ID1  
 BOARD\_ID[0] GPIO\_BOARD\_ID0

ID[3-0]	SYSTEM
1010	P105 AP
1011	P105 DEV
1100	P106 AP
1101	P106 DEV
1110	P107 AP
1111	P107 DEV

- S/W READ FLOW
1. SET GPIO AS INPUT
  2. DISABLE PU AND ENABLE PD
  3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 0
001	PROTO 1
010	PROTO 2
011	EVT
100	DVT

- S/W READ FLOW
1. SET GPIO AS INPUT
  2. ENABLE PU AND DISABLE PD
  3. READ

SINGLE-PIN NETS

NC_FMIO_DQS_NEG	FMIO_DQS_N
NC_FMIO_RE_POS	FMIO_RE_P
NC_FM11_DQS_NEG	FM11_DQS_N
NC_FM11_RE_POS	FM11_RE_P
NC_PMU_SHDWN	PMU_SHDWN
NC_JTAG_SOC_TDO	JTAG_SOC_TDO
NC_AP_MIPI0C_DPDATA2	NC_MIPI0C_CAM_REAR_DATA_P<2>
NC_AP_MIPI0C_DNDATA2	NC_MIPI0C_CAM_REAR_DATA_N<2>
NC_AP_MIPI0C_DPDATA3	NC_MIPI0C_CAM_REAR_DATA_P<3>
NC_AP_MIPI0C_DNDATA3	NC_MIPI0C_CAM_REAR_DATA_N<3>
NC_AP_MIPI1D_DPCLK	NC_MIPI1D_AP_CLK_P
NC_AP_MIPI1D_DNCLK	NC_MIPI1D_AP_CLK_N
NC_AP_MIPI1D_DPDATA0	NC_MIPI1D_AP_DATA_P<0>
NC_AP_MIPI1D_DNDATA0	NC_MIPI1D_AP_DATA_N<0>
NC_AP_MIPI1D_DPDATA1	NC_MIPI1D_AP_DATA_P<1>
NC_AP_MIPI1D_DNDATA1	NC_MIPI1D_AP_DATA_N<1>
NC_AP_MIPI1C_DPDATA1	NC_MIPI1C_CAM_FRONT_DATA_P<1>
NC_AP_MIPI1C_DNDATA1	NC_MIPI1C_CAM_FRONT_DATA_N<1>
NC_AP_USB11_DPD	NC_USB_FS_D_P
NC_AP_USB11_DND	NC_USB_FS_D_N

SYNC MASTER=N/A SYNC DATE=04/11/2011

AP: MISC & ALIASES



Apple Inc.

DRAWING NUMBER 051-9374

REVISION 13.0.0

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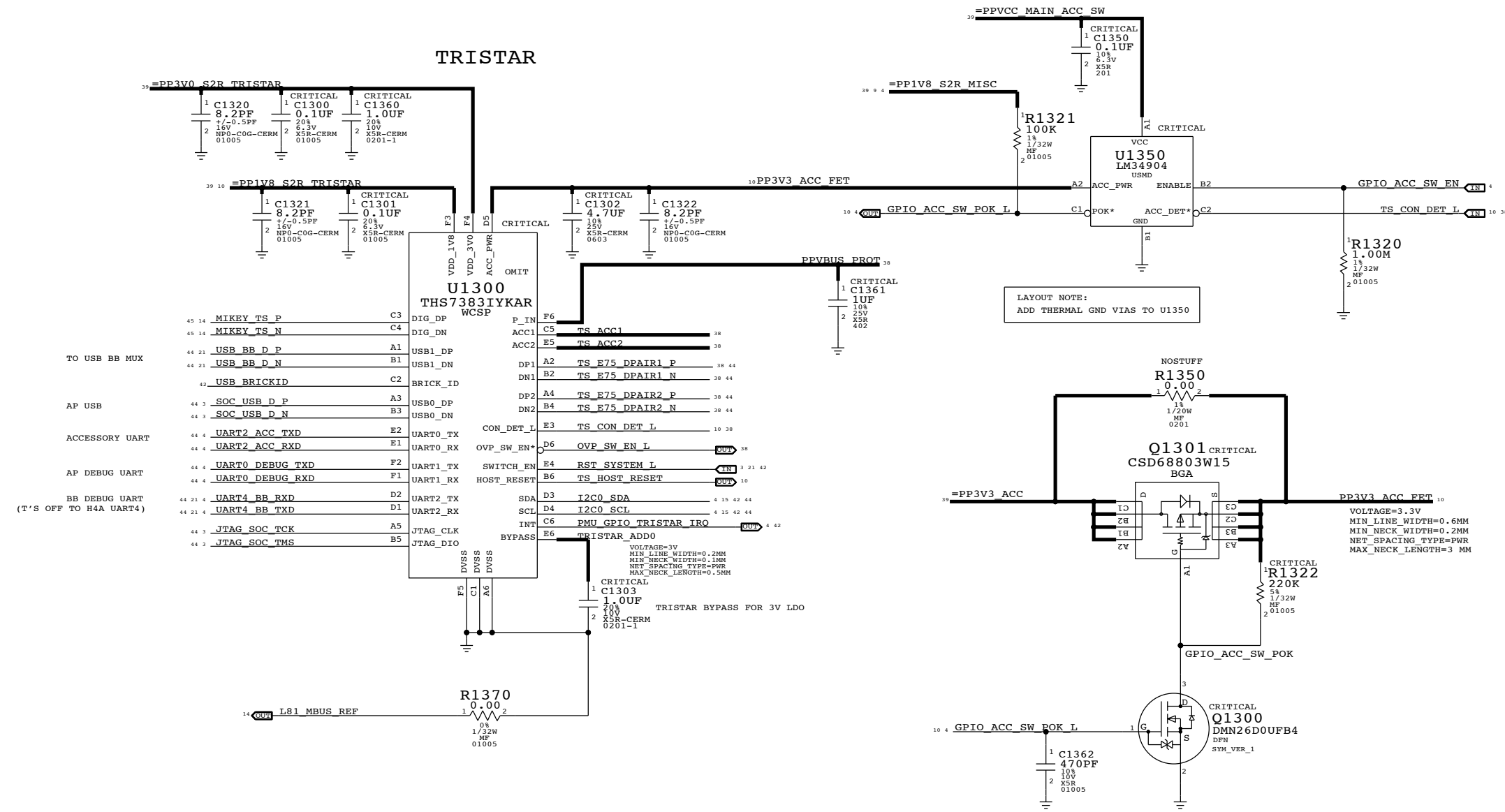
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PAGE 12 OF 102

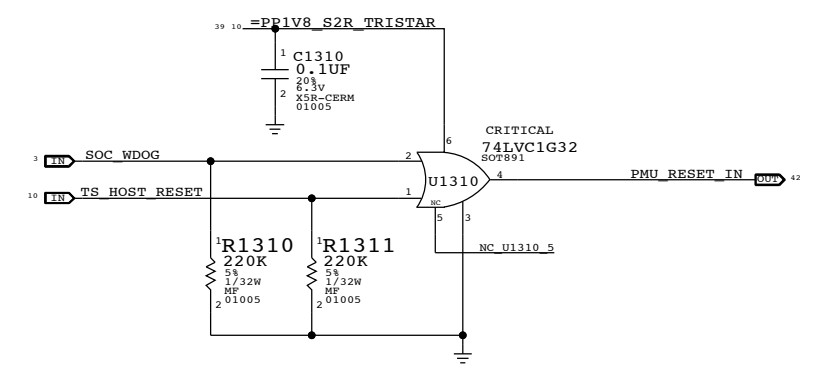
SHEET 9 OF 46

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
NXP 34380614	1	IC,ASIC,TRISTAR,CBTL1608,A1,MLCSP36	U1300	CRITICAL	COMMON

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
TI 34380620	34380614	COMMON	U1300	IC,ASIC,TRISTAR,CBTL1608,A1,MLCSP36



EITHER TRISTAR OR AP CAN RESET PMU

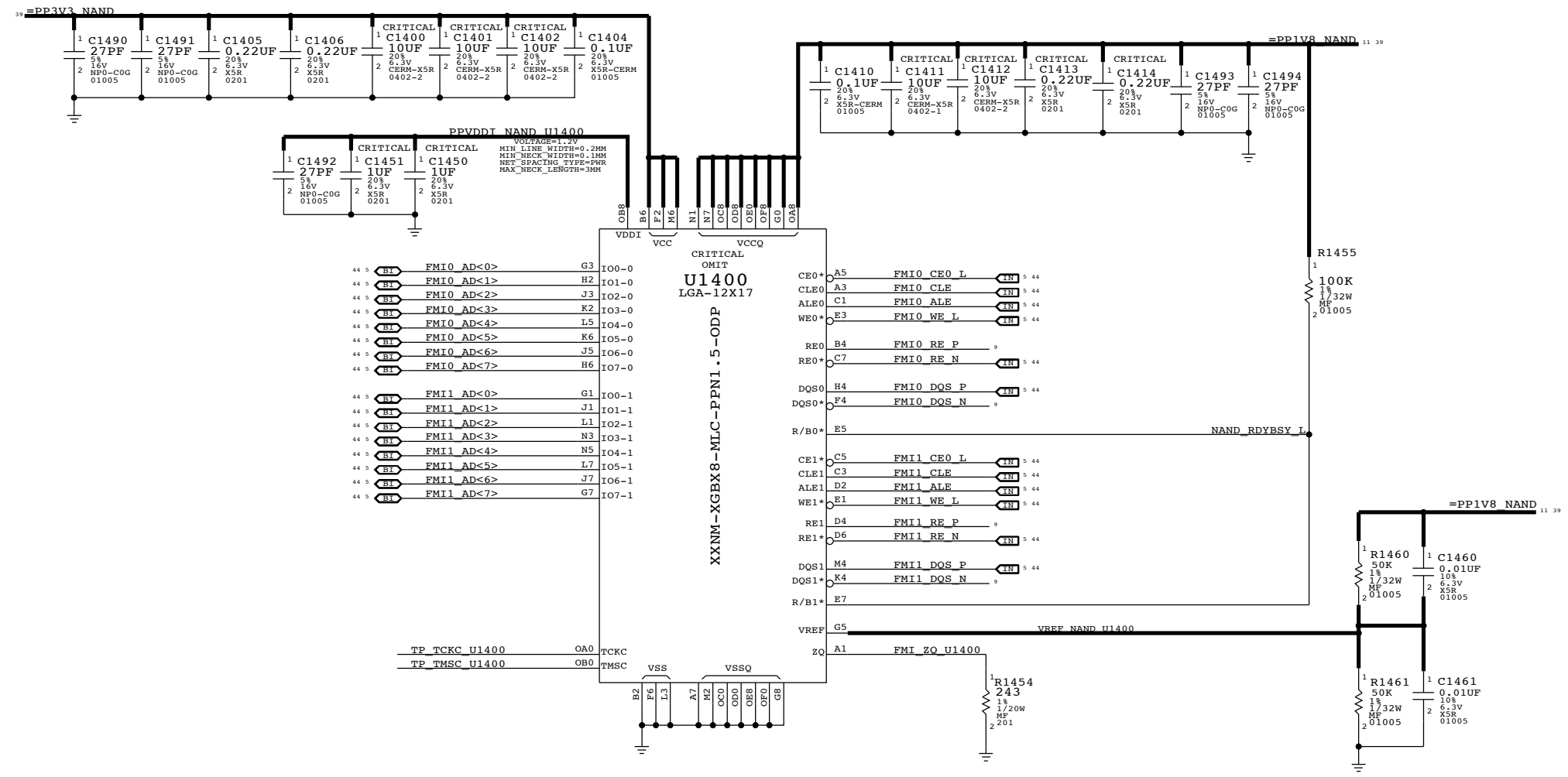


PAGE TITLE		SYNC DATE=N/A	
<b>E75 SUPPORT</b>			
Apple Inc.		DRAWING NUMBER	051-9374
		REVISION	13.0.0
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		PAGE	13 OF 102
		SHEET	10 OF 46

FLASH CONFIGURATIONS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0889	335S0890	8GB	U1400	HYNIX 20NM PPN1.5 8GB
335S0871	335S0878	16GB	U1400	HYNIX 20NM PPN1.5 16GB
335S0872	335S0879	32GB	U1400	HYNIX 20NM PPN1.5 32GB
335S0873	335S0880	64GB	U1400	HYNIX 20NM PPN1.5 64GB
335S0900	335S0880	16GB	U1400	SANDISK 19NM PPN1.5 16GB
335S0881	335S0880	16GB	U1400	SAMSUNG 21NM PPN1.5 16GB
335S0882	335S0880	32GB	U1400	SAMSUNG 21NM PPN1.5 32GB
335S0883	335S0880	64GB	U1400	SAMSUNG 21NM PPN1.5 64GB

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0890	1	TOSHIBA 19NM PPN1.5 8GB	U1400	8GB
335S0878	1	TOSHIBA 19NM PPN1.5 16GB	U1400	16GB
335S0879	1	TOSHIBA 19NM PPN1.5 32GB	U1400	32GB
335S0880	1	TOSHIBA 19NM PPN1.5 64GB	U1400	64GB



SYNC MASTER=MLB SYNC DATE=05/04/2012

**NAND STORAGE**

Apple Inc.

DRAWING NUMBER: 051-9374 SIZE: D

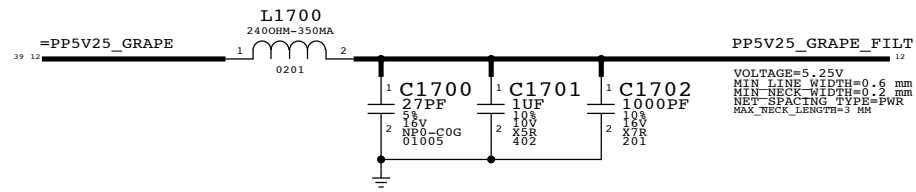
REVISION: 13.0.0

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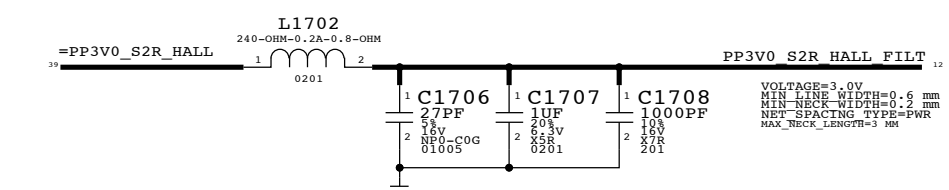
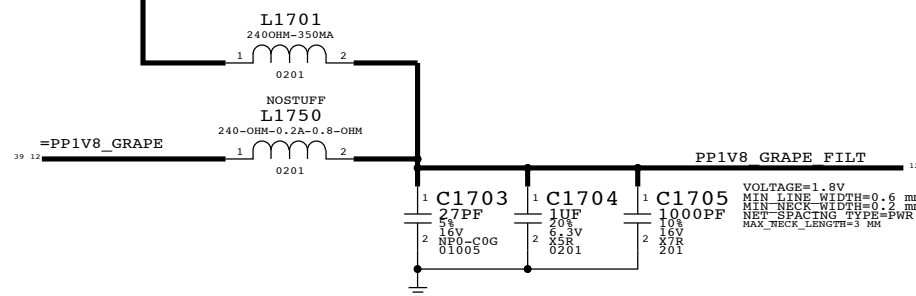
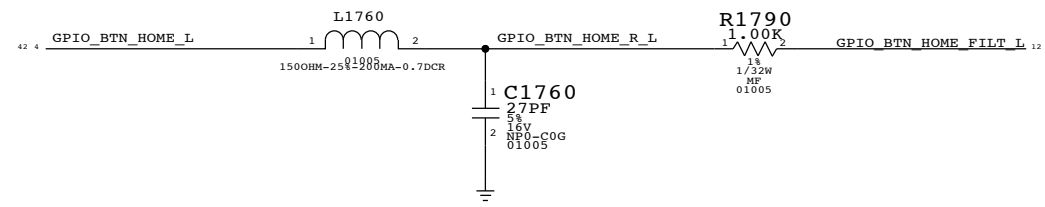
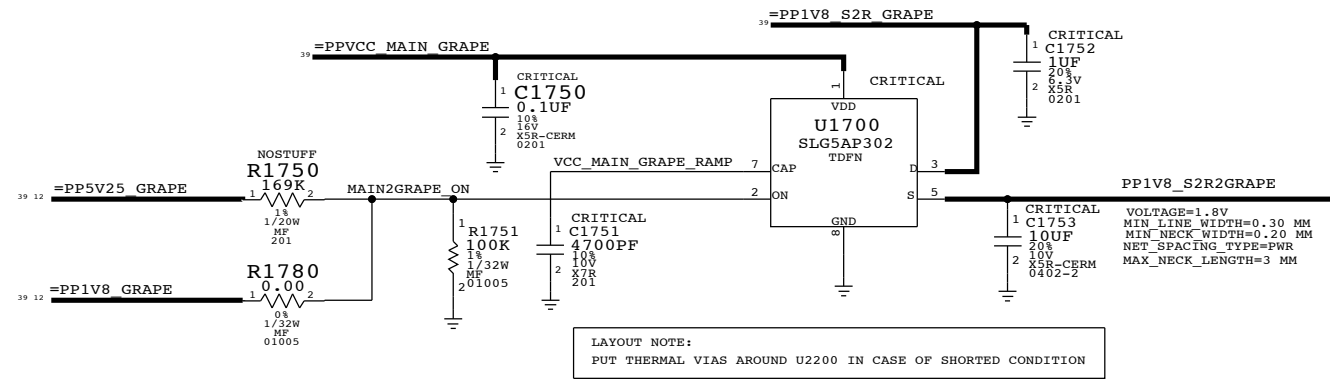
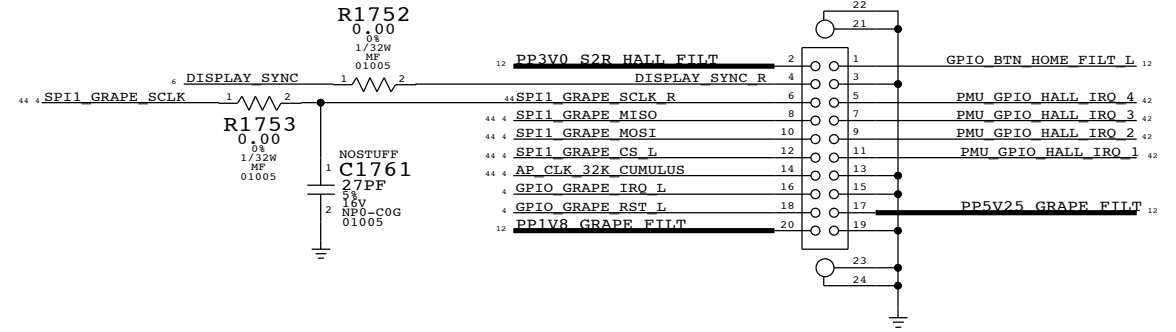
# TOUCH SUBSYSTEM

8 7 6 5 4 3 2 1



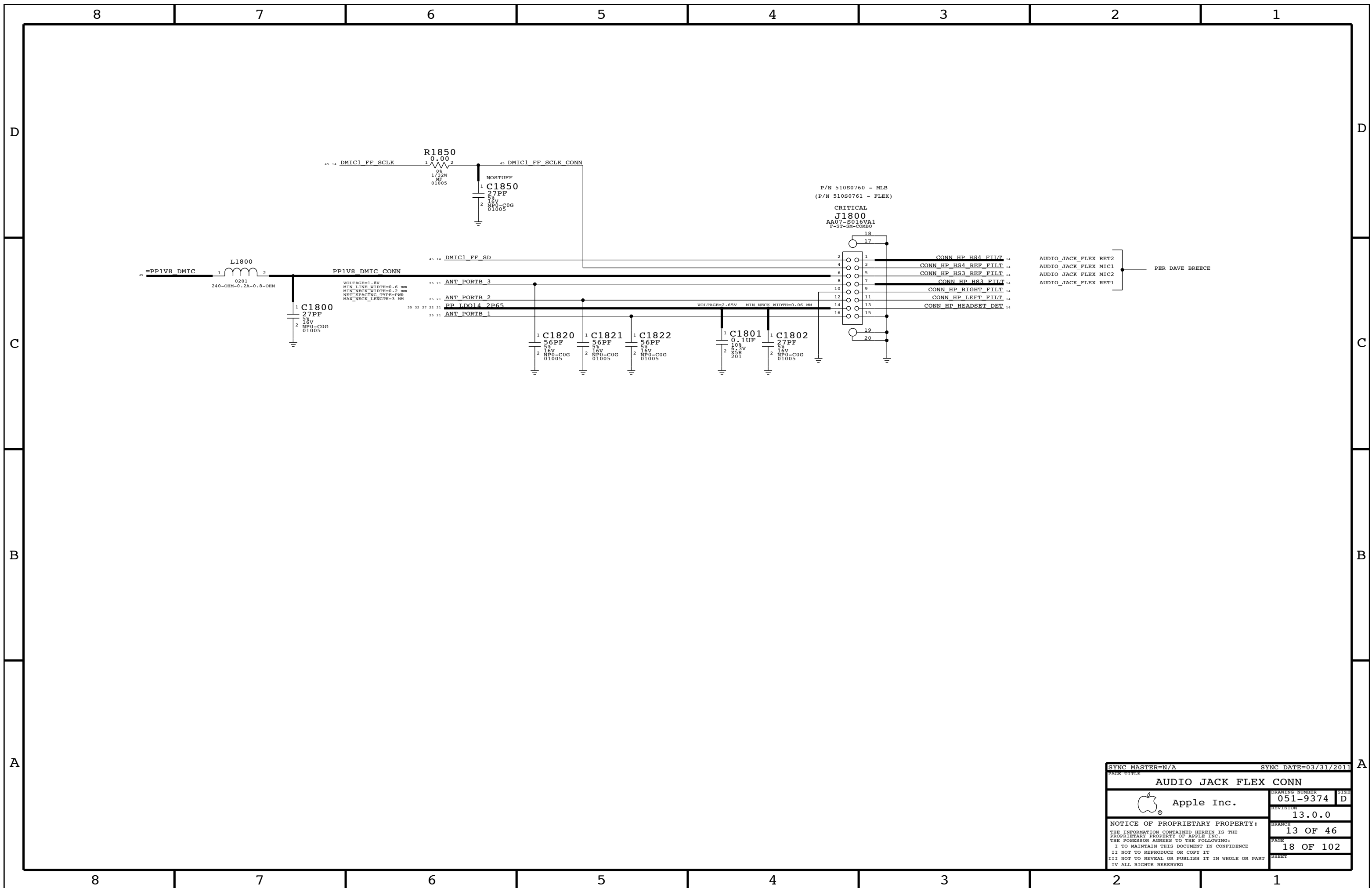
RCPT - MLB 998-4526 -> 516S1054  
(PLUG - FLEX 998-4527)

CRITICAL  
J1700  
503304-2010  
F-ST-SM-1

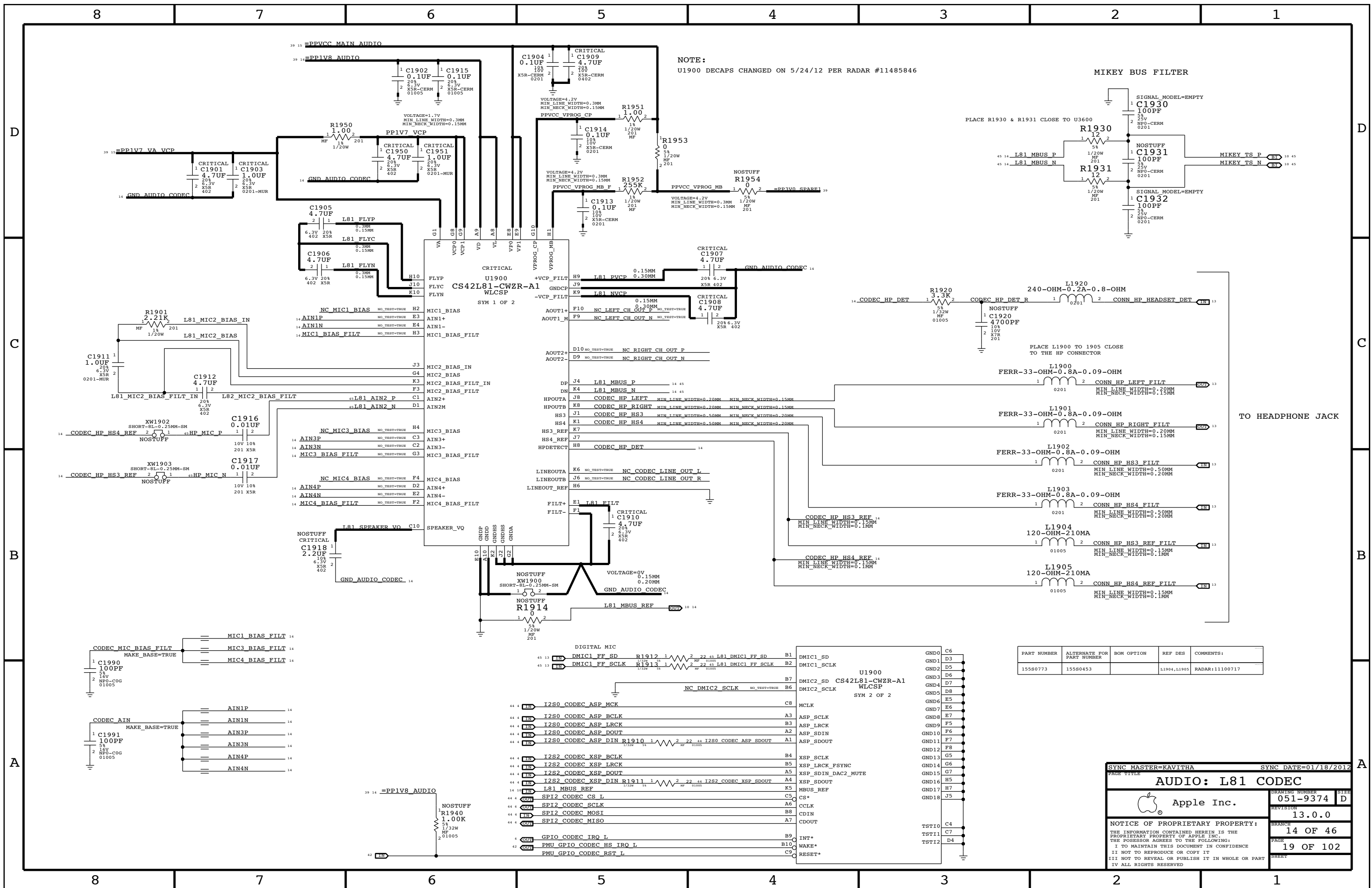


PAGE TITLE		SYNC DATE=06/21/2010	
<b>TOUCH: FLEX CONNECTOR</b>			
Apple Inc.	DRAWING NUMBER	051-9374	SIZE D
	REVISION	13.0.0	BRANCH
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8 7 6 5 4 3 2 1

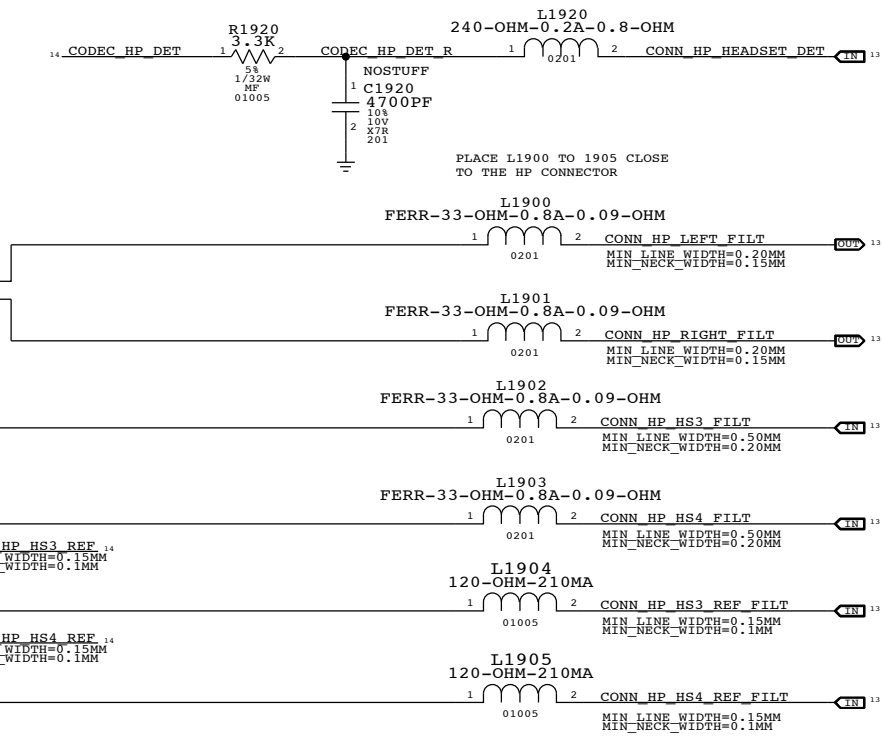
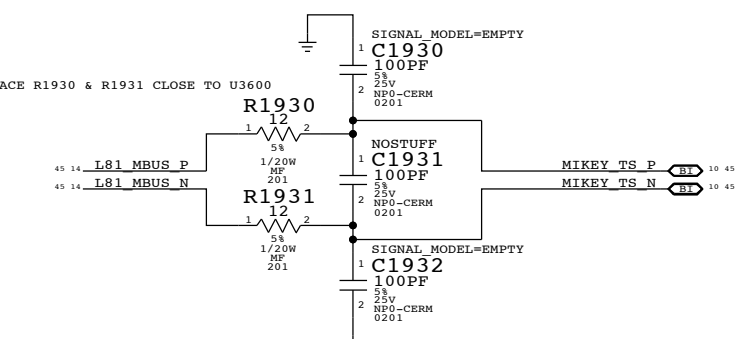


SYNC MASTER=N/A		SYNC DATE=03/31/2011	
<b>AUDIO JACK FLEX CONN</b>			
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		051-9374	D
		REVISION	
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		13 OF 46	
		PAGE	18 OF 102
		SHEET	



NOTE:  
U1900 DECAPS CHANGED ON 5/24/12 PER RADAR #11485846

MIKEY BUS FILTER



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580773	15580453		L1904, L1905	RADAR:11100717

U1900	CS42L81-CWZR-A1	WLCSP	SYN 2 OF 2
B1	DMIC1_FF_SD	R1912	L81 DMIC1_FF_SD
B2	DMIC1_FF_SCLK	R1913	L81 DMIC1_FF_SCLK
B6	NC DMIC2_SCLK		
B7	DMIC2_SD		
B8	DMIC2_SCLK		
C8	MCLK		
A3	ASP_SCLK		
B3	ASP_LRCK		
A2	ASP_SDIN		
A1	ASP_SDOUT	R1910	I2S0 CODEC ASP_SDOUT
B4	XSP_SCLK		
B5	XSP_LRCK_FSYNC		
A5	XSP_SDIN_DAC2_MUTE		
A4	XSP_SDOUT	R1911	I2S2 CODEC XSP_SDOUT
K5	MBUS_REF		
C5	CS*		
A6	CCLK		
B8	CDIN		
A7	CDOUT		
B9	INT*		
B10	WAKE*		
C9	RESET*		

SYNC MASTER=KAVITHA SYNC DATE=01/18/2012

**AUDIO: L81 CODEC**

Apple Inc.

DRAWING NUMBER: 051-9374 SIZE: D

REVISION: 13.0.0

BRANCH: 14 OF 46

PAGE: 19 OF 102

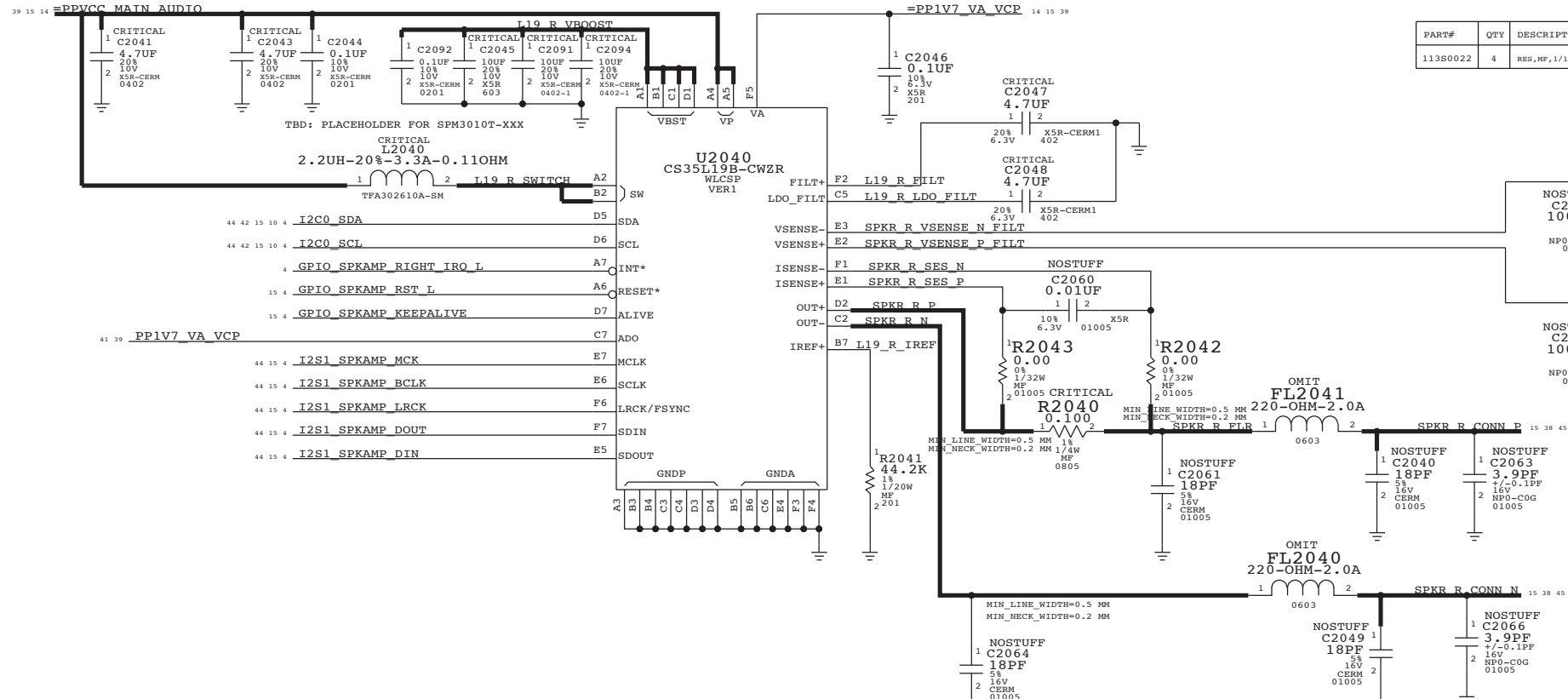
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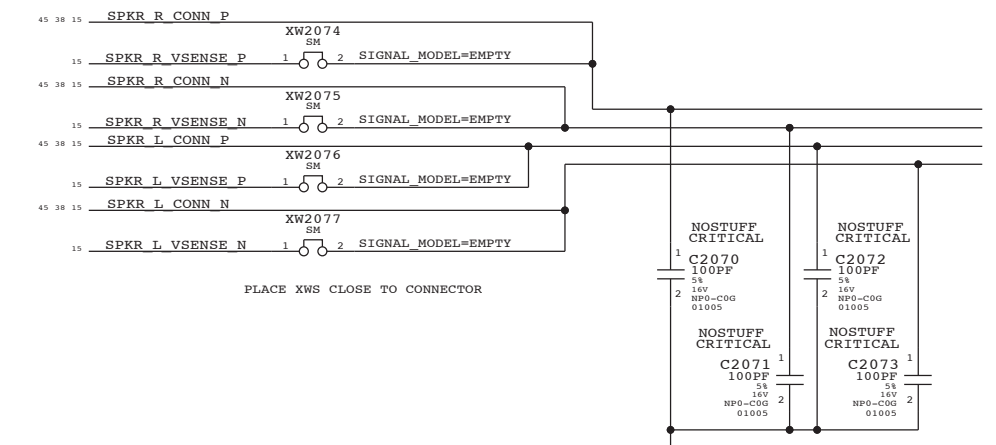
# RIGHT SPEAKER AMP

I2C ADDRESS: 100001X



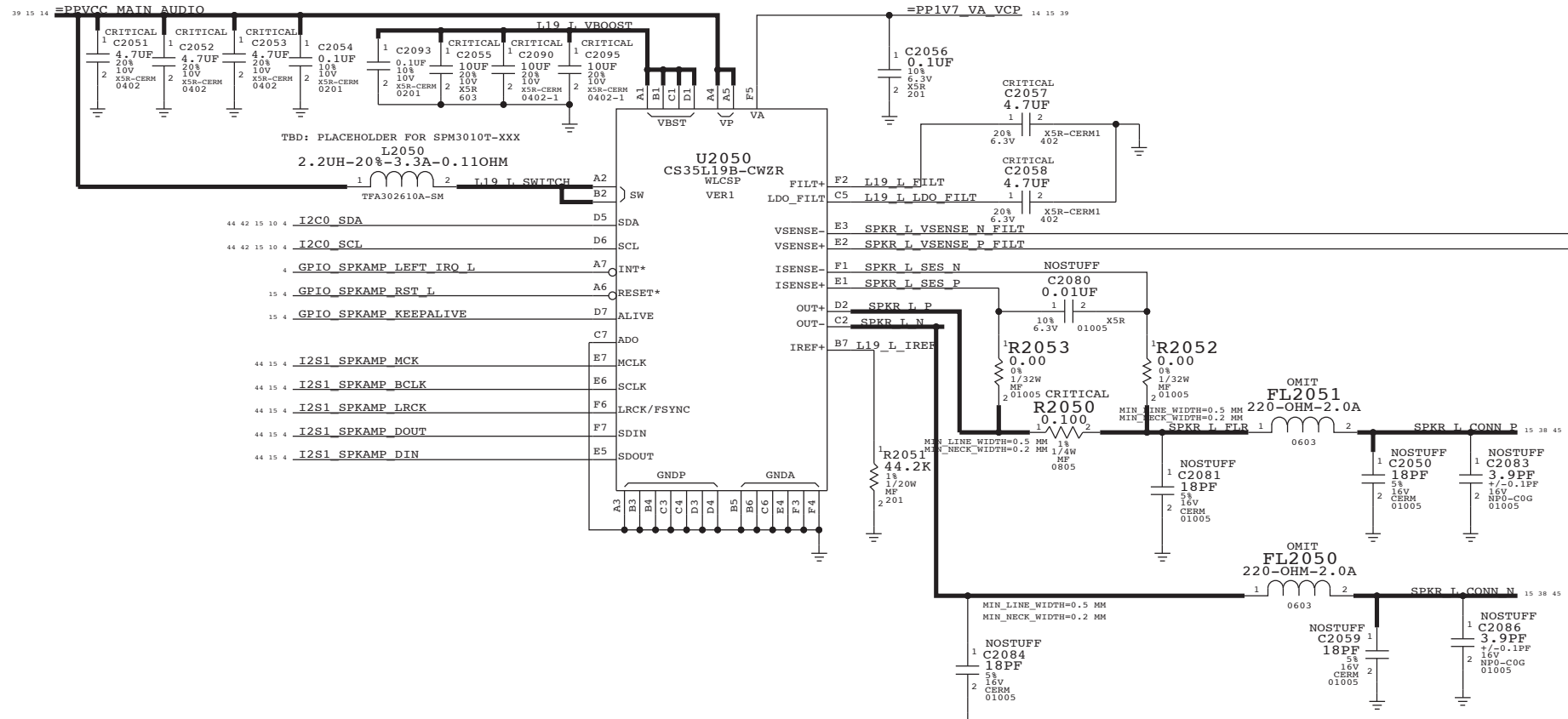
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11380022	4	RES, MF, 1/10W, 0 OHM, 5%, 0603, SMD, LF	FL2040, FL2041, FL2050, FL2051		

# SPEAKER CONNECTOR



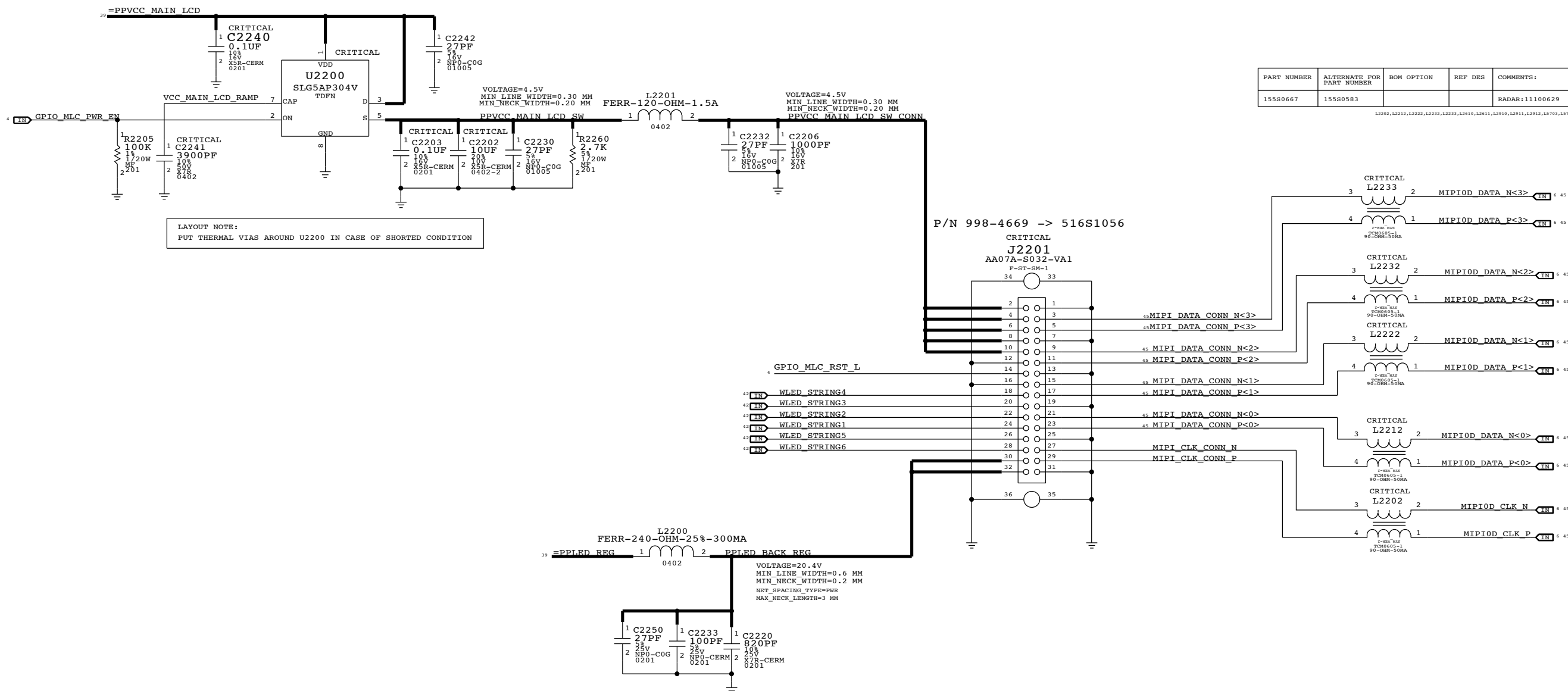
# LEFT SPEAKER AMP

I2C ADDRESS: 1000000X



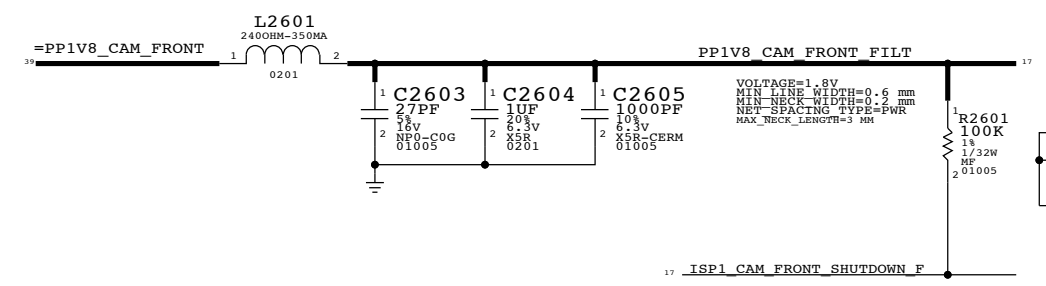
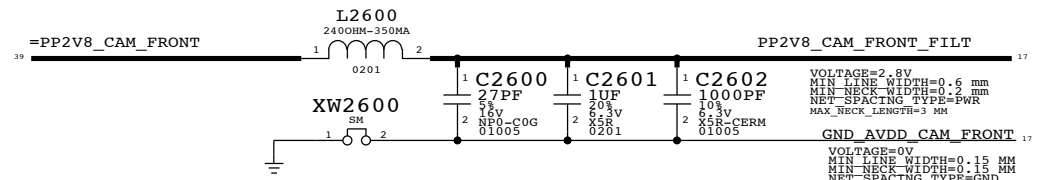
SYNC MASTER=KAVITHA		SYNC DATE=01/18/2012	
PAGE TITLE			
AUDIO: CS35L19A AMPS			
Apple Inc.		DRAWING NUMBER	051-9374
		REVISION	13.0.0
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# MIPI CONNECTOR

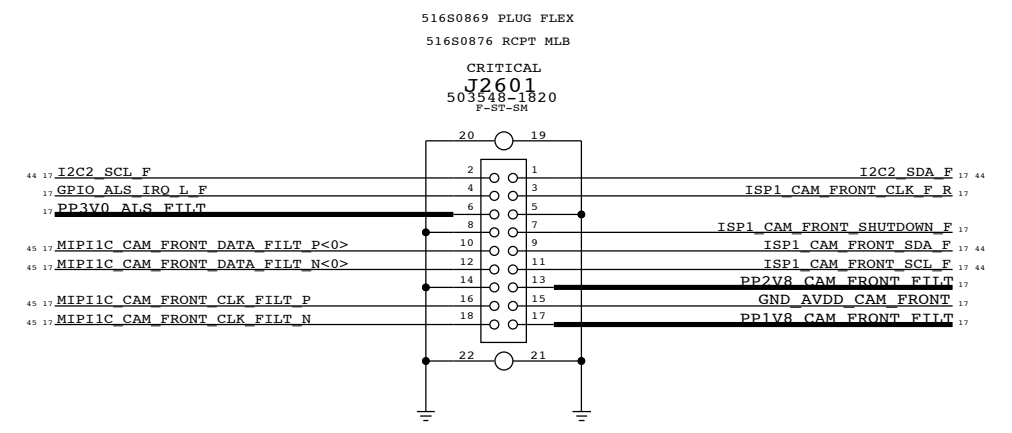
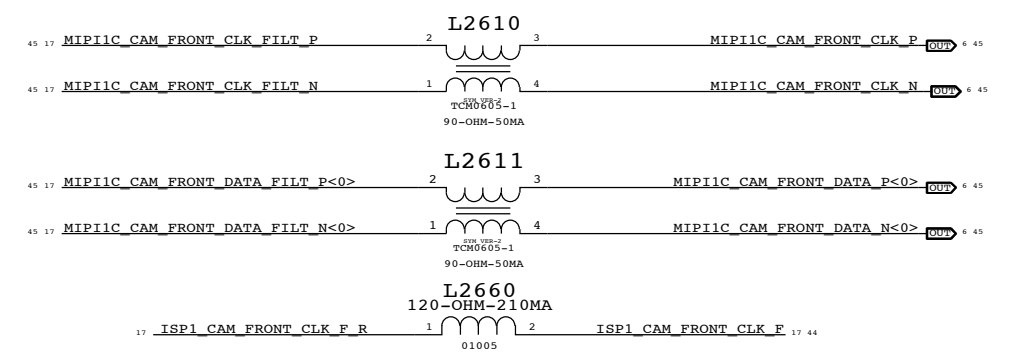
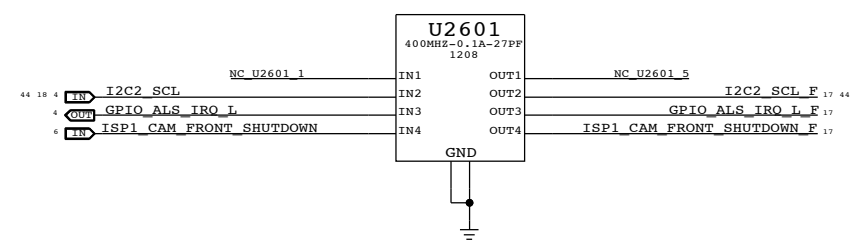
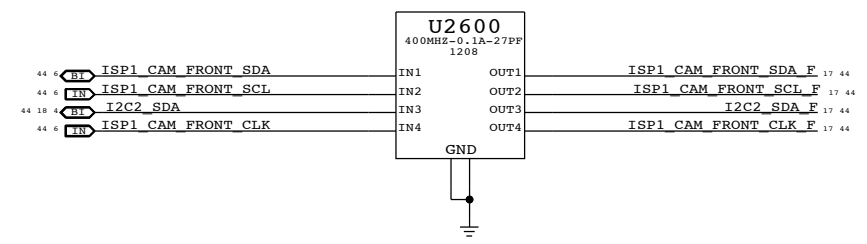
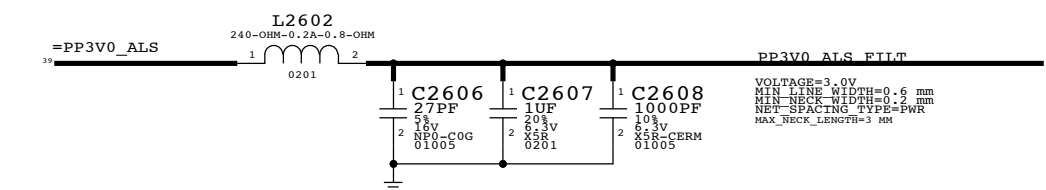


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PAGE TITLE <b>VIDEO: MIPI CONNECTOR</b>			
DRAWING NUMBER 051-9374		SIZE D	
REVISION 13.0.0		BRANCH	
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# VGA FRONT CAMERA CONNECTOR



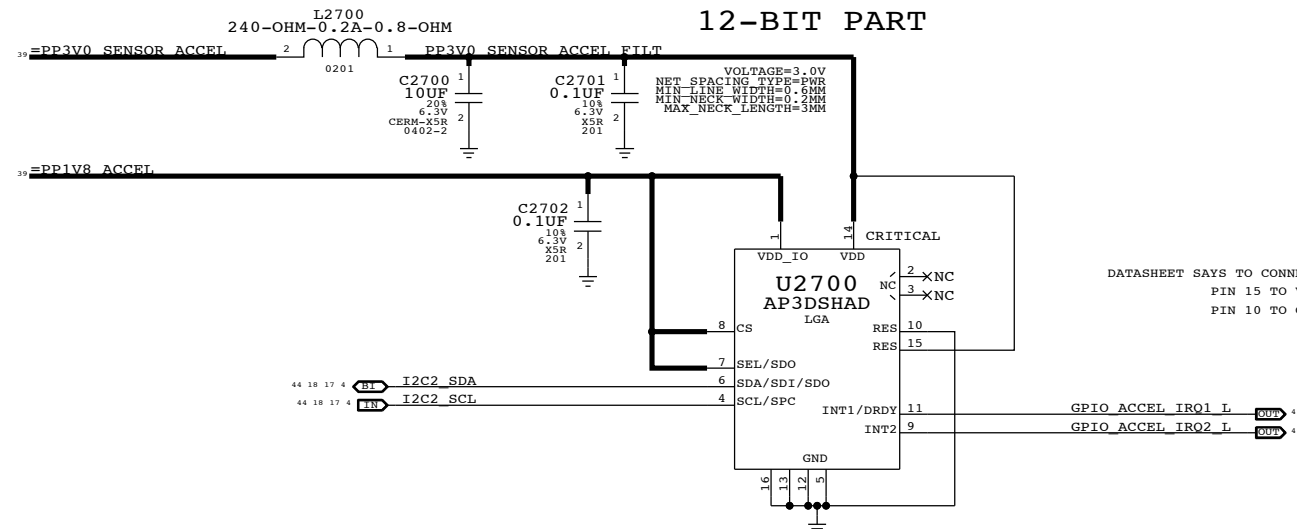
ISPI\_CAM\_FRONT\_SHUTDOWN  
 LOW = ENABLES CAMERA TO TURN ON  
 HIGH = DISABLES / TURNS OFF CAMERA



PAGE TITLE		SYNC MASTER=N/A		SYNC DATE=N/A	
<b>FF CAM &amp; MIC CONNECTORS</b>					
		DRAWING NUMBER	051-9374	SIZE	D
		REVISION	13.0.0	BRANCH	
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		PAGE	26 OF 102		
		SHEET	17 OF 46		

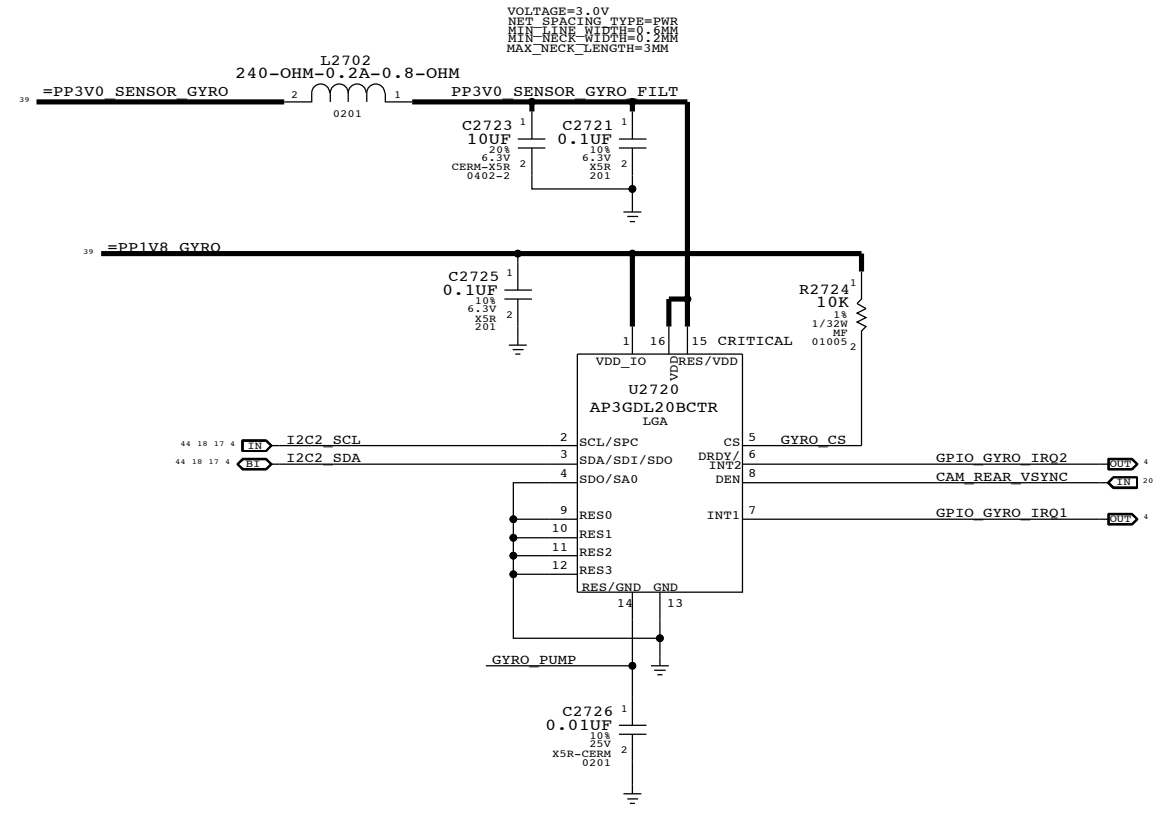
# ACCELEROMETER

(WRITE: 0X3A READ: 0X3B)



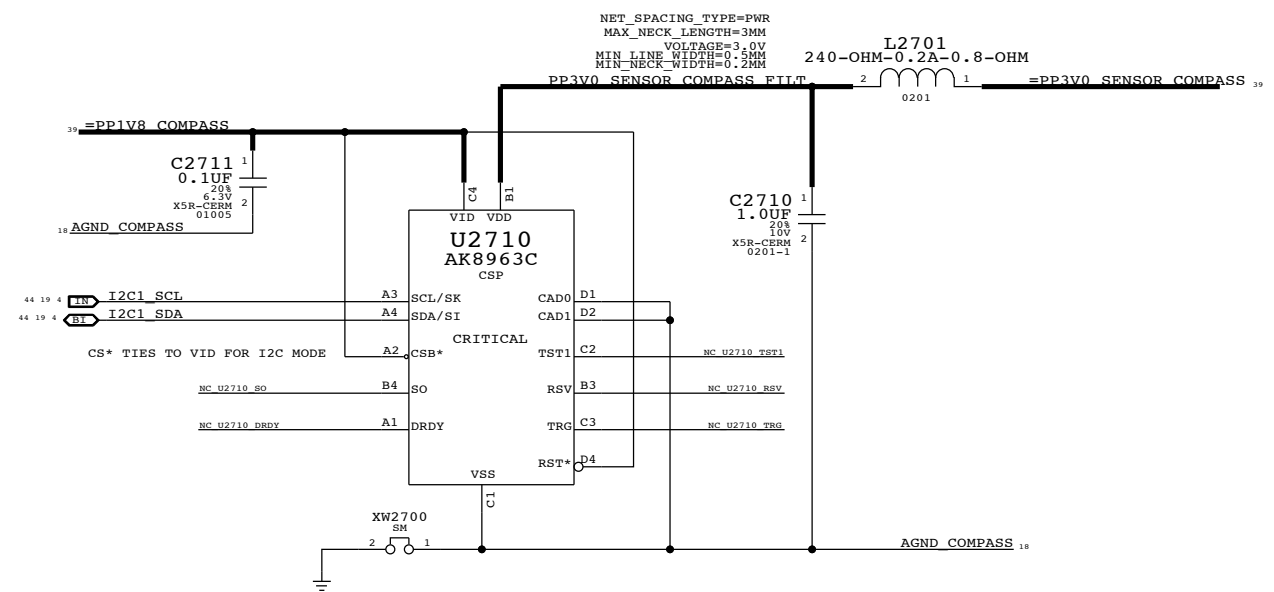
# GYRO

(WRITE: 0XD4 READ: 0XD5)



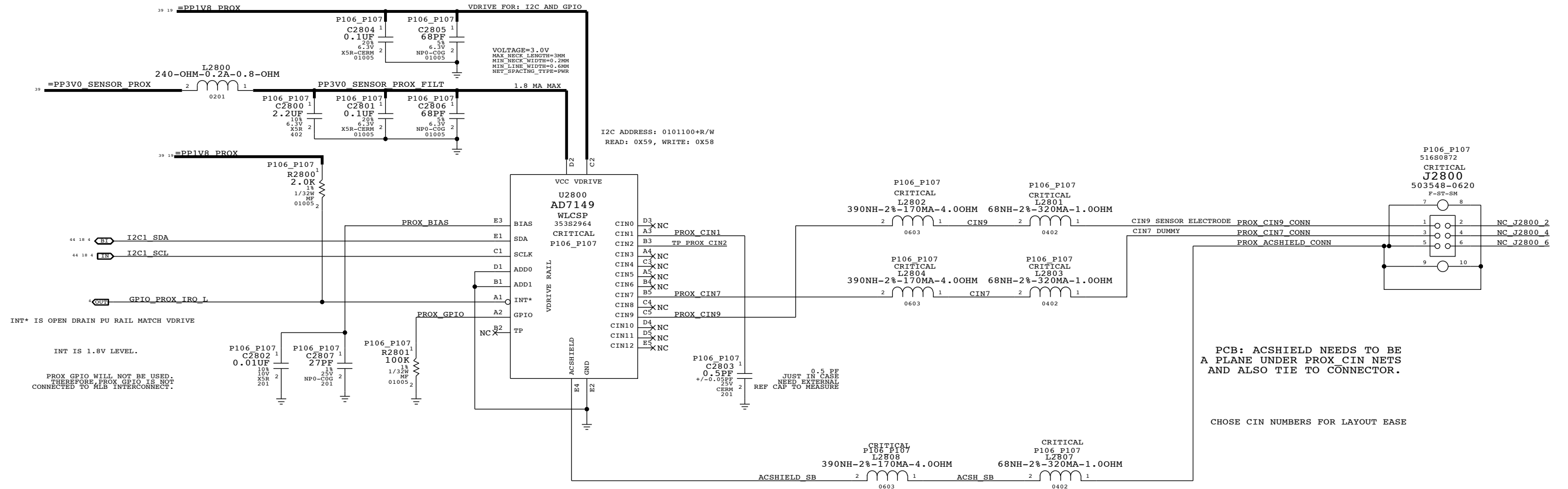
# COMPASS

WRITE: 0X18 READ: 0X19



SYNC MASTER=N/A		SYNC DATE=N/A	
<b>INERTIAL SENSORS</b>			
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# PROX SENSOR



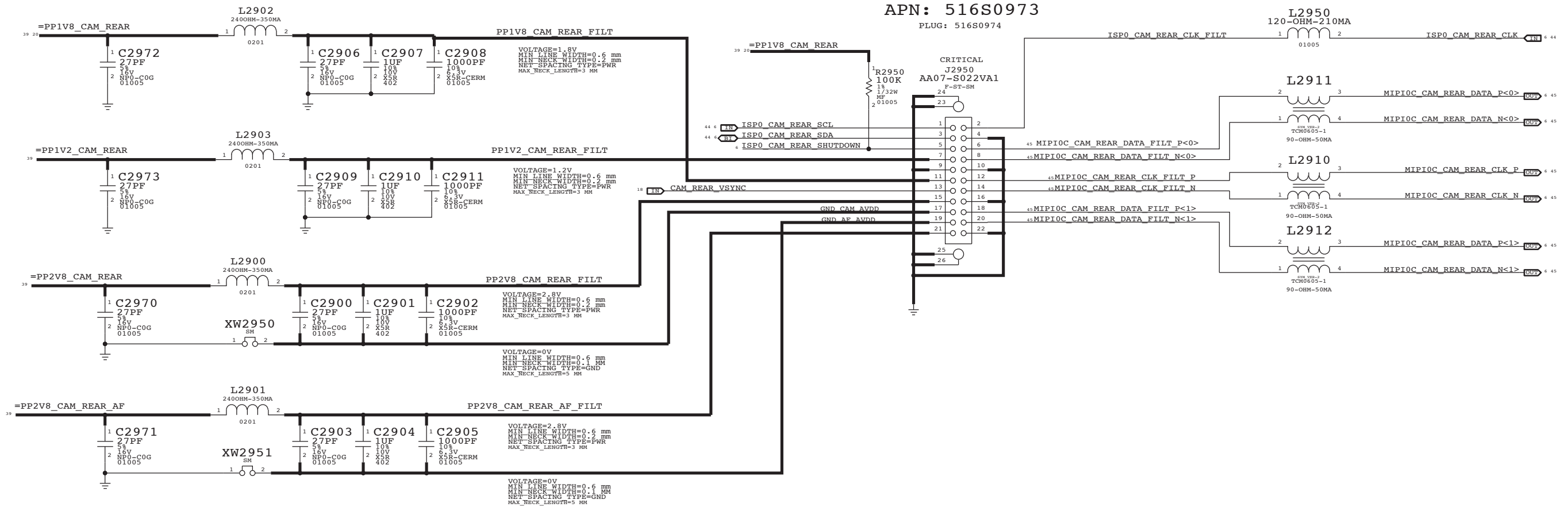
PCB: ENSURE ACSHIELD PLANE UNDER U3200, NO GND PLANE NEAR PROX\_CIN NETS..

PCB: ACSHIELD NEEDS TO BE A PLANE UNDER PROX\_CIN NETS AND ALSO TIE TO CONNECTOR.  
 CHOSE CIN NUMBERS FOR LAYOUT EASE

SYNC MASTER=N/A		SYNC DATE=N/A	
<b>PROX SENSOR</b>			
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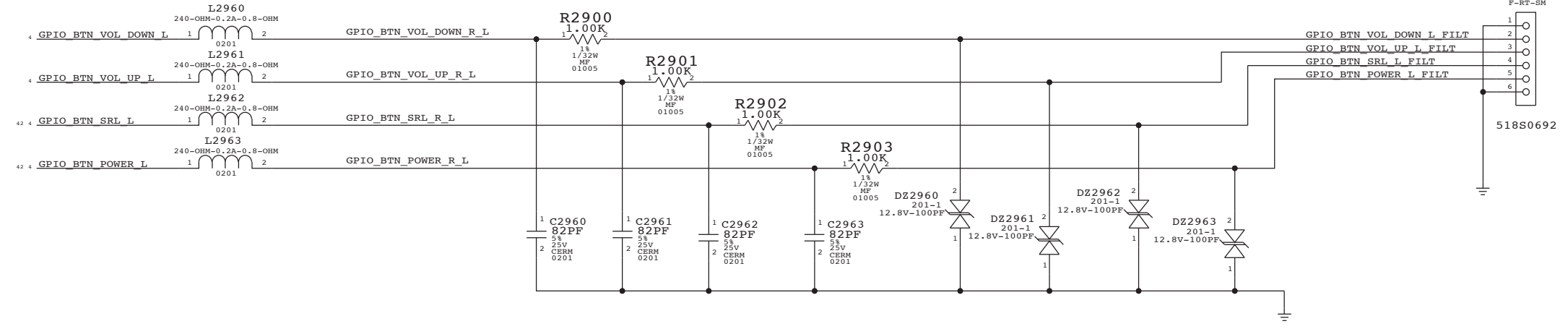
# REAR CAMERA CONNECTOR

APN: 516S0973  
PLUG: 516S0974



# BUTTON CONNECTOR

CRITICAL  
J2960  
FF18-6A-R11AD-B-3H  
F-RT-SM



PAGE TITLE		SYNC DATE=N/A	
<b>BUTTON &amp; REAR CAMERA CONN</b>			
Apple Inc.	DRAWING NUMBER	051-9374	SIZE
	REVISION	13.0.0	D
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# AP INTERFACE & DEBUG CONNECTOR

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## AP CONNECTIONS

34 33 31 30 29 23 22 21	PP_BATT_VCC_CONN	=	PPBATT_VCC_RF	39
25	TX_GTR_THRESH	=	GPIO_BB_GSM_TXBURST	4
24 23 21	BB_RST_L	=	GPIO_BB_RST_L	4
23 21	RESET_DET_L	=	GPIO_BB_RST_DET_L	4
23 21	RADIO_ON_L	=	GPIO_BB_RADIO_ON_L	4
23 21	RESET_PMU_L	=	PMU_GPIO_BB_RST_L	42
25 21	BB_WAKE_HOST	=	PMU_GPIO_BB_WAKE	42
21	RF_RESET_L	=	RST_SYSTEM_L	3 10 42
25 21	PBL_RUN_BB_HSIC1_RDY	=	GPIO_BB_HSIC_DEV_RDY	4
25	AP_WAKE_MODEM	=	GPIO_BB_IPC_GPIO	4
25 21	AP_HSIC1_RDY	=	GPIO_BB_HSIC_HOST_RDY	4
24 21	50_HSIC_BB_DATA	=	HSIC1_BB_DATA	3 44
24 21	50_HSIC_BB_STROBE	=	HSIC1_BB_STB	3 44

PP31007_RF	P4HM	SK 1	BB_ERROR_FLAG	25
PP31001_RF	P4HM	SK 1	SLEEP_CLK_32K	23 24
PP31006_RF	P4HM	SK 1	PMIC_SSB_I	23 24
PP31005_RF	P4HM	SK 1	RADIO_ON_L	21 23
PP31003_RF	P4HM	SK 1	PBL_RUN_BB_HSIC1_RDY	21 25
PP31004_RF	P4HM	SK 1	AP_HSIC1_RDY	21 25

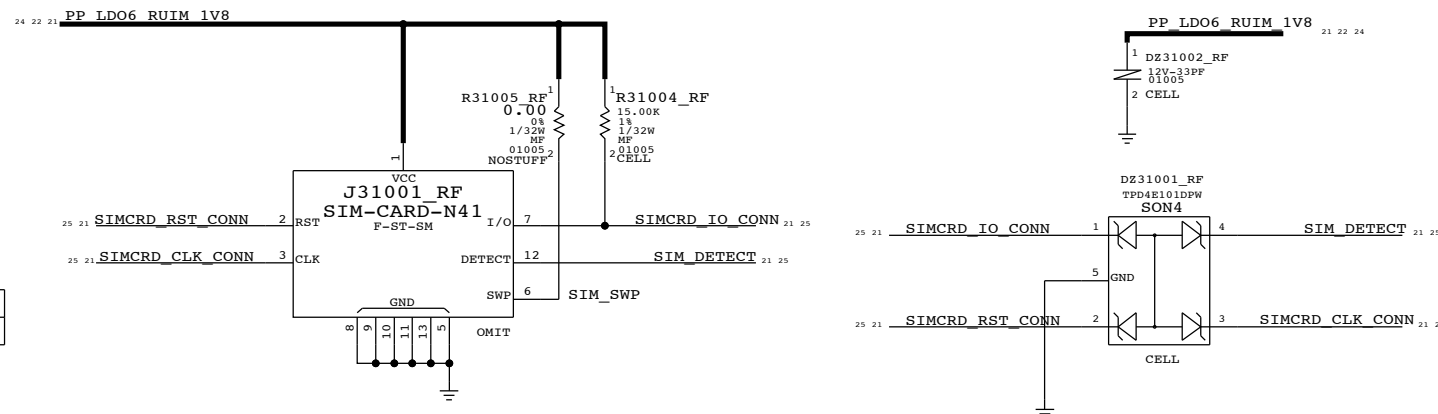
## BT UART

PP31013_RF	P4HM	SK 1	BT_UART_TXD	21 37
PP31014_RF	P4HM	SK 1	BT_UART_RXD	21 37

## BB NOR SPI

PP31015_RF	P4HM	SK 1	SPI_DATA_MOSI	25
PP31016_RF	P4HM	SK 1	SPI_DATA_MISO	25
PP31017_RF	P4HM	SK 1	SPI_CS_L	25
PP31018_RF	P4HM	SK 1	SPI_CLK	25

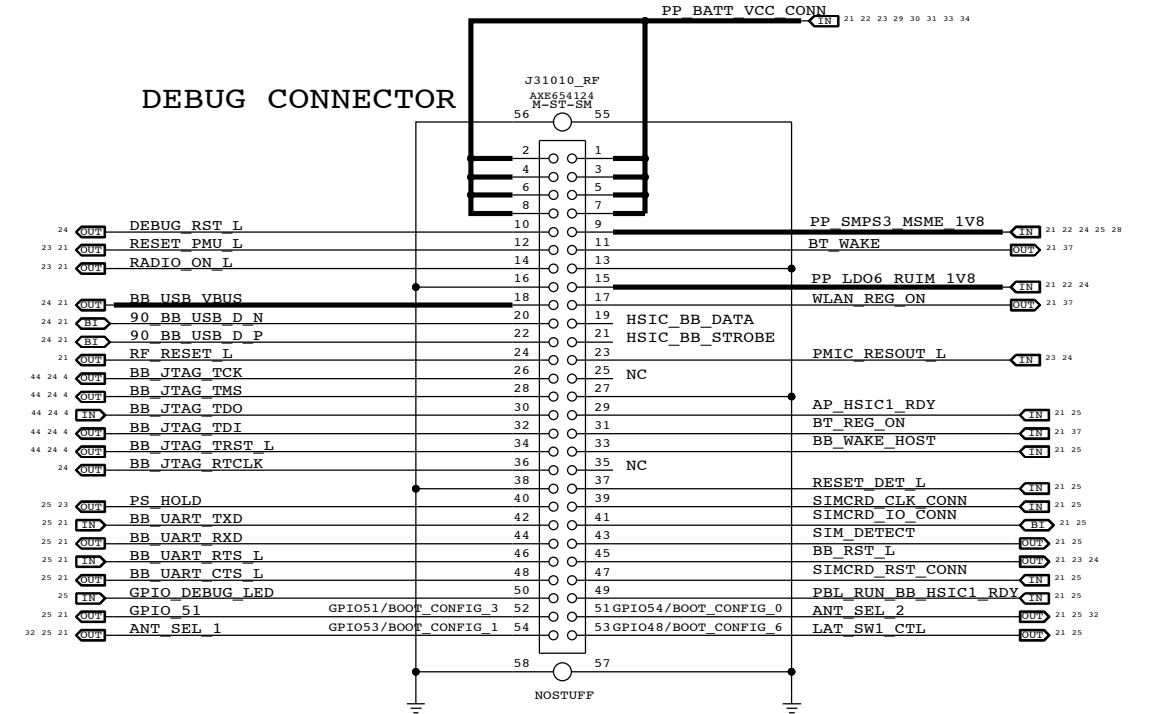
## SIM CARD CONNECTOR



PARTS TABLE FOR P105 SIM CARD, WHILE PINOUT IS BEING FIXED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
512S0098	1	P105 SIM TRAY	J31001_RF	CELL

## DEBUG CONNECTOR



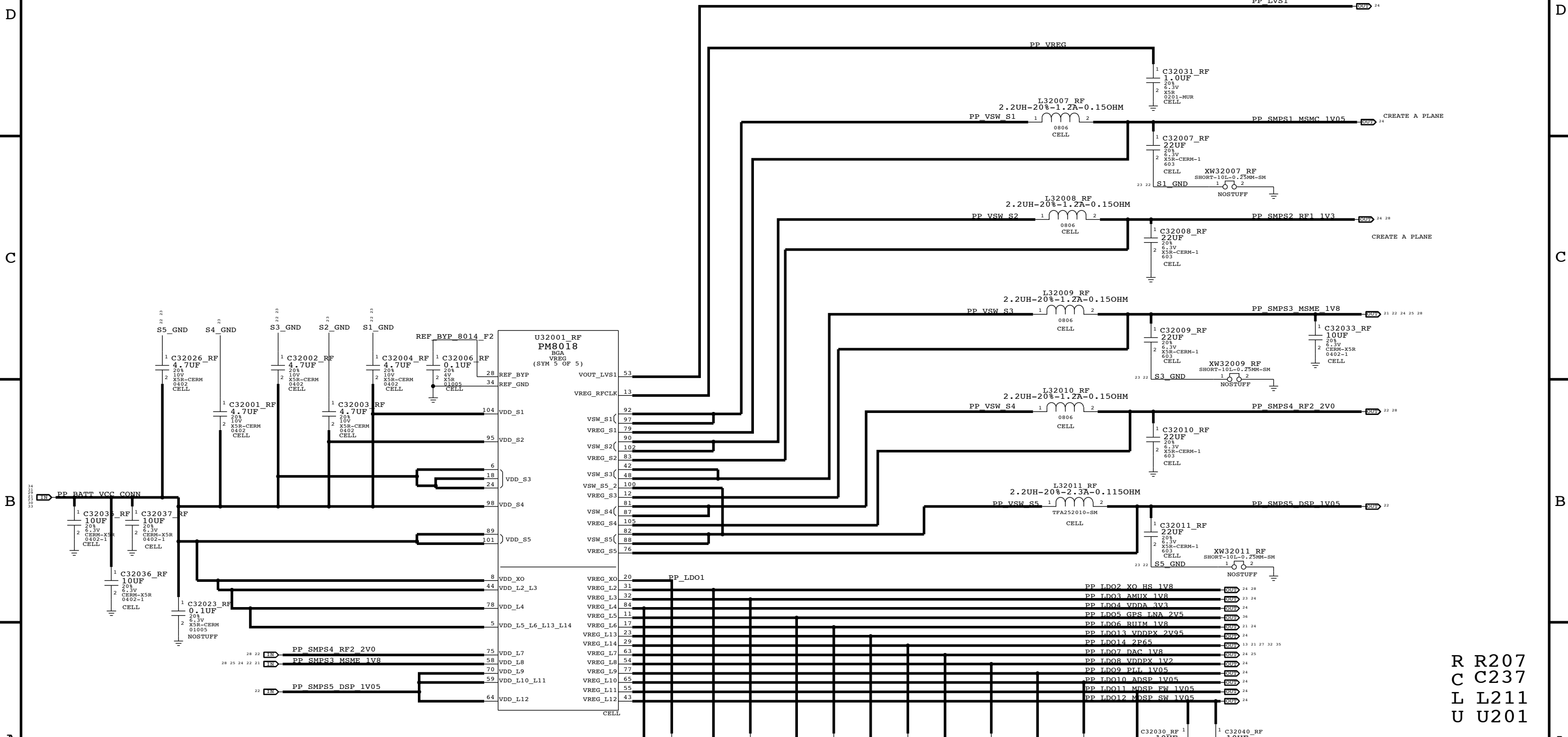
BOOT OPTIONS	BOOT_CONFIG SW REGISTER VALUE	GPIO/BOOT_CONFIG CONFIGURATION								
		6	5	4	3	2	1	0		
BOOT_DEFAULT_OPTION	0X00	X	0	0	0	0	0	0	0	X
BOOT_NAND_OPTION	0X01	X	1	0	0	0	0	0	1	X
BOOT_HSIC_OPTION	0X02	X	1	0	0	0	0	1	0	X
BOOT_USB_OPTION	0X03	X	1	0	0	0	0	1	1	X
ENABLE_SAHARA_PROTOCOL	0X08	X	1	0	0	1	0	X	X	X

R R104  
C CXXX  
XWXW206  
DZDZ101  
U U101

SYSTEM & DEBUG CONNECTORS		DRAWING NUMBER	SIZE
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# BASEBAND PMU (1 OF 2)

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R R207  
C C237  
L L211  
U U201

<b>BASEBAND PMU (1 OF 2)</b>	
	DRAWING NUMBER <b>051-9374</b>
REVISION <b>13.0.0</b>	
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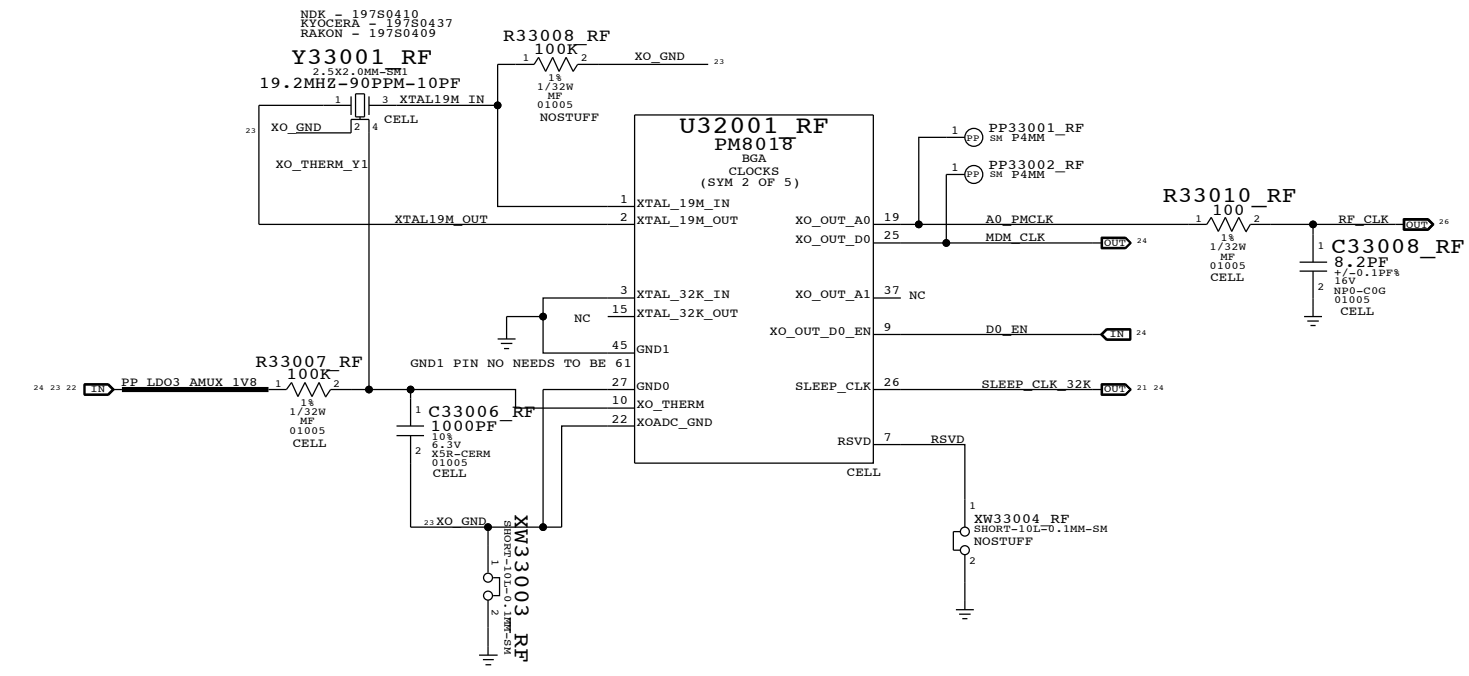
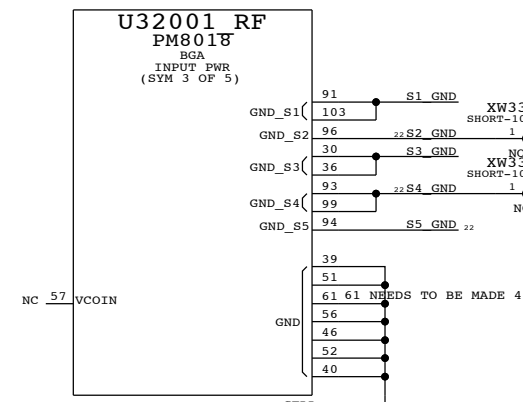
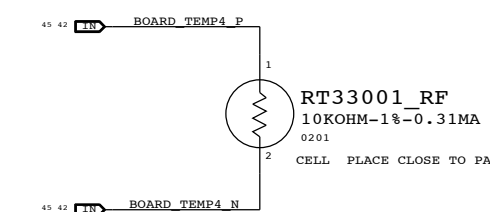
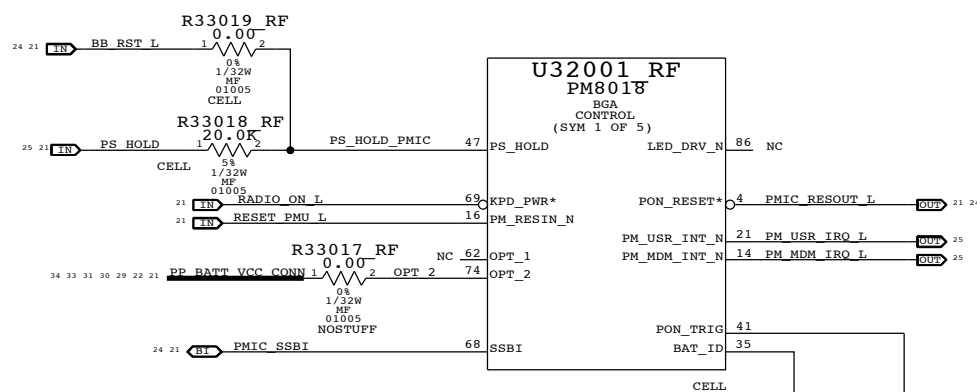
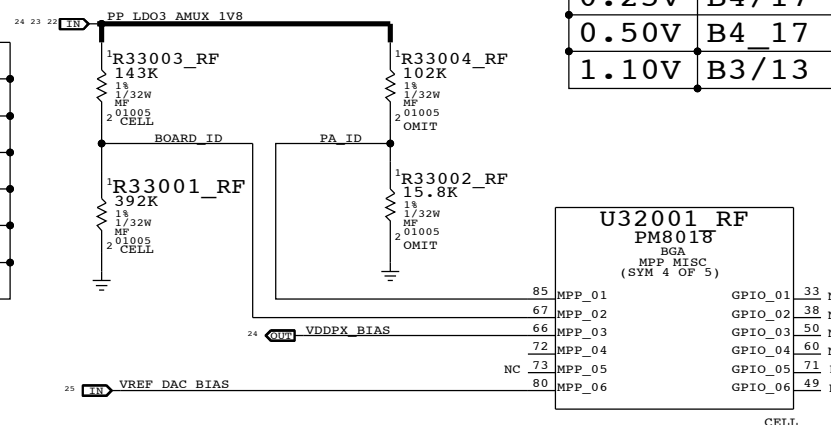


# BASEBAND PMU (2 OF 2)

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BOARD_ID	REVISION
0.25V	N41 PROTO 1
0.50V	N41 PROTO 2, X122 RF DEV 1
0.70V	N41 PROTO 3, X122 PROTO 0
0.90V	N41 EVT 1, X122 PROTO 1
1.10V	N41 EVT 2, X122 EVT
1.30V	N41 EVT 3, X122 DVT

PA_ID	PA CONFIG
0.25V	B4/17 CONFIG 0
0.50V	B4_17 CONFIG 1
1.10V	B3/13 CONFIG 0



## ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780437	19780410	CELL	Y33001_RF	KYOCERA CRYSTAL
19780409	19780410	CELL	Y33001_RF	RAKON CRYSTAL

## BOM OPTIONS

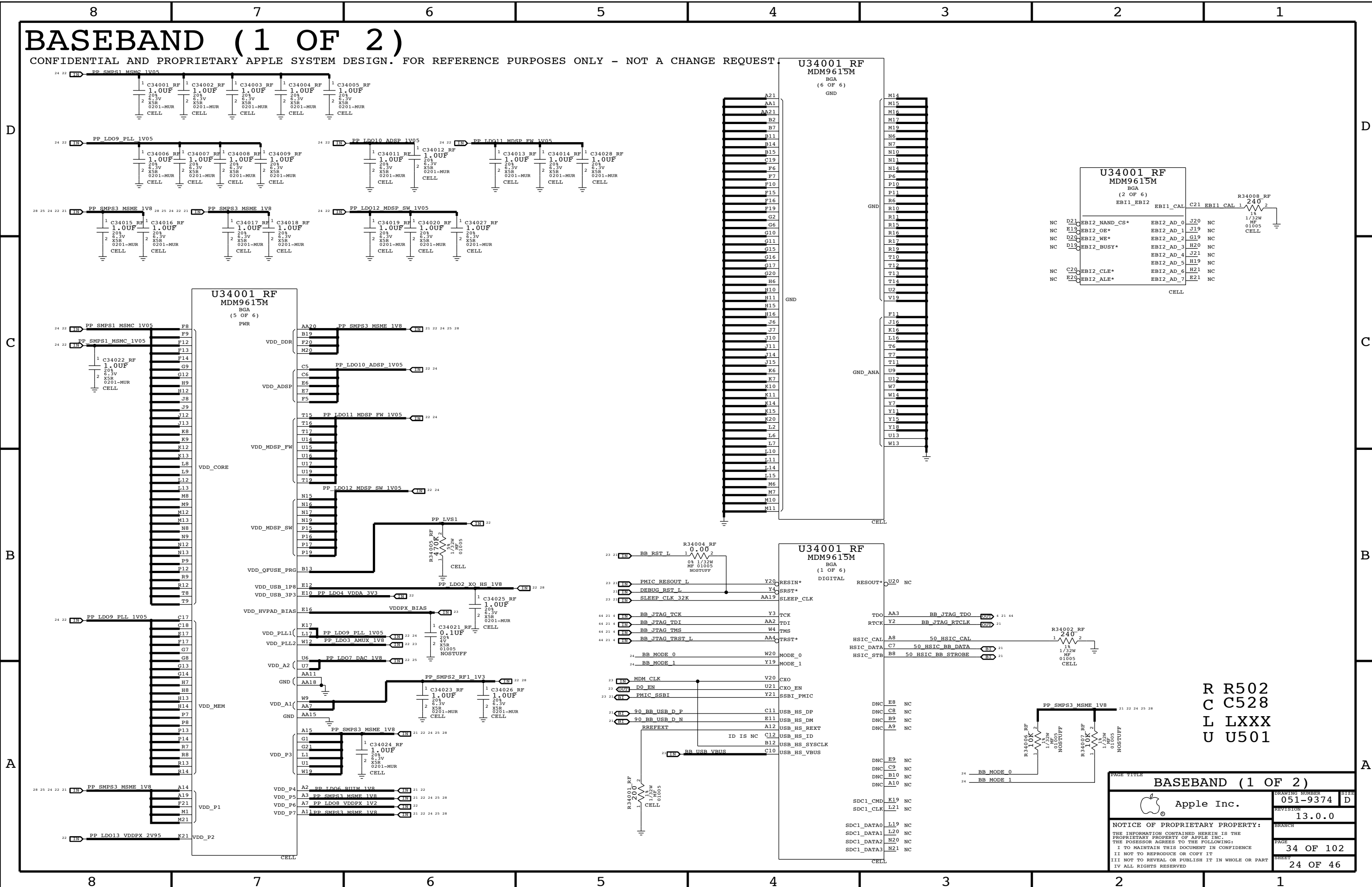
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
11880685	1	PA_ID RES DIVIDER 102K	R33004_RF	Y	B4_17
11880656	1	PA_ID RES DIVIDER 61.9K	R33004_RF	Y	B3_13
11880729	1	PA_ID RES DIVIDER 39K	R33002_RF	Y	B4_17
11880685	1	PA_ID RES DIVIDER 102K	R33002_RF	Y	B3_13

R R317  
C C309  
L LXXX  
U U301  
XW XW305


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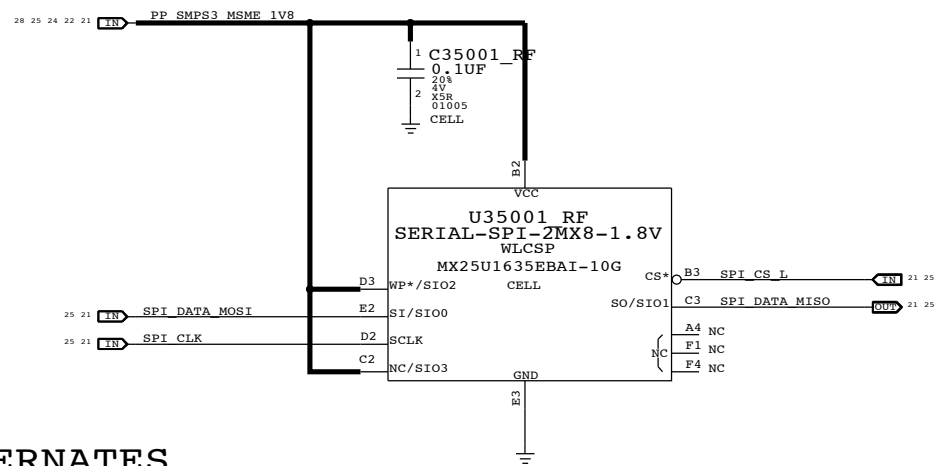
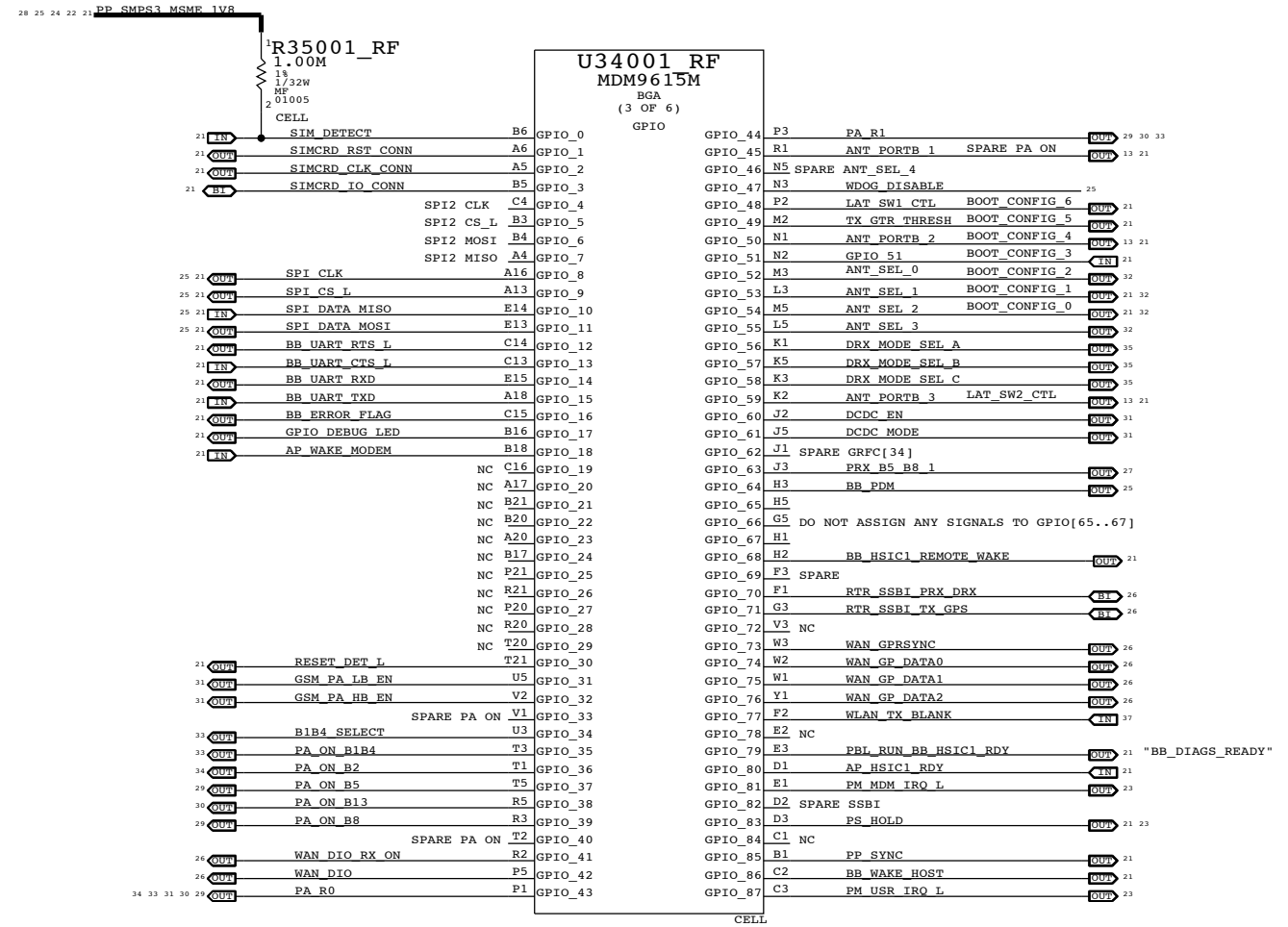
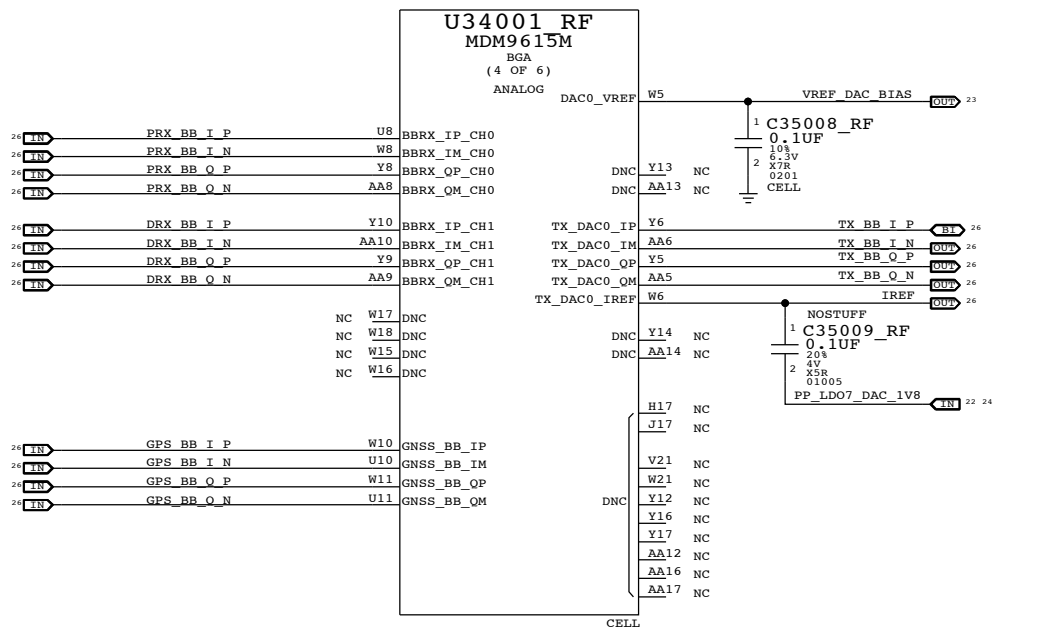


R R502  
C C528  
L LXXX  
U U501

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## ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
33580895	33580874	CELL	U35001_RF	WINBOND SPI NOR
33580899	33580874	CELL	U35001_RF	MICRON SPI NOR

R R608  
C C609  
L L601

**MOBILE DATA MODEM (2 OF 2)**

Apple Inc.

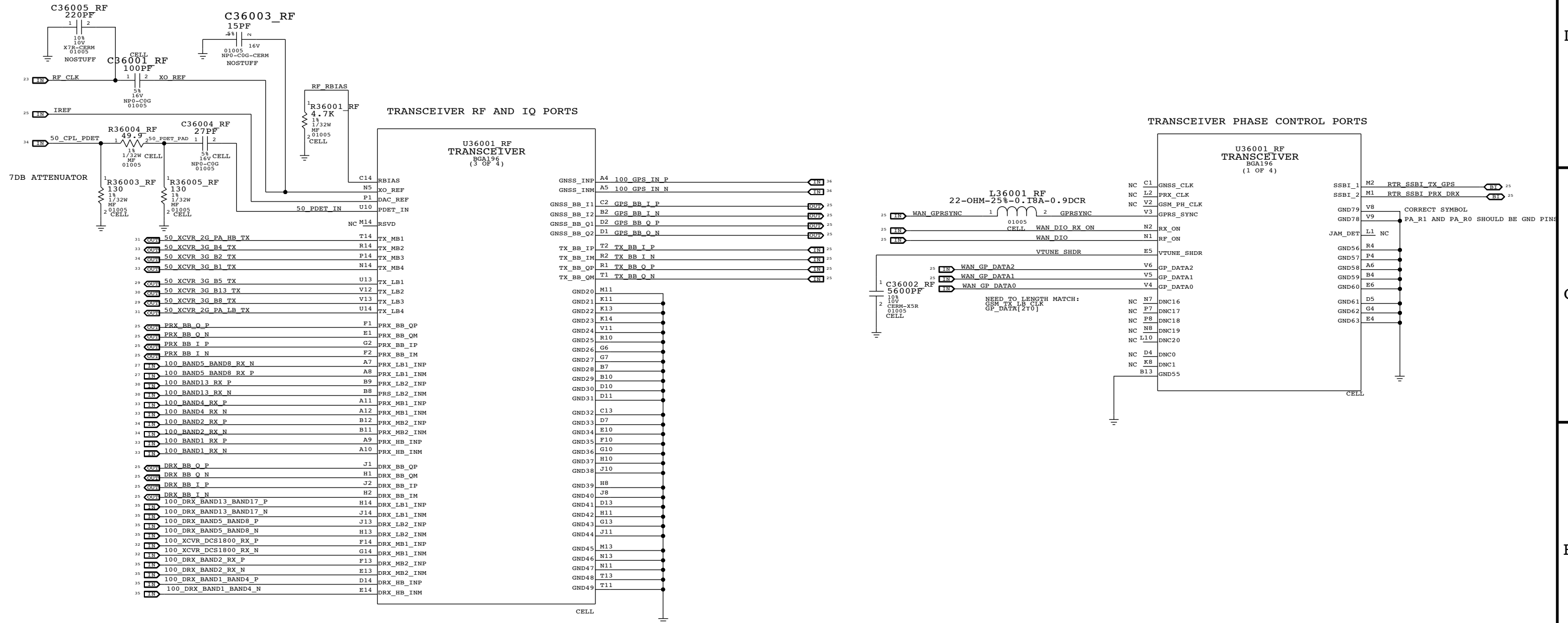
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REVISION: 13.0.0

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# RF TRANSCEIVER (1 OF 3)

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R R705  
C C705  
L LXXX  
U U701

RF TRANSCEIVER (1 OF 3)		
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# RF TRANSCEIVER SWITCHING NETWORKS (2 OF 3)

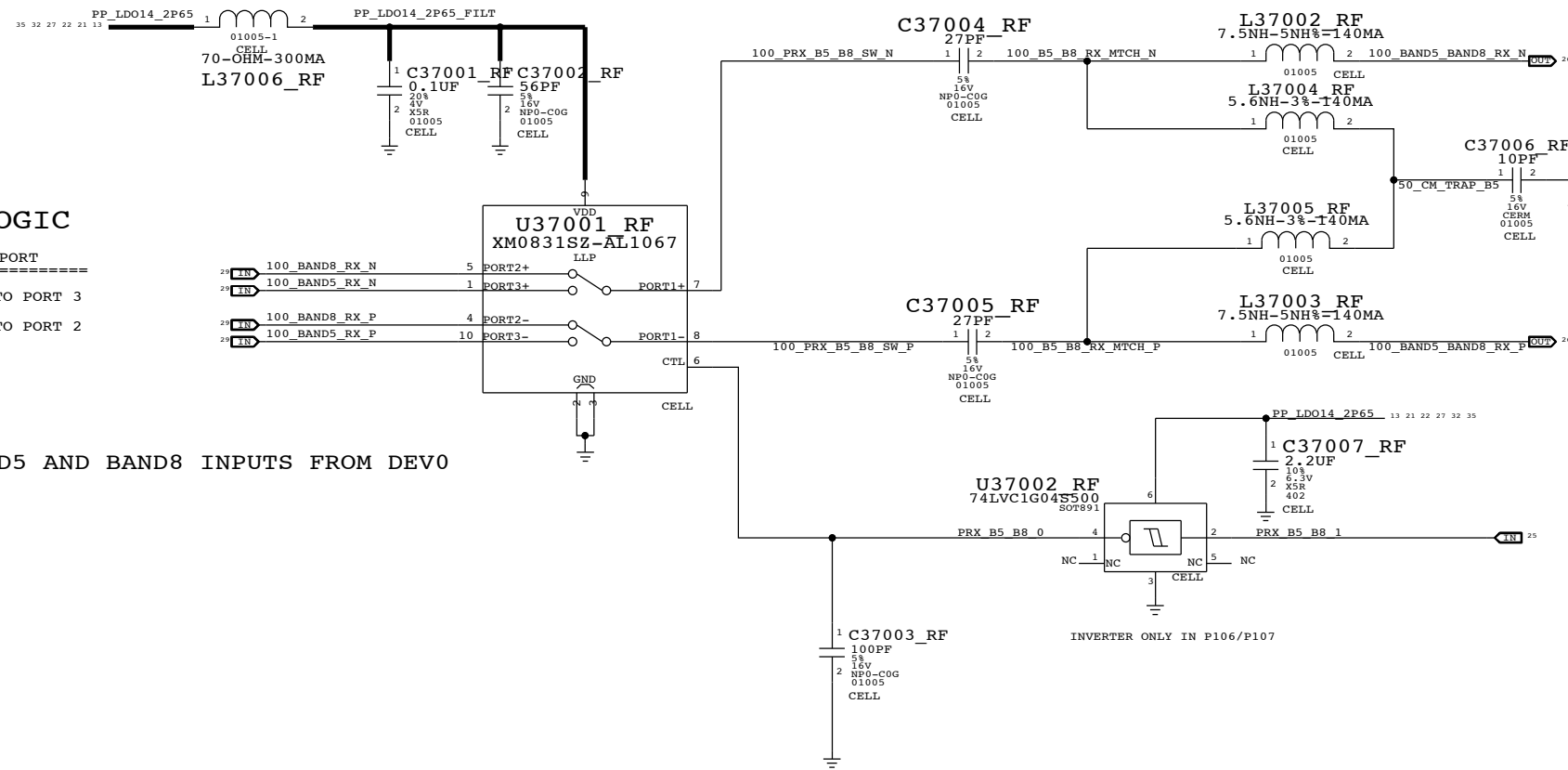
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## BAND 5/BAND 8 PRX TRANSCEIVER SWITCH

### XM0830SZ SWITCH LOGIC

PRX_B5_B8	ACTIVE BAND	PORT
HIGH	5	PORT 1 TO PORT 3
LOW	8	PORT 1 TO PORT 2

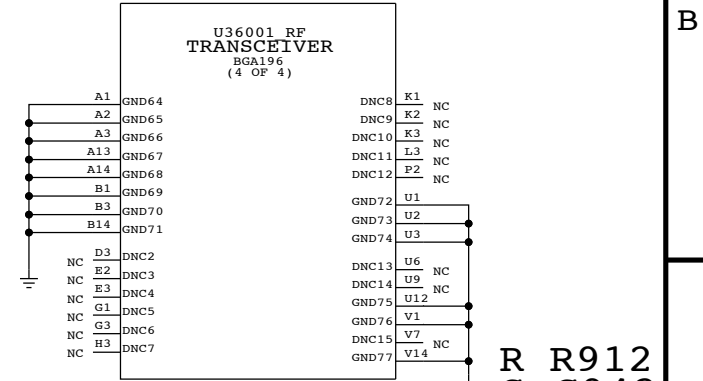
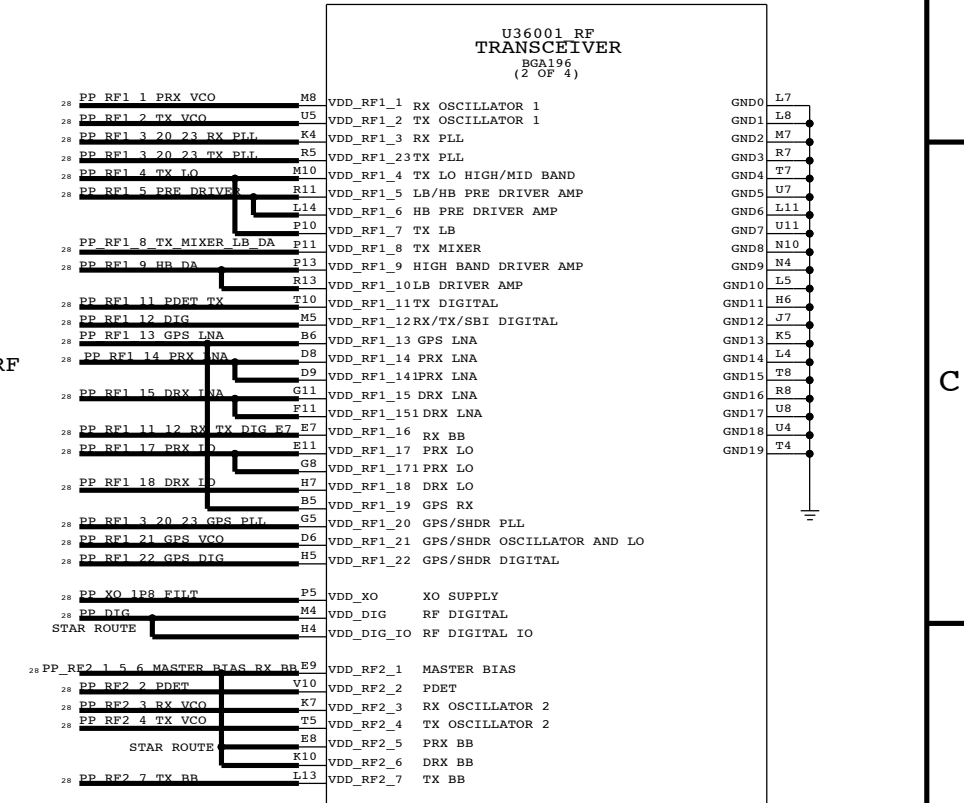
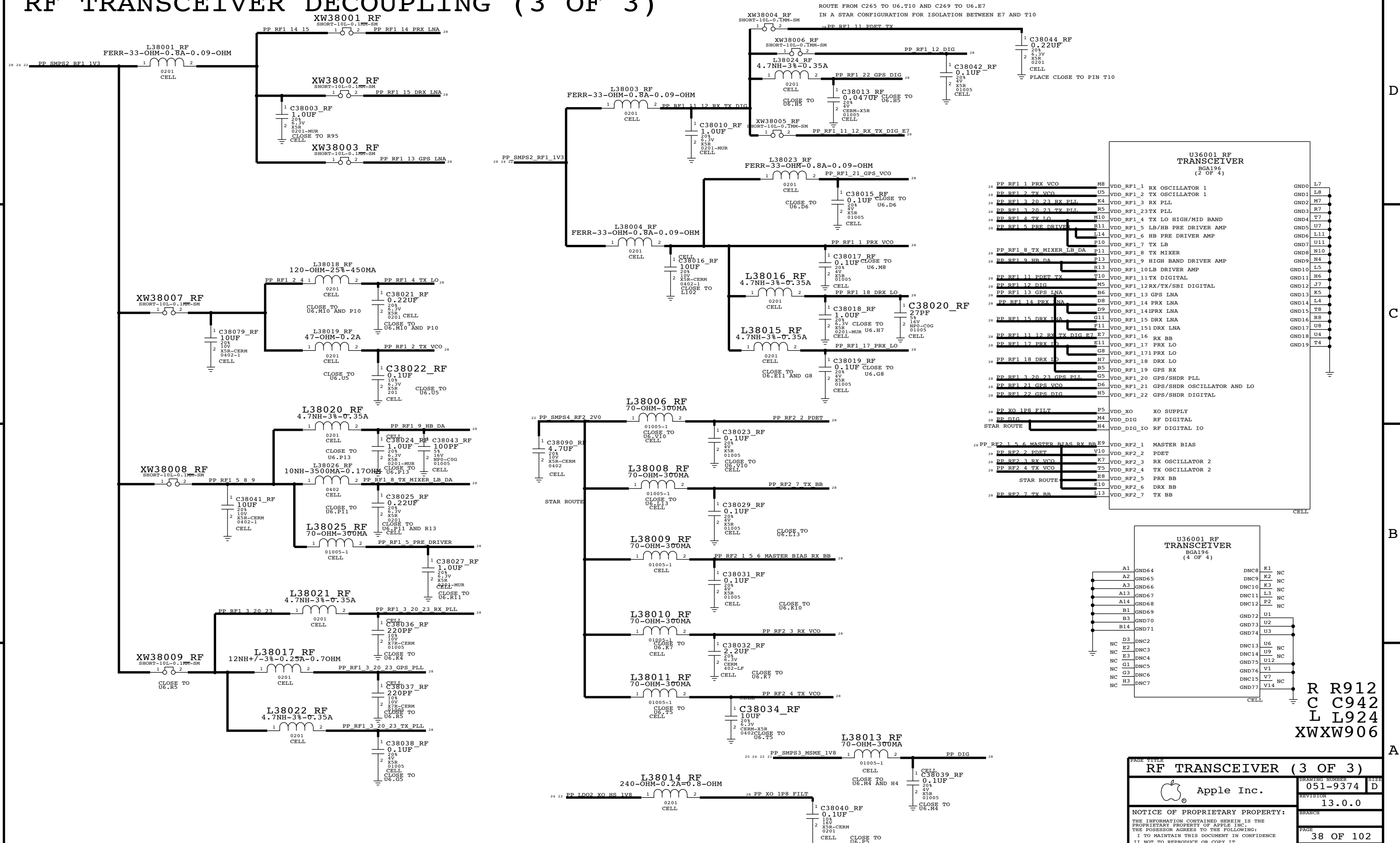
SWAPPED BAND5 AND BAND8 INPUTS FROM DEV0



R RXXX  
C C37007  
L L803  
U U801

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# RF TRANSCEIVER DECOUPLING (3 OF 3)

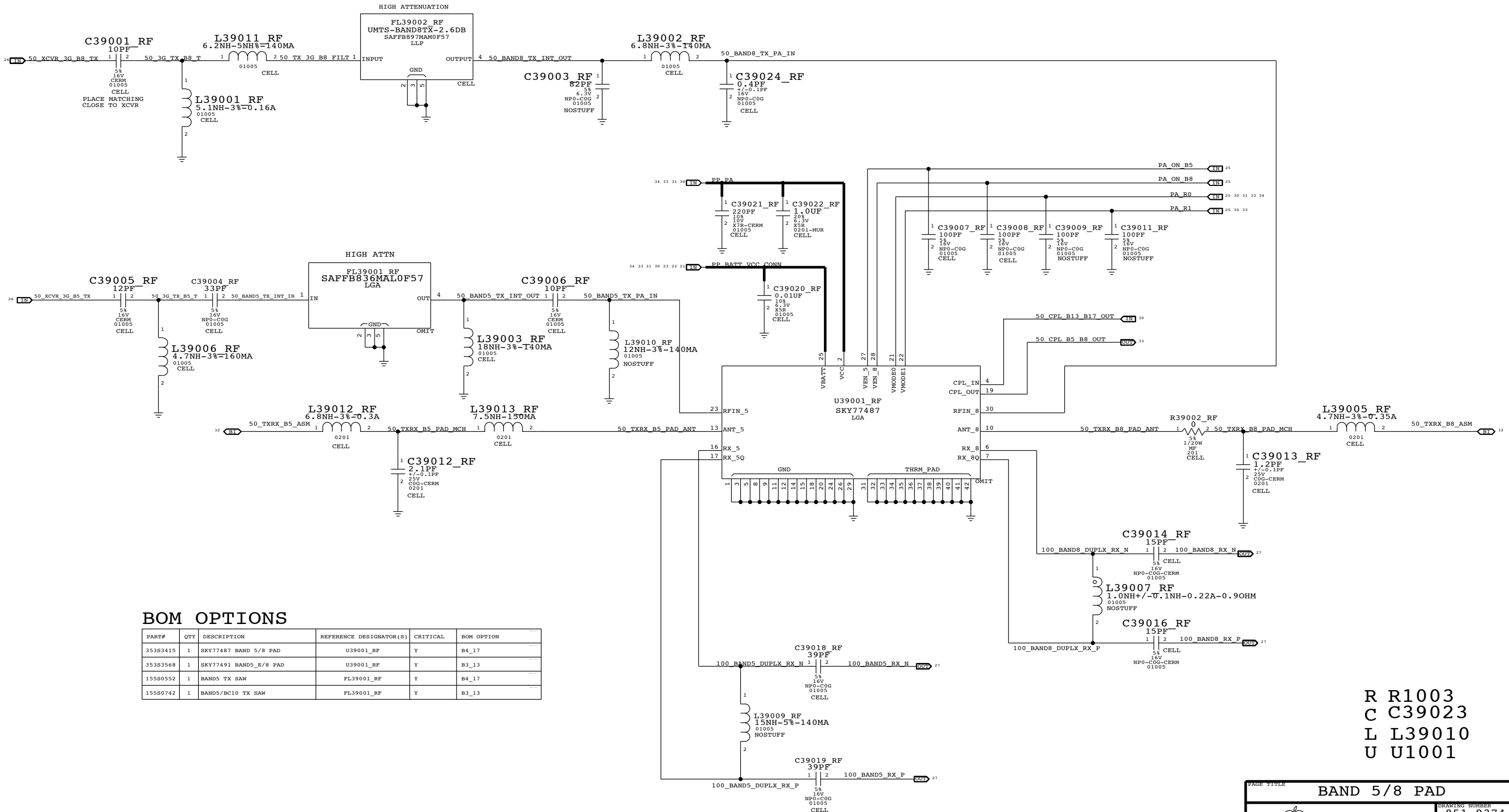


R R912  
C C942  
L L924  
XWXW906

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# BAND 5/8 PAD

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## BOM OPTIONS

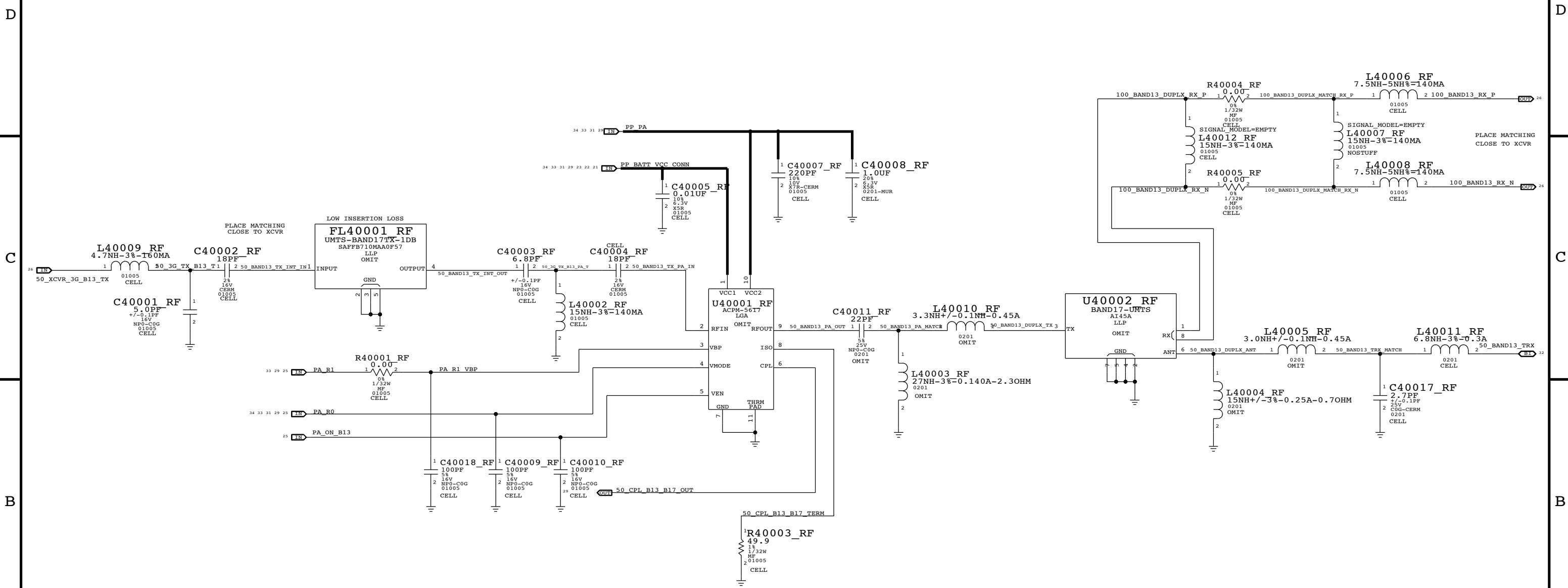
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S3415	1	SKY77487 BAND 5/8 PAD	U39001_RF	Y	B4_17
353S3568	1	SKY77491 BAND5_E/8 PAD	U39001_RF	Y	B3_13
155S0552	1	BAND5 TX SAW	FL39001_RF	Y	B4_17
155S0742	1	BAND5/BC10 TX SAW	FL39001_RF	Y	B3_13

R R1003  
C C39023  
L L39010  
U U1001

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# B13/17 INTERSTAGE, PA, AND DUPLEXER

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## BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15580620	1	BAND17 TX SAW	FL40001_RF	Y	B4_17
15580619	1	BAND13 TX SAW	FL40001_RF	Y	B3_13
35383567	1	BAND17 PAM - SKY77729	U40001_RF	Y	B4_17
35383441	1	BAND13 PAM - AVAGO ACPM-5613	U40001_RF	Y	B3_13
15580709	1	BAND17 DUPLEXER	U40002_RF	Y	B4_17
15580738	1	BAND13 DUPLEXER	U40002_RF	Y	B3_13
15281280	1	5.1 NH INDUCTOR, 0201	C40011_RF	Y	B4_17
13180129	1	22 PF CAPACITOR, 0201	C40011_RF	Y	B3_13
13180198	1	1.8 PF CAPACITOR, 0201	L40003_RF	Y	B4_17
11780002	1	0 OHMS RESISTOR, 0201	L40010_RF	Y	B4_17
15281284	1	3.3 NH INDUCTOR, 0201	L40010_RF	Y	B3_13
15281336	1	8.2 NH INDUCTOR, 0201	L40004_RF	Y	B4_17
15281342	1	15 NH INDUCTOR, 0201	L40004_RF	Y	B3_13
15281063	1	2.2 NH INDUCTOR, 0201	L40005_RF	Y	B4_17
15281222	1	3.0 NH INDUCTOR, 0201	L40005_RF	Y	B3_13

## PA POWER MODES

MODE	PA_R0	PA_R1
LOW	HIGH	HIGH
MEDIUM	LOW	HIGH
HIGH	LOW	LOW

FLFL1101  
R R1102  
C C1118  
L L1108  
U U1102

PAGE TITLE		
<b>BAND 13 PA</b>		
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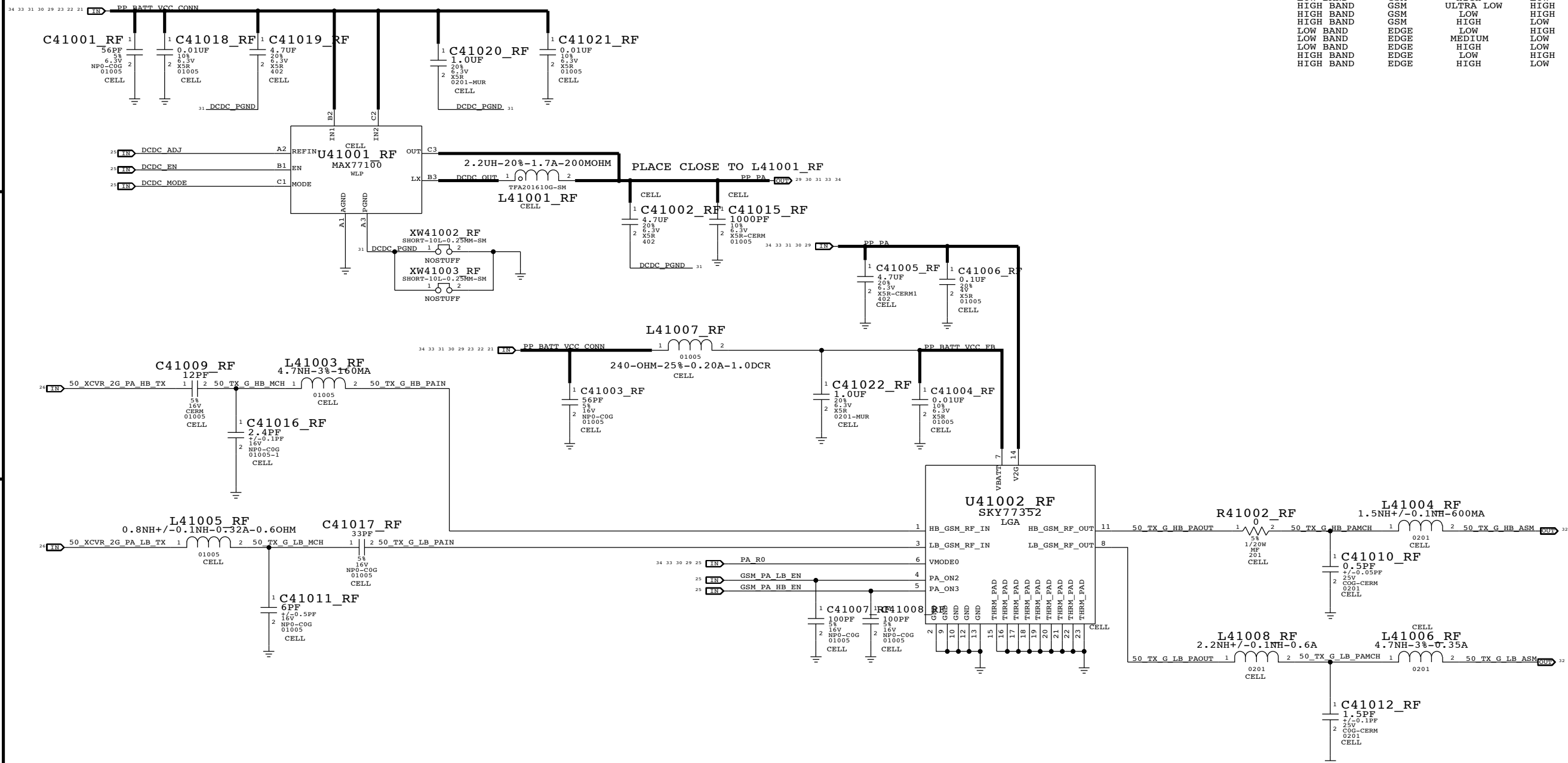


# 2G PA, PA DC/DC CONVERTER

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## 2G PA GAIN MODES

BAND	MODE	GAIN MODE	PA R1	PCL RANGE
LOW BAND	GSM	ULTRA LOW	HIGH	16 TO 19
LOW BAND	GSM	LOW	HIGH	14 TO 15
LOW BAND	GSM	MEDIUM	LOW	7 TO 13
LOW BAND	GSM	HIGH	LOW	5 TO 6
HIGH BAND	GSM	ULTRA LOW	HIGH	10 TO 15
HIGH BAND	GSM	LOW	HIGH	7 TO 9
HIGH BAND	GSM	HIGH	LOW	0 TO 6
LOW BAND	EDGE	LOW	HIGH	15 TO 19
LOW BAND	EDGE	MEDIUM	LOW	10 TO 14
LOW BAND	EDGE	HIGH	LOW	8 TO 9
HIGH BAND	EDGE	LOW	HIGH	9 TO 15
HIGH BAND	EDGE	HIGH	LOW	2 TO 8

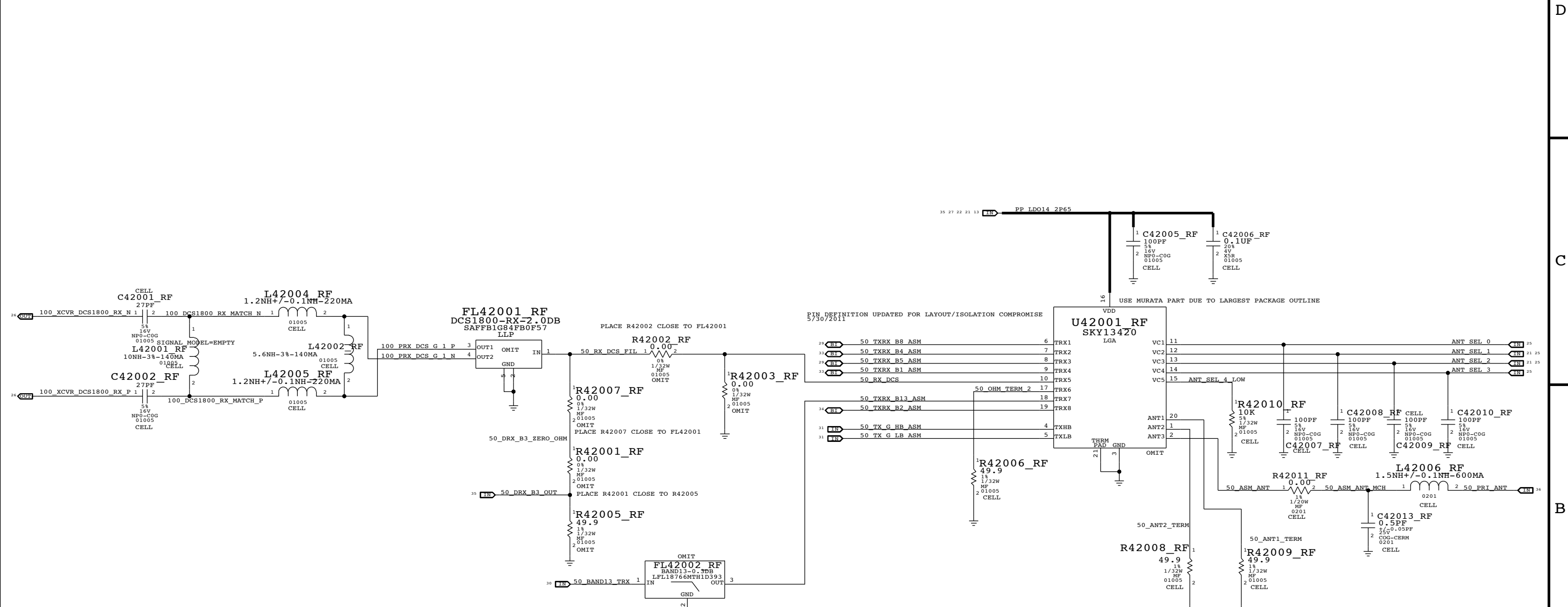


R R1209  
C C1215  
L L41007  
U U1202

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2G PA, DCDC CONVERTER		051-9374	D
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# ASM, DCS RX

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## BOM OPTIONS

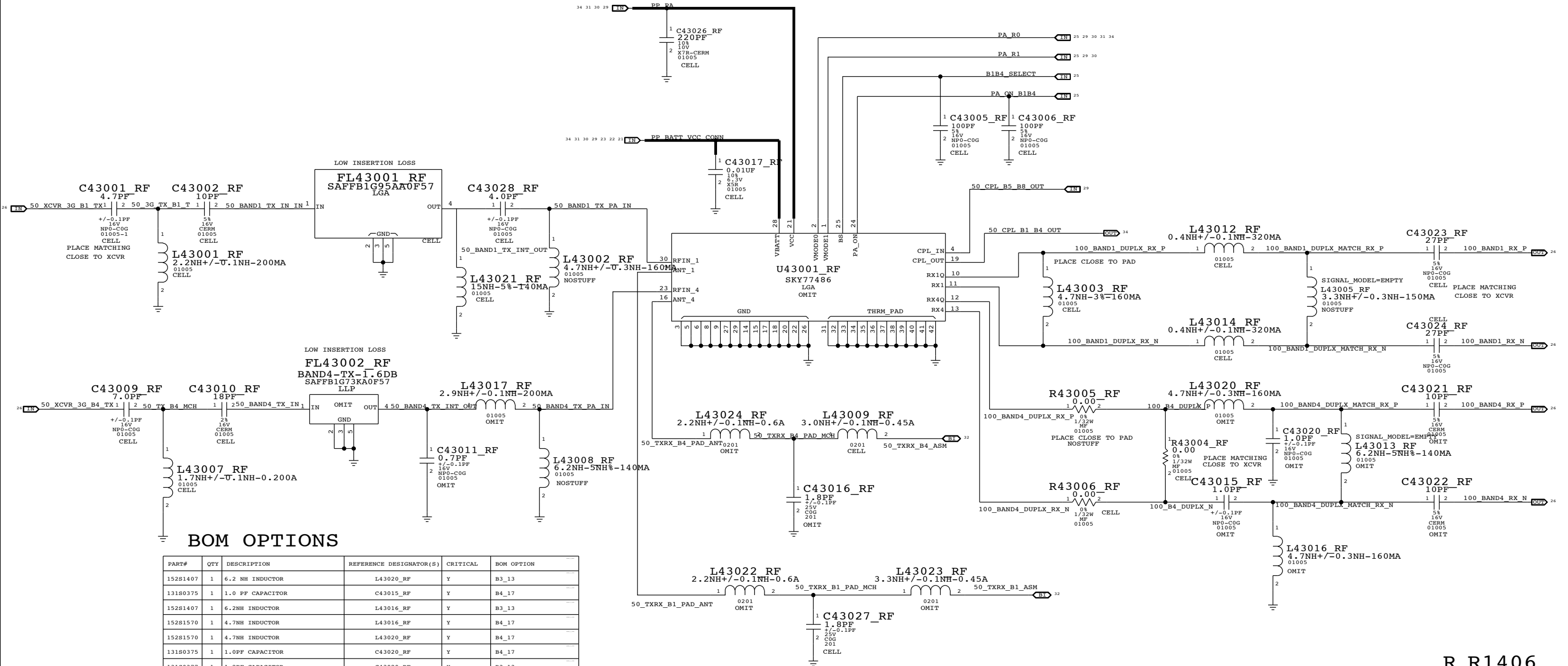
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15580596	1	DCS1800 RX FIL	FL42001_RF	Y	B4_17
15580729	1	BAND3 RX FIL	FL42001_RF	Y	B3_13
15580695	1	THRU LINE	FL42002_RF	Y	B4_17
15580722	1	BAND13 TX LFP	FL42002_RF	Y	B3_13
11780161	1	00HM RES	R42001_RF	Y	B3_13
11780161	1	00HM RES	R42002_RF	Y	B4_17
11880652	1	49.90HM RES	R42003_RF	Y	B3_13
11880652	1	49.90HM RES	R42005_RF	Y	B4_17
11780161	1	00HM RES	R42007_RF	Y	B3_13
35383573	1	ASM, SKYWORKS	U42001_RF	Y	B4_17
35383573	1	ASM, SKYWORKS	U42001_RF	Y	B3_13

R R42011  
C C42013  
L 42006  
U U1301  
FL FL1302

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DCS RX, ASM		
	DRAWING NUMBER	051-9374
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# BAND 1/4 PAD

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## BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
15281407	1	6.2 NH INDUCTOR	L43020_RF	Y	B3_13
13180375	1	1.0 PF CAPACITOR	C43015_RF	Y	B4_17
15281407	1	6.2NH INDUCTOR	L43016_RF	Y	B3_13
15281570	1	4.7NH INDUCTOR	L43016_RF	Y	B4_17
15281570	1	4.7NH INDUCTOR	L43020_RF	Y	B4_17
13180375	1	1.0PF CAPACITOR	C43020_RF	Y	B4_17
13180377	1	1.2PF CAPACITOR	C43020_RF	Y	B3_13
13180377	1	1.2PF CAPACITOR	C43015_RF	Y	B3_13
13180377	1	1.2 PF CAPACITOR	C43011_RF	Y	B4_17
15281571	1	5.6 NH INDUCTOR	C43011_RF	Y	B3_13
15281567	1	3.3 NH INDUCTOR	L43017_RF	Y	B4_17
13180215	1	22 PF CAPACITOR	L43017_RF	Y	B3_13
13180198	1	1.8 PF CAPACITOR	C43016_RF	Y	B4_17
13180337	1	1.5 PF CAPACITOR	C43016_RF	Y	B3_13
15281407	1	6.2NH INDUCTOR	L43013_RF	Y	B4_17
15281571	1	5.6NH INDUCTOR	L43013_RF	Y	B3_13
13180219	1	10PF CAPACITOR	C43021_RF	Y	B4_17
13180219	1	10PF CAPACITOR	C43022_RF	Y	B4_17
13180307	1	100PF CAPACITOR	C43021_RF	Y	B3_13
13180307	1	100PF CAPACITOR	C43022_RF	Y	B3_13

## BOM OPTIONS

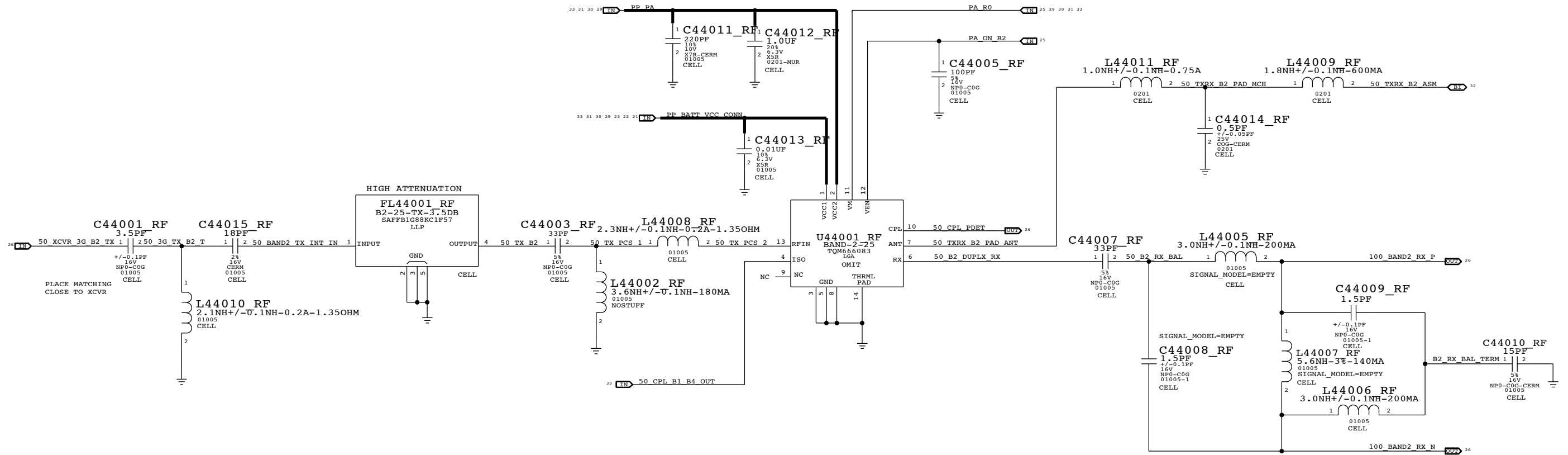
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35383255	1	B1/4 PAD, AVAGO AFEM-7814	U43001_RF	Y	B4_17
35383443	1	B1/3 PAD, AVAGO AFEM-7813	U43001_RF	Y	B3_13
15580590	1	B4 TX FIL	FL43002_RF	Y	B4_17
15580712	1	B3 TX FIL	FL43002_RF	Y	B3_13
15281063	1	2.2NH INDUCTOR	L43022_RF	Y	B4_17
15281222	1	3.0NH INDUCTOR	L43022_RF	Y	B3_13
15281284	1	3.3NH INDUCTOR	L43023_RF	Y	B4_17
15281222	1	3.0NH INDUCTOR	L43023_RF	Y	B3_13
15281063	1	2.2NH INDUCTOR	L43024_RF	Y	B4_17
15281222	1	3.0NH INDUCTOR	L43024_RF	Y	B3_13

R R1406  
C C43027  
L L43018  
U U1401  
FL FL1101

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# BAND2 PAD


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## BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35383715	1	B2 PAD, TRIQUINT B2 PAD	U44001_RF	Y	B4_17
35383459	1	B2 PAD, TRIQUINT B25 PAD	U44001_RF	Y	B3_13

R R1501  
 C C44014  
 L L1509  
 U U1501  
 FL FL1501

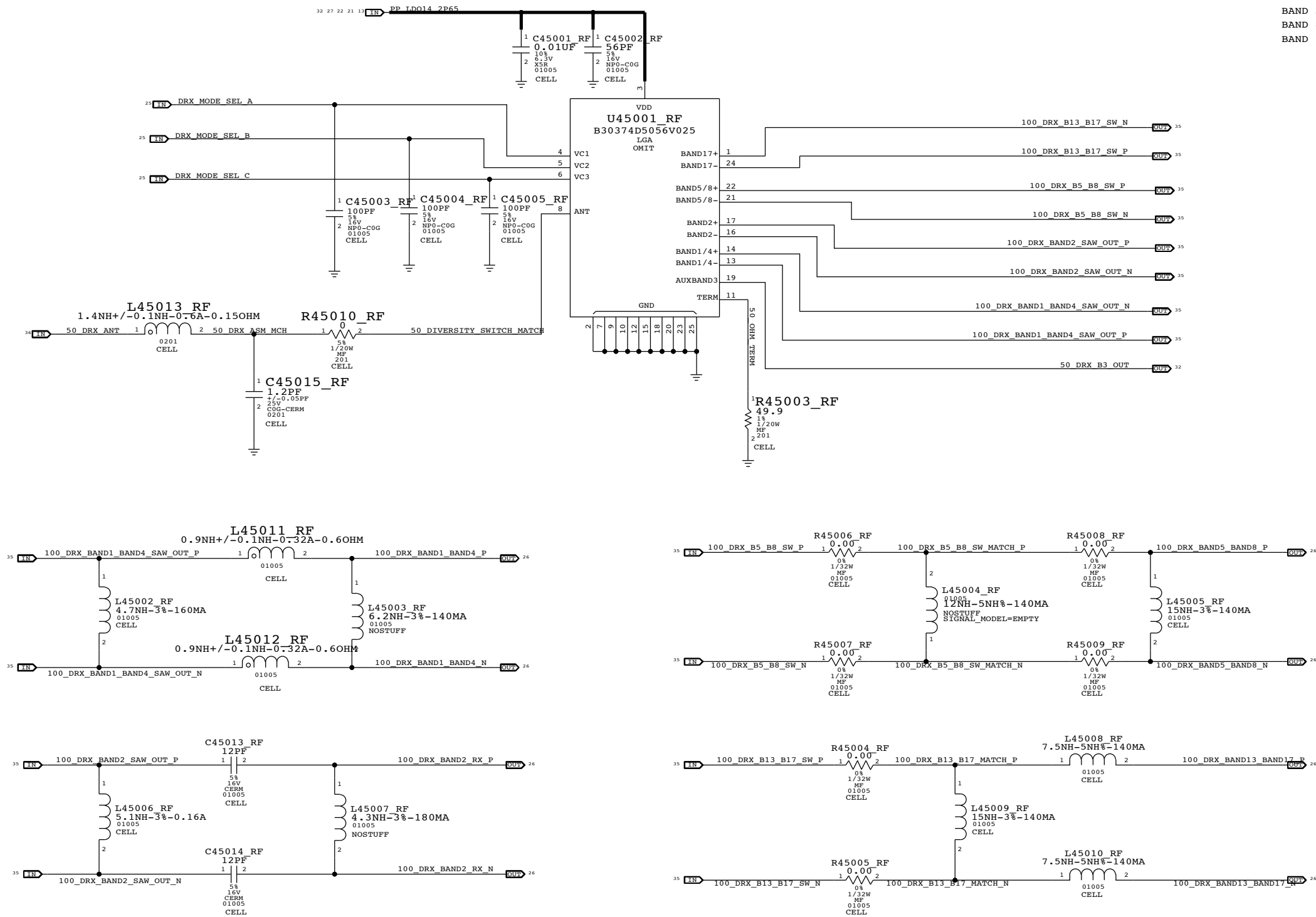
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# RX DIVERSITY

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## DIVERSITY MODULE LOGIC

BAND VC1 VC2 VC3  
 =====  
 BAND 1/4  
 BAND 2  
 BAND 5  
 BAND 8  
 BAND 13/17



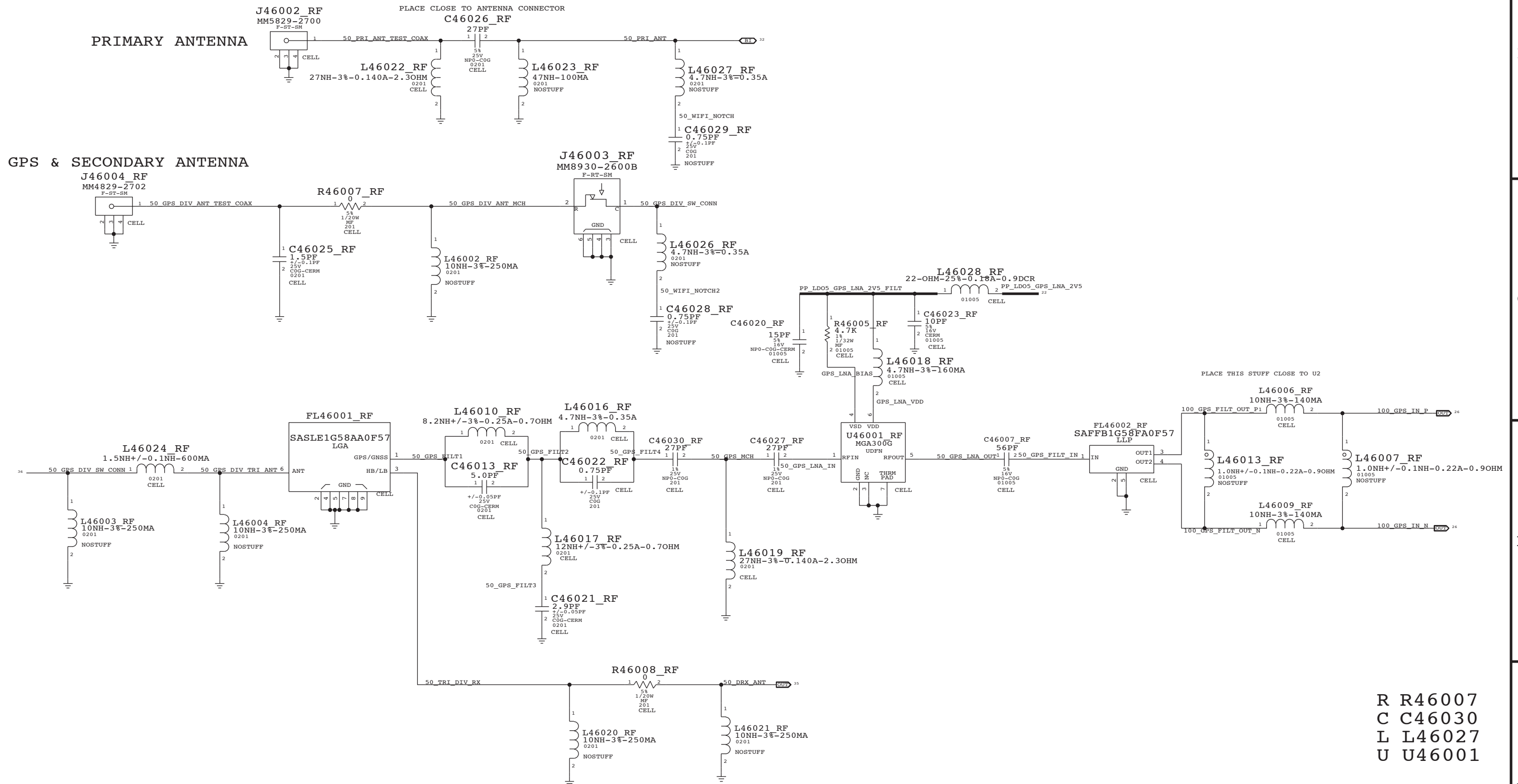
R R1603  
 C C1616  
 L L1610  
 U U1601

### BOM OPTIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
35383538	1	EPCOS B17 DIVERSITY MODULE	U45001_RF	Y	B4_17
35383537	1	EPCOS B13/BC10 DIV. MODULE	U45001_RF	Y	B3_13

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# GPS



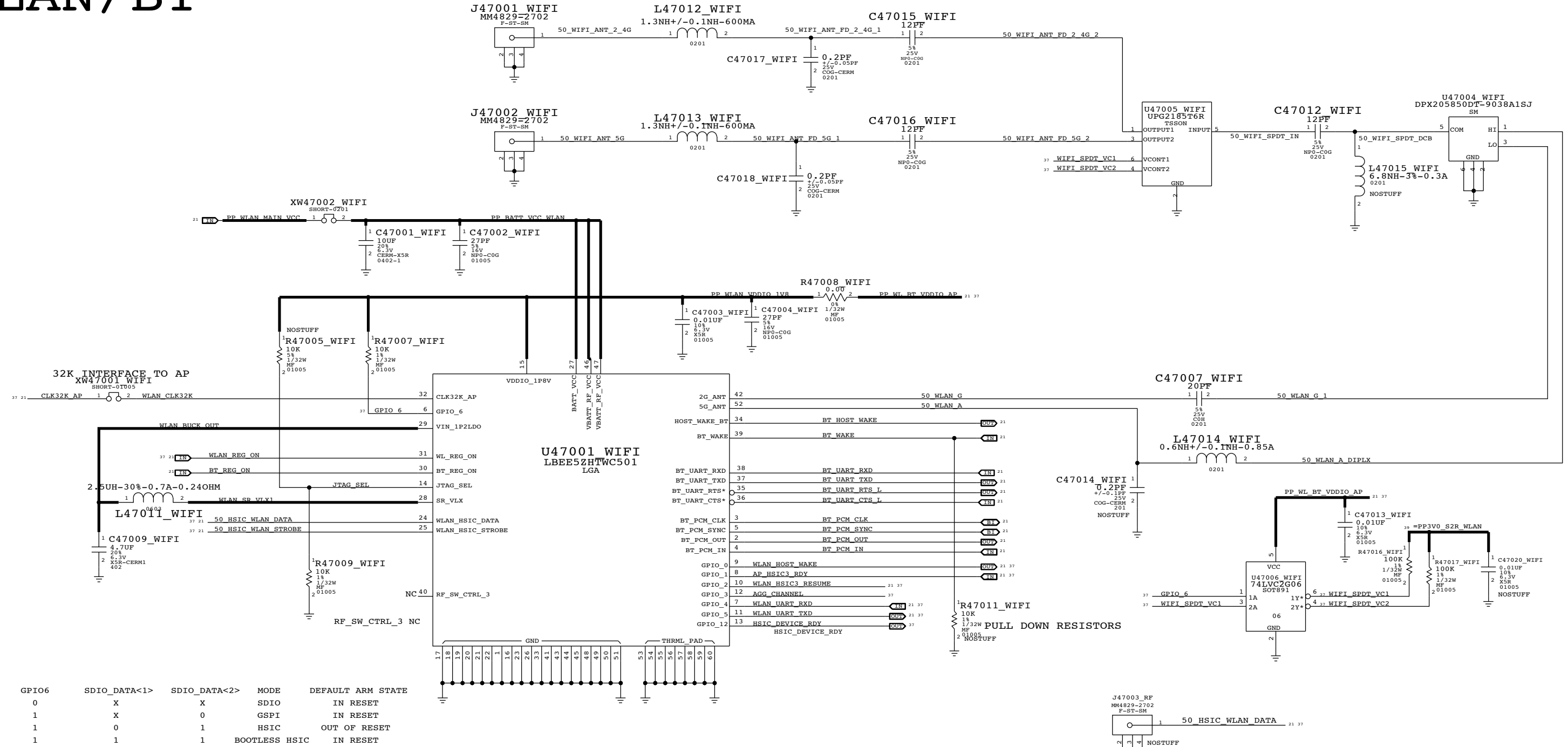
R R46007  
 C C46030  
 L L46027  
 U U46001

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# WLAN/BT

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GPIO6	SDIO_DATA<1>	SDIO_DATA<2>	MODE	DEFAULT ARM STATE
0	X	X	SDIO	IN RESET
1	X	0	GSPI	IN RESET
1	0	1	HSIC	OUT OF RESET
1	1	1	BOOTLESS HSIC	IN RESET

ALTERNATES				
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
31180548	31180398		U47002_WIFI	
33980175	33980171		U47001_WIFI	WIFI MODULE - USI
33980185	33980171		U47001_WIFI	WIFI MODULE - TDK

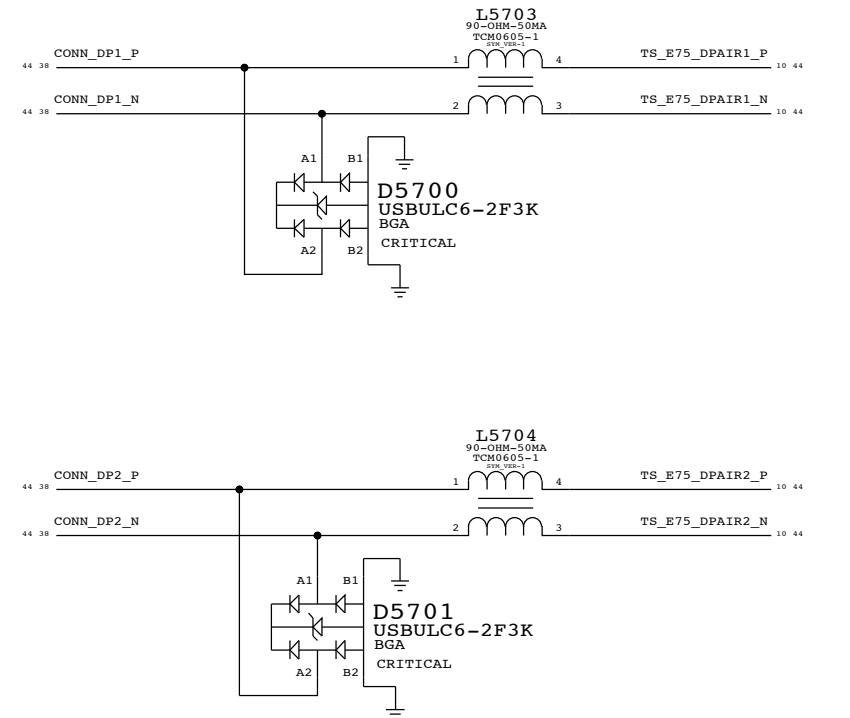
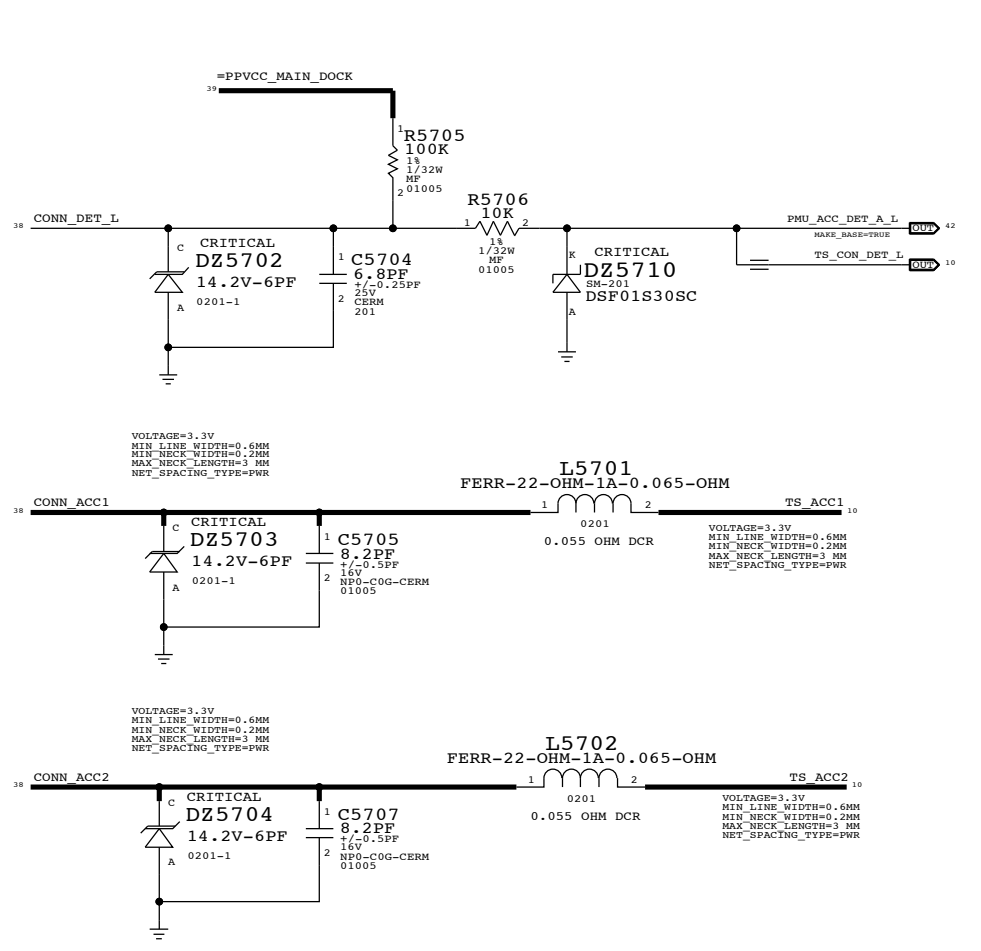
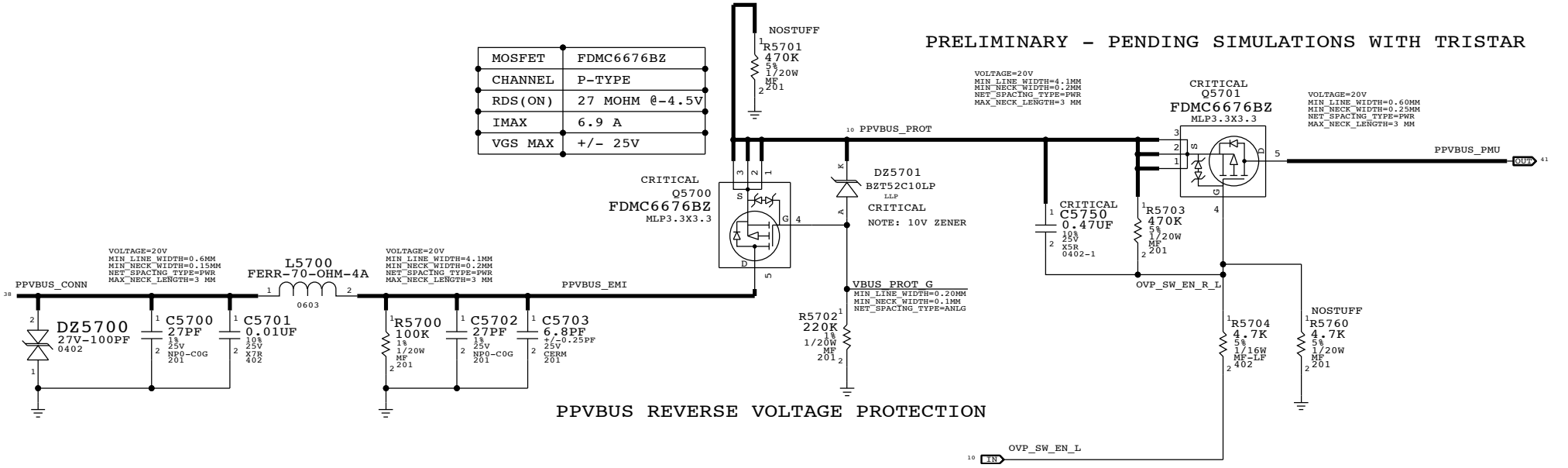
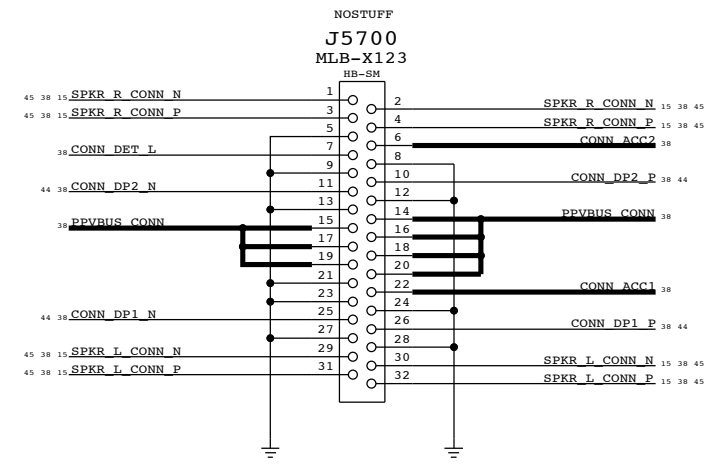
- 37 21 CLK32K\_AP 1 PP47001\_RF P4MM SM
- 37 21 WLAN\_REG\_ON 1 PP47002\_RF P4MM SM
- 37 21 WLAN\_HOST\_WAKE 1 PP47003\_RF P4MM SM
- 37 21 AP\_HSIC3\_RDY 1 PP47004\_RF P4MM SM
- 37 21 DEV\_HSIC3\_RDY 1 PP47005\_RF P4MM SM
- 37 21 WLAN\_UART\_RXD 1 PP47006\_RF P4MM SM
- 37 21 WLAN\_UART\_TXD 1 PP47007\_RF P4MM SM
- 37 21 GPIO\_6 1 PP47008\_RF P4MM SM
- 37 21 WLAN\_HSIC3\_RESUME 1 PP47009\_RF P4MM SM

R R47015  
C C47012  
L L1801  
U U47005  
J J47002

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PRELIMINARY - PENDING SIMULATIONS WITH TRISTAR

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V



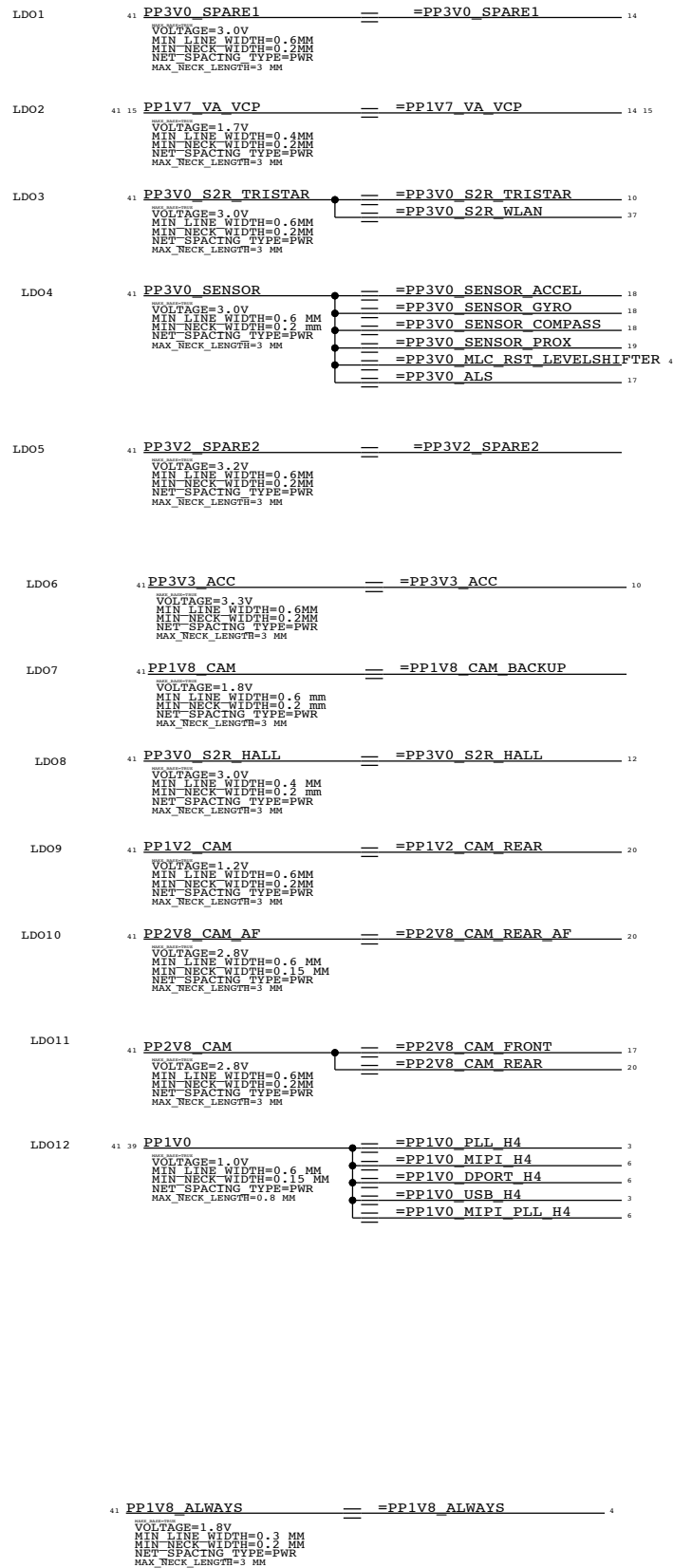
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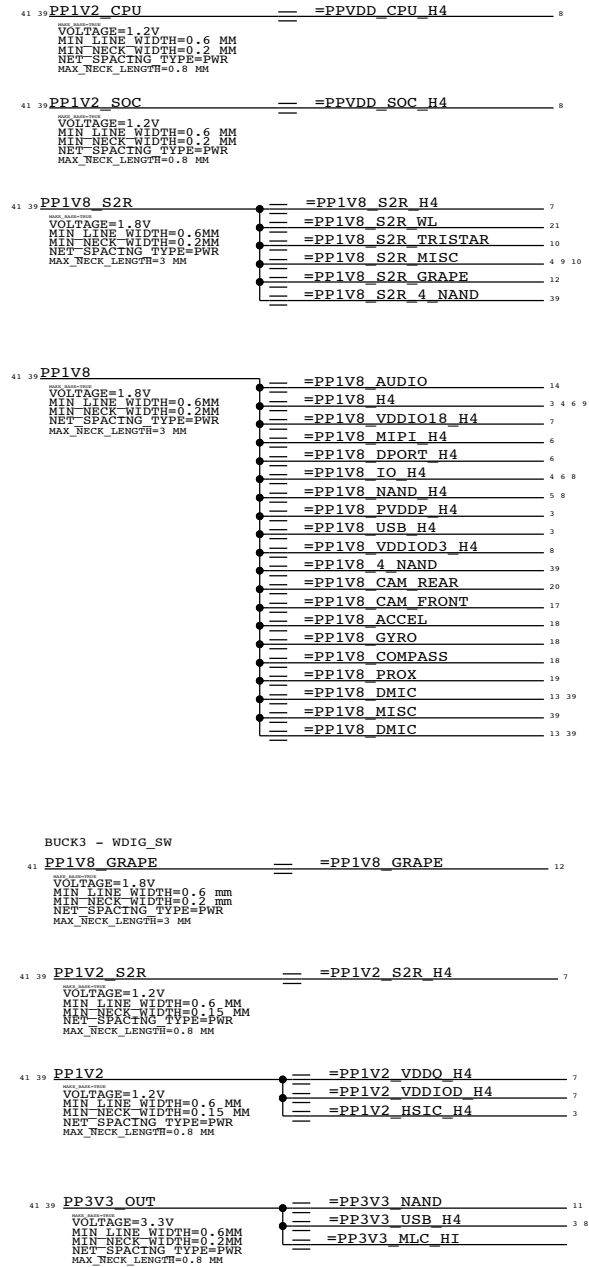
# POWER CONN / ALIAS

## LDO RAILS

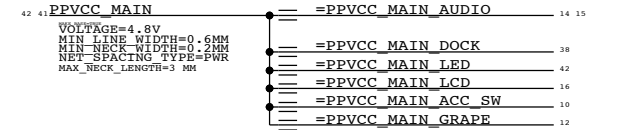
PROGRAMMABLE ON/OFF



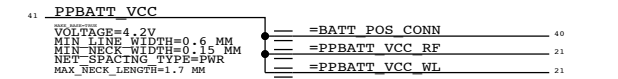
## BUCK RAILS



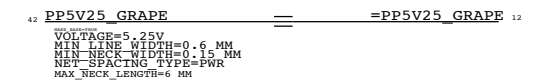
## CHARGER MAIN



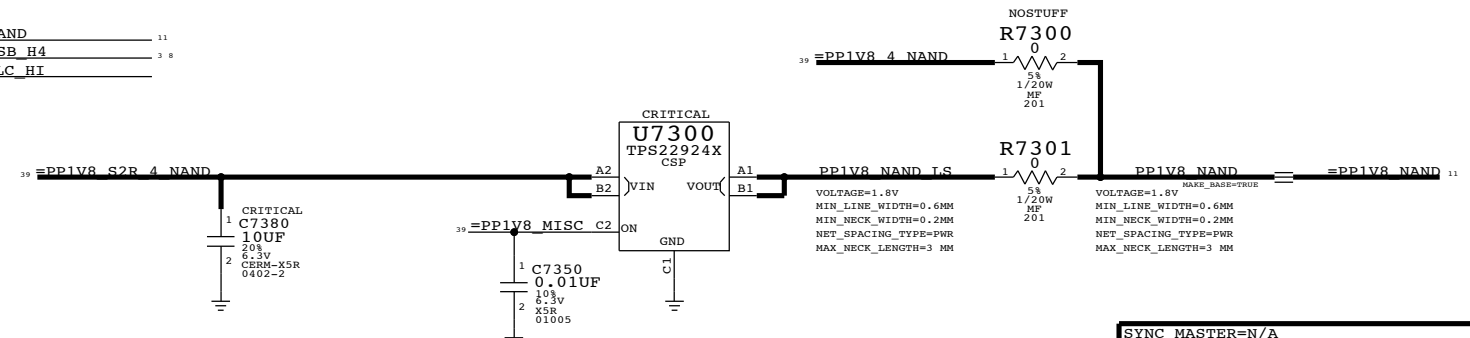
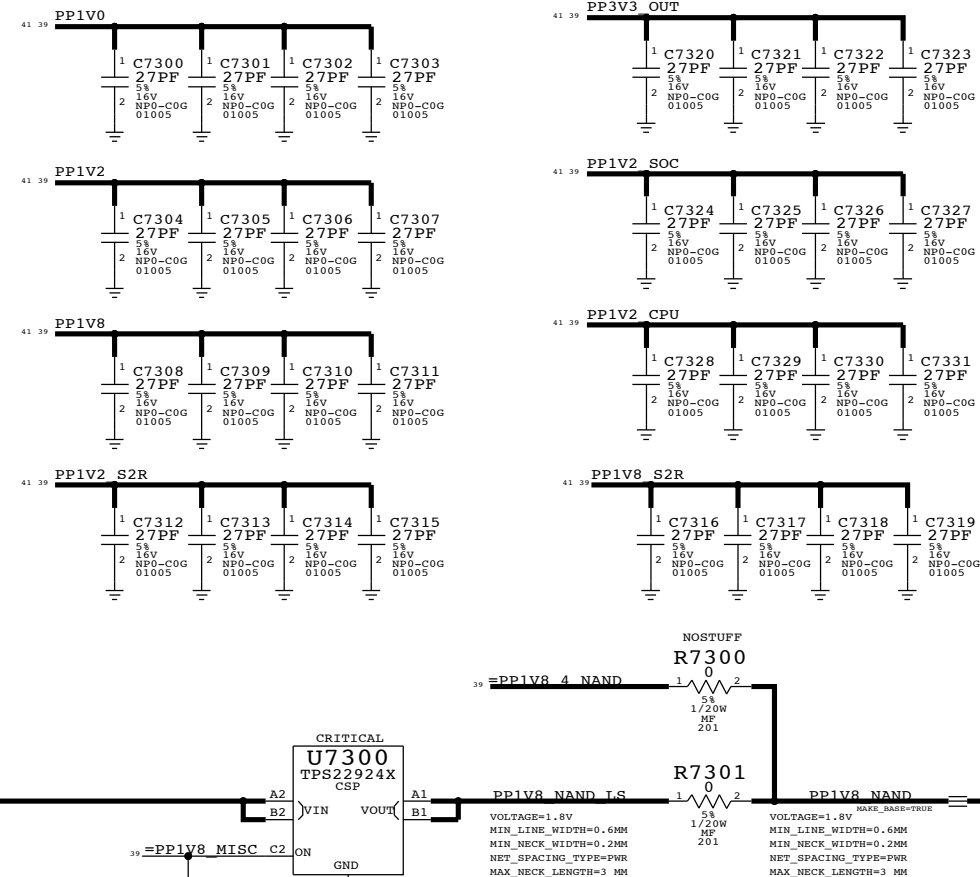
## BATTERY



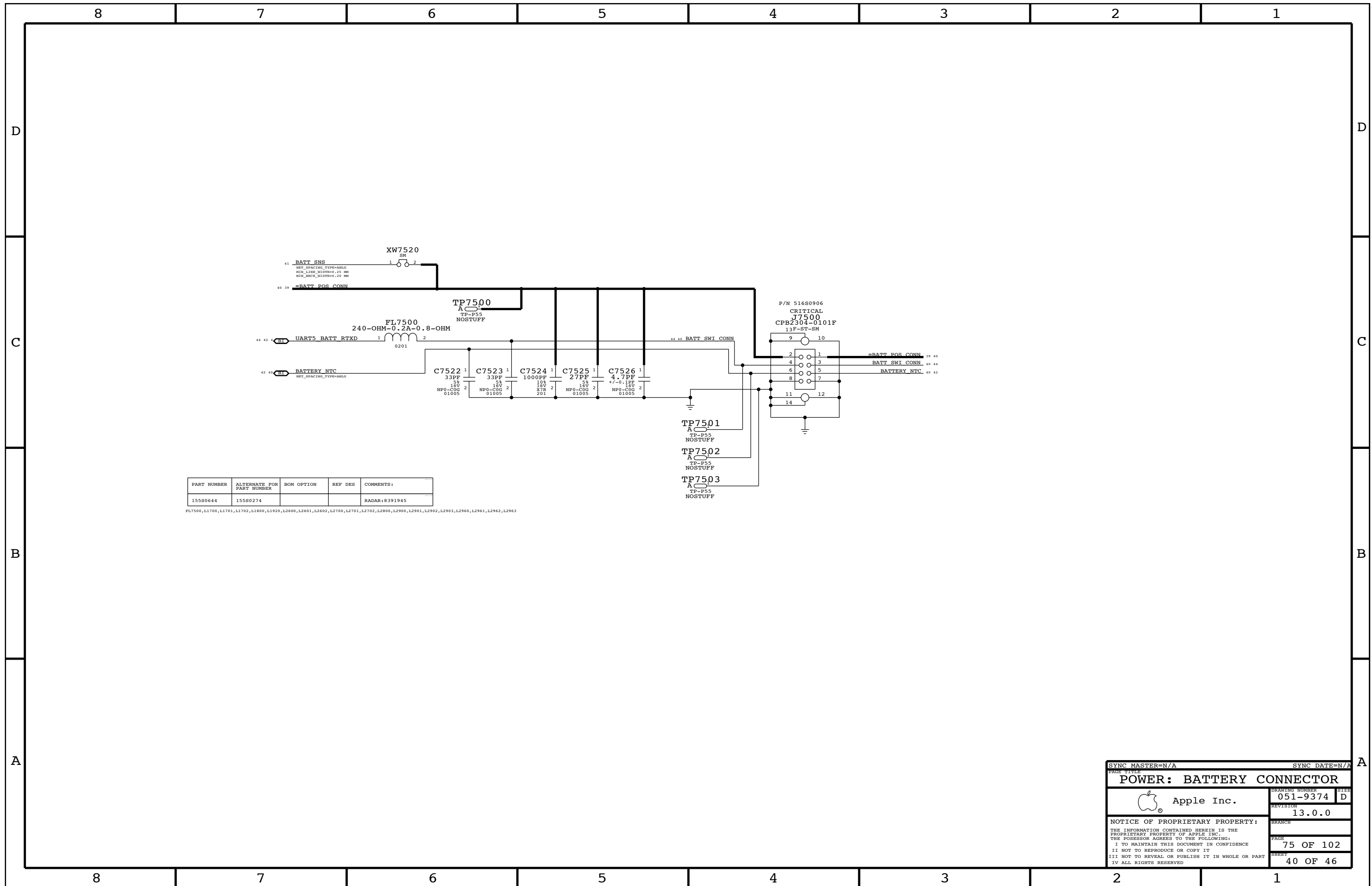
## BOOST->LDOS



## DESENSE CAPS



PAGE TITLE		SYNC DATE=N/A	
<b>Power: Aliases</b>			
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		39 OF 46	



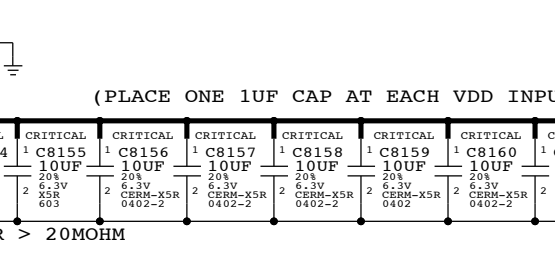
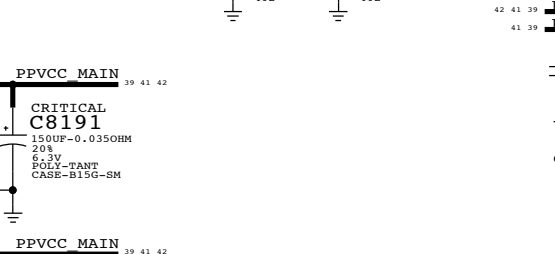
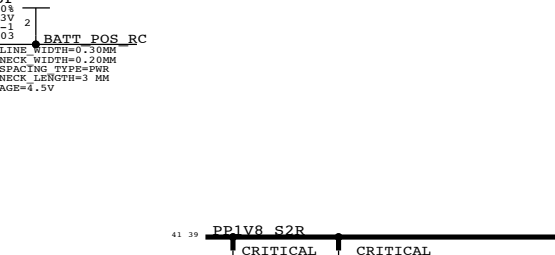
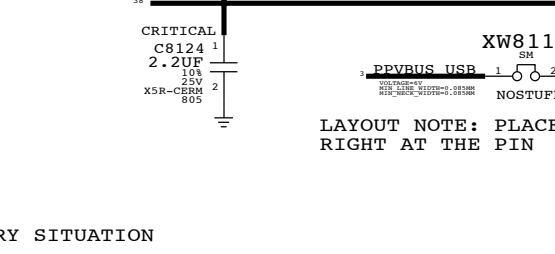
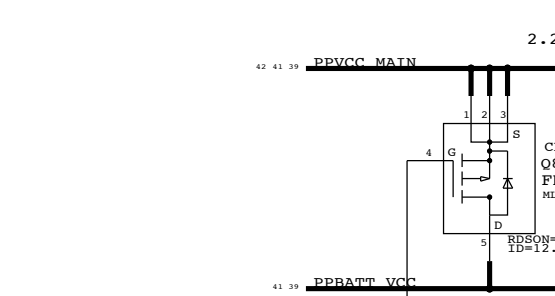
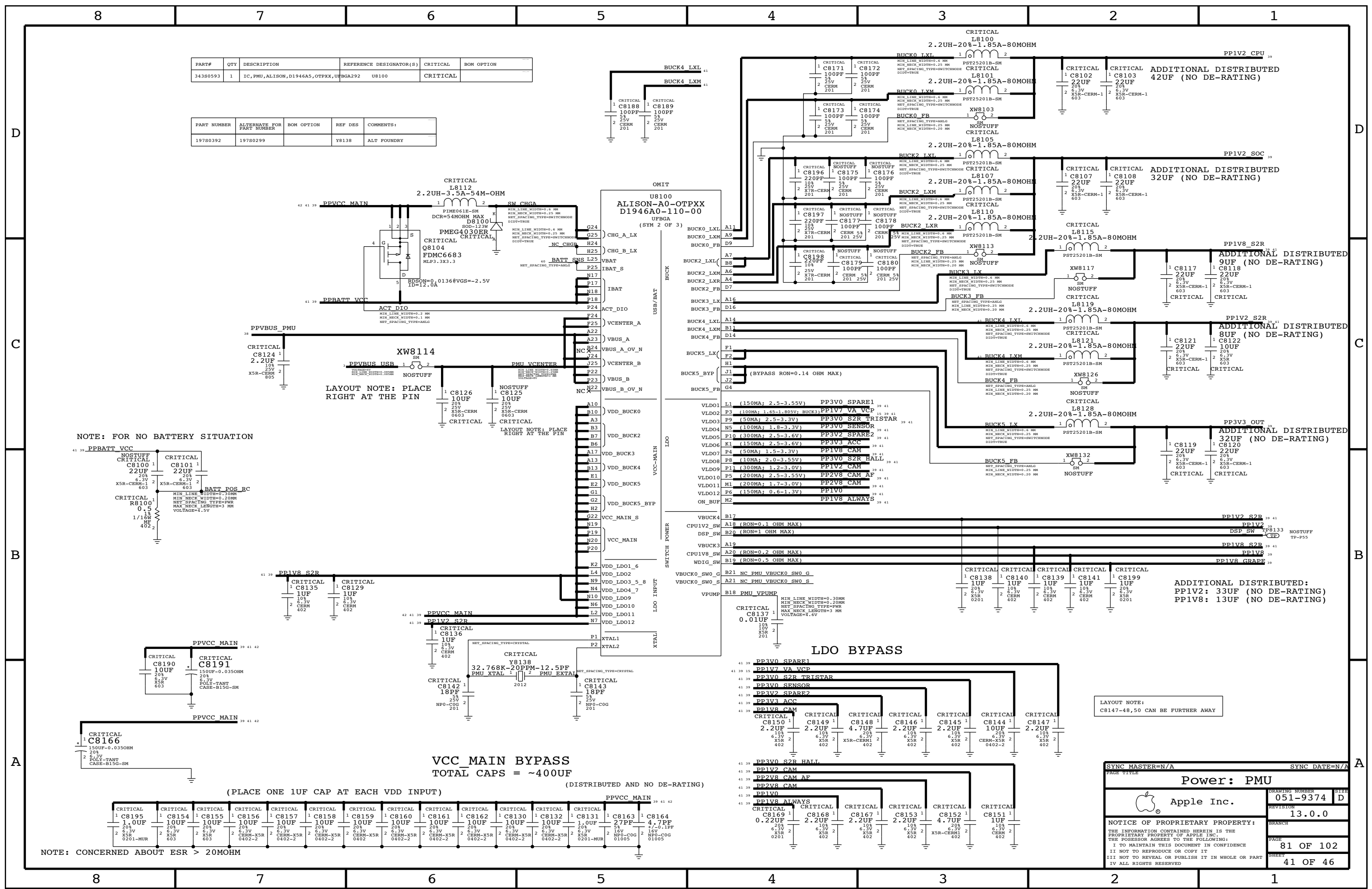
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
15580644	15580274			RADAR:8391945

FL7500, L1700, L1701, L1702, L1800, L1920, L2600, L2601, L2602, L2700, L2701, L2702, L2800, L2900, L2901, L2902, L2903, L2960, L2961, L2962, L2963

SYNC MASTER=N/A		SYNC DATE=N/A	
<b>POWER: BATTERY CONNECTOR</b>			
		DRAWING NUMBER	051-9374
		REVISION	13.0.0
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
34380593	1	IC, PMU, ALISON, D1946A5, OTPXX, UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
19780392	19780299		Y8138	ALT FOUNDRY

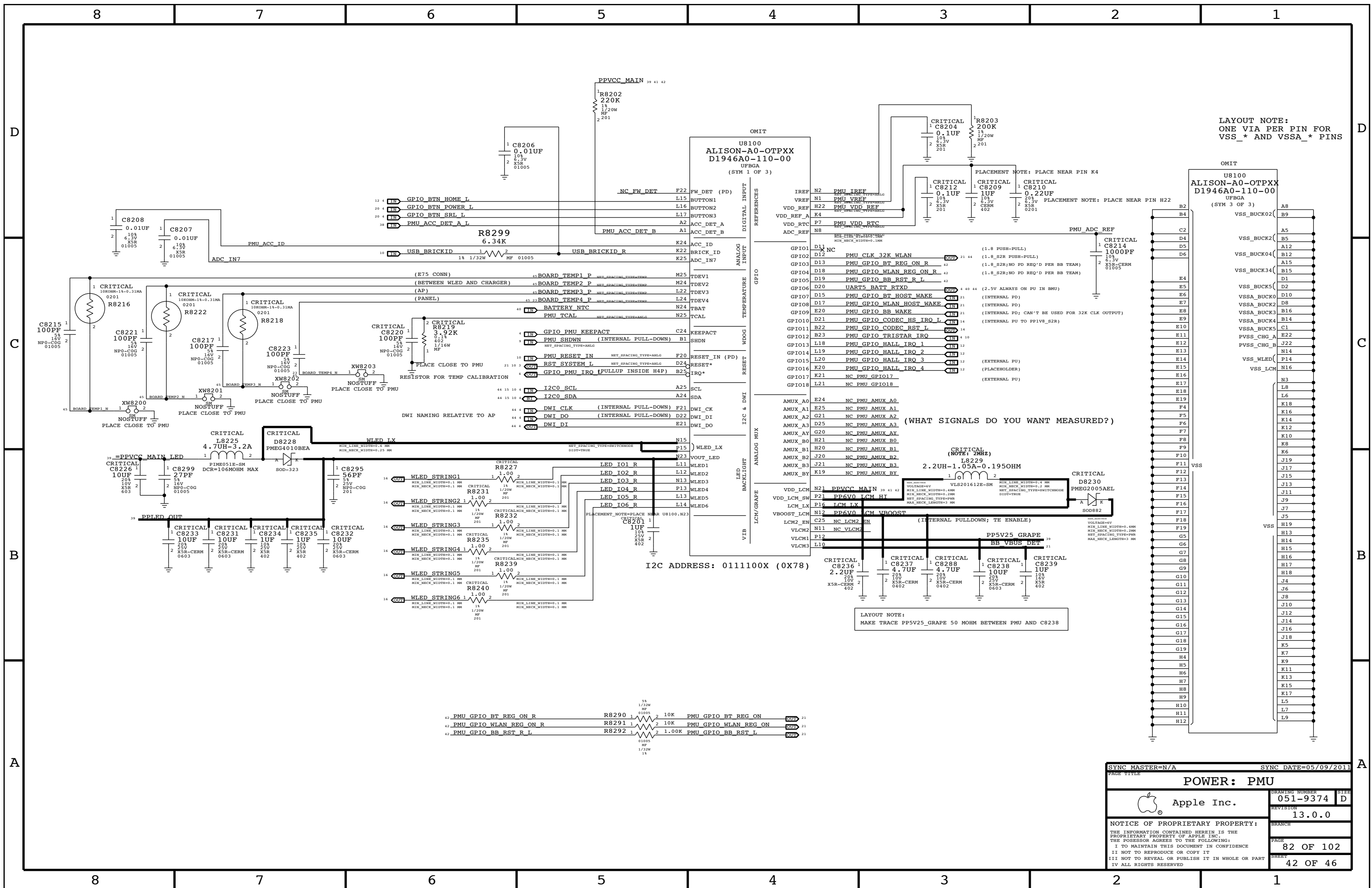


VCC\_MAIN BYPASS  
TOTAL CAPS = ~400UF  
(DISTRIBUTED AND NO DE-RATING)  
(PLACE ONE 1UF CAP AT EACH VDD INPUT)

LAYOUT NOTE:  
C8147-48,50 CAN BE FURTHER AWAY

PAGE TITLE		SYNC DATE=N/A	
<b>Power: PMU</b>			
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NOTE: CONCERNED ABOUT ESR > 20MOHM



LAYOUT NOTE:  
ONE VIA PER PIN FOR  
VSS\_\* AND VSSA\_\* PINS

(WHAT SIGNALS DO YOU WANT MEASURED?)

LAYOUT NOTE:  
MAKE TRACE PPSV25\_GRAPE 50 MOHM BETWEEN PMU AND C8238

I2C ADDRESS: 0111100X (0X78)

SYNC MASTER=N/A		SYNC DATE=05/09/2011	
<b>POWER: PMU</b>			
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# MECHANICAL PARTS

## PD PARTS

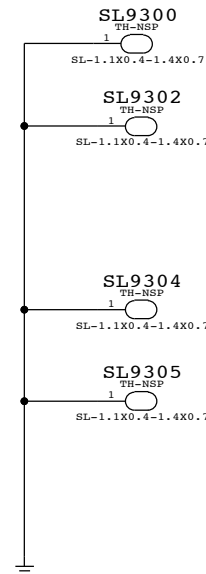
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-4017	1	FENCE,MAIN,MLB,YY	FENCE_MLB	
806-3782	1	CAN,MAIN,MLB,WIFI,YY	CAN_WIFI	
806-3715	1	FENCE,RADIO,MLB,SWAPPED,YY	CAN_RADIO	CELL

## TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)

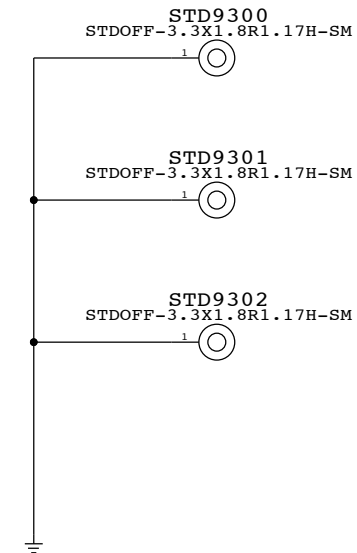
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	EEEE FOR 639-3251 (X123 ENTRY)	DNVV	CRITICAL	EEEE_X123_ENTRY
825-7639	1	EEEE FOR 639-4129 (X123A ENTRY)	F78H	CRITICAL	EEEE_X123A_ENTRY
825-7639	1	EEEE FOR 639-4130 (X123B ENTRY)	F78J	CRITICAL	EEEE_X123B_ENTRY
825-7639	1	EEEE FOR 639-3923 (X123 GOOD)	F3JV	CRITICAL	EEEE_X123_BETTER
825-7639	1	EEEE FOR 639-3924 (X123 BETTER)	F3JQ	CRITICAL	EEEE_X123_BEST
825-7639	1	EEEE FOR 639-3415 (X123A GOOD)	DY62	CRITICAL	EEEE_X123A_GOOD
825-7639	1	EEEE FOR 639-3925 (X123A BETTER)	F3JN	CRITICAL	EEEE_X123A_BETTER
825-7639	1	EEEE FOR 639-3926 (X123A BEST)	F3JP	CRITICAL	EEEE_X123A_BEST
825-7639	1	EEEE FOR 639-3416 (X123B GOOD)	DY63	CRITICAL	EEEE_X123B_GOOD
825-7639	1	EEEE FOR 639-3927 (X123B BETTER)	F3JR	CRITICAL	EEEE_X123B_BETTER
825-7639	1	EEEE FOR 639-3928 (X123B BEST)	F3JT	CRITICAL	EEEE_X123B_BEST


## PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM  
PLATING SIZE: 1.4MM X 0.7MM



## STANDOFFS: P/N 860-1542



PAGE TITLE		SYNC MASTER=N/A		SYNC DATE=N/A	
<b>MECHANICAL PARTS</b>					
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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R100	CLK_50S	CLK	AP_CLK_32K_CUMULUS 4 12
R101	CLK_50S	CLK	PMU_CLK_32K_WLAN 21 42
R102	CLK_50S	CLK	ISP0_CAM_REAR_CLK_R 4
R103	CLK_50S	CLK	ISP0_CAM_REAR_CLK 4 20
R104	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_R 4 17
R105	CLK_50S	CLK	ISP1_CAM_FRONT_CLK 4 17
R106	CLK_50S	CLK	ISP1_CAM_FRONT_CLK_F 17
R107	CLK_50S	CLK	I2S0_CODEC_ASP_MCK 4 14
R108	CLK_50S	CLK	I2S0_CODEC_ASP_MCK_R 4
R109	CLK_50S	CLK	I2S1_SPKAMP_MCK 4 15
R110	CLK_50S	CLK	I2S1_SPKAMP_MCK_R 4

JTAG

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
JTAG_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R111	JTAG_50S	JTAG	JTAG_SOC_TCK 3 10
R112	JTAG_50S	JTAG	JTAG_SOC_TMS 3 10
R113	JTAG_50S	JTAG	JTAG_SOC_TDI 3
R114	JTAG_50S	JTAG	JTAG_SOC_TDO 3 9
R115	JTAG_50S	JTAG	JTAG_SOC_TRST_L 3 9
R116	JTAG_50S	JTAG	BB_JTAG_TCK 4 21 24
R117	JTAG_50S	JTAG	BB_JTAG_TMS 4 21 24
R118	JTAG_50S	JTAG	BB_JTAG_TDI 4 21 24
R119	JTAG_50S	JTAG	BB_JTAG_TDO 4 21 24
R120	JTAG_50S	JTAG	BB_JTAG_TRST_L 4 21 24

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_45S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R121	I2S_45S	I2S	I2S0_CODEC_ASP_BCLK 4 14
R122	I2S_45S	I2S	I2S0_CODEC_ASP_LRCK 4 14
R123	I2S_45S	I2S	I2S0_CODEC_ASP_DOUT 4 14
R124	I2S_45S	I2S	I2S0_CODEC_ASP_DIN 4 14
R125	I2S_45S	I2S	I2S0_CODEC_ASP_SDOUT 14
R126	I2S_45S	I2S	I2S1_SPKAMP_BCLK 4 15
R127	I2S_45S	I2S	I2S1_SPKAMP_LRCK 4 15
R128	I2S_45S	I2S	I2S1_SPKAMP_DOUT 4 15
R129	I2S_45S	I2S	I2S1_SPKAMP_DIN 4 15
R130	I2S_45S	I2S	I2S2_CODEC_XSP_BCLK 4 14
R131	I2S_45S	I2S	I2S2_CODEC_XSP_LRCK 4 14
R132	I2S_45S	I2S	I2S2_CODEC_XSP_DOUT 4 14
R133	I2S_45S	I2S	I2S2_CODEC_XSP_DIN 4 14
R134	I2S_45S	I2S	I2S2_CODEC_XSP_SDOUT 14
R135	I2S_45S	I2S	I2S3_BT_BCLK 4 21
R136	I2S_45S	I2S	I2S3_BT_LRCK 4 21
R137	I2S_45S	I2S	I2S3_BT_DOUT 4 21
R138	I2S_45S	I2S	I2S3_BT_DIN 4 21

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R139	NAND_50S	NAND	FMIO_AD<7..0> 5 11
R140	NAND_50S	NAND	FMIO_CE0_L 5 11
R141	NAND_50S	NAND	FMIO_CLE 5 11
R142	NAND_50S	NAND	FMIO_ALE 5 11
R143	NAND_50S	NAND	FMIO_RE_N 5 11
R144	NAND_50S	NAND	FMIO_WE_L 5 11
R145	NAND_50S	NAND	FMIO_DOS_P 5 11
R146	NAND_50S	NAND	FMI1_AD<7..0> 5 11
R147	NAND_50S	NAND	FMI1_CE0_L 5 11
R148	NAND_50S	NAND	FMI1_CLE 5 11
R149	NAND_50S	NAND	FMI1_ALE 5 11
R150	NAND_50S	NAND	FMI1_RE_N 5 11
R151	NAND_50S	NAND	FMI1_WE_L 5 11
R152	NAND_50S	NAND	FMI1_DOS_P 5 11

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R153	I2C_50S	I2C	I2C0_SDA 4 10 15 42
R154	I2C_50S	I2C	I2C0_SCL 4 10 15 42
R155	I2C_50S	I2C	I2C1_SDA 4 18 19
R156	I2C_50S	I2C	I2C1_SCL 4 18 19
R157	I2C_50S	I2C	I2C2_SDA 4 17 18
R158	I2C_50S	I2C	I2C2_SCL 4 17 18
R159	I2C_50S	I2C	I2C2_SDA_F 17
R160	I2C_50S	I2C	I2C2_SCL_F 17
R161	I2C_50S	I2C	ISP0_CAM_REAR_SCL 6 20
R162	I2C_50S	I2C	ISP0_CAM_REAR_SDA 6 20
R163	I2C_50S	I2C	ISP1_CAM_FRONT_SCL 6 17
R164	I2C_50S	I2C	ISP1_CAM_FRONT_SDA 6 17
R165	I2C_50S	I2C	ISP1_CAM_FRONT_SCL_F 17
R166	I2C_50S	I2C	ISP1_CAM_FRONT_SDA_F 17
R167	I2C_50S	I2C	MLC_SDA_3V3
R168	I2C_50S	I2C	MLC_SCL_3V3
R169	I2C_50S	I2C	LVDS_DDC_DATA
R170	I2C_50S	I2C	LVDS_DDC_CLK

UART

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
UART_45S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
UART	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R171	UART_45S	UART	UART0_DEBUG_RXD 4 10
R172	UART_45S	UART	UART0_DEBUG_TXD 4 10
R173	UART_45S	UART	UART1_BT_RXD 4 21
R174	UART_45S	UART	UART1_BT_TXD 4 21
R175	UART_45S	UART	UART1_BT_RTS_L 4 21
R176	UART_45S	UART	UART1_BT_CTS_L 4 21
R177	UART_45S	UART	UART2_ACC_RXD 4 10
R178	UART_45S	UART	UART2_ACC_TXD 4 10
R179	UART_45S	UART	UART3_WLAN_RXD 4 21
R180	UART_45S	UART	UART3_WLAN_TXD 4 21
R181	UART_45S	UART	UART4_BB_RXD 4 10 21
R182	UART_45S	UART	UART4_BB_TXD 4 10 21
R183	UART_45S	UART	UART4_BB_RTS_L 4 21
R184	UART_45S	UART	UART4_BB_CTS_L 4 21
R185	UART_45S	UART	UART5_BATT_RTXD 4 40 42
R186	UART_45S	UART	BATT_SWI_CONN 40

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R187	USB_90D	USB	SOC_USB_D_P 3 10
R188	USB_90D	USB	SOC_USB_D_N 3 10
R189	USB_90D	USB	USB_BB_D_P 10 21
R190	USB_90D	USB	USB_BB_D_N 10 21
R191	USB_90D	USB	TS_E75_DPAIR1_P 10 38
R192	USB_90D	USB	TS_E75_DPAIR1_N 10 38
R193	USB_90D	USB	TS_E75_DPAIR2_P 10 38
R194	USB_90D	USB	TS_E75_DPAIR2_N 10 38
R195	USB_90D	USB	CONN_DP1_P 38
R196	USB_90D	USB	CONN_DP1_N 38
R197	USB_90D	USB	CONN_DP2_P 38
R198	USB_90D	USB	CONN_DP2_N 38

VREF

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
VREF	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R199	VREF	VREF	PPVREF_DDR0_CA 7
R200	VREF	VREF	PPVREF_DDR0_DO 7
R201	VREF	VREF	PPVREF_DDR1_CA 7
R202	VREF	VREF	PPVREF_DDR1_DO 7

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_45S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R203	SPI_45S	SPT	SPI1_GRAPE_MISO 4 12
R204	SPI_45S	SPT	SPI1_GRAPE_MOSI 4 12
R205	SPI_45S	SPT	SPI1_GRAPE_SCLK 4 12
R206	SPI_45S	SPT	SPI1_GRAPE_SCLK_R 12
R207	SPI_45S	SPT	SPI1_GRAPE_CS_L 4 12
R208	SPI_45S	SPT	SPI2_CODEC_MISO 4 14
R209	SPI_45S	SPT	SPI2_CODEC_MOSI 4 14
R210	SPI_45S	SPT	SPI2_CODEC_SCLK 4 14
R211	SPI_45S	SPT	SPI2_CODEC_CS_L 4 14

HSIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HSIC_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HSIC	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R212	HSIC_50S	HSIC	HSIC1_BB_STB 3 21
R213	HSIC_50S	HSIC	HSIC1_BB_DATA 3 21
R214	HSIC_50S	HSIC	HSIC2_WLAN_STB 3 21
R215	HSIC_50S	HSIC	HSIC2_WLAN_DATA 3 21

DWI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DWI_45S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	NET_TYPE
R216	DWI_45S	DWI	DWI_CLK 4 42
R217	DWI_45S	DWI	DWI_DI 4 42
R218	DWI_45S	DWI	DWI_DO 4 42

SYNC MASTER=N/A SYNC DATE=N/A

**CONSTRAINTS: ASSIGNMENTS**

Apple Inc.

DRAWING NUMBER: 051-9374 SIZE: D

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MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	NET_TYPE	VALUE
	PHYSICAL	SPACING			
E121	MIPI_90D	MIPI		MIPIOD_DATA_P<0>	6 16
E122	MIPI_90D	MIPI		MIPIOD_DATA_N<0>	6 16
E123	MIPI_90D	MIPI		MIPIOD_DATA_P<1>	6 16
E124	MIPI_90D	MIPI		MIPIOD_DATA_N<1>	6 16
E125	MIPI_90D	MIPI		MIPIOD_DATA_P<2>	6 16
E126	MIPI_90D	MIPI		MIPIOD_DATA_N<2>	6 16
E127	MIPI_90D	MIPI		MIPIOD_DATA_P<3>	6 16
E128	MIPI_90D	MIPI		MIPIOD_DATA_N<3>	6 16
E129	MIPI_90D	MIPI		MIPIOD_CLK_P	6 16
E130	MIPI_90D	MIPI		MIPIOD_CLK_N	6 16
E131	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_P<0>	6 20
E132	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_N<0>	6 20
E133	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_P<1>	6 20
E134	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_N<1>	6 20
E135	MIPI_90D	MIPI		MIPIOC_CAM_REAR_CLK_P	6 20
E136	MIPI_90D	MIPI		MIPIOC_CAM_REAR_CLK_N	6 20
E137	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_FILT_P<0>	6 20
E138	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_FILT_N<0>	6 20
E139	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_FILT_P<1>	6 20
E140	MIPI_90D	MIPI		MIPIOC_CAM_REAR_DATA_FILT_N<1>	6 20
E141	MIPI_90D	MIPI		MIPIOC_CAM_REAR_CLK_FILT_P	6 20
E142	MIPI_90D	MIPI		MIPIOC_CAM_REAR_CLK_FILT_N	6 20
E143	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_DATA_P<0>	6 17
E144	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_DATA_N<0>	6 17
E145	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_CLK_P	6 17
E146	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_CLK_N	6 17
E147	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_DATA_FILT_P<0>	6 17
E148	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_DATA_FILT_N<0>	6 17
E149	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_CLK_FILT_P	6 17
E150	MIPI_90D	MIPI		MIPI1C_CAM_FRONT_CLK_FILT_N	6 17

DMIC

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DMIC_45S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMIC	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	NET_TYPE	VALUE
	PHYSICAL	SPACING			
E151	DMIC_45S	DMIC		L81 DMIC1_FF_SCLK	14
E152	DMIC_45S	DMIC		L81 DMIC1_FF_SD	14
E153	DMIC_45S	DMIC		DMIC1_FF_SCLK	13 14
E154	DMIC_45S	DMIC		DMIC1_FF_SD	13 14
E155	DMIC_45S	DMIC		DMIC1_FF_SCLK_CONN	13

AUDIO

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	NET_TYPE	VALUE
	PHYSICAL	SPACING			
E156	USB_90D	USB		MIKEY_TS_P	10 14
E157	USB_90D	USB		MIKEY_TS_N	10 14
E158	USB_90D	USB		L81_MBUS_P	14
E159	USB_90D	USB		L81_MBUS_N	14
E160	SPEAKER	AUDIO		SPKR_L_CONN_P	15 38
E161	SPEAKER	AUDIO		SPKR_L_CONN_N	15 38
E162	SPEAKER	AUDIO		SPKR_R_CONN_P	15 38
E163	SPEAKER	AUDIO		SPKR_R_CONN_N	15 38
E164	AUDIO_DIFF	AUDIO		HP_MIC_P	14
E165	AUDIO_DIFF	AUDIO		HP_MIC_N	14
E166	AUDIO_DIFF	AUDIO		L81_AIN2_P	14
E167	AUDIO_DIFF	AUDIO		L81_AIN2_N	14

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	NET_TYPE	VALUE
	PHYSICAL	SPACING			
E168	LVDS_90D	LVDS		MIPI_DATA_CONN_P<3..0>	16
E169	LVDS_90D	LVDS		MIPI_DATA_CONN_N<3..0>	16
E170	LVDS_90D	LVDS		MIPI_CLK_CONN_P	16
E171	LVDS_90D	LVDS		MIPI_CLK_CONN_N	16

TEMP SENSORS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
TEMP	*	TEMP_SENSE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TEMP	*	*	3:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	NET_TYPE	VALUE
	PHYSICAL	SPACING			
E172	TEMP	TEMP		BOARD_TEMP1_P	42
E173	TEMP	TEMP		BOARD_TEMP1_N	42
E174	TEMP	TEMP		BOARD_TEMP2_P	42
E175	TEMP	TEMP		BOARD_TEMP2_N	42
E176	TEMP	TEMP		BOARD_TEMP3_P	42
E177	TEMP	TEMP		BOARD_TEMP3_N	42
E178	TEMP	TEMP		BOARD_TEMP4_P	23 42
E179	TEMP	TEMP		BOARD_TEMP4_N	23 42

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE		SPACING	NET_TYPE	VALUE
	PHYSICAL	SPACING			
E180	CRYSTAL	CRYSTAL		XTAL_SOC_24M_I	3
E181	CRYSTAL	CRYSTAL		XTAL_SOC_24M_O	3
E182	CRYSTAL	CRYSTAL		XTAL_SOC_24M_O_R	3

SYNC MASTER=N/A SYNC DATE=N/A

**CONSTRAINTS: ASSIGNMENTS**

Apple Inc.

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# MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL OR MM)	ALLEGRO VERSION
TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, BOTTOM	NO_TYPE, BGA	MM	16.2

## PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

## SINGLE-ENDED PHYSICAL RULES

### 45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2, ISL9	Y	0.053 MM	0.053 MM	3.0 MM		
45_OHM_SE	ISL4, ISL6	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	*	N	0.055 MM	0.055 MM	3.0 MM		

### 50 OHMS - CLEAR ON LAYER 2 AND 9

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP, BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.085 MM	0.085 MM	3.0 MM		

## DIFFERENTIAL PAIR PHYSICAL RULES

### 90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP	Y	0.089 MM	0.089 MM		0.150 MM	0.150 MM
90_OHM_DIFF	ISL2, ISL9	Y	0.051 MM	0.051 MM	=STANDARD	0.120 MM	0.120 MM
90_OHM_DIFF	ISL4, ISL6	Y	0.052 MM	0.052 MM	=STANDARD	0.120 MM	0.120 MM
90_OHM_DIFF	*	N	0.089 MM	0.089 MM	=STANDARD	0.150 MM	0.150 MM

## SPACING CONSTRAINTS

### DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	0.055 MM	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

### REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.055 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.0825 MM	?
2:1_SPACING	*	0.11 MM	?
2.5:1_SPACING	*	0.137 MM	?
3:1_SPACING	*	0.165 MM	?
4:1_SPACING	*	0.22 MM	?
5:1_SPACING	*	0.275 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

\*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

### POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	
GND_P1SPACING	*	0.1 MM	
SWITCHNODE	*	0.2 MM	

### NOTES:

- 0.075 MM ~ 3 MIL
- 0.089 MM ~ 3.5 MIL
- 0.102 MM ~ 4 MIL
- 0.114 MM ~ 4.5 MIL
- 0.125 MM ~ 5 MIL
- 0.140 MM ~ 5.5 MIL
- 0.15 MM ~ 6 MIL
- 0.18 MM ~ 7 MIL
- 0.2 MM ~ 8 MIL
- 0.25 MM ~ 10 MIL
- 0.3 MM ~ 12 MIL
- 0.33 MM ~ 13 MIL
- 0.4 MM ~ 16 MIL
- 1.0 MM = 39.37 MIL

## AUDIO/MISC PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.5 MM	0.20MM	10 MM	0.10 MM	0.10 MM
AUDIO_DIFF	*	Y	0.1 MM	0.10MM	10 MM	0.10 MM	0.10 MM
TEMP_SENSE	*	Y	0.1 MM	0.10MM	10 MM	0.08 MM	0.08 MM

## BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.055 MM	0.055 MM	=STANDARD	0.076 MM	0.075 MM

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