1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

K94 CHOPIN MLB

PVT

REV. A

LAST_MODIFIED=Mon Jan 10 13:11:06 2011

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
A	0001052699	PRODUCTION RELEASED	2011-01-10

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	TABLE OF CONTENTS	MIKE	N/A
2	2	BLOCK DIAGRAM: SYSTEM	MIKE	N/A
3	5	BOM TABLE	MIKE	N/A
4	6	AP: MAIN	JAMES	N/A
5	7	AP: I/Os	JAMES	N/A
6	8	AP: NAND	JAMES	N/A
7	9	AP: TV,DP,MIPI	JAMES	N/A
8	10	AP: PWR	JAMES	N/A
9	11	AP: PWR	JAMES	N/A
10	12	AP: MISC & ALIASES	JAMES	N/A
11	13	AP: VIDEO BUFFER,BB USB MUXES	JAMES	N/A
12	14	NAND	JONATHAN	N/A
13	17	VIDEO: DISPLAY PORT	JAMES	N/A
14	20	VIDEO: MLC	MIKE	N/A
15	21	VIDEO: MLC ALIASES	MIKE	N/A
16	22	VIDEO: LVDS CONNECTOR	ALEX	N/A
17	30	GRAPE: GROUNDHOG,CONN,BOOST	RAMSIN	N/A
18	31	GRAPE: Z1, Z2	RAMSIN	N/A
19	36	AUDIO: L63 CODEC	LENG	N/A
20	37	AUDIO: SPEAKER AMP	LENG	N/A
21	38	AUDIO: HEADPHONE OUT	LENG	N/A
22	39	AUDIO: BLANK	LENG	N/A
23	42	AUDIO: DETECT/MIC BIAS	LENG	N/A
24	43	AUDIO: HP/MIC FILTERS	LENG	N/A
25	54	CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES	MARK B.	N/A
26	55	CONNECTOR: CANADA FLEX FILTERS	MARK B.	N/A
27	56	CONNECTOR: SENSOR PANEL CONNECTOR	MARK B.	N/A
28	57	IO FLEX: DOCK COMPONENTS	JAMES	N/A
29	59	IO FELX: B2B Connector	JAMES	N/A
30	60	CONNECTOR: X23 WIFI/BT	MIKE	N/A
31	61	CONNECTOR: X24 CELLULAR/GPS	MIKE	N/A

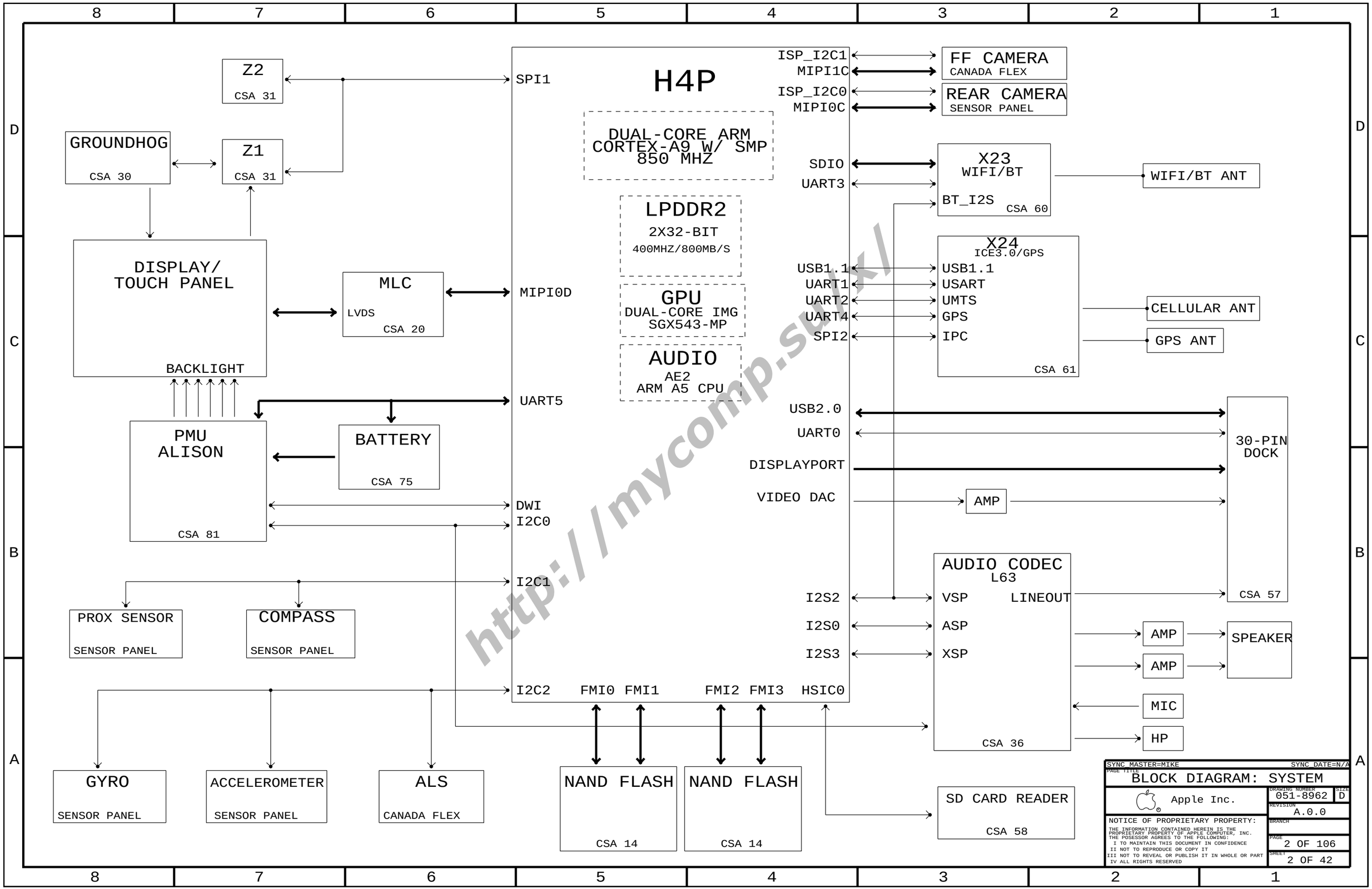
PDF	CSA	CONTENTS	SYNC MASTER	DATE
32	73	POWER: ALIASES	YOSH	N/A
33	75	POWER: BATTERY CONNECTOR	YOSH	N/A
34	81	POWER: PMU	YOSH	N/A
35	82	POWER: PMU	YOSH	N/A
36	83	POWER: 3.3V VR	YOSH	N/A
37	90	DEBUG AND MISC	MIKE	N/A
38	93	FCT/ICT TEST/BRACKETS	MIKE	N/A
39	100	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A
40	101	CONSTRAINTS: ASSIGNMENTS	MIKE	N/A
41	102	CONSTRAINTS: MLB RULES	MIKE	N/A
42	106	CONSTRAINTS: RF RULES	MIKE	N/A

DRAWING
TITLE=BACH
ABBREV=DRAWING

DRAWING TITLE: CHOPIN MLB

Apple Inc.

DRAWING NUMBER: 051-8962 | SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 1 OF 106
SHEET: 1 OF 42



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
BLOCK DIAGRAM: SYSTEM

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
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Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:

ALL AVAIL BOM OPTIONS

COMMON
ALTERNATE

16GB_PROD
32GB_PROD
64GB_PROD

BKLT_PLL

DEVELOPMENT_JTAG
DEVELOPMENT_JTAG_TAP
JTAG_VAR
JTAG_TAP_NOT

SPEAKER
INTERNAL_MIC

PORTRAIT_DOCK

MLC_DEV
MLC_PROD

K93
K94

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE

ADD DEVELOPMENT AND OTHER BOMS ONCE YOU GET BOM NUMBERS

BOM OPTIONS

PROGRAMMABLE PARTS

SCH AND BOARD P/N

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-8962	1	SCH,CHOPIN_AUDIO,MLB,K94	SCH1	
820-3069	1	PCBF,CHOPIN_AUDIO,MLB,K94	PCB1	

PD PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
806-1396	1	FENCE,GRAPE,MLB,K93/K94	FENCE1	
806-1397	1	CAN,GRAPE,MLB,K93/K94	CAN1	NOSTUFF
806-1398	1	FENCE,CPU,MLB,K93/K94	FENCE2	
806-1399	1	CAN,CPU,MLB,K93/K94	CAN2	NOSTUFF
806-1400	1	FENCE,NAND,MLB,K93/K94	FENCE3	
806-1401	1	CAN,NAND,MLB,K93/K94	CAN3	NOSTUFF

TOP BARCODE LABEL/EEE CODES (ONLY ONE IS USED PER BOM)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7651	1	EEEE FOR 639-1180 (K93 16G)	DH36	CRITICAL	EEEE_K93_16G
825-7651	1	EEEE FOR 639-1426 (K93 32G)	DH37	CRITICAL	EEEE_K93_32G
825-7651	1	EEEE FOR 639-1428 (K93 64G)	DG99	CRITICAL	EEEE_K93_64G
825-7651	1	EEEE FOR 639-1112 (K94 16G)	DFC4	CRITICAL	EEEE_K94_16G
825-7651	1	EEEE FOR 639-1181 (K94 32G)	DFC5	CRITICAL	EEEE_K94_32G
825-7651	1	EEEE FOR 639-1182 (K94 64G)	DFC6	CRITICAL	EEEE_K94_64G
825-7651	1	EEEE FOR 639-1430 (K95 16G)	DH3C	CRITICAL	EEEE_K95_16G
825-7651	1	EEEE FOR 639-1427 (K95 32G)	DH3D	CRITICAL	EEEE_K95_32G
825-7651	1	EEEE FOR 639-1429 (K95 64G)	DG9C	CRITICAL	EEEE_K95_64G

BOTTOM LABEL TYPE 1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7639	1	631- B/C LABEL	LBL1	CRITICAL	
825-7639	1	639- B/C LABEL	LBL2	CRITICAL	

BOTTOM LABEL TYPE 2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
825-7640	1	MATRIX LABEL	LBL3	CRITICAL	
825-7640	1	631- MATRIX LABEL	LBL4	CRITICAL	

SYNC MASTER=MIKE SYNC DATE=N/A

PAGE TITLE
BOM TABLE

Apple Inc.

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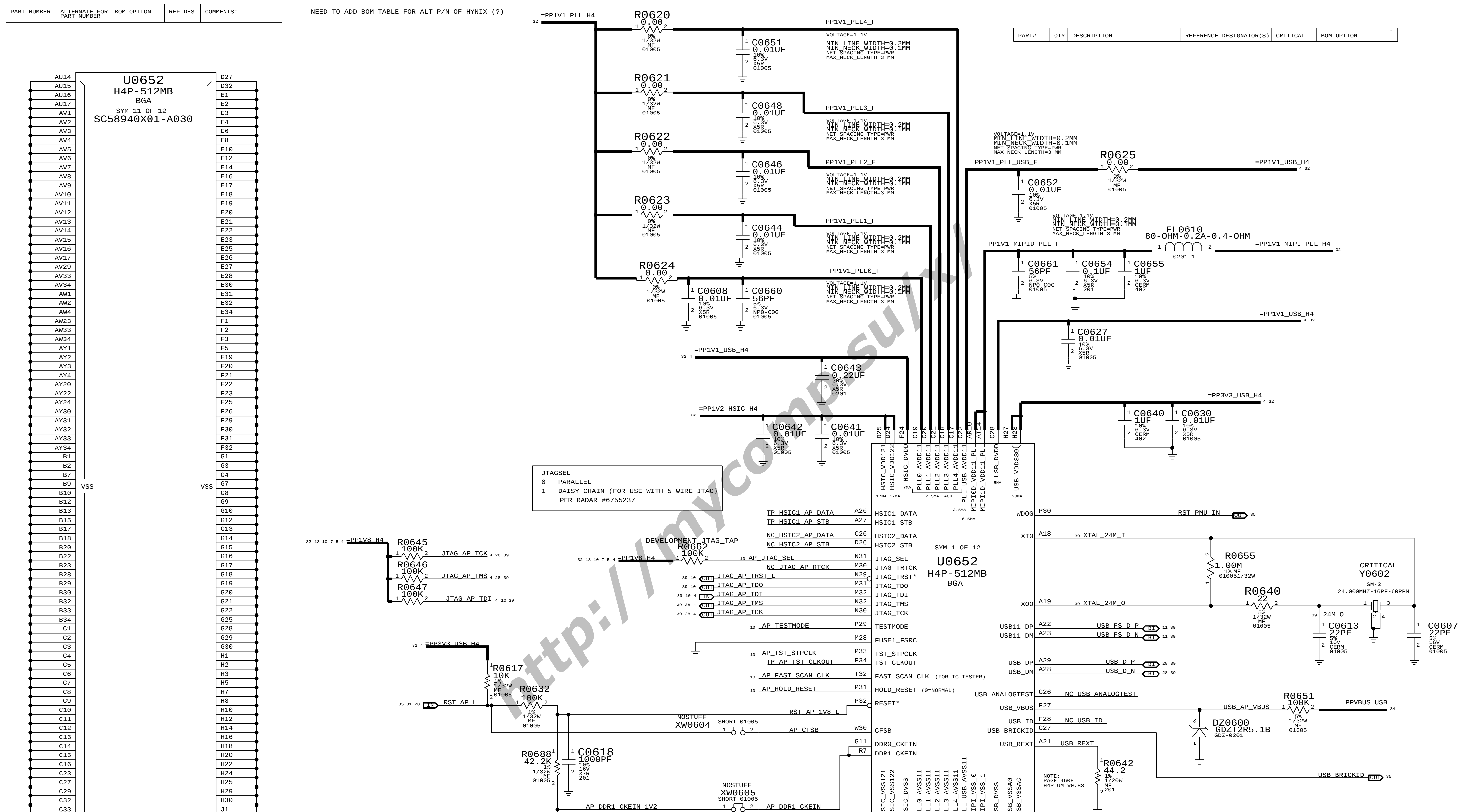


SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

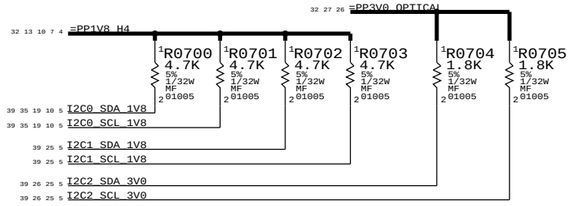
AP: MAIN

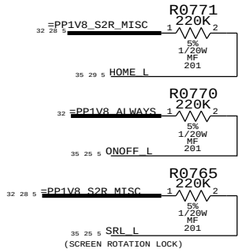
Apple Inc.

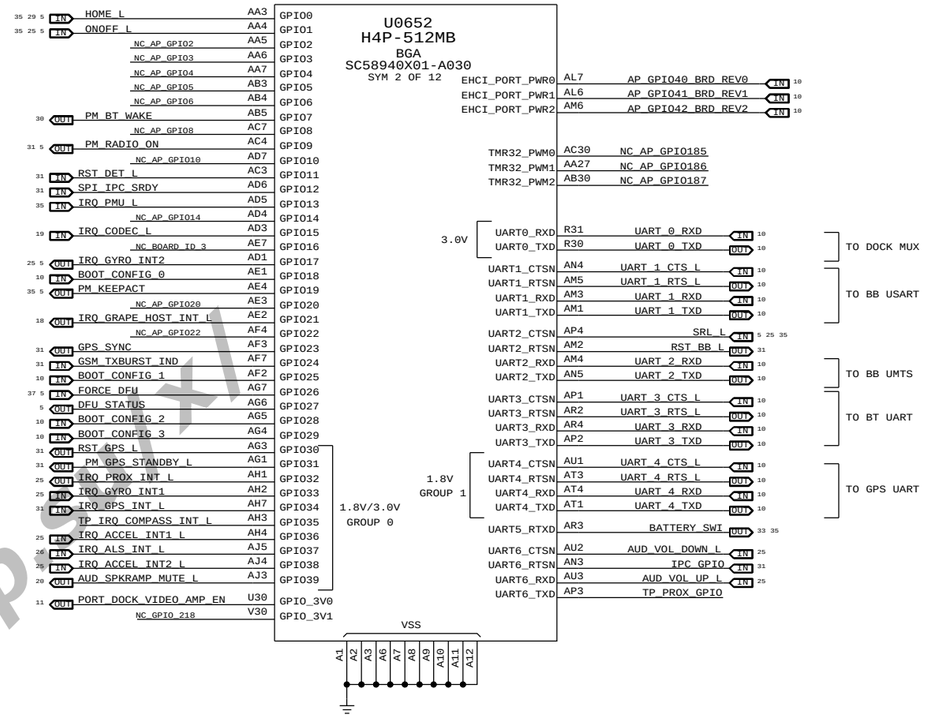
DRAWING NUMBER 051-8962 SIZE D

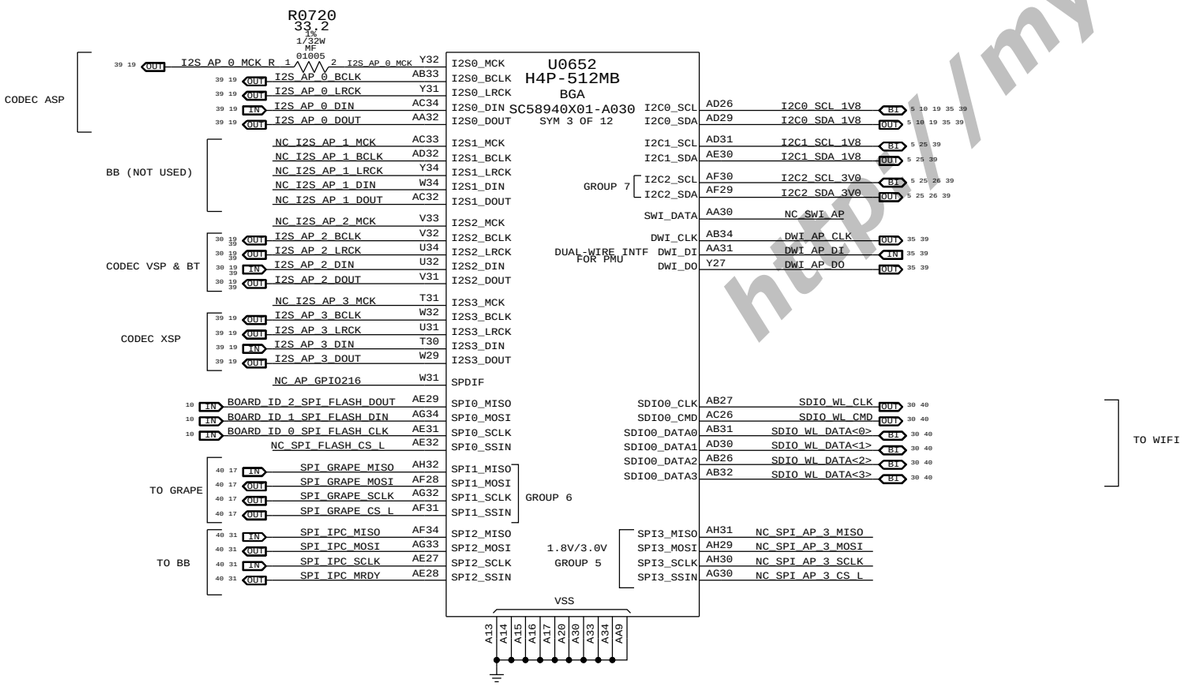
REVISION A.0.0

BRANCH









SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE: AP: I/Os

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

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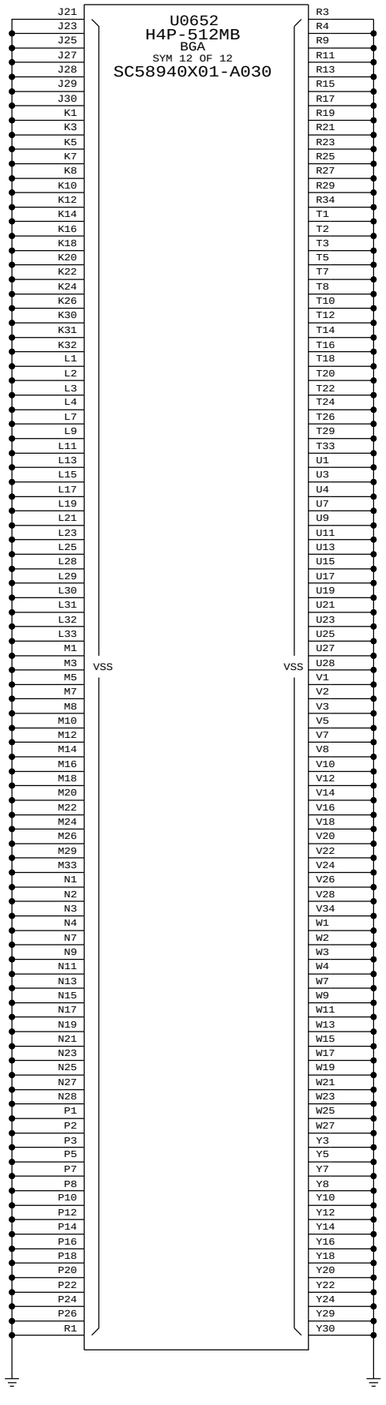

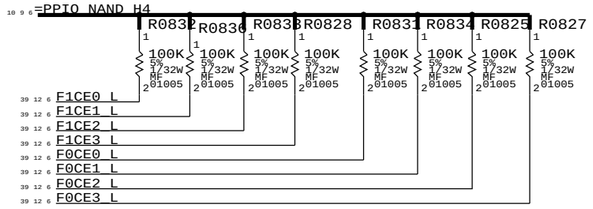

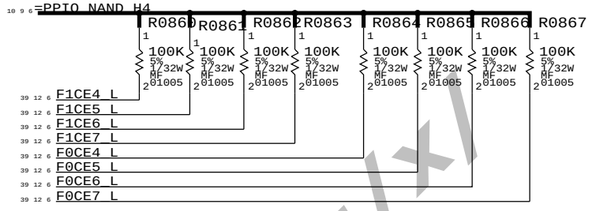

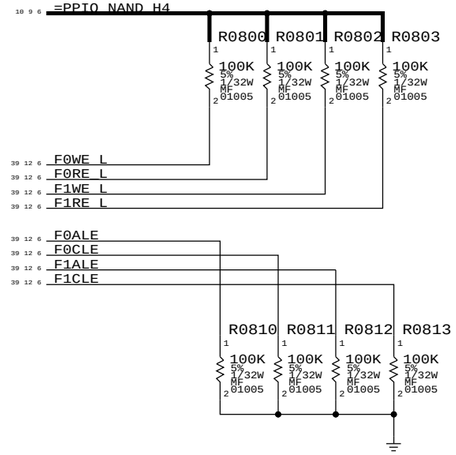

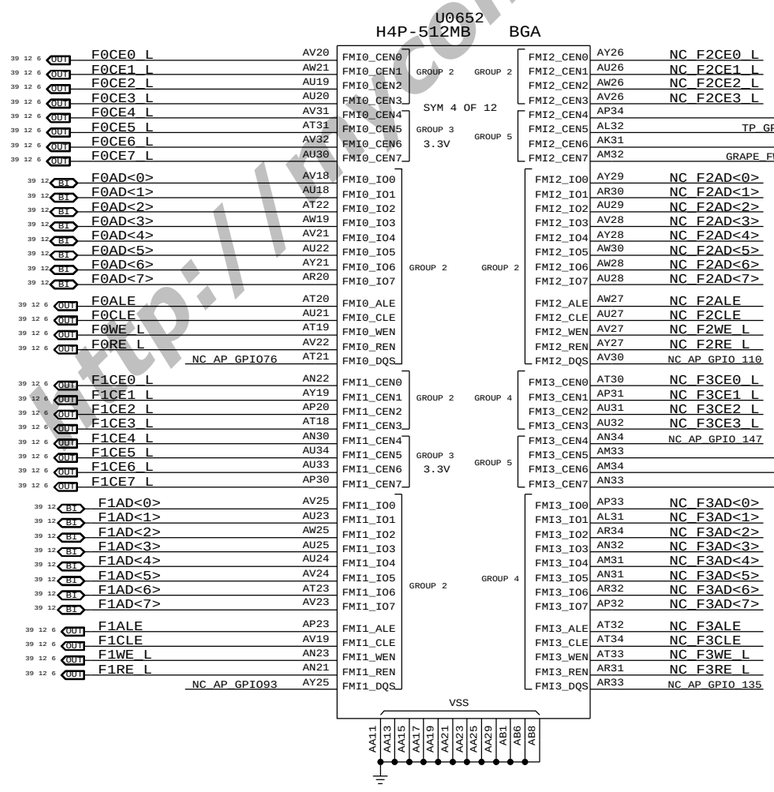

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
AP: NAND

Apple Inc.

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=PP3V0_IO_H4
C0954 0.01UF 10% 6.3V X6S 01005
MIN_NECK_MIDTH SHOULD BE 0.2MM
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
PP_AP_DP_AVDD_AUX
C0927 0.22UF 20% 6.3V X5R 402
C0926 0.22UF 20% 6.3V X5R 402
C0925 0.22UF 20% 6.3V X5R 402
C0924 56PF 5% 6.3V NP0-C0G 01005
R0910 0 5% 1/20W MF 201
=PP1V8_DPORT_H4
C0923 56PF 5% 6.3V NP0-C0G 01005
=PP3V0_VIDEO_H4
C0951 1UF 10% 6.3V CERM 402
C0952 0.01UF 10% 6.3V X5R 01005
PP_DP_PAD_AVDD0
PP_DP_PAD_AVDD1
=PP1V1_DPORT_H4
C0909 0.1UF 10% 6.3V X5R 201
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
FL0910
240-OHM-0.2A-0.8-OHM
0201
DAC_AP_COMP_FTR
C0955 0.1UF 10% 6.3V X5R 201
DAC_AP_VREF
DAC_AP_IREF
C0956 0.1UF 10% 6.3V X5R 201
R0950 6.34K 1% 1/20W MF 201
TP_DP_AP_ANALOG_TEST
NOTE: 0.6V ANALOG REF
AP_DP_R_BIAS H34
DP_PAD_R_BIAS
C0950 0.01UF 10% 6.3V X6S 01005 NOSTUFF
R0920 4.99K 1% 1/32W MF 01005
L27 K29 H31 E29 D30 D31 G32 J31
DAC_AVDD30A DAC_AVDD30D DP_PAD_AVDD_AUX DP_PAD_AVDD0 DP_PAD_AVDD1 DP_PAD_AVDDP0 DP_PAD_AVDDX DP_PAD_DVDD
21MA 6MA 63MA 63MA 2MA 5MA 1.2MA
<= 5MA
SYM 6 OF 12
SC58940X01-A030
U0652
H4P-512MB
BGA
DAC_VREF J33
DAC_IREF J34
DAC_COMP K34
DP_PAD_DC_TP H33
DP_PAD_R_BIAS H34
DAC_OUT3 L34
DAC_OUT2 M34
DAC_OUT1 N34
DP_HPD R32
DP_PAD_AUXP G34
DP_PAD_AUXN F34
DP_PAD_TX0P D34
DP_PAD_TX0N C34
DP_PAD_TX1P A32
DP_PAD_TX1N A31
DAC_AP_OUT3 OUT 11 40 YIN
DAC_AP_OUT2 OUT 11 40 CVBSIN
DAC_AP_OUT1 OUT 11 40 CIN
DP_AP_HPD IN 13
DP_AP_AUX_P BI 13 40
DP_AP_AUX_N BI 13 40
DP_AP_TX_P<0> OUT 10 13 40
DP_AP_TX_N<0> OUT 10 13 40
DP_AP_TX_P<1> OUT 10 13 40
DP_AP_TX_N<1> OUT 10 13 40
NOTE: PLACE R0955-57 NEAR U0652
R0955 200 1% 1/20W MF 201
R0956 200 1% 1/20W MF 201
R0957 200 1% 1/20W MF 201
DAC_AVSS30A DAC_AVSS30A DAC_AVSS30D DP_PAD_AVSS_AUX DP_PAD_AVSS0 DP_PAD_AVSS1 DP_PAD_AVSSP0 DP_PAD_AVSSX DP_PAD_DVSS
M27 K27 K28 G31 D29 C30 C31 H32 J32
=PP1V8_H4
R0930 4.7K 5% 1/32W MF 01005
R0931 4.7K 5% 1/32W MF 01005
R0932 1.00K 5% 1/32W MF 01005
R0933 1.00K 5% 1/32W MF 01005
ISP_AP_0_SCL
ISP_AP_0_SDA
ISP_AP_1_SCL
ISP_AP_1_SDA
VOLTAGE=0.4V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
=PP1V8_MIPI_H4
C0907 0.1UF 10% 6.3V X5R 201
PP_AP_MIPI0D_0P4V
C0902 2.2NF 10% 10V X5R 201
=PP1V1_MIPI_H4
C0930 1UF 10% 6.3V CERM 402
C0908 0.1UF 10% 6.3V X5R 201
C0903 0.1UF 10% 6.3V X5R 201
PP_AP_MIPI1D_0P4V
C0920 2.2NF 10% 10V X5R 201
AP10 AP11 AP13 AP14 AP15 AP16 AP17 AP18 AN12
MIPI_VDD11
28MA
MIPI0D_VDD18 MIPI1D_VDD18 AN13 AN15
2MA ???
MIPI0D_VREG_0P4V MIPI1D_VREG_0P4V AP11 AP15
NC_AP_GPIO184 AA26
MIPI_VSYNC
REAR CAMERA
MIPI0C_AP_DATA_P<0> AW10
MIPI0C_AP_DATA_N<0> AY10
MIPI0C_DPDATA0
MIPI0C_DNDATA0
NC_MIPI0C_AP_DATA_P<1> AW11
NC_MIPI0C_AP_DATA_N<1> AY11
MIPI0C_DPDATA1
MIPI0C_DNDATA1
NC_MIPI0C_AP_DATA_P<2> AW13
NC_MIPI0C_AP_DATA_N<2> AY13
MIPI0C_DPDATA2
MIPI0C_DNDATA2
NC_MIPI0C_AP_DATA_P<3> AW14
NC_MIPI0C_AP_DATA_N<3> AY14
MIPI0C_DPDATA3
MIPI0C_DNDATA3
MIPI0C_AP_CLK_P AW12
MIPI0C_AP_CLK_N AY12
MIPI0C_DPCLK
MIPI0C_DNCLK
MIPID_AP_DATA_P<0> AW5
MIPID_AP_DATA_N<0> AY5
MIPID_AP_DATA_P<1> AW6
MIPID_AP_DATA_N<1> AY6
MIPID_AP_DATA_P<2> AW8
MIPID_AP_DATA_N<2> AY8
MIPID_AP_DATA_P<3> AW9
MIPID_AP_DATA_N<3> AY9
MIPID_AP_CLK_P AW7
MIPID_AP_CLK_N AY7
MIPI_VSS
AN12 AP12 AR14 AR16 AR17 AR18
SYM 5 OF 12
SC58940X01-A030
GROUP 5
U0652
H4P-512MB
BGA
ISP0_FLASH AG31 NC_AP_GPIO153
ISP0_PRE_FLASH AG29 NC_AP_GPIO152
ISP0_SCL AE26 ISP_AP_0_SCL OUT 7 25 39
ISP0_SDA AC29 ISP_AP_0_SDA BI 7 25 39
REAR CAMERA
ISP1_FLASH AJ32 NC_AP_GPIO155
ISP1_PRE_FLASH AG28 NC_AP_GPIO154
ISP1_SCL AC31 ISP_AP_1_SCL OUT 7 26 39
ISP1_SDA AF27 ISP_AP_1_SDA BI 7 26 39
FRONT CAMERA
SENSOR0_CLK AA33 CLK_CAM_RF_R 22 R0900 CLK_CAM_RF OUT 27 39
SENSOR0_RST Y26 PM_REAR_CAM_SHUTDOWN OUT 25
SENSOR1_CLK AA34 CLK_CAM_FF_R 22 R0940 CLK_CAM_FF OUT 26 39
SENSOR1_RST Y33 PM_FRONT_CAM_SHUTDOWN OUT 26
MIPI1C_DPDATA0 AW15 MIPI1C_AP_DATA_P<0> IN 26 40
MIPI1C_DNDATA0 AY15 MIPI1C_AP_DATA_N<0> IN 26 40
MIPI1C_DPDATA1 AW17 NC_MIPI1C_AP_DATA_P<1>
MIPI1C_DNDATA1 AY17 NC_MIPI1C_AP_DATA_N<1>
MIPI1C_DPCLK AW16 MIPI1C_AP_CLK_P OUT 26 40
MIPI1C_DNCLK AY16 MIPI1C_AP_CLK_N OUT 26 40
FRONT CAMERA

SYNC_MASTER=JAMES
SYNC_DATE=N/A
PAGE TITLE
AP: TV,DP,MIPI
Apple Inc.
DRAWING NUMBER 051-8962
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=PP1V2_S2R_H4
R1005 2.21K 1% 1/32W MF 01005
PPVREF_DDR0_CA
R1006 2.21K 1% 1/32W MF 01005
NOSTUFF C1002 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM

=PP1V2_S2R_H4
R1051 2.21K 1% 1/32W MF 01005
PPVREF_DDR1_CA
R1052 2.21K 1% 1/32W MF 01005
NOSTUFF C1052 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM

=PP1V2_VDDQ_H4
R1053 1.00K 1% 1/32W MF 01005
PPVREF_DDR0_DQ
R1054 1.00K 1% 1/32W MF 01005
NOSTUFF C1054 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM

=PP1V2_VDDQ_H4
R1055 1.00K 1% 1/32W MF 01005
PPVREF_DDR1_DQ
R1056 1.00K 1% 1/32W MF 01005
NOSTUFF C1056 0.01UF 10% 6.3V X5R 01005
VOLTAGE=0.6V
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.3MM
NET_SPACING_TYPE=VREF
MAX_NECK_LENGTH=3 MM

=PP1V2_S2R_H4
C1000 0.22UF 20% 6.3V X5R 0201
C1001 0.22UF 20% 6.3V X5R 0201

U0652
BGA
H4P-512MB
SYM 7 OF 12
SC58940X01-A030

H11	DDR0_VDDQ_CKE <1MA	VSS_32	AB10
R8	DDR1_VDDQ_CKE <1MA	VSS_33	AB12
AY23	DDR0_VREF_CA	VSS_34	AB14
AE34	DDR1_VREF_CA	VSS_35	AB16
AA1	DDR1_VREF_DQ	VSS_36	AB18
A25	DDR0_VREF_DQ	VSS_37	AB20
AY18	DDR0_ZQ	VSS_38	AB22
AK34	DDR1_ZQ	VSS_39	AB24
AD33			AB29
AH33	VDDCA 80MA		AC1
AW20			AC5
AW24		VSS	AC9
AW29			AC11
W33			AC13
A24			AC15
AA2			AC17
AF33			AC19
AK33			AC21
AL1			AC23
AW22			AC25
AW31	VDD2 320MA	VSS	AC27
B4			AD2
B5			AD8
B25			AD10
F33			AD12
T34			AD14
Y1			AD16
A4			AD18
A5			AD20
AB2			AD22
AL2			AD24
AL33			AD27
AW18	VDD1 40MA	VSS	AD34
AW32			AE5
B26			AE9
E33			AE11
U33			AE13
AC2			AE15
AG2			AE17
AK2			AE19
AN2			AE21
AT2			AE23
AW3			AE25
B3			AE33
B6			AF1
B8			AF5
B11			AF8
B14			AF10
B16			AF12
B19			AF14
B21			AF16
B24			AF18
B27	VDDQ 500MA (VDDQ = VDDIOD: DON'T DOUBLE COUNT)	VSS	AF20
B31			AF22
D2			AF24
D33			AF26
G2			AF32
G33			AG9
K2			AG11
K33			AG13
M2			AG15
N33			AG17
R2			AG19
R33			AG21
U2			AG23
Y2			AG25

R1001 240 1% 1/20W MF 201
(DDR IMPEDANCE CONTROL)
R1000 240 1% 1/20W MF 201

=PP1V2_S2R_H4
C1004 0.22UF 20% 6.3V X5R 0201
C1005 0.22UF 20% 6.3V X5R 0201
C1006 0.22UF 20% 6.3V X5R 0201
C1007 0.22UF 20% 6.3V X5R 0201
C1008 10UF 20% 6.3V X5R 603
C1009 4.3UF 20% 4V X5R-CERM 0610
C1010 1UF 10% 6.3V CERM 402
C1011 1UF 10% 6.3V CERM 402
C1012 0.01UF 10% 16V X5R 201
C1013 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF

=PP1V8_S2R_H4
C1014 10UF 20% 6.3V X5R 603
C1015 1UF 10% 6.3V CERM 402
C1016 1UF 10% 6.3V CERM 402
C1017 0.01UF 10% 16V X5R 01005
C1018 0.01UF 10% 16V X5R 01005
C1019 0.22UF 20% 6.3V X5R 0201
C1020 0.22UF 20% 6.3V X5R 0201
C1021 0.22UF 20% 6.3V X5R 0201
C1022 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF

=PP1V2_VDDQ_H4
C1023 10UF 20% 6.3V X5R 603
C1024 4.3UF 20% 4V X5R-CERM 0610
C1026 0.01UF 10% 16V X5R 01005
C1027 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF
C1029 0.22UF 20% 6.3V X5R 0201
C1030 0.22UF 20% 6.3V X5R 0201
C1031 0.22UF 20% 6.3V X5R 0201

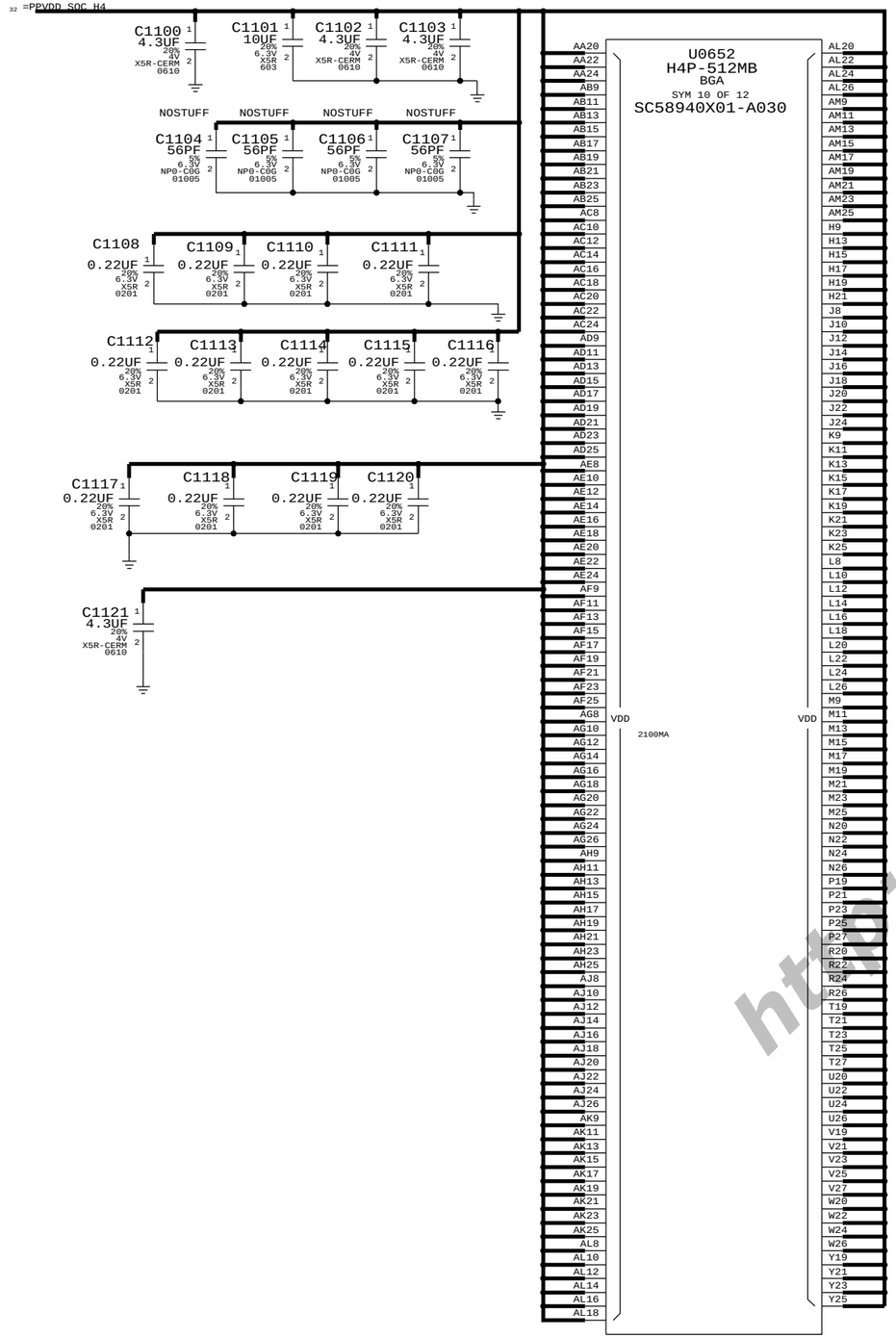
=PP1V2_VDDIOD_H4
C1032 10UF 20% 6.3V X5R 603
C1034 4.3UF 20% 4V X5R-CERM 0610
C1035 0.22UF 20% 6.3V X5R 0201
C1036 0.22UF 20% 6.3V X5R 0201
C1037 0.22UF 20% 6.3V X5R 0201
C1038 0.22UF 20% 6.3V X5R 0201
C1039 0.22UF 20% 6.3V X5R 0201
C1040 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF

U0652
H4P-512MB
BGA
SYM 9 OF 12
SC58940X01-A030

D4			AM16
D6			AM18
D8			AM20
D10			AM22
D12			AM24
D14			AM26
E5			AM28
E7			AM29
E9			AM30
E11			AN1
E13			AN14
E15			AN16
F4			AN17
F6			AN18
F7			AN19
F8			AN20
F9			AN24
F10			AN25
F11			AN26
F12			AN27
F13			AN28
F14			AN29
F15			AP5
F16			AP6
F17			AP7
F18			AP8
G5			AP9
G6			AP19
H4	VDDIOD 500MA (VDDQ = VDDIOD: DON'T DOUBLE COUNT)	VSS	AP21
H6			AP22
J5			AR1
J6			AR5
K4			AR6
K6			AR7
L5			AR8
L6			AR9
M4			AR13
M6			AR19
N5			AR24
N6			AR25
P4			AR26
P6			AR27
R5			AR28
R6			AR29
T4			AT5
T6			AT6
U5			AT7
U6			AT8
V4			AT9
V6			AT10
W5			AT11
W6			AT12
Y4			AT13
Y6			AT15
AA28			AT16
AB7			AT17
AB28			AT24
AC6			AT25
AC28			AT26
AD28			AT27
AE6			AT28
AF6			AT29
AH6			AU4
AN6			AU5
AN7	VDDIO18 44MA	VSS	AU6
AN8			AU7
H23			AU8
P28			AU9
R28			AU10
T28			AU11
W28			AU12
Y28			AU13

=PP1V8_VDDIO18_H4
C1041 56PF 5% 6.3V NP0-C0G 01005 NOSTUFF
C1042 0.22UF 20% 6.3V X5R 0201
C1043 1UF 10% 6.3V CERM 402
C1044 0.22UF 20% 6.3V X5R 0201
C1045 0.22UF 20% 6.3V X5R 0201
C1046 1UF 10% 6.3V CERM 402

SYNC_MASTER=JAMES SYNC_DATE=N/A
PAGE TITLE: AP: PWR
Apple Inc.
DRAWING NUMBER: 051-8962 SIZE: D
REVISION: A.0.0
BRANCH:
PAGE: 10 OF 106
SHEET: 8 OF 42



SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: PWR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

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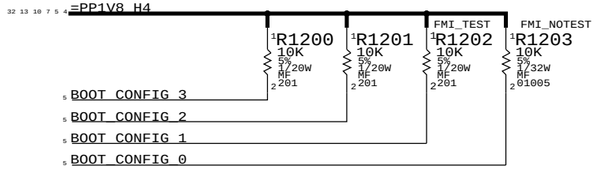
SHEET 9 OF 42

BOOT CONFIG ID

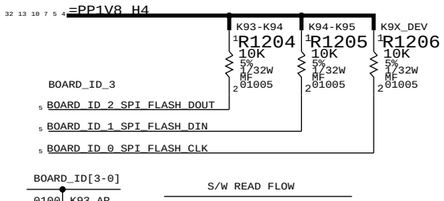


BOOT_CONFIG[3-0]	
1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS WITH TEST

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD ID

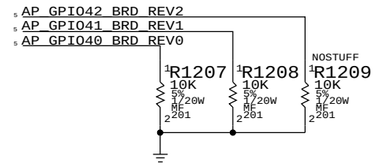


BOARD_ID[3-0]	
0100	K93 AP
0101	K93 DEV
0110	K94 AP
0111	K94 DEV
0010	K95 AP
0011	K95 DEV

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ

BOARD REVISION



BRD_REV[2-0]	
000	PROTO 1
001	PROTO 2
010	EVT
011	EVT2
100	DVT

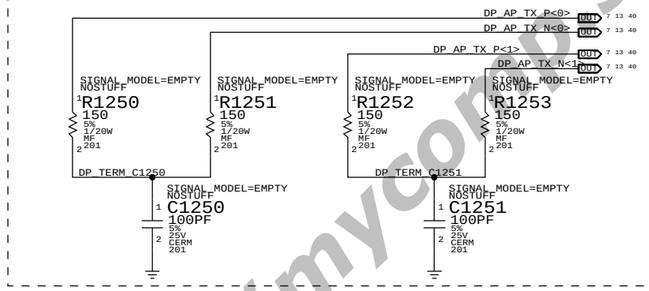
S/W READ FLOW

1. SET GPIO AS INPUT
2. ENABLE PU AND DISABLE PD
3. READ

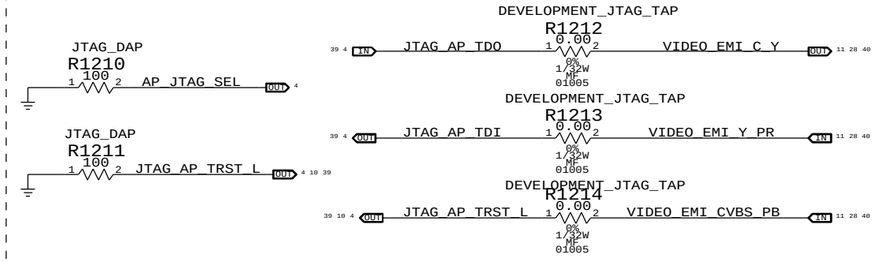
FOR REFERENCE

BOOT_CONFIG[3:0]	
0000	SPI0
0001	SPI3
0010	SPI0 W/TEST
0011	SPI3 W/TEST
0100	FMI0 2CS
0101	FMI0 4CS
0110	FMI0 4CS W/TEST
0111	RESERVED
1000	FMI1 2 CS
1001	FMI1 4 CS
1010	FMI1 4CS W/TEST
1011	RESERVED
1100	FMI0/1 2/2 CS
CURRENT SETTING -> 1101	FMI0/1 4/4 CS
1110	FMI0/1 4/4 CS W/TEST
1111	RESERVED

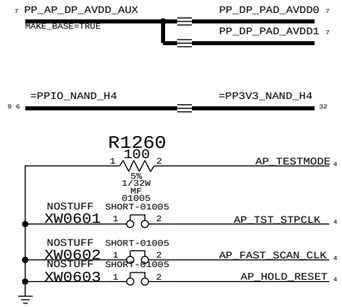
PLACEMENT NOTE: NEAR U0652

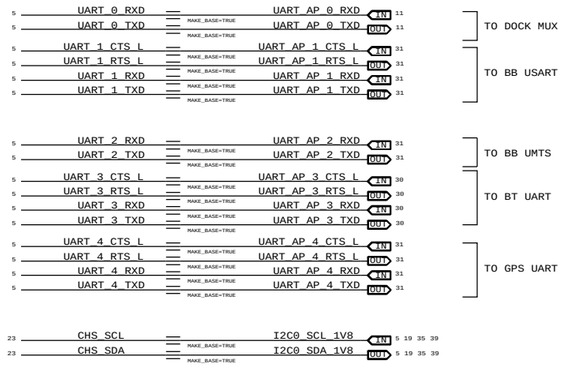


JTAG



2-WIRE DAP	SCAN DUMP	PRODUCTION
DEVELOPMENT_JTAG	DEVELOPMENT_JTAG	JTAG_DAP
JTAG_DAP	DEVELOPMENT_JTAG_TAP	





SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

AP: MISC & ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

REVISION A.0.0

BRANCH

PAGE 12 OF 106

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NOTE:
LDO3 PROVIDES 50MA TO BOTH H4P AND U1300
IF THAT'S NOT ENOUGH, STUFF R1371 AND NOSTUFF R1370

=PP3V0_VIDEO_BUF
R1371 0.00 0% 1/32W MF 01005
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
NOSTUFF
=PP3V0_VIDEO_BUFFER
R1370 0.00 0% 1/32W MF 01005
~15MA
PP3V0_U0900_FILTR
C1370 0.1UF 10% 6.3V X5R 201

=PP3V2_S2R_USBMUX
C1301 56PF 5% 6.3V NP0-C0G 01005
C1300 0.1UF 10% 6.3V X5R 201

U1300
THS7380IZSYR
UCSP

PORT_DOCK_VIDEO_AMP_EN
R1372 100K 5% 1/32W MF 01005

NOTE: PLACE R0960-62 NEAR U0900

YIN
CVBSIN
CIN
DAC_AP_OUT3
DAC_AP_OUT2
DAC_AP_OUT1
UART_AP_0_TXD
UART_AP_0_RXD
USB_BB_D_P
USB_BB_D_N

BUF_Y_PR
BUF_CVBS_PB
BUF_C_Y
JTAG DAP R1360 75 1% 1/20W MF 201
JTAG DAP R1361 75 1% 1/20W MF 201
JTAG DAP R1362 75 1% 1/20W MF 201
VIDEO_EMI_Y_PR
VIDEO_EMI_CVBS_PB
VIDEO_EMI_C_Y

USB_FS_P_ACC_RX
USB_FS_N_ACC_TX
USB_FS_D_P
USB_FS_D_N
DOCK_BB_EN
R1315 1.00M 5% 1/32W MF 01005
R1320 100K 5% 1/32W MF 01005

NOTE:
DOCK_BB_EN = 1: BB USB <-> DOCK SERIAL
DOCK_BB_EN = 0: BB USB <-> H4P FS USB
H4P UART0 <-> DOCK SERIAL

SYNC_MASTER=JAMES SYNC_DATE=N/A
PAGE TITLE
AP: VIDEO BUFFER,BB USB MUXES
Apple Inc.
DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
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16GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	1	TOSHIBA 32NM 16GB RAW	U1400	16GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	16GB_PROD	U1400	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	16GB_PROD	U1400	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	16GB_PROD	U1400	HYNIX 26NM 16GB PPN

32GB FLASH CONFIGURATIONS

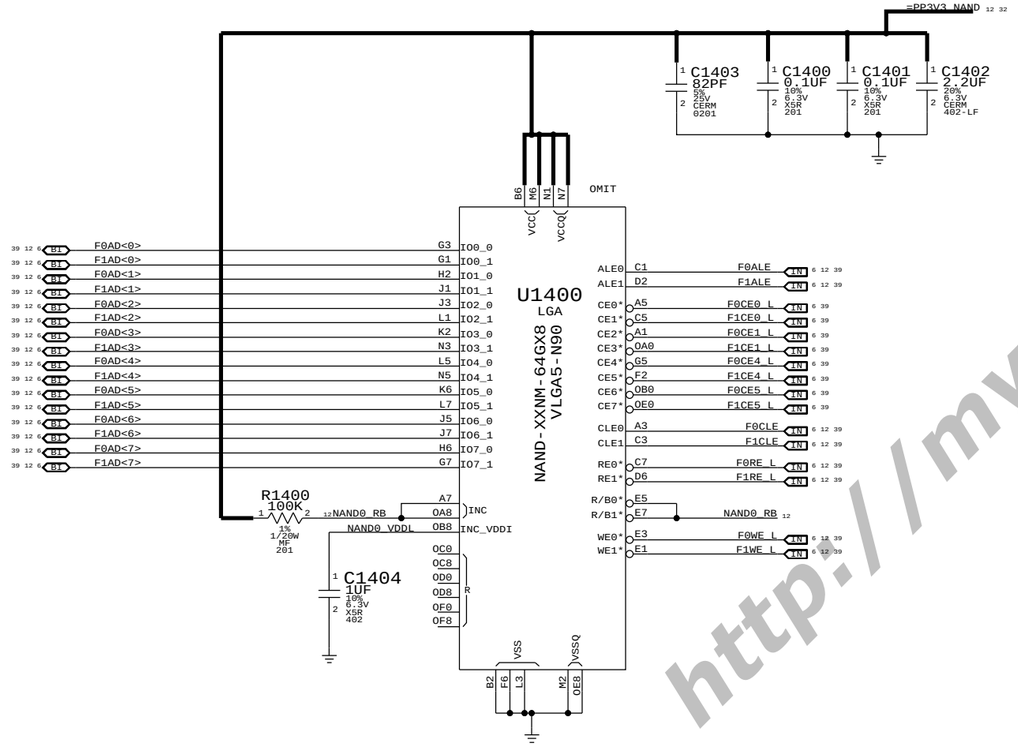
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0701	2	TOSHIBA 32NM 16GB RAW	U1400,U1410	32GB_PROD

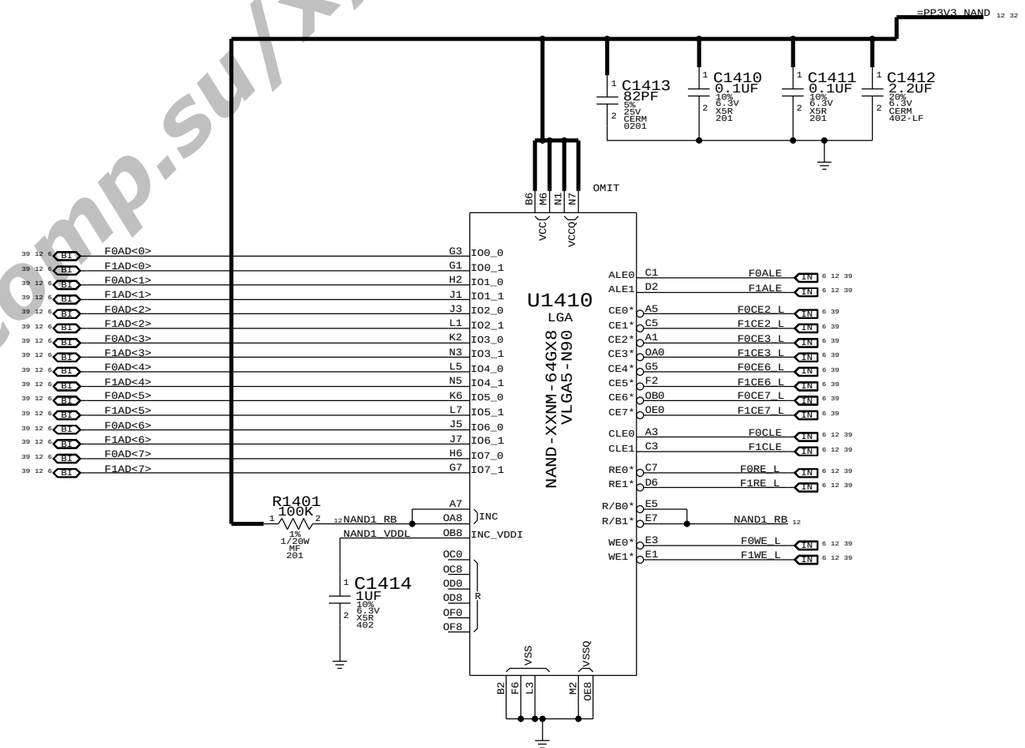
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0682	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 35NM 16GB RAW
335S0790	335S0701	32GB_PROD	U1400,U1410	SAMSUNG 27NM 16GB RAW
335S0781	335S0701	32GB_PROD	U1400,U1410	HYNIX 26NM 16GB PPN

64GB FLASH CONFIGURATIONS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S0702	2	TOSHIBA 32NM 32GB RAW	U1400,U1410	64GB_PROD

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
335S0665	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 35NM 32GB RAW
335S0791	335S0702	64GB_PROD	U1400,U1410	SAMSUNG 27NM 32GB RAW
335S0722	335S0702	64GB_PROD	U1400,U1410	SANDISK 32NM 32GB RAW
335S0782	335S0702	64GB_PROD	U1400,U1410	HYNIX 26NM 32GB PPN





SYNC_MASTER=JONATHAN SYNC_DATE=N/A

PAGE TITLE: NAND

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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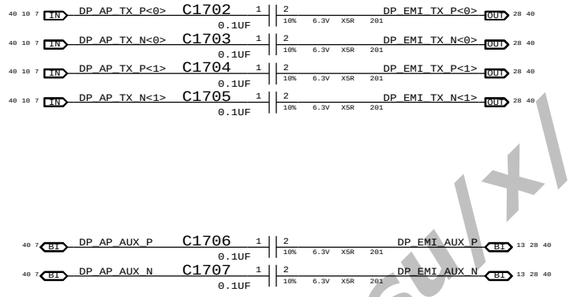
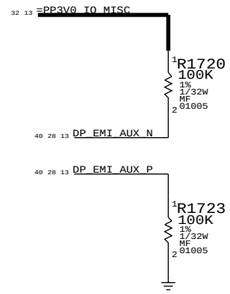
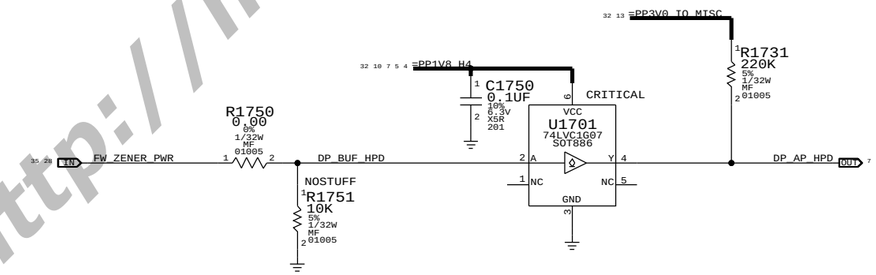
DISPLAYPORT AC COUPLING





DISPLAYPORT HOT PLUG DETECT



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0536	311S0341		U1701	RADAR:8481319

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
VIDEO: DISPLAY PORT

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
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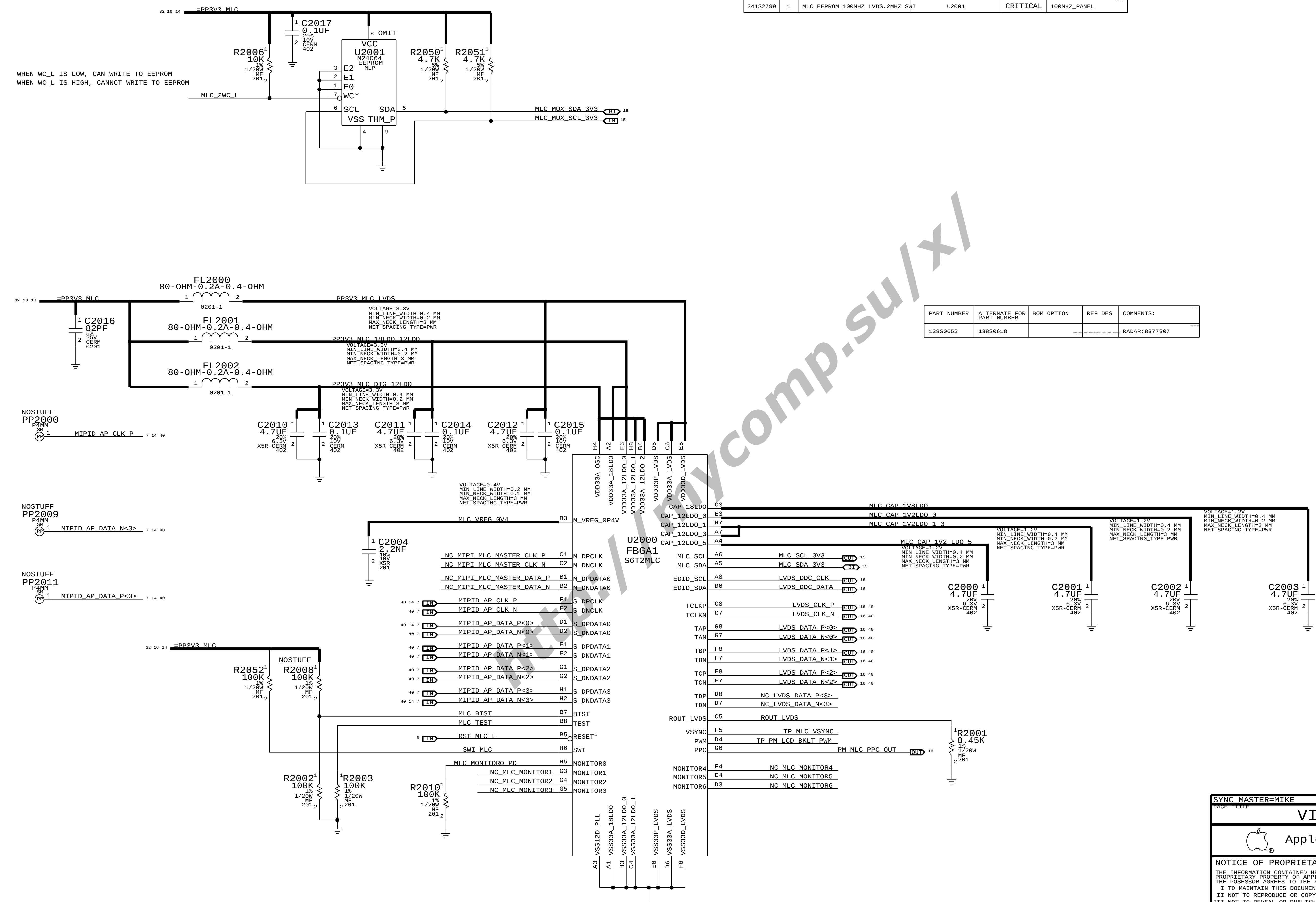
MLC EEPROM:RAW APN 335S0661

WHEN WC_L IS LOW, CAN WRITE TO EEPROM
WHEN WC_L IS HIGH, CANNOT WRITE TO EEPROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2799	1	MLC EEPROM 100MHZ LVDS,2MHZ SWI	U2001	CRITICAL	100MHZ_PANEL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0618			RADAR:8377307



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: VIDEO: MLC

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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14 MLC_SDA_3V3 ═══ MLC_MUX_SDA_3V3 14
14 MLC_SCL_3V3 ═══ MLC_MUX_SCL_3V3 14

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
VIDEO: MLC ALIASES

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
REVISION A.0.0
BRANCH
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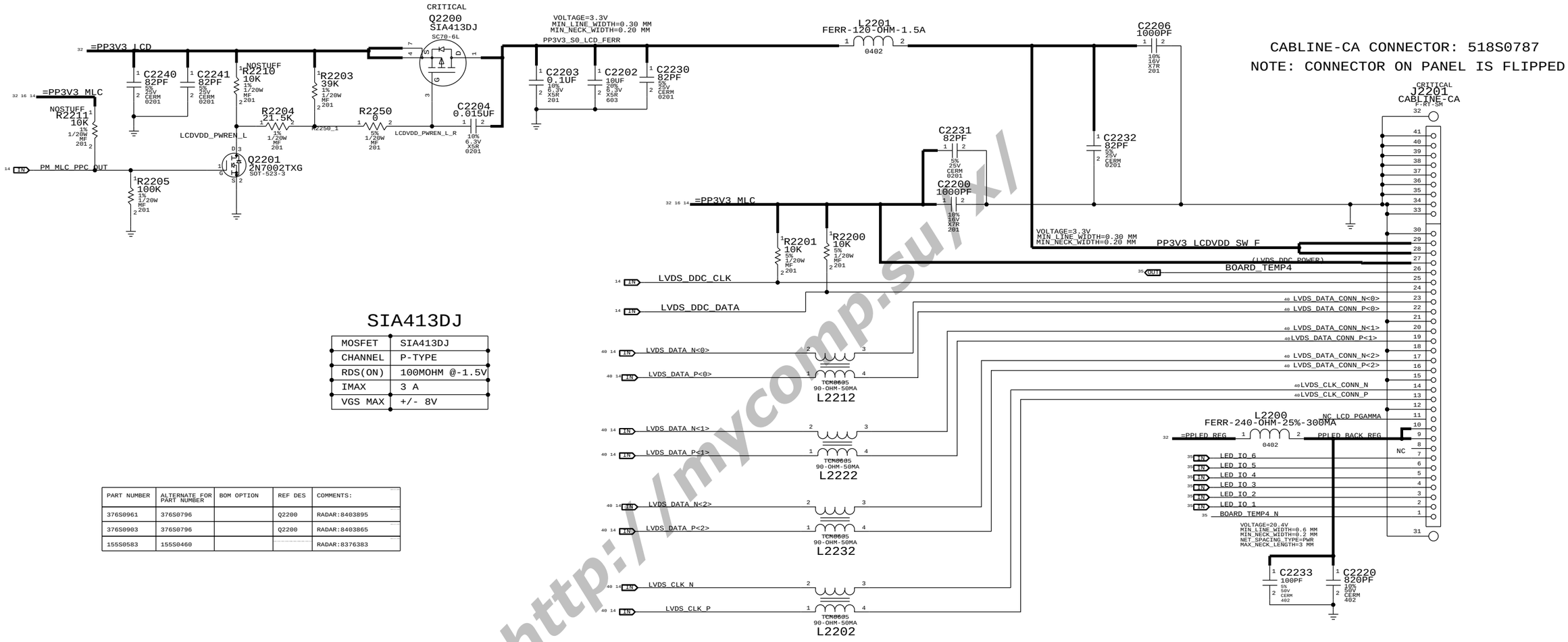
LVDS CONNECTOR



SIA413DJ

MOSFET	SIA413DJ
CHANNEL	P-TYPE
RDS(ON)	100MOHM @-1.5V
IMAX	3 A
VGS MAX	+/- 8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0961	376S0796		Q2200	RADAR:8403895
376S0903	376S0796		Q2200	RADAR:8403865
155S0583	155S0460			RADAR:8376383

NOSTUFF RESISTORS ARE THERE TO INVESTIGATE POSSIBILITY OF REMOVING THE CHOKE

SYNC_MASTER=ALEX SYNC_DATE=N/A

PAGE TITLE: VIDEO: LVDS CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH:

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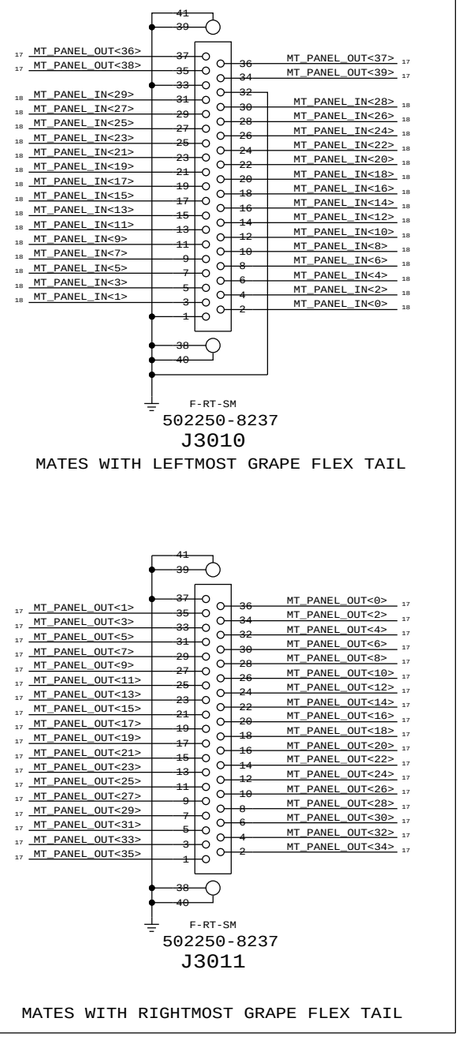
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0525	1	IC,ASIC,GROUNDHOG B0,120B BGA	U3003	CRITICAL	

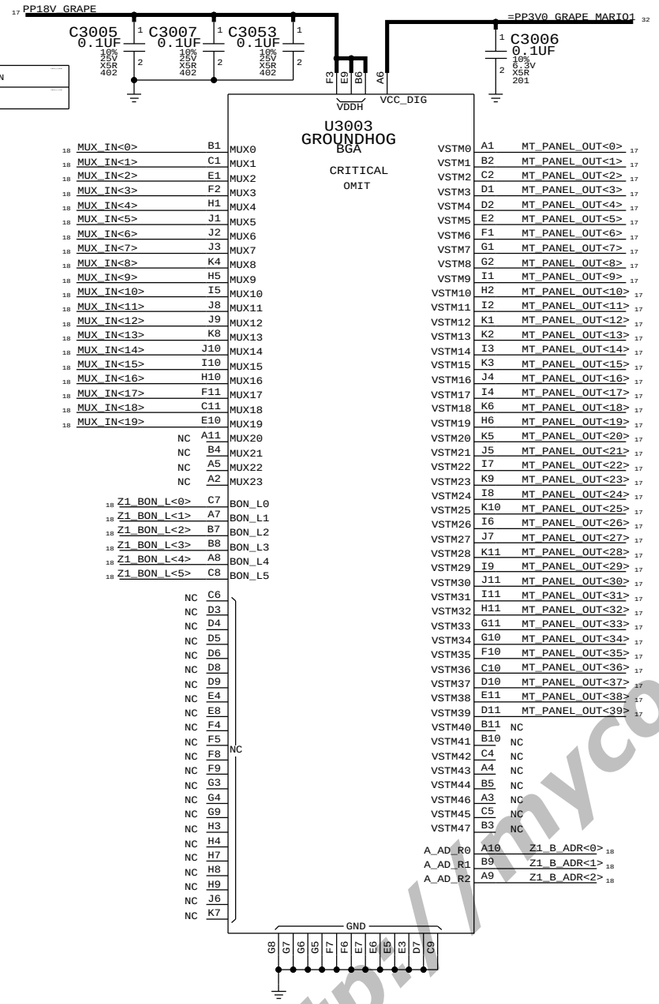
CONNECTORS TO GRAPE FLEX

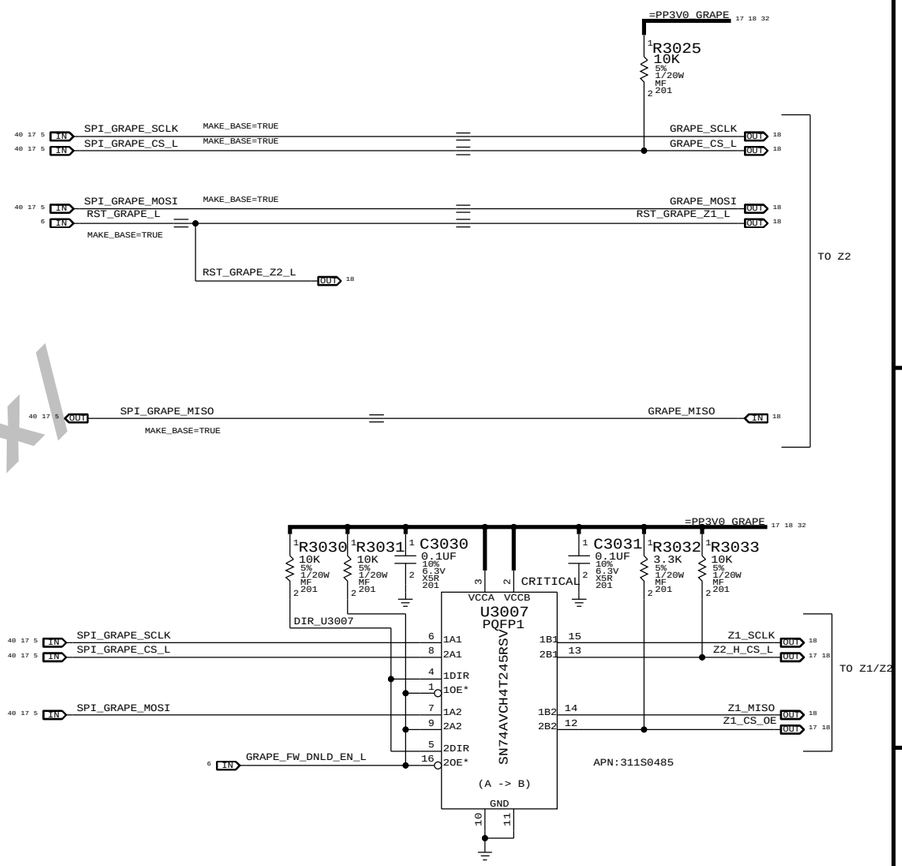
P/N 518S0817



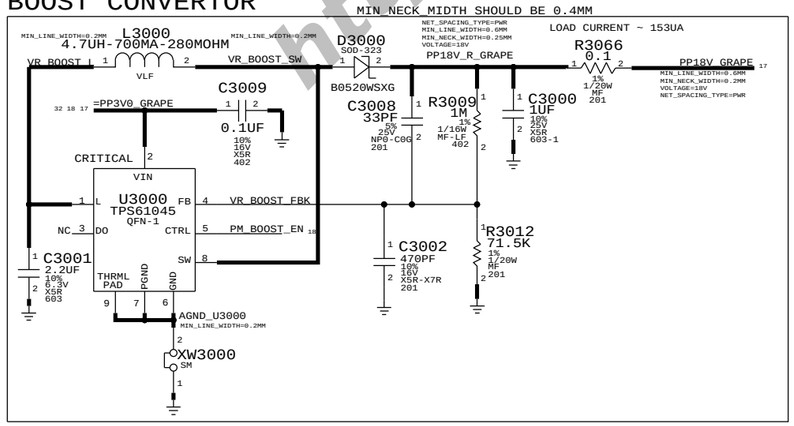
MATES WITH LEFTMOST GRAPE FLEX TAIL

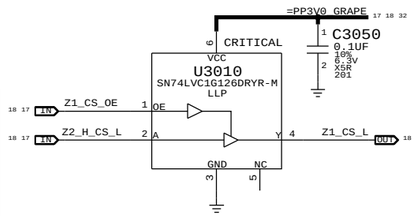
MATES WITH RIGHTMOST GRAPE FLEX TAIL

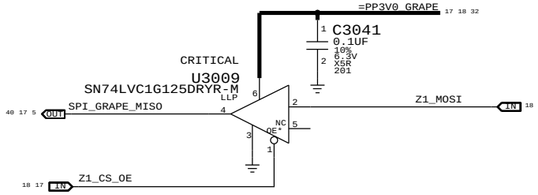




BOOST CONVERTOR







PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
311S0523	311S0485		U3007	
311S0524	311S0533		U3009	
311S0525	311S0532		U3010	

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

PAGE TITLE

GRAPE: GROUNDHOG,CONN,BOOST

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D

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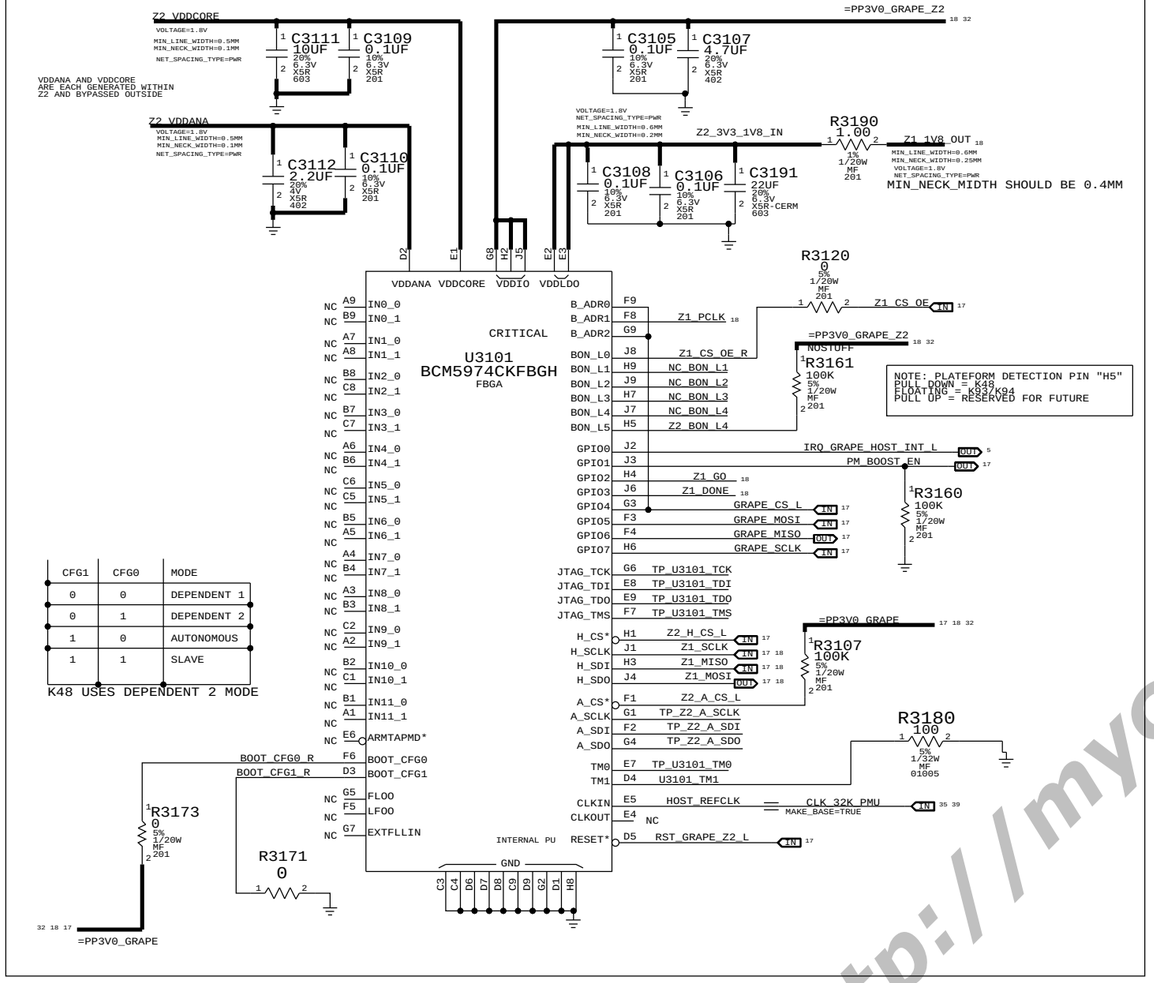
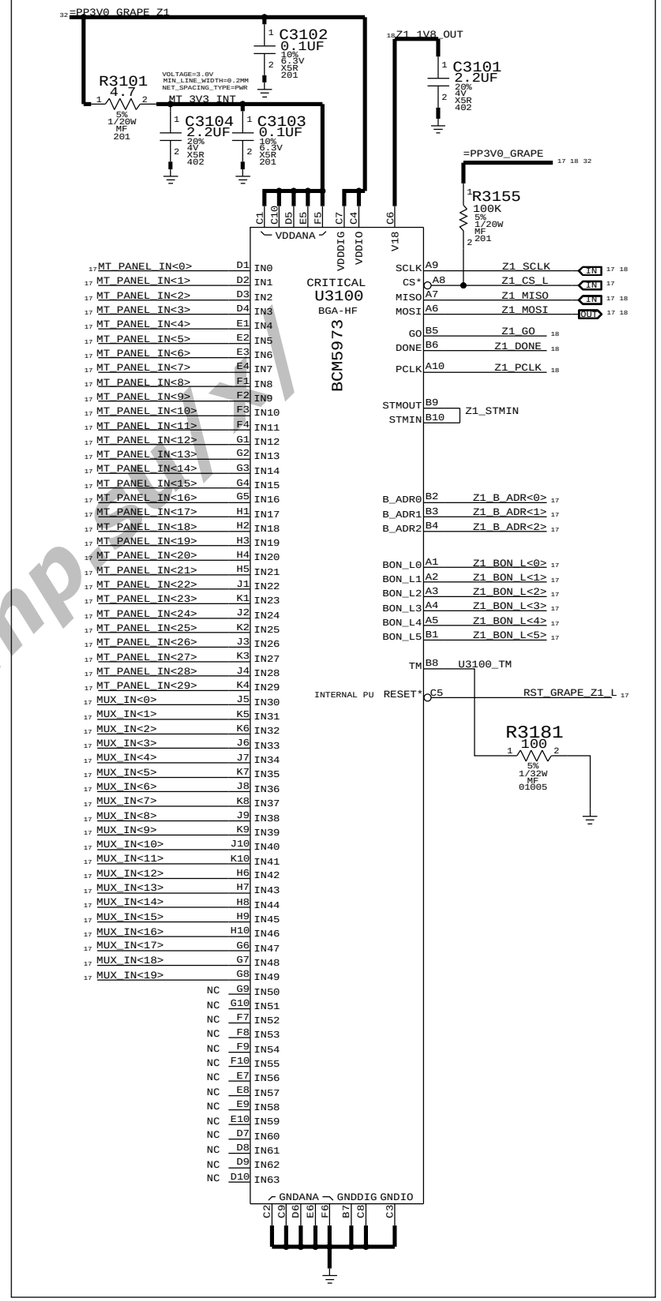
ARM9 MCU (Z2 BASED)



CFG1	CFG0	MODE
0	0	DEPENDENT 1
0	1	DEPENDENT 2
1	0	AUTONOMOUS
1	1	SLAVE

K48 USES DEPENDENT 2 MODE

ZEPHYR 1+ ASIC



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0652	138S0648		C3107	RADAR:8392120
138S0618	138S0648		C3107	BOM CONSOLIDATION

SYNC_MASTER=RAMSIN SYNC_DATE=N/A

PAGE TITLE: GRAPE: Z1, Z2

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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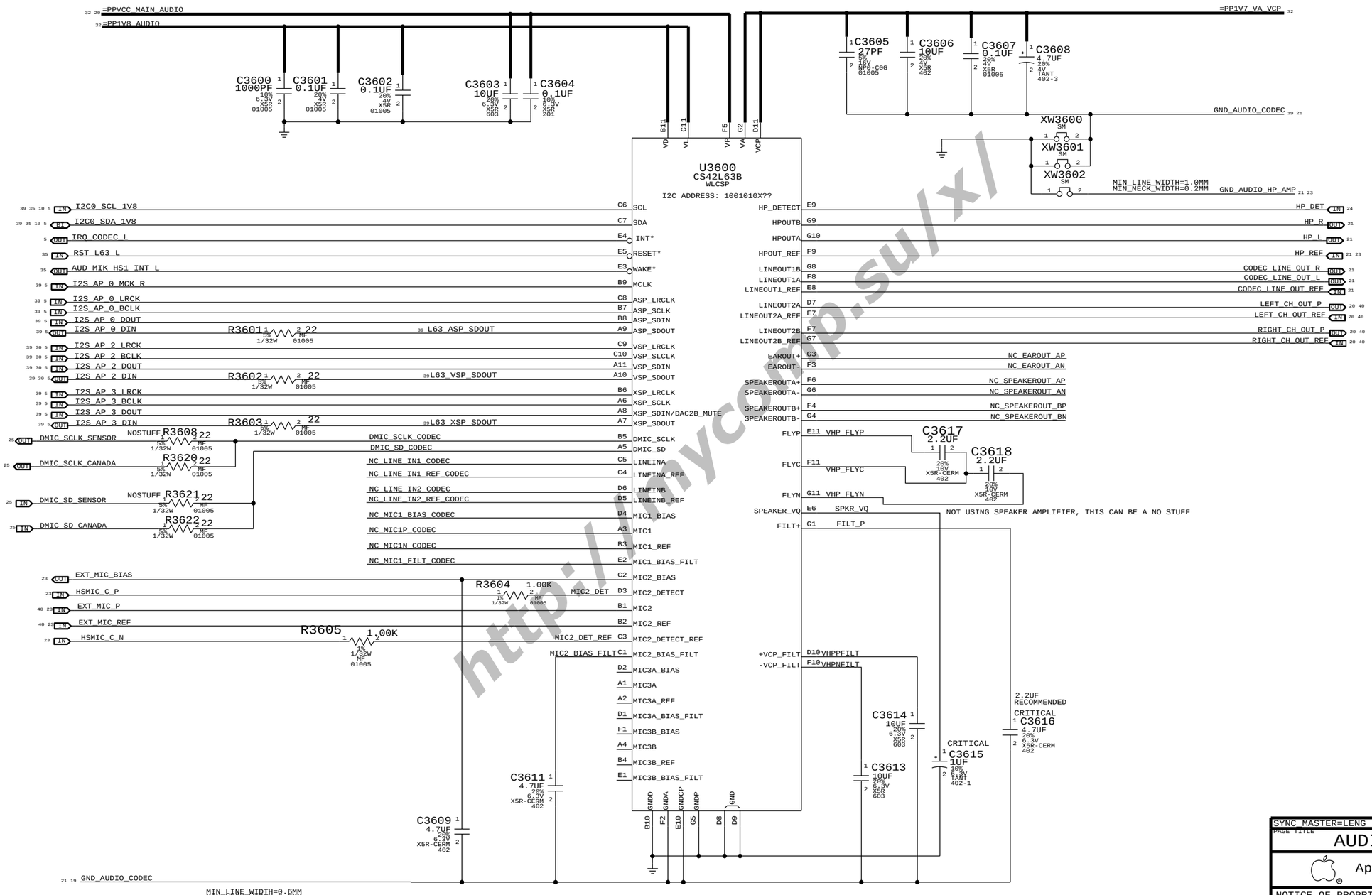
L63 AUDIO CODEC

APN:338S0940



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE: AUDIO: L63 CODEC

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

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SPEAKER AMPLIFIER

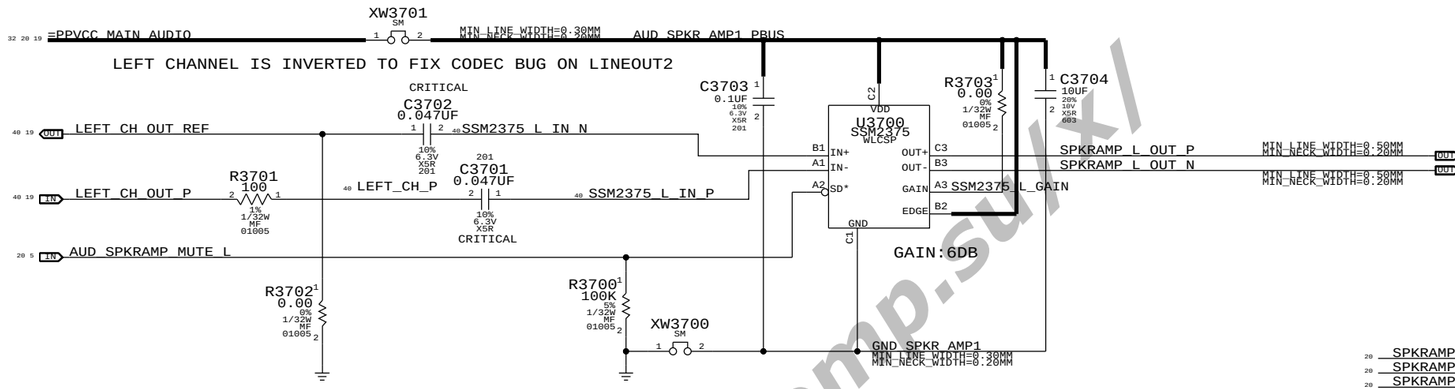
APN:353S2958

80HZ +/- XXX%

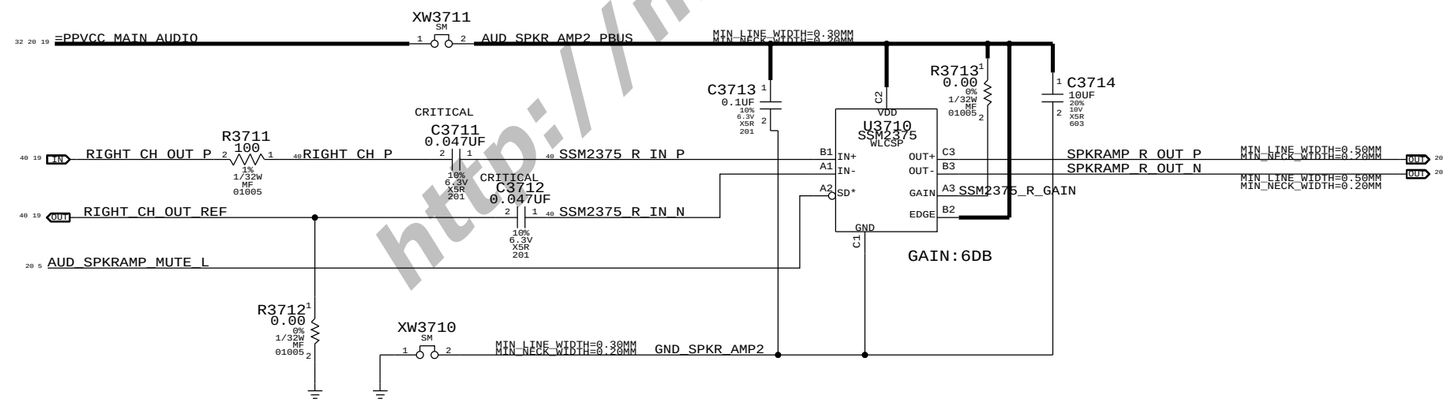
TURN ON TIME: 7.5MS

TURN ON DELAY: 20MS

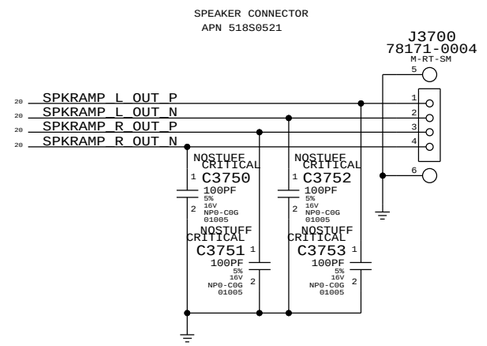
GAIN	VDD	GND
12DB	47K	NC
9DB	NC	47K
6DB	SHORT	NC
3DB	NC	NC
0DB	NC	SHORT



L63 LINEOUT2A IS CONNECTED TO U3700
L63 LINEOUT2B IS CONNECTED TO U3710



SPEAKER CONNECTOR
APN 518S0521



SYNC_MASTER=LENG	SYNC_DATE=N/A
PAGE TITLE: AUDIO: SPEAKER AMP	
Apple Inc.	DRAWING NUMBER: 051-8962 SIZE: D
	REVISION: A.0.0
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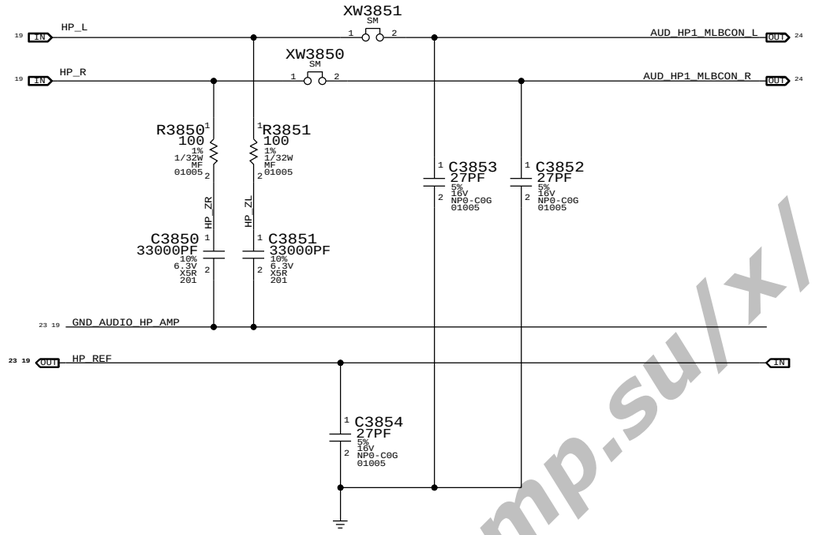
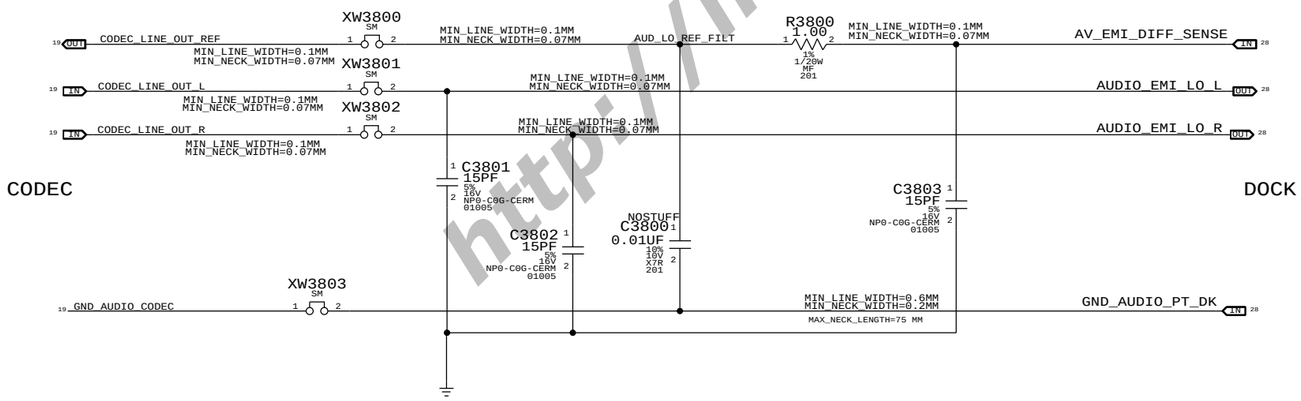
	SHEET: 20 OF 42

HEADPHONE OUTPUT ZOBEL NETWORK



DOCK LINE OUTPUT



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: HEADPHONE OUT

Apple Inc.

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SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE

AUDIO: BLANK

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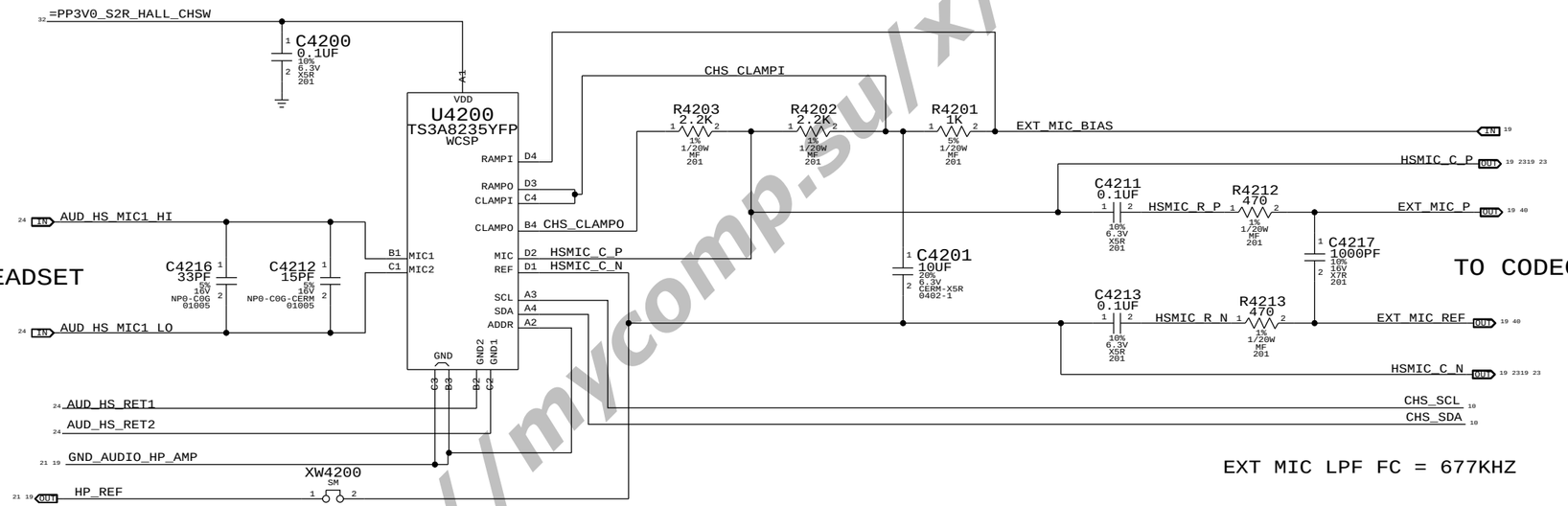
EXTERNAL (HEADSET) MIC INPUT CIRCUITRY



EXT MIC LPF FC = 677KHZ

SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: DETECT/MIC BIAS

Apple Inc.

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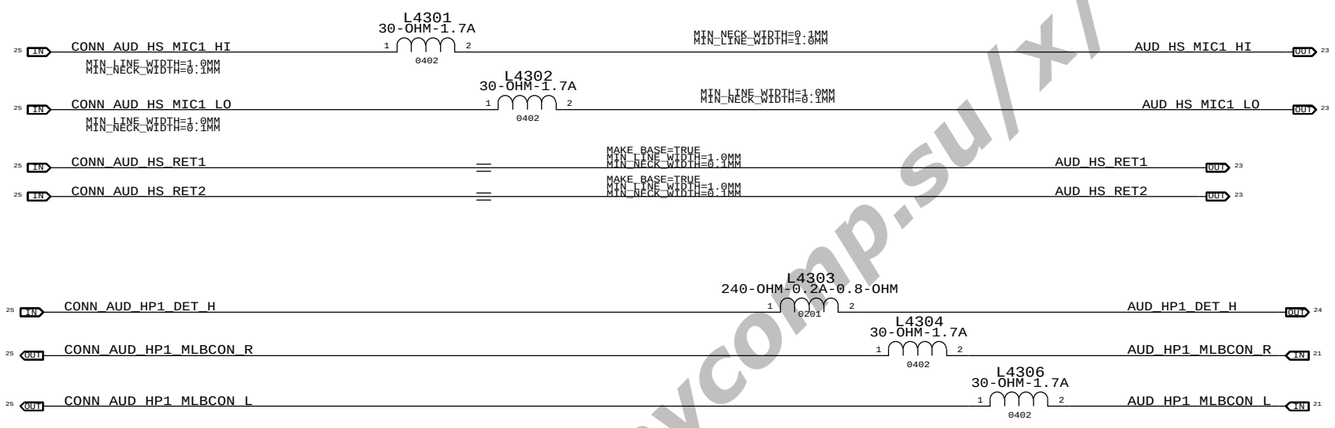
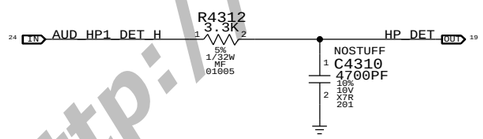
HEADPHONE JACK CONNECTION IS ON FRONT PANEL FLEX, CSA 55/PDF 29
PLACE ALL COMPONENTS NEAR J5501



HEADSET JACK INSERTION DETECT



SYNC_MASTER=LENG SYNC_DATE=N/A

PAGE TITLE
AUDIO: HP/MIC FILTERS

Apple Inc.

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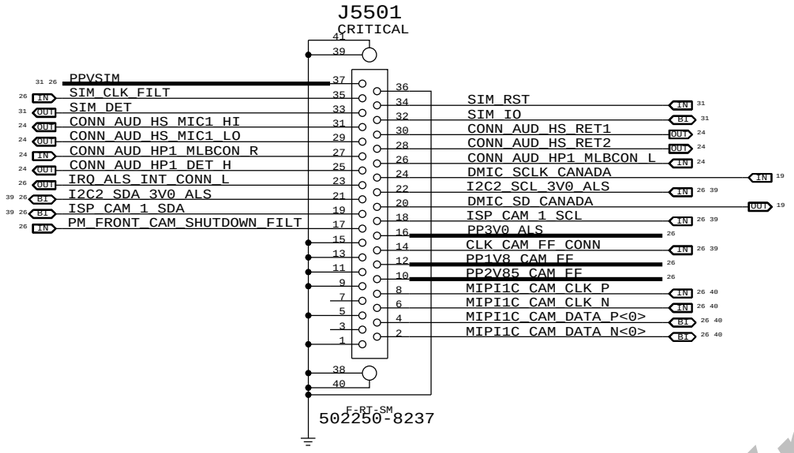
CANADA FLEXES CONN.

APN: 518S0817



SENSOR BOARD CONN ALIASES

39 27	CLK_CAM_RF_FILT	MAKE_BASE=TRUE	CONN_CLK_CAM_RF_FILT		27
40 27	MIPI0C_CAM_DATA_N<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_N<0>		27
40 27	MIPI0C_CAM_DATA_P<0>	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_DATA_P<0>		27
		MAKE_BASE=TRUE			
40 27	MIPI0C_CAM_CLK_N		CONN_MIPI0C_CAM_CLK_N		27
40 27	MIPI0C_CAM_CLK_P	MAKE_BASE=TRUE	CONN_MIPI0C_CAM_CLK_P		27
3	PM_REAR_CAM_SHUTDOWN	MAKE_BASE=TRUE	CONN_PM_REAR_CAM_SHUTDOWN		27
27	PP1V8_SENSOR_FILT	MAKE_BASE=TRUE	CONN_PP1V8_SENSOR_FILT		27
27	PP2V85_CAM_REAR	MAKE_BASE=TRUE	CONN_PP2V85_CAM_REAR		27
19	DMIC_SD_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SD_SENSOR		27
19	DMIC_SCLK_SENSOR	MAKE_BASE=TRUE	CONN_DMIC_SCLK_SENSOR		27
39 7	ISP_AP_0_SCL	MAKE_BASE=TRUE	CONN_ISP_AP_0_SCL		27
39 7	ISP_AP_0_SDA	MAKE_BASE=TRUE	CONN_ISP_AP_0_SDA		27
39 26 5	I2C2_SCL_3V0	MAKE_BASE=TRUE	CONN_I2C2_SCL_3V0		27
39 26 5	I2C2_SDA_3V0	MAKE_BASE=TRUE	CONN_I2C2_SDA_3V0		27
5	IRQ_ACCEL_INT1_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT1_L		27
5	IRQ_ACCEL_INT2_L	MAKE_BASE=TRUE	CONN_IRQ_ACCEL_INT2_L		27
5	IRQ_GYRO_INT1	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT1		27
5	IRQ_GYRO_INT2	MAKE_BASE=TRUE	CONN_IRQ_GYRO_INT2		27
39 5	I2C1_SCL_1V8	MAKE_BASE=TRUE	CONN_I2C1_SCL_1V8		27
39 5	I2C1_SDA_1V8	MAKE_BASE=TRUE	CONN_I2C1_SDA_1V8		27
35	IRQ_HALL	MAKE_BASE=TRUE	CONN_IRQ_HALL		27
5	IRQ_PROX_INT_L	MAKE_BASE=TRUE	CONN_IRQ_PROX_INT_L		27
27	PP3V0_S2R_HALL_FILT	MAKE_BASE=TRUE	CONN_PP3V0_S2R_HALL		27
35 5	ONOFF_L	MAKE_BASE=TRUE	CONN_ONOFF_FTR_L		27
35 5	SRL_L	MAKE_BASE=TRUE	CONN_SRL_FTR_L		27
5	AUD_VOL_UP_L	MAKE_BASE=TRUE	CONN_AUD_VOL_UP_FTR_L		27
5	AUD_VOL_DOWN_L	MAKE_BASE=TRUE	CONN_AUD_VOL_DOWN_FTR_L		27
		MAKE_BASE=TRUE			
27	PP3V0_OPTICAL_SENS	MAKE_BASE=TRUE	CONN_PP3V0_OPTICAL_SENS		27

SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: CANADA FLEX CONN,SENSOR PANEL ALIASES

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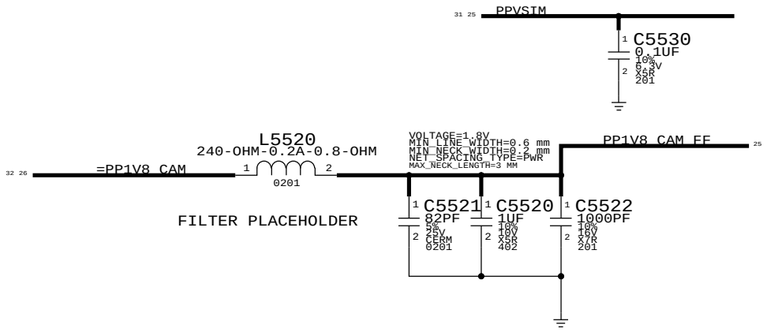
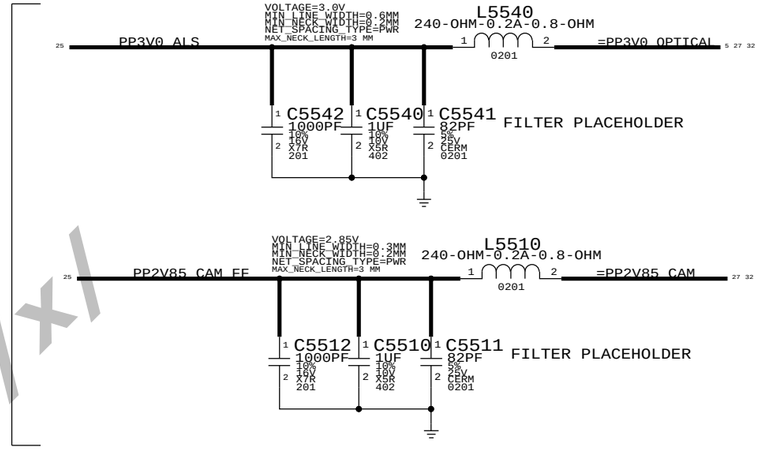
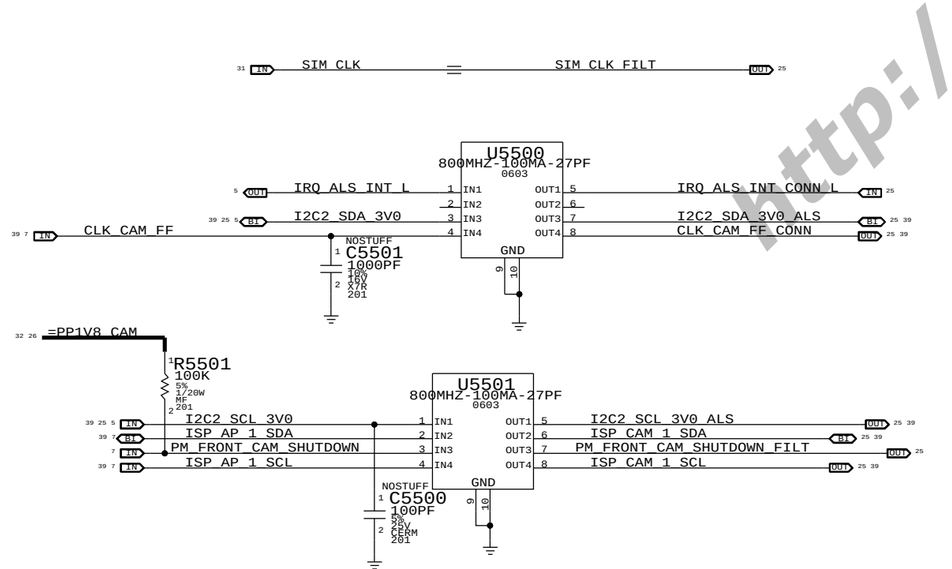
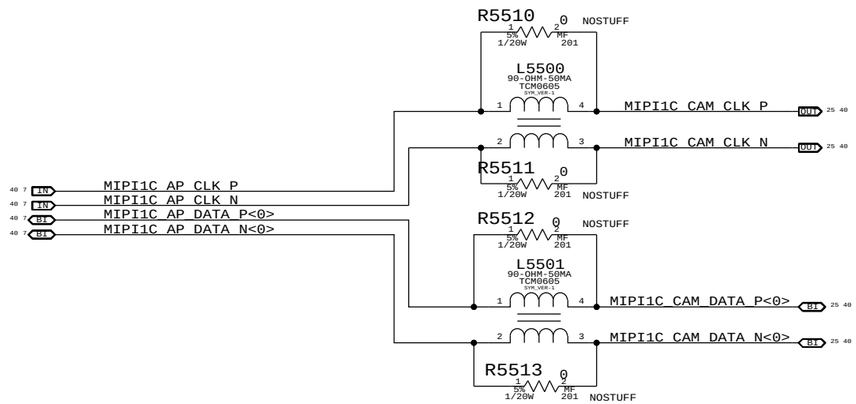


CANADA FLEX CONN ON PG 54



CANADA FLEX SIGNAL FILTERS





SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: CANADA FLEX FILTERS

Apple Inc.

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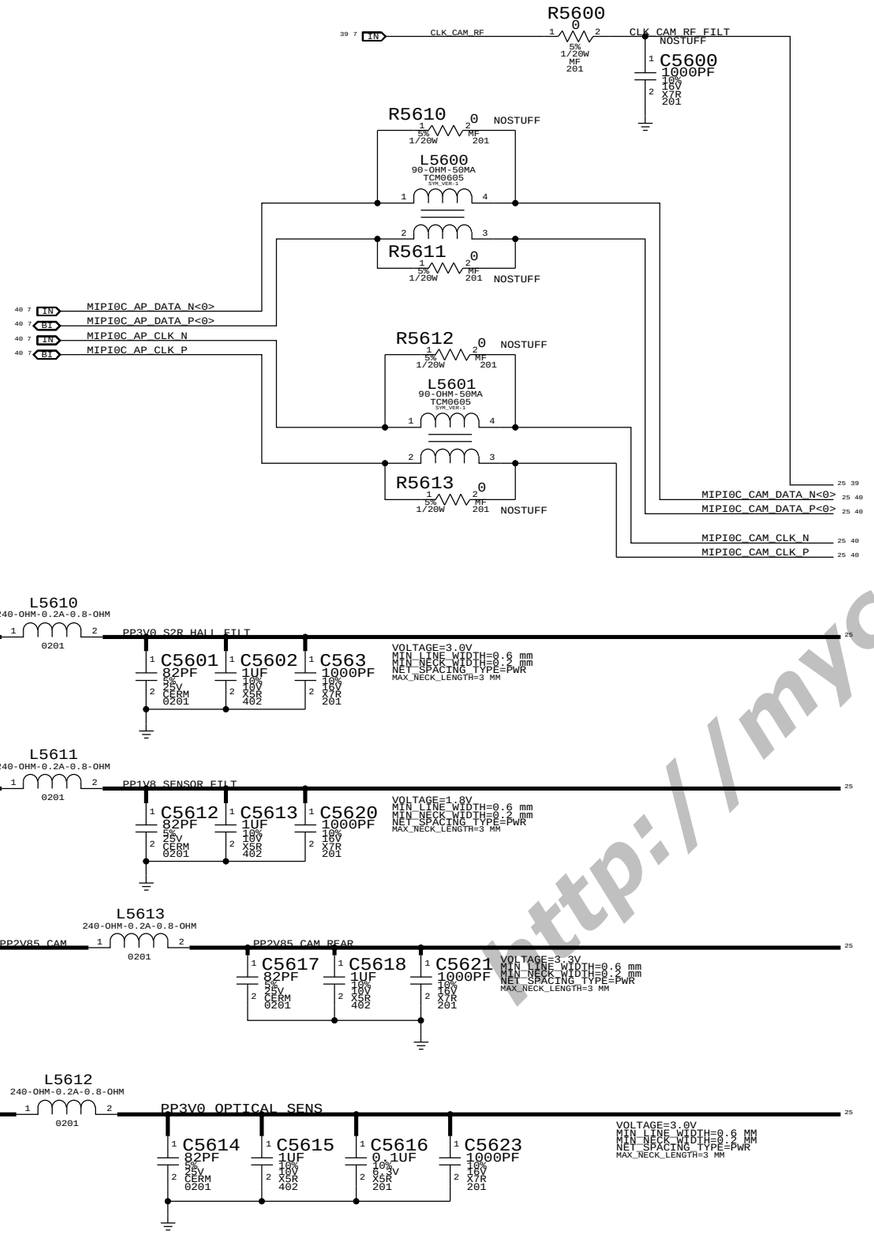
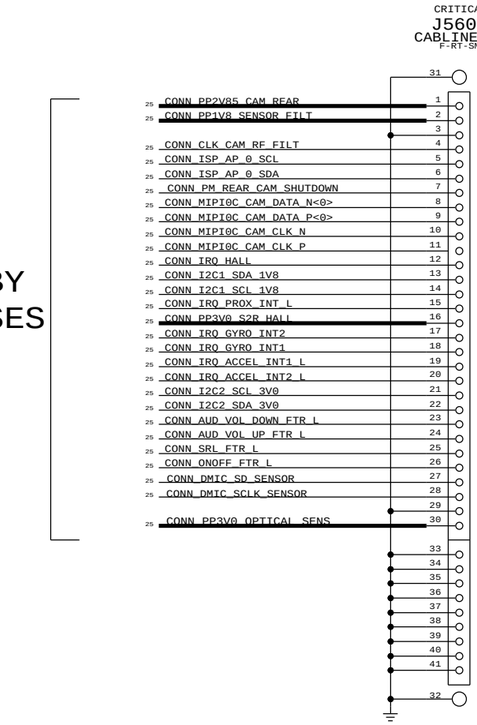


SENSOR PANEL CONNECTOR

CABLINE-CA CONNECTOR: 518S0787

CONNECTED BY
PG 54 ALIASES



SYNC_MASTER=MARK B. SYNC_DATE=N/A

PAGE TITLE

CONNECTOR: SENSOR PANEL CONNECTOR

Apple Inc.

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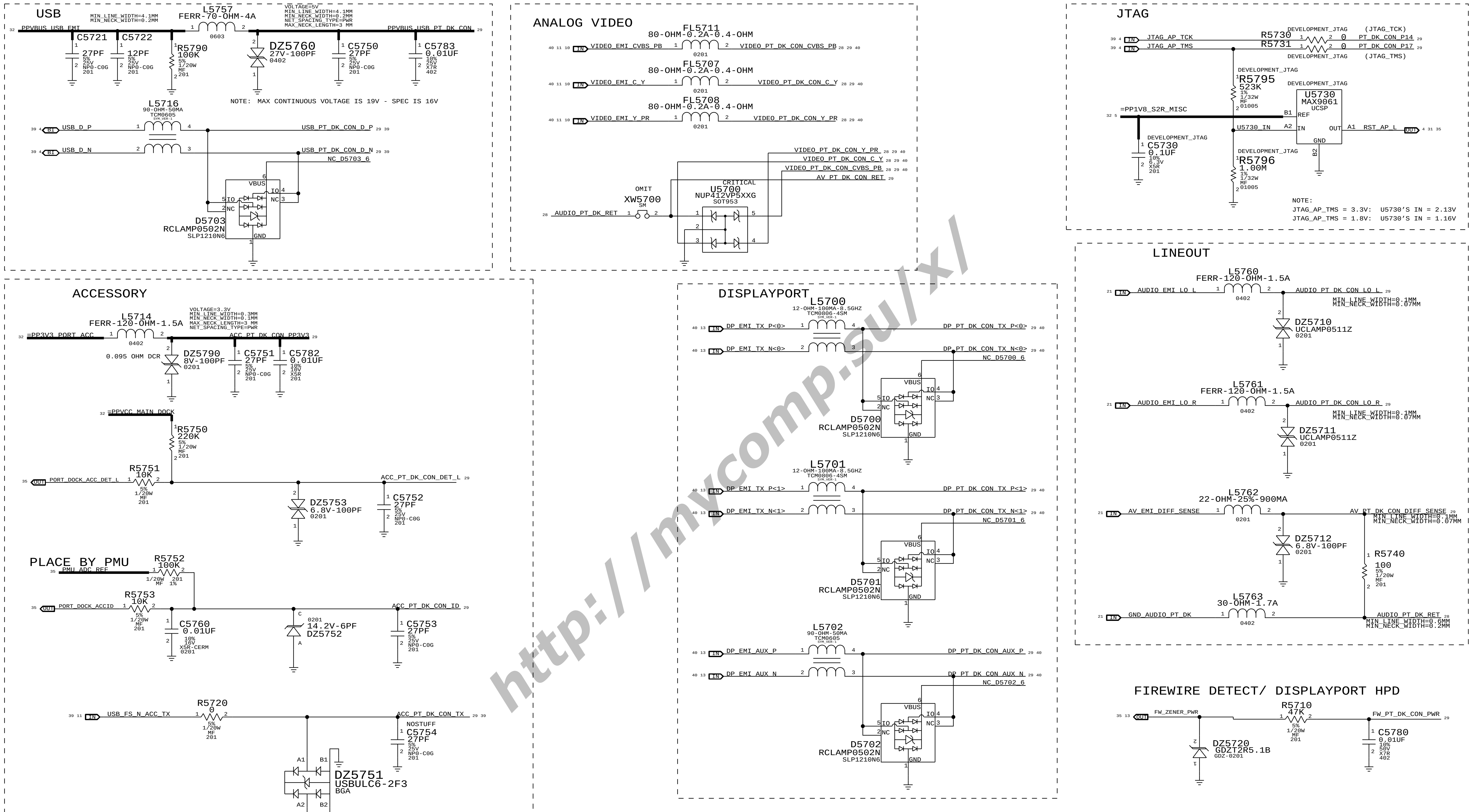

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
377S0090	377S0081		DZ5751	?
377S0111	377S0099		DZ5710,DZ5711	RADAR:8379541
377S0107	377S0066		D5700,D5701,D5702,D5703	RADAR:8289785
155S0625	155S0559		L5700,L5701	RADAR:8423156

SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE

IO FLEX: DOCK COMPONENTS

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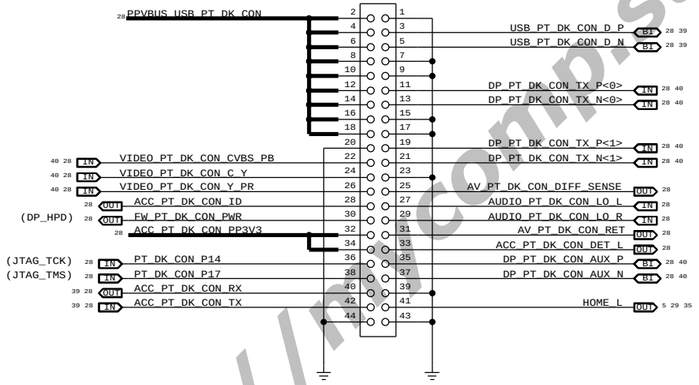
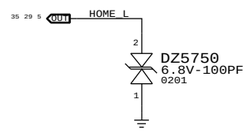
PN 516S0817 (PLUG - MALE)

CRITICAL

J5900
AXK844135WG
M-ST-SM





SYNC_MASTER=JAMES SYNC_DATE=N/A

PAGE TITLE
IO FELX: B2B Connector

Apple Inc.

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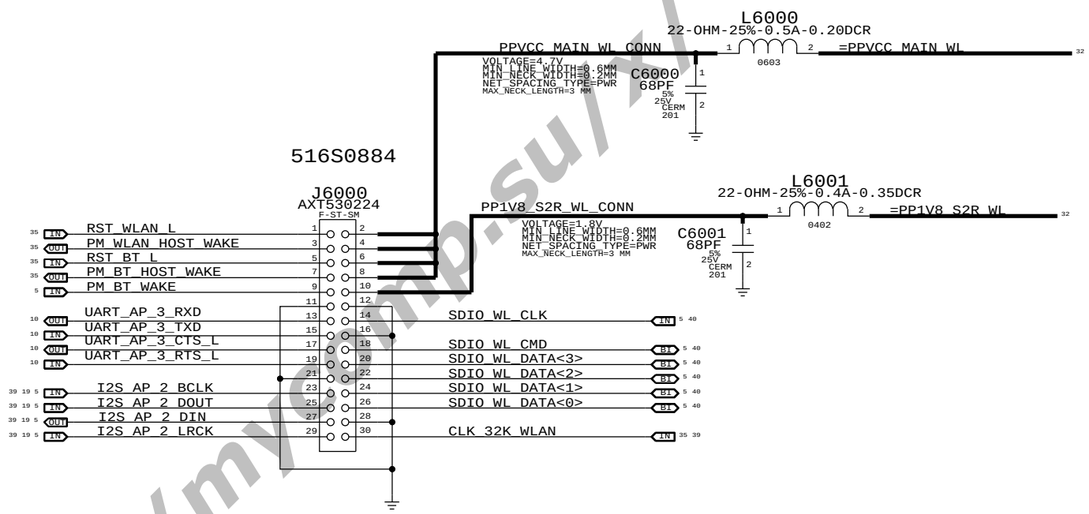
X23 WIFI/BT CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X23 WIFI/BT

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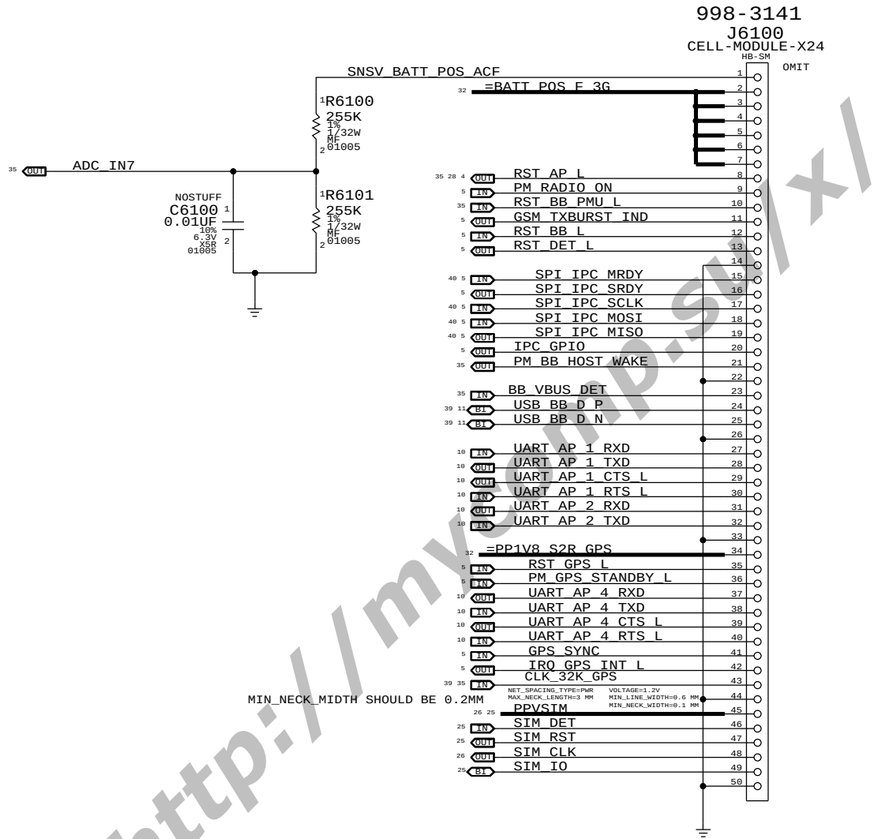
X24 CELLULAR/GPS CONNECTOR



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
CONNECTOR: X24 CELLULAR/GPS

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POWER CONN / ALIAS

LDO RAILS

PROGRAMMABLE ON/OFF

34 PP3V0_S2R_HALL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_S2R_HALL 27
= =PP3V0_S2R_HALL_CHSW 23

34 PP1V7_VA_VCP
MAKE_BASE=TRUE
VOLTAGE=1.7V
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V7_VA_VCP 19

34 PP3V0_VIDEO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_VIDEO_BUFFER 11
= =PP3V0_VIDEO_H4 7

34 PP3V0_OPTICAL
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_OPTICAL 5 26 27

34 PP3V2_SD
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM

34 PP3V3_ACC
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V3_PORT_ACC 28

34 PP3V0_VIDEO_BUF
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_VIDEO_BUF 11

34 PP3V2_S2R_USBMUX
MAKE_BASE=TRUE
VOLTAGE=3.2V
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V2_S2R_USBMUX 11

34 PP3V0_IO
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_IO_H4 7 9
= =PP3V0_IO_MISC 13

34 PP2V85_CAM
MAKE_BASE=TRUE
VOLTAGE=2.85V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP2V85_CAM 26 27

34 PP3V0_GRAPE
MAKE_BASE=TRUE
VOLTAGE=3.0V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V0_GRAPE 17 18
= =PP3V0_GRAPE_Z1 18
= =PP3V0_GRAPE_Z2 18
= =PP3V0_GRAPE_MARIO1 17

34 PP1V1
MAKE_BASE=TRUE
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V1_PLL_H4 4
= =PP1V1_MIPI_H4 7
= =PP1V1_DPORT_H4 7
= =PP1V1_USB_H4 4
= =PP1V1_MIPI_PLL_H4 4

34 PP1V8_ALWAYS
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V8_ALWAYS 5

BUCK RAILS

34 PP1V2_SOC
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PPVDD_SOC_H4 9

34 PP1V2_CPU
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PPVDD_CPU_H4 9

34 PP1V2_S2R
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V2_S2R_H4 8

34 PP1V8_S2R
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP1V8_S2R_H4 8
= =PP1V8_S2R_WL 30
= =PP1V8_S2R_GPS 31
= =PP1V8_S2R_MISC 5 28

34 PP1V8
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.1MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V8_CAM 26
= =PP1V8_SENSOR 27
= =PP1V8_AUDIO 19
= =PP1V8_H4 4 5 7 10 13
= =PP1V8_VDDIO18_H4 8 9
= =PP1V8_MIPI_H4 7
= =PP1V8_DPORT_H4 7

34 PP3V3_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP3V3_NAND 12
= =PP3V3_USB_H4 4
= =PP3V3_MLC_HI 36
= =PP3V3_LCD 16
= =PP3V3_NAND_H4 10

35 PPLED_OUT
MAKE_BASE=TRUE
VOLTAGE=20.4V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PPLED_REG 16

36 PP3V3_MLC_OUT
MAKE_BASE=TRUE
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PP3V3_MLC 14 16

34 PP1V2
MAKE_BASE=TRUE
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.1 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=0.8 MM
MIN_NECK_MIDTH SHOULD BE 0.2MM
= =PP1V2_VDDQ_H4 8
= =PP1V2_VDDIOD_H4 8
= =PP1V2_HSIC_H4 4

GND
MAKE_BASE=TRUE
VOLTAGE=0V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=GND
MAX_NECK_LENGTH=5 MM

CHARGER MAIN

35 34 PPVCC_MAIN
MAKE_BASE=TRUE
VOLTAGE=4.7V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=3 MM
= =PPVCC_MAIN_AUDIO 19 20
= =PPVCC_MAIN_WL 30
= =PPVCC_MAIN_DOCK 28
= =PPVCC_MAIN_LED 35

BATTERY

37 34 PPBATT_VCC
MAKE_BASE=TRUE
VOLTAGE=4.2V
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.15 MM
NET_SPACING_TYPE=PWR
MAX_NECK_LENGTH=1.7 MM
= =BATT_POS_F_3G 31
= =BATT_POS_CONN 33

USB POWER INPUT

28 PPVBUS_USB_EMI
= =PPVBUS_USB_DCIN 34
MAKE_BASE=TRUE

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: ALIASES

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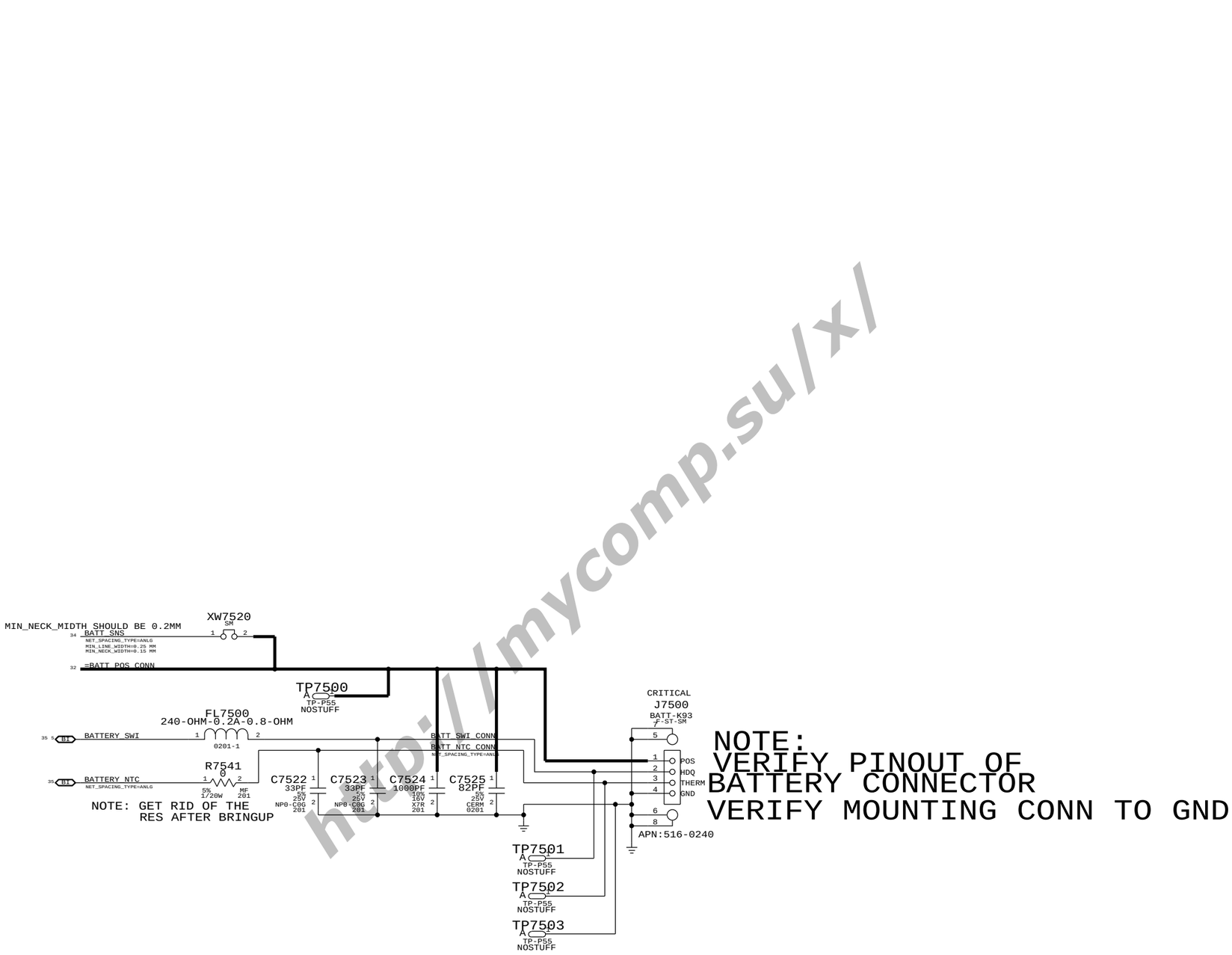

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: BATTERY CONNECTOR

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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BRANCH
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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0542	1	IC,PMU,ALISON,D1946A2,OTPXX,UFBGA292	U8100	CRITICAL	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0392	197S0299		Y8138	ALT FOUNDRY

MOSFET	FDMC6676BZ
CHANNEL	P-TYPE
RDS(ON)	27 MOHM @-4.5V
IMAX	6.9 A
VGS MAX	+/- 25V

USB REVERSE VOLTAGE PROTECTION

NOTE: FOR NO BATTERY SITUATION

VCC_MAIN BYPASS
TOTAL CAPS = ~400UF
(DISTRIBUTED AND NO DE-RATING)

(PLACE ONE 1UF CAP AT EACH VDD INPUT)

NOTE: CONCERNED ABOUT ESR > 20MOHM

LDO BYPASS

ADDITIONAL DISTRIBUTED:
PP1V2: 30UF (NO DE-RATING)
PP1V8: 6UF (NO DE-RATING)

SYNC_MASTER=YOSH	SYNC_DATE=N/A
PAGE TITLE	POWER: PMU
Apple Inc.	DRAWING NUMBER 051-8962 SIZE D
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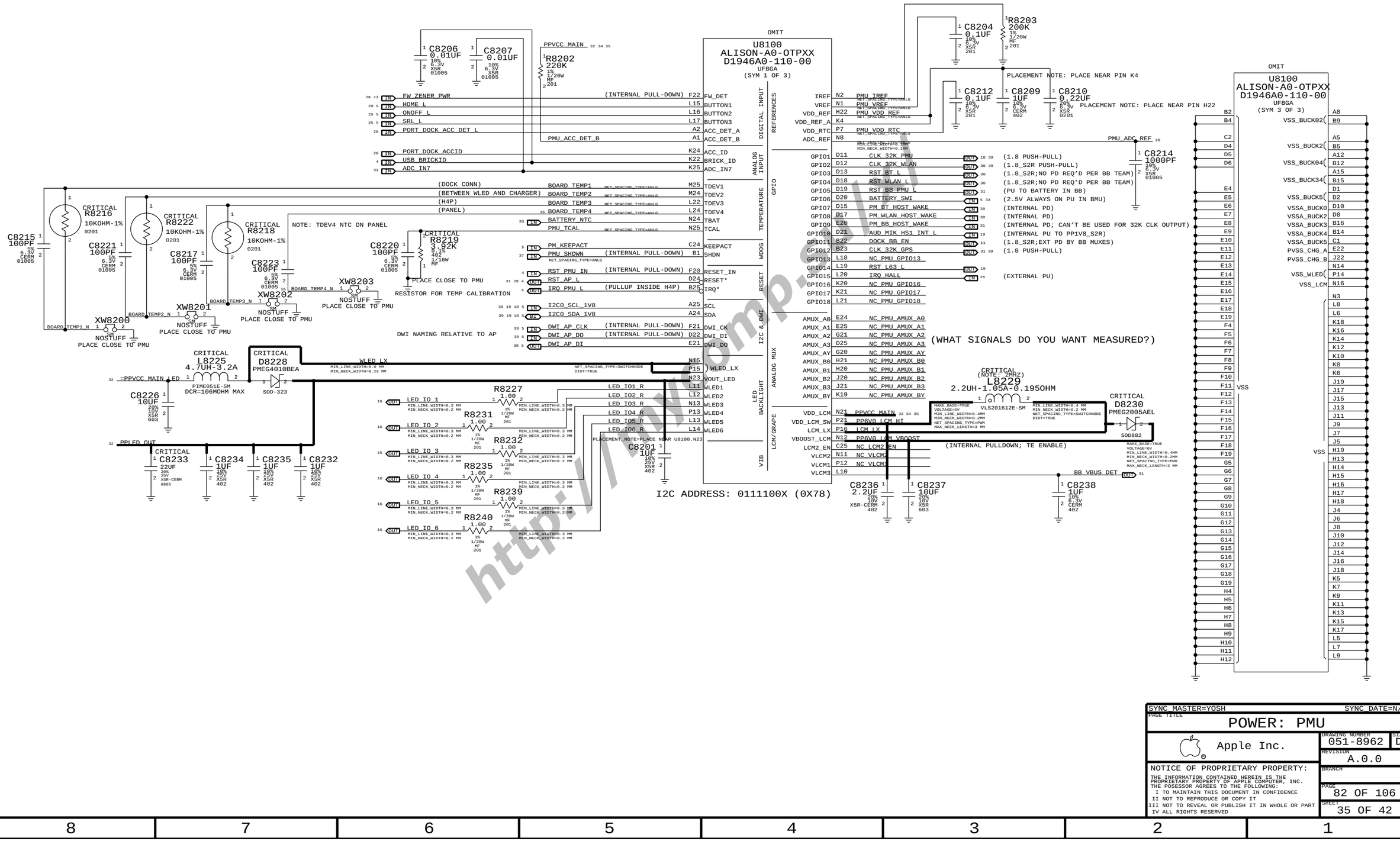

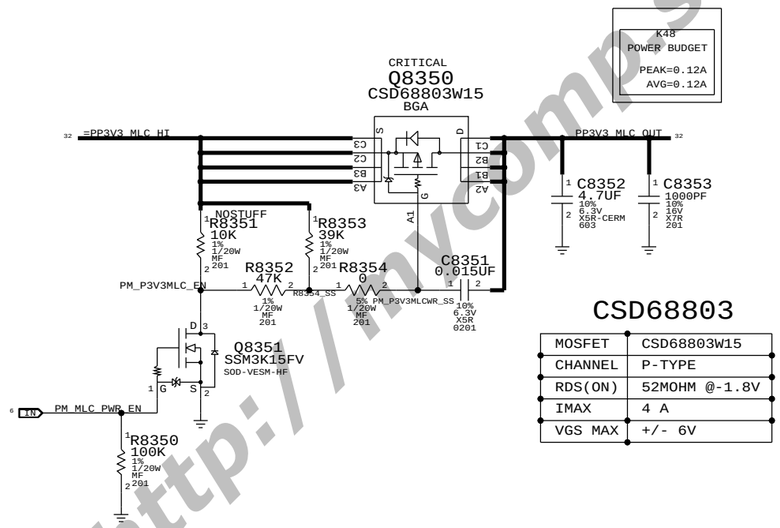

CSD68803

MOSFET	CSD68803W15
CHANNEL	P-TYPE
RDS(ON)	52MOHM @-1.8V
IMAX	4 A
VGS MAX	+/- 6V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0972	376S0612		Q8351	RADAR:8537160

SYNC_MASTER=YOSH SYNC_DATE=N/A

PAGE TITLE
POWER: 3.3V MLC & 1.2V VR

Apple Inc.

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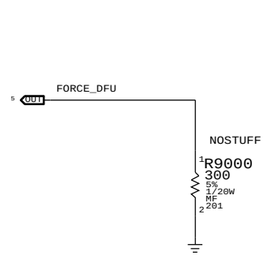
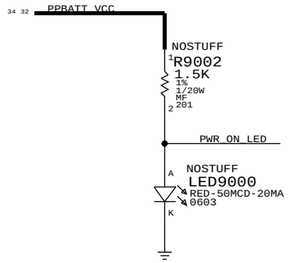
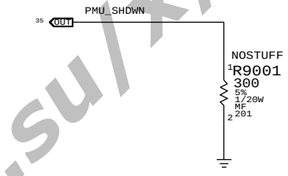
DEBUG RESET ACCESS

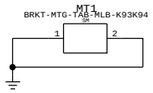
PLACE OUTSIDE OF CAN?







LEFT AND RIGHT MOUNTING TABS



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
DEBUG AND MISC

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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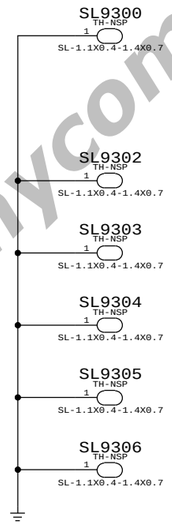
PLATED THROUGH HOLES

DRILL SIZE: 1.1MM X 0.4MM
PLATING SIZE: 1.4MM X 0.7MM



SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE
FCT/ICT TEST/BRACKETS

Apple Inc.

DRAWING NUMBER 051-8962 SIZE D
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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I63	CLK_50S	CLK	CLK_32K_PMU	18 35
I162	CLK_50S	CLK	CLK_32K_WLAN	30 35
I81	CLK_50S	CLK	CLK_32K_GPS	31 35
I88	CLK_50S	CLK	CLK_CAM_FF	7 26
I89	CLK_50S	CLK	CLK_CAM_FF_FILT	
I95	CLK_50S	CLK	CLK_CAM_FF_CONN	25 26
I96	CLK_50S	CLK	CLK_CAM_RF	7 27
I94	CLK_50S	CLK	CLK_CAM_RF_FILT	25 27
I130	CLK_50S	CLK	I2S_AP_0_MCK	5
I131	CLK_50S	CLK	I2S_AP_0_MCK_R	5 19
I157	CLK_50S	CLK	CLK_CAM_FF_R	7
I158	CLK_50S	CLK	CLK_CAM_RF_R	7

NAND

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
NAND_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
NAND	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I50	NAND_50S	NAND	F0AD<7..0>	6 12
I45	NAND_50S	NAND	F0CE0_L	6 12
I48	NAND_50S	NAND	F0CE1_L	6 12
I47	NAND_50S	NAND	F0CE2_L	6 12
I46	NAND_50S	NAND	F0CE3_L	6 12
I163	NAND_50S	NAND	F0CE4_L	6 12
I164	NAND_50S	NAND	F0CE5_L	6 12
I166	NAND_50S	NAND	F0CE6_L	6 12
I165	NAND_50S	NAND	F0CE7_L	6 12
I41	NAND_50S	NAND	F0CLE	6 12
I42	NAND_50S	NAND	F0ALE	6 12
I43	NAND_50S	NAND	F0RE_L	6 12
I44	NAND_50S	NAND	F0WE_L	6 12
I37	NAND_50S	NAND	F0WP_L	
I49	NAND_50S	NAND	F1AD<7..0>	6 12
I51	NAND_50S	NAND	F1CE0_L	6 12
I52	NAND_50S	NAND	F1CE1_L	6 12
I53	NAND_50S	NAND	F1CE2_L	6 12
I54	NAND_50S	NAND	F1CE3_L	6 12
I167	NAND_50S	NAND	F1CE4_L	6 12
I168	NAND_50S	NAND	F1CE5_L	6 12
I169	NAND_50S	NAND	F1CE6_L	6 12
I170	NAND_50S	NAND	F1CE7_L	6 12
I55	NAND_50S	NAND	F1CLE	6 12
I56	NAND_50S	NAND	F1ALE	6 12
I57	NAND_50S	NAND	F1RE_L	6 12
I58	NAND_50S	NAND	F1WE_L	6 12
I59	NAND_50S	NAND	F1WP_L	
I105	NAND_50S	NAND	F2AD<7..0>	
I104	NAND_50S	NAND	F2CE0_L	
I106	NAND_50S	NAND	F2CE1_L	
I108	NAND_50S	NAND	F2CE2_L	
I107	NAND_50S	NAND	F2CE3_L	
I109	NAND_50S	NAND	F2CLE	
I110	NAND_50S	NAND	F2ALE	
I111	NAND_50S	NAND	F2RE_L	
I113	NAND_50S	NAND	F2WE_L	
I112	NAND_50S	NAND	F2WP_L	
I114	NAND_50S	NAND	F3AD<7..0>	
I115	NAND_50S	NAND	F3CE0_L	
I116	NAND_50S	NAND	F3CE1_L	
I117	NAND_50S	NAND	F3CE2_L	
I118	NAND_50S	NAND	F3CE3_L	
I119	NAND_50S	NAND	F3CLE	
I120	NAND_50S	NAND	F3ALE	
I121	NAND_50S	NAND	F3RE_L	
I122	NAND_50S	NAND	F3WE_L	
I123	NAND_50S	NAND	F3WP_L	

JTAG

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
JTAG	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I16		JTAG	JTAG_AP_TCK	4 28
I15		JTAG	JTAG_AP_TMS	4 28
I14		JTAG	JTAG_AP_TDI	4 10
I13		JTAG	JTAG_AP_TDO	4 10
I20		JTAG	JTAG_AP_TRST_L	4 10

I2C

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2C_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2C	*	*	1.5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I1	I2C_50S	I2C	I2C1_SDA_1V8	5 25
I2	I2C_50S	I2C	I2C1_SCL_1V8	5 25
I3	I2C_50S	I2C	I2C0_SDA_1V8	5 10 19 35
I4	I2C_50S	I2C	I2C0_SCL_1V8	5 10 19 35
I61	I2C_50S	I2C	I2C2_SDA_3V0	5 25 26
I62	I2C_50S	I2C	I2C2_SCL_3V0	5 25 26
I98	I2C_50S	I2C	ISP_AP_0_SCL	7 25
I99	I2C_50S	I2C	ISP_AP_0_SDA	7 25
I100	I2C_50S	I2C	ISP_AP_1_SCL	7 26
I101	I2C_50S	I2C	ISP_AP_1_SDA	7 26
I102	I2C_50S	I2C	I2C2_SCL_3V0_ALS	25 26
I103	I2C_50S	I2C	I2C2_SDA_3V0_ALS	25 26
I124	I2C_50S	I2C	ISP_CAM_1_SCL	25 26
I125	I2C_50S	I2C	ISP_CAM_1_SDA	25 26

XTAL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CRYSTAL	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I92		CRYSTAL	XTAL_24M_I	4
I90		CRYSTAL	XTAL_24M_O	4
I93		CRYSTAL	24M_O	4

VREF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
VREF	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I136		VREF	PPVREF_DDR0_CA	8
I137		VREF	PPVREF_DDR0_DQ	8
I139		VREF	PPVREF_DDR1_CA	8
I138		VREF	PPVREF_DDR1_DQ	8

USB

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	5:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I5	USB_90D	USB	USB_D_P	4 28
I6	USB_90D	USB	USB_D_N	4 28
I7	USB_90D	USB	USB_PT_DK_CON_D_P	28 29
I8	USB_90D	USB	USB_PT_DK_CON_D_N	28 29
I82	USB_90D	USB	USB_BB_D_P	11 31
I83	USB_90D	USB	USB_BB_D_N	11 31
I84	USB_90D	USB	USB_FS_D_P	4 11
I85	USB_90D	USB	USB_FS_D_N	4 11
I128	USB_90D	USB	USB_FS_N_ACC_TX	11 28
I129	USB_90D	USB	USB_FS_P_ACC_RX	11 28
I171	USB_90D	USB	ACC_PT_DK_CON_TX	28 29
I172	USB_90D	USB	ACC_PT_DK_CON_RX	28 29

I2S

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
I2S_90S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
I2S	*	*	3:1_SPACING
I2S	I2S	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I140	I2S_50S	I2S	I2S_AP_0_BCLK	5 19
I143	I2S_50S	I2S	I2S_AP_0_LRCK	5 19
I142	I2S_50S	I2S	I2S_AP_0_DIN	5 19
I141	I2S_50S	I2S	I2S_AP_0_DOUT	5 19
I159	I2S_50S	I2S	L63_ASP_SDOUT	19
I144	I2S_50S	I2S	I2S_AP_2_BCLK	5 19 30
I148	I2S_50S	I2S	I2S_AP_2_LRCK	5 19 30
I147	I2S_50S	I2S	I2S_AP_2_DIN	5 19 30
I146	I2S_50S	I2S	I2S_AP_2_DOUT	5 19 30
I160	I2S_50S	I2S	L63_VSP_SDOUT	19
I145	I2S_50S	I2S	I2S_AP_3_BCLK	5 19
I149	I2S_50S	I2S	I2S_AP_3_LRCK	5 19
I150	I2S_50S	I2S	I2S_AP_3_DIN	5 19
I151	I2S_50S	I2S	I2S_AP_3_DOUT	5 19
I161	I2S_50S	I2S	L63_XSP_SDOUT	19

DWI

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DWI	*	*	2:1_SPACING

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	NET	PAGES
I152		DWI	DWI_AP_CLK	5 35
I153		DWI	DWI_AP_DI	5 35
I156		DWI	DWI_AP_DO	5 35

SYNC_MASTER=MIKE SYNC_DATE=N/A

PAGE TITLE: CONSTRAINTS: ASSIGNMENTS

Apple Inc.

DRAWING NUMBER: 051-8962 SIZE: D

REVISION: A.0.0

BRANCH

ANALOG VIDEO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
VID_50S	*	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ANALOG_VIDEO	*	*	5:1_SPACING
ANALOG_VIDEO	ANALOG_VIDEO	*	3:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I213	VID_50S	ANALOG_VIDEO	DAC_AP_OUT1 7 11
I214	VID_50S	ANALOG_VIDEO	DAC_AP_OUT2 7 11
I215	VID_50S	ANALOG_VIDEO	DAC_AP_OUT3 7 11
I232	VID_50S	ANALOG_VIDEO	BUF_C_Y 11
I233	VID_50S	ANALOG_VIDEO	BUF_CVBS_PB 11
I234	VID_50S	ANALOG_VIDEO	BUF_Y_PR 11
I219	VID_50S	ANALOG_VIDEO	VIDEO_EMI_CVBS_PB 10 11 28
I220	VID_50S	ANALOG_VIDEO	VIDEO_EMI_C_Y 10 11 28
I221	VID_50S	ANALOG_VIDEO	VIDEO_EMI_Y_PR 10 11 28
I222	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_CVBS_PB 28 29
I223	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_C_Y 28 29
I224	VID_50S	ANALOG_VIDEO	VIDEO_PT_DK_CON_Y_PR 28 29

LVDS

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I146	LVDS_100D	LVDS	LVDS_DATA_P<2..0> 14 16
I147	LVDS_100D	LVDS	LVDS_DATA_N<2..0> 14 16
I245	LVDS_100D	LVDS	LVDS_DATA_CONN_P<2..0> 16
I246	LVDS_100D	LVDS	LVDS_DATA_CONN_N<2..0> 16
I145	LVDS_100D	LVDS	LVDS_CLK_P 14 16
I148	LVDS_100D	LVDS	LVDS_CLK_N 14 16
I244	LVDS_100D	LVDS	LVDS_CLK_CONN_P 16
I243	LVDS_100D	LVDS	LVDS_CLK_CONN_N 16

DISPLAYPORT

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
DP_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DP	*	*	5:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I247	DP_100D	DP	DP_AP_TX_P<0> 7 10 13
I249	DP_100D	DP	DP_AP_TX_N<0> 7 10 13
I248	DP_100D	DP	DP_AP_TX_P<1> 7 10 13
I250	DP_100D	DP	DP_AP_TX_N<1> 7 10 13
I251	DP_100D	DP	DP_AP_AUX_P 7 13
I252	DP_100D	DP	DP_AP_AUX_N 7 13
I273	DP_100D	DP	DP_EMI_TX_P<0> 13 28
I274	DP_100D	DP	DP_EMI_TX_N<0> 13 28
I275	DP_100D	DP	DP_EMI_TX_P<1> 13 28
I276	DP_100D	DP	DP_EMI_TX_N<1> 13 28
I277	DP_100D	DP	DP_EMI_AUX_P 13 28
I278	DP_100D	DP	DP_EMI_AUX_N 13 28
I827	DP_100D	DP	DP_PT_DK_CON_TX_P<0> 28 29
I829	DP_100D	DP	DP_PT_DK_CON_TX_N<0> 28 29
I828	DP_100D	DP	DP_PT_DK_CON_TX_P<1> 28 29
I830	DP_100D	DP	DP_PT_DK_CON_TX_N<1> 28 29
I831	DP_100D	DP	DP_PT_DK_CON_AUX_P 28 29
I832	DP_100D	DP	DP_PT_DK_CON_AUX_N 28 29

MIPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MIPI_100D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I91	MIPI_100D	MIPI	MIPID_AP_DATA_P<0> 7 14
I92	MIPI_100D	MIPI	MIPID_AP_DATA_N<0> 7 14
I93	MIPI_100D	MIPI	MIPID_AP_DATA_P<1> 7 14
I94	MIPI_100D	MIPI	MIPID_AP_DATA_N<1> 7 14
I95	MIPI_100D	MIPI	MIPID_AP_DATA_P<2> 7 14
I96	MIPI_100D	MIPI	MIPID_AP_DATA_N<2> 7 14
I97	MIPI_100D	MIPI	MIPID_AP_DATA_P<3> 7 14
I274	MIPI_100D	MIPI	MIPID_AP_DATA_N<3> 7 14
I97	MIPI_100D	MIPI	MIPID_AP_CLK_P 7 14
I98	MIPI_100D	MIPI	MIPID_AP_CLK_N 7 14
I314	MIPI_100D	MIPI	MIPI0C_AP_DATA_P<0> 7 27
I317	MIPI_100D	MIPI	MIPI0C_AP_DATA_N<0> 7 27
I315	MIPI_100D	MIPI	MIPI0C_AP_CLK_P 7 27
I316	MIPI_100D	MIPI	MIPI0C_AP_CLK_N 7 27
I834	MIPI_100D	MIPI	MIPI0C_CAM_DATA_P<0> 25 27
I835	MIPI_100D	MIPI	MIPI0C_CAM_DATA_N<0> 25 27
I844	MIPI_100D	MIPI	MIPI0C_CAM_CLK_P 25 27
I847	MIPI_100D	MIPI	MIPI0C_CAM_CLK_N 25 27
I834	MIPI_100D	MIPI	MIPI1C_AP_DATA_P<0> 7 26
I840	MIPI_100D	MIPI	MIPI1C_AP_DATA_N<0> 7 26
I845	MIPI_100D	MIPI	MIPI1C_AP_CLK_P 7 26
I848	MIPI_100D	MIPI	MIPI1C_AP_CLK_N 7 26
I836	MIPI_100D	MIPI	MIPI1C_CAM_DATA_P<0> 25 26
I839	MIPI_100D	MIPI	MIPI1C_CAM_DATA_N<0> 25 26
I842	MIPI_100D	MIPI	MIPI1C_CAM_CLK_P 25 26
I836	MIPI_100D	MIPI	MIPI1C_CAM_CLK_N 25 26

AUDIO/SPEAKER

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
AUDIO	*	1:1_DIFFPAIR
SPEAKER	*	SPEAKER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
AUDIO	*	*	3:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I587	AUDIO	AUDIO	LEFT_CH_OUT_P 19 20
I588	AUDIO	AUDIO	LEFT_CH_OUT_REF 19 20
I589	AUDIO	AUDIO	LEFT_CH_P 20
I590	AUDIO	AUDIO	SSM2375_L_IN_P 20
I591	AUDIO	AUDIO	SSM2375_L_IN_N 20
I592	AUDIO	AUDIO	RIGHT_CH_OUT_P 19 20
I593	AUDIO	AUDIO	RIGHT_CH_OUT_REF 19 20
I594	AUDIO	AUDIO	RIGHT_CH_P 20
I595	AUDIO	AUDIO	SSM2375_R_IN_P 20
I596	AUDIO	AUDIO	SSM2375_R_IN_N 20
I597	AUDIO	AUDIO	EXT_MIC_P 19 23
I598	AUDIO	AUDIO	EXT_MIC_REF 19 23

SDIO

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SDIO_50S	*	50_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SDIO	*	*	2:1_SPACING
SDIO_CLK	*	*	4:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I404	SDIO_50S	SDIO_CLK	SDIO_WL_CLK 5 30
I405	SDIO_50S	SDIO_CLK	SDIO_WL_CLK_R
I403	SDIO_50S	SDIO	SDIO_WL_CMD 5 30
I400	SDIO_50S	SDIO	SDIO_WL_DATA<3..0> 5 30

SPI

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SPI_50S	*	45_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SPI	*	*	2:1_SPACING

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING	
I396	SPI_50S	SPI	SPI_GRAPE_MISO 5 17
I395	SPI_50S	SPI	SPI_GRAPE_MOSI 5 17
I394	SPI_50S	SPI	SPI_GRAPE_SCLK 5 17
I392	SPI_50S	SPI	SPI_GRAPE_CS_L 5 17
I364	SPI_50S	SPI	SPI_IPC_MISO 5 31
I366	SPI_50S	SPI	SPI_IPC_MOSI 5 31
I365	SPI_50S	SPI	SPI_IPC_SCLK 5 31
I367	SPI_50S	SPI	SPI_IPC_MRDY 5 31

SYNC_MASTER=MIKE SYNC_DATE=N/A

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MLB CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,BOTTOM	NO_TYPE,BGA,BGA06-06	MM	15.2

PHYSICAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	30 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT

SINGLE-ENDED PHYSICAL RULES
45 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	ISL2,ISL3,ISL8,ISL9	Y	0.055 MM	0.055 MM	3.0 MM		
45_OHM_SE	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	3.0 MM		
45_OHM_SE	*	N	0.060 MM	0.060 MM	3.0 MM		

50 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM	3.0 MM		
50_OHM_SE	*	N	0.050 MM	0.050 MM	3.0 MM		

50 OHMS - CLEAR ON LAYER 2 AND 5

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE_RF	TOP	Y	0.240 MM	0.240 MM	3.0 MM		
50_OHM_SE	ISL4	Y	0.060 MM	0.060 MM	3.0 MM		

50 OHMS - CLEAR ON TOP AND BOTTOM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	ISL2,ISL9	Y	0.090 MM	0.090 MM	3.0 MM		

DIFFERENTIAL PAIR PHYSICAL RULES
100 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	TOP,BOTTOM	Y	0.076 MM	0.076 MM		0.210 MM	0.210 MM
100_OHM_DIFF	N	Y	0.057 MM	0.057 MM	=STANDARD	0.300 MM	0.300 MM

90 OHMS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	TOP,BOTTOM	Y	0.095 MM	0.095 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL3,ISL8,ISL9	Y	0.054 MM	0.054 MM	=STANDARD	0.200 MM	0.100 MM
90_OHM_DIFF	ISL4,ISL5,ISL6,ISL7	Y	0.060 MM	0.060 MM	=STANDARD	0.200 MM	0.100 MM

AUDIO PHYSICAL RULES

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.08 MM	0.08 MM
SPEAKER	*	Y	0.3 MM	0.19MM	10 MM	0.08 MM	0.08 MM

BGA AREA PHYSICAL RULES

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	BGA	BGA_PHY

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
BGA_PHY	*	Y	0.060 MM	0.060 MM	=STANDARD	0.076 MM	0.075 MM

SPACING CONSTRAINTS

DEFAULT/BGA SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.08 MM	?
STANDARD	*	=DEFAULT	?
BGA_SPA	*	=DEFAULT	?

REGULAR SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.060 MM	?
0P08_SPACING	*	0.080 MM	?
1.5:1_SPACING	*	0.090 MM	?
2:1_SPACING	*	0.120 MM	?
2.5:1_SPACING	*	0.150 MM	?
3:1_SPACING	*	0.180 MM	?
4:1_SPACING	*	0.240 MM	?
5:1_SPACING	*	0.300 MM	?
0P5MM_SPACING	*	0.5 MM	?
0P64MM_SPACING	*	0.64 MM	?

*NOTE: ASSUMING 0.060MM DIELECTRIC THICKNESS

POWER/GND SPACING RULES

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PWR_P1SPACING	*	0.1 MM	900
GND_P1SPACING	*	0.1 MM	950
SWITCHNODE	*	0.5 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_SPA
CLK	*	BGA	BGA_SPA
PWR	*	*	PWR_P1SPACING
GND	*	*	GND_P1SPACING
SWITCHNODE	*	*	SWITCHNODE
ANLG	*	*	3:1_SPACING

NOTES:

0.075 MM ~ 3 MIL
0.089 MM ~ 3.5 MIL
0.102 MM ~ 4 MIL
0.114 MM ~ 4.5 MIL
0.125 MM ~ 5 MIL
0.140 MM ~ 5.5 MIL
0.15 MM ~ 6 MIL
0.18 MM ~ 7 MIL
0.2 MM ~ 8 MIL
0.25 MM ~ 10 MIL
0.3 MM ~ 12 MIL
0.33 MM ~ 13 MIL
0.4 MM ~ 16 MIL
1.0 MM = 39.37 MIL

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